ME3 Block Diagram

Project code : 91.4X601.001
PCB P/N :
Revision :

Intel CPU
Meron 2M/4M SV
FSB:667 or 800 MHz
4,5,6

Host BUS
533/667MHz

G792 22

CLK GEN
REALTEK RTM875 3

DDRII Slot 0 13,14
DDRII Slot 1 13,14

DDRII 667 Channel A
DDRII 667 Channel B

Crestline-GM/GML
AGTL+ CPU I/F DDR I/F
INTEGRATED GRAHPICS
LVDS, CRT I/F
7,8,9,10,11,12

PCIE x 16

nVIDIA
NB8M-GS
44,45,46

TV OUT 15
CRT 15
LCD 16
HDMI 17
EEPROM 46

DMI I/F
100MHz

GDDR3
Graphics RAM
256-Mbit
47,48

Power Switch G577 23
New card 23
PCI-E x 1

Mini Card_2 Robson 23
Mini Card_1 802.11a/b/g/n 23
PCI-E x 2

RJ45 CONN 25
10/100 Controller Realtek RTL8101E 24
PCI-E x 1

INTEL
ICH8-M
10 USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
ATA 66/100
ACPI 1.1
LPC I/F
PCI/PCI BRIDGE
18,19,20,21

Mic In
Line In
Codec ALC662 34
AZALIA

INT.SPKR
AMP G1432 35
Line Out (SPDIF)
AMP G1412 35

RJ11
MODEM MDC Card 28
AZALIA

INT. MIC Array Digital
HDMI (SPDIF)
Codec ALC268 28

E-SATA CONN 28
E-SATA SIL3531 29

SATA
SATA
PATA

HDD 30
CDROM 30

27MHz
32.768KHz

Finger print 26
Camera 26
RF 26
or
Blue tooth 26
USB X 4 28
Realtek RTL5158 27
MS/MS Pro/xD/ MMC/SD 4 in 1 27

USB 2.0

LPC BUS

LPC DEBUG CONN. 32

KBC Winbond WPC8763 31
32.768KHz
SPI

TPM SLB9635TT 32
32.768KHz

CAPACITY BUTTON 33
Touch Pad 33
INT. KB 33
Flash Rom W25X80-VSS 32

SYSTEM DC/DC
TPS51120

INPUTS	OUTPUTS
DCBATOUT	5V_S3 3V_S5

SYSTEM DC/DC
MAX8743

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3

SYSTEM DC/DC
FAN5234

INPUTS	OUTPUTS
DCBATOUT	VGA_CORE_S0 11A

MAXIM CHARGER
MAX8725

INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA

CPU DC/DC
MAX8736ETL

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 44A

PCB LAYER

L1: Signal 1
L2: GND
L3: Signal 2
L4: Signal 3
L5: GND
L6: VCC
L7: Signal 4
L8: Signal 5
L9: GND
L10: Signal 5

Prepare by Steven CF Chou

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram
Size: A3 | Document Number: ME3-Discrete | Rev: SA
Date: Monday, July 30, 2007 | Sheet 1 of 51

INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIE Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCL1_5 VRM Enable/Disable.Always sampled.	Enables integrated VccSus1_05,VccSus1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIE LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overidden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap

ICH_RSVD	TP3	AZ_DOUT_ICH	Description
0	0	0	RSVD
0	0	1	Enter XOR Chain
1	0	0	Normal Operation(default)
1	0	1	Set PCIE port cofig bit1

A16 swap override strap

PCI_GNT#3: low = A16 swap override enable; high = default

BOOT BIOS Strap

PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

integrated VccSus1_05,VccSus1_5,VccCL1_5

SM_INTVRMEN	High=Enable	Low=Disable

integrated VccLan1_05VccCL1_05

LAN100_SLP	High=Enable	Low=Disable

DEFAULE HIGH

No Reboot Strap

SPKR: LOW = Defaule; High=No Reboot

8.2K PULL HIGH

U45 : 71.0NB8M.00U (VGA)
U35: 71.00662.00G (Audio)
U28: 71.08763.B0G (KBC)
U74: 71.08101.B0G (LAN)
U26: 71.ICH8M.C0U (SB)
U18: 71.PM96S.A0U (NB)
TV1: 22.10021.H21
Hole,Spring
HDMI1: 22.10296.011

INTEL CRESTLINE STRAP PIN

CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	DMI X 4 ★
CFG 8 Low Power PCI Express	Normal★	Low Power mode
CFG 9 PCI Express Graphics Lane Reversal	Lane Reversal	Normal Mode(Lanes number in order)★
CFG 16 FSB Dynamic ODT	Disabled	Enabled ★
CFG 19 DMI Lane Reversed	Normal Operation ★	Reserved Lane
CFG 20 Concurrent SDVO/PCIE	Only PCIE or SDVO is operation★	PCIE and SDVO are operation simultaneous
SDVO_CTRL_DATA SDVO Present	NO SDVO Card Present ★	SDVO Card Present

CFG 12 CFG 13	XOR/ALL-Z
LL(00)	Reserved
LH(01)	XOR Mode Enabled
HL(10)	All Z Mode Enabled
HH(11)	Normal Operation

MB: 07230
LED: 07537
FP: 07546
Audio: 07545
USB: 07547

INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	TBD

<Core Design>

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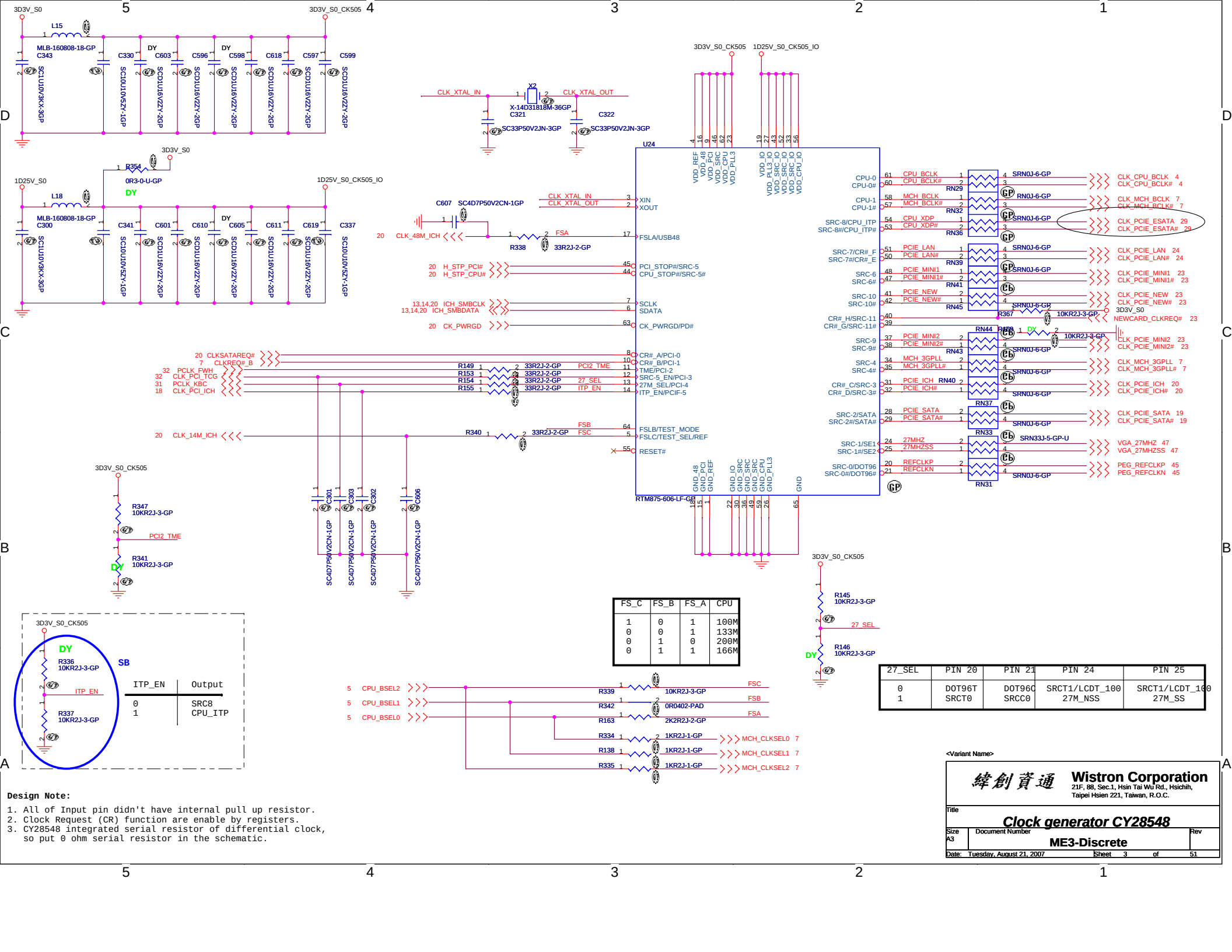
Title: Table of Content

Size: A3 | Document Number: ME3-Discrete | Rev:

Date: Friday, September 14, 2007 | Sheet 2 of 51



Design Note:

1. All of Input pin didn't have internal pull up resistor.
2. Clock Request (CR) function are enable by registers.
3. CY28548 integrated serial resistor of differential clock, so put 0 ohm serial resistor in the schematic.

<Variant Name>

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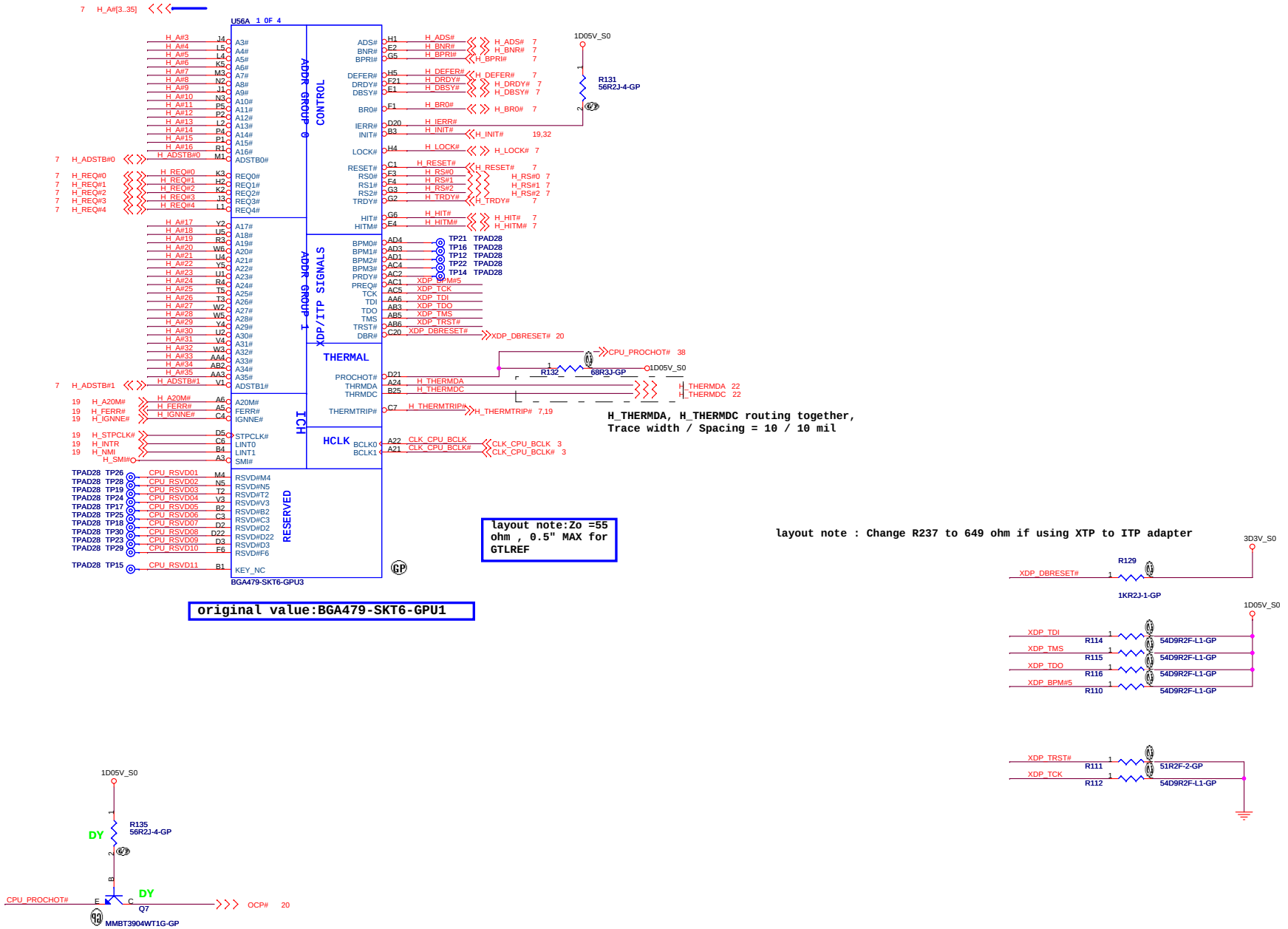
Title: ***Clock generator CY28548***

Size	Document Number	Rev
A3	ME3-Discrete	

Date: Tuesday, August 21, 2007 Sheet 3 of 51



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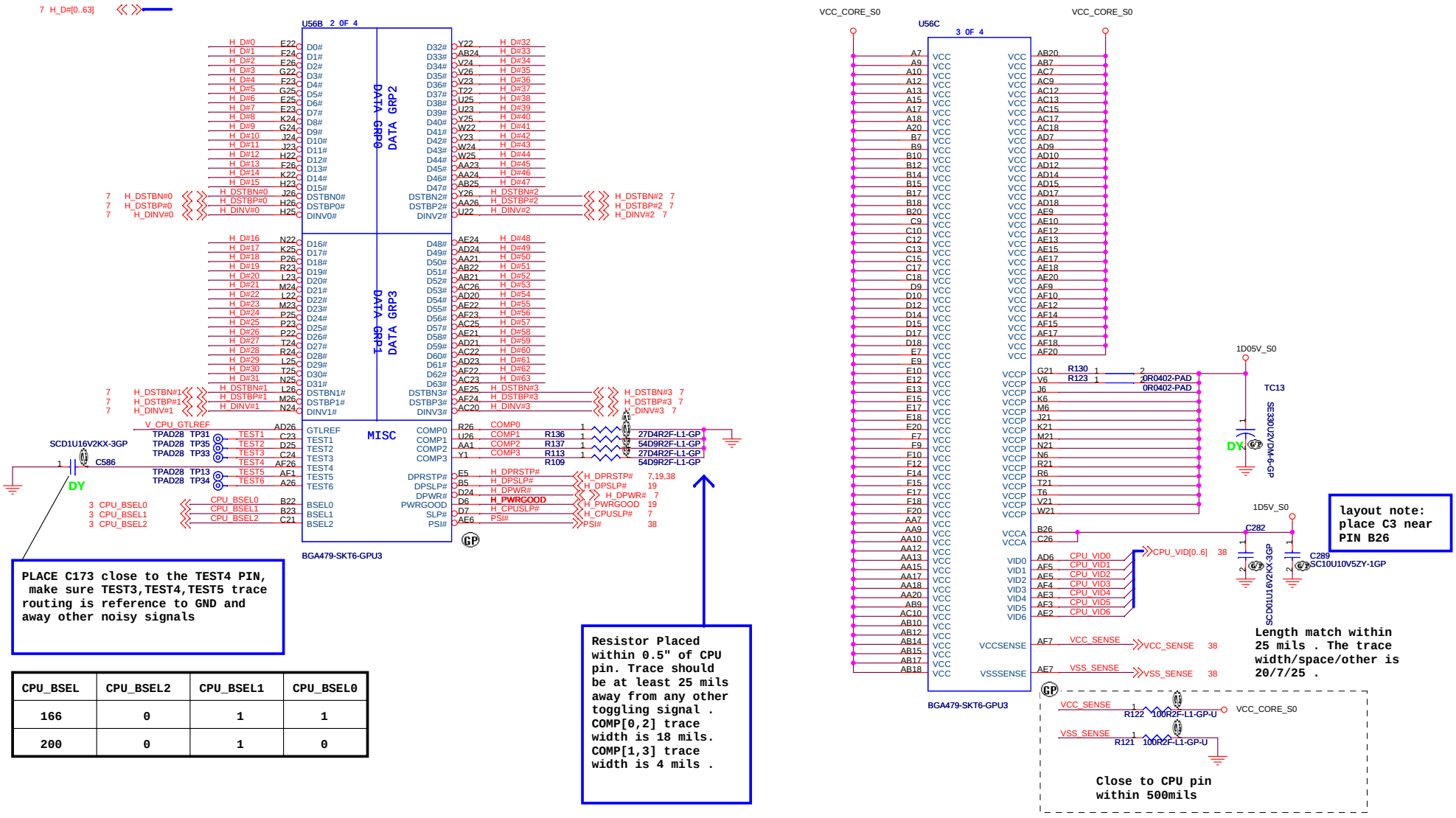
Title: Meron(1/3)-AGTL+/XDP

Size: Custom | Document Number: ME3-Discrete | Rev:

Date: Wednesday, August 15, 2007 | Sheet 4 of 51



CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

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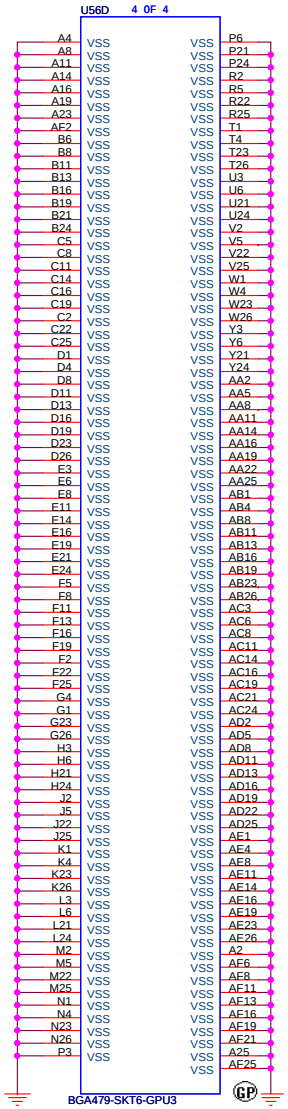
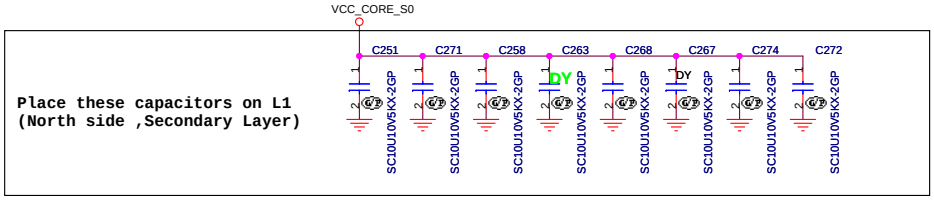
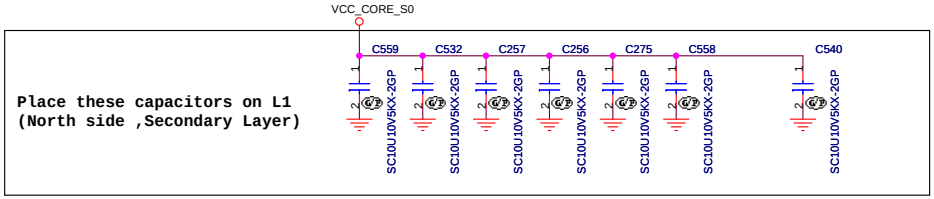
Title: Meron(2/3)-AGTL+/PWR

Size: A3 | Document Number: ME3-Discrete | Rev:

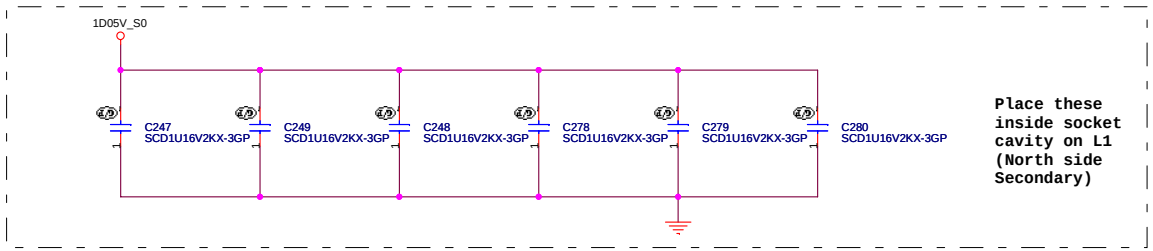
Date: Wednesday, August 15, 2007 | Sheet 5 of 51







Mid Frequencd Decoupling



<Core Design>

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Title: ***Meron(3/3)-GND&Bypass***

Size: A3 | Document Number: ME3-Discrete | Rev:

Date: Monday, July 30, 2007 | Sheet 6 of 51

FOR Calero: 80.6 ohm
Crestline: 20 ohm

CFG[17:3] have internal pull up
CFG[19:18] have internal pull down

From Astro demo schematic

layout note :
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces

Layout Note :
H_RCOMP / H_VREF / H_SWNG
trace width and spacing is 10/20

Layout Note :
Place C151 within 100 mils of NB

Layout Note :
Place C153 near pin B3 of NB

<Core Design>

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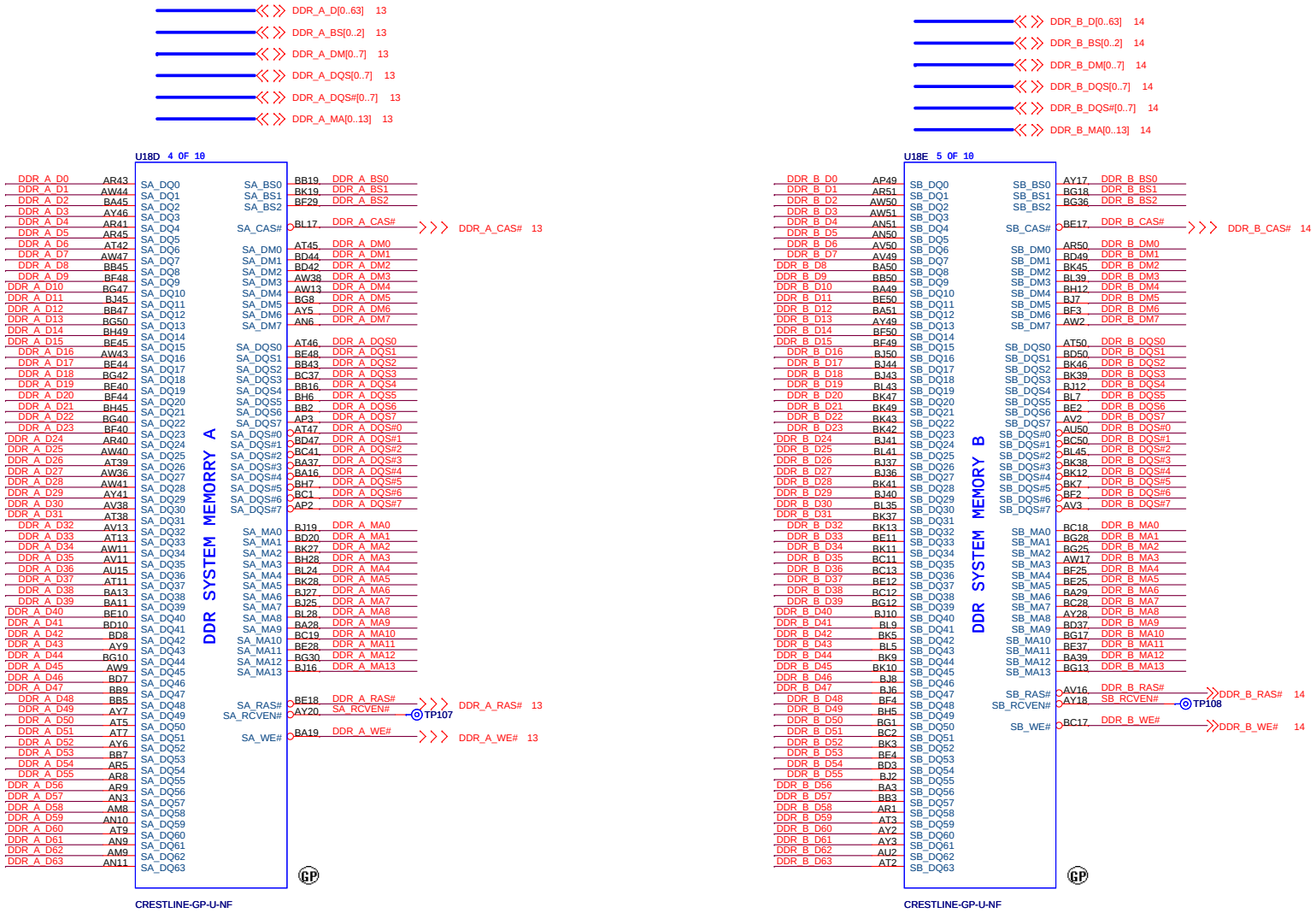
Title
CRESTLINE(1/6)-AGTL+/DMI/DDR2

Size: Custom | Document Number: ME3-Discrete | Rev:
Date: Wednesday, August 15, 2007 | Sheet 7 of 51



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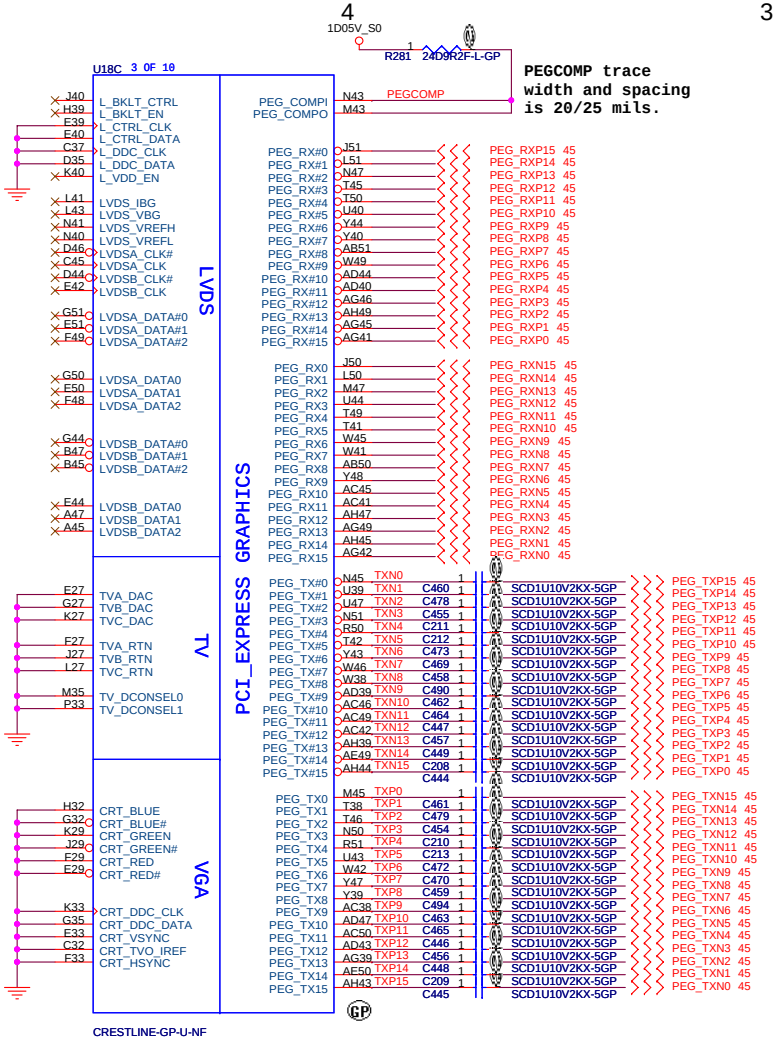
Title
CRESTLINE(2/6)-DDR2 A/B CH

Size	Document Number	Rev
A3	ME3-Discrete	

Date: Wednesday, August 15, 2007 Sheet 8 of 51



Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default)*
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disable 1 = Enable *
CFG[18:17]	Reversed
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19(DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse lane
CFG20(PCIE/SDVO consurrent)	0 = Only PCIE or SDVO is operational * 1 = PCIE/SDVO are operating simu.

<Core Design>

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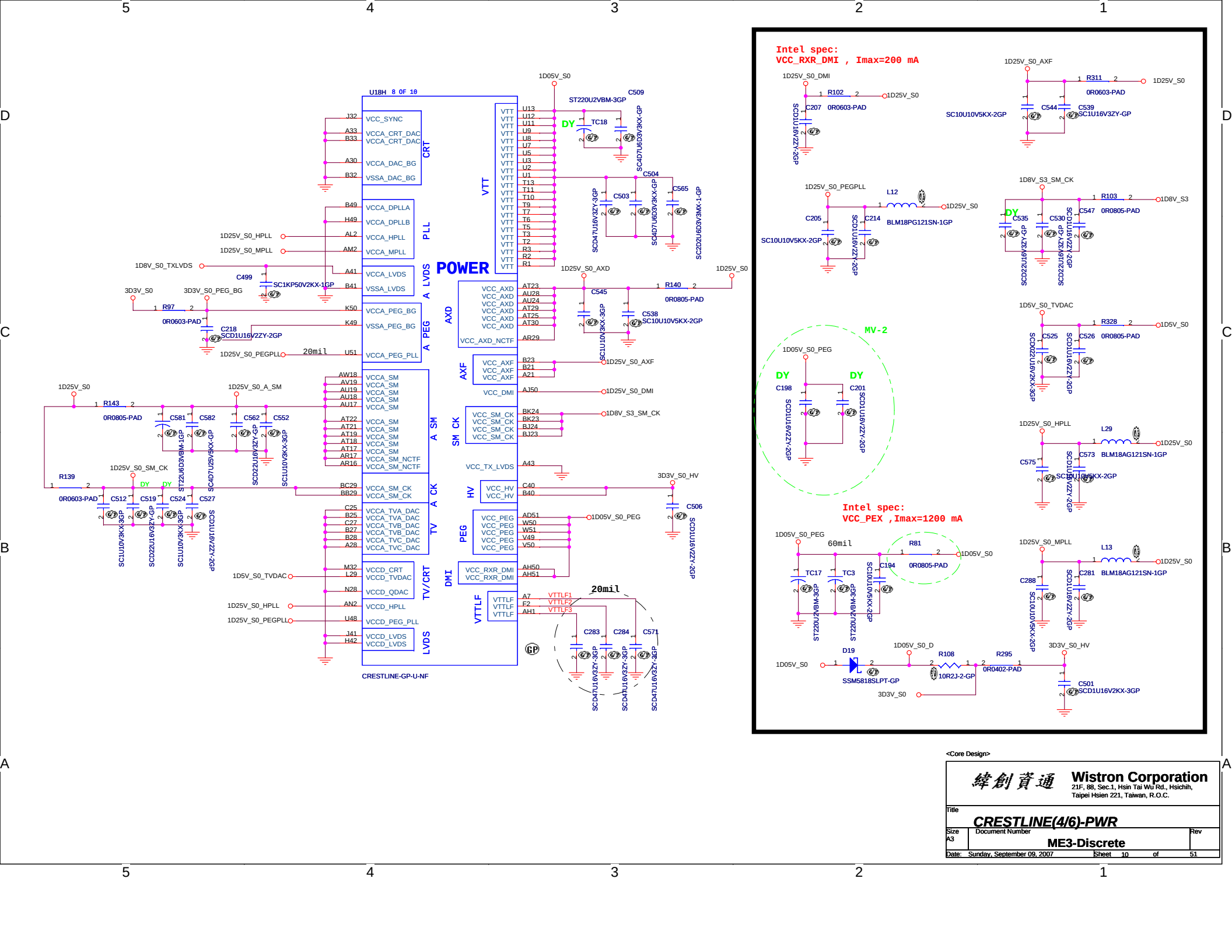
Title: CRESTLINE(3/6)-VGA/LVDS/TV

Size	Document Number	Rev
A3	ME3-Discrete	

Date: Wednesday, August 15, 2007 Sheet 9 of 51


U18H 8 OF 10
POWER
CRESTLINE-GP-U-NF
Intel spec:
VCC_RXR_DMI , Imax=200 mA
Intel spec:
VCC_PEX ,Imax=1200 mA
MV-2
20mil
60mil
<Core Design>
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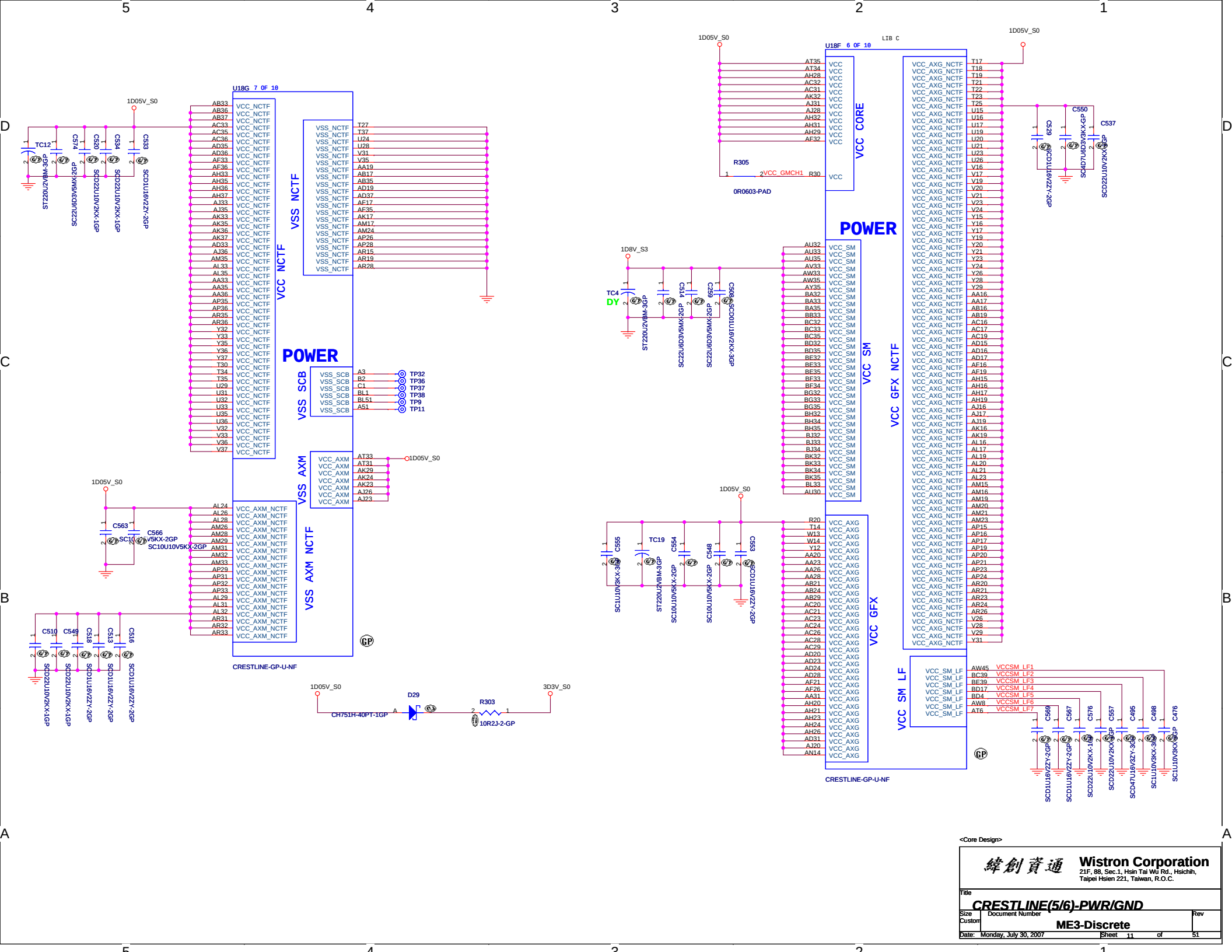
Title
CRESTLINE(4/6)-PWR
Size A3
Document Number
ME3-Discrete
Rev
Date: Sunday, September 09, 2007
Sheet 10 of 51


U18G 7 OF 10
VCC_NCTF
VSS_NCTF
VCC NCTF
VSS NCTF
POWER
VSS SCB
VSS_SCB
VSS AXM
VCC_AXM
VSS AXM NCTF
VCC_AXM_NCTF
CRESTLINE-GP-U-NF
1D05V_S0
U18F 6 OF 10
LIB C
VCC CORE
VCC
R305
0R0603-PAD
VCC_GMCH1
1D8V_S3
VCC SM
VCC_SM
VCC GFX NCTF
VCC_AXG_NCTF
VCC GFX
VCC_AXG
VCC SM LF
VCC_SM_LF
VCCSM_LF1
VCCSM_LF2
VCCSM_LF3
VCCSM_LF4
VCCSM_LF5
VCCSM_LF6
VCCSM_LF7
TP32
TP36
TP37
TP38
TP9
TP11
D29
CH751H-40PT-1GP
R303
10R2J-2-GP
3D3V_S0
TC12
TC4
TC19
C574
C520
C534
C533
C563
C566
C510
C549
C518
C513
C516
C554
C555
C548
C539
C514
C529
C550
C537
C569
C567
C576
C557
C495
C498
C476
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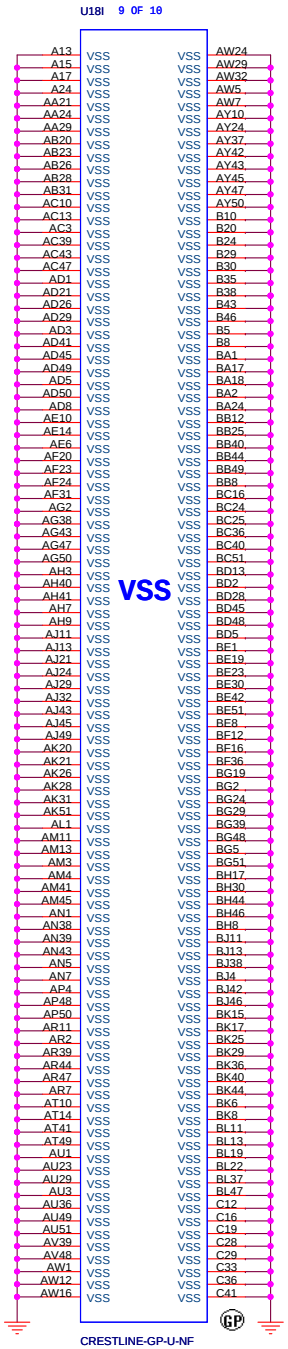
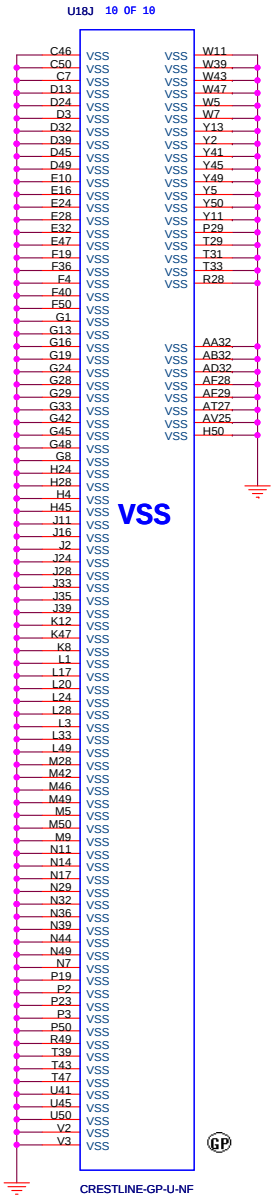
Title
CRESTLINE(5/6)-PWR/GND
Size
Custom
Document Number
ME3-Discrete
Rev
Date: Monday, July 30, 2007
Sheet 11 of 51





<Core Design>

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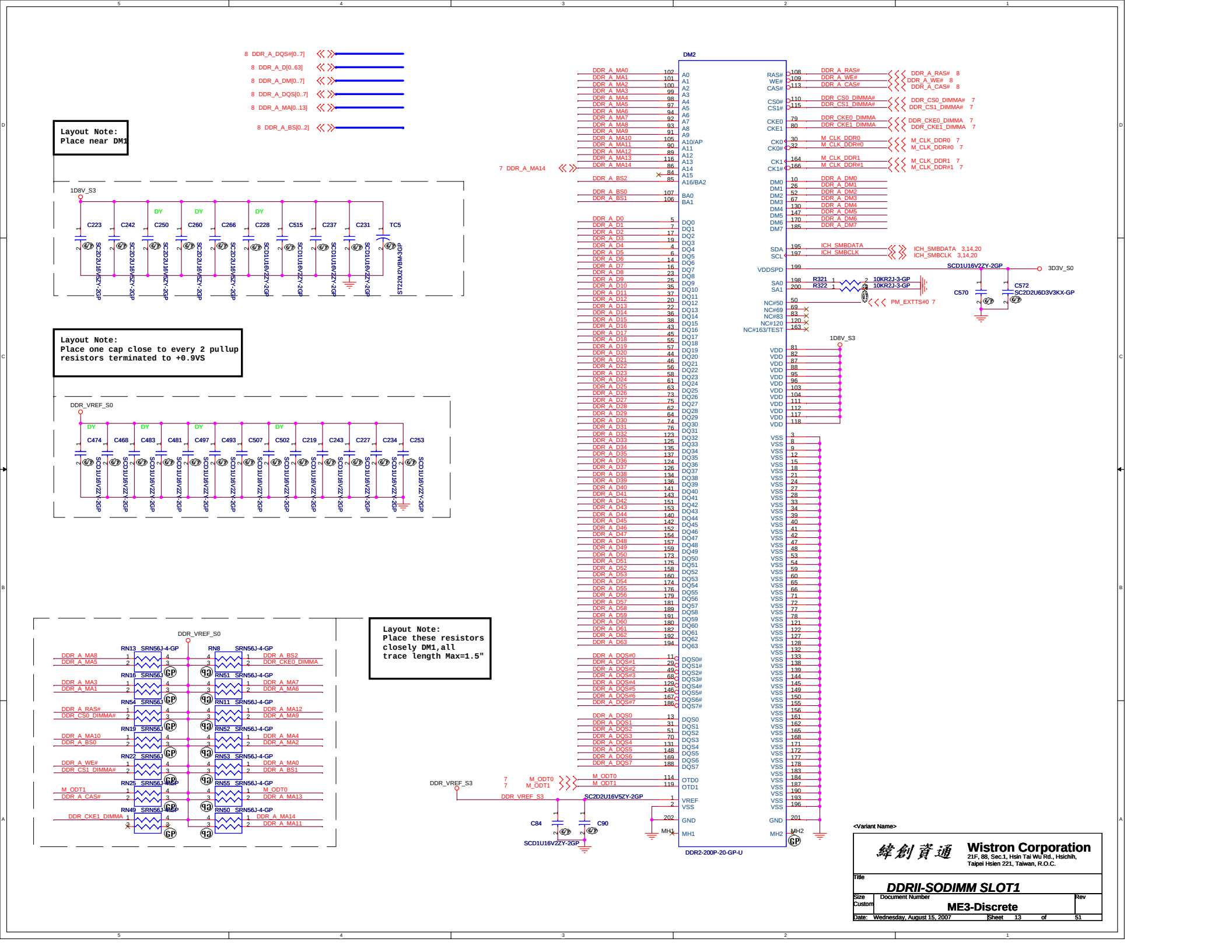
Title: CRESTLINE(6/6)-PWR/GND

Size: A3 | Document Number: ME3-Discrete | Rev:

Date: Monday, July 30, 2007 | Sheet 12 of 51


8 DDR_A_DQS#[0..7]
8 DDR_A_D[0..63]
8 DDR_A_DM[0..7]
8 DDR_A_DQS[0..7]
8 DDR_A_MA[0..13]
8 DDR_A_BS[0..2]
Layout Note:
Place near DM1
1D8V_S3
C223
C242
C250
C260
C266
C228
C515
C237
C231
TC5
SC2D2U16VZY-2GP
SC1U16V2ZY-2GP
ST220U2VBM-3GP
DY
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS
DDR_VREF_S0
C474
C468
C483
C481
C497
C493
C507
C502
C219
C243
C227
C234
C253
SC1U16V2ZY-2GP
Layout Note:
Place these resistors
closely DM1,all
trace length Max=1.5"
DDR_VREF_S0
RN13 SRN56J-4-GP
RN8 SRN56J-4-GP
RN16 SRN56J-GP
RN51 SRN56J-4-GP
RN54 SRN56J-GP
RN11 SRN56J-4-GP
RN19 SRN56J-GP
RN52 SRN56J-4-GP
RN22 SRN56J-GP
RN53 SRN56J-4-GP
RN25 SRN56J-GP
RN55 SRN56J-4-GP
RN49 SRN56J-GP
RN50 SRN56J-4-GP
DDR_A_MA8
DDR_A_MA5
DDR_A_BS2
DDR_CKE0_DIMMA
DDR_A_MA3
DDR_A_MA1
DDR_A_MA7
DDR_A_MA6
DDR_A_RAS#
DDR_CS0_DIMMA#
DDR_A_MA12
DDR_A_MA9
DDR_A_MA10
DDR_A_BS0
DDR_A_MA4
DDR_A_MA2
DDR_A_WE#
DDR_CS1_DIMMA#
DDR_A_MA0
DDR_A_BS1
M_ODT1
DDR_A_CAS#
M_ODT0
DDR_A_MA13
DDR_CKE1_DIMMA
DDR_A_MA14
DDR_A_MA11
DM2
DDR_A_MA0
DDR_A_MA1
DDR_A_MA2
DDR_A_MA3
DDR_A_MA4
DDR_A_MA5
DDR_A_MA6
DDR_A_MA7
DDR_A_MA8
DDR_A_MA9
DDR_A_MA10
DDR_A_MA11
DDR_A_MA12
DDR_A_MA13
DDR_A_MA14
DDR_A_BS2
DDR_A_BS0
DDR_A_BS1
DDR_A_D0
DDR_A_D1
DDR_A_D2
DDR_A_D3
DDR_A_D4
DDR_A_D5
DDR_A_D6
DDR_A_D7
DDR_A_D8
DDR_A_D9
DDR_A_D10
DDR_A_D11
DDR_A_D12
DDR_A_D13
DDR_A_D14
DDR_A_D15
DDR_A_D16
DDR_A_D17
DDR_A_D18
DDR_A_D19
DDR_A_D20
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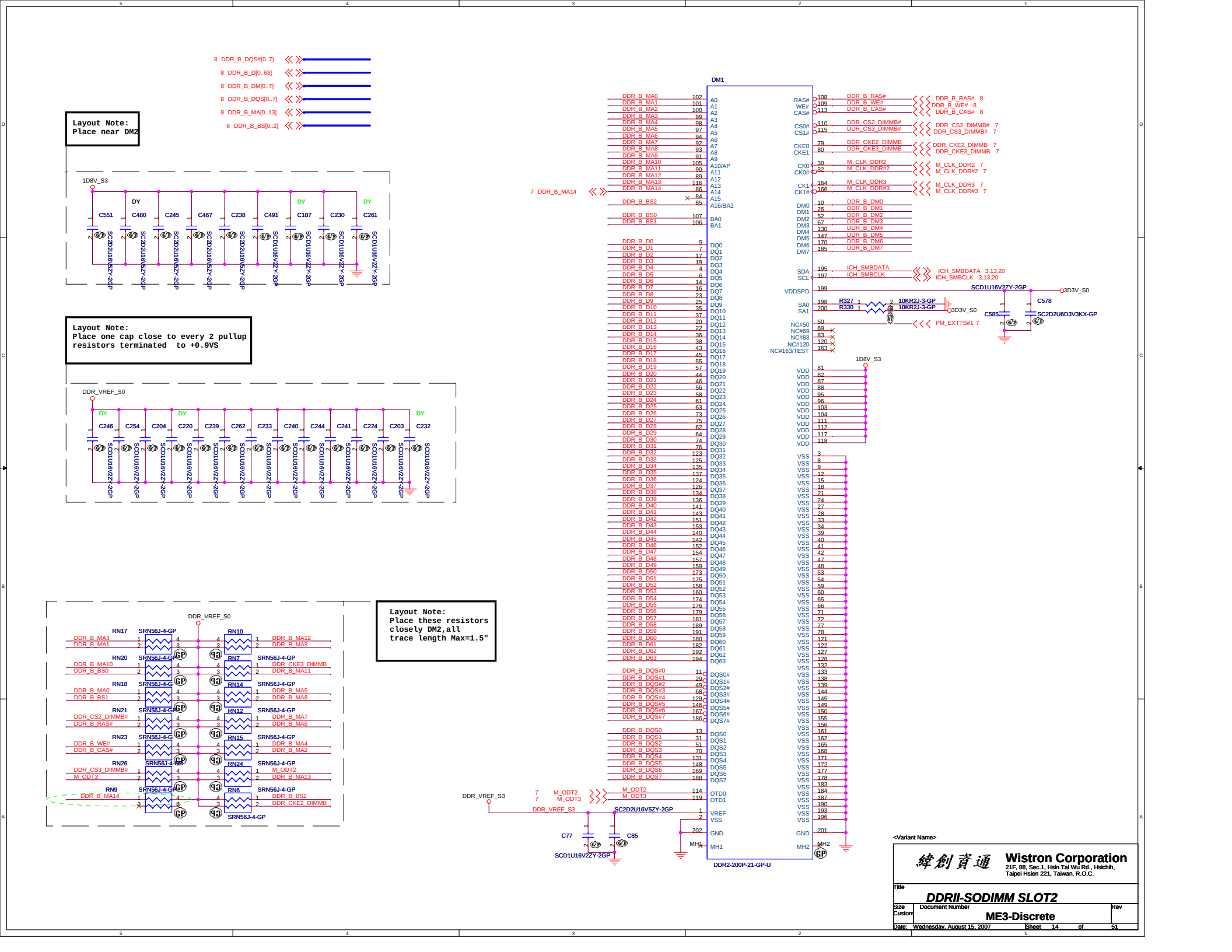
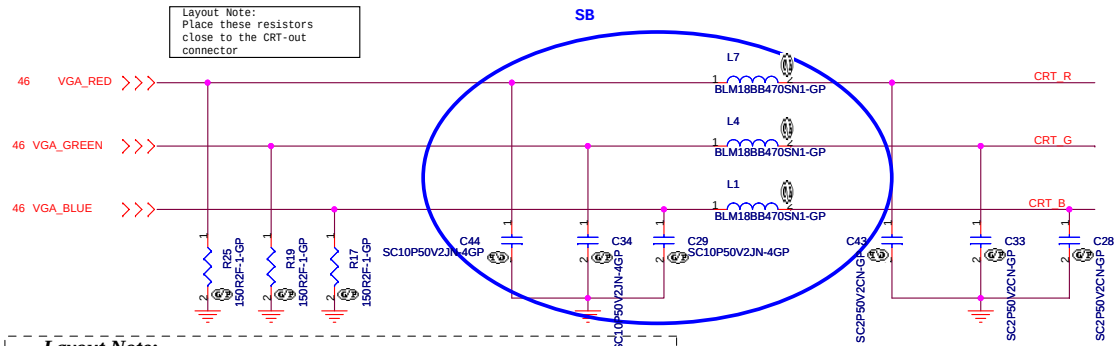
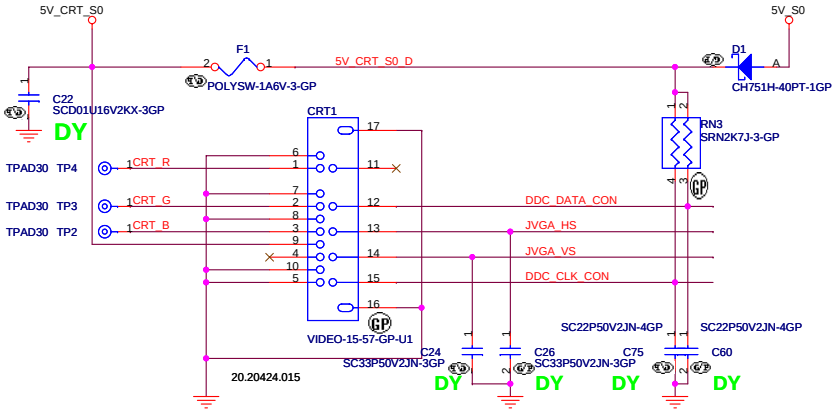
DDR_A_D36
DDR_A_D37
DDR_A_D38
DDR_A_D39
DDR_A_D40
DDR_A_D41
DDR_A_D42
DDR_A_D43
DDR_A_D44
DDR_A_D45
DDR_A_D46
DDR_A_D47
DDR_A_D48
DDR_A_D49
DDR_A_D50
DDR_A_D51
DDR_A_D52
DDR_A_D53
DDR_A_D54
DDR_A_D55
DDR_A_D56
DDR_A_D57
DDR_A_D58
DDR_A_D59
DDR_A_D60
DDR_A_D61
DDR_A_D62
DDR_A_D63
DDR_A_DQS#0
DDR_A_DQS#1
DDR_A_DQS#2
DDR_A_DQS#3
DDR_A_DQS#4
DDR_A_DQS#5
DDR_A_DQS#6
DDR_A_DQS#7
DDR_A_DQS0
DDR_A_DQS1
DDR_A_DQS2
DDR_A_DQS3
DDR_A_DQS4
DDR_A_DQS5
DDR_A_DQS6
DDR_A_DQS7
M_ODT0
M_ODT1
DDR_VREF_S3
SC2D2U16V5ZY-2GP
C84
C90
SCD1U16V2ZY-2GP
MH1
MH2
DDR2-200P-20-GP-U
DDR_A_RAS#
DDR_A_WE#
DDR_A_CAS#
DDR_CS0_DIMMA#
DDR_CS1_DIMMA#
DDR_CKE0_DIMMA
DDR_CKE1_DIMMA
M_CLK_DDR0
M_CLK_DDR#0
M_CLK_DDR1
M_CLK_DDR#1
DDR_A_DM0
DDR_A_DM1
DDR_A_DM2
DDR_A_DM3
DDR_A_DM4
DDR_A_DM5
DDR_A_DM6
DDR_A_DM7
ICH_SMBDATA
ICH_SMBCLK
ICH_SMBDATA 3,14,20
ICH_SMBCLK 3,14,20
SCD1U16V2ZY-2GP
3D3V_S0
R321
R322
10KR2J-3-GP
C570
C572
SC2D2U6D3V3KX-GP
PM_EXTTS#0 7
1D8V_S3
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDRII-SODIMM SLOT1
Size
Custom
Document Number
ME3-Discrete
Rev
Date: Wednesday, August 15, 2007
Sheet 13 of 51


8 DDR_B_DQS#[0..7]
8 DDR_B_D[0..63]
8 DDR_B_DM[0..7]
8 DDR_B_DQS[0..7]
8 DDR_B_MA[0..13]
8 DDR_B_BS[0..2]
Layout Note:
Place near DM2
1D8V_S3
DY
C551 C480 C245 C467 C238 C491 C187 C230 C261
SC2D2U16V5ZY-2GP
SCD1U16V2ZY-2GP
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS
DDR_VREF_S0
C246 C254 C204 C220 C239 C262 C233 C240 C244 C241 C224 C203 C232
SCD1U16V2ZY-2GP
DDR_VREF_S0
RN17 SRN56J-4-GP DDR_B_MA3 DDR_B_MA1
RN20 SRN56J-4-GP DDR_B_MA10 DDR_B_BS0
RN18 SRN56J-4-GP DDR_B_MA0 DDR_B_BS1
RN21 SRN56J-4-GP DDR_CS2_DIMMB# DDR_B_RAS#
RN23 SRN56J-4-GP DDR_B_WE# DDR_B_CAS#
RN26 SRN56J-4-GP DDR_CS3_DIMMB# M_ODT3
RN9 SRN56J-4-GP DDR_B_MA14
RN10 DDR_B_MA12 DDR_B_MA9
RN7 DDR_CKE3_DIMMB DDR_B_MA11
RN14 DDR_B_MA5 DDR_B_MA8
RN12 DDR_B_MA7 DDR_B_MA6
RN15 DDR_B_MA4 DDR_B_MA2
RN24 M_ODT2 DDR_B_MA13
RN6 DDR_B_BS2 DDR_CKE2_DIMMB
SRN56J-4-GP
Layout Note:
Place these resistors
closely DM2,all
trace length Max=1.5"
DM1
DDR_B_MA0 DDR_B_MA1 DDR_B_MA2 DDR_B_MA3 DDR_B_MA4 DDR_B_MA5 DDR_B_MA6 DDR_B_MA7 DDR_B_MA8 DDR_B_MA9 DDR_B_MA10 DDR_B_MA11 DDR_B_MA12 DDR_B_MA13 DDR_B_MA14
DDR_B_BS2 DDR_B_BS0 DDR_B_BS1
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12 A13 A14 A15 A16/BA2 BA0 BA1
DDR_B_D0 DDR_B_D1 DDR_B_D2 DDR_B_D3 DDR_B_D4 DDR_B_D5 DDR_B_D6 DDR_B_D7 DDR_B_D8 DDR_B_D9 DDR_B_D10 DDR_B_D11 DDR_B_D12 DDR_B_D13 DDR_B_D14 DDR_B_D15 DDR_B_D16 DDR_B_D17 DDR_B_D18 DDR_B_D19 DDR_B_D20 DDR_B_D21 DDR_B_D22 DDR_B_D23 DDR_B_D24 DDR_B_D25 DDR_B_D26 DDR_B_D27 DDR_B_D28 DDR_B_D29 DDR_B_D30 DDR_B_D31 DDR_B_D32 DDR_B_D33 DDR_B_D34 DDR_B_D35 DDR_B_D36 DDR_B_D37 DDR_B_D38 DDR_B_D39 DDR_B_D40 DDR_B_D41 DDR_B_D42 DDR_B_D43 DDR_B_D44 DDR_B_D45 DDR_B_D46 DDR_B_D47 DDR_B_D48 DDR_B_D49 DDR_B_D50 DDR_B_D51 DDR_B_D52 DDR_B_D53 DDR_B_D54 DDR_B_D55 DDR_B_D56 DDR_B_D57 DDR_B_D58 DDR_B_D59 DDR_B_D60 DDR_B_D61 DDR_B_D62 DDR_B_D63
DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15 DQ16 DQ17 DQ18 DQ19 DQ20 DQ21 DQ22 DQ23 DQ24 DQ25 DQ26 DQ27 DQ28 DQ29 DQ30 DQ31 DQ32 DQ33 DQ34 DQ35 DQ36 DQ37 DQ38 DQ39 DQ40 DQ41 DQ42 DQ43 DQ44 DQ45 DQ46 DQ47 DQ48 DQ49 DQ50 DQ51 DQ52 DQ53 DQ54 DQ55 DQ56 DQ57 DQ58 DQ59 DQ60 DQ61 DQ62 DQ63
DDR_B_DQS#0 DDR_B_DQS#1 DDR_B_DQS#2 DDR_B_DQS#3 DDR_B_DQS#4 DDR_B_DQS#5 DDR_B_DQS#6 DDR_B_DQS#7
DQS0# DQS1# DQS2# DQS3# DQS4# DQS5# DQS6# DQS7#
DDR_B_DQS0 DDR_B_DQS1 DDR_B_DQS2 DDR_B_DQS3 DDR_B_DQS4 DDR_B_DQS5 DDR_B_DQS6 DDR_B_DQS7
DQS0 DQS1 DQS2 DQS3 DQS4 DQS5 DQS6 DQS7
M_ODT2 M_ODT3
OTD0 OTD1
VREF VSS GND MH1
DDR2-200P-21-GP-U
RAS# WE# CAS# CS0# CS1# CKE0 CKE1 CK0 CK0# CK1 CK1#
DDR_B_RAS# DDR_B_WE# DDR_B_CAS# DDR_CS2_DIMMB# DDR_CS3_DIMMB# DDR_CKE2_DIMMB DDR_CKE3_DIMMB M_CLK_DDR2 M_CLK_DDR#2 M_CLK_DDR3 M_CLK_DDR#3
DM0 DM1 DM2 DM3 DM4 DM5 DM6 DM7
DDR_B_DM0 DDR_B_DM1 DDR_B_DM2 DDR_B_DM3 DDR_B_DM4 DDR_B_DM5 DDR_B_DM6 DDR_B_DM7
SDA SCL
ICH_SMBDATA ICH_SMBCLK
VDDSPD SA0 SA1
R327 10KR2J-3-GP R330 10KR2J-3-GP
3D3V_S0
SCD1U16V2ZY-2GP C578
C585 SC2D2U6D3V3KX-GP
NC#50 NC#69 NC#83 NC#120 NC#163/TEST
PM_EXTTS#1
1D8V_S3
VDD VSS
DDR_VREF_S3
M_ODT2 M_ODT3
SC2D2U16V5ZY-2GP
C77 C85
SCD1U16V2ZY-2GP
MH1 MH2
<Variant Name>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDRII-SODIMM SLOT2
Size Custom
Document Number
ME3-Discrete
Rev
Date: Wednesday, August 15, 2007
Sheet 14 of 51

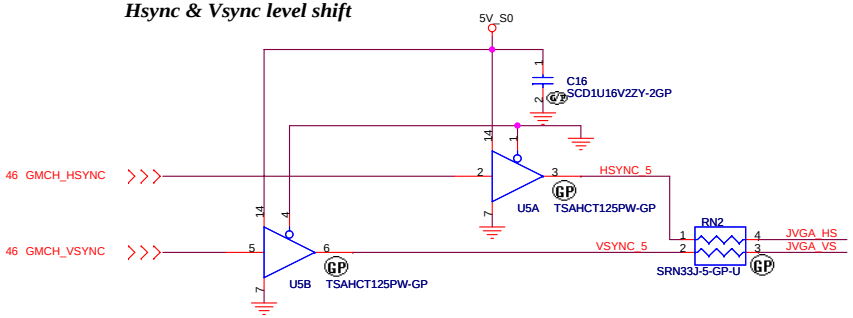
CRT I/F & CONNECTOR

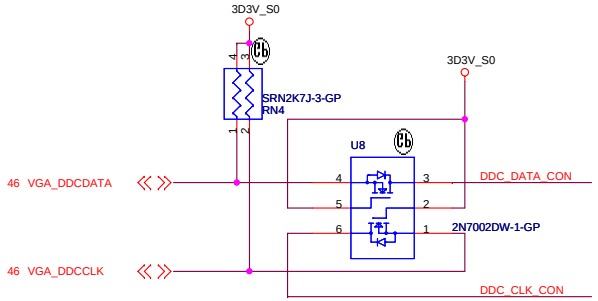


Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

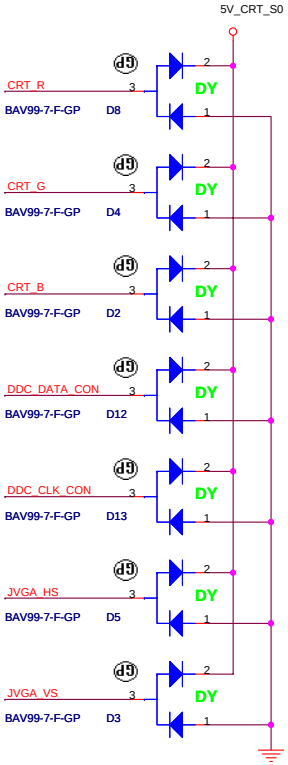


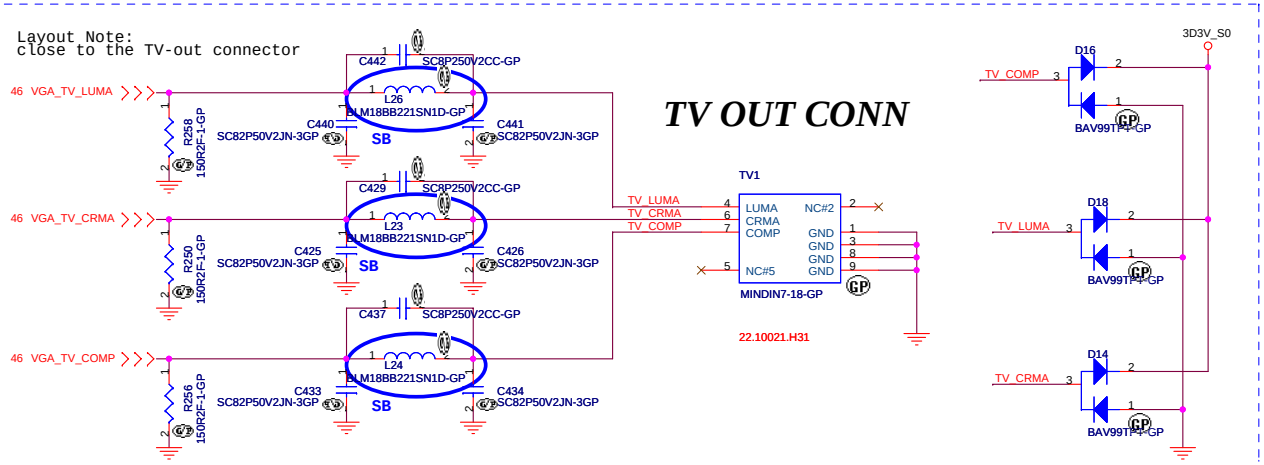
Hsync & Vsync level shift





DDC_CLK & DATA level shift



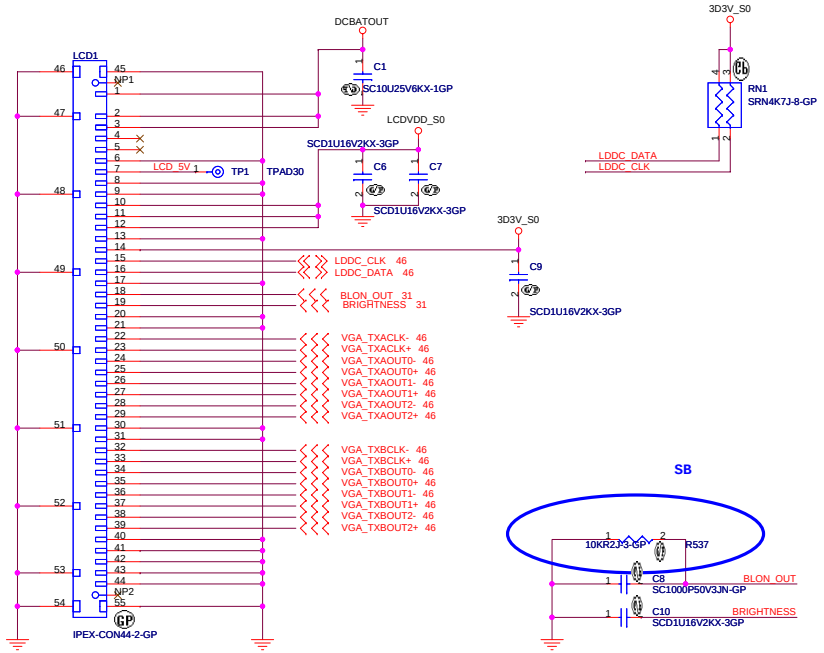


TV OUT CONN

<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**CRT/TV CONNECTOR**	
Size A3	Document Number **ME3-Discrete**	Rev
Date: Thursday, September 13, 2007	Sheet 15 of 51	

LCD/INVERTER CONN



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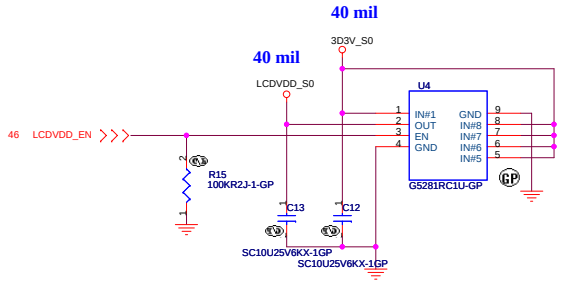
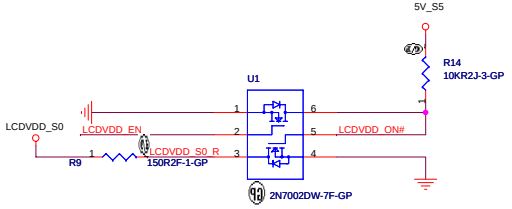
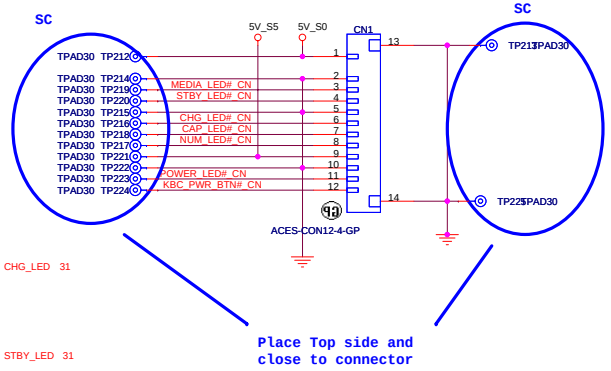
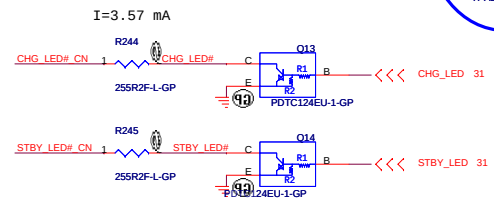
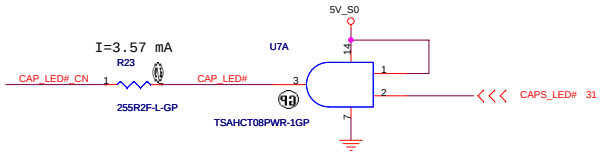


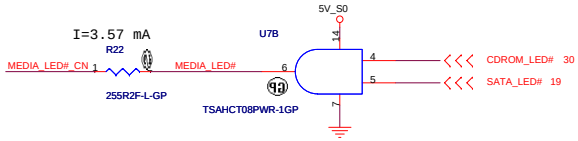


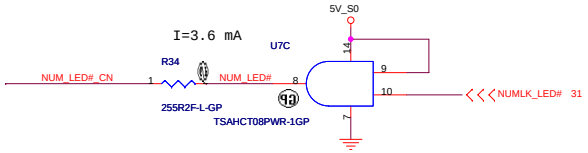
LED CONN

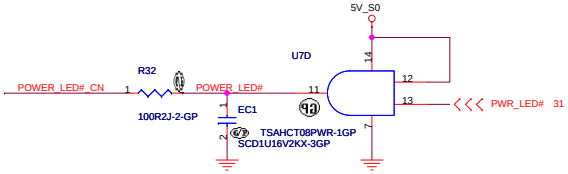


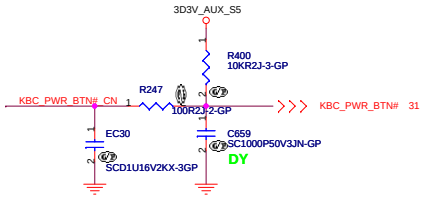






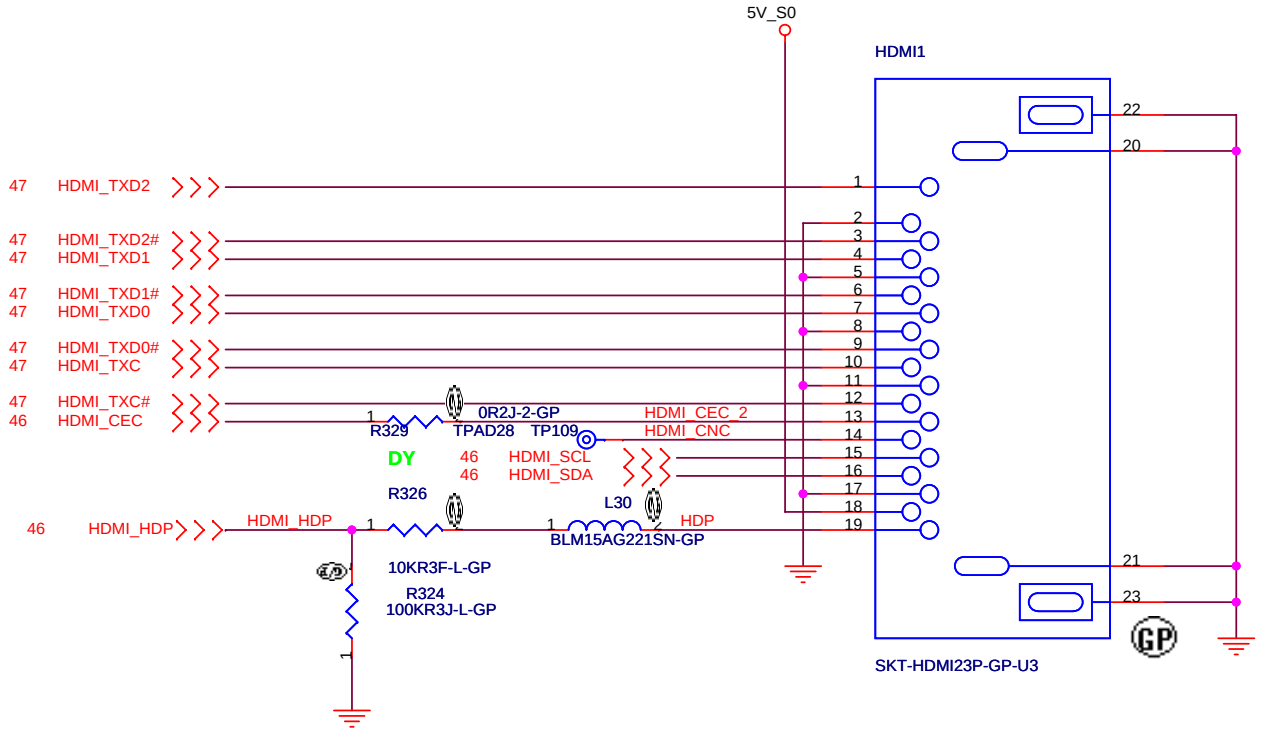




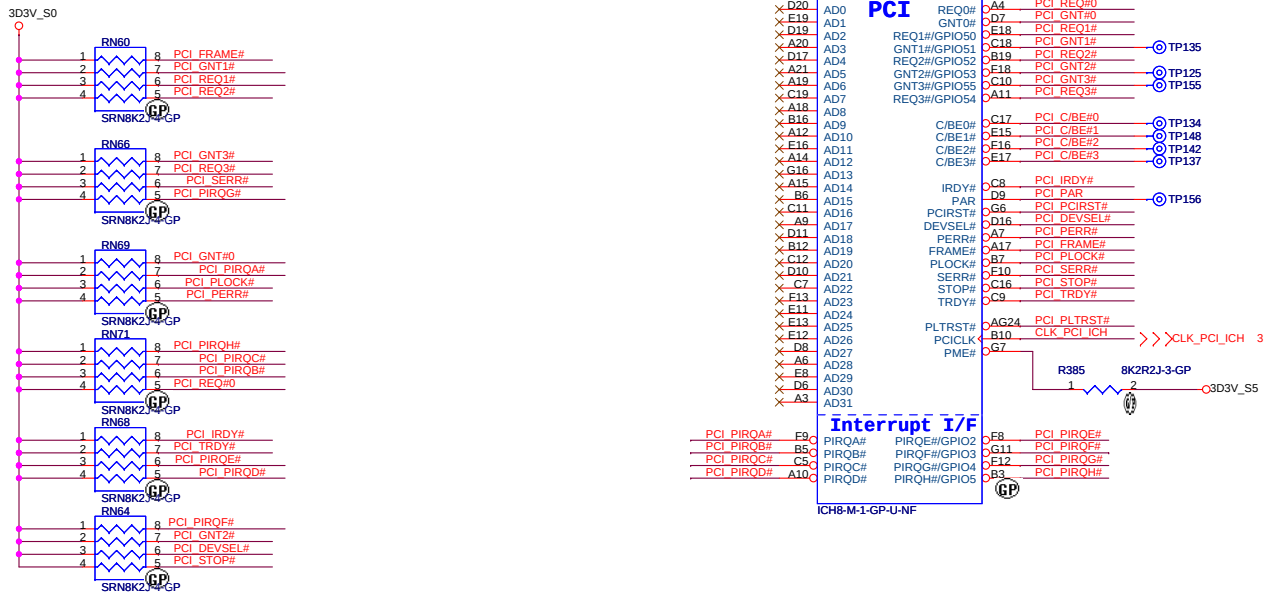


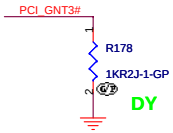
<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*LCD CONN & LED*
Size / Document Number	**ME3-Discrete** / Rev
Date: Thursday, September 13, 2007	Sheet 16 of 51

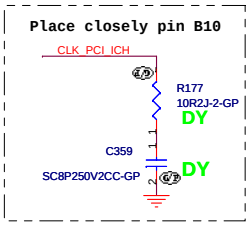


緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: ***HDMI***		
Size	Document Number: **ME3-Discrete**	Rev
Date: Wednesday, August 15, 2007	Sheet 17 of 51	

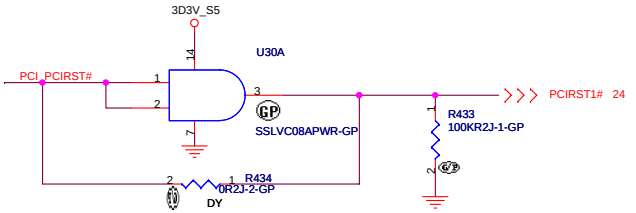


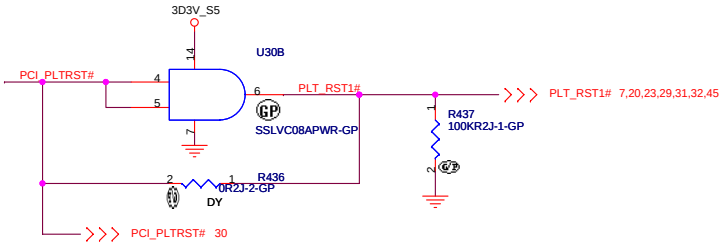


A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default *



Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *





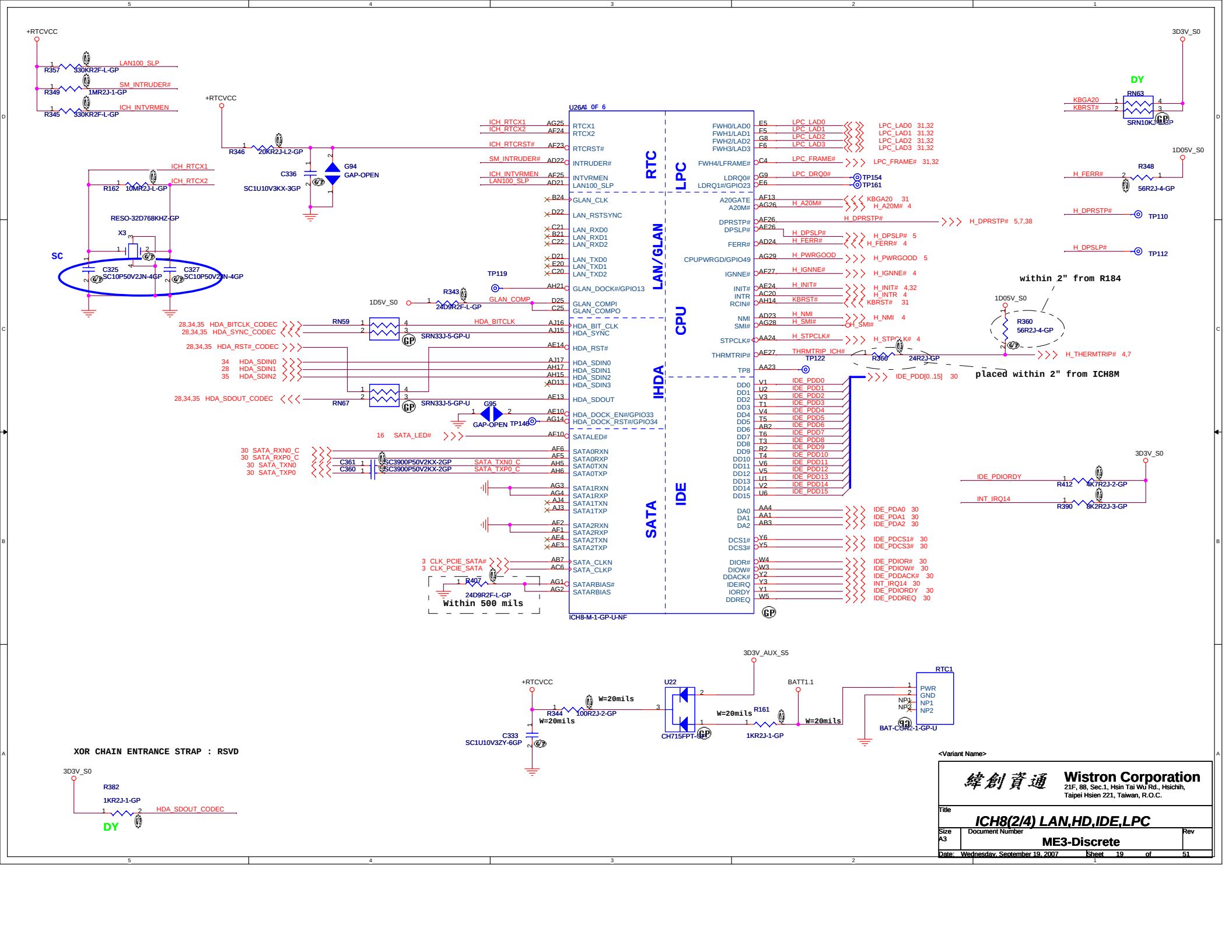
<Variant Name>

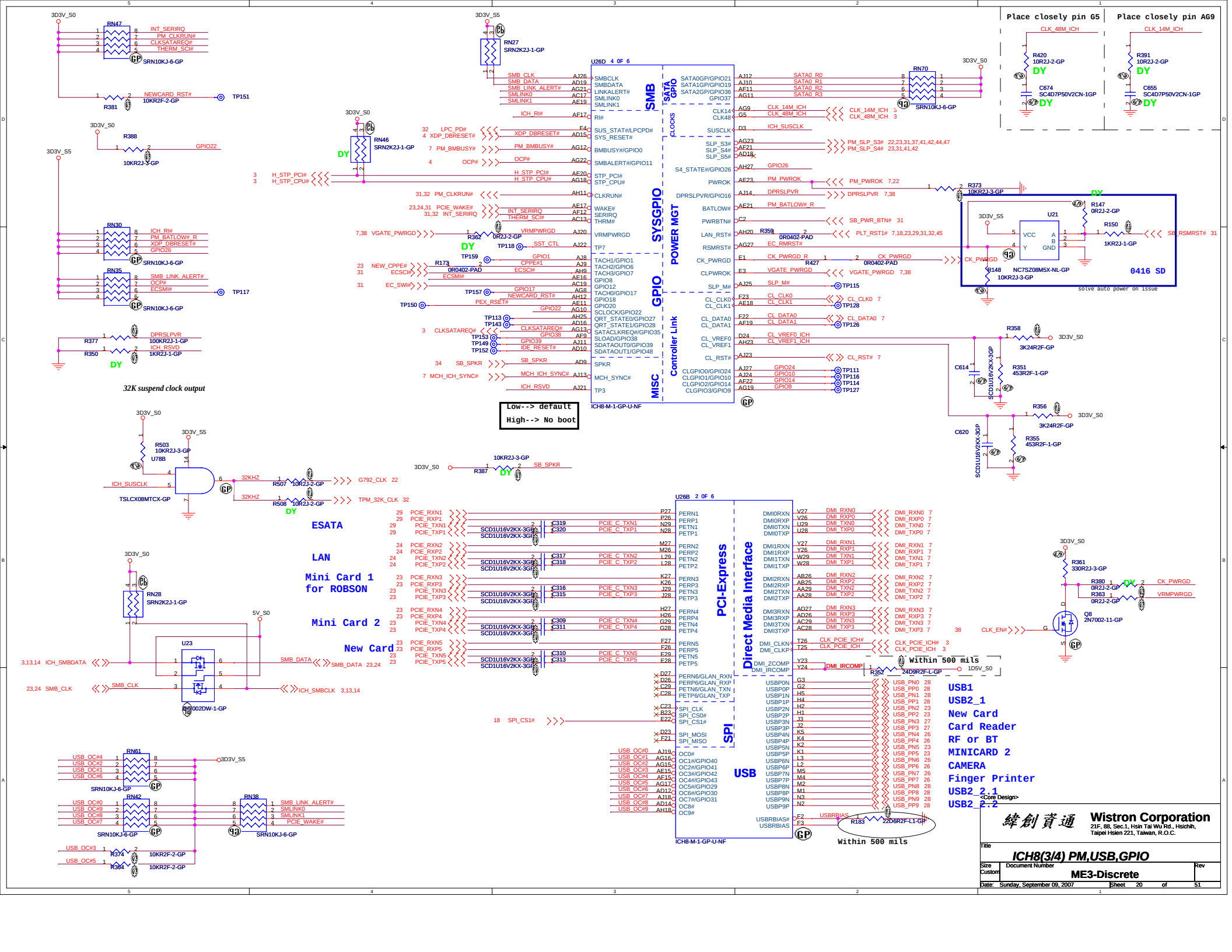
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

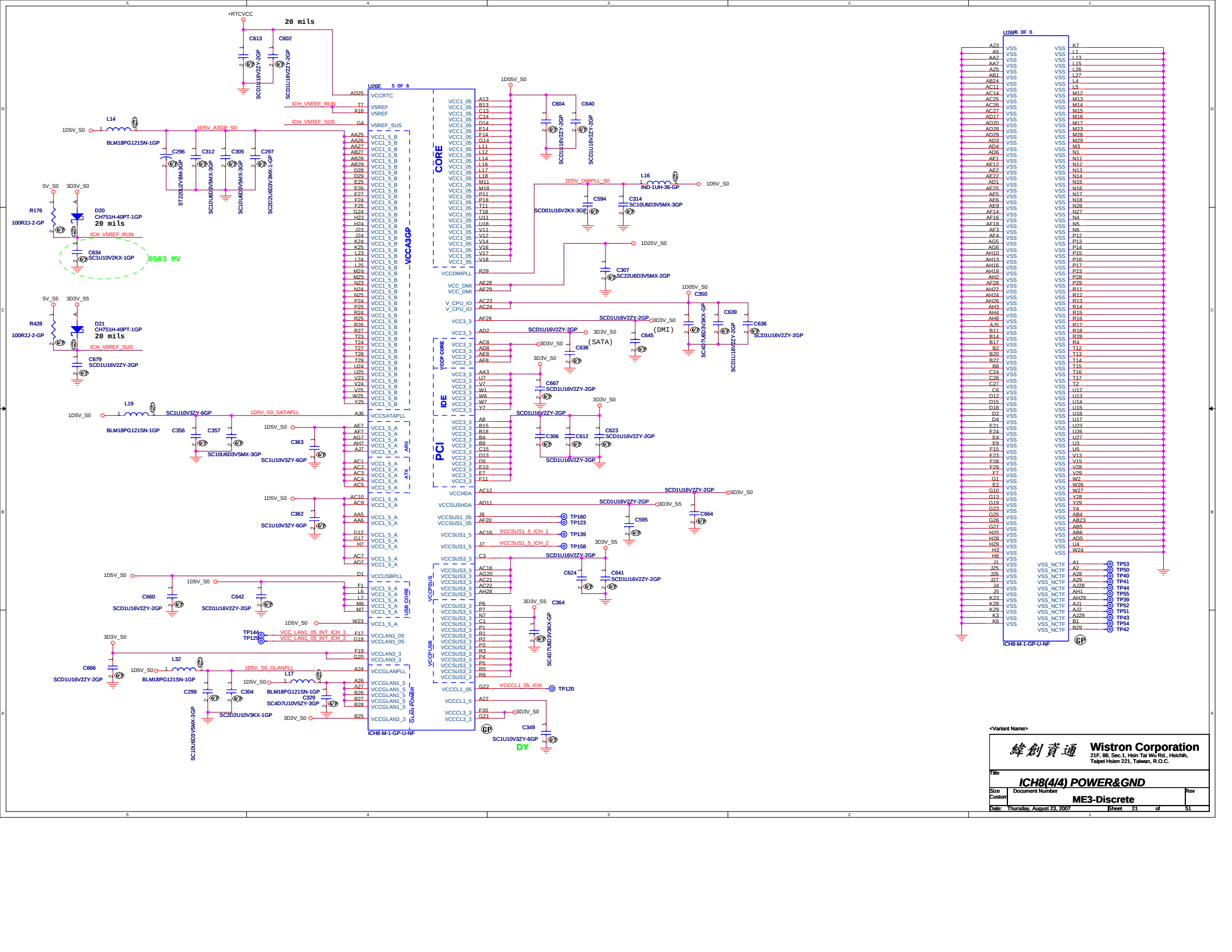
Title: **ICH8(1/4)-PCI/INT**

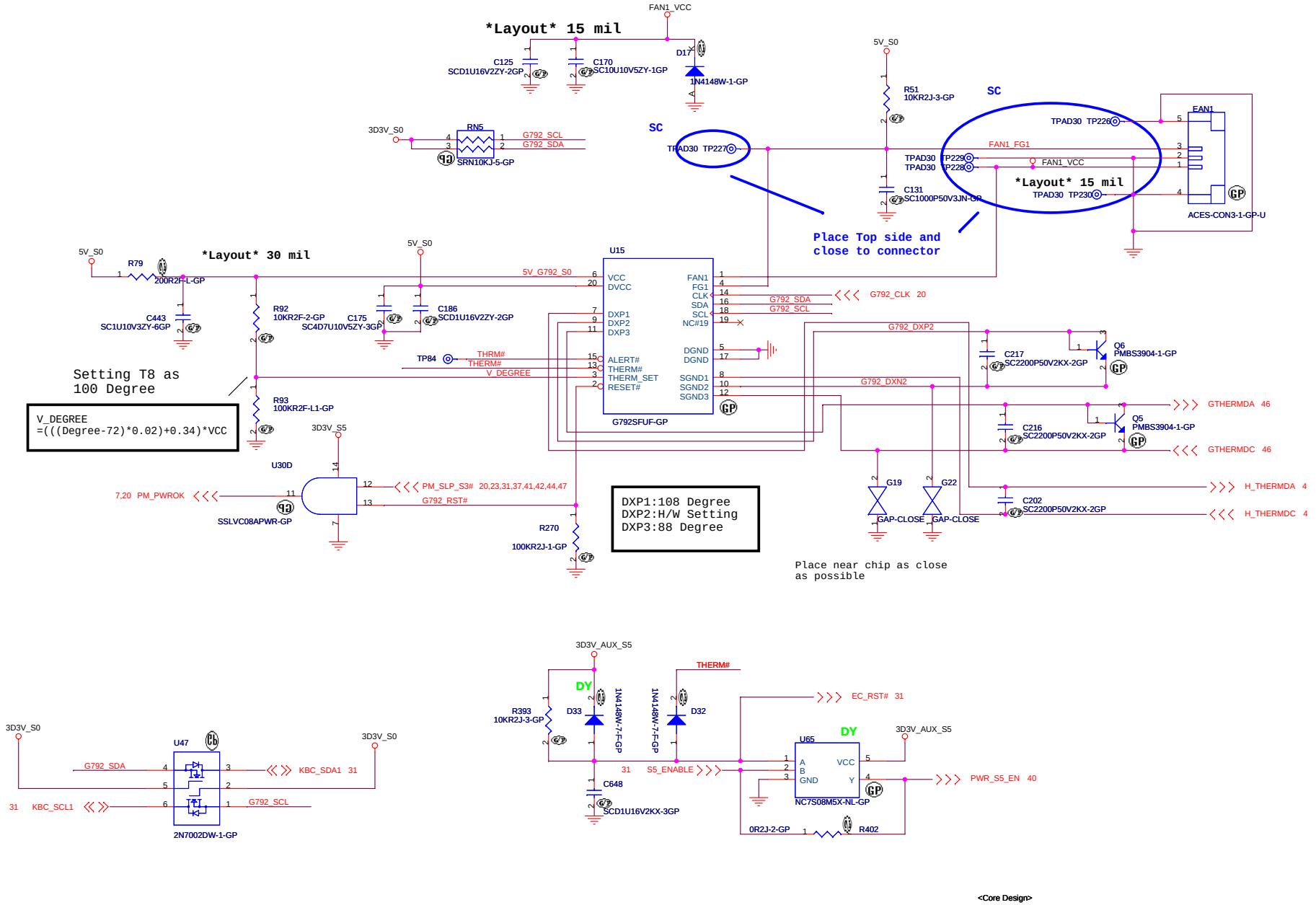
Size	Document Number	Rev
A3	ME3-Discrete	

Date: Wednesday, August 15, 2007 Sheet 18 of 51


+RTCVCC
LAN100_SLP
R357 330KR2F-L-GP
SM_INTRUDER#
R349 1MR2J-1-GP
ICH_INTVRMEN
R345 330KR2F-L-GP
ICH_RTCX1
ICH_RTCX2
R162 10MR2J-L-GP
RESO-32D768KHZ-GP
X3
SC
C325 SC10P50V2JN-4GP
C327 SC10P50V2JN-4GP
R346 20KR2J-L2-GP
C336 SC1U10V3KX-3GP
G94 GAP-OPEN
U26A1 0F 6
RTCX1
RTCX2
ICH_RTCRST#
SM_INTRUDER#
ICH_INTVRMEN
LAN100_SLP
INTRUDER#
INTVRMEN
LAN100_SLP
RTC
GLAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
GLAN_DOCK#/GPIO13
GLAN_COMPI
GLAN_COMPO
LAN/GLAN
TP119
R343 24D9R2F-L-GP
1D5V_S0
GLAN_COMP
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDOUT
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO34
IHDA
CPU
RN59 SRN33J-5-GP-U
RN67 SRN33J-5-GP-U
HDA_BITCLK_CODEC
HDA_SYNC_CODEC
HDA_RST#_CODEC
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDOUT_CODEC
G95 GAP-OPEN
TP146
SATALED#
SATA_LED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA_CLKN
SATA_CLKP
SATARBIAS#
SATARBIAS
SATA
IDE
C361 SC3900P50V2KX-2GP
C360 SC3900P50V2KX-2GP
SATA_TXN0_C
SATA_TXP0_C
CLK_PCIE_SATA#
CLK_PCIE_SATA
R407 24D9R2F-L-GP
Within 500 mils
ICH8-M-1-GP-U-NF
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
LPC_LAD0
LPC_LAD1
LPC_LAD2
LPC_LAD3
LPC_FRAME#
LPC_DRQ0#
LPC
TP154
TP161
A20GATE
A20M#
DPRSTP#
DPSLP#
FERR#
CPUPWRGD/GPIO49
IGNNE#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THRMTRIP#
TP8
TP122
H_A20M#
H_DPRSTP#
H_DPSLP#
H_FERR#
H_PWRGOOD
H_IGNNE#
H_INIT#
H_INTR
KBRST#
H_NMI
H_SMI#
H_STPCLK#
H_THERMTRIP#
R360 24R2J-GP
within 2" from R184
placed within 2" from ICH8M
DD0
DD1
DD2
DD3
DD4
DD5
DD6
DD7
DD8
DD9
DD10
DD11
DD12
DD13
DD14
DD15
IDE_PDD0
IDE_PDD1
IDE_PDD2
IDE_PDD3
IDE_PDD4
IDE_PDD5
IDE_PDD6
IDE_PDD7
IDE_PDD8
IDE_PDD9
IDE_PDD10
IDE_PDD11
IDE_PDD12
IDE_PDD13
IDE_PDD14
IDE_PDD15
IDE_PDD[0..15]
DA0
DA1
DA2
DCS1#
DCS3#
DIOR#
DIOW#
DDACK#
IDEIRQ
IORDY
DDREQ
IDE_PDA0
IDE_PDA1
IDE_PDA2
IDE_PDCS1#
IDE_PDCS3#
IDE_PDIOR#
IDE_PDIOW#
IDE_PDDACK#
INT_IRQ14
IDE_PDIORDY
IDE_PDDREQ
3D3V_S0
DY
RN63 SRN10KJ-GP
KBGA20
KBRST#
1D05V_S0
R348 56R2J-4-GP
H_FERR#
H_DPRSTP#
TP110
H_DPSLP#
TP112
R412 4K7R2J-2-GP
R390 8K2R2J-3-GP
IDE_PDIORDY
INT_IRQ14
3D3V_AUX_S5
+RTCVCC
U22 CH715FPT-GP
W=20mils
R344 100R2J-2-GP
C333 SC1U10V3ZY-6GP
R161 1KR2J-1-GP
BATT1.1
RTC1 BAT-CON2-1-GP-U
PWR
GND
NP1
NP2
XOR CHAIN ENTRANCE STRAP : RSVD
R382 1KR2J-1-GP
HDA_SDOUT_CODEC
DY
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH8(2/4) LAN,HD,IDE,LPC
Size A3
Document Number
ME3-Discrete
Rev
Date: Wednesday, September 19, 2007
Sheet 19 of 51


Place closely pin G5
Place closely pin AG9
ESATA
LAN
Mini Card 1 for ROBSON
Mini Card 2
New Card
USB1
USB2_1
New Card
Card Reader
RF or BT
MINICARD 2
CAMERA
Finger Printer
USB2_2_1
USB2_2_2
32K suspend clock output
Low--> default
High--> No boot
0416 SD
solve auto power on issue
Within 500 mils
Within 500 mils
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ICH8(3/4) PM,USB,GPIO
ME3-Discrete
Date: Sunday, September 09, 2007
Sheet 20 of 51


+RTCVCC
20 mils
C613
C602
SCD1U16V2ZY-2GP
U26E 5 OF 6
ICH_V5REF_RUN
ICH_V5REF_SUS
L14
BLM18PG121SN-1GP
1D5V_S0
1D5V_A3GP_S0
C296
C312
C305
C297
ST220U2V6M-3GP
SC10U6D3V5MX-3GP
SC22U6D3V3MX-1GP
5V_S0
3D3V_S0
R176
100R2J-2-GP
D20
CH751H-40PT-1GP
20 mils
C634
SC1U10V2KX-1GP
0503 MV
5V_S5
3D3V_S5
R428
D21
C679
SCD1U16V2ZY-2GP
L19
SC1U10V3ZY-6GP
C356
C357
SC10U6D3V5MX-3GP
1D5V_S0_SATAPLL
C363
C362
C660
C642
L32
C666
L17
C299
C304
C329
SC4D7U10V5ZY-3GP
SC2D2U10V3KX-1GP
SC10U6D3V5MX-3GP
TP144
TP129
VCC_LAN1_05_INT_ICH_1
VCC_LAN1_05_INT_ICH_2
CORE
VCCA3GP
IDE
PCI
ICC_CORE
ARX
ATX
USB_CORE
VCCPSUS
VCCPUSB
GLAN_POWER
ICH8-M-1-GP-U-NF
1D05V_S0
C604
C640
SCD1U16V2ZY-2GP
1D5V_DMIPLL_S0
L16
IND-1UH-36-GP
C594
C314
SCD01U16V2KX-3GP
SC10U6D3V5MX-3GP
1D25V_S0
C307
SC22U6D3V5MX-2GP
VCC_DMI
V_CPU_IO
VCCDMIPLL
VCCSUSHDA
VCCSUS1_05
VCCSUS1_5
VCCSUS3_3
VCCHDA
VCCUSBPLL
VCCLAN1_05
VCCLAN3_3
VCCGLANPLL
VCCGLAN1_5
VCCGLAN3_3
VCCCL1_05
VCCCL1_5
VCCCL3_3
VCCRTC
VSREF
VSREF_SUS
VCCSATAPLL
VCC1_5_A
VCC1_5_B
VCC3_3
1D05V_S0
C350
C639
C636
SC4D7U06D3V3KX-GP
SCD1U16V2ZY-2GP
SCD1U16V2ZY-2GP
3D3V_S0
(DMI)
(SATA)
C645
C638
C667
SCD1U16V2ZY-2GP
C306
C612
C623
SCD1U16V2ZY-2GP
SCD1U16V2ZY-2GP
C664
C595
SCD1U16V2ZY-2GP
3D3V_S5
TP160
TP123
TP139
TP158
VCCSUS1_5_ICH_1
VCCSUS1_5_ICH_2
C624
C641
SCD1U16V2ZY-2GP
C364
SC4D7U06D3V3KX-GP
VCCCL1_05_ICH
TP120
C349
SC1U10V3ZY-6GP
DY
U26F6 0F 6
VSS
VSS_NCTF
TP53
TP50
TP40
TP41
TP44
TP55
TP39
TP52
TP51
TP43
TP54
TP42
ICH8-M-1-GP-U-NF
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH8(4/4) POWER&GND
Size
Custom
Document Number
ME3-Discrete
Rev
Date: Thursday, August 23, 2007
Sheet 21 of 51



<Core Design>

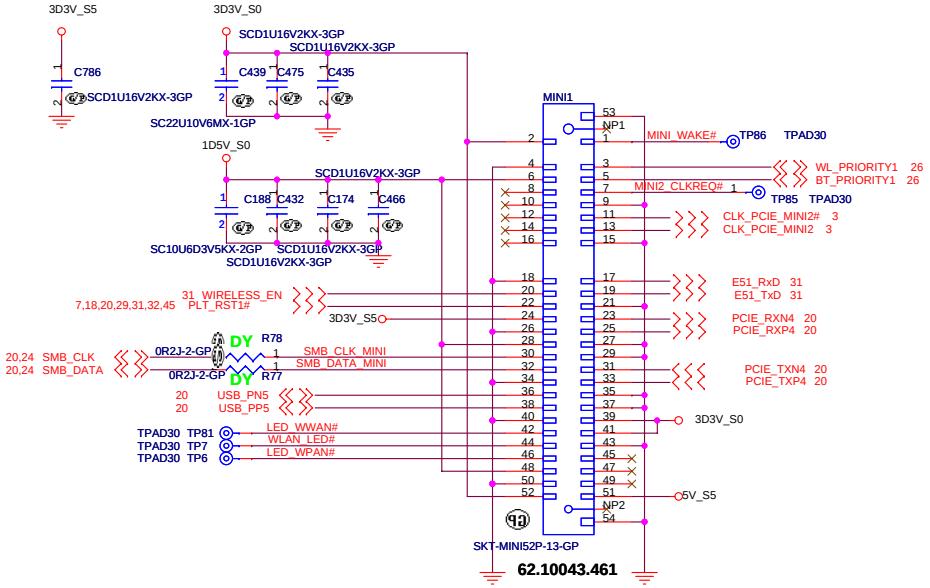
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Thermal/Fan Controllor G792***

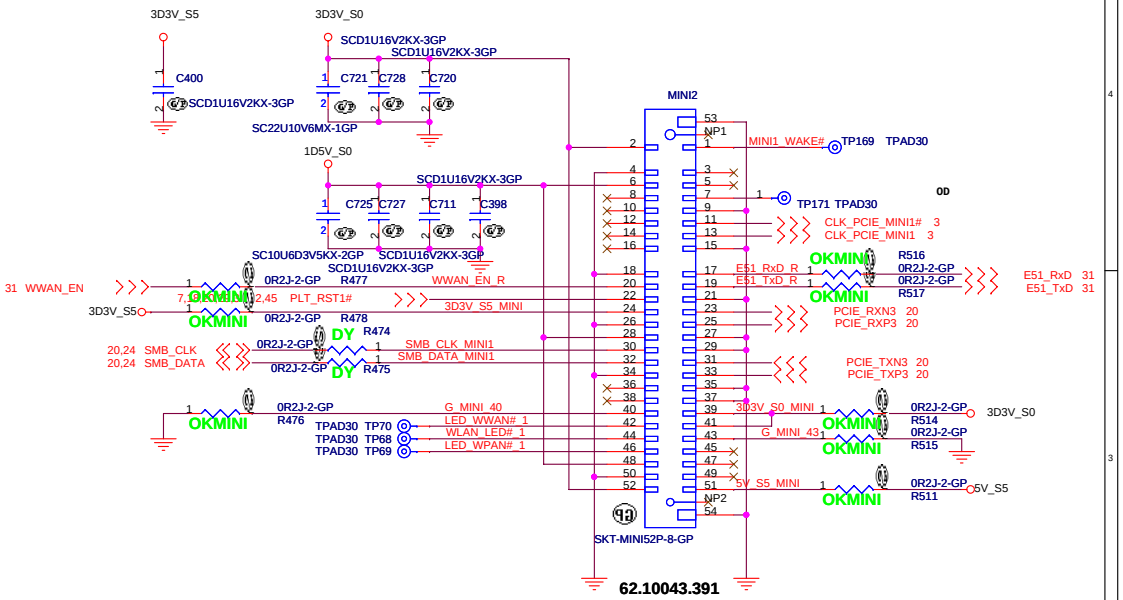
Size	Document Number	Rev
Custom	ME3-Discrete	

Date: Thursday, September 13, 2007 Sheet 22 of 51

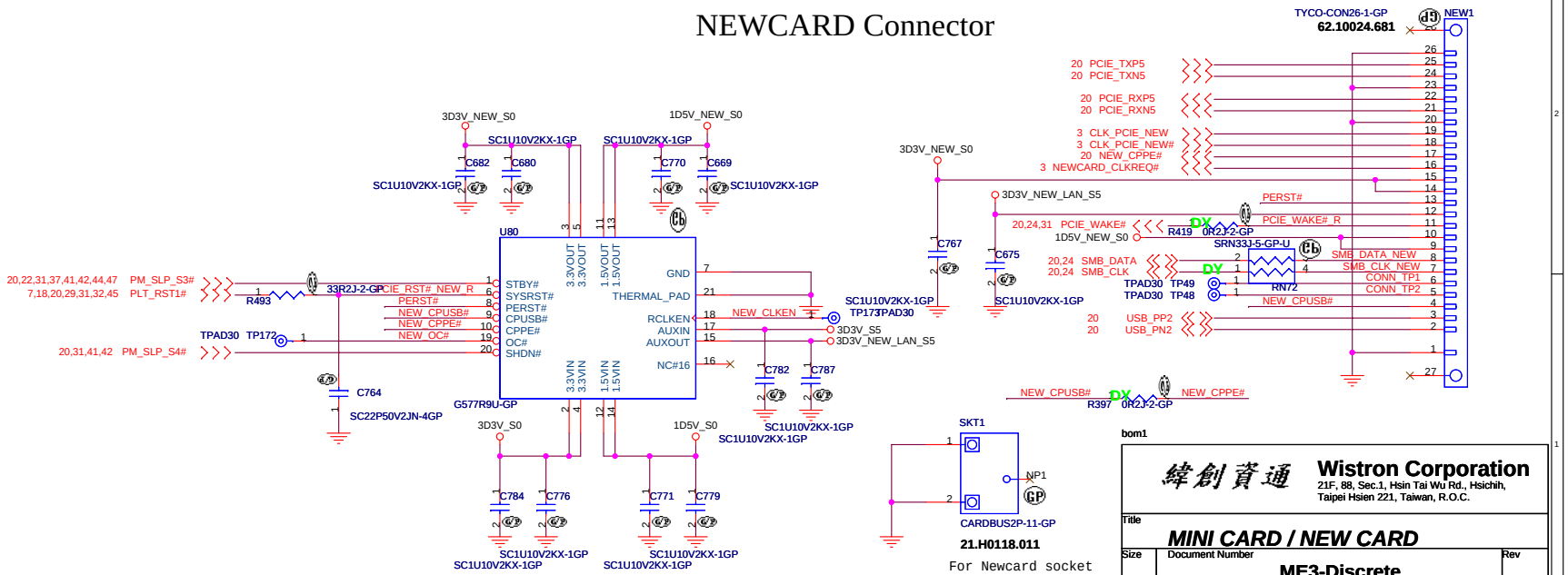
Mini Card Connector



Mini Card Connector for ROBSON



NEWCARD Connector



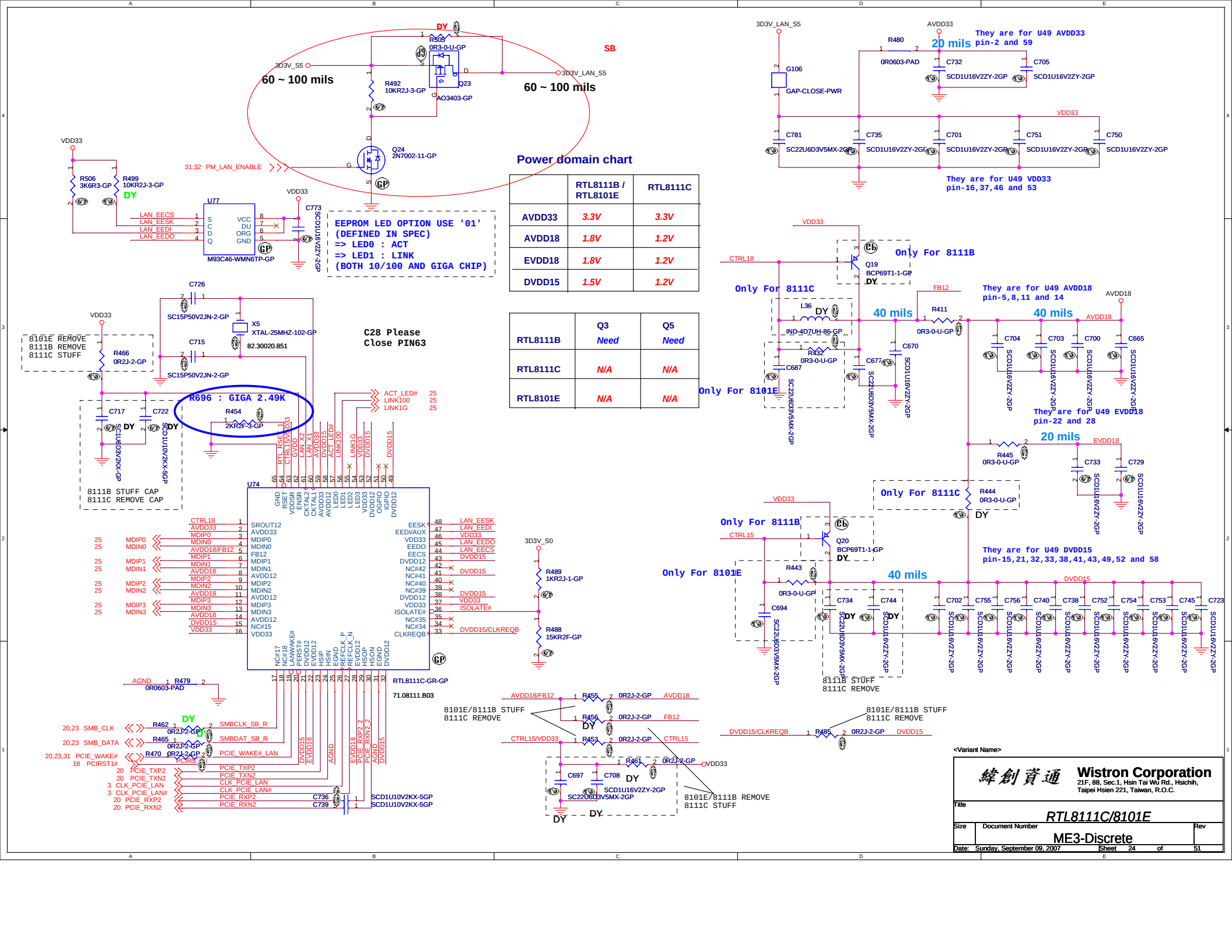
bom1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **MINI CARD / NEW CARD**

Size	Document Number	Rev
	ME3-Discrete	

Date: Thursday, August 23, 2007 Sheet 23 of 51


SB
60 ~ 100 mils
60 ~ 100 mils
3D3V_S5
3D3V_LAN_S5
R506 0R3-0-U-GP
R492 10KR2J-3-GP
Q23 AO3403-GP
Q24 2N7002-11-GP
31,32 PM_LAN_ENABLE
R506 3K6R3-GP
R499 10KR2J-3-GP
U77
M93C46-WMN6TP-GP
LAN_EECS
LAN_EESK
LAN_EEDI
LAN_EEDO
C773
EEPROM LED OPTION USE '01'
(DEFINED IN SPEC)
=> LED0 : ACT
=> LED1 : LINK
(BOTH 10/100 AND GIGA CHIP)
Power domain chart
RTL8111B / RTL8101E
RTL8111C
AVDD33 3.3V 3.3V
AVDD18 1.8V 1.2V
EVDD18 1.8V 1.2V
DVDD15 1.5V 1.2V
RTL8111B Q3 Need Q5 Need
RTL8111C N/A N/A
RTL8101E N/A N/A
C28 Please Close PIN63
X5 XTAL-25MHZ-102-GP
82.30020.851
C726
C715
R466 0R2J-2-GP
8101E REMOVE
8111B REMOVE
8111C STUFF
R696 : GIGA 2.49K
R454 2KR2F-3-GP
C717
C722
8111B STUFF CAP
8111C REMOVE CAP
U74
RTL8111C-GR-GP
71.08111.B03
R489 1KR2J-1-GP
R488 15KR2F-GP
3D3V_S0
R479 0R0603-PAD
R462 0R2J-2-GP
R465 0R2J-2-GP
R470 0R2J-2-GP
SMB_CLK
SMB_DATA
PCIE_WAKE#
PCIRST1#
PCIE_TXP2
PCIE_TXN2
CLK_PCIE_LAN
CLK_PCIE_LAN#
PCIE_RXP2
PCIE_RXN2
C736
C739
SCD1U10V2KX-5GP
8101E/8111B STUFF
8111C REMOVE
R455 0R2J-2-GP
R456 0R2J-2-GP
R453 0R2J-2-GP
R461 0R2J-2-GP
C697
C708
SC22D6D3V5MX-2GP
8101E/8111B REMOVE
8111C STUFF
3D3V_LAN_S5
AVDD33
R480 0R0603-PAD
20 mils
They are for U49 AVDD33 pin-2 and 59
G106 GAP-CLOSE-PWR
C732
C705
C781
C735
C701
C751
C750
They are for U49 VDD33 pin-16,37,46 and 53
Only For 8111B
Q19 BCP69T1-1-GP
Only For 8111C
Only For 8101E
L36 IND-4D7UH-86-GP
R411 0R3-0-U-GP
R432 0R3-0-U-GP
40 mils
40 mils
They are for U49 AVDD18 pin-5,8,11 and 14
C704
C703
C700
C665
C670
C677
C687
They are for U49 EVDD18 pin-22 and 28
20 mils
R445 0R3-0-U-GP
C733
C729
R444 0R3-0-U-GP
Only For 8111C
Only For 8111B
Q20 BCP69T1-1-GP
Only For 8101E
R443 0R3-0-U-GP
40 mils
They are for U49 DVDD15 pin-15,21,32,33,38,41,43,49,52 and 58
C694
C734
C744
C702
C755
C756
C740
C738
C752
C754
C753
C745
C723
8111B STUFF
8111C REMOVE
R485 0R2J-2-GP
8101E/8111B STUFF
8111C REMOVE
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
RTL8111C/8101E
Size
Document Number
ME3-Discrete
Rev
Date: Sunday, September 09, 2007
Sheet 24 of 51

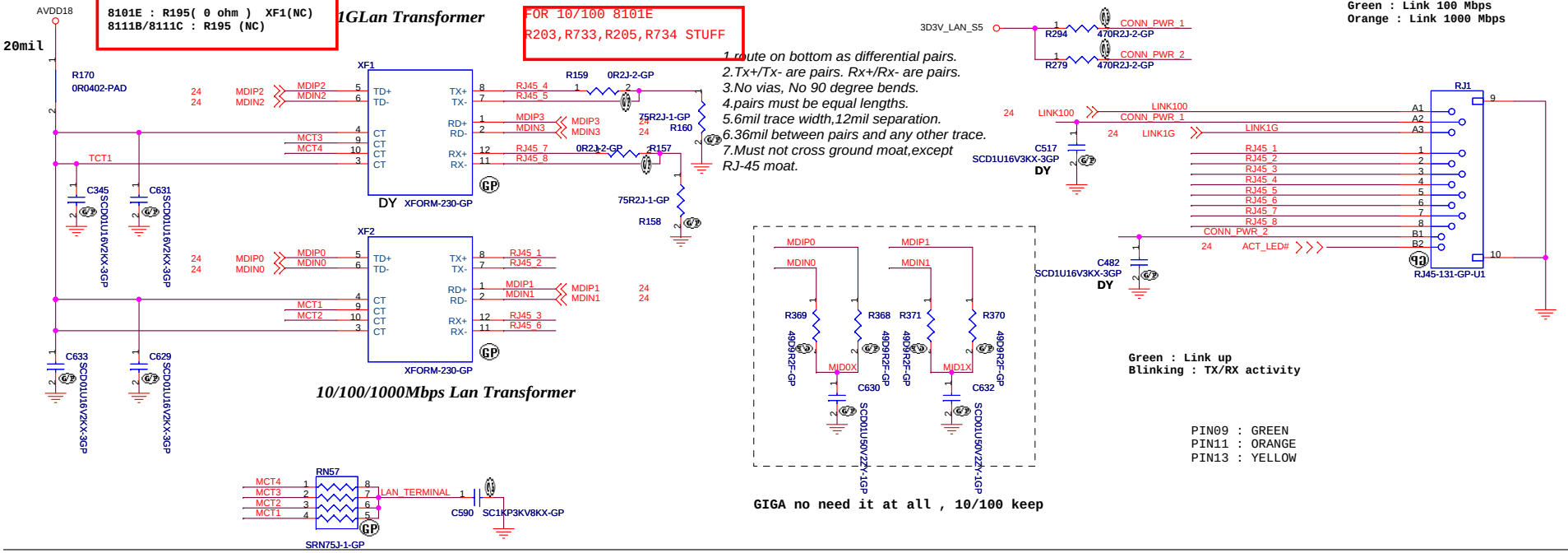
8101E : R195(0 ohm) XF1(NC)
8111B/8111C : R195 (NC)

1GLan Transformer

FOR 10/100 8101E
R203,R733,R205,R734 STUFF

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

Off : Link 10 Mbps
Green : Link 100 Mbps
Orange : Link 1000 Mbps



10/100/1000Mbps Lan Transformer

GIGA no need it at all , 10/100 keep

Green : Link up
Blinking : TX/RX activity

PIN09 : GREEN
PIN11 : ORANGE
PIN13 : YELLOW

<Core Design>

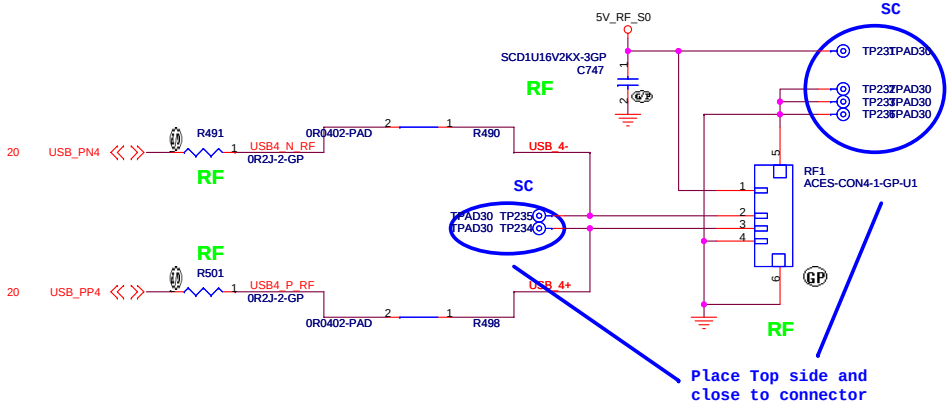
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

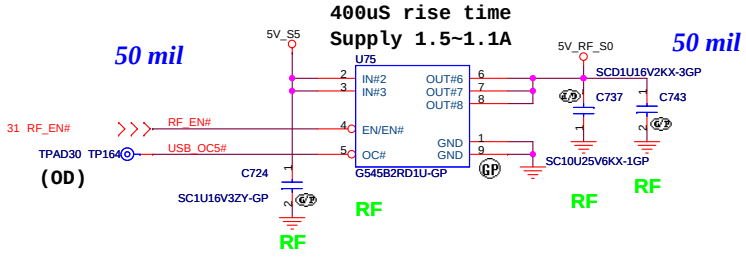
Title: LAN connector/NEW CARD/SIM

Size	Document Number	Rev
Custom	ME3-Discrete	

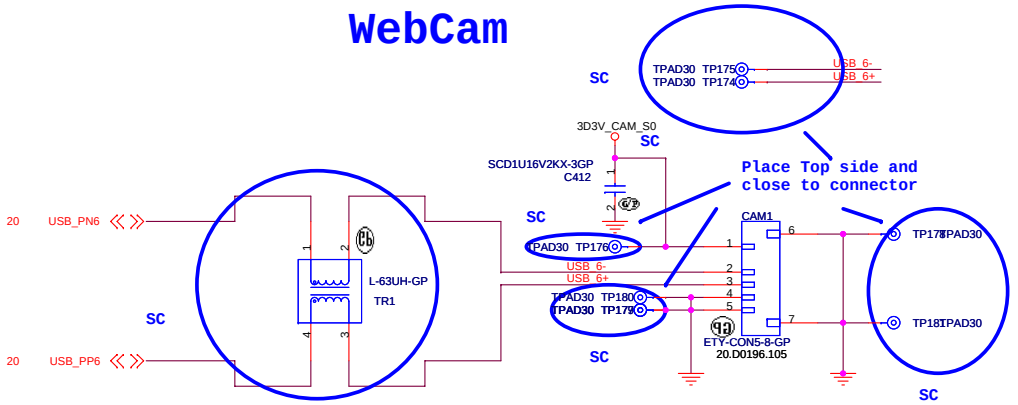
Date: Sunday, September 09, 2007 Sheet 25 of 51

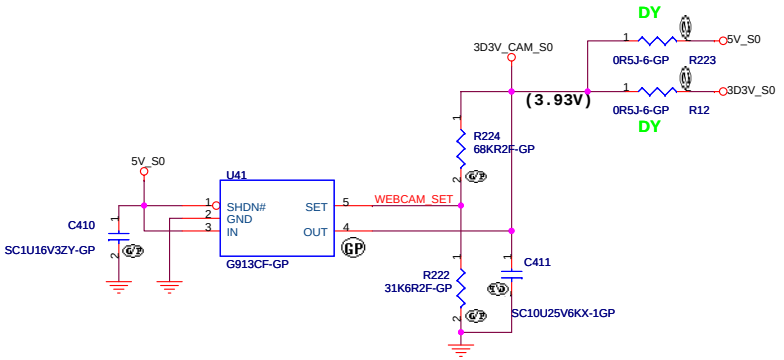
RF



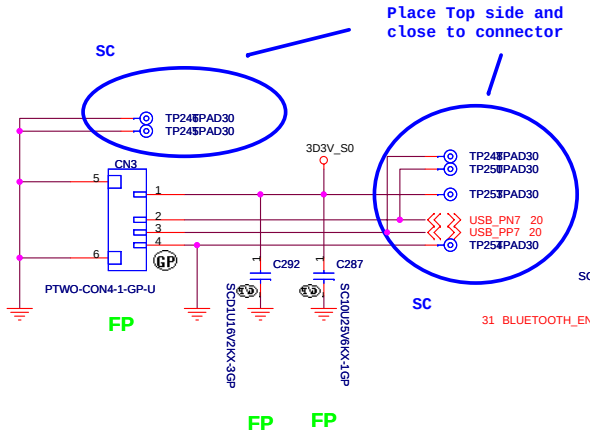


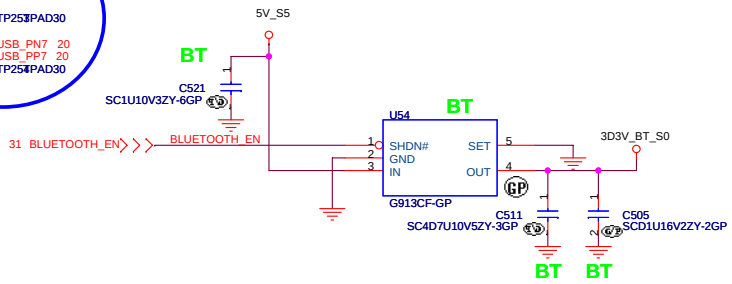
WebCam

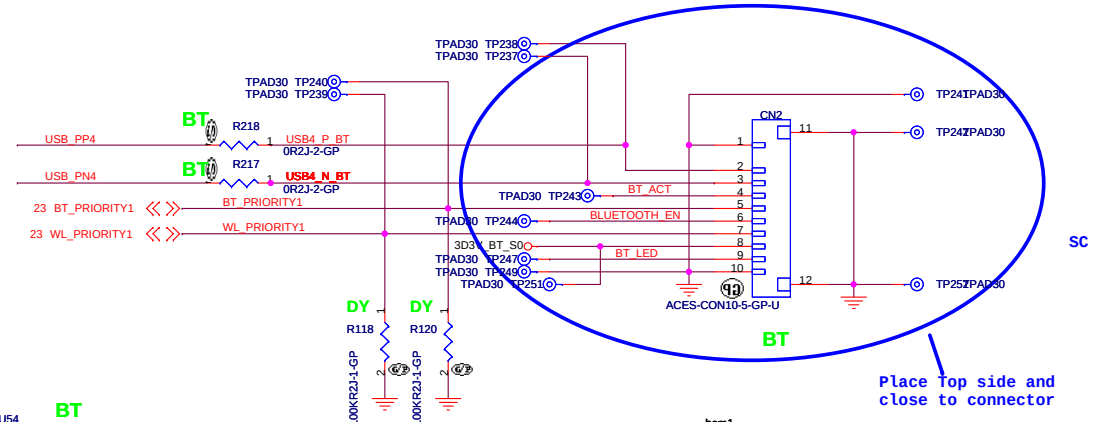




Finger Printer

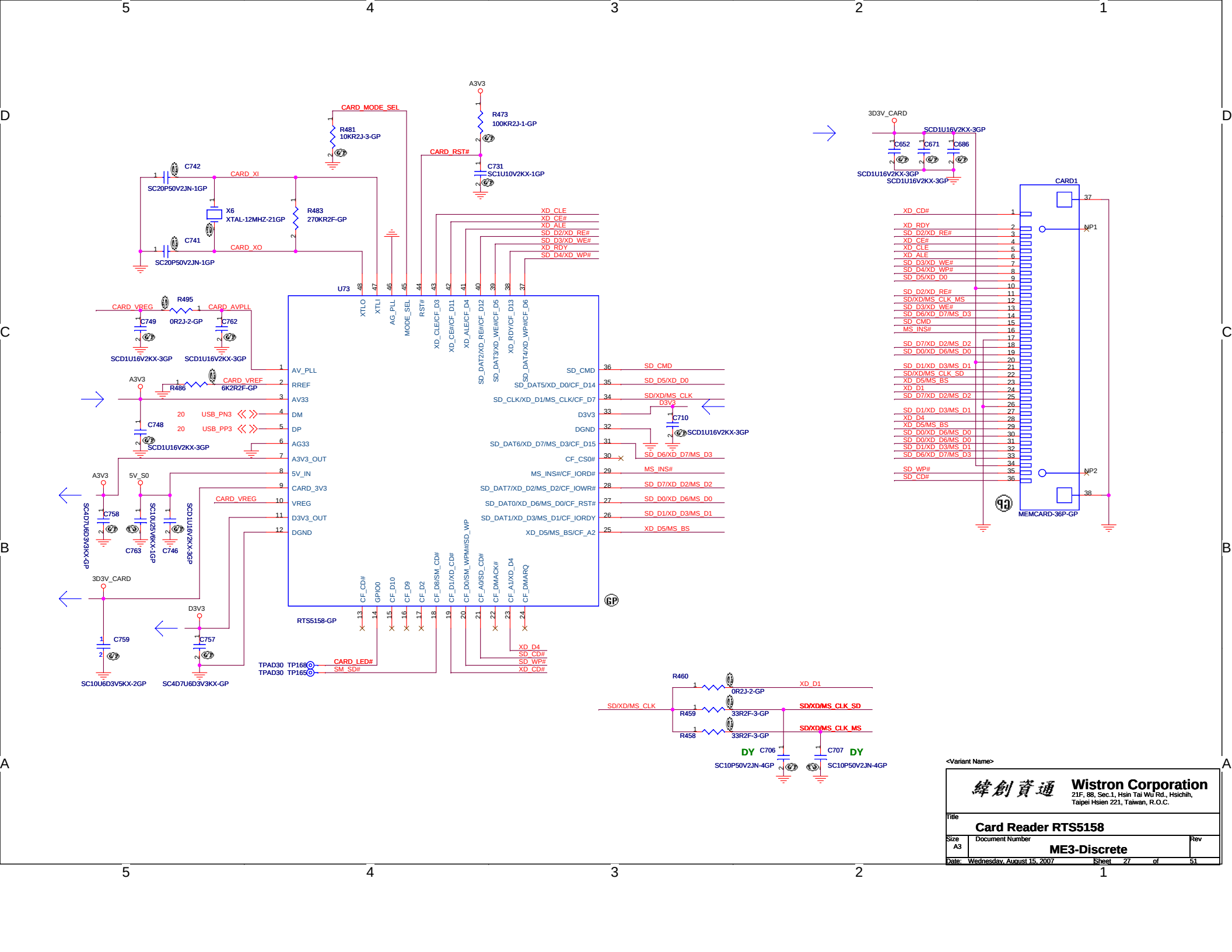






bom1

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***FP / Camera / RF / BT***	
Size	Document Number **ME3-Discrete**	Rev
Date: Thursday, September 13, 2007	Sheet 26 of 51	



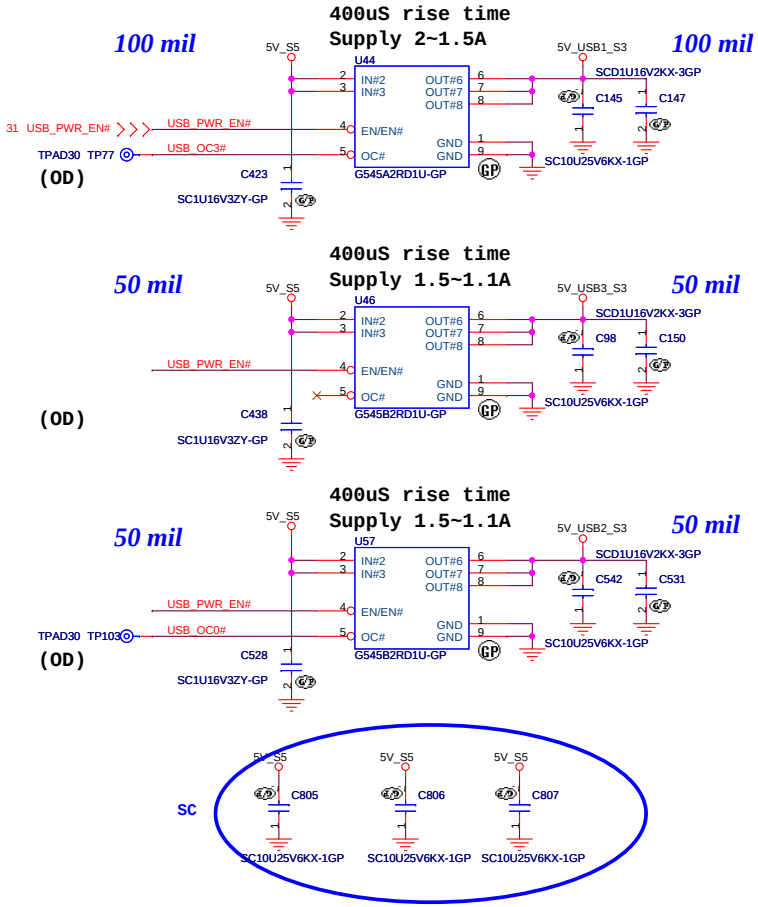
<variant_name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

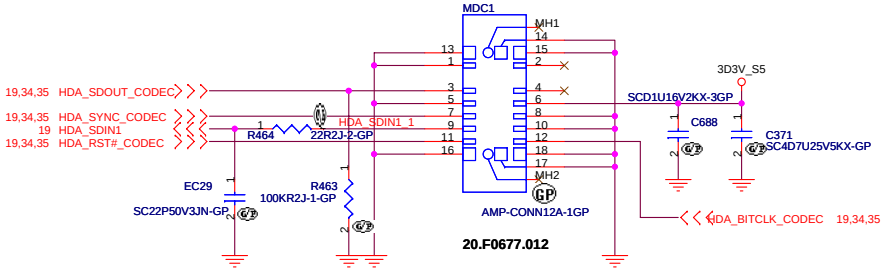
Title: Card Reader RTS5158

Size	Document Number	Rev
A3	ME3-Discrete	

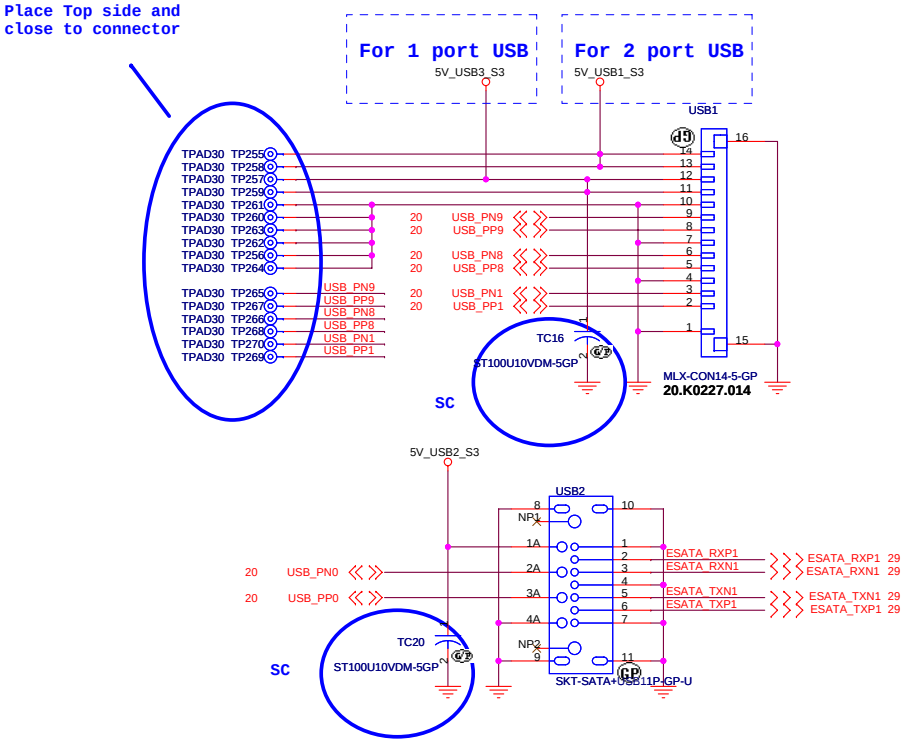
Date: Wednesday, August 15, 2007 Sheet 27 of 51



MDC 1.5 CONN



USB PORT



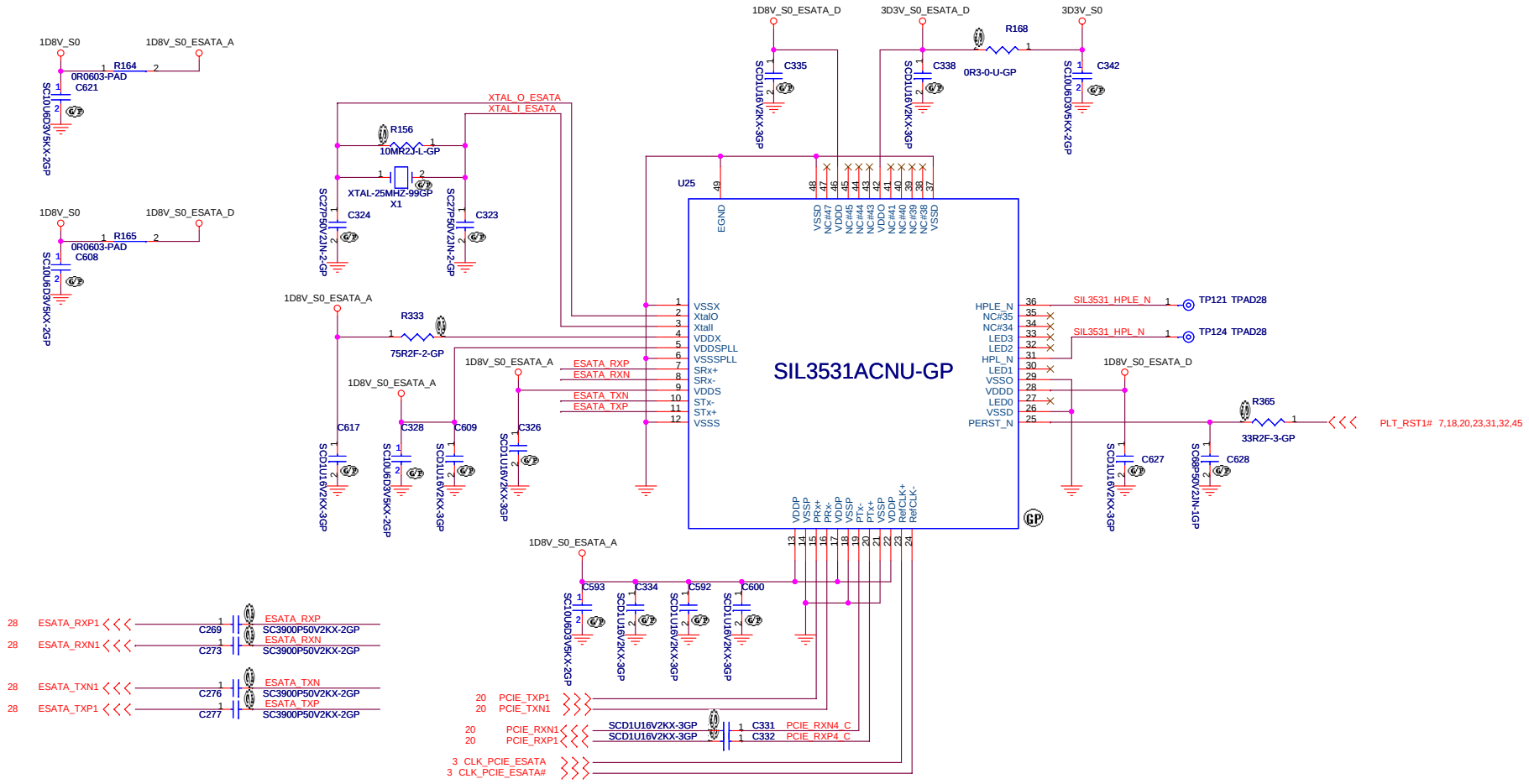
bom1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB / MDC / E-SATA CON

Size	Document Number	Rev
	ME3-Discrete	

Date: Wednesday, September 19, 2007 Sheet 28 of 51



<Core Design>

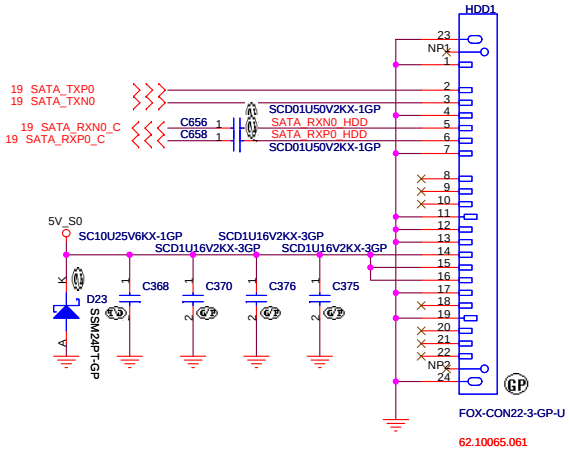
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ESATA**

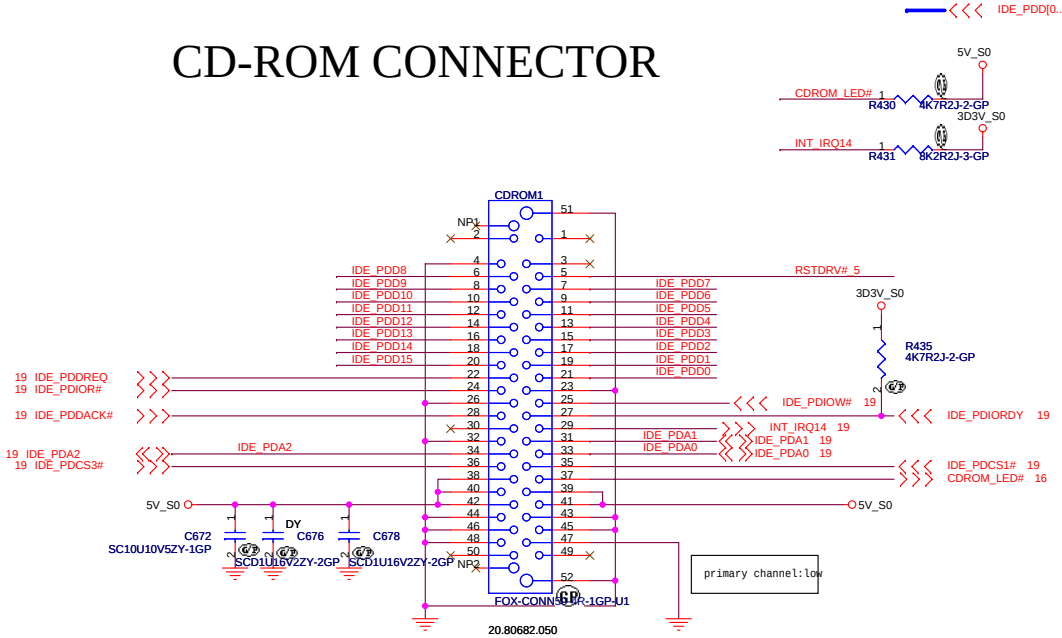
Size	Document Number	Rev
A3	ME3-Discrete	

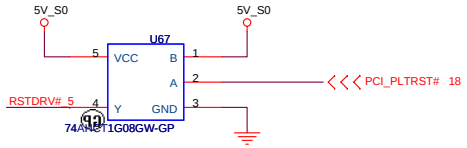
Date: Sunday, September 09, 2007 Sheet 29 of 51

SATA HD Connector



CD-ROM CONNECTOR

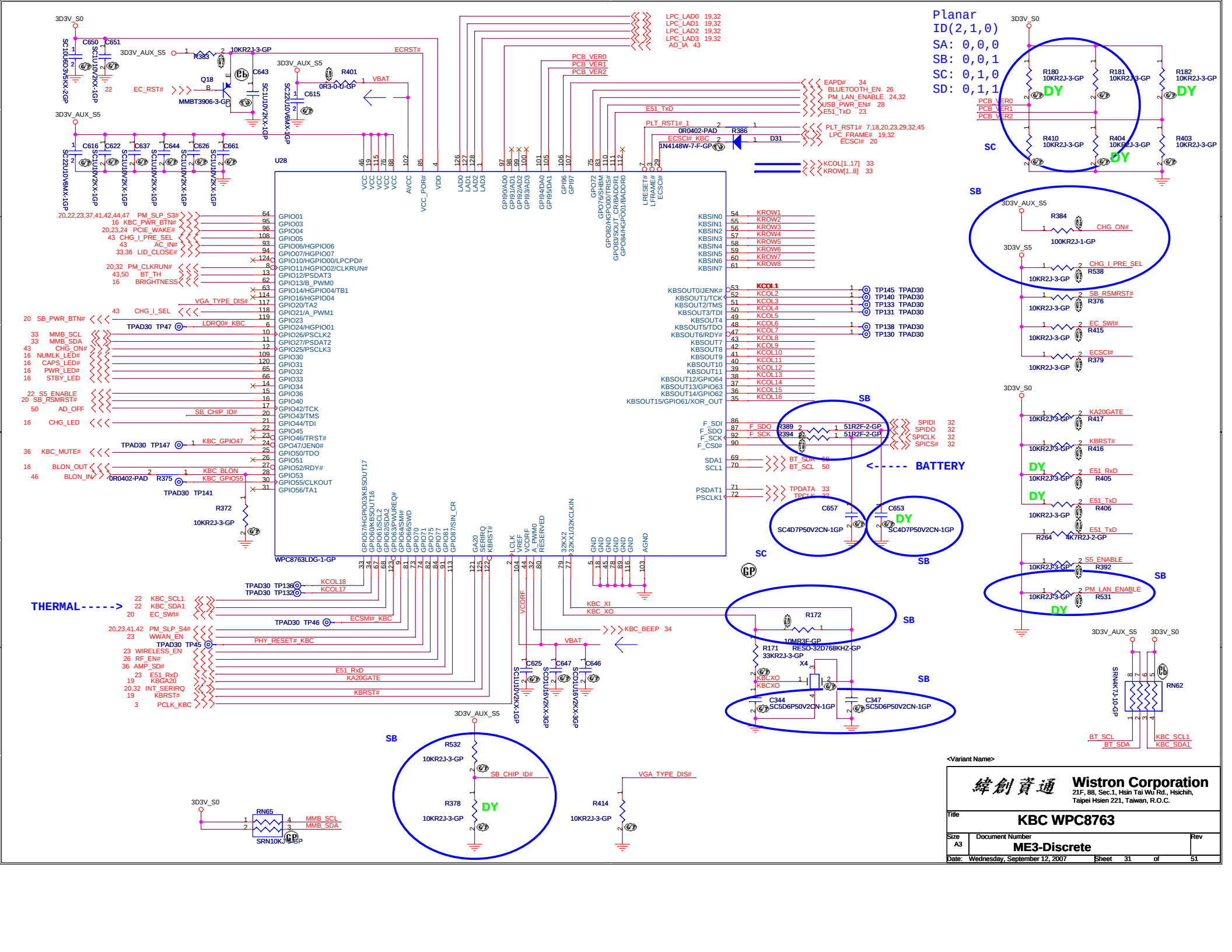


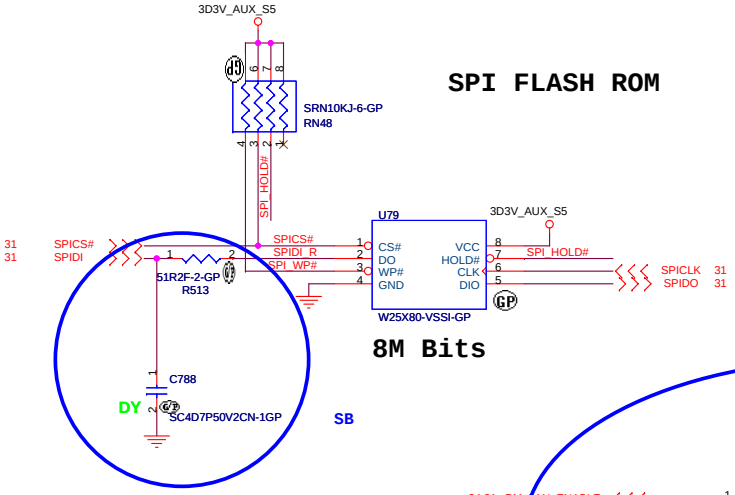


<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

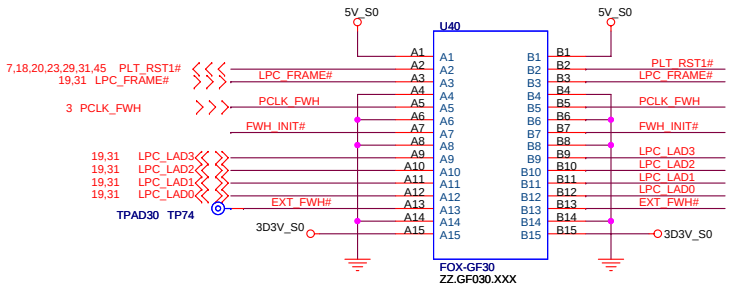
Title	HD/CDROM	
Size A3	Document Number ME3-Discrete	Rev
Date: Wednesday, August 15, 2007	Sheet 30 of 51	


Planar ID(2,1,0)
SA: 0,0,0
SB: 0,0,1
SC: 0,1,0
SD: 0,1,1
WPC8763LDG-1GP
U28
THERMAL
BATTERY
SB
SC
DY
GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC8763
ME3-Discrete
Wednesday, September 12, 2007
Sheet 31 of 51

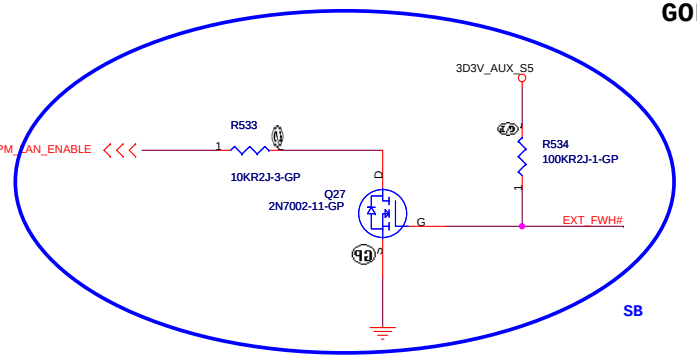


SPI FLASH ROM

8M Bits



GOLDEN FINGER FOR DEBUG BOARD

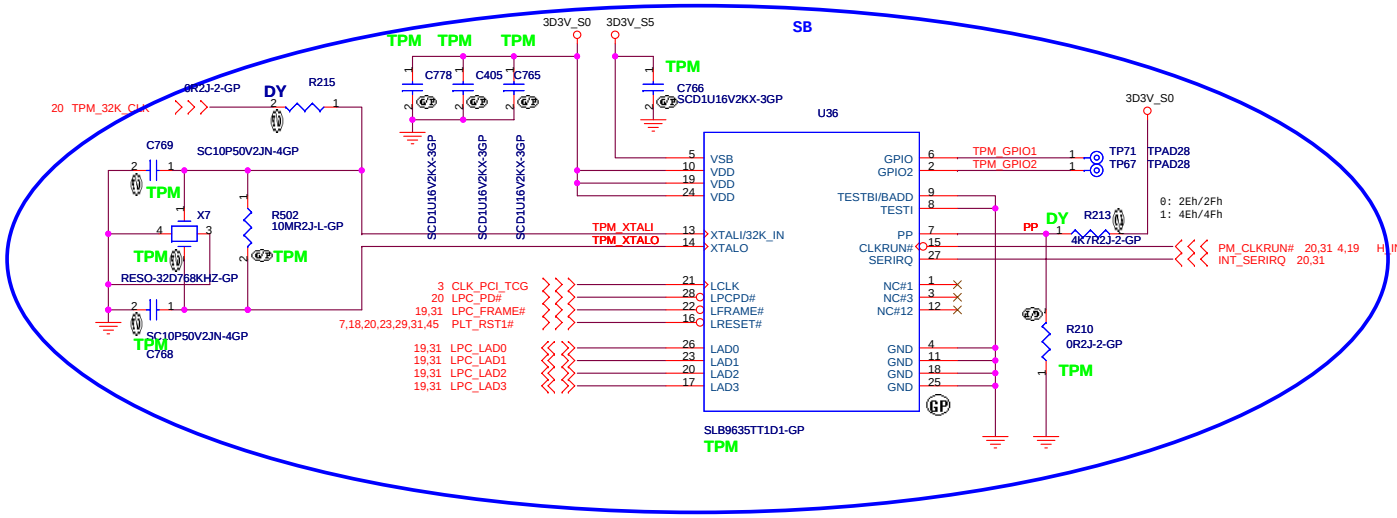


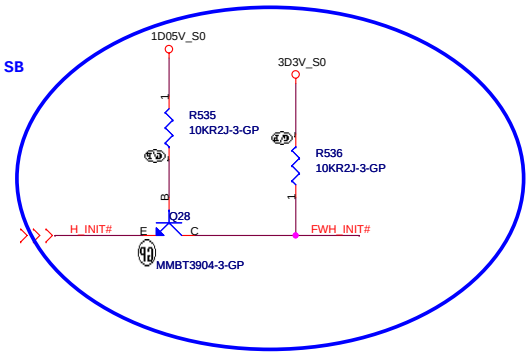
TOP VIEW

A15	(B1)
A14	(B2)
⋮	
A2	(B14)
A1	(B15)

(BOTTOM VIEW)

TPM 1.2



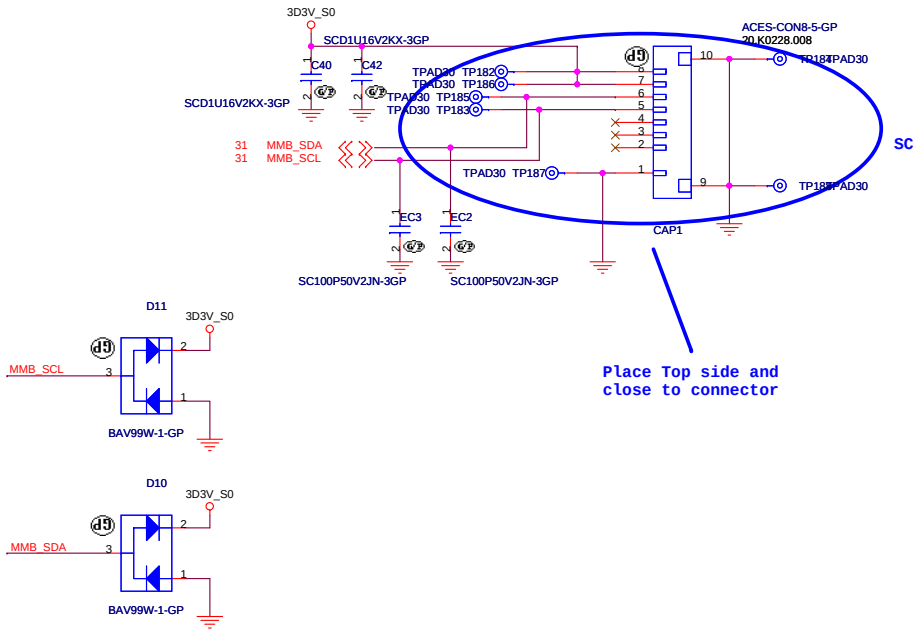


<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

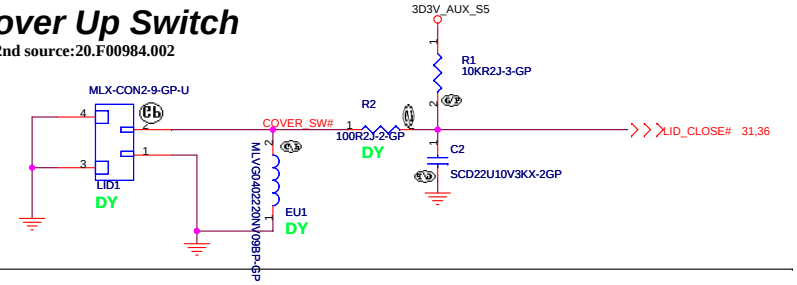
Title: BIOS
Size: A3 | Document Number: ME3-Discrete | Rev:
Date: Thursday, August 23, 2007 | Sheet 32 of 51

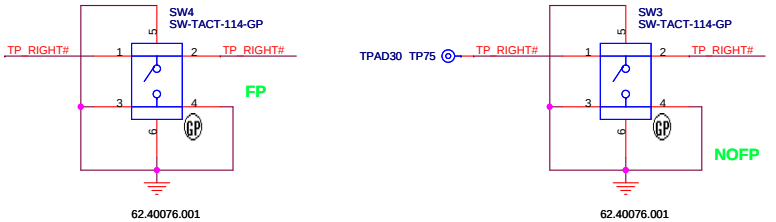
CAPACITY BUTTON

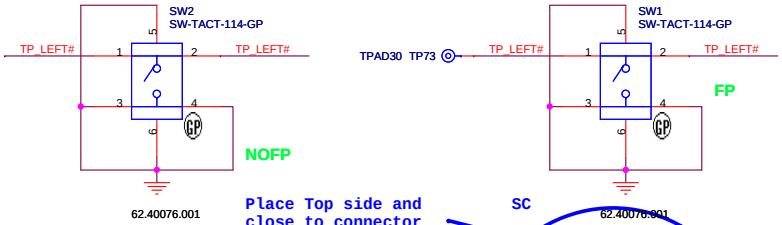


Cover Up Switch

2nd source:20.F00984.002

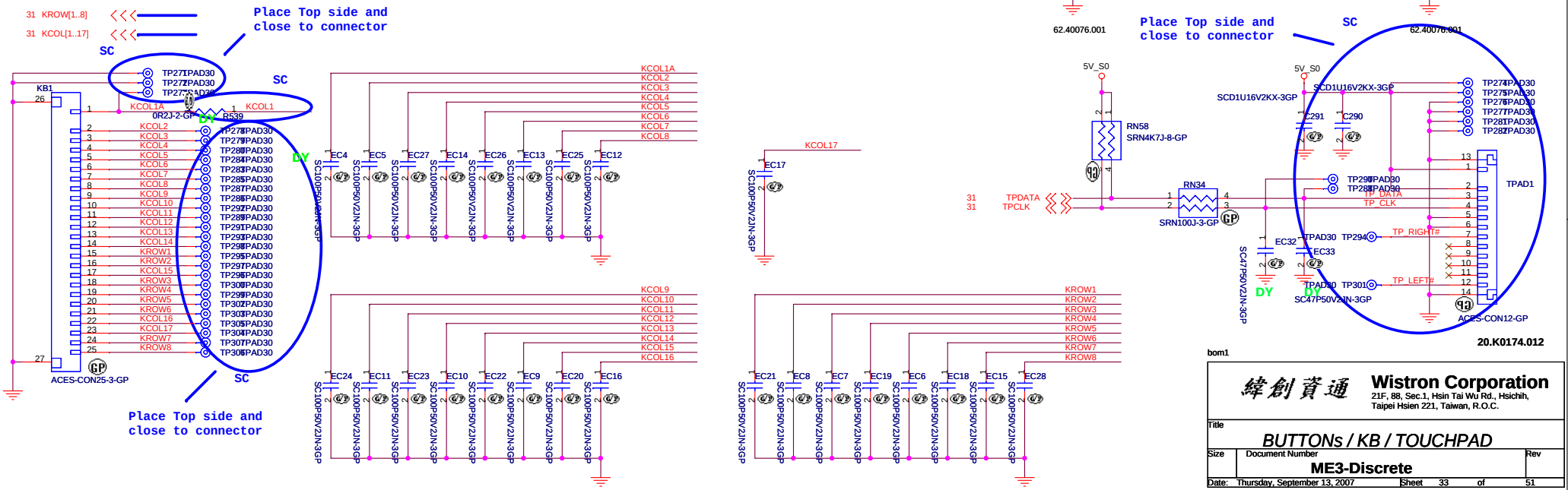






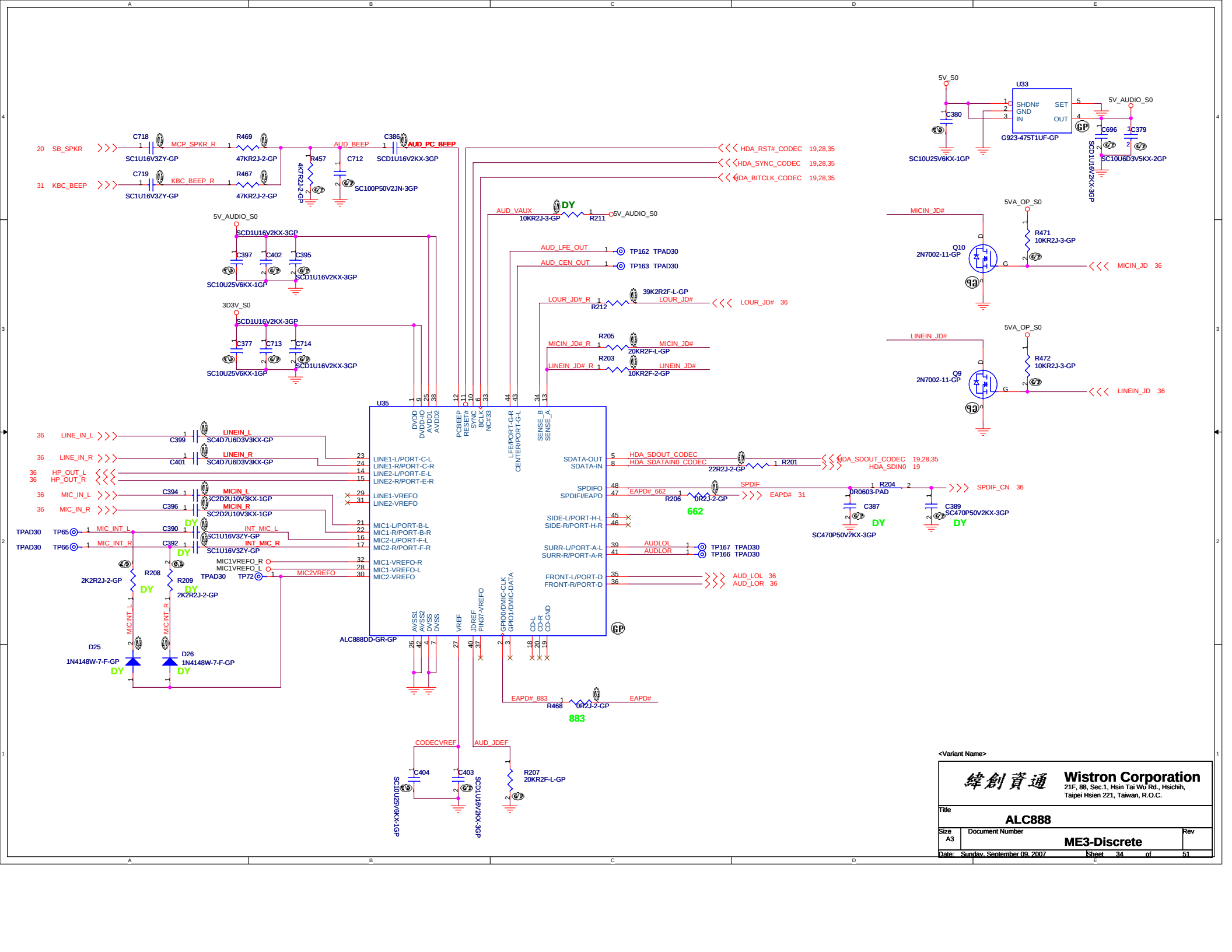
Internal KeyBoard CONN

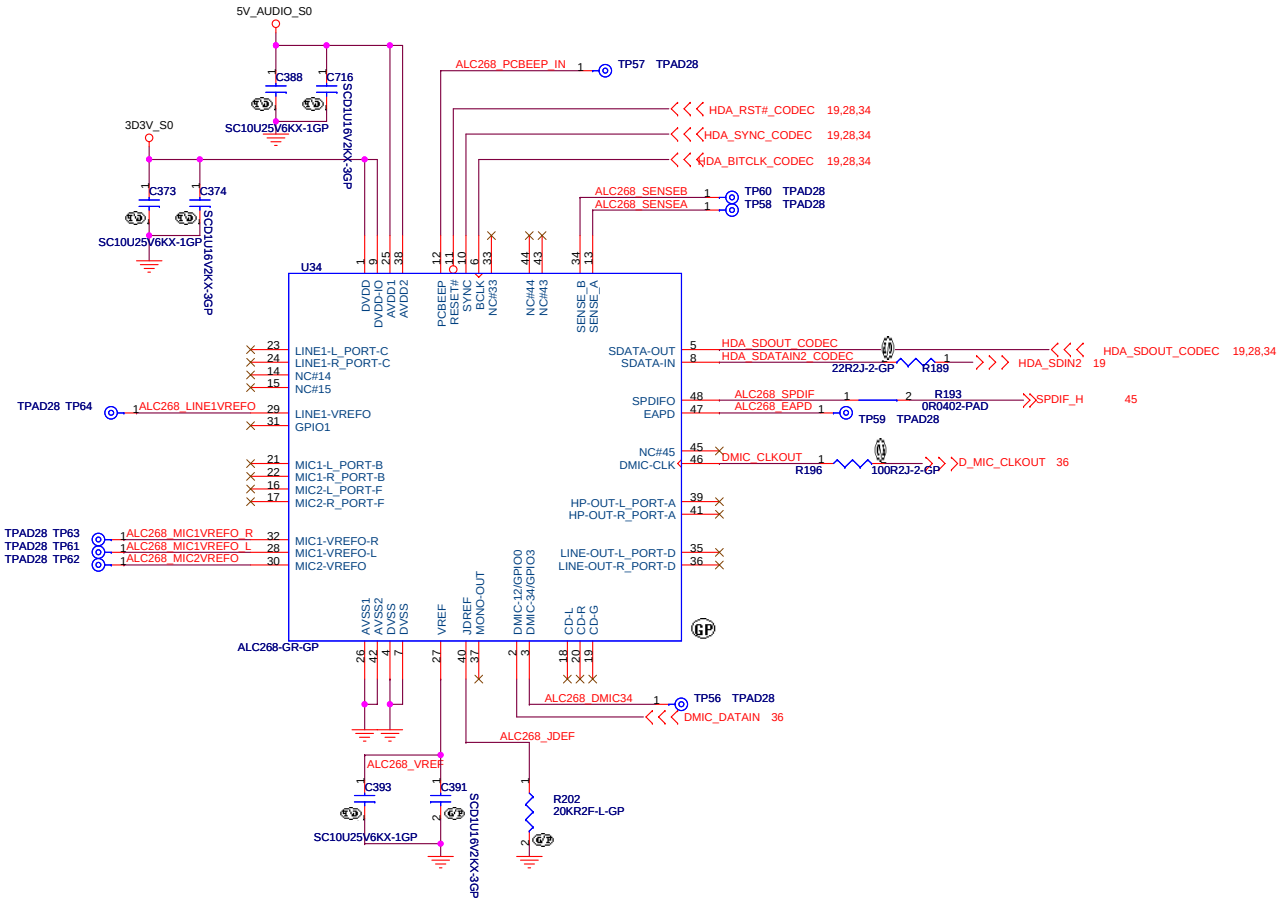
EMI Bypass cap.



bom1

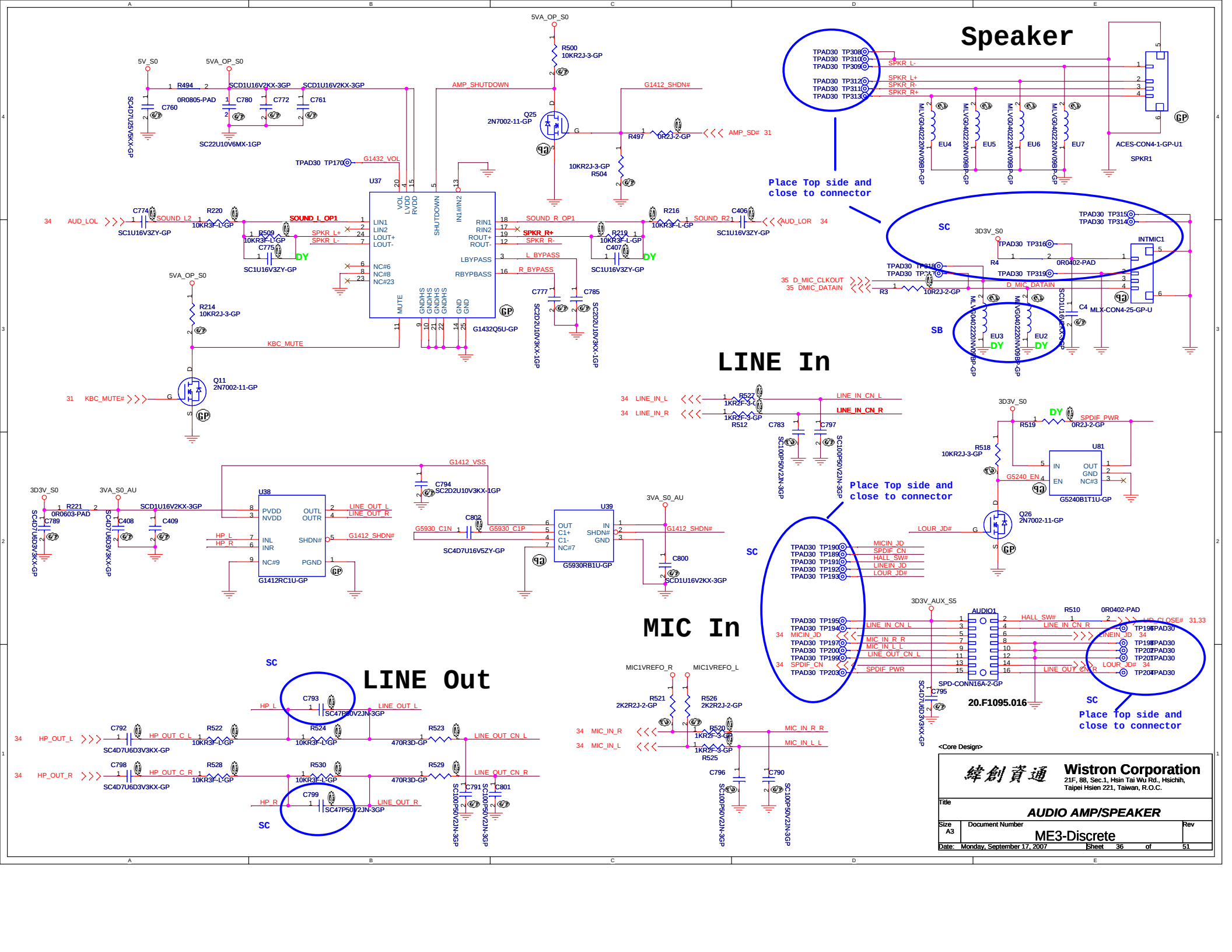
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*BUTTONs / KB / TOUCHPAD*	
Size	Document Number **ME3-Discrete**	Rev
Date: Thursday, September 13, 2007	Sheet 33 of 51	


U33
SHDN#
GND
IN
SET
OUT
G923-475T1UF-GP
5V_S0
5V_AUDIO_S0
SC10U25V6KX-1GP
SC10U6D3V5KX-2GP
SCD1U16V2KX-3GP
C380
C696
C379
20 SB_SPKR
31 KBC_BEEP
MCP_SPKR_R
KBC_BEEP_R
SC1U16V3ZY-GP
47KR2J-2-GP
4KR2J-2-GP
SC100P50V2JN-3GP
AUD_BEEP
AUD_PC_BEEP
HDA_RST#_CODEC 19,28,35
HDA_SYNC_CODEC 19,28,35
HDA_BITCLK_CODEC 19,28,35
AUD_VAUX
10KR2J-3-GP
R211
DY
AUD_LFE_OUT
AUD_CEN_OUT
TP162 TPAD30
TP163 TPAD30
LOUR_JD# 36
39K2R2F-L-GP
MICIN_JD# 36
LINEIN_JD# 36
20KR2F-L-GP
10KR2F-2-GP
2N7002-11-GP
Q10
Q9
R471
R472
10KR2J-3-GP
5VA_OP_S0
3D3V_S0
SCD1U16V2KX-3GP
SC10U25V6KX-1GP
U35
ALC888DD-GR-GP
DVDD
DVDD-IO
AVDD1
AVDD2
PCBEEP
RESET#
SYNC
BCLK
NC#33
LFE/PORT-G-R
CENTER/PORT-G-L
SENSE_B
SENSE_A
LINE1-L/PORT-C-L
LINE1-R/PORT-C-R
LINE2-L/PORT-E-L
LINE2-R/PORT-E-R
LINE1-VREFO
LINE2-VREFO
MIC1-L/PORT-B-L
MIC1-R/PORT-B-R
MIC2-L/PORT-F-L
MIC2-R/PORT-F-R
MIC1-VREFO-R
MIC1-VREFO-L
MIC2-VREFO
SDATA-OUT
SDATA-IN
HDA_SDOUT_CODEC
HDA_SDATAIN0_CODEC
HDA_SDOUT_CODEC 19,28,35
HDA_SDIN0 19
22R2J-2-GP
SPDIFO
SPDIF/EAPD
EAPD# 662
SPDIF
EAPD# 31
0R2J-2-GP
662
0R0603-PAD
SPDIF_CN 36
SC470P50V2KX-3GP
SIDE-L/PORT-H-L
SIDE-R/PORT-H-R
SURR-L/PORT-A-L
SURR-R/PORT-A-R
AUDLOL
AUDLOR
TP167 TPAD30
TP166 TPAD30
FRONT-L/PORT-D
FRONT-R/PORT-D
AUD_LOL 36
AUD_LOR 36
AVSS1
AVSS2
DVSS
DVSS
VREF
JDREF
PIN37-VREFO
GPIO0/DMIC-CLK
GPIO1/DMIC-DATA
CD-L
CD-R
CD-GND
EAPD# 883
0R2J-2-GP
883
CODECVREF
AUD_JDEF
SC10U25V6KX-1GP
SCD1U16V2KX-3GP
R207
20KR2F-L-GP
LINE_IN_L 36
LINE_IN_R 36
HP_OUT_L 36
HP_OUT_R 36
MIC_IN_L 36
MIC_IN_R 36
SC4D7U6D3V3KX-GP
SC2D2U10V3KX-1GP
LINEIN_L
LINEIN_R
MICIN_L
MICIN_R
MIC_INT_L
MIC_INT_R
INT_MIC_L
INT_MIC_R
TPAD30 TP65
TPAD30 TP66
TPAD30 TP72
MIC2VREFO
2K2R2J-2-GP
R208
R209
MICINT_L
MICINT_R
D25
D26
1N4148W-7-F-GP
DY
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ALC888
Size
A3
Document Number
ME3-Discrete
Rev
Date: Sunday, September 09, 2007
Sheet 34 of 51



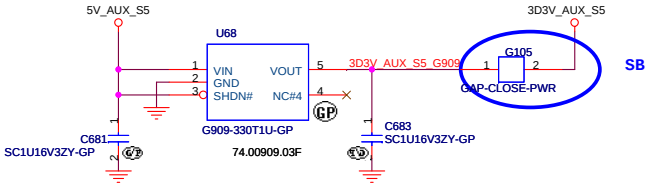
<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**CODEC ALC268**
Size A3 / Document Number	**ME3-Discrete** / Rev
Date: Sunday, September 09, 2007	Sheet 35 of 51

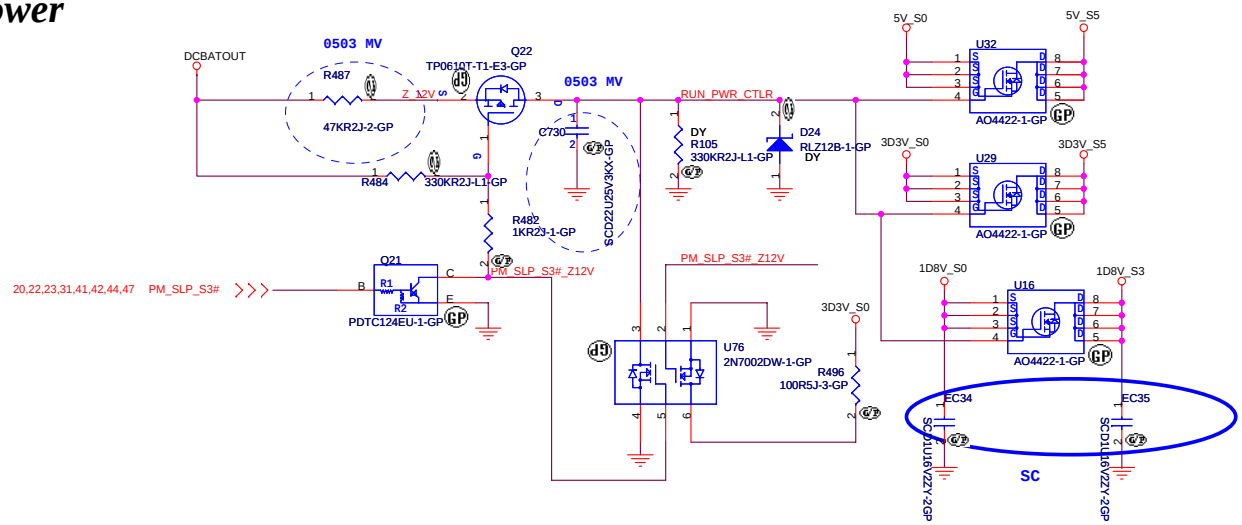

Speaker
LINE In
MIC In
LINE Out
Place Top side and close to connector
Place Top side and close to connector
Place Top side and close to connector
SC
SB
DY
U37
G1432Q5U-GP
U38
G1412RC1U-GP
U39
G5930RB1U-GP
U81
G5240B1T1U-GP
Q11
2N7002-11-GP
Q25
2N7002-11-GP
Q26
2N7002-11-GP
INTMIC1
MLX-CON4-25-GP-U
ACES-CON4-1-GP-U1
SPKR1
SPD-CONN16A-2-GP
AUDIO1
20.F1095.016
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
AUDIO AMP/SPEAKER
ME3-Discrete
Size A3
Document Number
Rev
Date: Monday, September 17, 2007
Sheet 36 of 51

5V_AUX_S5 TO 3D3V_AUX_S5

Aux Power 3D3V_AUX_S5

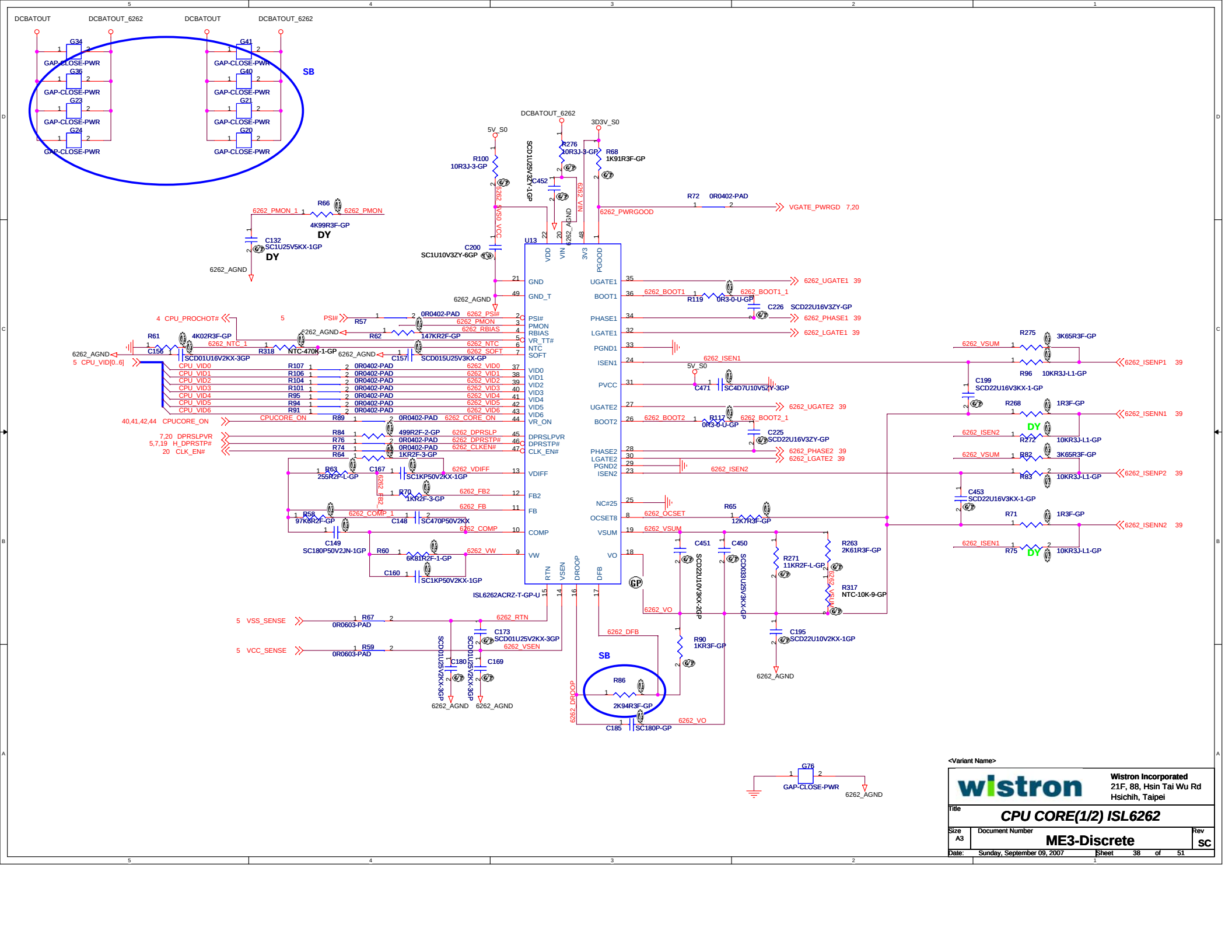


Run Power



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***PWRPLANE&RESETLOGIC***		
Size: A3	Document Number: **ME3-Discrete**	Rev:
Date: Wednesday, September 19, 2007	Sheet 37 of 51	



<Variant Name>

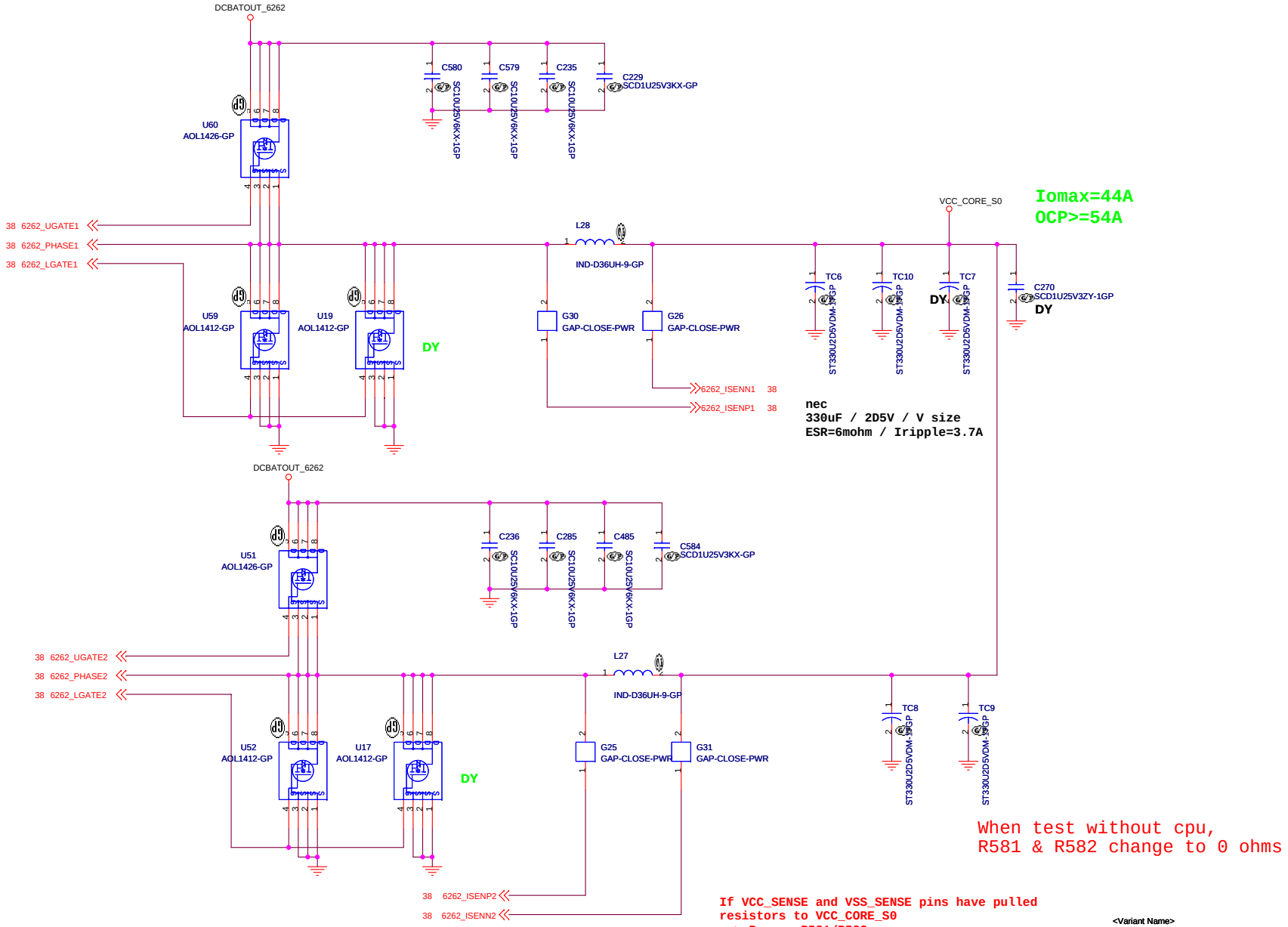
wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CPU CORE(1/2) ISL6262

Size	Document Number	Rev
A3	ME3-Discrete	SC

Date: Sunday, September 09, 2007 Sheet 38 of 51



<Variant Name>

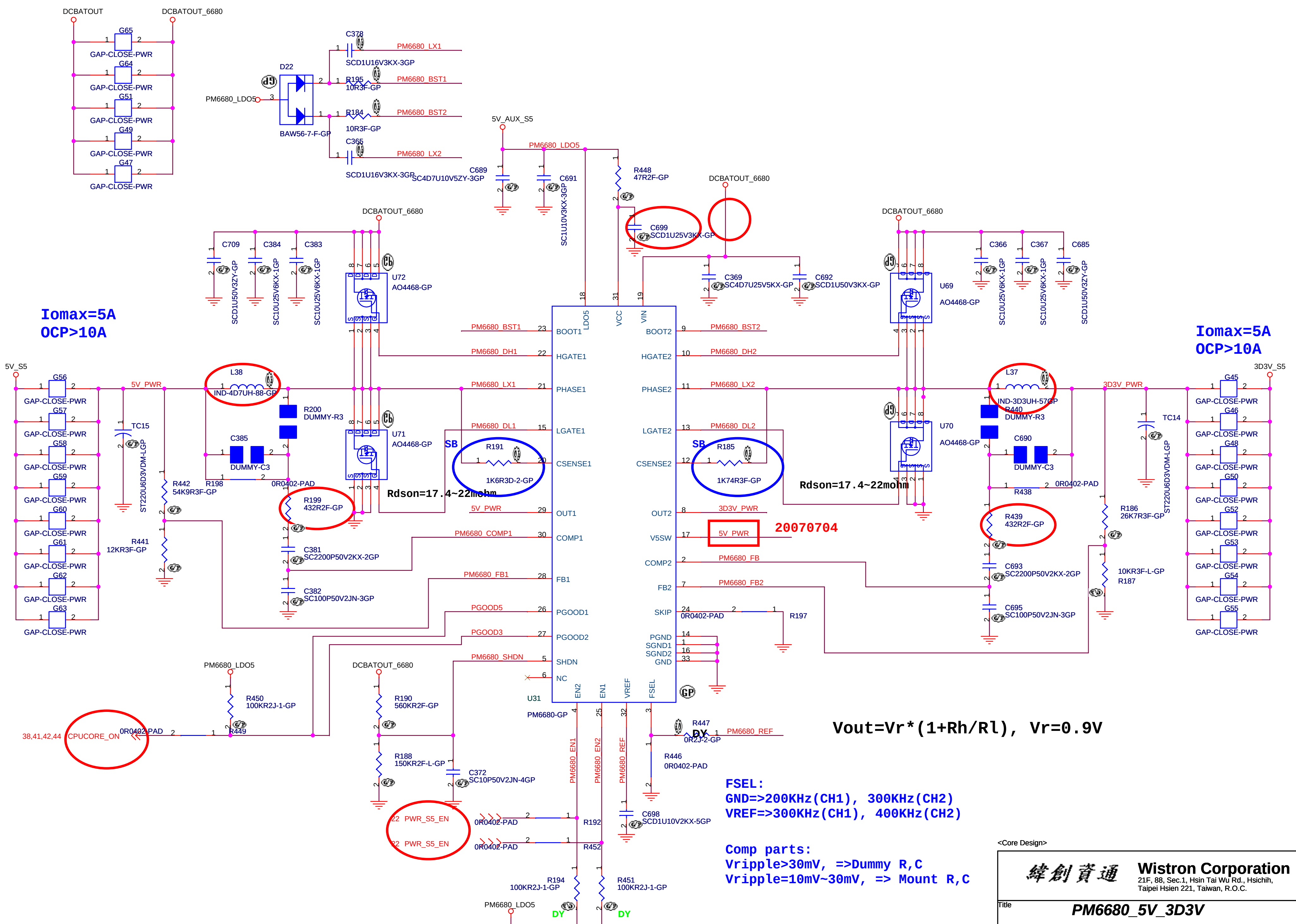
wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CPU CORE(2/2) ISL6262

Size: A3 | Document Number: ME3-Discrete | Rev: SC

Date: Wednesday, August 15, 2007 | Sheet 39 of 51


DCBATOUT
DCBATOUT_6680
GAP-CLOSE-PWR
PM6680_LDO5
D22
BAW56-7-F-GP
C378
SCD1U16V3KX-3GP
R195
10R3F-GP
R184
10R3F-GP
C365
PM6680_LX1
PM6680_BST1
PM6680_BST2
PM6680_LX2
5V_AUX_S5
C689
SC4D7U10V5ZY-3GP
C691
SC1U10V3KX-3GP
R448
47R2F-GP
C699
SCD1U25V3KX-GP
C369
SC4D7U25V5KX-GP
C692
SCD1U50V3KX-GP
C709
C384
C383
SCD1U50V3ZY-GP
SC10U25V6KX-1GP
U72
AO4468-GP
U69
C366
C367
C685
Iomax=5A
OCP>10A
5V_S5
3D3V_S5
5V_PWR
3D3V_PWR
L38
IND-4D7UH-88-GP
L37
IND-3D3UH-57GP
R200
DUMMY-R3
R440
TC15
TC14
ST220U6D3VDM-LGP
C385
DUMMY-C3
C690
U71
AO4468-GP
U70
SB
R191
1K6R3D-2-GP
R185
1K74R3F-GP
R442
54K9R3F-GP
R198
0R0402-PAD
R438
R199
432R2F-GP
R439
Rdson=17.4~22mohm
R441
12KR3F-GP
R186
26K7R3F-GP
C381
SC2200P50V2KX-2GP
C693
C382
SC100P50V2JN-3GP
C695
R187
10KR3F-L-GP
20070704
BOOT1
HGATE1
PHASE1
LGATE1
CSENSE1
OUT1
COMP1
FB1
PGOOD1
PGOOD2
SHDN
NC
LDO5
VCC
VIN
BOOT2
HGATE2
PHASE2
LGATE2
CSENSE2
OUT2
V5SW
COMP2
FB2
SKIP
PGND
SGND1
SGND2
GND
EN2
EN1
VREF
FSEL
U31
PM6680-GP
PM6680_DH1
PM6680_DL1
PM6680_DH2
PM6680_DL2
PM6680_COMP1
PM6680_FB1
PM6680_FB
PM6680_FB2
PGOOD5
PGOOD3
PM6680_SHDN
R197
R450
100KR2J-1-GP
R449
38,41,42,44
CPUCORE_ON
R190
560KR2F-GP
R188
150KR2F-L-GP
C372
SC10P50V2JN-4GP
R447
DY
0R2J-2-GP
PM6680_REF
R446
0R0402-PAD
C698
SCD1U10V2KX-5GP
22 PWR_S5_EN
R192
R452
PM6680_EN1
PM6680_EN2
R194
100KR2J-1-GP
R451

Vout=Vr*(1+Rh/Rl), Vr=0.9V

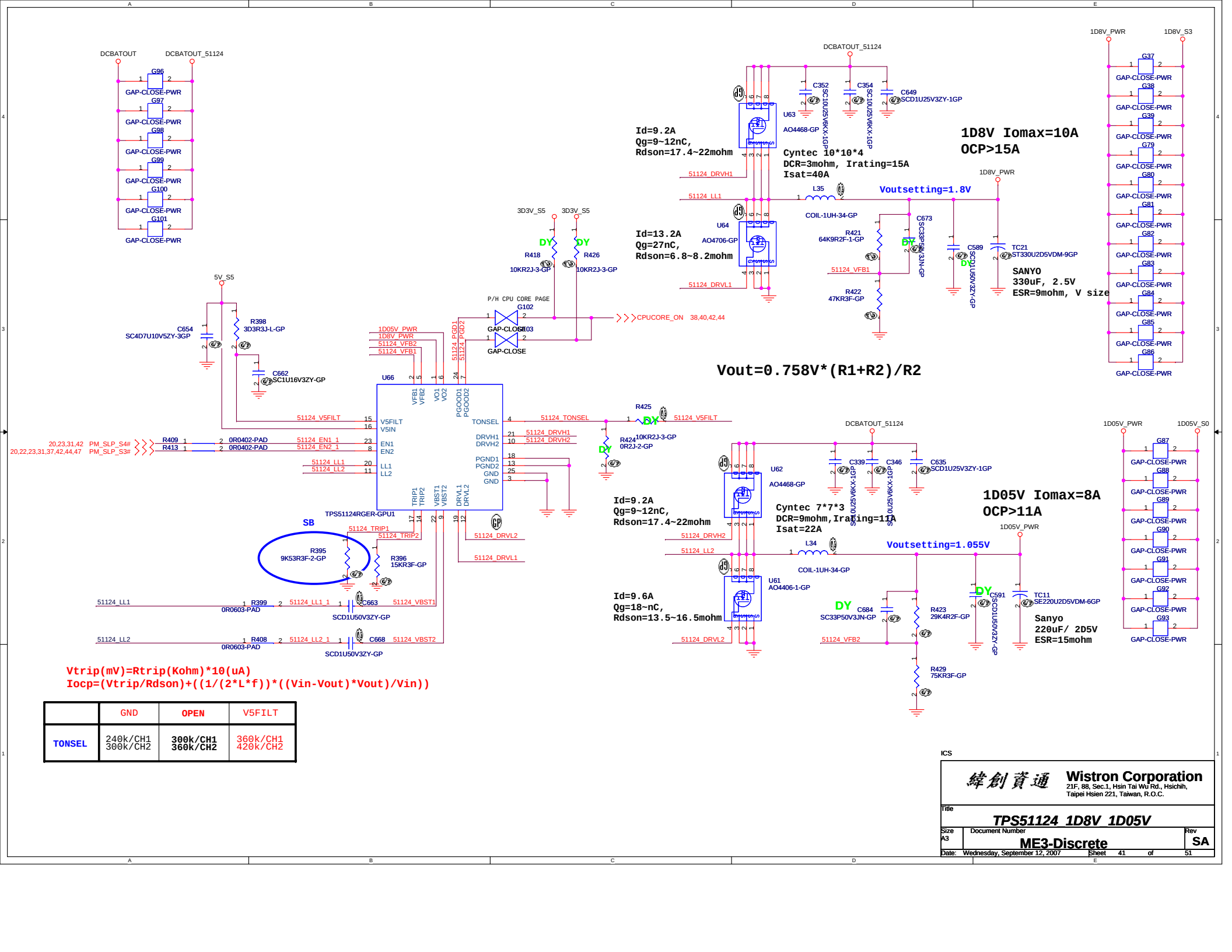
FSEL:
GND=>200KHz(CH1), 300KHz(CH2)
VREF=>300KHz(CH1), 400KHz(CH2)

Comp parts:
Vripple>30mV, =>Dummy R,C
Vripple=10mV~30mV, => Mount R,C

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	PM6680_5V_3D3V
Size: Custom	Document Number: ME3-Discrete	Rev
Date: Sunday, September 09, 2007	Sheet 40 of 51



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	**300k/CH1** **360k/CH2**	360k/CH1 420k/CH2

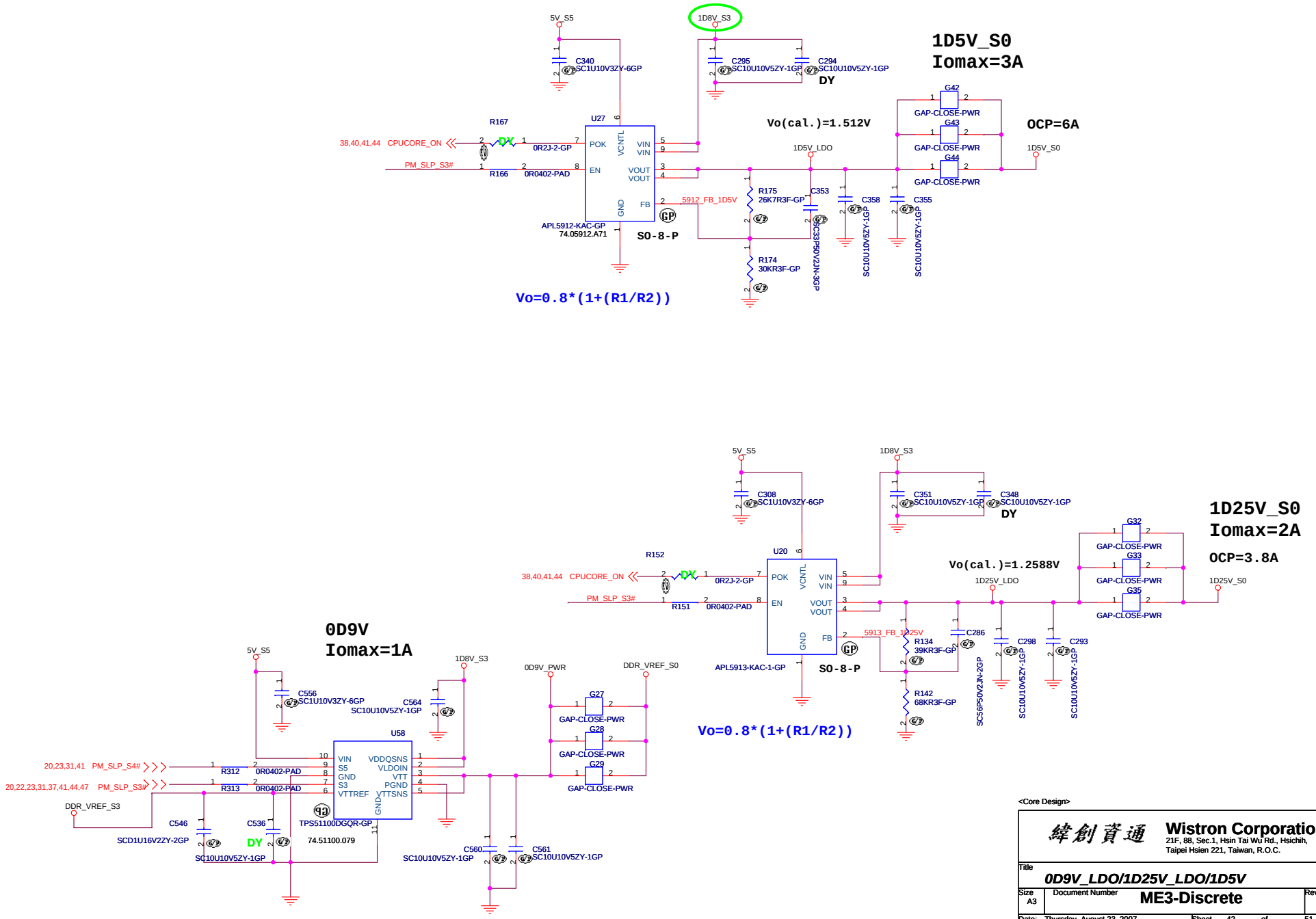
ICS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124_1D8V_1D05V

Size: A3 | Document Number: ME3-Discrete | Rev: SA

Date: Wednesday, September 12, 2007 | Sheet 41 of 51



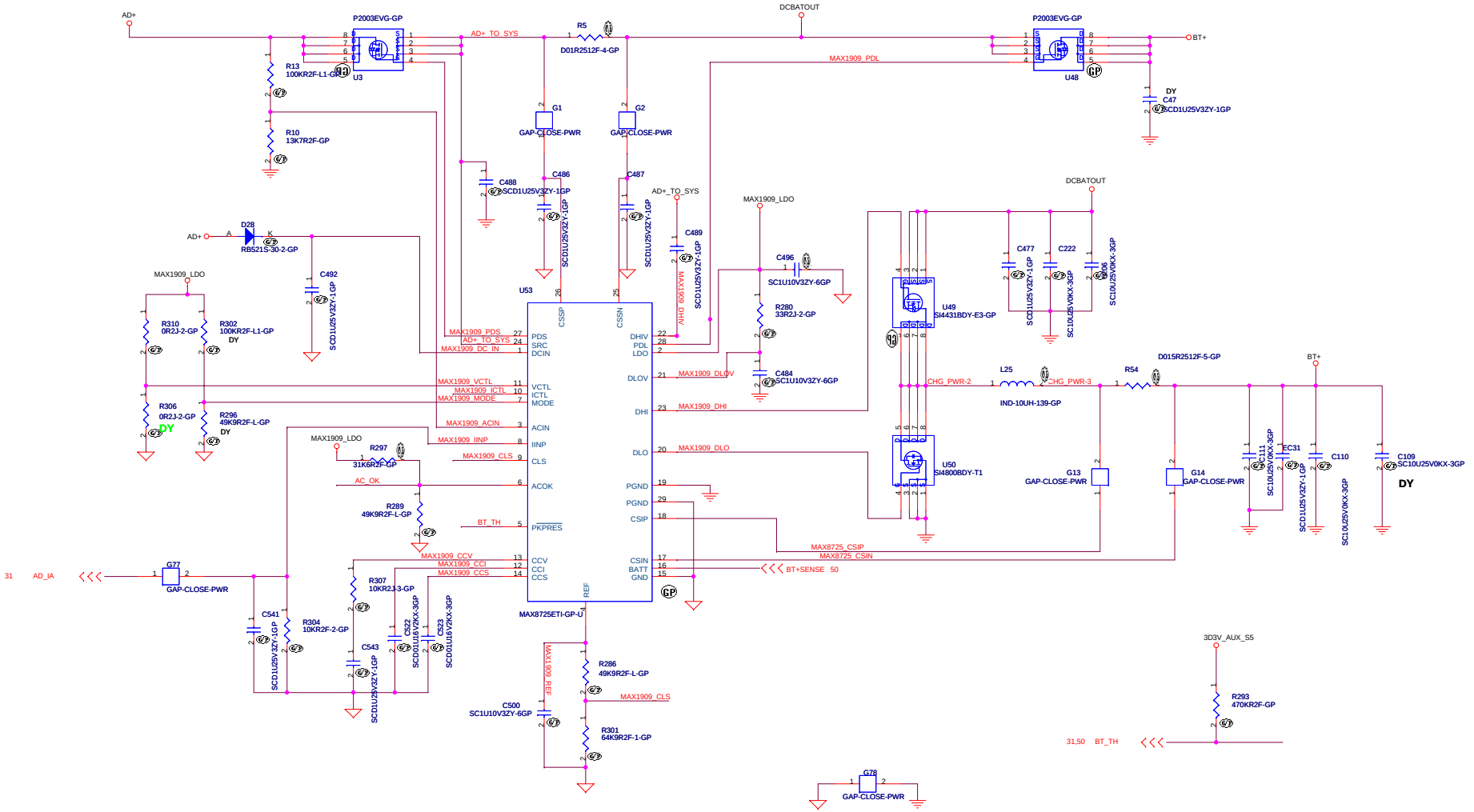
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 0D9V_LDO/1D25V_LDO/1D5V

Size	Document Number	Rev
A3	ME3-Discrete	

Date: Thursday, August 23, 2007 Sheet 42 of 51



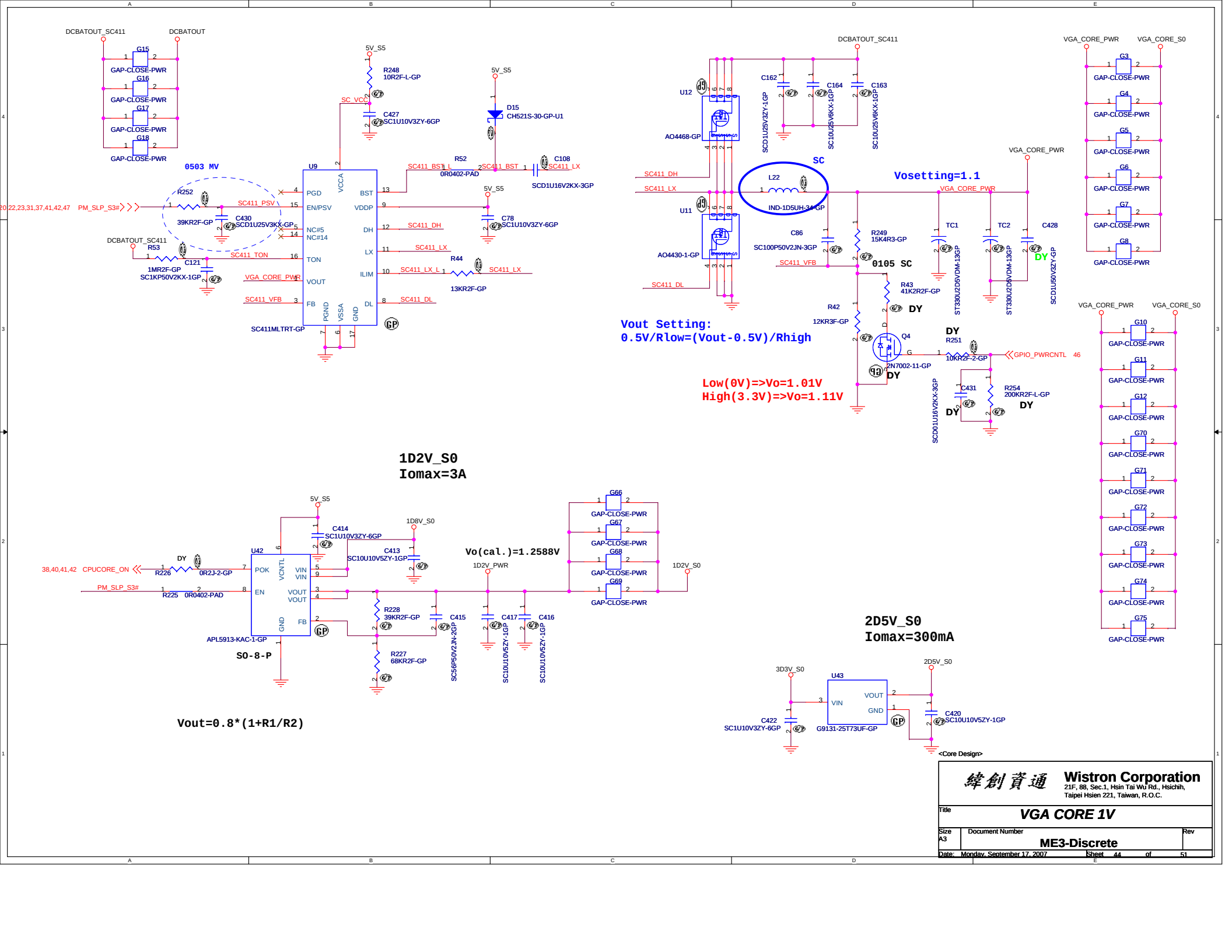
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

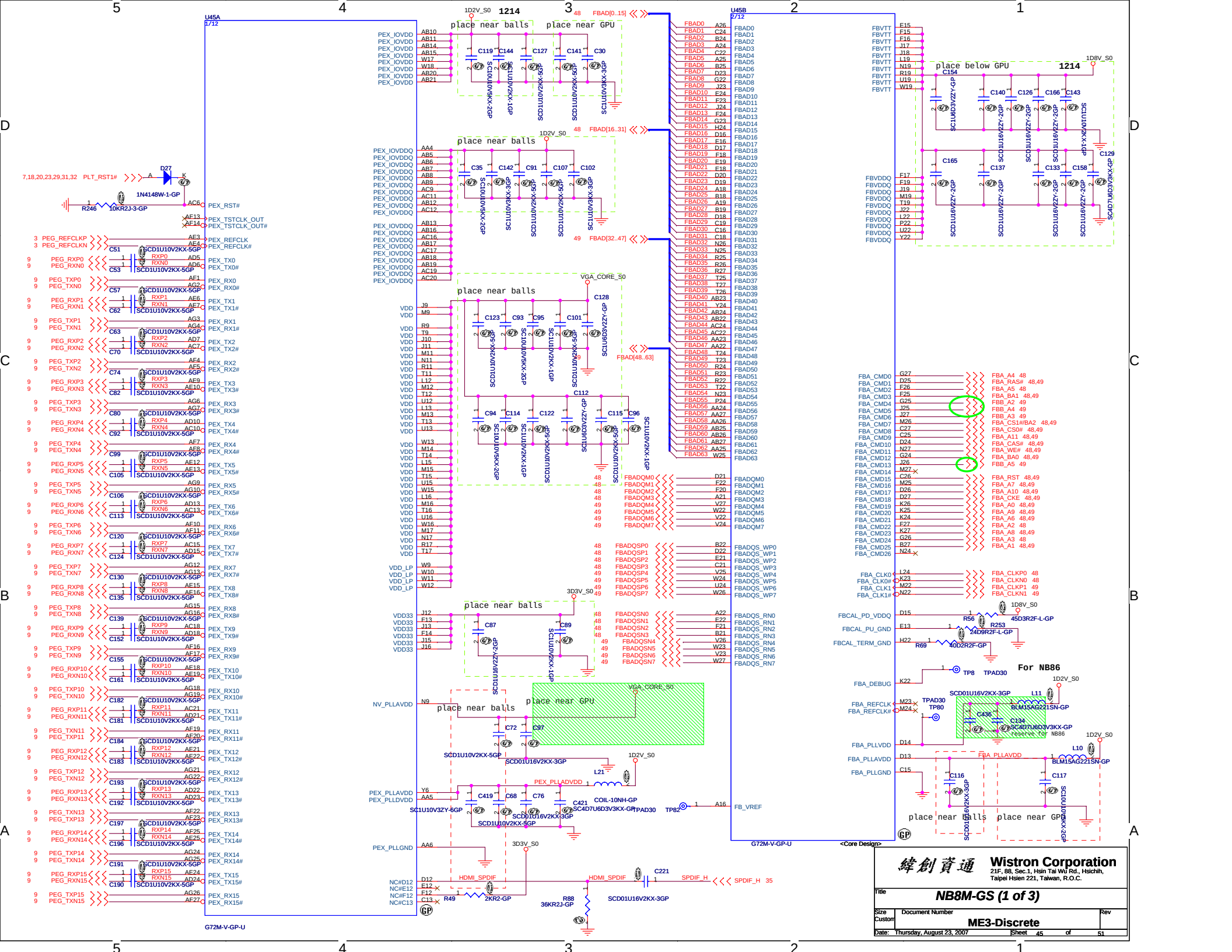
Title: CHARGER MAX8725ETI

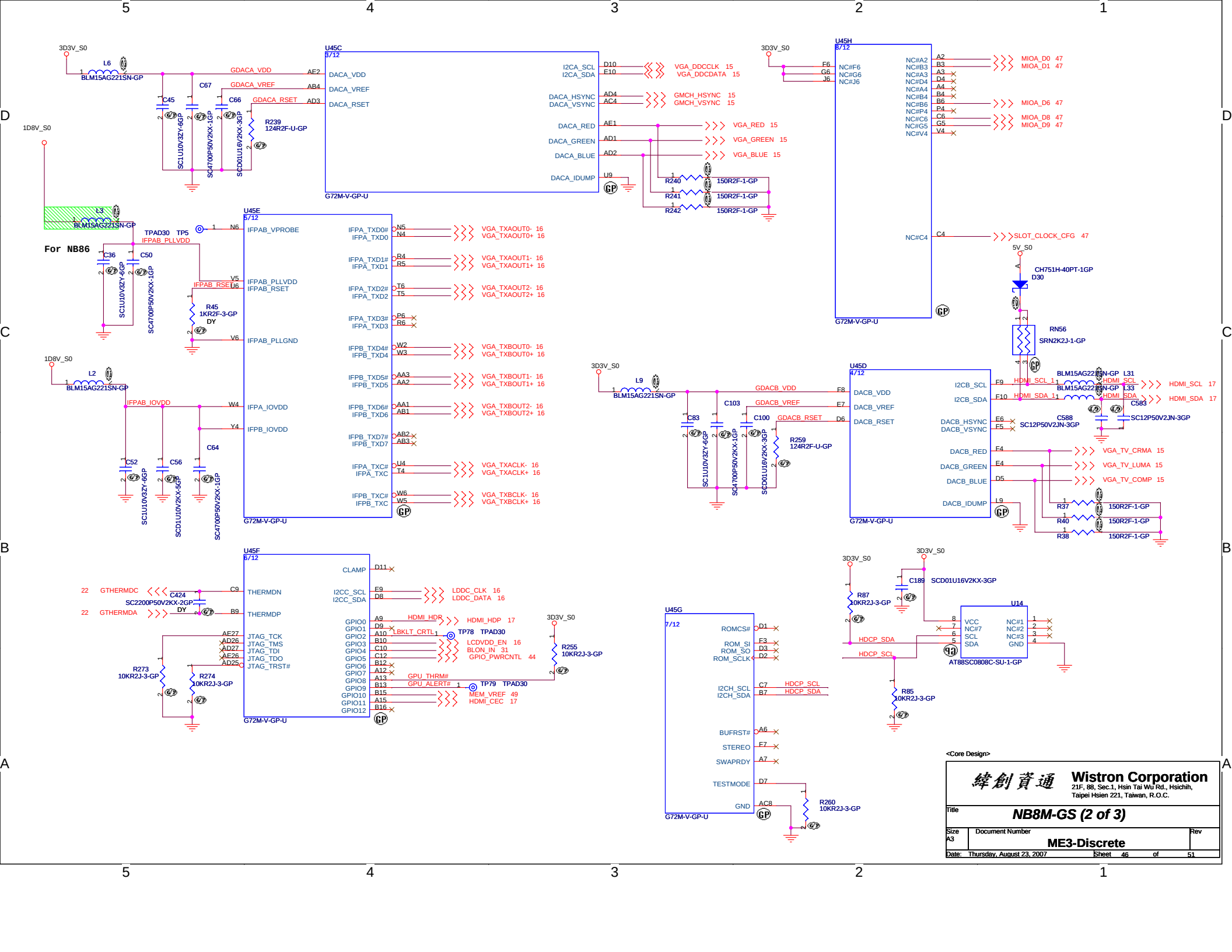
Size	Document Number	Rev
C	ME3-Discrete	

Date: Wednesday, September 19, 2007 Sheet 43 of 51



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***VGA CORE 1V***
Size A3	Document Number: **ME3-Discrete** Rev
Date: Monday, September 17, 2007	Sheet 44 of 51


U45A
1/12
U45B
2/12
place near balls
place near GPU
place below GPU
1214
1D2V_S0
1D8V_S0
3D3V_S0
VGA_CORE_S0
PEX_RST#
PEX_TSTCLK_OUT
PEX_TSTCLK_OUT#
PEX_REFCLK
PEX_REFCLK#
PEX_TX0
PEX_TX0#
PEX_RX0
PEX_RX0#
PEX_TX1
PEX_TX1#
PEX_RX1
PEX_RX1#
PEX_TX2
PEX_TX2#
PEX_RX2
PEX_RX2#
PEX_TX3
PEX_TX3#
PEX_RX3
PEX_RX3#
PEX_TX4
PEX_TX4#
PEX_RX4
PEX_RX4#
PEX_TX5
PEX_TX5#
PEX_RX5
PEX_RX5#
PEX_TX6
PEX_TX6#
PEX_RX6
PEX_RX6#
PEX_TX7
PEX_TX7#
PEX_RX7
PEX_RX7#
PEX_TX8
PEX_TX8#
PEX_RX8
PEX_RX8#
PEX_TX9
PEX_TX9#
PEX_RX9
PEX_RX9#
PEX_TX10
PEX_TX10#
PEX_RX10
PEX_RX10#
PEX_TX11
PEX_TX11#
PEX_RX11
PEX_RX11#
PEX_TX12
PEX_TX12#
PEX_RX12
PEX_RX12#
PEX_TX13
PEX_TX13#
PEX_RX13
PEX_RX13#
PEX_TX14
PEX_TX14#
PEX_RX14
PEX_RX14#
PEX_TX15
PEX_TX15#
PEX_RX15
PEX_RX15#
FBAD[0..15]
FBAD[16..31]
FBAD[32..47]
FBAD[48..63]
FBADQM0
FBADQM1
FBADQM2
FBADQM3
FBADQM4
FBADQM5
FBADQM6
FBADQM7
FBADQS_WP0
FBADQS_WP1
FBADQS_WP2
FBADQS_WP3
FBADQS_WP4
FBADQS_WP5
FBADQS_WP6
FBADQS_WP7
FBADQS_RN0
FBADQS_RN1
FBADQS_RN2
FBADQS_RN3
FBADQS_RN4
FBADQS_RN5
FBADQS_RN6
FBADQS_RN7
FBA_A4
FBA_RAS#
FBA_A5
FBA_BA1
FBB_A2
FBB_A4
FBB_A3
FBA_CS1#/BA2
FBA_CS0#
FBA_A11
FBA_CAS#
FBA_WE#
FBA_BA0
FBB_A5
FBA_RST
FBA_A7
FBA_A10
FBA_CKE
FBA_A0
FBA_A9
FBA_A6
FBA_A2
FBA_A8
FBA_A3
FBA_A1
FBA_CLKP
FBA_CLKN
FBA_CLK0
FBA_CLK0#
FBA_CLK1
FBA_CLK1#
FBCAL_PD_VDDQ
FBCAL_PU_GND
FBCAL_TERM_GND
FBA_DEBUG
FBA_REFCLK
FBA_REFCLK#
FBA_PLLVDD
FBA_PLLAVDD
FBA_PLLGND
FB_VREF
PEX_PLLADVDD
PEX_PLLDVDD
PEX_PLLGND
NV_PLLAVDD
HDMI_SPDIF
SPDIF_H
For NB86
Reserve for NB86
<Core Design>
G72M-V-GP-U
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
NB8M-GS (1 of 3)
ME3-Discrete
Thursday, August 23, 2007
45
51


U45C
6/12
G72M-V-GP-U
U45H
6/12
G72M-V-GP-U
U45E
6/12
G72M-V-GP-U
U45D
4/12
G72M-V-GP-U
U45F
6/12
G72M-V-GP-U
U45G
7/12
G72M-V-GP-U
U14
AT88SC0808C-SU-1-GP
For NB86
3D3V_S0
1D8V_S0
5V_S0
L6
BLM15AG221SN-GP
L3
BLM15AG221SN-GP
L2
BLM15AG221SN-GP
L9
BLM15AG221SN-GP
L31
BLM15AG221SN-GP
L33
BLM15AG221SN-GP
C45
SC1U10V3ZY-6GP
C67
SC4700P50V2KX-1GP
C66
SCD01U16V2KX-3GP
C36
SC1U10V3ZY-6GP
C50
SC4700P50V2KX-1GP
C52
SC1U10V3ZY-6GP
C56
SCD1U10V2KX-5GP
C64
SC4700P50V2KX-1GP
C83
SC1U10V3ZY-6GP
C103
SC4700P50V2KX-1GP
C100
SCD01U16V2KX-3GP
C424
SC2200P50V2KX-2GP
C189
SCD01U16V2KX-3GP
C583
SC12P50V2JN-3GP
C588
SC12P50V2JN-3GP
R239
124R2F-U-GP
R240
150R2F-1-GP
R241
150R2F-1-GP
R242
150R2F-1-GP
R45
1KR2F-3-GP
DY
R259
124R2F-U-GP
R37
150R2F-1-GP
R40
150R2F-1-GP
R38
150R2F-1-GP
R273
10KR2J-3-GP
R274
10KR2J-3-GP
R255
10KR2J-3-GP
R87
10KR2J-3-GP
R85
10KR2J-3-GP
R260
10KR2J-3-GP
RN56
SRN2K2J-1-GP
D30
CH751H-40PT-1GP
TPAD30
TP5
TP78
TPAD30
TP79
TPAD30
I2CA_SCL
I2CA_SDA
DACA_VDD
DACA_VREF
DACA_RSET
DACA_HSYNC
DACA_VSYNC
DACA_RED
DACA_GREEN
DACA_BLUE
DACA_IDUMP
VGA_DDCCLK 15
VGA_DDCDATA 15
GMCH_HSYNC 15
GMCH_VSYNC 15
VGA_RED 15
VGA_GREEN 15
VGA_BLUE 15
GDACA_VDD
GDACA_VREF
GDACA_RSET
IFPAB_VPROBE
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IFPAB_RSET
IFPAB_PLLGND
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IFPA_IOVDD
IFPB_IOVDD
IFPA_TXD0# IFPA_TXD0
IFPA_TXD1# IFPA_TXD1
IFPA_TXD2# IFPA_TXD2
IFPA_TXD3# IFPA_TXD3
IFPB_TXD4# IFPB_TXD4
IFPB_TXD5# IFPB_TXD5
IFPB_TXD6# IFPB_TXD6
IFPB_TXD7# IFPB_TXD7
IFPA_TXC# IFPA_TXC
IFPB_TXC# IFPB_TXC
VGA_TXAOUT0- 16
VGA_TXAOUT0+ 16
VGA_TXAOUT1- 16
VGA_TXAOUT1+ 16
VGA_TXAOUT2- 16
VGA_TXAOUT2+ 16
VGA_TXBOUT0- 16
VGA_TXBOUT0+ 16
VGA_TXBOUT1- 16
VGA_TXBOUT1+ 16
VGA_TXBOUT2- 16
VGA_TXBOUT2+ 16
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VGA_TXACLK+ 16
VGA_TXBCLK- 16
VGA_TXBCLK+ 16
NC#F6
NC#G6
NC#J6
NC#A2
NC#B3
NC#A3
NC#D4
NC#A4
NC#B4
NC#B6
NC#P4
NC#C6
NC#G5
NC#V4
MIOA_D0 47
MIOA_D1 47
MIOA_D6 47
MIOA_D8 47
MIOA_D9 47
NC#C4
SLOT_CLOCK_CFG 47
DACB_VDD
DACB_VREF
DACB_RSET
DACB_HSYNC
DACB_VSYNC
DACB_RED
DACB_GREEN
DACB_BLUE
DACB_IDUMP
I2CB_SCL
I2CB_SDA
HDMI_SCL 17
HDMI_SDA 17
VGA_TV_CRMA 15
VGA_TV_LUMA 15
VGA_TV_COMP 15
GDACB_VDD
GDACB_VREF
GDACB_RSET
CLAMP
THERMDN
THERMDP
GTHERMDC
GTHERMDA
I2CC_SCL
I2CC_SDA
LDDC_CLK 16
LDDC_DATA 16
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_TRST#
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8
GPIO9
GPIO10
GPIO11
GPIO12
HDMI_HDR
HDMI_HDP 17
LBKLT_CRTL
LCDVDD_EN 16
BLON_IN 31
GPIO_PWRCNTL 44
GPU_THRM#
GPU_ALERT#
MEM_VREF 49
HDMI_CEC 17
ROMCS#
ROM_SI
ROM_SO
ROM_SCLK
I2CH_SCL
I2CH_SDA
HDCP_SCL
HDCP_SDA
BUFRST#
STEREO
SWAPRDY
TESTMODE
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VCC
NC#7
SCL
SDA
NC#1
NC#2
NC#3
GND
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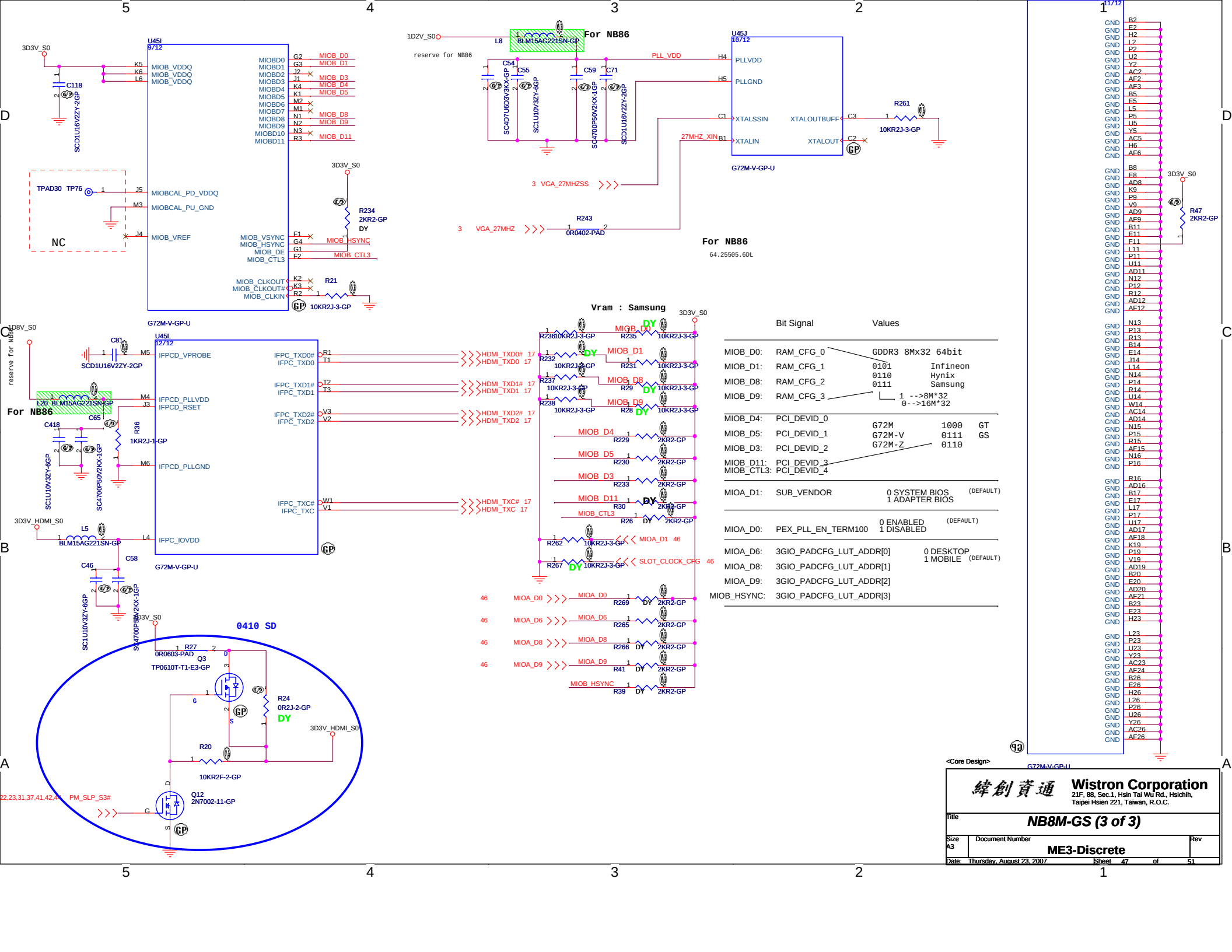
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
NB8M-GS (2 of 3)
Size
A3
Document Number
ME3-Discrete
Rev
Date: Thursday, August 23, 2007
Sheet 46 of 51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8/12
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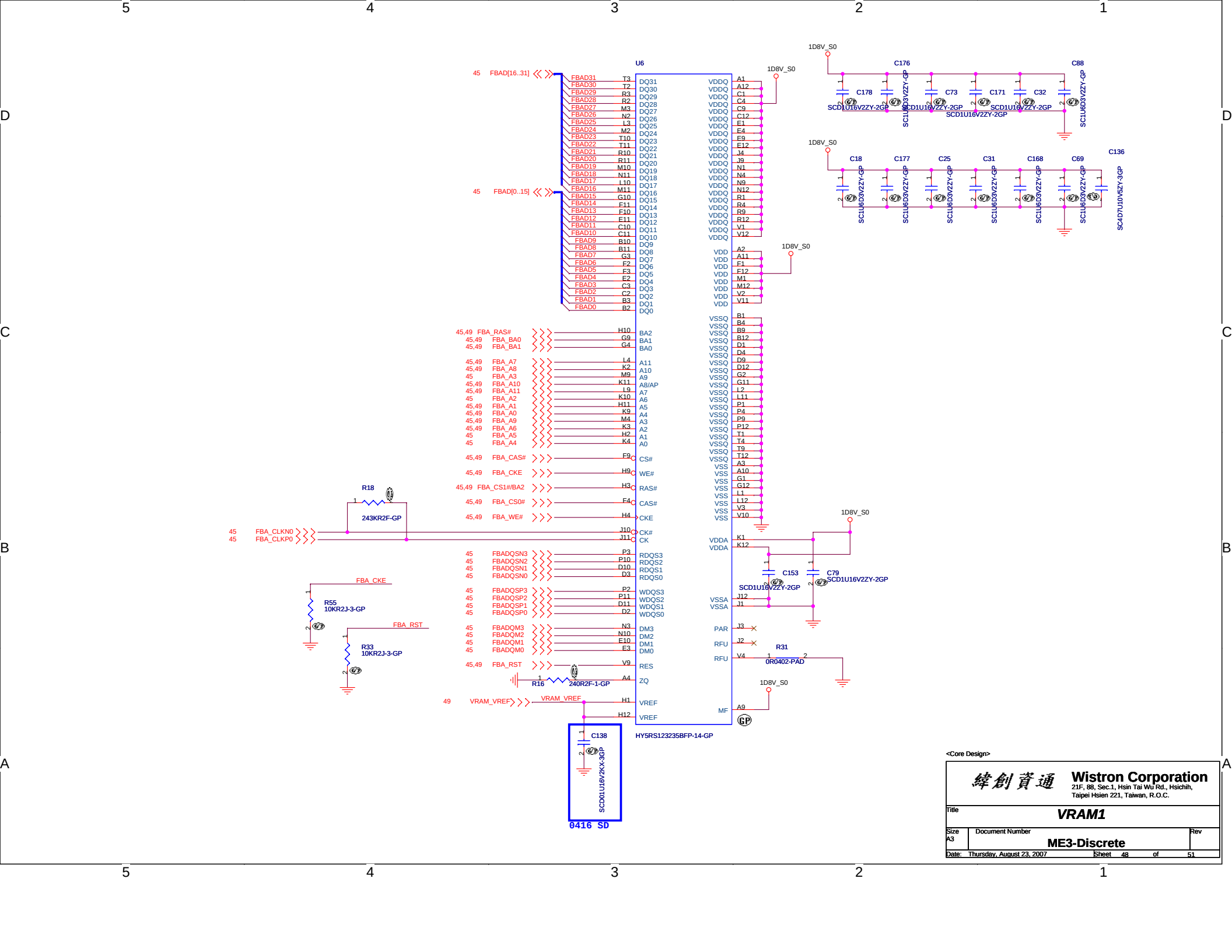
MIOBD2
MIOBD3
MIOBD4
MIOBD5
MIOBD6
MIOBD7
MIOBD8
MIOBD9
MIOBD10
MIOBD11
MIOB_D0
MIOB_D1
MIOB_D3
MIOB_D4
MIOB_D5
MIOB_D8
MIOB_D9
MIOB_D11
MIOB_VDDQ
MIOBCAL_PD_VDDQ
MIOBCAL_PU_GND
MIOB_VREF
MIOB_VSYNC
MIOB_HSYNC
MIOB_DE
MIOB_CTL3
MIOB_CLKOUT
MIOB_CLKOUT#
MIOB_CLKIN
3D3V_S0
SCD1U16V2ZY-2GP
TPAD30
TP76
NC
R234
2KR2-GP
DY
R21
10KR2J-3-GP
1D2V_S0
reserve for NB86
L8
BLM15AG221SN-GP
For NB86
C54
C55
C59
C71
SC4D7U6D3V3KX-GP
SC1U10V3ZY-6GP
SC4700P50V2KX-1GP
SCD1U16V2ZY-2GP
PLL_VDD
U45J
10/12
PLLVDD
PLLGND
XTALSSIN
XTALIN
XTALOUTBUFF
XTALOUT
G72M-V-GP-U
R261
10KR2J-3-GP
27MHZ_XIN
3 VGA_27MHZSS
3 VGA_27MHZ
R243
0R0402-PAD
For NB86
64.25505.6DL
11/12
GND
3D3V_S0
R47
2KR2-GP
1D8V_S0
reserve for NB86
L20 BLM15AG221SN-GP
For NB86
C81
SCD1U16V2ZY-2GP
C418
C65
R36
1KR2J-1-GP
SC1U10V3ZY-6GP
SC4700P50V2KX-1GP
U45L
12/12
IFPCD_VPROBE
IFPCD_PLLVDD
IFPCD_RSET
IFPCD_PLLGND
IFPC_TXD0#
IFPC_TXD0
IFPC_TXD1#
IFPC_TXD1
IFPC_TXD2#
IFPC_TXD2
IFPC_TXC#
IFPC_TXC
IFPC_IOVDD
HDMI_TXD0# 17
HDMI_TXD0 17
HDMI_TXD1# 17
HDMI_TXD1 17
HDMI_TXD2# 17
HDMI_TXD2 17
HDMI_TXC# 17
HDMI_TXC 17
G72M-V-GP-U
3D3V_HDMI_S0
L5
BLM15AG221SN-GP
C58
C46
SC1U10V3ZY-6GP
SA4700P50V2KX-1GP
Vram : Samsung
MIOB_D11
MIOB_D1
MIOB_D8
MIOB_D9
MIOB_D4
MIOB_D5
MIOB_D3
MIOB_D11
MIOB_CTL3
MIOA_D1 46
SLOT_CLOCK_CFG 46
MIOA_D0 46
MIOA_D6 46
MIOA_D8 46
MIOA_D9 46
MIOB_HSYNC
10KR2J-3-GP
2KR2-GP
DY
Bit Signal Values
MIOB_D0: RAM_CFG_0 GDDR3 8Mx32 64bit
MIOB_D1: RAM_CFG_1 0101 Infineon
MIOB_D8: RAM_CFG_2 0110 Hynix
MIOB_D9: RAM_CFG_3 0111 Samsung
1 -->8M*32
0-->16M*32
MIOB_D4: PCI_DEVID_0
MIOB_D5: PCI_DEVID_1 G72M 1000 GT
MIOB_D3: PCI_DEVID_2 G72M-V 0111 GS
MIOB_D11: PCI_DEVID_3 G72M-Z 0110
MIOB_CTL3: PCI_DEVID_4
MIOA_D1: SUB_VENDOR 0 SYSTEM BIOS (DEFAULT)
1 ADAPTER BIOS
MIOA_D0: PEX_PLL_EN_TERM100 0 ENABLED (DEFAULT)
1 DISABLED
MIOA_D6: 3GIO_PADCFG_LUT_ADDR[0] 0 DESKTOP
1 MOBILE (DEFAULT)
MIOA_D8: 3GIO_PADCFG_LUT_ADDR[1]
MIOA_D9: 3GIO_PADCFG_LUT_ADDR[2]
MIOB_HSYNC: 3GIO_PADCFG_LUT_ADDR[3]
0410 SD
R27
0R0603-PAD
Q3
TP0610T-T1-E3-GP
R24
0R2J-2-GP
DY
R20
10KR2F-2-GP
Q12
2N7002-11-GP
PM_SLP_S3#
22,23,31,37,41,42,47
<Core Design>
G72M-V-GP-U
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
NB8M-GS (3 of 3)
Size
A3
Document Number
ME3-Discrete
Rev
Date: Thursday, August 23, 2007
Sheet 47 of 51



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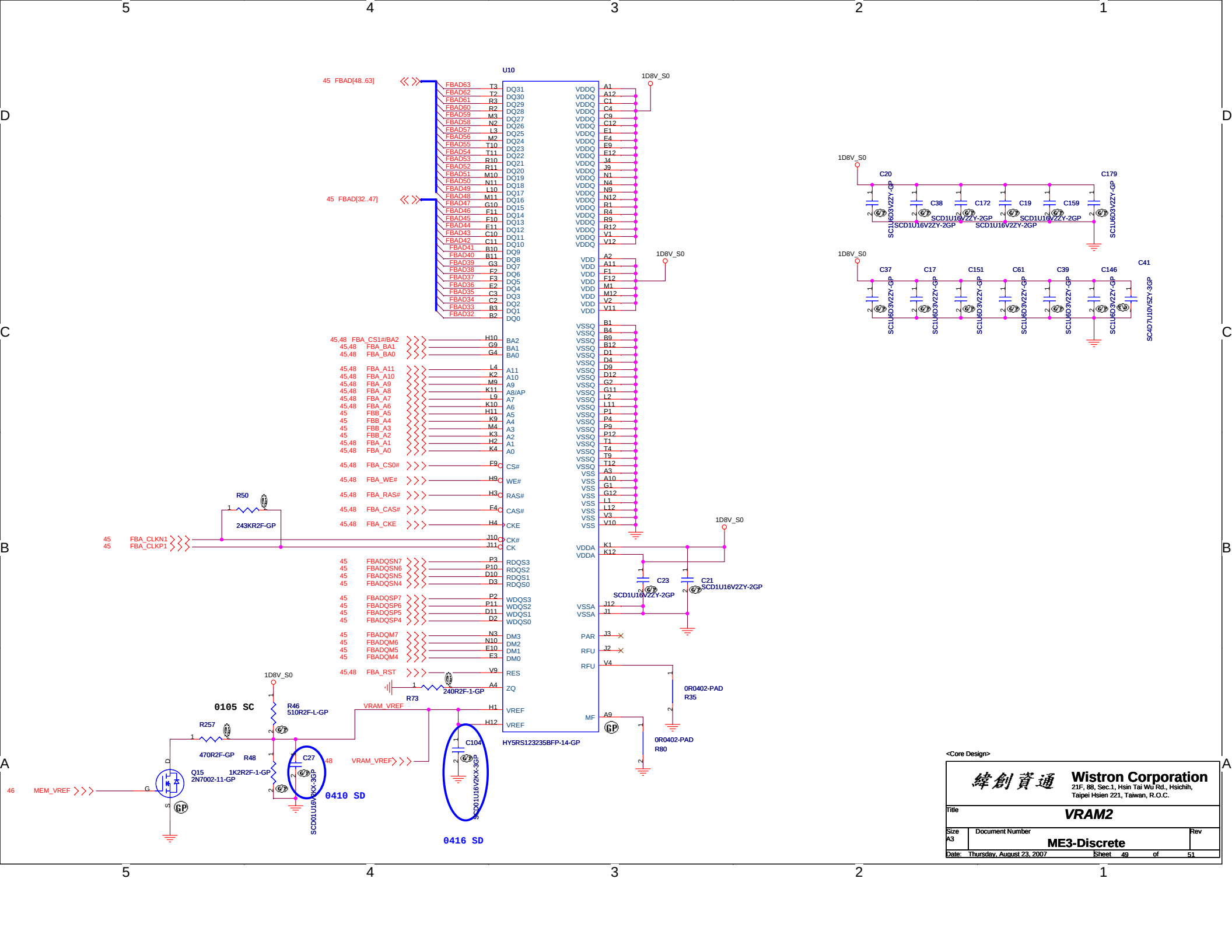
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***VRAM1***
Size A3	Document Number: **ME3-Discrete** — Rev
Date: Thursday, August 23, 2007	Sheet 48 of 51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C179
C38
C172
C19
C159
C37
C17
C151
C61
C39
C146
C41
SCD1U16V2ZY-2GP
SC1U6D3V2ZY-GP
SC4D7U10V5ZY-3GP
R50
243KR2F-GP
R73
240R2F-1-GP
R46
510R2F-L-GP
0105 SC
R257
470R2F-GP
R48
1K2R2F-1-GP
Q15
2N7002-11-GP
C27
SCD01U16V2KX-3GP
0410 SD
C104
0416 SD
C23
C21
0R0402-PAD
R35
R80
VRAM_VREF
MEM_VREF
FBA_CLKN1
FBA_CLKP1
FBA_RST
FBA_CS0#
FBA_WE#
FBA_RAS#
FBA_CAS#
FBA_CKE
FBA_BA0
FBA_BA1
FBA_CS1#/BA2
FBA_A0
FBA_A1
FBA_A2
FBA_A3
FBA_A4
FBA_A5
FBA_A6
FBA_A7
FBA_A8
FBA_A9
FBA_A10
FBA_A11
FBA_BA0
FBA_BA1
FBA_BA2
FBA_CKE
FBA_CAS#
FBA_RAS#
FBA_WE#
FBA_CS0#
FBA_RST
FBADQSN4
FBADQSN5
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FBADQSN7
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FBADQM5
FBADQM6
FBADQM7
FBAD[48..63]
FBAD[32..47]
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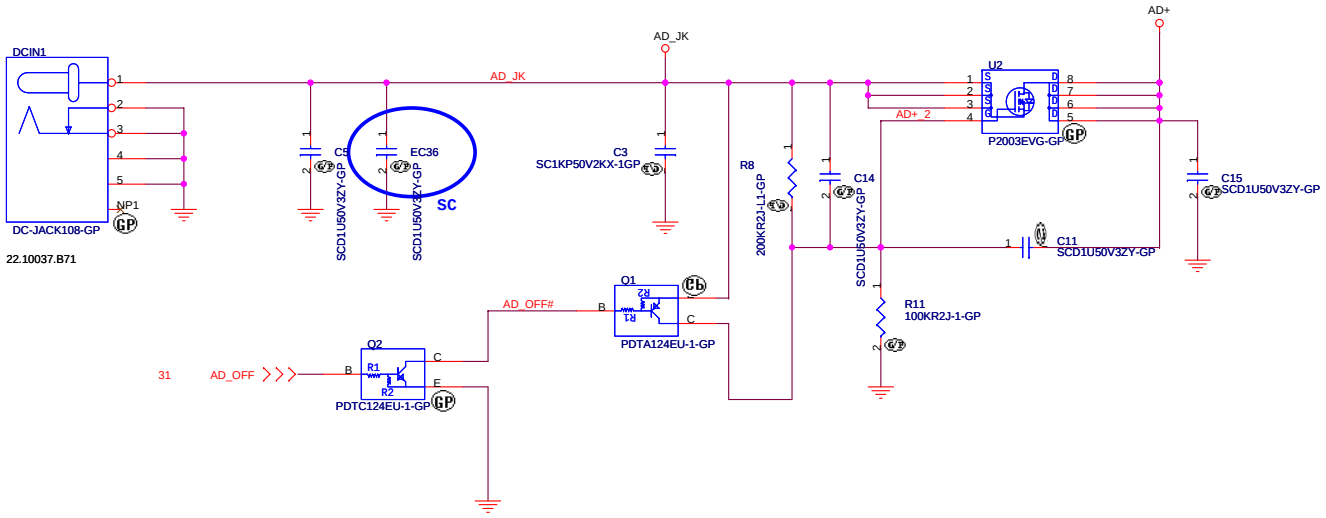
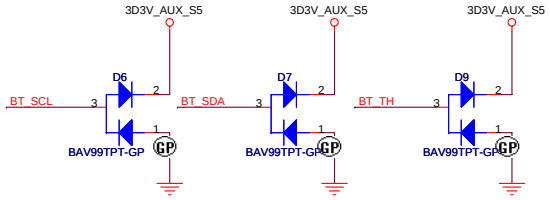
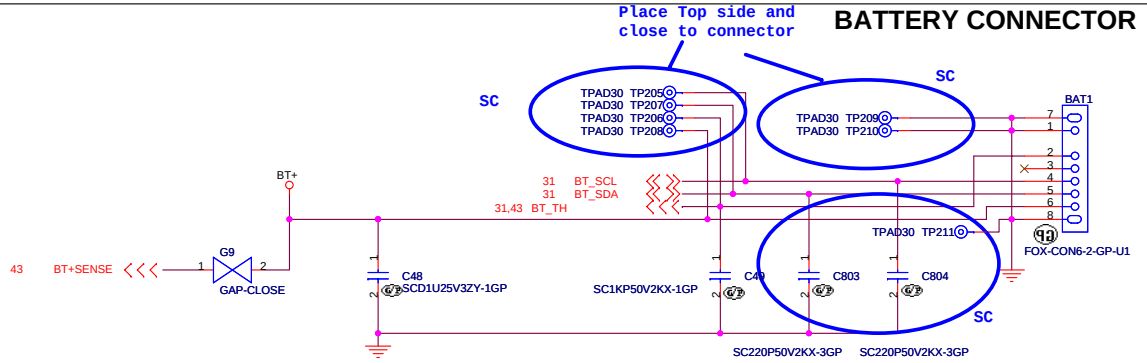
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
VRAM2
Size A3
Document Number
ME3-Discrete
Rev
Date: Thursday, August 23, 2007
Sheet 49 of 51

Adaptor in to generate DCBATOUT







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緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **AD/BATT CONN**

Size	Document Number	Rev
A3	ME3-Discrete	

Date: Wednesday, September 19, 2007 Sheet 50 of 51

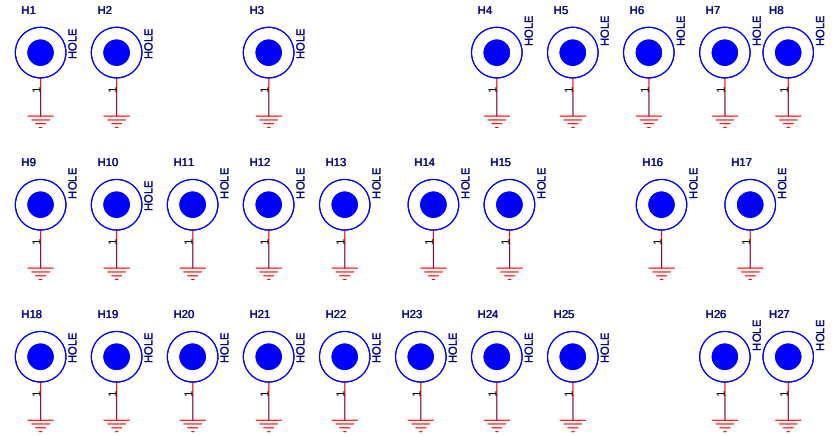
H13 34.4B602.001

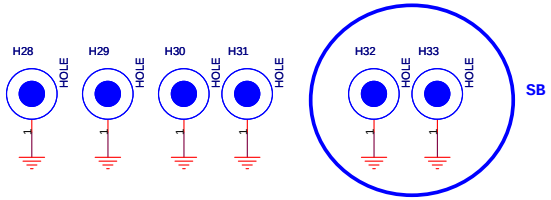
H25,24 34.4Q102.001

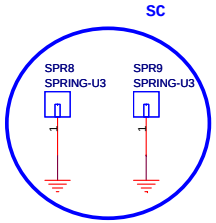
H30 87.66383.231

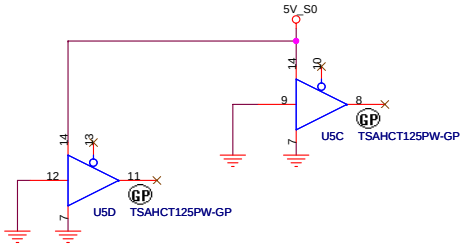
SPR7 34.40V16.001

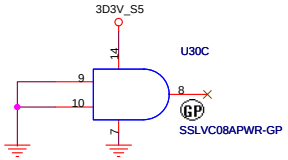
SPR9 34.40V16.001

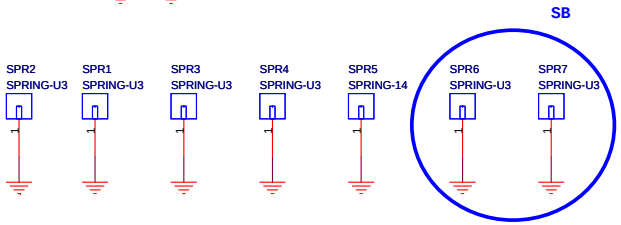












<Variant Name> 07221

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MISC

Size: A3 | Document Number: ME3-Discrete | Rev:

Date: Friday, September 14, 2007 | Sheet 51 of 51