Four Peaks (15") Block Diagram

Project code: 91.4Z901.001
PCB P/N : 48.4Z901.011
REVISION : -1M

Crystal 14.318MHz
CLK GEN. ICS 9LPRS365 3
Mobile CPU Penryn 4, 5
SMSC EMC2102 37
HOST BUS 667/800/1066MHz@1.05V
DDR3 800/1033 MHz 12,13
DDR3 800/1033 MHz 12,13
Cantiga
AGTL+ CPU I/F
DDR Memory I/F
INTEGRATED GRAHPICS
LVDS, CRT I/F
6,7,8,9,10,11
X4 DMI 400MHz
C-Link0
PCIex16
VGA Borad (MXM Connector) 46
SWITCH PI5C3257QE
SWITCH PS8122QFN48G
LCD 15
CRT 17
DVI 18
CRT
DVI
ezDockII/II+
USB/Express Card/MediaBay/1394*2port RJ45/RJ11/PS2*2/Serial Port/Parallel Port/CRT/TV/DVI-D/SPDIF/MIC in/Line in/Line out/AC Jack
44,45
2nd Battery
Crystal 32.768MHz
Int MIC 40
Codec ALC268 38
AZALIA
MIC In 40
OP AMP APL2057 39
40
INT.SPKR 1.5W
40
Line Out (No-SPDIF)
RJ11
MODEM MDC Card 27
ICH9M
6 PCIe ports
PCI/PCI BRIDGE
ACPI 2.0
4 SATA
12 USB 2.0/1.1 ports
ETHERNET (10/100/1000MbE)
High Definition Audio
LPC I/F
Serial Peripheral I/F
Matrix Storage Technology(DO)
Active Managemnet Technology(DO)
19,20,21,22
PCI
CardBus OZ711MZ0 30,31
MS/MS Pro/xD /MMC/SD 5 in 1 31
PCMCIA SLOT 35
SMART CARD 35
SPI
BIOS (4MB) 42
Crystal 24.576MHz
IEEE1394 TSB43AB22A 25
1394x2
Crystal 25MHz
LAN Giga LAN Intel 82567 32
SWITCH PI3L500ZFEX
TXFM 33
RJ45 33
LAN
New Card 34
PWR SW TPS2231 34
PCIe
Mini Card 36 (Robson2/3G)
Mini Card Kedron a/b/g/n 36 (WLAN)
C Link1
LPC BUS
Parallel-port
Seria-port
SATA
HDD SATA 24
SATA
ODD SATA (Module Bay) 23
USB
Mini USB Blue Tooth 26
Finger Printer 29
Camera
USB 4 Port 28
Crystal 32.768MHz
KBC Winbond WPCE773LA0DG 41
SPI
BIOS (1MB) 42
Launch Buttom 16
Touch Pad 41
INT. KB 41
LPC DEBUG CONN. 42
TPM SLB9635TT1D1 42
SuperIO PC87383MG 44
FIR 44
Crystal 32.768MHz
PSx2
MIC in/Line-out/Line-in
USB

SYSTEM DC/DC TPS51125 50

INPUTS	OUTPUTS
DCBATOUT	5V_S5(7A) 3D3V_S5(7A) 5V_AUX_S5 3D3V_AUX_S5

SYSTEM DC/DC TPS51124 51

INPUTS	OUTPUTS
DCBATOUT	1D05V_M(16A) 1D5V_S3(12A)

RT9026 52

1.5V_S3	DDR_VREF_S3 (1.2A)

G9131 52

3D3V_S0	2D5V_S0 (300mA)

TPS51117 54

DCBATOUT	1D8V_S0 (9.4A)

CHARGER BQ24750 55

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A

CPU DC/DC ISL6266A 49

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0~1.3V 38A

GFX DC/DC ISL6263 53

INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE 0~1.3V 6.5A

PCB STACKUP

TOP
VCC
S
S
GND
BOTTOM

Four Peaks
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Title: BLOCK DIAGRAM
Size: A2 | Document Number: Four Peaks | Rev: -1M
Date: Friday, November 21, 2008 | Sheet 1 of 57

ICH9M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9M Integrated Pull-up and Pull-down Resistors

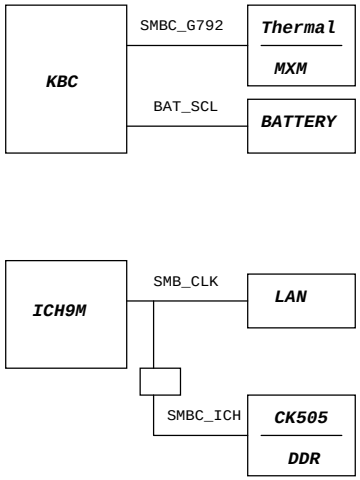
SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) **1=The iTPM Host Interface is disalbed(default)**
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality (default)**
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1= Disabled (default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) **11 = Disabled (default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation(Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 =Digital display Port and PCIe are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	**0 =No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.

SMBus



PCI Routing

page 17

	IDSEL	INT	REQ	GNT
TI7412	AD22	G:CARDBUS B:1394 F:Flash Media G:SD Host	0	0

PCIE Routing

LANE1	LAN BCM5787M
LANE2	MiniCard WLAN
LANE3	NewCard WLAN

USB Table

USB	
Pair	Device
0	NC
1	NC
2	USB2
3	USB4
4	USB3
5	BLUETOOTH
6	WEBCAM
7	FT
8	MINICARD
9	NEW1

Four Peaks

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Title: **Reference**

Size	Document Number	Rev
A3	Four Peaks	-1M

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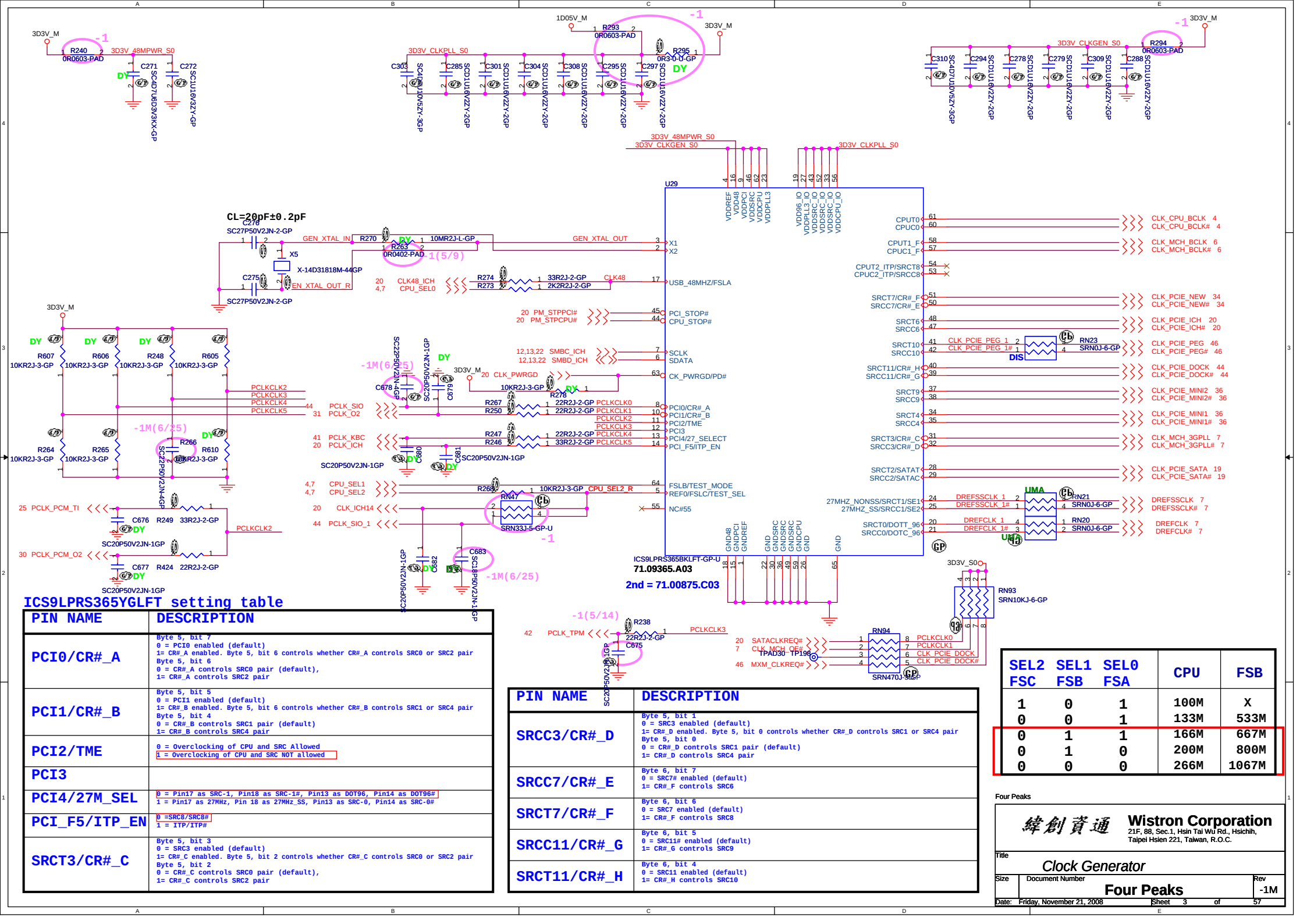

ICS9LPRS365YGLFT setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1= CR#_C controls SRC2 pair

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1= CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7# enabled (default) 1= CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1= CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1= CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1= CR#_H controls SRC10

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

Four Peaks

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Title: Clock Generator

Size	Document Number	Rev
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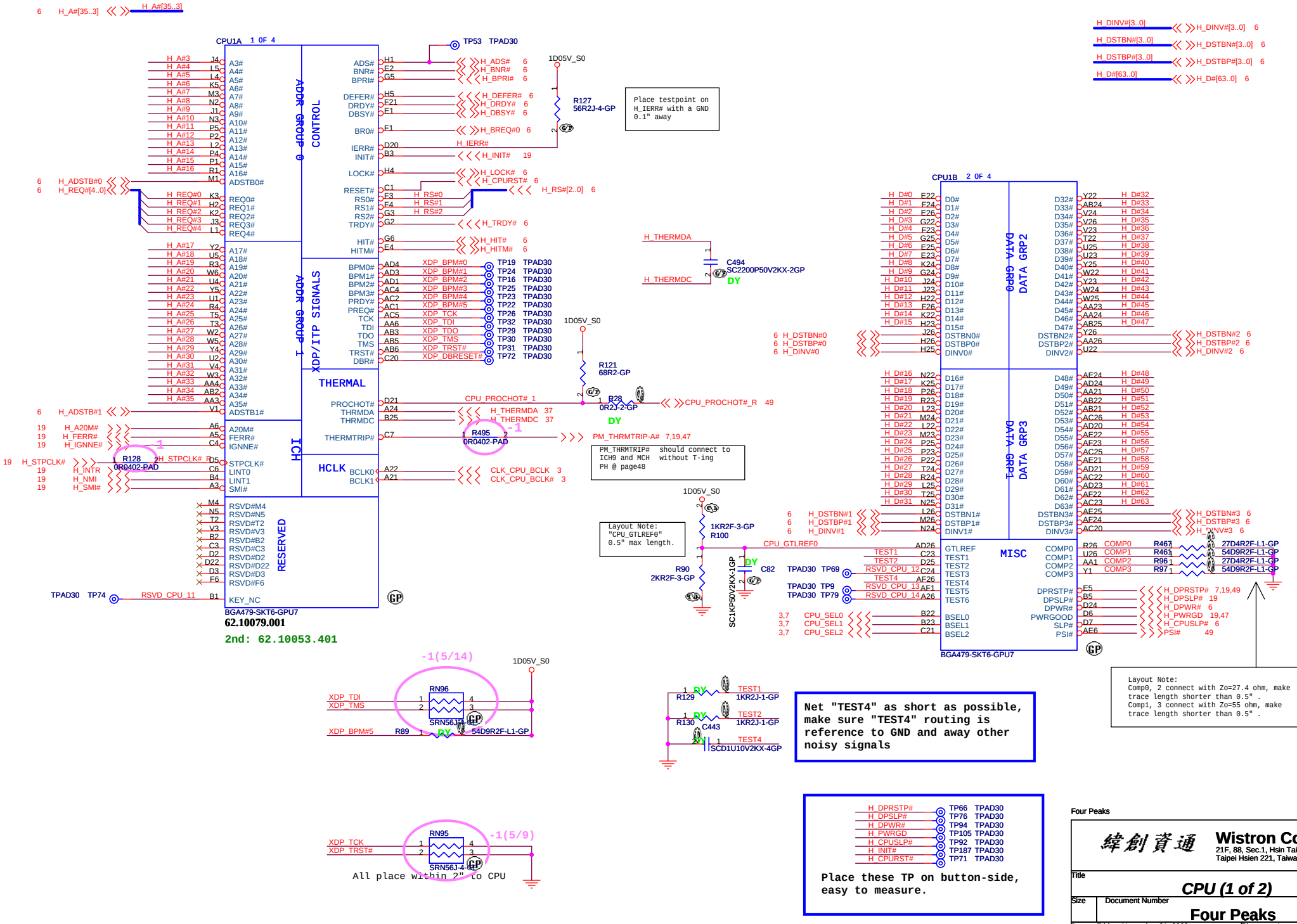
CPU1A 1 OF 4
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERMAL
HCLK
RESERVED
ICH
BGA479-SKT6-GPU7
62.10079.001
2nd: 62.10053.401
CPU1B 2 OF 4
DATA GRP2
DATA GRP0
DATA GRP3
DATA GRP1
MISC
BGA479-SKT6-GPU7
Place testpoint on H_IERR# with a GND 0.1" away
PM_THRMTRIP# should connect to ICH9 and MCH without T-ing PH @ page48
Layout Note: "CPU_GTLREF0" 0.5" max length.
Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals
Place these TP on button-side, easy to measure.
All place within 2" to CPU
Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" . Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .
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CPU (1 of 2)
Four Peaks
-1M
Friday, November 21, 2008
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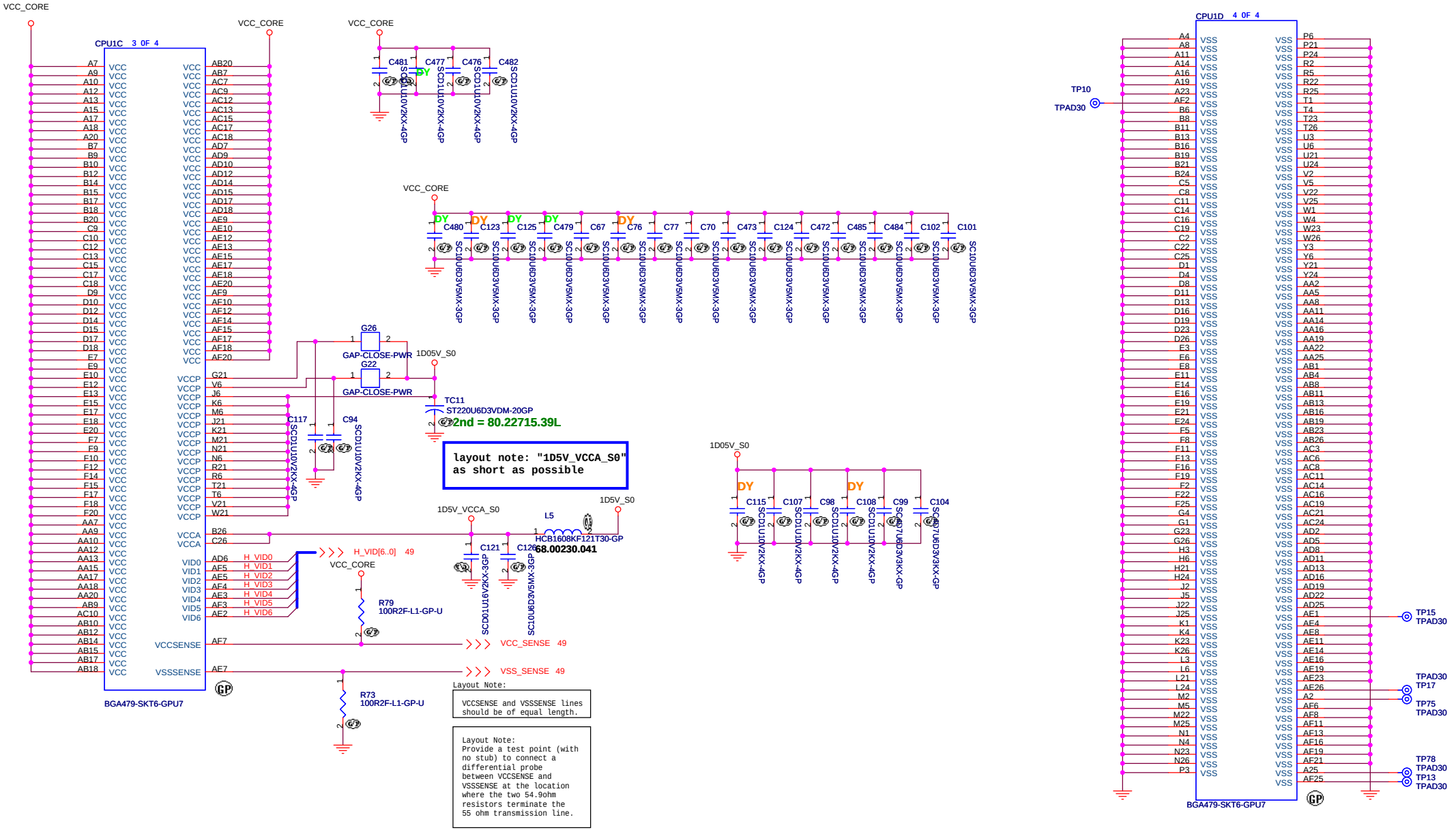

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Title	*CPU (2 of 2)*	
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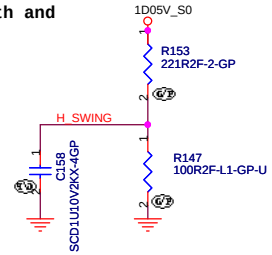
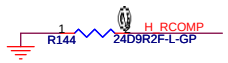
H_SWING routing Trace width and Spacing use 10 / 20 mil

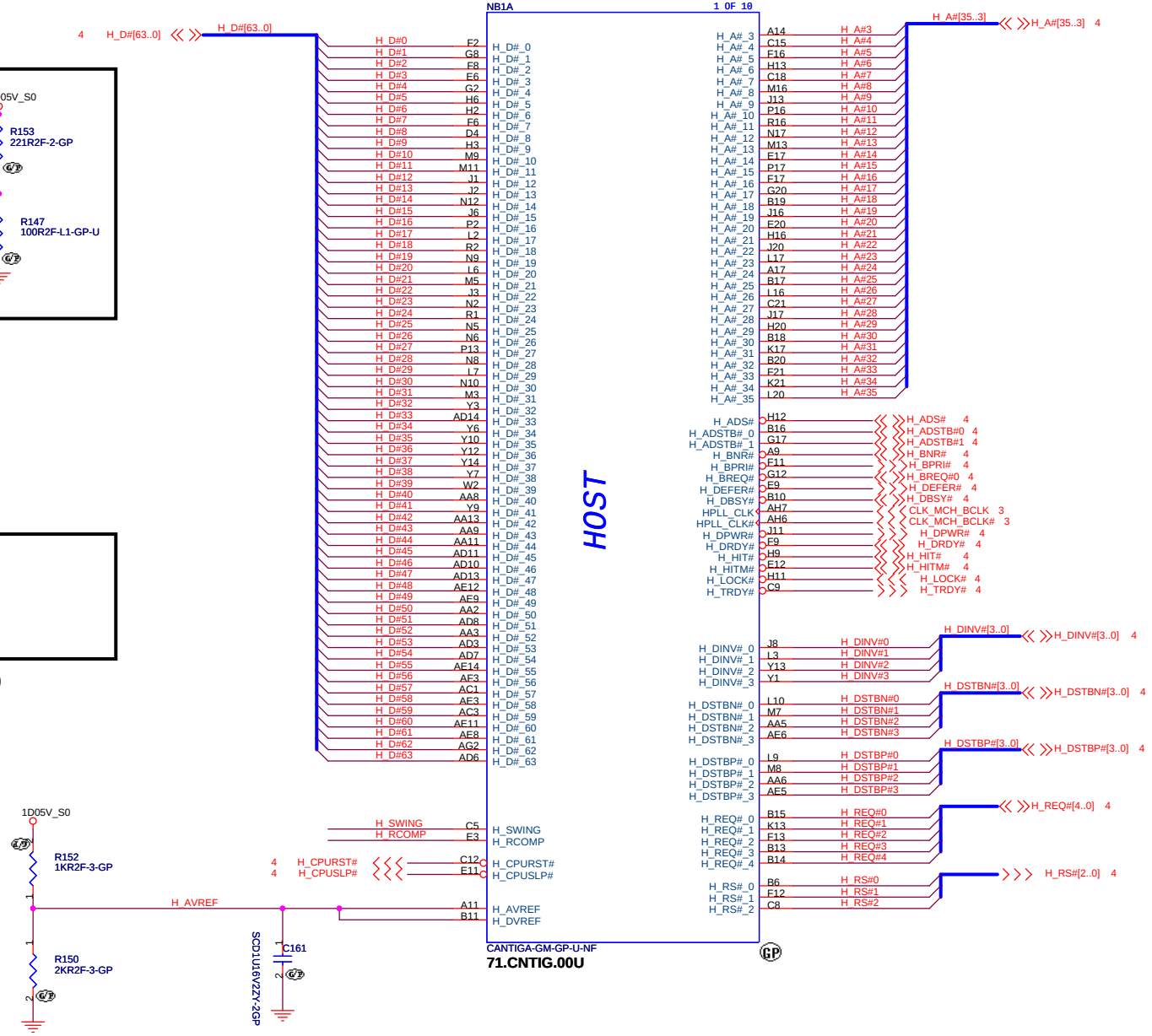
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")



Four Peaks

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Title	***Cantiga (1 of 6)***	
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Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1067MHz 011 = FSB 667MHz 010 = FSB 800MHz Others = Reserved
CFG4:3; 8; 11; 14:15; 17; 18	Reserved
CFG5 (DMI select)	Low = DMI x 2 High = DMI x 4 *
CFG6 (ITPM Host Interface)	High = The ITPM Host Interface is disabled Low = The ITPM Host Interface is enabled *
CFG7 (Intel Management Engine Crypto Strap)	Low = Intel Management Engine Crypto Transport Layer Security (TLS) cipher site with no confidentiality High = Intel Management Engine Crypto TLS Cipher suite with confidentiality *
CFG9 (PCIE Graphics Lane)	Low = Reverse Lanes, 15->0, 14->1 etc... High = Normal operation:Lane Numbered in Order *
CFG10 (PCIE Loopback enable)	Low = Enabled High = Disabled *
CFG12 (ALLZ)	Low = ALLZ mode Enabled High = Disabled *
CFG13 (XOR)	Low = XOR mode Enabled High = Disabled *
CFG16 (FSB Dynamic ODT)	Low = Dynamic ODT Disabled High = Dynamic ODT Enabled *
CFG19 (DMI Lane Reversal)	Low = Noraml operation: Lane Numbered in Order * High = Reverse Lanes DMI x 4 mode[MCH->ICH]: (0->3, 2->1, 1->2 and 0->3) DMI x 2 mode[MCH->ICH]: (3->0, 2->1)
CFG20 (Digital Display Port (SDVO/DP /iHDMI) Concurrent with PCIE)	Low = Only Digital Display Port (SDVO/iHDMI) or PCIE is operational * High = Digital Display Port (SDVO/DP/iHDMI) and PCIE are operating simulatneously via the PEG port
SDVO_CTRLDATA (SDVO Present)	Low = No SDVO Card Present * High = SDVO Card Present
L_DDC_DATA (Local Flat Panel (LFP) Present)	Low = LFP Disabled * High = LFP Card Present; PCIE disabled
DDPC_CTRLDATA (Digital Display Present)	Low = DisplayPort Disabled * High = DisplayPort Device Present

Close to GMCH as 500 mils.

CRT_IREF routing Trace width use 20 mil

FOR Cantiga: 1.02k_1% ohm
Teenah: 1.3k ohm

for HDMI port C

FOR Cantiga:500 ohm
Teenah: 392 ohm

layout take note

FOR Discrete,change to 0 ohm
63.R0034.1DL

CANTIGA-GM-GP-U-NF
71.CNTIG.00U

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Title	Cantiga (2 of 6)
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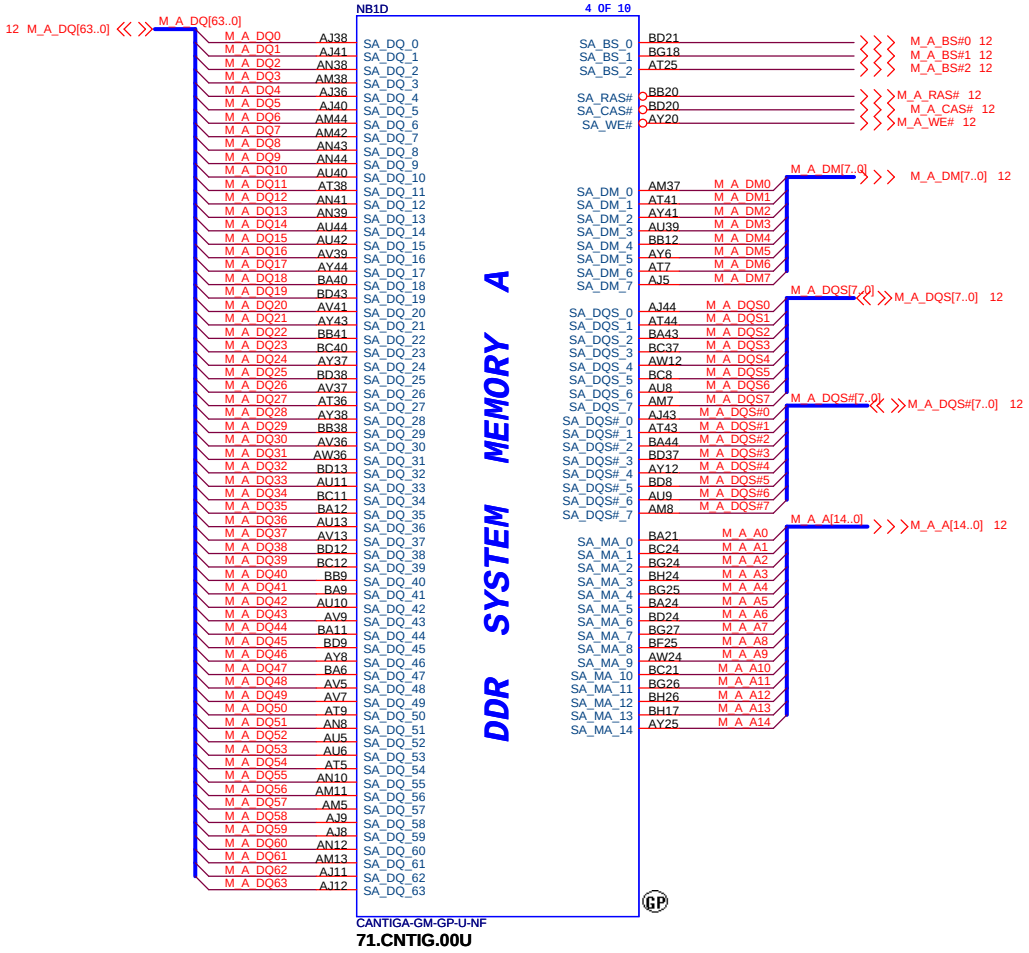

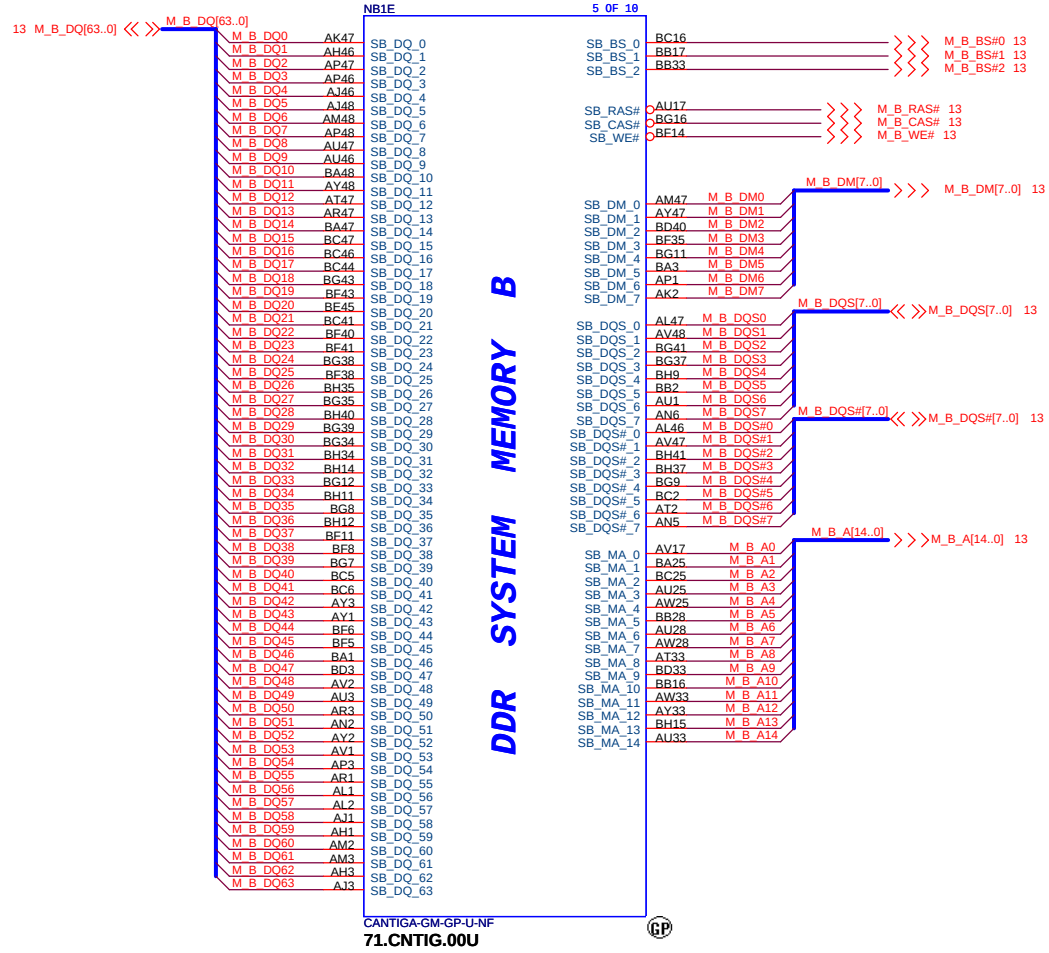

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Title: Cantiga (3 of 6)

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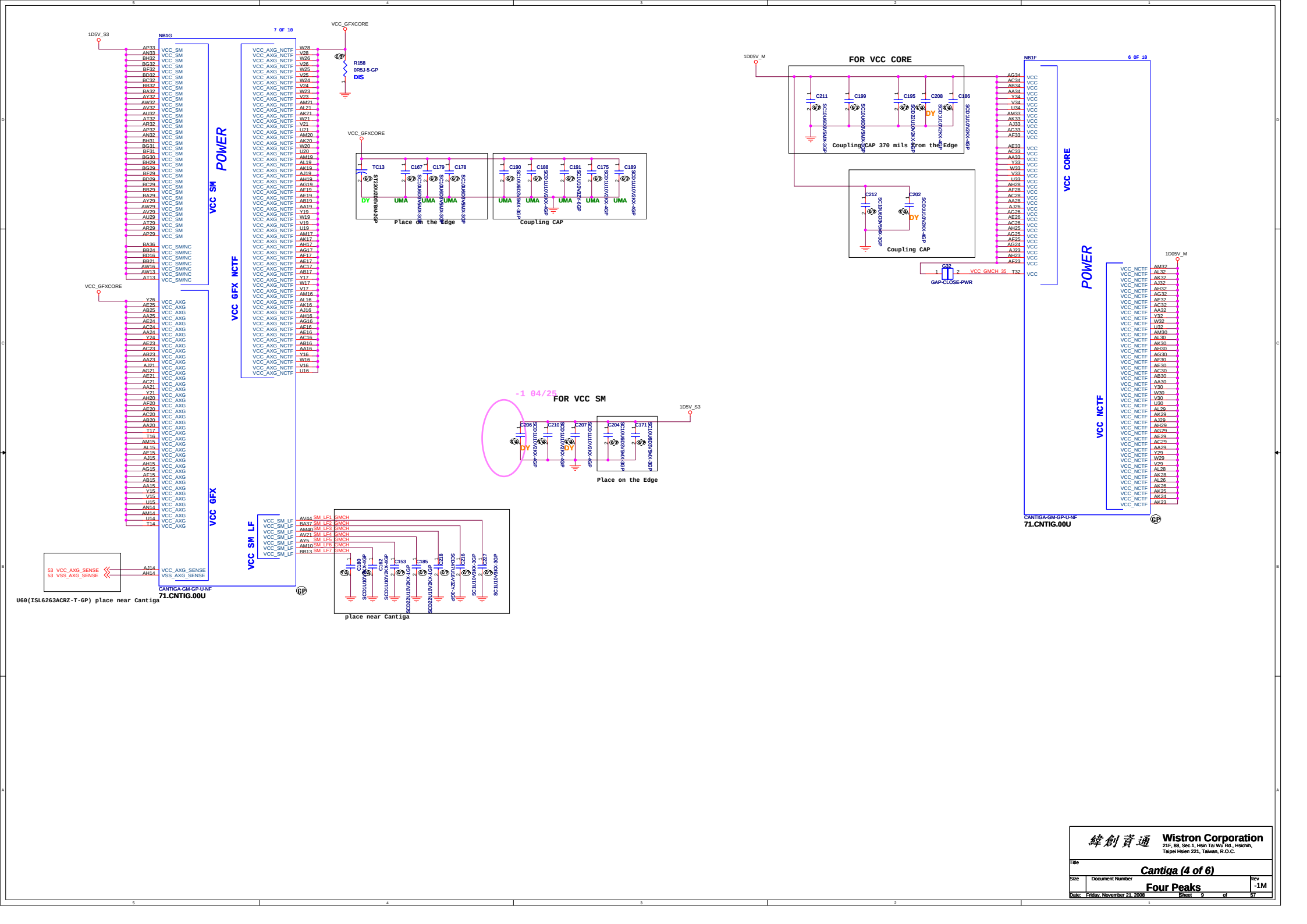

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Title	***Cantiga (4 of 6)***	
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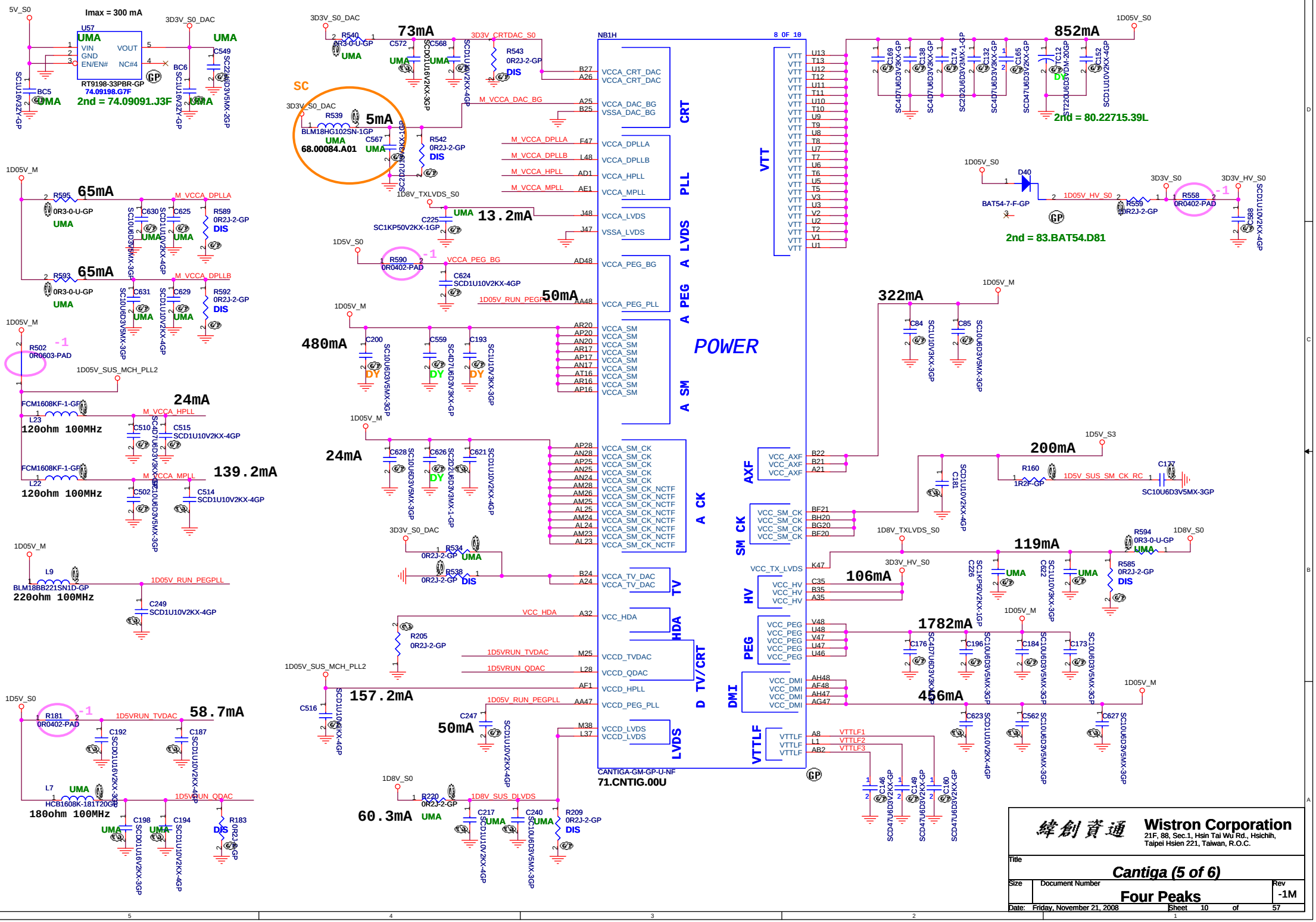

Wistron Corporation	Title: Cantiga (5 of 6)		
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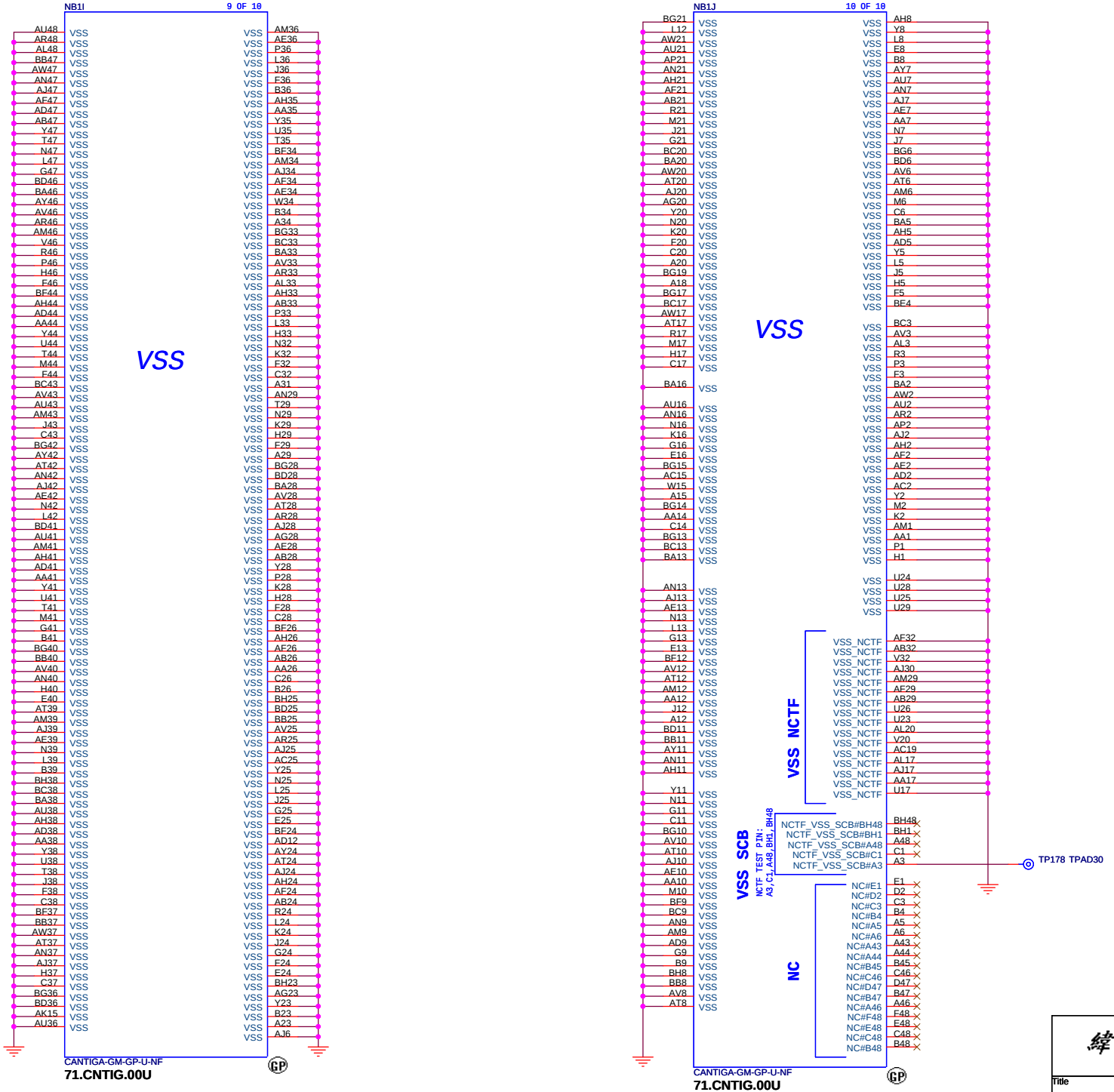

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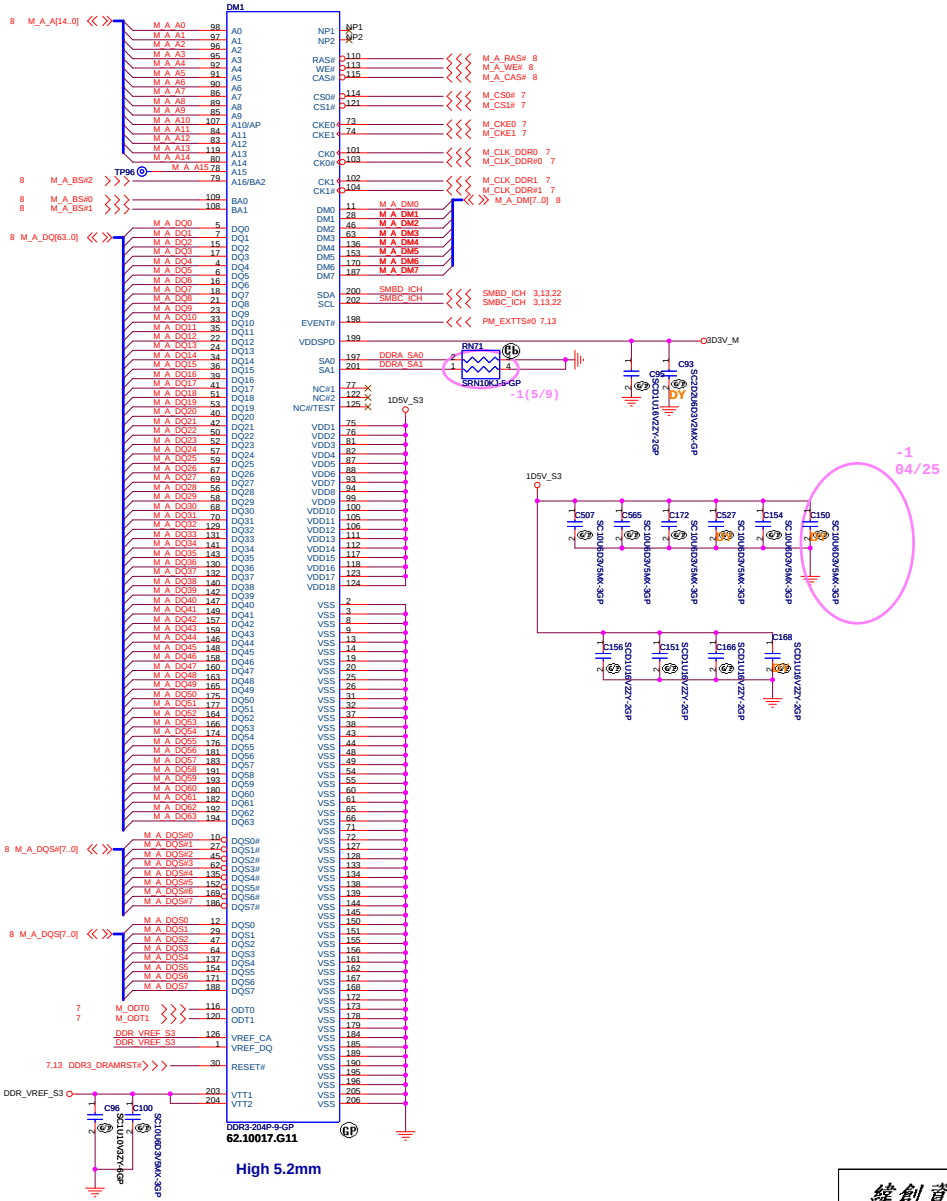
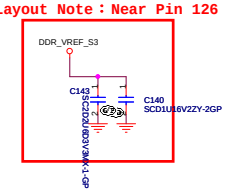
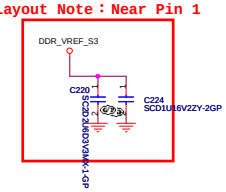
DDR3 SOCKET_1



Layout Note：Near Pin 126



Layout Note：Near Pin 1



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Title	DDR3 Socket	
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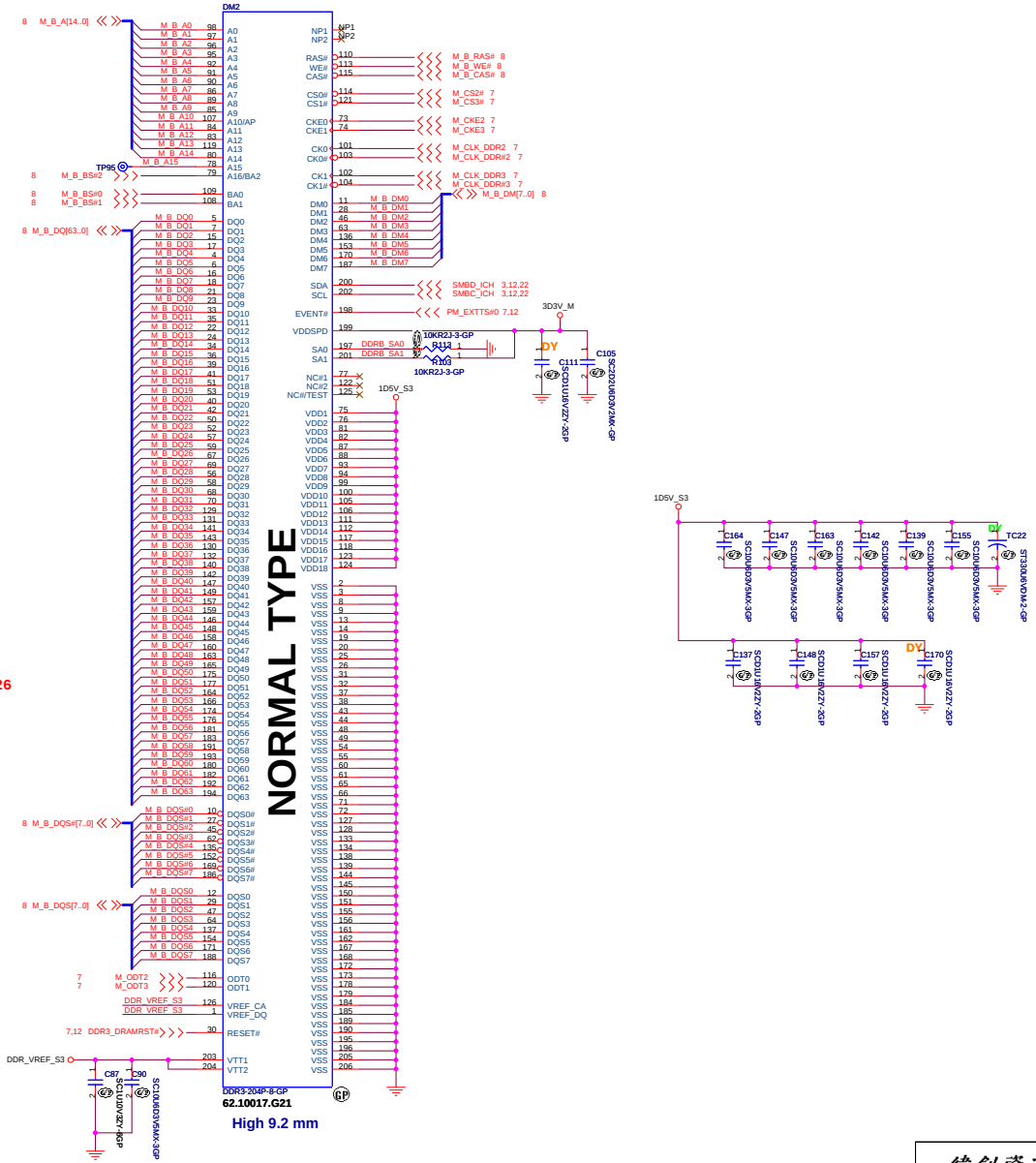
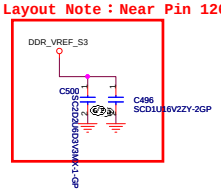
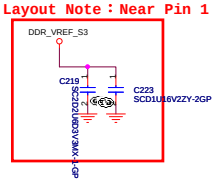
DDR3 SOCKET_2



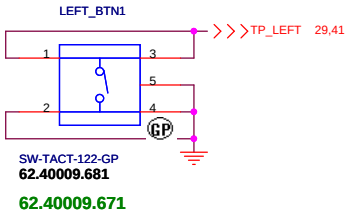
Layout Note：Near Pin 126

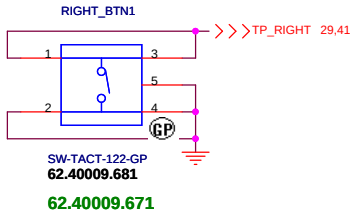


Layout Note：Near Pin 1

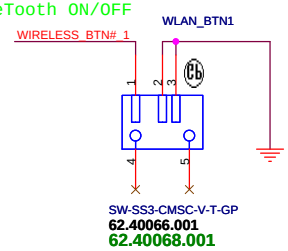


緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***DDR3 Termination Resistor***	
Size	Document Number **Four Peaks**	Rev -1M
Date: Friday, November 21, 2008	Sheet 13 of 57	



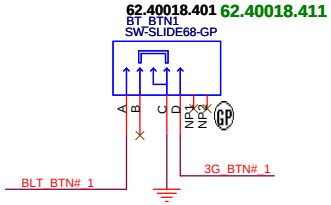


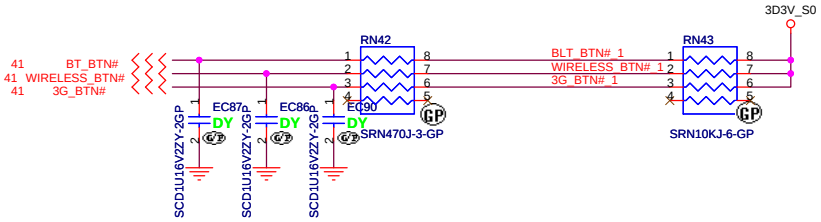
BlueTooth ON/OFF



Wireless ON/OFF

Check Wireless Button left or right





Four Peaks

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Taipei Hsien 221, Taiwan, R.O.C.

Title	***SWITCH / Button***	
Size	Document Number **Four Peaks**	Rev -1M
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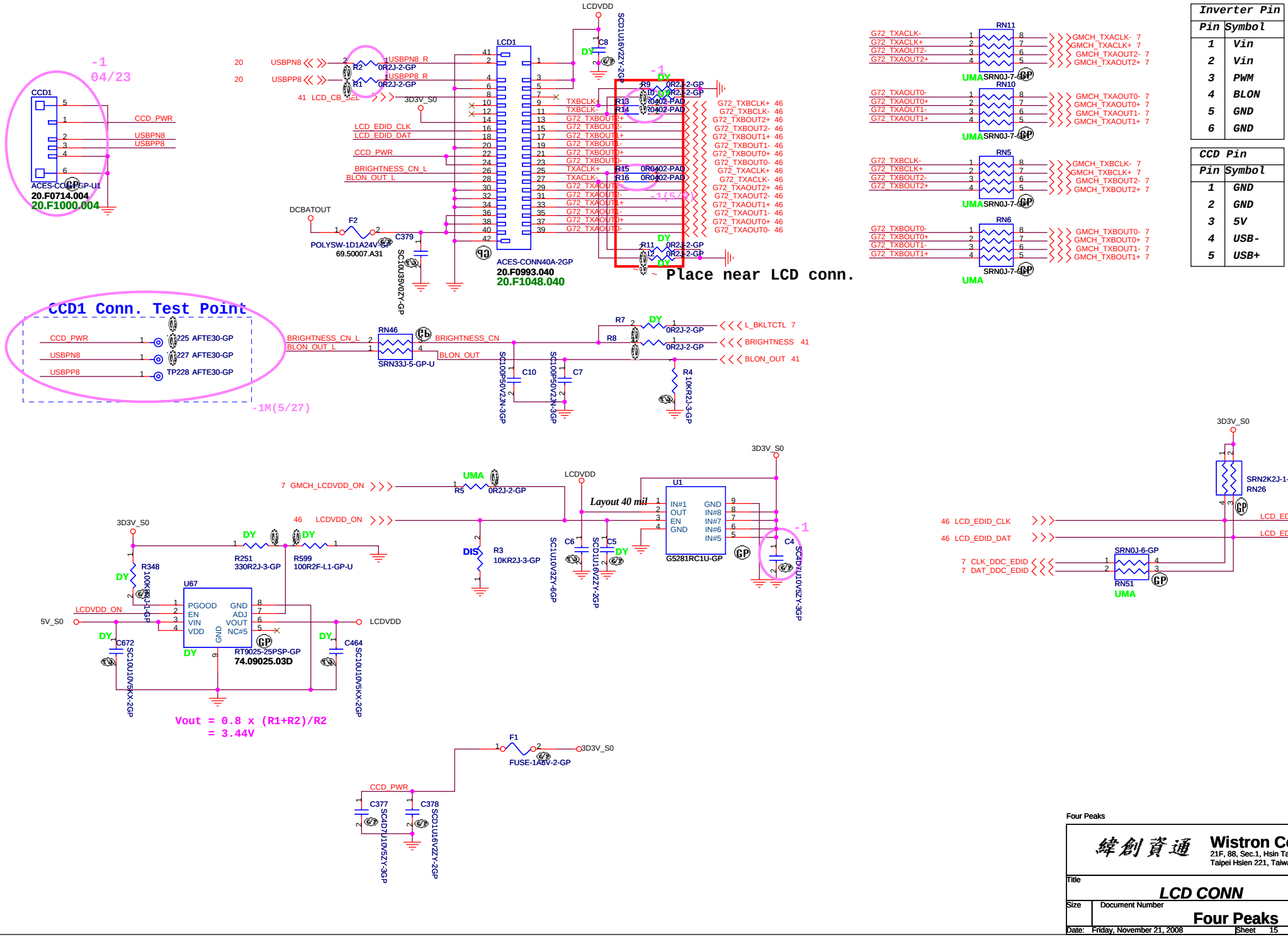
LCD/INVERTER/CCD CONN



Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	PWM
4	BLON
5	GND
6	GND

CCD Pin	
Pin	Symbol
1	GND
2	GND
3	5V
4	USB-
5	USB+

Four Peaks

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **LCD CONN**

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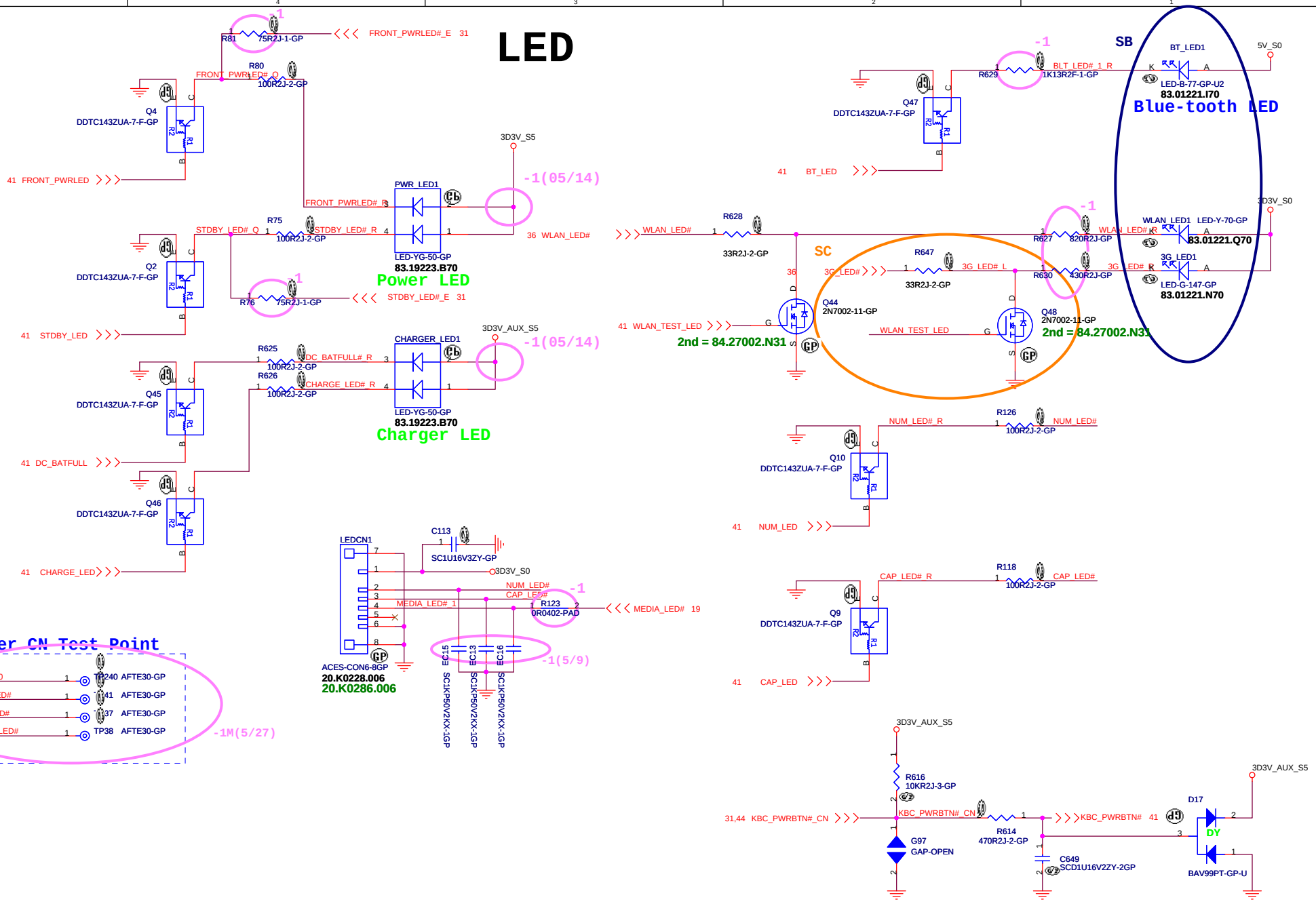
LED



Four Peaks

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Taipei Hsien 221, Taiwan, R.O.C.

Title	***LED&POWERBD CONN***	
Size	Document Number: **Four Peaks**	Rev: -1M
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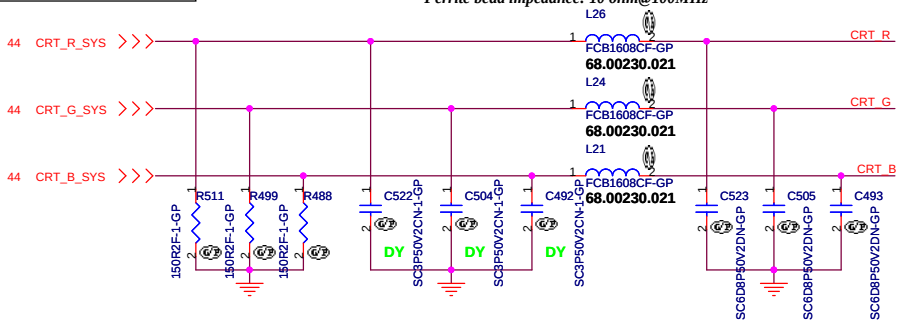
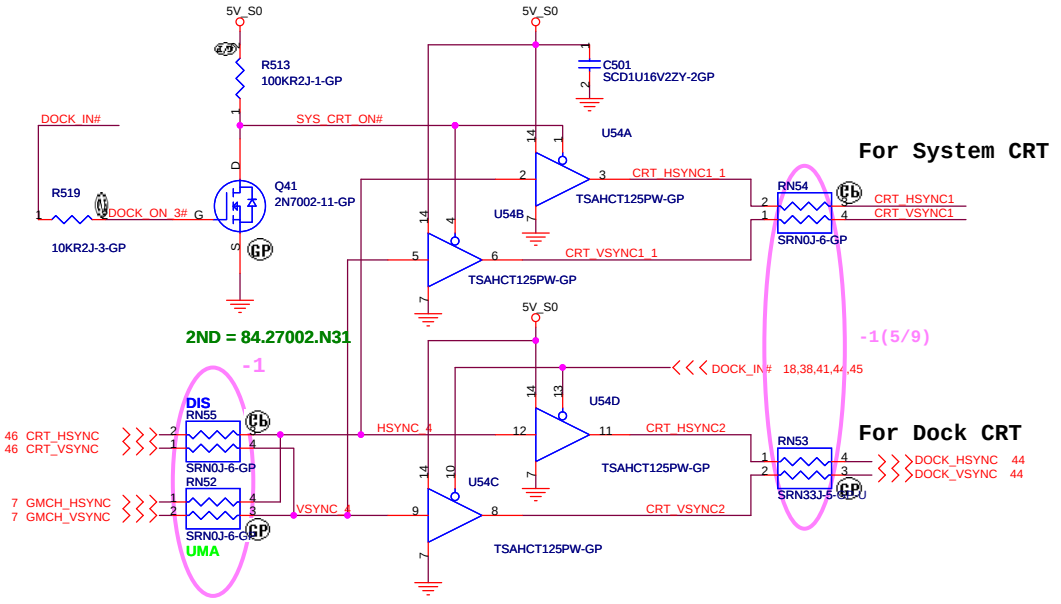
Layout Note:
Place these resistors close to the CRT-out connector

Ferrite bead impedance: 10 ohm@100MHz



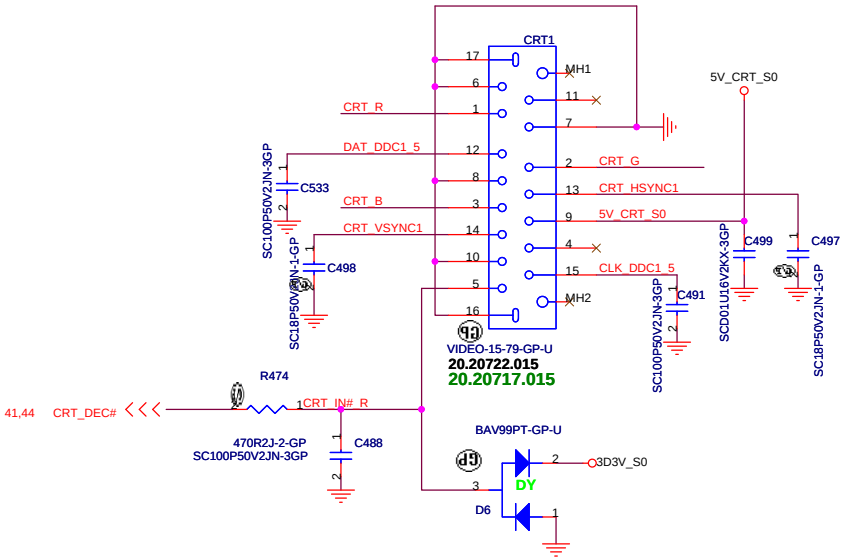
Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift

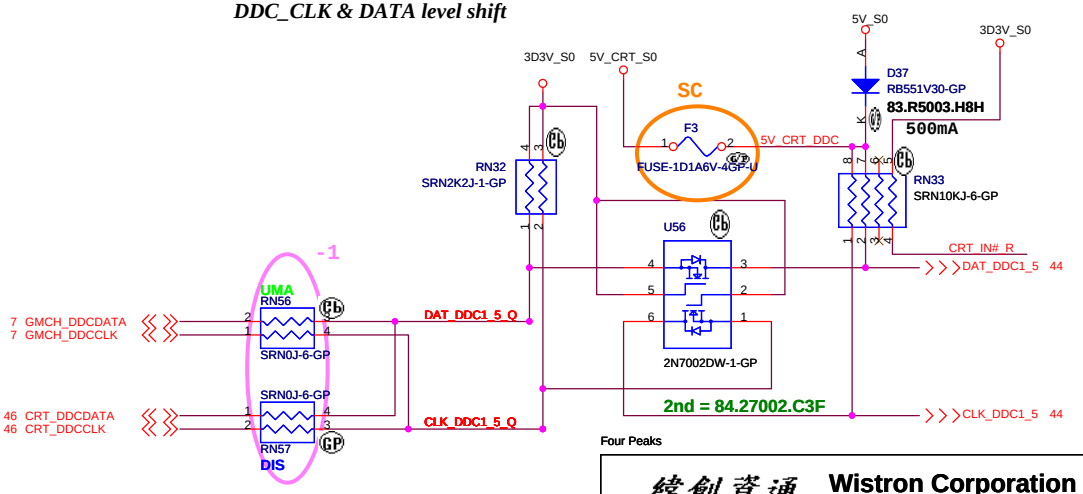


Function	DOCK_CRT_SEL#
SYSTEM	H
DOCK	L

CRT I/F & CONNECTOR



DDC_CLK & DATA level shift



Four Peaks

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Title: **CRT CONN**

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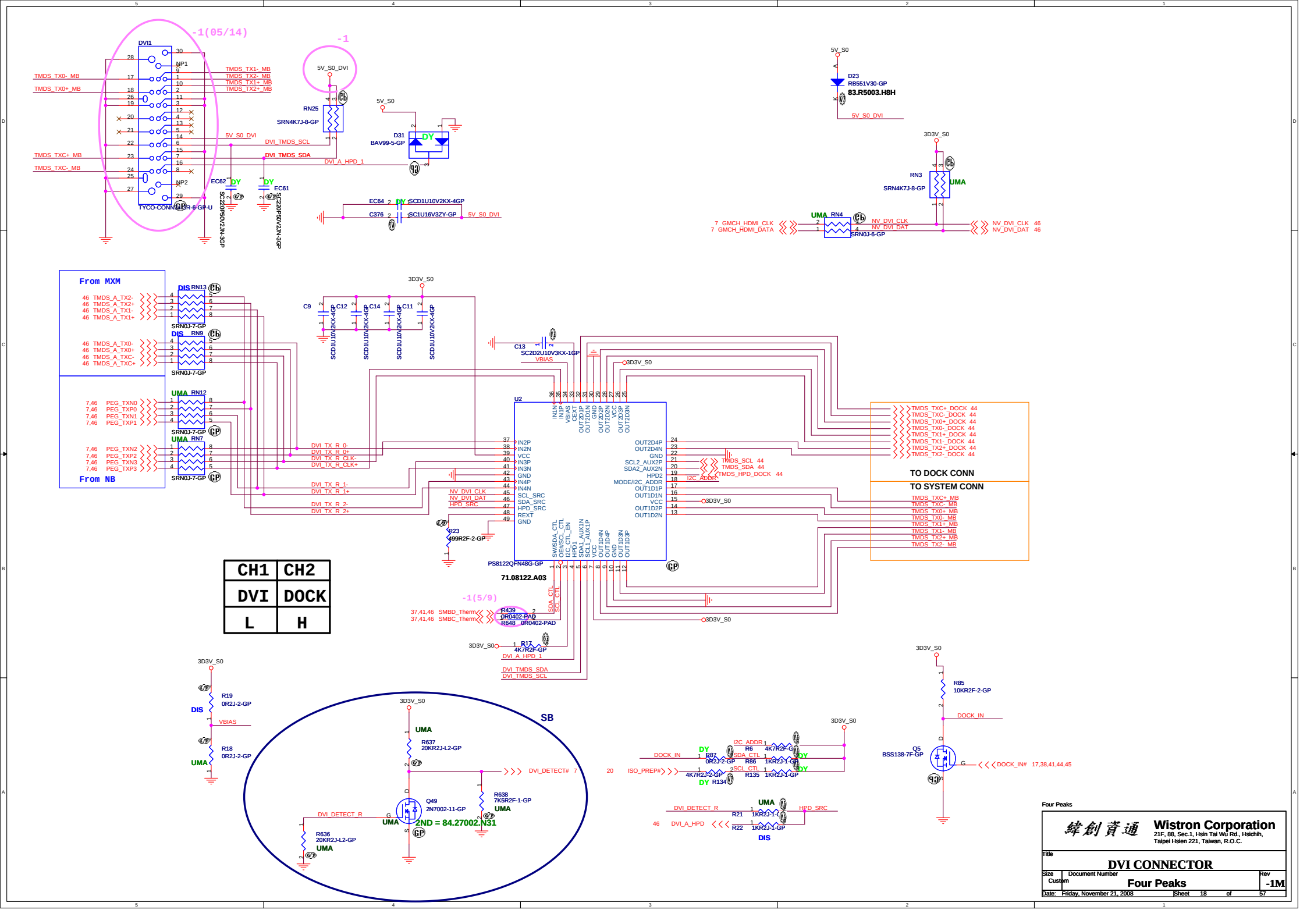
6 1 7 2 8 3 9 4 10 5


-1(05/14)
DVI1
TYCO-CONN_DVI-R-6-GP-U
TMDS_TX0- MB
TMDS_TX0+ MB
TMDS_TXC+ MB
TMDS_TXC- MB
TMDS_TX1- MB
TMDS_TX2- MB
TMDS_TX1+ MB
TMDS_TX2+ MB
5V_S0_DVI
DVI_TMDS_SCL
DVI_TMDS_SDA
DVI_A_HPD_1
EC62
EC61
SC220P50V2JN-3GP
-1
RN25
SRN4K7J-8-GP
D31
BAV99-5-GP
EC64
C376
SCD1U10V2KX-4GP
SC1U16V3ZY-GP
D23
RB551V30-GP
83.R5003.H8H
RN3
UMA
SRN4K7J-8-GP
UMA_RN4
SRN0J-6-GP
7 GMCH_HDMI_CLK
7 GMCH_HDMI_DATA
NV_DVI_CLK
NV_DVI_DAT
NV_DVI_CLK 46
NV_DVI_DAT 46
From MXM
From NB
DIS_RN13
DIS_RN9
UMA_RN12
UMA_RN7
SRN0J-7-GP
46 TMDS_A_TX2-
46 TMDS_A_TX2+
46 TMDS_A_TX1-
46 TMDS_A_TX1+
46 TMDS_A_TX0-
46 TMDS_A_TX0+
46 TMDS_A_TXC-
46 TMDS_A_TXC+
7,46 PEG_TXN0
7,46 PEG_TXP0
7,46 PEG_TXN1
7,46 PEG_TXP1
7,46 PEG_TXN2
7,46 PEG_TXP2
7,46 PEG_TXN3
7,46 PEG_TXP3
C9
C12
C14
C11
C13
SC2D2U10V3KX-1GP
VBIAS
3D3V_S0
U2
PS8122QFN48G-GP
71.08122.A03
DVI_TX_R_0-
DVI_TX_R_0+
DVI_TX_R_CLK-
DVI_TX_R_CLK+
DVI_TX_R_1-
DVI_TX_R_1+
DVI_TX_R_2-
DVI_TX_R_2+
NV_DVI_CLK
NV_DVI_DAT
HPD_SRC
R23
499R2F-2-GP
TMDS_SCL 44
TMDS_SDA 44
TMDS_HPD_DOCK 44
I2C_ADDR
TMDS_TXC+_DOCK 44
TMDS_TXC-_DOCK 44
TMDS_TX0+_DOCK 44
TMDS_TX0-_DOCK 44
TMDS_TX1+_DOCK 44
TMDS_TX1-_DOCK 44
TMDS_TX2+_DOCK 44
TMDS_TX2-_DOCK 44
TO DOCK CONN
TO SYSTEM CONN
TMDS_TXC+_MB
TMDS_TXC-_MB
TMDS_TX0+_MB
TMDS_TX0-_MB
TMDS_TX1+_MB
TMDS_TX1-_MB
TMDS_TX2+_MB
TMDS_TX2-_MB
-1(5/9)
37,41,46 SMBD_Therm
37,41,46 SMBC_Therm
R439 0R0402-PAD
R648 0R0402-PAD
R17 4K7R2F-GP
SDA_CTL
SCL_CTL
CH1 CH2
DVI DOCK
L H
R19 0R2J-2-GP
R18 0R2J-2-GP
VBIAS
SB
R637 20KR2J-L2-GP
R638 7K5R2F-1-GP
R636 20KR2J-L2-GP
Q49 2N7002-11-GP
2ND = 84.27002.N31
DVI_DETECT# 7
DVI_DETECT_R
R85 10KR2F-2-GP
DOCK_IN
Q5 BSS138-7F-GP
DOCK_IN# 17,38,41,44,45
R87 0R2J-2-GP
R6 4K7R2F-GP
R86 1KR2J-1-GP
R135 1KR2J-1-GP
R134 4K7R2J-2-GP
I2C_ADDR
ISO_PREP#
20
DVI_A_HPD
46
R21 1KR2J-1-GP
R22 1KR2J-1-GP
HPD_SRC
Four Peaks
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DVI CONNECTOR
Size Custom
Document Number
Four Peaks
Rev -1M
Date: Friday, November 21, 2008
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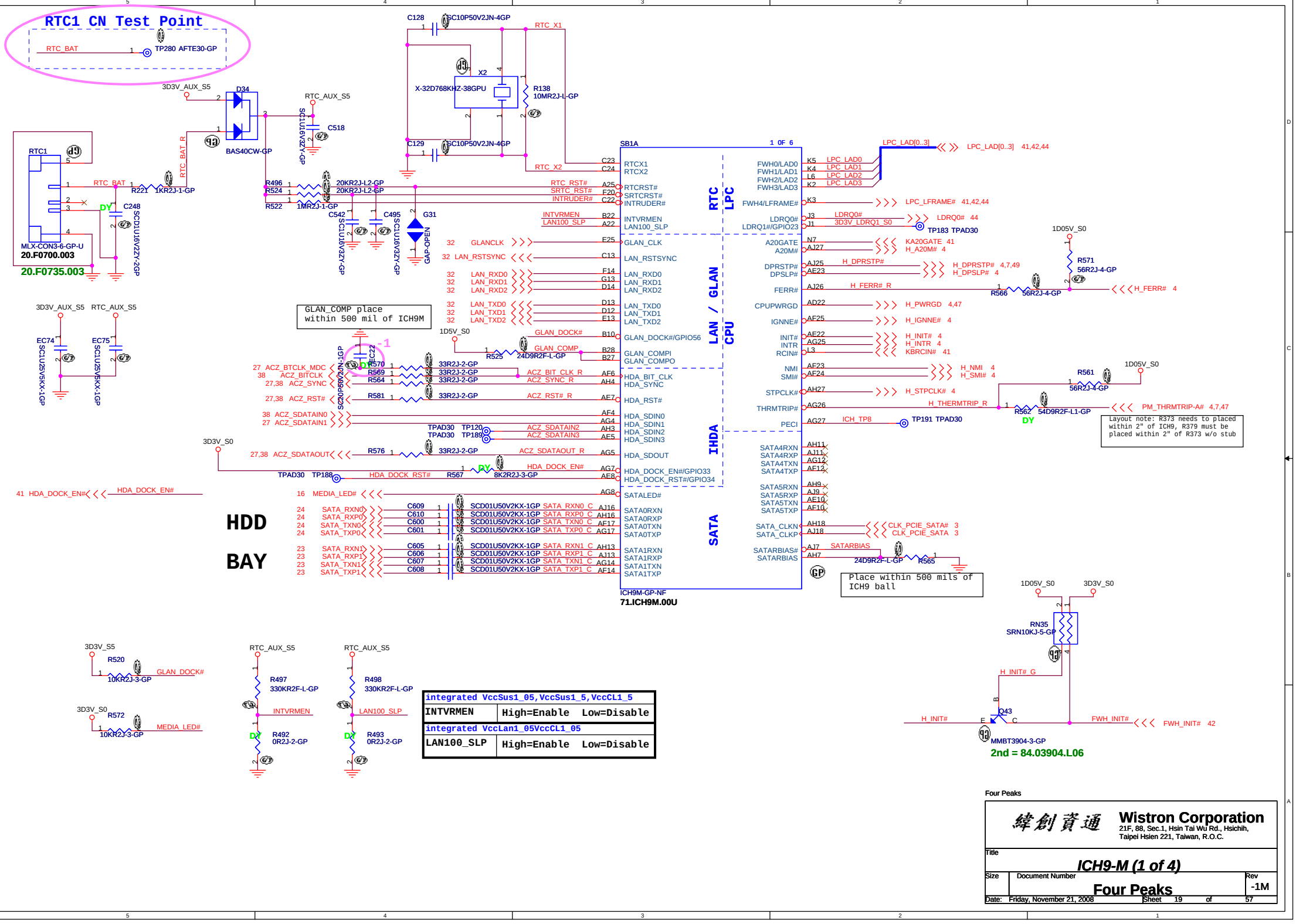
RTC1 CN Test Point
RTC_BAT
TP280 AFTE30-GP
3D3V_AUX_S5
D34
BAS40CW-GP
RTC_AUX_S5
C518
SC1U16V2ZY-GP
RTC1
MLX-CON3-6-GP-U
20.F0700.003
20.F0735.003
RTC_BAT_R
R221 1KR2J-1-GP
C248
SCD1U16V2ZY-2GP
C128 SC10P50V2JN-4GP
C129 SC10P50V2JN-4GP
X2
X-32D768KHZ-38GPU
R138 10MR2J-L-GP
RTC_X1
RTC_X2
R496 20KR2J-L2-GP
R524 20KR2J-L2-GP
R522 1MR2J-1-GP
C542 SCD1U16V2ZY-4GP
C495 SCD1U16V2ZY-4GP
G31 GAP-OPEN
SB1A
1 OF 6
RTCX1
RTCX2
RTCRST#
SRTCRST#
INTRUDER#
INTVRMEN
LAN100_SLP
RTC_RST#
SRTC_RST#
INTRUDER#
RTC
LPC
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
LPC_LAD[0..3]
LPC_LAD0
LPC_LAD1
LPC_LAD2
LPC_LAD3
LPC_LFRAME# 41,42,44
LDRQ0# 44
3D3V_LDRQ1_S0
TP183 TPAD30
GLANCLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
GLAN_DOCK#
GLAN_COMP
GLAN_DOCK#/GPIO56
GLAN_COMPI
GLAN_COMPO
LAN / GLAN
GLAN_COMP place within 500 mil of ICH9M
R525 24D9R2F-L-GP
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDOUT
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO34
IHDA
A20GATE
A20M#
DPRSTP#
DPSLP#
FERR#
CPUPWRGD
IGNNE#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THRMTRIP#
PECI
H_DPRSTP# 4,7,49
H_DPSLP# 4
H_FERR# R
H_PWRGD 4,47
H_IGNNE# 4
H_INIT# 4
H_INTR 4
KBRCIN# 41
H_NMI 4
H_SMI# 4
H_STPCLK# 4
H_THERMTRIP_R
ICH_TP8
TP191 TPAD30
CPU
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
SATA_CLKN
SATA_CLKP
SATARBIAS#
SATARBIAS
SATA
CLK_PCIE_SATA# 3
CLK_PCIE_SATA 3
R565 24D9R2F-L-GP
Place within 500 mils of ICH9 ball
ICH9M-GP-NF
71.ICH9M.00U
R571 56R2J-4-GP
R566 56R2J-4-GP
R561 56R2J-4-GP
R562 54D9R2F-L1-GP
PM_THRMTRIP-A# 4,7,47
Layout note: R373 needs to placed within 2" of ICH9, R379 must be placed within 2" of R373 w/o stub
EC74 SC1U25V5KX-1GP
EC75 SC1U25V5KX-1GP
R570 33R2J-2-GP
R569 33R2J-2-GP
R564 33R2J-2-GP
R581 33R2J-2-GP
R576 33R2J-2-GP
R567 8K2R2J-3-GP
C522 SC20P50V2JN-1GP
ACZ_BIT_CLK_R
ACZ_SYNC_R
ACZ_RST#_R
ACZ_SDATAIN2
ACZ_SDATAIN3
ACZ_SDATAOUT_R
HDA_DOCK_EN#
HDA_DOCK_RST#
TPAD30 TP120
TPAD30 TP189
TPAD30 TP188
HDD BAY
SATA_RXN0
SATA_RXP0
SATA_TXN0
SATA_TXP0
SATA_RXN1
SATA_RXP1
SATA_TXN1
SATA_TXP1
SCD01U50V2KX-1GP
R520 10KR2J-3-GP
R572 10KR2J-3-GP
GLAN_DOCK#
MEDIA_LED#
R497 330KR2F-L-GP
R498 330KR2F-L-GP
R492 0R2J-2-GP
R493 0R2J-2-GP
INTVRMEN
LAN100_SLP
RN35 SRN10KJ-5-GP
H_INIT# G
Q43 MMBT3904-3-GP
H_INIT#
FWH_INIT#
FWH_INIT# 42
2nd = 84.03904.L06
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
Four Peaks
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9-M (1 of 4)
Size
Document Number
Four Peaks
Rev
-1M
Date: Friday, November 21, 2008
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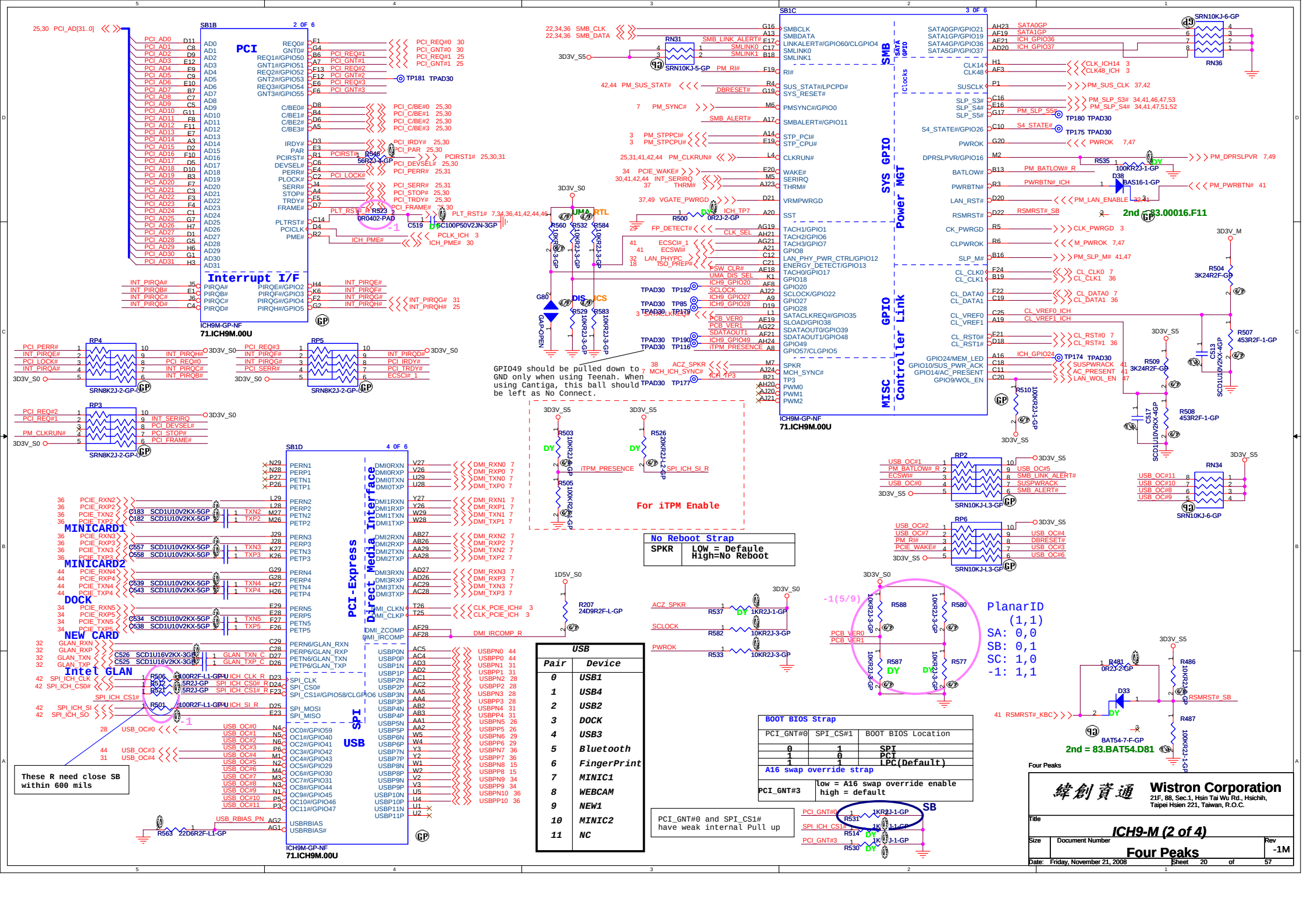
SB1B
2 OF 6
PCI
Interrupt I/F
ICH9M-GP-NF
71.ICH9M.00U
SB1C
3 OF 6
SMB
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
ICH9M-GP-NF
71.ICH9M.00U
SB1D
4 OF 6
PCI-Express
Direct Media Interface
SPI
USB
ICH9M-GP-NF
71.ICH9M.00U
GPIO49 should be pulled down to GND only when using Teenah. When using Cantiga, this ball should be left as No Connect.
For iTPM Enable
No Reboot Strap
SPKR | LOW = Defaule
High=No Reboot
USB
Pair | Device
0 | USB1
1 | USB4
2 | USB2
3 | DOCK
4 | USB3
5 | Bluetooth
6 | FingerPrint
7 | MINIC1
8 | WEBCAM
9 | NEW1
10 | MINIC2
11 | NC
BOOT BIOS Strap
PCI_GNT#0 | SPI_CS#1 | BOOT BIOS Location
0 | 1 | SPI
1 | 0 | PCI
1 | 1 | LPC(Default)
A16 swap override strap
PCI_GNT#3 | low = A16 swap override enable
high = default
PCI_GNT#0 and SPI_CS1# have weak internal Pull up
These R need close SB within 600 mils
PlanarID
(1,1)
SA: 0,0
SB: 0,1
SC: 1,0
-1: 1,1
2nd = 83.00016.F11
2nd = 83.BAT54.D81
Four Peaks
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9-M (2 of 4)
Size
Document Number
Four Peaks
Rev
-1M
Date: Friday, November 21, 2008
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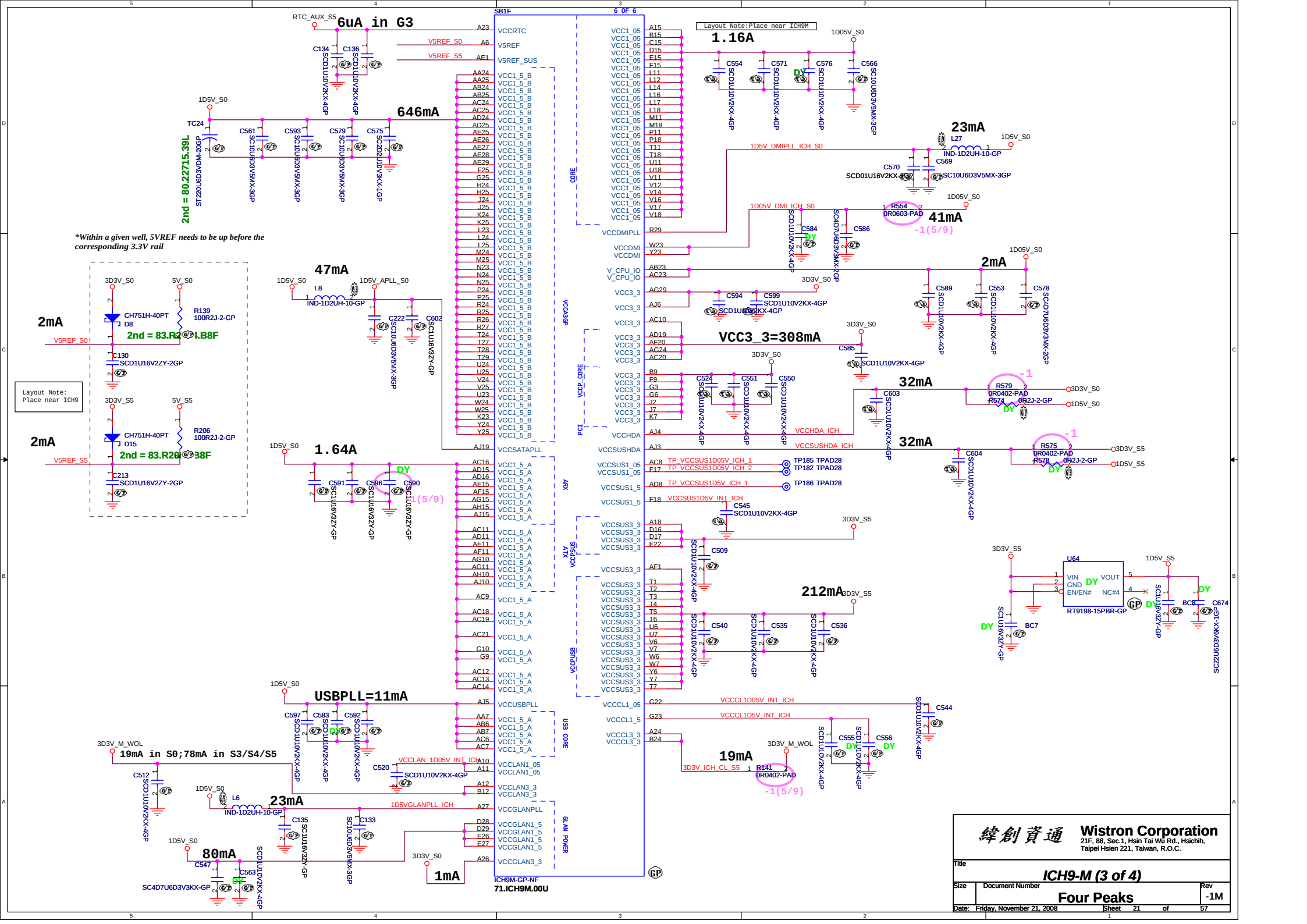
6uA in G3
646mA
2nd = 80.22715.39L
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
2mA
2nd = 83.R2[illegible]I.B8F
Layout Note: Place near ICH9
2mA
2nd = 83.R20[illegible]38F
47mA
1.64A
USBPLL=11mA
19mA in S0;78mA in S3/S4/S5
23mA
80mA
1mA
1.16A
23mA
41mA
-1(5/9)
2mA
VCC3_3=308mA
32mA
32mA
212mA
19mA
SB1F
6 OF 6
ICH9M-GP-NF
71.ICH9M.00U
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ICH9-M (3 of 4)
Four Peaks
-1M
Friday, November 21, 2008
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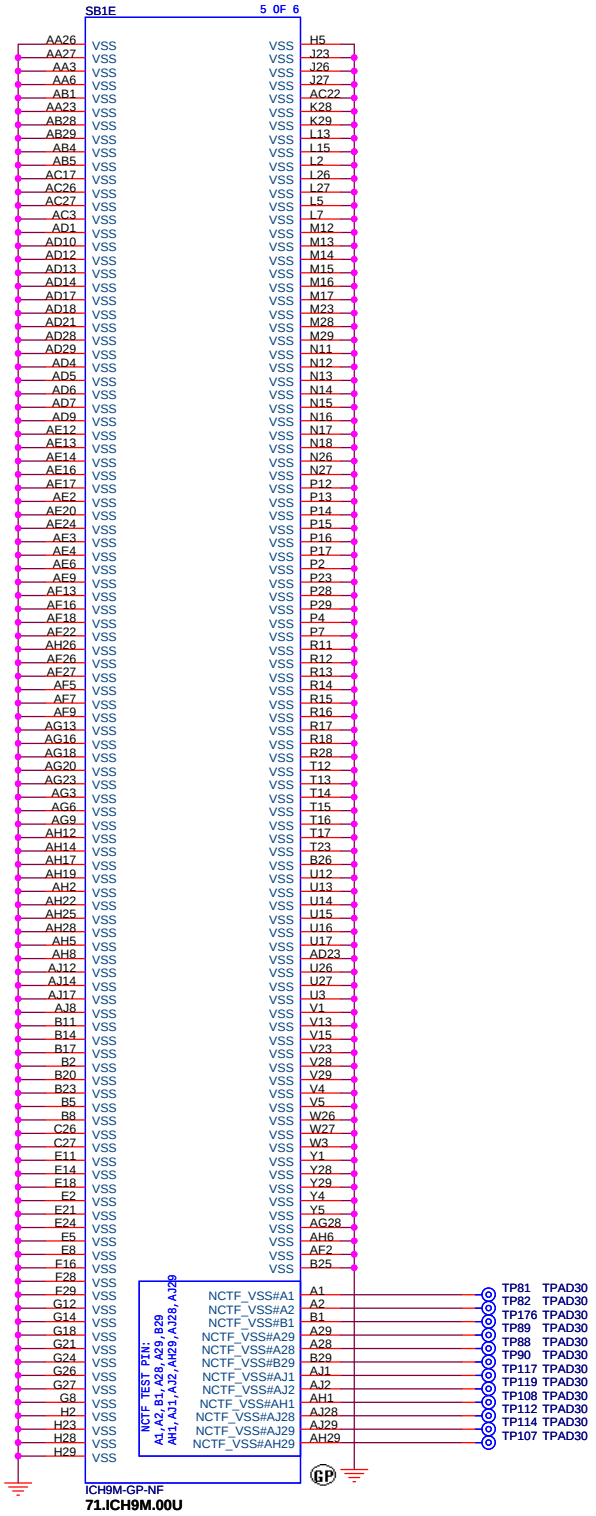

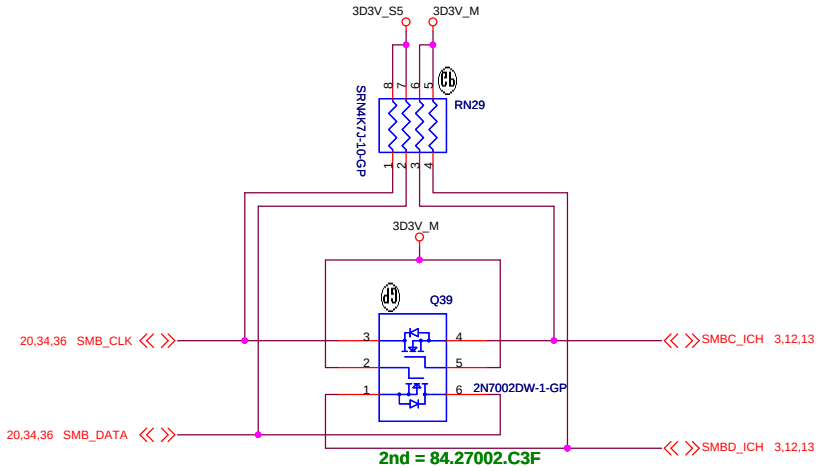

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *ICH9-M (4 of 4)*

Size | Document Number: **Four Peaks** | Rev: -1M

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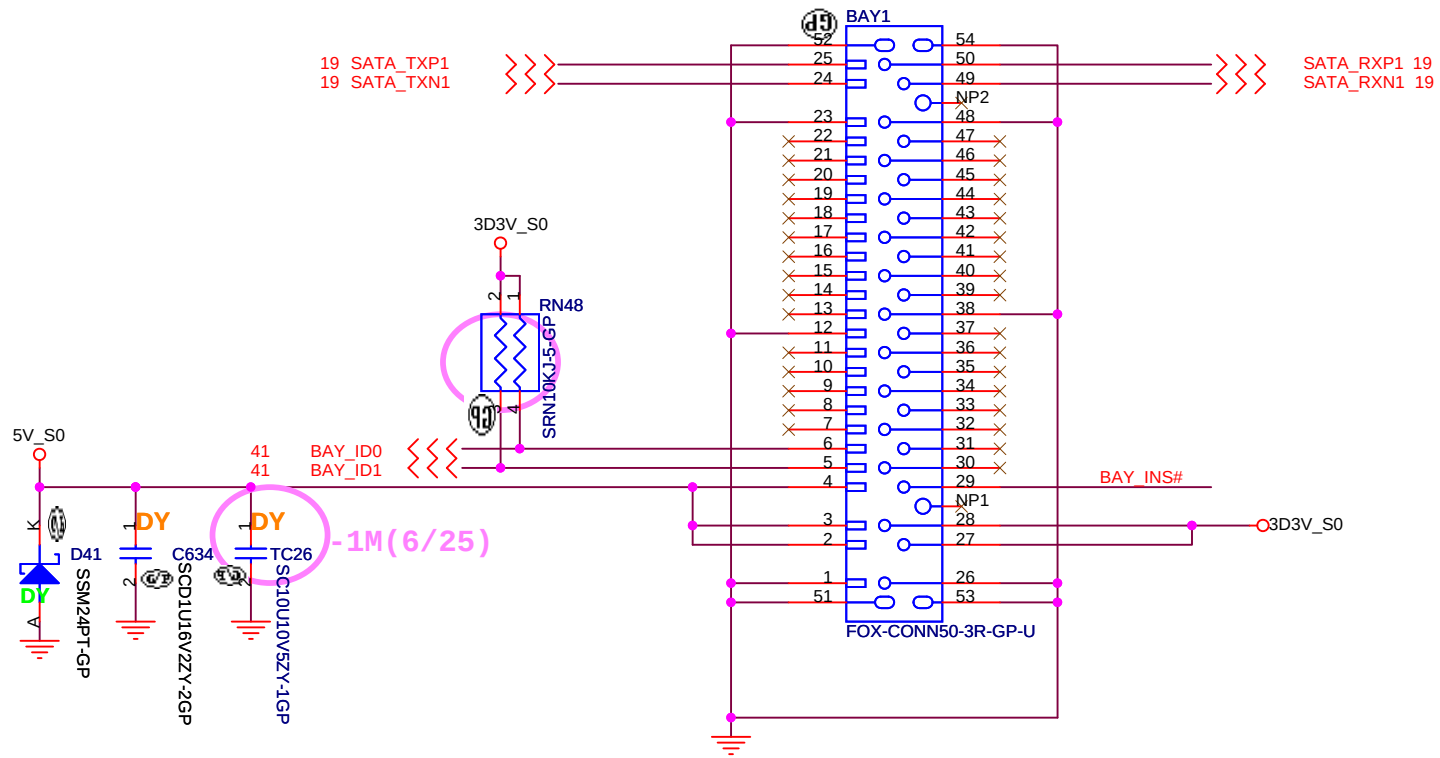
ODD Connector

ODD Conn. Test Point

SATA_TXP1	TP125 TPAD30
SATA_TXN1	TP124 TPAD30
SATA_RXP1	TP127 TPAD30
SATA_RXN1	TP126 TPAD30
BAY_ID0	TP194 TPAD30
BAY_ID1	TP195 TPAD30
BAY_INS#	TP193 TPAD30
3D3V_S0	TP277 TPAD30
5V_S0	TP278 TPAD30



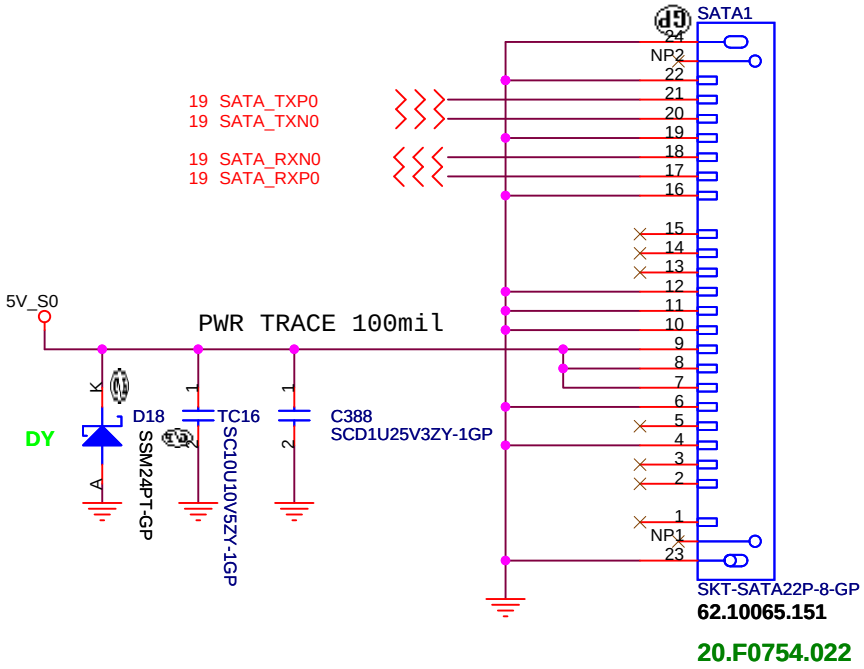
	BAY_ID0	BAY_ID1
SATA ODD	0	0
SATA HDD	1	1

Four Peaks

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	ODD	
Size	Document Number: Four Peaks	Rev: -1M
Date: Friday, November 21, 2008	Sheet 23 of 57	

SATA Connector

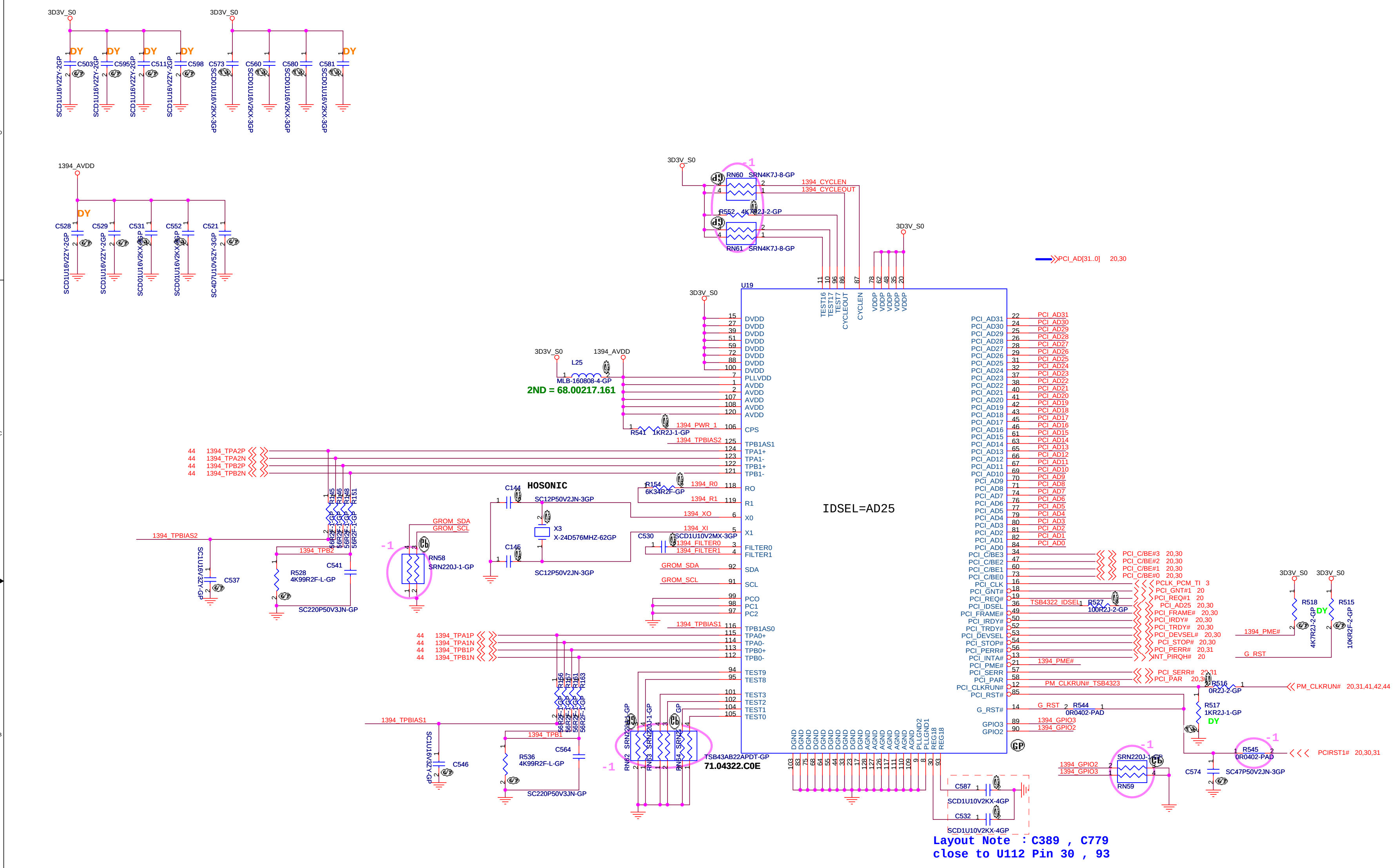


HDD Conn. Test Point

Four Peaks

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***HDD CONN***	
Size	Document Number **Four Peaks**	Rev -1M
Date: Friday, November 21, 2008	Sheet 24 of 57	


3D3V_S0
1394_AVDD
RN60 SRN4K7J-8-GP
RN61 SRN4K7J-8-GP
1394_CYCLEN
1394_CYCLEOUT
PCI_AD[31..0] 20,30
U19
IDSEL=AD25
2ND = 68.00217.161
L25
MLB-160808-4-GP
HOSONIC
X3
X-24D576MHZ-62GP
SC12P50V2JN-3GP
RN58
SRN220J-1-GP
R528
4K99R2F-L-GP
R536
4K99R2F-L-GP
SC220P50V3JN-GP
TSB43AB22APDT-GP
71.04322.C0E
1394_TPA2P
1394_TPA2N
1394_TPB2P
1394_TPB2N
1394_TPA1P
1394_TPA1N
1394_TPB1P
1394_TPB1N
1394_TPBIAS1
1394_TPBIAS2
GROM_SDA
GROM_SCL
PM_CLKRUN# 20,31,41,42,44
PCIRST1# 20,30,31
R545
0R0402-PAD
RN59
SRN220J
Layout Note : C389 , C779
close to U112 Pin 30 , 93

Four Peaks

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	TSB43AB22A	
Size	Document Number: Four Peaks	Rev: -1M
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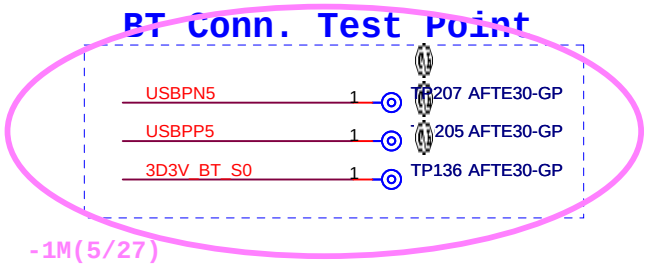
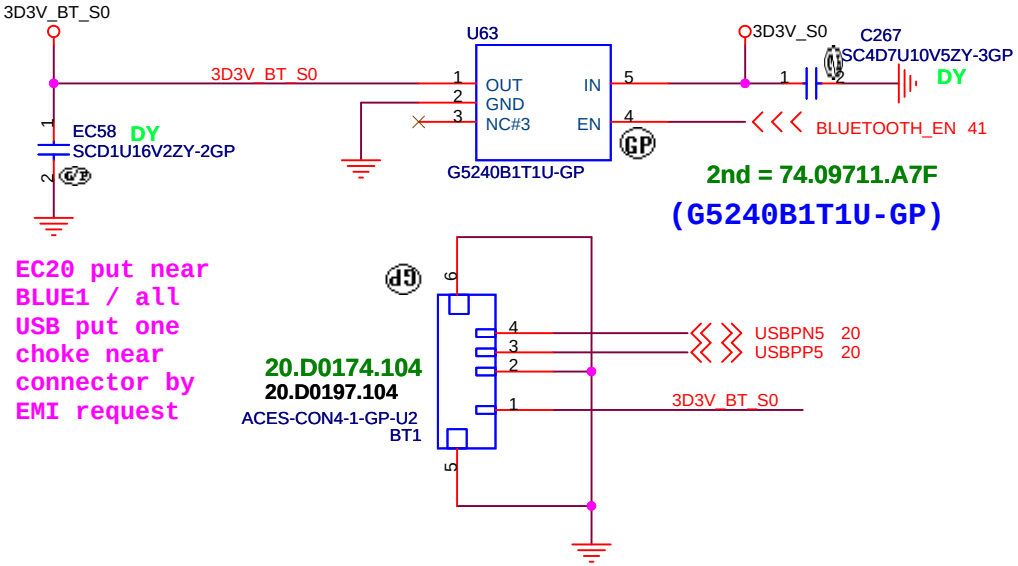
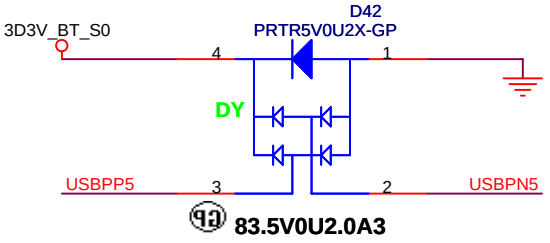
BLUETOOTH MODULE







Need check conn.

Four Peaks

綽創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***BLUETOOTH***

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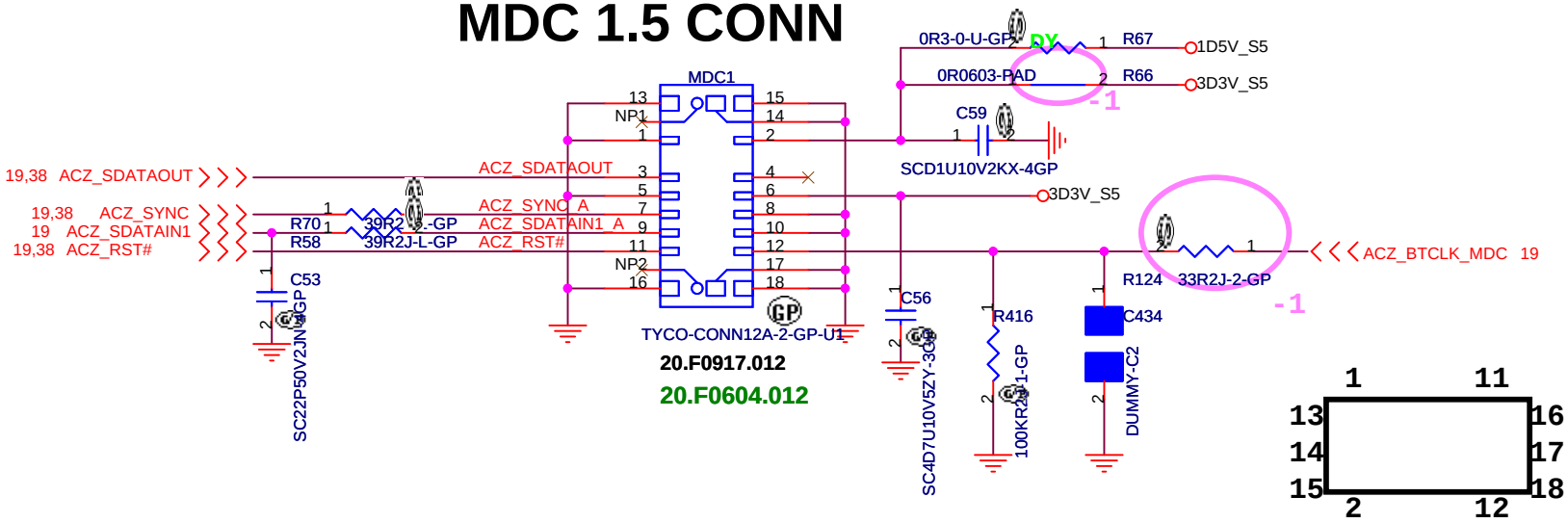
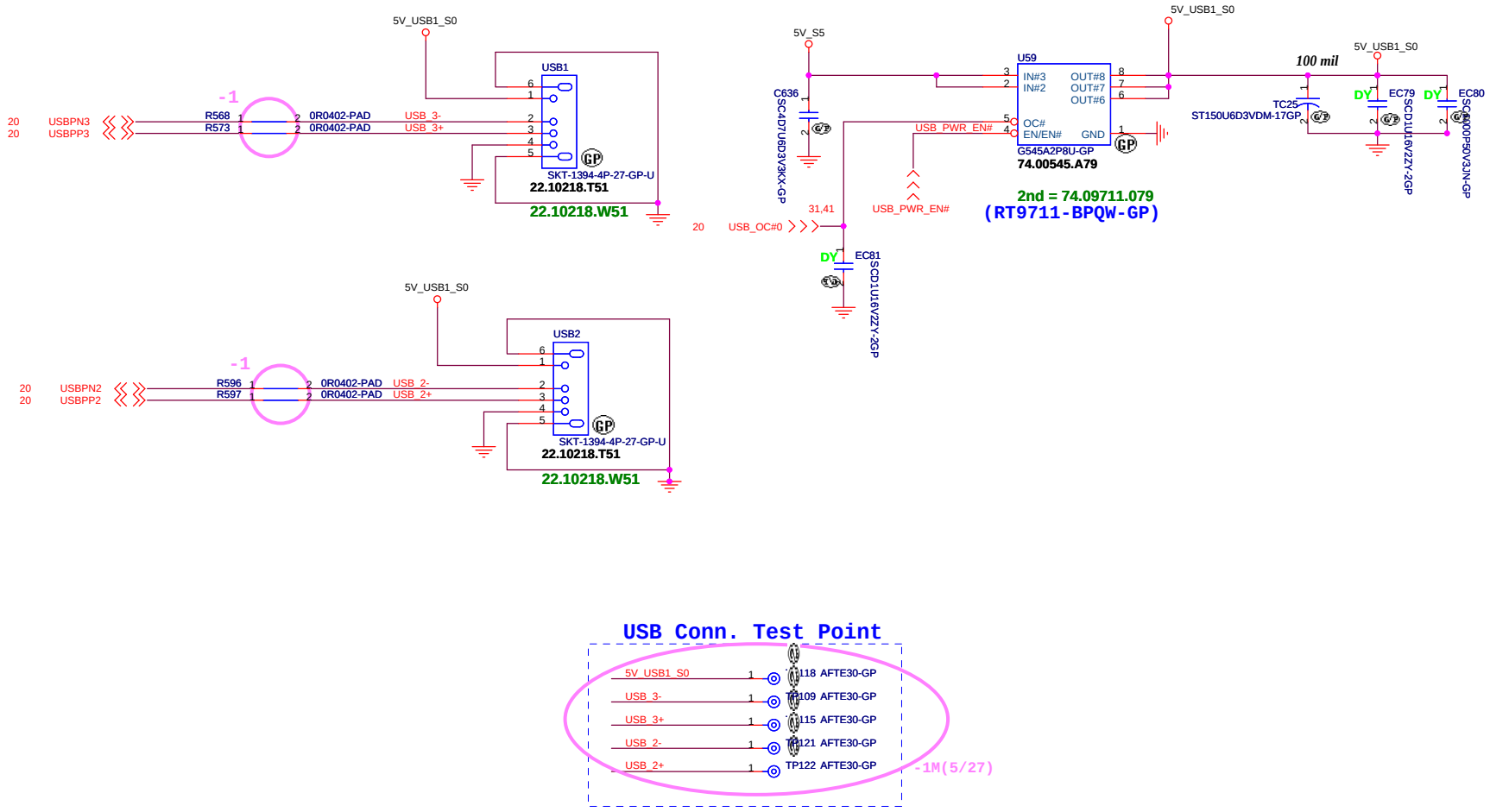
MDC 1.5 CONN



Four Peaks

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***MDC***	
Size	Document Number **Four Peaks**	Rev -1M
Date: Friday, November 21, 2008	Sheet 27 of	57



USB Conn. Test Point

Four Peaks

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *USB*		
Size	Document Number: Four Peaks	Rev: -1M
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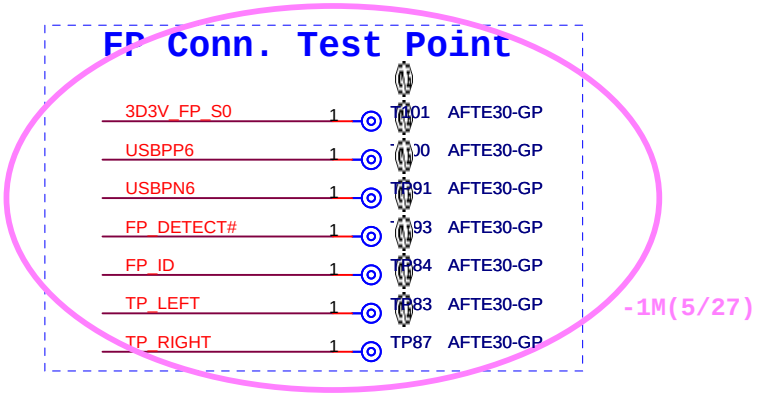
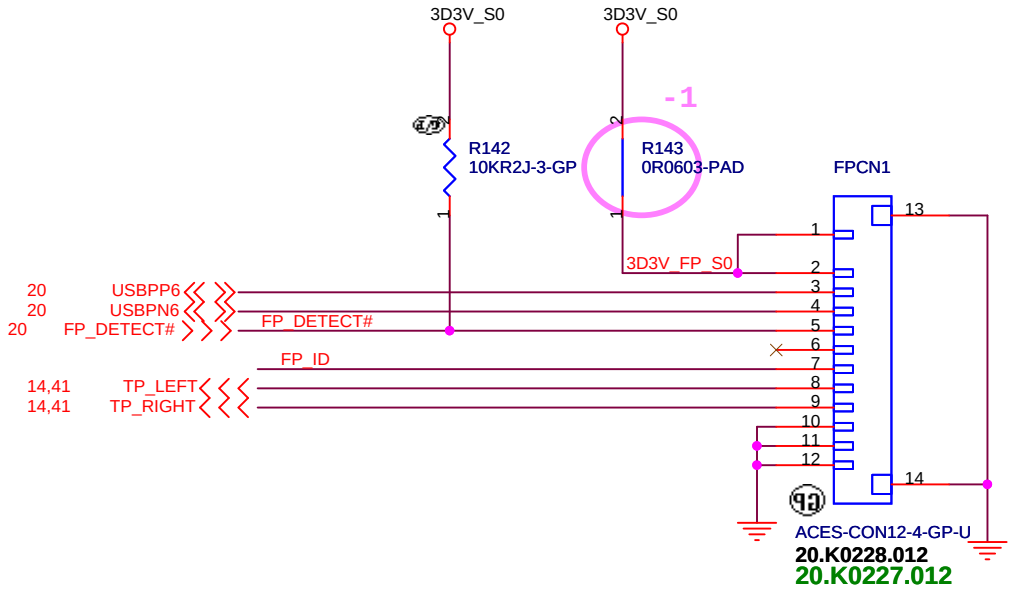
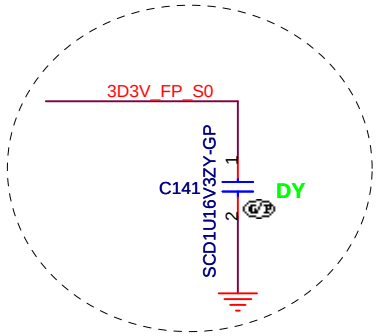
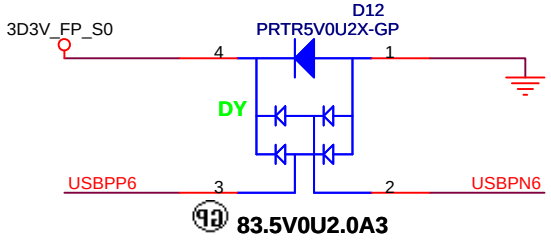
Finger printer







For EMI



Four Peaks

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Finger Printer*		
Size	Document Number: Four Peaks	Rev: -1M
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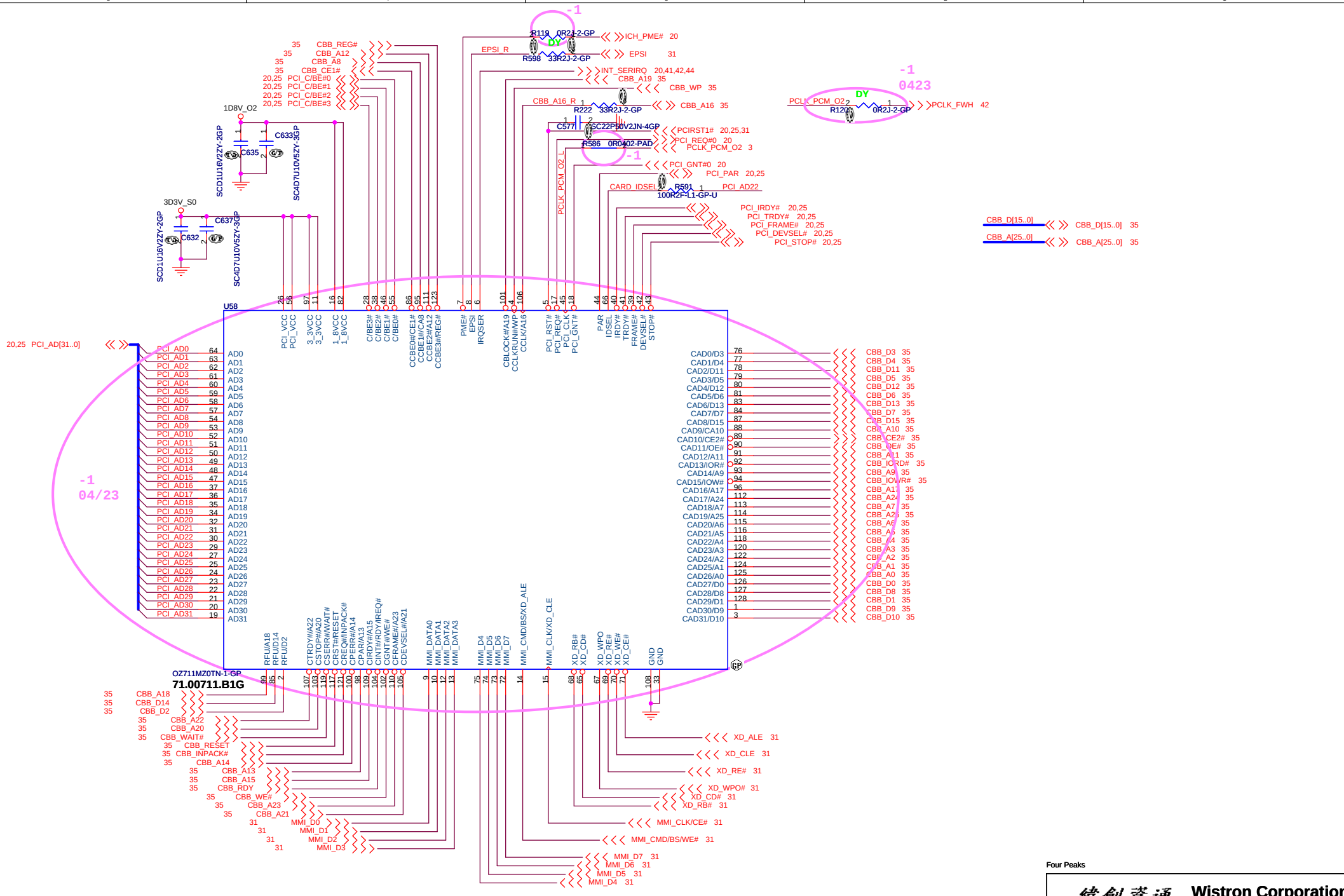

Four Peaks

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Card Reader - OZ711MZ0*

Size	Document Number	Rev
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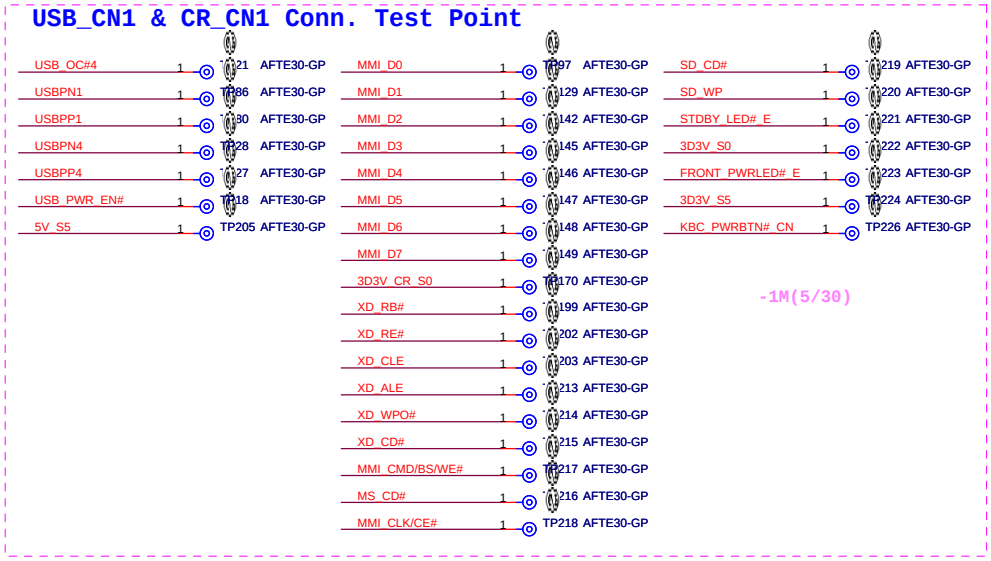

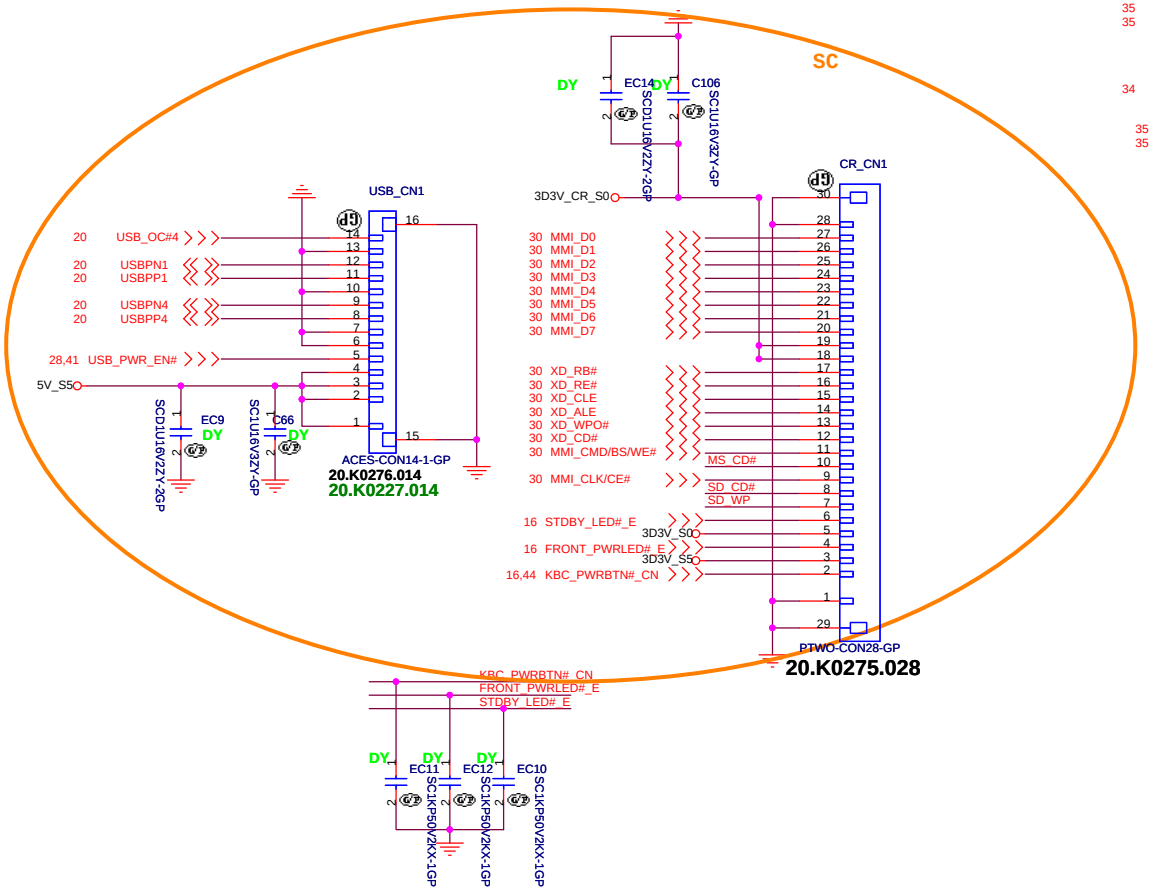

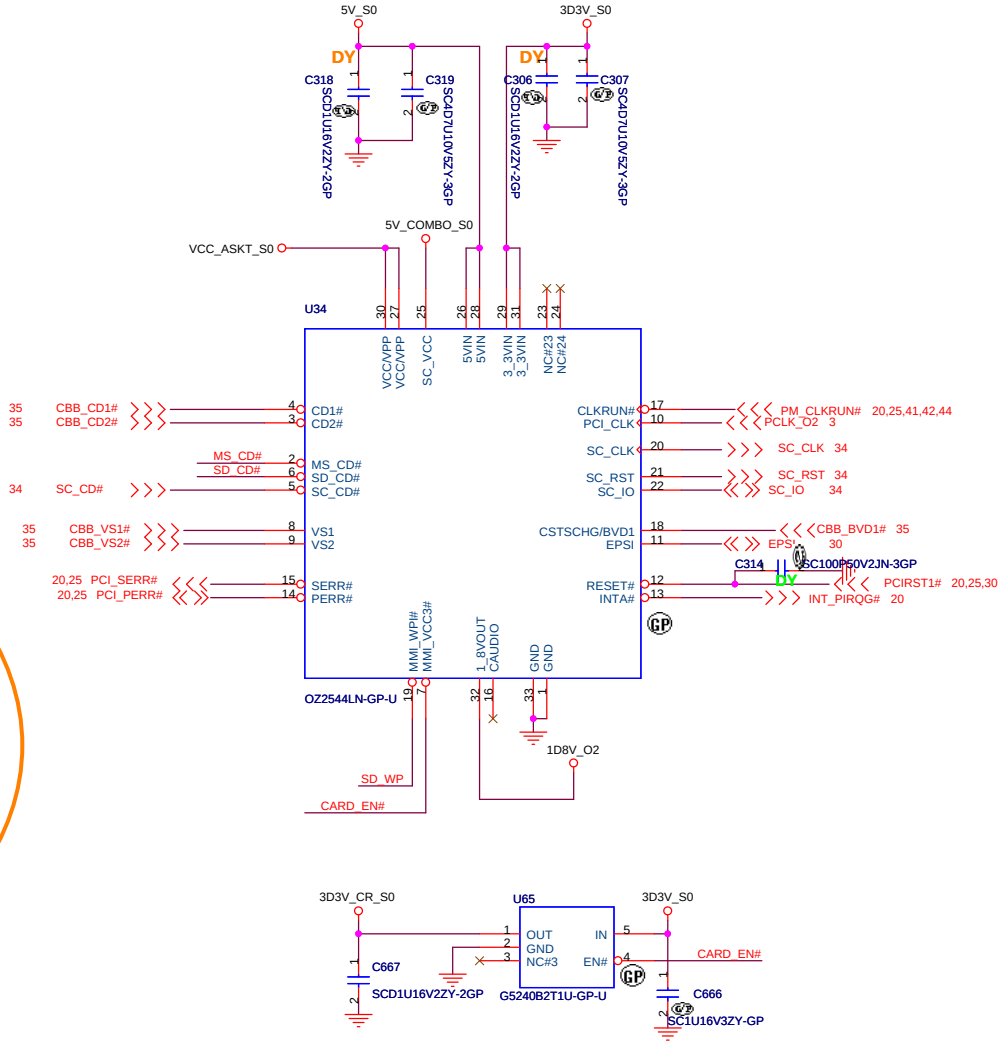

Four Peaks

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Card Reader Connector

Size	Document Number	Rev
	Four Peaks	-1M

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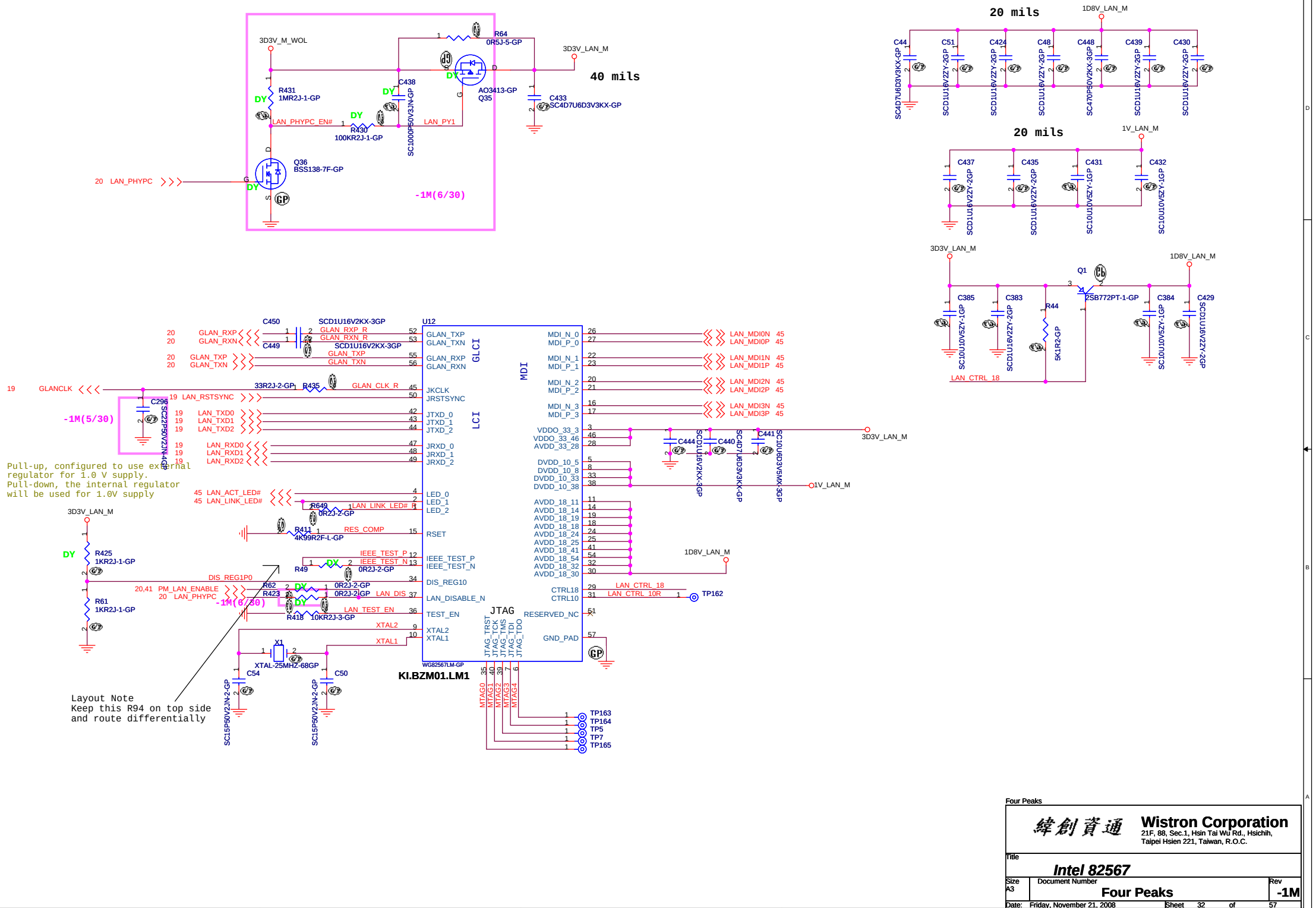

Four Peaks

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Intel 82567***

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A3	**Four Peaks**	**-1M**

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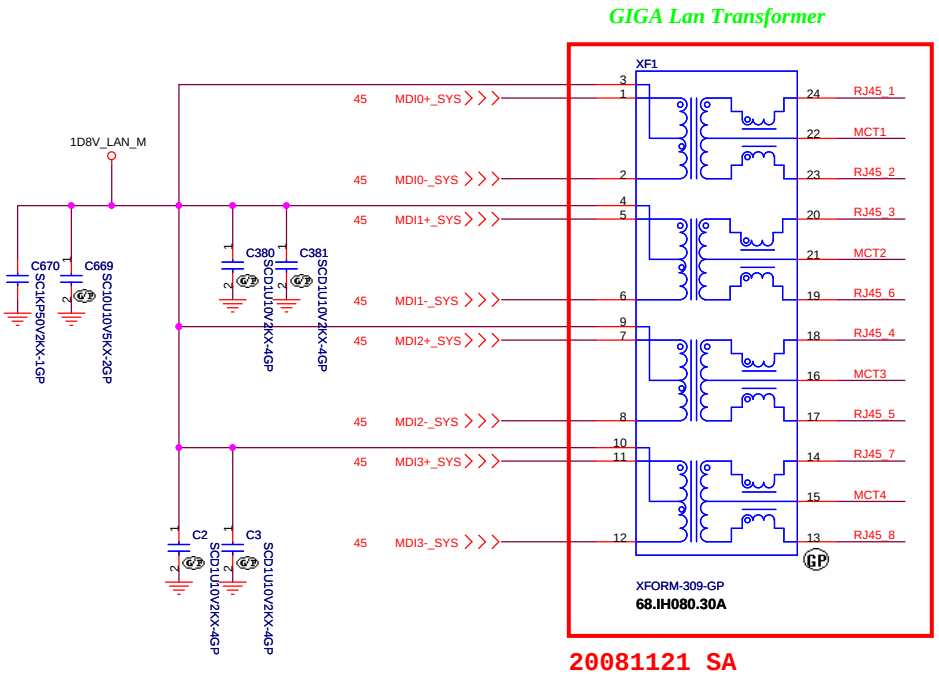
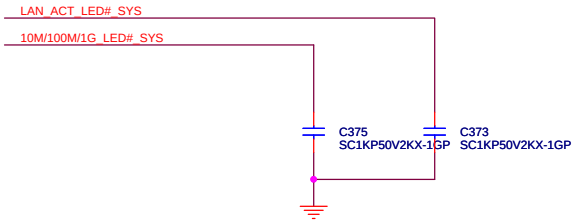
LAN Connector

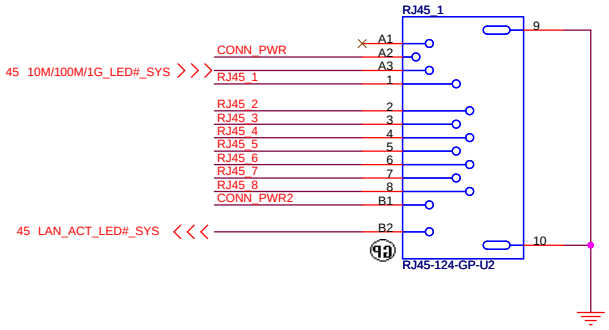
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

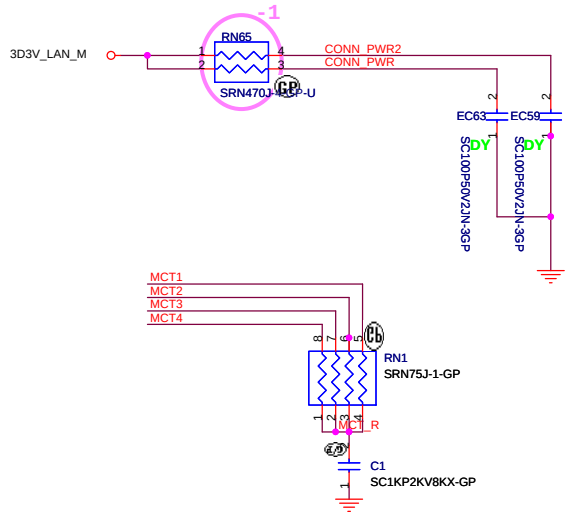


20081121 SA
change to 68.IH080.30A



LAN Connector





Four Peaks

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LAN CONN	
Size A3	Document Number	Rev -1M
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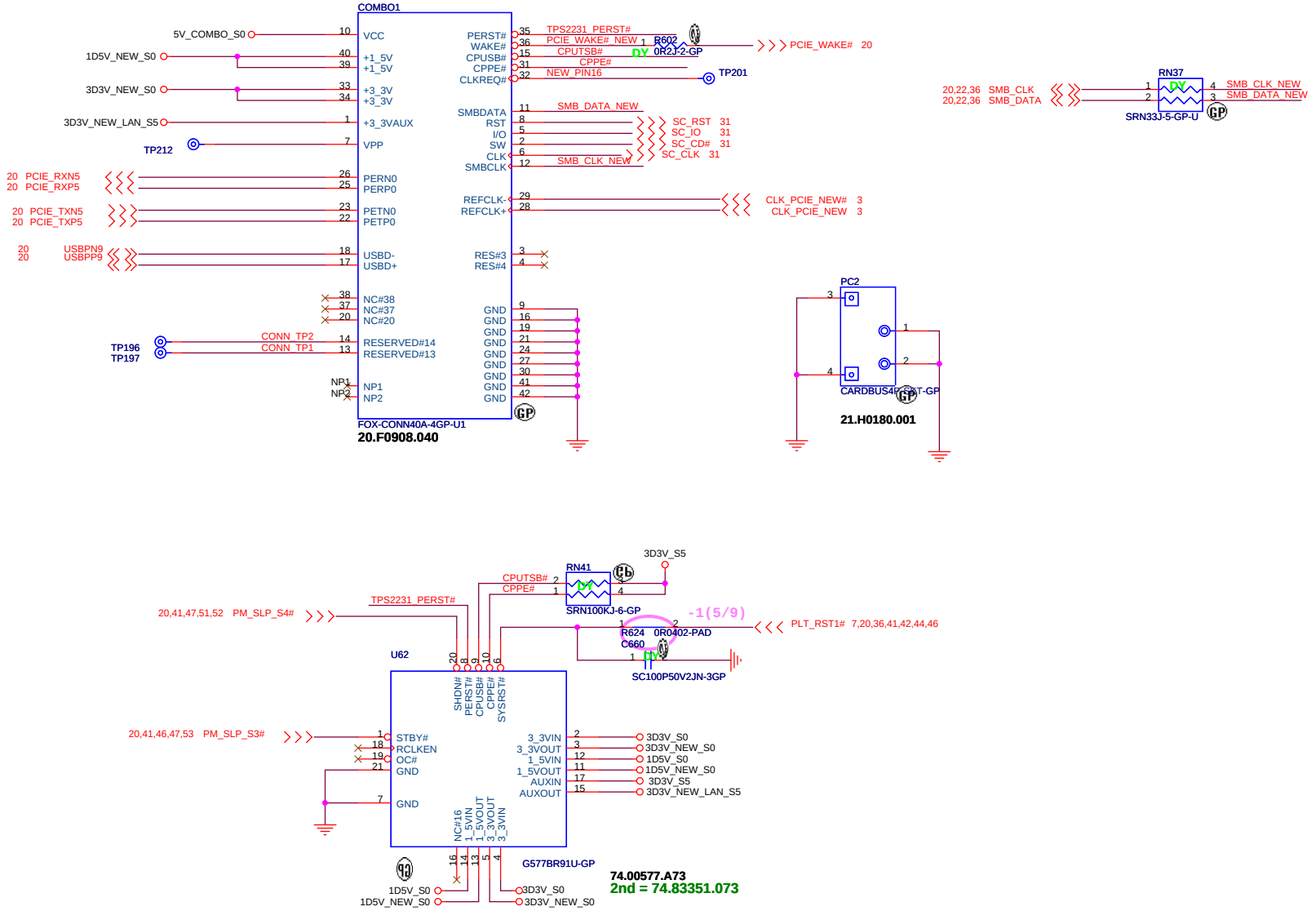

Four Peaks

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **NEW CARD**

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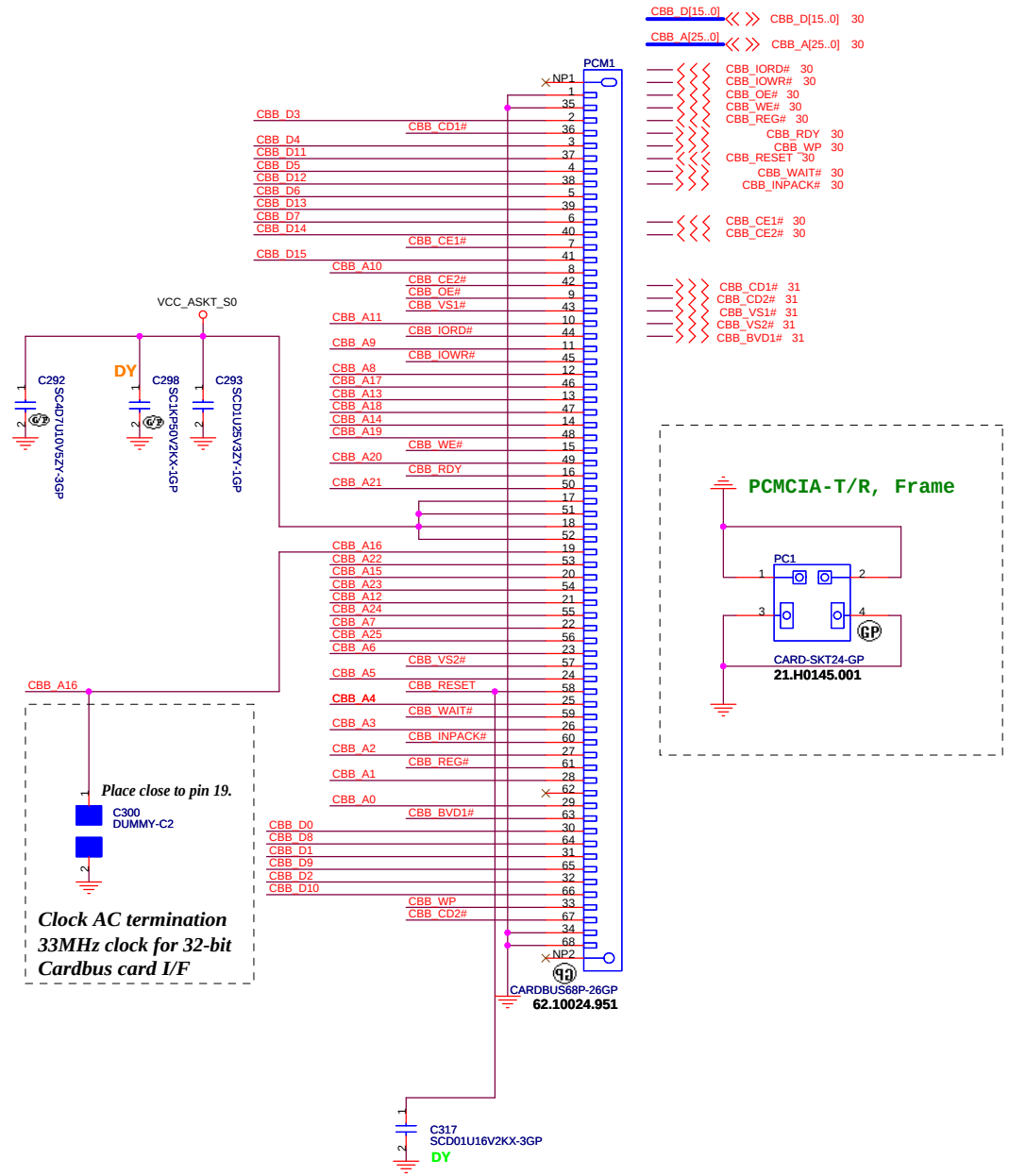
PCMCIA Socket

Cardbus I/F



Four Peaks

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	PCMCIA	
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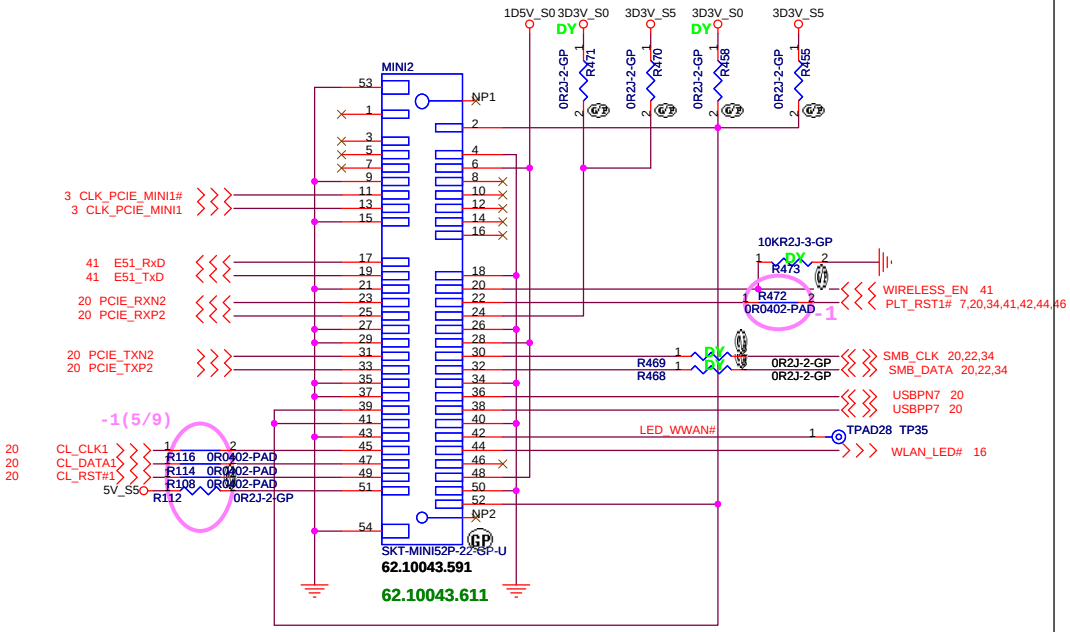
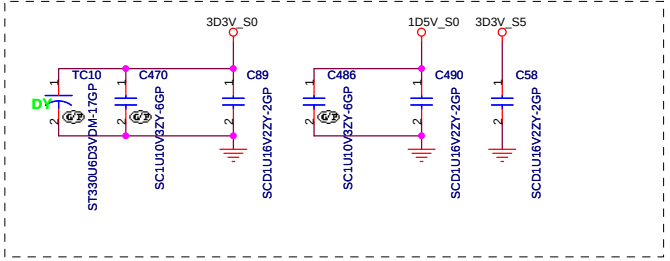
Mini Card Connector(WLAN)

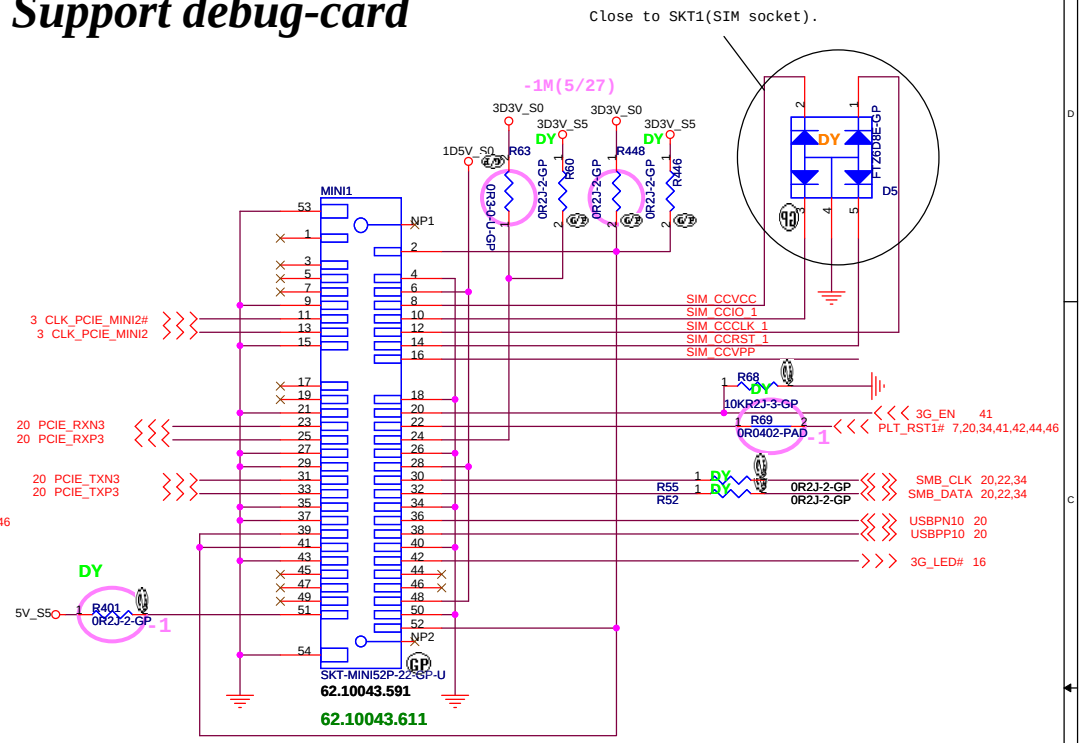


Place near MINIC1

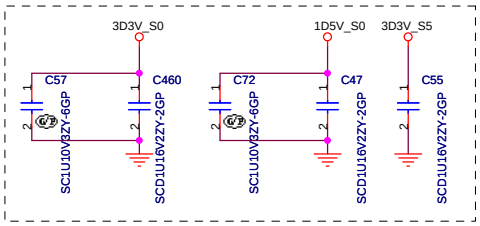


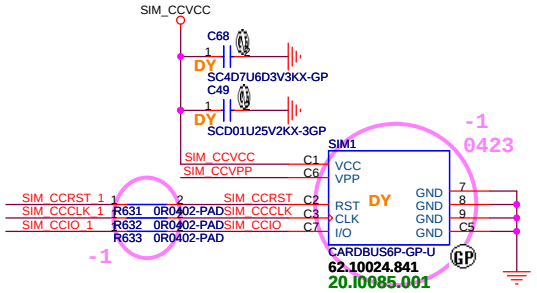
Mini Card Connector(Robson2 and 3G)

Support debug-card



Place near MINIC2





Four Peaks

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	MINI CARD	
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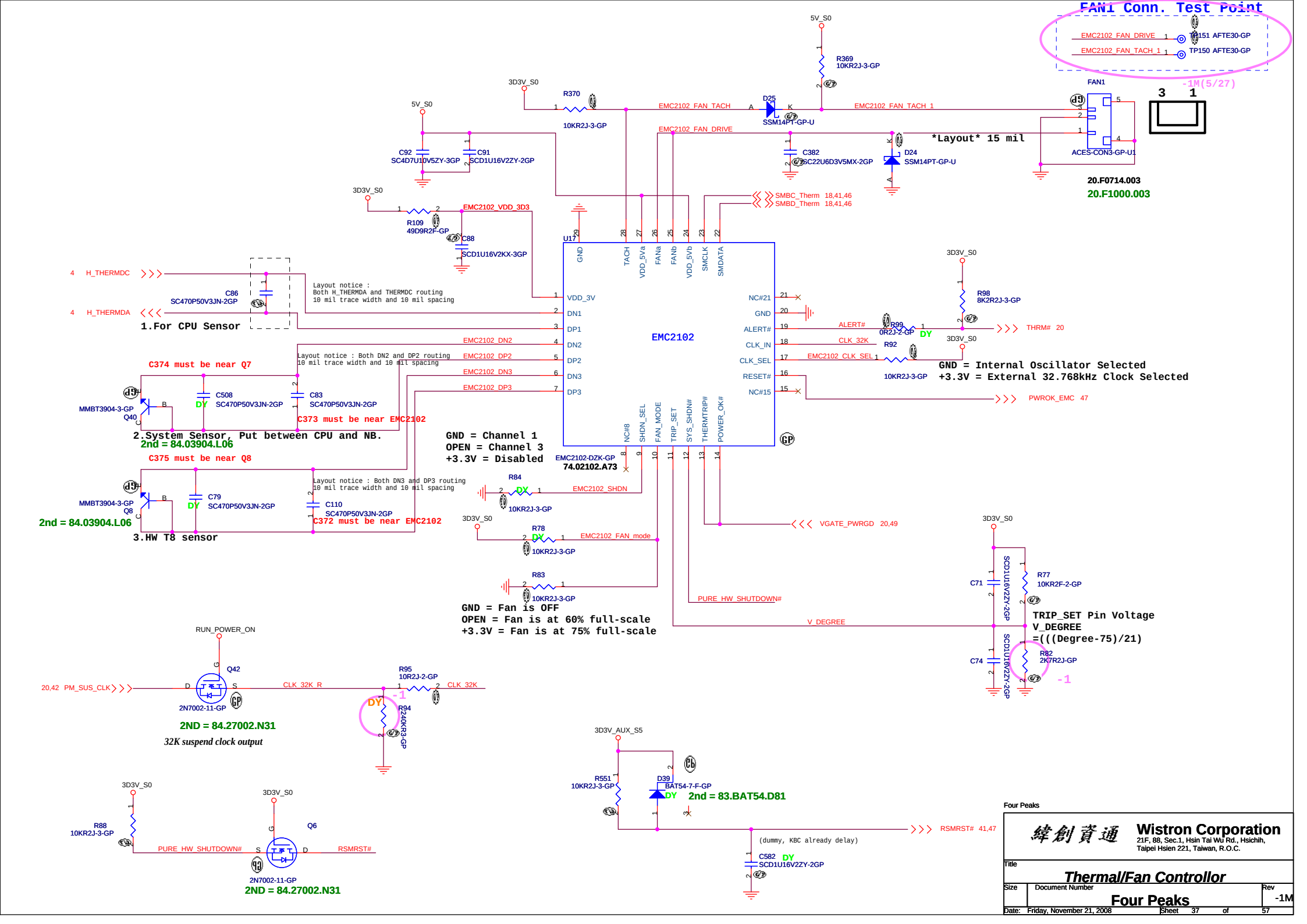

Four Peaks

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Thermal/Fan Controllor***

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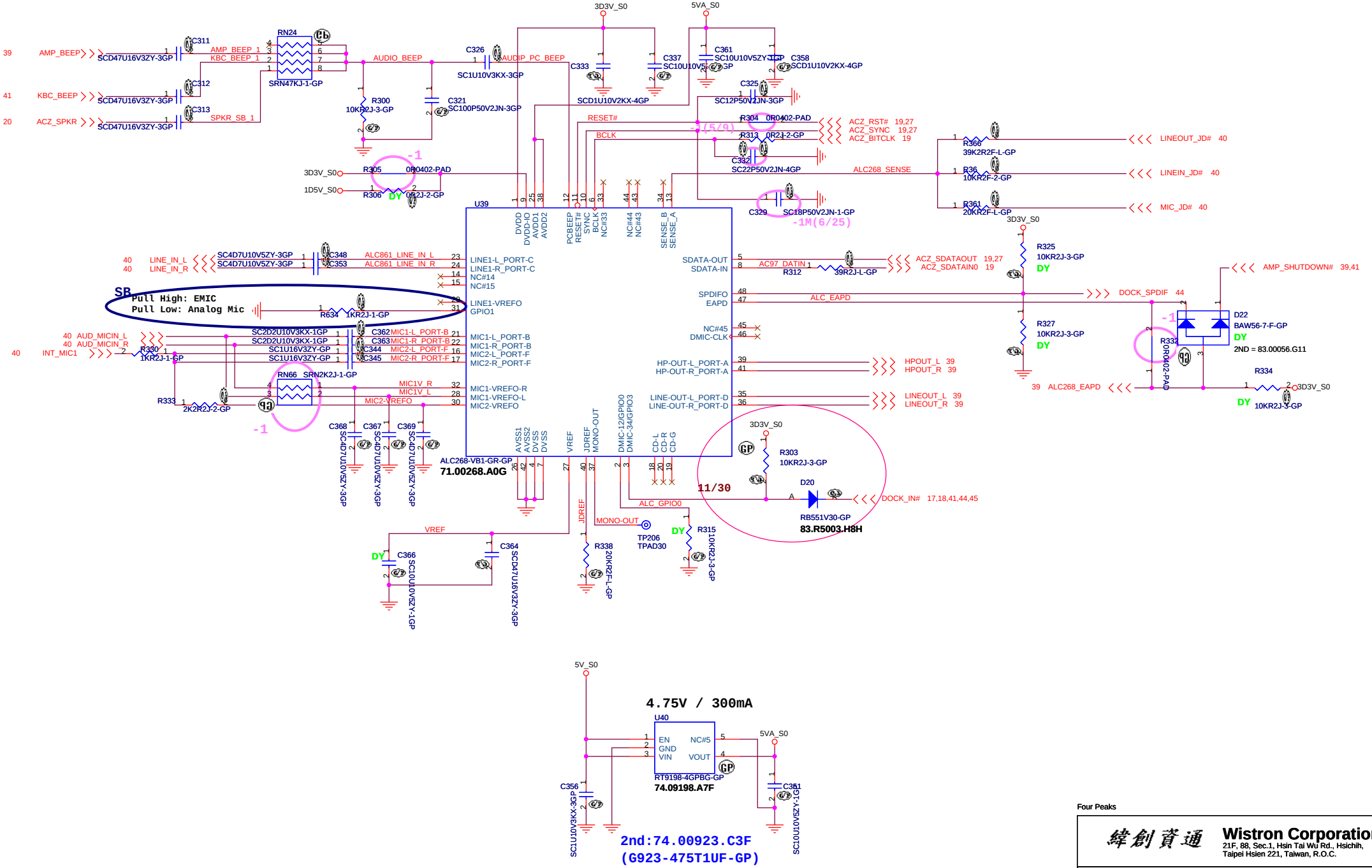

Four Peaks

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Azalia codec ALC268	
Size A3	Document Number: Four Peaks	Rev: -1M
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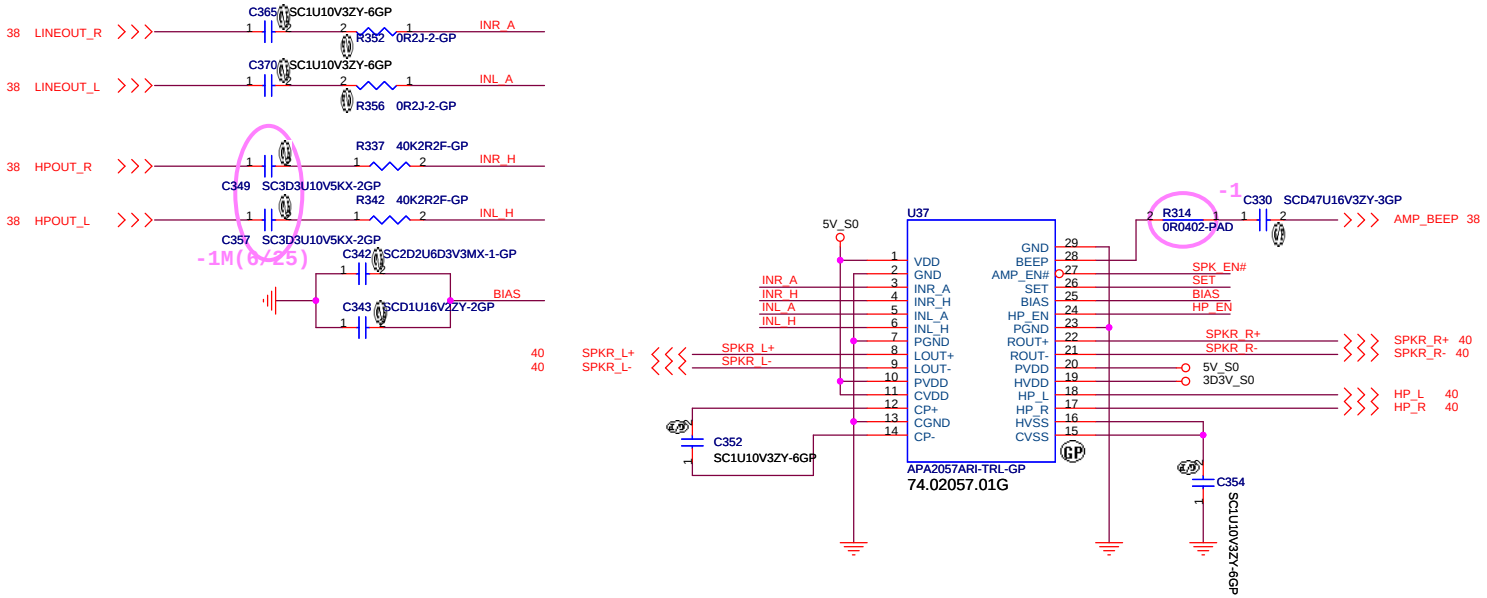
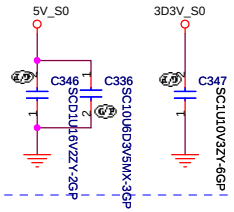
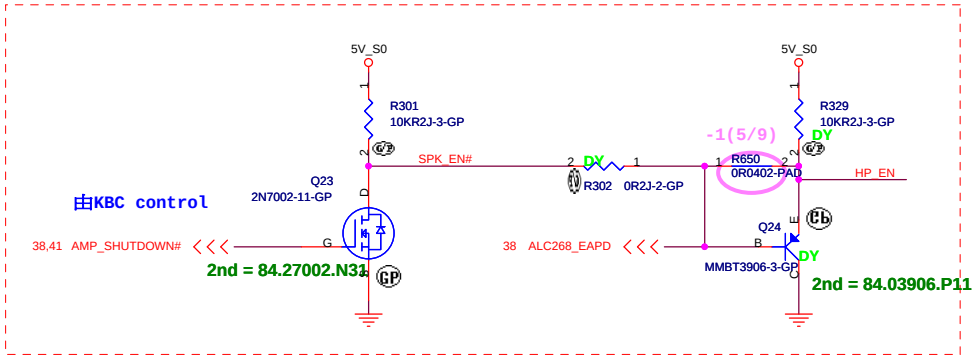
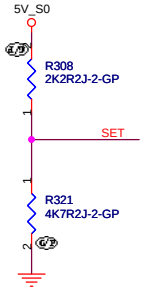
AUDIO OP AMPLIFIER



Layout Note :
C218,C219,C220 near U110







Four Peaks

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	AUDIO AMP	
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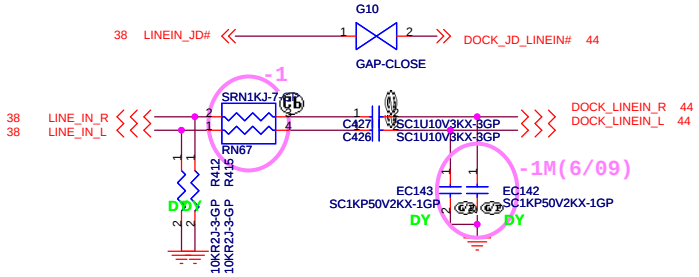
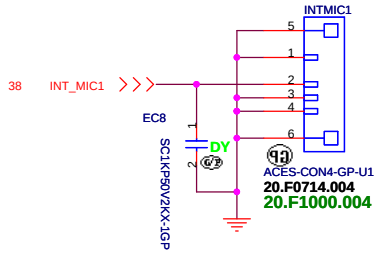
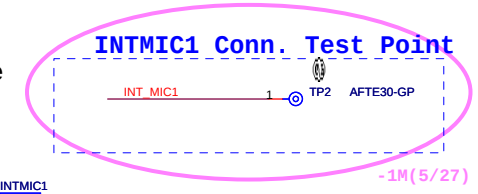
LINE IN



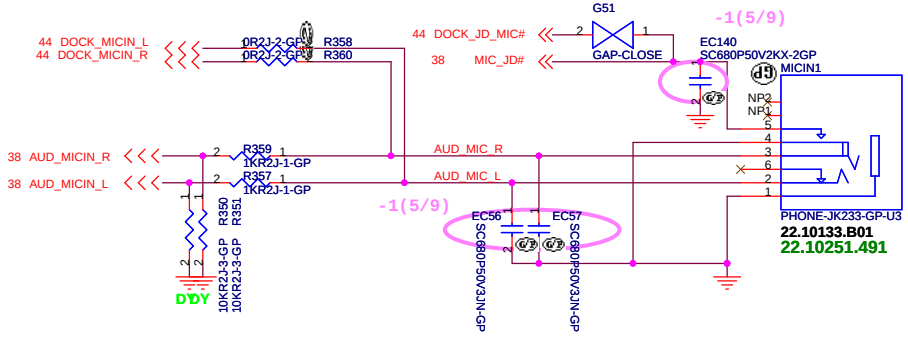
Internal Microphone



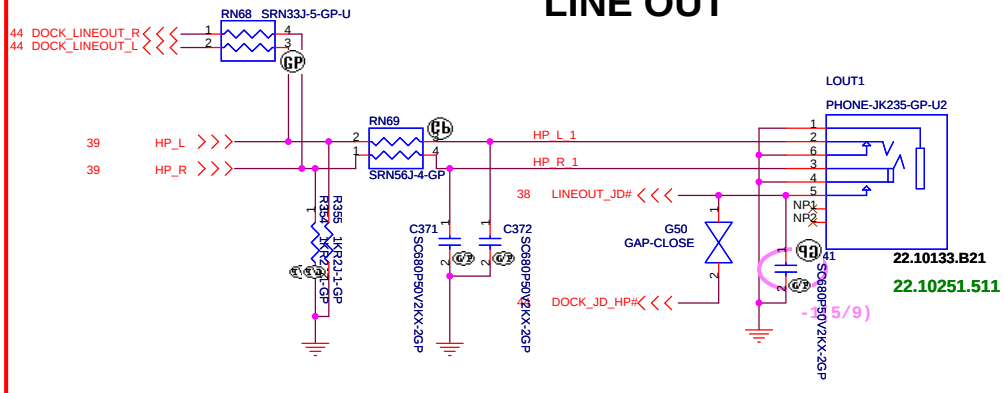
INTMIC1 Conn. Test Point



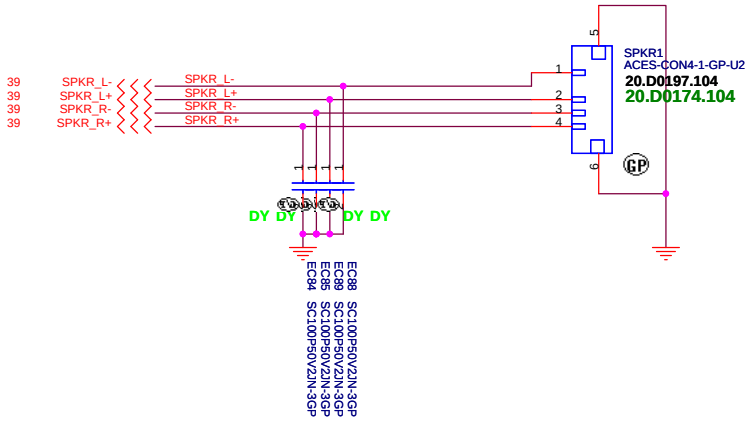
MIC IN



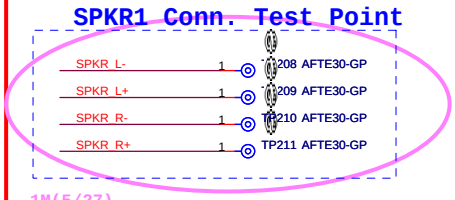
LINE OUT



Internal Speaker



SPKR1 Conn. Test Point



Four Peaks

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	AUDIO JACK	
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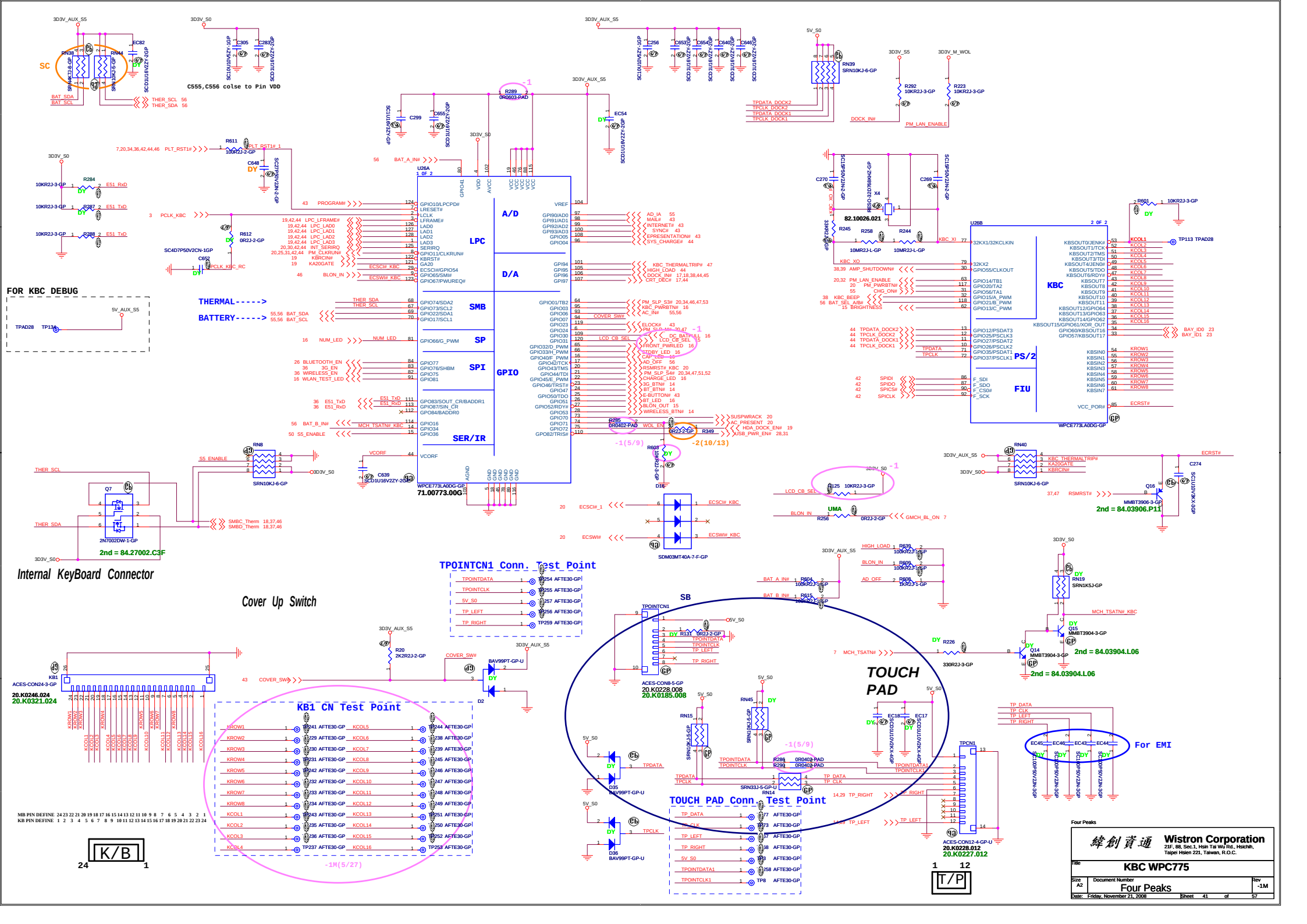
FOR KBC DEBUG
Internal KeyBoard Connector
Cover Up Switch
TPOINTCN1 Conn. Test Point
KB1 CN Test Point
TOUCH PAD Conn. Test Point
TOUCH PAD
SB
THERMAL----->
BATTERY----->
C555,C556 colse to Pin VDD
2nd = 84.27002.C3F
2nd = 84.03906.P11
2nd = 84.03904.L06
2nd = 84.03904.L06
20.K0246.024
20.K0321.024
20.K0228.008
20.K0185.008
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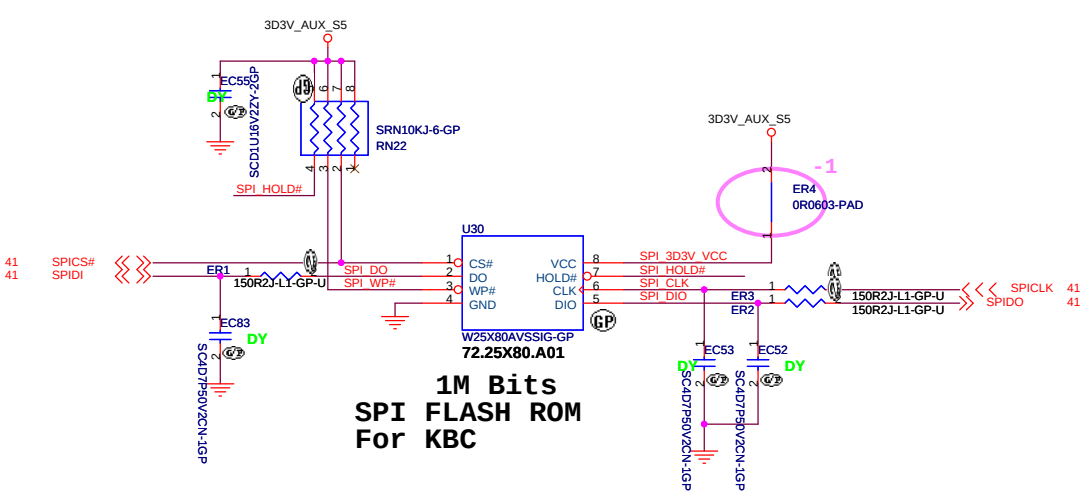
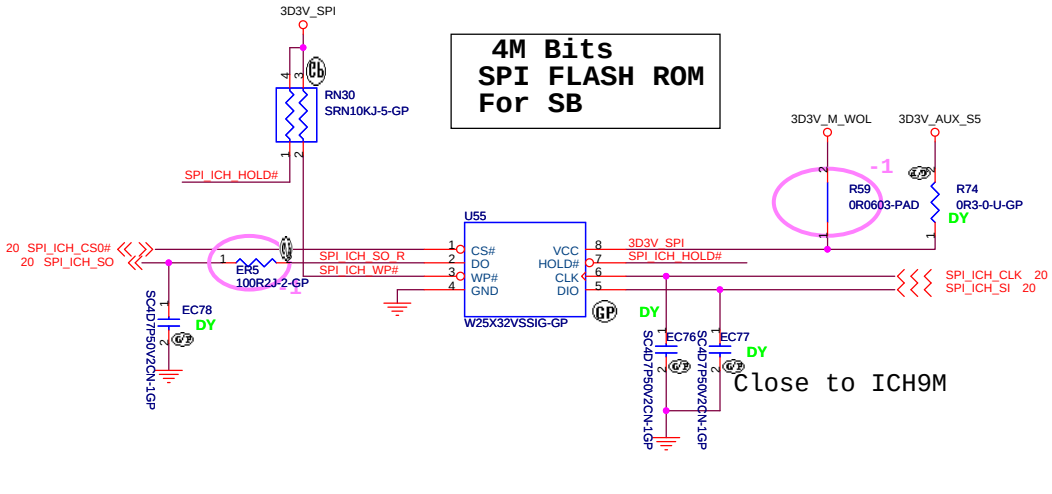
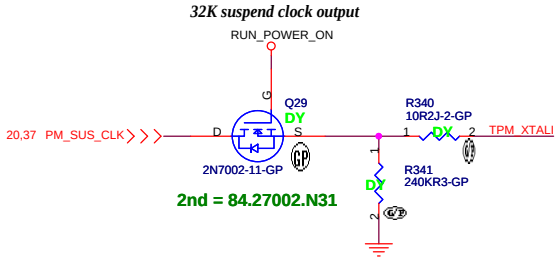
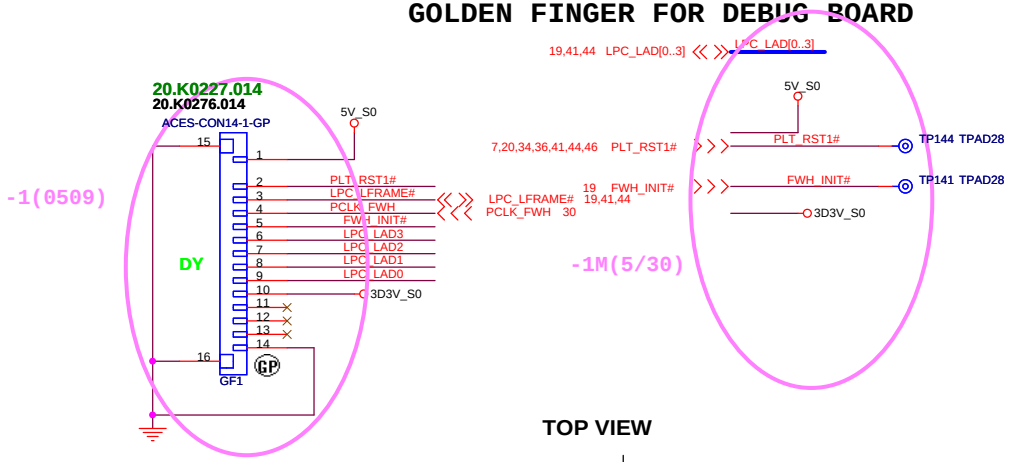
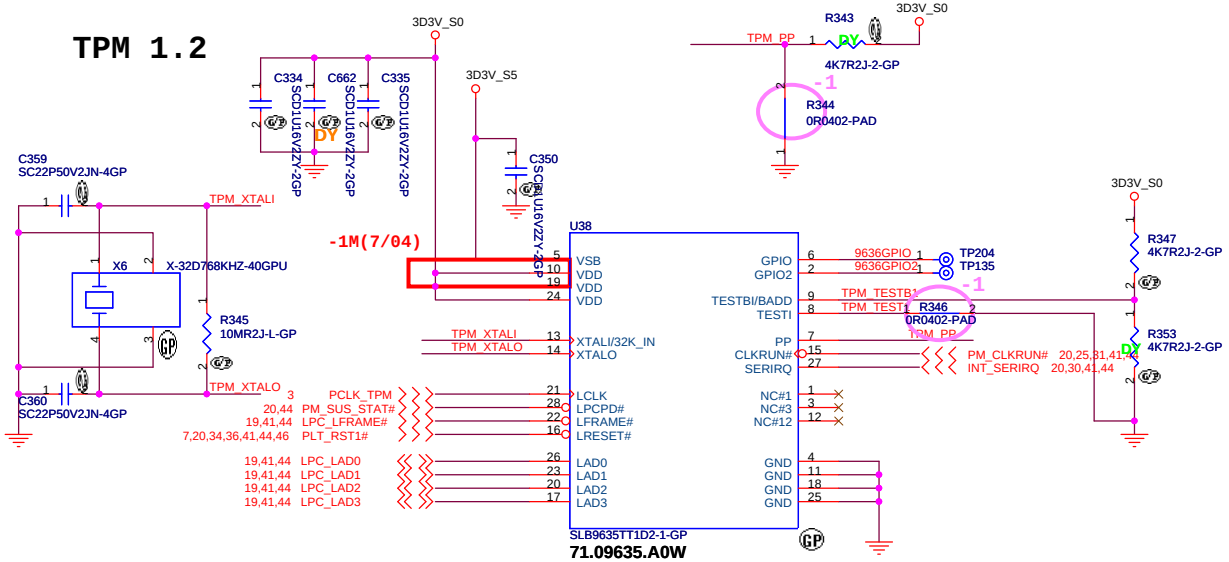
71.00773.00G
Wistron Corporation
KBC WPC775
Four Peaks
Rev -1M











TOP VIEW

A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

(BOTTOM VIEW)

Four Peaks

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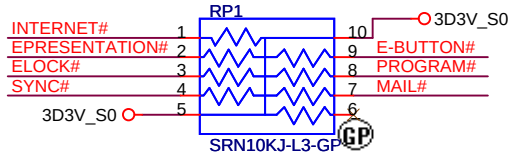
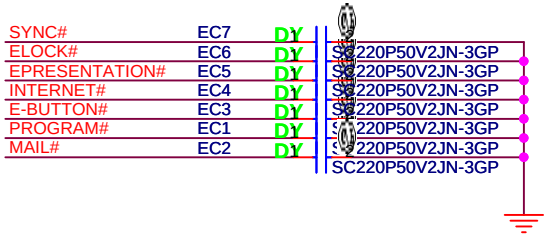
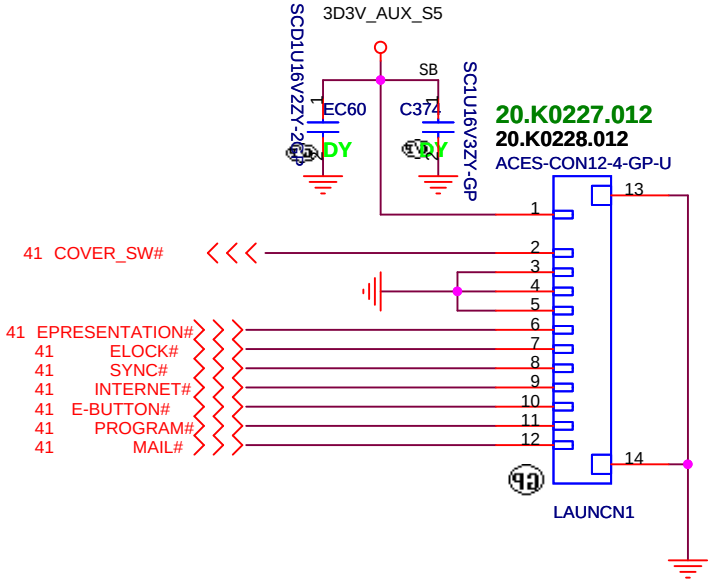
Title: BIOS & TPM

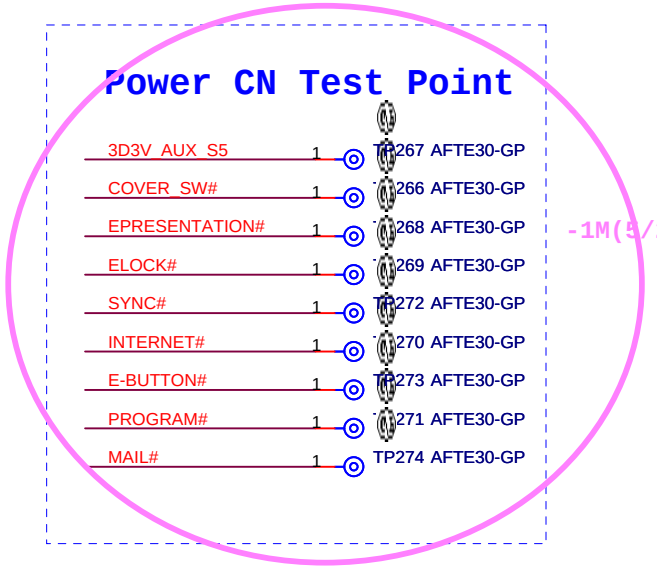
Size	Document Number	Rev
	Four Peaks	-1M

Date: Friday, November 21, 2008 Sheet 42 of 57









Four Peaks

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***LAUNCH***

Size	Document Number	Rev
	Four Peaks	-1M

Date: Friday, November 21, 2008 Sheet 43 of 57

CRT SWITCH

Function	CRT
SYSTEM	H
DOCK	L

Power CN Test Point

DOCK_TIP_1 — TP276 AFTE30-GP
DOCK_RING_1 — TP275 AFTE30-GP

-1M(5/27)

DOCKRING1 — ETY-CON2-10-GP
20.F0984.002
20.F0070.002

L1 BK1608HM102-T-GP (DOCK_TIP)
L2 BK1608HM102-T-GP (DOCK_RING)

-1(5/9)

CRT_R_DOCK — EC70 SC1U8P50V2JN-1GP — FCB1608CF-GP — R_DOCK_R
CRT_G_DOCK — EC71 SC1U8P50V2JN-1GP — FCB1608CF-GP — R_DOCK_G
CRT_B_DOCK — EC72 SC1U8P50V2JN-1GP — FCB1608CF-GP — R_DOCK_B

R407 R408 R409

C421 C422 C423 SC12P50V2JN-3GP

-1(5/9)

5V_S0 — SCD1U16V2KX-4GP — C78 — U16 PI5C3257QE-GP 73.53257.B0C

CRT_G_SYS, CRT_B_SYS, CRT_R_SYS

CRT_G_DOCK, CRT_B_DOCK, CRT_R_DOCK

CRT_G_1, CRT_B_1, CRT_R_1

0R2J-2-GP — R104 DIS CRT_GREEN 46
0R2J-2-GP — R105 UMA GMCH_GREEN 7
0R2J-2-GP — R101 DIS CRT_BLUE 46
0R2J-2-GP — R102 UMA GMCH_BLUE 7
0R2J-2-GP — R110 DIS CRT_RED 46
0R2J-2-GP — R111 UMA GMCH_RED 7

DOCK1 — NP1 — NP2 — FOX-CONN1-GP 20.F1202.154

DOCK_AD_JK — RN27 SRN2K2J-1-GP — TMDS_SDA, TMDS_SCL

DOCK_IN# R — 78

1394_TPA1P 25 / 1394_TPA1N 25 — 1394_TPA2P 25 / 1394_TPA2N 25
1394_TPB1P 25 / 1394_TPB1N 25 — 1394_TPB2P 25 / 1394_TPB2N 25

PCIE_TXP4 20 / PCIE_TXN4 20 — DOCK_PCIE_SMB_DT — TP155 TPAD28
PCIE_RXP4 20 / PCIE_RXN4 20 — DOCK_PCIE_SMB_CLK — TP152 TPAD28
DOCK_PCIE_RST# — TP151 TPAD28
DOCK_PCIE_CLKREQ# — R377 0R2J-2-GP
DOCK_PCIE_COPP# — SRN0J-6-GP — CLK_PCIE_DOCK_R / CLK_PCIE_DOCK_R# — RN70 — CLK_PCIE_DOCK 3 / CLK_PCIE_DOCK# 3

SYS_CHARGE# 41
HIGH_LOAD 41

R376 0R0402-PAD — PLT_RST1# 7,20,34,36,41,42,46
USB_OC#3 20 — C390 SC100P50V2JN-3GP

TMDS_SDA 18 / TMDS_SCL 18 / TMDS_HPD_DOCK 18
TMDS_TX2+_DOCK 18 / TMDS_TX2-_DOCK 18
TMDS_TXC+_DOCK 18 / TMDS_TXC-_DOCK 18
TMDS_TX0+_DOCK 18 / TMDS_TX0-_DOCK 18
TMDS_TX1+_DOCK 18 / TMDS_TX1-_DOCK 18

LAN_ACT_LED#_DOCK — 10M/100M/1G_LED#_DOCK — LAN_ACT_LED#_DOCK 45 / 10M/100M/1G_LED#_DOCK 45

MDI0+_DOCK 45 / MDI0-_DOCK 45
MDI1+_DOCK 45 / MDI1-_DOCK 45
MDI2+_DOCK 45 / MDI2-_DOCK 45
MDI3+_DOCK 45 / MDI3-_DOCK 45

3D3V_LAN_M
TPDATA_DOCK2 41 / TPCLK_DOCK2 41
TPDATA_DOCK1 41 / TPCLK_DOCK1 41

COM_SIN1, COM_SOUT1, COM_DSR1#, PRN_PE, PRN_BUSY, PRN_ACK#, PRN_ERROR#, PRN_AUTOFD#, PRN_STROB#
COM_RTS1#, COM_CTS1#, COM_DTR1#, COM_RI_232#, COM_DCD1#, PRN_INIT#, PRN_SLCTIN#
PRN_D0 … PRN_D7, PRN_SLCT

R_DOCK_R, R_DOCK_G, R_DOCK_B

DOCK_HSYNC 17, DOCK_VSYNC 17, DAT_DDC1_9 17, CLK_DDC1_9 17, CRT_DEC# 17
CRT_DEC# PIN SHARE WITH MB CRT DEC# PIN
R652 — CRT_DEC#_R — SC

TV_COMP_DOCK — TP154 TPAD28
TV_CRMA_DOCK — TP157 TPAD28
TV_LUMA_DOCK — TP153 TPAD28

DOCK_LINEIN_L 40 / DOCK_LINEIN_R 40
DOCK_LINEOUT_L 40 / DOCK_LINEOUT_R 40
DOCK_MICIN_L 40 / DOCK_MICIN_R 40 / DOCK_JD_MIC# 40
DOCK_SPDIF 38
DOCK_JD_HP# 40
DOCK_JD_LINEIN# 40

USBPP0 20 / USBPN0 20

KBC_PWRBTN#_CN_DOCK

R651 33R2J-2-GP — DOCK_IN#_R — 17,18,38,41,45 DOCK_IN#

5V_DOCK_S0 — G5 GAP-CLOSE-PWR — 5V_S0
C391 SCD1U10V2KX-5GP

DOCK_TIP — DOCK_RING

DOCK_AGND

G106 GAP-CLOSE-PWR — DOCK_AGND

DOCK_IN# — R380 0R2J-2-GP — C386 SCD1U16V2ZY-2GP
Q31 PDTA143ET-GP
16,31 KBC_PWRBTN#_CN — KBC_PWRBTN#_CN_DOCK
R381 0R2J-2-GP

3D3V_S0 — SCD1U16V2ZY-2GP ×4 — C453 C446 C447 C45

U13 PC87383MG-GP

SIO_14M — R422 10R2J-2-GP — PCLK_SIO_1 3
R419 DUMMY-R2 — C436 DUMMY-C2

GPIO0 … GPIO7
TP20 TPAD30
RI1#/GPIO10, CTS1#/GPIO11, SOUT1/GPO12/TEST#, RTS1#/GPO13/TRIS#, SIN1/GPIO14, DSR1#/GPIO15, DCD1#/GPIO16, IRRX2_IRSL0/GPIO17, GPIO20, GPIO21/LPCPD#, GPIO24/ACK#, DTR1#_BOUT1/BADDR
PD0 … PD7 / GPIO23/PD7
PE, INIT#, ERR#, BUSY_WAIT#, AFD#_DSTRB#, SLCT, STB#_WRITE#, SLIN#_ASTRB#
IRRX1, IRTX

PRN_ACK# — R417 10KR23-3-GP — COM_DTR1#

R426 DUMMY-R2 — 20,42 PM_SUS_STAT# — LPCPD# — R427 10KR2J-3-GP — 3D3V_S0

19,41,42 LPC_LAD0 … LPC_LAD3
3 PCLK_SIO

SB
R429 DUMMY-R2
19,41,42 LPC_LFRAME#
7,20,34,36,41,42,46 PLT_RST1#
20,30,41,42 INT_SERIRQ
19,31,41,42 PM_CLKRUN#

3D3V_S0 — Place C? /C? near Pin1 and Pin6
C663 SCD1U10V2ZY-2GP — TC29 STA70U83VCM — C664 SCD1U16V2ZY-2GP — C665 SCD1U16V2ZY-2GP

30mil
10mil IRTX
10mil IRRX1
10mil IRSL0

FIR1 — VCC2/IRED_ANODE, IRED_CATHODE, TXD, RXD, SD, VCC1, MODE, GND — DY
FIR-TFDU6103-GP
56.15001.131

-1(5/9)

C445 DUMMY-C2

Four Peaks
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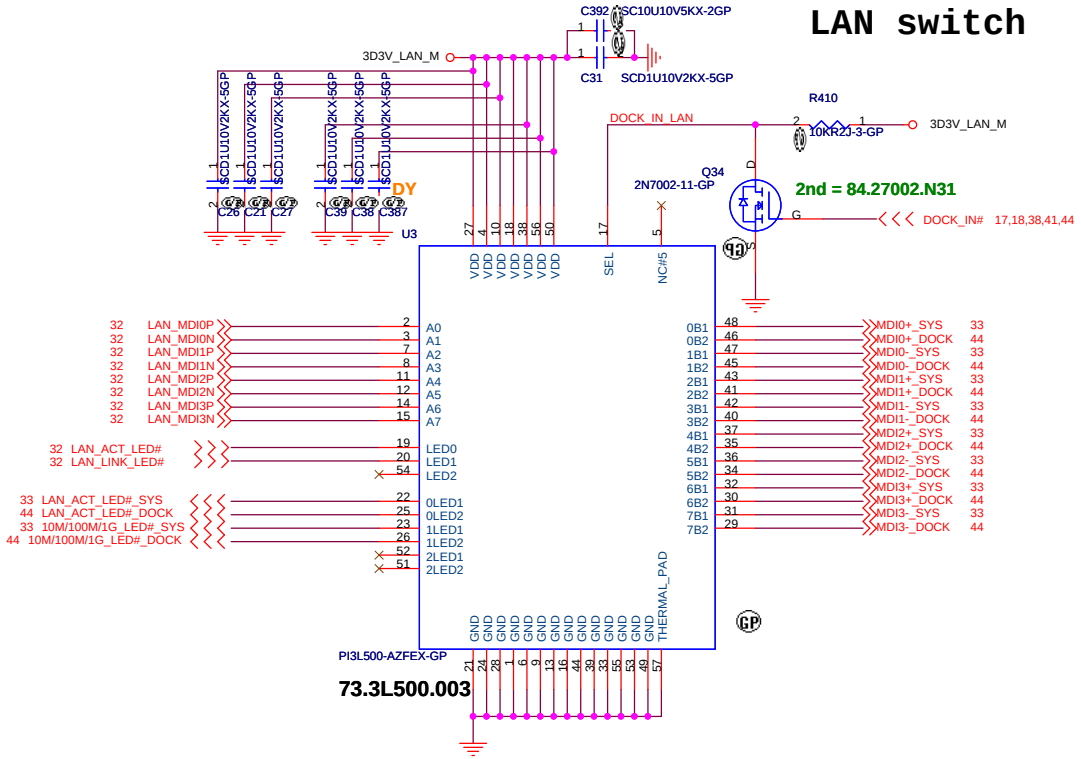
Title: EASY PORT4 (1/2) SIO
Size: Custom — Document Number: Four Peaks — Rev: -1M
Date: Friday, November 21, 2008 — Sheet 44 of 57

LAN switch



Function	SEL	
to An	L	DOCK
to Bn	H	SYSTEM

Four Peaks

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Title: ***EASY PORT4 (2/2)***

Size	Document Number	Rev
A3	Four Peaks	-1M

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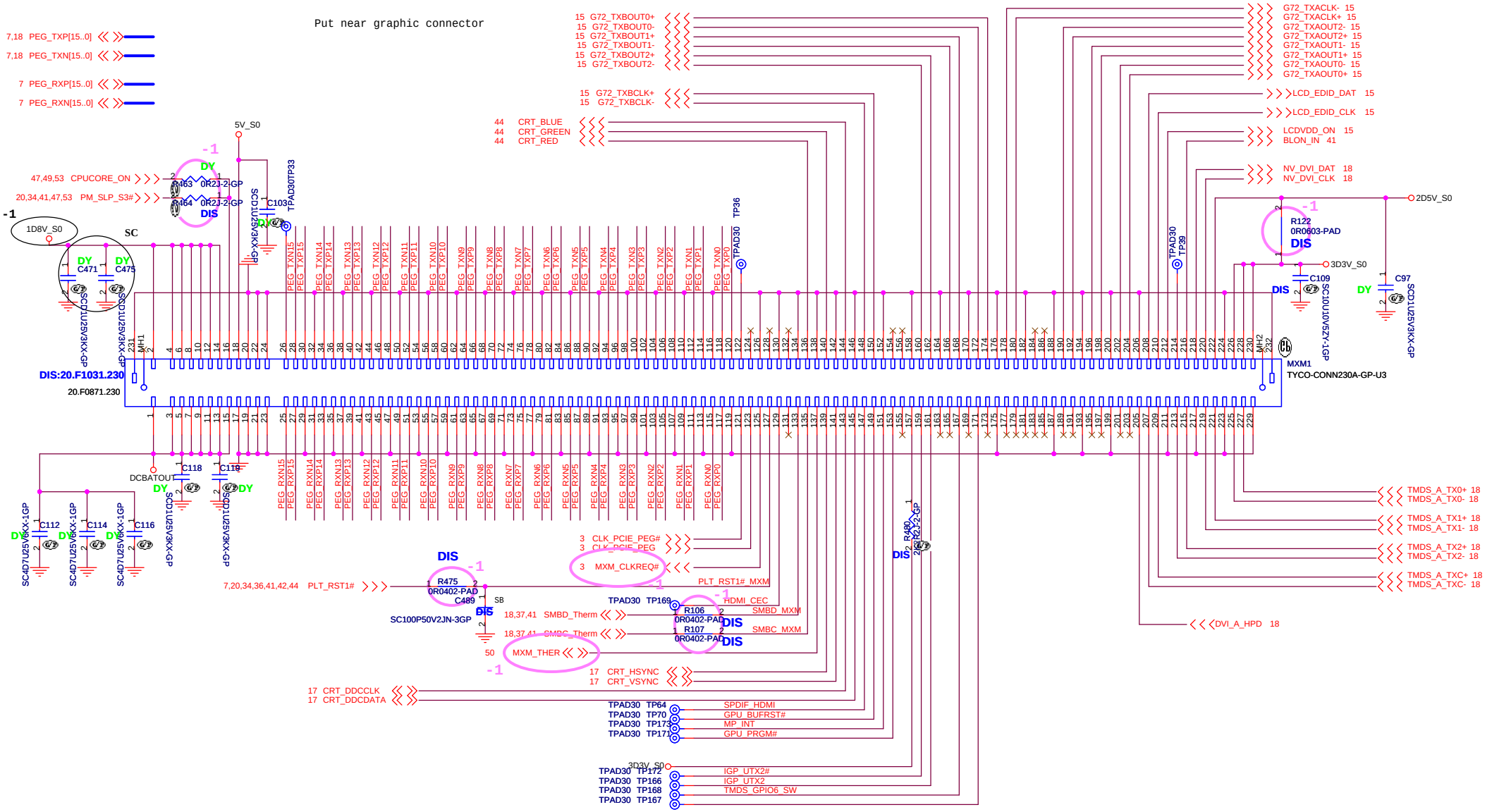
NV SMBus
A(pin143&145) : VGA(CRT) / DOCK
B(pin218&220) : DVI
C(pin208&210) : HDMI / TPI / LVDS



Four Peaks

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Title: **Graphic MXM CONN**

Size	Document Number	Rev
A3	**Four Peaks**	-1M

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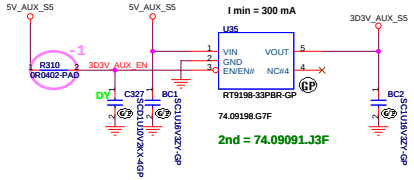
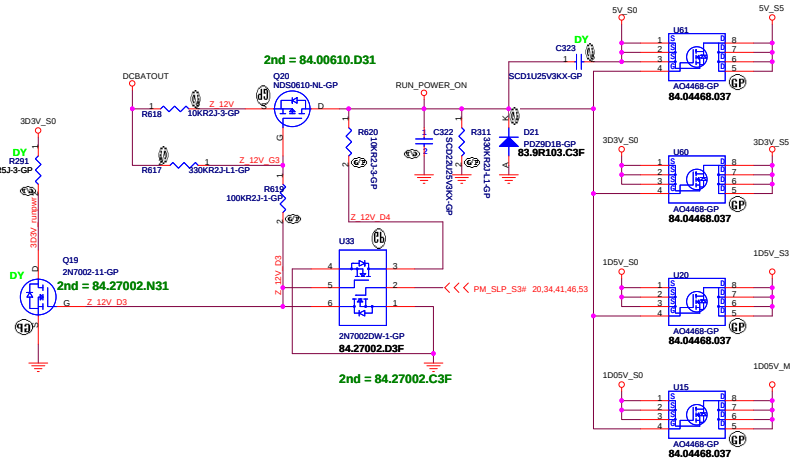
Aux Power

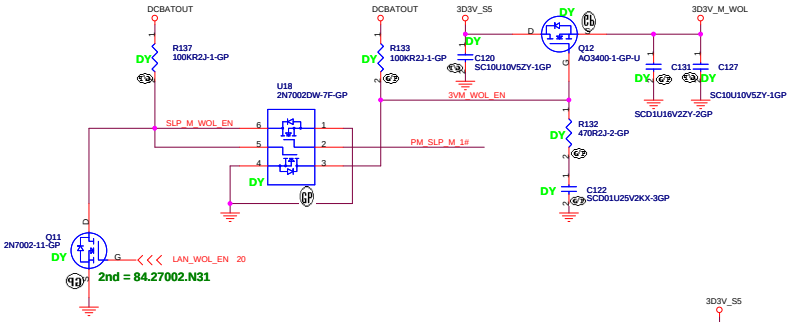
3D3V_AUX_S5

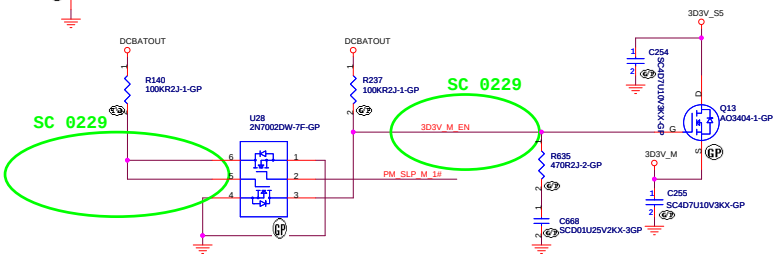
I min = 300 mA

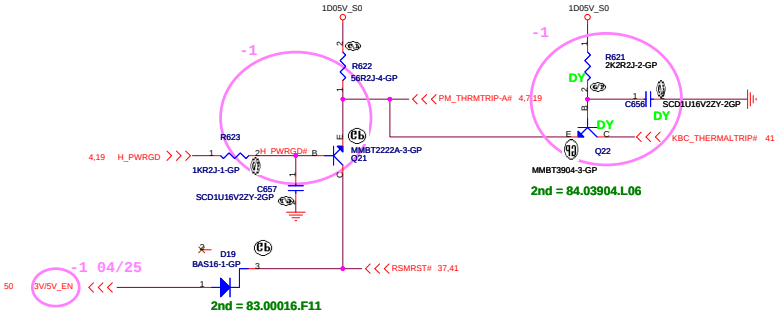


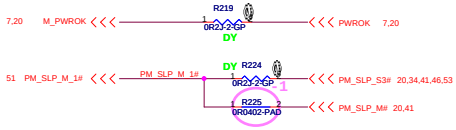
Run Power

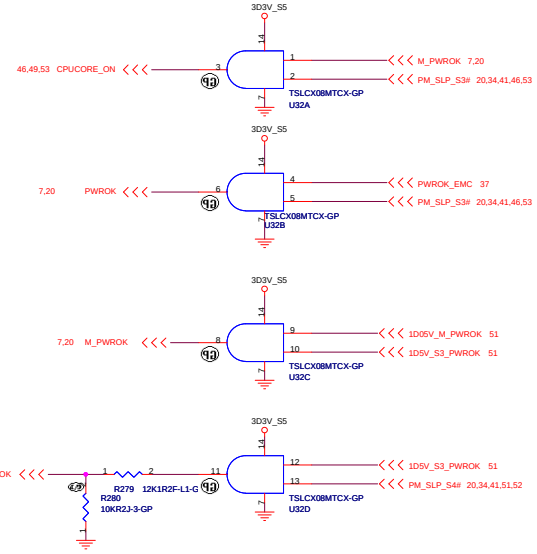


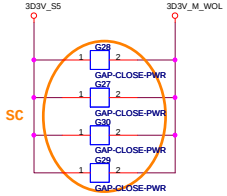












Four Peaks

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Title: RUN POWER and 3D3V_AUX_S5

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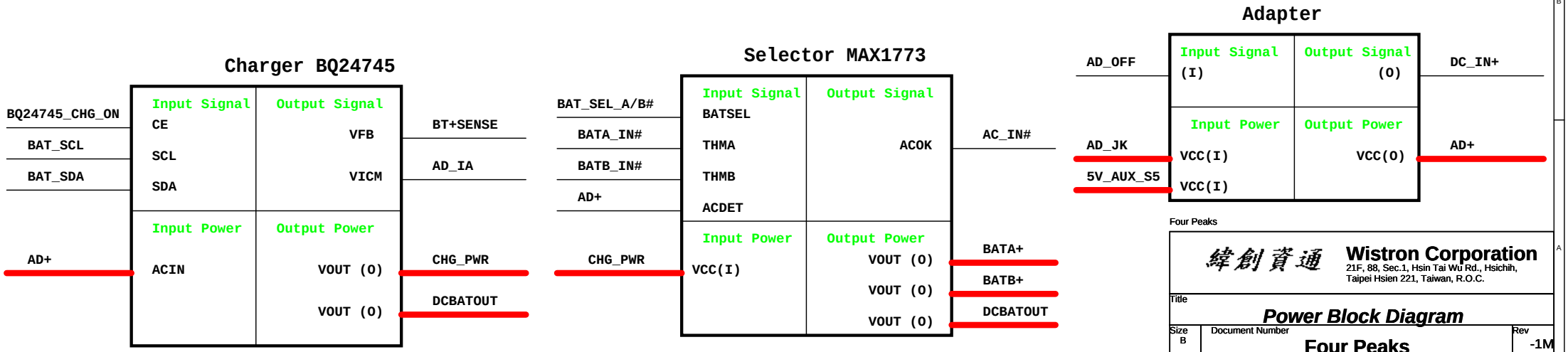

Four Peaks

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Title: ***Power Block Diagram***

Size	Document Number	Rev
B	Four Peaks	-1M

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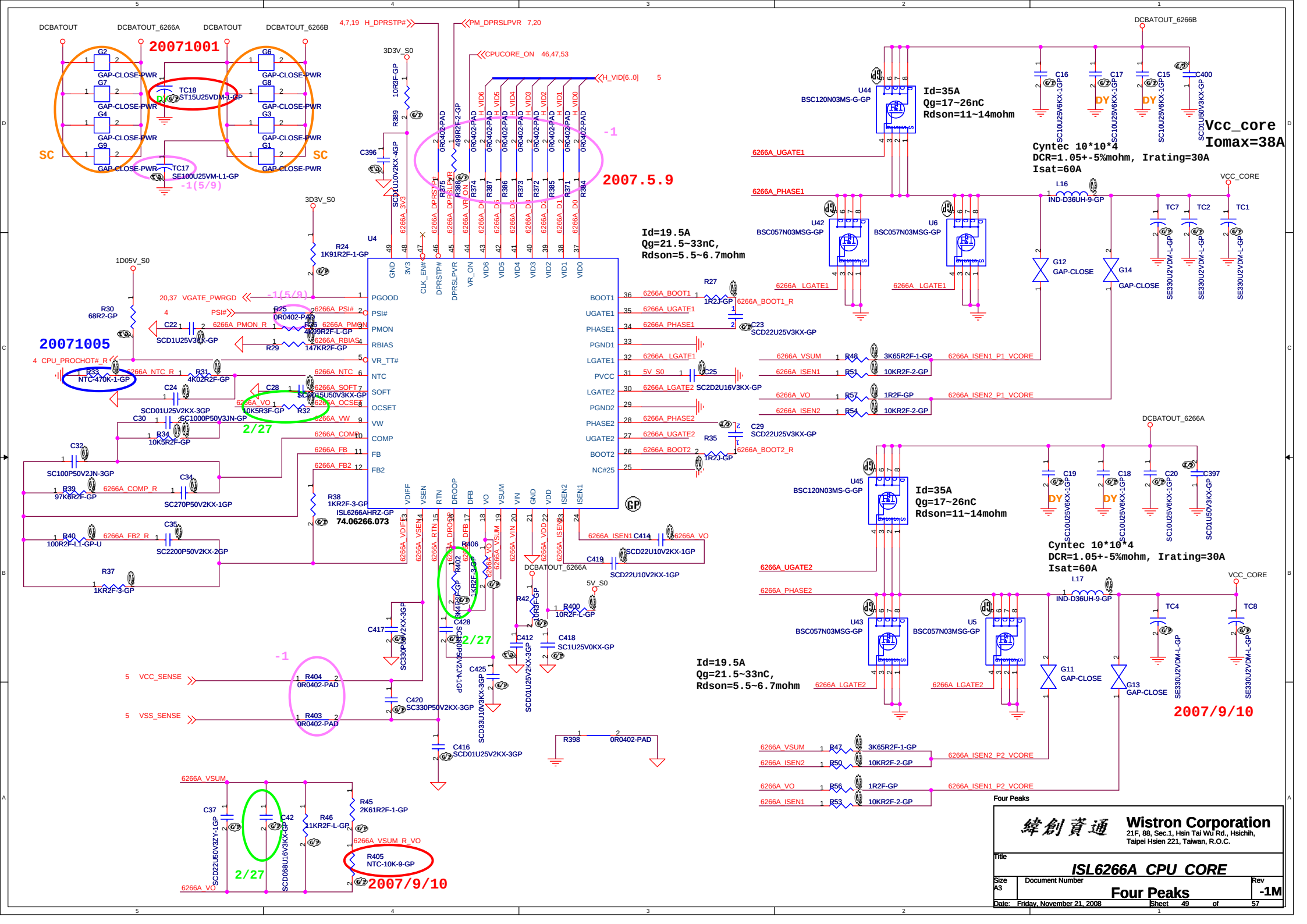
DCBATOUT
DCBATOUT_6266A
DCBATOUT
DCBATOUT_6266B
20071001
SC
SC
-1(5/9)
4,7,19 H_DPRSTP#
PM_DPRSLPVR 7,20
CPUCORE_ON 46,47,53
H_VID[6..0] 5
3D3V_S0
-1
2007.5.9
Id=19.5A
Qg=21.5~33nC,
Rdson=5.5~6.7mohm
U4
1D05V_S0
20071005
20,37 VGATE_PWRGD
4 CPU_PROCHOT#_R
4 PSI#
PGOOD
PSI#
PMON
RBIAS
VR_TT#
NTC
SOFT
OCSET
VW
COMP
FB
FB2
BOOT1
UGATE1
PHASE1
PGND1
LGATE1
PVCC
LGATE2
PGND2
PHASE2
UGATE2
BOOT2
NC#25
VDIFF
VSEN
RTN
DROOP
DFB
VO
VSUM
VIN
GND
VDD
ISEN2
ISEN1
ISL6266AHRZ-GP
74.06266.073
2/27
2/27
-1
5 VCC_SENSE
5 VSS_SENSE
6266A_VSUM
6266A_VO
2/27
R405
NTC-10K-9-GP
2007/9/10
Id=35A
Qg=17~26nC
Rdson=11~14mohm
Cyntec 10*10*4
DCR=1.05+-5%mohm, Irating=30A
Isat=60A
Vcc_core
Iomax=38A
VCC_CORE
Id=19.5A
Qg=21.5~33nC,
Rdson=5.5~6.7mohm
Id=35A
Qg=17~26nC
Rdson=11~14mohm
Cyntec 10*10*4
DCR=1.05+-5%mohm, Irating=30A
Isat=60A
2007/9/10
Four Peaks
Wistron Corporation
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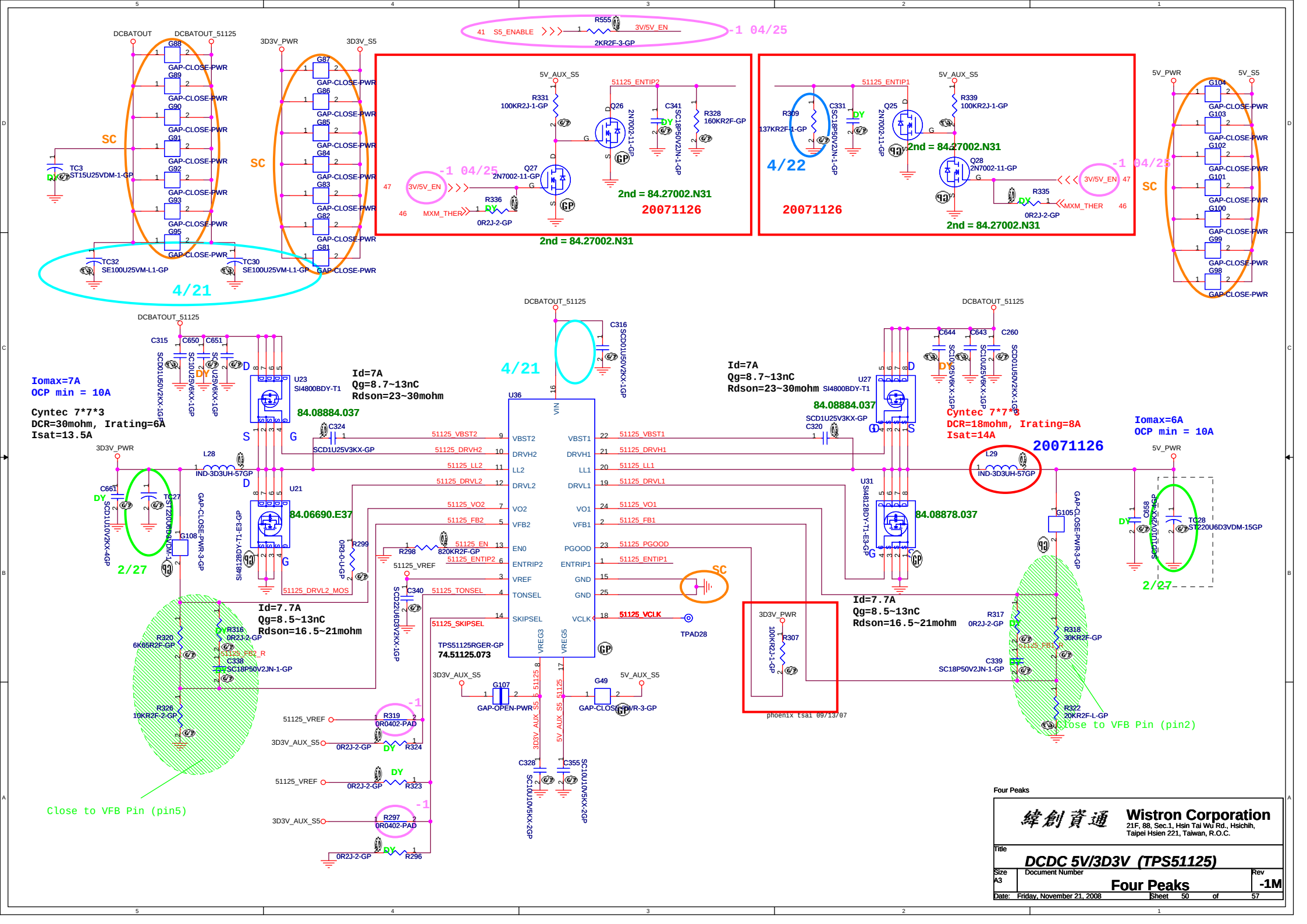
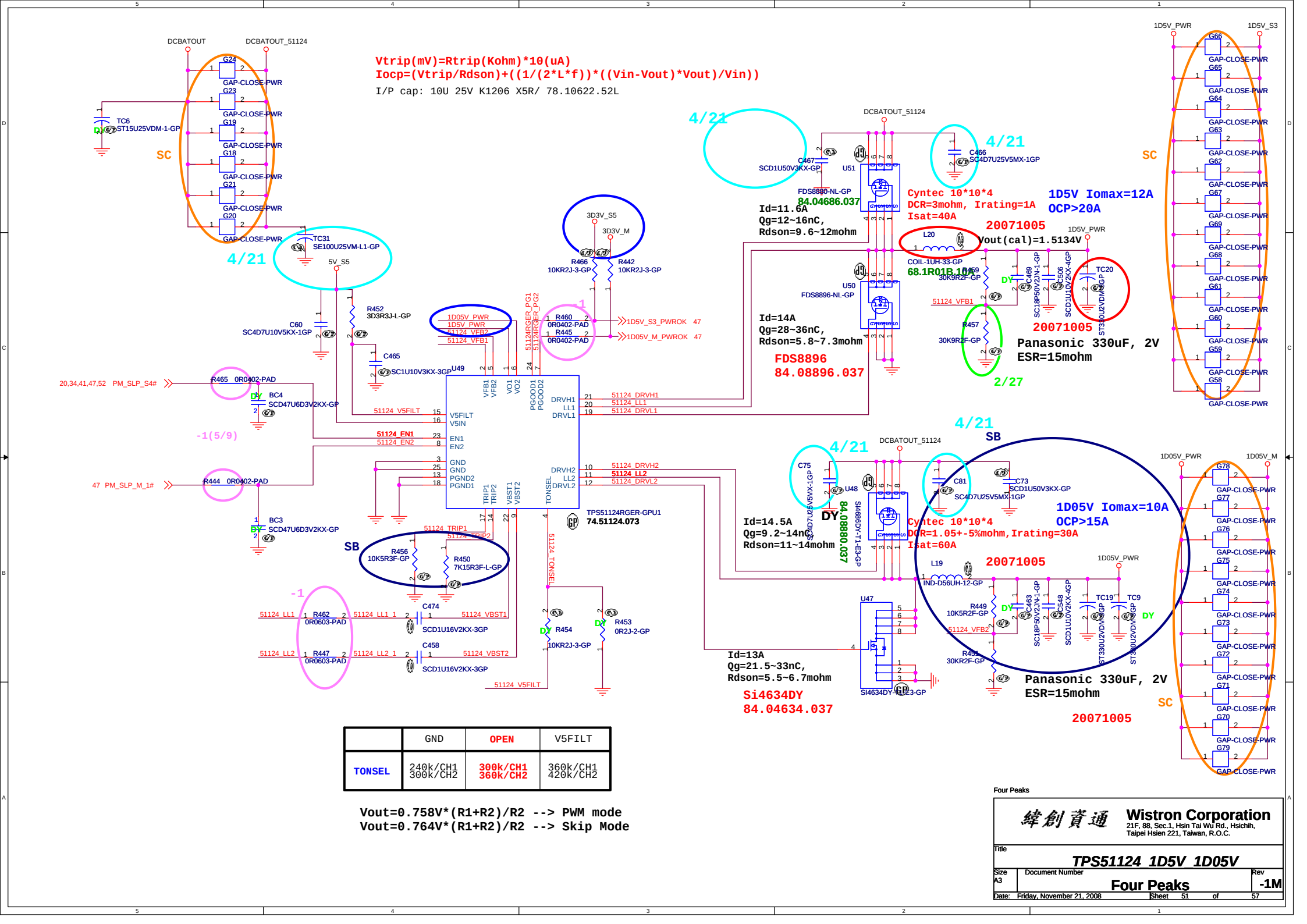
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL6266A CPU CORE
Size A3
Document Number
Four Peaks
Rev -1M
Date: Friday, November 21, 2008
Sheet 49 of 57


DCBATOUT
DCBATOUT_51125
3D3V_PWR
3D3V_S5
5V_AUX_S5
5V_PWR
5V_S5
SC
GAP-CLOSE-PWR
TC3 ST15U25VDM-1-GP
TC32 SE100U25VM-L1-GP
TC30 SE100U25VM-L1-GP
4/21
41 S5_ENABLE
R555 2KR2F-3-GP
3V/5V_EN
-1 04/25
R331 100KR2J-1-GP
51125_ENTIP2
Q26 2N7002-11-GP
C341 SC18P50V2JN-1-GP
R328 160KR2F-GP
Q27 2N7002-11-GP
R336 0R2J-2-GP
MXM_THER
2nd = 84.27002.N31
20071126
51125_ENTIP1
R309 137KR2F-1-GP
C331 SC18P50V2JN-1-GP
Q25 2N7002-11-GP
R339 100KR2J-1-GP
4/22
Q28 2N7002-11-GP
R335 0R2J-2-GP
G104
G103
G102
G101
G100
G99
G98
Iomax=7A
OCP min = 10A
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
C315
C650
C651
SCD01U50V2KX-1GP
SC10U25V6KX-1GP
U23 SI4800BDY-T1
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
84.08884.037
C324 SCD1U25V3KX-GP
U36
VIN
C316 SCD01U50V2KX-1GP
51125_VBST2
51125_DRVH2
51125_LL2
51125_DRVL2
51125_VO2
51125_FB2
51125_EN
51125_ENTIP2
51125_VREF
51125_TONSEL
51125_SKIPSEL
VBST2
DRVH2
LL2
DRVL2
VO2
VFB2
EN0
ENTRIP2
VREF
TONSEL
SKIPSEL
VBST1
DRVH1
LL1
DRVL1
VO1
VFB1
PGOOD
ENTRIP1
GND
VCLK
VREG3
VREG5
51125_VBST1
51125_DRVH1
51125_LL1
51125_DRVL1
51125_VO1
51125_FB1
51125_PGOOD
51125_ENTIP1
51125_VCLK
TPS51125RGER-GP
74.51125.073
TPAD28
SC
L28 IND-3D3UH-57GP
U21 SI4812BDY-T1-E3-GP
84.06690.E37
C661
TC27 ST220U6D3VDM-1-GP
G108
2/27
R320 6K65R2F-GP
R316 0R2J-2-GP
C338 SC18P50V2JN-1-GP
R326 10KR2F-2-GP
R299 0R3-0-U-GP
R298 820KR2F-GP
C340 SCD22U6D3V2KX-1GP
51125_DRVL2_MOS
51125_FB2_R
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
Close to VFB Pin (pin5)
R319 0R0402-PAD
R324 0R2J-2-GP
R323 0R2J-2-GP
R297 0R0402-PAD
R296 0R2J-2-GP
G107 GAP-OPEN-PWR
G49 GAP-CLOSE-PWR-3-GP
C328 SC10U10V5KX-2GP
C355 SC10U10V5KX-2GP
U27 SI4800BDY-T1
84.08884.037
SCD1U25V3KX-GP
C320
C644
C643
C260
SCD01U50V2KX-1GP
Cyntec 7*7*3
DCR=18mohm, Irating=8A
Isat=14A
20071126
U31 SI4812BDY-T1-E3-GP
84.08878.037
L29 IND-3D3UH-57GP
Iomax=6A
OCP min = 10A
C658 SCD1U10V2KX-4GP
TC28 ST220U6D3VDM-15GP
2/27
R307 100KR2J-1-GP
phoenix tsai 09/13/07
R317 0R2J-2-GP
R318 30KR2F-GP
C339 SC18P50V2JN-1-GP
R322 20KR2F-L-GP
Close to VFB Pin (pin2)
Four Peaks
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DCDC 5V/3D3V (TPS51125)
Size A3
Document Number
Four Peaks
Rev -1M
Date: Friday, November 21, 2008
Sheet 50 of 57



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

Vout=0.758V*(R1+R2)/R2 --> PWM mode
Vout=0.764V*(R1+R2)/R2 --> Skip Mode

Four Peaks

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124 1D5V 1D05V

Size	Document Number	Rev
A3	Four Peaks	-1M

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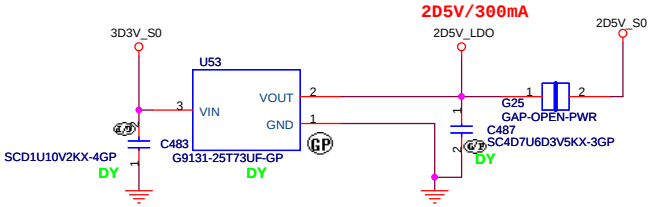
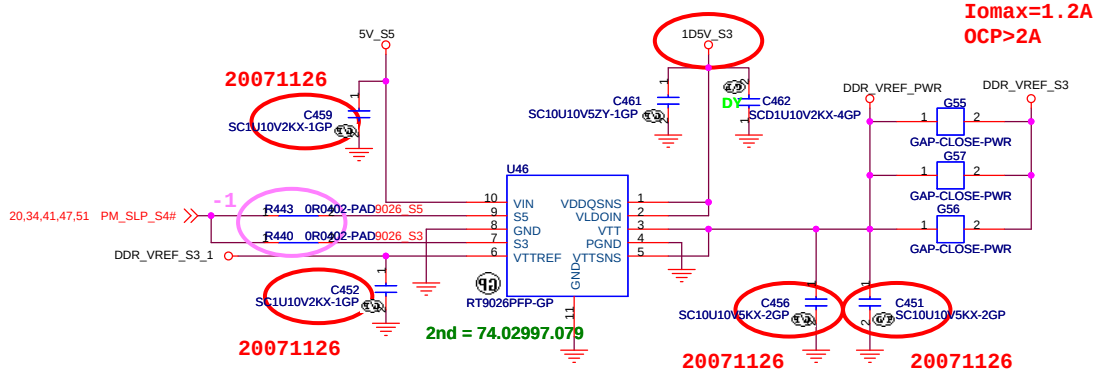
2D5V_S0
Iomax=0.3A

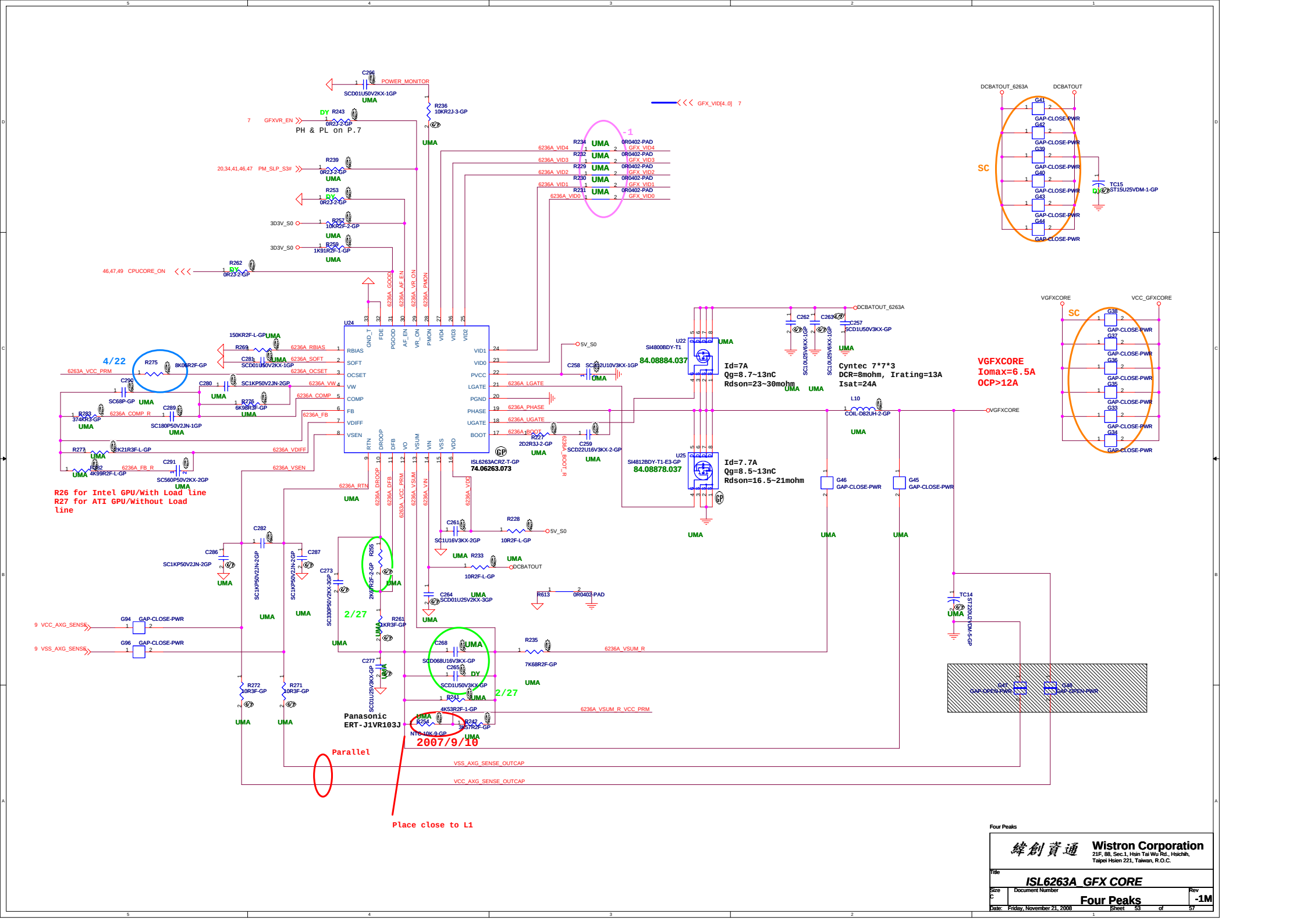




Four Peaks

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***0D75V & 2D5V***	
Size A3	Document Number **Four Peaks**	Rev **-1M**
Date: Friday, November 21, 2008	Sheet 52 of 57	


U24
ISL6263ACRZ-T-GP
74.06263.073
SI4800BDY-T1
84.08884.037
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
Cyntec 7*7*3
DCR=8mohm, Irating=13A
Isat=24A
SI4812BDY-T1-E3-GP
84.08878.037
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
VGFXCORE
Iomax=6.5A
OCP>12A
R26 for Intel GPU/With Load line
R27 for ATI GPU/Without Load line
Panasonic
ERT-J1VR103J
2007/9/10
Parallel
Place close to L1
4/22
2/27
2/27
PH & PL on P.7
VSS_AXG_SENSE_OUTCAP
VCC_AXG_SENSE_OUTCAP
Four Peaks
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ISL6263A_GFX CORE
Four Peaks
-1M
Friday, November 21, 2008
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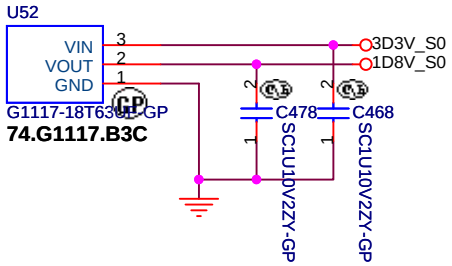

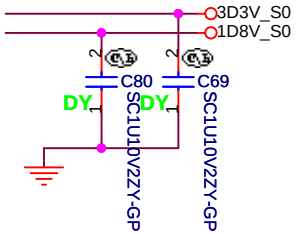

Four Peaks

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***VGA_CORE_S0 (UMA)***

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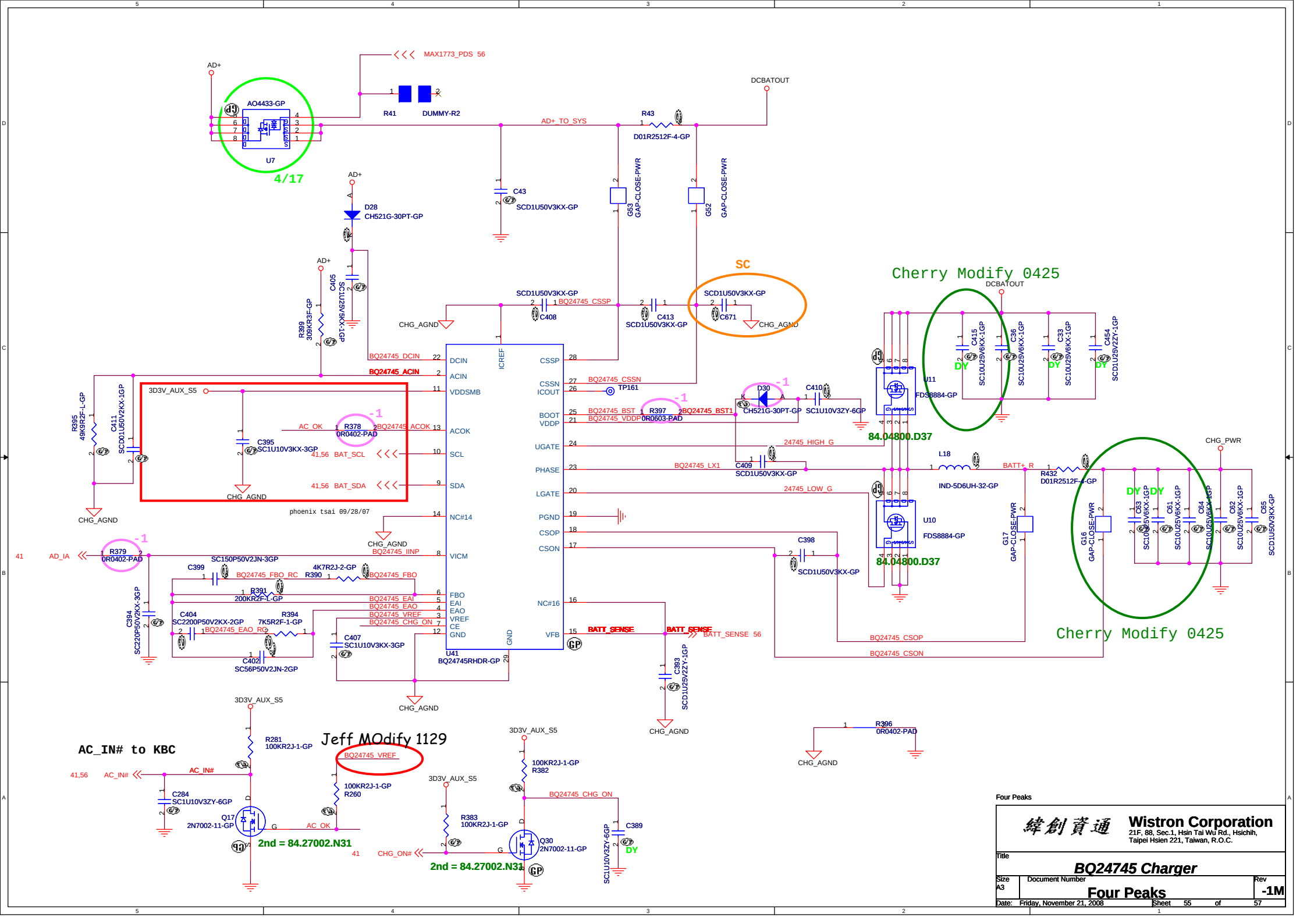
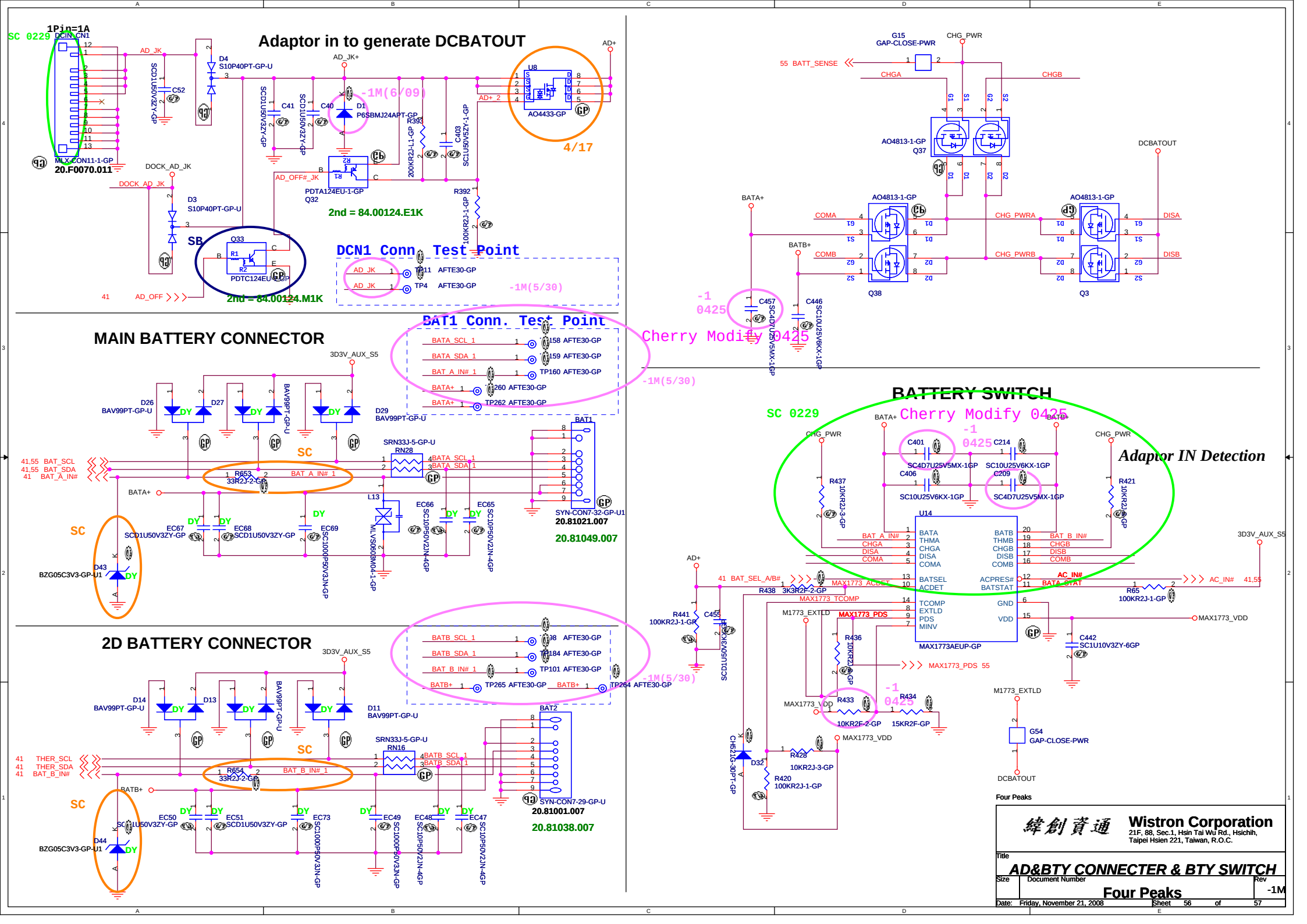
A4	**Four Peaks**	**-1M**

Date: Friday, November 21, 2008 Sheet 54 of 57


MAX1773_PDS 56
AD+
AO4433-GP
U7
4/17
R41
DUMMY-R2
AD+_TO_SYS
DCBATOUT
R43
D01R2512F-4-GP
C43
SCD1U50V3KX-GP
G53 GAP-CLOSE-PWR
G52 GAP-CLOSE-PWR
D28
CH521G-30PT-GP
SC
SCD1U50V3KX-GP
C408
C413
C671
CHG_AGND
BQ24745_CSSP
R399 309KR3F-GP
C405 SCD1U25V3KX-1GP
BQ24745_DCIN
BQ24745_ACIN
3D3V_AUX_S5
R395 49K9R2F-L-GP
C411 SCD01U50V2KX-1GP
C395 SC1U10V3KX-3GP
AC_OK
R378 0R0402-PAD
BQ24745_ACOK
41,56 BAT_SCL
41,56 BAT_SDA
phoenix tsai 09/28/07
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#14
VICM
FBO
EAI
EAO
VREF
CE
GND
ICREF
CSSP
CSSN
ICOUT
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
U41
BQ24745RHDR-GP
BQ24745_CSSN
TP161
BQ24745_BST
BQ24745_VDDP
R397 0R0603-PAD
BQ24745_BST1
D30
CH521G-30PT-GP
C410
SC1U10V3ZY-6GP
24745_HIGH_G
BQ24745_LX1
C409
SCD1U50V3KX-GP
24745_LOW_G
C398
SCD1U50V3KX-GP
U11
FDS8884-GP
U10
FDS8884-GP
84.04800.D37
84.04800.D37
L18
IND-5D6UH-32-GP
BATT+_R
R432 D01R2512F-4-GP
CHG_PWR
G16 GAP-CLOSE-PWR
G17 GAP-CLOSE-PWR
DY
C415 SC10U25V6KX-1GP
C36 SC10U25V6KX-1GP
C33 SC10U25V6KX-1GP
C454 SCD1U25V2ZY-1GP
C63 SC10U25V6KX-1GP
C61 SC10U25V6KX-1GP
C64 SC10U25V6KX-1GP
C62 SC10U25V6KX-1GP
C65 SCD1U50V3KX-GP
Cherry Modify 0425
Cherry Modify 0425
AD_IA
R379 0R0402-PAD
SC150P50V2JN-3GP
C399
BQ24745_FBO_RC
4K7R2J-2-GP
R390
BQ24745_FBO
R391 200KR2F-L-GP
C394 SC220P50V2KX-3GP
C404 SC2200P50V2KX-2GP
BQ24745_EAO_RC
R394 7K5R2F-1-GP
C402 SC56P50V2JN-2GP
BQ24745_EAI
BQ24745_EAO
BQ24745_VREF
BQ24745_CHG_ON
C407 SC1U10V3KX-3GP
BATT_SENSE
C393 SCD1U25V2ZY-1GP
BATT_SENSE 56
BQ24745_CSOP
BQ24745_CSON
R396 0R0402-PAD
AC_IN# to KBC
41,56 AC_IN#
R281 100KR2J-1-GP
C284 SC1U10V3ZY-6GP
Q17 2N7002-11-GP
2nd = 84.27002.N31
Jeff MOdify 1129
BQ24745_VREF
R260 100KR2J-1-GP
AC_OK
3D3V_AUX_S5
R382 100KR2J-1-GP
BQ24745_CHG_ON
R383 100KR2J-1-GP
Q30 2N7002-11-GP
CHG_ON#
2nd = 84.27002.N31
C389
SC1U10V3ZY-6GP
Four Peaks
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BQ24745 Charger
Size A3
Document Number
Four Peaks
Rev -1M
Date: Friday, November 21, 2008
Sheet 55 of 57


Adaptor in to generate DCBATOUT
1Pin=1A
SC 0229
DCIN_CN1
MLX_CON11-1-GP
20.F0070.011
AD_JK
DOCK_AD_JK
D4
S10P40PT-GP-U
D3
S10P40PT-GP-U
C52
C41
C40
D1
P6SBMJ24APT-GP
-1M(6/09)
R393
200KR2J-L1-GP
C403
SC1U50V5ZY-1-GP
R392
100KR2J-1-GP
AD_OFF#_JK
PDTA124EU-1-GP
Q32
2nd = 84.00124.E1K
SB
Q33
PDTC124EU-1-GP
2nd = 84.00124.M1K
41
AD_OFF
U8
AO4433-GP
AD+
AD+ 2
4/17
DCN1 Conn. Test Point
AD_JK
TP11 AFTE30-GP
TP4 AFTE30-GP
-1M(5/30)
MAIN BATTERY CONNECTOR
3D3V_AUX_S5
D26
BAV99PT-GP-U
D27
D29
BAV99PT-GP-U
BAT1 Conn. Test Point
BATA_SCL_1
BATA_SDA_1
BAT_A_IN#_1
BATA+
TP158 AFTE30-GP
TP159 AFTE30-GP
TP160 AFTE30-GP
TP260 AFTE30-GP
TP262 AFTE30-GP
SRN33J-5-GP-U
RN28
R653
33R2J-2-GP
BAT_A_IN#_1
BAT1
SYN-CON7-32-GP-U1
20.81021.007
20.81049.007
L13
MLVS0603N04-1-GP
EC66
EC65
EC67
EC68
EC69
SC1000P50V3JN-GP
SC10P50V2JN-4GP
D43
BZG05C3V3-GP-U1
41,55 BAT_SCL
41,55 BAT_SDA
41 BAT_A_IN#
SC
DY
2D BATTERY CONNECTOR
D14
BAV99PT-GP-U
D13
D11
BAV99PT-GP-U
BATB_SCL_1
BATB_SDA_1
BAT_B_IN#_1
BATB+
TP238 AFTE30-GP
TP184 AFTE30-GP
TP101 AFTE30-GP
TP265 AFTE30-GP
TP264 AFTE30-GP
SRN33J-5-GP-U
RN16
R654
33R2J-2-GP
BAT2
SYN-CON7-29-GP-U
20.81001.007
20.81038.007
EC50
EC51
EC73
EC49
EC48
EC47
SC10P50V2JN-4GP
D44
BZG05C3V3-GP-U1
41 THER_SCL
41 THER_SDA
41 BAT_B_IN#
-1M(5/30)
Cherry Modify 0425
-1
0425
C457
SC4D7U25V5MX-1GP
C446
SC10U25V6KX-1GP
BATA+
BATB+
CHG_PWR
G15
GAP-CLOSE-PWR
55 BATT_SENSE
CHGA
CHGB
AO4813-1GP
Q37
Q38
Q3
COMA
COMB
CHG_PWRA
CHG_PWRB
DISA
DISB
DCBATOUT
BATTERY SWITCH
SC 0229
Adaptor IN Detection
C401
C214
C406
C209
R437
10KR2J-3-GP
R421
10KR2J-3-GP
U14
MAX1773AEUP-GP
BAT_A_IN#
CHGA
DISA
COMA
BATB
THMB
CHGB
DISB
COMB
BAT_B_IN#
BATSEL
ACDET
ACPRES#
BATSTAT
AC_IN#
TCOMP
EXTLD
PDS
MINV
GND
VDD
MAX1773_ACDET
MAX1773_TCOMP
MAX1773_PDS
MAX1773_EXTLD
MAX1773_VDD
41 BAT_SEL_A/B#
R438
3K3R2F-2-GP
R441
100KR2J-1-GP
C455
SC1K50V5ZY-1-GP
R436
10KR2J-3-GP
R433
10KR2F-2-GP
R434
15KR2F-GP
R428
10KR2J-3-GP
R420
100KR2J-1-GP
D32
CH521G-30PT-GP
MAX1773_PDS 55
C442
SC1U10V3ZY-6GP
R65
100KR2J-1-GP
AC_IN#
AC_IN# 41,55
3D3V_AUX_S5
MAX1773_VDD
M1773_EXTLD
G54
GAP-CLOSE-PWR
DCBATOUT
Four Peaks
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AD&BTY CONNECTER & BTY SWITCH
Size
Document Number
Four Peaks
Rev
-1M
Date: Friday, November 21, 2008
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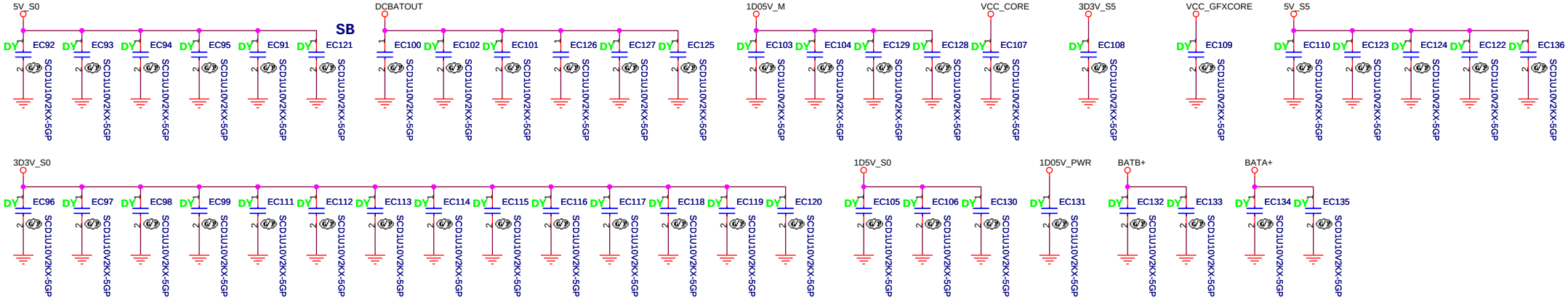
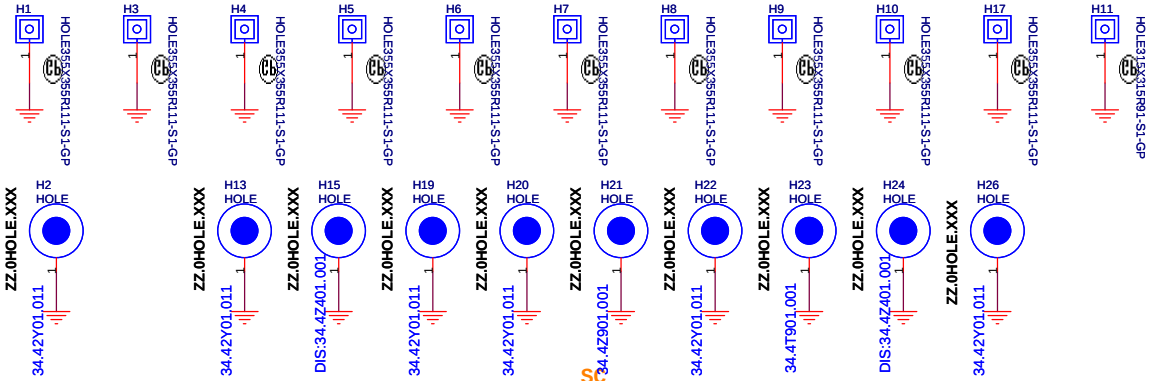
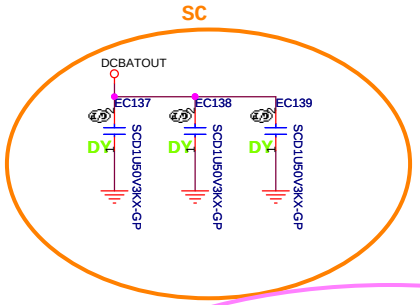
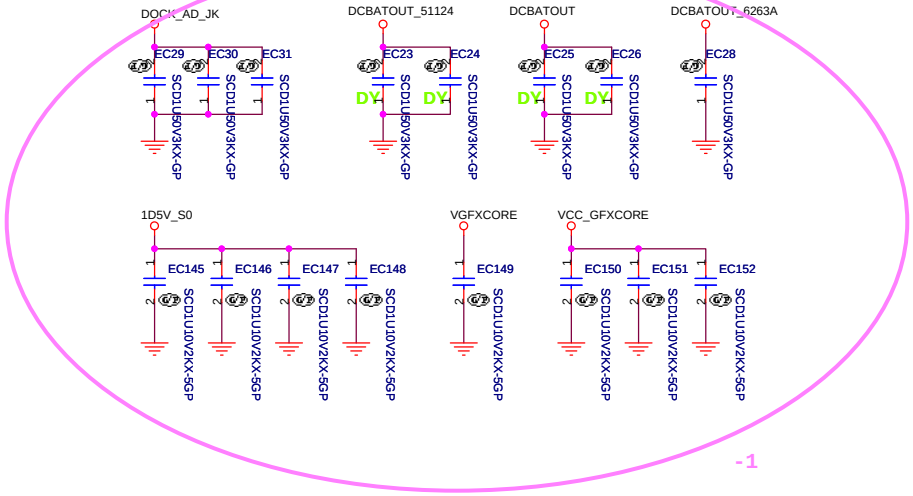
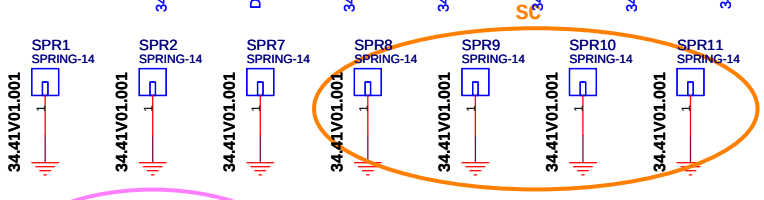


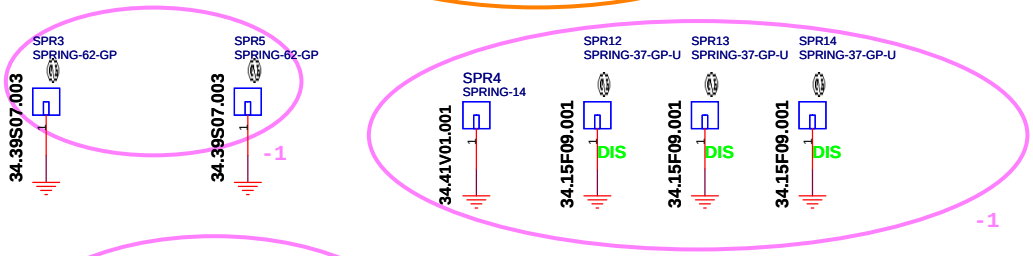
Stand off Location

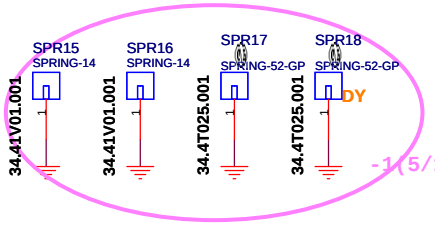












Four Peaks

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: EMI/Spring/Boss

Size	Document Number	Rev
	Four Peaks	-1M

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