

P162, NV34, 8Mx16DDR, 128bit, 128MB, DVI, TV OUT, VGA

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- 13 TMDS LinkA and its power supplies, Backdrive.
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P160 HISTORY:

X00	INITIAL VERSION
X01	Cleaned up schematics - changes from initial design review meeting
X02	Imported board file #65 and synchronized with latest version of schematics.
X03	Nov 18/02 - Replaced LB502 with an 805 bead, changed PLLVDD rail to 3V3 instead of A3V3, and removed AGPVDDQ deoupling caps C130, C257, and C570.
X04	Nov 21/02 - C75 is changed to decouple 3V3 to GND.
X05	Nov 22/02 - VIP interface rail changed to 3V3 instead of A3V3 due to short between VIPVDDQ and VDD33.
X06	Nov 25/02 - FRWR_VAUXP rail changed to 3V3.
X07	Nov 26/02 - Changed DACB_LOAD_TEST GPIO assignment for NV34.
X08	Dec 02/02 - AGP_PLL_VDD and FB_DLLVDD are supplied from A3V3 rail.

600-10162-0000-003

P162-A00 History:

- 1-Added P162 specific features:

- SW PS,TMDS LinkA, Backdrive, new slim VGA, Fan Cntl.
- Added Current sharing, TMDS IO and PLL linear regulators.
- 2-Added TH parts in PS section as ALT.
- 3-Added SST serial support.
- 4-Changed AGP_PLL_VDD, FB_PLLVDD, DAC_A/B_VDD and PLL_VDD to A3V3.
- 5-Added 10 caps as part of P160 sync up.
- 6-Added PU resitors on Jtag TMS and TDI
- 7-Incorporated recommendations from PS Vendor.
- 8-Added extra X elements near connectors to bridge CGND and GND cut.
- 9-Added an option to use a single dual FET for low end bd.
- 10-Fixed error on 6529 power good and current supplement.
- 11-Changed C302 to 0603 (too big pkg for .1uf in 0805)
- 12-Deleted C296 and C293 (shared them with C313, C324)
- 13-Changed C329 and C324 to 0603 pkg.
- 14-Removed alternate Semtech SW (could not route).

Changes after the design review:

- 1-Remove C301 and R137-left over from Semtech PS circuit.
- 2-Remove sync buffer bypass resistors.
- 3-Remove R122 and R123 from Intersil power rails.
- 4-Add snubber circuit for NVVDD PS.
- 5-Add PD res on TP_XTALOUTBUF to terminate the signal.
- 6-Fan controler PU to 3V3 from A3V3.
- 7-Cleaned up Unnamed nets.

- 8-Split CGND into 2 nets (added CGND1 to J6.25 and J2. 16).
- 9-Added PD resistor on FAN_ON.
- 10-Added 8 caps for DQS/DQM routings that break plane reference.

X-RELEASE.

P162-A01 History:

- Merged net IFPBIOVDD with IFPAIOVDD.
- Merged Q4 and Q5 into one package.
- Implemented TV signal return scheme thru zero Ohm resistors.

P162-A02 History:

The main changes for this revision is to improve routing for DAC B and add 100ps inter-pair skew to pass EMC as modeled on A01 board. See 149- document for detail.

P162-A03 History:

Merged CGND and GND to become GND net to pass EMI at 16x12. This modificaiton was tested on P162-A02

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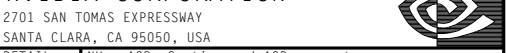
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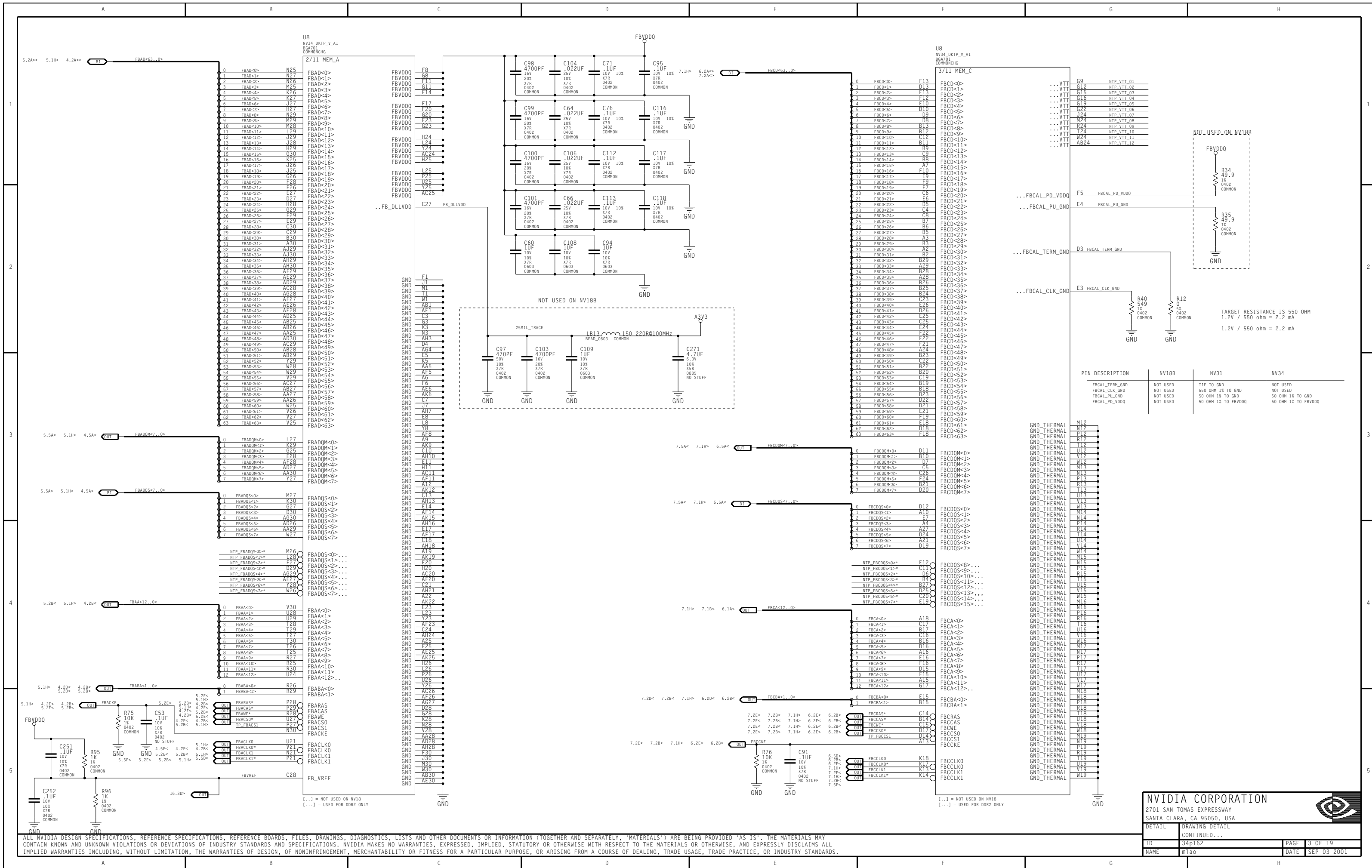


DETAIL	DRAWING DETAIL		
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AGP BUS NET_SPACING_TYPE



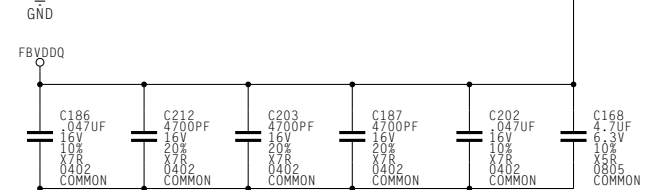
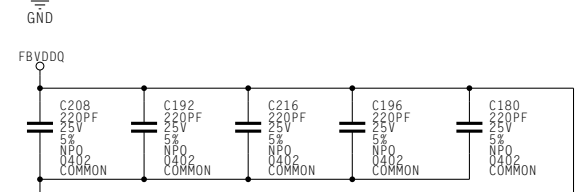
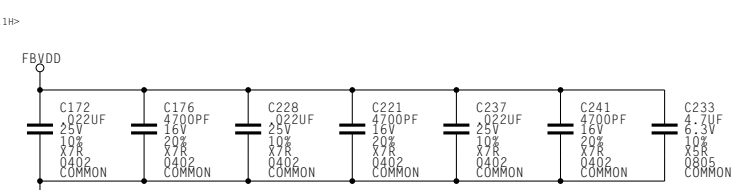
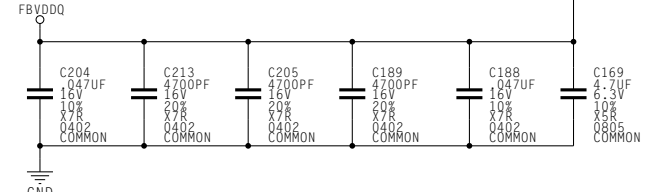
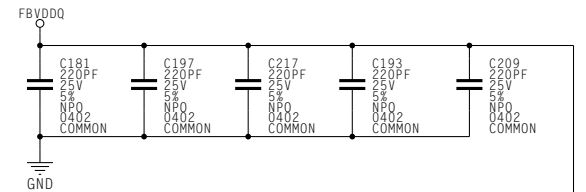
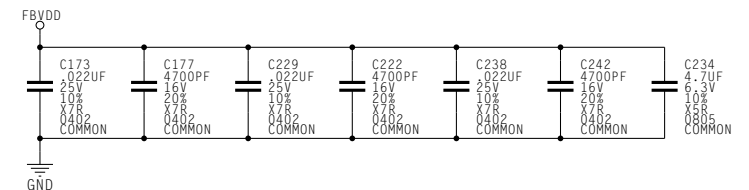
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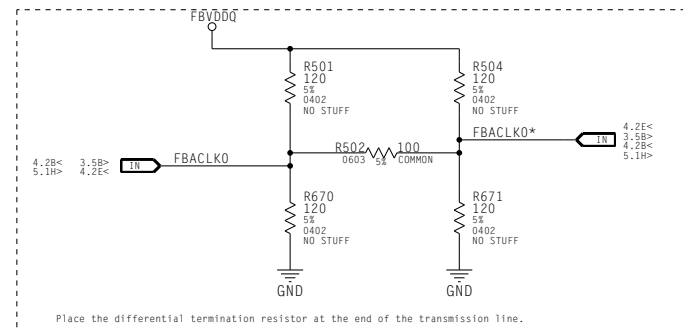
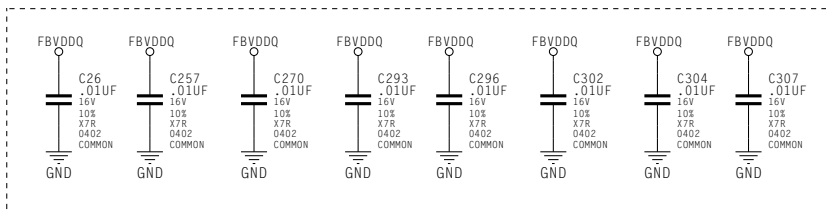
```
MEMORY 1st bank 0..31
PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY
```

NV31 FB i/f can be configured in two ways:
2x64 bits or 2x32 bits

THIS REQUIRES THAT BOTH PARTITIONS
TO BE CONNECTED TO BE FUNCTIONAL



Place plane decoupling caps near DQS-DQM pairs.



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DETAIL	MEMORY 64MB 4/8MX16 Bits 0..31
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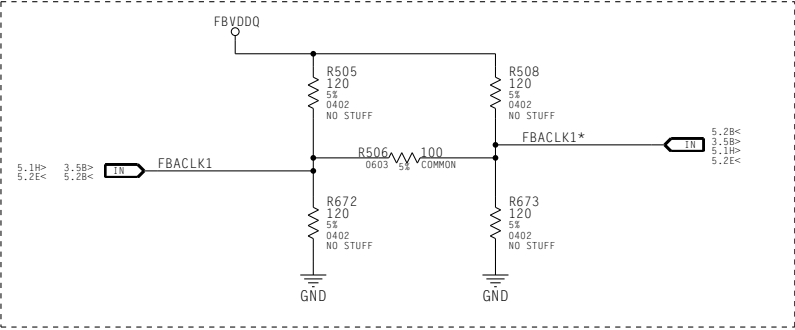
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DETAIL	MEMORY 64MB 4/8MX16 Bits 32..63		
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Figure 1 shows five schematic diagrams of different types of FBVDDQ capacitors. Each diagram consists of a capacitor symbol connected between the FBVDDQ pin and a common ground (GND). The capacitors are labeled with their values and part numbers: C272 .01UF, C292 .01UF, C318 .01UF, C320 .01UF, C322 .01UF, C289 .01UF, C317 .01UF, C319 .01UF, C321 .01UF, and C23 .01UF. Each capacitor has a tolerance of ±10% and is connected to GND through a common connection.

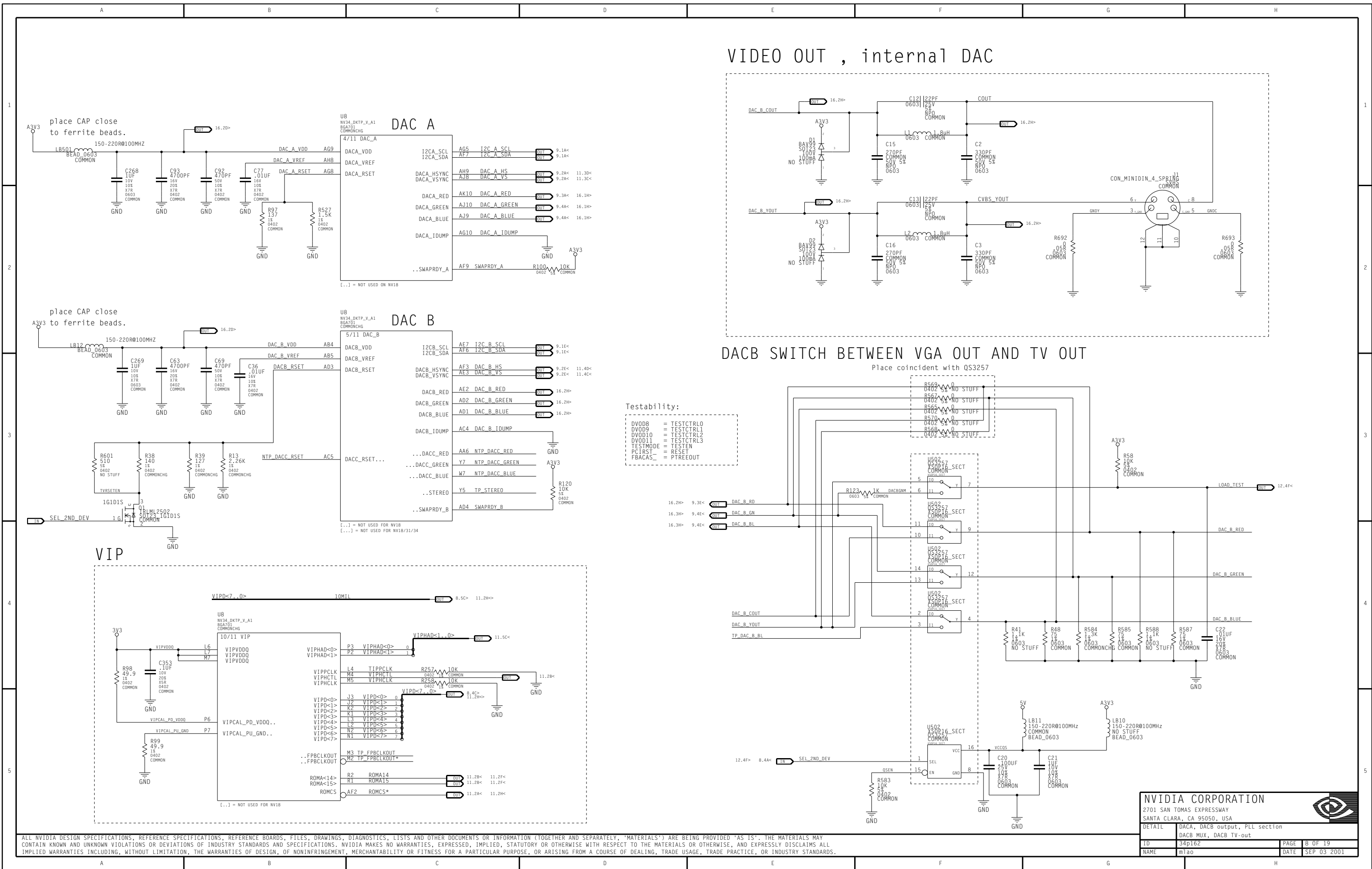
DETAIL	MEMORY 64MB 4/8MX16 Bits 64..95
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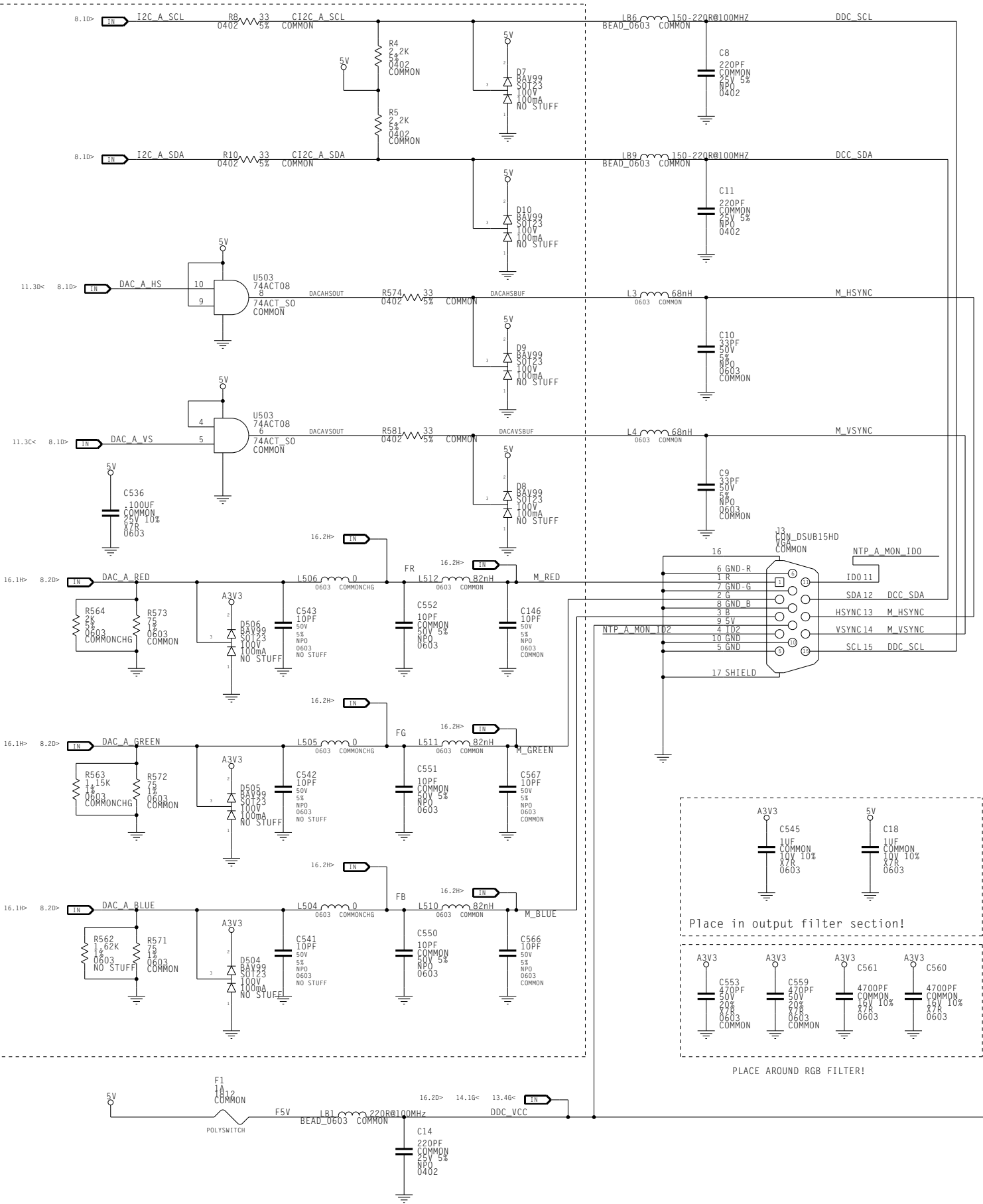
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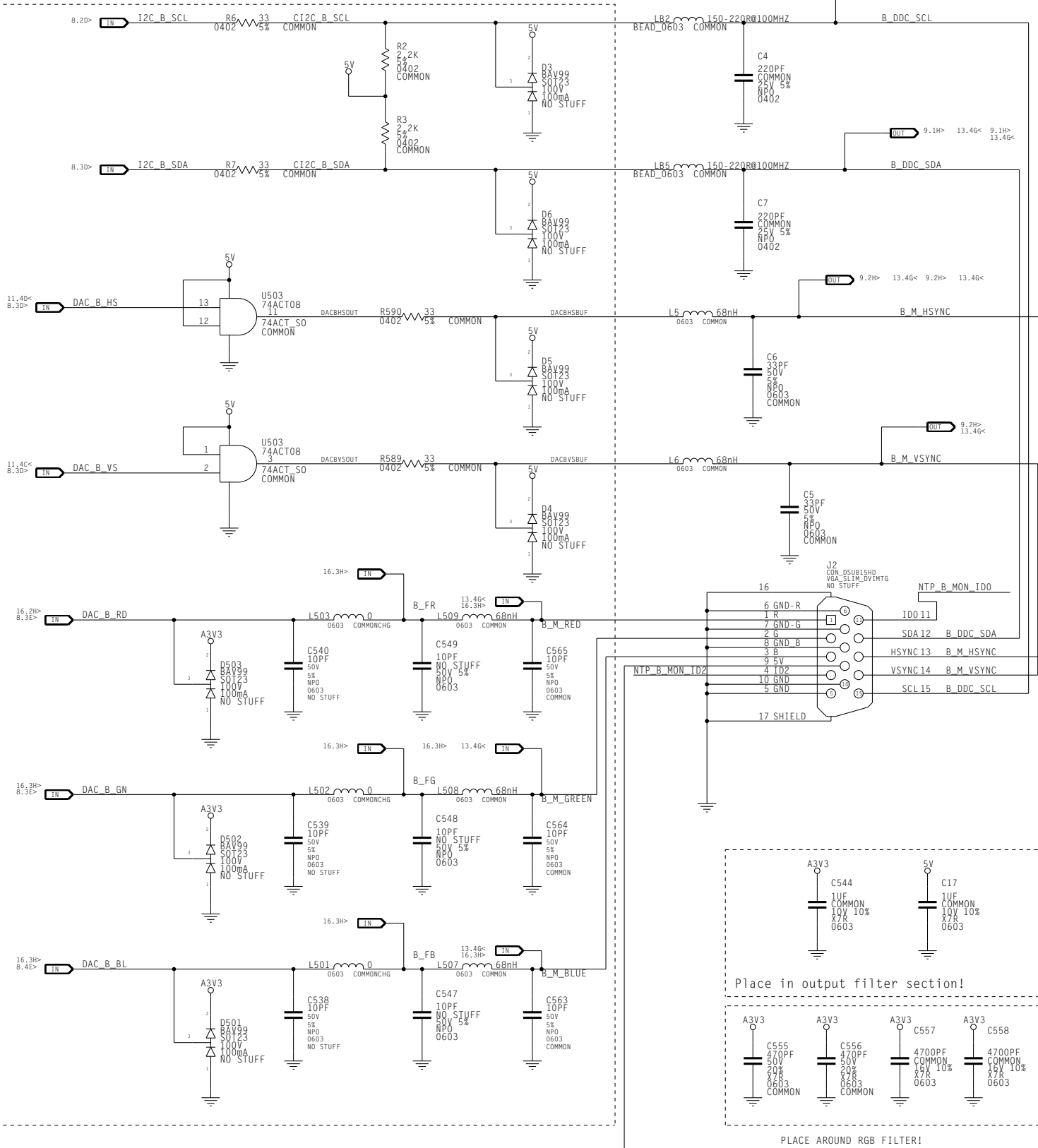




DAC A RGB-FILTER



DAC B RGB-FILTER



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DETAIL	DACA, DACB display filter and connector	
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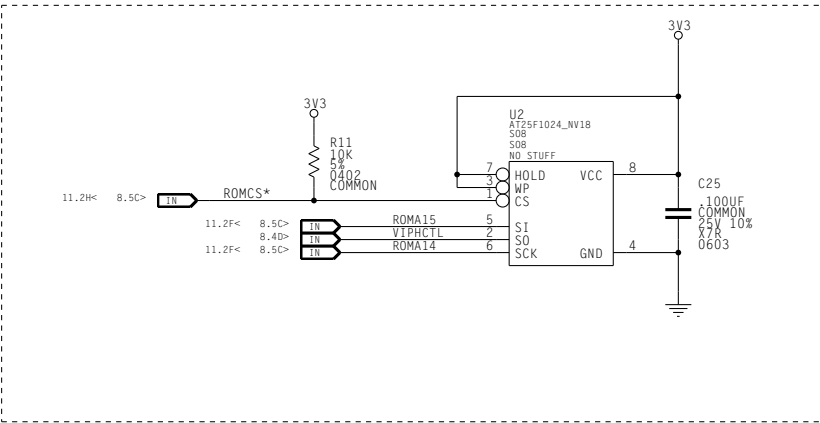
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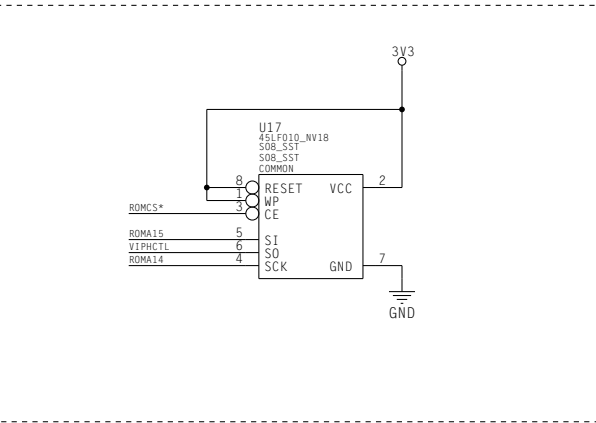
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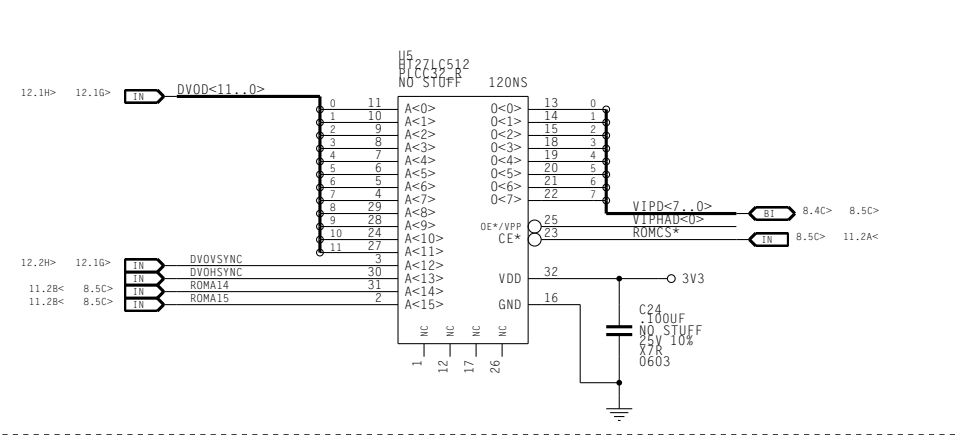
ATL BIOS (ATMEL Serial ROM)



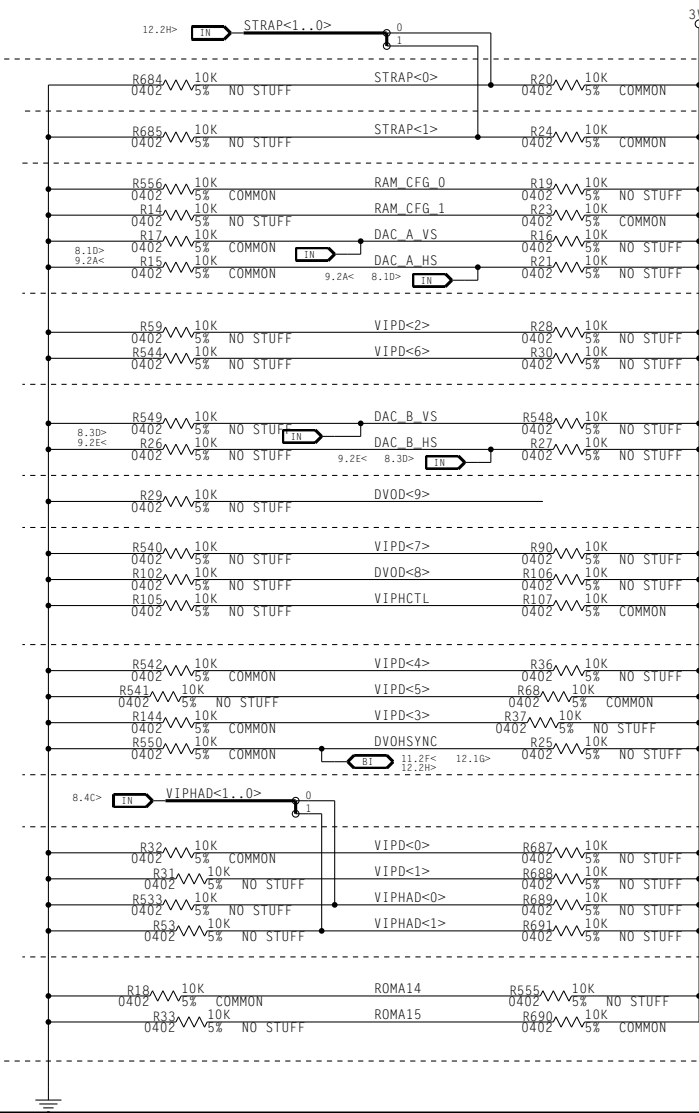
BIOS (SST Serial ROM)



PARALLEL EPROM



STRAPPING

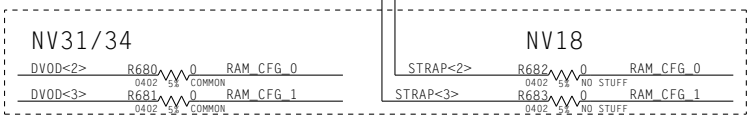


NV18B

NV34

PCI_AD	PCI_AD	1 : NORMAL	default
SUB_VENDOR	SUB_VENDOR	1 : Adapter BIOS	default
RAM_CFG_0	RAM_CFG_0	[3:0]	0011: NV18, 8Mx16 D Samsung 0001: NV18, 8Mx16 E Samsung 0010: NV34, 8Mx16 Samsung
RAM_CFG_1	RAM_CFG_1		
RAM_CFG_2	RAM_CFG_2		
RAM_CFG_3	RAM_CFG_3		
CRYSTAL_0	CRYSTAL_0	[1:0]	00 : 13.5 MHz 01 : 14.31 MHz 10 : 27 MHz 11 : NOT SUPPORTED
CRYSTAL_1	CRYSTAL_1		
TVMODE_0	TVMODE_0	[1:0]	00 : SECAM 01 : NTSC 10 : PAL 11 : VGA
TVMODE_1	TVMODE_1		
0 DEFAULT	AGP4x	0 : enabled 1 : disabled	
AGP_SBA	AGP_SBA	0 : enabled 1 : disabled	
AGP_FASTRWR	0 DEFAULT		
BUS_TYPE - PCI	BUS_TYPE - AGP	1 : AGP	default
PCI_DEVID_0	PCI_DEVID_0		
PCI_DEVID_1	PCI_DEVID_1	[3:0]	0001: NV18B-A3 0x181
PCI_DEVID_2	PCI_DEVID_2		
PCI_DEVID_3	PCI_DEVID_3		
USER_0	USER_0		default
USER_1	USER_1		
USER_2	USER_2		
USER_3	USER_3		
ROMTYPE_0	ROMTYPE_0	[1:0]	00 : Parallel OTP option 01 : Serial AT25F 10 : Serial SST
ROMTYPE_1	ROMTYPE_1		default

RAM CONFIG OPTIONS



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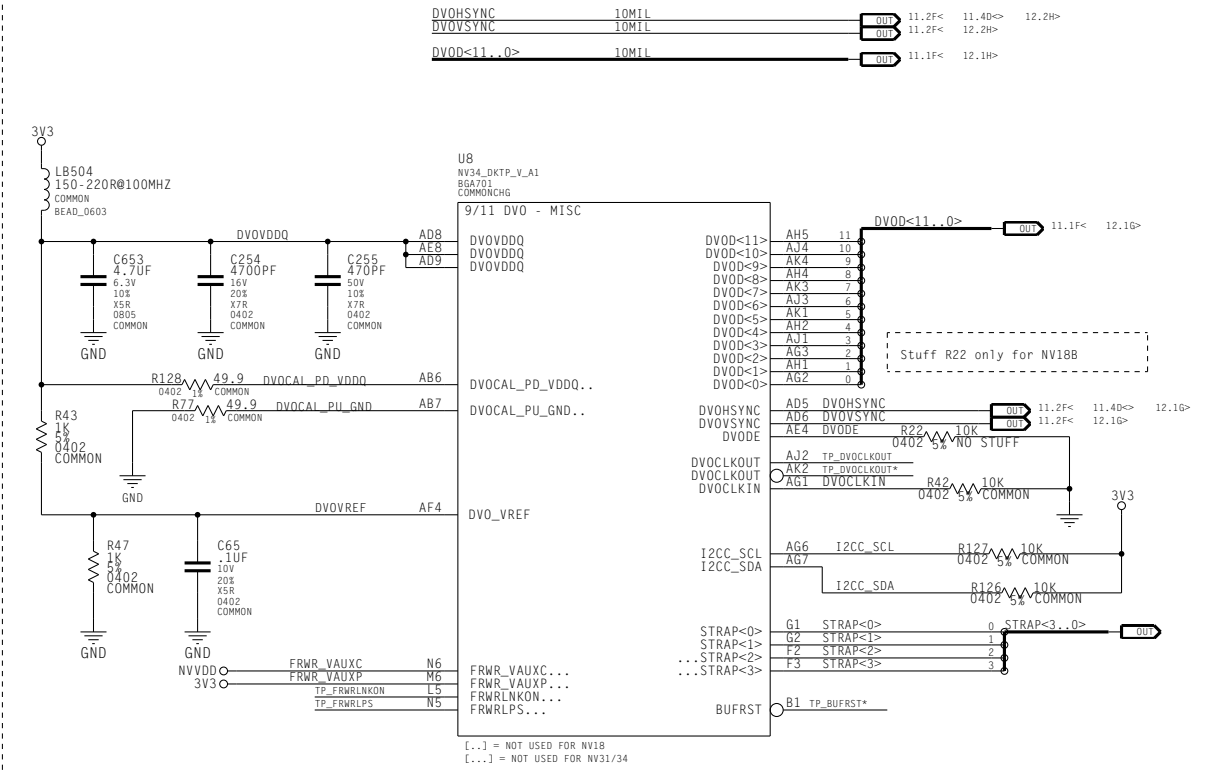
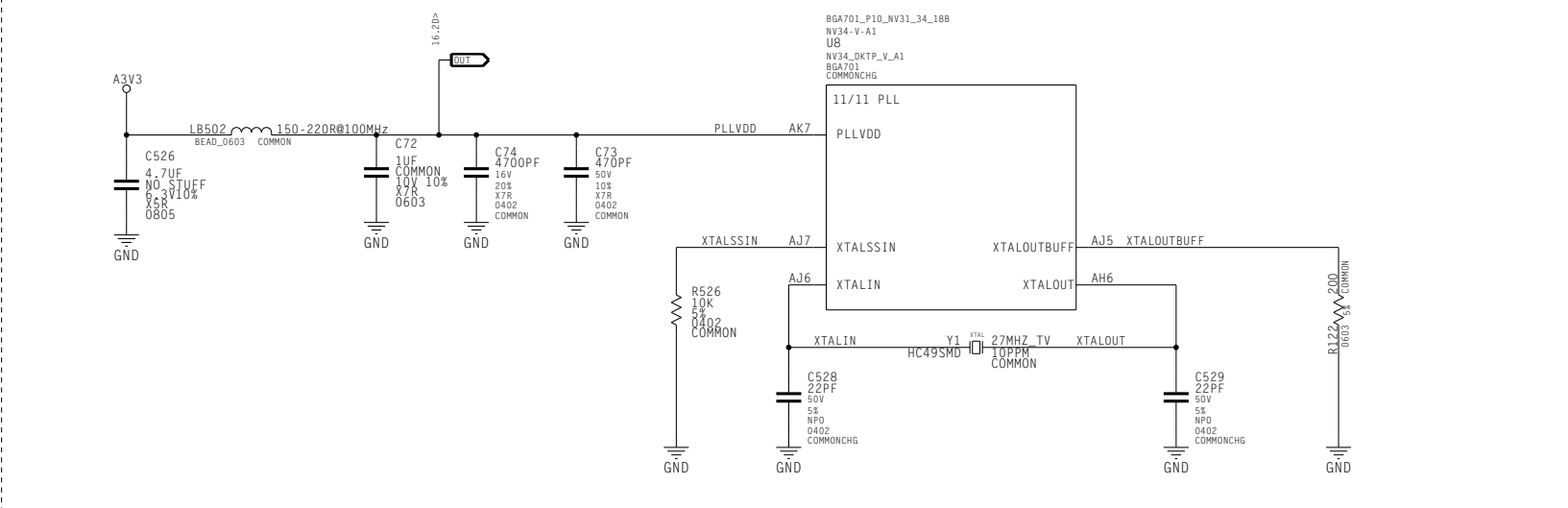
DETAIL NV17 STRAPPING, BIOS

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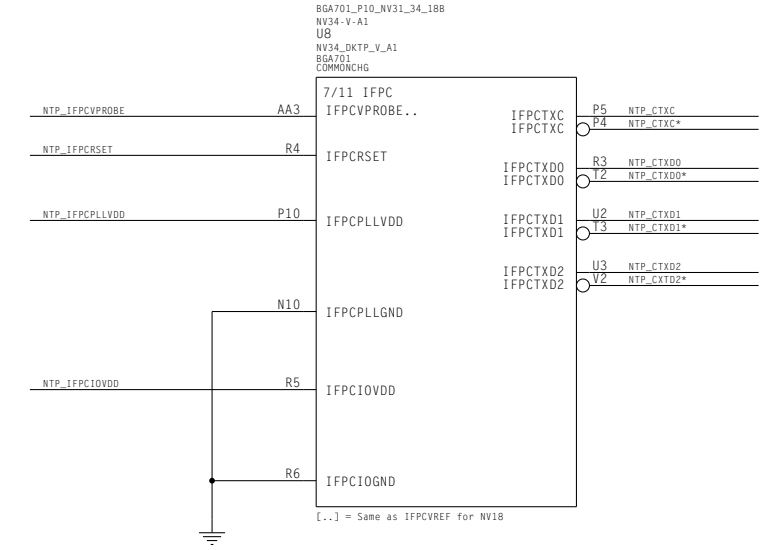
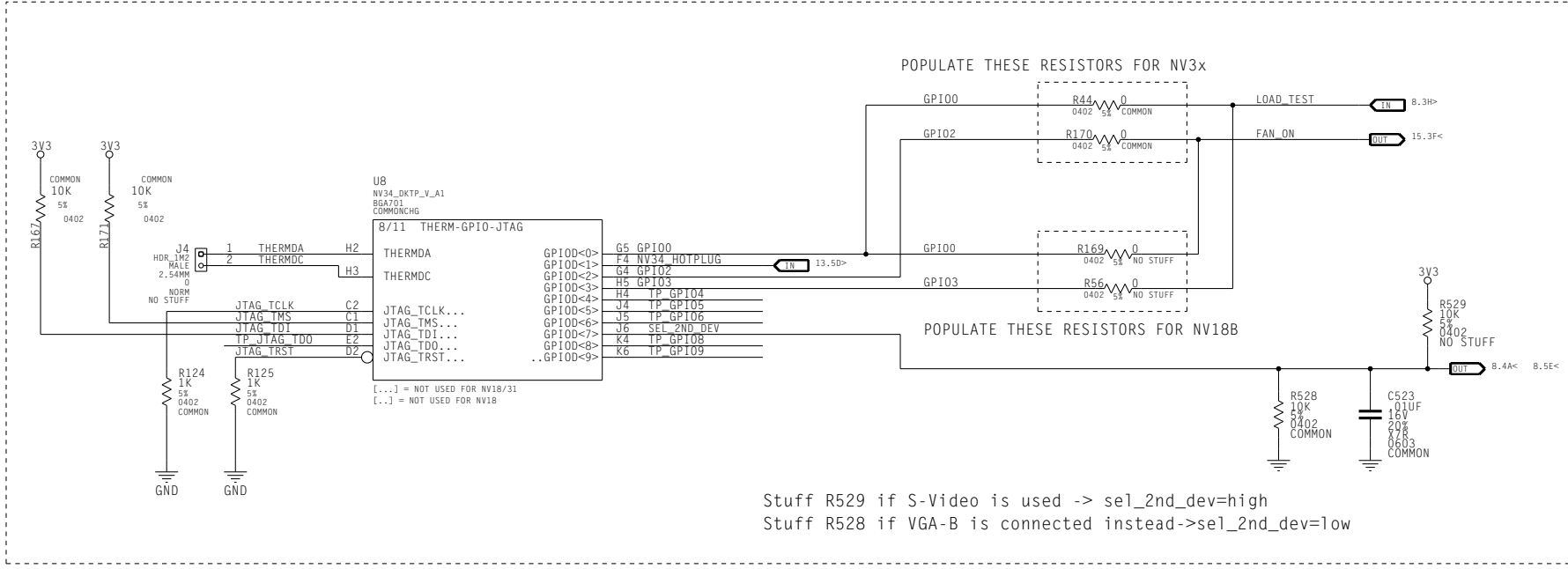
CLOCK

DVO

NET_PHYSICAL_TYPE	NET_SPACING_TYPE	NO_GLOSS
XTALIN	10MIL_TRACE	20MIL
XTALOUT	10MIL_TRACE	20MIL



JTAG, THERMAL and GPIOs



Stuff R529 if S-Video is used -> sel_2nd_dev=high
Stuff R528 if VGA-B is connected instead->sel_2nd_dev=low

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5

DETAIL	Power Supplies: A3V3,TMDS3V3, TMDSPLLVDD, FBVDDQ, NVVDD		
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NET RULES

Power Nets:

	NET_PHYSICAL_TYPE	NET_SPACING_TYPE
GND 	GND	12MIL_TRACE
5V 	5V	12MIL_TRACE
A3V3 	A3V3	12MIL_TRACE
3V3 	3V3	12MIL_TRACE
AGPVDDQ 	AGPVDDQ	12MIL_TRACE
FBVDDQ 	FBVDDQ	12MIL_TRACE
FBVDD 	FBVDD	12MIL_TRACE
NVVDD 	NVVDD	12MIL_TRACE
	DAC_A_VDD	12MIL_TRACE  8.1B>
	DAC_B_VDD	12MIL_TRACE  8.2B>
	PLLVD	12MIL_TRACE  12.1B>
	DDC_VCC	12MIL_TRACE  9.5C< 13.4G< 14.1G<
	FBVREF	12MIL_TRACE  3.5B>

RAM_DAC : impedance controlled by constraint manager

	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	NO_GLOSS
DAC_A_RED	20MIL	TRUE	 8.2D> 9.3A<
DAC_A_GREEN	20MIL	TRUE	 8.2D> 9.4A<
DAC_A_BLUE	20MIL	TRUE	 8.2D> 9.4A<
FR	20MIL	TRUE	 9.3B<
FG	20MIL	TRUE	 9.3B<
FB	20MIL	TRUE	 9.4B<
M_RED	20MIL	TRUE	 9.3B<
M_GREEN	20MIL	TRUE	 9.3B<
M_BLUE	20MIL	TRUE	 9.4B<
DAC_B_RED	20MIL	TRUE	 8.3D>
DAC_B_GREEN	20MIL	TRUE	 8.3D>
DAC_B_BLUE	20MIL	TRUE	 8.3D>
DAC_B_YOUT	20MIL	TRUE	 8.2E>
DAC_B_COUT	20MIL	TRUE	 8.1E>
CVBS_YOUT	20MIL	TRUE	 8.2G>
COUT	20MIL	TRUE	 8.1F>
DAC_B_RD	20MIL	TRUE	 8.3E> 9.3E<
DAC_B_GN	20MIL	TRUE	 8.3E> 9.4E<
DAC_B_BL	20MIL	TRUE	 8.4E> 9.4E<
B_FR	20MIL	TRUE	 9.3F<
B_FG	20MIL	TRUE	 9.3F<
B_FB	20MIL	TRUE	 9.4F<
B_M_RED	20MIL	TRUE	 9.3F< 13.4G<
B_M_GREEN	20MIL	TRUE	 9.3F< 13.4G<
B_M_BLUE	20MIL	TRUE	 9.4F< 13.4G<

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DETAIL DESIGN NET RULES

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1	R93 R 2.5C R94 R 2.5C R95 R 3.5A R96 R 3.5A R97 R 8.2B R98 R 8.4A R99 R 8.5A R100 R 8.2D R101 R 2.5D R102 R 11.4C R103 R 2.4D R104 R 2.5C R105 R 11.4C R106 R 11.4D R107 R 11.4D R108 R 13.3F R109 R 13.4F R110 R 13.3F R111 R 13.4F R112 R 13.5F R113 R 13.5F R115 R 14.4B R116 R 14.4B R117 R 14.3C R118 R 14.3C R119 R 14.4C R120 R 8.3D R121 R 14.4C R122 R 12.2D R123 R 8.3F R124 R 12.4B R125 R 12.4B R126 R 12.2H R127 R 12.2H R128 R 12.2F R129 R 14.4D R130 R 14.4D R131 R 14.5F R132 R 13.1D R133 R 13.2D R134 R 14.4F R135 R 14.5F R136 R 14.4G R137 R 14.4F R138 R 15.3F R140 R 15.3A R141 R 15.3B R142 R 15.3A R144 R 11.4C R145 R 15.3C R146 R 15.3C R147 R 15.3C R148 R 15.3C R149 R 15.3C R150 R 15.3C R151 R 15.3C R152 R 15.3C R153 R 15.3C R154 R 15.4C R155 R 15.4C R156 R 15.4C R157 R 15.4C R158 R 15.4C R159 R 15.4C R160 R 15.4C R161 R 15.4C R164 R 15.3F R165 R 13.1B R166 R 13.2B R167 R 12.4B R168 R 15.3C R169 R 12.4E R170 R 12.4E R171 R 12.4B R253 R 2.4B R257 R 8.4C R258 R 8.4C R501 R 4.5E R502 R 4.5E R504 R 4.5E R505 R 5.5E R506 R 5.5E R508 R 5.5E R517 R 2.4D R520 R 6.5E R521 R 6.5E R523 R 6.5E R524 R 2.4D R525 R 2.4E R526 R 12.2C R527 R 8.2B R528 R 12.4E R529 R 12.4F R533 R 11.5C R534 R 2.4B R536 R 7.5E R537 R 7.5E R538 R 7.5E R540 R 11.4C R541 R 11.4C R542 R 11.4C R544 R 11.3C R547 R 2.4A R548 R 11.4D R549 R 11.4C R550 R 11.4C R551 R 2.5D R552 R 2.5D R555 R 11.5D R556 R 11.3C R562 R 9.4A R563 R 9.4A R564 R 9.3A	R565 R 8.3F R567 R 8.3F R568 R 8.3F R569 R 8.3F R570 R 8.3F R571 R 9.4A R572 R 9.4A R573 R 9.3A R574 R 9.2B R581 R 9.2B R583 R 8.5F R584 R 8.4G R585 R 8.4G R587 R 8.4G R588 R 8.4G R589 R 9.2F R590 R 9.2F R591 R 10.2D R592 R 10.2D R601 R 8.3A R645 R 2.4A R646 R 2.4A R670 R 4.5E R671 R 4.5E R672 R 5.5E R673 R 5.5E R674 R 6.5E R675 R 6.5E R676 R 7.5E R677 R 7.5E R680 R 11.3A R681 R 11.3A R682 R 11.3B R683 R 11.3B R684 R 11.3C R685 R 11.3C R687 R 11.5D R688 R 11.5D R689 R 11.5D R690 R 11.5D R691 R 11.5D R692 R 8.2G R693 R 8.2H RP1 R_PAK 5.2A RP2 R_PAK 5.2A 5.3A 5.3A RP3 R_PAK 5.3A RP4 R_PAK 4.4A RP5 R_PAK 5.4A RP6 R_PAK 7.4A RP7 R_PAK 7.3A 7.3A 7.4A RP8 R_PAK 7.2A RP9 R_PAK 5.5B RP10 R_PAK 7.5B RP11 R_PAK 5.5B RP501 R_PAK 4.4A RP502 R_PAK 5.4A RP503 R_PAK 4.5B RP504 R_PAK 5.3A RP505 R_PAK 4.3A RP506 R_PAK 6.3A RP507 R_PAK 6.3A RP508 R_PAK 6.5B RP509 R_PAK 6.4A RP510 R_PAK 5.4A RP511 R_PAK 6.4A RP512 R_PAK 5.3A 5.3A 5.4A RP513 R_PAK 4.3A RP514 R_PAK 4.3A 4.4A RP515 R_PAK 4.5B RP516 R_PAK 4.2A 4.3A RP517 R_PAK 4.2A RP518 R_PAK 4.4A RP519 R_PAK 7.2A 7.3A 7.3A RP520 R_PAK 7.3A RP521 R_PAK 7.3B RP522 R_PAK 7.4A RP523 R_PAK 7.4A RP524 R_PAK 7.4A RP525 R_PAK 6.2A RP526 R_PAK 6.2A 6.3A 6.3A RP527 R_PAK 6.5B RP528 R_PAK 6.3A 6.3A 6.4A RP529 R_PAK 6.4A TP1 TESTPOINT 14.4A TP2 TESTPOINT 14.4B TP3 TESTPOINT 14.4C TP4 TESTPOINT 14.4F TP5 TESTPOINT 14.5G TP6 TESTPOINT 14.4H U1 U_VREG_3PIN 10.2D U2 U_MEM_FL_SER_12BKX8 11.1B U3 U_SWREG_ISL6529 14.4C U4 U_VREG_5PIN 13.1C U5 U_MEM_EP_OTP_64KX8 11.1G U6 U_MEM_SD_DDR_4_BMX16 6.4C 6.4E 7.2E U7 U_MEM_SD_DDR_4_BMX16 6.3C 6.3E 7.2C U8 U_GPU_DDR2M64X2-V1 2.1E 3.1B 3.1F 8.1B 8.2B 8.4B 12.1C 12.1F 12.3G 12.4C 13.3C U9 U_MEM_SD_DDR_4_BMX16 6.2E 7.4D 7.4E U10 U_MEM_SD_DDR_4_BMX16 6.2C 7.3D 7.3E U11 U_MEM_SD_DDR_4_BMX16 4.4C 4.4E 5.2E U12 U_MEM_SD_DDR_4_BMX16 4.3C 4.3E 5.2C U13 U_MEM_SD_DDR_4_BMX16 4.2E 5.4D 5.4E U14 U_MEM_SD_DDR_4_BMX16 4.2C 5.3D 5.3E U16 U_VREG_5PIN 13.1A U17 U_MEM_FL_SER_12BKX8 11.1D U502 U_SW_ANA_32S7 8.3F 8.4F 8.5F U503 U_AND_2TIN 9.2B 9.2F Y1 XTAL 12.2C							
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