NDU00/NDU10

Streamline-S 11.6"

Streamline-M 13.3"

LA-6031P REV 1.0 Schematic

Intel Arrandale SFF/IBEX PEAK

2010-04-12 Rev 1.0

Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

Compal Electronics, Inc.

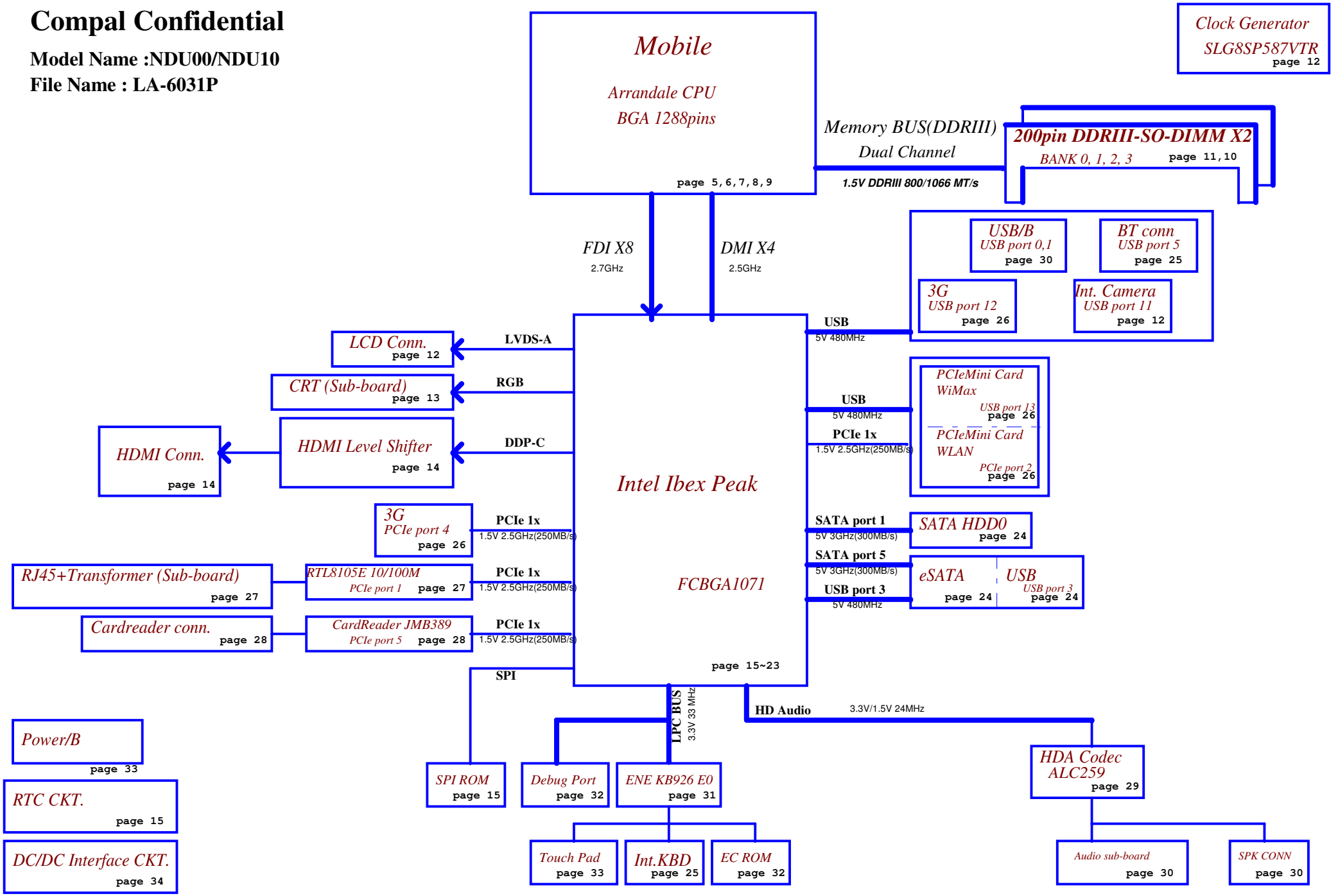
Title: **Cover Page**

Size	Document Number	Rev
B	NDU00_LA-6031P M/B	1.0

Date: Monday, April 12, 2010 Sheet 1 of 45

Compal Confidential

Model Name :NDU00/NDU10
File Name : LA-6031P

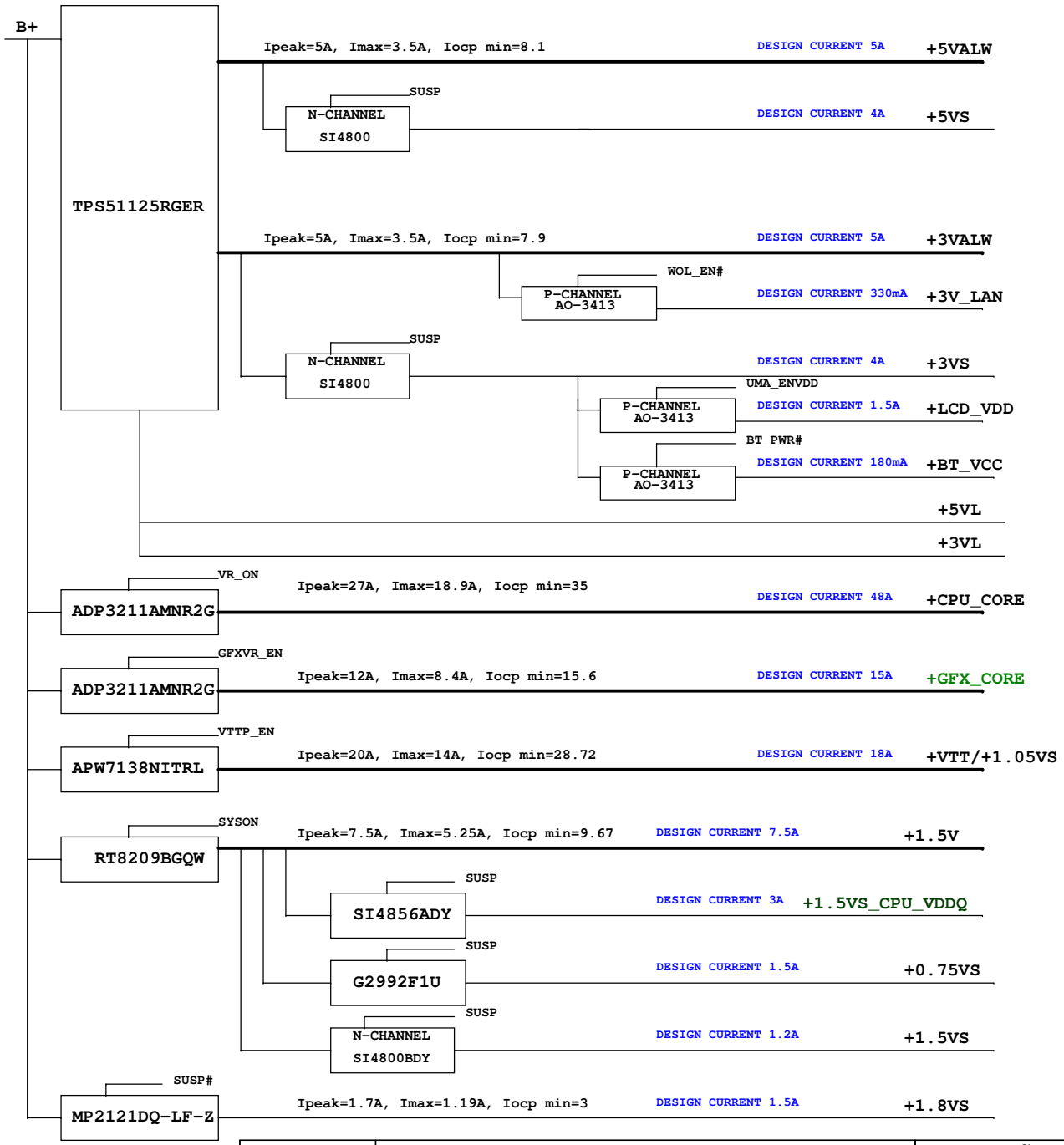


Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title	Block Diagrams	
Size	Document Number: NDU00_LA-6031P M/B	Rev: 1.0
Date: Monday, April 12, 2010	Sheet 2 of 45	

NSWAA Liverpool Intel Arrandale
NTWAA Sunderland Intel Arrandale



Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **Power Tree**

Size	Document Number	Rev
	NDU00_LA-6031P M/B	1.0

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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane / State	+RTCVCC	+B +5VL +3VL	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +GFX_CORE +CPU_CORE +VTT +0.75VS +1.8VS +1.5VS_CPU_VDDQ
S0	O	O	O	O	O
S1	O	O	O	O	O
S3	O	O	O	O	X
S5 S4/AC	O	O	O	X	X
S5 S4/ Battery only	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X

BTO Option Table

Function	Bluetooth	HDMI	3G	Mini Card	Mini Card	Gensor	
						main	2nd
explain	Bluetooth	HDMI	3G	WIRELESS	WIMAX	R5F211B4D31SP	R5F211B4D34SP
BTO	BT@	IHDMI@	3G@	WLAN@	WIMAX@	GSENSOR@ 1STGSENSOR@ 1ST@	GSENSOR@ 2NDGSENSOR@ 2ND@

STATE / SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1(Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

EC SM Bus1 address

Power	Device	Address
+3VL	EC KB926 D3	
+3VL	Smart Battery	0001 011x b

EC SM Bus2 address

Power	Device	Address
+3VS	EC KB926 D3	
+3VS	Gensor	
+3VS	PCH	0100 110x b

PCH SM Bus address

Power	Device	Address
+3VALW	PCH	
+3VS	Clock Generator	1101 001x b
+3VS	DDR DIMM0	1001 000x b
+3VS	DDR DIMM1	1001 010x b
+3VS	WLAN/Wimax/3G	

Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **Notes List**

Size: Custom | Document Number: **NDU00_LA-6031P M/B** | Rev: 1.0

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Layout rule：10mil width
trace length < 0.5",
spacing 20mil

U1B

Misc
Clocks
Thermal
DDR3 Misc
Power Management
JTAG & MBP

COMP3 COMP2 COMP1 COMP0 PROC_DETECT CATERR# PECI PROCHOT# THERMTRIP# RESET_OBS# PM_SYNC VCCPWRGOOD_1 VCCPWRGOOD_0 SM_DRAMPWROK VTTPWRGOOD TAPPWRGD RSTIN#

INTEL_ARRANDALE_1288

BCLK BCLK# BCLK_ITP BCLK_ITP# PEG_CLK PEG_CLK# DPLL_REF_SSCLK DPLL_REF_SSCLK#

SM_DRAMRST# SM_RCOMP[0] SM_RCOMP[1] SM_RCOMP[2] PM_EXT_TS[0] PM_EXT_TS[1]

PRDY# PREQ# TCK TMS TRST# TDI TDO TDI_M TDO_M DBR#

BPM[0] BPM[1] BPM[2] BPM[3] BPM[4] BPM[5] BPM[6] BPM[7]

Design guide
1.11update,PLTRST series
resittor 1.5K, PL
resistor 750 ohm

For S3 CPU power saving

JTAG MAPPING

Scan Chain (Default)	STUFF -> R20, R23, R27 NO STUFF -> R21, R26
CPU Only	STUFF -> R20, R21 NO STUFF -> R23, R26, R27
GMCH Only	STUFF -> R26, R27 NO STUFF -> R20, R21, R23

EMI reverse, close to CPU

For S3 CPU power saving

12/22 follow NWQAA

XDP Connector

JXDP1

SAMTE_BSH-030-01-L-D-A

Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: CPU CLK/MISC/JTAG

Size: Custom | Document Number: NDU00_LA-6031P M/B | Rev: 1.0

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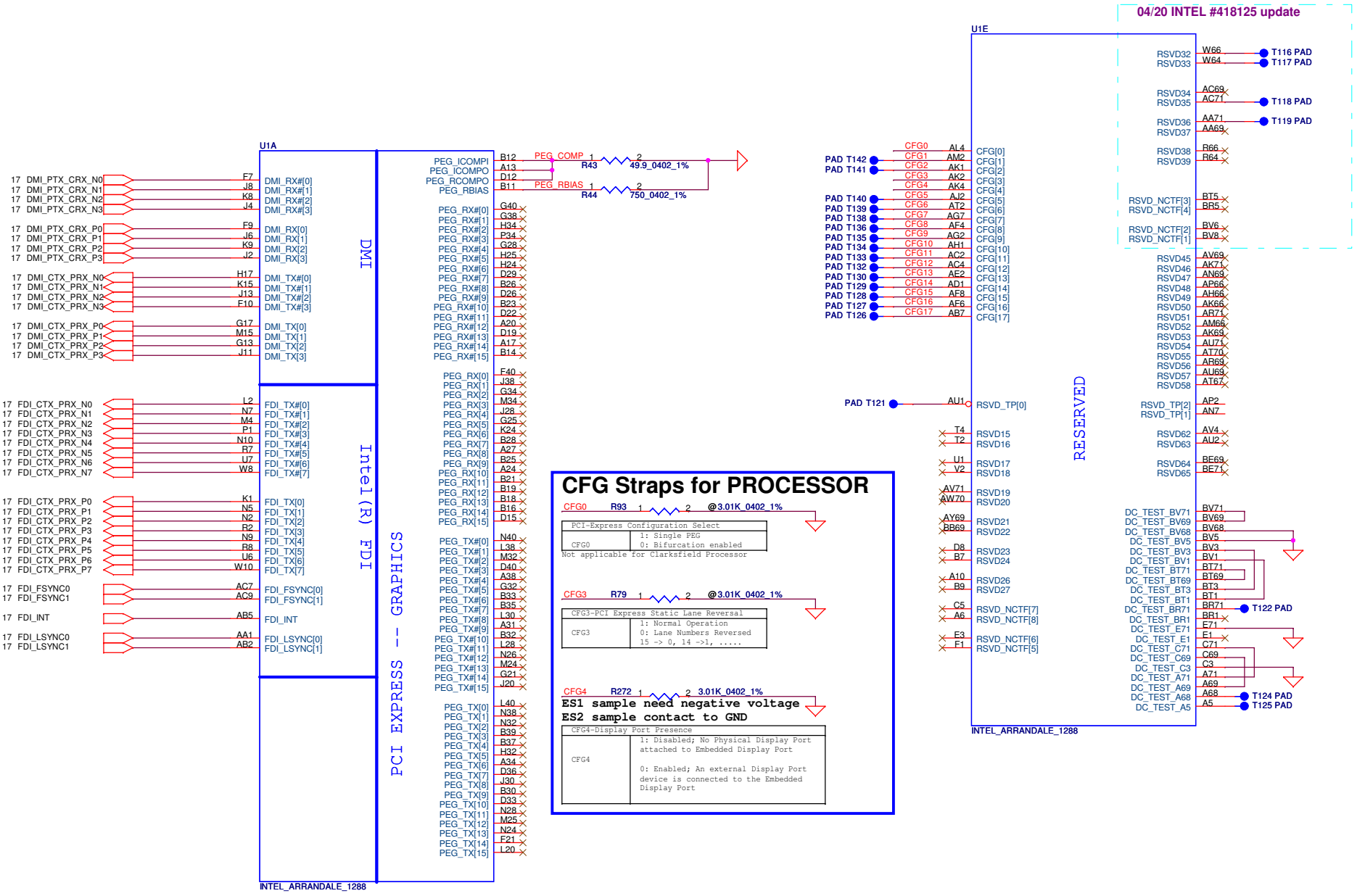

Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **CPU DMI/FDI/PEG**

Size	Document Number	Rev
B	NDU00_LA-6031P M/B	1.0

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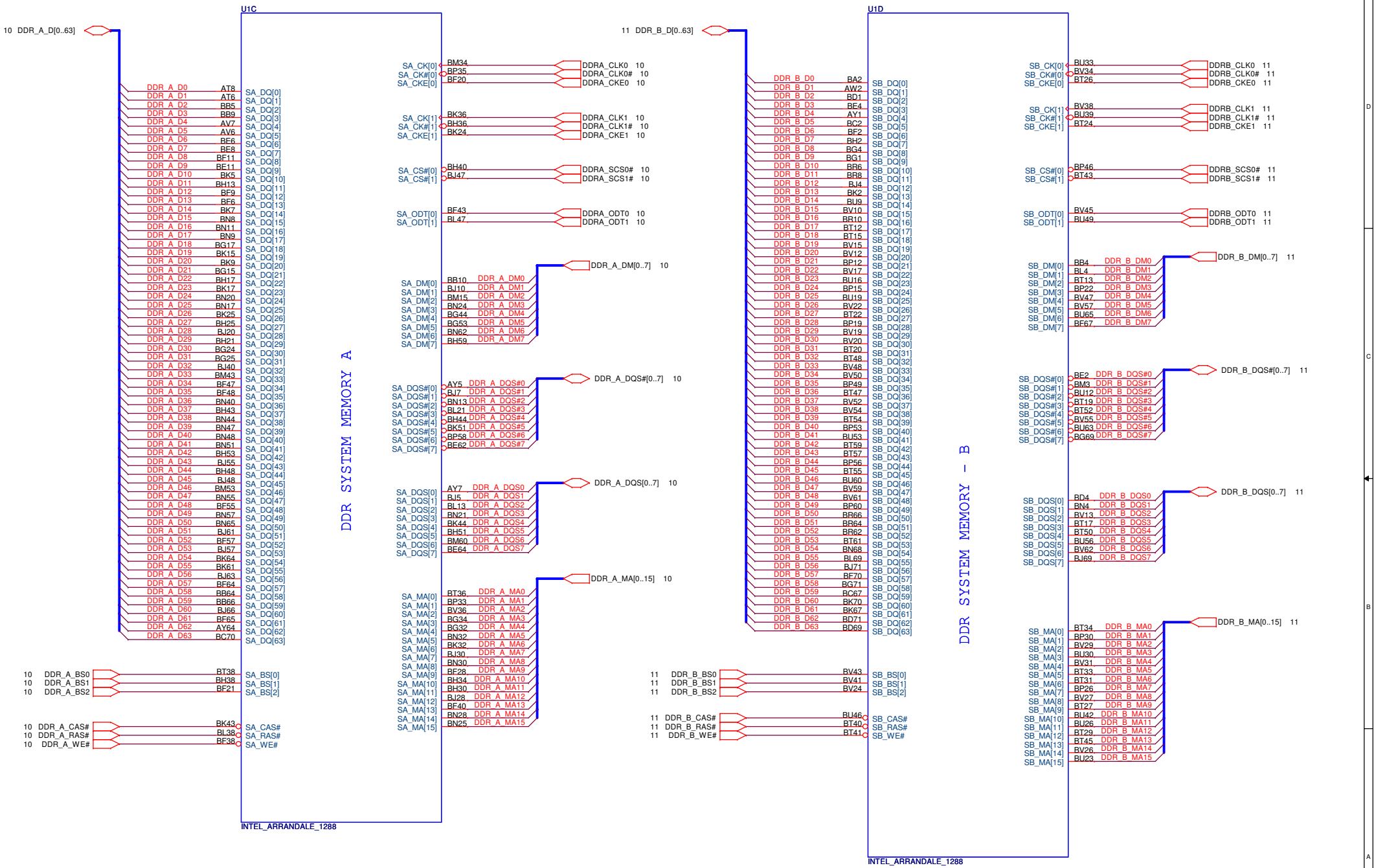

Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **CPU DDRIII**

Size	Document Number	Rev
B	NDU00_LA-6031P M/B	1.0

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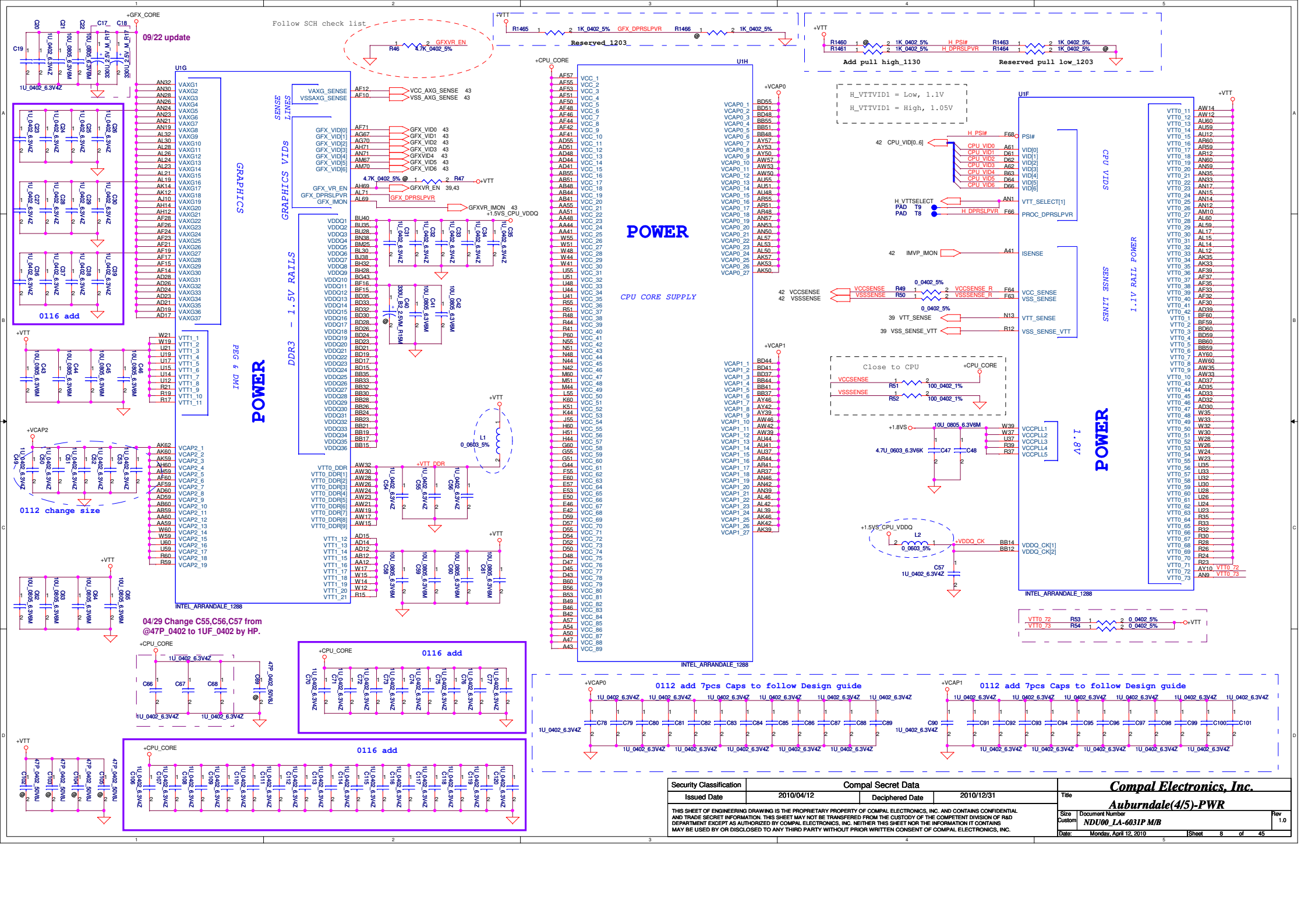
Follow SCH check list
09/22 update
0116 add
0112 change size
04/29 Change C55,C56,C57 from
@47P_0402 to 1UF_0402 by HP.
Reserved_1203
Add pull high_1130
Reserved pull low_1203
H_VTTVID1 = Low, 1.1V
H_VTTVID1 = High, 1.05V
Close to CPU
0112 add 7pcs Caps to follow Design guide
POWER
CPU CORE SUPPLY
DDR3 - 1.5V RAILS
PCH & DMI
GRAPHICS
GRAPHICS VIDs
SENSE LINES
CPU VIDS
1.1V RAIL POWER
1.8V
INTEL_ARRANDALE_1288
Compal Secret Data
2010/04/12
2010/12/31
Compal Electronics, Inc.
Auburndale(4/5)-PWR
NDU00_LA-6031P M/B
Monday, April 12, 2010
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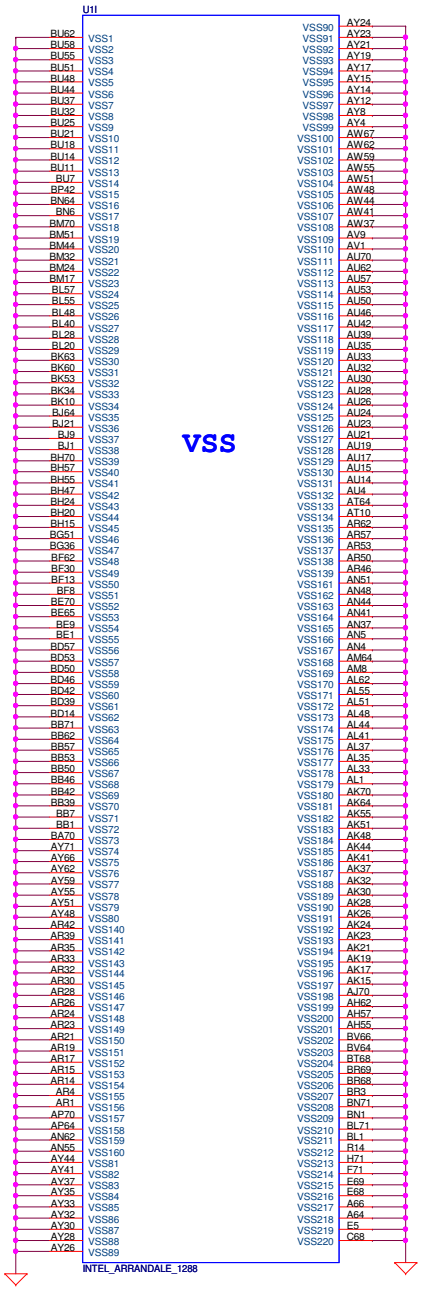

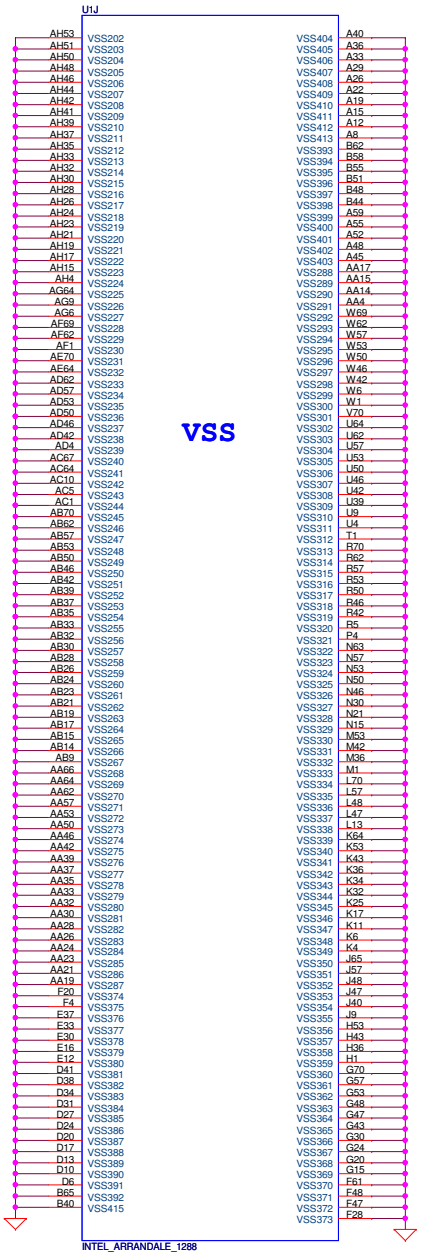

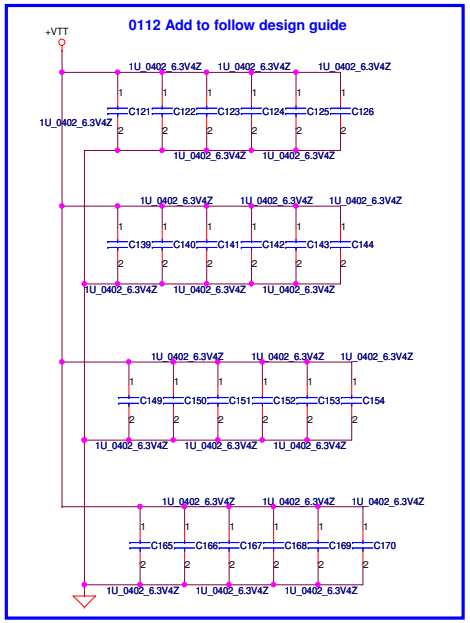

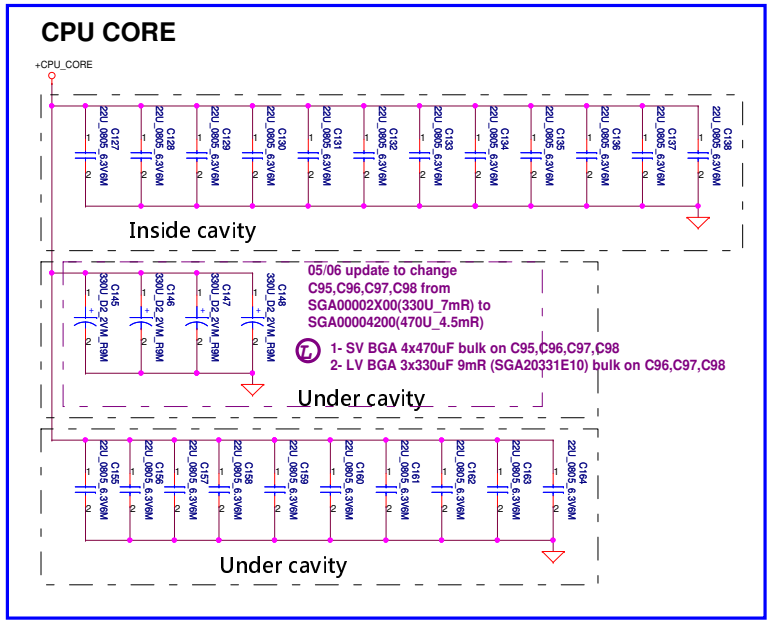

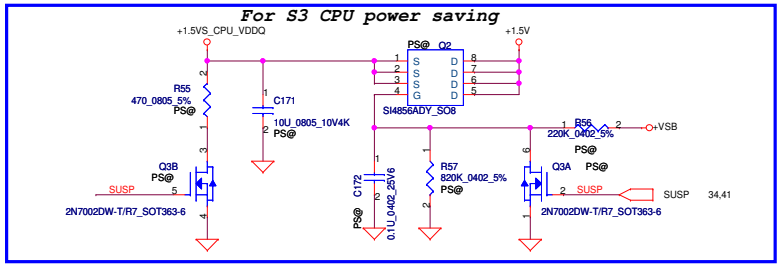

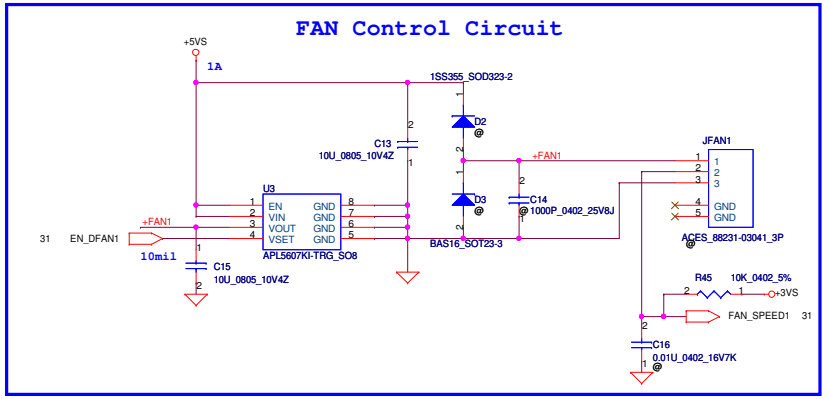

Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: Auburndale(5/5)-GND/Bypass

Size	Document Number	Rev
Custom	NDU00_LA-6031P M/B	1.0

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DDR3 SO-DIMM A
Standard Type

JDDRL1

+VREF_DQA

+1.5V

C173 0.1U_0402_16V4Z

C174 22U_0603_6.3V4Z

close to JDDRL.1

R60 1K_0402_1% PS@

For S3 CPU power saving

SM_DRAMRST# 5,11

7 DDR_A_DQS[0..7]
7 DDR_A_DQS#[0..7]
7 DDR_A_D[0..63]
7 DDR_A_DM[0..7]
7 DDR_A_MA[0..15]

M1 Circuit

R59 1K_0402_1%
R62 1K_0402_1%
+V_DDR3_DIMM_REF
R58 0_0402_5%
R61 0_0402_5%
+VREF_DQB
+VREF_DQA

VREF_DQ	1	2	VSS1
VSS2	3	4	DQ4
DQ0	5	6	DQ5
DQ1	7	8	VSS3
VSS4	9	10	DQS#0
DM0	11	12	DQS0
VSS5	13	14	VSS6
DQ2	15	16	DQ6
DQ3	17	18	DQ7
VSS7	19	20	VSS8
DQ8	21	22	DQ12
DQ9	23	24	DQ13
VSS9	25	26	VSS10
DQS#1	27	28	DM1
DQS1	29	30	RESET#
VSS11	31	32	VSS12
DQ10	33	34	DQ14
DQ11	35	36	DQ15
VSS13	37	38	VSS14
DQ16	39	40	DQ20
DQ17	41	42	DQ21
VSS15	43	44	VSS16
DQS#2	45	46	DM2
DQS2	47	48	VSS17
VSS18	49	50	DQ22
DQ18	51	52	DQ23
DQ19	53	54	VSS19
VSS20	55	56	DQ28
DQ24	57	58	DQ29
DQ25	59	60	VSS21
VSS22	61	62	DQS#3
DM3	63	64	DQS3
VSS23	65	66	VSS24
DQ26	67	68	DQ30
DQ27	69	70	DQ31
VSS25	71	72	VSS26
CKE0	73	74	CKE1
VDD1	75	76	VDD2
NC1	77	78	A15
BA2	79	80	A14
VDD3	81	82	VDD4
A12/BC#	83	84	A11
A9	85	86	A7
VDD5	87	88	VDD6
A8	89	90	A6
A5	91	92	A4
VDD7	93	94	VDD8
A3	95	96	A2
A1	97	98	A0
VDD9	99	100	VDD10
CK0	101	102	CK1
CK0#	103	104	CK1#
VDD11	105	106	VDD12
A10/AP	107	108	BA1
BA0	109	110	RAS#
VDD13	111	112	VDD14
WE#	113	114	S0#
CAS#	115	116	ODT0
VDD15	117	118	VDD16
A13	119	120	ODT1
S1#	121	122	NC2
VDD17	123	124	VDD18
NCTEST	125	126	VREF_CA
VSS27	127	128	VSS28
DQ32	129	130	DQ36
DQ33	131	132	DQ37
VSS29	133	134	VSS30
DQS#4	135	136	DM4
DQS4	137	138	VSS31
VSS32	139	140	DQ38
DQ34	141	142	DQ39
DQ35	143	144	VSS33
VSS34	145	146	DQ44
DQ40	147	148	DQ45
DQ41	149	150	VSS35
VSS36	151	152	DQS#5
DM5	153	154	DQS5
VSS37	155	156	VSS38
DQ42	157	158	DQ46
DQ43	159	160	DQ47
VSS39	161	162	VSS40
DQ48	163	164	DQ52
DQ49	165	166	DQ53
VSS41	167	168	VSS42
DQS#6	169	170	DM6
DQS6	171	172	VSS43
VSS44	173	174	DQ54
DQ50	175	176	DQ55
DQ51	177	178	VSS45
VSS46	179	180	DQ60
DQ56	181	182	DQ61
DQ57	183	184	VSS47
VSS48	185	186	DQS#7
DM7	187	188	DQS7
VSS49	189	190	VSS50
DQ58	191	192	DQ62
DQ59	193	194	DQ63
VSS51	195	196	VSS52
SA0	197	198	EVENT#
VDDSPD	199	200	SDA
SA1	201	202	SCL
VTT1	203	204	VTT2
G1	205	206	G2

@FOX_AS0A626-U4SG-7H

DDRA_CKE0 7
DDRA_CKE1 7
DDR_A_BS2 7
DDRA_CLK0 7
DDRA_CLK0# 7
DDRA_CLK1 7
DDRA_CLK1# 7
DDR_A_BS0 7
DDR_A_BS1 7
DDR_A_RAS# 7
DDR_A_WE# 7
DDR_A_CAS# 7
DDRA_SCS0# 7
DDRA_ODT0 7
DDRA_SCS1# 7
DDRA_ODT1 7

+V_DDR3_DIMM_REF
R63 0_0402_5%
+DDR_VREF_CA_DIMMA
C175 2.2U_0603_6.3V4Z
C176 0.1U_0402_16V4Z
close to JDDRL.126

Reserve for cost down
C192 330U_2.5V_M_R17

+3VS
C194 2.2U_0603_6.3V4Z
C195 0.1U_0402_16V4Z
R64 10K_0402_5%
R65 10K_0402_5%
+0.75VS

PM_EXTTS# 5,11
PM_SMBDATA 11,12,16,20
PM_SMBCLK 11,12,16,20

Layout Note:
Place near JDDRL

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

C177 @ 330U_B2_2.5VM_R15M
C180 10U_0805_6.3V6M
C182 10U_0805_6.3V6M
C185 10U_0805_6.3V6M
C188 10U_0805_6.3V6M
C190 10U_0805_6.3V6M
C193 10U_0805_6.3V6M

C178 0.1U_0402_16V4Z
C181 0.1U_0402_16V4Z
C184 0.1U_0402_16V4Z
C187 0.1U_0402_16V4Z

Layout Note:
Place near JDDRL1.203 and 204

C179 10U_0805_6.3V6M
C183 1U_0402_6.3V4Z
C186 1U_0402_6.3V4Z
C189 1U_0402_6.3V4Z
C191 1U_0402_6.3V4Z

Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **DDRIII-SODIMM0**

Size: Custom | Document Number: **NDU00_LA-6031P M/B** | Rev: 1.0

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Standard Type
DDR3 SO-DIMM B

7 DDR_B_DQS#[0..7]
7 DDR_B_DQS[0..7]
7 DDR_B_D[0..63]
7 DDR_B_DM[0..7]
7 DDR_B_MA[0..15]

JDDRH1

+VREF_DQB	1	VREF_DQ	
DDR_B_D0	3	VSS2	
DDR_B_D1	5	DQ0	
	7	DQ1	
DDR_B_DM0	9	VSS3	
	11	DM0	
DDR_B_D2	13	VSS4	
DDR_B_D3	15	DQ2	
	17	DQ3	
DDR_B_D8	19	VSS5	
DDR_B_D9	21	DQ8	
	23	DQ9	
DDR_B_DQS#1	25	VSS6	
DDR_B_DQS1	27	DQS#1	
	29	DQS1	
DDR_B_D10	31	VSS7	
DDR_B_D11	33	DQ10	
	35	DQ11	
DDR_B_D16	37	VSS8	
DDR_B_D17	39	DQ16	
	41	DQ17	
DDR_B_DQS#2	43	VSS9	
DDR_B_DQS2	45	DQS#2	
	47	DQS2	
DDR_B_D18	49	VSS10	
DDR_B_D19	51	DQ18	
	53	DQ19	
DDR_B_D24	55	VSS11	
DDR_B_D25	57	DQ24	
	59	DQ25	
DDR_B_DM3	61	VSS12	
	63	DM3	
DDR_B_D26	65	VSS13	
DDR_B_D27	67	DQ26	
	69	DQ27	
	71	VSS14	
7 DDRB_CKE0	73	CKE0	
	75	VDD1	
7 DDR_B_BS2	77	NC1	
	79	BA2	
DDR_B_MA12	81	VDD2	
DDR_B_MA9	83	A12/BC#	
	85	A9	
DDR_B_MA8	87	VDD3	
DDR_B_MA5	89	A8	
	91	A5	
DDR_B_MA3	93	VDD4	
DDR_B_MA1	95	A3	
	97	A1	
7 DDRB_CLK0	99	VDD5	
7 DDRB_CLK0#	101	CK0	
	103	CK0#	
DDR_B_MA10	105	VDD6	
	107	A10/AP	
7 DDR_B_BS0	109	BA0	
	111	VDD7	
7 DDR_B_WE#	113	WE#	
7 DDR_B_CAS#	115	CAS#	
	117	VDD8	
DDR_B_MA13	119	A13	
7 DDRB_SCS1#	121	S1#	
	123	VDD9	
	125	NCTEST	
	127	VSS15	
DDR_B_D32	129	DQ32	
DDR_B_D33	131	DQ33	
	133	VSS16	
DDR_B_DQS#4	135	DQS#4	
DDR_B_DQS4	137	DQS4	
	139	VSS17	
DDR_B_D34	141	DQ34	
DDR_B_D35	143	DQ35	
	145	VSS18	
DDR_B_D40	147	DQ40	
DDR_B_D41	149	DQ41	
	151	VSS19	
DDR_B_DM5	153	DM5	
	155	VSS20	
DDR_B_D42	157	DQ42	
DDR_B_D43	159	DQ43	
	161	VSS21	
DDR_B_D48	163	DQ48	
DDR_B_D49	165	DQ49	
	167	VSS22	
DDR_B_DQS#6	169	DQS#6	
DDR_B_DQS6	171	DQS6	
	173	VSS23	
DDR_B_D50	175	DQ50	
DDR_B_D51	177	DQ51	
	179	VSS24	
DDR_B_D56	181	DQ56	
DDR_B_D57	183	DQ57	
	185	VSS25	
DDR_B_DM7	187	DM7	
	189	VSS26	
DDR_B_D58	191	DQ58	
DDR_B_D59	193	DQ59	
	195	VSS27	
	197	SA0	
	199	VDDSPD	
	201	SA1	
	203	VTT1	
	205	G1	

	2	VSS1	
	4	DQ4	DDR_B_D4
	6	DQ5	DDR_B_D5
	8	VSS3	
	10	DQS#0	DDR_B_DQS#0
	12	DQS0	DDR_B_DQS0
	14	VSS6	
	16	DQ6	DDR_B_D6
	18	DQ7	DDR_B_D7
	20	VSS8	
	22	DQ12	DDR_B_D12
	24	DQ13	DDR_B_D13
	26	VSS10	
	28	DM1	DDR_B_DM1
SM_DRAMRST# 5,10	30	RESET#	
	32	VSS12	
	34	DQ14	DDR_B_D14
	36	DQ15	DDR_B_D15
	38	VSS14	
	40	DQ20	DDR_B_D20
	42	DQ21	DDR_B_D21
	44	VSS16	
	46	DM2	DDR_B_DM2
	48	VSS17	
	50	DQ22	DDR_B_D22
	52	DQ23	DDR_B_D23
	54	VSS19	
	56	DQ28	DDR_B_D28
	58	DQ29	DDR_B_D29
	60	VSS21	
	62	DQS#3	DDR_B_DQS#3
	64	DQS3	DDR_B_DQS3
	66	VSS24	
	68	DQ30	DDR_B_D30
	70	DQ31	DDR_B_D31
	72	VSS26	
DDRB_CKE1 7	74	CKE1	
	76	VDD2	
	78	A15	DDR_B_MA15
	80	A14	DDR_B_MA14
	82	VDD4	
	84	A11	DDR_B_MA11
	86	A7	DDR_B_MA7
	88	VDD6	
	90	A6	DDR_B_MA6
	92	A4	DDR_B_MA4
	94	VDD8	
	96	A2	DDR_B_MA2
	98	A0	DDR_B_MA0
	100	VDD10	
DDRB_CLK1 7	102	CK1	
DDRB_CLK1# 7	104	CK1#	
	106	VDD12	
DDR_B_BS1 7	108	BA1	
DDR_B_RAS# 7	110	RAS#	
	112	VDD14	
DDRB_SCS0# 7	114	S0#	
DDRB_ODT0 7	116	ODT0	
	118	VDD16	
DDRB_ODT1 7	120	ODT1	
	122	NC2	
	124	VDD18	
+DDR_VREF_CA_DIMMB	126	VREF_CA	
	128	VSS28	
DDR_B_D36	130	DQ36	
DDR_B_D37	132	DQ37	
	134	VSS30	
DDR_B_DM4	136	DM4	
	138	VSS31	
DDR_B_D38	140	DQ38	
DDR_B_D39	142	DQ39	
	144	VSS33	
DDR_B_D44	146	DQ44	
DDR_B_D45	148	DQ45	
	150	VSS35	
DDR_B_DQS#5	152	DQS#5	
DDR_B_DQS5	154	DQS5	
	156	VSS38	
DDR_B_D46	158	DQ46	
DDR_B_D47	160	DQ47	
	162	VSS40	
DDR_B_D52	164	DQ52	
DDR_B_D53	166	DQ53	
	168	VSS42	
DDR_B_DM6	170	DM6	
	172	VSS43	
DDR_B_D54	174	DQ54	
DDR_B_D55	176	DQ55	
	178	VSS45	
DDR_B_D60	180	DQ60	
DDR_B_D61	182	DQ61	
	184	VSS47	
DDR_B_DQS#7	186	DQS#7	
DDR_B_DQS7	188	DQS7	
	190	VSS50	
DDR_B_D62	192	DQ62	
DDR_B_D63	194	DQ63	
	196	VSS52	
PM_EXTTS# 5,10	198	EVENT#	
PM_SMBDATA 10,12,16,26	200	SDA	
PM_SMBCLK 10,12,16,26	202	SCL	
+0.75VS	204	VTT2	
	206	G2	

@ FOX_AS0A626-U4RN-7F

+1.5V
+1.5V
+3VS
+0.75VS
+0.75VS
+V_DDR3_DIMM_REF

C196 2.2U_0603_6.3V4Z
C197 0.1U_0402_16V4Z
close to JDDRH.1
C198 2.2U_0603_6.3V4Z
C199 0.1U_0402_16V4Z
close to JDDRH.126
R66 0_0402_5%
R67 10K_0402_5%
R68 10K_0402_5%
2.2U_0603_6.3V4Z
C216
C217
0.1U_0402_16V4Z

Layout Note:
Place near JDDRH

Layout Note: Place these 4 Caps near Command and Control signals of DIMMB

Layout Note:
Place near JDDRH.203 and 204

+1.5V
C200 @ 330U_B2_2.5VM_R15M
C203 10U_0805_6.3V6M
C205 10U_0805_6.3V6M
C208 10U_0805_6.3V6M
C211 10U_0805_6.3V6M
C213 10U_0805_6.3V6M
C215 10U_0805_6.3V6M

+1.5V
C201 0.1U_0402_16V4Z
C204 0.1U_0402_16V4Z
C207 0.1U_0402_16V4Z
C210 0.1U_0402_16V4Z

+0.75VS
C202 10U_0805_6.3V6M
C206 1U_0402_6.3V4Z
C209 1U_0402_6.3V4Z
C212 1U_0402_6.3V4Z
C214 1U_0402_6.3V4Z

Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **DDRIII-SODIMM1**

Size	Document Number	Rev
Custom	NDU00_LA-6031P M/B	1.0

Date: Monday, April 12, 2010 Sheet 11 of 45

Clock Generator

Clock gen	R72	R70 R73
RTM	no-mount	mount
IDT		

CPU_SEL	CPU_0/0#	CPU_1/1#
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

Routing the trace at least 10mil

03/23 cap reserval.

04/12 Q25B replace Q5B.

Silego Have Internal Pull-Up

IDT Have Internal Pull-Down

LCD/PANEL BD. Conn.

Reserve for EMI request

Change to PCH control.

01/30 EMI request

03/04 Pin24 +LCD_INV-->NC

Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: Clock Generator (CK505)/ LVDS CONN

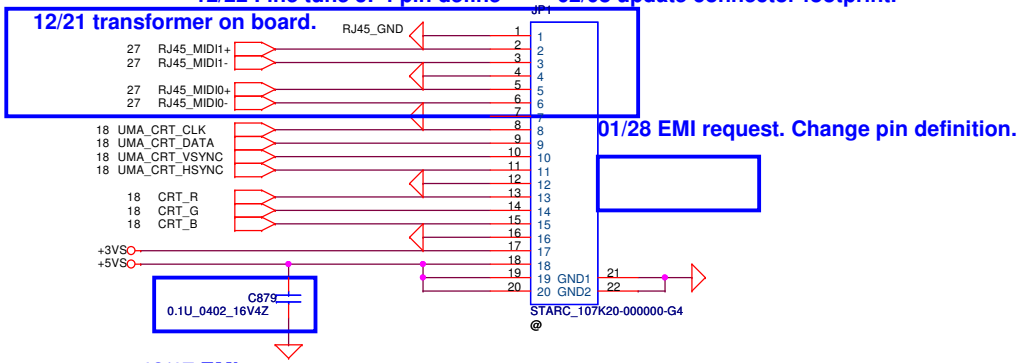
Size: Custom | Document Number: NDU00_LA-6031P M/B | Rev: 1.0

Date: Monday, April 12, 2010 | Sheet 12 of 45

CRT CONNECTOR

12/14 Fine tune pin define JP1 Pin1 Pin2 Pin8-->GND
12/21 pin 2,3 to RJ45_GND
12/22 Fine tune JP4 pin define
02/08 update connector footprint.

12/21 transformer on board.



01/28 EMI request. Change pin definition.

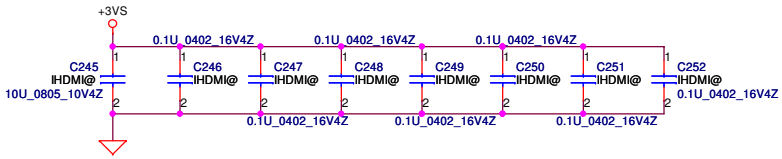
12/17 EMI request.

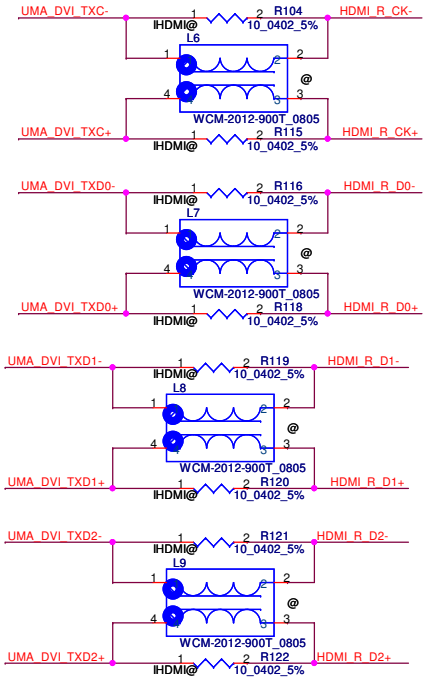
Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

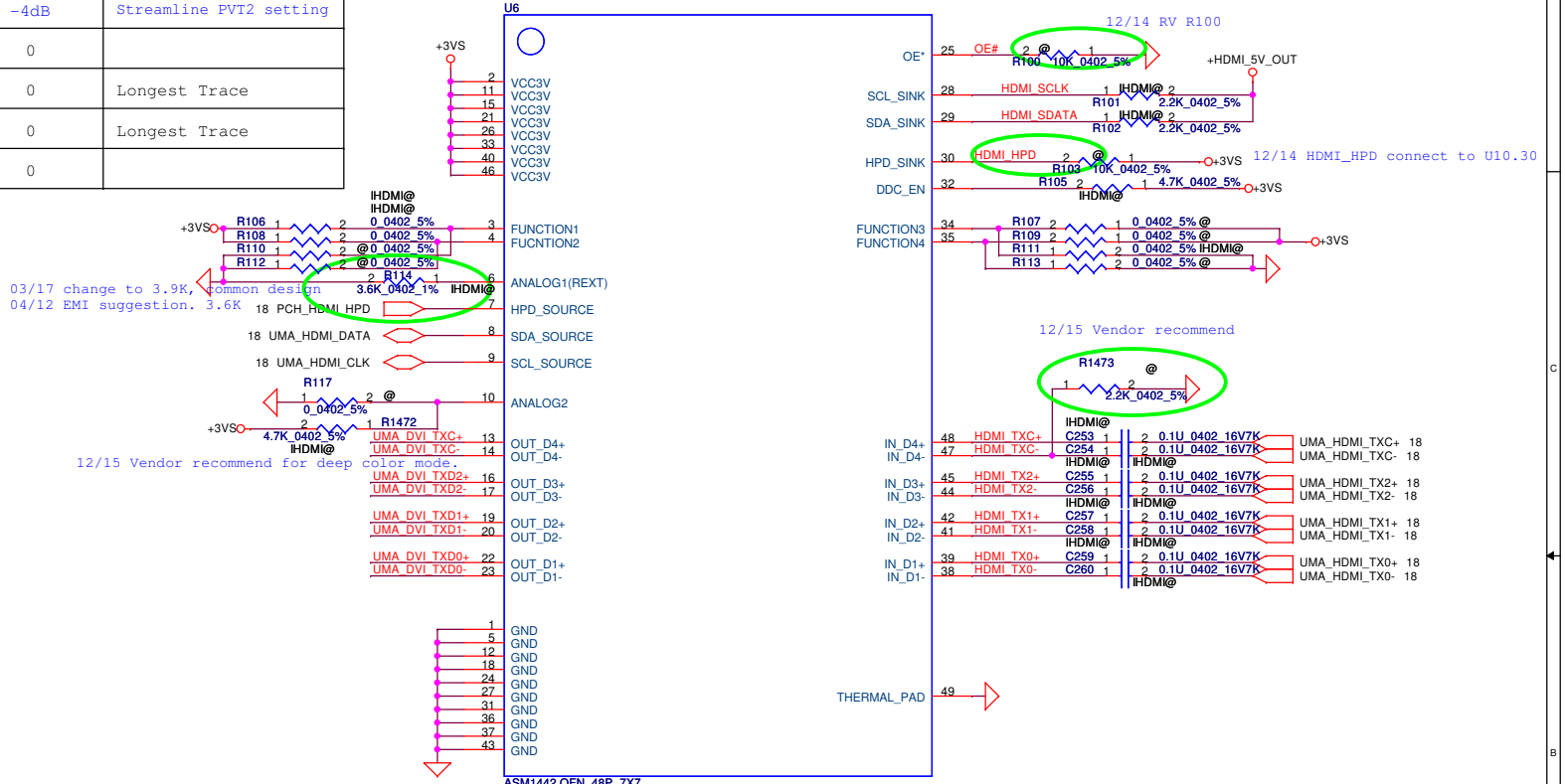
Compal Electronics, Inc.

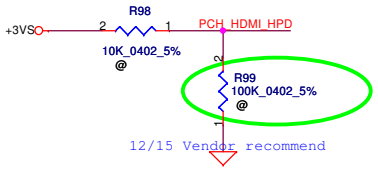
Title	CRT\TV\LVDS	
Size	Document Number: NDU00_LA-6031P M/B	Rev: 1.0
Date: Monday, April 12, 2010	Sheet 13 of 45	

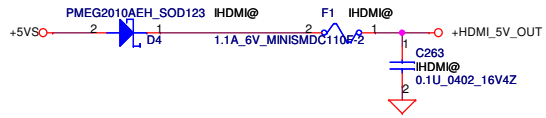
ANALOG2	Function2	Function1	Swing	Pre-Amp	Slew-rate	Note
Low	Low	Low	450	0	0	
Low	Low	High	420	0	-3dB	Shortest trace
Low	High	Low	450	0	-3dB	Shortest trace
Low	High	High	460	0	-4dB	Streamline PVT2 setting
High	Low	Low	340	0	0	
High	Low	High	400	2dB	0	Longest Trace
High	High	Low	400	2dB	0	Longest Trace
High	High	High	420	0	0	

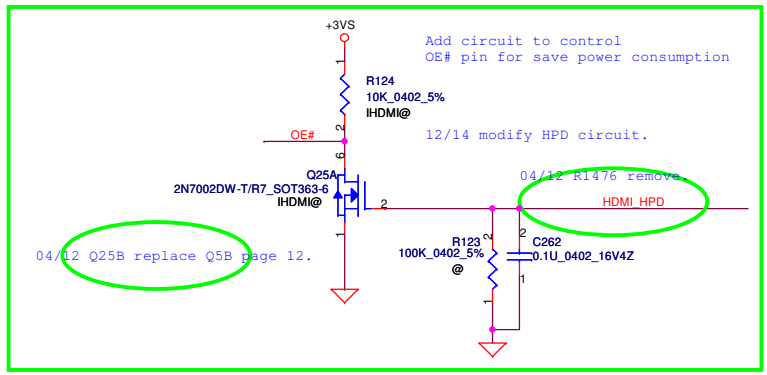






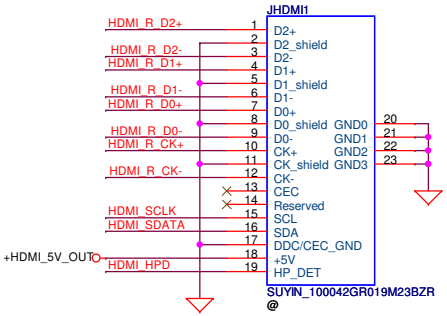






HDMI Connector

<01/27 update HDMI Connector >



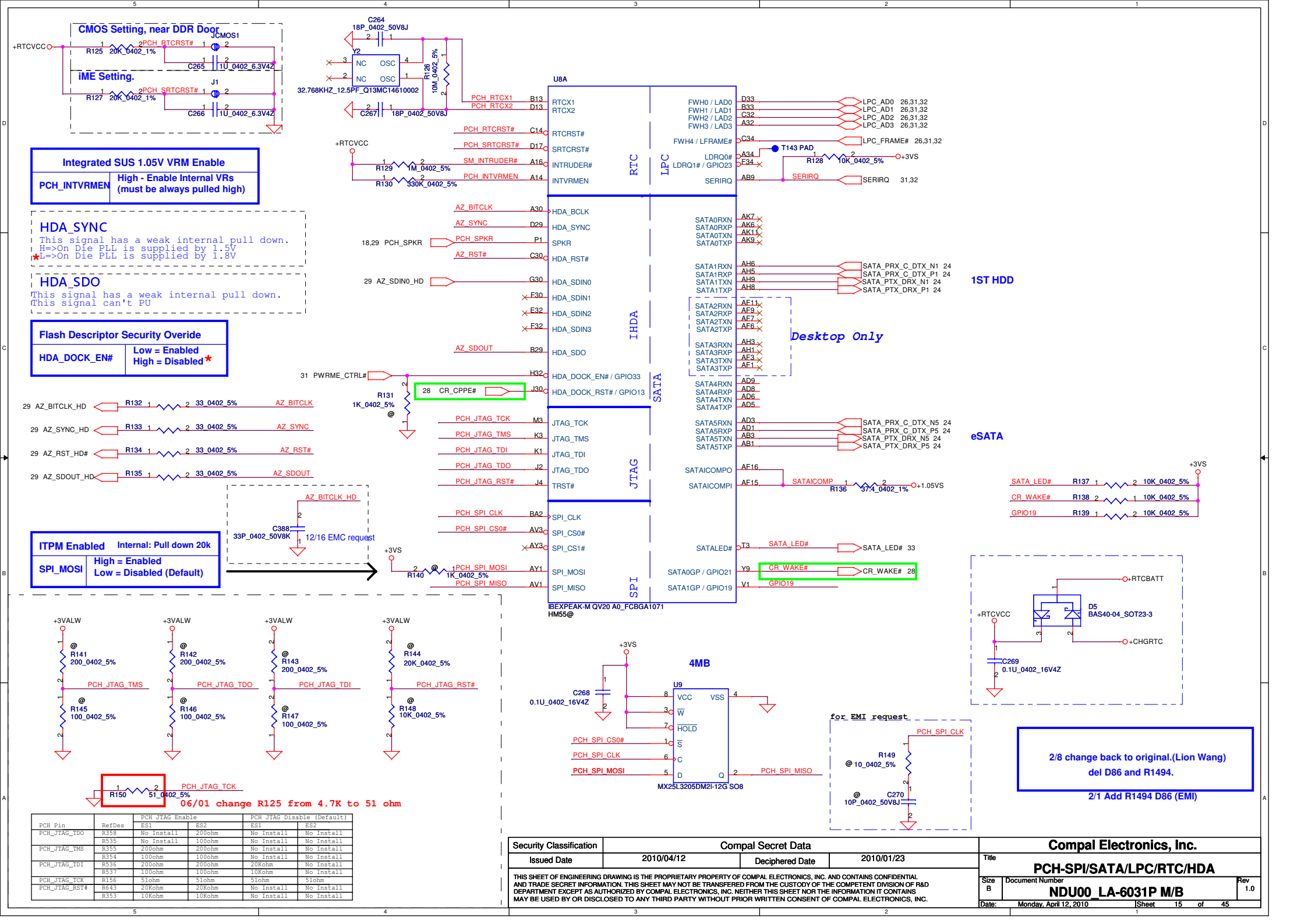
Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: HDMI Connector

Size	Document Number	Rev
	NDU00_LA-6031P M/B	1.0

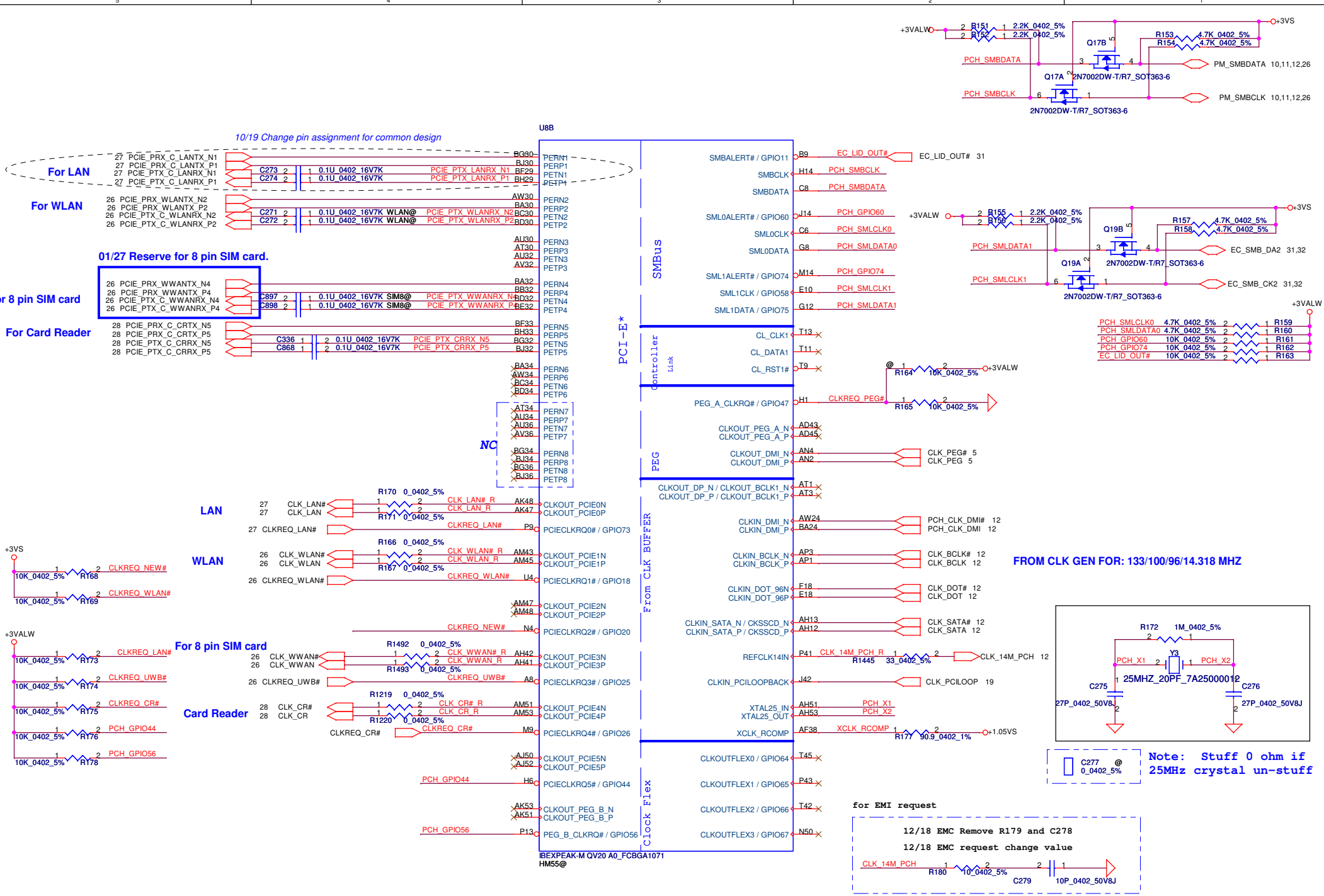
Date: Monday, April 12, 2010 Sheet 14 of 45



PCH Pin	RefDes	PCH JTAG Enable ES1	PCH JTAG Enable ES2	PCH JTAG Disable (Default) ES1	PCH JTAG Disable (Default) ES2
PCH_JTAG_TDO	R358	No Install	200ohm	No Install	No Install
	R535	No Install	100ohm	No Install	No Install
PCH_JTAG_TMS	R355	200ohm	200ohm	No Install	No Install
	R354	100ohm	100ohm	No Install	No Install
PCH_JTAG_TDI	R536	200ohm	200ohm	20Kohm	No Install
	R537	100ohm	100ohm	10Kohm	No Install
PCH_JTAG_TCK	R156	51ohm	51ohm	51ohm	51ohm
PCH_JTAG_RST#	R643	20Kohm	20Kohm	No Install	No Install
	R353	10Kohm	10Kohm	No Install	No Install

Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

Compal Electronics, Inc.	
Title	PCH-SPI/SATA/LPC/RTC/HDA
Size B	Document Number NDU00_LA-6031P M/B
Rev	1.0
Date: Monday, April 12, 2010	Sheet 15 of 45



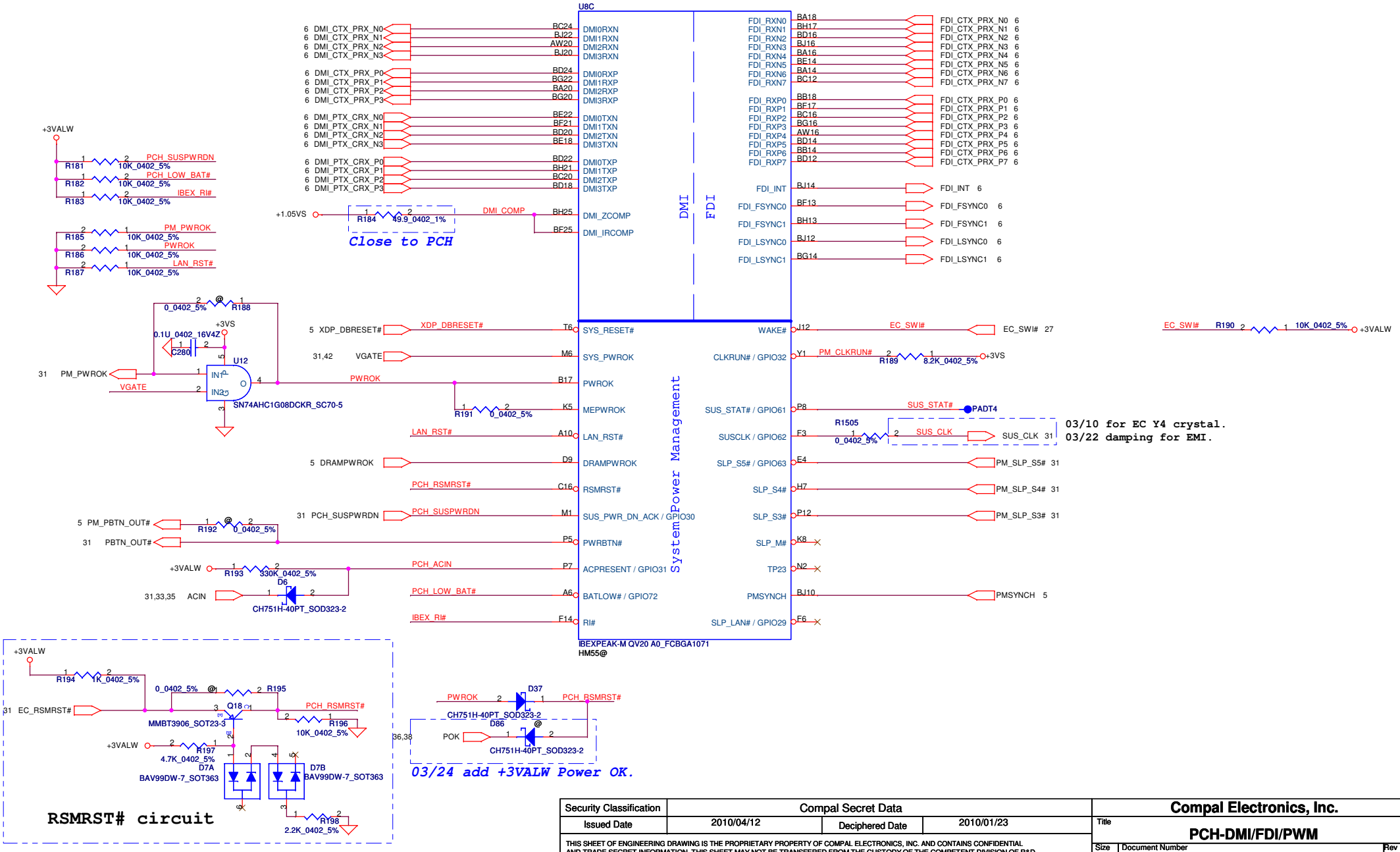
Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **CLK/PCIE/SMBUS**

Size	Document Number	Rev
B	NDU00_LA-6031P M/B	1.0

Date: Monday, April 12, 2010 Sheet 16 of 45



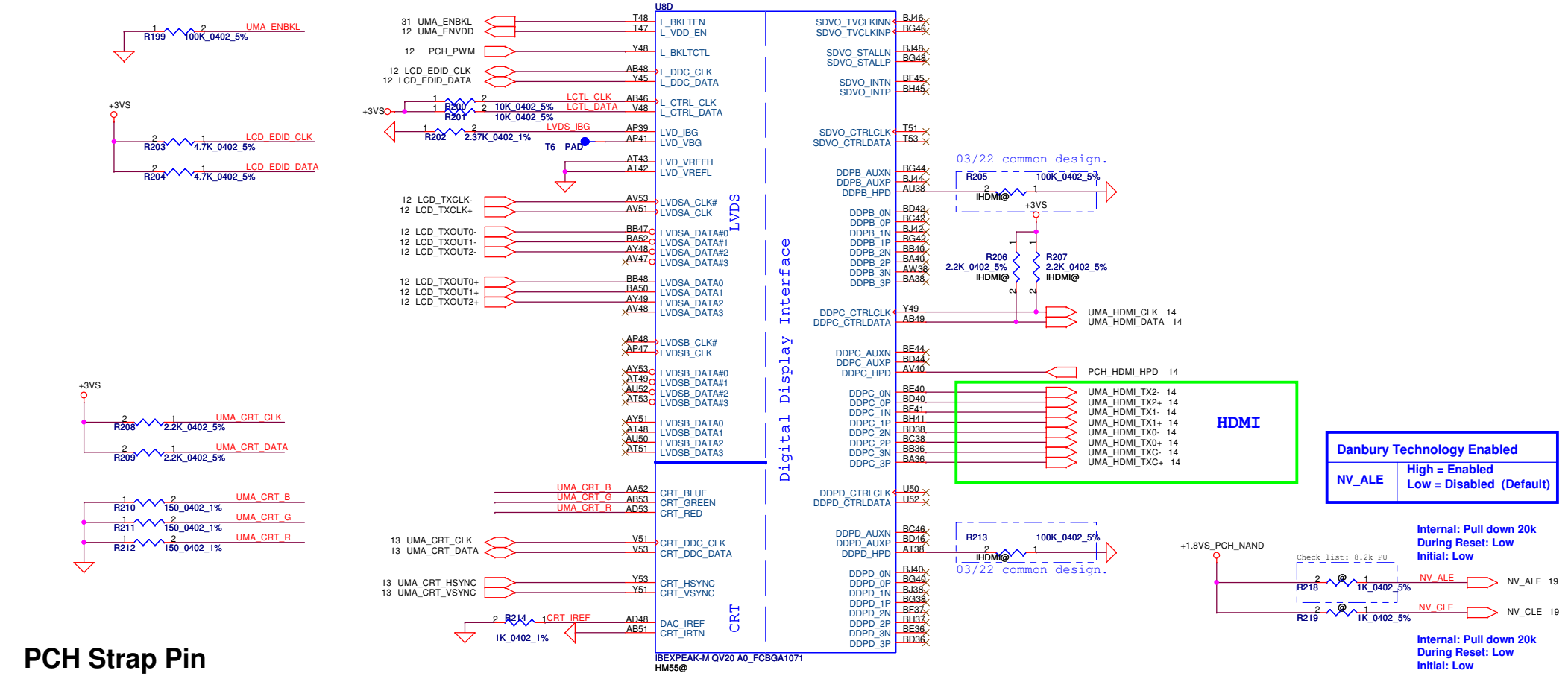
Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **PCH-DMI/FDI/PWM**

Size	Document Number	Rev
B	NDU00_LA-6031P M/B	1.0

Date: Monday, April 12, 2010 Sheet 17 of 45



PCH Strap Pin

Internal: Pull down 20k
During Reset: HZ
Initial: Low

Internal: Pull up 20k
During Reset: High
Initial: High

Internal: Pull up 20k
During Reset: High
Initial: High

Internal: Pull up 20k
During Reset: High
Initial: High

NO REBOOT Strap	
PCH_SPKR	Low= Disable High= Enable

Boot BIOS Strap		
PCI_GNT#1	PCI_GNT#0	Boot BIOS Loaction
0	0	LPC (Default)
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= A16 swap override Disable

Danbury Technology Enabled	
NV_ALE	High = Enabled Low = Disabled (Default)

Internal: Pull down 20k
During Reset: Low
Initial: Low

Internal: Pull down 20k
During Reset: Low
Initial: Low

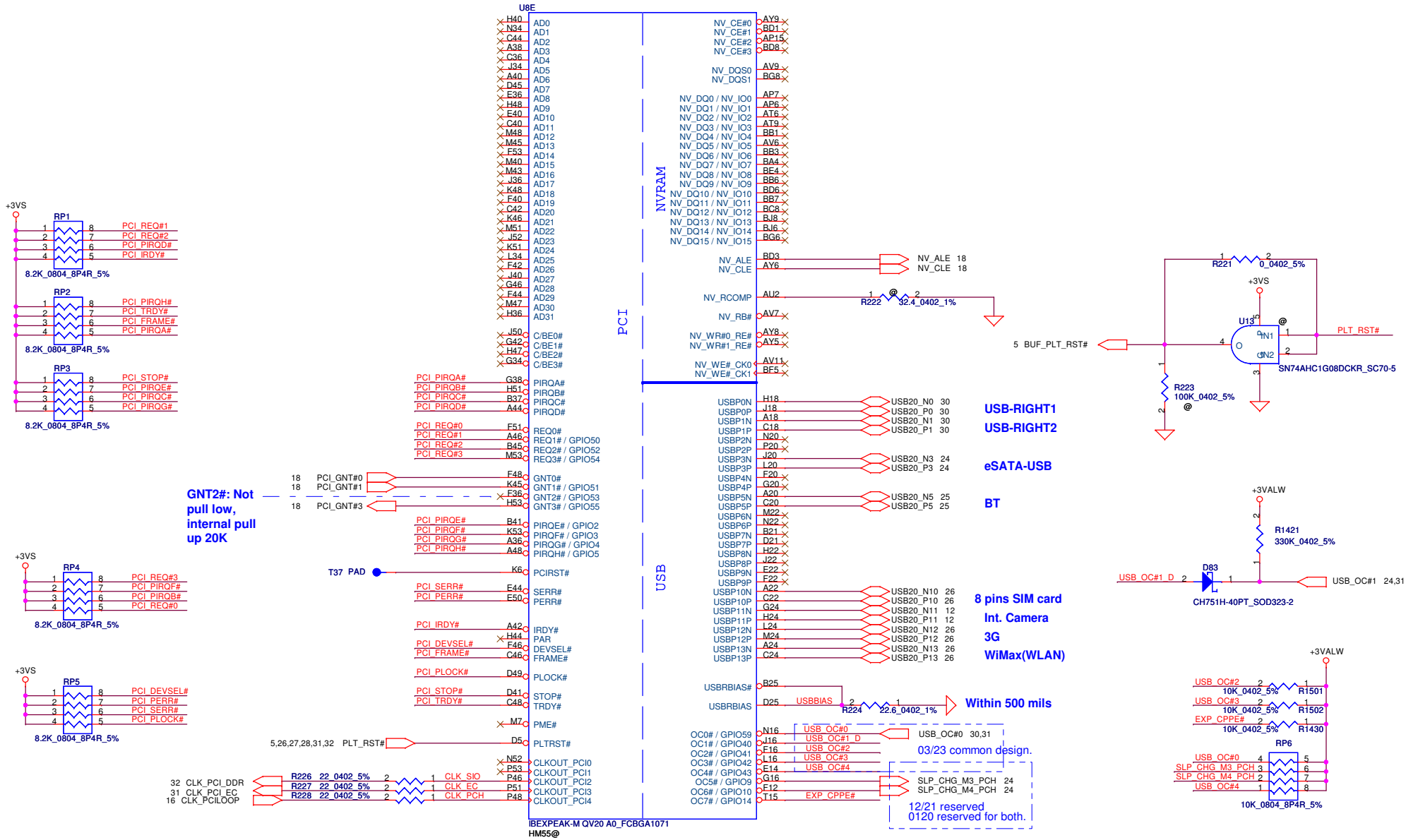
DMI Termination Voltage	
NV_CLE	Low= Set to Vss (Default) High= Set to Vcc

modify.....

2/2 Add L41 L42 L43 C900 C901 C902 for EMI request

Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

Compal Electronics, Inc.			
Title	PCH-CRT/LVDS/HDMI		
Size: Custom	Document Number: NDU00_LA-6031P M/B		Rev: 1.0
Date: Monday, April 12, 2010	Sheet 18 of 45		



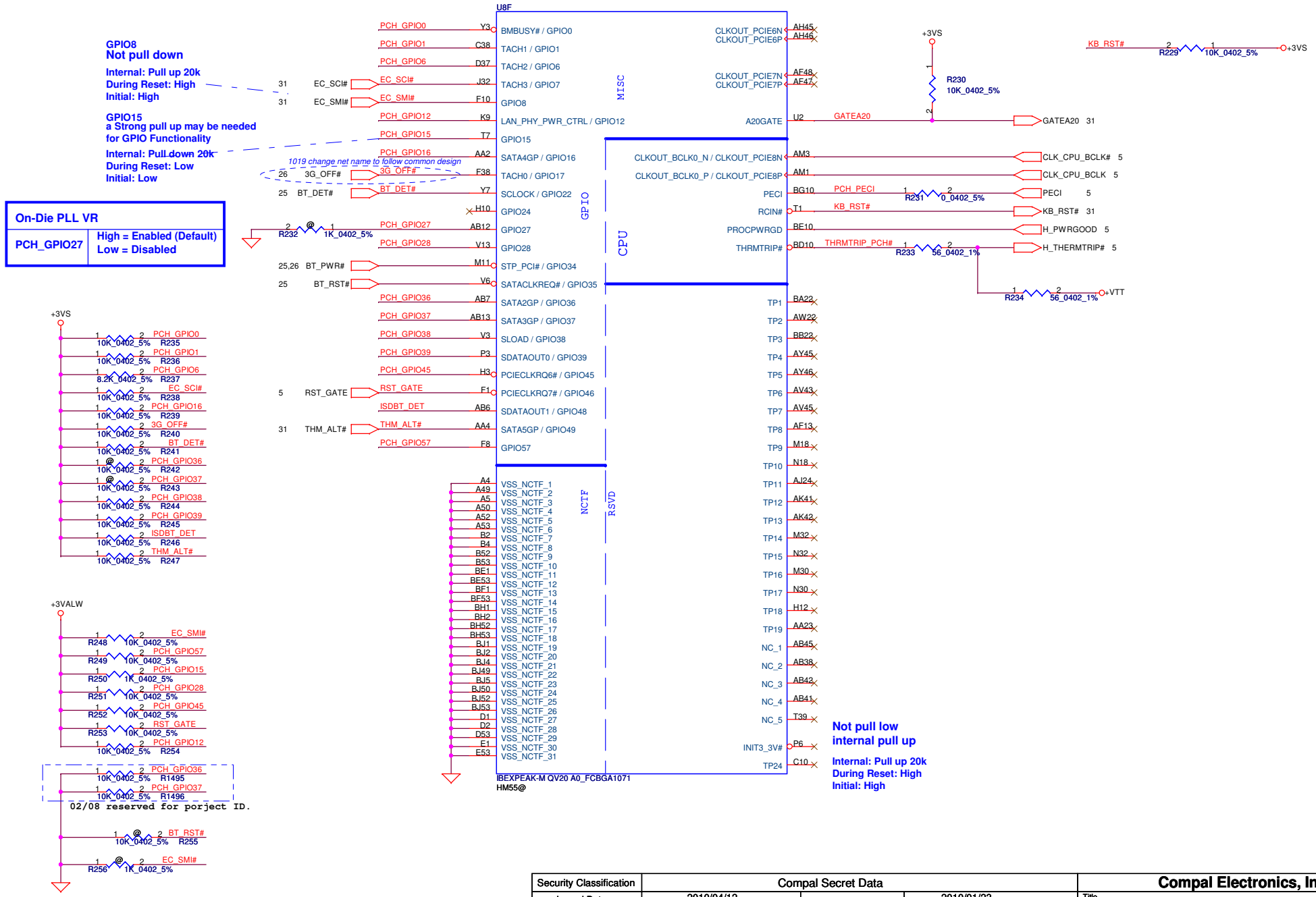
Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **PCH USB/PCI/NAND**

Size	Document Number	Rev
B	NDU00_LA-6031P M/B	1.0

Date: Monday, April 12, 2010 Sheet 19 of 45



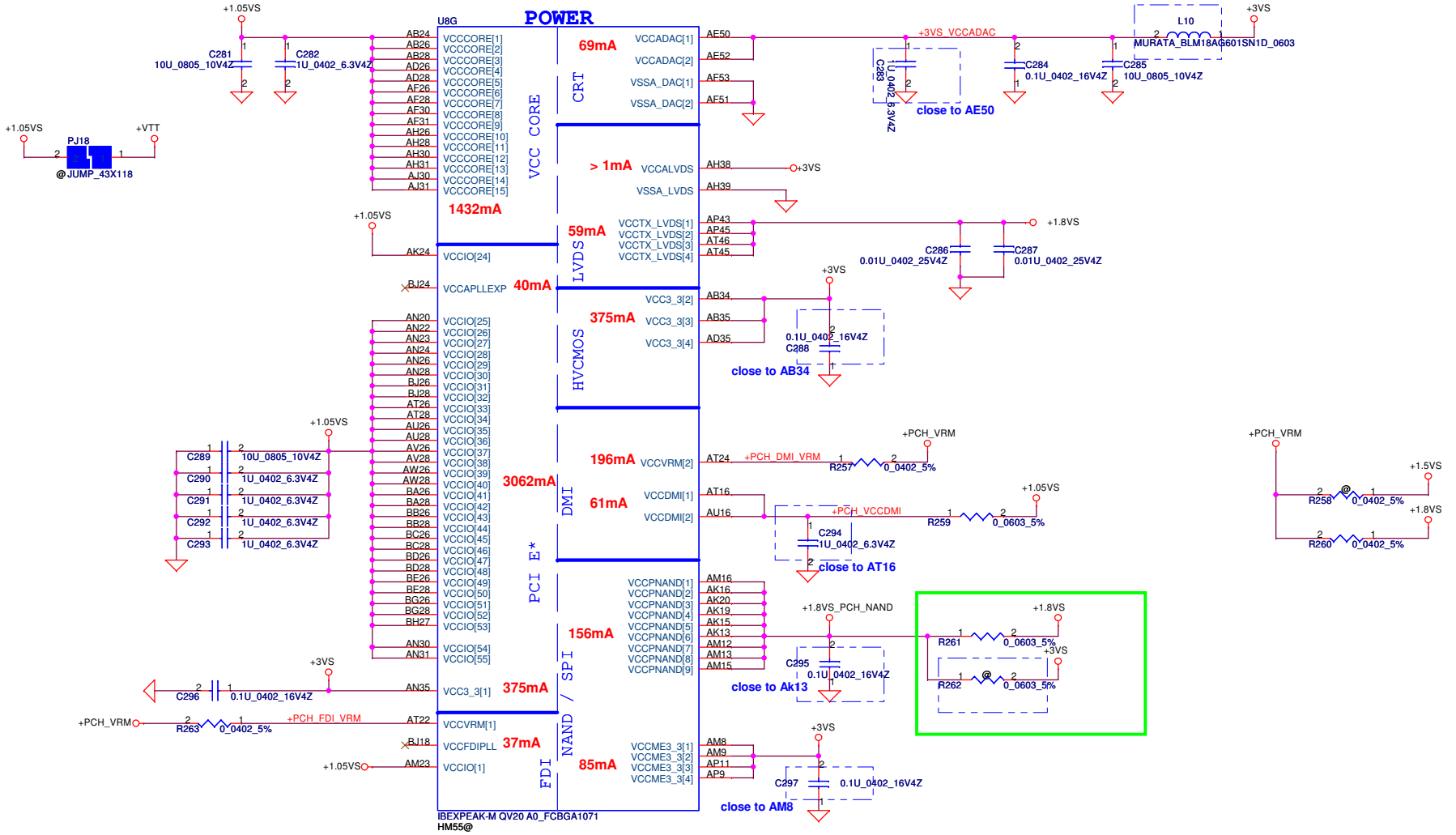
Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **PCH CPU/GPIO**

Size	Document Number	Rev
B	NDU00_LA-6031P M/B	1.0

Date: Monday, April 12, 2010 Sheet 20 of 45



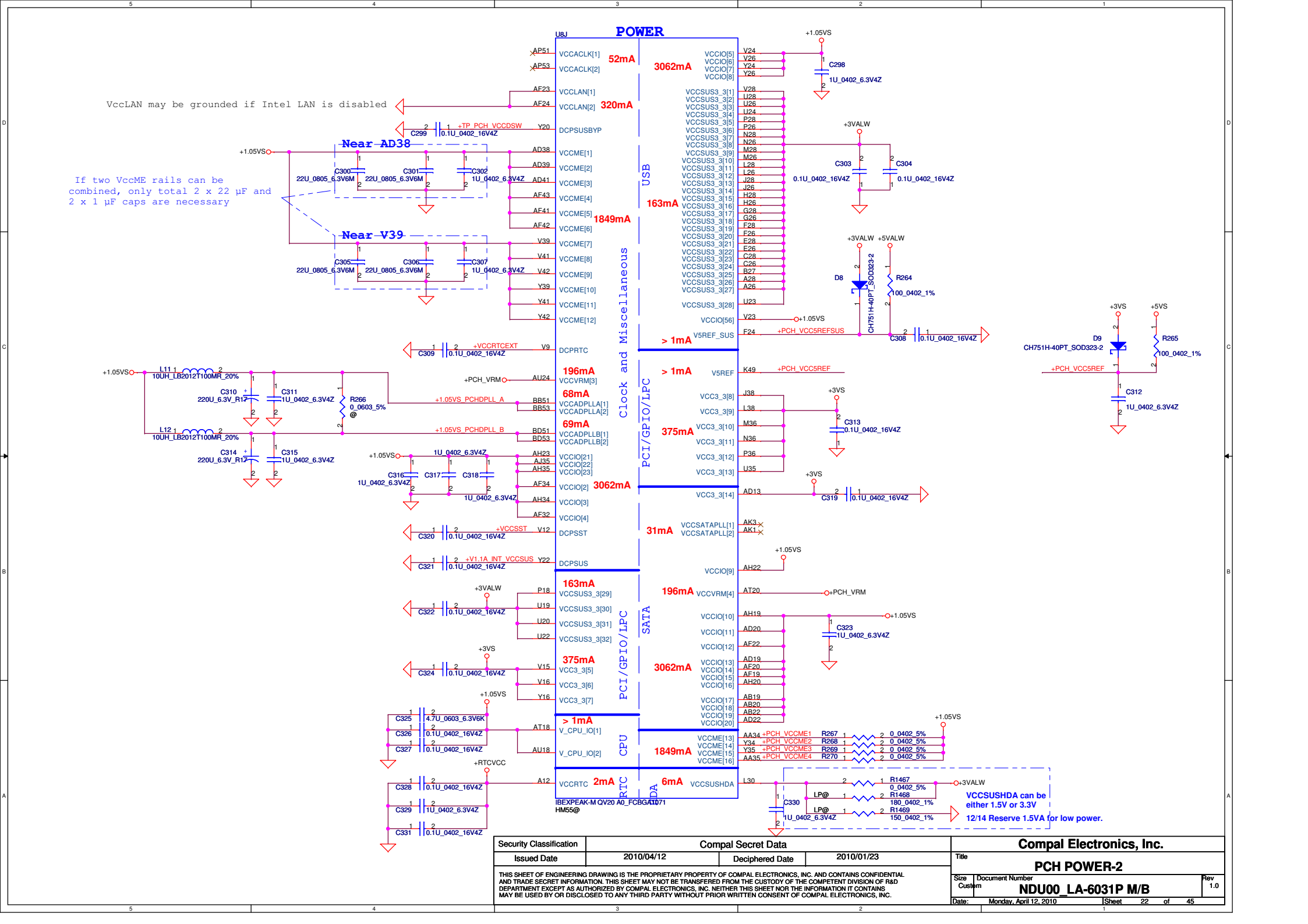
Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **PCH POWER-1**

Size	Document Number	Rev
B	NDU00_LA-6031P M/B	1.0

Date: Monday, April 12, 2010 Sheet 21 of 45



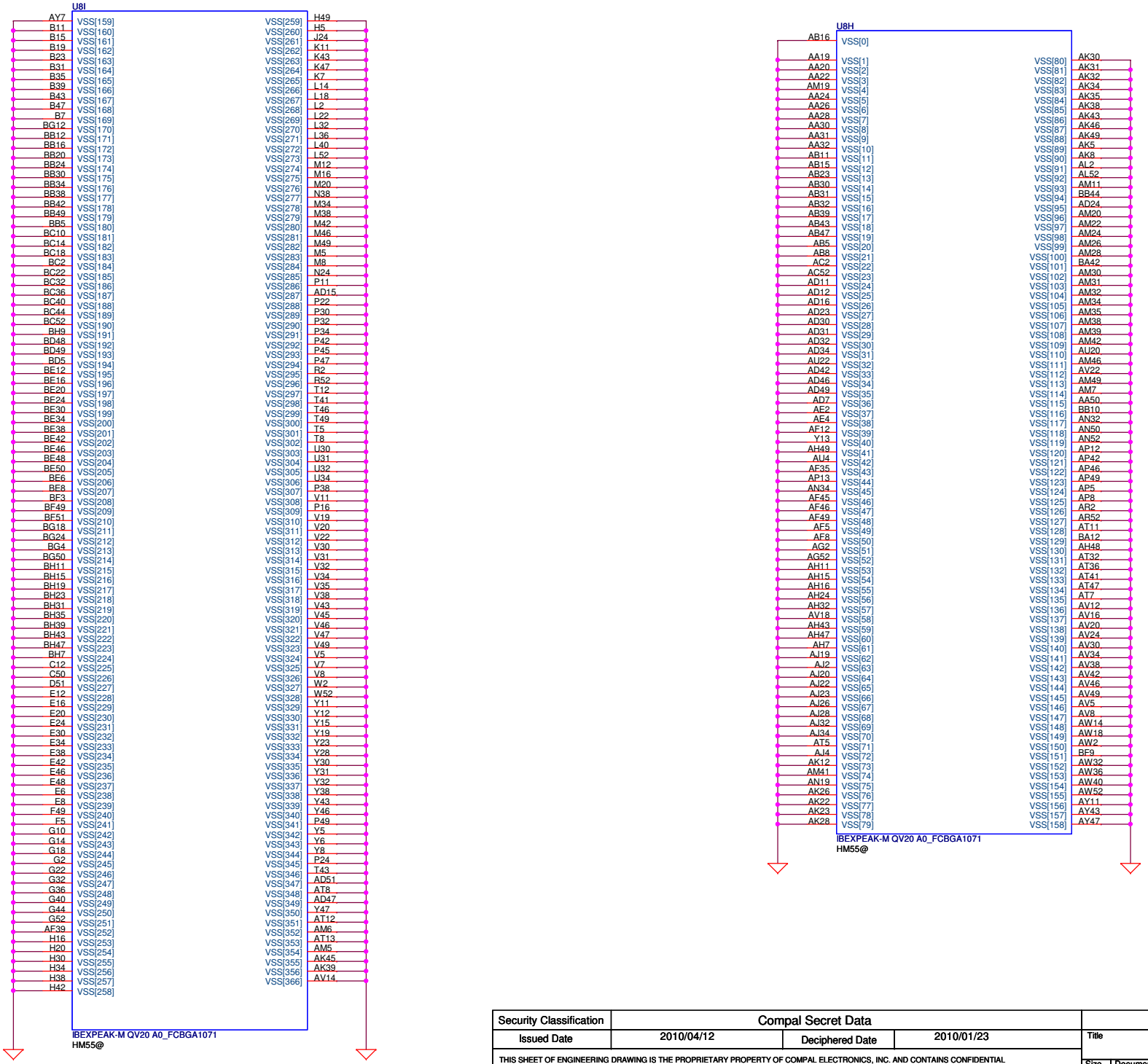
Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **PCH POWER-2**

Size	Document Number	Rev
Custom	NDU00_LA-6031P M/B	1.0

Date: Monday, April 12, 2010 | Sheet 22 of 45



Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

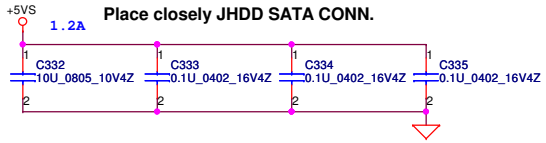
Compal Electronics, Inc.

Title: **PCH-GND**

Size	Document Number	Rev
Custom	NDU00_LA-6031P M/B	1.0

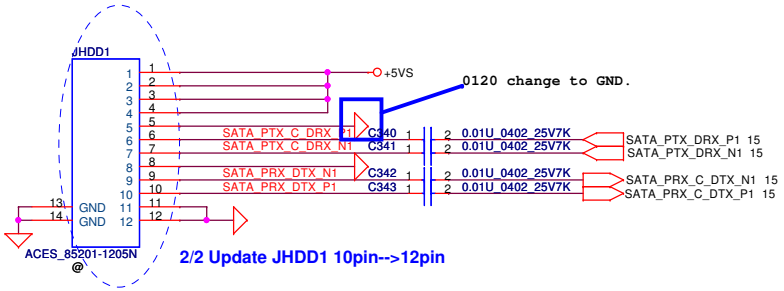
Date: Monday, April 12, 2010 | Sheet 23 of 45

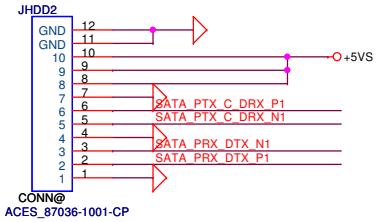
SATA HDD Conn.



1/28 Add JHDD2

JHDD2 Layout symbol reverse JHDD1, recerse the pin define



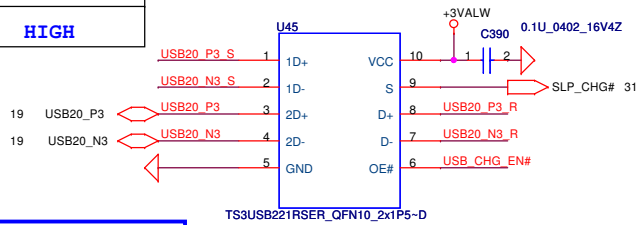


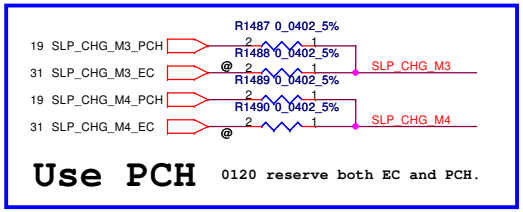
Add wire connector for H/W SATA verify

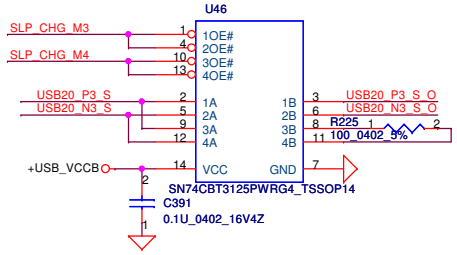
eSATA/USB Combo

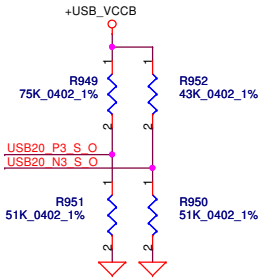
	SLP_CHG_M3	SLP_CHG_M4
Mode 3	HIGH	LOW
Mode 4	LOW	HIGH

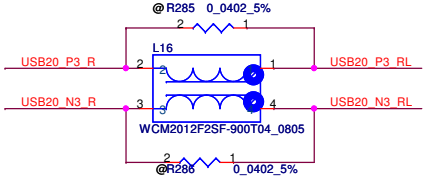
SLP_CHG	FUNCTION
LOW	D=1D
HIGH	D=2D

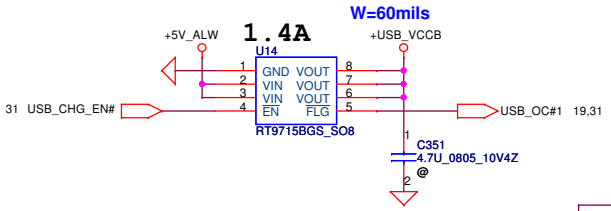


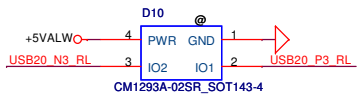


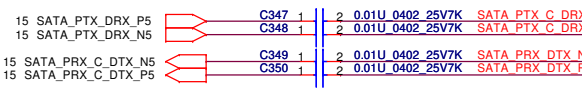


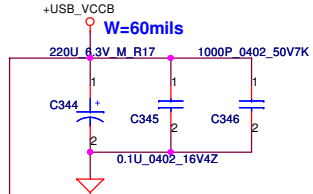






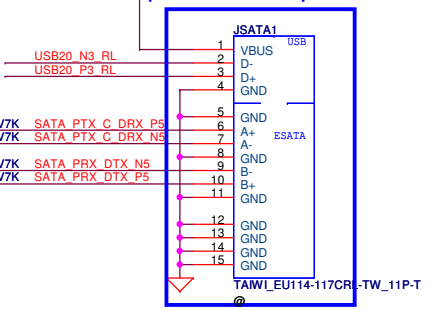






eSATA/USB Conn

1/26 update JSATA1 footprint



Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: SATA-HDD/ODD/USB

Size | Document Number: NDU00_LA-6031P M/B | Rev: 1.0

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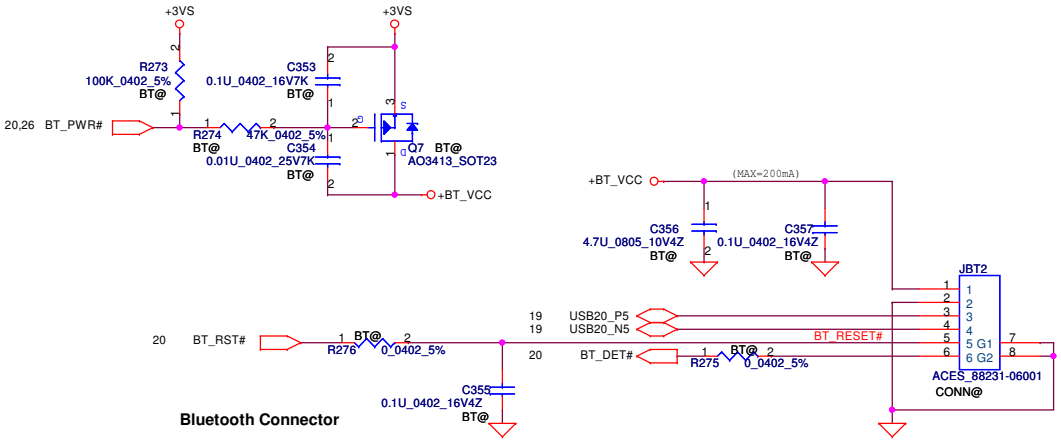
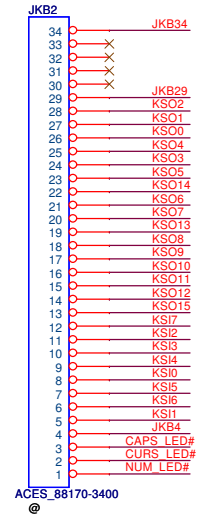
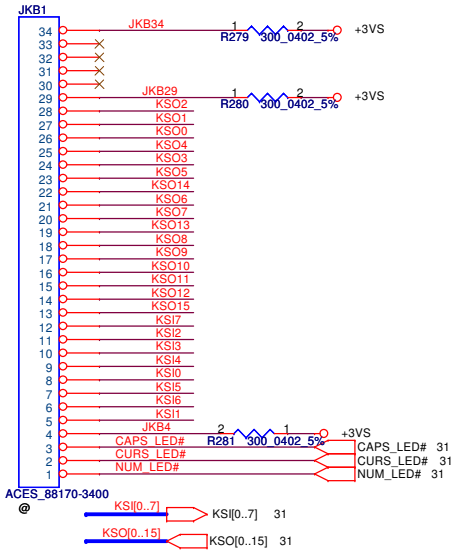
BlueTooth Interface

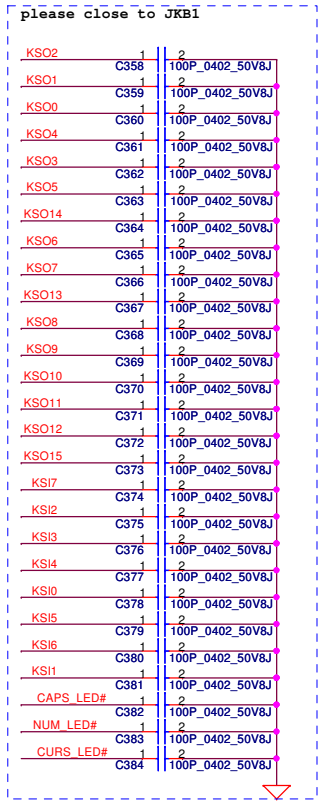


KEYBOARD CONN. for 11.6"



KEYBOARD CONN. for 13.3"





Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

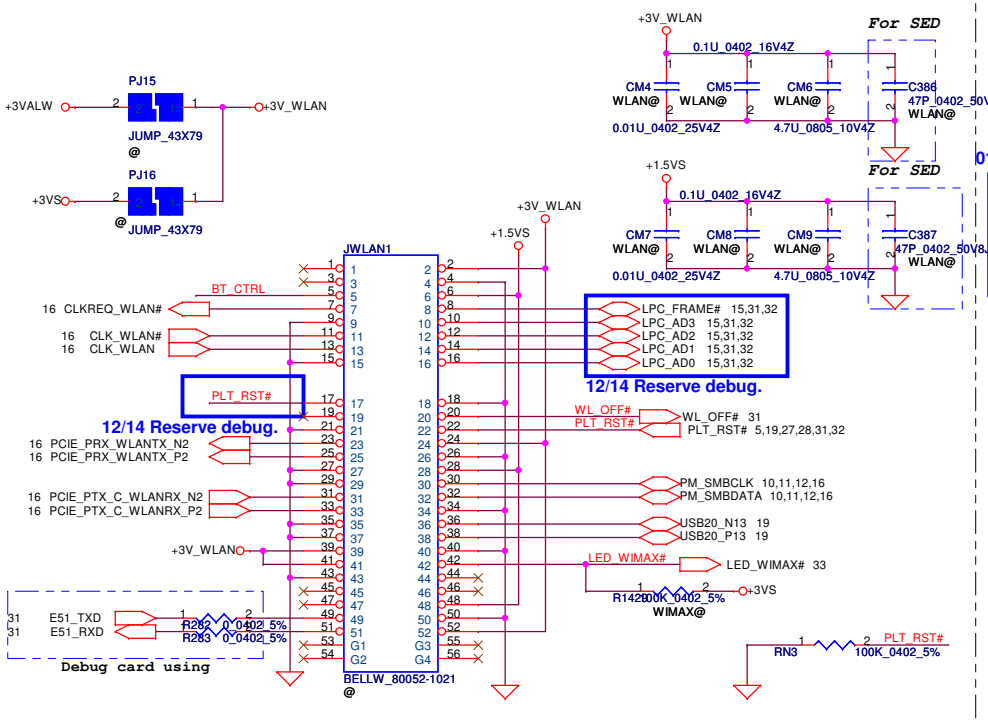
Compal Electronics, Inc.

Title: USB/BT/FP/Int. Cam

Size | Document Number: NDU00_LA-6031P M/B | Rev: 1.0

Date: Monday, April 12, 2010 | Sheet 25 of 45

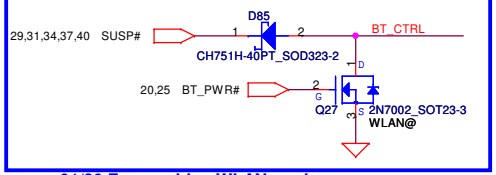
PCIe Mini Card-WLAN/WiMax



WLAN&BT Combo module circuits

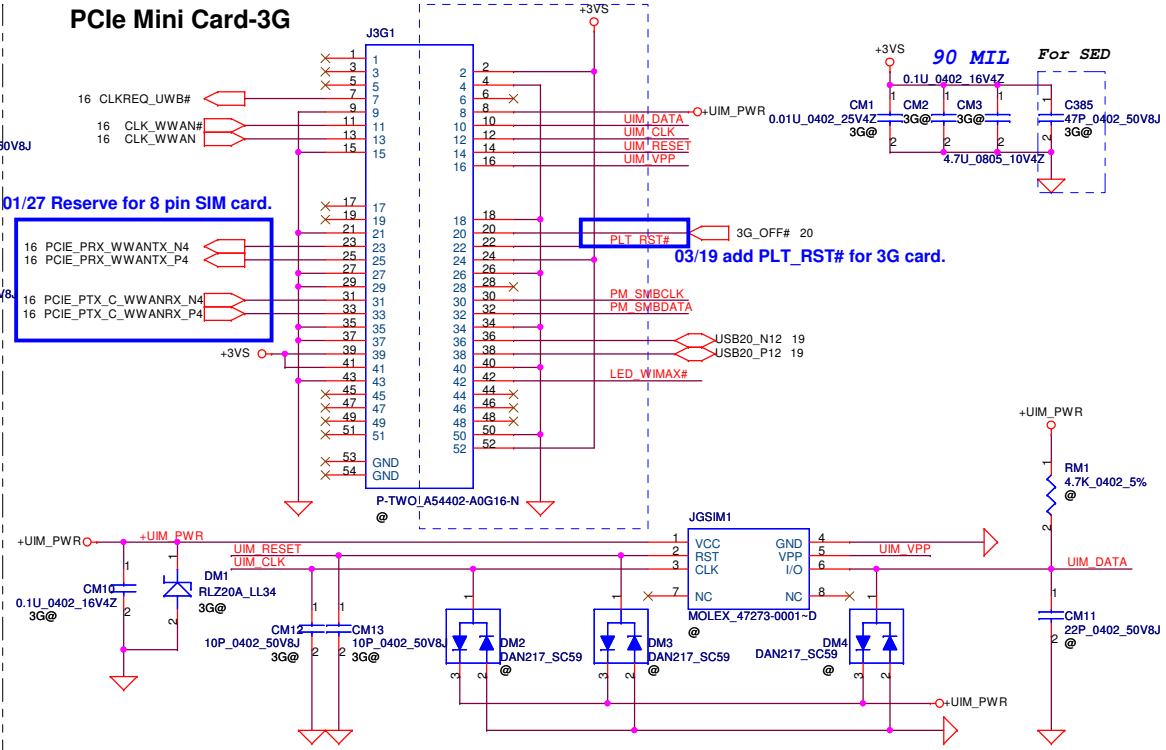
	BT on module Enable	BT on module Disable
BT_CRTL	HI	LO
BT_PWR#	LO	HI

**If +3V_WLAN is +3VS, please remove D21.



01/20 For combine WLAN card.

PCIe Mini Card-3G



01/26 Co-lay with JGSIM1.

Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: PCIe-WLAN/HDDVD/NAND/NEW

Size	Document Number	Rev
	NDU00_LA-6031P M/B	1.0

Date: Monday, April 12, 2010 Sheet 26 of 45

12/14 Fine tune pin define UL1 Pin37 Pin40 -->Dummy

UL1

16 PCIE_PRX_C_LANTX_P1 — CL1 0.1U_0402_16V7K — PCIE_PRX_LANTX_P1 — 22 HSOP
16 PCIE_PRX_C_LANTX_N1 — CL2 0.1U_0402_16V7K — PCIE_PRX_LANTX_N1 — 23 HSON
16 PCIE_PTX_C_LANRX_P1 — 17 HSIP
16 PCIE_PTX_C_LANRX_N1 — 18 HSIN
16 CLKREQ_LAN# — RL19 0_0402_5% — 16 CLKREQB
5,19,26,28,31,32 PLT_RST# — 25 PERSTB
16 CLK_LAN — 19 REFCLK_P
16 CLK_LAN# — 20 REFCLK_N
LAN_X1 — 43 CKXTAL1
LAN_X2 — 44 CKXTAL2
17 EC_SWI# — LAN_WAKE# — 28 LANWAKEB
ISOLATEB — 26 ISOLATEB
+3V_LAN — @ RL20 1K_0402_5% — 14 NC/SMBCLK
@ RL21 1K_0402_5% — 15 NC/SMBDATA
RL22 1K_0402_5% — 38 GPO/SMBALERT
ENSWREG — 33 ENSWREG
+LAN_VDDREG — 34 VDDREG
35 VDDREG
RL5 2.49K_0402_1% — 46 RSET
24 GND
49 PGND

LED3/EEDO — 31
LED1/EESK — 37
LED0 — 40
EECS/SCL — 30 — RL2 10K_0402_5%
EEDI/SDA — 32 — RL1 10K_0402_5%
MDIP0 — 1 — LAN_MDI0+
MDIN0 — 2 — LAN_MDI0-
MDIP1 — 4 — LAN_MDI1+
MDIN1 — 5 — LAN_MDI1-
NC/MDIP2 — 7
NC/MDIN2 — 8
NC/MDIP3 — 10
NC/MDIN3 — 11
DVDD10 — 13 — +LAN_VDD10
DVDD10 — 29
DVDD10 — 41
DVDD33 — 27 — +3V_LAN
DVDD33 — 39
AVDD33 — 12
AVDD33 — 42 — +3V_AVDDXTAL — +3V_LAN
AVDD33 — 47
AVDD33 — 48
EVDD10 — 21 — +LAN_EVDD10
AVDD10 — 3 — +LAN_VDD10
AVDD10 — 6
AVDD10 — 9
AVDD10 — 45
REGOUT — 36 — +LAN_REGOUT

RTL8105E-VB-GR_QFN48_6X6
8111E@ Need to re-link database

12/18 vendor request

+3V_LAN — @ RL3 — EC_SWI# — 10K_0402_5%

+3VS — RL6 1K_0402_1% — ISOLATEB — RL7 15K_0402_5%

YL1 25MHZ_20PF_7A25000012
LAN_X1 — CL26 27P_0402_50V8J
LAN_X2 — CL27 27P_0402_50V8J

+3V_AVDDXTAL — RL8 0_0402_5% — +3V_LAN
RL9 @ 0_0402_5% — +LAN_VDD10
CL11@ 0.1U_0402_16V4Z
Reserved For 1.05V Crystal

+3V_LAN — RL4 0_0402_5% — ENSWREG — RL23 0_0402_5% @

Main: SHI0000AA00 2nd : SHI0000AB00

Can change to 2.2uH&4.7uF

+LAN_REGOUT — LL1 4.7UH_1008HC-472EJFS-A_5%_1008 — +LAN_VDD10
CL13 4.7U_0805_6.3V6M
CL9 0.1U_0402_16V4Z

Layout Note: LL1 must be within 200mil to Pin36
CL8,CL9 must be within 200mil to LL1
+LAN_REGOUT: Width =60mil

+LAN_VDD10 — 0_0603_5% LL2 — +LAN_EVDD10
CL18 1U_0402_6.3V4Z
CL17 0.1U_0402_16V4Z
Close to Pin 21

+3V_LAN — 0_0603_5% LL3 — +LAN_VDDREG
CL28 4.7U_0603_6.3V6K
CL29 0.1U_0402_16V4Z

Close to Pin 27,39,12,47,48
+3V_LAN
CL10 0.1U_0402_16V4Z
CL4 0.1U_0402_16V4Z
CL5 0.1U_0402_16V4Z
CL6 0.1U_0402_16V4Z
CL7 0.1U_0402_16V4Z

Close to Pin 3,6,9,13,29,41,45
+LAN_VDD10
CL19 0.1U_0402_16V4Z
CL20 0.1U_0402_16V4Z
CL21 0.1U_0402_16V4Z
CL22 0.1U_0402_16V4Z

+3VALW TO +3V_LAN

+3VALW — RL24 100K_0402_5% — WOL_EN# — RL16 47K_0402_5%
+3VALW — Vgs=-4.5V, Id=3A, Rds<97mohm
CL12 0.1U_0402_16V7K
QL1 AO3413_SOT23
CL14 0.01U_0402_25V7K
PJ17 JUMP_43X39 @ — +3V_LAN
CL15 4.7U_0805_10V4Z @
CL8 1U_0402_6.3V4Z

UL2 NS681680

CL30 0.01U_0402_16V7K — LAN_MDI1+ / LAN_MDI1- — TD+/TD-/CT/NC/NC/CT/RD+/RD- — TX+/TX-/CT/NC/NC/CT/RX+/RX-
RJ45_MIDI1+ — RJ45_MIDI1+ 13
RJ45_MIDI1- — RJ45_MIDI1- 13
CL31 1000P_0402_50V7K
CL32 1000P_0402_50V7K
RL25 75_0402_1%
RL26 75_0402_1%
LAN_MDI0+ / LAN_MDI0- — RJ45_MIDI0+ — RJ45_MIDI0+ 13
RJ45_MIDI0- — RJ45_MIDI0- 13
RJ45_GND — RJ45_GND

12/21 place transformer on board.

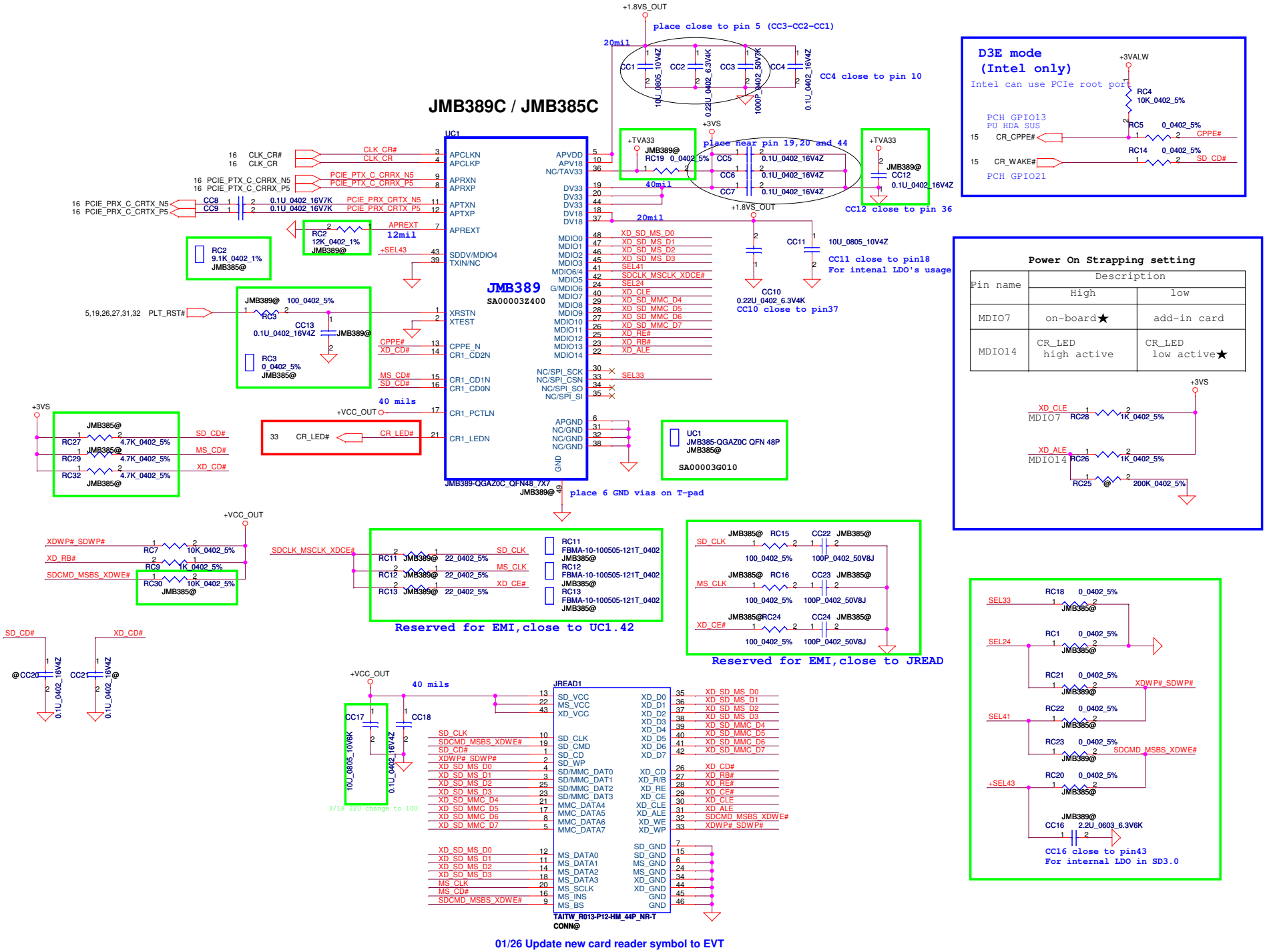
Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/02/02

Compal Electronics, Inc.

Title: RTL8105E/RTL8111E

Size | Document Number: NDU00_LA-6031P M/B | Rev: 1.0

Date: Monday, April 12, 2010 | Sheet 27 of 45



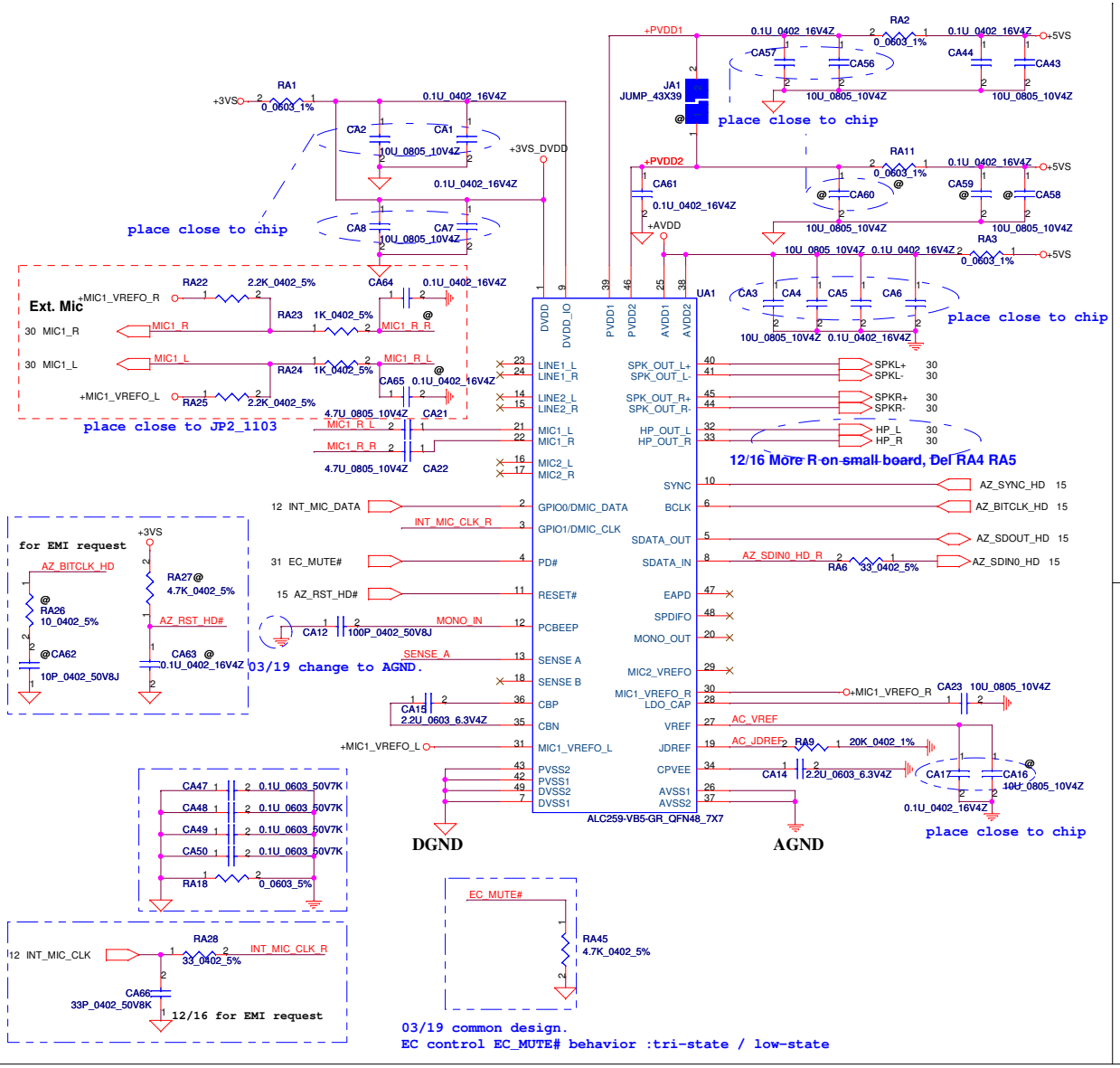
Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/10/08

Compal Electronics, Inc.

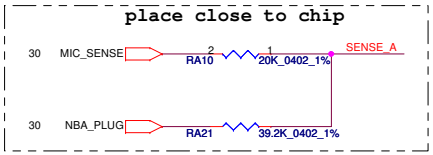
Title: **Card Reader-JMB389C/385C**

Size	Document Number	Rev
Custom	NBQAA LA6071P M/B	1.0

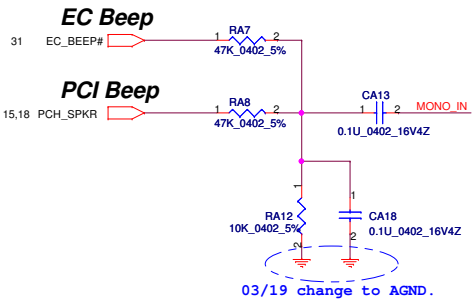
Date: Monday, April 12, 2010 Sheet 28 of 45

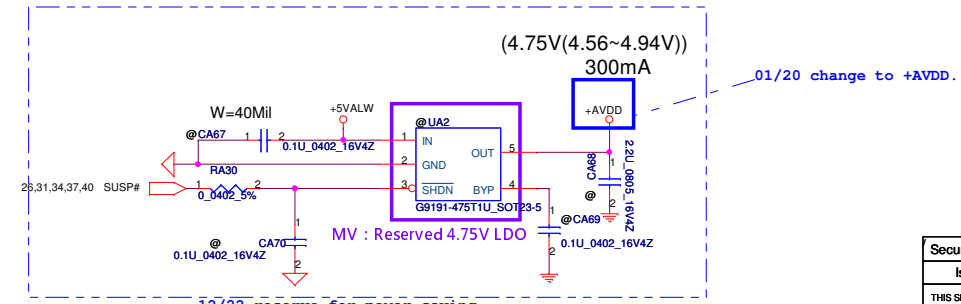


Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	



Beep sound



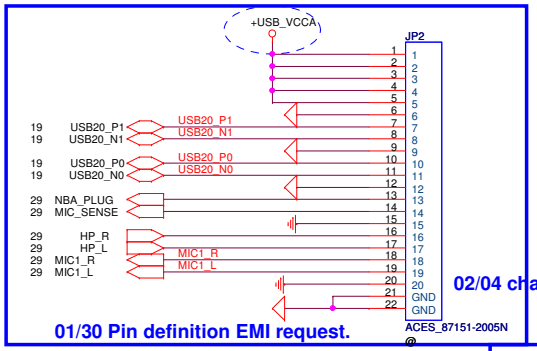


Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2009/04/14

Compal Electronics, Inc.			
Title	HD Audio ALC272 Codec		
Size: Custom	Document Number: NDU00_LA-6031P M/B		Rev: 1.0
Date: Monday, April 12, 2010	Sheet 29 of 45		

USB+Audio FFC conn
Pin=20pin, pitch=0.5

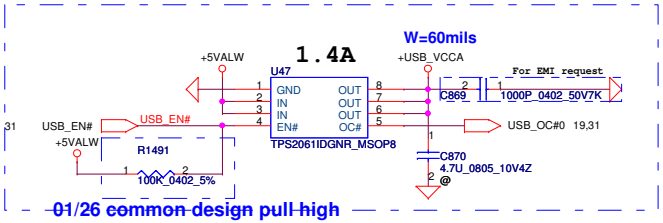
01/30 New JP2 Layout symbol reverse old conn, reserse the pin define



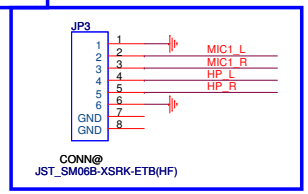
01/30 Pin definition EMI request.

02/04 change back to 20 pins.

W=60mils

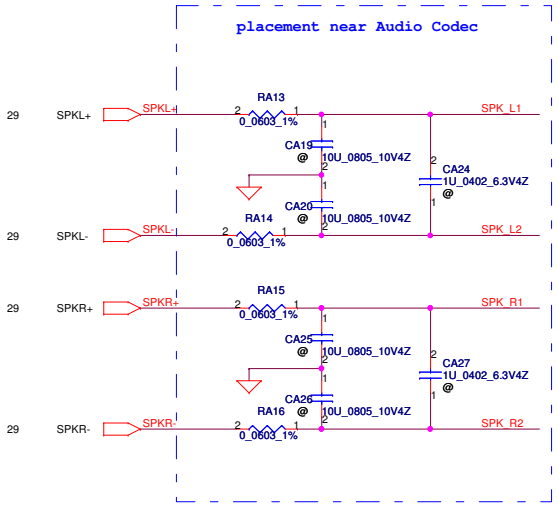


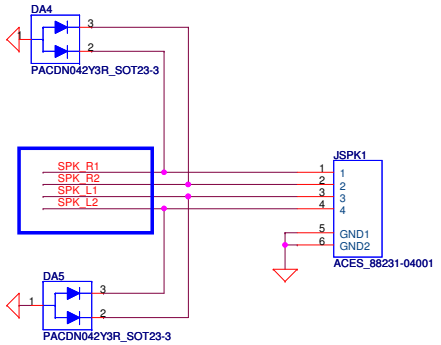
~~01/26 common design pull high~~



12/19 Reserved JP6 for audio test

Speaker Connector





12/16 Fine tune SPK_L1,SPK_L2,SPK_R1 and SPK_R2 for SPK

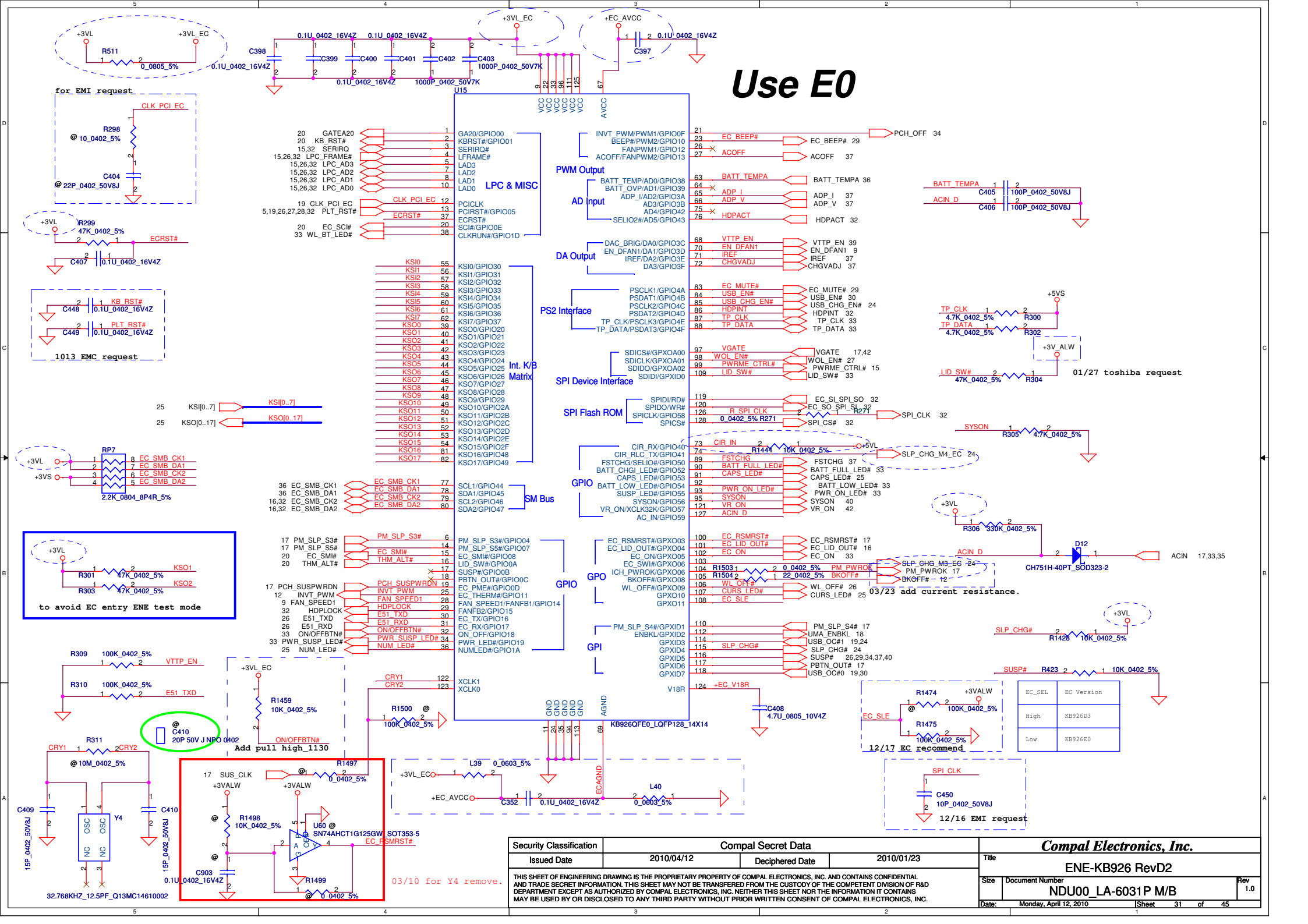
Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2009/04/14

Compal Electronics, Inc.

Title: *AMP/Audio Jack/HP/SPEAKER/VR*

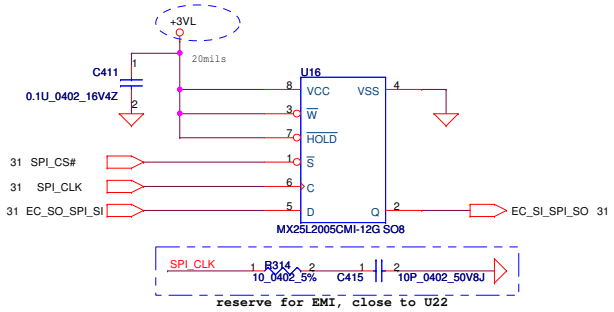
Size	Document Number	Rev
Custom	*NDU00_LA-6031P M/B*	1.0

Date: Monday, April 12, 2010 | Sheet 30 of 45


Use E0
for EMI request
1013 EMC request
to avoid EC entry ENE test mode
Add pull high_1130
03/10 for Y4 remove.
01/27 toshiba request
03/23 add current resistance.
12/17 EC recommend
12/16 EMI request
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
GPIO
SM Bus
GPO
GPI
KB926QFE0_LQFP128_14X14
Security Classification
Compal Secret Data
Issued Date
2010/04/12
Deciphered Date
2010/01/23
Compal Electronics, Inc.
ENE-KB926 RevD2
NDU00_LA-6031P M/B
Rev 1.0
Monday, April 12, 2010
Sheet 31 of 45

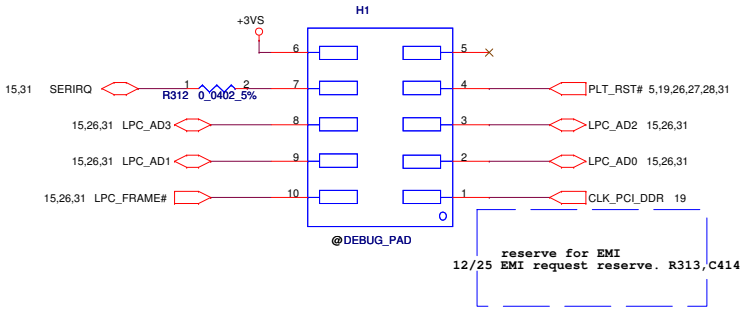
SPI Flash (256KB)

Socket: SP07000F500 & SP07000H900

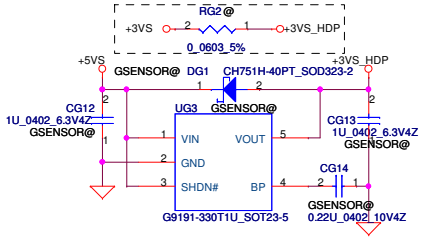


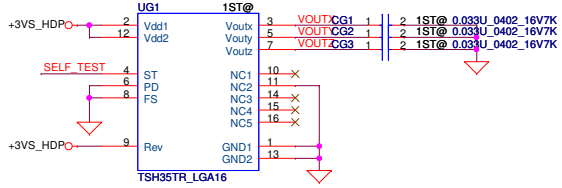
LPC Debug Port

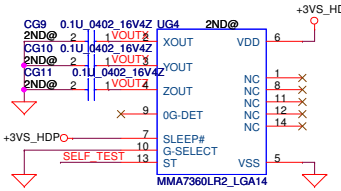
Please place the PAD under DDR DIMM.

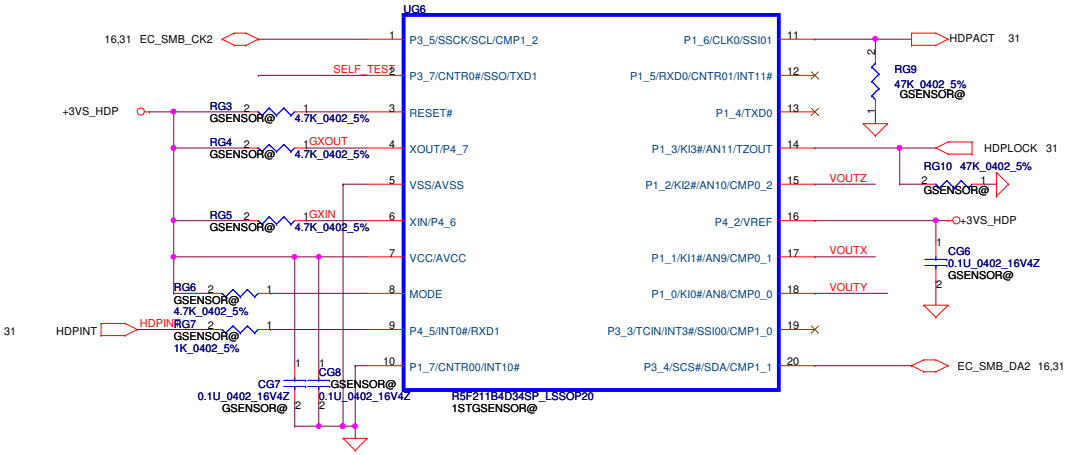


G-Sensor





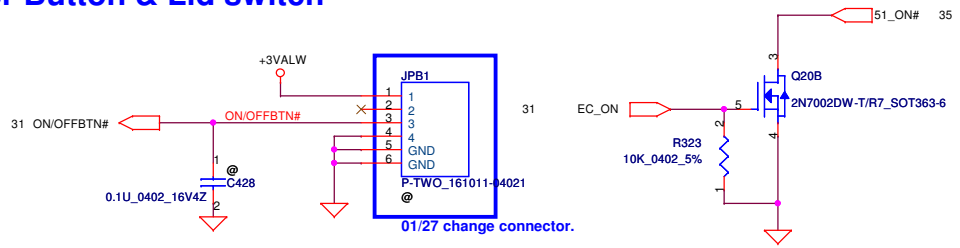




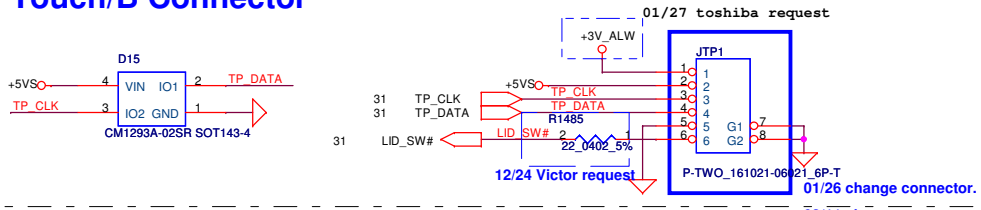
Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2009/04/14

Compal Electronics, Inc.			
Title	SPI/LPC/PS2/MDC/FM/CIR		
Size: Custom	Document Number: NDU00_LA-6031P M/B		Rev: 1.0
Date: Monday, April 12, 2010	Sheet 32 of 45		

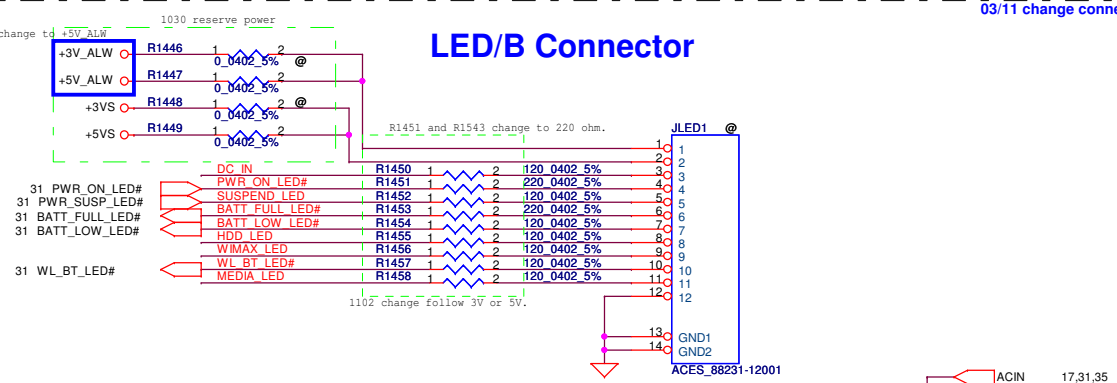
Power Button & Lid switch

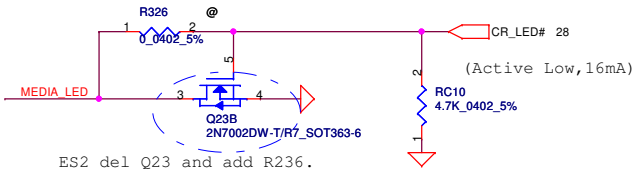


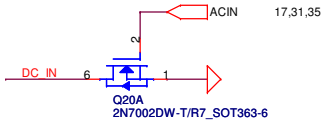
Touch/B Connector

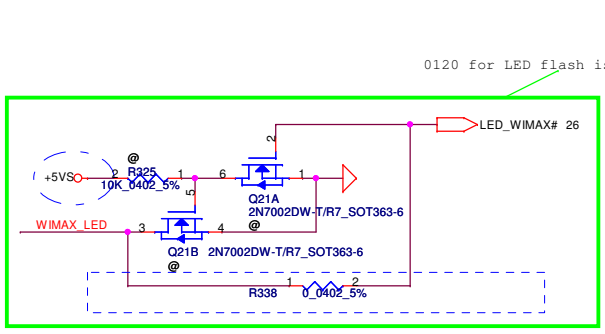


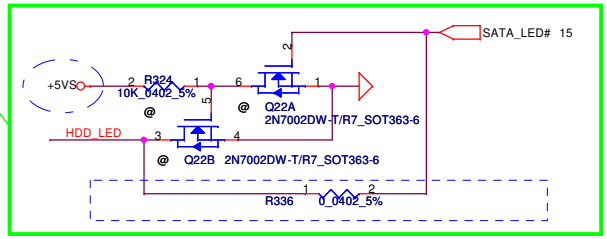
LED/B Connector





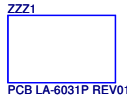




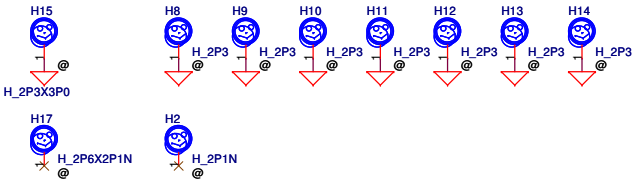


ISPD

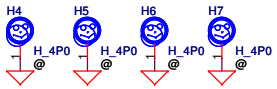
PCB



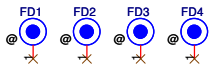
Screw Hole

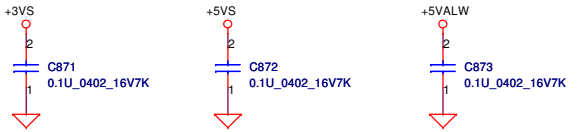


CPU



PCB Fedical Mark PAD





Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

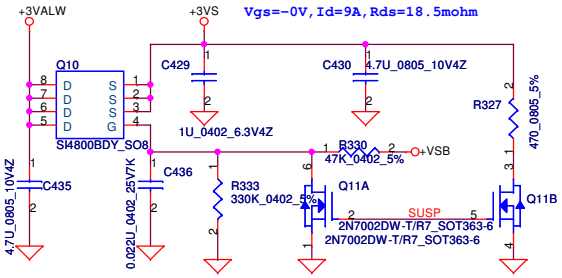
Compal Electronics, Inc.

Title: Comm. SW/ Sub Conn./LEDS

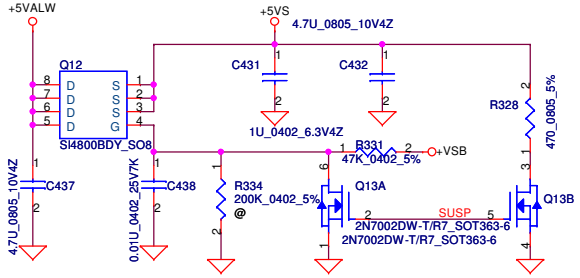
Size | Document Number: NDU00_LA-6031P M/B | Rev: 1.0

Date: Monday, April 12, 2010 | Sheet 33 of 45

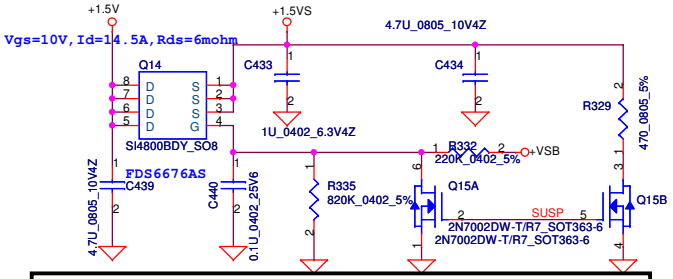
+3VALW TO +3VS



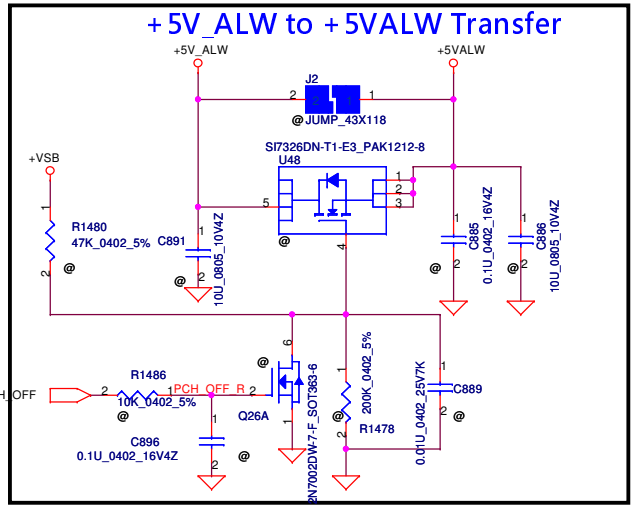
+5VALW TO +5VS



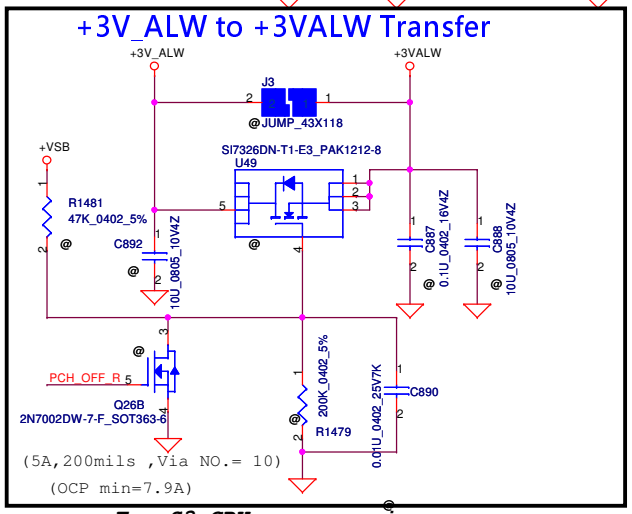
+1.5V to +1.5VS



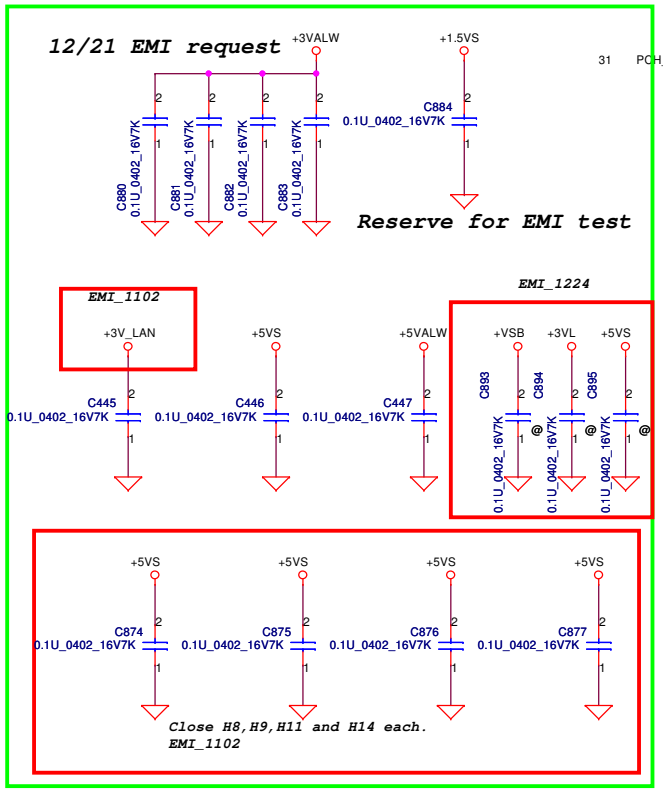
+5V_ALW to +5VALW Transfer



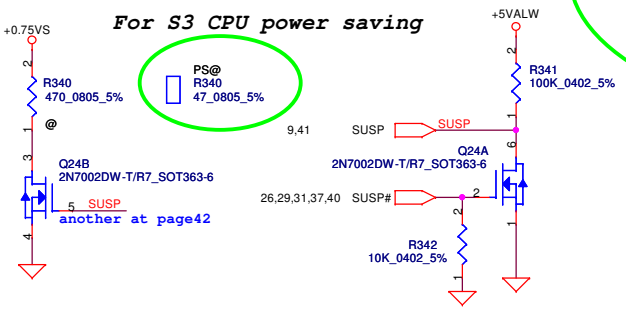
+3V_ALW to +3VALW Transfer



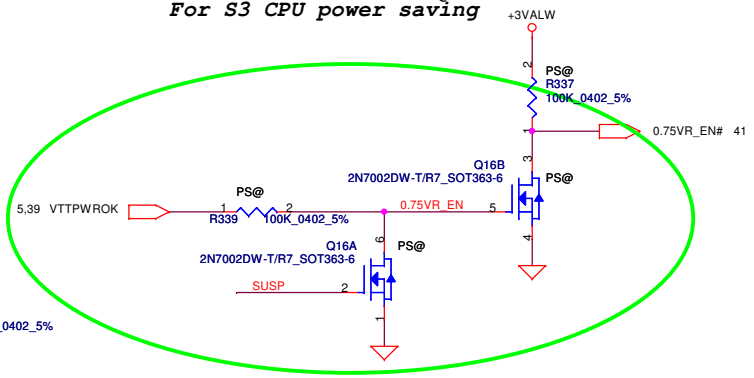
12/21 EMI request



For S3 CPU power saving



For S3 CPU power saving



Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: DC-DC INTERFACE

Size	Document Number	Rev
	NDU00_LA-6031P M/B	1.0

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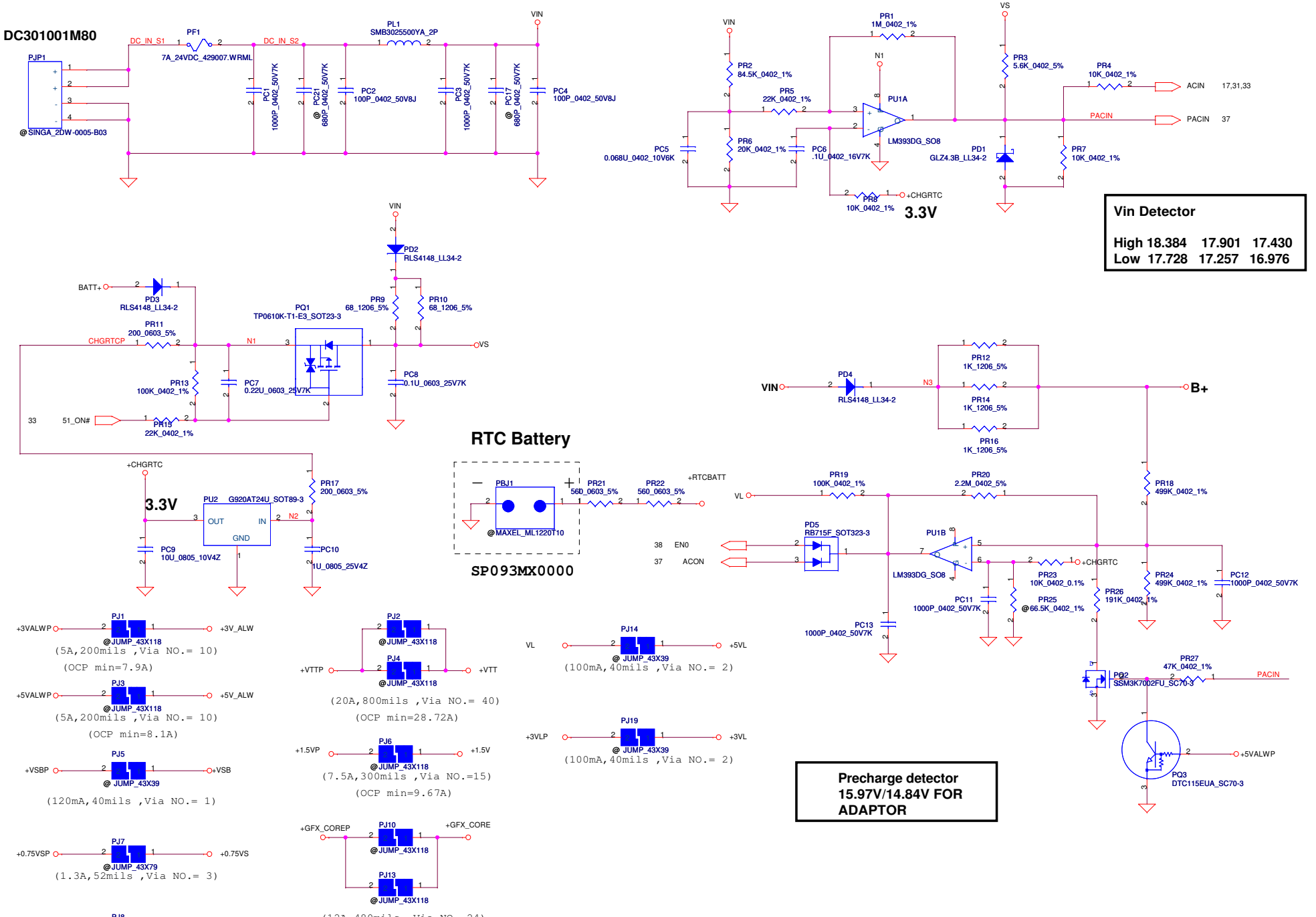

Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/10/02

Compal Electronics, Inc.

Title: DCIN / DETECTOR

Size	Document Number	Rev
	LA-6031P	1.0

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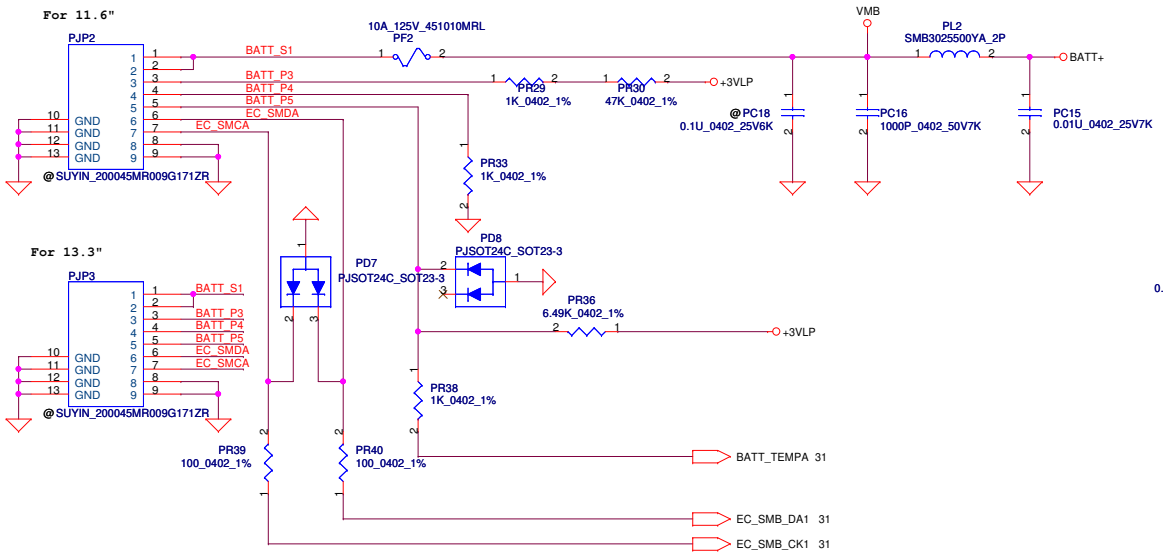
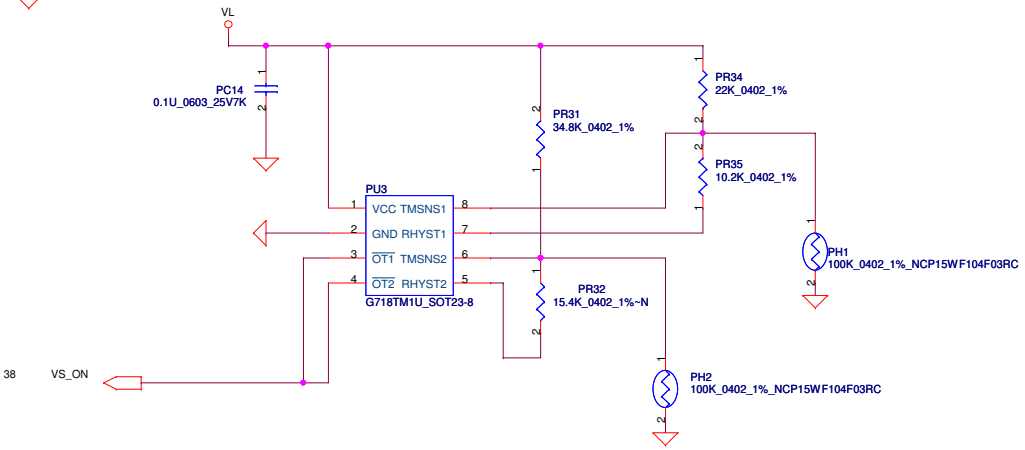
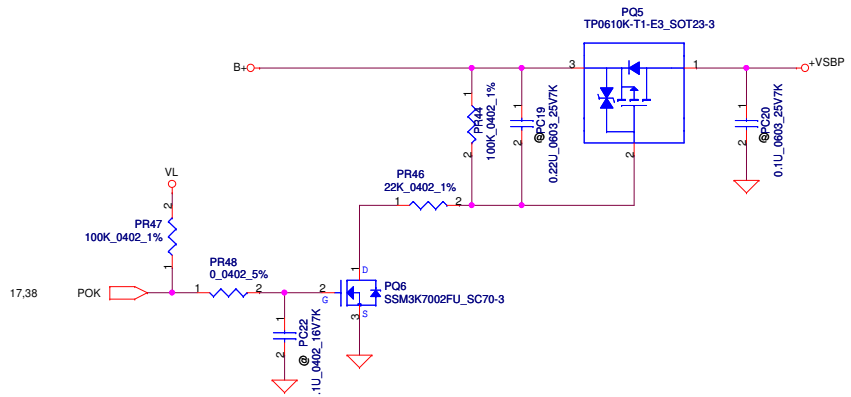
PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C

PH2 near main battery CONN:
BAT.thermal protection at 78 degree C
Recovery at 42 degree C







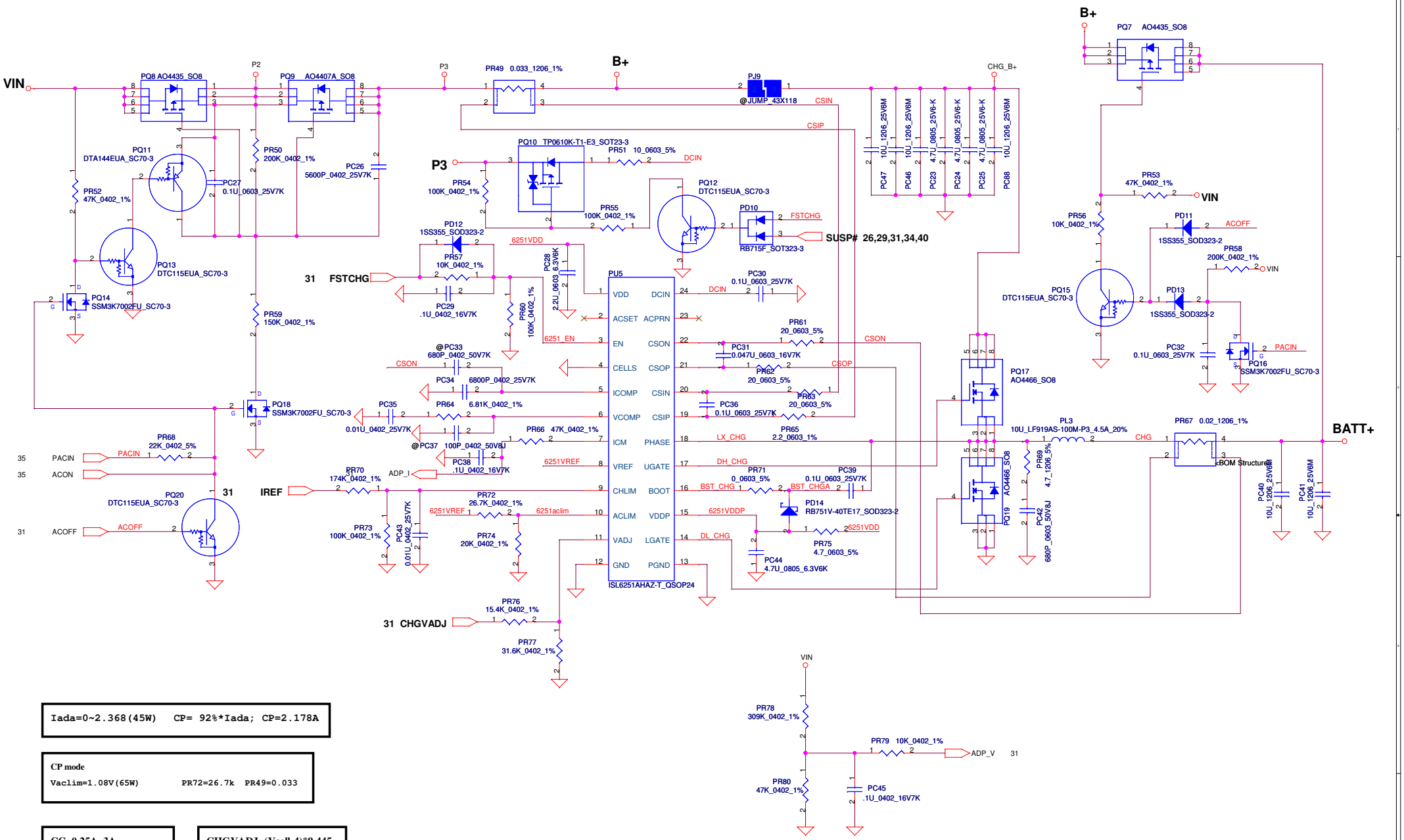
Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/10/02

Compal Electronics, Inc.

Title: BATTERY CONN / OTP

Size	Document Number	Rev
	LA-6031P	1.0

Date: Monday, April 12, 2010 | Sheet 36 of 45



Iada=0~2.368(45W) CP= 92%*Iada; CP=2.178A

CP mode

Vaclim=1.08V(65W) PR72=26.7k PR49=0.033

CC=0.25A~3A
IREF=1.096*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

CHGVADJ=(Vcell-4)*9.445

Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

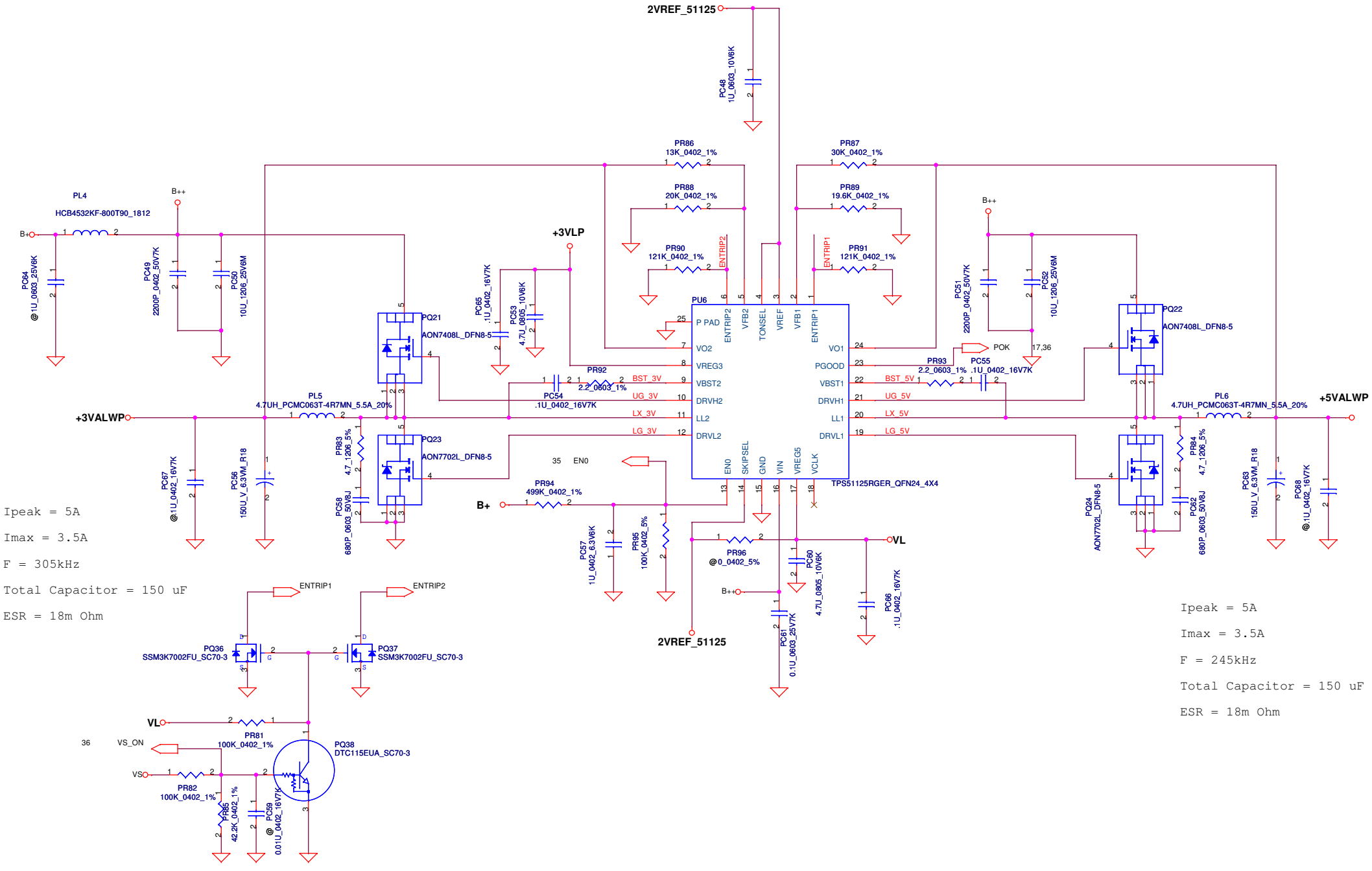
Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/10/02

Compal Electronics, Inc.

Title: CHARGER

Size	Document Number	Rev
	LA-6031P	1.0

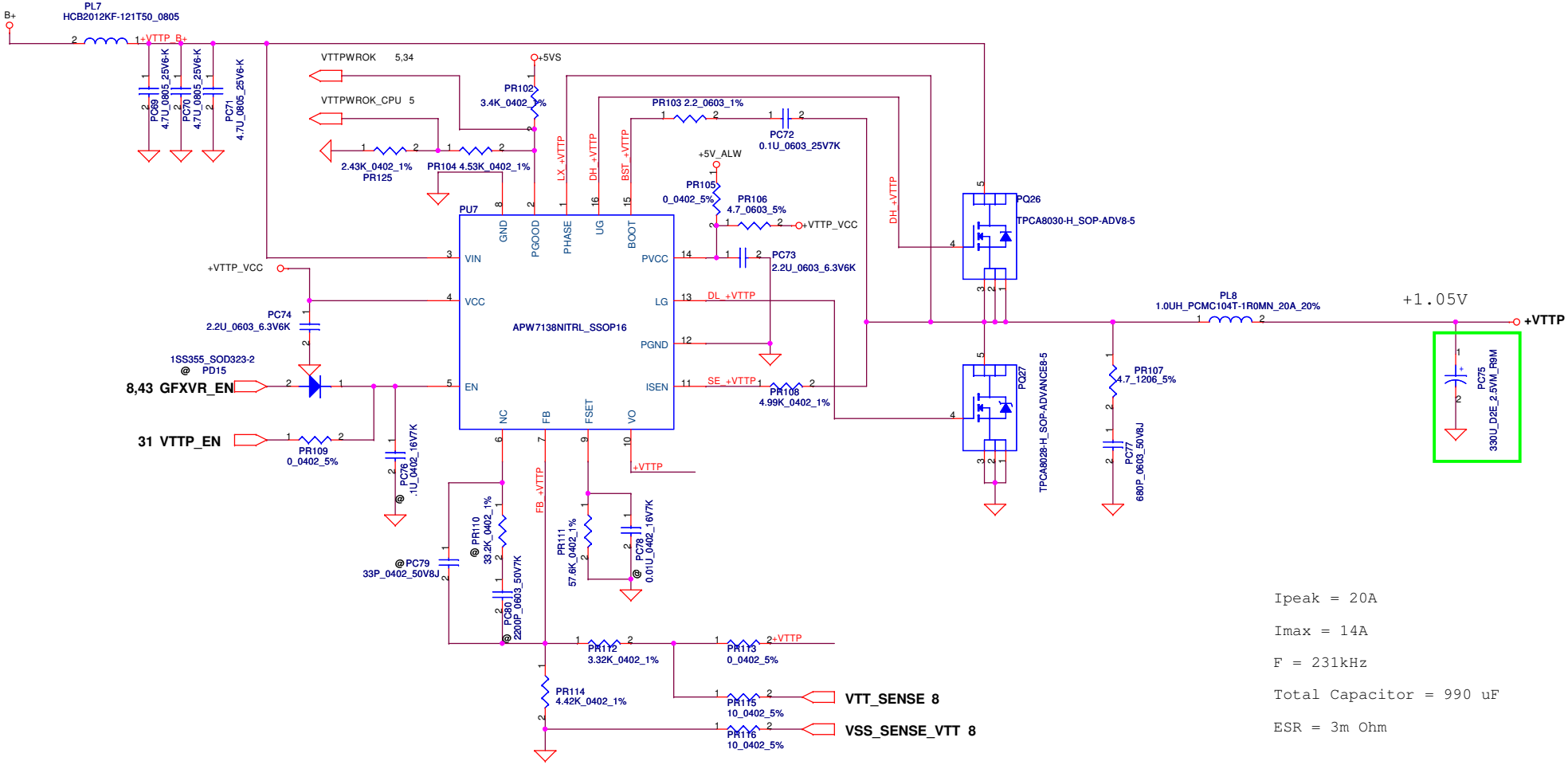
Date: Monday, April 12, 2010 Sheet 37 of 45



Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/10/02

Compal Electronics, Inc.

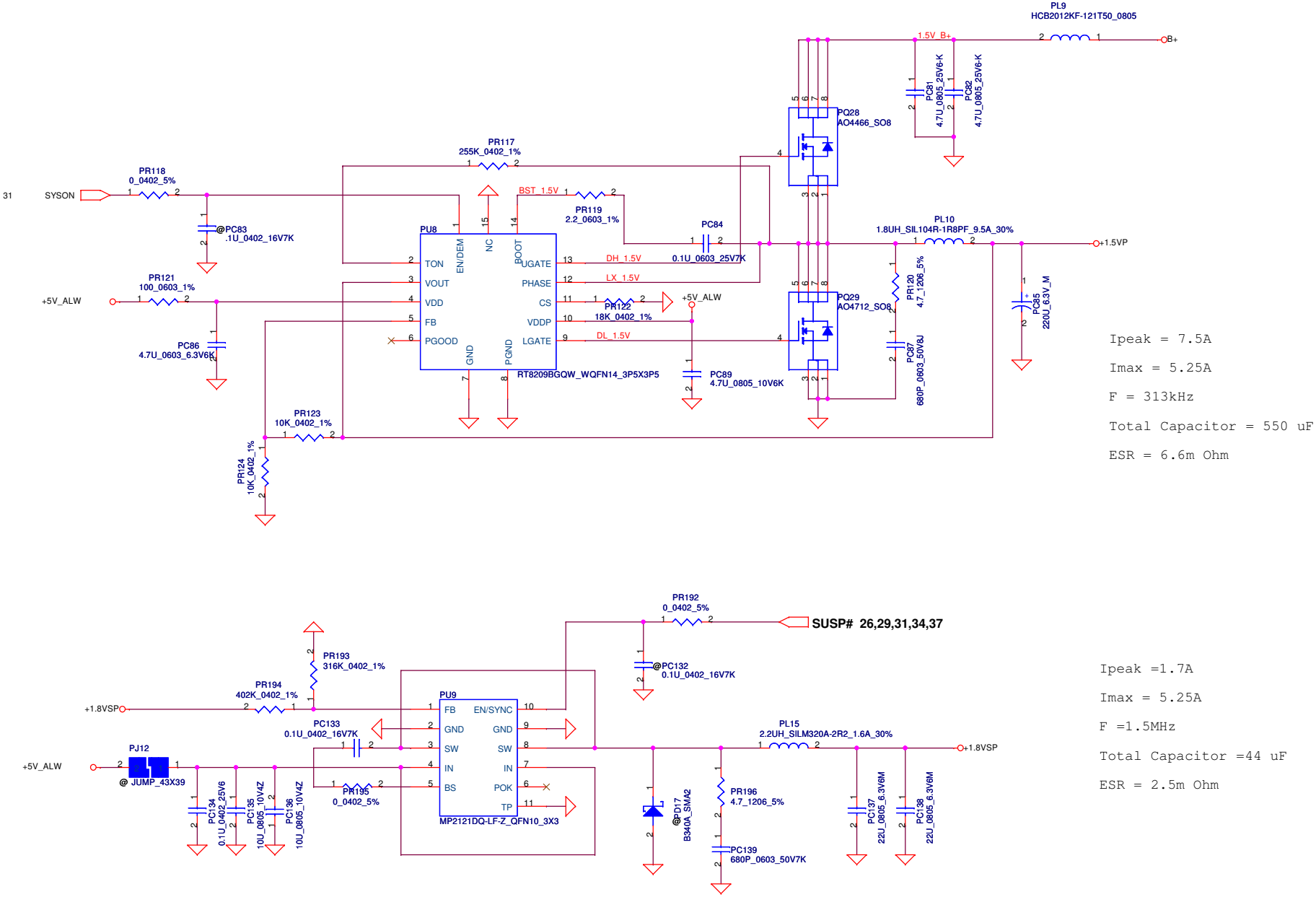
Title	+5VALWP/+3VALWP	
Size	Document Number: LA-6032P	Rev: 1.0
Date: Monday, April 12, 2010	Sheet 38 of 45	



Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

Compal Electronics, Inc.

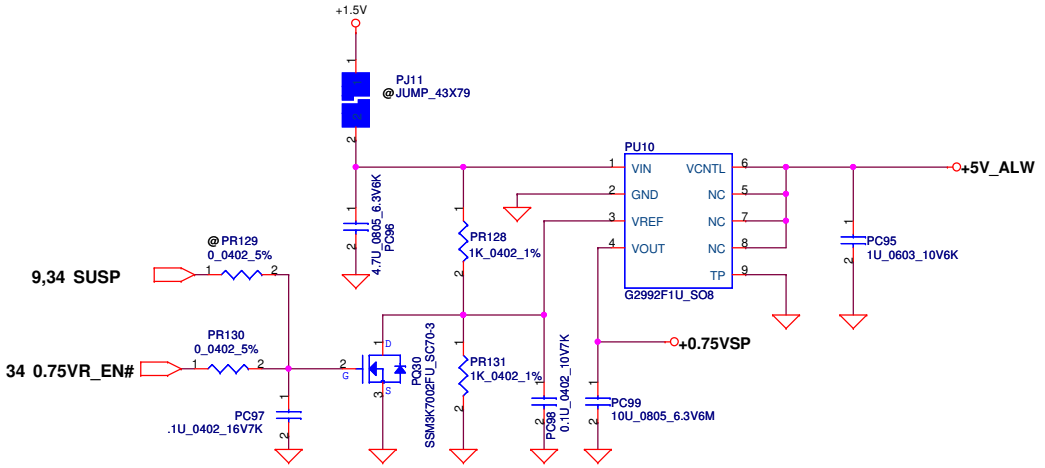
Title	+VTTP	
Size	Document Number	Rev
	NDU00_LA-6031P M/B	1.0
Date: Monday, April 12, 2010	Sheet 39 of 45	



Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/10/02

Compal Electronics, Inc.

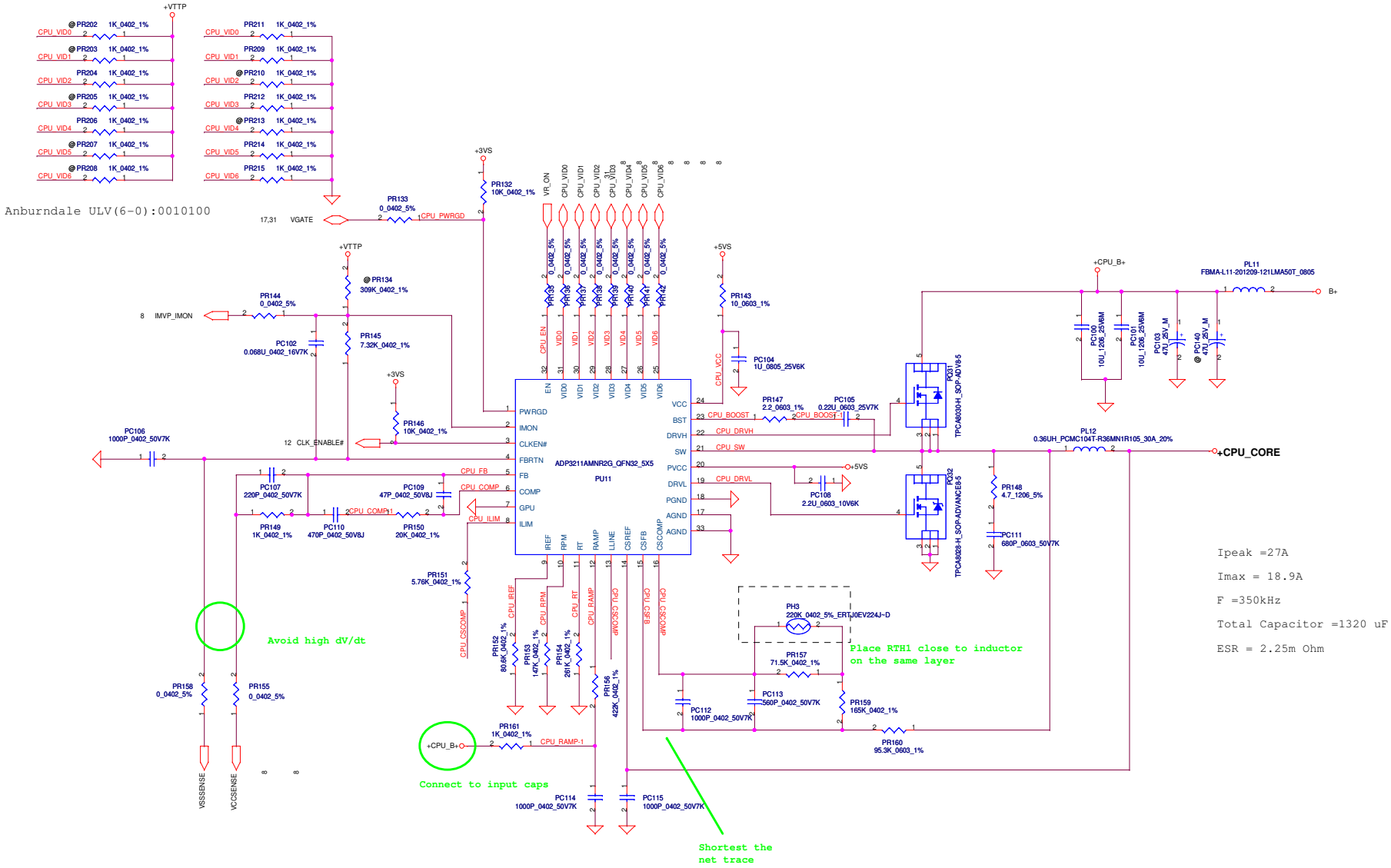
Title	+1.5VP/+1.8VSP	
Size: Custom	Document Number: NDU00_LA-6031P M/B	Rev: 1.0
Date: Monday, April 12, 2010	Sheet 40 of 45	



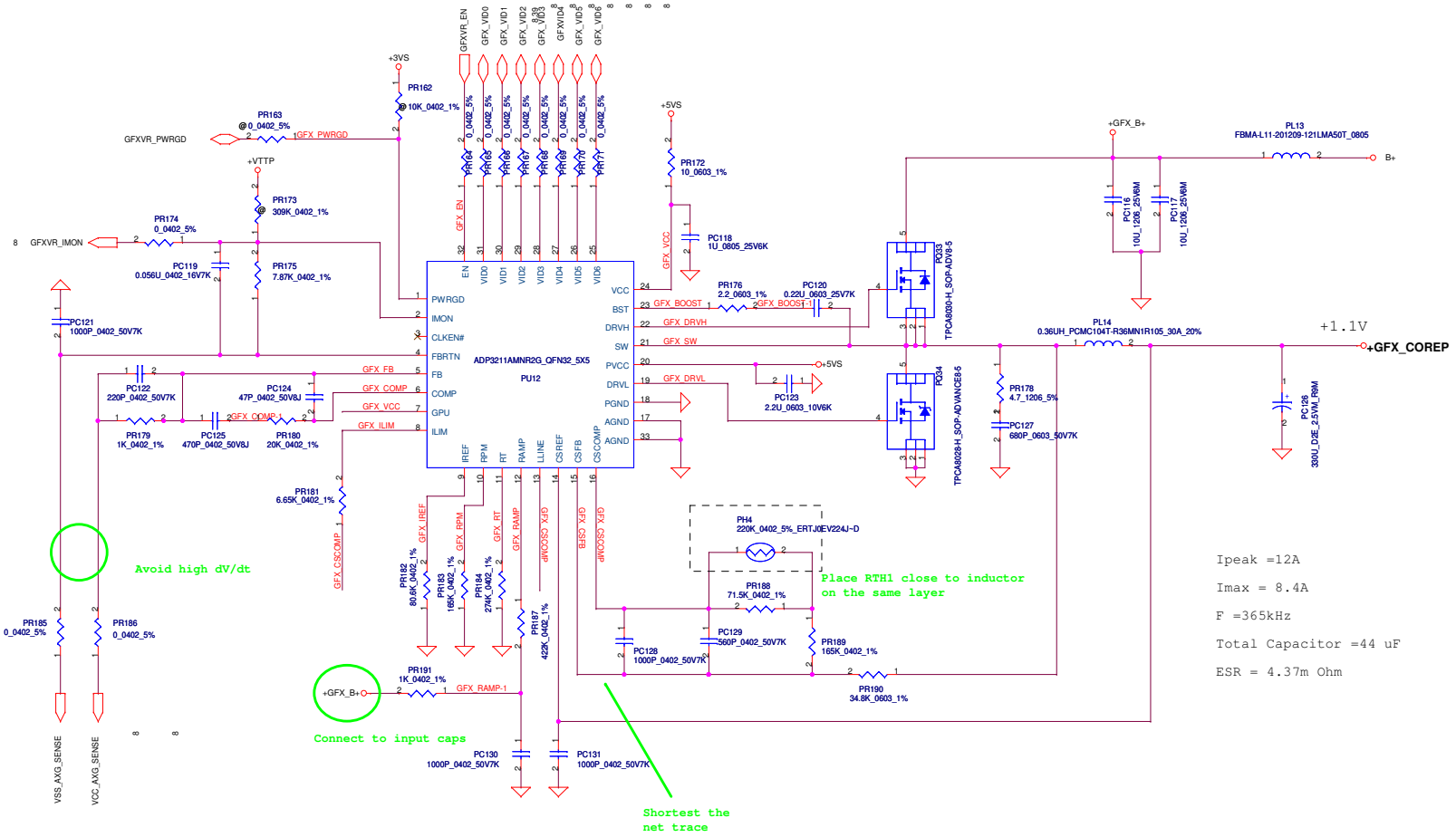
Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/10/02

Compal Electronics, Inc.

Title	0.75VSP	
Size	Document Number: NDU00_LA-6031P M/B	Rev: 1.0
Date: Monday, April 12, 2010	Sheet 41 of 45	



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2010/04/12	Deciphered Date	2010/10/02
Title	+CPU_CORE		
Size	Document Number		Rev
	NDU00_LA-6031P M/B		1.0
Date: Monday, April 12, 2010		Sheet 42 of 45	



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2010/04/12	Deciphered Date	2010/10/02
Title	+GFX		
Size	Document Number		Rev
	NDU00_LA-6031P M/B		1.0
Date: Monday, April 12, 2010		Sheet 43 of 45	

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
	2009/11/9(EVT)	P38 +5VALWP/+3VALWP	PC54,PC55,PC65,PC66 change SE076104KM8 to SE076104K80	change to A51 material
	2009/11/9(EVT)	P39 +VTTP	Resever PD15	Design change
	2009/11/9(EVT)	P41 +0.75VSP	Change PQ30 to SB000009610	Design change
	2009/11/9(EVT)	P42 CPU_CORE	Change PU11 change to ADP3211	Design change
	2009/11/9(EVT)	P42 CPU_CORE	Change PH3 &PH4	change to A51 material
	2009/11/9(EVT)	P37 CHARGE	Change PR49 change to 33m	Design change
	2009/11/9(EVT)	P38 +5VALWP/+3VALWP	PR90 & PR91 change to 121K	Design change
	2009/12/1(DVT)	P39 +CPU-CORE	Add PR202~PR215 pull-up & pull-down	Design change
	2009/12/17(DVT)	P36 Battery	Change PR31,PR32,PR34,PR35	Design change
	2009/12/17(DVT)	P37 CHARGE	Change PC23,PC24,PC25,PC81,PC82 1206 to 0805	Design change
	2009/12/22(DVT)	P42 CPU_CORE	Change PR147 0 ohm change to 2.2 ohm	EMI commond
	2009/12/22(DVT)	P43 GFX	Change PR176 0 ohm change to 2.2 ohm	EMI commond
	2009/12/22(DVT)	P39 +VTTP	ADD material PR125 & PR104 & PR102 and add net VTTPWORK_CPU	Design change
	2010/01/25(PVT)	P36 Battery	Add PD7,PD8	EMI require
	2010/01/27(PVT)	P37 CHARGE	Add 10u x3 PC46,PC47,PC88	EMC require
	2010/02/04(PVT)	P41 +0.75VSP	Resever PR129 Add PR130 and PC97	Design change
	2009/02/04(PVT)	P38 +5VALWP/+3VALWP	Change PQ38	Design change
	2010/02/04(PVT)	P42 CPU_CORE	Change PR160 to 95.3K and PR145 to 7.32K	Design change
	2010/02/08(PVT-2)	P36 Battery	Change PR21&PR22 and +CHGRTC	Design change

Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
1	Intel S3 power saving	05	Install Q1, R1484, C878, R8, R40 and Remove R2, R42	12/25	DVT
2	HDMI Detection function	14	modify HDMI_HPD circuit (Remove U7)	12/25	DVT
3	Sleep charge control method change	19 & 31	SLP_CHG_M3_R & SLP_CHG_M4_R change from PCH to Pin103 & 74 of EC	12/25	DVT
4	Implement Low power HDA	22	Reserve R1468 & R1469 for 1.5VALW (Low Power HDA)	12/25	DVT
5	Debug usage	26	Reserve LPC bus at WLAN solt	12/14	DVT
6	LAN circuit change for Vendore request	27	RL21 contact to GND	12/18	DVT
7	Avoid power leakage & reduce double pull up	27	Remove RL3	12/25	DVT
8	Transformer change	27	Move Transformer from Sub-board to M/B	12/21	DVT
9	Prevent Card Reader IC damagewhen insert dummy card	28	Add F2	12/24	DVT
10	Audio PD# issue (Could not work)	29	Add RA29 pull up	12/19	DVT
11	Avoid Audio noise	29	reserve and unistall CA70, CA68, CA69, UA2, RA30, CA67	12/22	DVT
12	Enhance Right side USB ability	30	modify JP2 pin assignment and reserve JP3 pad for test	12/19	DVT
13	Sleep charge control method change	31	add pin 21 of EC for control ALW power MOS	12/21	DVT
14	Sleep charge control method change	34	add twoV_ALW power transfer circuits (3V_ALW to 3VALW & 5V_ALW to 5VALW)	12/21	DVT
15	system idle hang up issue	8	CPU_PSI# Pull down 1k ohm & H_DPRSLPVR pull up 1k ohm to Vtt	12/19	DVT
16	Sleep charge control method change	24	change U14 power from 5VALW to 5V_ALW	12/21	DVT
17					
18	EC_SWI# pull up twice. R190	27	RL3 reserved.	01/20	PVT
19	Audio LDO reserved for AVDD.	29	UA2 pin 5 for +AVDD	01/20	PVT
20	For S3 power saving.	05	Reserve R2 and change R1484 to 0 ohm.	01/20	PVT
21	For 3G LED flash when resume from S3.	33	Reserve Q21 and Q22 circuit. Add R338 and R336.	01/20	PVT
22	Don't need discharge circuit.	34	Modify Q26 and Q27 circuit.	01/20	PVT
23	Reserve for PCH and EC both.	19,24,31	Add R1487,R1488,R1489 and R1490.	01/20	PVT
24	Change JHDD1 pin 4 to GND.	24		01/20	PVT
25	Add BT power control circuit.	26	Add D85 and Q27.	01/20	PVT
26	change cardreader connector.	28	ME request	01/26	PVT
27	change LED always power	33	3G LED flash issue.	01/26	PVT
28	change TP connector.	33	ME request	01/26	PVT
29	JGSIM2 connector.	26		01/26	PVT
30	add R1491 in USB_EN#	30		01/26	PVT
31	Lid switch change to +3V_ALW	31,33	Toshiba request.	01/26	PVT
32	add USB port 9 and PCIe port 4 for 8 pin SIM card.	16,19,26		01/27	PVT
33	add R1494 and D84 near D5 and add L,C near U8	15,18	EMI request	02/03	PVT
34	change MIC1_R and MIC1_L pull high.	29	MIC issue.	02/03	PVT
35	JLVDS1 pin24 change to NC.	12	Common design.	03/04	PVT2
36	CRT trace modify.	18	wrong trace.	03/04	PVT2
37	D5 layout close to PCH (U8)		layout change.	03/04	PVT2
38	Change O2 to JMicron card reader.	28		03/22	PVT2
39	USB OC# change.	19	Common design.	03/22	PVT2
40	Add R1505.	17	EMI request	03/22	PVT2

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Title: PIR

Size: Document Number: NDI300_LA-6891P M/B Rev: 1.0

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