# BU1 Block Diagram

**PCB STACK UP**

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT

- VCC_CORE
- +1.5V
- +1.05V
- +1.25V
- +1.8VSUS
- +3VPCU
  +3V_S5
  +3VSUS
  +3V
  +5VPCU
  +5V_S5
  +5V
  SMDDR_VTERM
  SMDDR_VREF

**Intel**
Merom
(35W)
Page 3,4

**CLOCK GENERATOR**
CK505
ICS9LPR363
Page 2

FSB(667/800MHZ)

**Crestline GM**
Page 5,7,8,9,10,11

R.G.B
LVDS X1
533/ 667 MHZ DDR II

**CRT** Page 18
**LCD(WXGA 13W)** Page 18
**DDRII-SODIMM1**
**DDRII-SODIMM2** Page 12,13

SATA
PATA
DMI(x2/x4)

**SATA - HDD** Page 19 G SENSOR
**IDE - ODD** Page 19

**ICH8M**
Page 14,15,16,17

PCI-Express

**MINI CARD WLAN** Page 23
**MINI CARD** Page 23 (BOT)
**NEW CARD** Page 24 (BOT)
**100/10 LAN RTL8101E** Page 20
**Connector**
RJ11/RJ45/USB DAUGHTER BOARD
**RJ45** **RJ11** **USB**

USB 2.0

DAUGHTER BORD

**System 0** Page 24 USB PORT 0
**System 1** Page 24 USB PORT 1
**System 2** Page 24 USB PORT 2
**WLAN** Page 23 USB PORT 3
**Finger Printer** (BOT) Page 24 USB PORT 4
**Bluetooth** (BOT) Page 24 USB PORT 5
**New Card** (BOT) Page 24 USB PORT 6
**Reserved** (BOT) Page 23 USB PORT 7
**Camera** (BOT) Page 18 USB PORT 8

Azalia

PCI Bus

**PCMCIA Controller (CB 1410)** Page 21 (BOT)
**Card Reader/1394 (R5C833)** Page 22
**PCMCIA** (BOT)
**5 IN 1**
**1394** (BOT)

LPC

32.768KHz

**WPC8763LDG**
Page 26

**FAN** **Touch PAD** **Key Board** **FLASH ROM**

| PCI ROUTING TABLE | IDSEL | INTERUPT | DEVICE |
|---|---|---|---|
| REQ0# / GNT0# | AD17 | INTA#,INTB# | R5C832 |
| REQ1# / GNT1# | AD20 | INTC# | CB1410 |

AUDIO/FM/USB DAUGHTER BOARD

**HP** **HP AMP** **AUDIO CODEC (ALC262)** **Connector**
**INT SPK** **SPK AMP** **MDC 1.5** Page 25
**USB**
**RJ11**

**BTO BOM OPTION**

```
CB@ : CARD BUS
FP@ : FINGER PRINTER
BT@ : BLUETOOTH
CM@ : CAMERA
GS@ : G-SENSOR
NEW@ : NEW CARD
LCD@ : LCD TYPE PANEL
LED@ : LED TYPE PANEL
1394@ : 1394
```

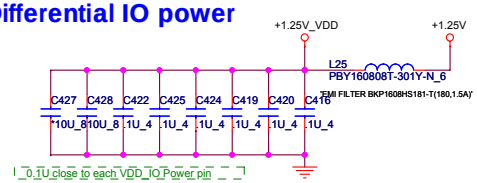
**Quanta Computer Inc.**
**PROJECT : BU1 Santa Rosa**

| Size | Document Number | Rev |
|---|---|---|
| | Block Diagram | 1A |

Date: Monday, March 26, 2007 Sheet 1 of 33

# Clock Generator

## Clock Gen Differential IO power

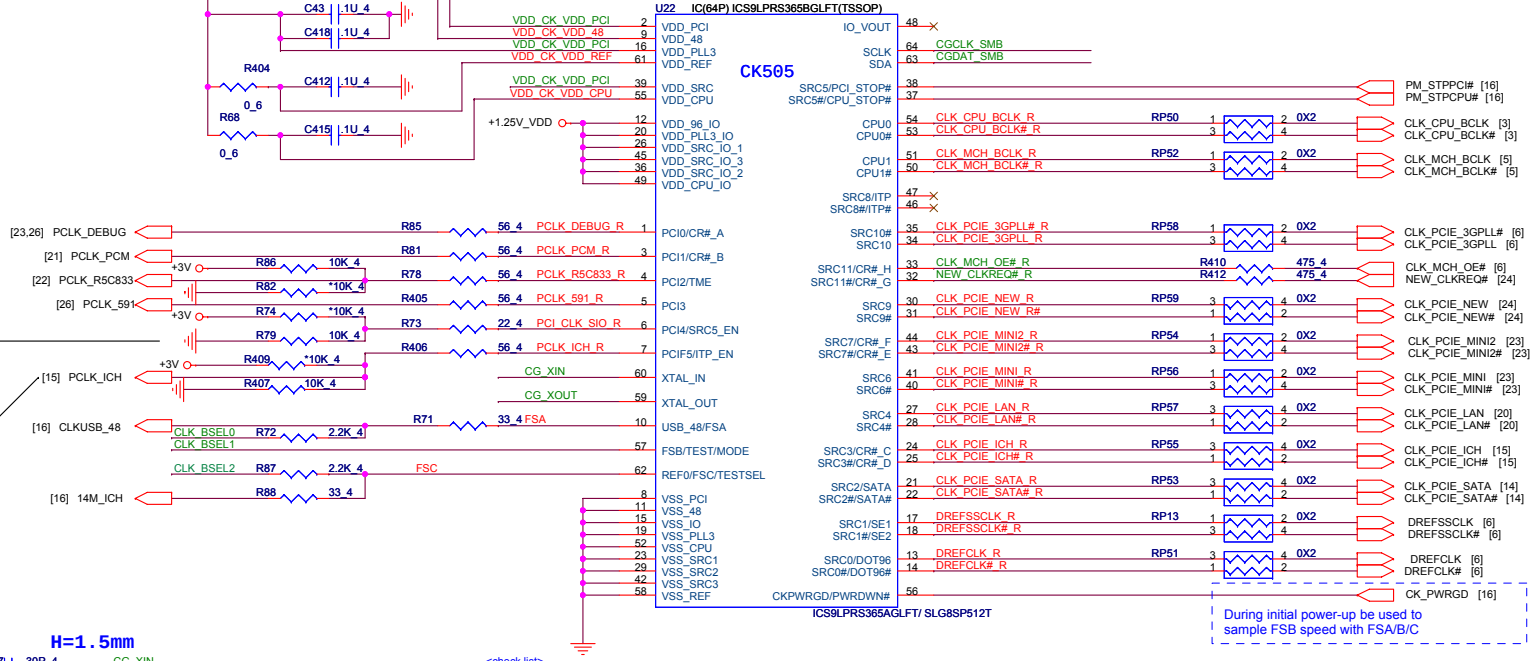



H=1.2mm

ICS9LPRS365BGLFT
SLG8SP512T: AL8SP512K05

U22 IC(64P) ICS9LPRS365BGLFT(TSSOP)

CK505



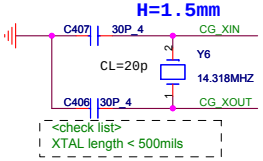




<check list>
PCI4/SRC5_EN: PU be used, the CK505 will be configured to use Pin37/38 to SRC5 clock.If PD be detect at powe-on,the CK505 will setting Pin 37/38 to PCI_STOP/CUP_SOTP(Default is setting to PCI_STOP/CUP_SOTP)

<check list>
PCIF5/ITP_EN: PU be used, the CK505 will be configured to use Pin46/47 to CPU ITP clock.If PD be detect at powe-on,the CK505 will setting Pin 46/47 to SRC8(Default is setting to SRC8)

H=1.5mm




<check list>
XTAL length < 500mils

<check list>
(1)PCI2/TME: PU be used, the CK505 cannot over clock any of the clock for Trust Mode security purposes.

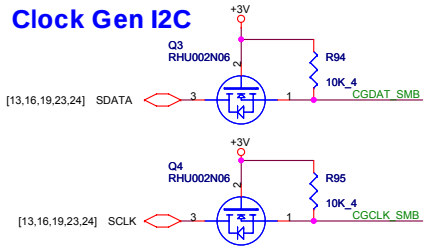
(2)PCI4/SRC5_EN: PU be used, the CK505 will be configured to use Pin37/38 to SRC5 clock.
If PD be detect at powe-on,the CK505 will setting Pin 37/38 to PCI_STOP/CUP_SOTP
(Default is setting to PCI_STOP/CUP_SOTP)

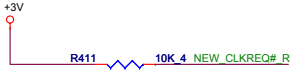
(3)PCIF5/ITP_EN: PU be used, the CK505 will be configured to use Pin46/47 to CPU ITP clock.
If PD be detect at powe-on,the CK505 will setting Pin 46/47 to SRC8
(Default is setting to SRC8)

(4)SLG8SP512 Pin 6 select Pin 17, 18 output is LCDCLK or 27 M, PD is LCDCLK, PU is 27 M , Pin 37, 38 will fixed be use CPU_Stop and PCI_Stop.

(5)SLG505YC64 CK505 Standar parts follow standar setting

## Clock Gen I2C

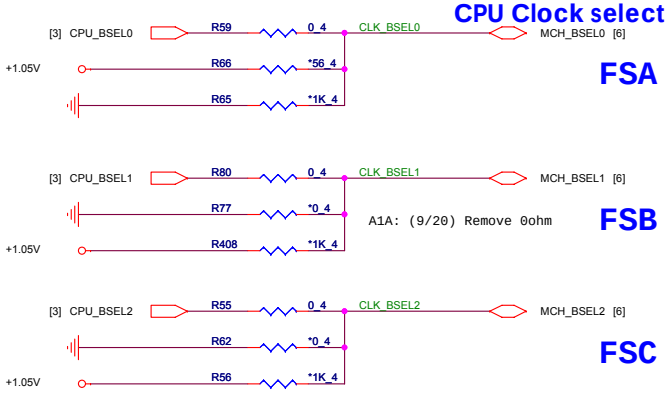



## BSEL Frequency Select Table

| FSC | FSB | FSA | Frequency |
|---|---|---|---|
| 0 | 0 | 0 | 266Mhz |
| 0 | 0 | 1 | 133Mhz |
| 0 | 1 | 1 | 166Mhz |
| 0 | 1 | 0 | 200Mhz |
| 1 | 1 | 0 | 400Mhz |
| 1 | 1 | 1 | Reserved |
| 1 | 0 | 1 | 100Mhz |
| 1 | 0 | 0 | 333Mhz |

## CPU Clock select




Quanta Computer Inc.
PROJECT : BU1 Santa Rosa

| Size | Document Number | Rev |
|---|---|---|
| | CLK. GEN./ CK505 | 1A |
| Date: Monday, March 26, 2007 | Sheet 2 of 33 | |

# CPU(HOST)

U24A

ADDR GROUP 0: H_A#3 H_A#4 H_A#5 H_A#6 H_A#7 H_A#8 H_A#9 H_A#10 H_A#11 H_A#12 H_A#13 H_A#14 H_A#15 H_A#16 — [5] H_A#[16:3]
ADDR GROUP 1: H_A#17 H_A#18 H_A#19 H_A#20 H_A#21 H_A#22 H_A#23 H_A#24 H_A#25 H_A#26 H_A#27 H_A#28 H_A#29 H_A#30 H_A#31 H_A#32 H_A#33 H_A#34 H_A#35 — [5] H_A#[35:17]
REQ: [5] H_ADSTB0# [5] H_REQ#[4:0] — H_REQ#0 H_REQ#1 H_REQ#2 H_REQ#3 H_REQ#4
[5] H_ADSTB1#

CONTROL:
ADS# BNR# BPRI# — H_ADS# [5] H_BNR# [5] H_BPRI# [5]
DEFER# DRDY# DBSY# — H_DEFER# [5] H_DRDY# [5] H_DBSY# [5]
BR0# — H_BREQ#0 [5]
IERR# — H_IERR# R16 56.2_4 +1.05V
INIT# — H_INIT# [14]
LOCK# — H_LOCK# [5]
RESET# RS[0]# RS[1]# RS[2]# TRDY# — H_CPURST# [5] H_RS#0 [5] H_RS#1 [5] H_RS#2 [5] H_TRDY# [5]
HIT# HITM# — H_HIT# [5] H_HITM# [5]

XDP/ITP SIGNALS:
BPM[0]# BPM[1]# BPM[2]# BPM[3]# PRDY# PREQ# TCK TDI TDO TMS TRST# DBR#
XDP_TCK XDP_TDI XDP_TMS XDP_TRST# XDP_DBRESET# R19 0_4 SYS_RST# [16]

THERMAL:
PROCHOT# THERMDA THERMDC — H_PROCHOT_R# H_THERMDA H_THERMDC
THERMTRIP# — THERMTRIP#_PWR
R17 56.2_4 +1.05V
R18 *2.2K_4 H_PROCHOT# [29]

<check list>
Default PU 56ohm if no use.
Serial R NC, If connect to power side PU 68ohm. Serial R 2.2K

H CLK:
BCLK[0] BCLK[1] — CLK_CPU_BCLK [2] CLK_CPU_BCLK# [2]

[14] H_A20M# [14] H_FERR# [14] H_IGNNE#
[14] H_STPCLK# R26 0_4 H_STPCLK_R#
[14] H_INTR [14] H_NMI [14] H_SMI#

RESERVED:
TP_CPU_RSVD01 TP_CPU_RSVD02 TP_CPU_RSVD03 TP_CPU_RSVD04 TP_CPU_RSVD05 TP_CPU_RSVD06 TP_CPU_RSVD07 TP_CPU_RSVD08 TP_CPU_RSVD09 TP_CPU_RSVD10
T3 T5 T8 T1 T146 T7 T6 T9 T4 T12

Merom Ball-out Rev 1a

U24B

DATA GRP 0: H_D#0 H_D#1 H_D#2 H_D#3 H_D#4 H_D#5 H_D#6 H_D#7 H_D#8 H_D#9 H_D#10 H_D#11 H_D#12 H_D#13 H_D#14 H_D#15 — [5] H_D#[15:0]
DATA GRP 1: H_D#16 H_D#17 H_D#18 H_D#19 H_D#20 H_D#21 H_D#22 H_D#23 H_D#24 H_D#25 H_D#26 H_D#27 H_D#28 H_D#29 H_D#30 H_D#31 — [5] H_D#[31:16]
DATA GRP 2: H_D#32 H_D#33 H_D#34 H_D#35 H_D#36 H_D#37 H_D#38 H_D#39 H_D#40 H_D#41 H_D#42 H_D#43 H_D#44 H_D#45 H_D#46 H_D#47 — H_D#[47:32] [5]
DATA GRP 3: H_D#48 H_D#49 H_D#50 H_D#51 H_D#52 H_D#53 H_D#54 H_D#55 H_D#56 H_D#57 H_D#58 H_D#59 H_D#60 H_D#61 H_D#62 H_D#63 — H_D#[63:48] [5]

DSTBN[0]# DSTBP[0]# DINV[0]# — [5] H_DSTBN#0 [5] H_DSTBP#0 [5] H_DINV#0
DSTBN[1]# DSTBP[1]# DINV[1]# — [5] H_DSTBN#1 [5] H_DSTBP#1 [5] H_DINV#1
DSTBN[2]# DSTBP[2]# DINV[2]# — H_DSTBN#2 [5] H_DSTBP#2 [5] H_DINV#2 [5]
DSTBN[3]# DSTBP[3]# DINV[3]# — H_DSTBN#3 [5] H_DSTBP#3 [5] H_DINV#3 [5]

MISC:
GTLREF TEST1 TEST2 TEST3 TEST4 TEST5 TEST6 — H_GTLREF AD26, CPU_TEST1 C23, CPU_TEST2 D25, CPU_TEST3 C24, CPU_TEST4 AF26, CPU_TEST5 AF1, CPU_TEST6 A26
R21 *1K_4 R20 *1K_4 C14 *.1U_4 T10 T2 T11
R11 1K_4 R9 2K_6 +1.05V
<Check list & CRB> Layout note: Z=55 ohm H_GTLREF<0.5"

COMP[0] COMP[1] COMP[2] COMP[3] — R26 COMP0 R14 27.4_6; U26 COMP1 R13 54.9_4; AA1 COMP2 R10 27.4_6; Y1 COMP3 R8 54.9_4
<CRB & Design guide> Layout Note:Connect from SB and daisy chain to CPU CORE VR.Not use T connect.(SB/VR/CPU/NB)
<Check list & CRB> Layout note: L<0.5" COMP0/2 Z=27.4ohm COMP1/3 Z=54.9

DPRSTP# DPSLP# DPWR# PWRGOOD SLP# PSI# — ICH_DPRSTP# [6,14,29] H_DPSLP# [14] H_DPWR# [5] H_PWRGD [14] H_CPUSLP# [5] PSI# [29]
BSEL[0] BSEL[1] BSEL[2] — [2] CPU_BSEL0 [2] CPU_BSEL1 [2] CPU_BSEL2

Merom Ball-out Rev 1a

# CPU Thermal monitor

Q33 RHU002N06 — [18,26,27] MBCLK
Q34 RHU002N06 — [18,26,27] MBDATA
R431 10K_4 R432 10K_4 R437 200_6 +3V
LM86VCC C455 .1U_4
H=1.75mm
U23 MAX6657 ADDRESS: 98H
SCLK SDA ALERT# OVERT# VCC DXP DXN GND
H_THERMDA H_THERMDC C454 2200P_4
R434 *10K_4 R435 *0_4 R438 10K_4 THERM_ALERT# R THER_SHD#
[16] THERM_ALERT#

<check list>
Layout Note:Routing 10:10 mils and away from noise source with ground gard

# CPU FAN

Q37 MMBT3904 — THER_SHD# — SYS_SHDN# [28]
R458 330_4 R1 10K_4 +3V
H=1.75mm
U26 G995 — VIN VO /FON GND VSET GND
C290 1U_4 +5V
[26] VFAN [26] FANSIG
TH_FAN_POWER
C489 10U_8 C491 .01U_4 C9 *.01U_4
CN34 PTI_CWY030-B0G1Z
FANPWR = 1.6*VSET

# PU/PD (ITP700)

+1.05V
XDP_TMS R7 39_4
XDP_TDI R6 150_4
XDP_TCK R5 27_4
XDP_TRST# R4 680_4

# Thermal Trip

+1.05V
Q1 FDV301N — [6,16,29] DELAY_VR_PWRGOOD
R23 *10K_4 D3 *BAS316 C35 *1U_6
R25 56.2_4 Q2 MMBT3904
THERMTRIP#_PWR — SYS_SHDN# [28]
R24 *0_4 PM_THRMTRIP# [6,14]

<CRB & Design guide>
Layout Note: Thermal trip should connect to ICH8 & GMCH without T-ing (ZS1 default NC)

Quanta Computer Inc.
PROJECT : BU1 Santa Rosa
Size | Document Number: CPU(1 of 2)/FAN/Thermal | Rev 3A
Date: Monday, March 26, 2007 | Sheet 3 of 33

# CPU(Power)

VCC_CORE

C465 C25 C466 C461 C473 C472 C477 C471 C21 C476 — 10U_8

C475 C469 C463 C474 C464 C19 C20 C23 C459 C460 — 10U_8

C31 C28 C470 C462 C30 C467 — 10U_8

DESIGN GUIDE
CHANGE FROM 22UF *20 TO 10UF *32

C468 C27 C458 C24 C26 C457 — 10U_8
CH6102K9A01
'CAP CHIP 10U 10V(+-10%,X5R,0805)'

C32 330U_7343
C13 *330U_7343
C29 330U_7343

<Check list>
Option1:330U*6(ESR=1.5m ohm aggregate , ESL=0.8nH/6) and 22U*20(ESR=3mohm typ/20 , ESL=0.6nH/20)
Option2:330U*6(ESR=1.5m ohm aggregate , ESL=1.8nH/6) and 22U*32(ESR=3mohm typ/32 , ESL=0.6nH/32)

U24C

VCC[001] A7, VCC[002] A9, VCC[003] A10, VCC[004] A12, VCC[005] A13, VCC[006] A15, VCC[007] A17, VCC[008] A18, VCC[009] A20, VCC[010] B7, VCC[011] B9, VCC[012] B10, VCC[013] B12, VCC[014] B14, VCC[015] B15, VCC[016] B17, VCC[017] B18, VCC[018] B20, VCC[019] C9, VCC[020] C10, VCC[021] C12, VCC[022] C13, VCC[023] C15, VCC[024] C17, VCC[025] C18, VCC[026] D9, VCC[027] D10, VCC[028] D12, VCC[029] D14, VCC[030] D15, VCC[031] D17, VCC[032] D18, VCC[033] E7, VCC[034] E9, VCC[035] E10, VCC[036] E12, VCC[037] E13, VCC[038] E15, VCC[039] E17, VCC[040] E18, VCC[041] E20, VCC[042] F7, VCC[043] F9, VCC[044] F10, VCC[045] F12, VCC[046] F14, VCC[047] F15, VCC[048] F17, VCC[049] F18, VCC[050] F20, VCC[051] AA7, VCC[052] AA9, VCC[053] AA10, VCC[054] AA12, VCC[055] AA13, VCC[056] AA15, VCC[057] AA17, VCC[058] AA18, VCC[059] AA20, VCC[060] AB9, VCC[061] AC10, VCC[062] AB10, VCC[063] AB12, VCC[064] AB14, VCC[065] AB15, VCC[066] AB17, VCC[067] AB18, VCC[068] AB20, VCC[069] AB7, VCC[070] AC7, VCC[071] AC9, VCC[072] AC12, VCC[073] AC13, VCC[074] AC15, VCC[075] AC17, VCC[076] AC18, VCC[077] AD7, VCC[078] AD9, VCC[079] AD10, VCC[080] AD12, VCC[081] AD14, VCC[082] AD15, VCC[083] AD17, VCC[084] AD18, VCC[085] AE9, VCC[086] AE10, VCC[087] AE12, VCC[088] AE13, VCC[089] AE15, VCC[090] AE17, VCC[091] AE18, VCC[092] AE20, VCC[093] AF9, VCC[094] AF10, VCC[095] AF12, VCC[096] AF14, VCC[097] AF15, VCC[098] AF17, VCC[099] AF18, VCC[100] AF20

VCCP[01] G21, VCCP[02] V6, VCCP[03] J6, VCCP[04] K6, VCCP[05] M6, VCCP[06] J21, VCCP[07] K21, VCCP[08] M21, VCCP[09] N21, VCCP[10] N6, VCCP[11] R21, VCCP[12] R6, VCCP[13] T21, VCCP[14] T6, VCCP[15] V21, VCCP[16] W21

VCCA[01] B26, VCCA[02] C26

VID[0] AD6, VID[1] AF5, VID[2] AE5, VID[3] AF4, VID[4] AE3, VID[5] AF3, VID[6] AE2

VCCSENSE AF7

VSSSENSE AE7

Merom Ball-out Rev 1a

CPU_G21
CPU_V6

<CRB>
R for test only

R15 0_4
R12 0_4

+VCCA_PROC

H_VID0 [29]
H_VID1 [29]
H_VID2 [29]
H_VID3 [29]
H_VID4 [29]
H_VID5 [29]
H_VID6 [29]

<REV.NO. 0.5/REF.NO.19343>

Ivcc Max 52A

Ivccp Max 6A(VCCP supply before Vcc stable)
Max 2A(VCCP supply after Vcc stable)

Ivcca Max 130mA

+1.05V

C16 C18 C17 C456 C15 C22 — .1U_6

+1.05V

C36 330U_7343

<Check list>
ESR=12m ohm

<CRB>
.01U near to B26 ball

+1.5V

R22 0_6

VCC_CORE

C33 .01U_4
C34 10U_8

R2 100/F_6

VCCSENSE [29]

VSSSENSE [29]

R3 100/F_6

<Demo board>
Routing 27.4ohm with 50mils spacing
PU/PD near to CPU 1"

U24D

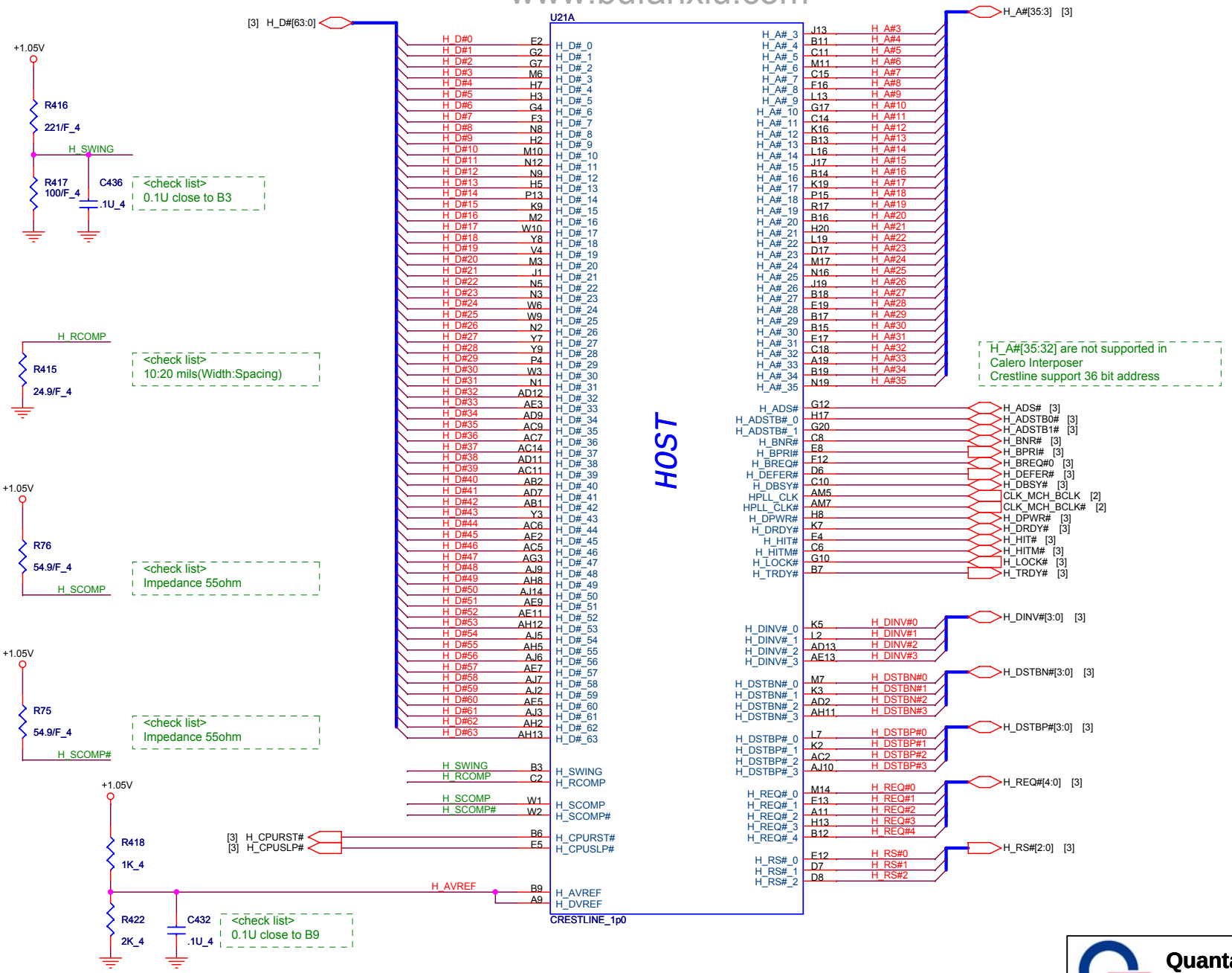
VSS[001] A4, VSS[002] A8, VSS[003] A11, VSS[004] A14, VSS[005] A16, VSS[006] A19, VSS[007] A23, VSS[008] AF2, VSS[009] B6, VSS[010] B8, VSS[011] B11, VSS[012] B13, VSS[013] B16, VSS[014] B19, VSS[015] B21, VSS[016] B24, VSS[017] C5, VSS[018] C8, VSS[019] C11, VSS[020] C14, VSS[021] C16, VSS[022] C19, VSS[023] C2, VSS[024] C22, VSS[025] C25, VSS[026] D1, VSS[027] D4, VSS[028] D8, VSS[029] D11, VSS[030] D13, VSS[031] D16, VSS[032] D19, VSS[033] D23, VSS[034] D26, VSS[035] E3, VSS[036] E6, VSS[037] E8, VSS[038] E11, VSS[039] E14, VSS[040] E16, VSS[041] E19, VSS[042] E21, VSS[043] E24, VSS[044] F5, VSS[045] F8, VSS[046] F11, VSS[047] F13, VSS[048] F16, VSS[049] F19, VSS[050] F2, VSS[051] F22, VSS[052] F25, VSS[053] G4, VSS[054] G1, VSS[055] G23, VSS[056] G26, VSS[057] H3, VSS[058] H6, VSS[059] H21, VSS[060] H24, VSS[061] J2, VSS[062] J5, VSS[063] J22, VSS[064] J25, VSS[065] K1, VSS[066] K4, VSS[067] K23, VSS[068] K26, VSS[069] L3, VSS[070] L6, VSS[071] L21, VSS[072] L24, VSS[073] M2, VSS[074] M5, VSS[075] M22, VSS[076] M25, VSS[077] N1, VSS[078] N4, VSS[079] N23, VSS[080] N26, VSS[081] P3, VSS[082] P6, VSS[083] P21, VSS[084] P24, VSS[085] R2, VSS[086] R5, VSS[087] R22, VSS[088] R25, VSS[089] T1, VSS[090] T4, VSS[091] T23, VSS[092] T26, VSS[093] U3, VSS[094] U6, VSS[095] U21, VSS[096] U24, VSS[097] V2, VSS[098] V5, VSS[099] V22, VSS[100] V25, VSS[101] W1, VSS[102] W4, VSS[103] W23, VSS[104] W26, VSS[105] Y3, VSS[106] Y6, VSS[107] Y21, VSS[108] Y24, VSS[109] AA2, VSS[110] AA5, VSS[111] AA8, VSS[112] AA11, VSS[113] AA14, VSS[114] AA16, VSS[115] AA19, VSS[116] AA22, VSS[117] AA25, VSS[118] AB1, VSS[119] AB4, VSS[120] AB8, VSS[121] AB11, VSS[122] AB13, VSS[123] AB16, VSS[124] AB19, VSS[125] AB23, VSS[126] AB26, VSS[127] AC3, VSS[128] AC6, VSS[129] AC8, VSS[130] AC11, VSS[131] AC14, VSS[132] AC16, VSS[133] AC19, VSS[134] AC21, VSS[135] AC24, VSS[136] AD2, VSS[137] AD5, VSS[138] AD8, VSS[139] AD11, VSS[140] AD13, VSS[141] AD16, VSS[142] AD19, VSS[143] AD22, VSS[144] AD25, VSS[145] AE1, VSS[146] AE4, VSS[147] AE8, VSS[148] AE11, VSS[149] AE14, VSS[150] AE16, VSS[151] AE19, VSS[152] AE23, VSS[153] AE26, VSS[154] A2, VSS[155] AF6, VSS[156] AF8, VSS[157] AF11, VSS[158] AF13, VSS[159] AF16, VSS[160] AF19, VSS[161] AF21, VSS[162] A25, VSS[163] AF25

Merom Ball-out Rev 1a

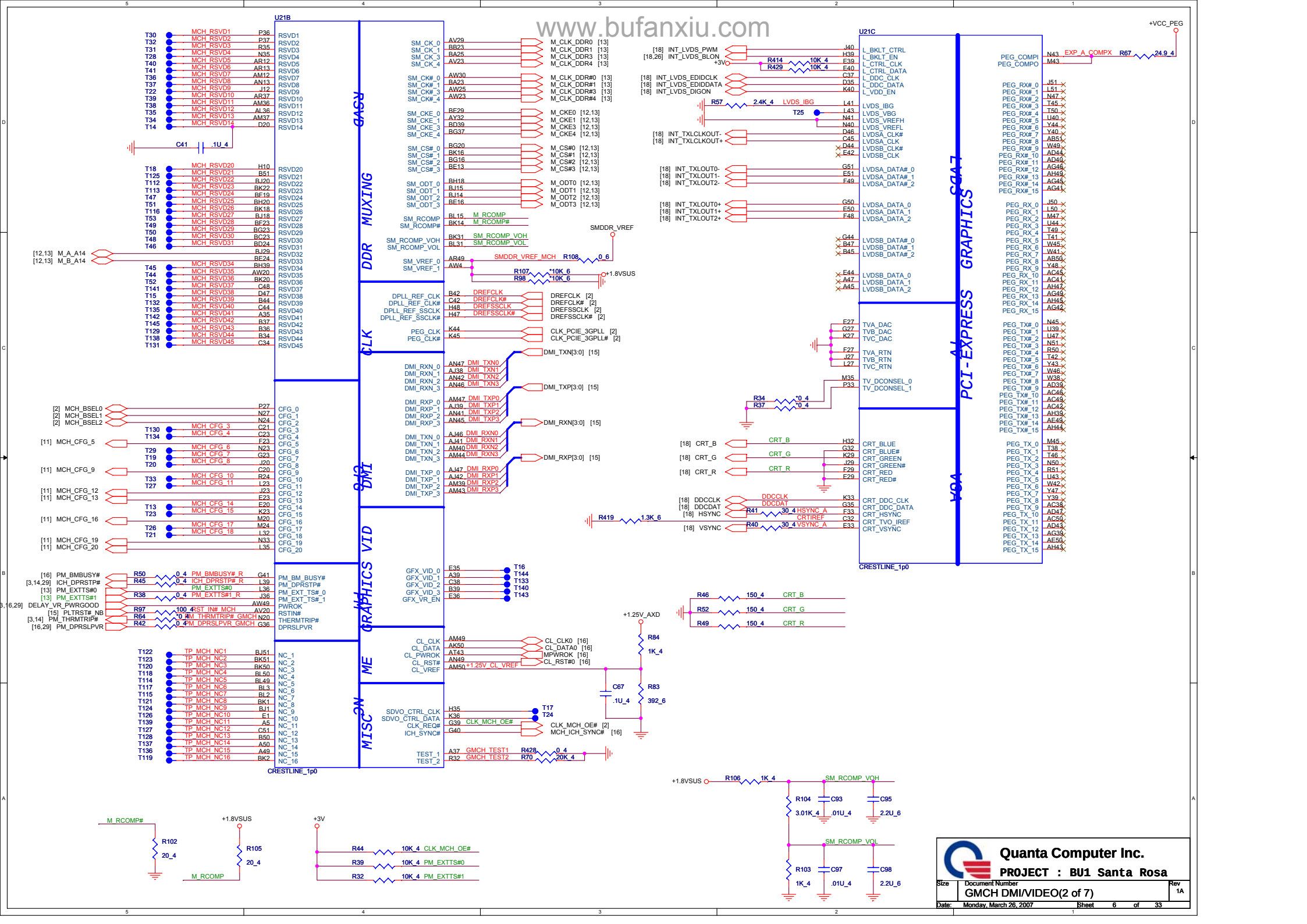
| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : BU1 Santa Rosa | | |
| Size | Document Number: CPU(2 of 2) | Rev: 1A |
| Date: Monday, March 26, 2007 | Sheet 4 of 33 | |

# NB(HOST)



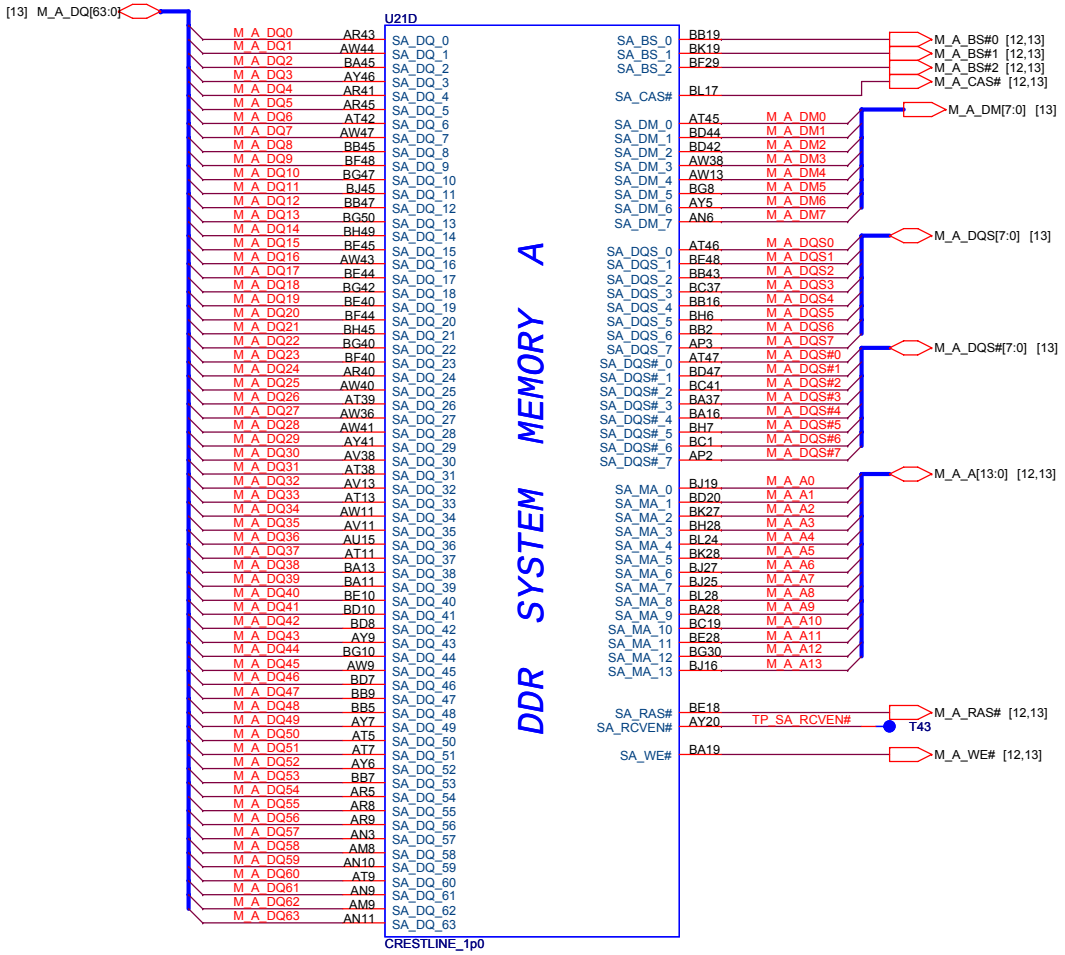


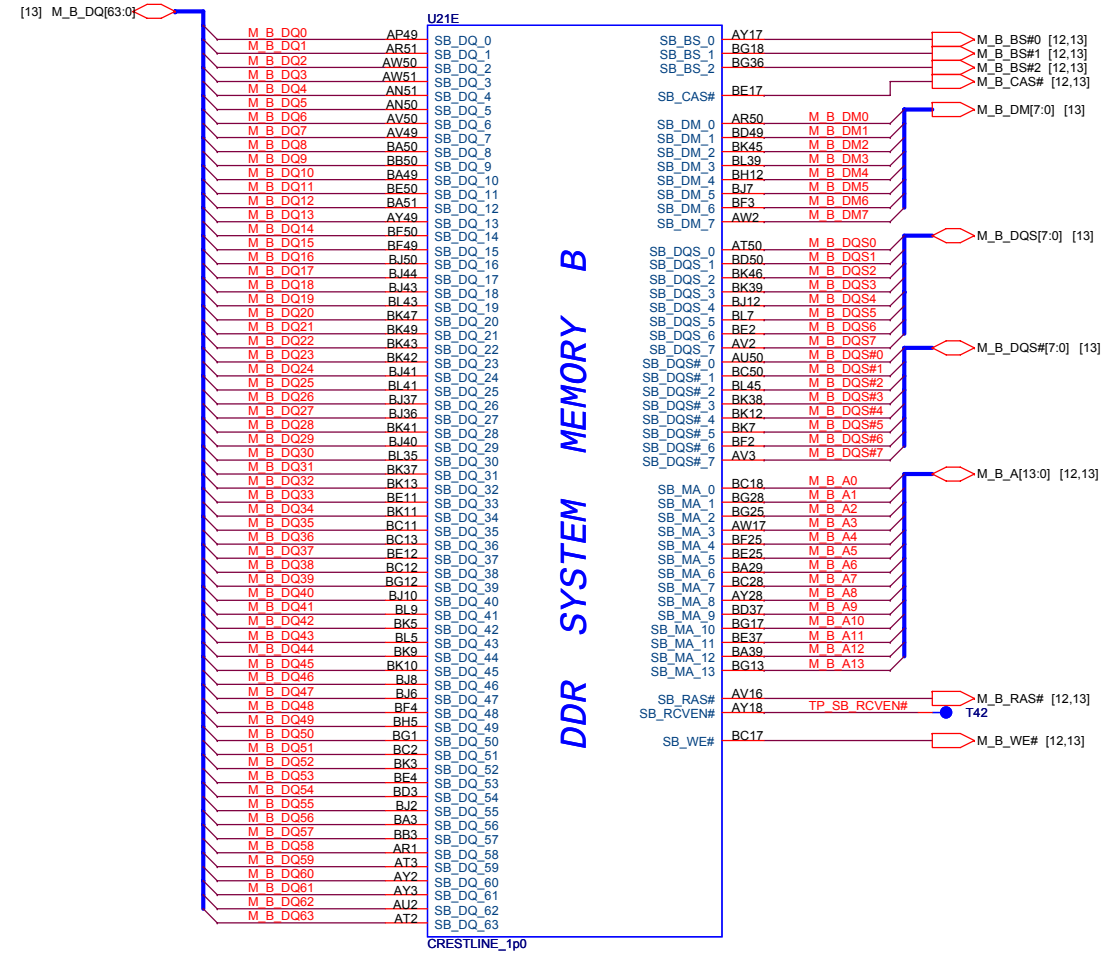

| | |
|---|---|
| Quanta Computer Inc. | |
| PROJECT : BU1 Santa Rosa | |
| Size | Document Number: GMCH HOST(1 of 7) — Rev: 1A |
| Date: Monday, March 26, 2007 | Sheet 5 of 33 |



# NB(Memory controller)



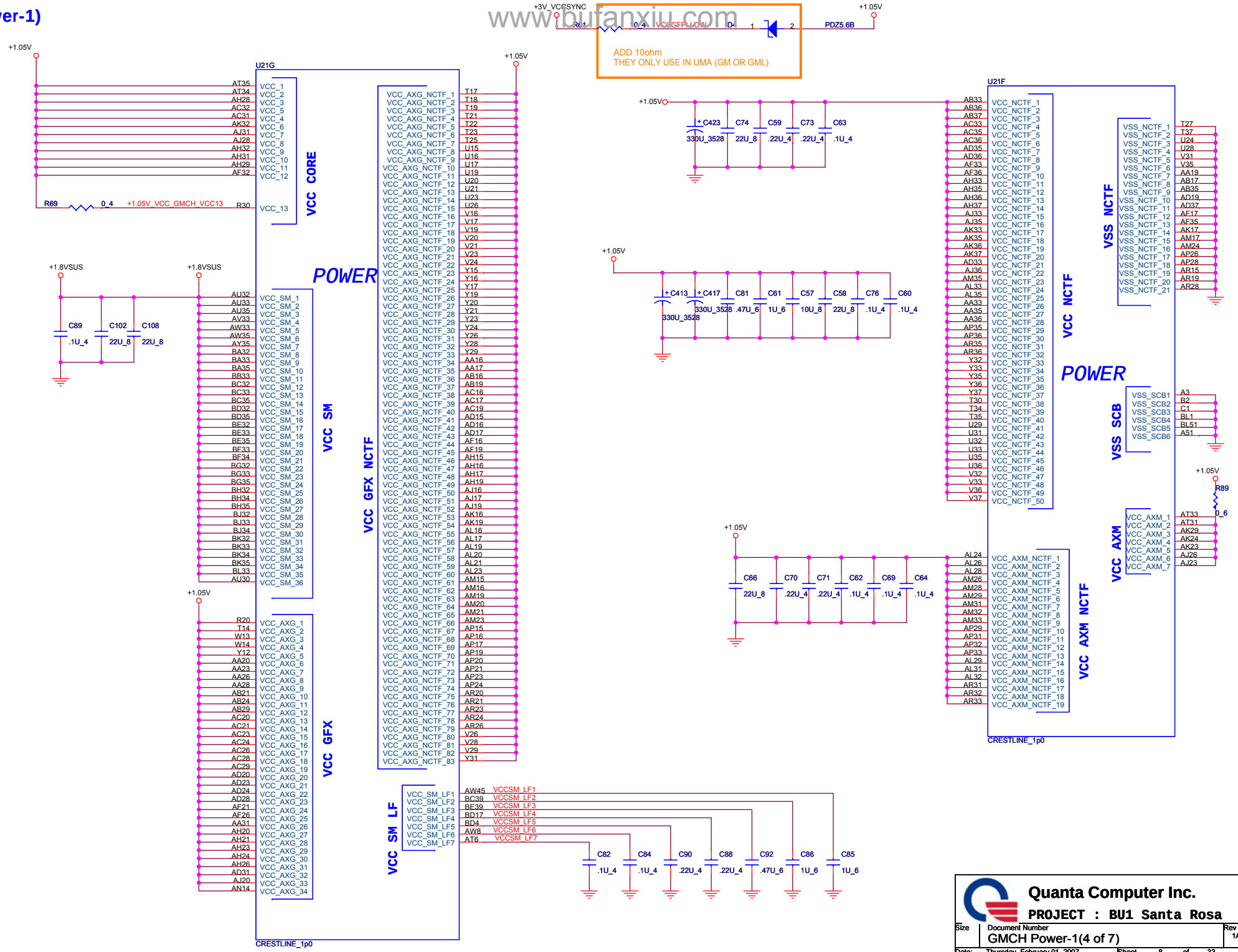



| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : BU1 Santa Rosa | | |
| Size | Document Number: MCH DDR(3 of 7) | Rev: 1A |
| Date: Monday, March 26, 2007 | Sheet 7 of 33 | |

# NB(Power-1)






Quanta Computer Inc.

PROJECT : BU1 Santa Rosa

| Size | Document Number | Rev |
|---|---|---|
| | GMCH Power-1(4 of 7) | 1A |
| Date: Thursday, February 01, 2007 | Sheet 8 of 33 | |

# NB(Power-2)



## CRT/TV Disable/Enable guideline

| Ball | Enable | Disable | Ball | Enable | Disable |
|---|---|---|---|---|---|
| VCCA_CRT | 3.3V | GND | VCCA_C_TVO | 3.3V | GND |
| VCCD_CRT | 1.5V | GND | VCCD_TVO | 1.5V | 1.5V |
| VCCDQ_CRT | 1.5V | GND | VCCABG_DAC | 3.3V | GND |
| VCCA_A_TVO | 3.3V | GND | VSSABG_DAC | GND | GND |
| VCCA_B_TVO | 3.3V | GND | VCC_SYNC | 3.3V | GND |

## LVDS Disable/Enable guideline

External VGA with EV@part,Internal VGA with IV@ part

| Signal | If SDVO Disable LVDS Disable | If SDVO enable LVDS Disable | If SDVO enable LVDS enable |
|---|---|---|---|
| VCCD_LVDS | GND | 1.8V | 1.8V |
| VCCA_LVDS | GND | GND | 1.8V |
| VCCTX_LVDS | GND | GND | 1.8V |
| | EXTERNAL | | INTERNAL |

'IND CHIP 10UH(20%,100MA,LB2012T100MR)'

'EMI FILTER BKP1608HS181-T(180,1.5A)'

<FAE>
INT VGA disable
VCCSYNC connect to GND

<FAE>
VCC_RXR_DMI and VCC_PEG
connect to+1.05V

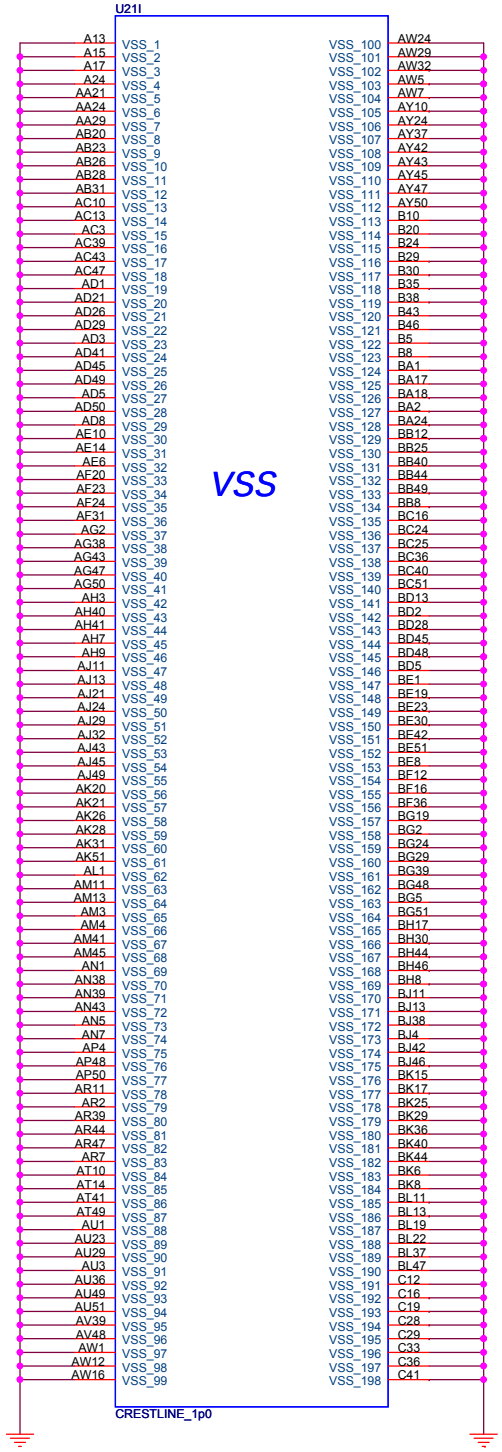
<CRB>
+1.25V AND +1.25M shall be
+1.5V for Calero Interposer

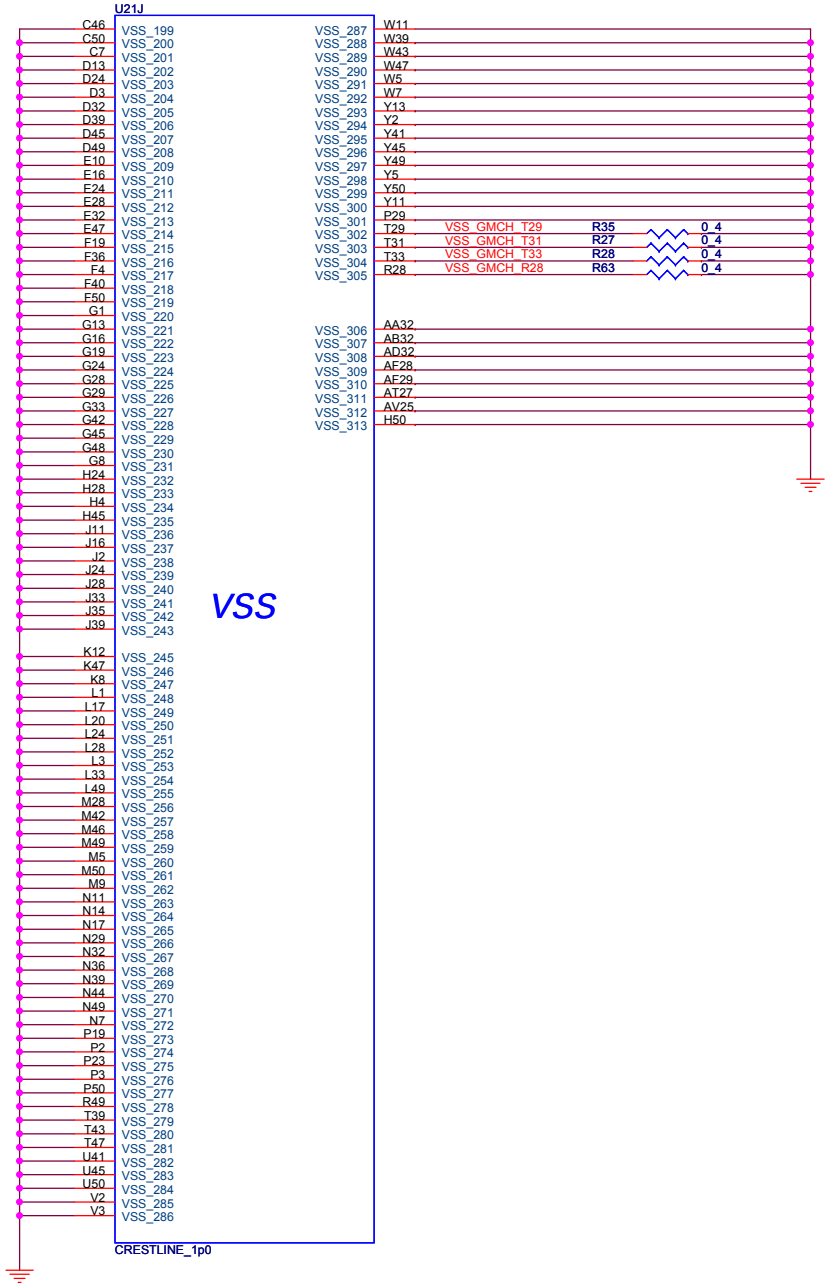
CRESTLINE_1p0

| | | | |
|---|---|---|---|
| Quanta Computer Inc. | | | |
| PROJECT : BU1 Santa Rosa | | | |
| Size | Document Number: GMCH Power-2(5 of 7) | | Rev: 1A |
| Date: Tuesday, February 06, 2007 | Sheet 9 of 33 | | |

# NB(Power-3)






| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : BU1 Santa Rosa | | |
| Size | Document Number: GMCH Power-3(6 of 7) | Rev: 1A |
| Date: Thursday, February 01, 2007 | Sheet 10 of 33 | |

# Strap table



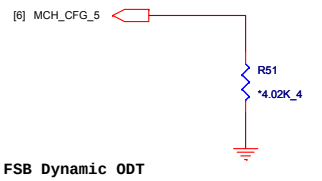
All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal

CFG[17:3] Have internal Pull-up
CFG[18:19] Have internal Pull-down
Any CFG signal strapping option not list below should be left NC Pin

| Pin Name | Strap description | Configuration |
|---|---|---|
| CFG[2:0] | FSB Frequency Select | 010 = FSB 800MHz<br>011 = FSB 667MHz |
| CFG[4:3] | Reserved | |
| CFG5 | DMI X2 Select | 0 = DMI X2<br>1 = DMI X4(Default) |
| CFG6 | Reserved | |
| CFG7 | CPU Strap | 0 = Reserved<br>1 = Mobile CPU(Default) |
| CFG8 | Low power PCI Express | 0 = Normal mode<br>1 = Low Power mode |
| CFG9 | PCI Express Graphics Lane Reversal | 0 = Reverse Lanes<br>1 = Normal operation(Default) |
| CFG[11:10] | Reserved | |
| CFG[13:12] | XOR/ALLZ | 00 = Reserved<br>01 = XOR Mode Enable<br>10 = All-Z Mode Enabled<br>11 = Normal operation(Default) |
| CFG[15:14] | Reserved | |
| CFG16 | FSB Dynamic ODT | 0 = Dynamic ODT disable<br>1 = Dynamic ODT Enable(Default) |
| CFG[18:17] | Reserved | |
| SDVO_CTRLDATA | SDVO Present | 0 = No SDVO Card present(Default)<br>1 = SDVO Card Present |
| CFG19 | DMI Lane Reversal | 0 = Normal operation(Default)<br>1 = Reverse Lanes |
| CFG20 | SDVO/PCIe concurrent | 0 = Only SDVO or PCIE x1 is operation(Default)<br>1 = SDVO and PCIE x1 are operating simultaneously via the PEG port |

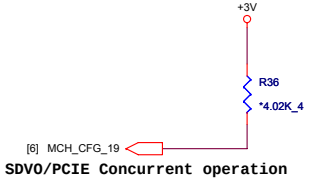
**DMI X2 Select**

| | |
|---|---|
| MCH_CFG_5 | Low = DMIX2<br>High = IDMIX4(Default) |




**DMI Lane Reversal**

| | |
|---|---|
| MCH_CFG_19 | Low = Normal operation(Default)<br>High = Reverse Lane |

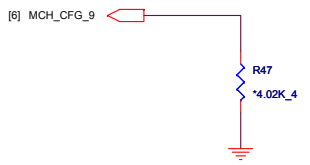



**XOR /ALLz /Clock Un-gating**

| MCH_CFG_12 | MCH_CFG_13 | Configuration |
|---|---|---|
| 0 | 0 | Clock gating disable |
| 0 | 1 | XOR Mode Enable |
| 1 | 0 | ALL-z Mode Enable |
| 1 | 1 | Normal operation(Default) |

**PCI Express Graphics**

| | |
|---|---|
| MCH_CFG_9 | Low = Reverse Lane<br>High = Normal operation(Default) |

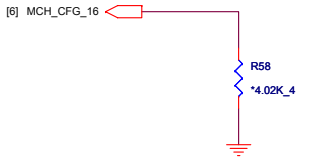



**SDVO Present**

Strap define at External DVI control page

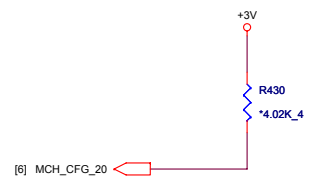
**FSB Dynamic ODT**

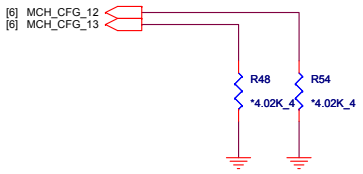
| | |
|---|---|
| MCH_CFG_16 | Low = ODT Disable<br>High = ODT Enable(Default) |




**SDVO/PCIE Concurrent operation**

| | |
|---|---|
| MCH_CFG_20 | Low = Only SDVO or PCIE X1 is operational(Default)<br>High = SDVO andPCIE X1 are operating simultaneously via the PEG port |




Quanta Computer Inc.

PROJECT : BU1 Santa Rosa

| Size | Document Number | Rev |
|---|---|---|
| | GMCH Strap(7 of 7) | 1A |

Date: Monday, March 26, 2007 Sheet 11 of 33

# DDR2 Dual channel A/B PU



M_A_A[13..0] → M_A_A[13..0] [7,13]

M_B_A[13..0] → M_B_A[13..0] [7,13]

## DDRII A CHANNEL

SMDDR_VTERM

C176 .1U_4, C145 .1U_4, C143 .1U_4, C148 .1U_4, C195 .1U_4, C146 .1U_4, C230 .1U_4, C201 .1U_4, C228 .1U_4, C227 .1U_4, C142 .1U_4, C173 .1U_4, C200 .1U_4

## DDRII B CHANNEL

SMDDR_VTERM

C174 .1U_4, C172 .1U_4, C177 .1U_4, C175 .1U_4, C231 .1U_4, C196 .1U_4, C197 .1U_4, C199 .1U_4, C171 .1U_4, C144 .1U_4, C226 .1U_4, C147 .1U_4, C225 .1U_4

Place one cap close to every 2 pull-up resistor terminated to SMDDR_VTERM

| | | | |
|---|---|---|---|
| M_A_A3 / M_A_A1 | RP16 | 56X2 | SMDDR_VTERM |
| M_A_A9 / M_A_A5 | RP18 | 56X2 | SMDDR_VTERM |
| M_A_A2 / M_A_A4 | RP21 | 56X2 | SMDDR_VTERM |
| M_A_A11 / [6,13] M_CKE1 | RP23 | 56X2 | SMDDR_VTERM |
| [6,13] M_CKE0 / M_A_A8 | RP19 | 56X2 | SMDDR_VTERM |
| M_A_A12 / [7,13] M_A_BS#2 | RP20 | 56X2 | SMDDR_VTERM |
| [7,13] M_A_BS#1 / M_A_A0 | RP25 | 56X2 | SMDDR_VTERM |

| | | | |
|---|---|---|---|
| M_B_A10 / [7,13] M_B_WE# | RP30 | 56X2 | SMDDR_VTERM |
| M_B_A3 / M_B_A1 | RP31 | 56X2 | SMDDR_VTERM |
| [7,13] M_B_BS#1 / M_B_A0 | RP38 | 56X2 | SMDDR_VTERM |
| M_B_A7 / M_B_A11 | RP35 | 56X2 | SMDDR_VTERM |
| M_B_A8 / M_B_A5 | RP27 | 56X2 | SMDDR_VTERM |
| M_B_A2 / M_B_A4 | RP34 | 56X2 | SMDDR_VTERM |
| M_B_A9 / M_B_A12 | RP28 | 56X2 | SMDDR_VTERM |

| | | | |
|---|---|---|---|
| M_A_A7 / M_A_A6 | RP22 | 56X2 | SMDDR_VTERM |
| [6,13] M_CKE3 / [7,13] M_B_BS#2 | RP32 | 56X2 | SMDDR_VTERM |
| [6,13] M_ODT1 / [6,13] M_CS#1 | RP14 | 56X2 | SMDDR_VTERM |
| [6,13] M_ODT3 / [7,13] M_B_BS#0 | RP33 | 56X2 | SMDDR_VTERM |
| M_A_A10 / [7,13] M_A_BS#0 | RP17 | 56X2 | SMDDR_VTERM |
| [7,13] M_A_CAS# / [7,13] M_A_WE# | RP15 | 56X2 | SMDDR_VTERM |
| [6,13] M_CS#0 / [7,13] M_A_RAS# | RP26 | 56X2 | SMDDR_VTERM |
| [7,13] M_B_CAS# / [6,13] M_CS#3 | RP29 | 56X2 | SMDDR_VTERM |
| M_B_A6 / [6,13] M_CKE4 | RP39 | 56X2 | SMDDR_VTERM |
| [6,13] M_ODT2 / [7,13] M_B_RAS# | RP37 | 56X2 | SMDDR_VTERM |
| [6,13] M_ODT0 / M_A_A13 | RP24 | 56X2 | SMDDR_VTERM |
| M_B_A13 / [6,13] M_CS#2 | RP36 | 56X2 | SMDDR_VTERM |

INTEL FAE (08/17)
ADD MA14 FOR DUAL LAYERS RAM

[6,13] M_A_A14 / [6,13] M_B_A14 — R199 / R219 56_4 / 56_4 — SMDDR_VTERM

Quanta Computer Inc.
PROJECT : BU1 Santa Rosa

| Size | Document Number | Rev |
|---|---|---|
| | DDR RES. ARRAY | 1A |

Date: Monday, March 26, 2007 Sheet 12 of 33

# DDR2 Dual channel A/B CONN



PC4800 DDR2 SDRAM SO-DIMM (200P)

CN30

TYCO_1-1734071-1

SMDDR_VREF_DIMM

+1.8VSUS

+3V

M_A_DM[0..7] [7]
M_A_DQ[0..63] [7]
M_A_DQS[0..7] [7]
M_A_DQS#[0..7] [7]
M_A_A[0..13] [7,12]

M_CLK_DDR0 [6]
M_CLK_DDR0# [6]
M_CLK_DDR1 [6]
M_CLK_DDR1# [6]

PM_EXTTS#0 [6]

M_CKE0 [6,12]
M_CKE1 [6,12]

M_A_BS#2 [7,12]
M_A_A14 [6,12]

M_A_BS#1 [7,12]
M_A_RAS# [7,12]
M_CS#0 [6,12]
M_ODT0 [6,12]
M_A_A13

M_A_BS#0 [7,12]
M_A_WE# [7,12]
M_A_CAS# [7,12]
M_CS#1 [6,12]
M_ODT1 [6,12]

DDRDAT_SMB
DDRCLK_SMB

R202 10K_4
R201 10K_4

SO-DIMM0 SPD Address is 0xA0
SO-DIMM0 TS Address is 0x30

INTEL FAE (08/17)
ADD MA14 FOR DUAL LAYERS RAM

**H: 5.6mm**

CLOCK 0,1
CKE 0,1

PC4800 DDR2 SDRAM SO-DIMM (200P)

CN25

TYCO_292564-4

SMDDR_VREF_DIMM

+1.8VSUS

+3V

M_B_DM[0..7] [7]
M_B_DQ[0..63] [7]
M_B_DQS[0..7] [7]
M_B_DQS#[0..7] [7]
M_B_A[0..13] [7,12]

M_CLK_DDR3 [6]
M_CLK_DDR3# [6]
M_CLK_DDR4 [6]
M_CLK_DDR4# [6]

PM_EXTTS#1 [6]

M_CKE3 [6,12]
M_CKE4 [6,12]

M_B_BS#2 [7,12]
M_B_A14 [6,12]

M_B_BS#1 [7,12]
M_B_RAS# [7,12]
M_CS#2 [6,12]
M_ODT2 [6,12]
M_B_A13

M_B_BS#0 [7,12]
M_B_WE# [7,12]
M_B_CAS# [7,12]
M_CS#3 [6,12]
M_ODT3 [6,12]

DDRDAT_SMB
DDRCLK_SMB

R217 10K_4
R216 10K_4

SO-DIMM1 SPD Address is 0xA4
SO-DIMM1 TS Address is 0x34

INTEL FAE (08/17)
ADD MA14 FOR DUAL LAYERS RAM

**H: 10.1mm**

CLOCK 3,4
CKE 2,3

+1.8VSUS

C370 330U_3528
C376 2.2U_6
C379 2.2U_6
C367 2.2U_6
C368 2.2U_6
C380 2.2U_6

C185 .1U_4
C183 .1U_4
C369 .1U_4
C182 .1U_4

SMDDR_VREF_DIMM

C202 .1U_4
C198 2.2U_6
C141 2.2U_6
C150 .1U_4

+3V

Close to DIMM0

C364 330U_3528
C375 2.2U_6
C365 2.2U_6
C377 2.2U_6
C366 2.2U_6
C378 2.2U_6

C184 .1U_4
C187 .1U_4
C181 .1U_4
C186 .1U_4
C149 .1U_4
C140 2.2U_6
C193 2.2U_6
C194 .1U_4

Close to DIMM1

Q9 RHU002N06
R225 10K_4
R224 10K_4

[2,16,19,23,24] SDATA
DDRDAT_SMB

Q8 RHU002N06

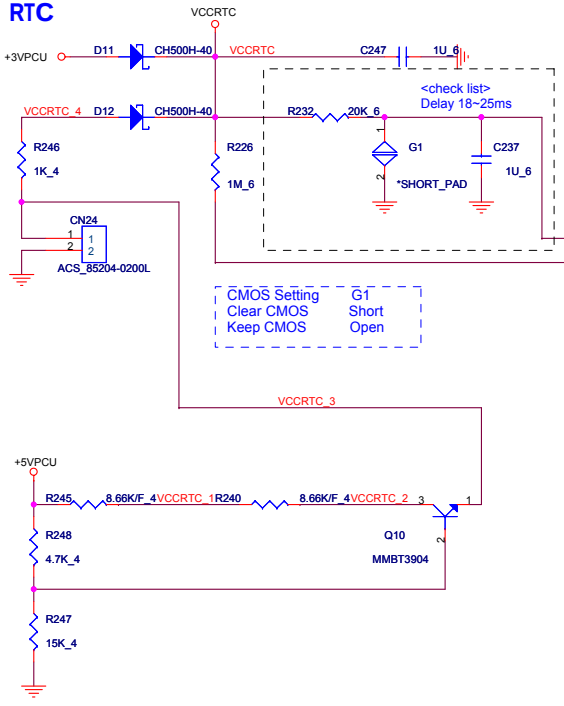
[2,16,19,23,24] SCLK
DDRCLK_SMB

R208 0_6
SMDDR_VREF

R209 *10K_4
R117 *10K_4
+1.8VSUS

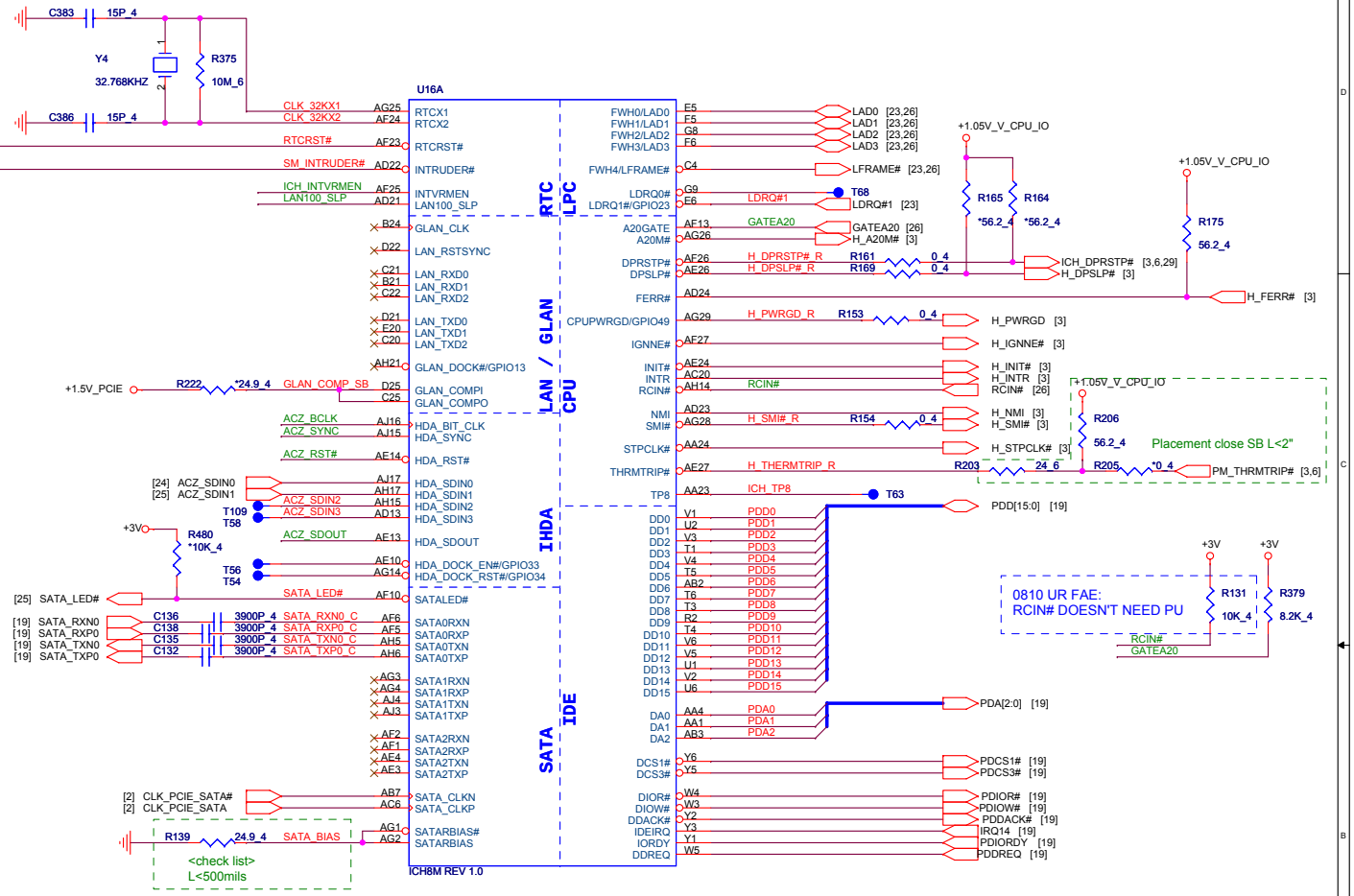
| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : BU1 Santa Rosa | | |
| Size | Document Number: DDR SO-DIMM(200P) | Rev: 3A |
| Date: Monday, March 26, 2007 | Sheet 13 of 33 | |

## RTC




## SATA Disable

1.Connect to GND: SATA[2:0]RXp/n , SATARBIAS , SATARBIAS# , SATA_CLKP , SATACLKN
2.NC: SATA[2:0]TXp/n , SATALED#
3.VccSATAPLL should be connected directly to Vcc1_5,Filter cap are not required
4.BIOS disable




## SB Strap

**ICH8-M Internal VR Enable strap**
**(Internal VR for Vccsus1_05,VccSus1_5 and VccCL1_5)**

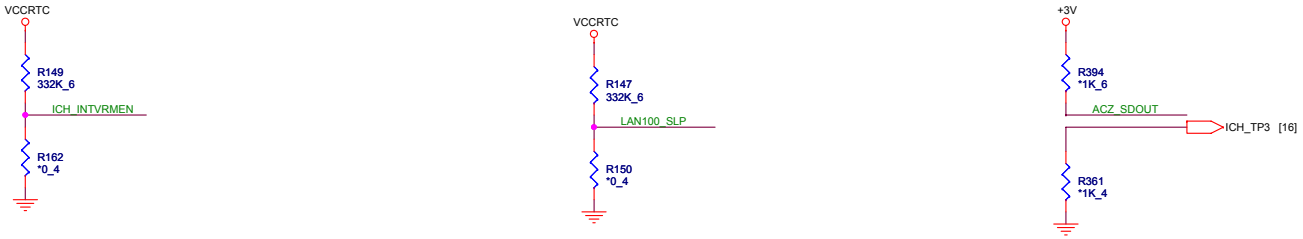
| | |
|---|---|
| INTVRMEN | Low = Internal VR disable<br>High = Internal VR enable(Default) |

**ICH8-M LAN100_SLP Strap**
**(Internal VR for VccLAN1_05 and VccCL1.05)**

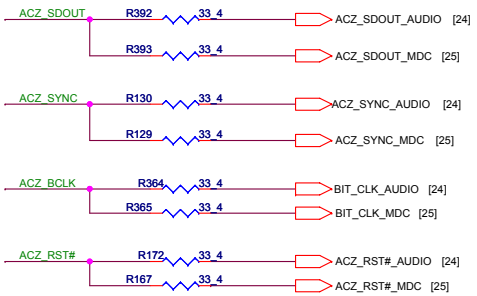
| | |
|---|---|
| LAN100_SLP | Low = Internal VR disable<br>High = Internal VR enable(Default) |

**XOR Chain Entrance Strap**

| ICH_RSV0 | HDA_SDOUT | Description |
|---|---|---|
| 0 | 0 | RSVD |
| 0 | 1 | Enter XOR Chain |
| 1 | 0 | Normal opration(Default) |
| 1 | 1 | Set PCIE port config bit 1 |



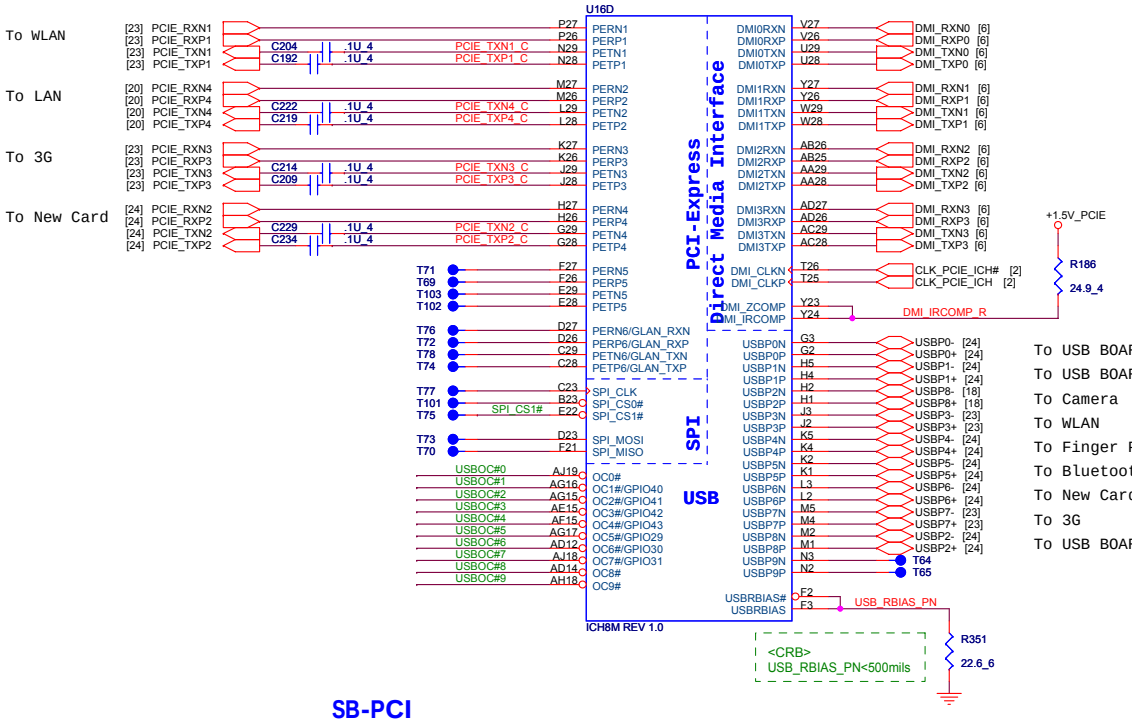

## HDA




Quanta Computer Inc.
PROJECT : BU1 Santa Rosa

| Size | Document Number | Rev |
|---|---|---|
| | ICH8M HOST(1 of 4) | 2A |
| Date: Tuesday, March 27, 2007 | Sheet 14 of 33 | |

## SB-PCIE/USB/DMI




### A16 SWAP Override strap

| PCI_GNT#3 | Low = A16 swap override enabled<br>High = Default |
|---|---|

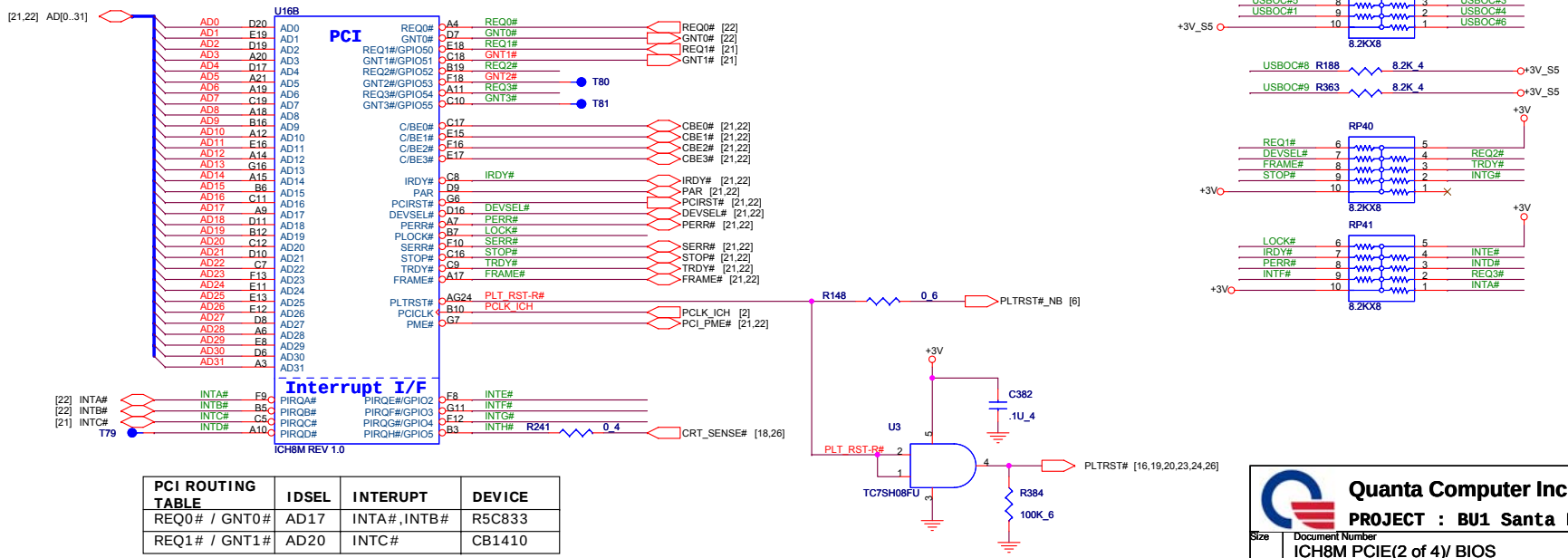
GNT3# R227 *1K_4

### ICH8 Boot BIOS select

| PCI_GNT#0 | SPI_CS#1 | Boot BIOS Location |
|---|---|---|
| 0 | 1 | SPI(Default) |
| 1 | 0 | PCI |
| 1 | 1 | LPC |

SPI_CS1# R220 *1K_4
GNT0# R223 *1K_4

## SB-PCI




| PCI ROUTING TABLE | IDSEL | INTERUPT | DEVICE |
|---|---|---|---|
| REQ0# / GNT0# | AD17 | INTA#,INTB# | R5C833 |
| REQ1# / GNT1# | AD20 | INTC# | CB1410 |

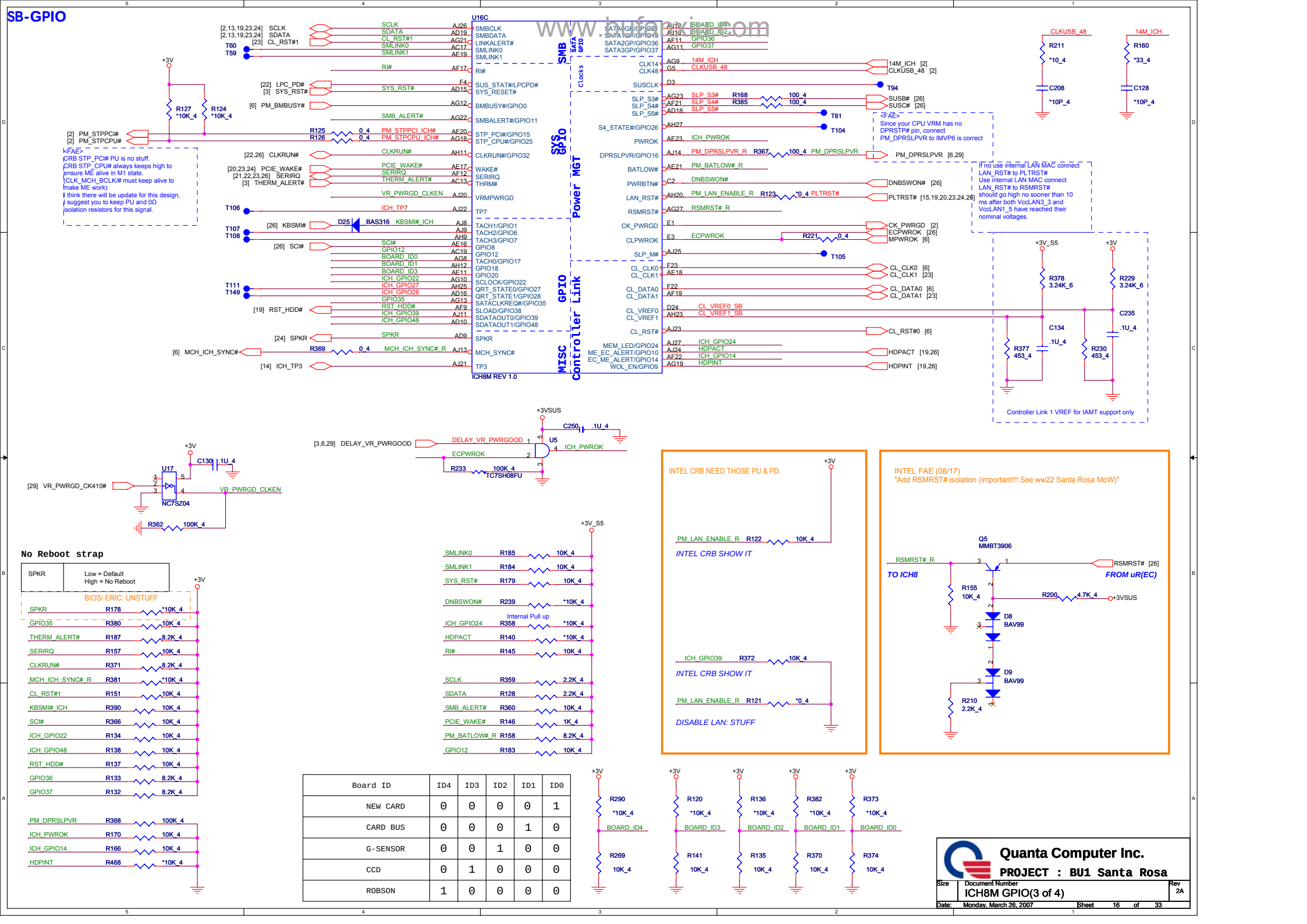



Quanta Computer Inc.
PROJECT : BU1 Santa Rosa

| Size | Document Number | Rev |
|---|---|---|
| | ICH8M PCIE(2 of 4)/ BIOS | 1A |

Date: Monday, March 26, 2007 Sheet 15 of 33

# SB-GPIO










**No Reboot strap**

| SPKR | Low = Default<br>High = No Reboot |
|---|---|

BIOS/ ERIC: UNSTUFF













| Board ID | ID4 | ID3 | ID2 | ID1 | ID0 |
|---|---|---|---|---|---|
| NEW CARD | 0 | 0 | 0 | 0 | 1 |
| CARD BUS | 0 | 0 | 0 | 1 | 0 |
| G-SENSOR | 0 | 0 | 1 | 0 | 0 |
| CCD | 0 | 1 | 0 | 0 | 0 |
| ROBSON | 1 | 0 | 0 | 0 | 0 |

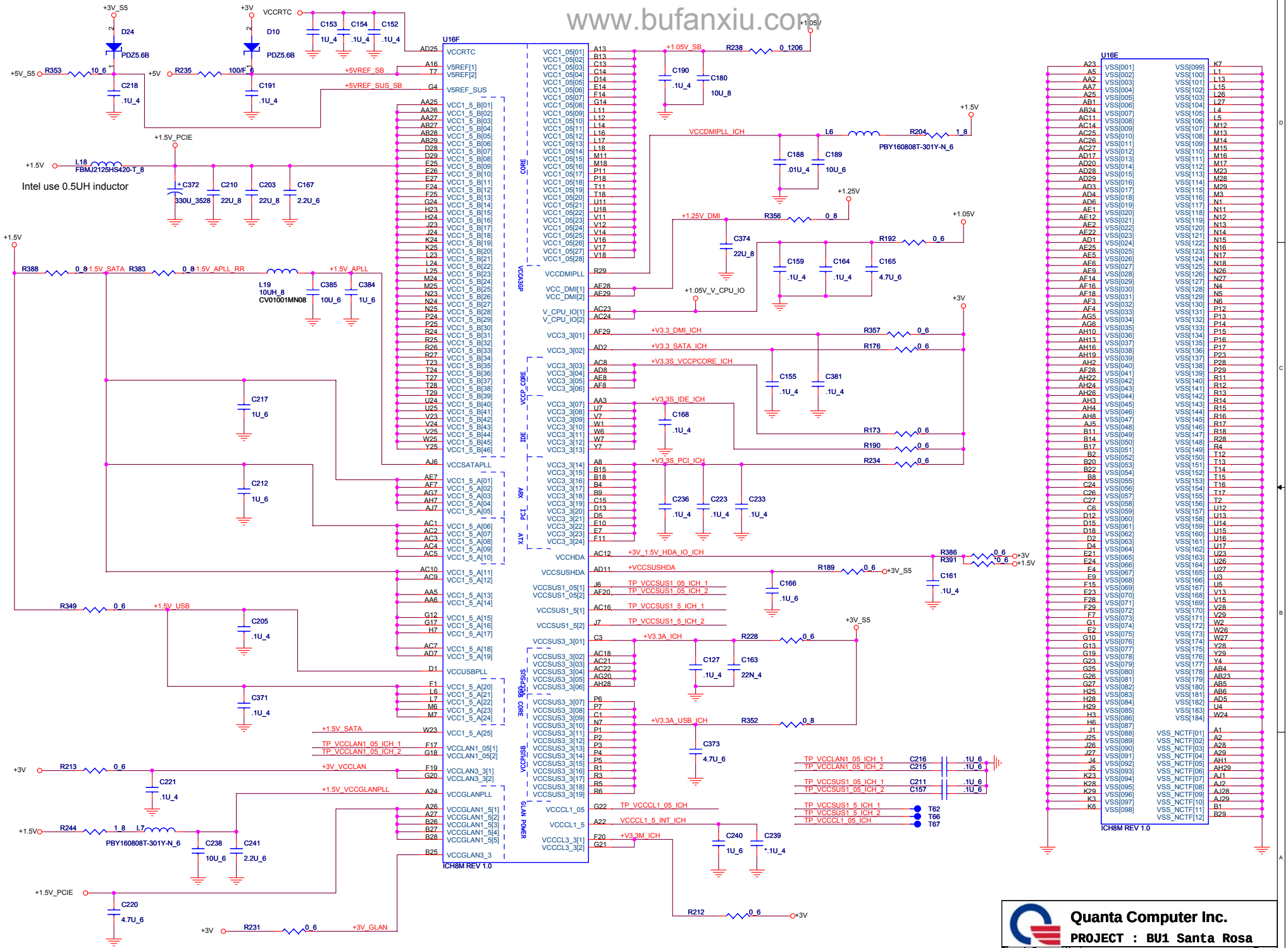



Quanta Computer Inc.

PROJECT : BU1 Santa Rosa

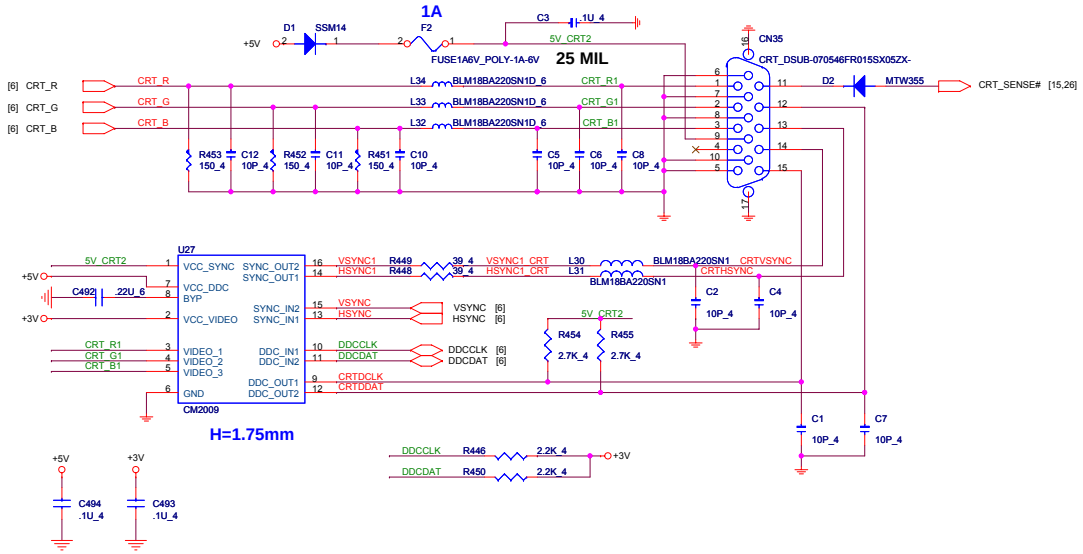
| Size | Document Number | Rev |
|---|---|---|
| | ICH8M GPIO(3 of 4) | 2A |

Date: Monday, March 26, 2007 Sheet 16 of 33

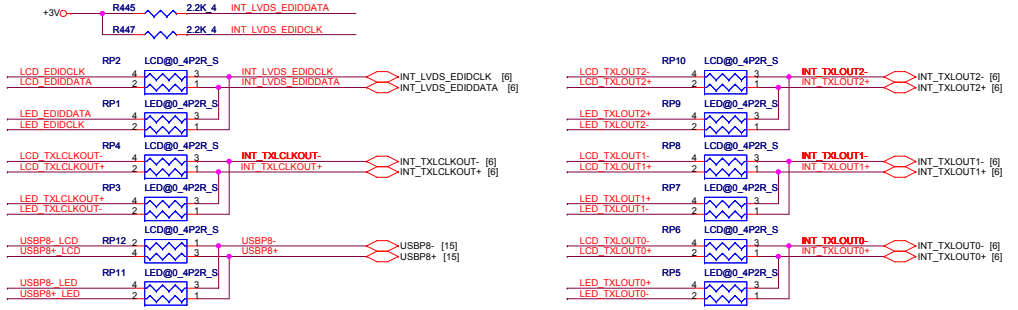


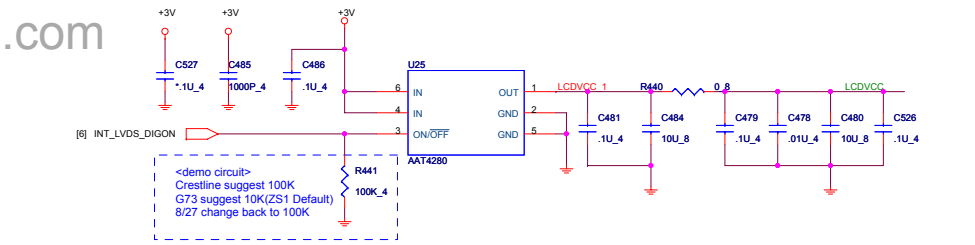

| | | | |
|---|---|---|---|
| Quanta Computer Inc. | | | |
| PROJECT : BU1 Santa Rosa | | | |
| Size | Document Number | | Rev |
| | ICH8M Power(4 of 4) | | 3A |
| Date: Tuesday, March 27, 2007 | Sheet 17 of 33 | | |

# CRT PORT

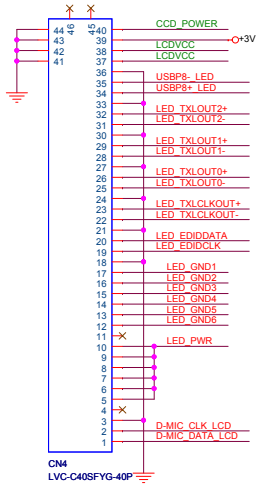



# LCD/LED TYPE CONNECTOR

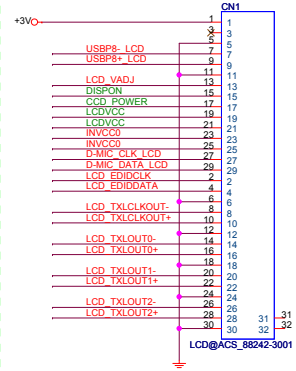


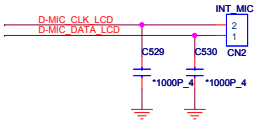

# TOSHIBA LED PANEL MODULE

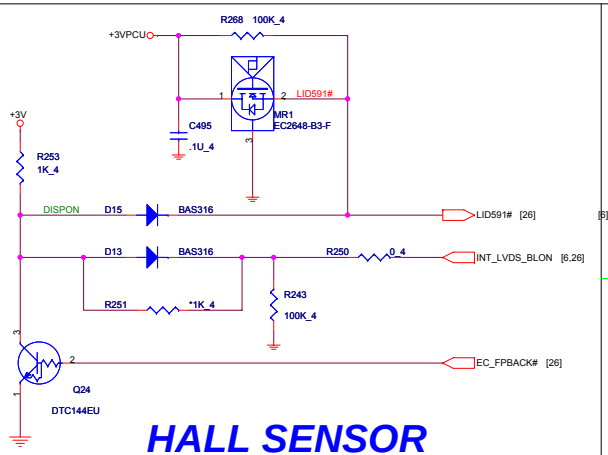



# CHI MEI LED PANEL MODULE

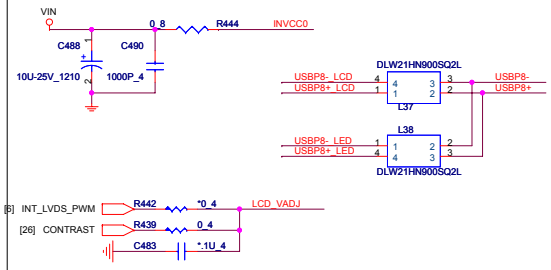


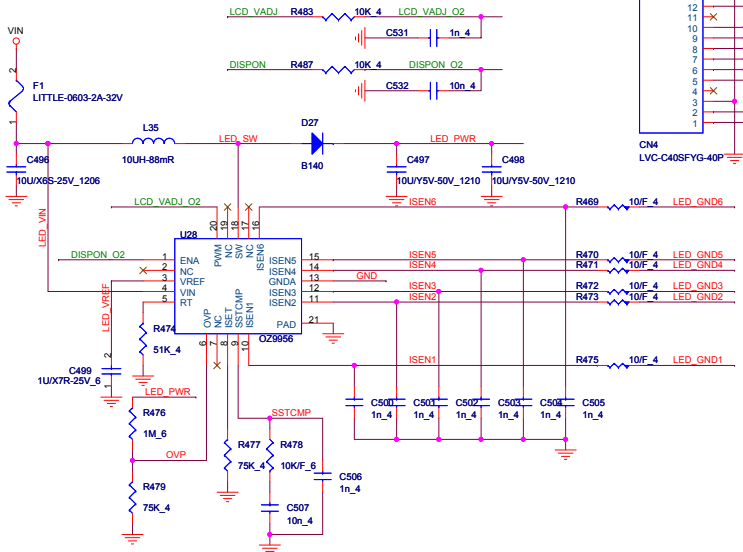

# LCD PANEL MODULE



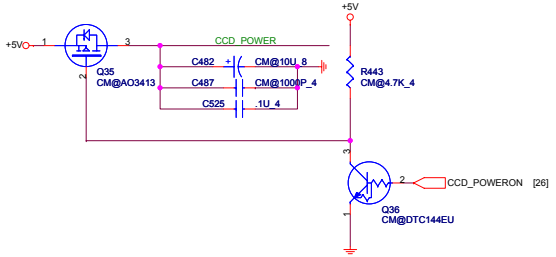




# HALL SENSOR




# CAMERA MODULE

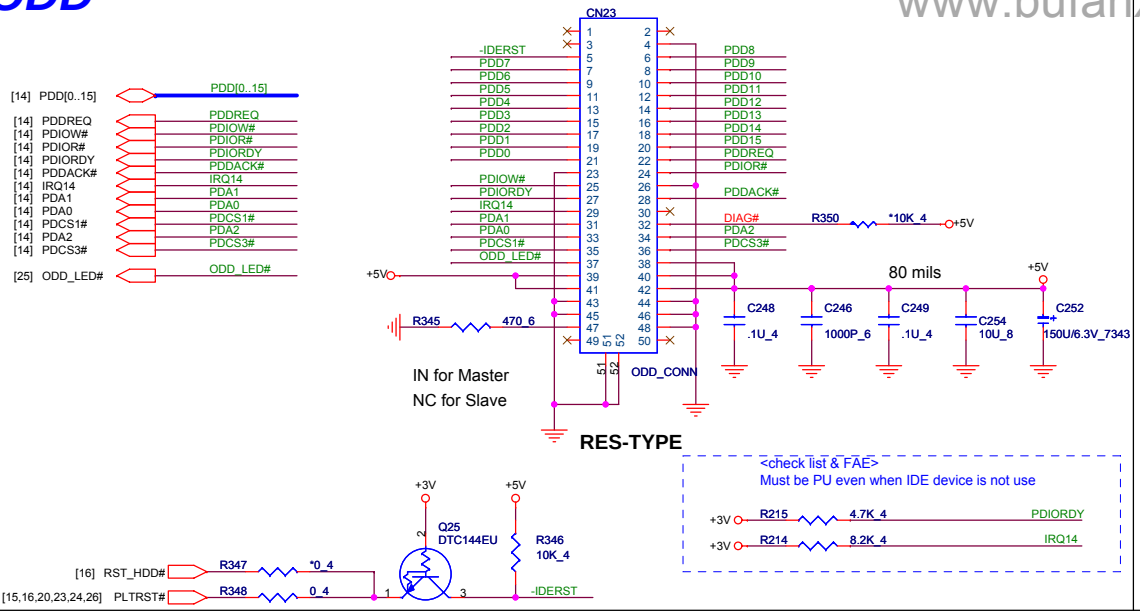



Quanta Computer Inc.

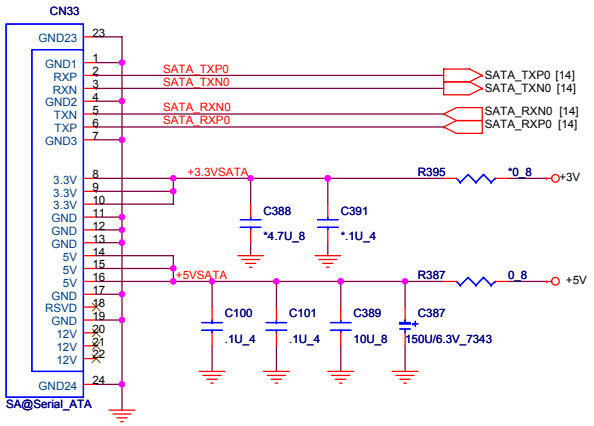
PROJECT : BU1 Santa Rosa

| Size | Document Number | Rev |
|---|---|---|
| | LCD/CRT/LID/CAMERA | 3A |
| Date: Sunday, April 01, 2007 | Sheet 18 of 33 | |

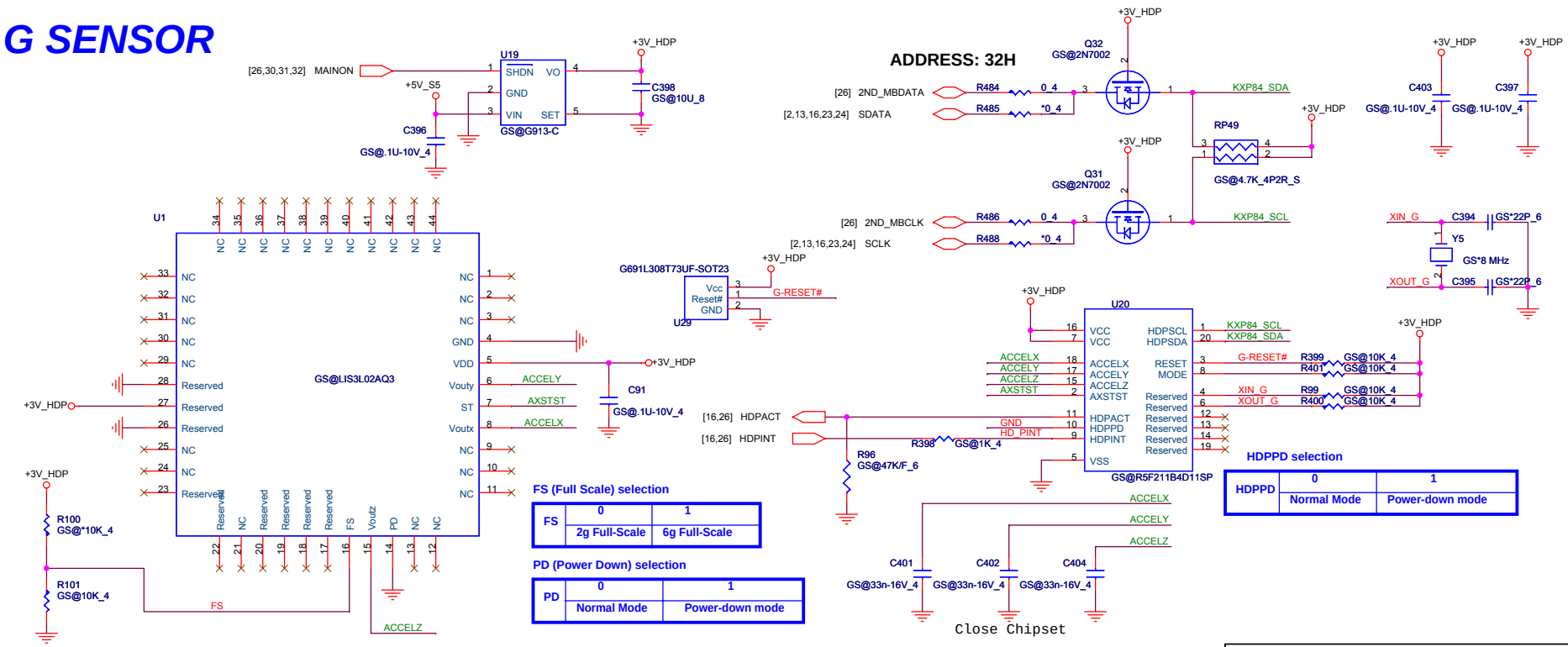
# ODD




# SATA HDD




# G SENSOR

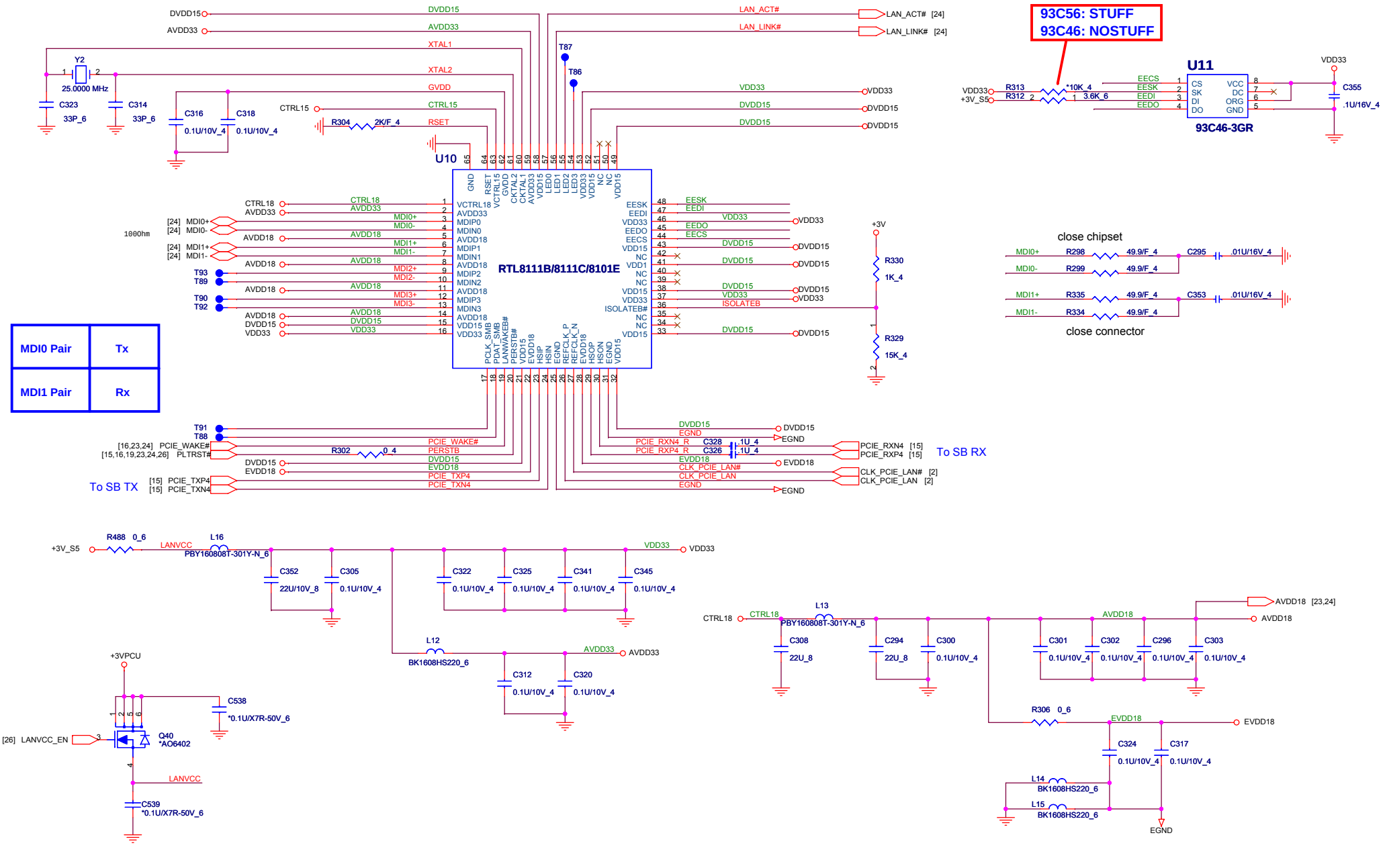


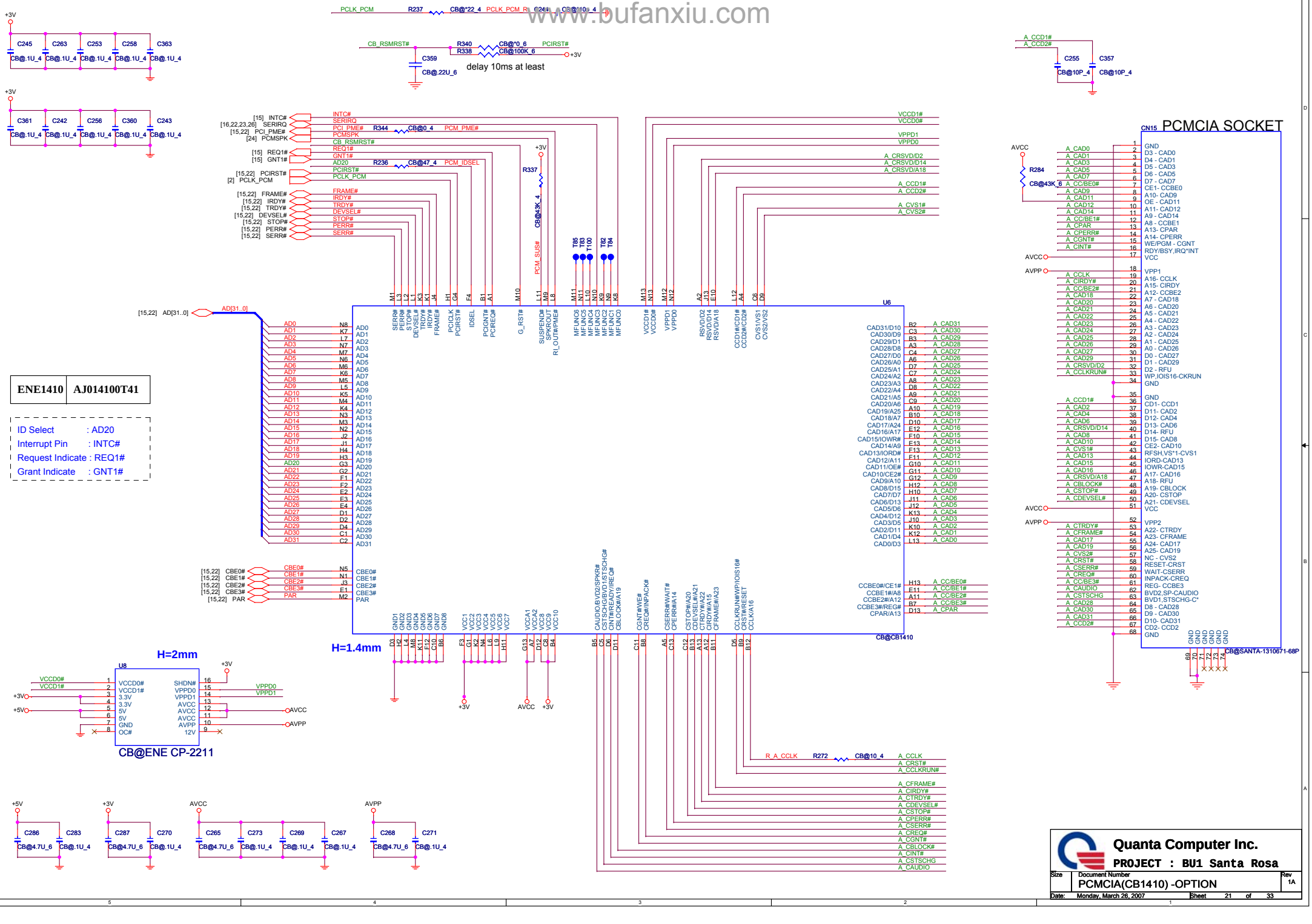

Quanta Computer Inc.

PROJECT : BU1 Santa Rosa

| Size | Document Number | Rev |
|---|---|---|
| | PATA/ODD/G SENSOR | 2A |

Date: Monday, March 26, 2007 Sheet 19 of 33





# R5C832 : AJ5C8320H26
# R5C833 : AJ5C8330H05

## 5 IN 1 CARD READER

## CARDREADER POWER

## 1394

## EEPROM

Reserve MS DUO card issue (For A-test only)

PCI / OTHER

IEEE1394/SD

PowerOnReset for Vcc

When GRESET# is controlled by system, the pull-up resistor and capacitor do not need to apply.

REQ0# AD17
GNT0# INTA#,B#

If VCC_3V tied to +3V, PME# function is not supported

When HWSPND# is controlled by system, the pull-up resistor(R4059) dose not need to apply.

Default setting:
INTA# is assert to 1394
INTB# is assert to Cardreader

22ohm/1A

AS CLOSE AS POSSIBLE TO R5C833 and GUARD GND

24.576MHz Y1 better than 50ppm

R5C832 stuff only

H=1.2mm

H=1.4mm

AS CLOSE AS POSSIBLE TO R5C833

30mil

XD_RE#/CLK should shield GND.

Close to CONN.

* NOT Use EEPROM :
==>UDIO5 need pull-high.
* Use EEPROM :
==>UDIO5 need pull-down.

SD can't recognize issue in ES1 sample

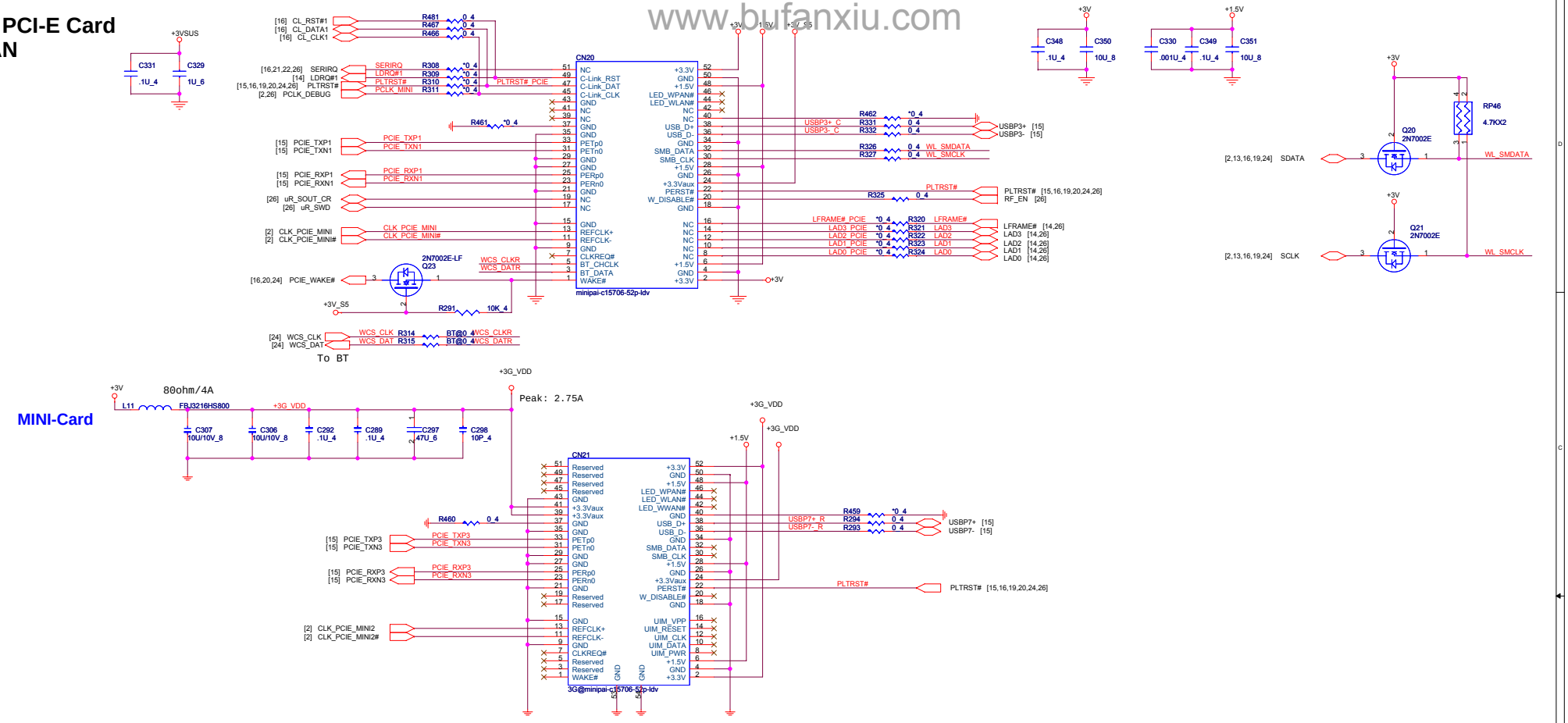
Reduced external noise by FAE confirm

> 1 ms
>60 ns
>100 ns
VCC
GRST#
PRST#
PCLK(33MHz)

Quanta Computer Inc.
PROJECT : BU1 Santa Rosa
Size | Document Number: R5C832/833(5IN1/1394) | Rev: 3A
Date: Wednesday, March 28, 2007 | Sheet 22 of 33

# Mini PCI-E Card
# WLAN






## NB SINK

HOLE8 H-C165D122P2-8
HOLE9 H-C165D122P2-8

## CPU SINK

HOLE3 H-C165D122P2-8
HOLE5 H-C165D122P2-8
HOLE4 H-C165D122P2-8
HOLE6 H-C165D122P2-8

## MINI CARD SINK

HOLE13 H-C197D122P2-8
HOLE14 H-C197D122P2-8

## MB SINK

HOLE7 *H-C236D94P2-8
HOLE1 *H-C236D106P2-8
HOLE20 *H-C236D94P2-8
HOLE21 *H-C236D94P2-8
HOLE12 *H-TC295BC236D94P2-8
HOLE16 *H-C315D94P2-8
HOLE10 *H-C236D94P2-8
HOLE2 *H-C236D106P2-8
HOLE19 *H-C189D189N
HOLE15 *H-C197D94P2-8

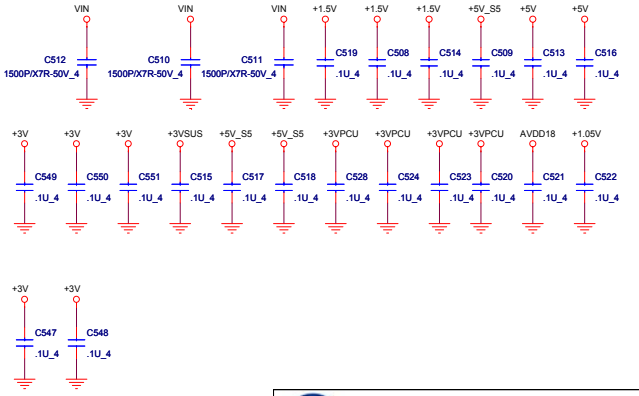
## PCMCIA SINK

HOLE17 *H-C177D138P2-8
HOLE18 *H-C177D138P2-8

## MDC PCMCIA SINK

HOLE11 H-C165D122P2-8
HOLE22 *H-C177D138P2-8

## EMI




Quanta Computer Inc.
PROJECT : BU1 Santa Rosa

| Size | Document Number | Rev |
|---|---|---|
| | MINI PCIE/HOLE | 3A |

Date: Thursday, March 29, 2007 Sheet 23 of 33

## INT KeyBoard

RP43 10KX8

100Px4 CP1 / CP2 / CP3 / CP5 / CP6

CN8 → BL121-28R-TAND-28P-L-BU1

CN37 → 196130-34020T-34P-R

CN5 → 8817-3400L-34P-R

CN6 → BL121-28R-TAND-28P-L-BU1

Keyboard Side

## Audio Board

CN12 → BT@88266-100XX-XXX-10P-R

Wire Cable 1.25mm Pitch

U18 SN74LVC1G86DCKR

CN7 → BL121-14R-TAND-14P-L-BU1-BU1

FFC Cable 0.5mm Pitch

## T/P

CN11 → *88058-6

CN10 → BL123-06R-6P-L

FFC Cable 1.0mm Pitch

## Finger Printer

CN14 → FP@88266-040XX-XXX-4P-R

Wire Cable 1.25mm Pitch

## BLUETOOTH MODULE CONNECTOR

CN9 → BT@88266-100XX-XXX-10P-R

Wire Cable 1.25mm Pitch

USB_DETACH: Low USB connect
High USB disconnect

## RJ45/USB

U12 G545B2RD1U

CN19 → BL123-12R-12P-L-BU1

Wire Cable 1.25mm Pitch

D32 / D33 CHN217

U30 TC7SH08FU

## BUTTONS ON KB COVER

CN13 → BL123-10R-TAND-10P-L-BU1

SW1

FFC Cable 1.0mm Pitch

## NEW CARD'S POWER SWITCH

Q15 / Q14 NEW@2N7002E

RP44 NEW@4.7KX2_4

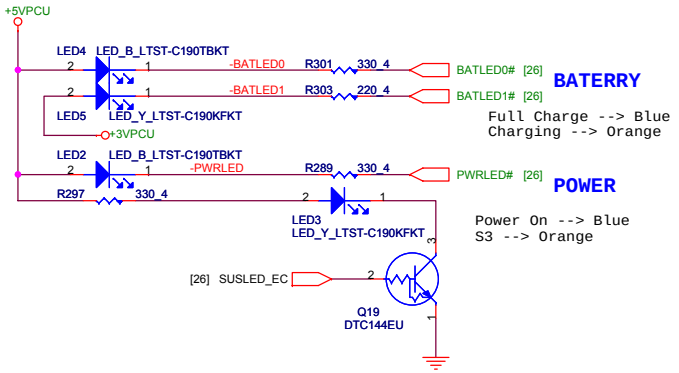
U9 NEW@TPS2231PWG4 H=1.2mm

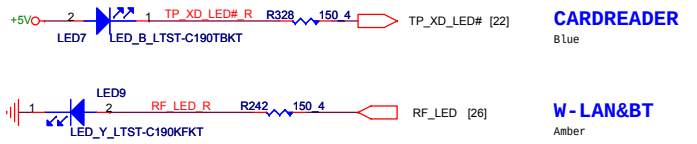
Q13 NEW@*DTC144EU

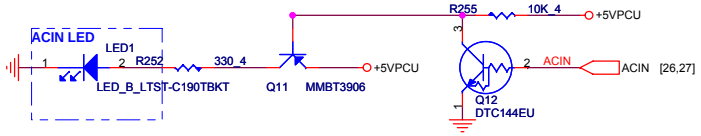
CN16 → NEW@13160171-1

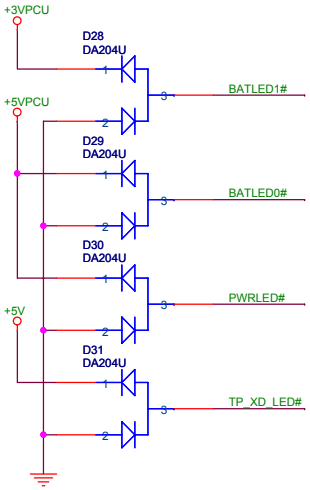
CPPE# : ( Internal Pull Up , active low when card support PCIE )
CPUSB# : ( Internal Pull Up , active low when card support USB )
SHDN# : ( Internal Pull Up )

## New card (BTO)

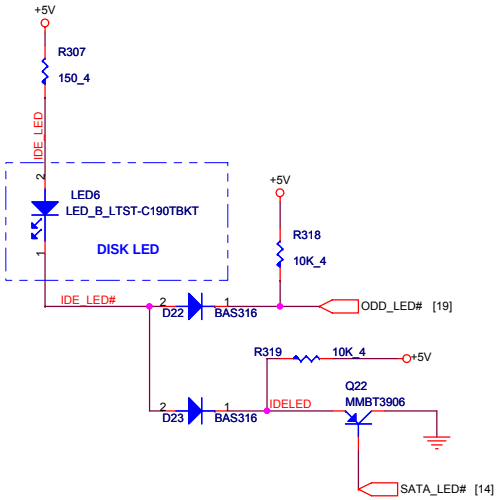


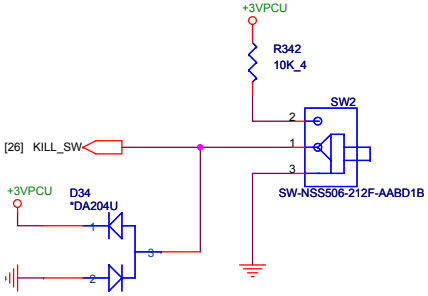




## ODD / HDD

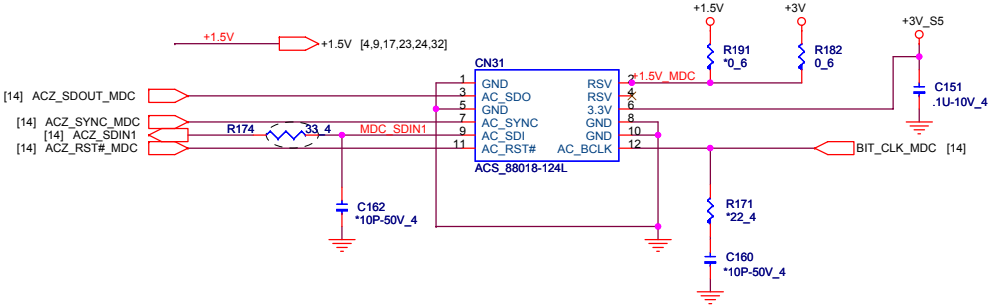



W_LAN&BT / 3G (Amber) (Blue)

DC-IN / Power / Battery /HDD(ODD) / Bridge Media access (Blue)(Blue) (Amber) (Amber) (Blue) (Blue) (Blue)

## MDC




Quanta Computer Inc.

PROJECT : BU1 Santa Rosa

| Size | Document Number | Rev |
|---|---|---|
| | TP/SW/LED | 3A |

Date: Sunday, April 01, 2007 Sheet 25 of 33

## SM BUS PU

| | | |
|---|---|---|
| MBCLK | R259 | 4.7K_4 |
| MBDATA | R258 | 4.7K_4 |
| 2ND_MBCLK | R256 | 4.7K_4 |
| 2ND_MBDATA | R257 | 4.7K_4 |
| WWW | R282 | 4.7K_4 |
| MEDIDA | R283 | 4.7K_4 |

+3VPCU

CRT_SENSE# R266 4.7K_4 +3V

## I/O ADDRESS SETTING

| BADDR1-0 | I/O Address | |
|---|---|---|
| | Index | Data |
| 0 0 | XOR TREE TEST MODE | |
| 0 1 | CORE DEFINED | |
| 1 0 | 2Eh | 2Fh |
| 1 1 | 164Eh | 164Fh |

SHBM=0: Enable shared memory with host BIOS

BADDR0 — BADDR0 R278 10K_4
BADDR1 — SOUT_CR_DEBUG R273 *10K_4
SHBM — RF_EN R265 10K_4

1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

## ID

H=1.75mm

U13 24LC08BT-I
MBCLK, MBDATA, WP, A0, A1, A2, VCC, GND
C257 .1U_4
+3VPCU

ADDRESS: A0H

## SPI FLASH

H=2.16mm

U14 W25X80VSSIG
SPI_SDI_uR R463 33_4 SPI_SDI
SPI_SDO_uR R464 33_4 SPI_SDO
SPI_SCK_uR R465 33_4 SPI_SCK
SPI_CS0# uR R343 10K_4 +3VPCU
C251 .1U_4
+3VPCU

1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

TPCLK R261 10K_4
TPDATA R260 10K_4
+5V

## INTERNAL KEYBOARD STRIP SET

+3VPCU
MY0 R277 10K_4
MY16 R279 10K_4
MY17 R280 10K_4

## DEBUG PORTS

EC Debug Port — +3VPCU — SOUT_CR_DEBUG, SWD_DEBUG — CNT8 *ACES_88231-0400

Reserved for LPC debug card — +3V — LAD0, LAD1, LAD2, LAD3, LFRAME#, PLTRST#, SERIRQ — [2,23] PCLK_DEBUG — CN17 *ACS

-- DAISY CHAIN TOPOLOGY --

08/10 FAE:
L83 CAN CHANGE FROM BEAD TO SHORT.
BUT, PLEASE PUT AGND & 32K CAP & AVCC CAP AT ONE POINT.

ZS1 STILL USE BEAD FOR SAFE.

0~AVCC power for DA pin power reference

08/14 FAE:
Please connect VREF(uRider pin104) to +A3VPCU instead of +3VPCU.

To Keyboard

0810 FAE:
CHECK X'TAL'S FOOTPRINT
CEECK RESULT: OK

08/10 FAE:
ADD ONE GAD PAD UNDER X'TAL, AND KEEP CLEANCE.

1/13 Comfirm by vendor mail :
Connect to AGND
8769AGND

1/13 Vendor mail:
Dedicate cap for AVCC

1/13 Comfirm by vendor mail:
VDD must power up after VCC/AVCC

1/13 Comfirm by vendor mail:
VBAT for keep PLL power let power up can quick!
If no VBAT will switch to VCCpower.
If PLL no power will cause boot time delay.

08/10 FAE: SMI DOESNT NEED DIODE

FOLLOW INTEL ME-EC INTERFACE SPECIFICATION.
2ND_SMB IS DEDICATED FOR ICH8 CONTROLLER LINK BUS.

EC_ME_ALERT (Intel 08/28)
Logic high = "AC present", Logic low = "AC not present (DC operation)".
EC must not drive a high value on pin until SUS Well is fully powered to prevent leakage.
AC/DC indication should be de-bounced by EC.

WPC8763LDG

LPC: LFRAME#, LAD0, LAD1, LAD2, LAD3, LCLK, CLKRUN/GPIO11/HGPIO02, GA20, KBRST, ECSCI, LDRQ/GPIO24/HGPIO01, LPCPD/GPIO10/HGPIO00, LRESET, PWUREQ, SERIRQ, SMI
A/D: AD0/GPIO90, AD1/GPIO91, AD2/GPIO92, AD3/GPIO93, AD4/GPIO05, AD5/GPIO04
D/A: DA0/GPIO94, DA1/GPIO95, DA2/GPIO96, DA3/GPIO97
GPIO: GPIO01, GPIO03, GPIO06/HGPIO06, GPIO07/HGPIO07, GPIO23, GPIO30, GPIO31, GPIO32, GPIO33, GPIO36, GPIO40, GPIO42/TCK, GPIO43/TMS, GPIO44/TDI, GPIO45, GPIO46/TRST, GPO47/UEN0, GPIO50/TDO, GPIO51, GPIO52/RDY, GPIO53, GPIO81, GPO82/HGPIO00/TRIS, GPO84/HGPIO01/BADDR0
KB: KBSIN0–KBSIN7, KBSOUT0/IENR–KBSOUT17/GPIO57/HGPIO03
TIMER: TA1/GPIO56, TA2/GPIO20, TB1/GPIO14/HGPIO4, A_PWM0, A_PWM1/GPIO21, B_PWM0/GPIO13
SPI: SPI_DI/GPIO77, SPI_DO/GPO76/SHBM, SPI_SCK/GPIO75
IR: IRRX1/GPIO72, IRRX2_IRSL0/GPIO70, IRTX/GPIO71, SIN_CR/CIRRX/GPIO87, GPIO34/CIRRX2, CIRTX/GPIO16/HGPIO04, SOUT_CR/GPO83/BADDR1
SMB: SCL1, SDA1, SCL2, SDA2
PS/2: PSCLK1, PSDAT1, PSCLK2/GPIO26, PSDAT2/GPIO27, PSCLK3/GPIO25, PSDAT3/GPIO12
FIU: F_SDI, F_SDO, F_CS0, F_SCK
SWD/GPIO66, CLKOUT/GPIO55, VCC_POR, VREF, 32KX1/32KCLKIN, 32KX2

| | | | |
|---|---|---|---|
| TEMP_MBAT [27] | R482 0_4 | | |
| INT_LVDS_BLON [6,18] | | | |
| WWW [24] | | | |
| MEDIDA [24] | | | |
| DIGVOL_UP [24] | | | |
| DIGVOL_DN [24] | | | |
| CC-SET [27] | | | |
| VFAN [3] | | | |
| SUSLED_EC [25] | | | |
| ACIN [25,27] | | | |
| NBSWON# [24] | | | |
| LID591# [18] | | | |
| SUSB# [16] | | | |
| EC_FPBACK# [18] | | | |
| LANVCC_EN [20] | | | |
| BATLED0# [25] | | | |
| BATLED1# [25] | | | |
| PWRLED# [25] | | | |
| VRON [29] | | | |
| MAINON [19,30,31,32] | | | |
| RF_LED [25] | | | |
| AMP_MUTE# [24] | | | |
| ID [27] | | | |
| SUSON [31,32] | | | |
| T99 | | | |
| T147 | | | |
| D/C# [27] | | | |
| S5_ON [28] | | | |
| BT_EN [24] | | | |
| DNBSWON# [16] | D14 BAS316 | DNBSWON_uR | |
| LED_LOGO [24] | | | |
| HDPACT [16,19] | R456 GS@*0_4 | | |
| HDPINT [16,19] | R457 GS@*0_4 | | |
| FANSIG [3] | | | |
| CONTRAST [18] | | | |
| KILL_SW [25] | | | |
| CRT_SENSE# [15,18] | | | |
| RF_EN [23] | | | |
| CELL-SET [27] | | | |
| RSMRST# [16] | RSMRST_uR 0_6 | R254 | |
| SUS# [16] | | | |
| ECPWROK [16] | PWROK_EC_uR R262 | 0_4 | |
| CCD_POWERON [18] | | | |
| USB_EN# [24] | | | |
| uR_SOUT_CR [23] | SOUT_CR_DEBUG R274 | 0_4 | |
| uR_SWD [23] | SWD_DEBUG R264 | 0_4 | |
| | VCC_POR# R267 | 4.7K_4 | +3VPCU |
| | VREF_uR R263 | 0_4 | +A3VPCU |

| | | | |
|---|---|---|---|
| [24] MX0 | MX0 | 54 | KBSIN0 |
| [24] MX1 | MX1 | 55 | KBSIN1 |
| [24] MX2 | MX2 | 56 | KBSIN2 |
| [24] MX3 | MX3 | 57 | KBSIN3 |
| [24] MX4 | MX4 | 58 | KBSIN4 |
| [24] MX5 | MX5 | 59 | KBSIN5 |
| [24] MX6 | MX6 | 60 | KBSIN6 |
| [24] MX7 | | 61 | KBSIN7 |
| [24] MY0 | | 53 | KBSOUT0/IENR |
| [24] MY1 | | 52 | KBSOUT1/TCK |
| [24] MY2 | | 51 | KBSOUT2/TMS |
| [24] MY3 | | 50 | KBSOUT3/TDI |
| [24] MY4 | | 49 | KBSOUT4 |
| [24] MY5 | | 48 | KBSOUT5/TDO |
| [24] MY6 | | 47 | KBSOUT6/RDY |
| [24] MY7 | | 43 | KBSOUT7 |
| [24] MY8 | | 42 | KBSOUT8 |
| [24] MY9 | | 41 | KBSOUT9 |
| [24] MY10 | | 40 | KBSOUT10 |
| [24] MY11 | | 39 | KBSOUT11 |
| [24] MY12 | | 38 | KBSOUT12/GPIO64 |
| [24] MY13 | | 37 | KBSOUT13/GPIO63 |
| [24] MY14 | | 36 | KBSOUT14/GPIO62 |
| [24] MY15 | | 35 | KBSOUT15/GPIO61/XOR_OUT |
| [24] MY16 | MY16 | 34 | KBSOUT16/GPIO60 |
| [24] MY17 | MY17 | 33 | KBSOUT17/GPIO57/HGPIO03 |
| [3,18,27] MBCLK | MBCLK | 70 | SCL1 |
| [3,18,27] MBDATA | MBDATA | 69 | SDA1 |
| [19] 2ND_MBCLK | 2ND_MBCLK | 67 | SCL2 |
| [19] 2ND_MBDATA | 2ND_MBDATA | 68 | SDA2 |
| [24] TPCLK | | 72 | PSCLK1 |
| [24] TPDATA | | 71 | PSDAT1 |
| [24] USB_EN2# | | 10 | PSCLK2/GPIO26 |
| [24] CAPSLED | | 11 | PSDAT2/GPIO27 |
| [24] FN_F10 | | 12 | PSCLK3/GPIO25 |
| [24] NUMLED | | 13 | PSDAT3/GPIO12 |
| | | 77 | 32KX1/32KCLKIN |
| | | 79 | 32KX2 |
| | | 30 | CLKOUT/GPIO55 |
| | | 104 | VREF |

| | | | |
|---|---|---|---|
| SPI_SDI | SPI_SDI_uR | 86 | F_SDI |
| SPI_SDO | SPI_SDO_uR | 87 | F_SDO |
| SPI_CS0# | SPI_CS0#_uR | 90 | F_CS0 |
| SPI_SCK | SPI_SCK_uR | 92 | F_SCK |

| | | | |
|---|---|---|---|
| [32] HWPG_2.5V | D16 | BAS316 | |
| [28] SYS_HWPG | D21 | BAS316 | |
| [30] HWPG_1.05V | D17 | BAS316 | |
| [31] HWPG_1.8V | D19 | BAS316 | |
| [32] HWPG_1.5V | D20 | BAS316 | |

R281 10K_4 +3V HWPG

R339 20M_6 H=2.5mm Y3 32.768KHZ C358 15P_4 C362 15P_4 R341 33K_6

L8 BLM18AG601SN1 L36 BLM18AG601SN1 L9 HZ0603B601R-00

C260 .1U_4, C266 10U_8, C264 .1U_4, C284 .1U_4, C288 10U_8, C280 1U_6

C281 10U_8, C277 .1U_4, C261 .1U_4, C282 .1U_4, C278 .1U_4, C259 .1U_4

C262 .1U_4, C272 .1U_4, C291 .1U_4

PCLK_591 R285 *22_4 C285 *10P_4

D18 BAS316 SCI#_uR

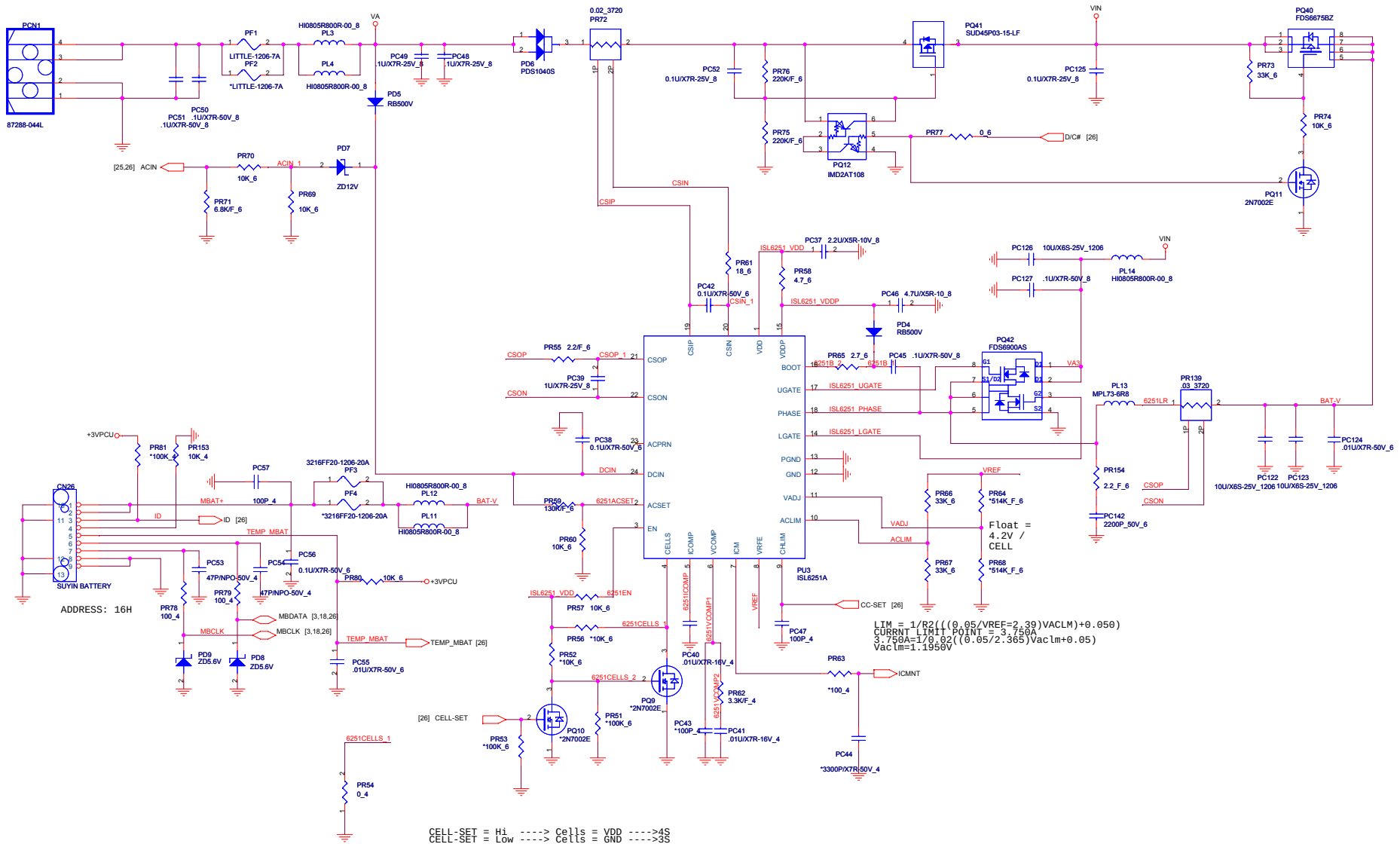
T96 TP_uR_PWUREQ#

8769AGND, 08/10 FAE: 0.1UF

+3VPCU, +A3VPCU, +3V

H=1.6mm

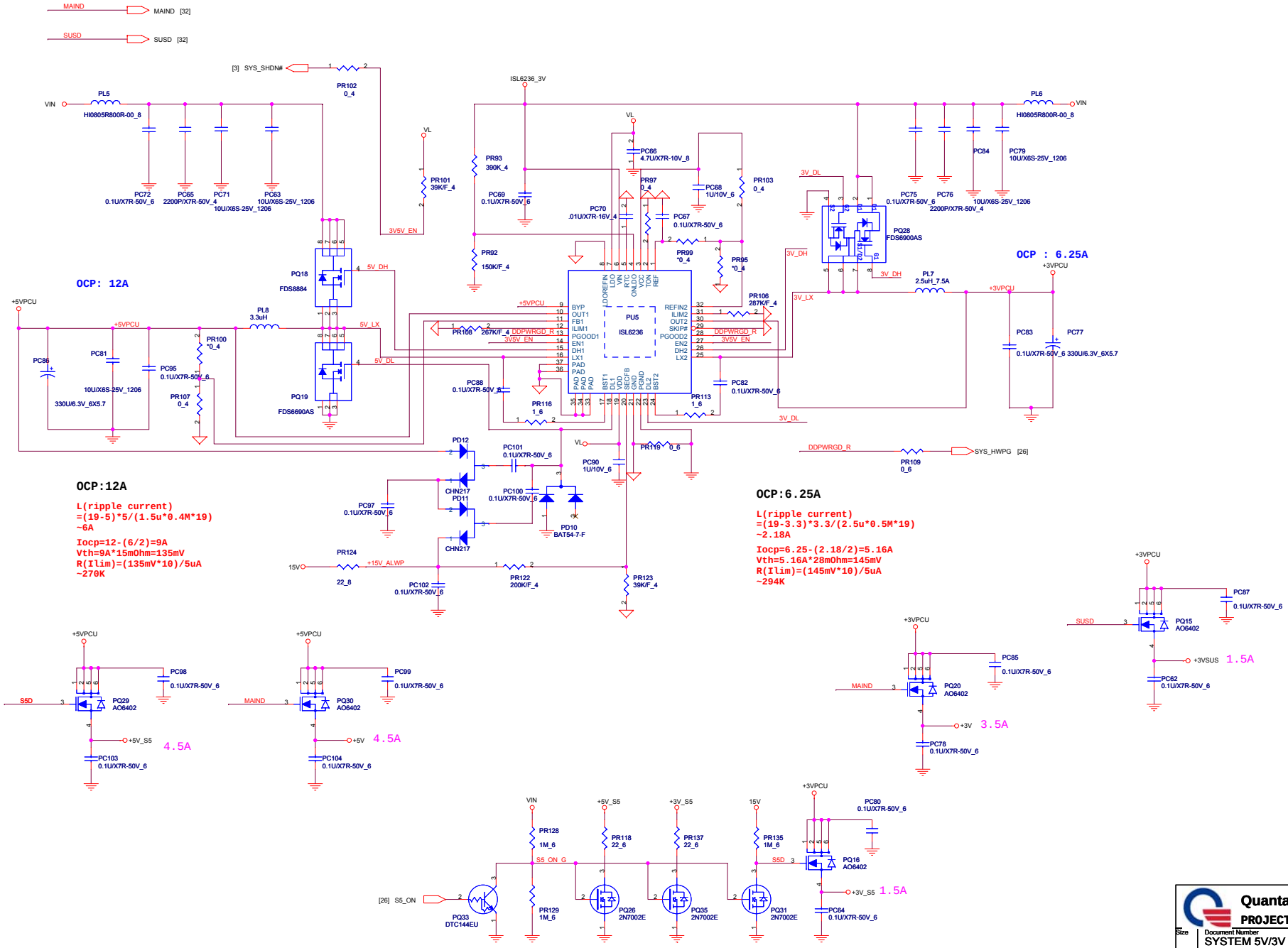
| | | |
|---|---|---|
| [14,23] LFRAME# | LFRAME# | 3 |
| [14,23] LAD0 | LAD0 | 126 |
| [14,23] LAD1 | LAD1 | 127 |
| [14,23] LAD2 | LAD2 | 128 |
| [14,23] LAD3 | LAD3 | 1 |
| [2] PCLK_591 | PCLK_591 | 2 |
| [16,22] CLKRUN# | | 8 |
| [14] GATEA20 | | 121 |
| [14] RCIN# | | 122 |
| [16] SCI# | | 29 |
| | | 6 |
| | | 124 |
| [15,16,19,20,23,24] PLTRST# | PLTRST# | 7 |
| [16,21,22,23] SERIRQ | SERIRQ | 125 |
| [16] KBSMI# | | 9 |



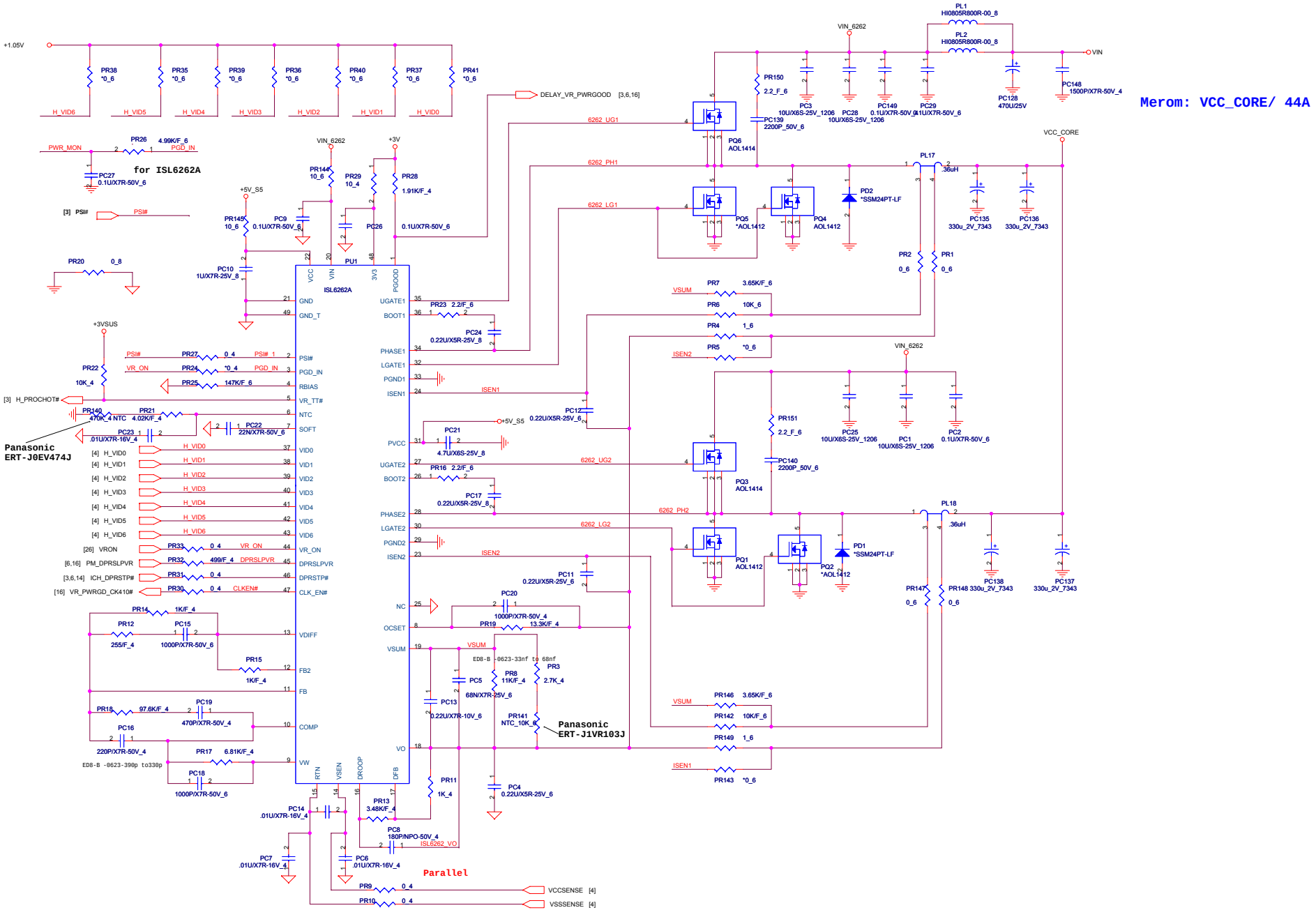

Quanta Computer Inc.
PROJECT : BU1 Santa Rosa

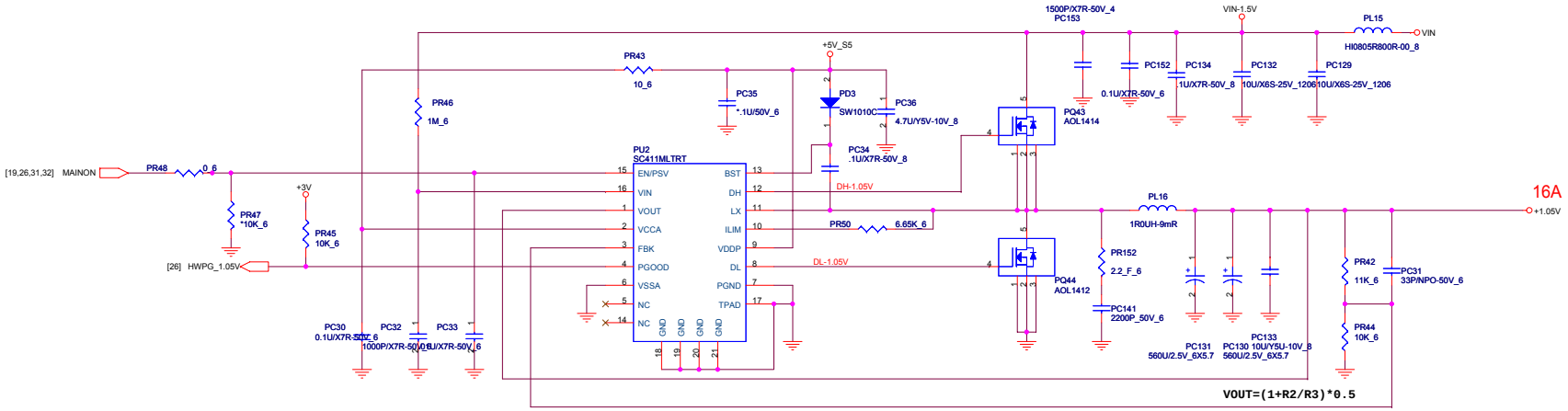
| Size | Document Number | Rev |
|---|---|---|
| | ISL6251 | 3A |

Date: Sunday, April 01, 2007 Sheet 27 of 33

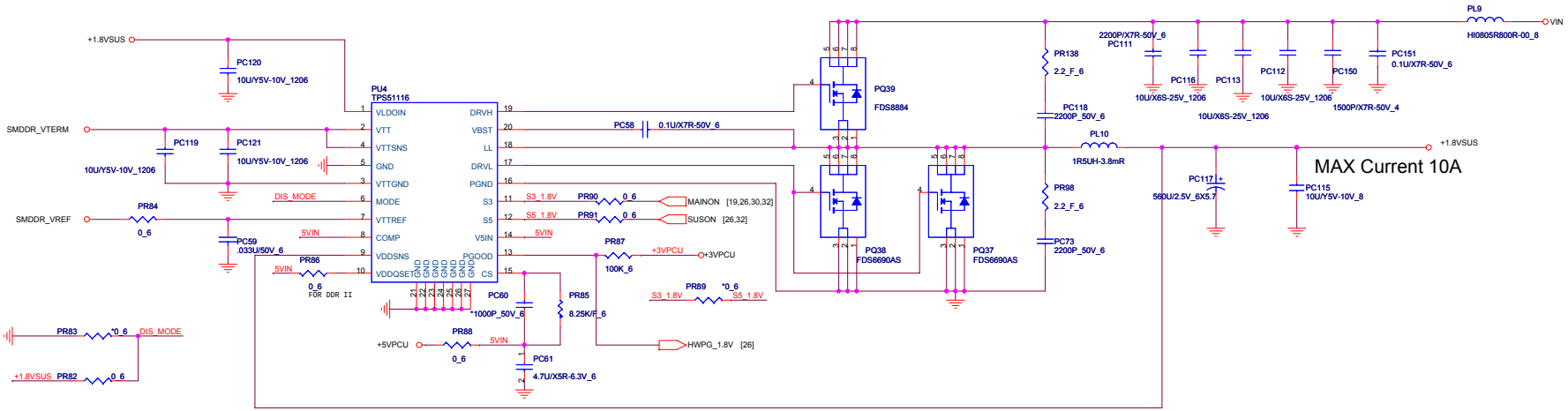



| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : BU1 Santa Rosa | | |
| Size | Document Number: SYSTEM 5V/3V | Rev: 1A |
| Date: Monday, March 26, 2007 | Sheet 28 of 33 | |

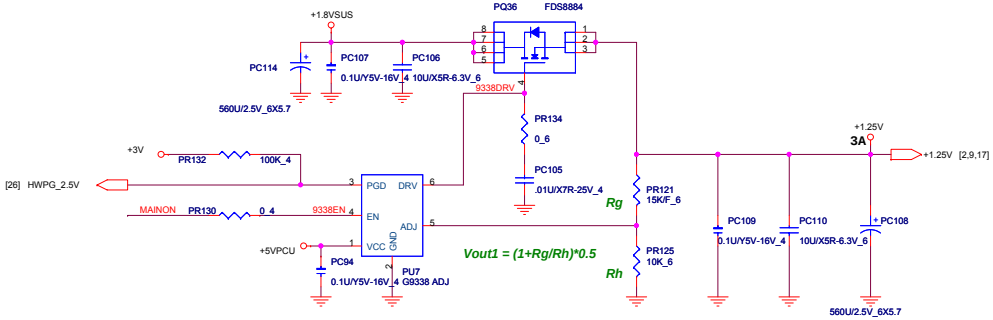


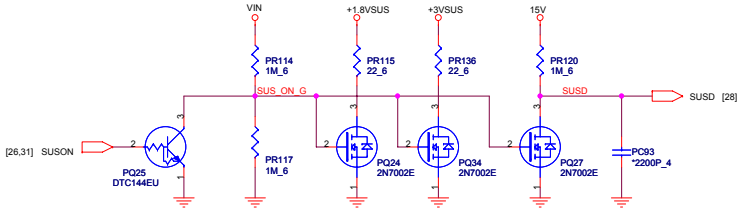


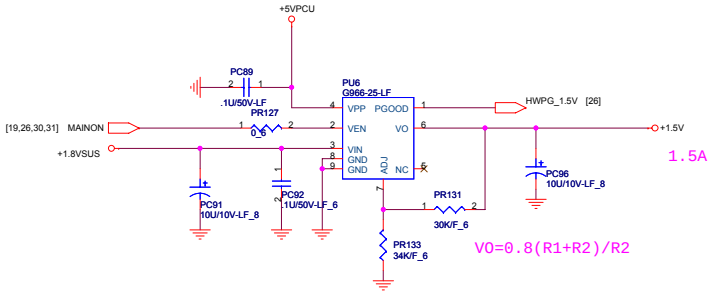

| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : BU1 Santa Rosa | | |
| Size | Document Number: VTT 1.05V (SC11) | Rev: 2A |
| Date: Thursday, March 29, 2007 | Sheet 30 of 33 | |

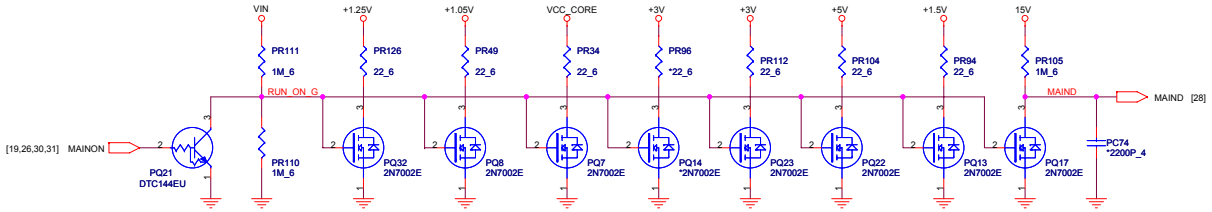



| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : BU1 Santa Rosa | | |
| Size | Document Number: DDR2 1.8V(TP1116) | Rev: 3A |
| Date: Sunday, April 01, 2007 | Sheet 31 of 33 | |




Quanta Computer Inc.

PROJECT : BU1 Santa Rosa

| Size | Document Number | Rev |
|---|---|---|
| | DISCHARGE/1.5V/VCC1.25 | 1A |

Date: Monday, March 26, 2007 Sheet 32 of 33

| Model | REV | DATE | CHANGE LIST | NOTE |
|---|---|---|---|---|
| BU1 | 00 | 20061218 | **FIRST RELEASED : 20061218** | |
| | 01 | 20061225 | Page02: Change CLK GEN. low power outs from +1.05V to +1.25V.Because VDD_IO will drop out when high loading | Circuit modify |
| | | | Page02: REV_01 Remove CLK_MCH_OE#_R had pull up resistor,because had be pull up at NB side | Circuit modify |
| | | | Page03: Del R382,R383,Q60,D39 | Circuit modify |
| | | | Page04: Del R176 for FBS signals batter return path under +1.05V plane | Circuit modify |
| | | | Page08: Change Crestline VCC_AXM to 1.25V, reference to SR ww48 MoW. reserved 0 ohm resister | Circuit modify |
| | | | Page16: Add D43 to avoid leakage from EC to SB,Del R242 | Circuit modify |
| | | | Page18: REV_01 Reserved LCD/LED type panel module and Digital/analogy MIC | Circuit modify |
| | | | Page19: Modify G-Sensor circuit | Circuit modify |
| | | | Page22: Reserved LPC_PD# control signal from SB to R5C833 | Circuit modify |
| | | | Page23: Increase HOLE | Circuit modify |
| | | | Page24: Add 0.1u CAP. C810 from +5VPCU to GND | Circuit modify |
| | | | Page25: Modify IDE LED circuit | Circuit modify |
| | | | Page26: Reserved R756,R766 for EC control G-Sensor | Circuit modify |
| | | | Page27: Add 3 cell Battery always setting circuit | Circuit modify |
| | | | Page28: Add +3V_S5 discharge circuit | Circuit modify |
| | | | Page30: Reserved PD resistor to avoid leakage voltage | Circuit modify |
| | | | Page32: Reserve +3V discharge circuit | Circuit modify |
| | 1A | 20061227 | **A TEST (PCB REV_1A) RELEASED : 20061227** | |
| | 2A | 20070201 | Page03: Modify thermal protect circuit and FAN control | Circuit modify |
| | | | Page14: Modify RTC charge current / SB strip setting / Reserved PU resistor on SATALED# signal / Change XTAL capacitor value | BOM/Circuit modify |
| | | | Page16: Reserver Pull down resistor on HDPINT signal / Reserved C-Link to WLAN / Delete FM function / Add Board ID | Circuit modify |
| | | | Page18: Change panel backlight signal pull up resistor / Change camera power source / Add LED type panel circuit / Add fuse on CRT power | BOM/Circuit modify |
| | | | / Reserved EMI choke on USB signals and add EMI solution / Add RC circuit on LED panel driver IC | Circuit modify |
| | | | Page19: Modify LDO power source / Add Microprocessor reset IC / Reserved G-sensor SMBUS to SB chipset | Circuit modify |
| | | | Page22: Reserved Cardreader external EEPROM | Circuit modify |
| | | | Page23: Separate RF enable/disable pin from WLAN and 3G card / Add EMI solution and Reserved C-Link circuit / Delete 3G card function | Circuit modify |
| | | | / Add HOLE for card Bus connector | Circuit modify |
| | | | Page24: Increase CN7 pin for control illumination logo and enable/disable USB port power / Add capacitor on keyboard signals for EMI | Circuit modify |
| | | | / Change LAN/B cable connector / Delete FM function | Circuit modify |
| | | | Page25: Modify battery LED and RF SW power source / Delete 3G card LED | Circuit modify |
| | | | Page26: Modify EC control circuit / Add EMI solution / Change XTAL capacitor value | BOM/Circuit modify |
| | | | Page27: Change fuse rating and switch MOS | Circuit modify |
| | | | Page29: Add EMI solution | Circuit modify |
| | | | Page30: Add EMI solution | Circuit modify |
| | | | Page31: Add EMI solution | Circuit modify |
| | | | Page32: Add EMI solution | Circuit modify |
| | 3A | 20070326 | Page03: Add CAP to GND for FAN controller IC U12 power pin decoupling | Circuit modify |
| | | | Page13: Change DDR socket height | Circuit modify |
| | | | Page18: Exchange Dioid and Fuse placement | Circuit modify |
| | | | Page20: Add control LAN power circuit to enable/disable LAN | Circuit modify |
| | | | Page22: Change 1394 connector type and delete card reader connector 2nd source | Circuit modify |
| | | | Page23: Change mini-card 3V power source from +3VSUS to +3V_S5 for support wake on WLAN from S3/S4 / Change HOLE pad size | Circuit modify |
| | | | Page24: Reserve EMI capacitor / add solve insert PCMCIA Card speaker has bo sound circuit | Circuit modify |
| | | | Page25: Add ESD protect circuit | Circuit modify |
| | | | Page27: Change MOS footprint | Circuit modify |
| | | 20070327 | Page14: Modify RTC short pad footprint | Circuit modify |
| | | | Page17: Modify inductance type | Circuit modify |
| | | | Page23: Add capacitors for EMI | Circuit modify |
| | | | Page24: Modify FFC connector footprint | Circuit modify |
| | | | Page26: Add capacitor for EMI | Circuit modify |
| | | | Page27: Reserve EMI circuit | Circuit modify |
| | | 20070328 | Page22: Delete card reader external EEPROM | Circuit modify |
| | | | Page23: Add pull up resistor on PCIE_WAKE# signal | Circuit modify |
| | | 20070329 | Page18: Delete CMO LED type connector | Circuit modify |
| | | | Page25: Reserve ESD protect on kill-switch | Circuit modify |
| | | | Page31: Stuff R/C Snubber for EMI | BOM modify |