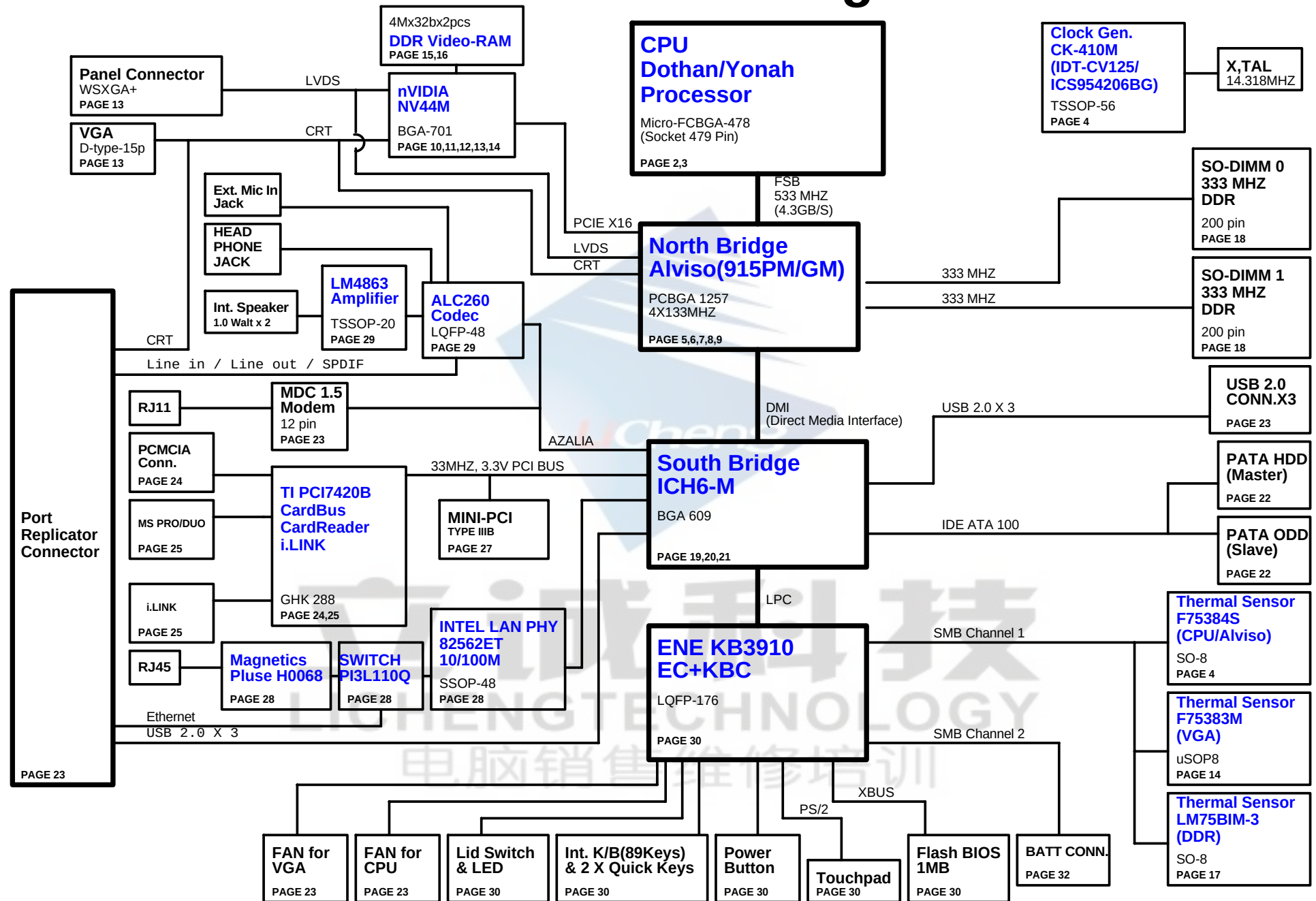
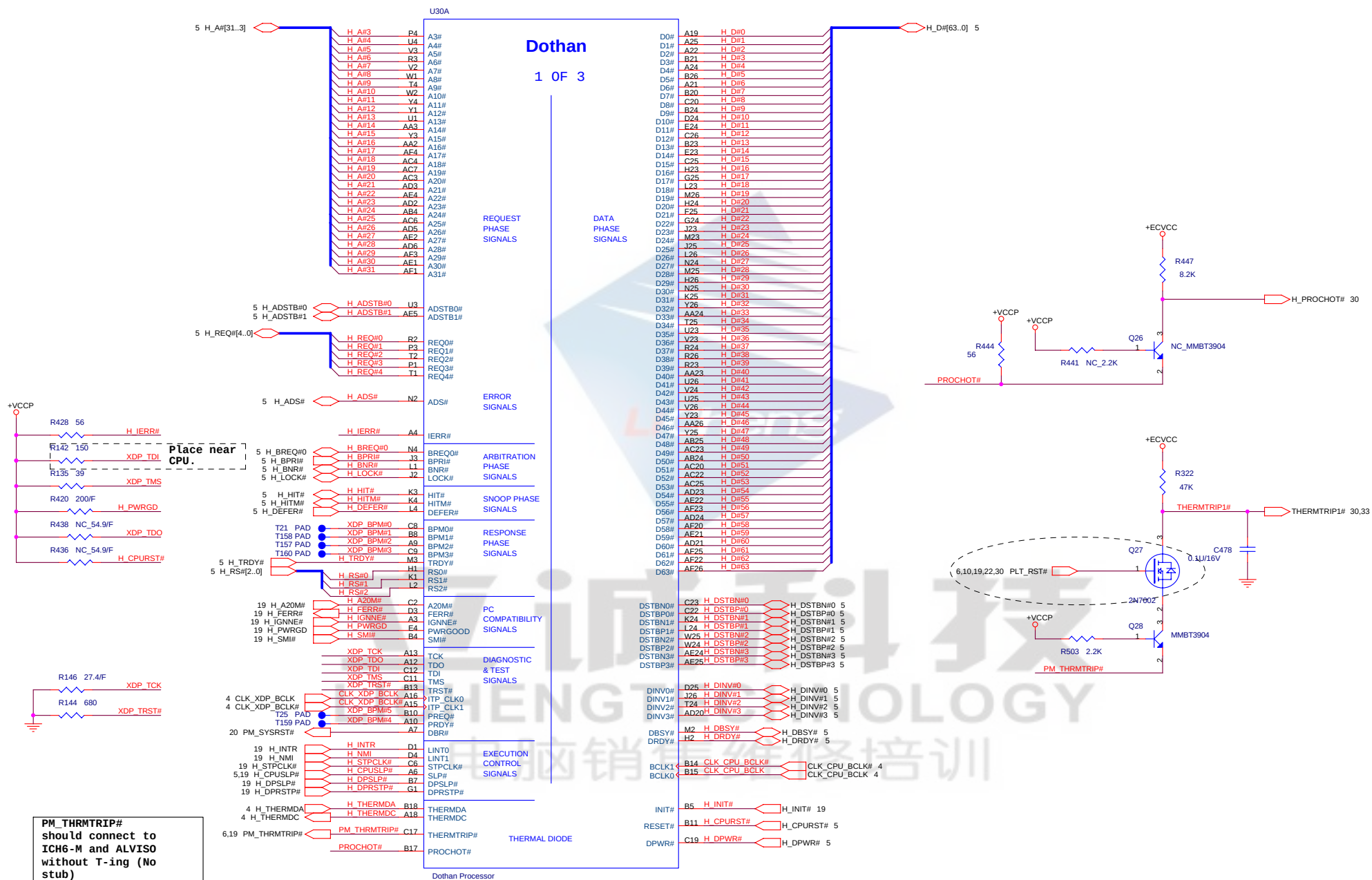
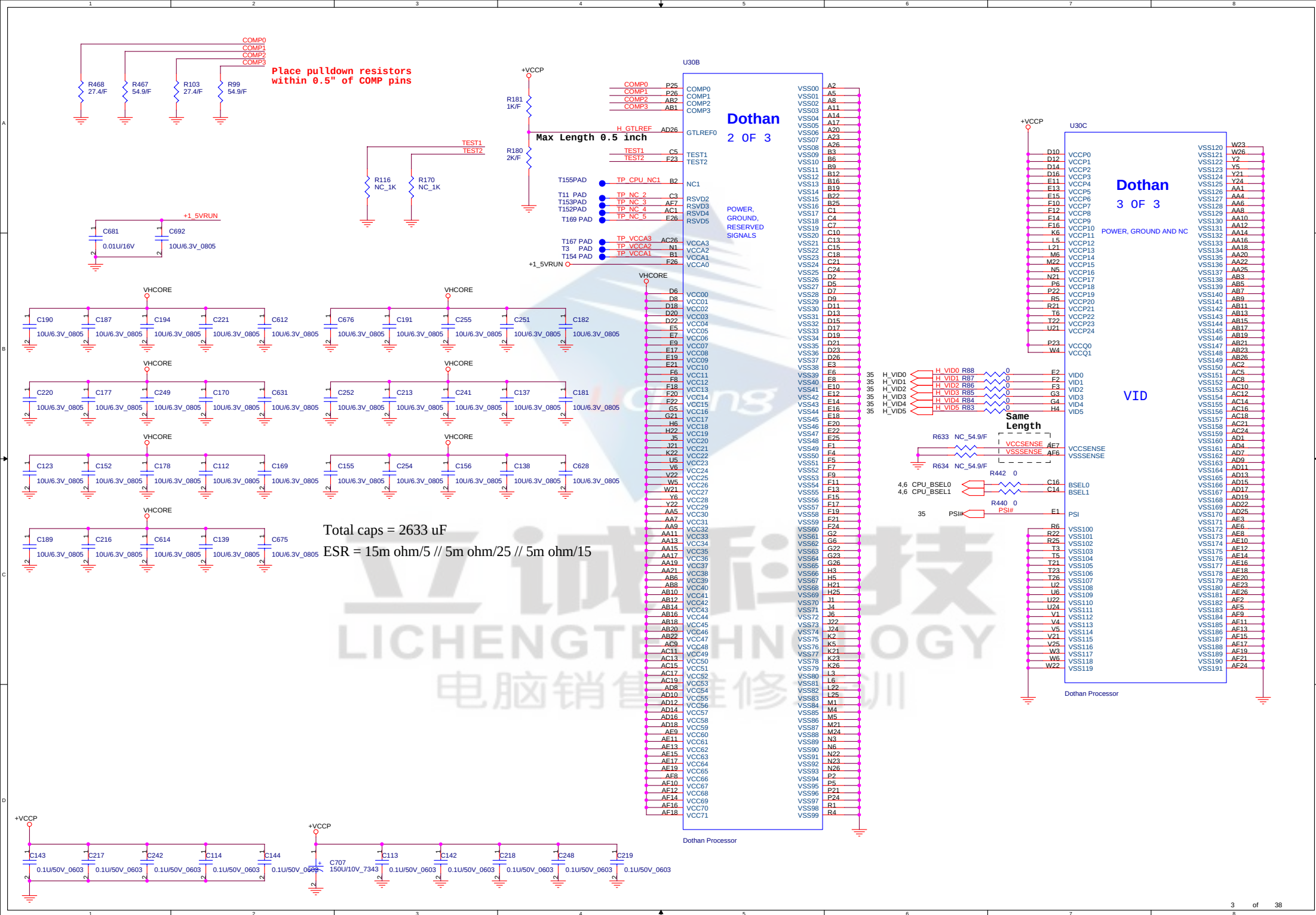


915PM/GM+Gfx Block Diagram







FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

Length as short as possible.

Placed within 500mils of Y1

Alviso Chip HOST

CPU

Alviso Chip

ICH6 DMI

Graphic NV44M

ALVISO SSCK

SM bus Address :
1101001 (ICH6)
For clock generator

SM bus Address :
1001101 (EC)
For F75384S

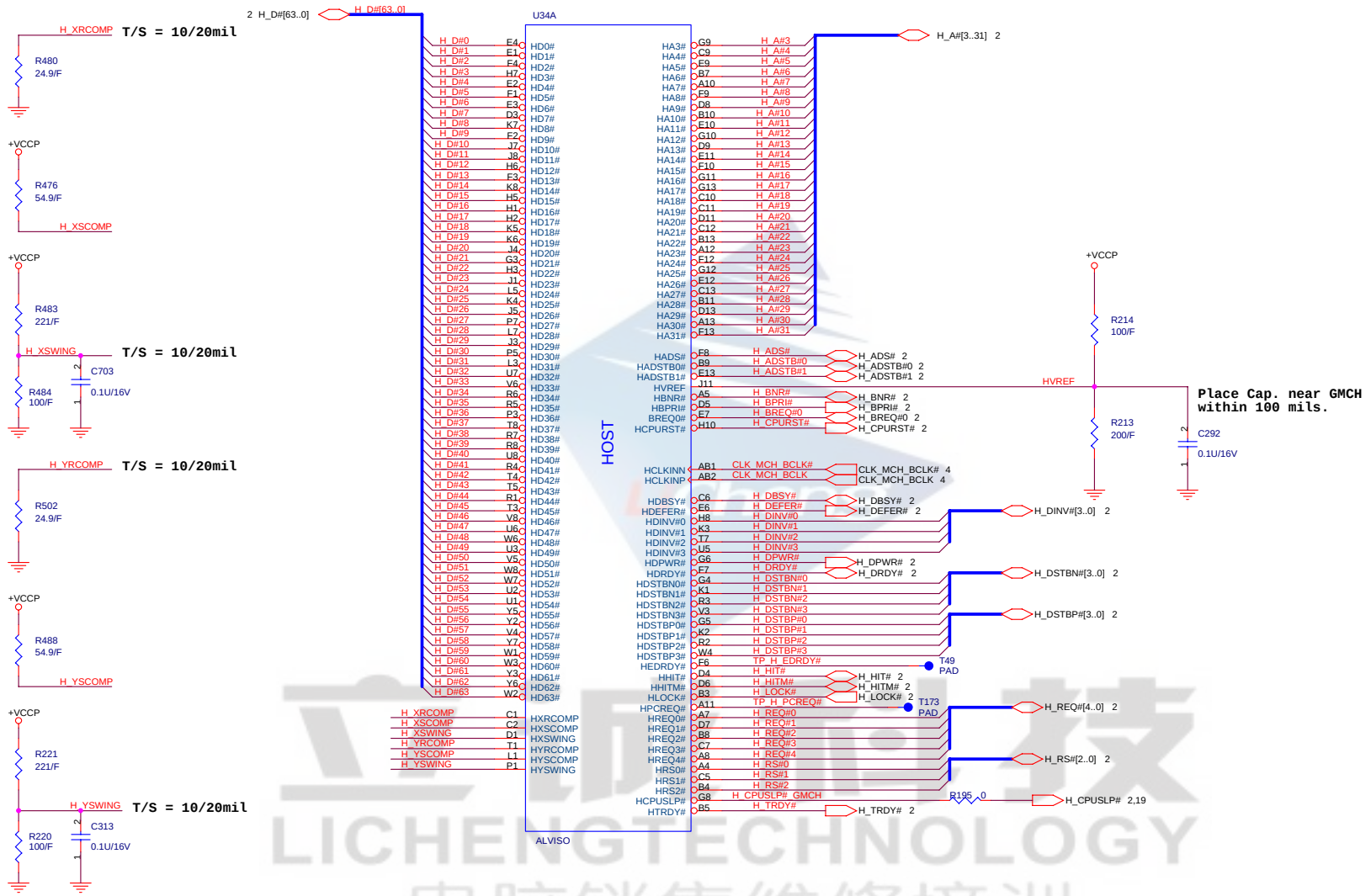
Place Thermal-Sensor near CPU & GMCH.

CLK_XDP_BCLK# R460 NC 49.9/F
CLK_XDP_BCLK# R458 NC 49.9/F
CLK_MCH_BCLK R465 49.9/F
CLK_MCH_BCLK# R463 49.9/F
CLK_CPU_BCLK R471 49.9/F
CLK_CPU_BCLK# R469 49.9/F
CLK_MCH_3GPLL R457 49.9/F
CLK_MCH_3GPLL# R455 49.9/F

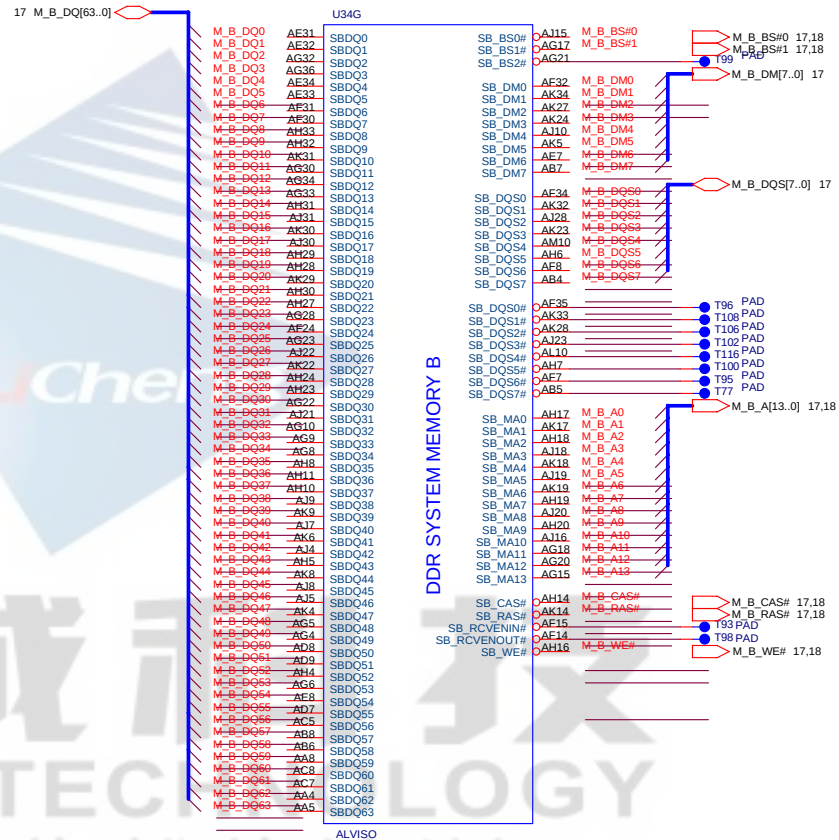
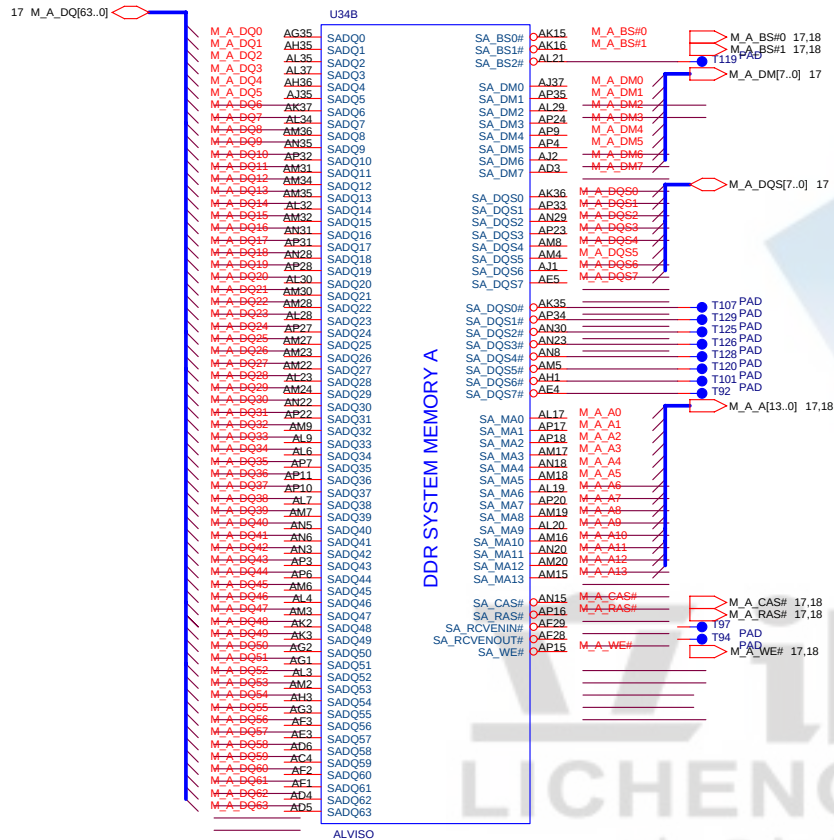
CLK_PCIE_ICH R459 49.9/F
CLK_PCIE_ICH# R456 49.9/F

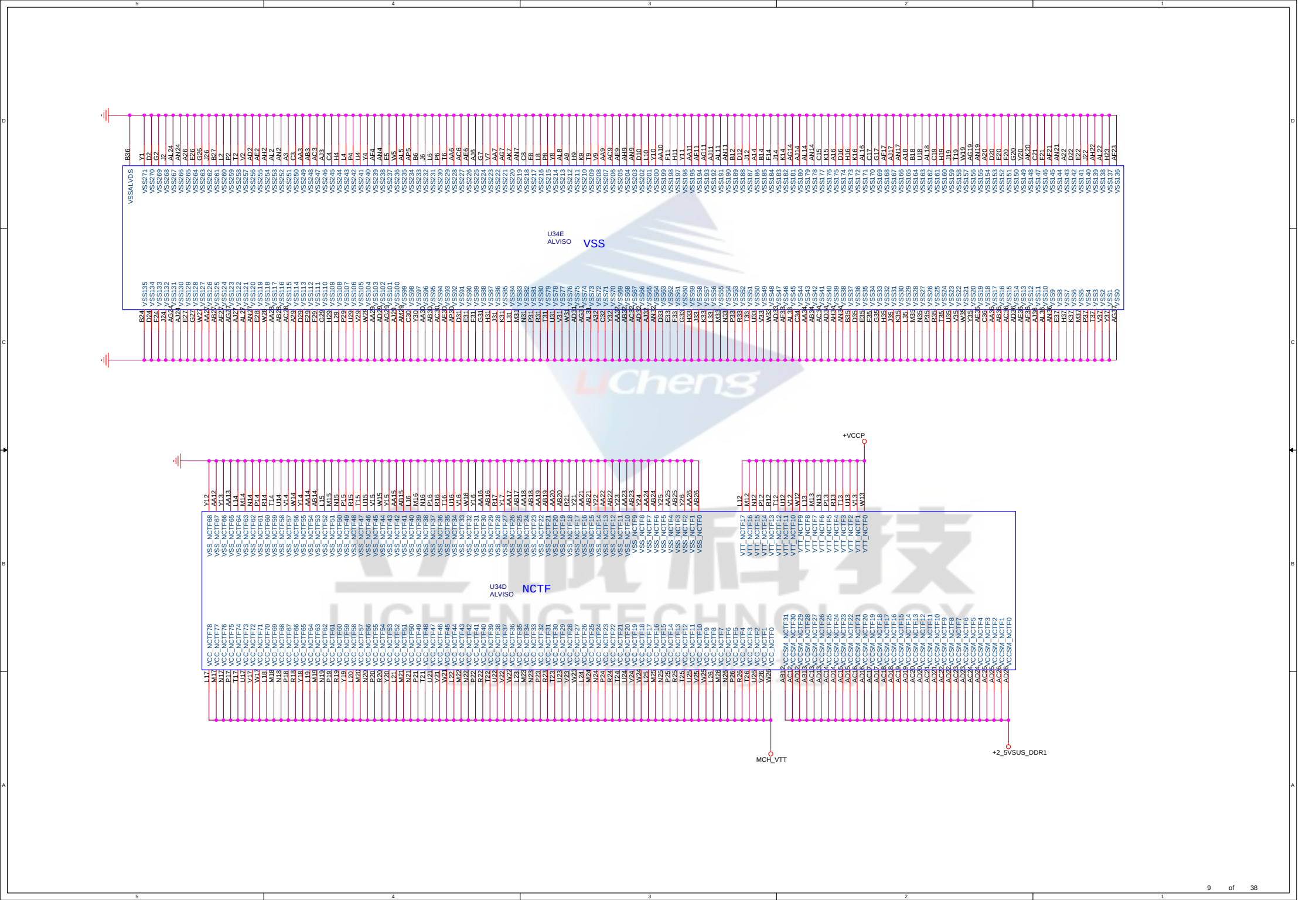
CLK_PCIE_PEG R462 NV 49.9/F
CLK_PCIE_PEG# R461 NV 49.9/F
DREFCLK# R470 AL 49.9/F
DREFSSCLK# R466 NV 0
DREFSSCLK# R185 AL 49.9/F
DREFSSCLK# R183 NV 0
DREFCLK# R631 AL 49.9/F
DREFSSCLK# R632 AL 49.9/F

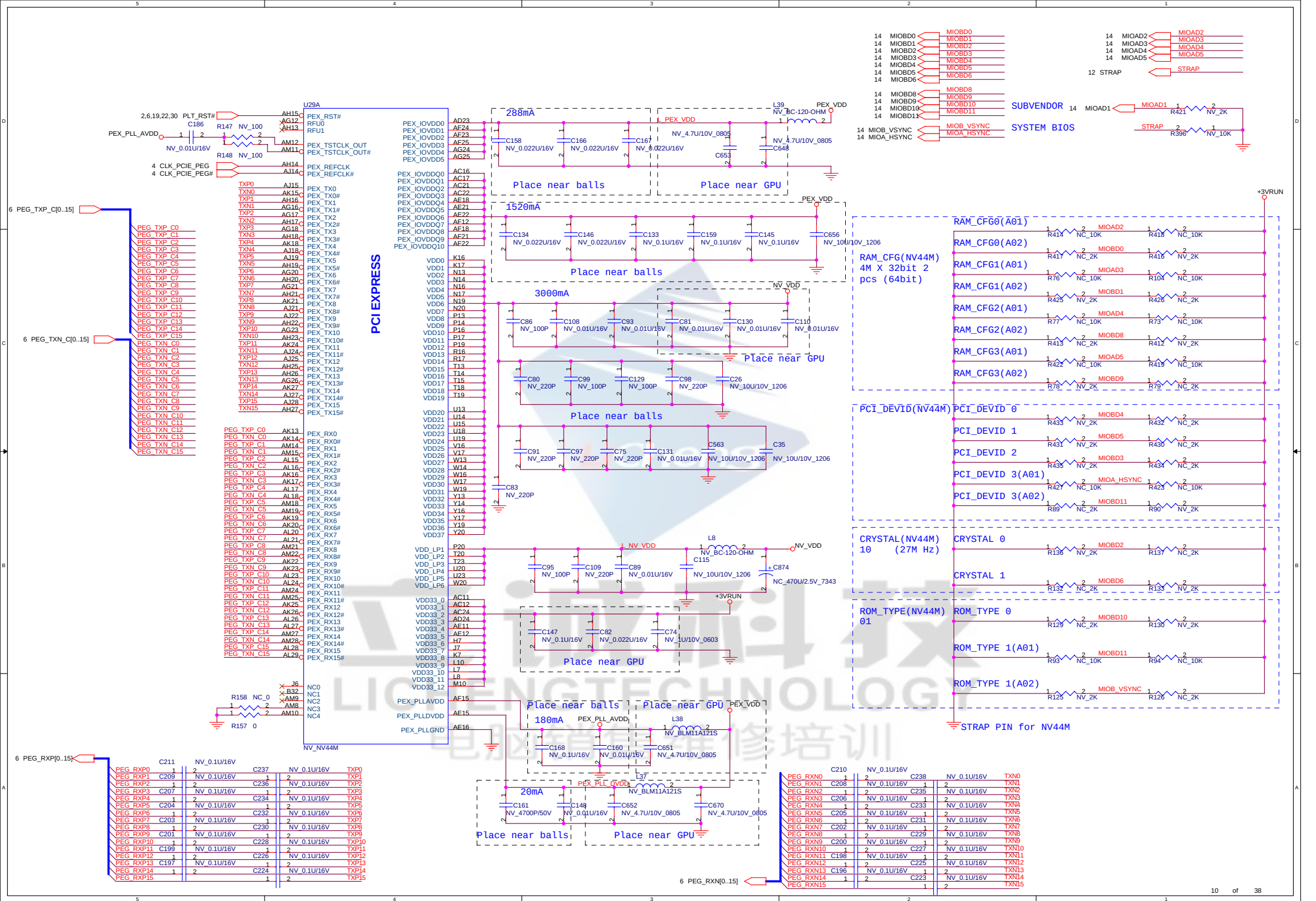
For NV44M & Alviso option
R_CLK_KBCPCI R626 NC 10K
R_PCLK_MINI R627 NC 10K

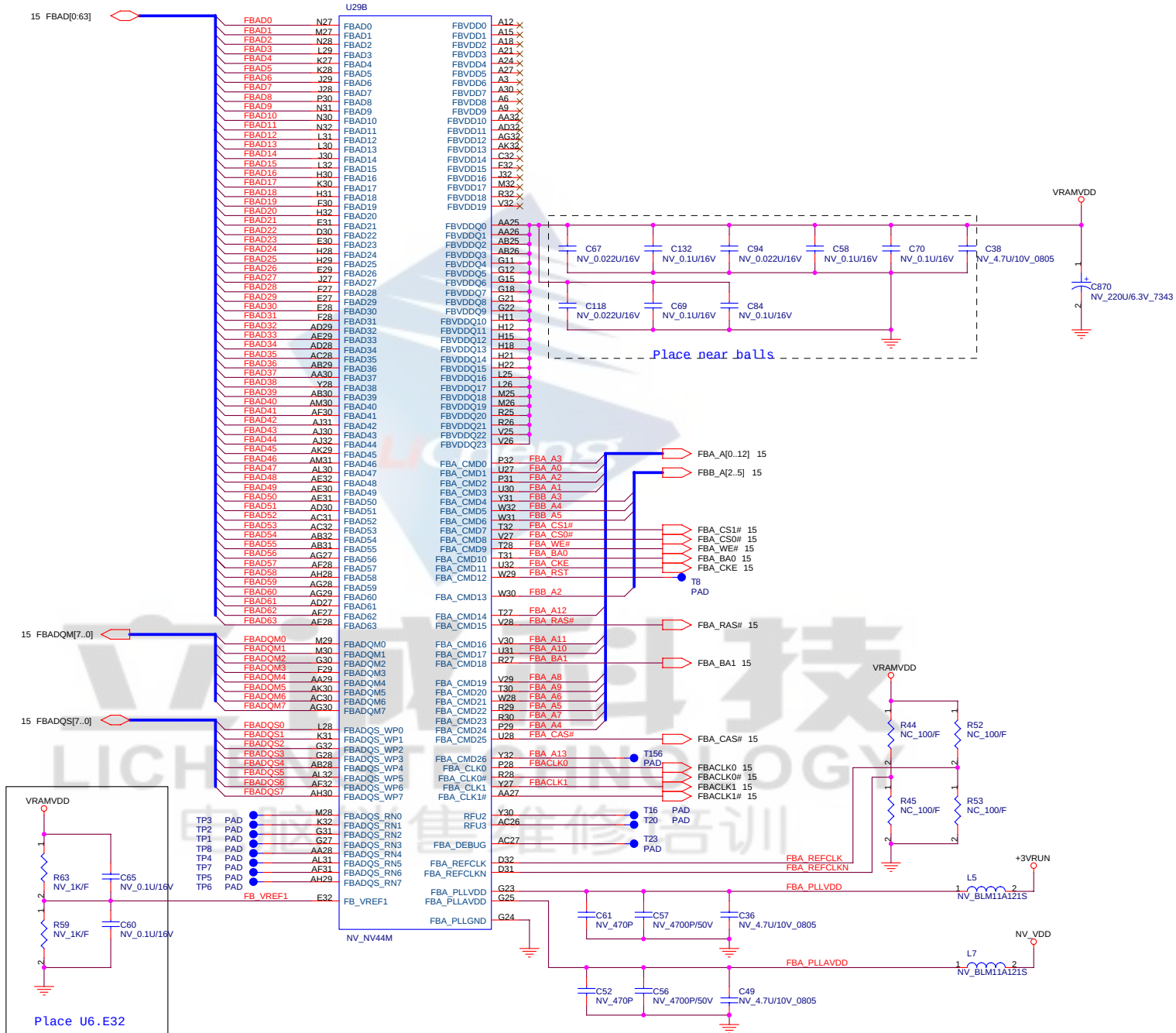
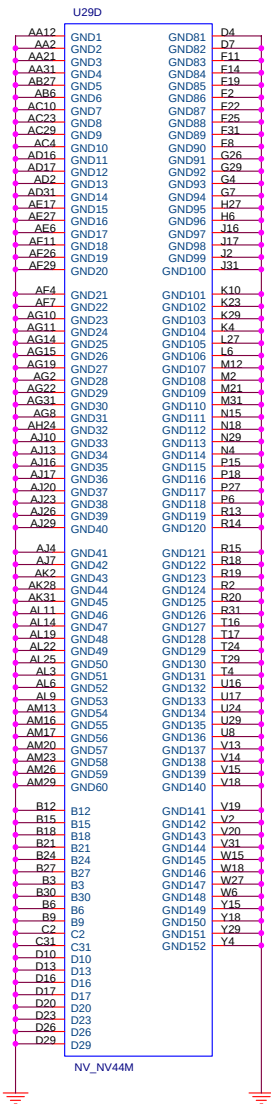






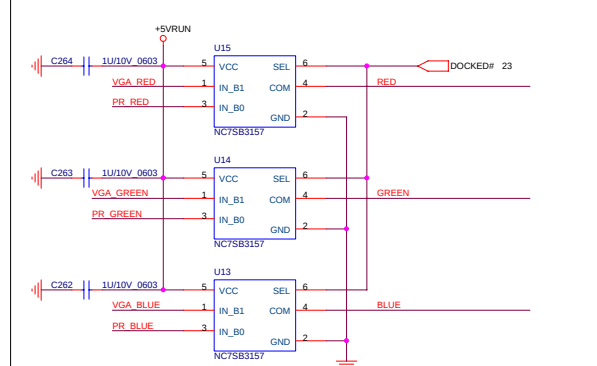
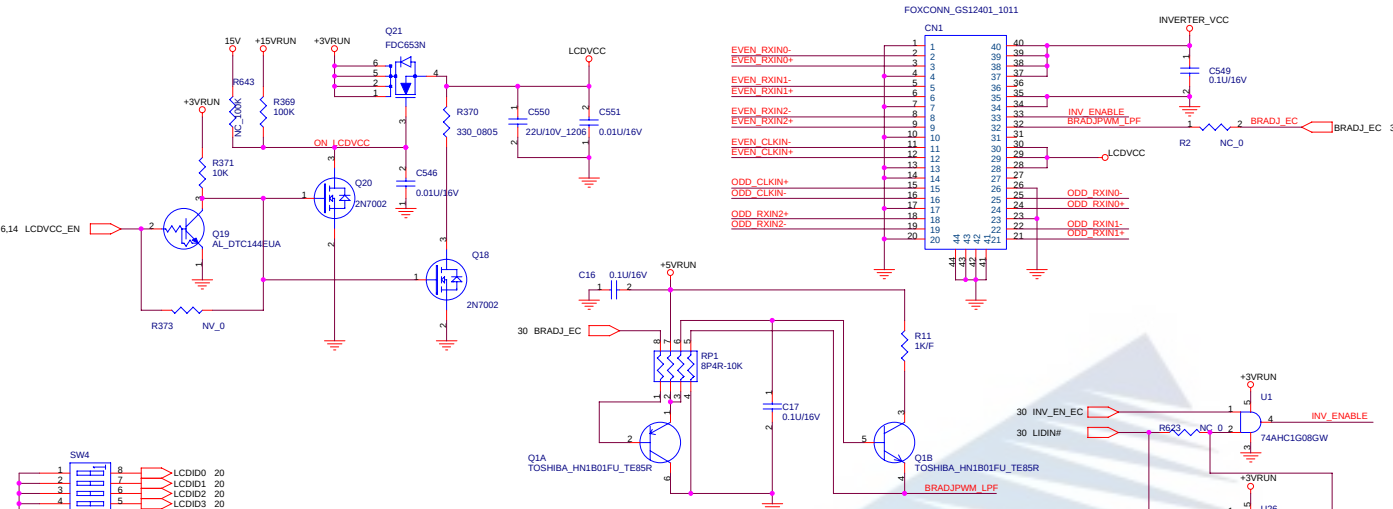




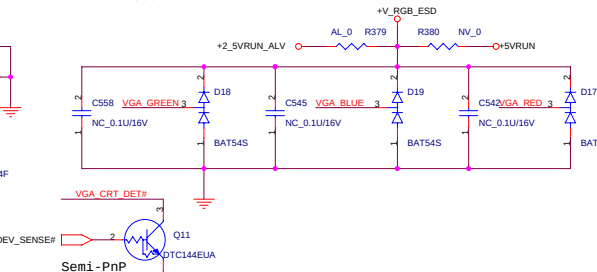
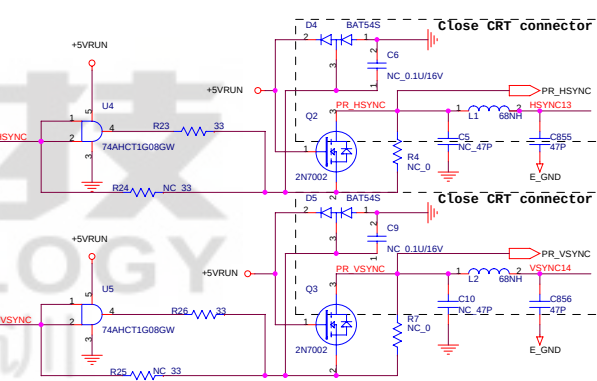
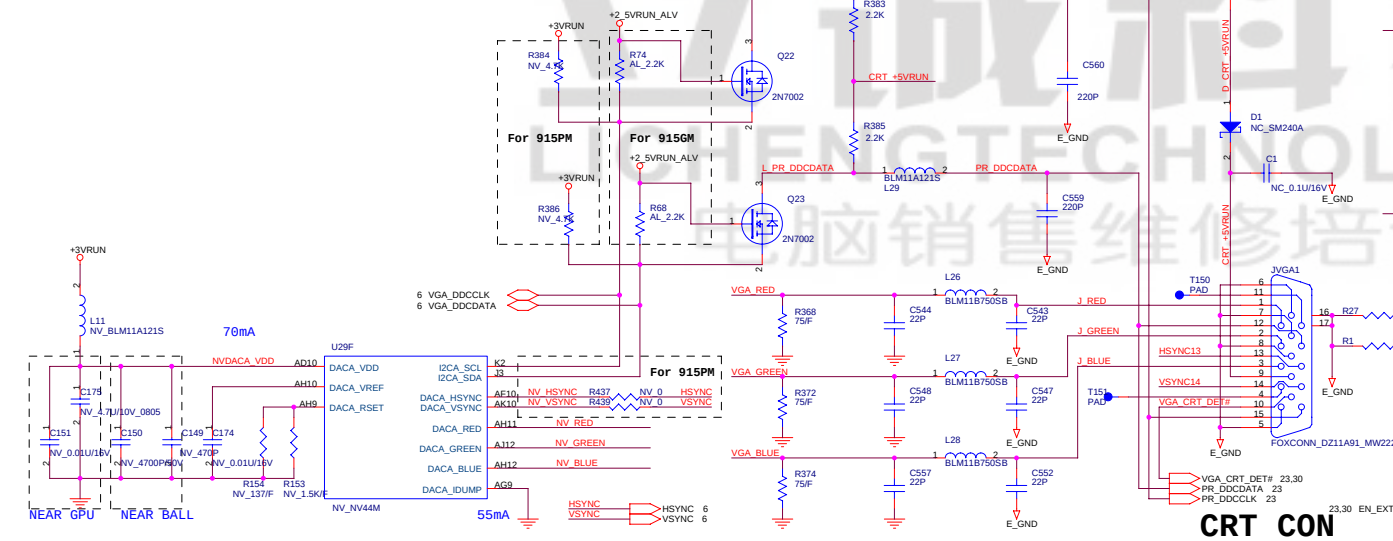
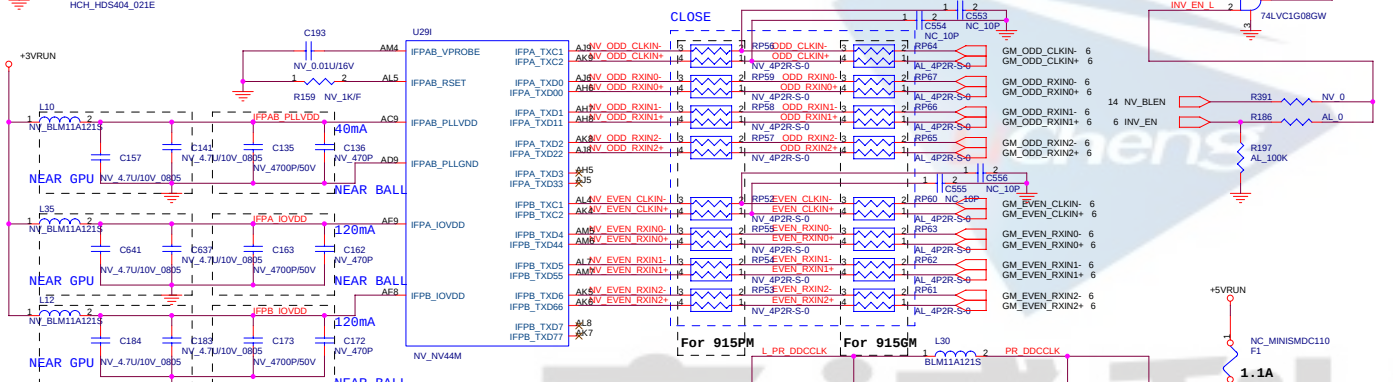
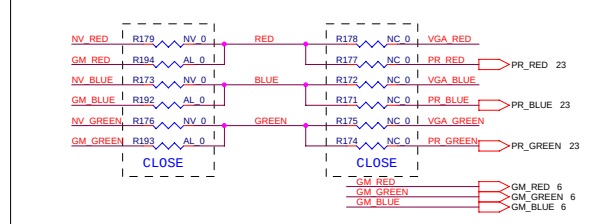


LVDS CONNECTOR

H : NOTEBOOK
L : PORT REPLICATOR

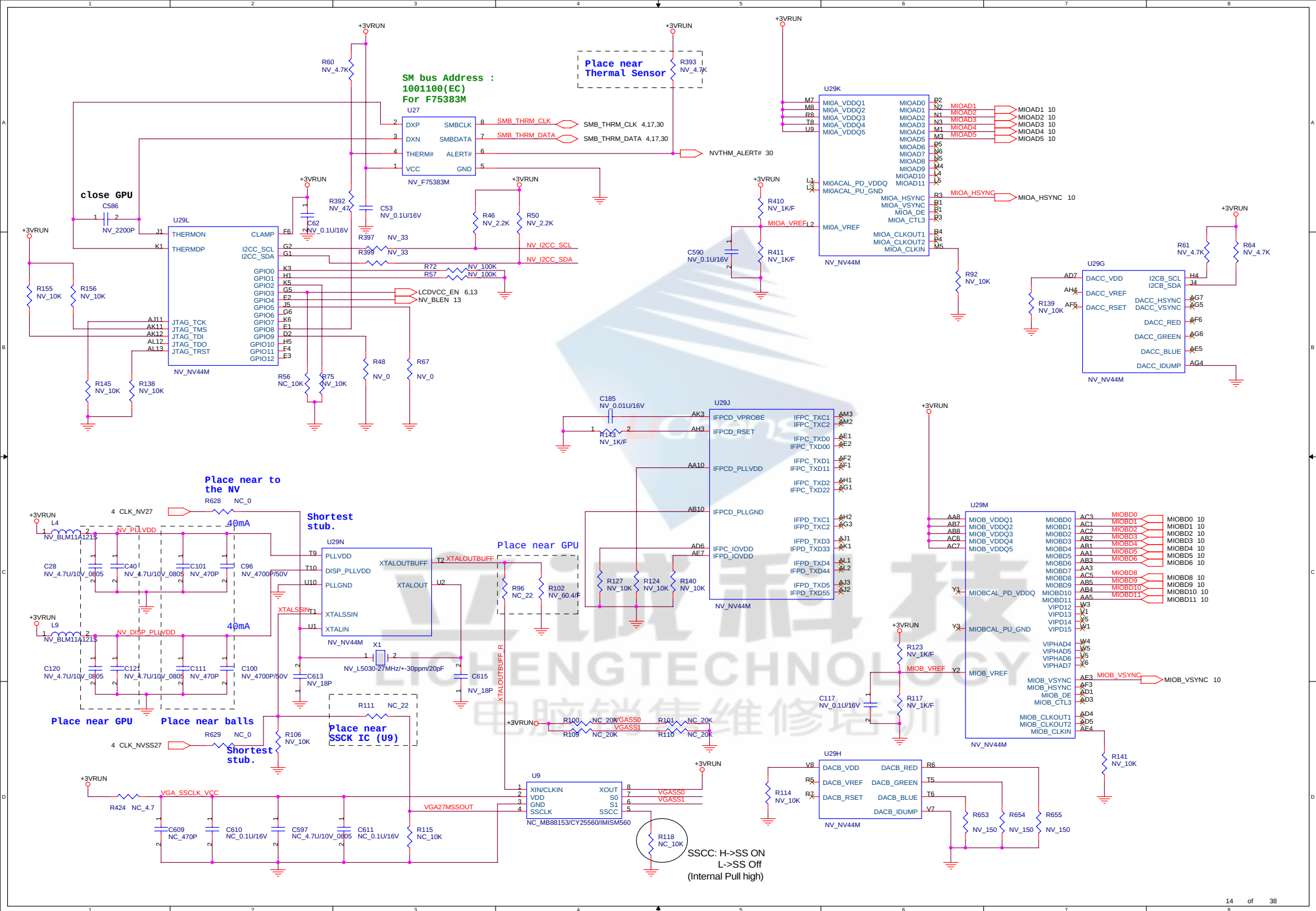


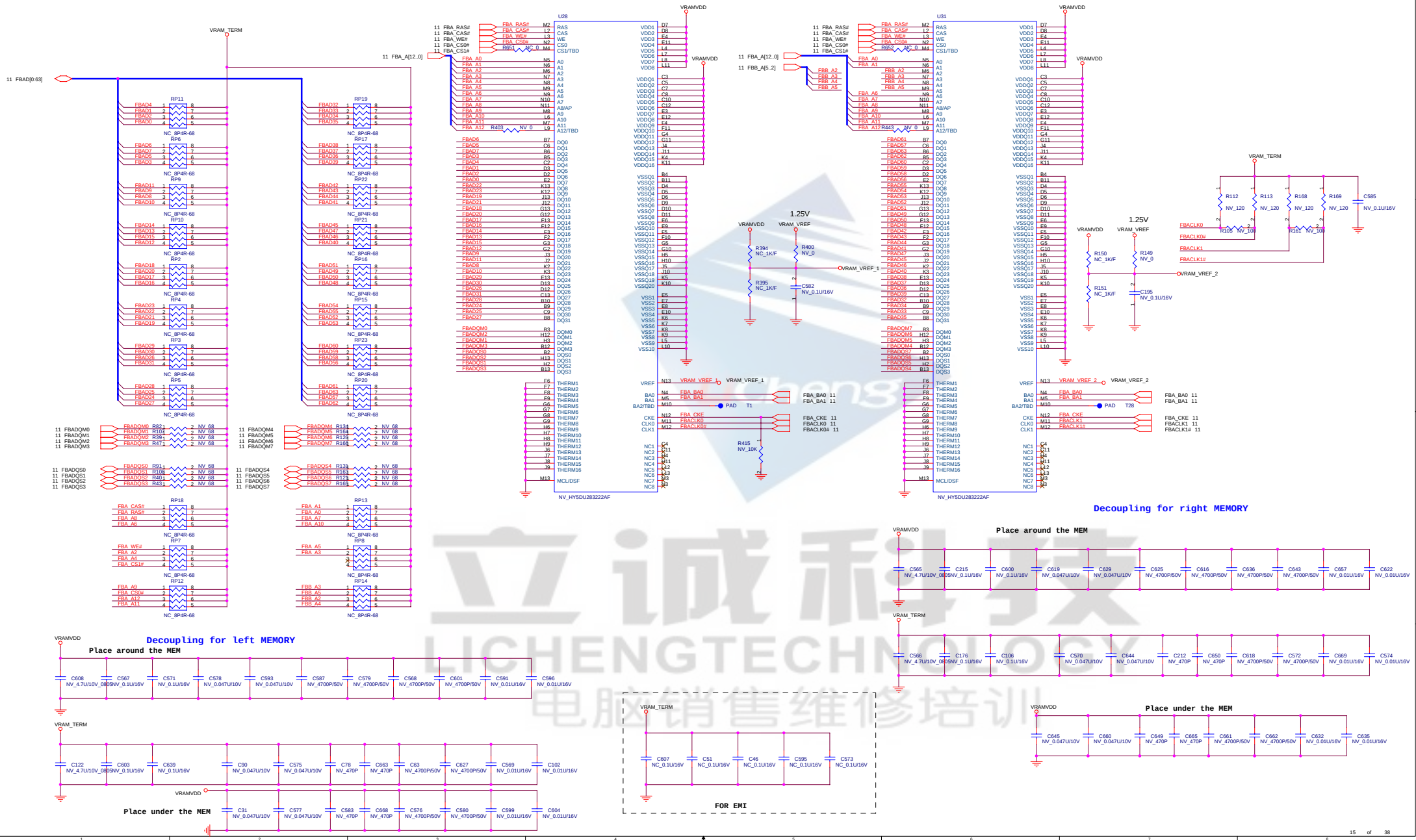
RGB ANALOG SWITCH

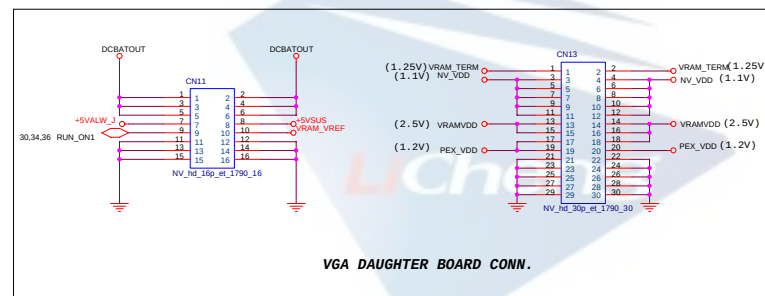


CRT CON

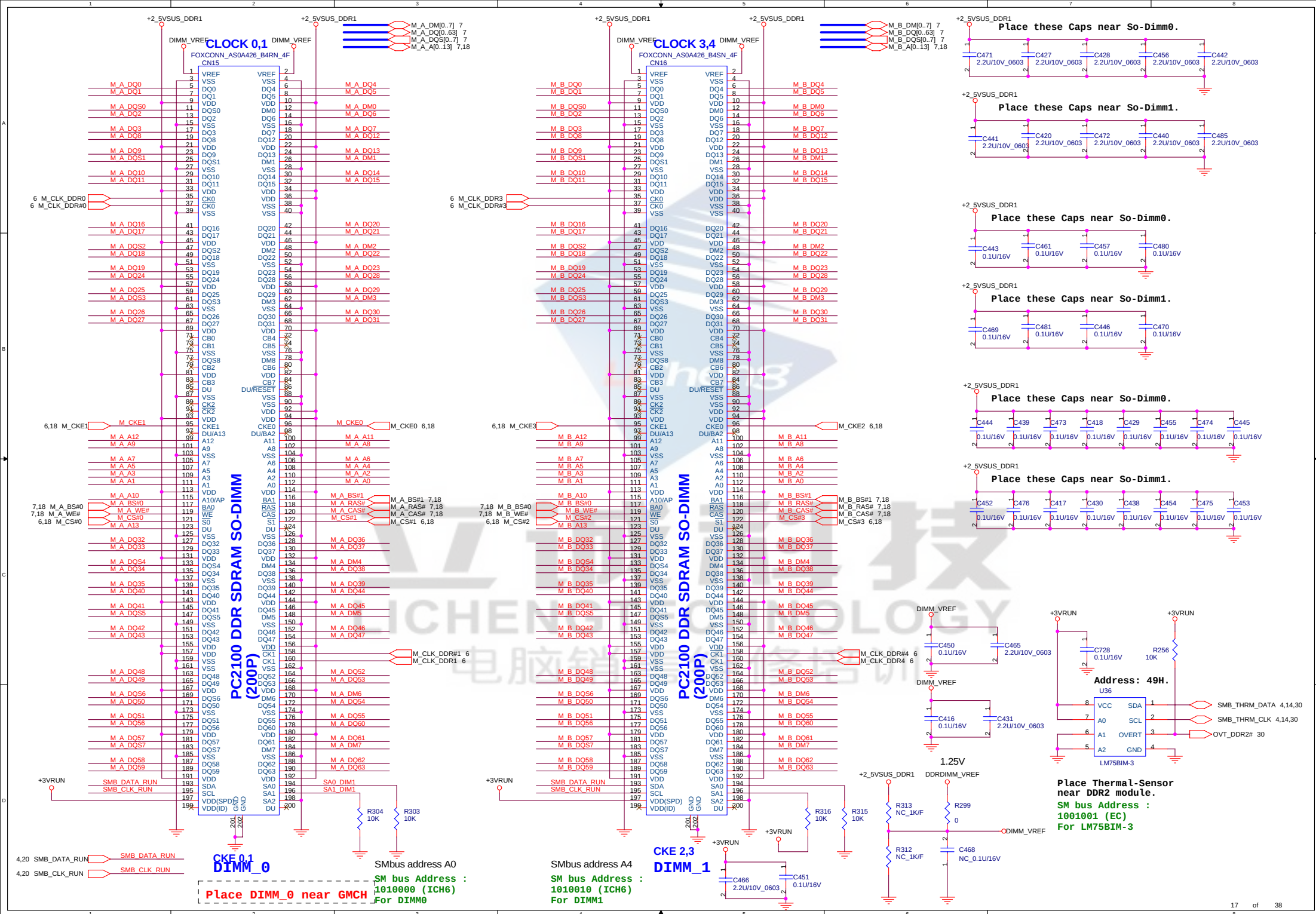
R235, R237, R241 L30, L32, L33
<1000 mils to JVGA1. <500mils to JVGA1.





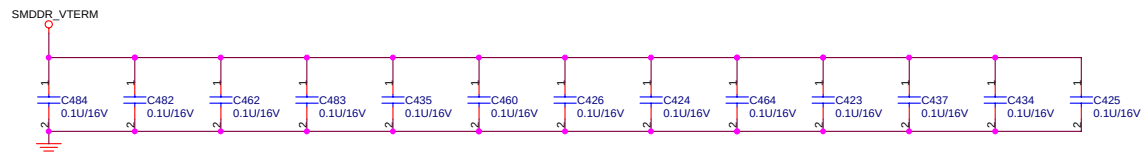


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LICHENGTECHNOLOGY
电脑销售维修培训

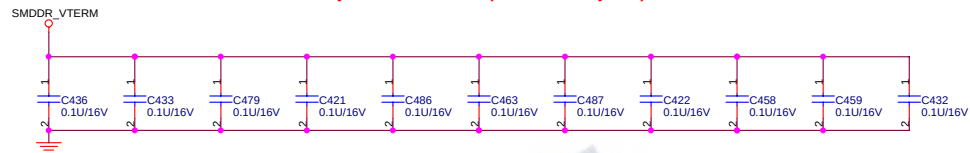


M_A_A[0..13] 7.17

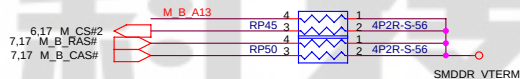
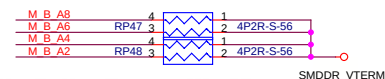
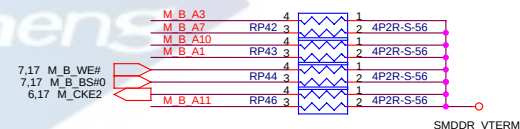
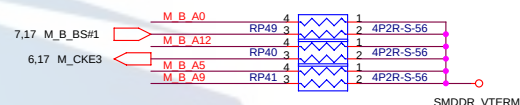
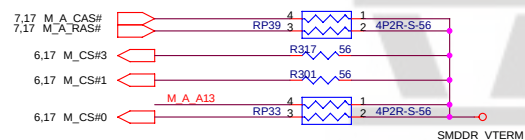
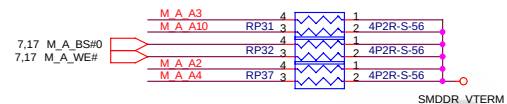
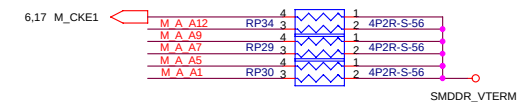
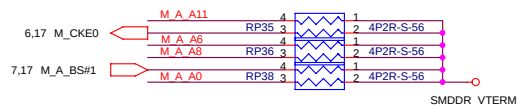
M_B_A[0..13] 7.17



Layout note: Place 1 cap close to every 1 R-pack terminated to SMDR_VTERM.

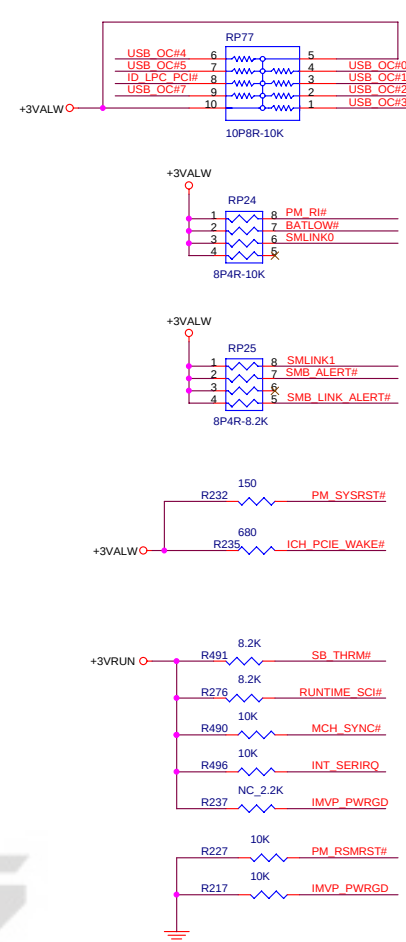
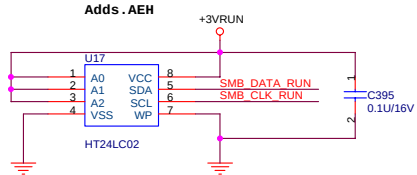
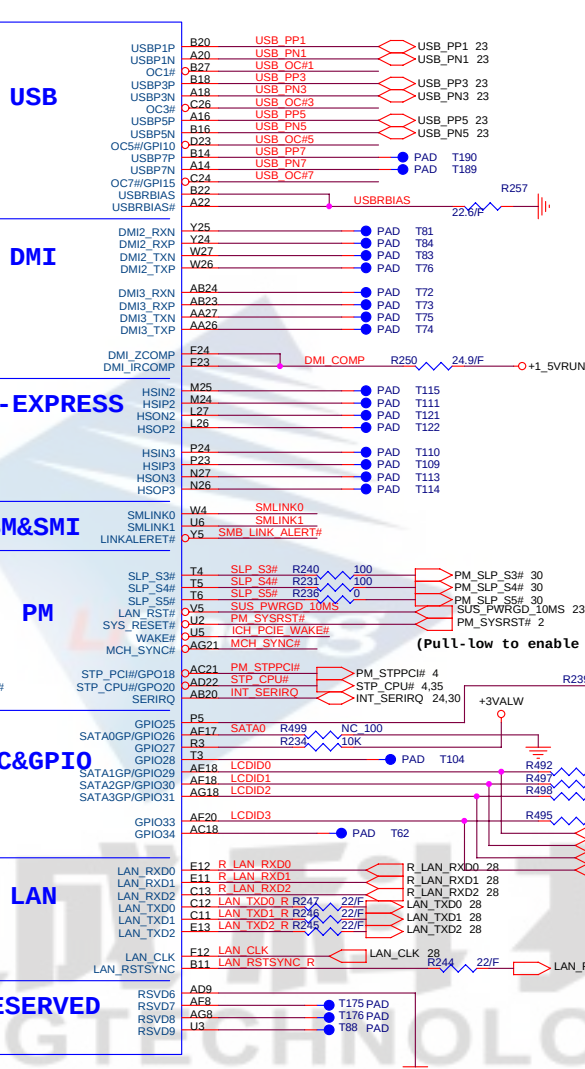
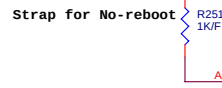
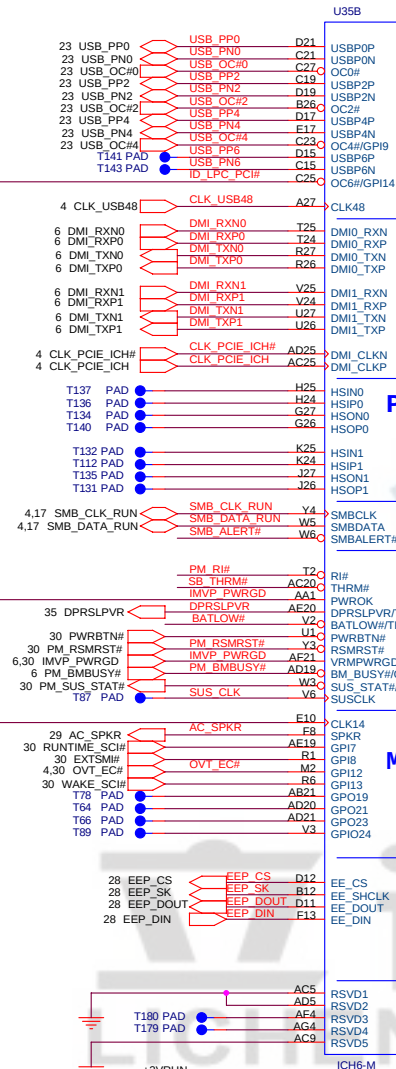
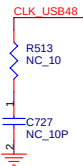
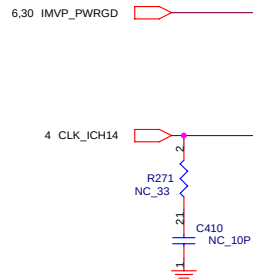


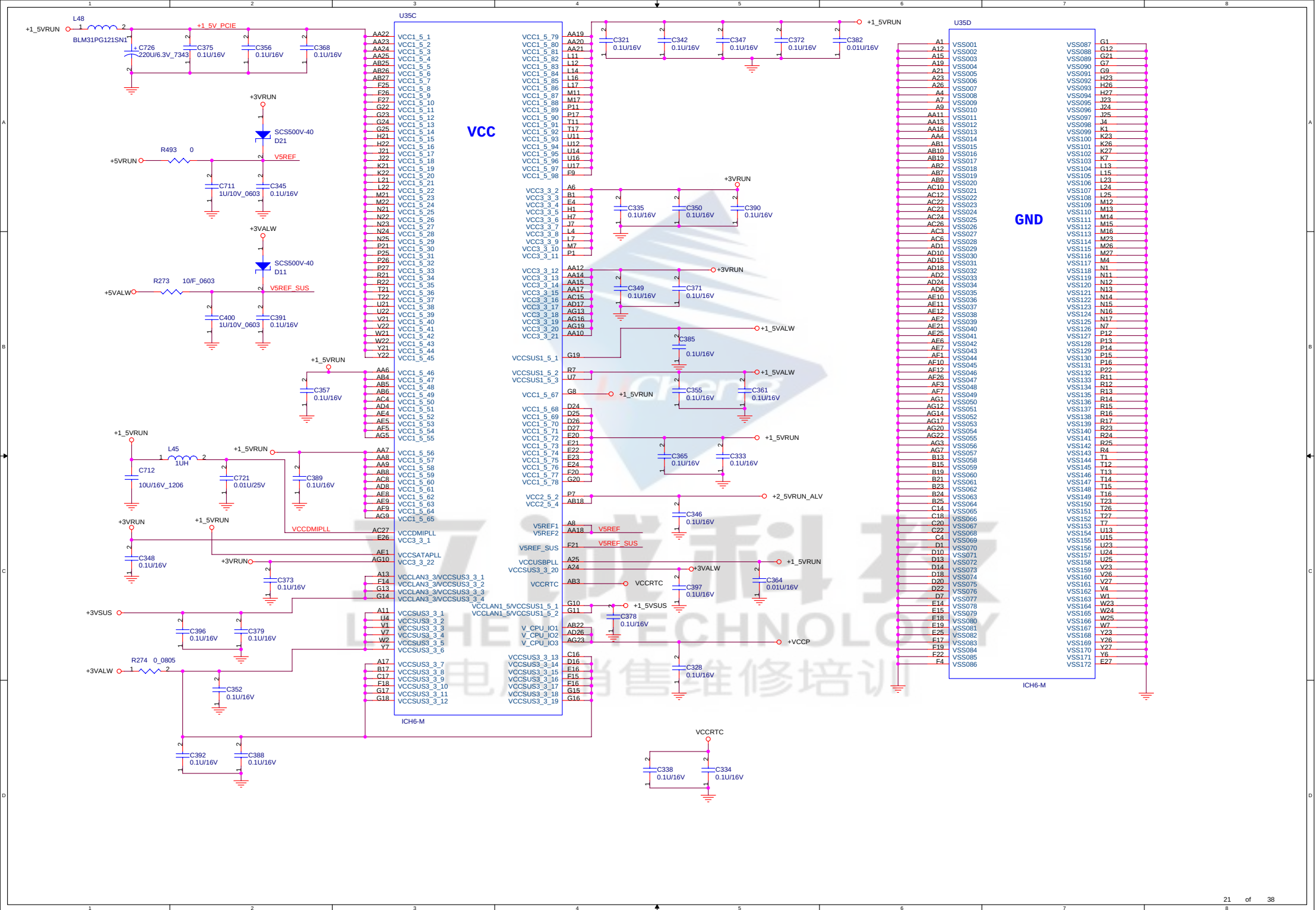
Layout note: Place 1 cap close to every 1 R-pack terminated to SMDR_VTERM.

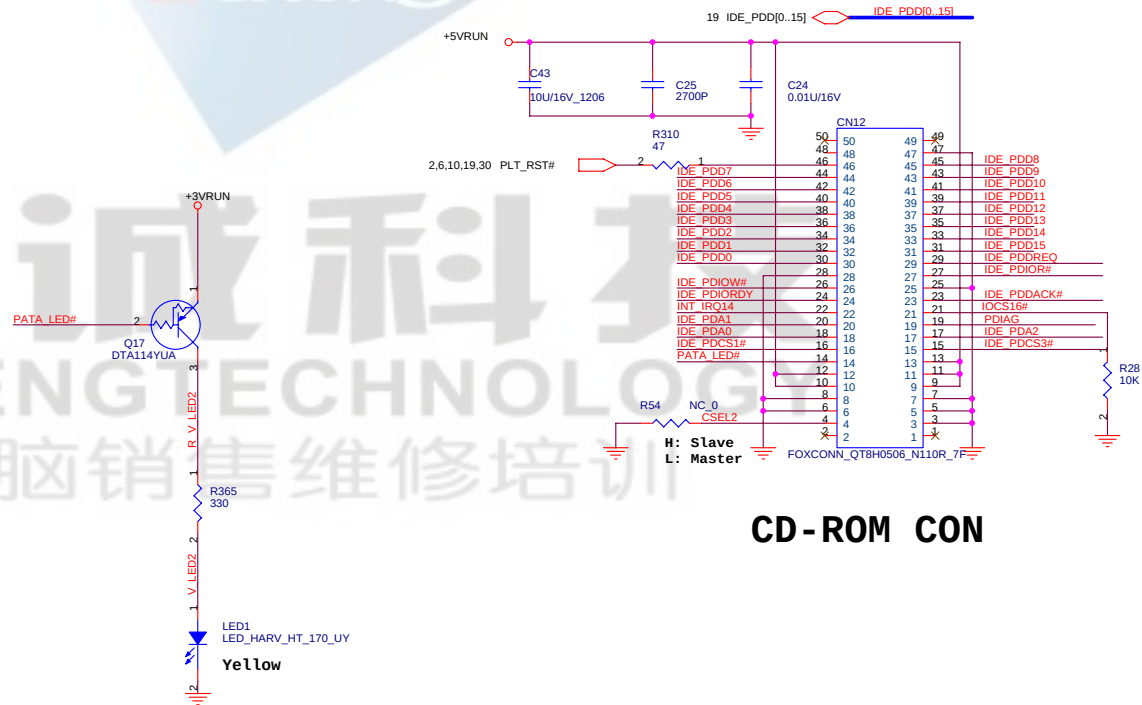
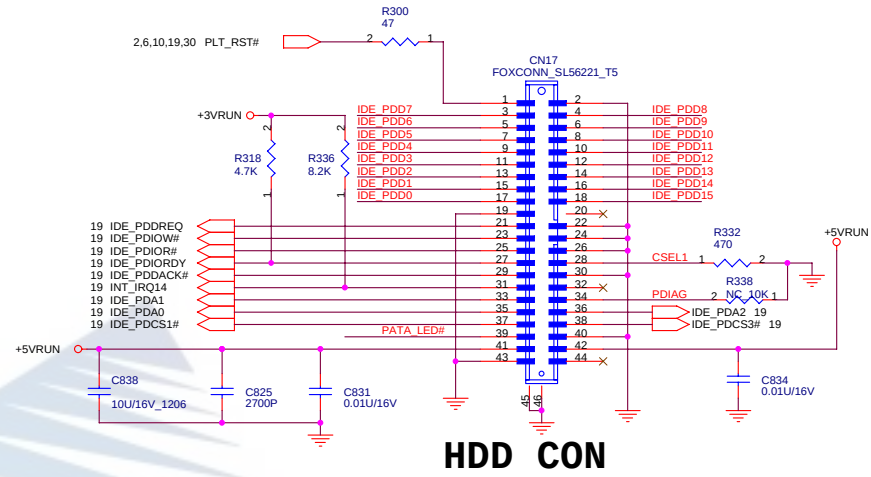


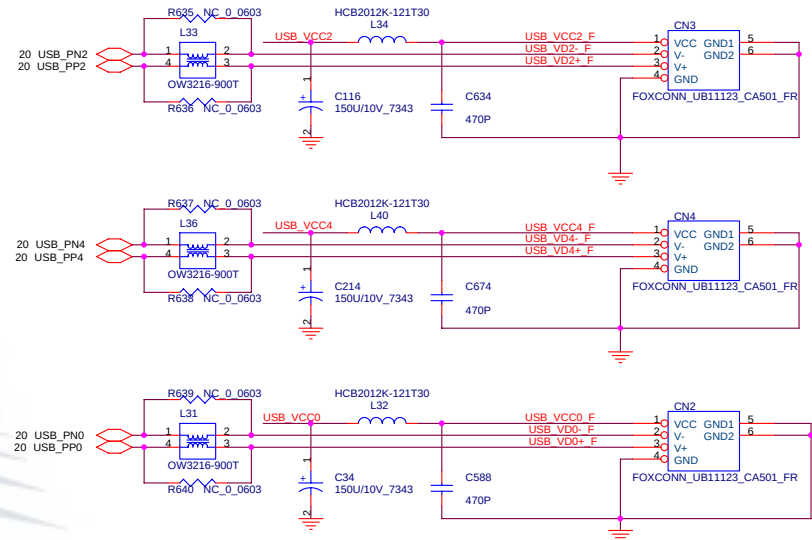


30 ID_LPC_PCI#
80 Port I/F:
H: LCP bus
L: PCI bus

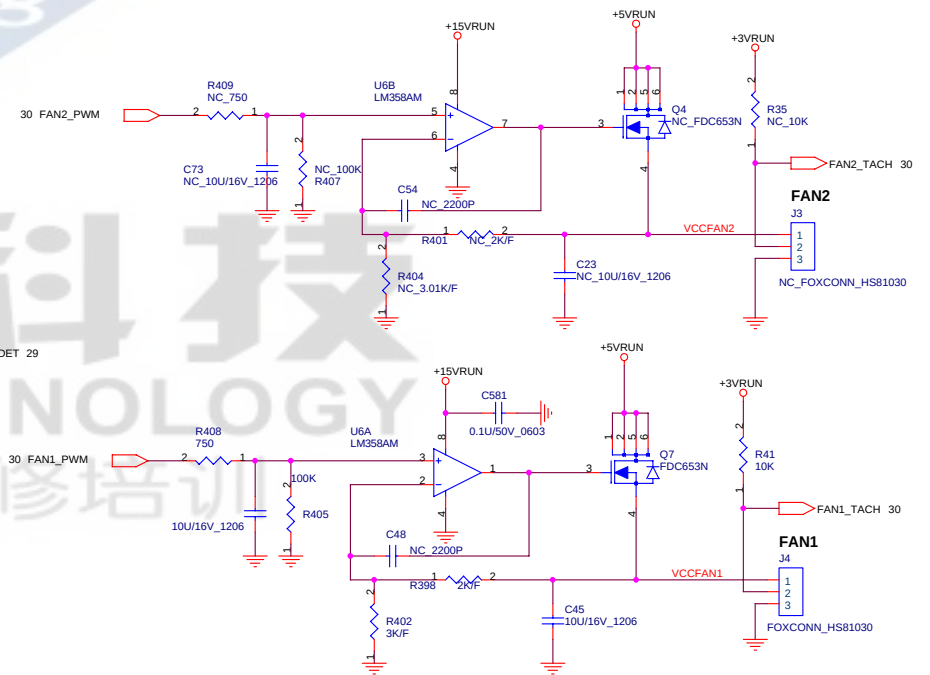
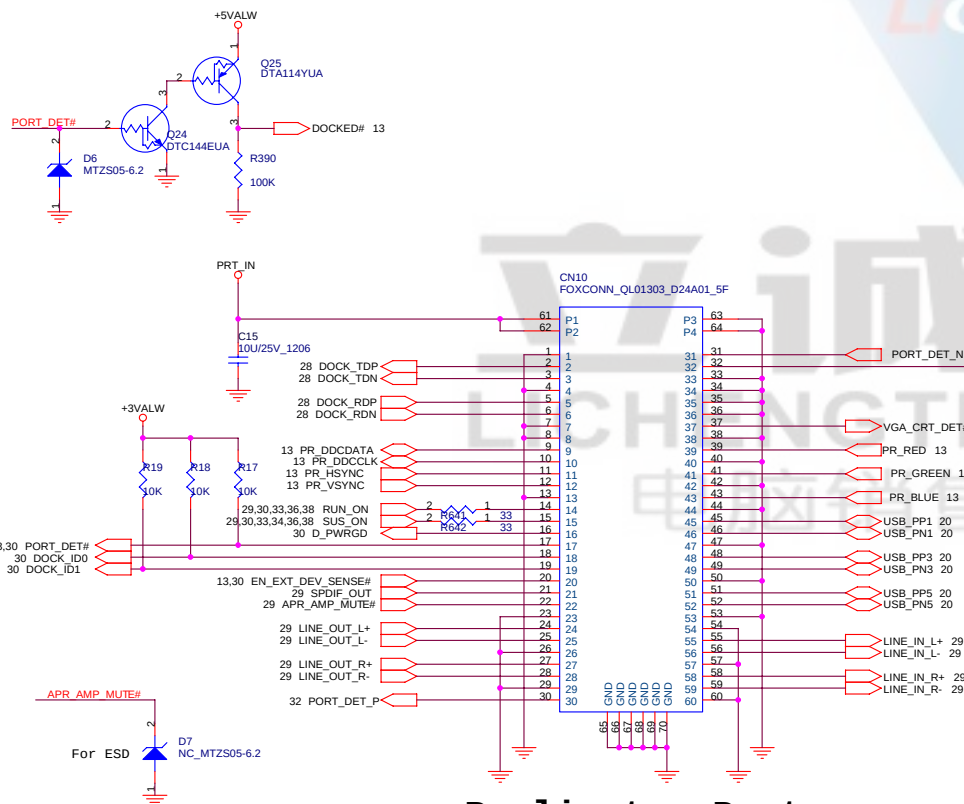




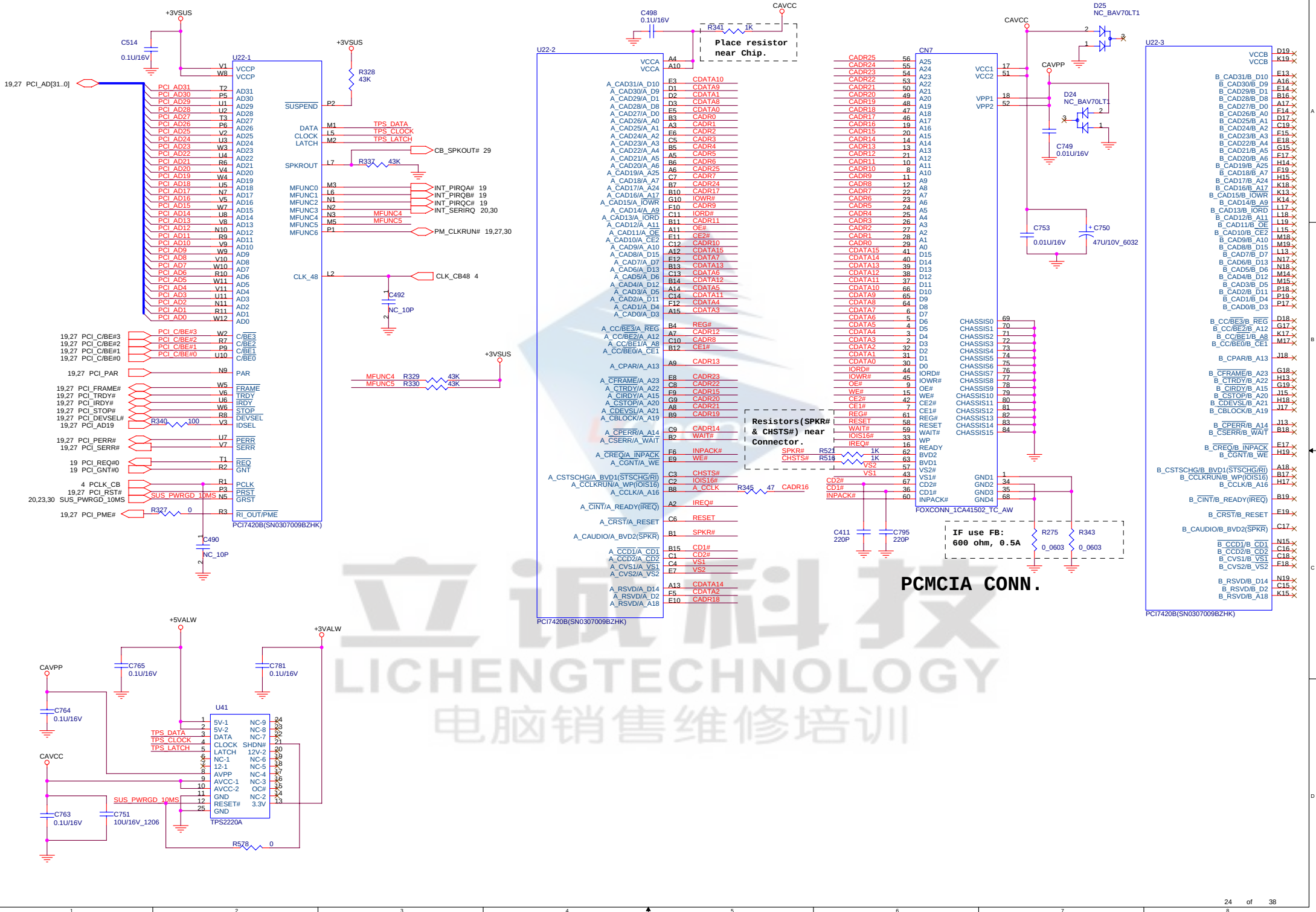




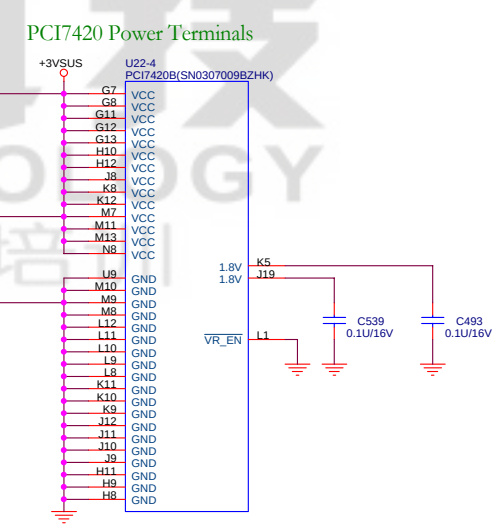
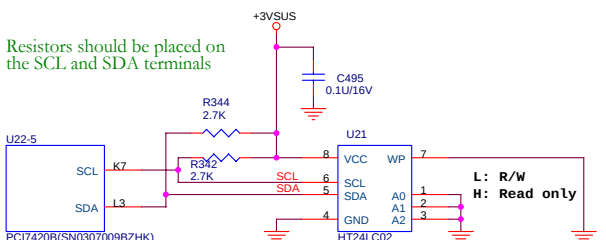
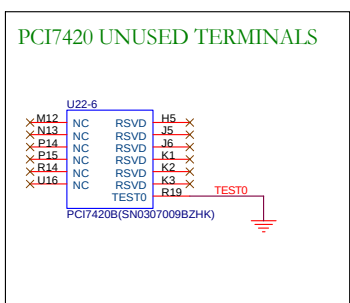
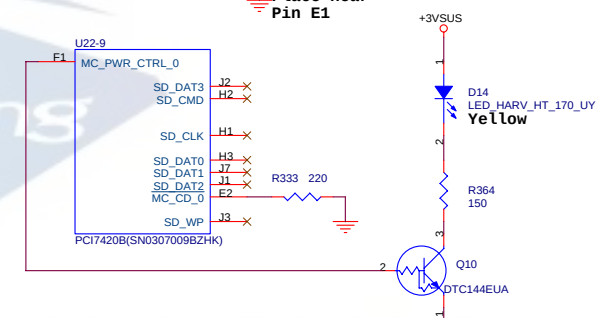
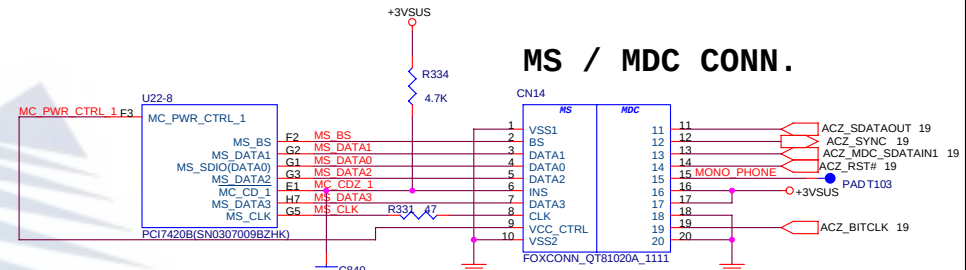
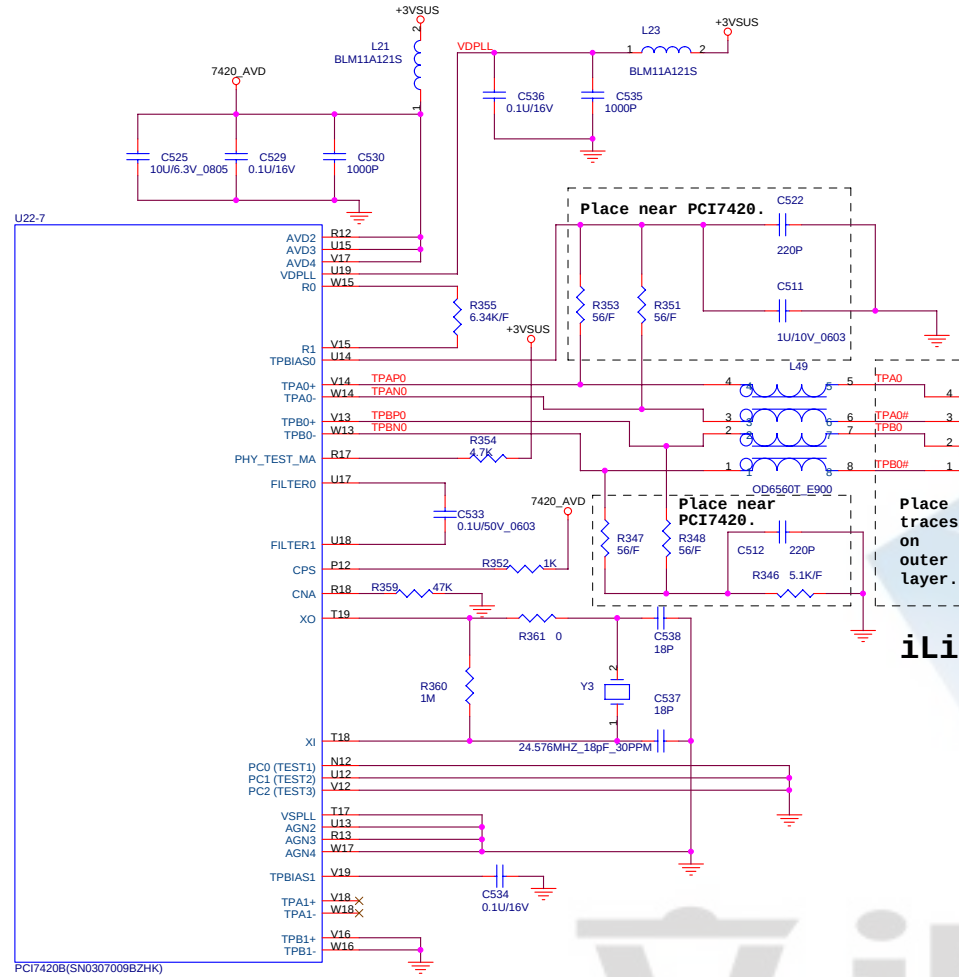
Replicator Port

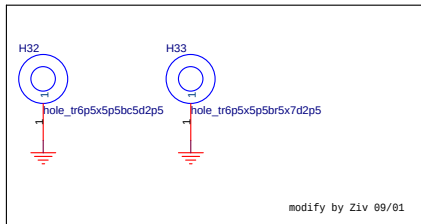
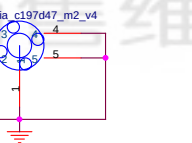
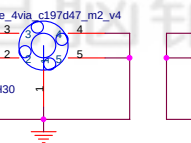
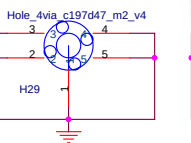
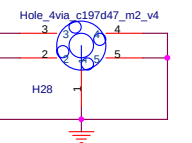
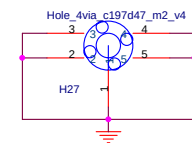
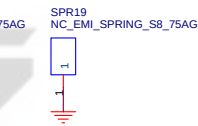
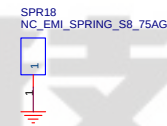
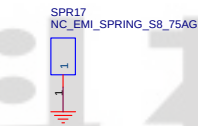
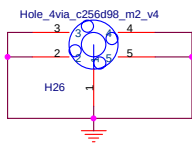
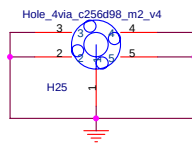
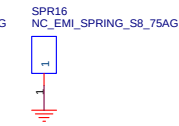
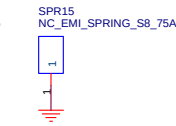
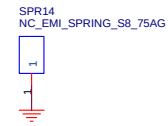
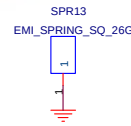
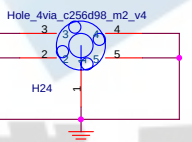
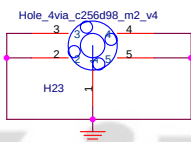
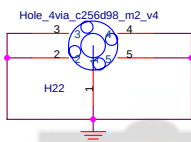
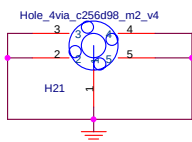
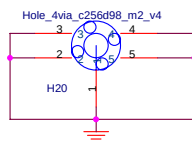
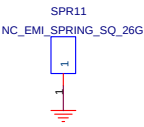
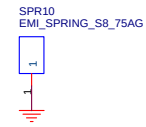
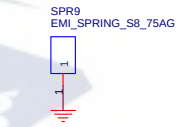
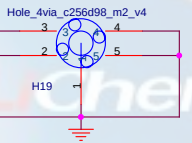
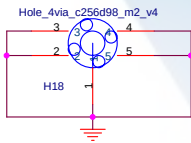
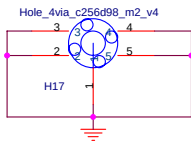
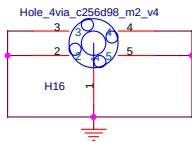
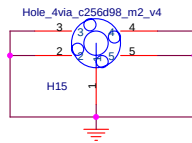
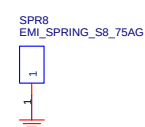
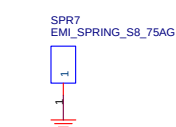
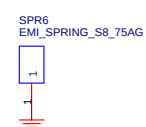
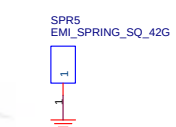
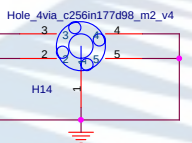
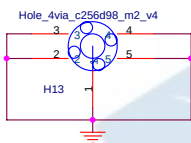
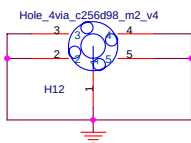
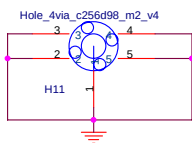
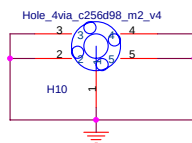
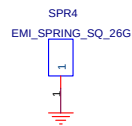
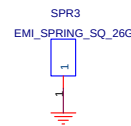
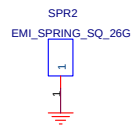
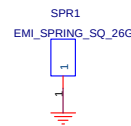
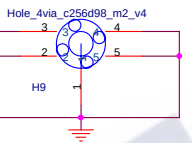
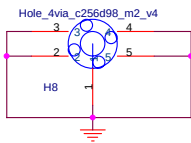
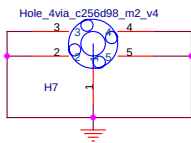
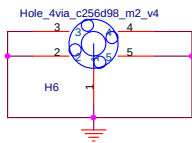
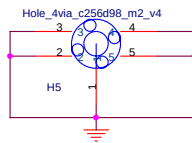
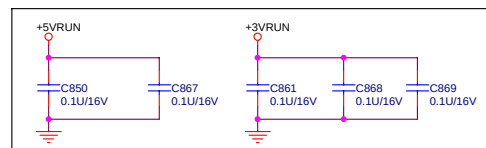


FAN

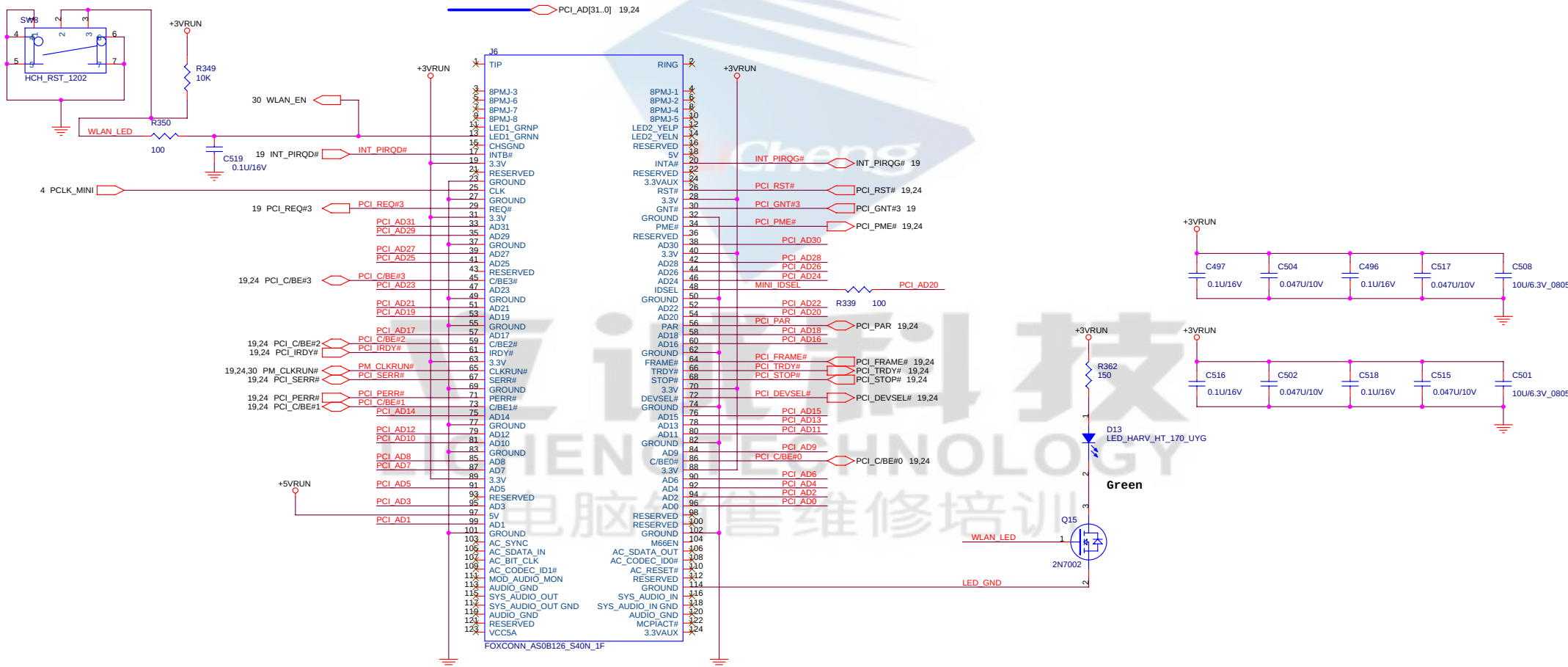


PCMCIA CONN.





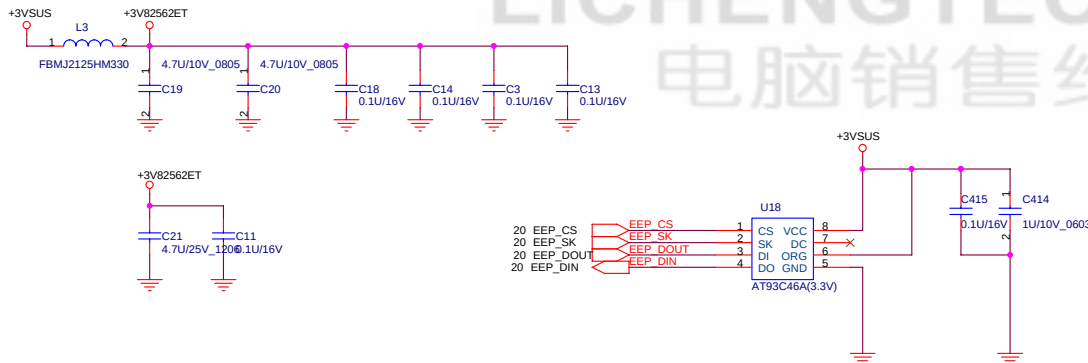
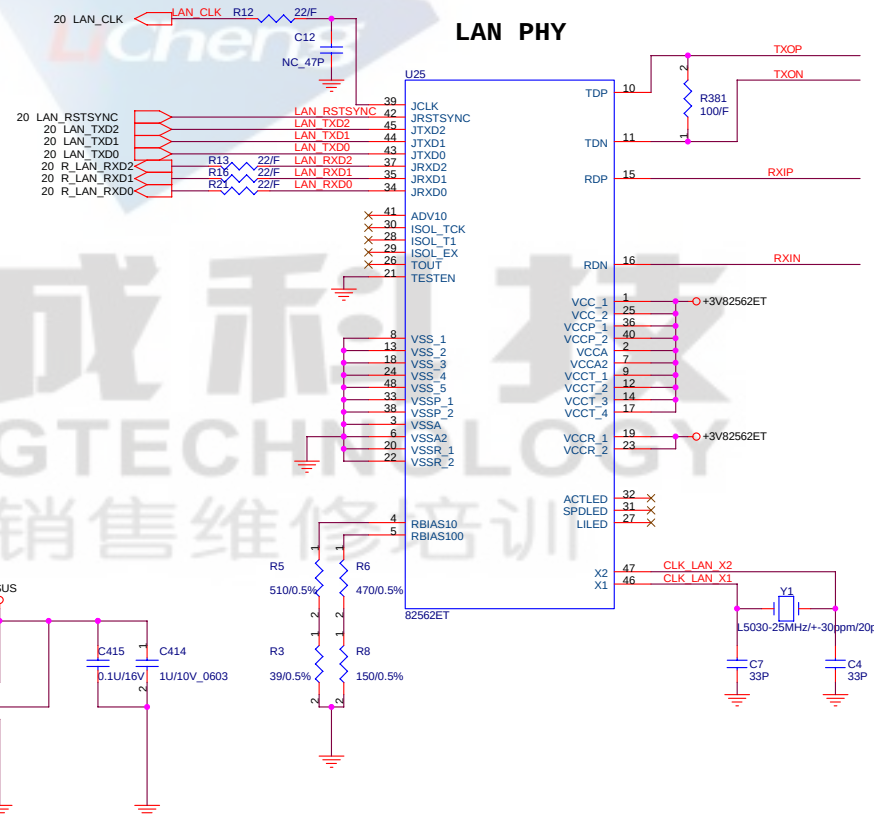
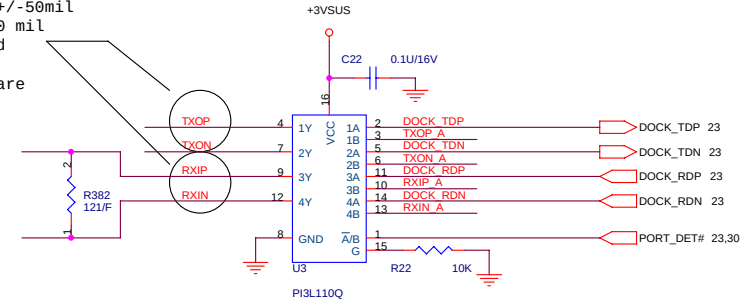
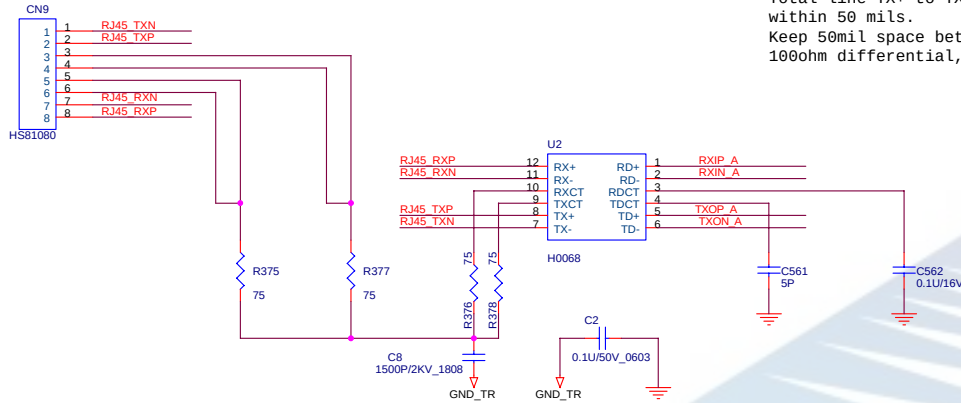
立诚科技
LICHENGTECHNOLOGY
电脑销售维修培训

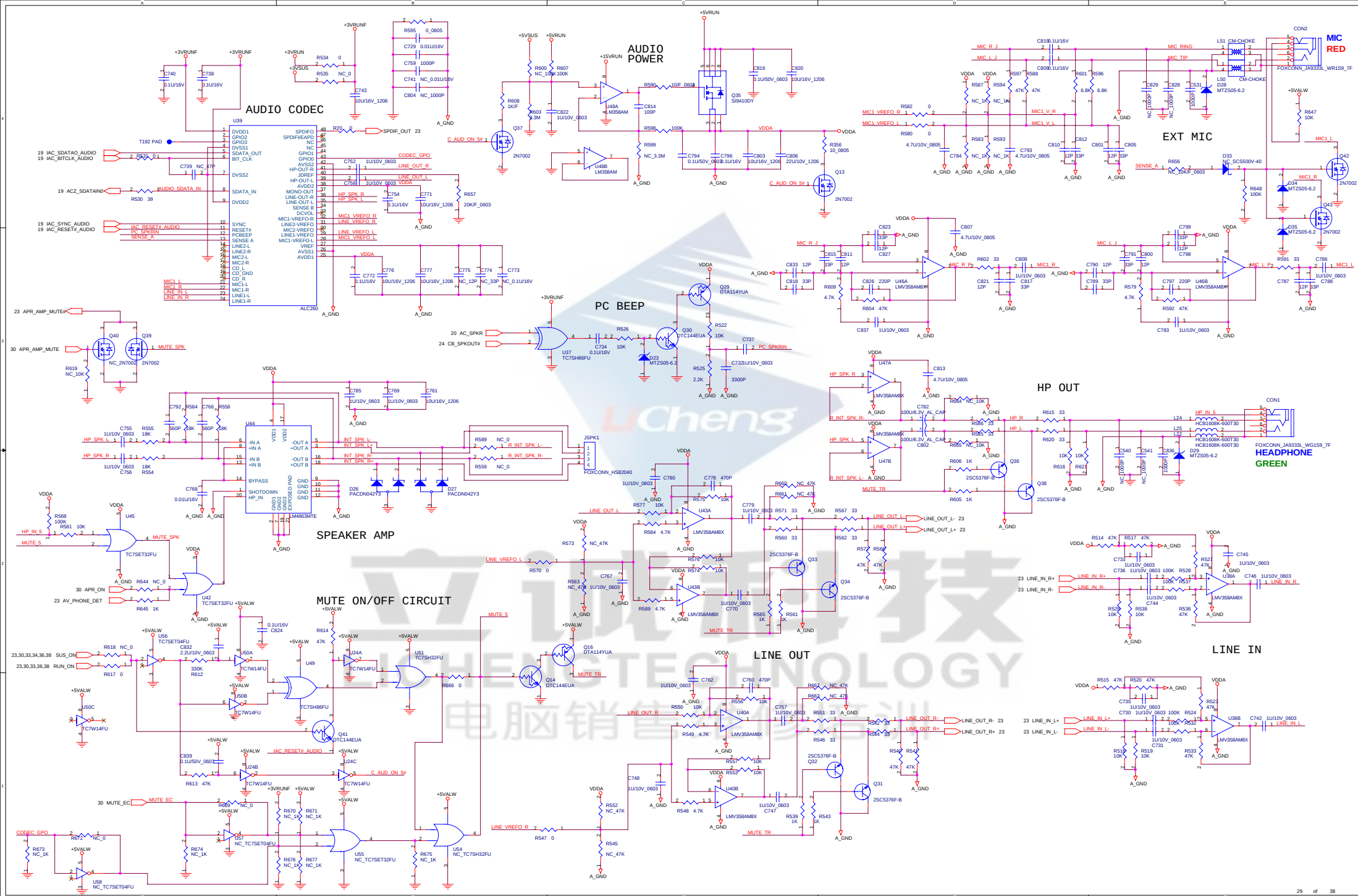


Match trace length

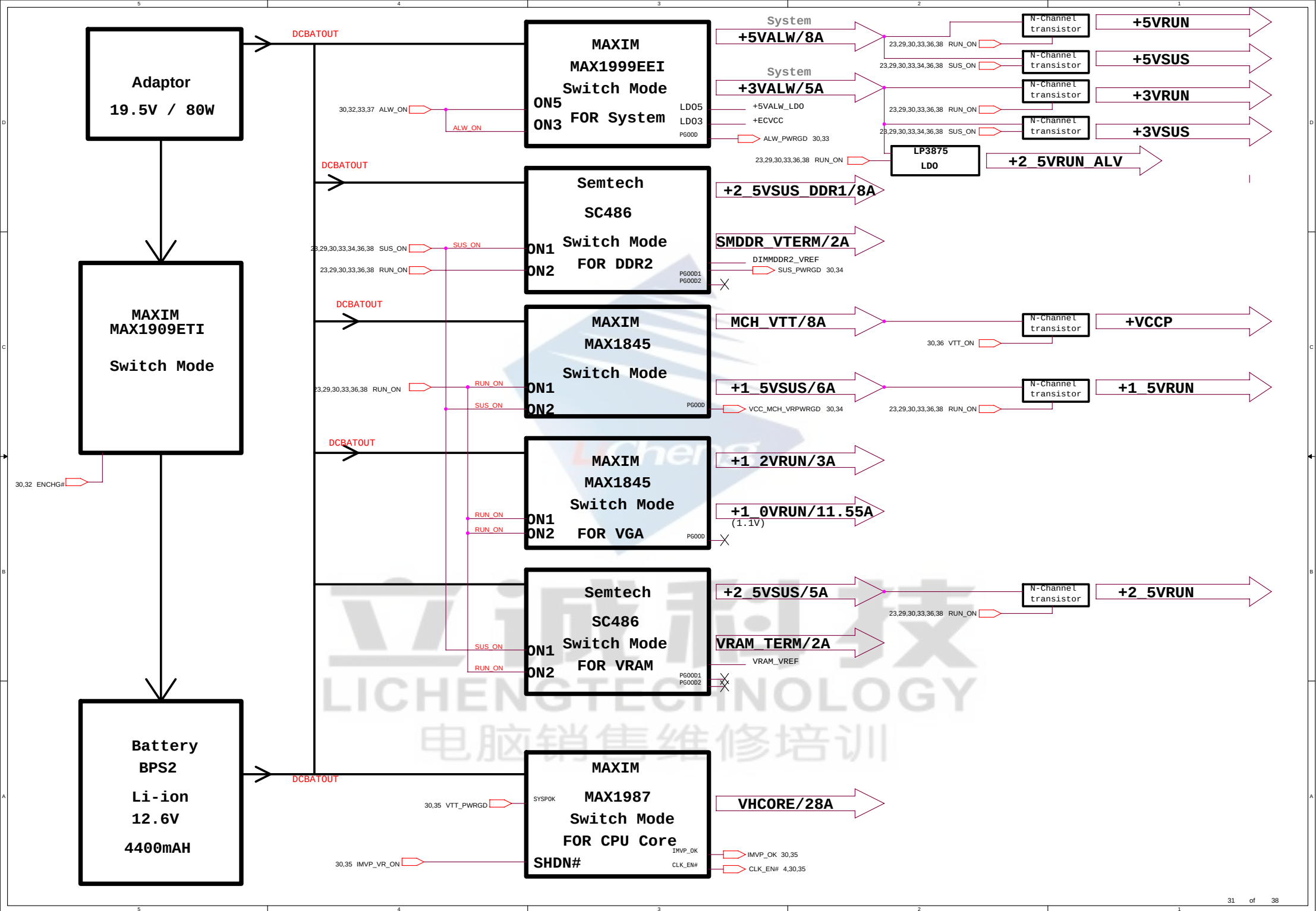
LAYOUT NOTES:

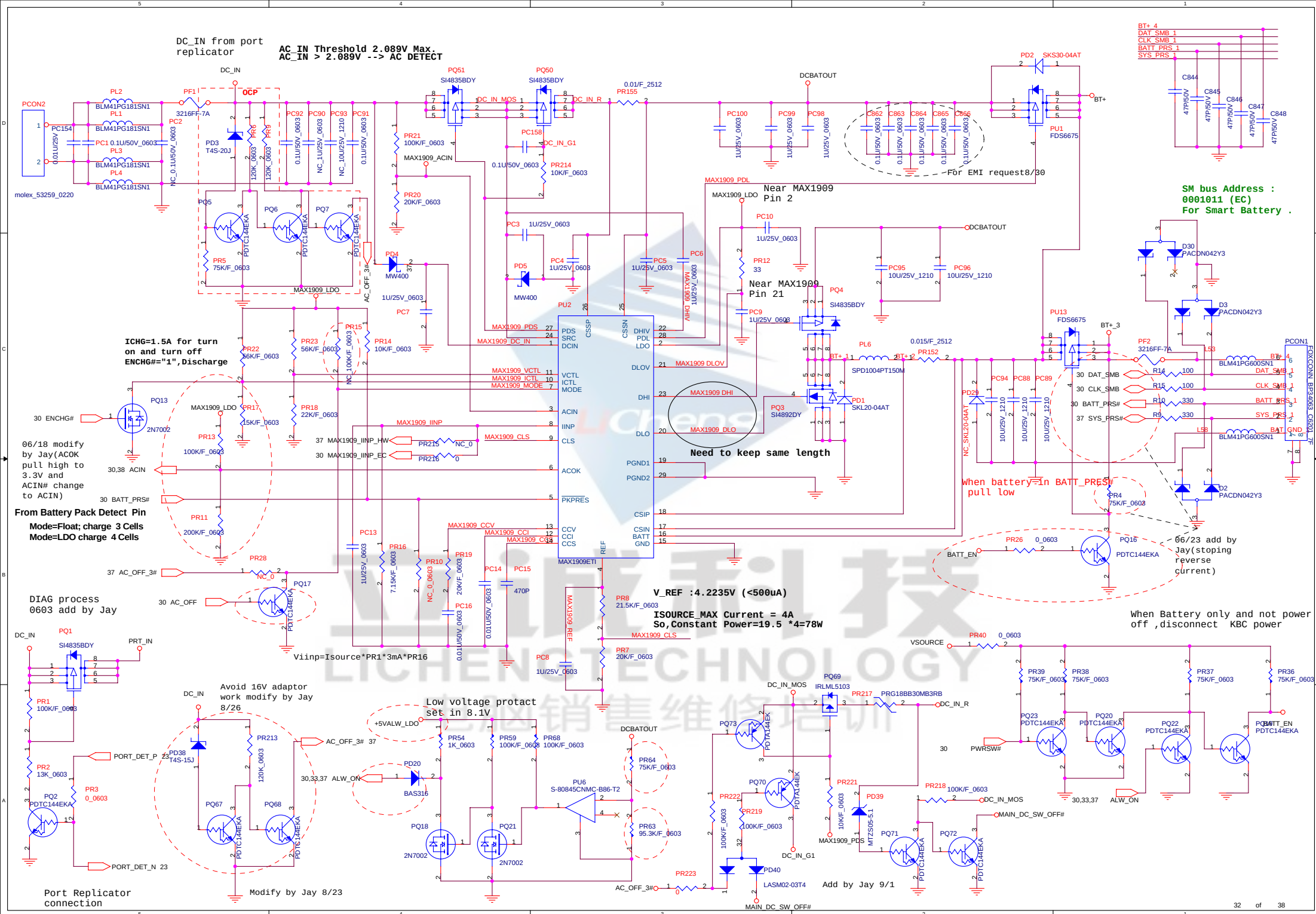
Match total length of chip side Rx and Tx pair traces +/-50mil
Match length of cable side Rx and Tx pair traces +/- 50 mil
Total line TX+ to TX- and RX- and RX+ should be matched within 50 mils.
Keep 50mil space between pairs and other traces.Pairs are 100ohm differential,

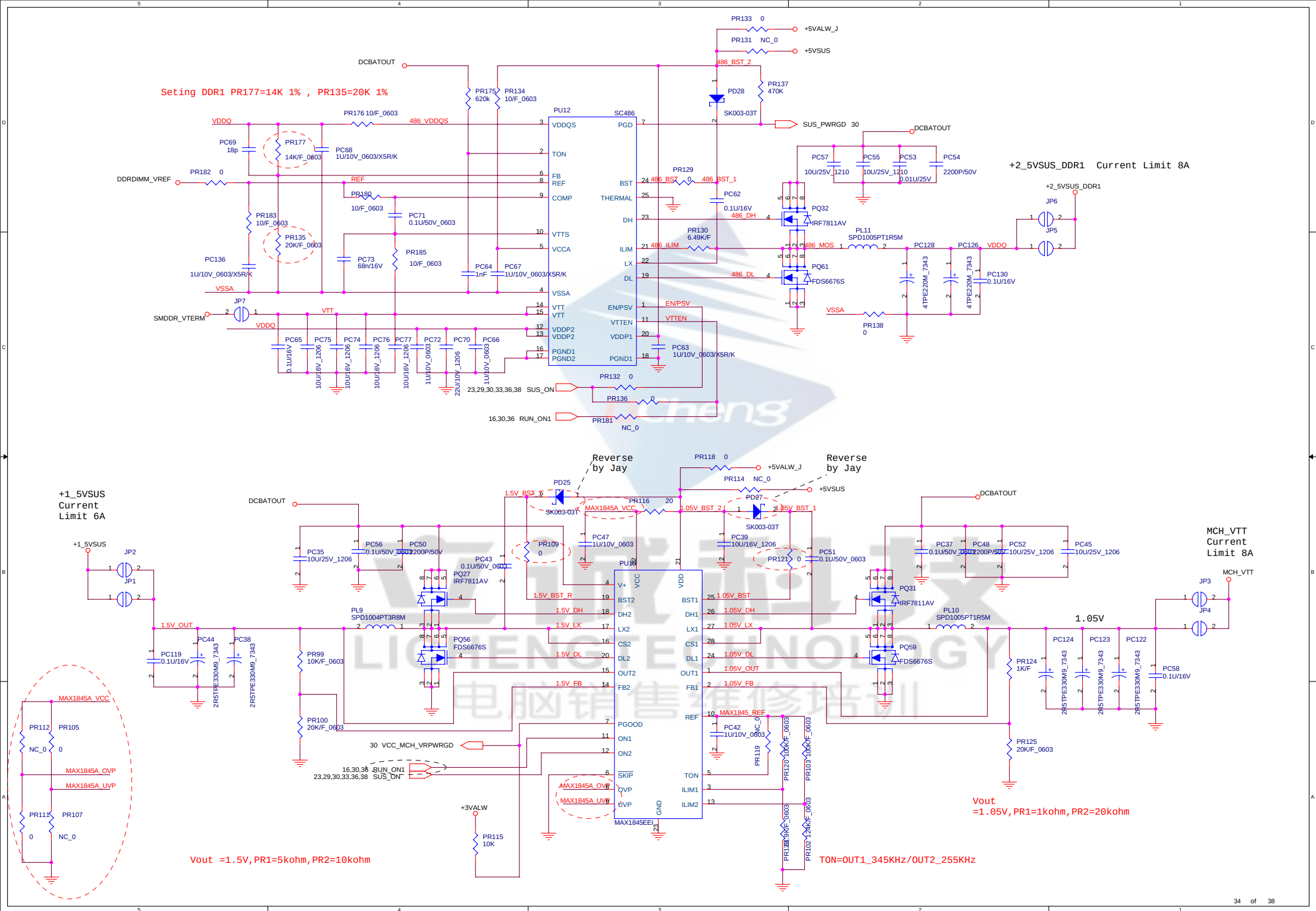












Setting DDR1 PR177=14K 1% , PR135=20K 1%

+2_5VSUS_DDR1 Current Limit 8A

+1_5VSUS Current Limit 6A

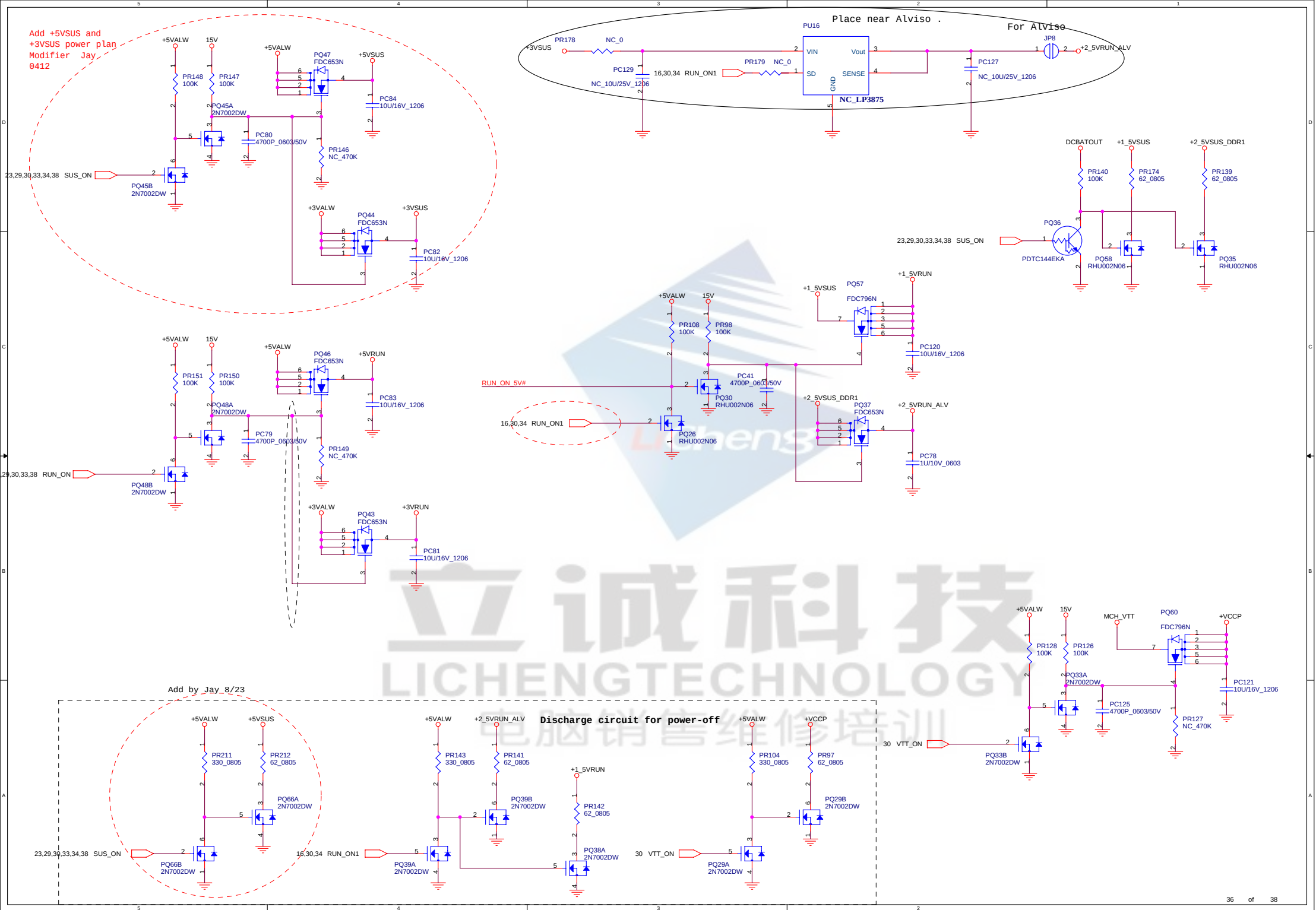
MCH_VTT Current Limit 8A

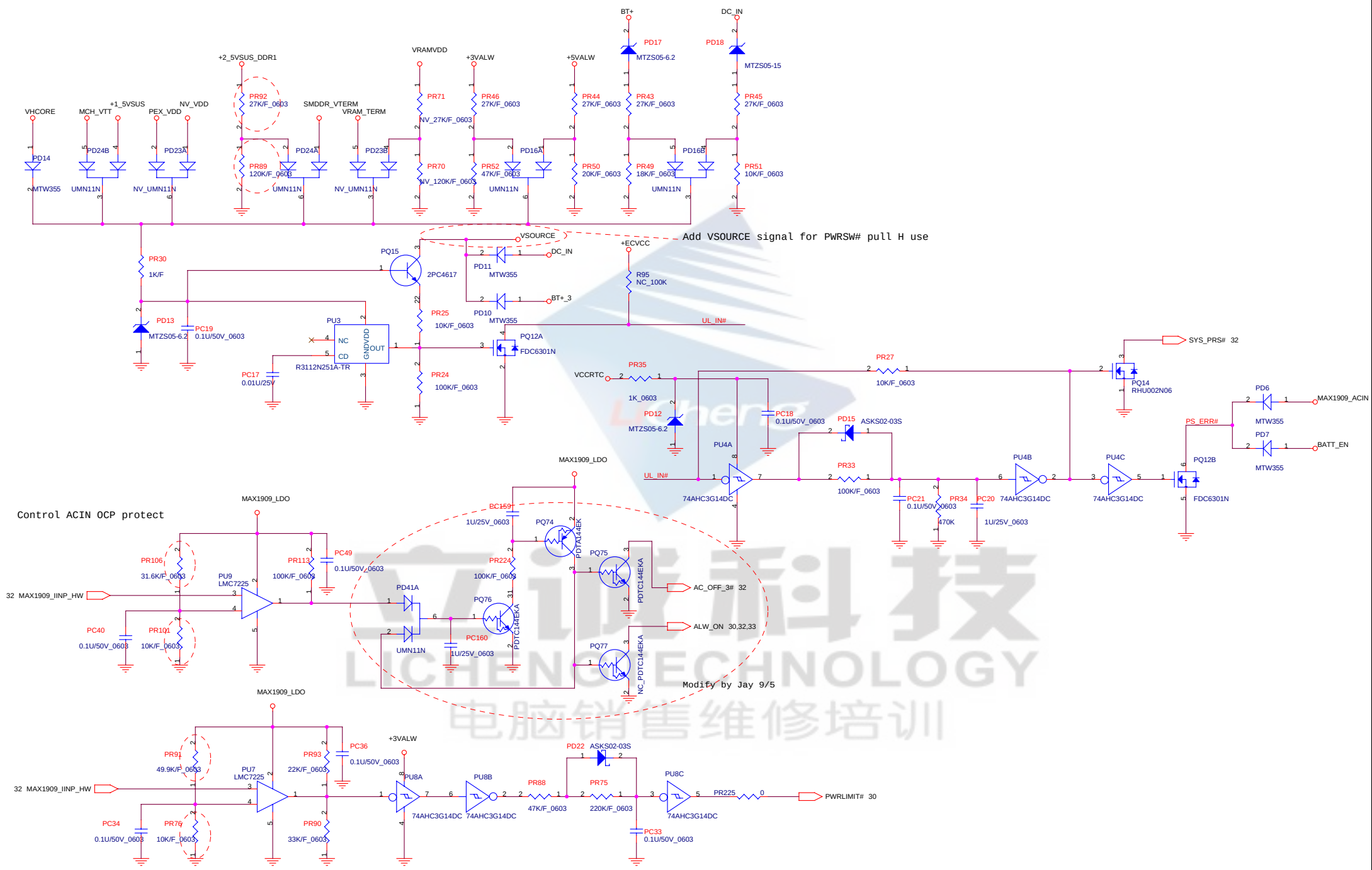
Vout =1.5V, PR1=5kohm, PR2=10kohm

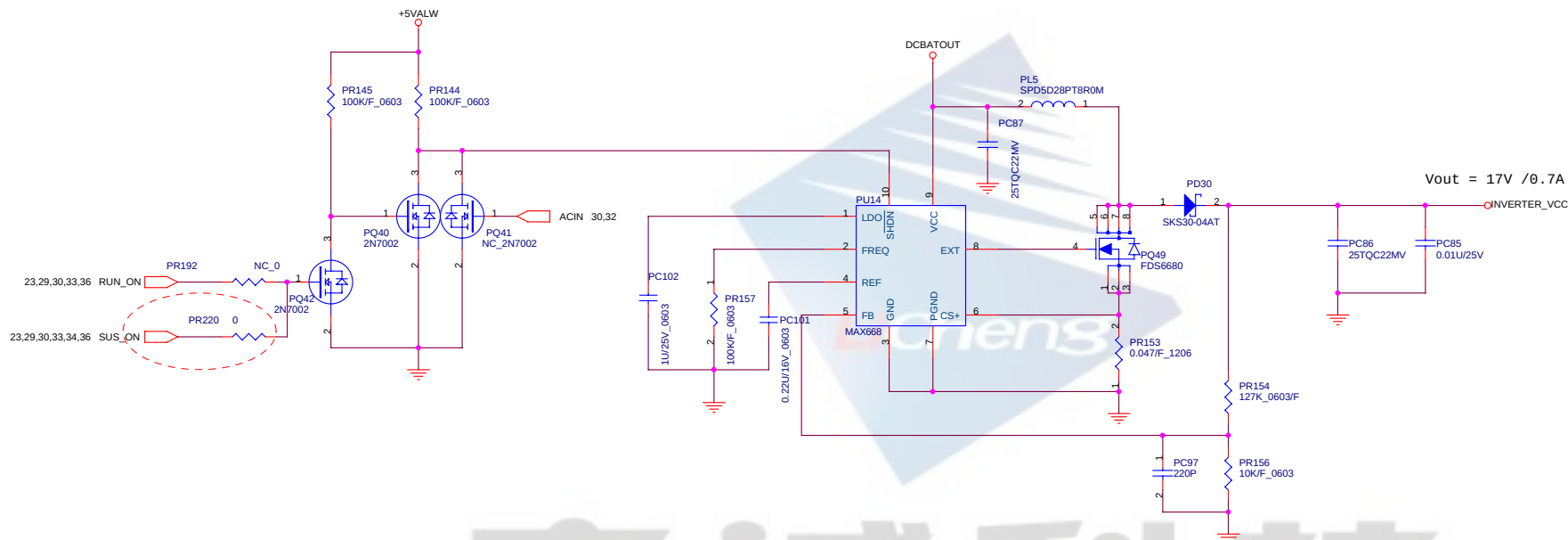
Vout =1.05V, PR1=1kohm, PR2=20kohm

TON=OUT1_345KHz/OUT2_255KHz

Add +5VSUS and
+3VSUS power plan
Modifier Jay
0412







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