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8. Block diagram and Schematic

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CANNES-L

CPU : Intel Penryn
Chip Set : Intel Cantiga & ICH9M
Remarks : Montevina Platform

Model Name : R719
PBA Name : MAIN
PCB Code : GCE :
 NAN :
 HAN :
Dev. Step : PV
Revision : 1.0
T.R. Date : 2009.06.04

Design	CHECK	APPROVAL

■ Owner : SEC Mobile R & D Signature : X

DATE	BY	REVISION	TITLE	SAMSUNG ELECTRONICS
2009.06.04	YJLH	PV	CANNES-L MAIN COVER	
2009.06.04	YJLH	SP		
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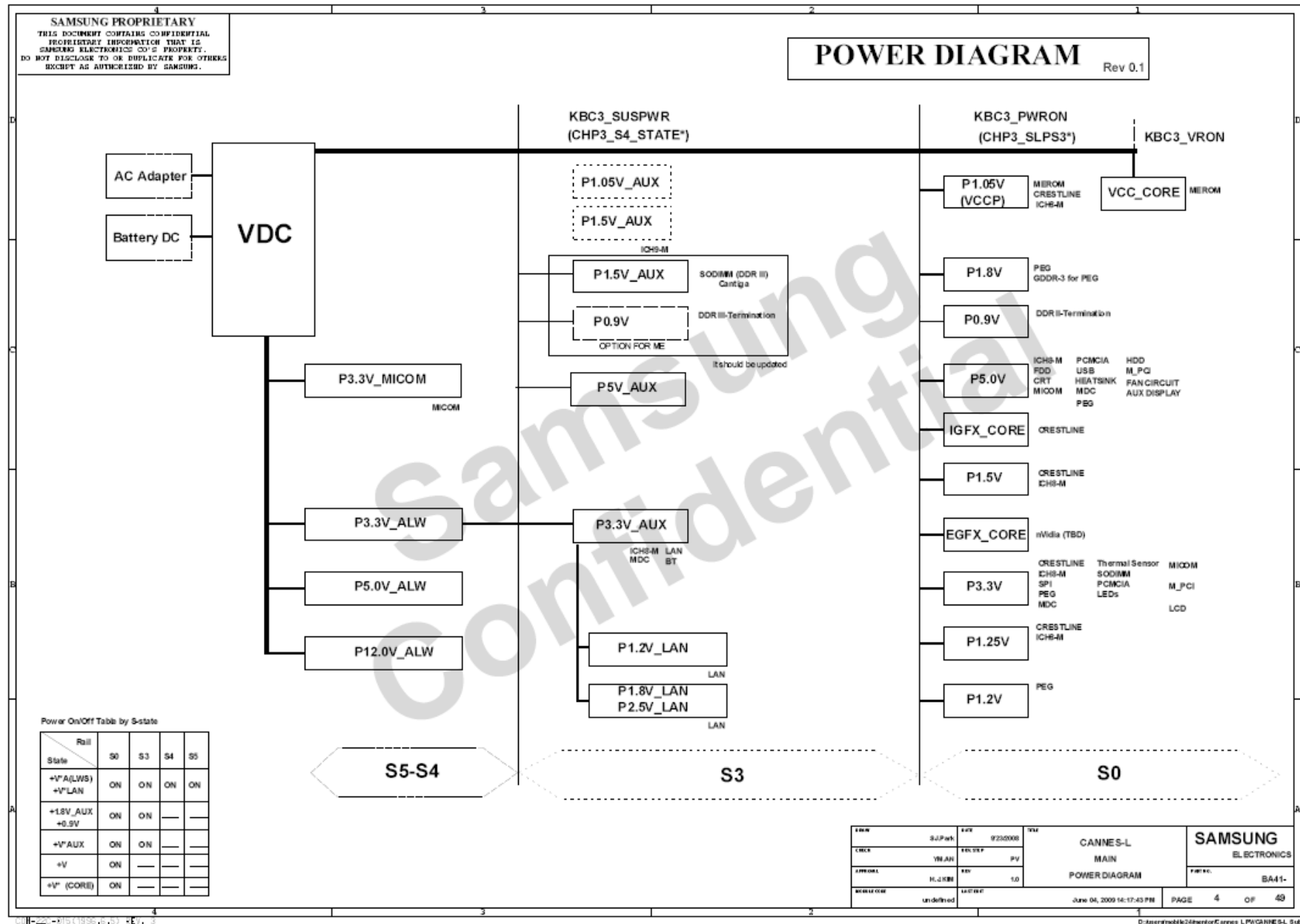
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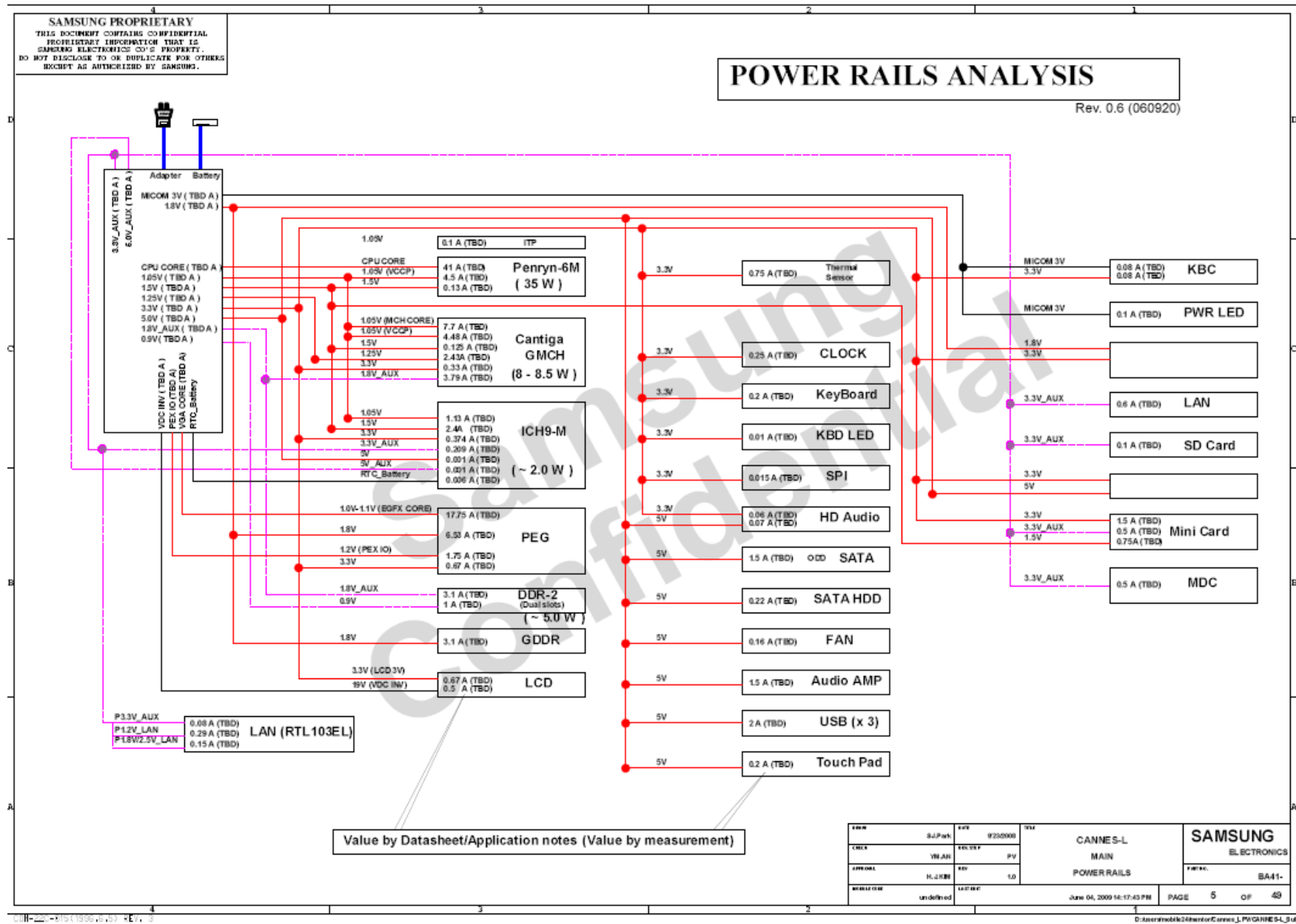


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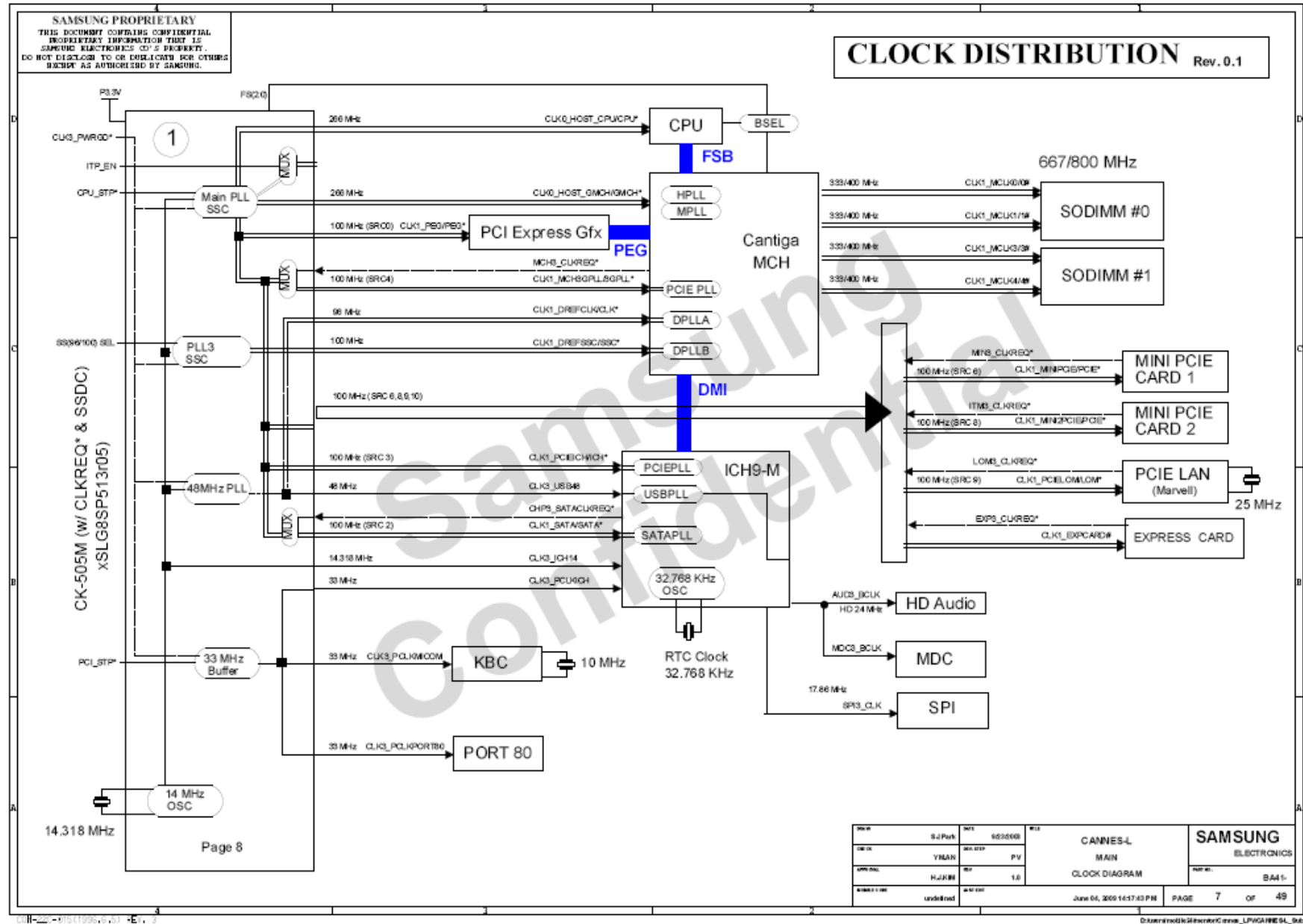
8. Block diagram and Schematic



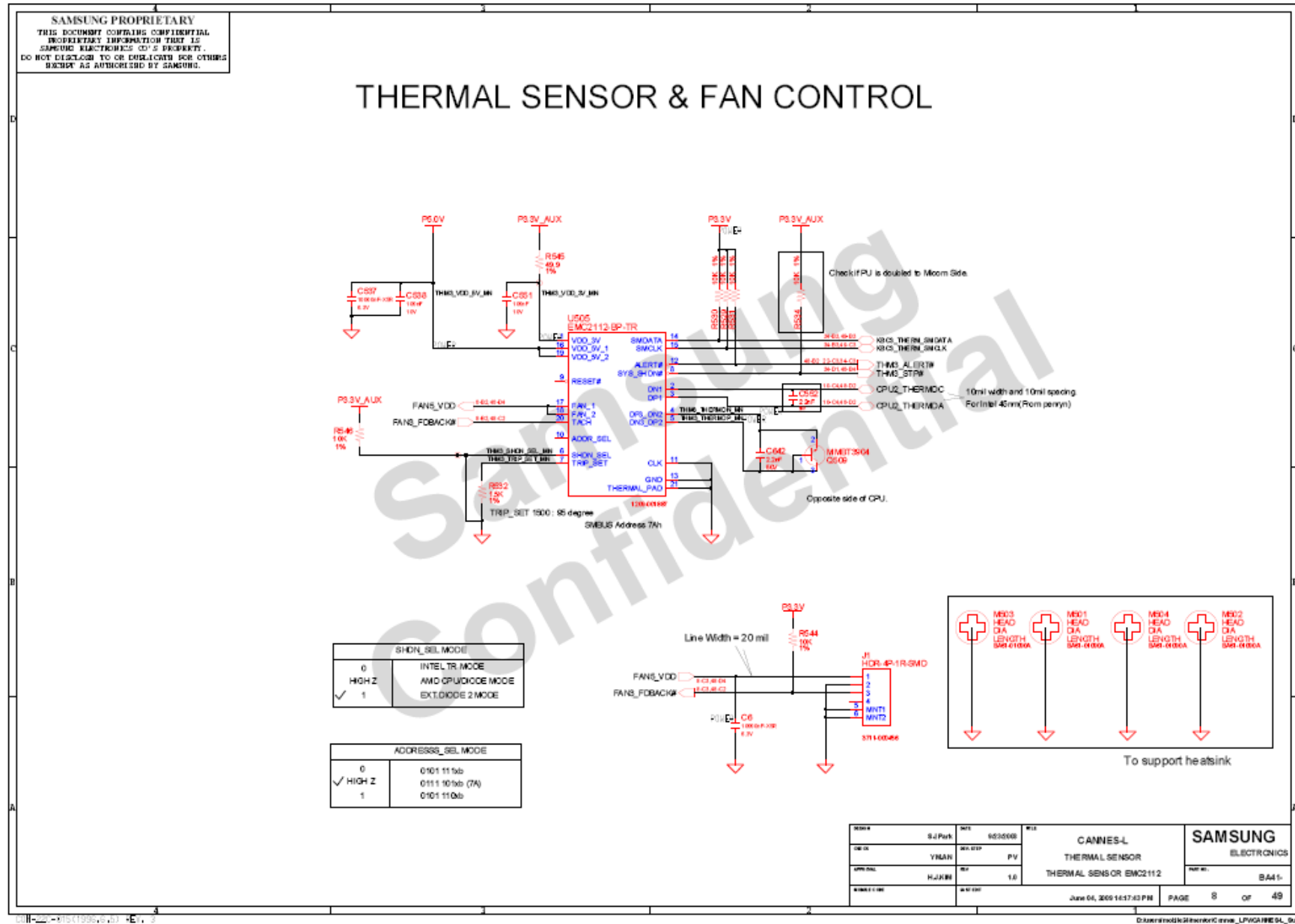
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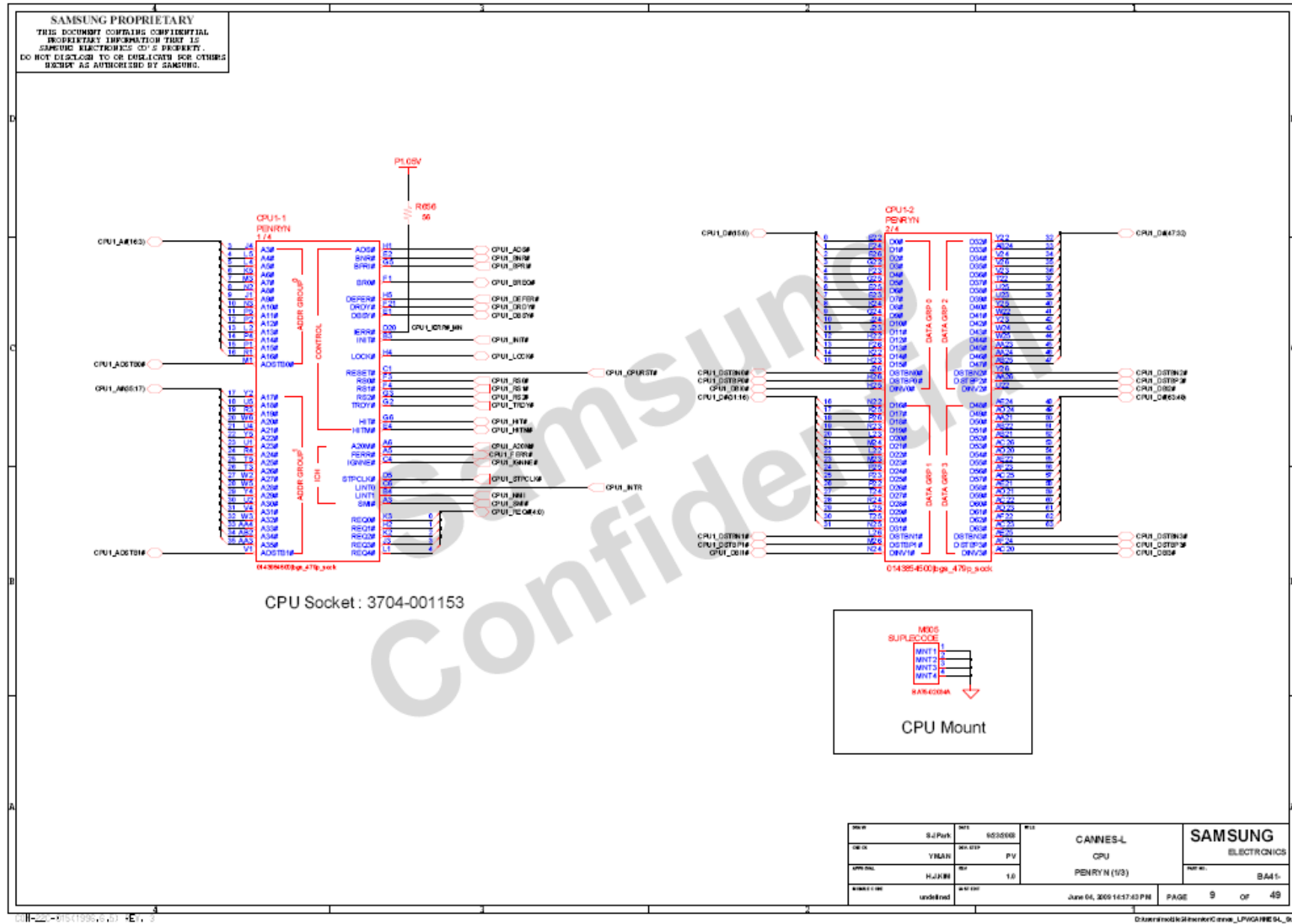
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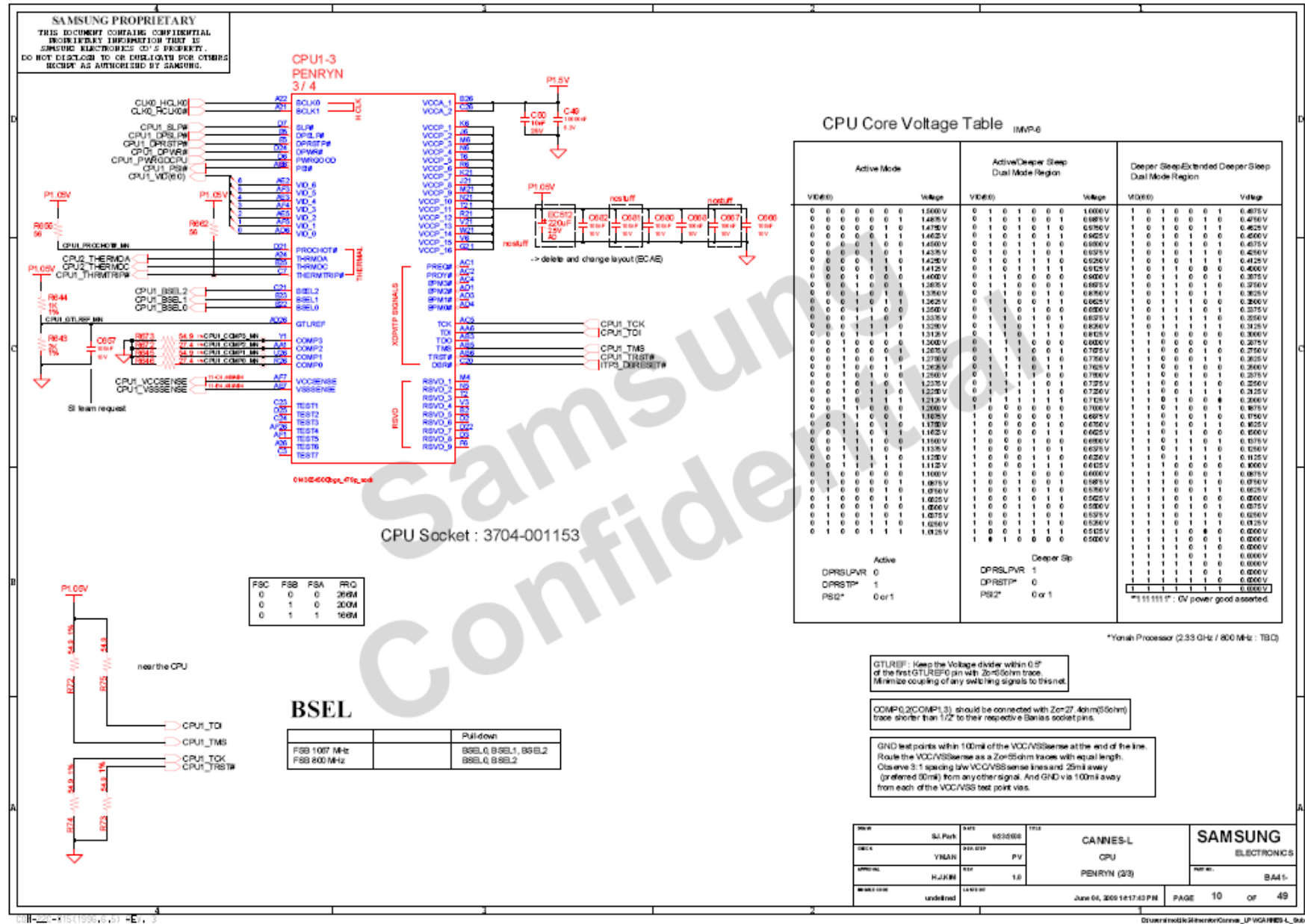
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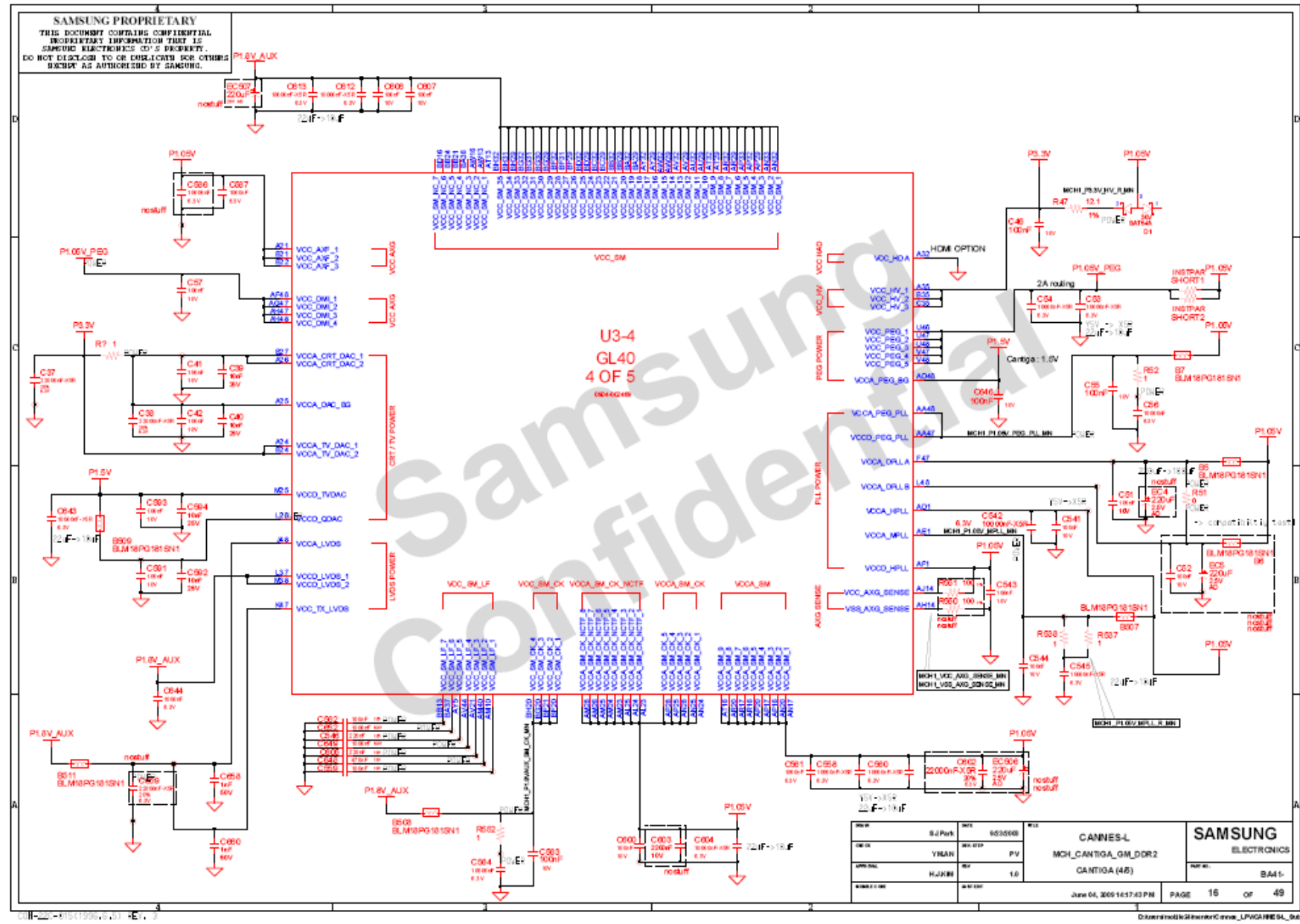
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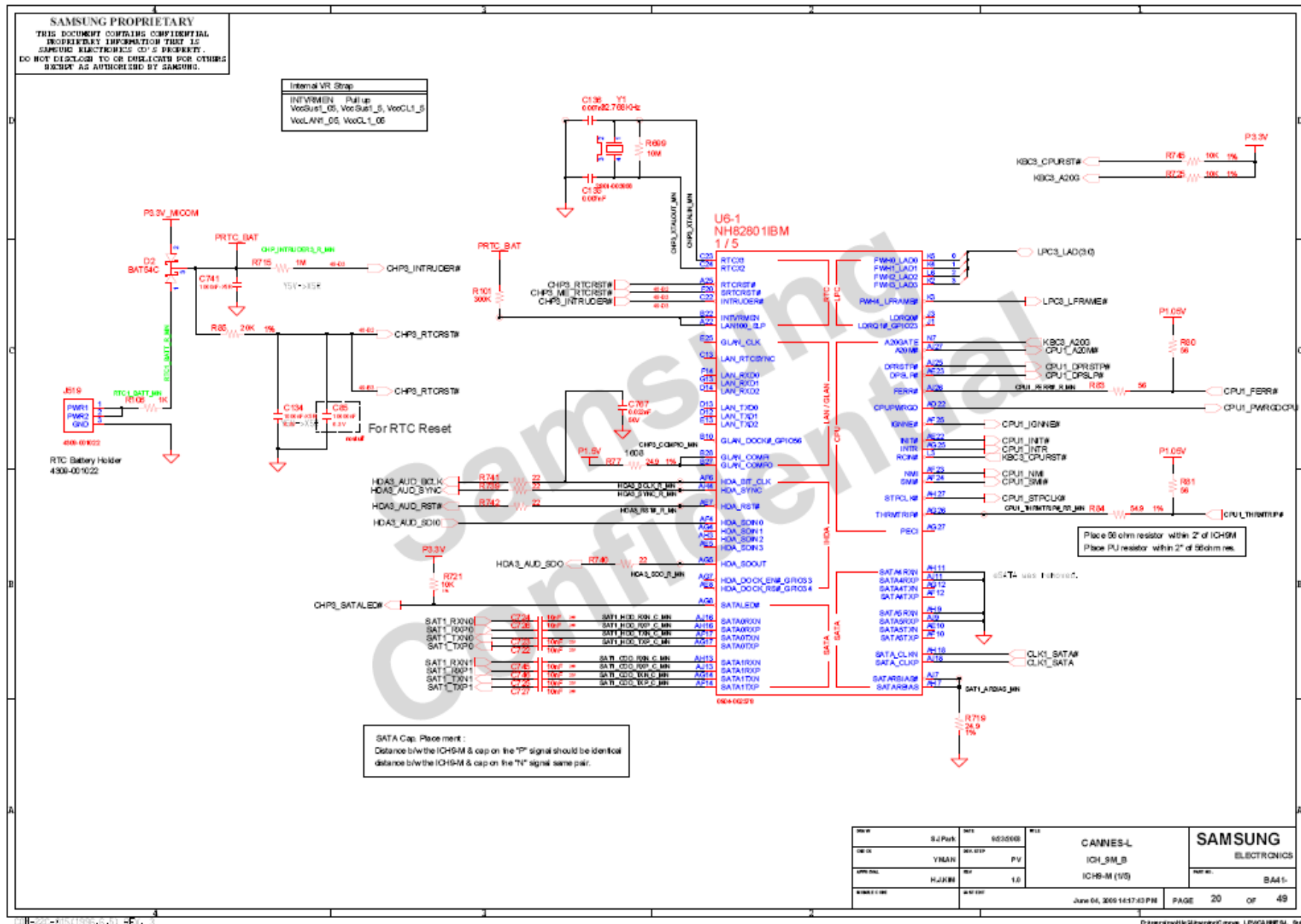
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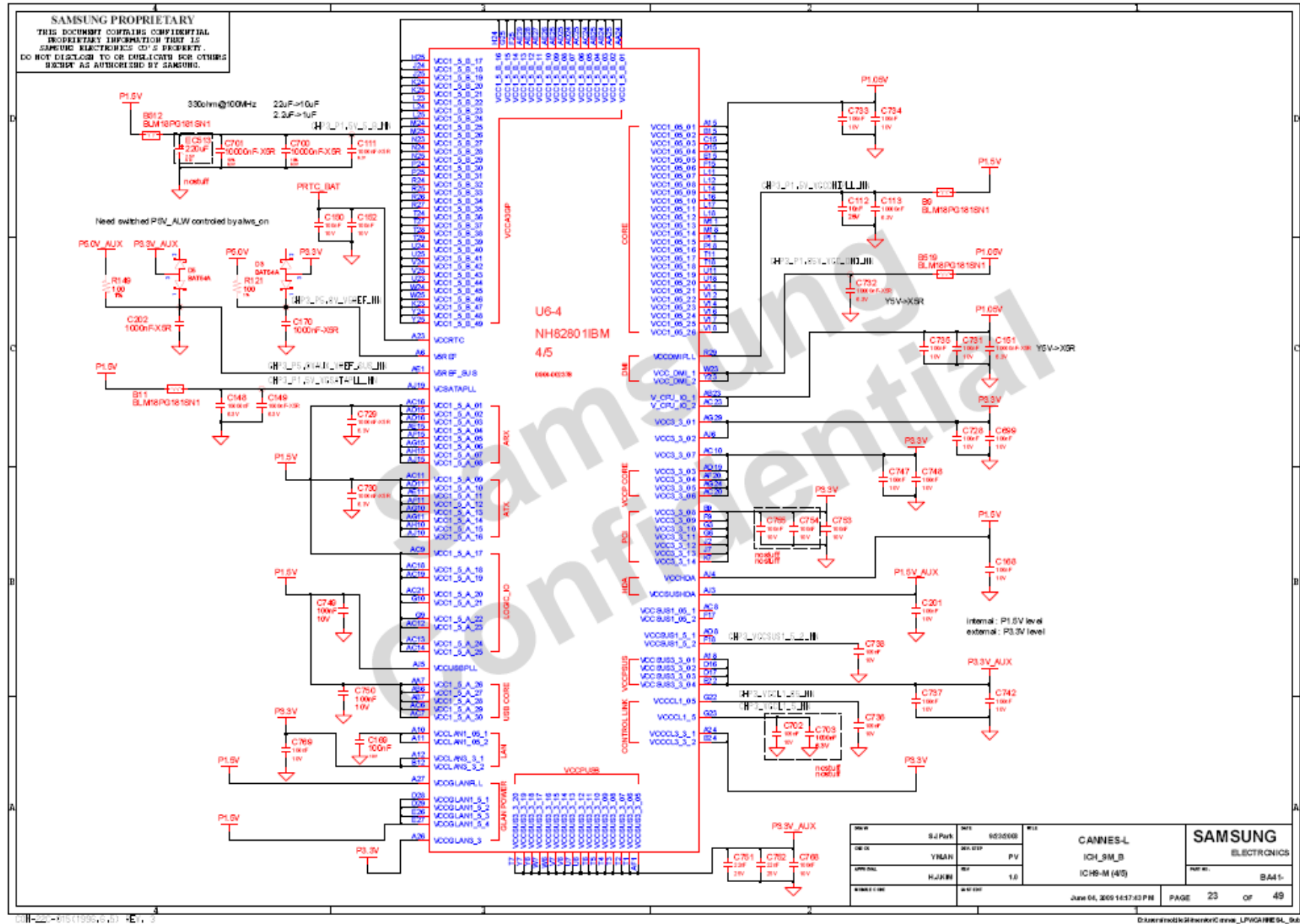
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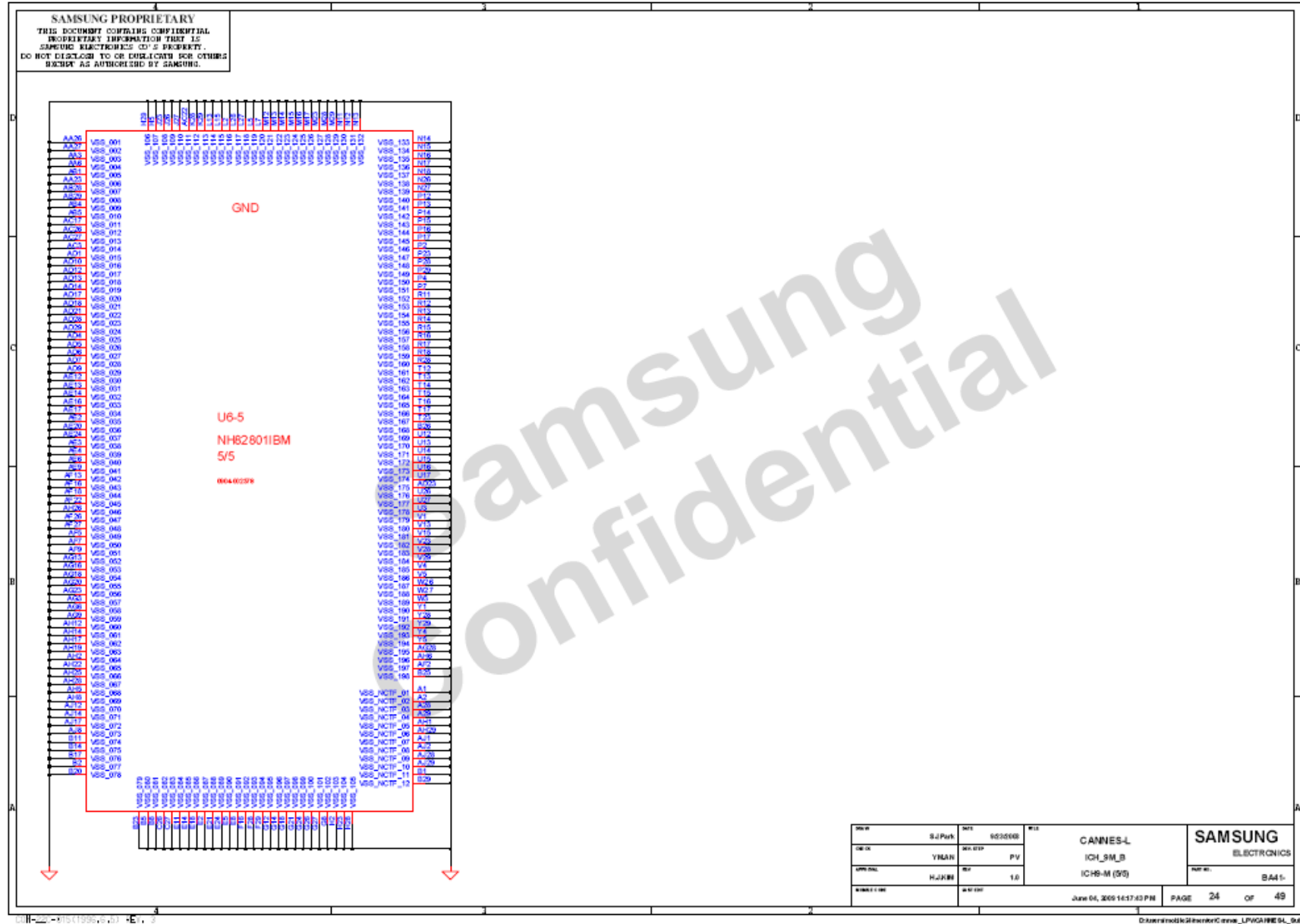
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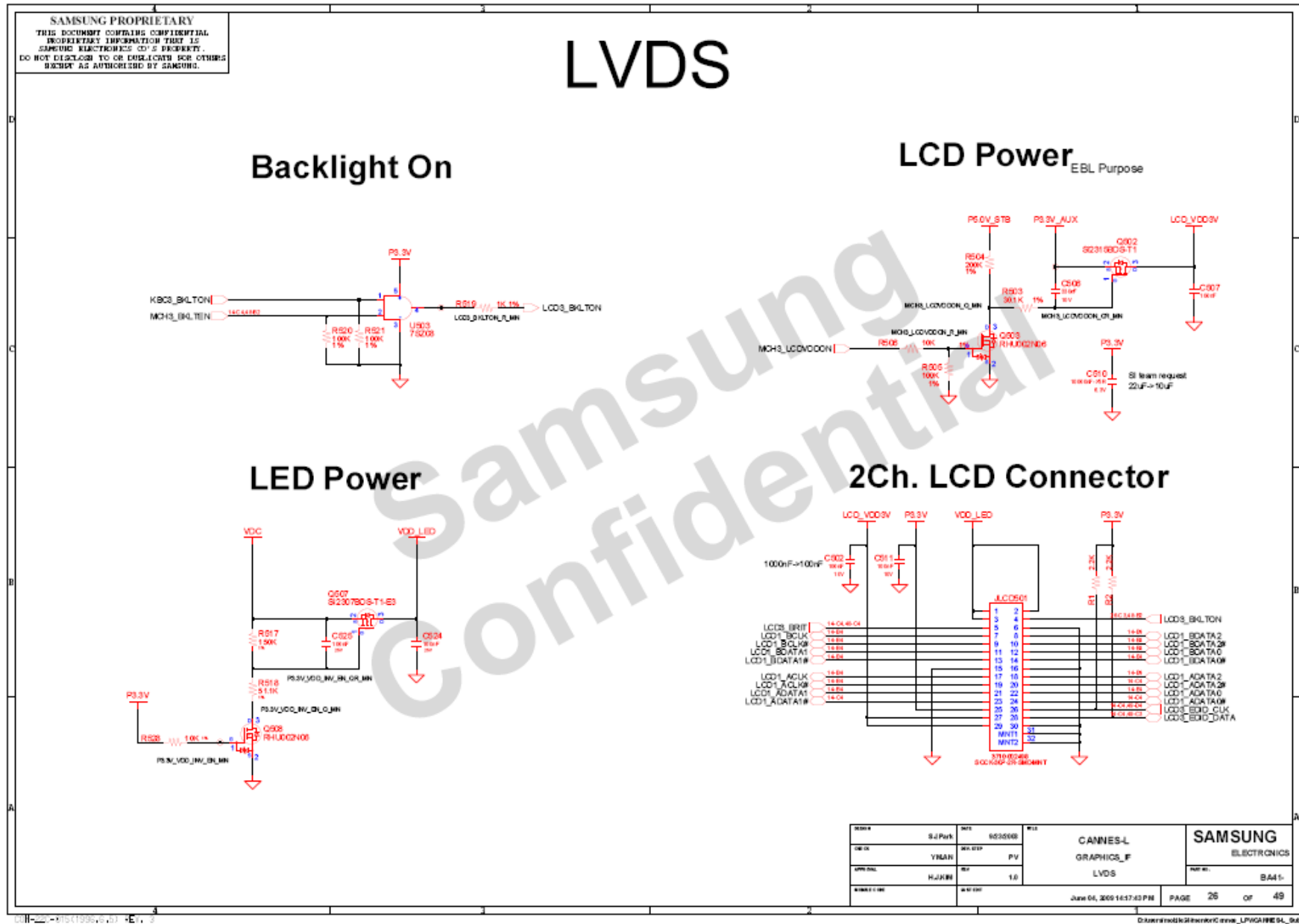
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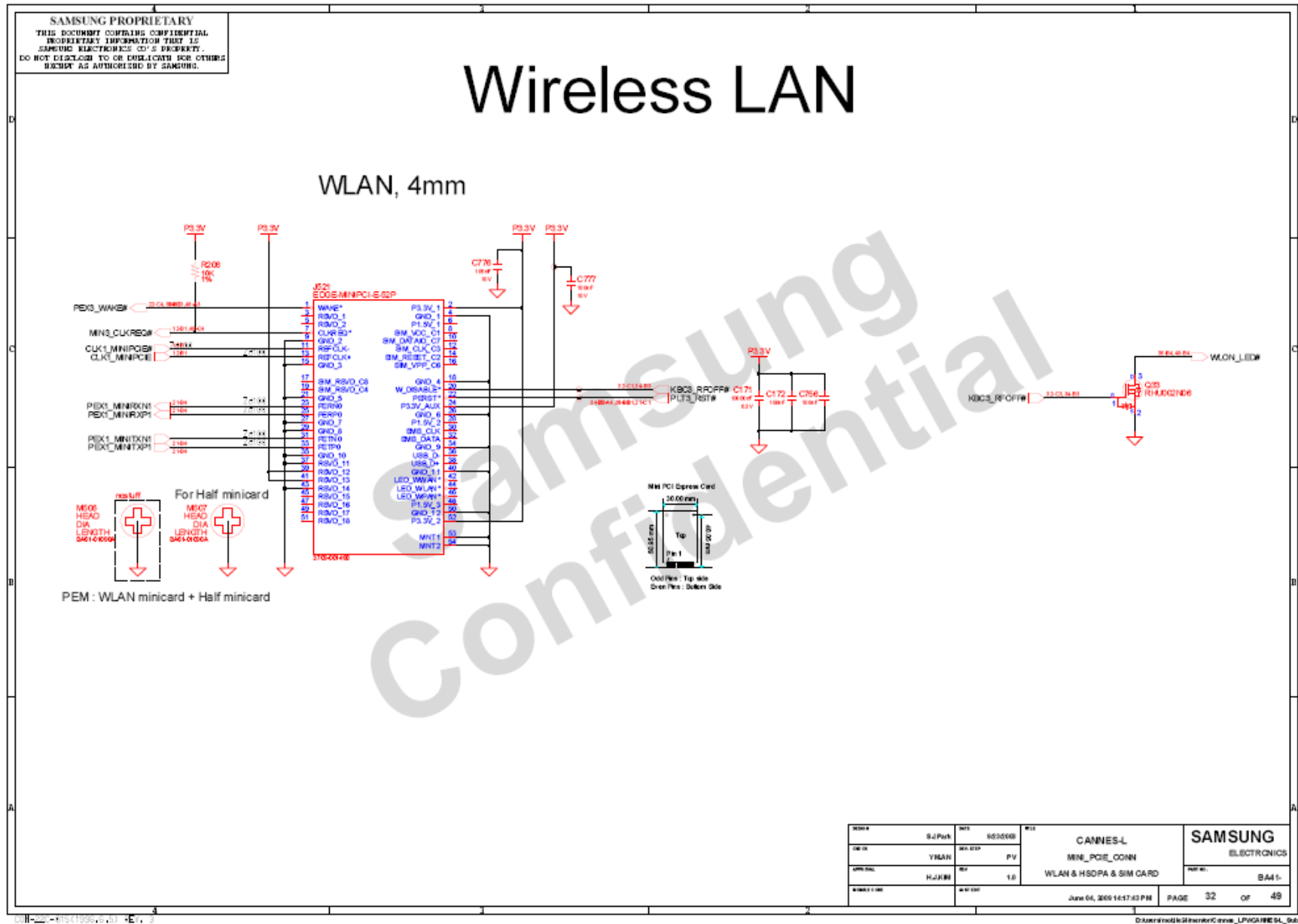
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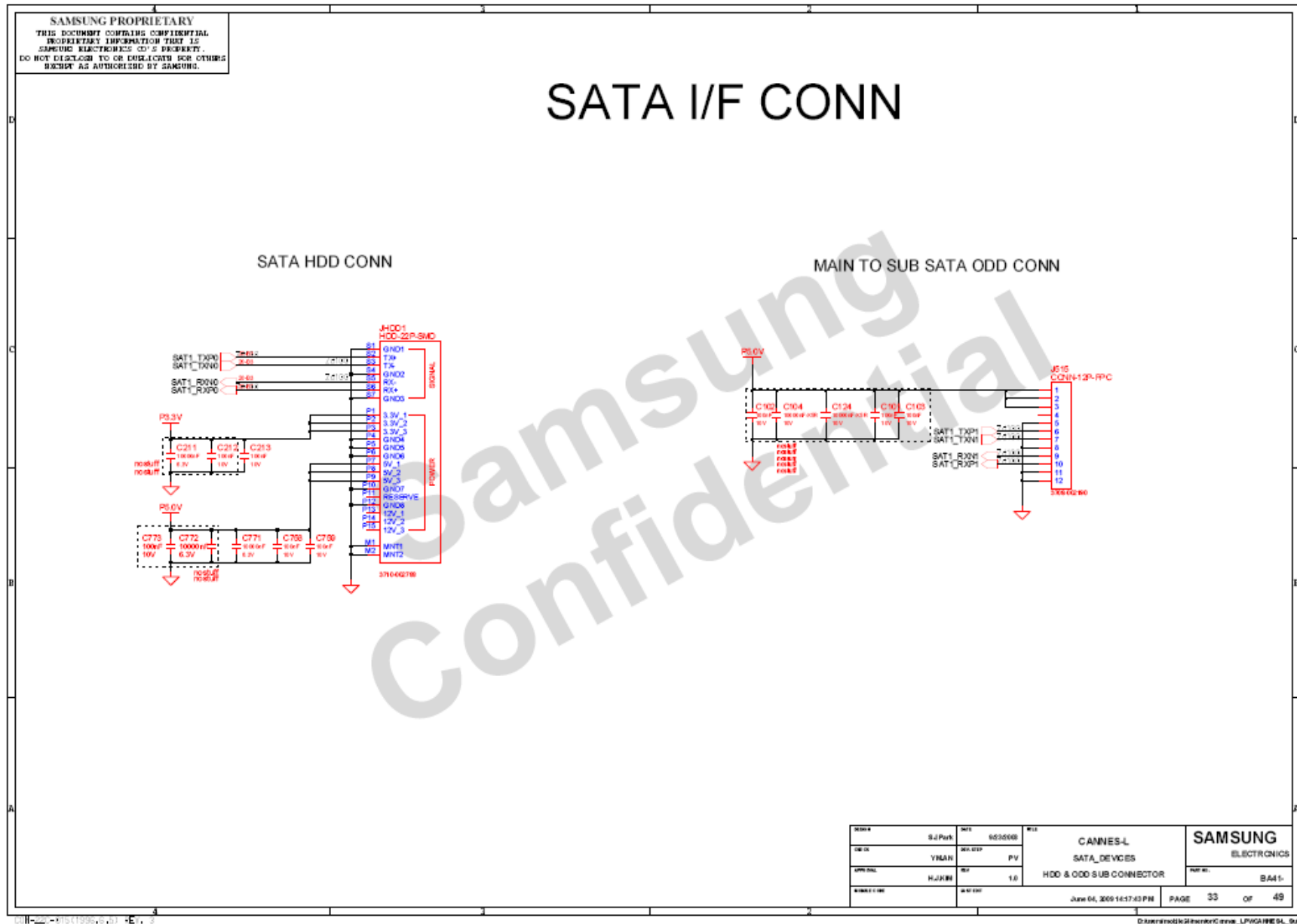
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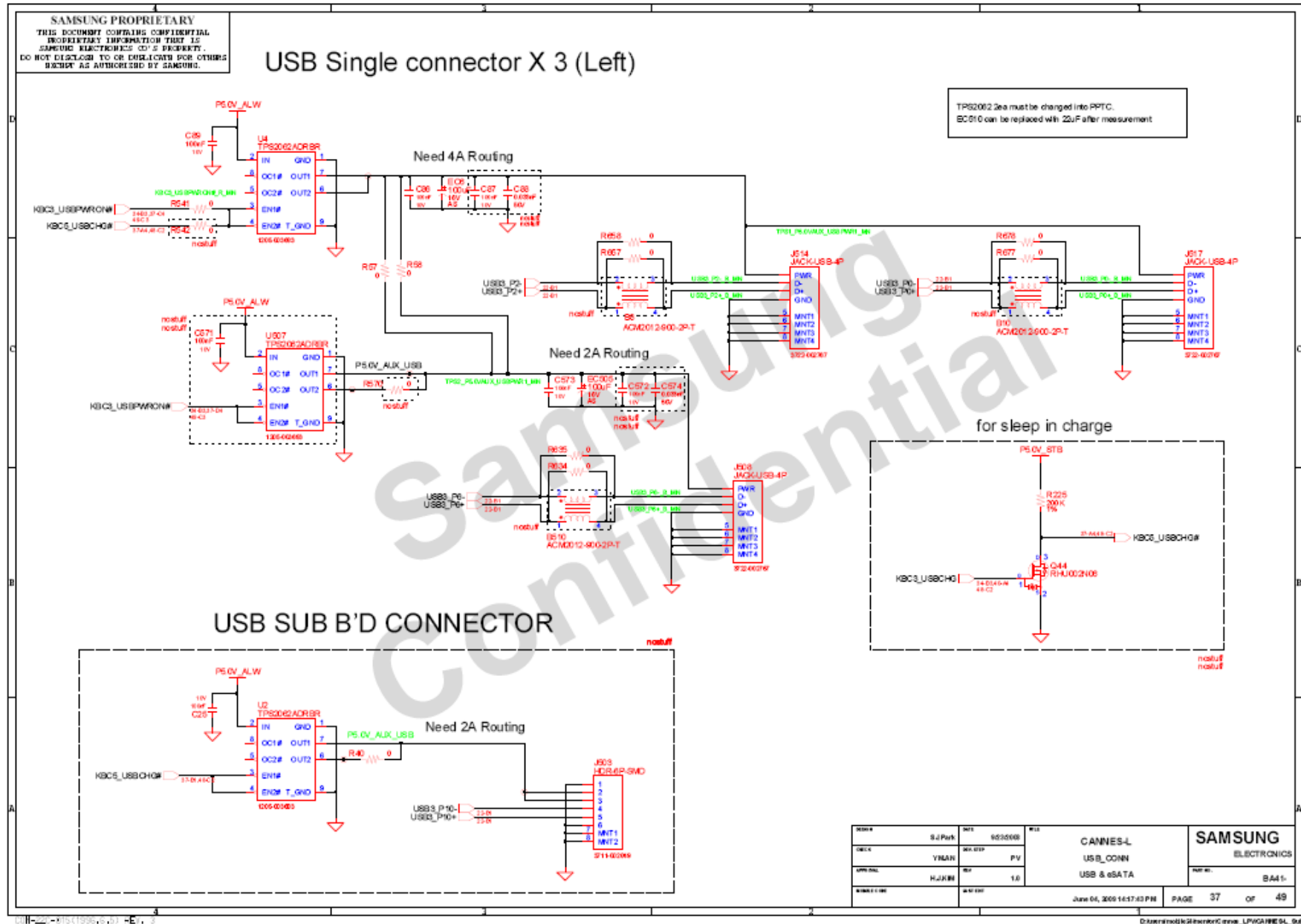
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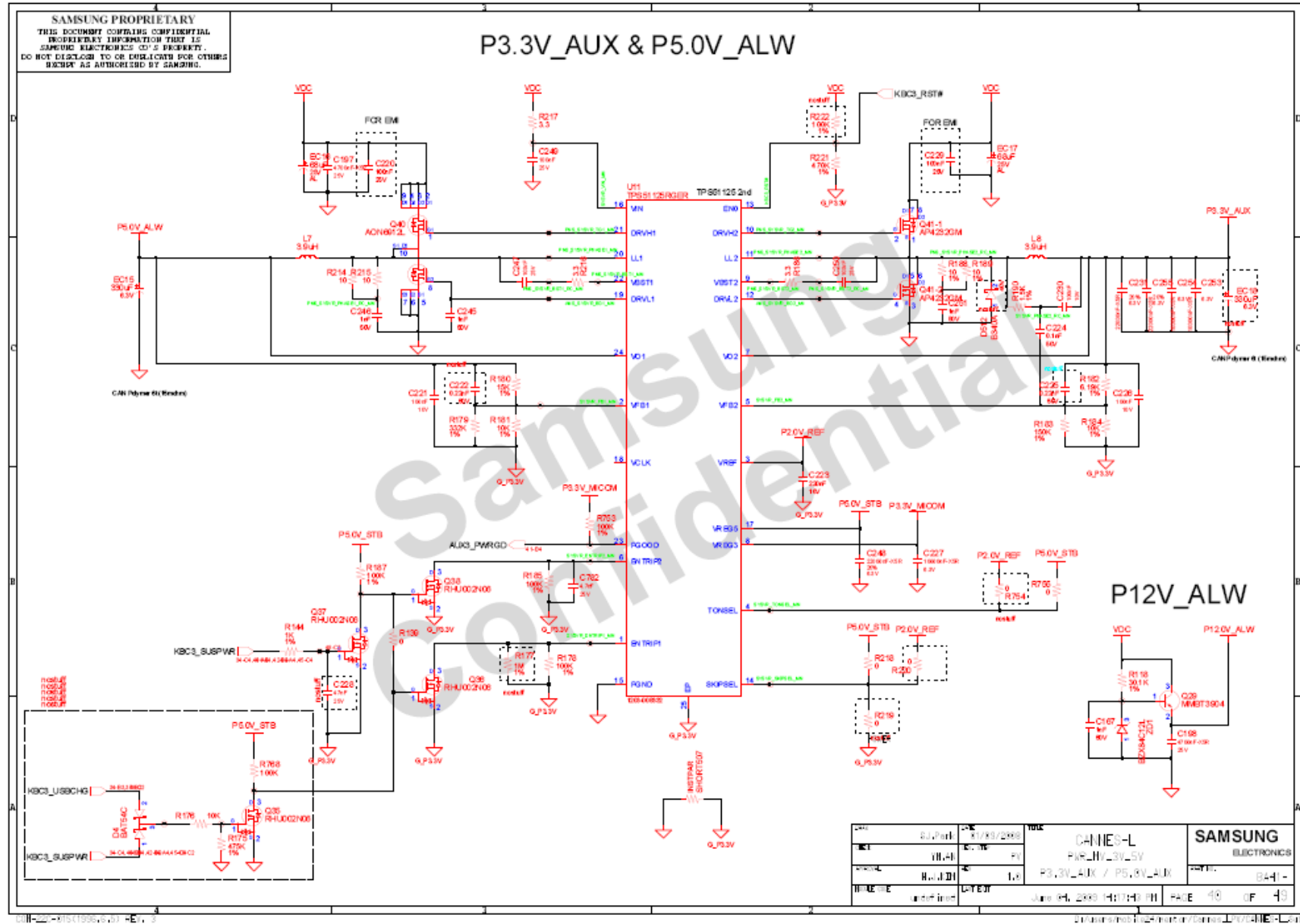
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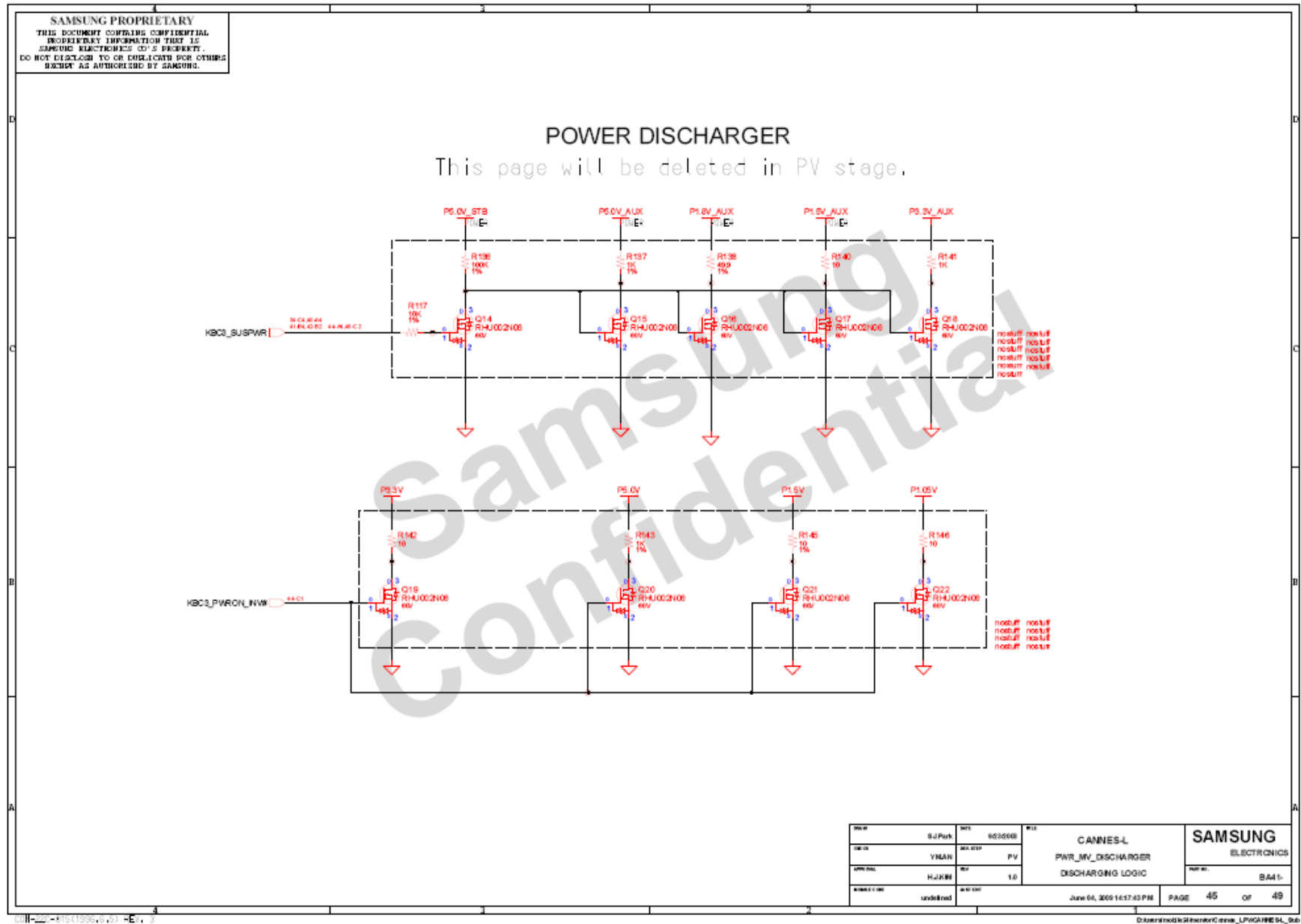
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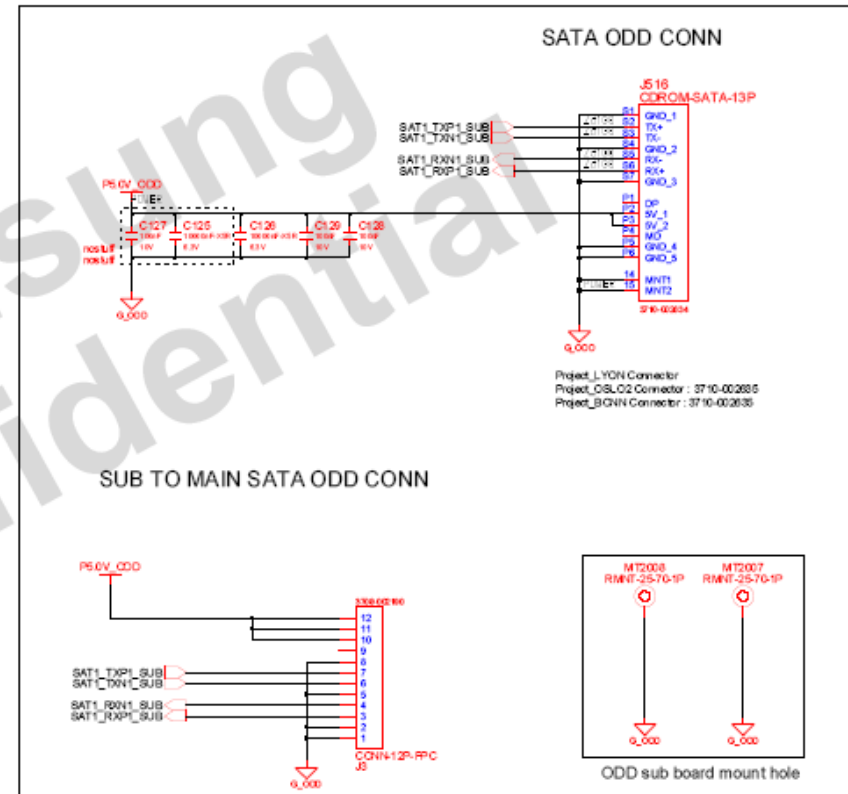
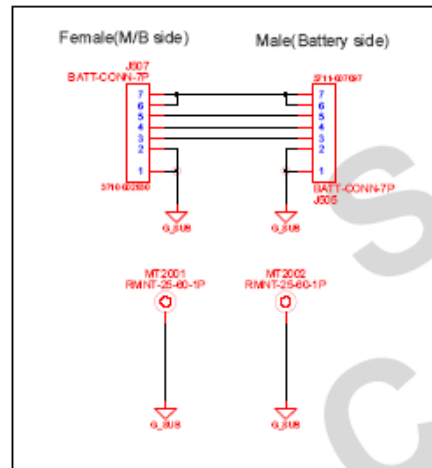


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Battery & SATA ODD SUBBOARD

SATA ODD SUB BOARD



Rev. 01	S.J. Park	DATE	05/05/08	W.D.		SAMSUNG
CHK. 01	Y.N.A.R.	REV. 01	P.V.			ELECTRONICS
APPR. 01	H.J.H.B.	REV.	1.0			
Rev. 01	underlined	Rev. 01	June 04, 2008 14:17:43 PM	PAGE	46	OF 49



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