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GENEVA 2 EXT

CPU : Penryn
Chip Set : Cantiga + ICH9M
Remarks : Mobility Platform

Model Name : GENEVA 2 EXT
PBA Name : MAIN
PCB Code : SGCE BA41-00930A
NAYA BA41-00936A
Dev. Step : PV1.0
Revision : 1.0
T.R. Date :

DRAW	CHECK	APPROVAL
SUN XIAO	WUSHIJIANG	BC.LEE

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CHECK: WU SHIJIANG,	DEV. STEP: PV	COVER	PART NO.: BA41-####A
APPROVAL: BYEONGCHANG LEE,	REV: 1.0		
Dimensions: undefined	Unit: TEXT	May 08, 2008 19:01:59 PM	PAGE 1 OF 23

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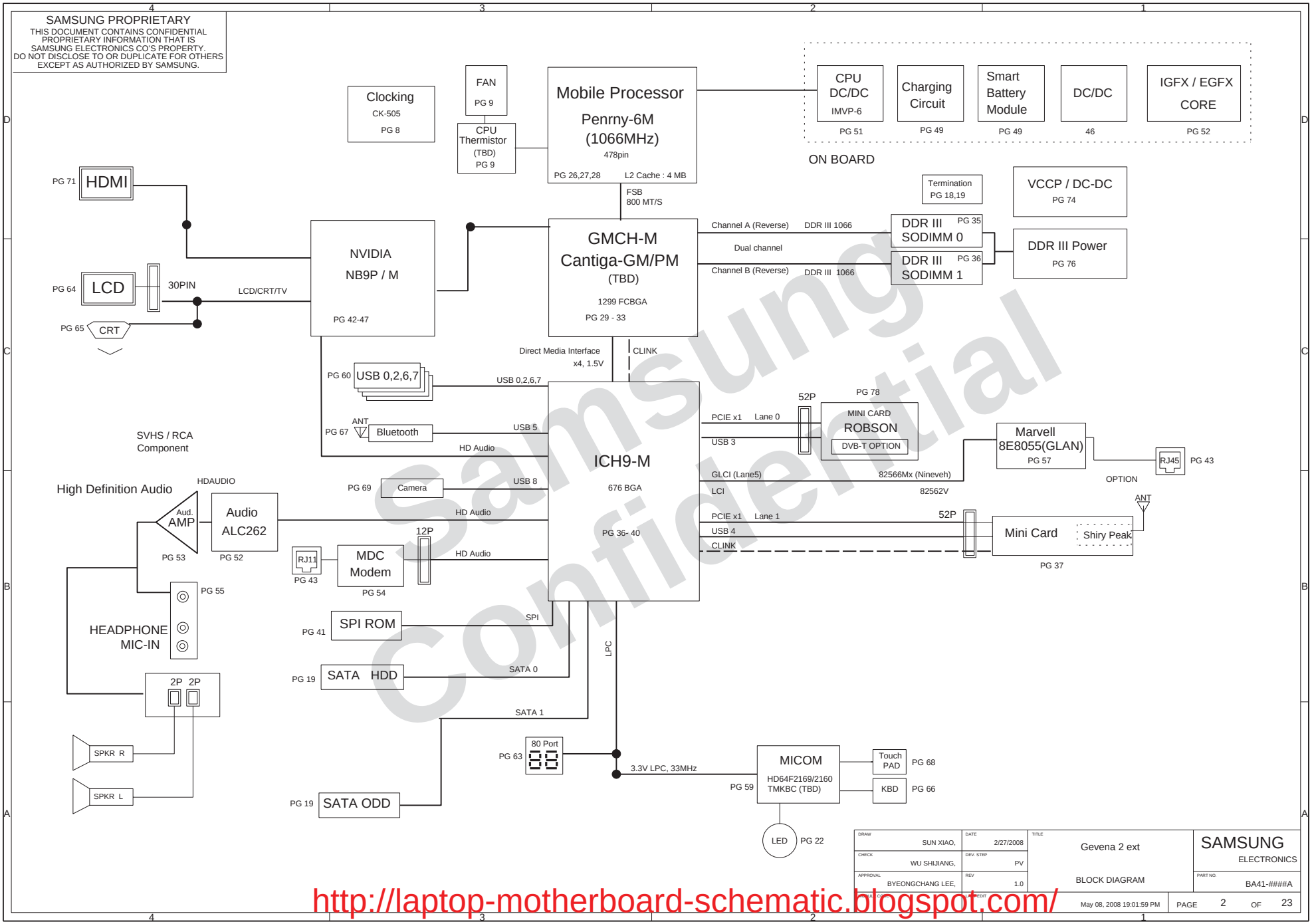

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CHECK: WU SHIJIANG,	DEV. STEP: PV	BLOCK DIAGRAM	
APPROVAL: BYEONGCHANG LEE,	REV: 1.0		PART NO.: BA41-####A
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BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	3	B,C,D
DT PCI SLOT	AD22	1	B,C,D,C
MiniPCI SLOT	AD23	2	A,B
USB	AD29(internal)	-	USB2.0 #0 (USB0) : A USB2.0 #1 (USB1) : D USB2.0 #2 (USB4) : C USB2.0 #3 (USB5) : E USB2.0 #4 (EHCI) : H
Hub to PCI	AD30(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	B
Internal MAC	AD24(internal)	-	E
AC Link	-	-	B
GLAN	-	-	F

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH8-M	Real Time Clock
Crystal	10MHz	MICOM	HD64F2169/2160
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	24.576MHz	Cardbus Controller	1394
Crystal	25MHz	LAN	Intel LAN
Crystal	27MHz (TBD)	VIDEO	PEG
Crystal	24.576MHz (TBD)	HD Audio	Audio

LCD Pannel Detect (TBD)

Devices	Resolution	PANNEL_DETECT_0

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core Voltage for CPU
MCH_CORE	Core Voltage for CPU
ICH_CORE	Core Voltage for CPU
P1.05V (VCCP)	VTT for CPU, Crestline & ICH8-M
P1.05V_M	1.05V switched power rail for ME (on in M0/M1)
P1.25V_M	1.25V switched power rail for ME (on in M0/M1)
P3.3V_M	3.3V switched power rail for ME (on in M0/M1)
P3.3V_A	3.3V always power rail (by KBC3_ALWS_ON)
MICOM_P3V	3.3V always power rail (for Micom)
LAN_3.3V	3.3V always power rail (for LAN)
P1.5V	1.5V switched off power rail (off in S3-S5)
P1.5V_AUX	1.5V switched on power rail
P2.5V	2.5V switched off power rail (off in S3-S5)
P1.8V	1.8V switched off power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail for DDR
P0.9V	0.9V power rail for DDR
P3.3V	3.3V switched off power rail (off in S3-S5)
P3.3V_AUX	3.3V switched on power rail
P5V	5.0V switched off power rail (off in S3-S5)
P5V_AUX	5.0V switched on power rail

I^2C / SMB Address

Devices	Address	Hex	Bus
ICH8-m	Master	-	SMBUS Master
CPU Thermal Sensor	1001 110x	9Ch	Thermal Sensor
SODIMM0	1010 000x	A0h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable
DB400 (PCI Express Clocks)	1101 110x	DCh	Clock Buffer for PCI Express
TBD	0100 1100	4Ch	Thermal Sensor
TBD : (LVDS BackLight Inverter)	0101 1000	58h	-
TBD : (ALS)	0111 0010	72h	Ambient Light Sensor
TBD : (AUX DISPLAY)	0011 110x	3Ch	EMA
LAN	1100 1000	C8h	82566
PCI Express Docking	TBD	TBD	TBD
TPM	TBD	TBD	TBD

USB PORT Assign

PORT #	ASSIGNED TO
0	SYSTEM PORT 0
1	SYSTEM PORT 1
2	DMB
3	Expresas Card
4	DOCKING PORT 0
5	Bluetooth
6	Mini PCI Express
7	Aux Display
8	Test Port (RSVD)
9	WWAN/WIBRO (TBD)

PCI Express Assign

PORT #	ASSIGNED TO
0	PCIE x1 Slot
1	Mini Card (Golan)
2	Mini Card (WIBRO : RSVD)
3	Expresas Card
4	DOCKING PORT 0
5	GLAN

REVISION HISTORY

See rev notes for more information.

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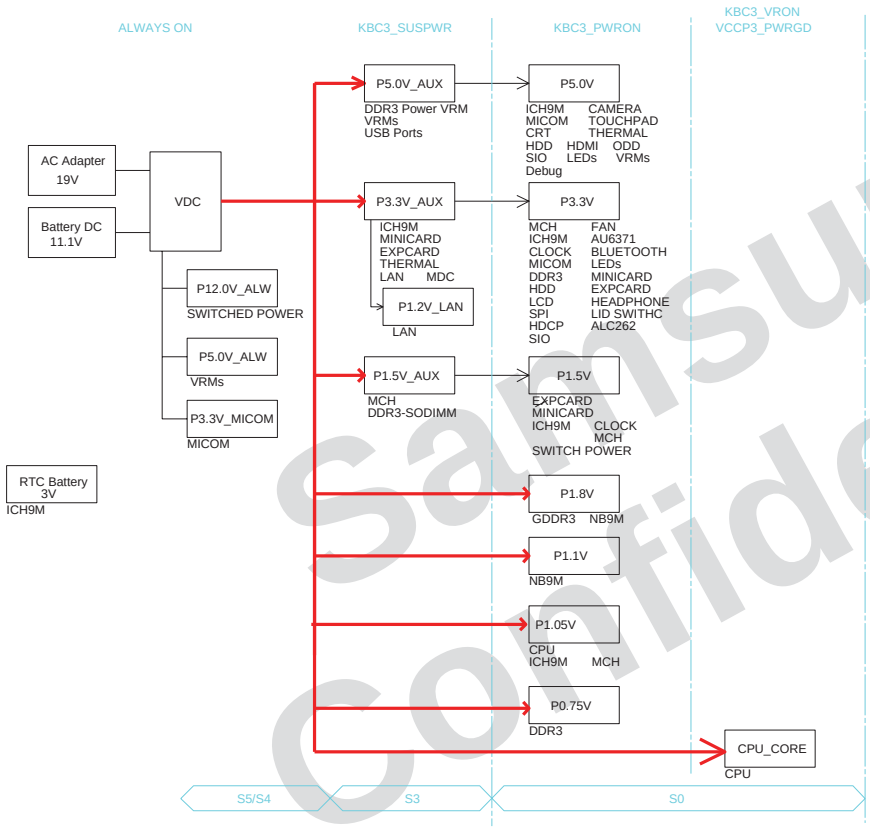
POWER DIAGRAM



State \ Rail	+V*Always	+V*AUX	+V	SUSPWR	PWRON	VRON
Full On	ON	ON	ON	H	H	H
S3	ON	ON	OFF	H	L	L
S4	ON	OFF	OFF	H	L	L
S5	ON	OFF	OFF	L	L	L

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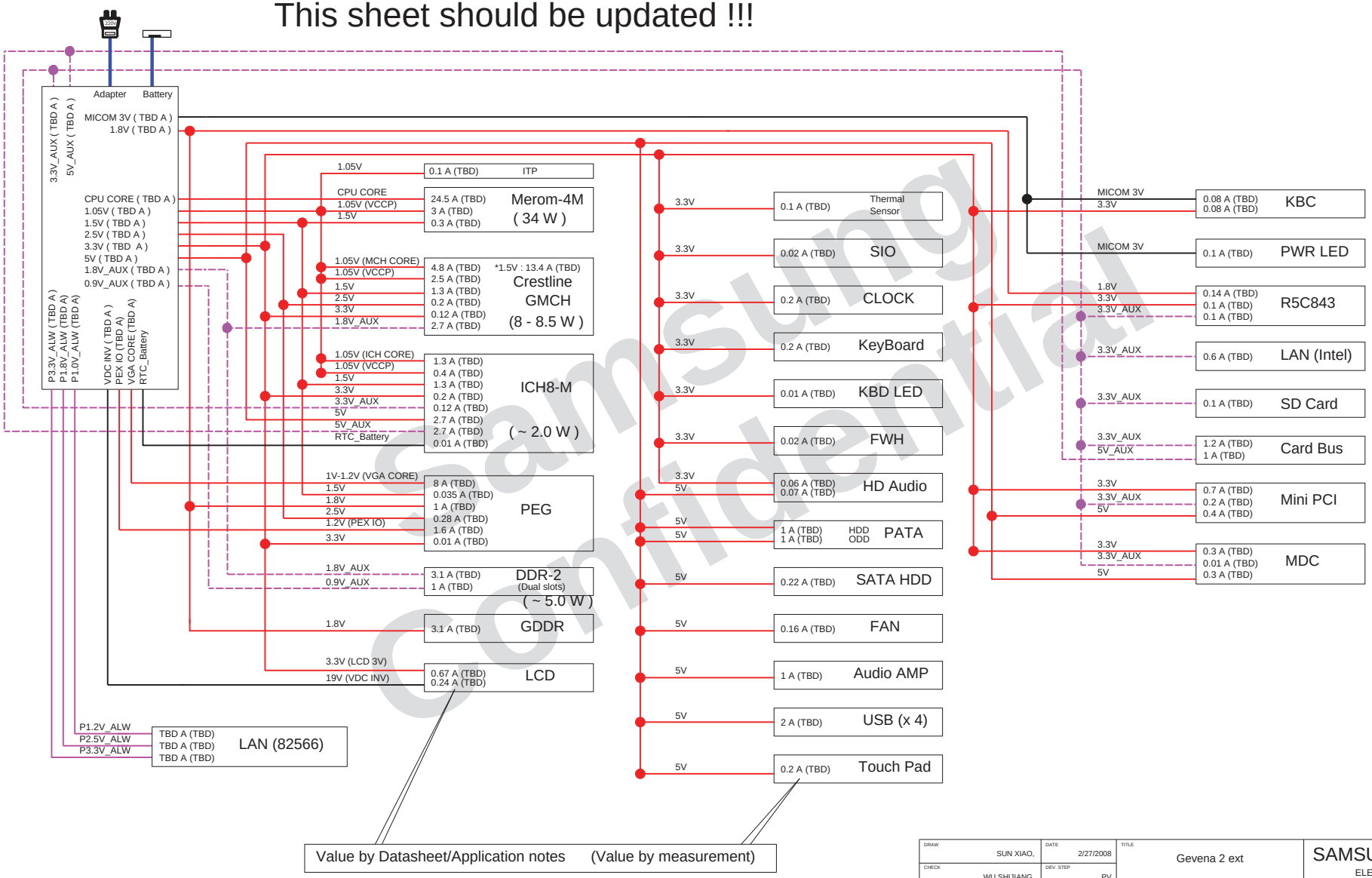
POWER RAILS ANALYSIS

Rev. 0.5

This sheet should be updated !!!



Value by Datasheet/Application notes (Value by measurement)

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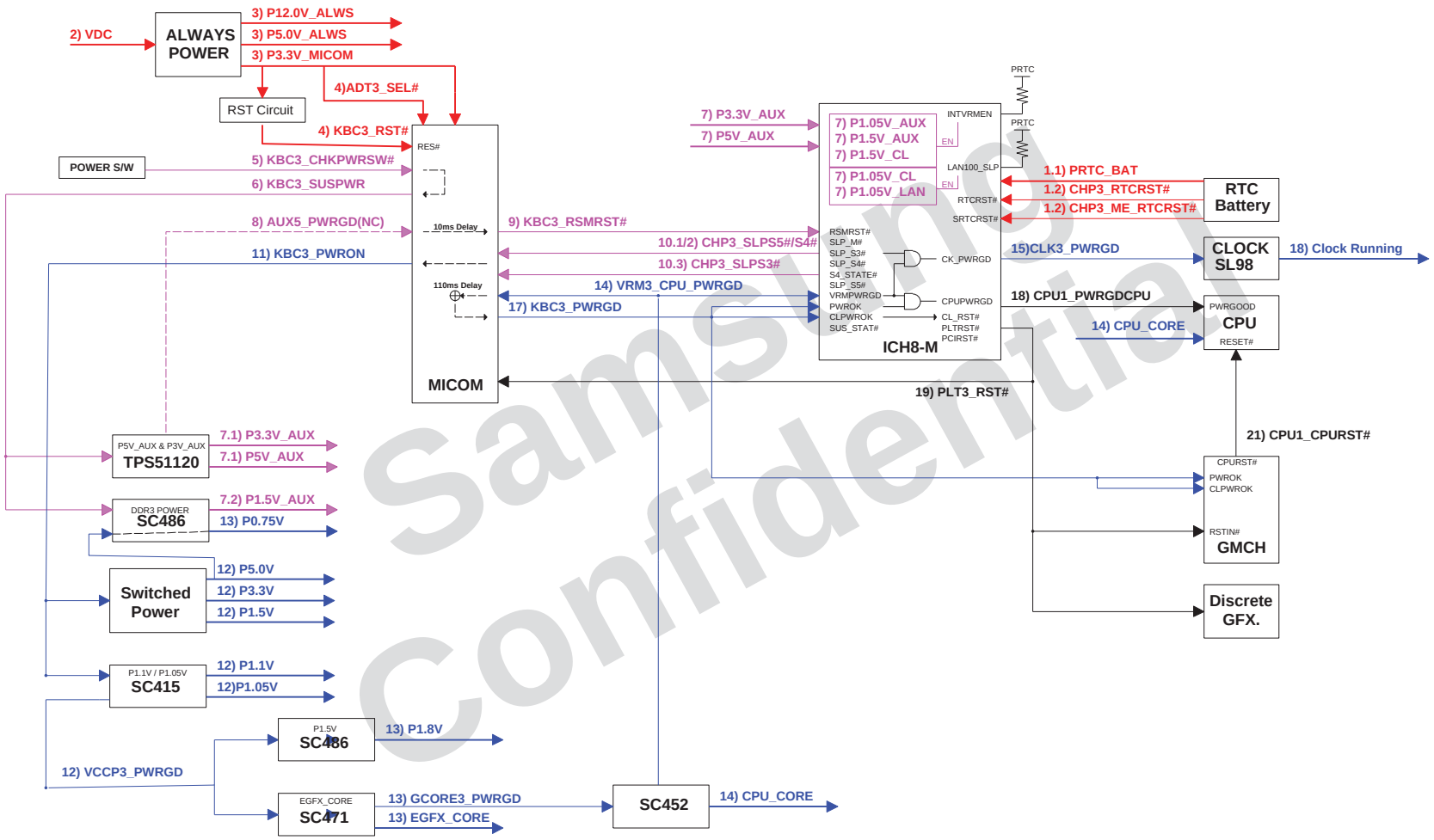
POWER SEQUENCE



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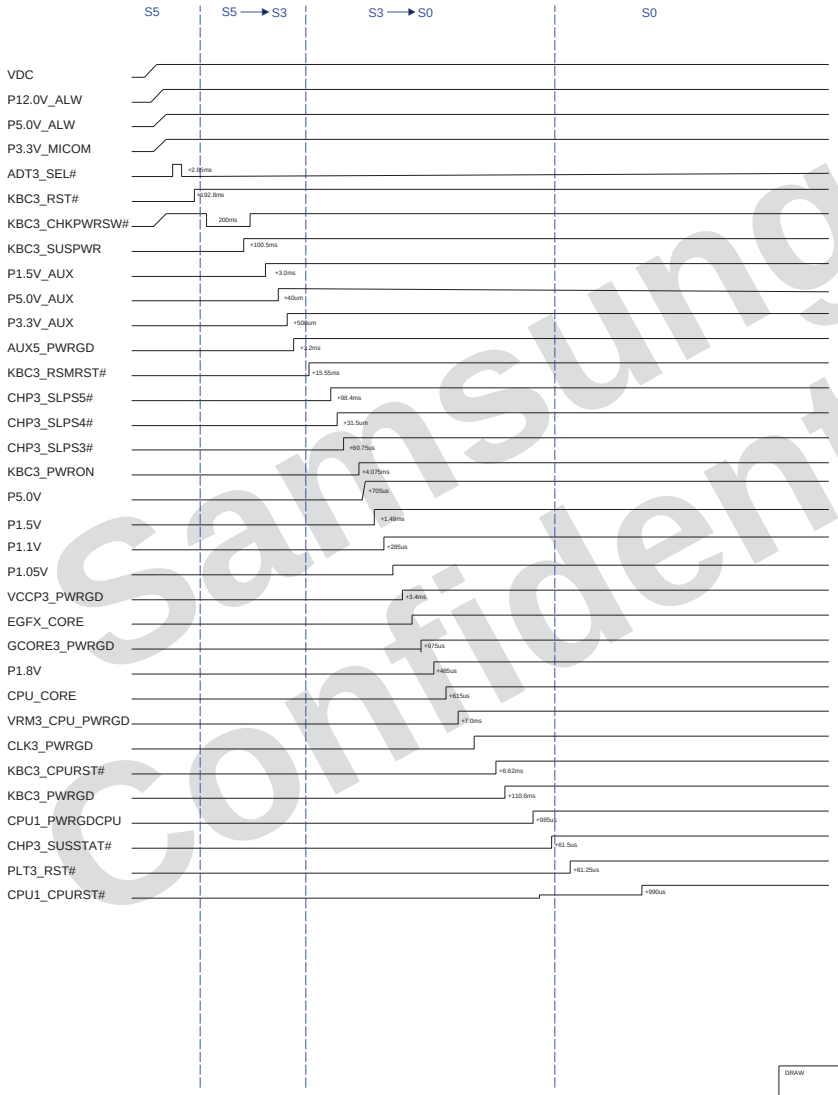
Timing Diagram, Power ON

Rev. 1.0 2008-05--5



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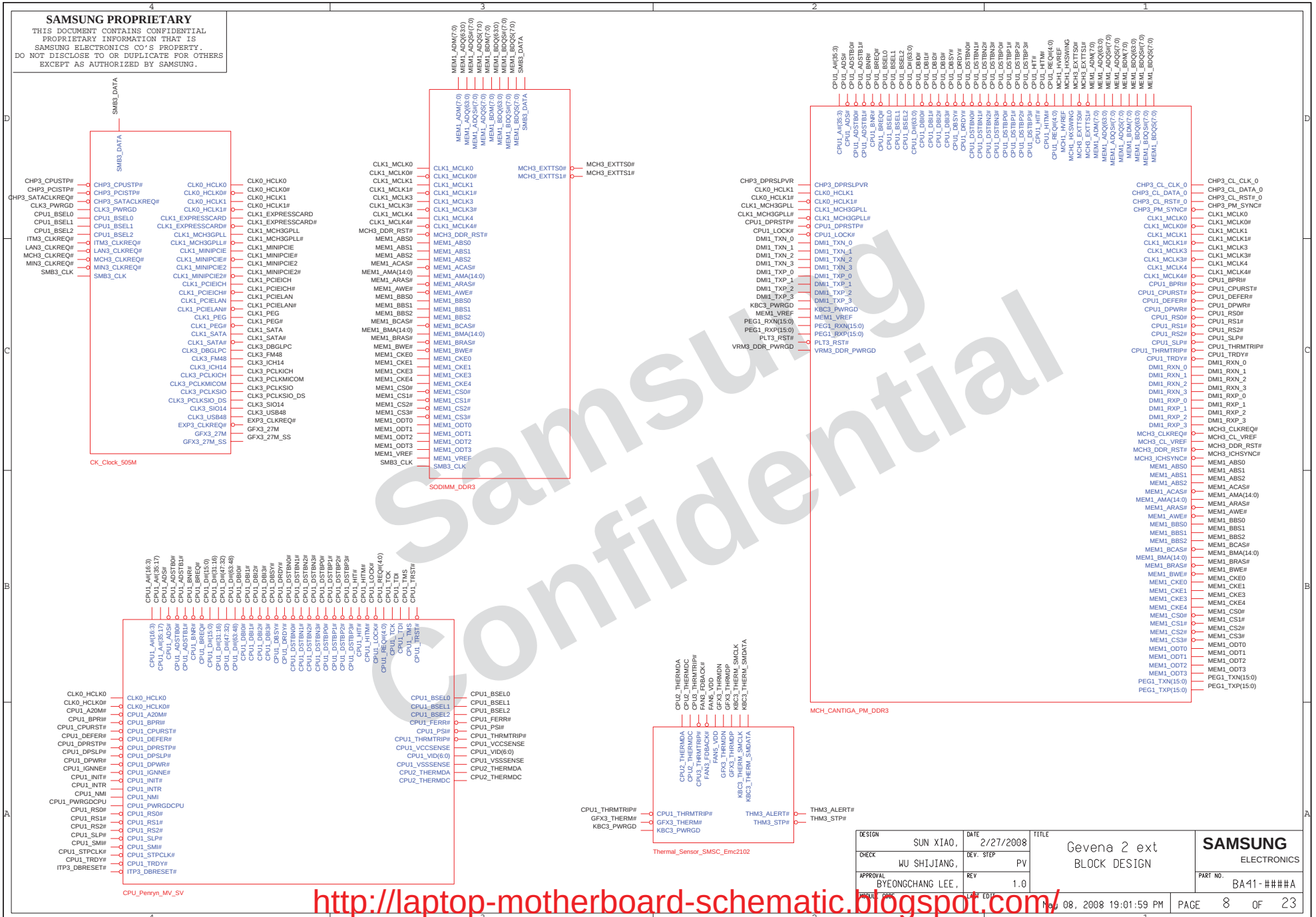

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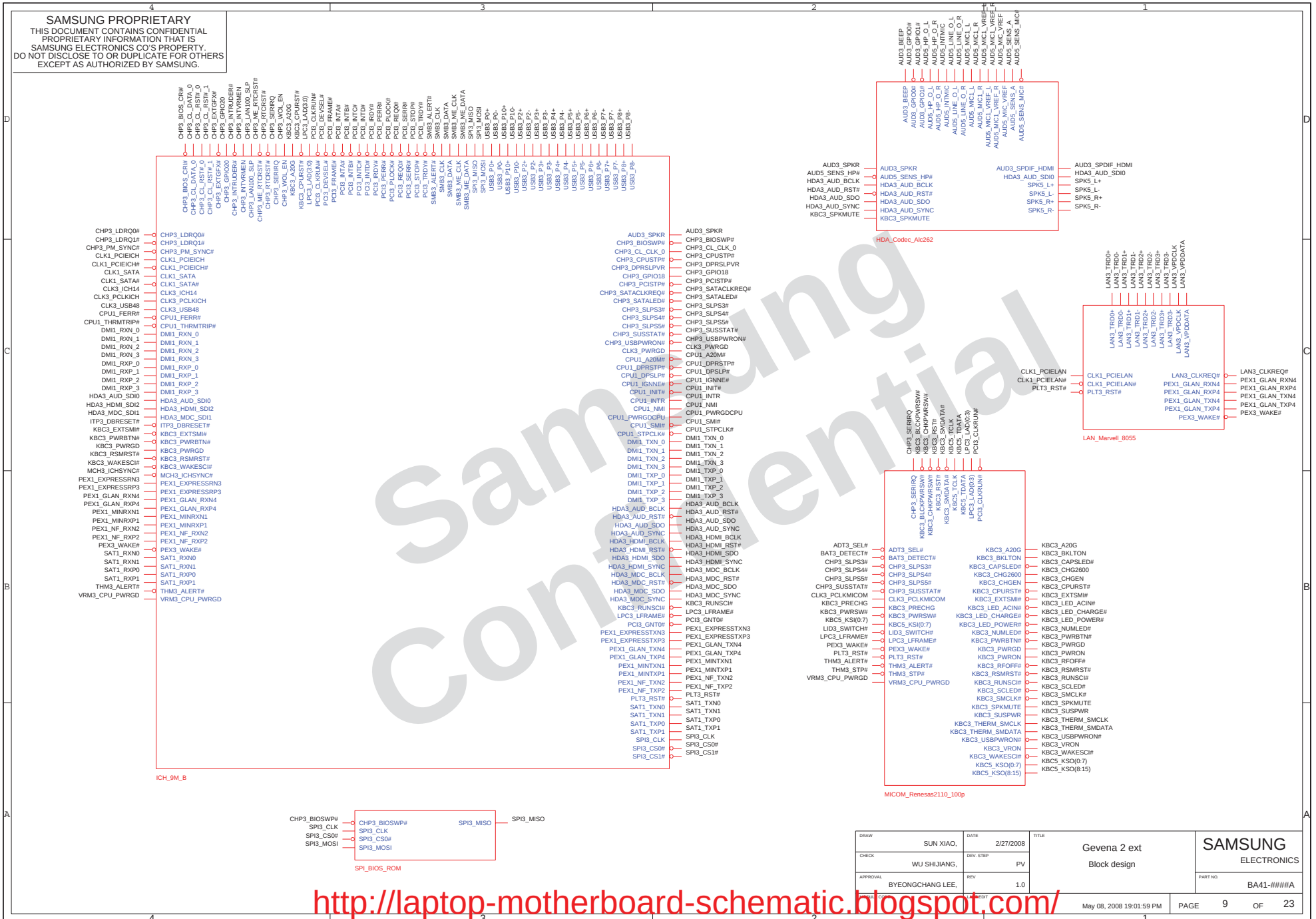

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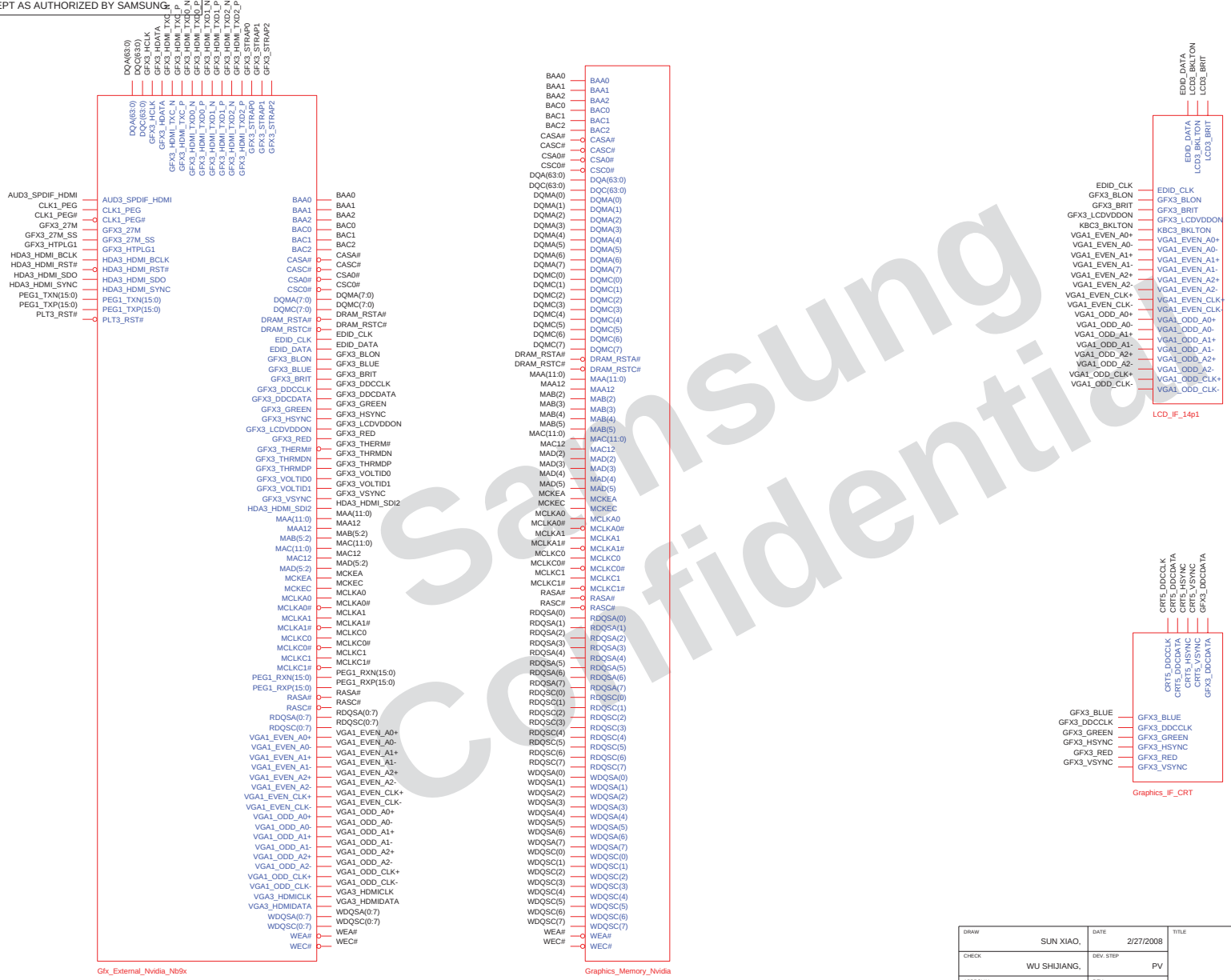

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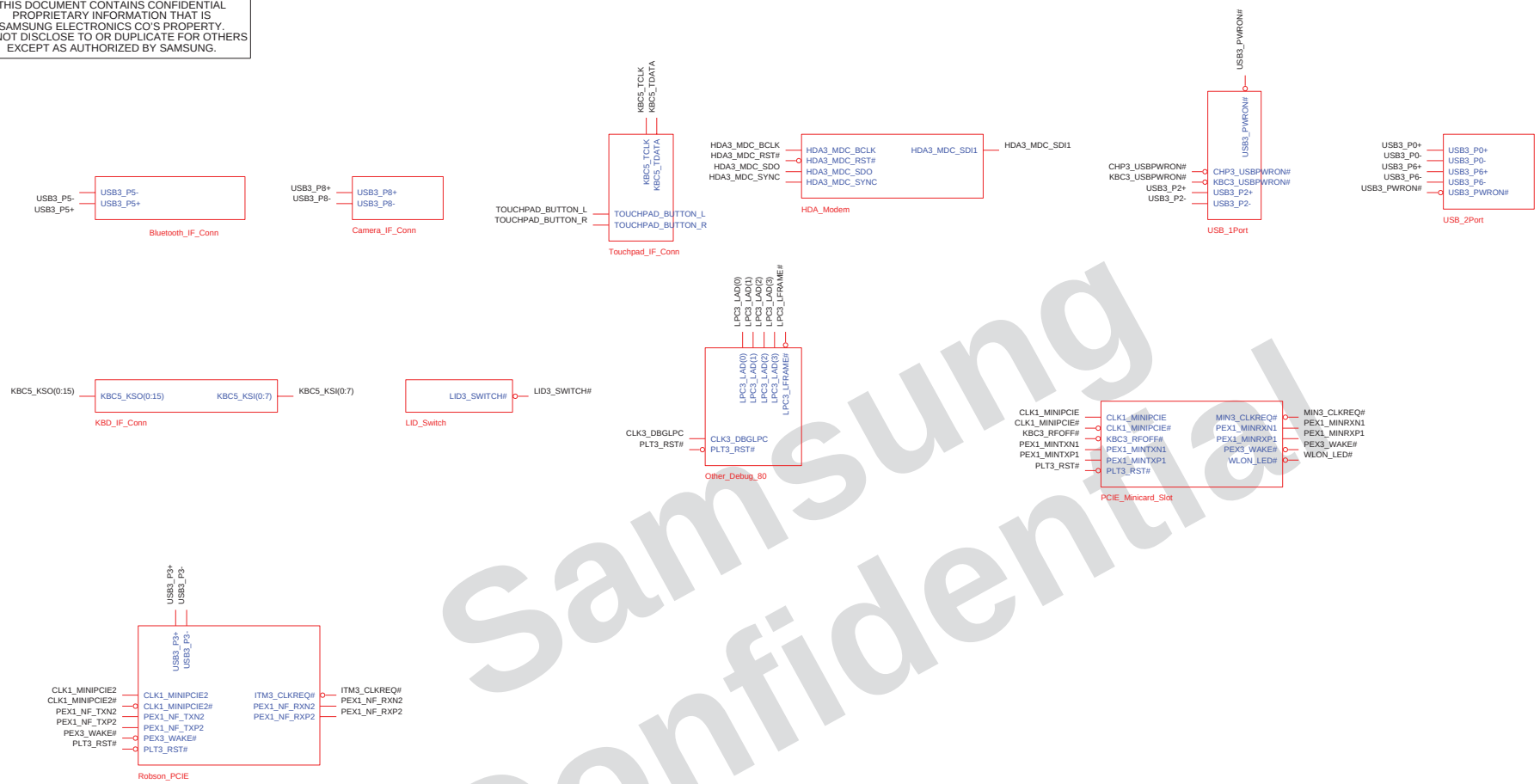

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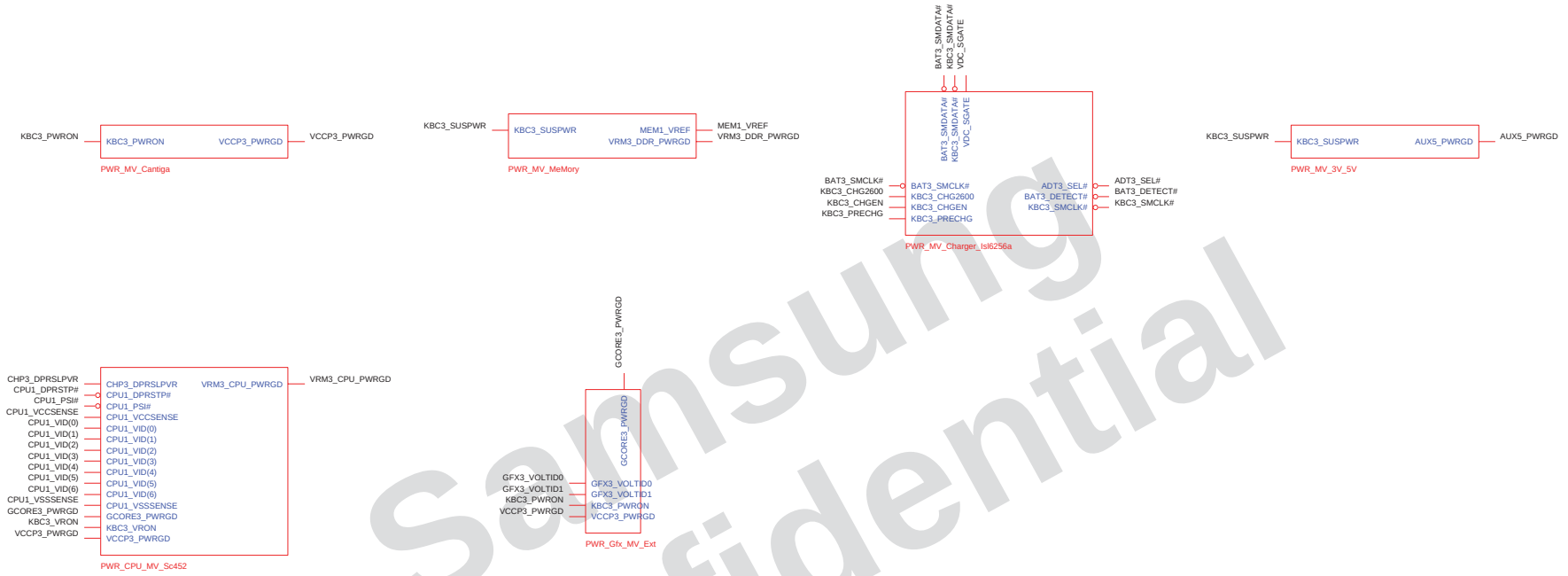

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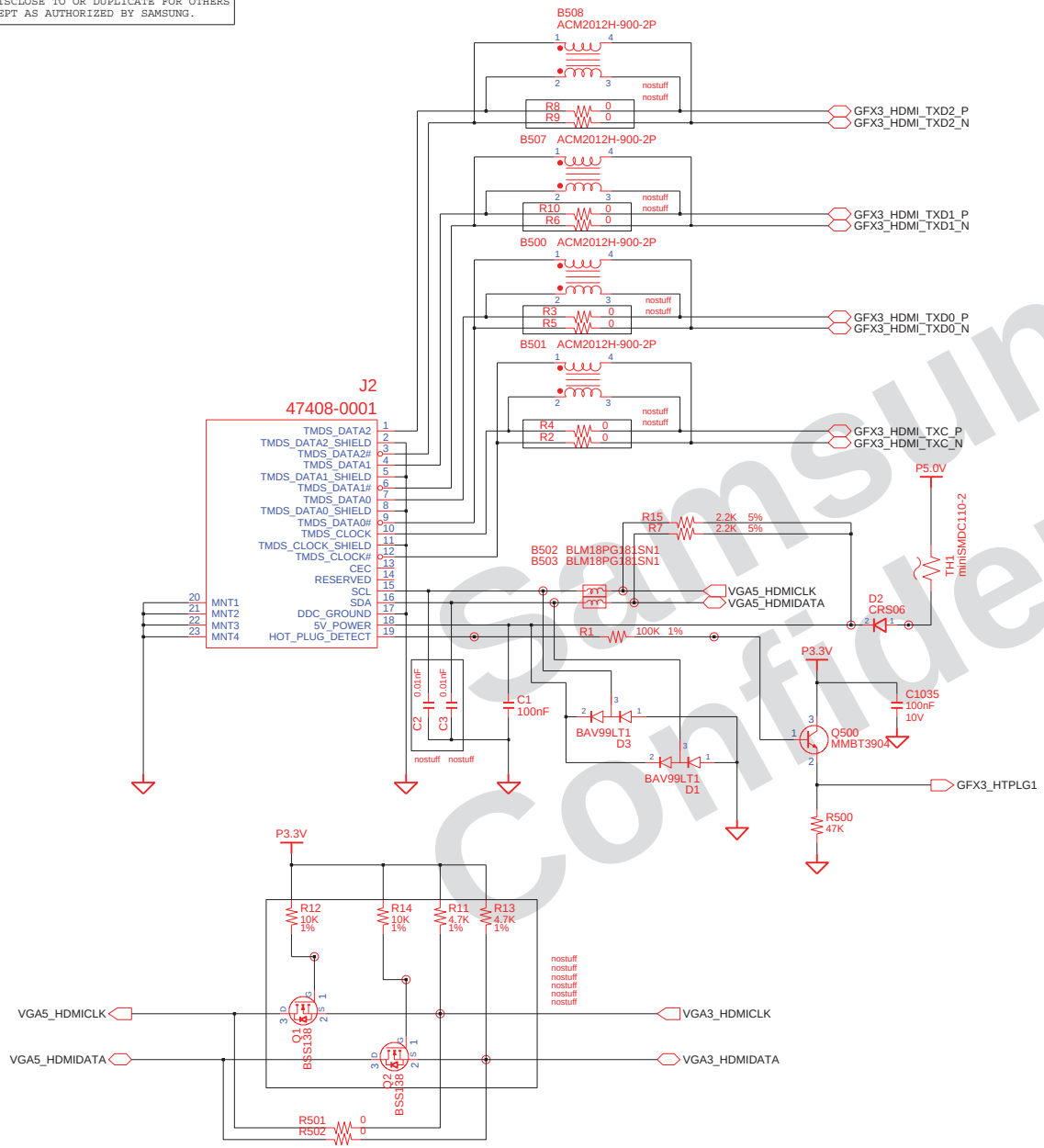

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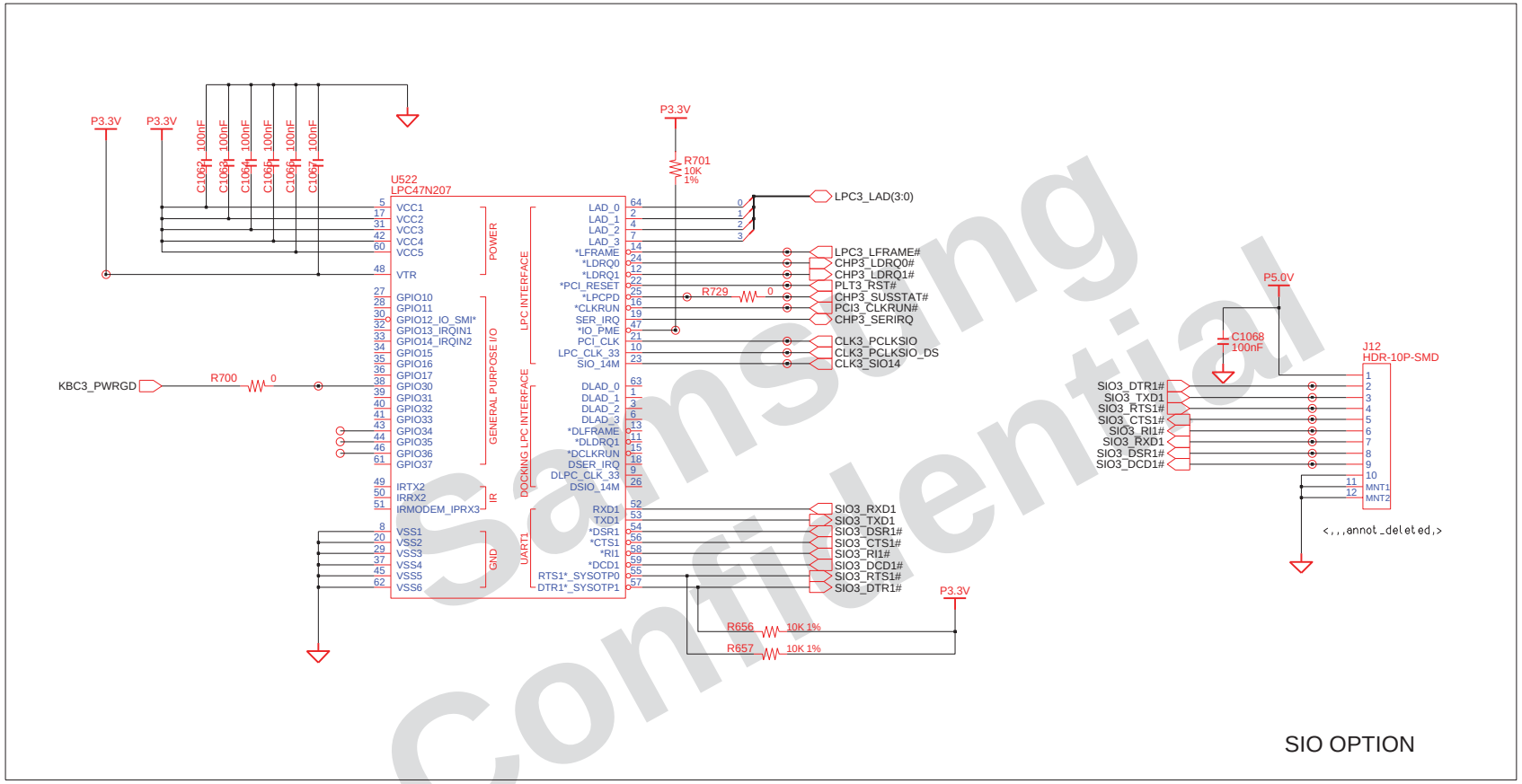

SIO OPTION

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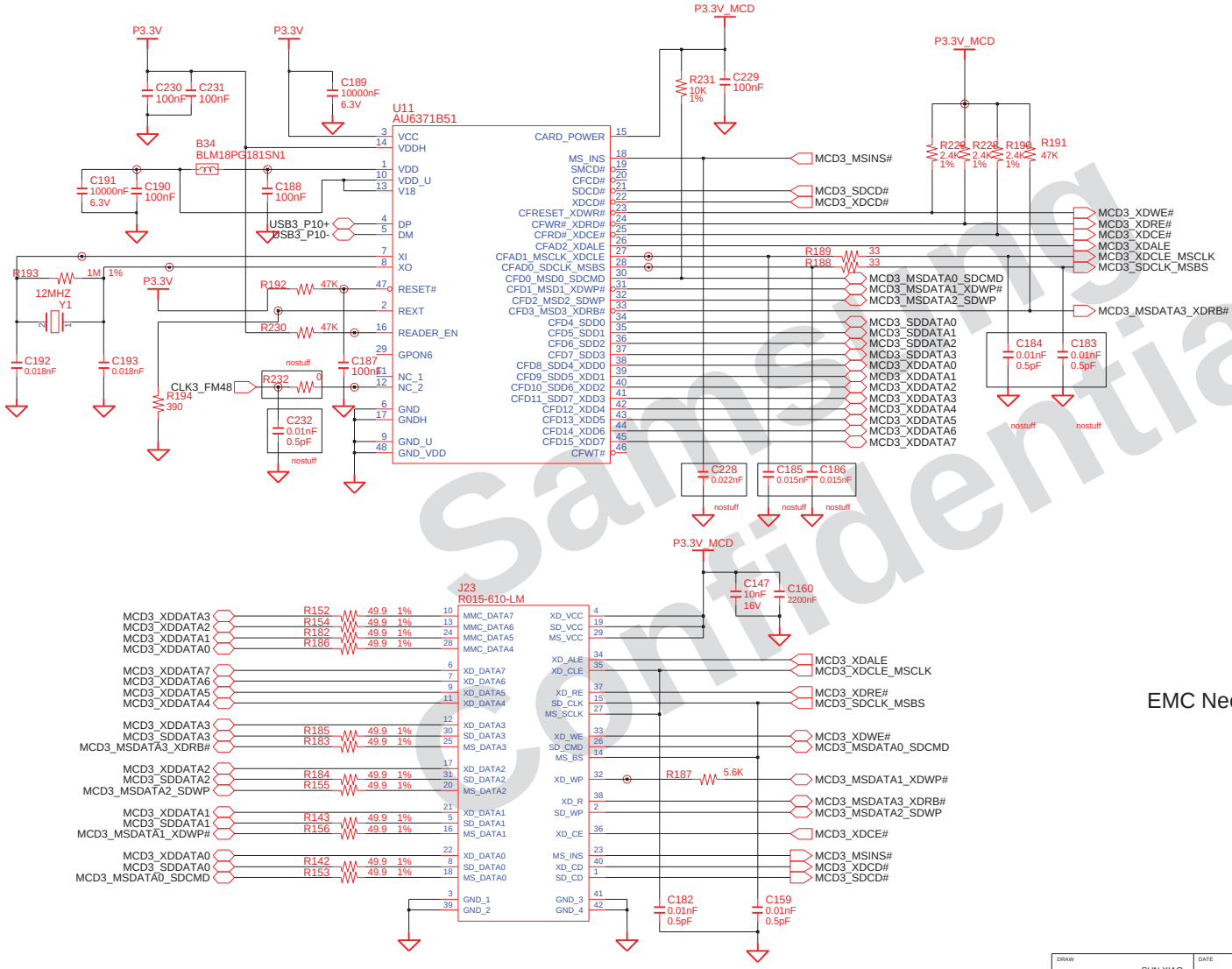
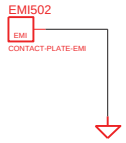


EMC Need Added for SD card Noise



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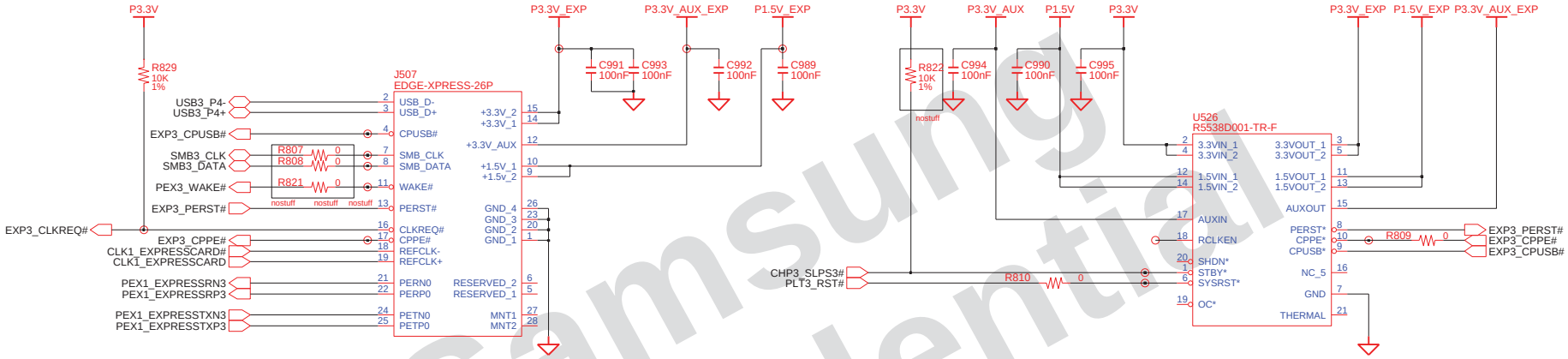

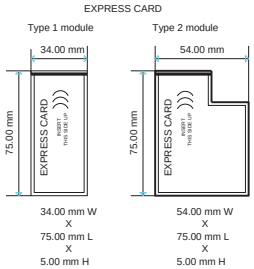

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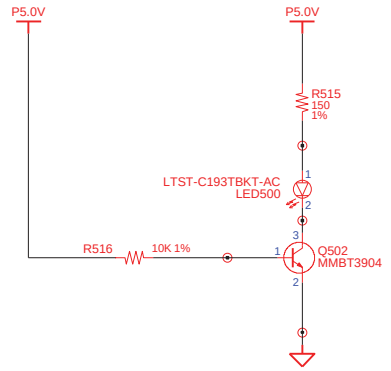
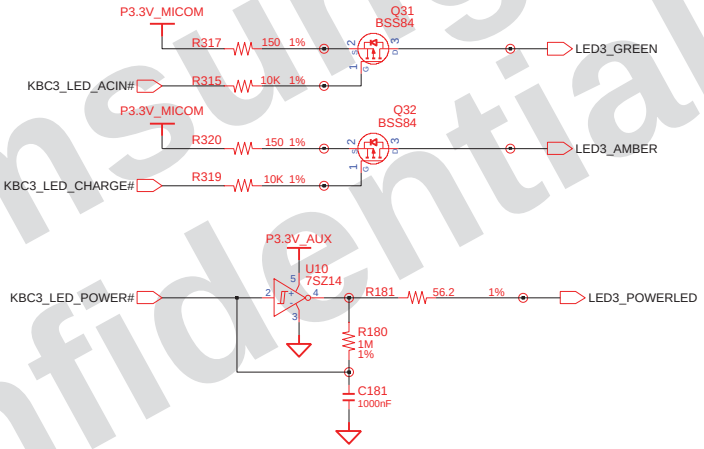
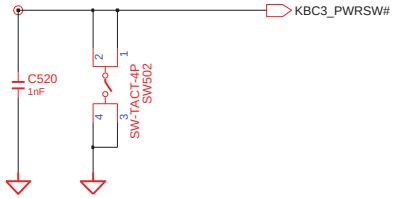
POWER ON LED



ADAPTERIN/CHARGING LED



POWER ON SW BUTTON



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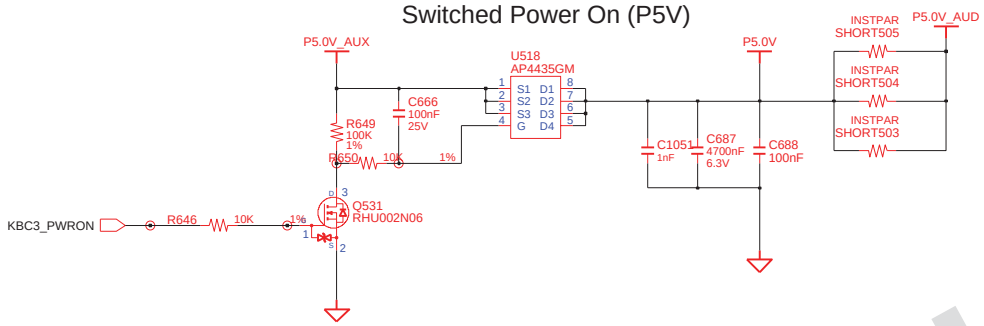
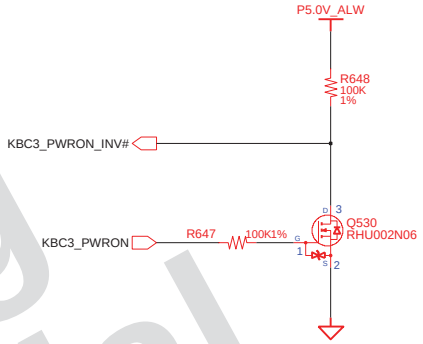
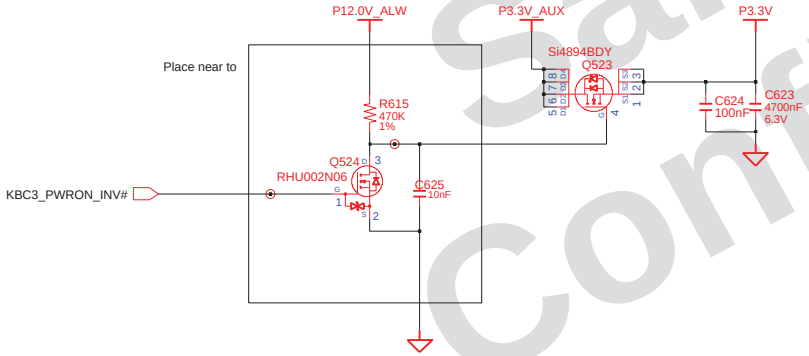
Switched Power On (P5V)



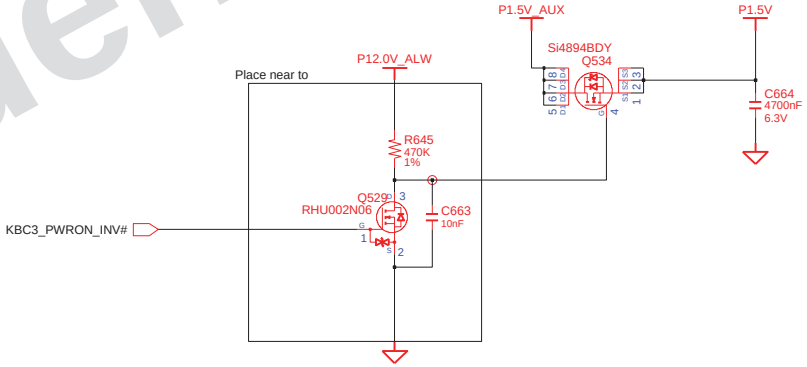
SIGNAL SWITCH



Switched Power On (P3.3V)



Switched Power On (P1.5V)



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DRAW SUN XIAO,	DATE 2/27/2008	TITLE Gevena 2 ext MAIN SWITCH POWER P1.5V	SAMSUNG ELECTRONICS
CHECK WU SHIJIANG,	DEV. STEP PV		
APPROVAL BYEONGCHANG LEE,	REV 1.0		PART NO. BA41-####A
		May 08, 2008 19:01:59 PM	PAGE 18 OF 23

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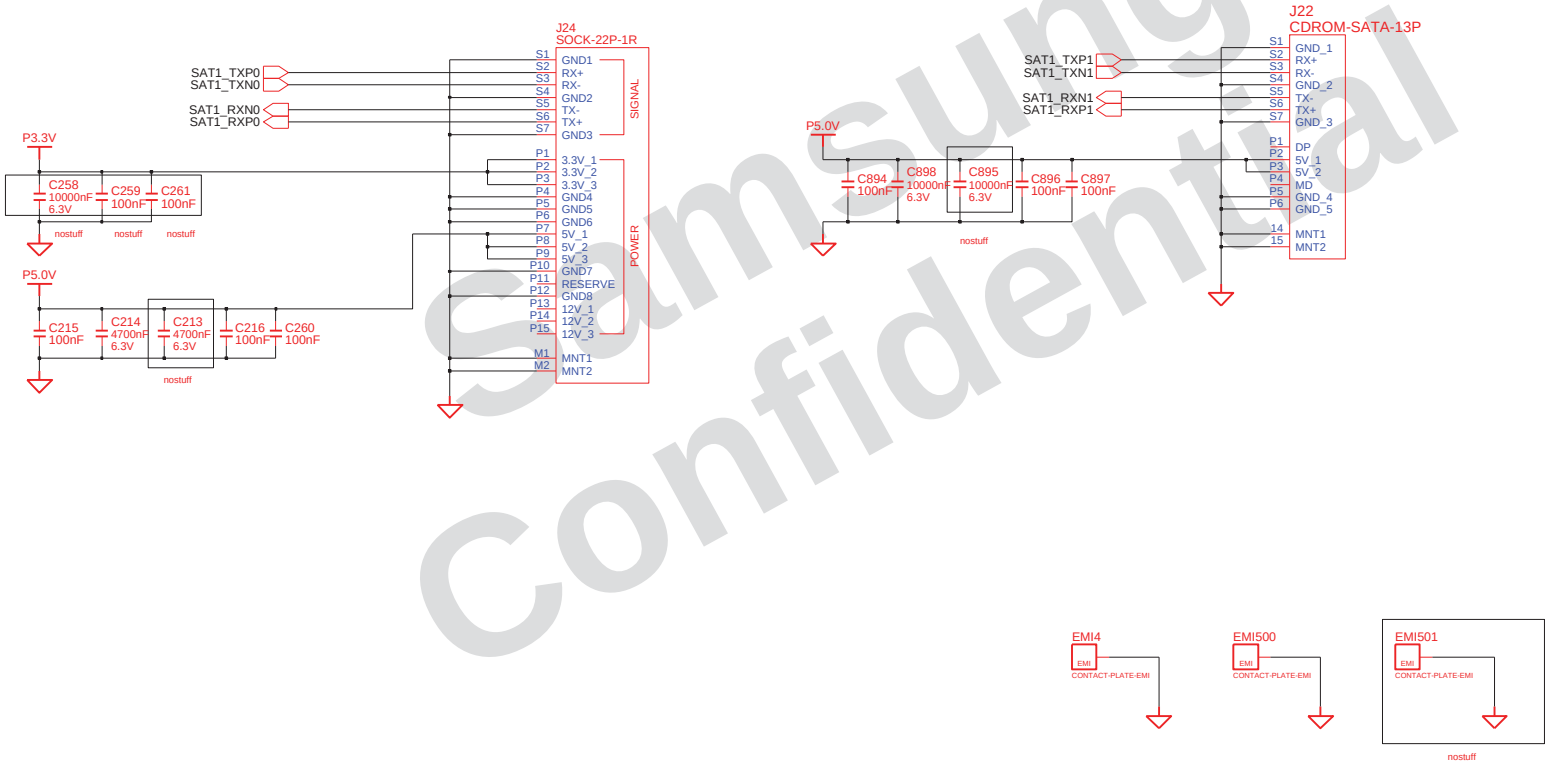
Main to HDD



DRAW: SUN XIAO,	DATE: 2/27/2008	TITLE: Gevena 2 ext CONNECTOR HDD & ODD CONNECTOR	SAMSUNG ELECTRONICS
CHECK: WU SHIJIANG,	DEV. STEP: PV		
APPROVAL: BYEONGCHANG LEE,	REV: 1.0		PART NO.: BA41-####A
		May 08, 2008 19:01:59 PM	PAGE 19 OF 23

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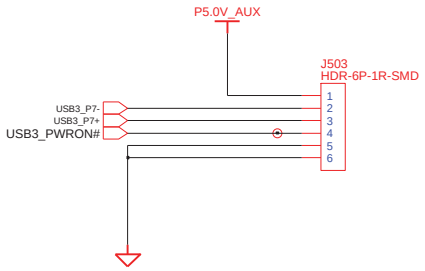
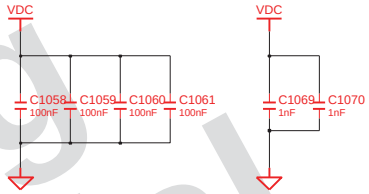
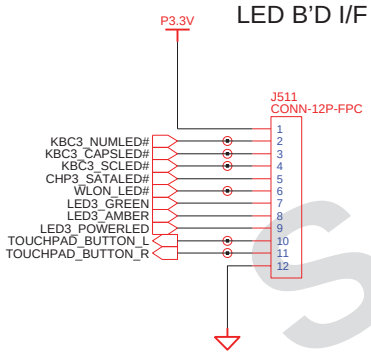
USB I/F B'D



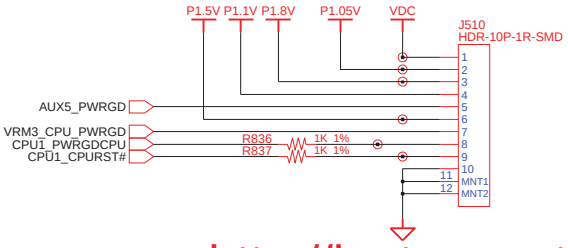
EMC ADD decape CAP



LED B'D I/F



ICT PORT



DRAW SUN XIAO,	DATE 2/27/2008	TITLE Gevena 2 ext	SAMSUNG ELECTRONICS
CHECK WU SHIJIANG,	DEV. STEP PV	KEYBOARD 80PORT ICT PORT	
APPROVAL BYEONGCHANG LEE,	REV 1.0	LID SWITCH LED B'D USB I/O B'D	PART NO. BA41-####A
		May 08, 2008 19:01:59 PM	PAGE 20 OF 23

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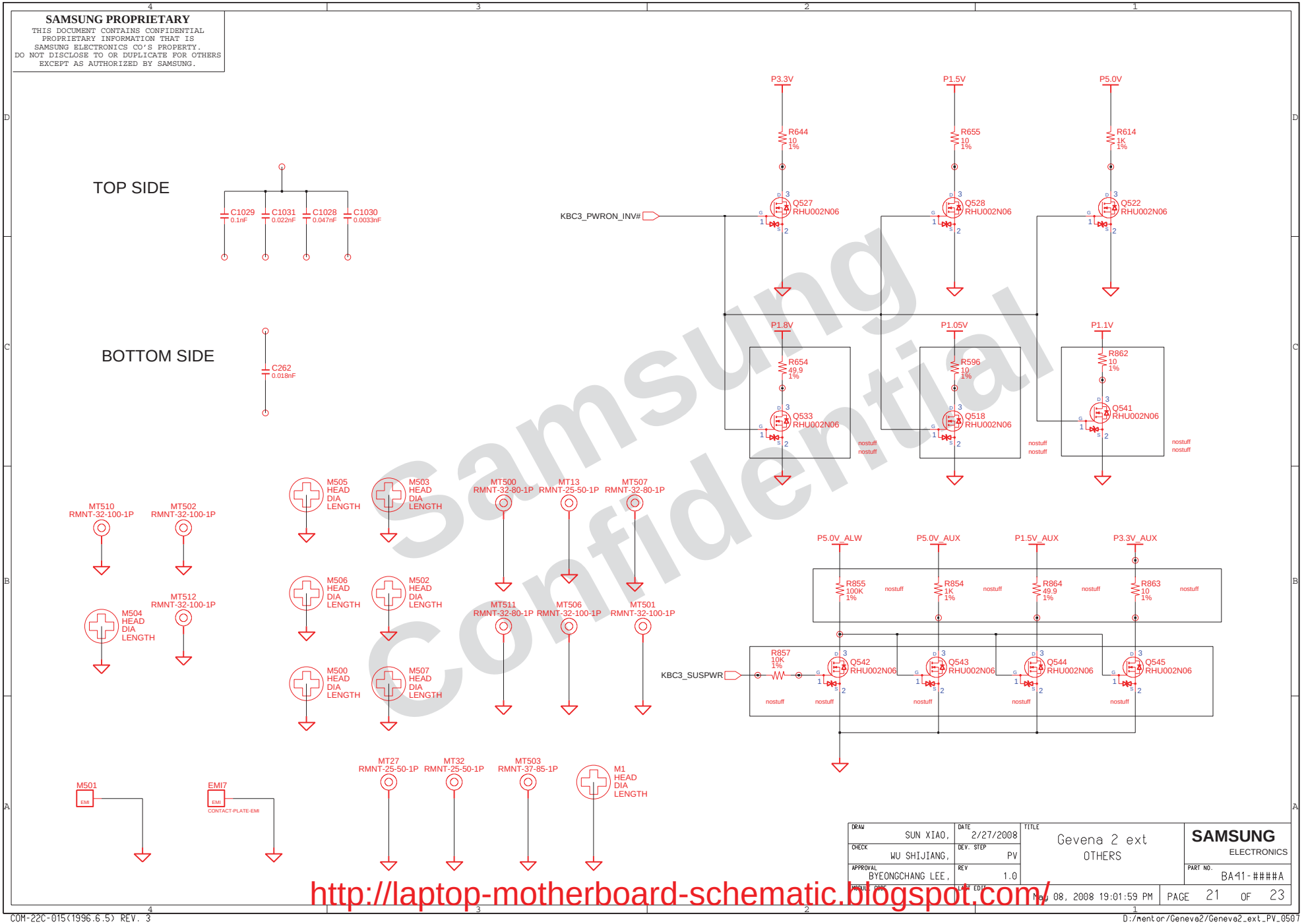

DRAW: SUN XIAO,	DATE: 2/27/2008	TITLE: Gevena 2 ext OTHERS	SAMSUNG ELECTRONICS
CHECK: WU SHIJIANG,	DEV. STEP: PV		
APPROVAL: BYEONGCHANG LEE,	REV: 1.0		PART NO. BA41-####A
MODULE CODE:	LAST EDIT: May 08, 2008 19:01:59 PM		PAGE 21 OF 23

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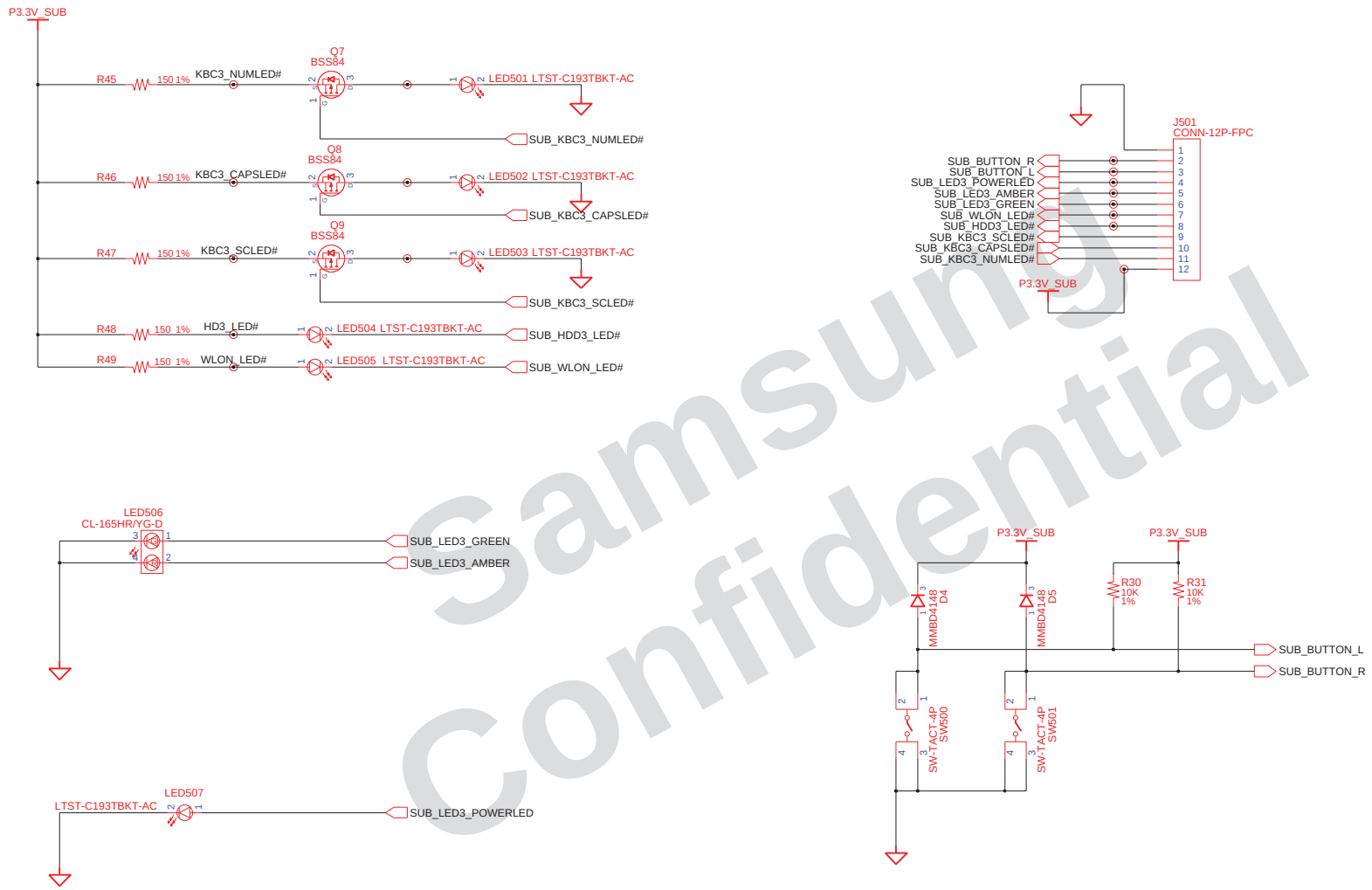
TOUCHPAD AND LED B'D



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DRAW SUN XIAO,	DATE 2/27/2008	TITLE Gevena 2 ext TOUCHPAD AND LED B'D	SAMSUNG ELECTRONICS
CHECK WU SHIJIANG,	DEV. STEP PV		
APPROVAL BYEONGCHANG LEE,	REV 1.0		PART NO. BA41-####A
MODULE CODE	LAST EDIT May 08, 2008 19:01:59 PM		PAGE 22 OF 60

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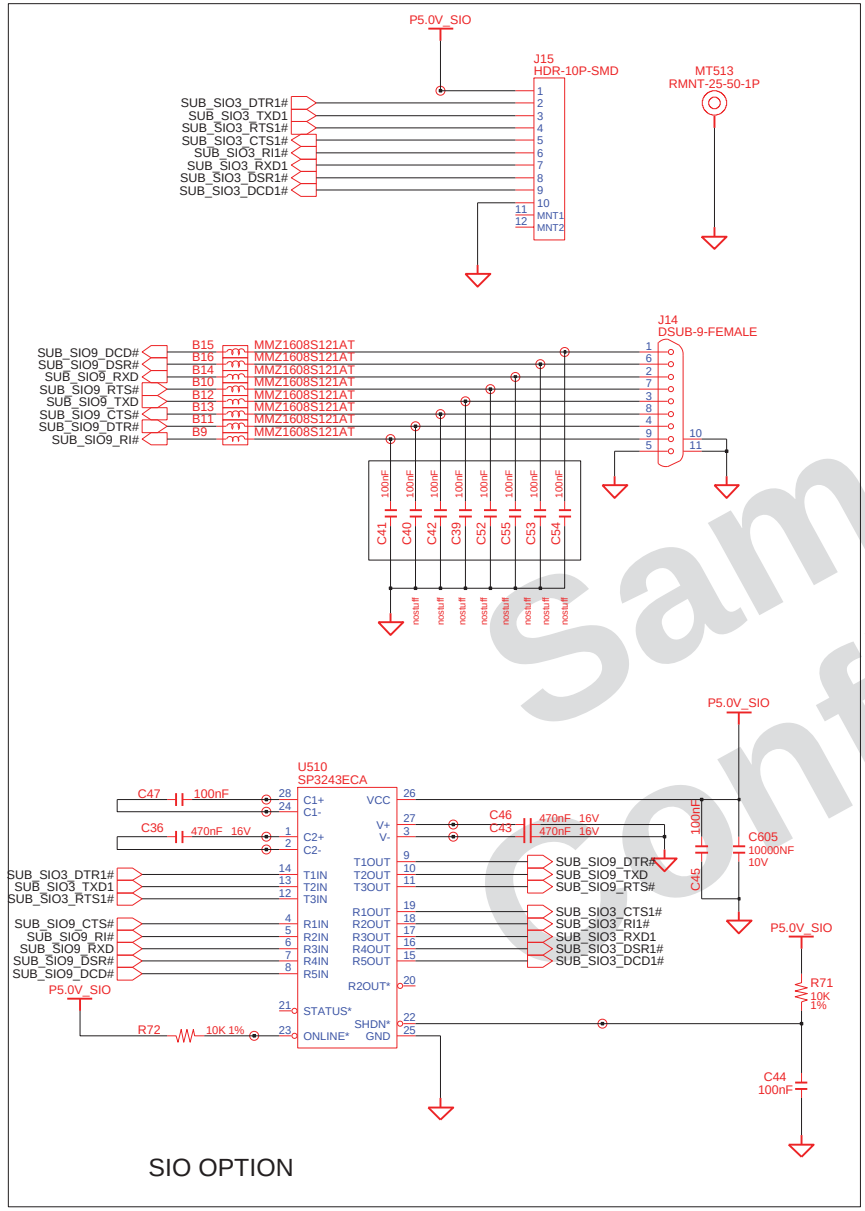
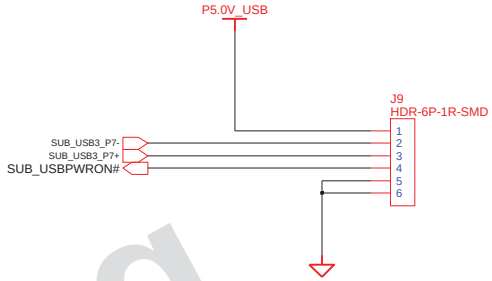
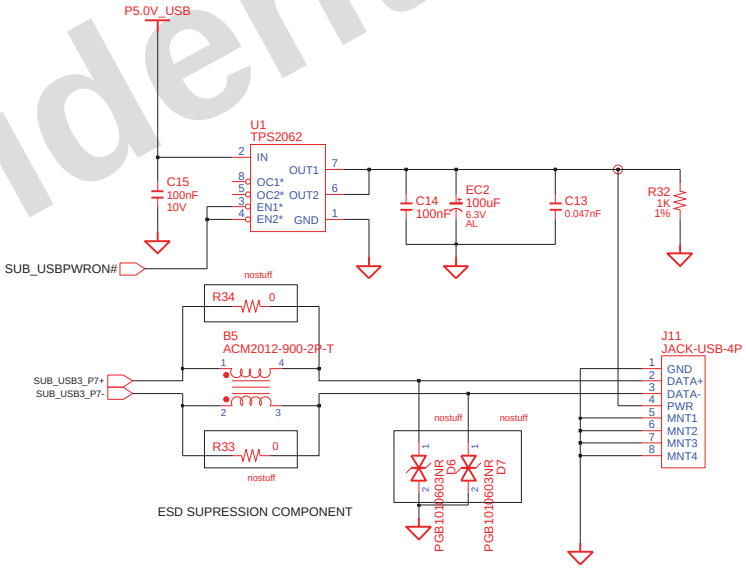
SIO AND USB SUB B'D







DRAW SUN XIAO,	DATE 2/27/2008	TITLE Gevena 2 ext MIO BOARD USB AND SIO SUB B'D	SAMSUNG ELECTRONICS
CHECK WU SHIJIANG,	DEV. STEP PV		
APPROVAL BYEONGCHANG LEE,	REV 1.0		PART NO. BA41-####A
PRODUCT CODE	LAST EDIT May 08, 2008 19:01:59 PM		PAGE 23 OF 60

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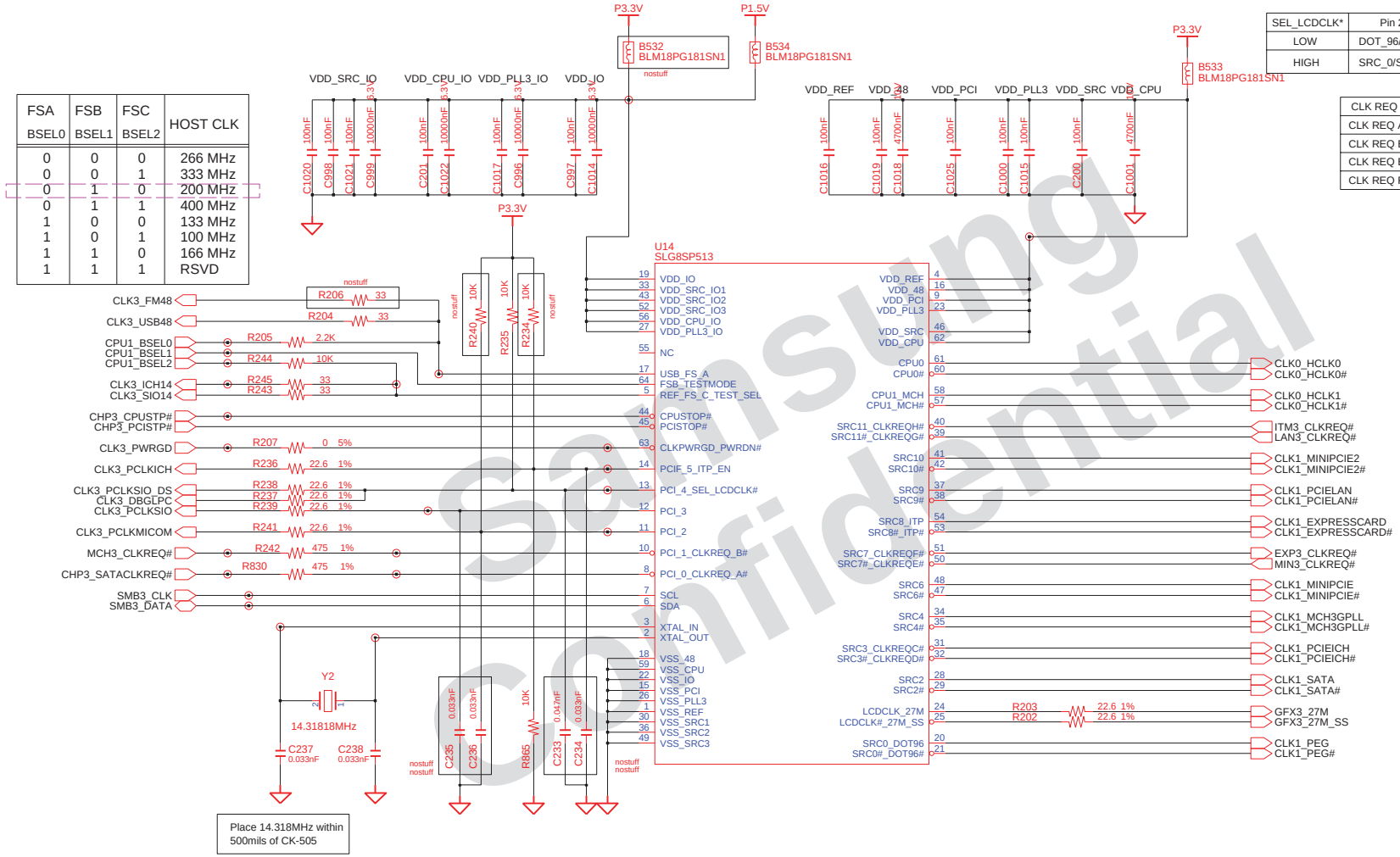
FSA BSEL0	FSB BSEL1	FSC BSEL2	HOST CLK
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD

SEL_LCDCLK*	Pin 20/21	Pin 24/25
LOW	DOT_96/DOT_96#	LCDCLK/LCDCLK#
HIGH	SRC_0/SRC_0#	27M & 27M_SS

CLK REQ	DEVICE	SRC PORT
CLK REQ A	SATA	SRC2
CLK REQ B	GMCH	SRC4
CLK REQ E	MINI CARD	SRC6
CLK REQ F	EXPRESS CARD	SRC8



Place 14.318MHz within 500mils of CK-505

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DRAW: SUN XIAO,	DATE: 2/27/2007	TITLE: Gevena 2 ext Main_Clock_Circuit CK_Clock_505M	SAMSUNG ELECTRONICS
CHECK: WU SHIJIANG,	DEV. STEP: PV		
APPROVAL: BYEONGCHANG LEE,	REV: 1.0		PART NO. BA41-####A
MODULE CODE: Unassigned	LAST EDIT: May 08, 2008 19:01:59 PM		PAGE 1 OF 1

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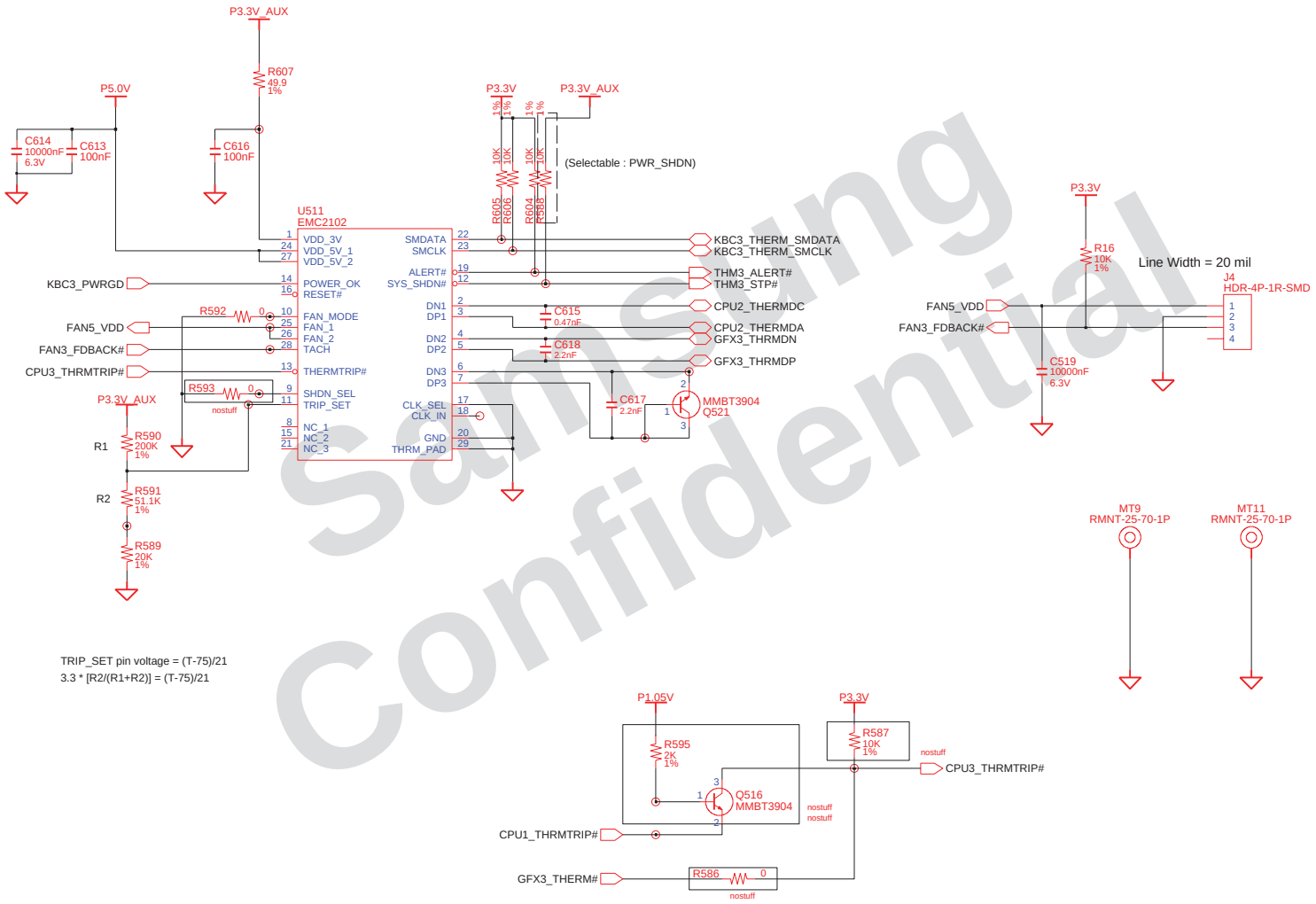
THERMAL SENSOR & FAN CONTROL



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DESIGN: SUN XIAO,	DATE: 2/27/2008	TITLE: Gevena 2 ext	SAMSUNG ELECTRONICS
CHECK: WU SHIJIANG,	DEV. STEP: PV	THERMAL_SENSOR_SMSC_EMC2102	
APPROVAL: BYEONGCHANG LEE,	REV: 1.0	THERMAL_SENSOR_SMSC_EMC2102	PART NO. BA41-####A
MODULE CODE:	LAST EDIT: May 08, 2008 19:01:59 PM	PAGE 1 OF 1	

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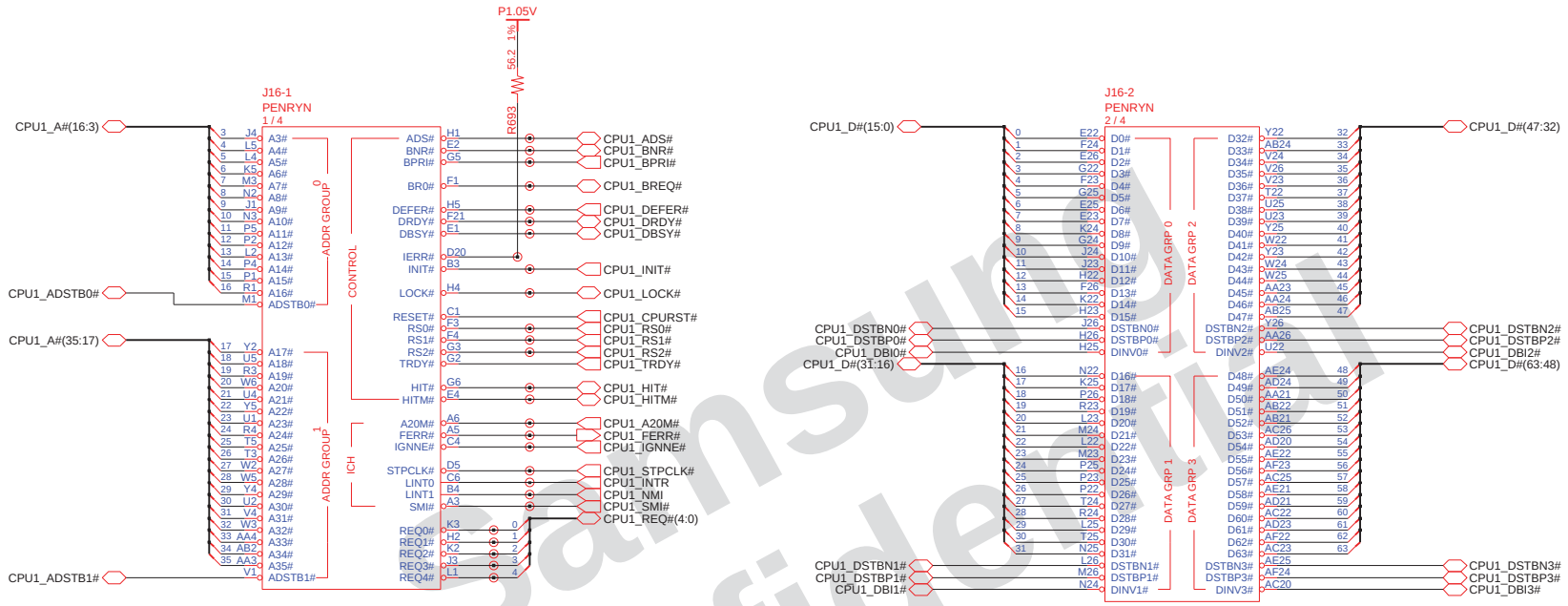
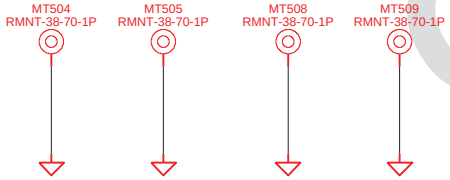


CPU CONNECTOR P/N 3704-001153



DRAW: SUN XIAO,	DATE: 2/27/2008	TITLE: Gevena 2 ext CPU PENRYN (1/3)	SAMSUNG ELECTRONICS
CHECK: WU SHIJIANG,	DEV. STEP: PV		
APPROVAL: BYEONGCHANG LEE,	REV: 1.0		PART NO.: BA41-####A
MODULE CODE: Undefined	LAST EDIT: May 08, 2008 19:01:59 PM		PAGE 1 OF 3

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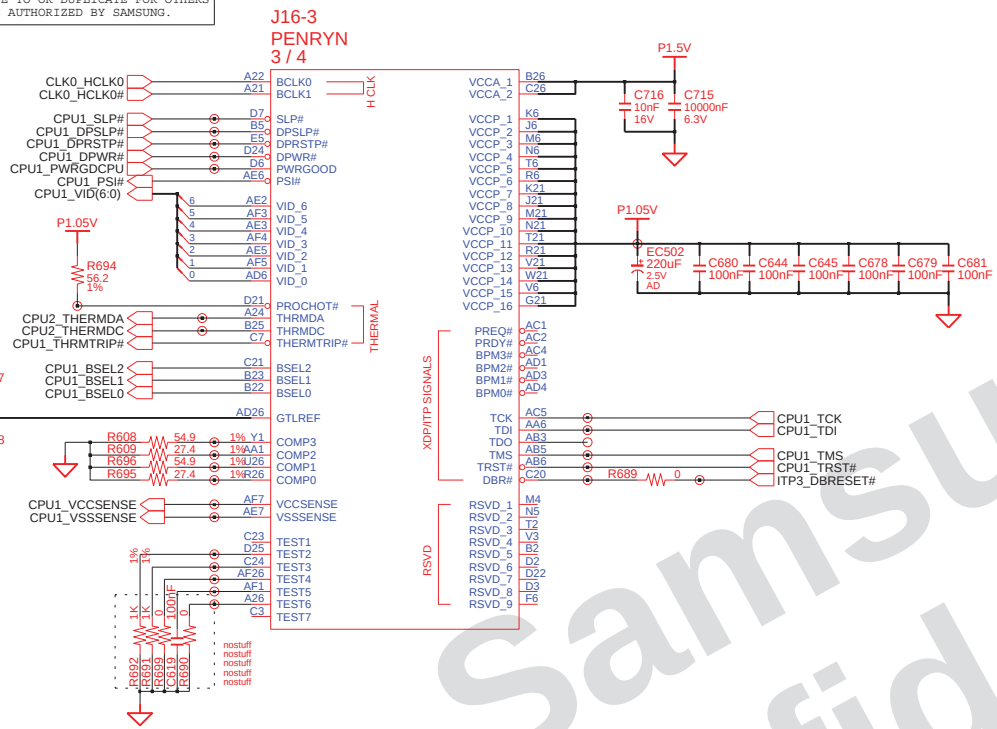
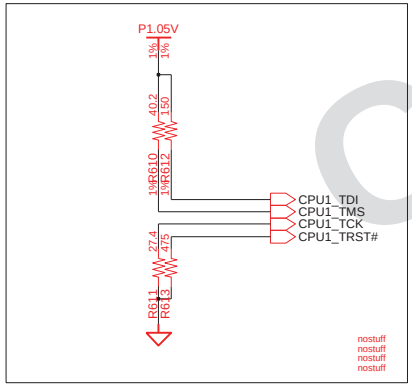


ITP DISABLE



CPU Core Voltage Table

IMVP-6

Active Mode VID(6:0)	Voltage	Active/Deeper Sleep Dual Mode Region VID(6:0)	Voltage	Deeper Sleep/Extended Deeper Sleep Dual Mode Region VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 1 0	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 0 1 1	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 0 1 1	0.9625 V	1 0 1 0 1 0 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 0	0.9500 V	1 0 1 0 1 0 1	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 0 1	0.9375 V	1 0 1 0 1 1 0	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 0	0.9250 V	1 0 1 0 1 1 1	0.4125 V
0 0 0 0 1 1 1	1.4125 V	0 1 0 1 1 1 1	0.9125 V	1 0 1 1 0 0 0	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 0	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 0 1	0.8875 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 1 0	0.8750 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 0 0 1 1	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 0 1 0 0	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 0 1	1.3375 V	0 1 1 0 1 0 1	0.8375 V	1 0 1 1 1 1 0	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 0 1 1 0	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 0 1 1 1	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	1.3000 V	0 1 1 1 0 0 0	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 0 1	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	1.2750 V	0 1 1 1 0 1 0	0.7750 V	1 1 0 0 0 1 1	0.2625 V
0 0 1 0 0 1 1	1.2625 V	0 1 1 1 0 1 1	0.7625 V	1 1 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 0 0	0.7500 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 0 1	0.7375 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 1 0	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 1 0 1 1 1	1.2125 V	0 1 1 1 1 1 1	0.7125 V	1 1 0 1 0 0 0	0.2000 V
0 0 1 1 0 0 0	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 1 0 1 0 0 1	0.1875 V
0 0 1 1 0 0 1	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 0	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 1 0 1 0 1 1	0.1625 V
0 0 1 1 0 1 1	1.1625 V	1 0 0 0 0 1 1	0.6625 V	1 1 0 1 1 0 0	0.1500 V
0 0 1 1 1 0 0	1.1500 V	1 0 0 0 1 0 0	0.6500 V	1 1 0 1 1 0 1	0.1375 V
0 0 1 1 1 0 1	1.1375 V	1 0 0 0 1 0 1	0.6375 V	1 1 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 0	1.1250 V	1 0 0 0 1 1 0	0.6250 V	1 1 0 1 1 1 1	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 0 0 0 1 1 1	0.6125 V	1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 1 0 0 0	0.6000 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 1 0 0 1	0.5875 V	1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 1 0 1 0	0.5750 V	1 1 1 0 0 1 1	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 1 0 1 1	0.5625 V	1 1 1 0 1 0 0	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 0 0 1 1 0 0	0.5500 V	1 1 1 0 1 0 1	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 0 0 1 1 0 1	0.5375 V	1 1 1 0 1 1 0	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 0 0 1 1 1 0	0.5250 V	1 1 1 0 1 1 1	0.0125 V
0 1 0 0 1 1 1	1.0125 V	1 0 0 1 1 1 1	0.5125 V	1 1 1 1 0 0 0	0.0000 V
		1 0 1 0 0 0 0	0.5000 V	1 1 1 1 0 0 1	0.0000 V
				1 1 1 1 0 1 0	0.0000 V
				1 1 1 1 0 1 1	0.0000 V
				1 1 1 1 1 0 0	0.0000 V
				1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0	0.0000 V
				1 1 1 1 1 1 1	0.0000 V

	Active	Deeper Slp
DPRSLPVR	0	1
DPRSTP*	1	0
PSI2*	0 or 1	0 or 1

*"1111111" : 0V power good asserted.

*Yonah Processor (2.33 GHz / 800 MHz : TBD)

GTLREF : Keep the Voltage divider within 0.5" of the first GTLREF0 pin with Zo=55ohm trace. Minimize coupling of any switching signals to this net.

COMP0,2(COMP1,3) should be connected with Zo=27.4ohm(55ohm) trace shorter than 1/2" to their respective Banias socket pins.

GND test points within 100mil of the VCC/VSSsense at the end of the line. Route the VCC/VSSsense as a Zo=55ohm traces with equal length. Observe 3:1 spacing b/w VCC/VSSsense lines and 25mil away (preferred 50mil) from any other signal. And GND via 100mil away from each of the VCC/VSS test point vias.

DRAW: SUN XIAO,	DATE: 2/27/2008	TITLE: Gevena 2 ext CPU PENRYN (2/3)	SAMSUNG ELECTRONICS
CHECK: WU SHIJIANG,	DEV. STEP: PV		
APPROVAL: BYEONGCHANG LEE,	REV: 1.0		PART NO. BA41-####A
MODULE CODE: Undefined	LAST EDIT: May 08, 2008 19:01:59 PM		PAGE 2 OF 3

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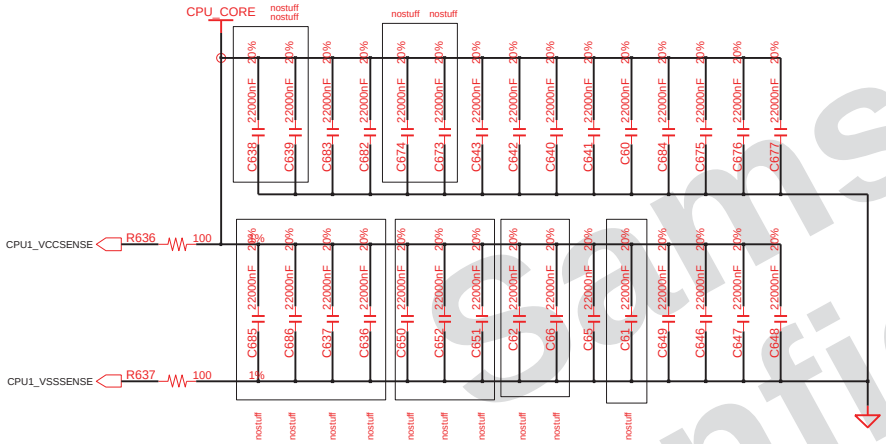
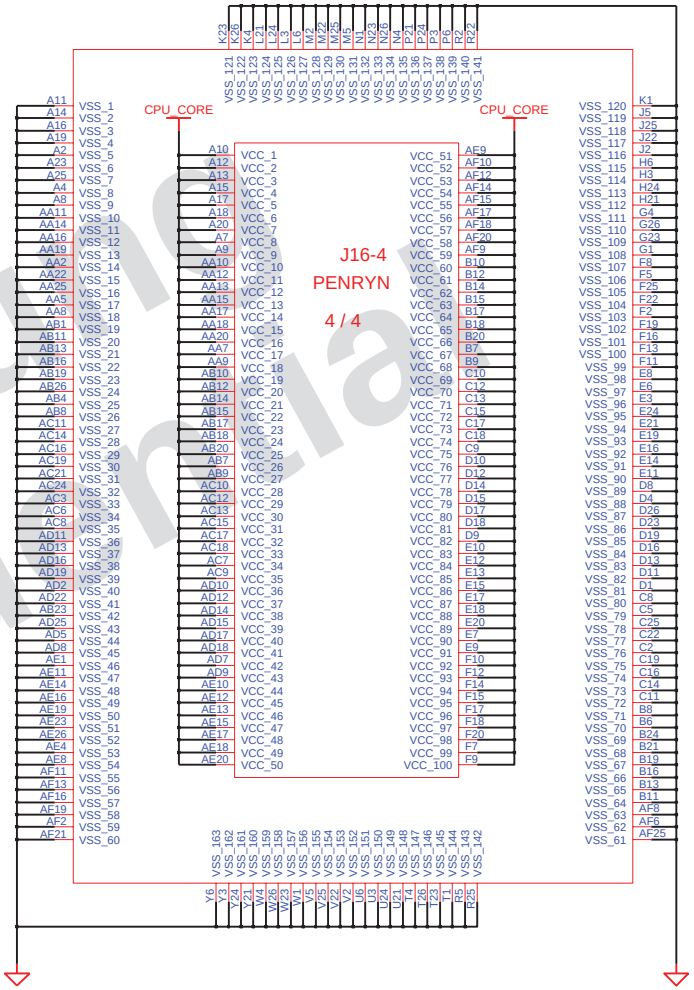


6x 330 uF : CPU VR side

Be Caution the placement of decap!!



DRAW SUN XIAO,	DATE 2/27/2008	TITLE Gevena 2 ext CPU PENRYN (3/3)	SAMSUNG ELECTRONICS
CHECK WU SHIJIANG,	DEV. STEP PV		
APPROVAL BYEONGCHANG LEE,	REV 1.0		PART NO. BA41-####A
PROJECT CODE Undefined	LAST EDIT May 08, 2008 19:01:59 PM		PAGE 3 OF 3

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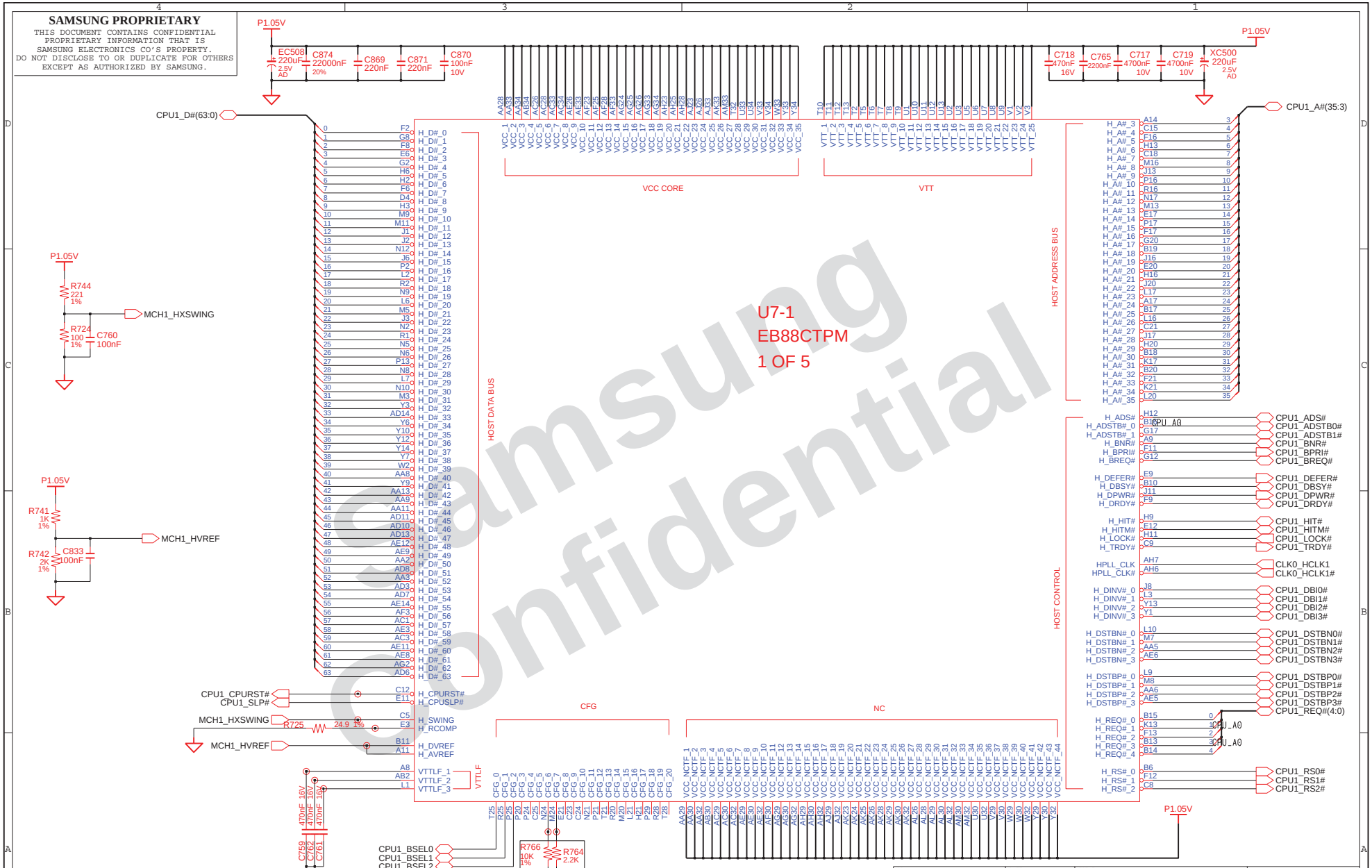

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DRAW: SUN XIAO,	DATE: 2/27/2008	TITLE: Gevena 2 ext MCH_CANTIGA_PM_DDR3 CANTIGA (1/5)	SAMSUNG ELECTRONICS
CHECK: WU SHIJIANG,	DEV. STEP: PV		
APPROVAL: BYEONGCHANG LEE,	REV: 1.0		PART NO. BA41-####A
MODULE CODE: Undefined		LAST SAVE: May 08, 2008 19:01:59 PM	PAGE 1 OF 5

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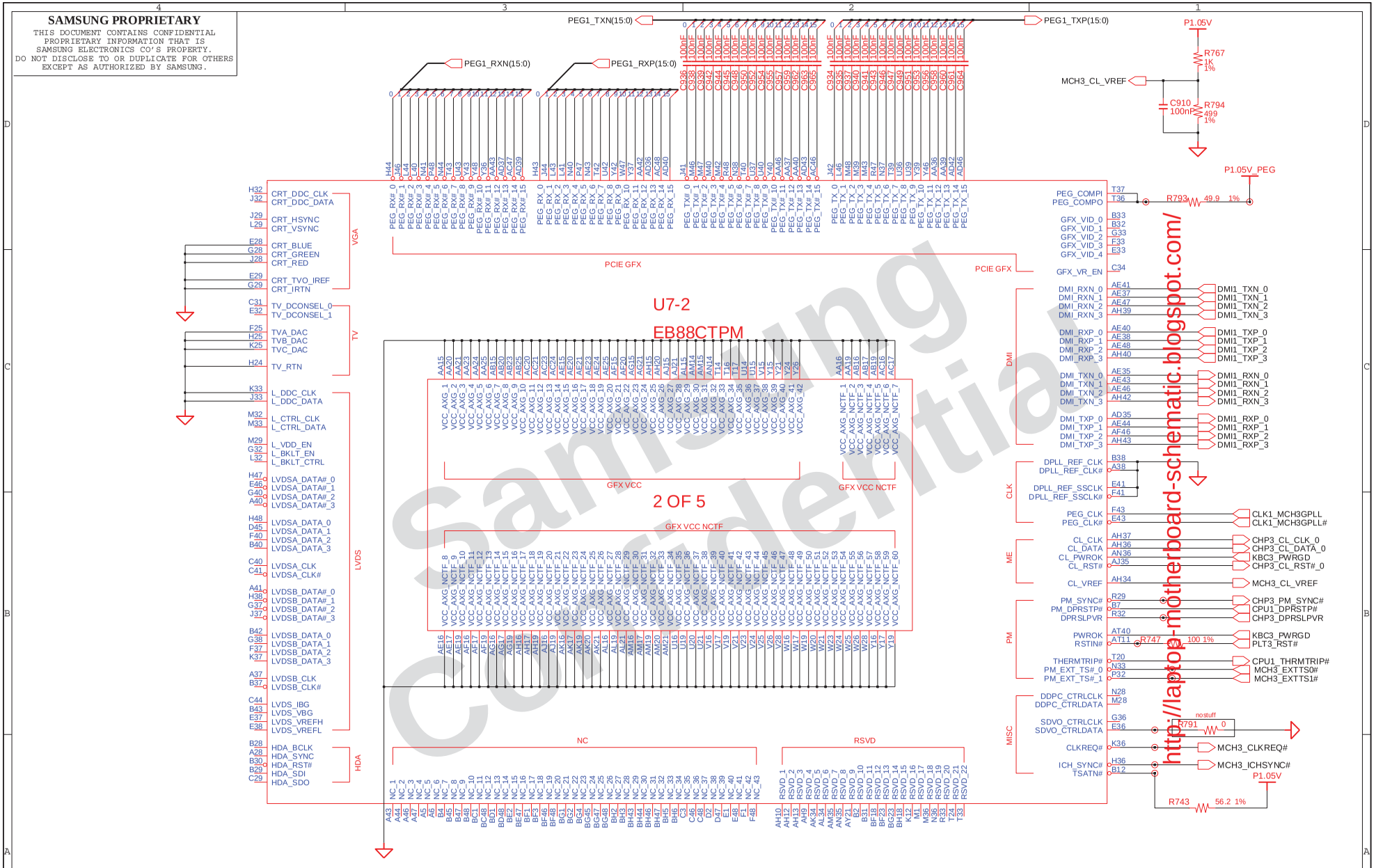

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CHECK: WU SHIJIANG,	DEV. STEP: PV		PART NO. BA41-####A
APPROVAL: BYEONGCHANG LEE,	REV: 1.0		
MODULE CODE	LAST EDIT: May 08, 2008 19:01:59 PM		PAGE 2 OF 5

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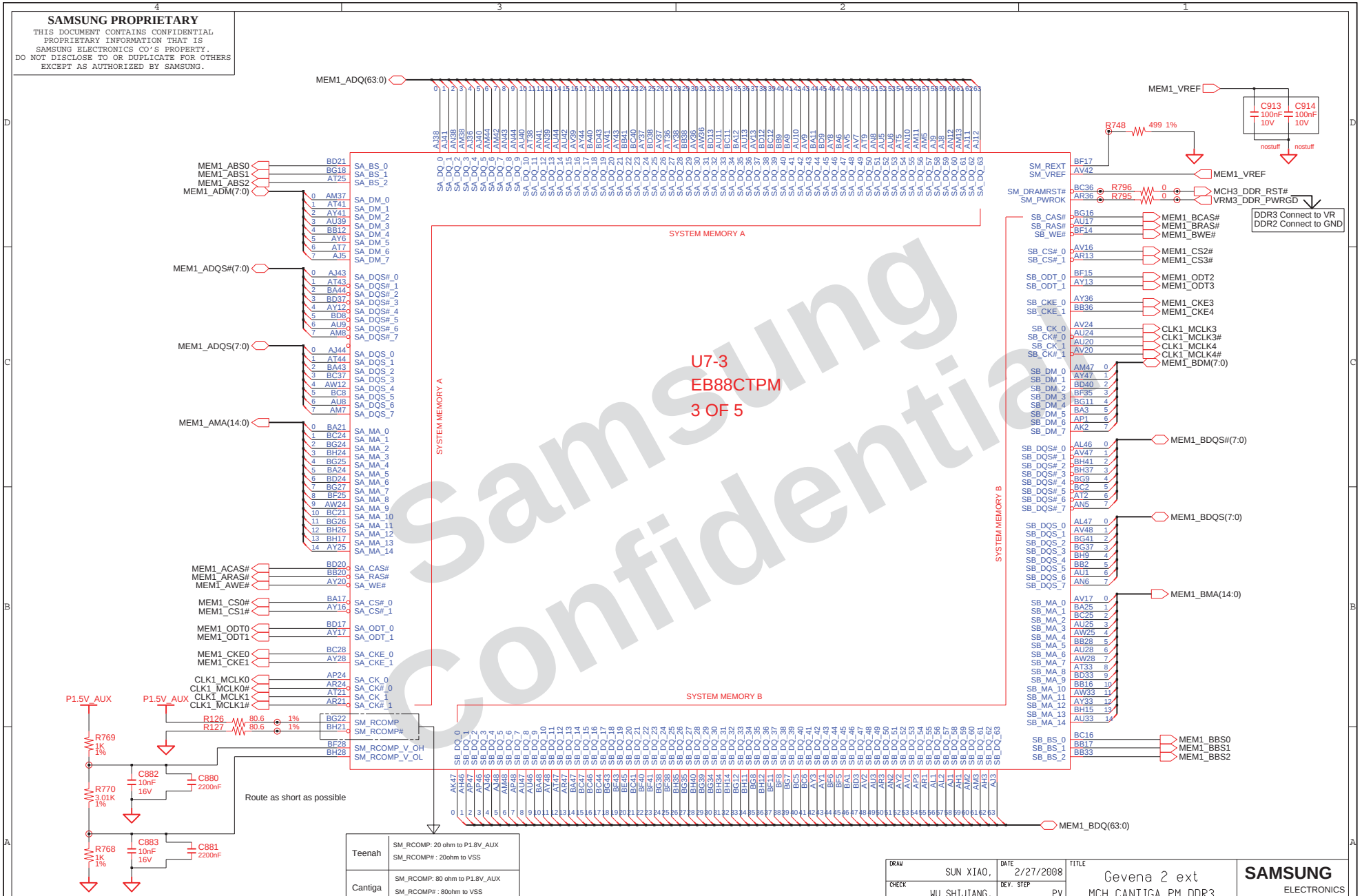

Teenah	SM_RCOMP: 20 ohm to P1.8V_AUX SM_RCOMP# : 20ohm to VSS
Cantiga	SM_RCOMP: 80 ohm to P1.8V_AUX SM_RCOMP# : 80ohm to VSS

DRAW SUN XIAO,	DATE 2/27/2008	TITLE Gevena 2 ext MCH_CANTIGA_PM_DDR3 CANTIGA (3/5)	SAMSUNG ELECTRONICS
CHECK WU SHIJIANG,	DEV. STEP PV		PART NO. BA41-####A
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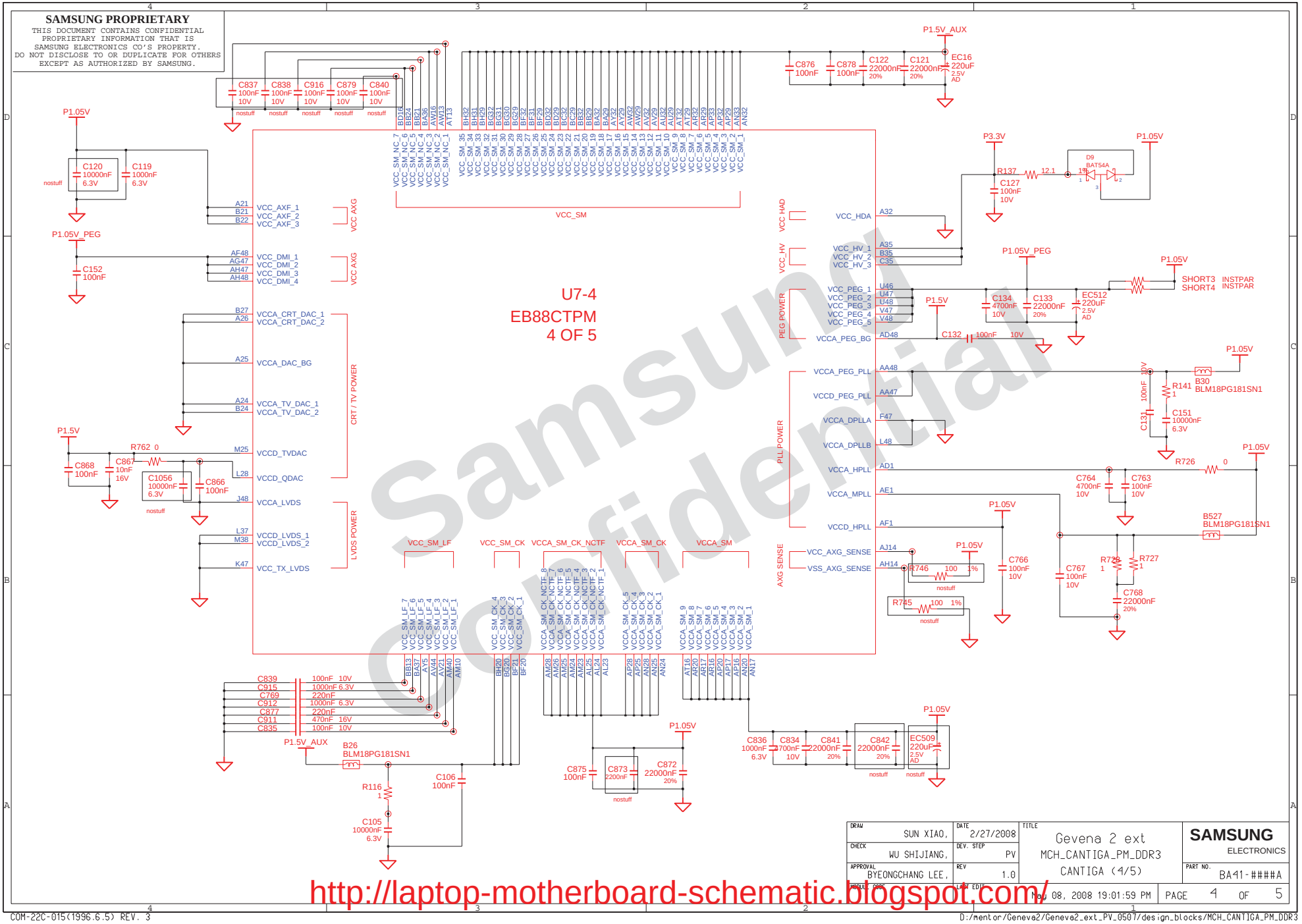

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APPROVAL	BYEONGCHANG LEE,	REV	1.0			PART NO. BA41-####A
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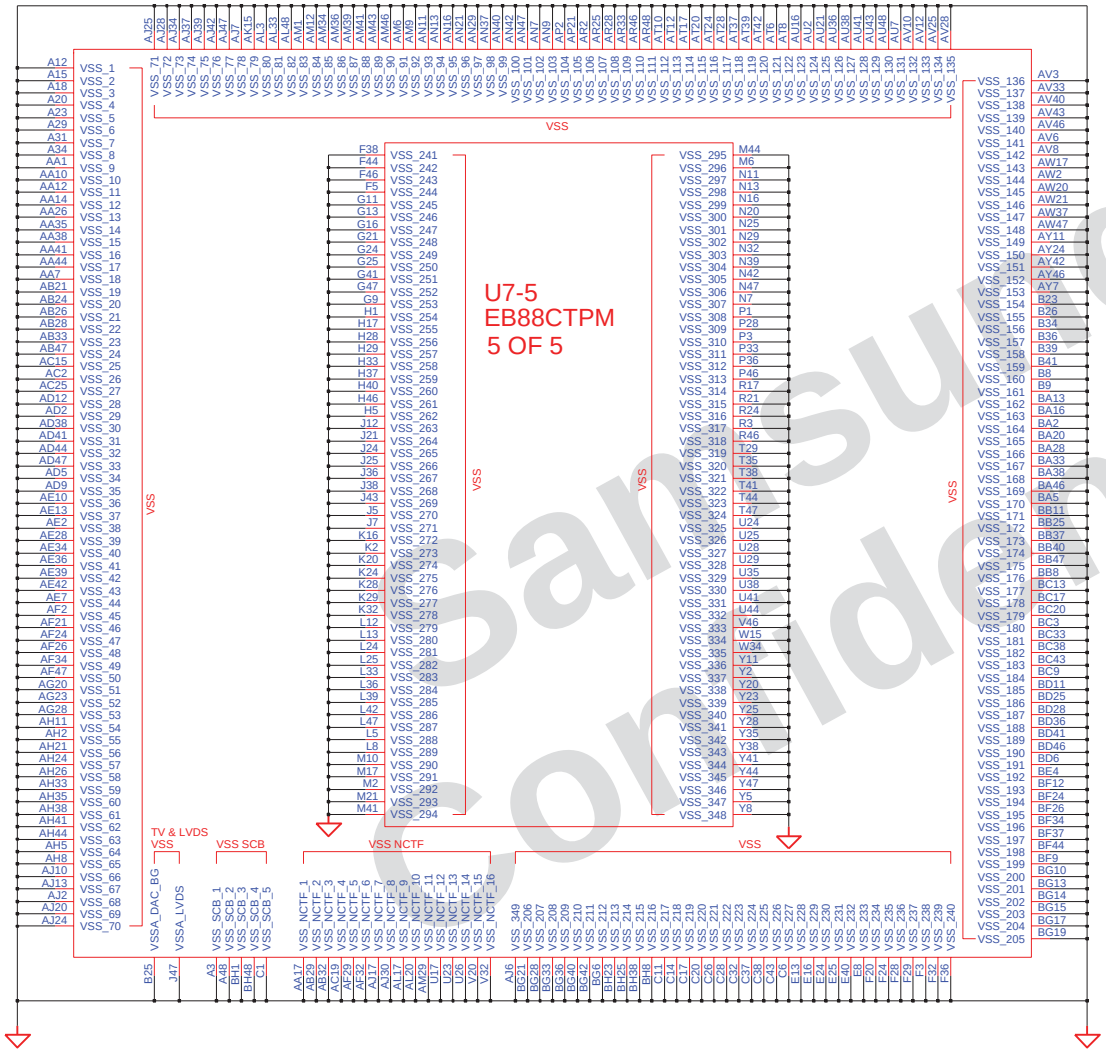

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APPROVAL BYEONGCHANG LEE,	REV 1.0		
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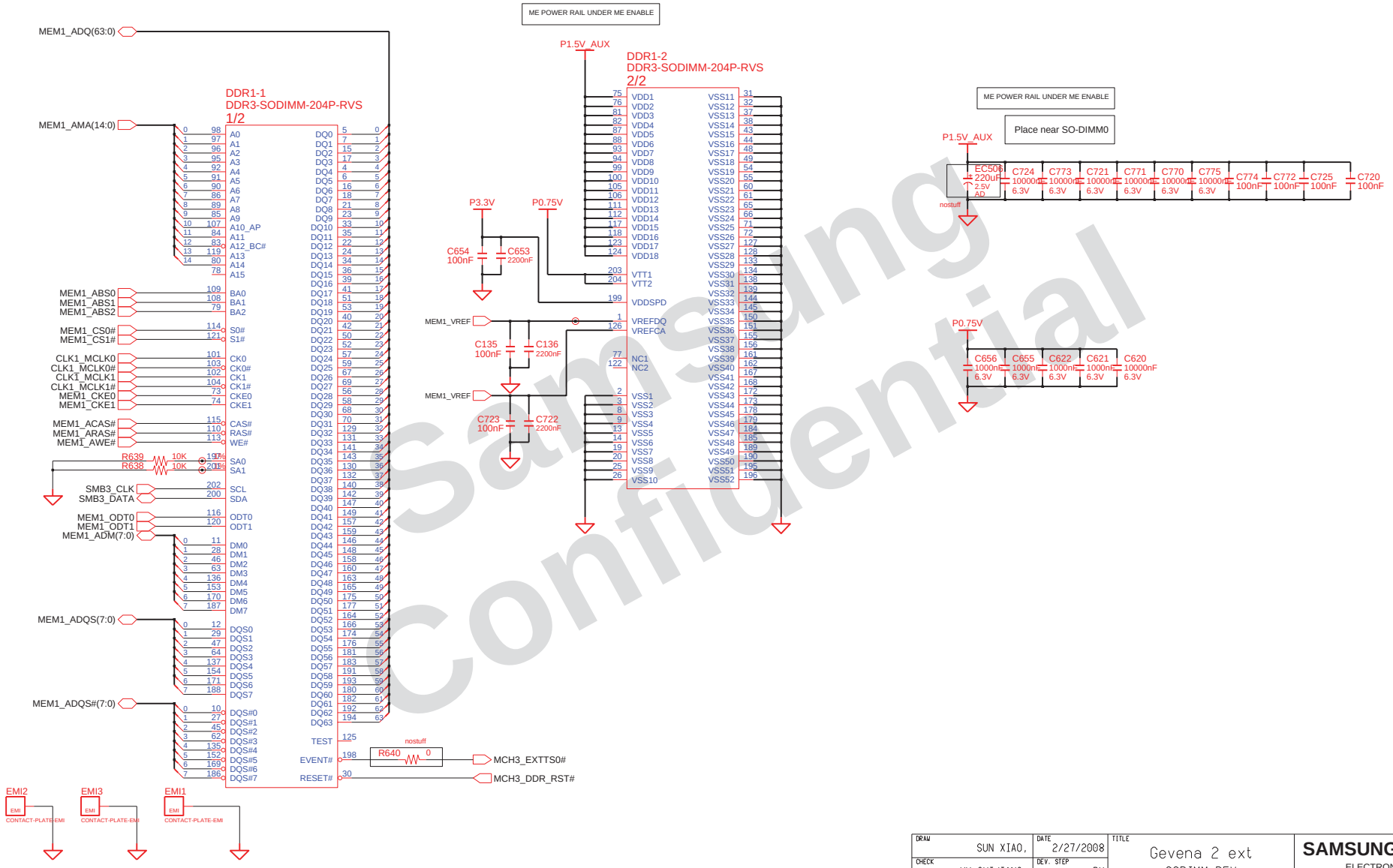

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CHECK WU SHIJIANG,	DEV. STEP PV		
APPROVAL BYEONGCHANG LEE,	REV 1.0		PART NO. BA41-####A
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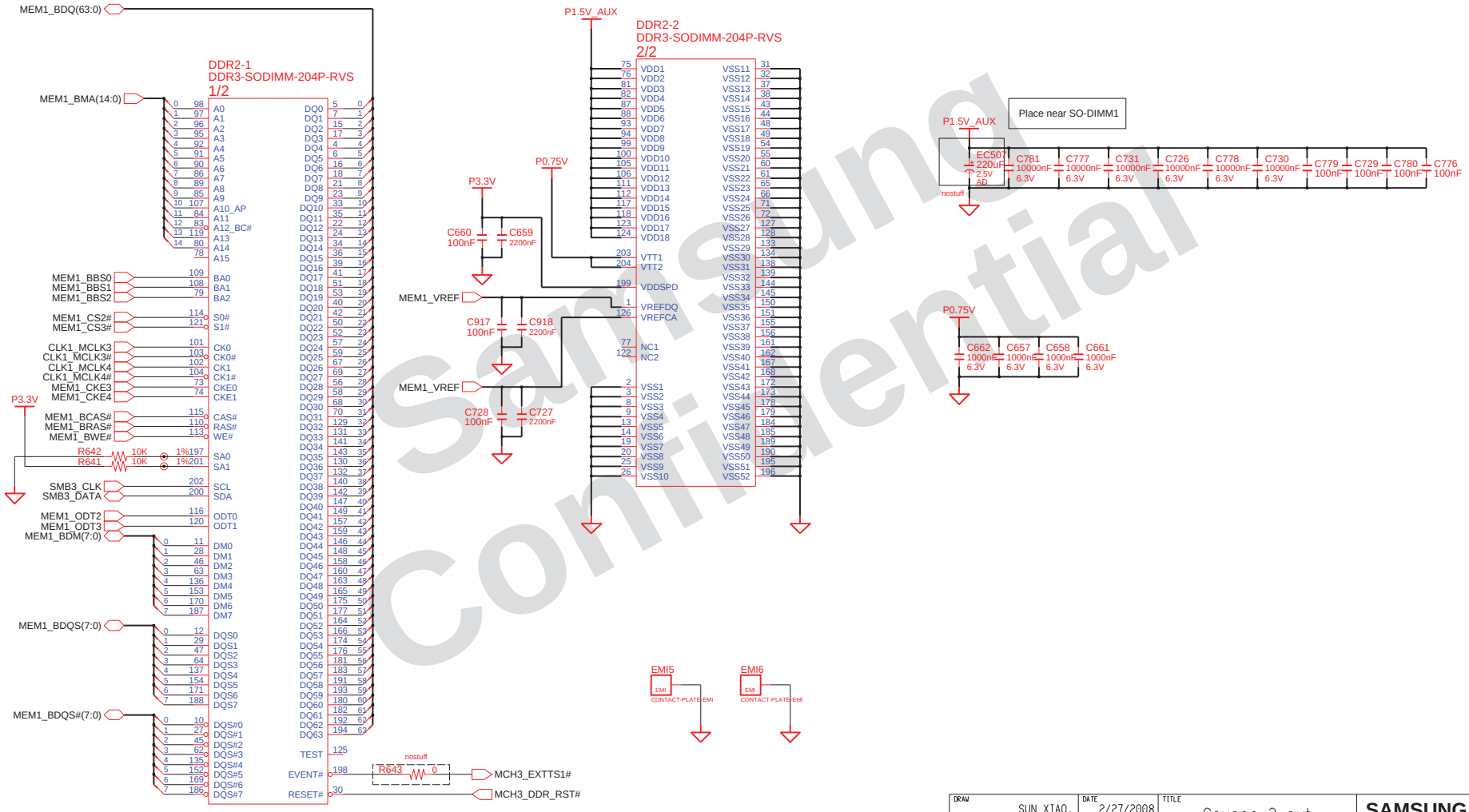
DDR SO-DIMM #1



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CHECK WU SHIJIANG,	DEV. STEP PV		PART NO. BA41-####A
APPROVAL BYEONGCHANG LEE,	REV 1.0		
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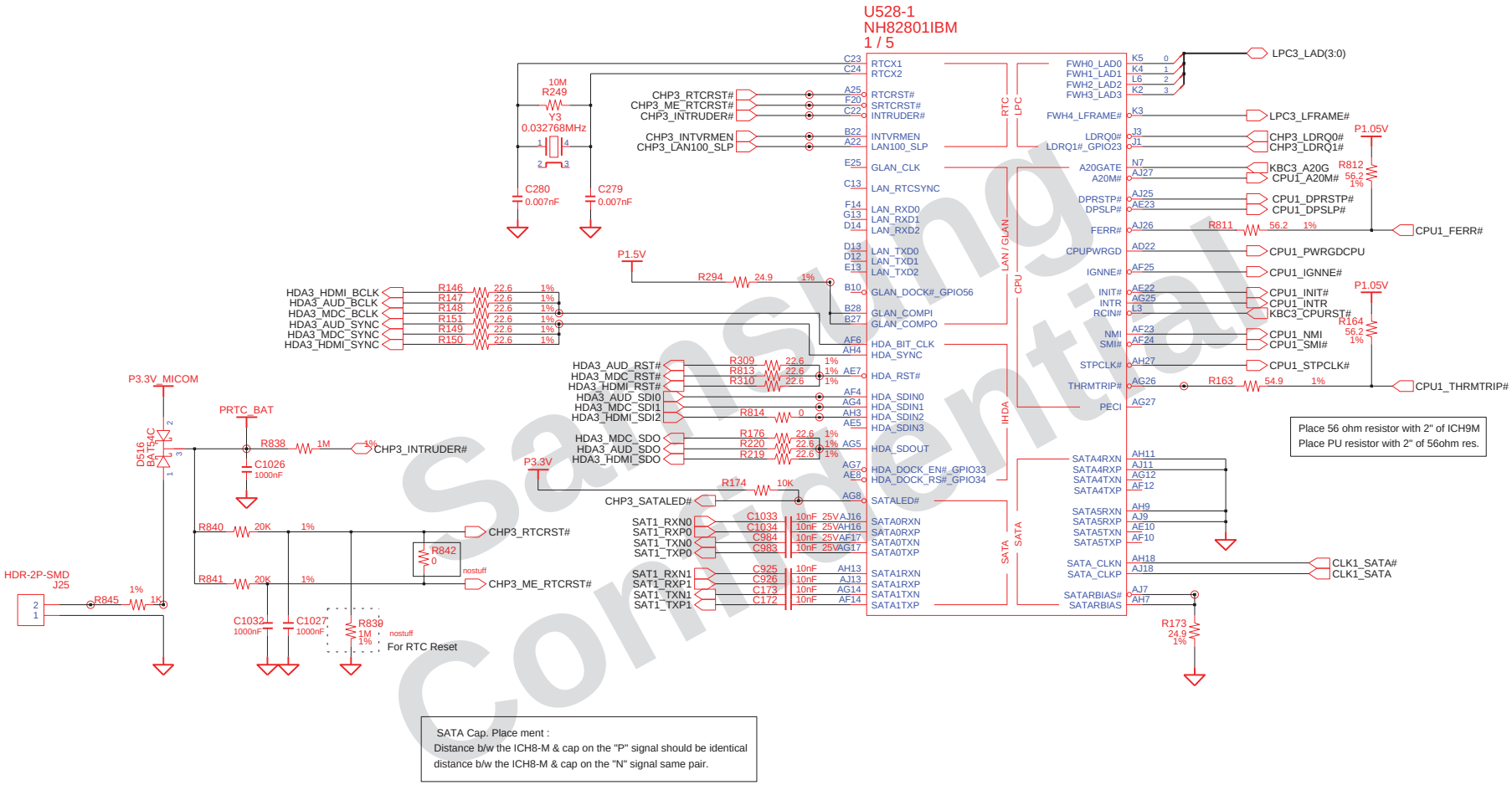

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CHECK: WU SHIJIANG,	DEV. STEP: PV		
APPROVAL: BYEONGCHANG LEE,	REV: 1.0		PART NO. BA41-####A
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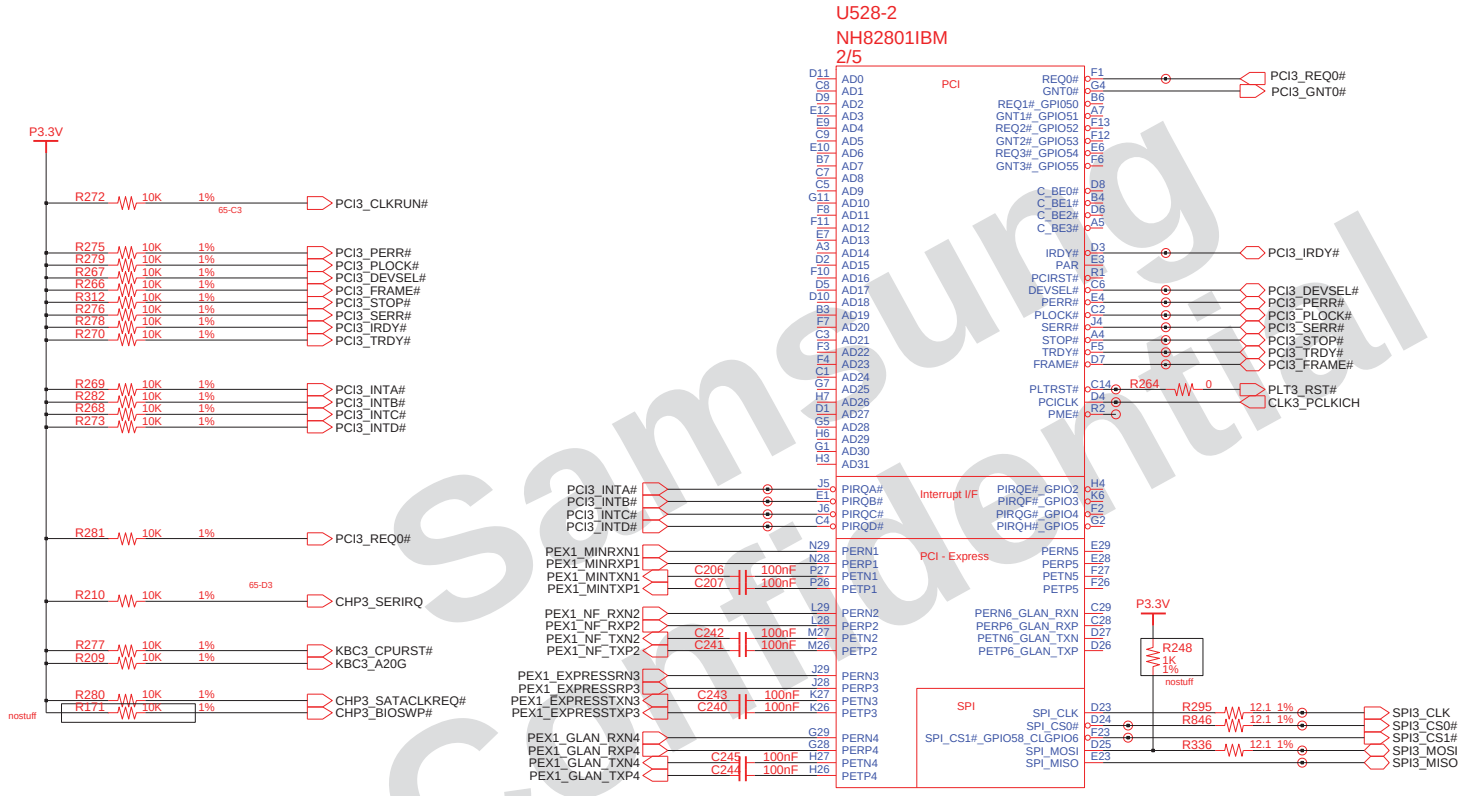

AC caps : PCIE need to be within 250mils of the driver
Resistor for Test : Place Stuffing Option to minimize stubs

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CHECK WU SHIJIANG,	DEV. STEP PV		
APPROVAL BYEONGCHANG LEE,	REV 1.0		PART NO. BA41-####A
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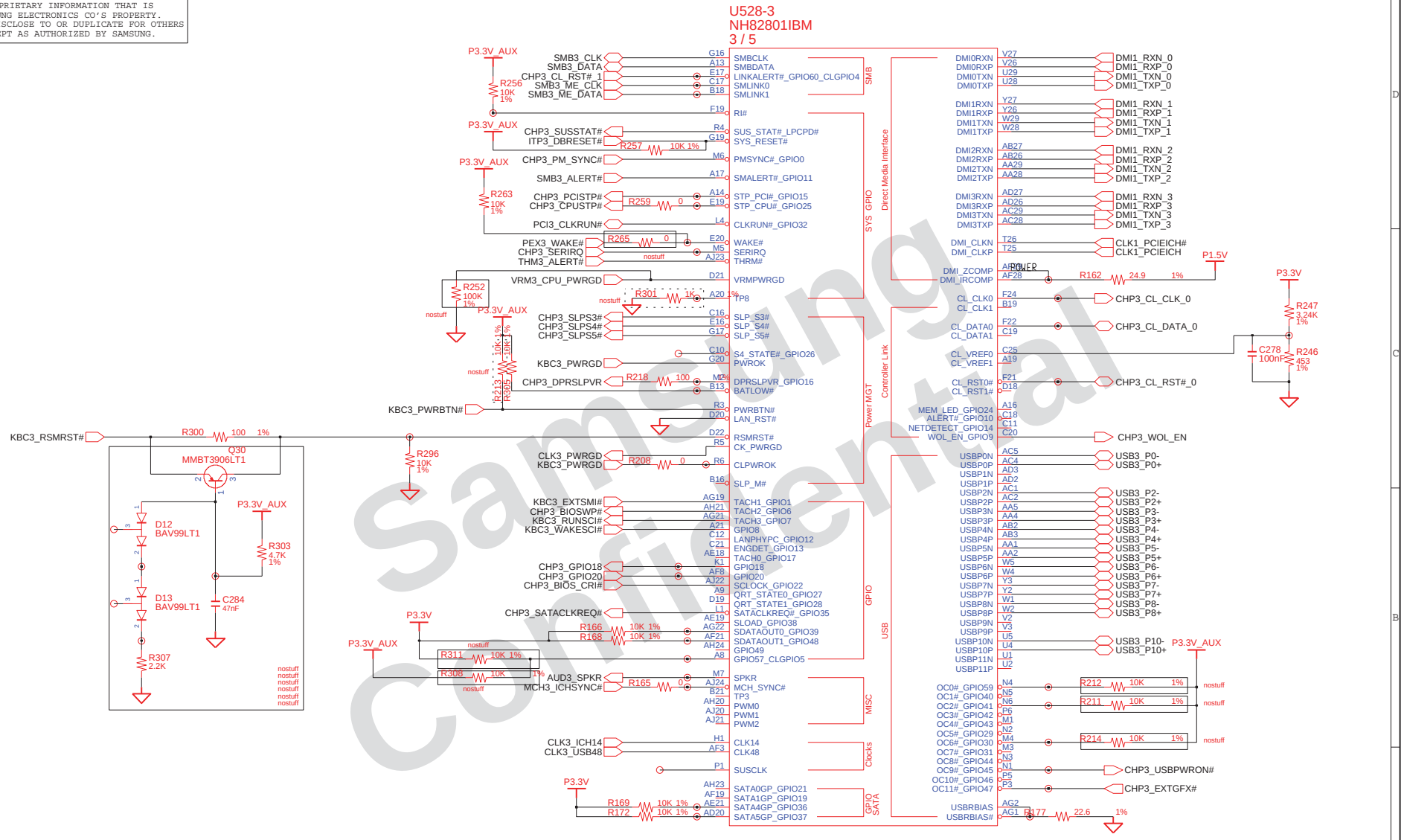

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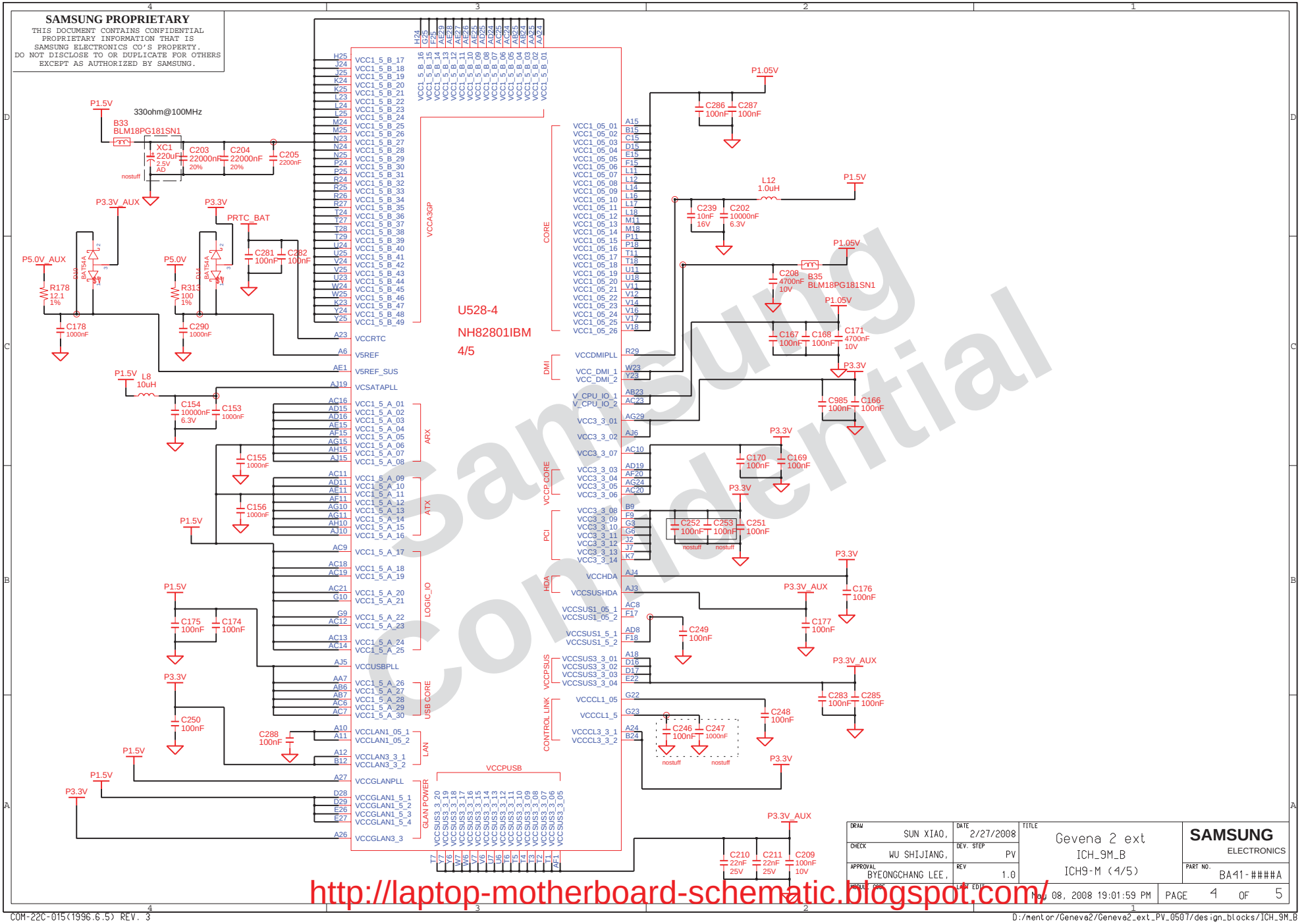

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CHECK	WU SHIJIANG,	DEV. STEP	PV			
APPROVAL	BYEONGCHANG LEE,	REV	1.0			PART NO. BA41-####A
PROJECT CODE		LAST EDIT	May 08, 2008 19:01:59 PM	PAGE	4 OF 5	

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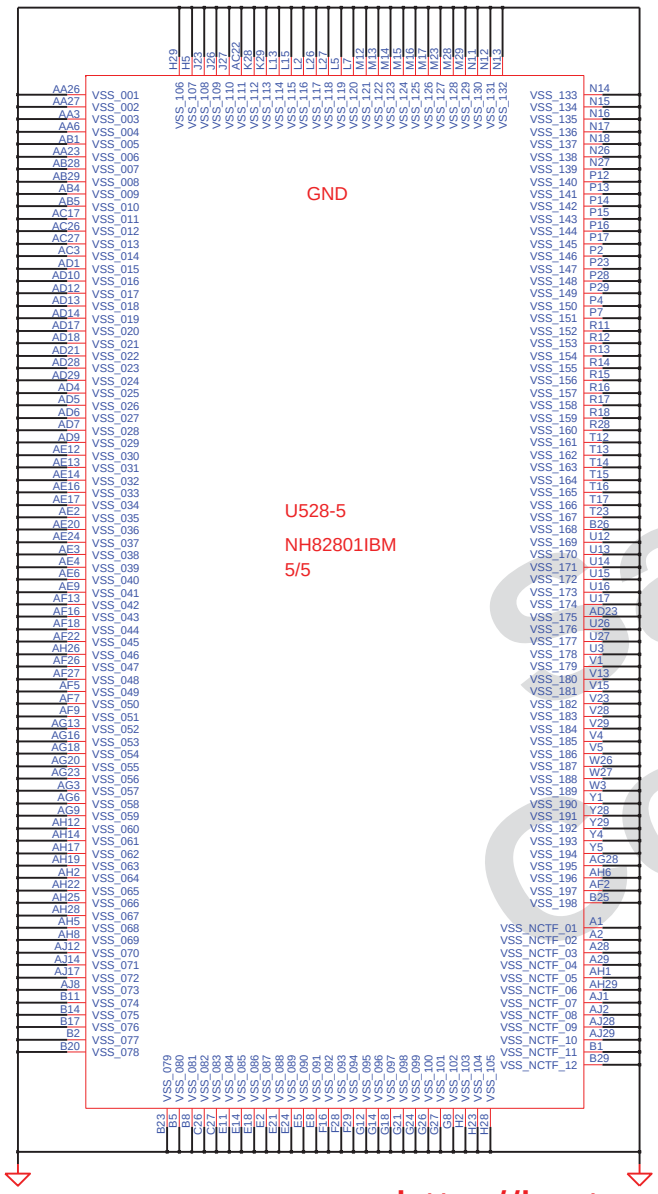
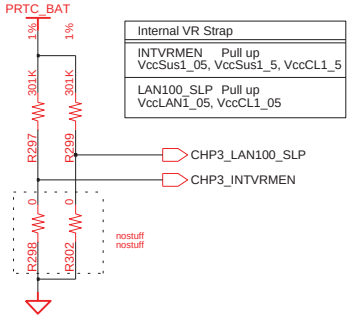
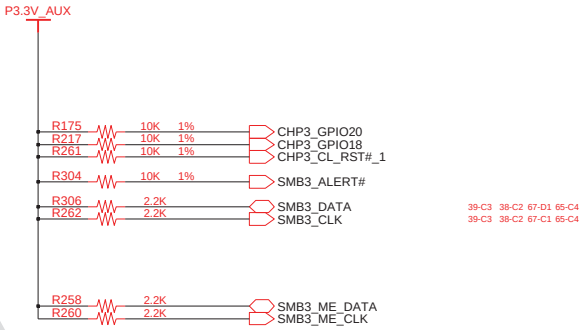
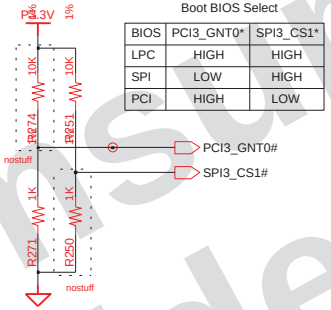




Internal VR Strap	
INTVRMEN	Pull up VccSus1_05, VccSus1_5, VccCL1_5
LAN100_SLP	Pull up VccLAN1_05, VccCL1_05

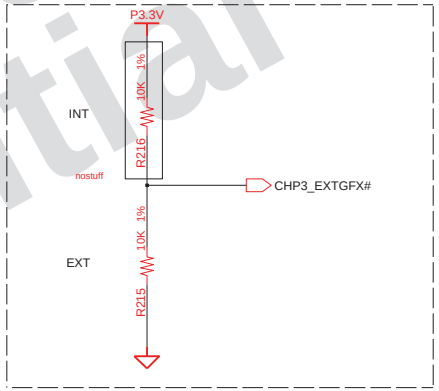


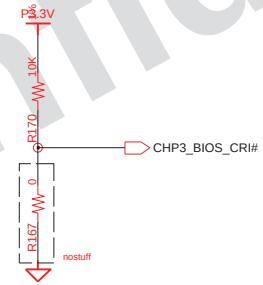


Boot BIOS Select

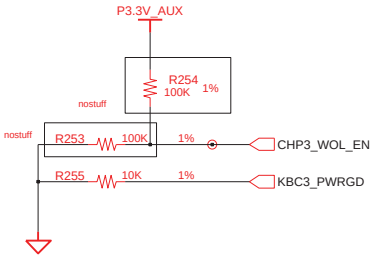
BIOS	PCI3_GNT0*	SPI3_CS1*
LPC	HIGH	HIGH
SPI	LOW	HIGH
PCI	HIGH	LOW

Model Dependent





BIOS CRISIS RECOVER STRAP
PLACE NEAR KEYBOARD



DRAW SUN XIAO,	DATE 2/27/2008	TITLE Gevena 2 ext ICH_9M_B ICH9-M (5/5)	SAMSUNG ELECTRONICS
CHECK WU SHIJIANG,	DEV. STEP PV		PART NO. BA41-####A
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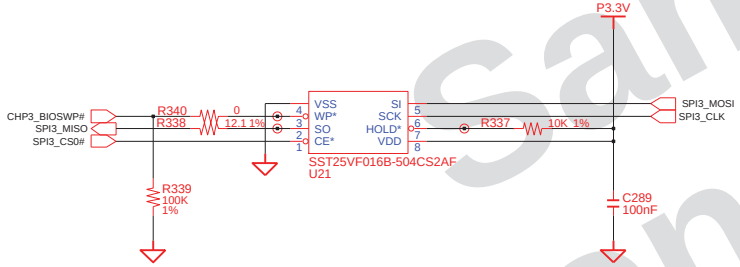
- SPI ROM LIST -

- Macronix - MX25L8005M2C-15G
- STM - M25PE80
- ATMEL - AT26DF081A-SU

SST - 25VF080B-50-4C-S2AF
WINBOND - W25X80-VSSI-G



02	VERIFY REAL MODE
03	DISABLE NMI
04	GET CPU TYPE
06	INIT. SYSTEM H/W
08	INIT. CHIPSET REG.
09	SET IN POST FLAG
0A	INIT CPU.REG
0B	CPU CACHE ON
0C	INIT.CACHE TO POST
OE	INIT. I/O VALUE
0F	ENABLE THE L-BUS IDE
10	INIT. POWER MANAGER
11	LOAD ALTERNATE REG.
13	PCI BUS MASTER RESET WITH INITIAL POST VALUE
14	INIT. KEYBOARD CONTROLLER
16	CHECK CHECKSUM
18	8254 TIMER INIT.
1A	8237 DMA CONTROLLER INIT.
1C	RESET INTERRUP CONTROLLER
20	TEST DRAM REFRESH
22	TEST 8742 KEYBOARD CONTROLLER
24	SET ES SEGMENT REG. TO 4GB
26	ENABLE A20
28	AUTO SIZING DRAM
32	COMPUTE THE CPU SPEED
34	TESET CMOS RAM
38	SHADOW SYSTEM BIOS ROM
3A	AUTO SIZING CACHE
3C	CONFIGURE ADVANCED CHIPSET REG.
3D	LOAD ALTER REG. WITH CMOS VALUE
42	INIT. INTERRUPT VECTOR
44	INIT. BIOS INTERRUPT
46	CHECK ROM COPYRIGHT NOTICE
47	INIT. I20 SUPPORT IF INSTALLED
48	CHECK VIDEO CONFIGURE AGAINST CMOS
49	INIT. PCI BUS AND DEVICE
4A	INIT. ALL VIDEO BIOS ROM
4C	SHADOW VIDEO BIOS ROM
50	DISPLAY CPU TYPE AND SPEED
52	TEST KEYBOARD
54	SET KEYCLICK IF ENABLED
56	ENABLE KEYBOARD
58	TEST FOR UNEXPECTED INTERRUPTS
5A	DISPLAY " PRESS ..... SETUP"
5C	TEST RAM GETWEEN 512K AND 640K
60	TEST EXTENDED MEMORY
62	TEST EXTENDED MEMORY ADDRESS LINE
64	JUMP TO USER PATCH 1
66	CONFIGURE ADVANCE CACHE REG.
6A	DISPLAY EXTERNAL CACHE SIZE
6C	DISPLAY SHADOW MESSAGE
6E	DISPLAY NON-DISPOSABLE SEGMENT
70	DISPLAY ERROR MESSAGE
72	CHECK FOR CONFIGURATION ERROR
74	TEST REAL-TIME CLOCK
76	CHECK FOR KEYBOARD EERROR
7C	SETUP HARDWARE INTERRUPT VECTOR
7E	TEST COPROCESSER IF PRESENT
80	DISABLE ON-BOARD I/O PORT
82	DETECT AND INSTALL EXT.RS232C
84	DETECT AND INSTALL EXT.PARALLEL
86	RE-INIT. ON-BOARD I/O PORT
88	INIT. BIOS DATA ROM
8A	INIT.EXTENDED BIOS DATA AREA
8C	INIT. FDD CONTROLLER
9A	SHADOW OPTION ROMS
9C	SETUP POWER MANAGEMENT
9E	ENABLE H/W INTERRUPT
A0	SET TIME OF DAY
A4	INIT. TYPEMATIC RATE
A8	ERASE F2 PROMPT
AA	SCAN FOR F2 KEY STROKE
AC	ENTER SETUP
AE	CLEAR IN POST FLAG
B0	CHECK FOR ERRORS
B2	POST DONE-PREPARE TO BOOT O/S
B4	ONE BEEP
B6	CHECK PASSWORD (OPTION)
B7	ACPI INIT
BA	DMI INIT
BE	CLEAR SCREEN
C0	TRY BOOT WITH INT19
D0	INTERRUPT HANDLER ERROR
D2	UNKNOWN INTERRUPT ERROR
D4	PENDING INTERRUPT ERROR
D6	SHUTDOWN 5
D8	SHUTDOWN ERROR
DA	EXTENDED BLOCK MOVE
DC	SHUTDOWN 10
89	ENABLE NMI
90	INIT. HDD CONTROLLER
91	INIT. LOCAL BUS HDD CONTROLLER
92	JUMP TO USER PATCH 2
94	DISABLE A20 ADDRESS LINE
96	CLEAR HUGE ES SEGMENT REG.
98	SEARCH FOR OPTION ROMS

DRAW SUN XIAO,	DATE 2/27/2008	TITLE Gevena 2 ext SPI_BIOS_ROM SPI_BIOS_ROM	SAMSUNG ELECTRONICS
CHECK WU SHIJIANG,	DEV. STEP PV		PART NO. BA41-####A
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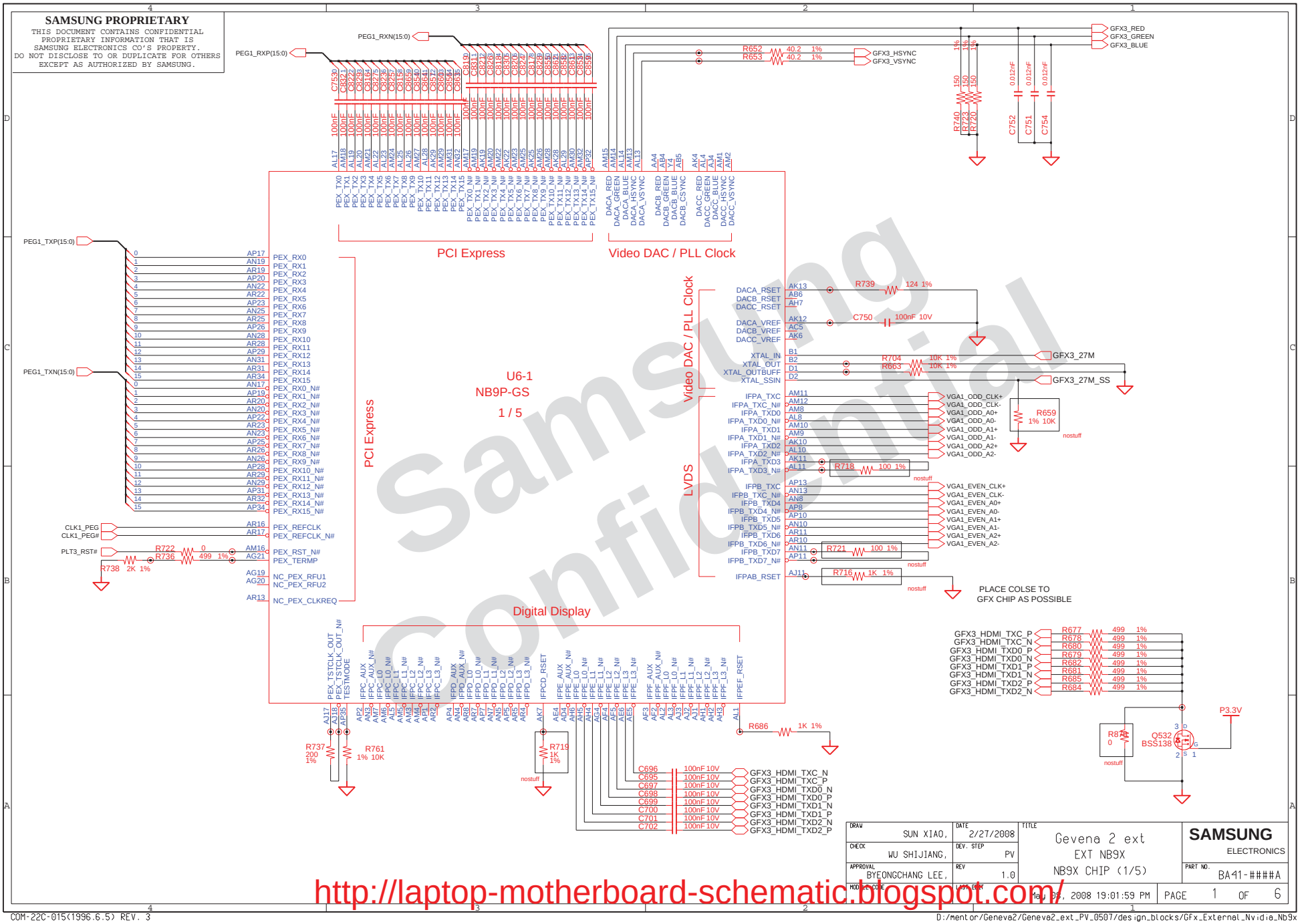

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CHECK: WU SHIJIANG,	DEV. STEP: PV		
APPROVAL: BYEONGCHANG LEE,	REV: 1.0		PART NO. BA41-####A
MODEL CODE	LAST EDIT: Mar. 03, 2008 19:01:59 PM		PAGE 1 OF 6

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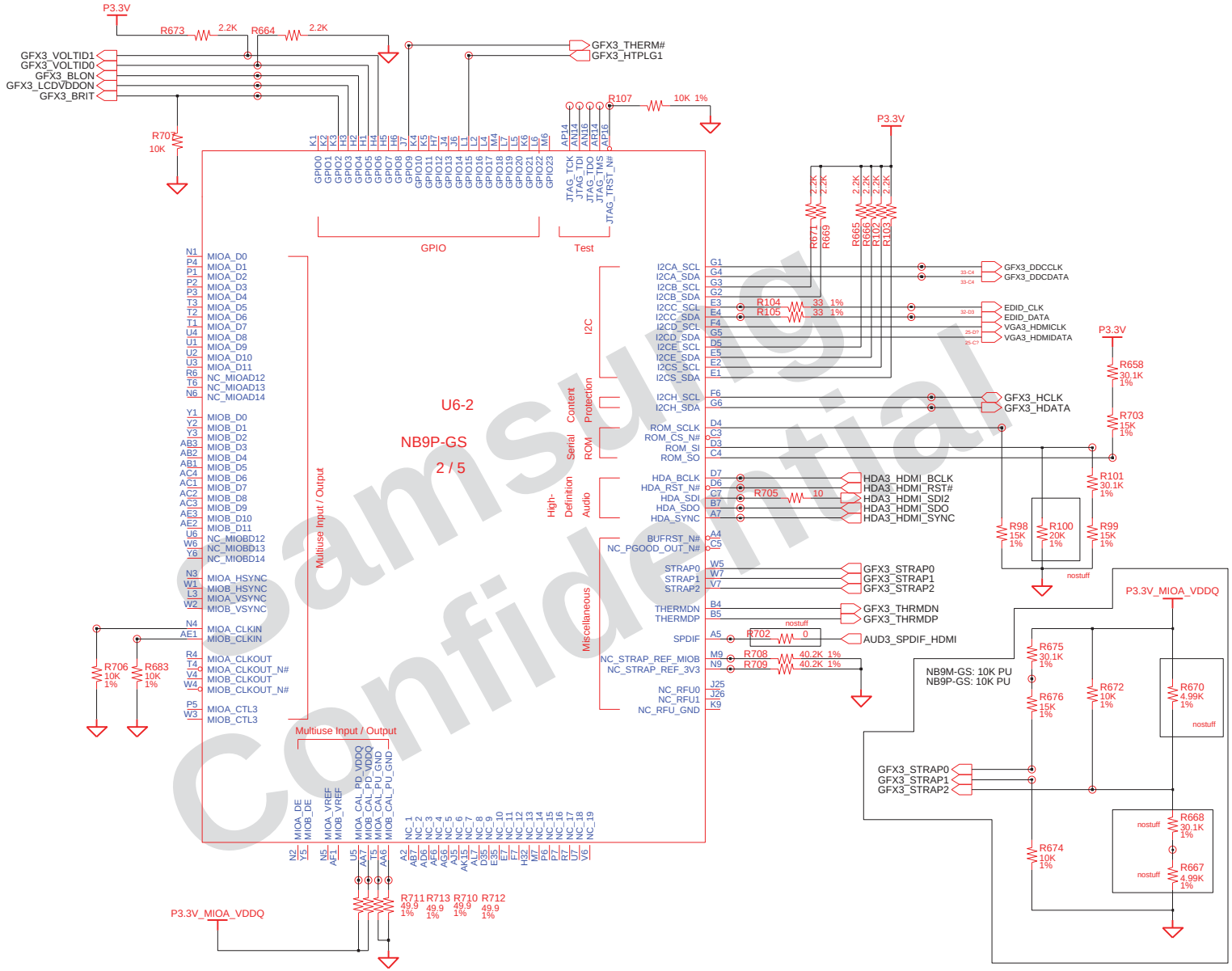

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CHECK: WU SHIJIANG,	DEV. STEP: PV		
APPROVAL: BYEONGCHANG LEE,	REV: 1.0		PART NO. BA41-####A
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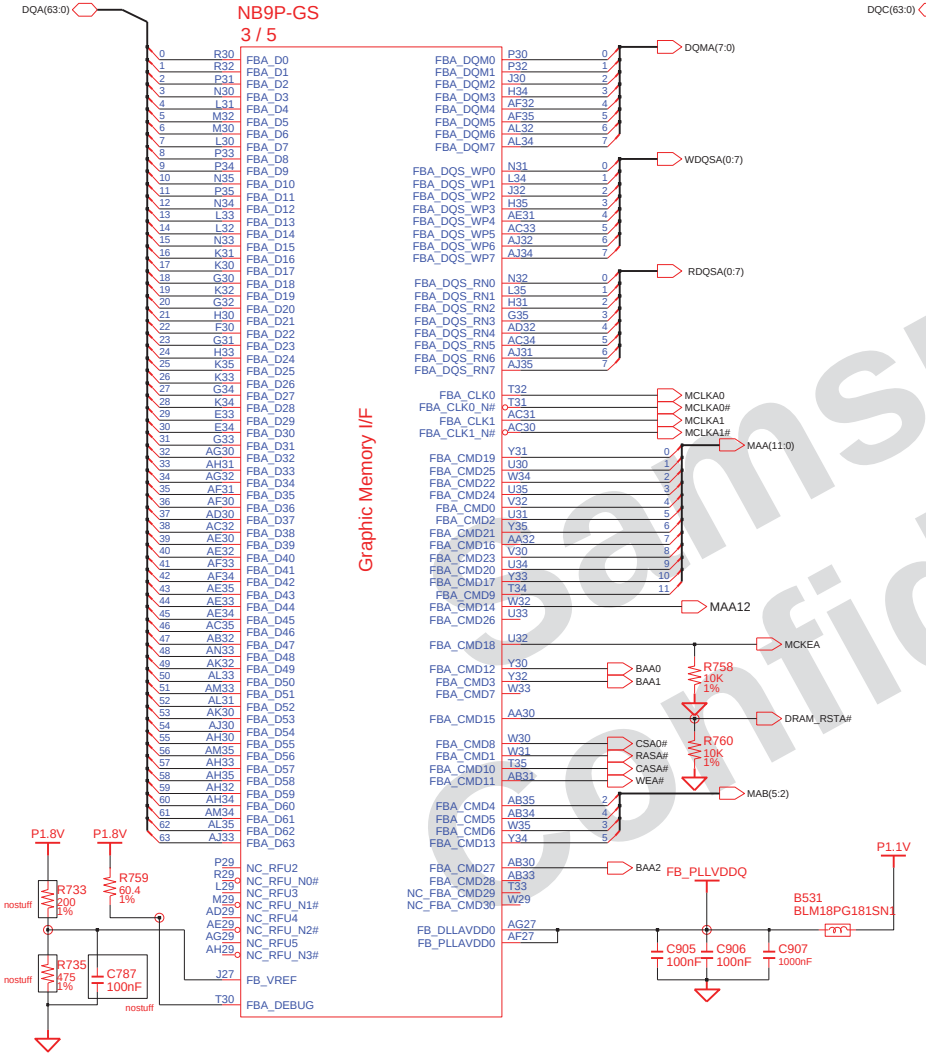
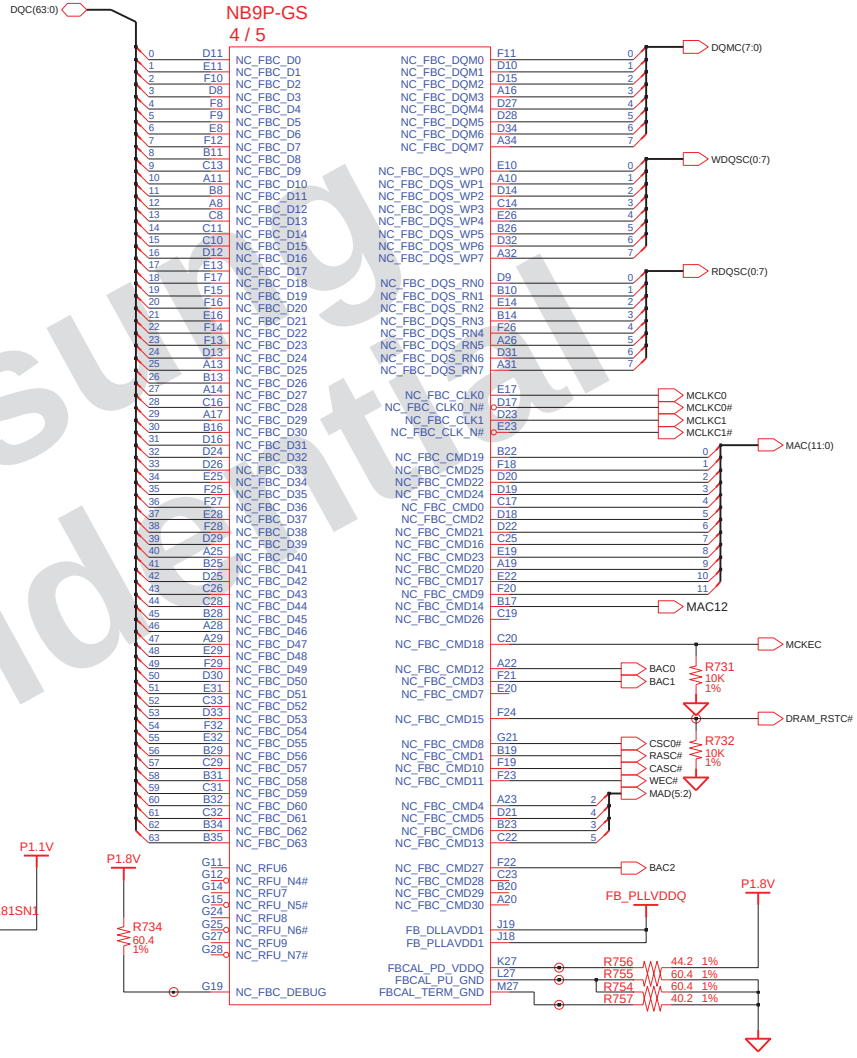
Graphic Memory I/F (Using FBA Channel)

U6-3
NB9P-GS
3 / 5



Graphic Memory I/F (Using FBC Channel)

U6-4
NB9P-GS
4 / 5



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CHECK: WU SHIJIANG,	DEV. STEP: PV		
APPROVAL: BYEONGCHANG LEE,	REV: 1.0		PART NO.: BA41-####A
MODULE CODE:	LAST EDIT: May 08, 2008 19:01:59 PM		PAGE 3 OF 6

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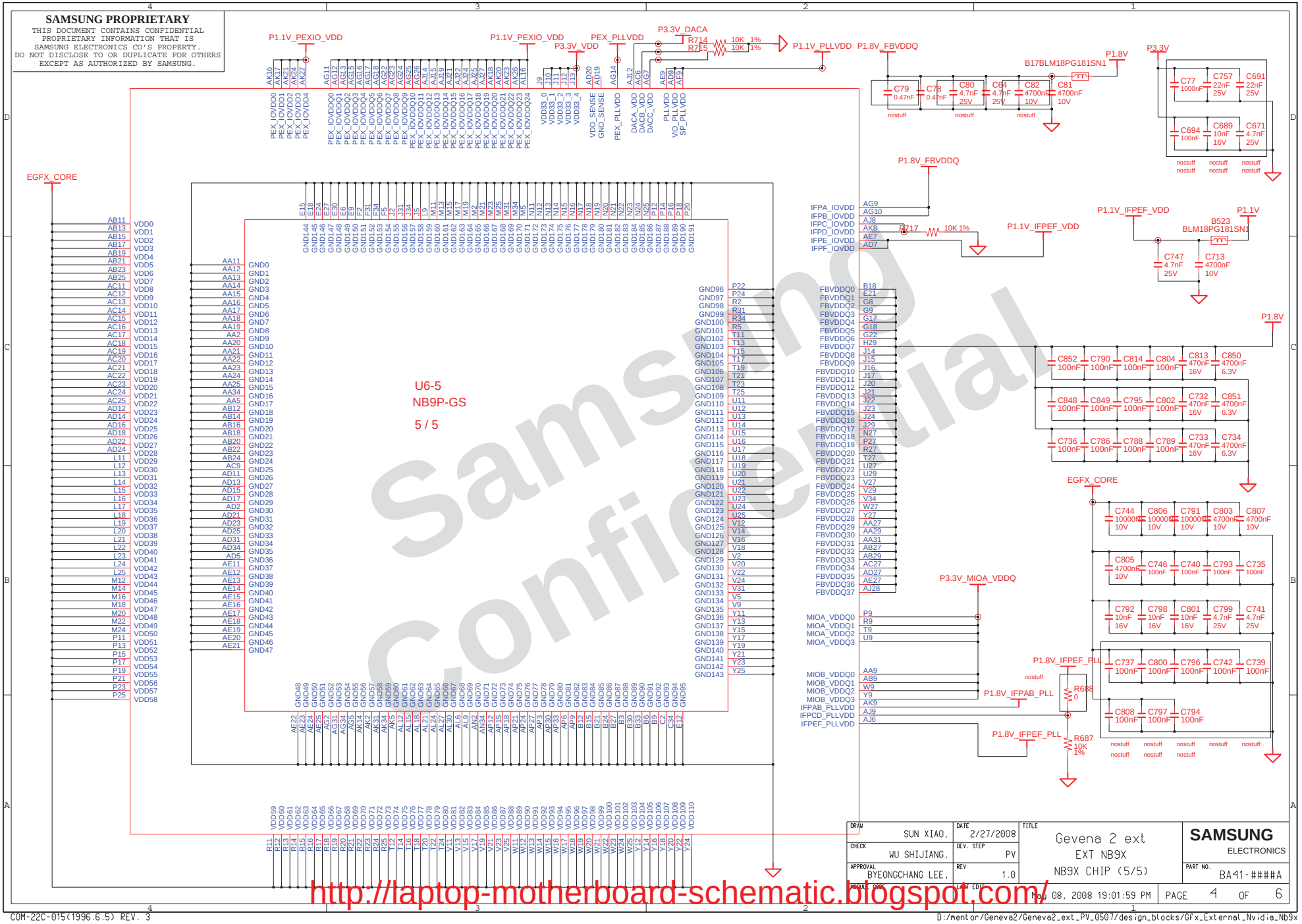

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CHECK: WU SHIJIANG,	DEV. STEP: PV		PART NO. BA41-####A
APPROVAL: BYEONGCHANG LEE,	REV: 1.0		
MODULE CODE:	LAST EDIT: May 08, 2008 19:01:59 PM		PAGE 4 OF 6

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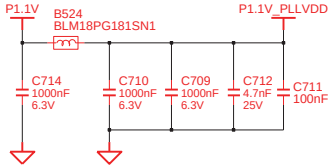
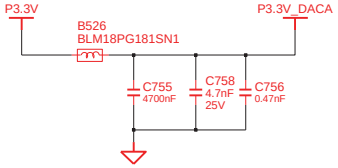
PLL_VDD



DACA/B/C



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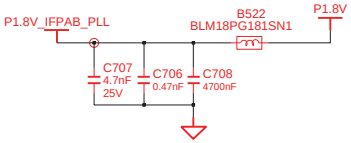

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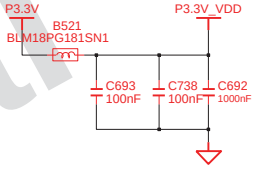

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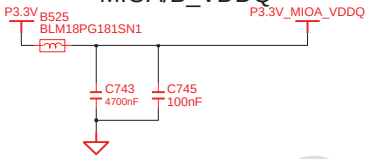

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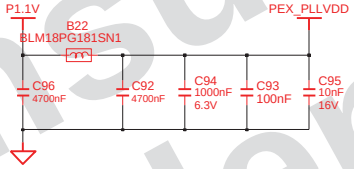

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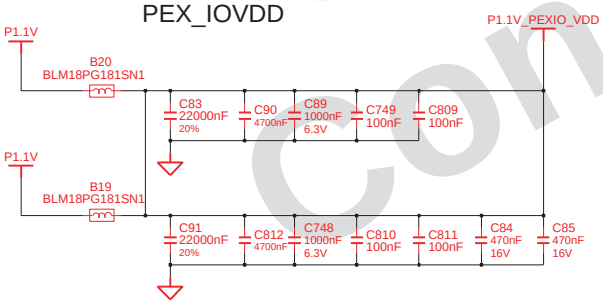

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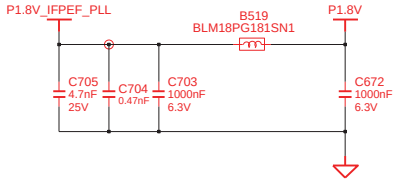

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CHECK WU SHIJIANG,	DEV. STEP PV		PART NO. BA41-####A
APPROVAL BYEONGCHANG LEE,	REV 1.0		
MODULE CODE	LAST EDIT May 08, 2008 19:01:59 PM		PAGE 5 OF 6

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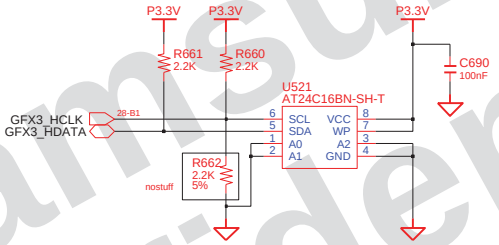
HDCP



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CHECK WU SHIJIANG,	DEV. STEP PV		
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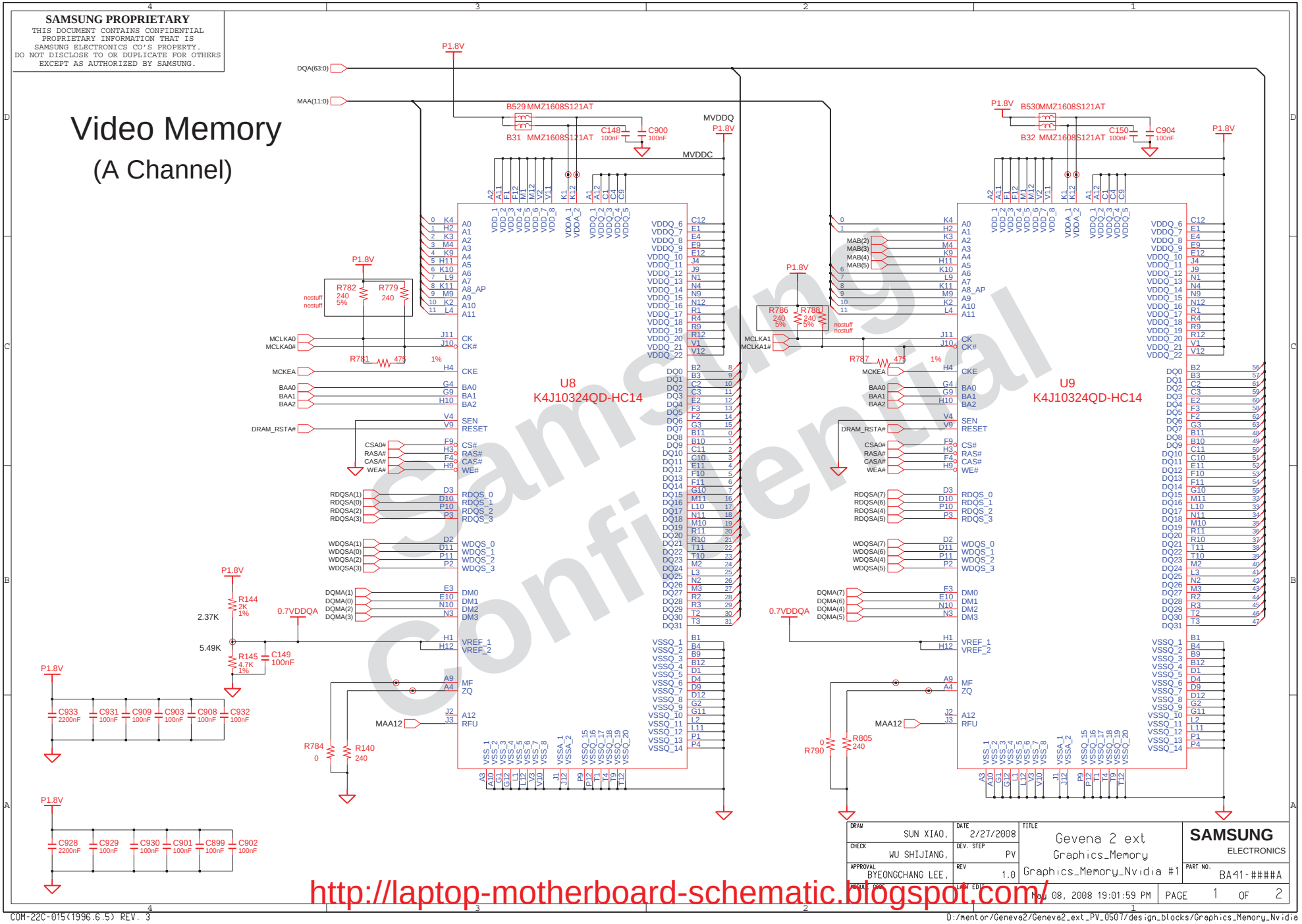
Video Memory

(A Channel)



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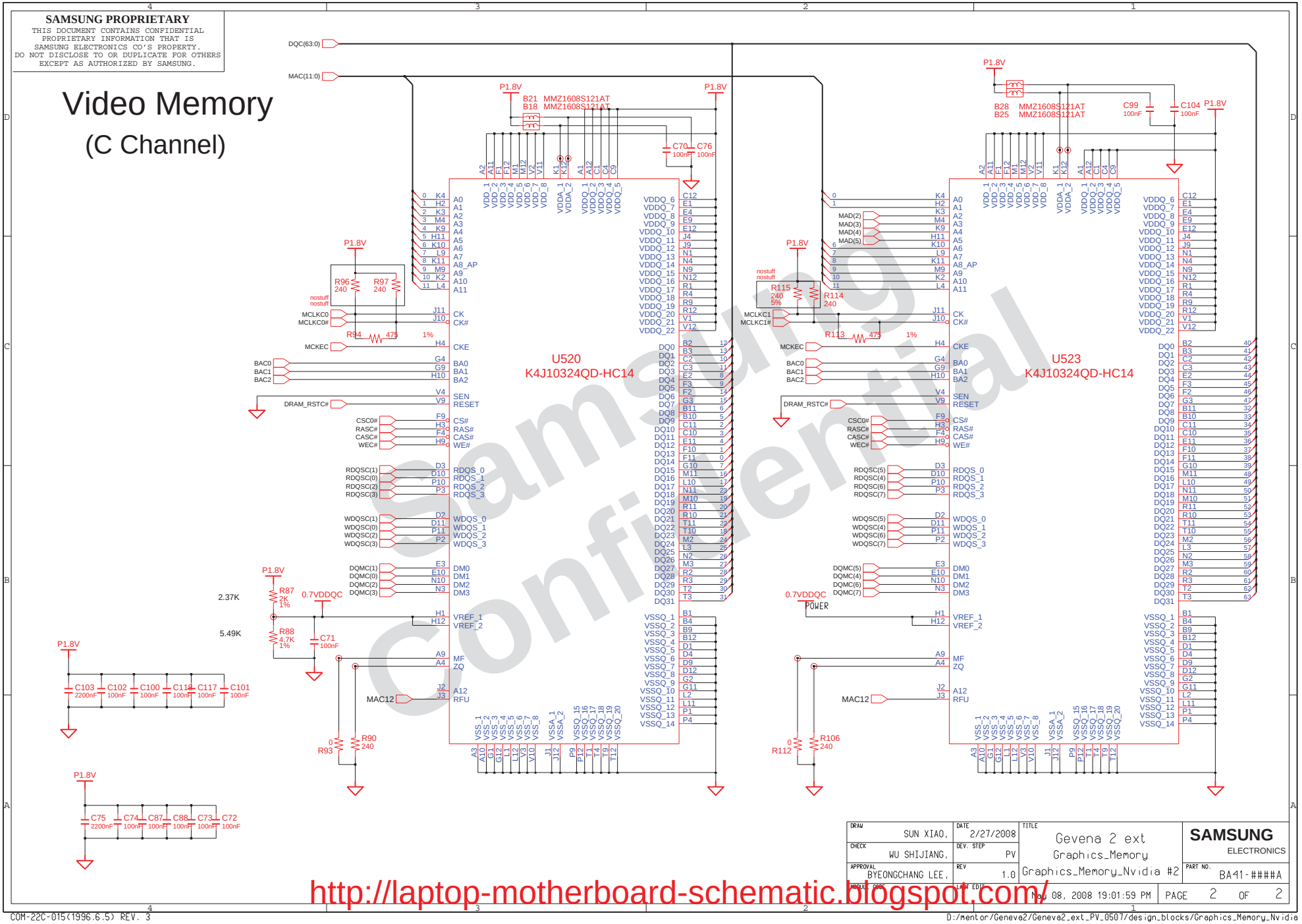
Video Memory

(C Channel)



DRAW SUN XIAO,	DATE 2/27/2008	TITLE Gevena 2 ext Graphics_Memory Graphics_Memory_Nvidia #2	SAMSUNG ELECTRONICS
CHECK WU SHIJIANG,	DEV. STEP PV		
APPROVAL BYEONGCHANG LEE,	REV 1.0		PART NO. BA41-####A
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DRAW SUN XIAO,	DATE 2/27/2008	TITLE Gevena 2 ext Graphics_Memory Graphics_Memory_Nvidia #3	SAMSUNG ELECTRONICS
CHECK WU SHIJIANG,	DEV. STEP PV		
APPROVAL BYEONGCHANG LEE,	REV 1.0		PART NO. BA41-####A
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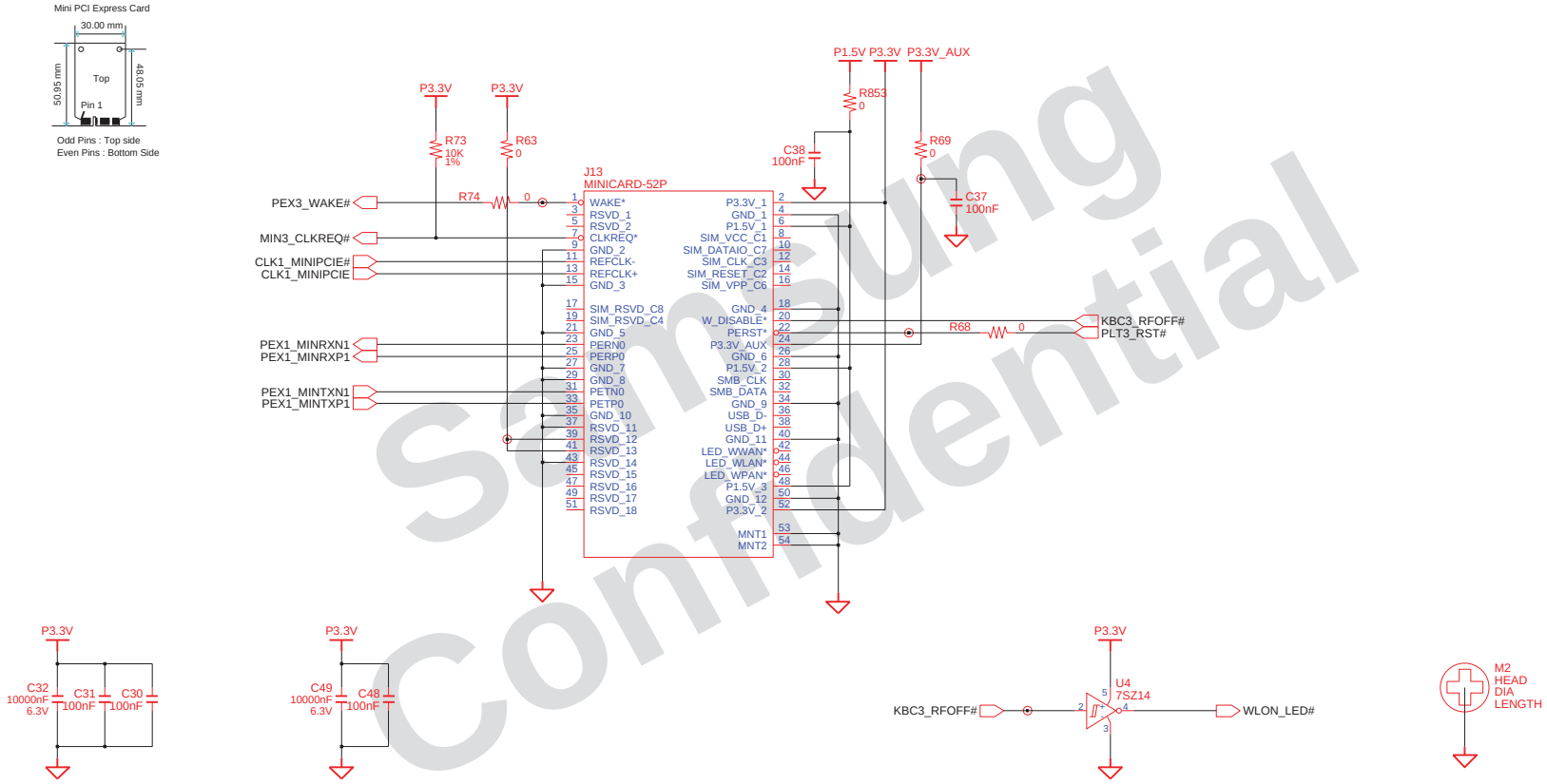
Mini Card



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CHECK: WU SHIJIANG,	DEV. STEP: PV		
APPROVAL: BYEONGCHANG LEE,	REV: 1.0		PART NO. BA41-####A
MODULE CODE: Unspecified	LAST EDIT: May 08, 2008 19:01:59 PM		PAGE 1 OF 1

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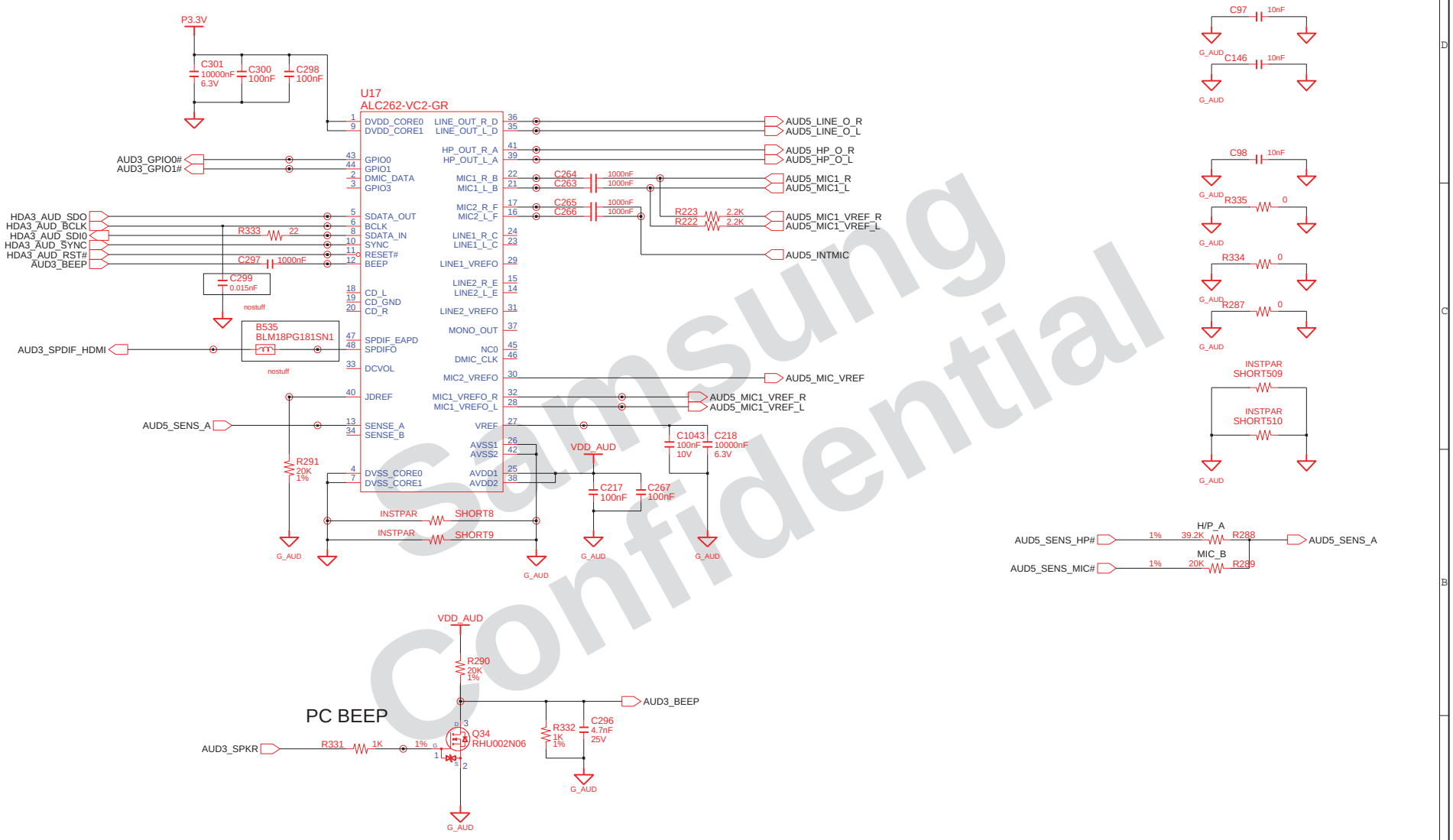

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CHECK WU SHIJIANG,	DEV. STEP PV		
APPROVAL BYEONGCHANG LEE,	REV 1.0		PART NO. BA41-####A
MODULE CODE Undefined	LAST EDIT May 08, 2008 19:01:59 PM		PAGE 1 OF 5

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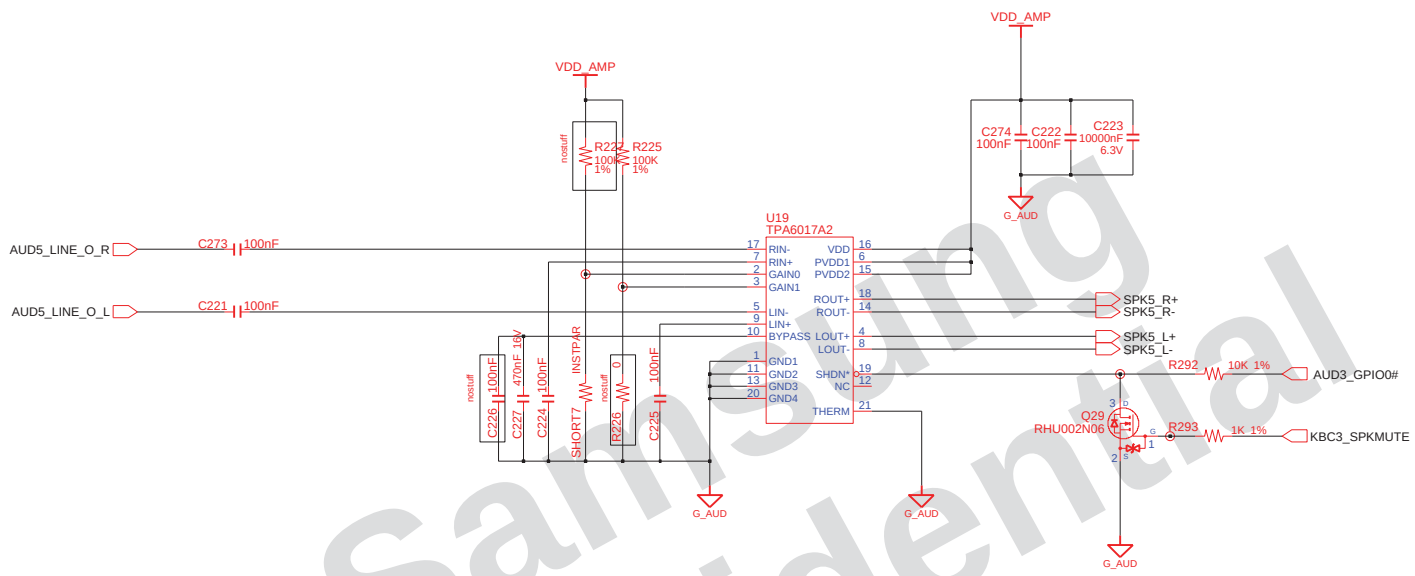
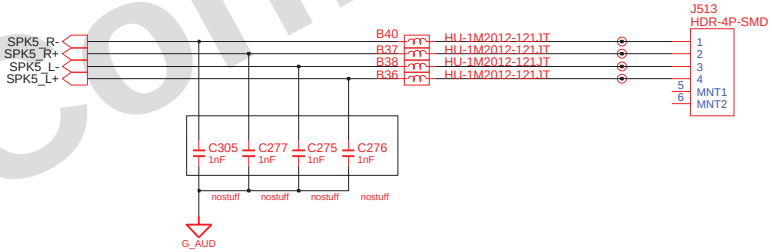


INTERNAL STEREO SPEAKERS



DRAW SUN XIAO,	DATE 2/27/2008	TITLE Gevena 2 ext HDA_Codec_Alc262 HDA_Codec_Alc262 #2	SAMSUNG ELECTRONICS
CHECK WU SHIJIANG,	DEV. STEP PV		
APPROVAL BYEONGCHANG LEE,	REV 1.0		PART NO. BA41-####A
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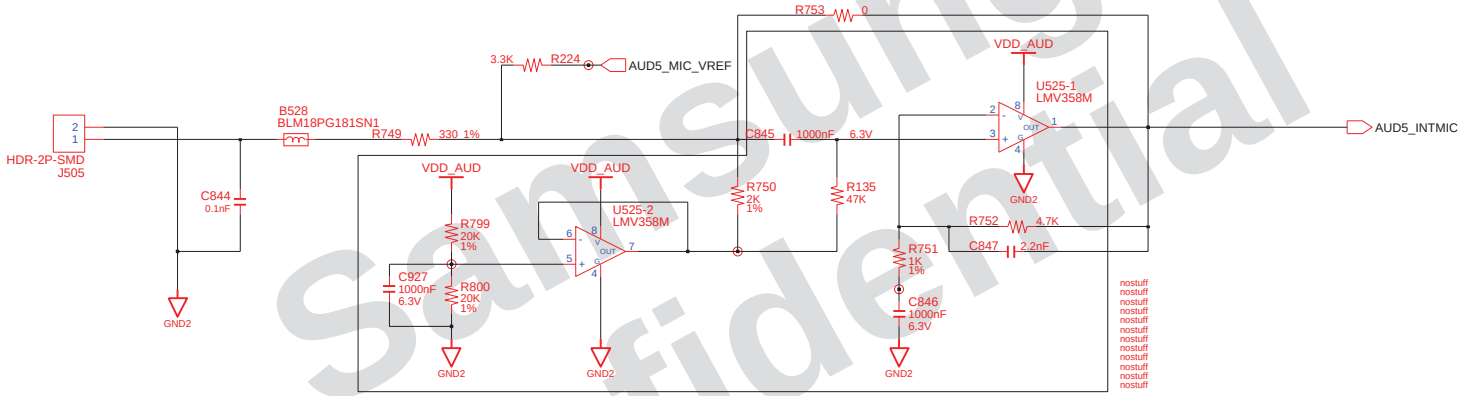
Internal MIC



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DRAW SUN XIAO,	DATE 2/27/2008	TITLE Gevena 2 ext HDA_Codec_Alc262 HDA_Codec_Alc262 #3	SAMSUNG ELECTRONICS
CHECK WU SHIJIANG,	DEV. STEP PV		
APPROVAL BYEONGCHANG LEE,	REV 1.0		PART NO. BA41-####A
MODULE CODE Undefined	LAST EDIT May 08, 2008 19:01:59 PM		PAGE 3 OF 5

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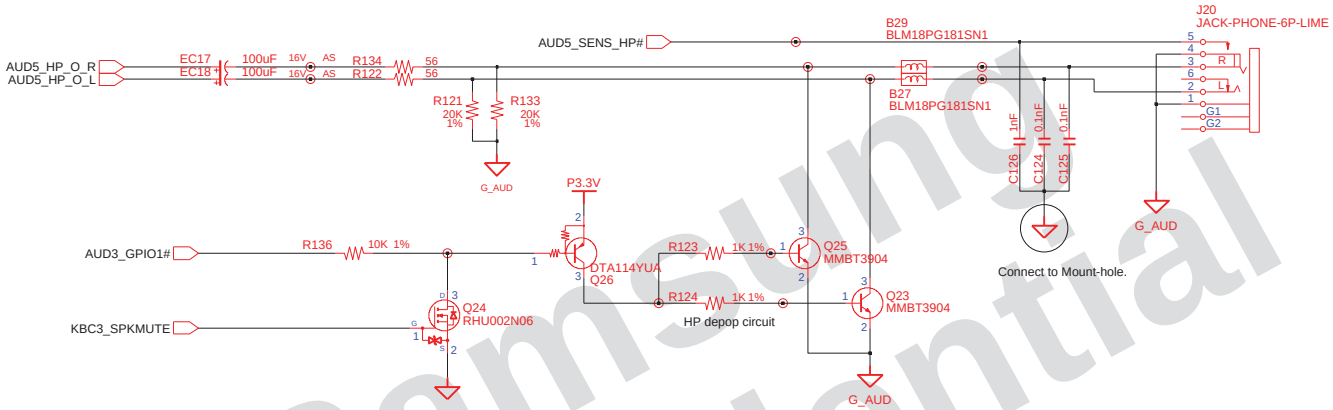
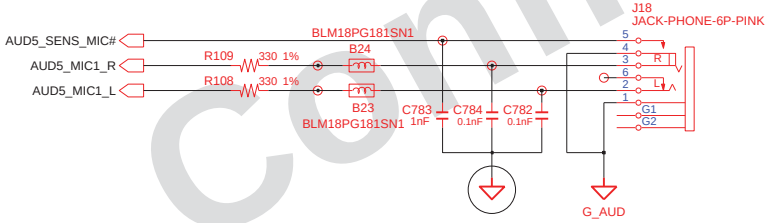
HEADPHONE



MIC JACK



The traces led to Audio Jacks have the width over 10mil

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DRAW SUN XIAO,	DATE 2/27/2008	TITLE Gevena 2 ext HDA_Codec_Alc262 HDA_Codec_Alc262 #4	SAMSUNG ELECTRONICS
CHECK WU SHIJIANG,	DEV. STEP PV		
APPROVAL BYEONGCHANG LEE,	REV 1.0		PART NO. BA41-####A
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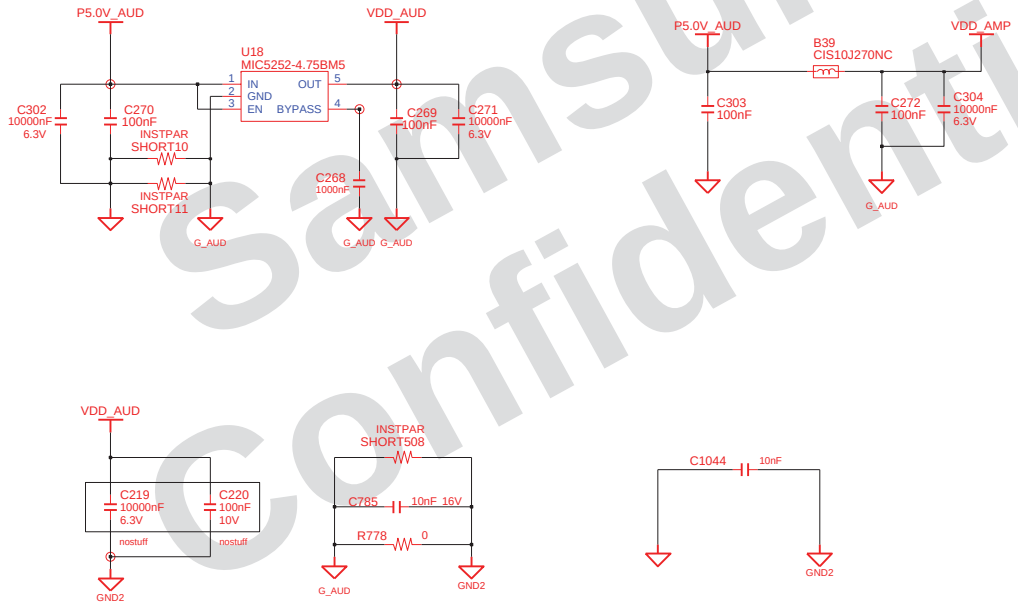
AUDIO POWER



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CHECK WU SHIJIANG,	DEV. STEP PV		
APPROVAL BYEONGCHANG LEE,	REV 1.0		PART NO. BA41-####A
MODULE CODE Unspecified	LAST EDIT May 08, 2008 19:01:59 PM		PAGE 5 OF 5

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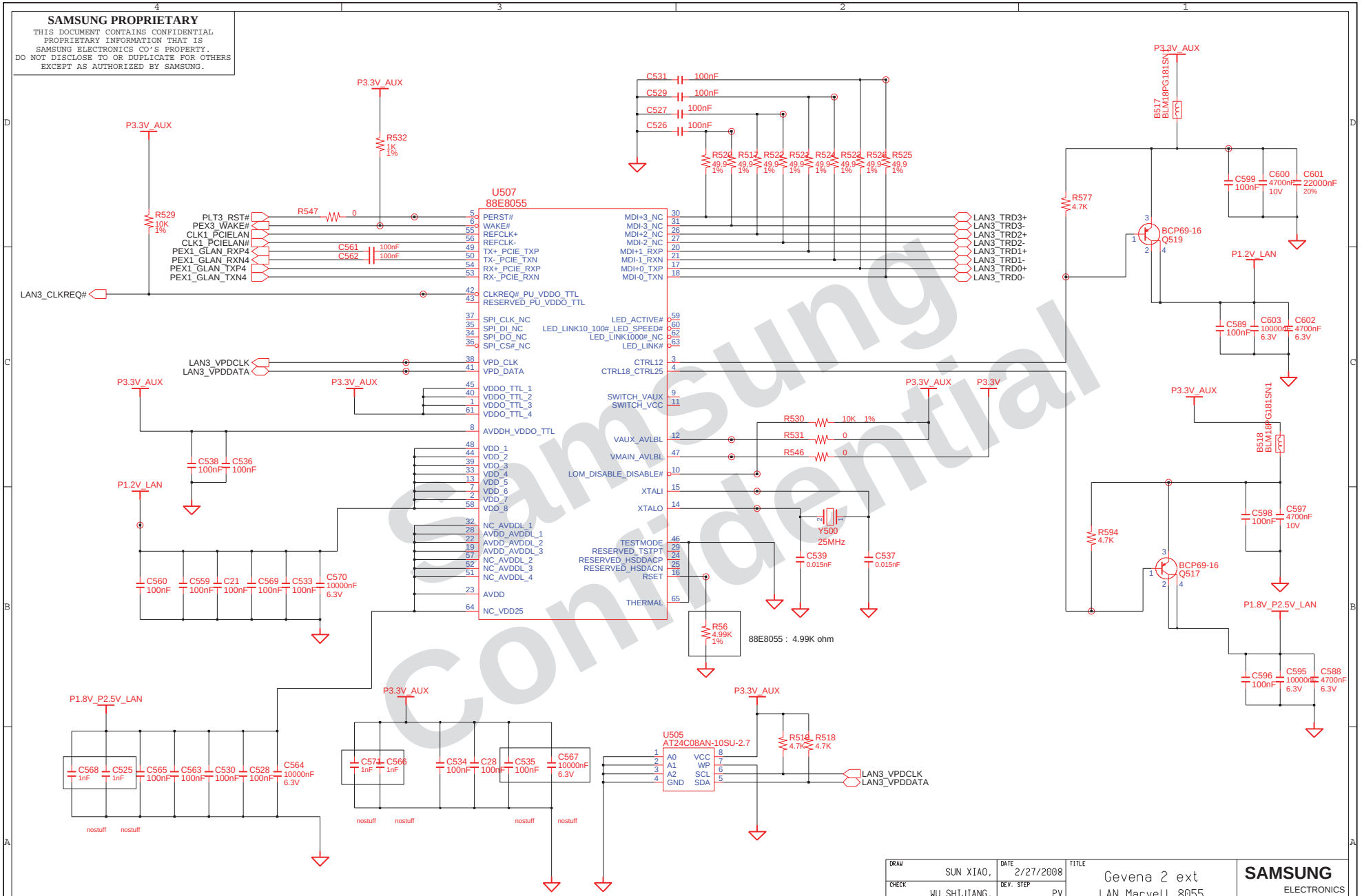

DRAW SUN XIAO,	DATE 2/27/2008	TITLE Gevena 2 ext	SAMSUNG ELECTRONICS
CHECK WU SHIJIANG,	DEV. STEP PV	LAN_Marvell_8055	
APPROVAL BYEONGCHANG LEE,	REV 1.0	LAN_Marvell_8055	PART NO. BA41-####A
MODULE CODE	LAST EDIT May 08, 2008 19:01:59 PM		PAGE 1 OF 2

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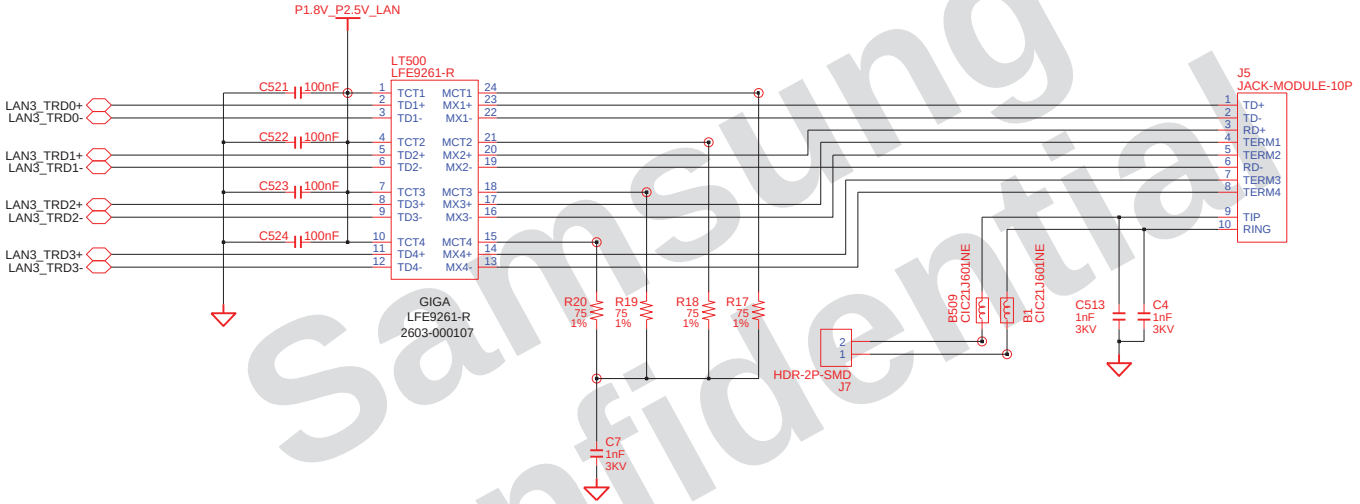
The ditance between LAN controller
and transformer is designed to extend less than two inches.



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CHECK WU SHIJIANG,	DEV. STEP PV	LAN_Marvell_8055	
APPROVAL BYEONGCHANG LEE,	REV 1.0	LAN_Marvell_8055	PART NO. BA41-####A
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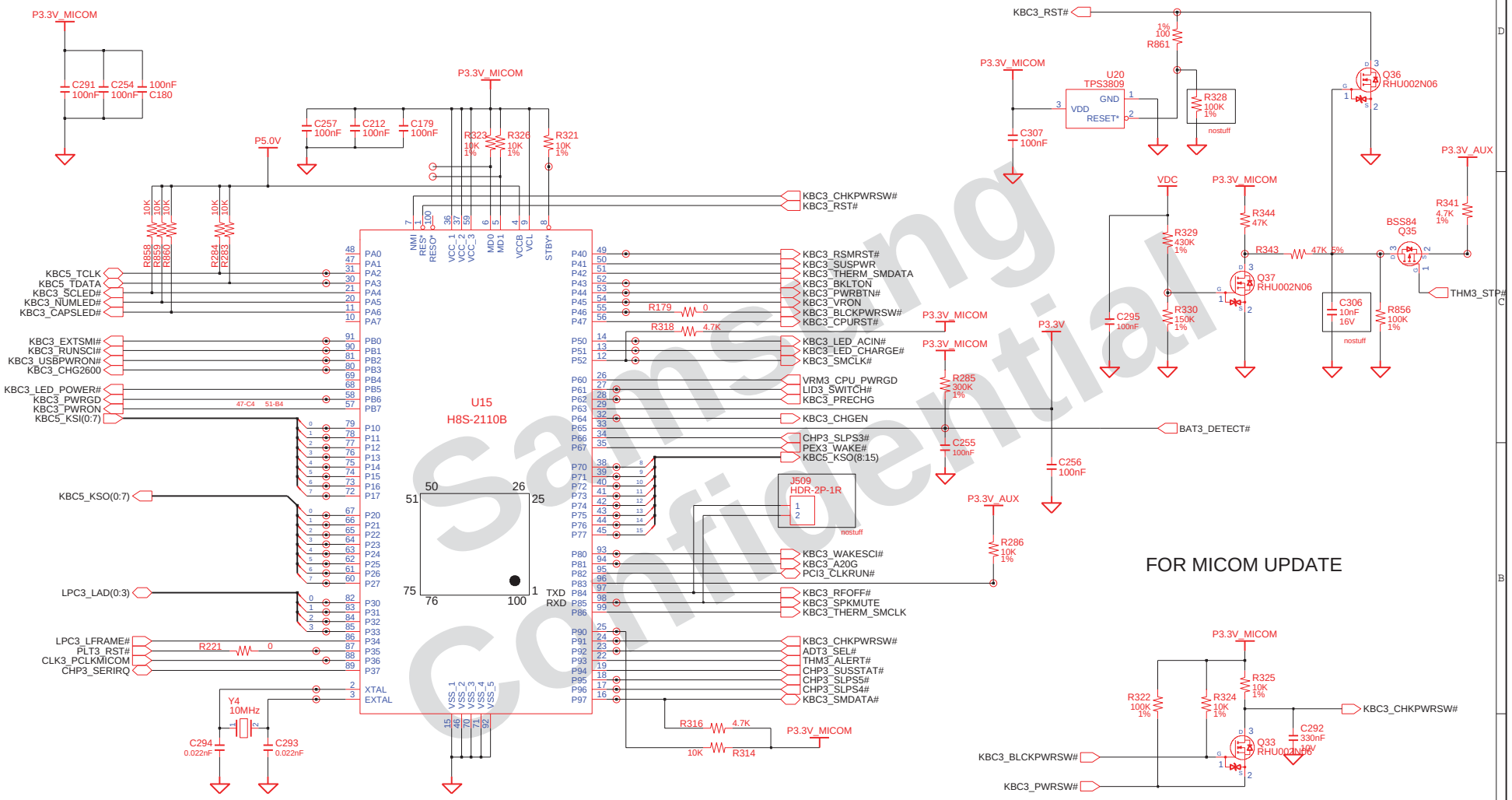
MICOM RESET



FOR MICOM UPDATE

POWER SWITCH BLOCK WHILE MICOM UPDATE

DRAW SUN XIAO,	DATE 2/27/2008	TITLE Gevena 2 ext	SAMSUNG ELECTRONICS
CHECK WU SHIJIANG,	DEV. STEP PV	MICOM_Renesas2110_100p	
APPROVAL BYEONGCHANG LEE,	REV 1.0	MICOM_Renesas2110_100p	PART NO. BA41-####A
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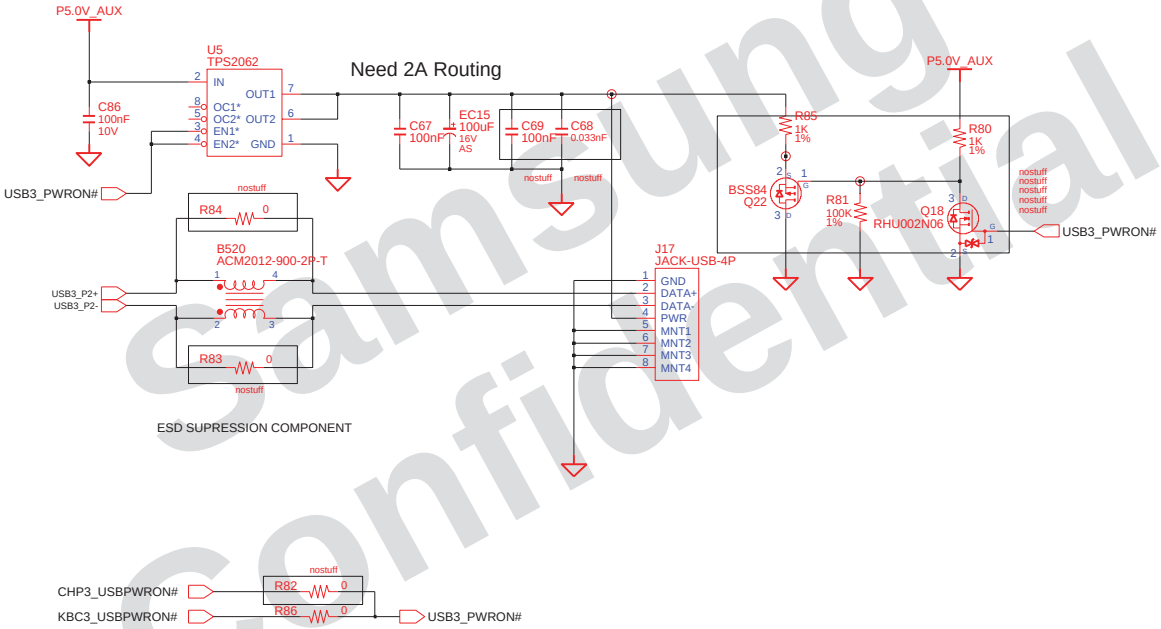
1 PORT USB CONNECTOR



DRAW SUN XIAO,	DATE 2/27/2008	TITLE Gevena 2 ext USB_1Port USB_1Port	SAMSUNG ELECTRONICS
CHECK WU SHIJIANG,	DEV. STEP PV		PART NO. BA41-####A
APPROVAL BYEONGCHANG LEE,	REV 1.0		
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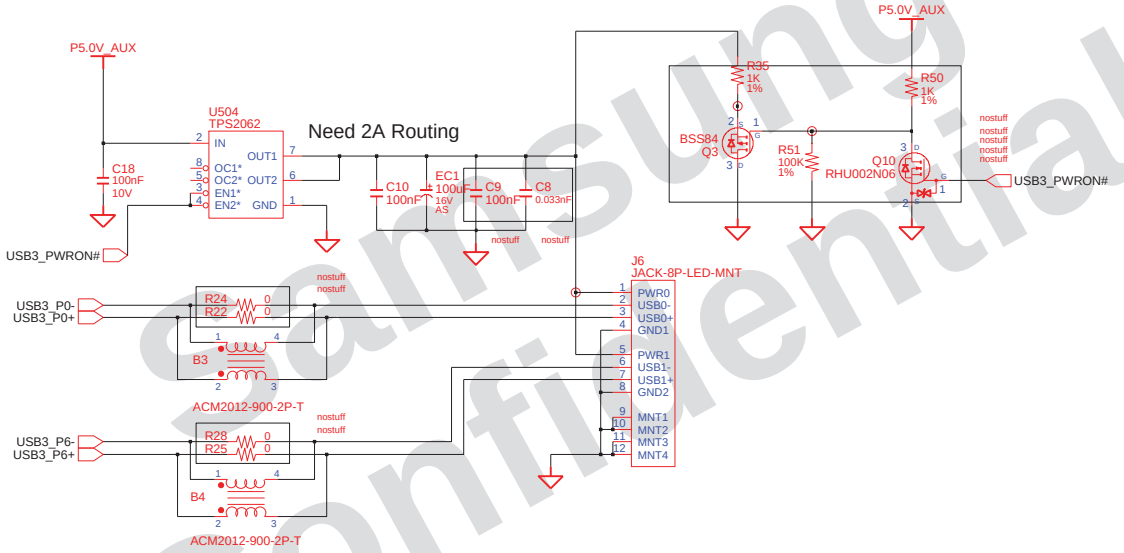
2 PORT USB CONNECTOR



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CHECK WU SHIJIANG,	DEV. STEP PV		
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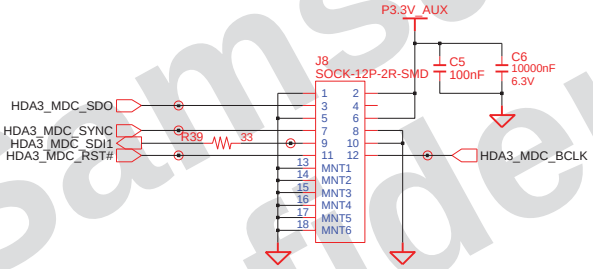
MDC Connecter



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APPROVAL BYEONGCHANG LEE,	REV 1.0		PART NO. BA41-####A
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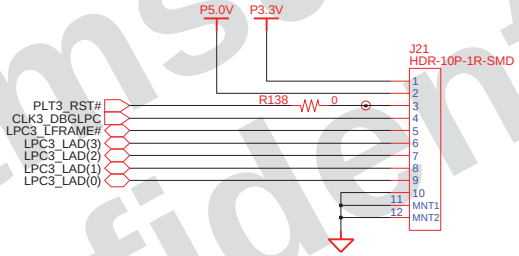
80H DECODER CONNECTOR



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DRAW SUN XIAO,	DATE 2/27/2008	TITLE Gevena 2 ext Other_Debug_80 Other_Debug_80	SAMSUNG ELECTRONICS
CHECK WU SHIJIANG,	DEV. STEP PV		
APPROVAL BYEONGCHANG LEE,	REV 1.0		PART NO. BA41-####A
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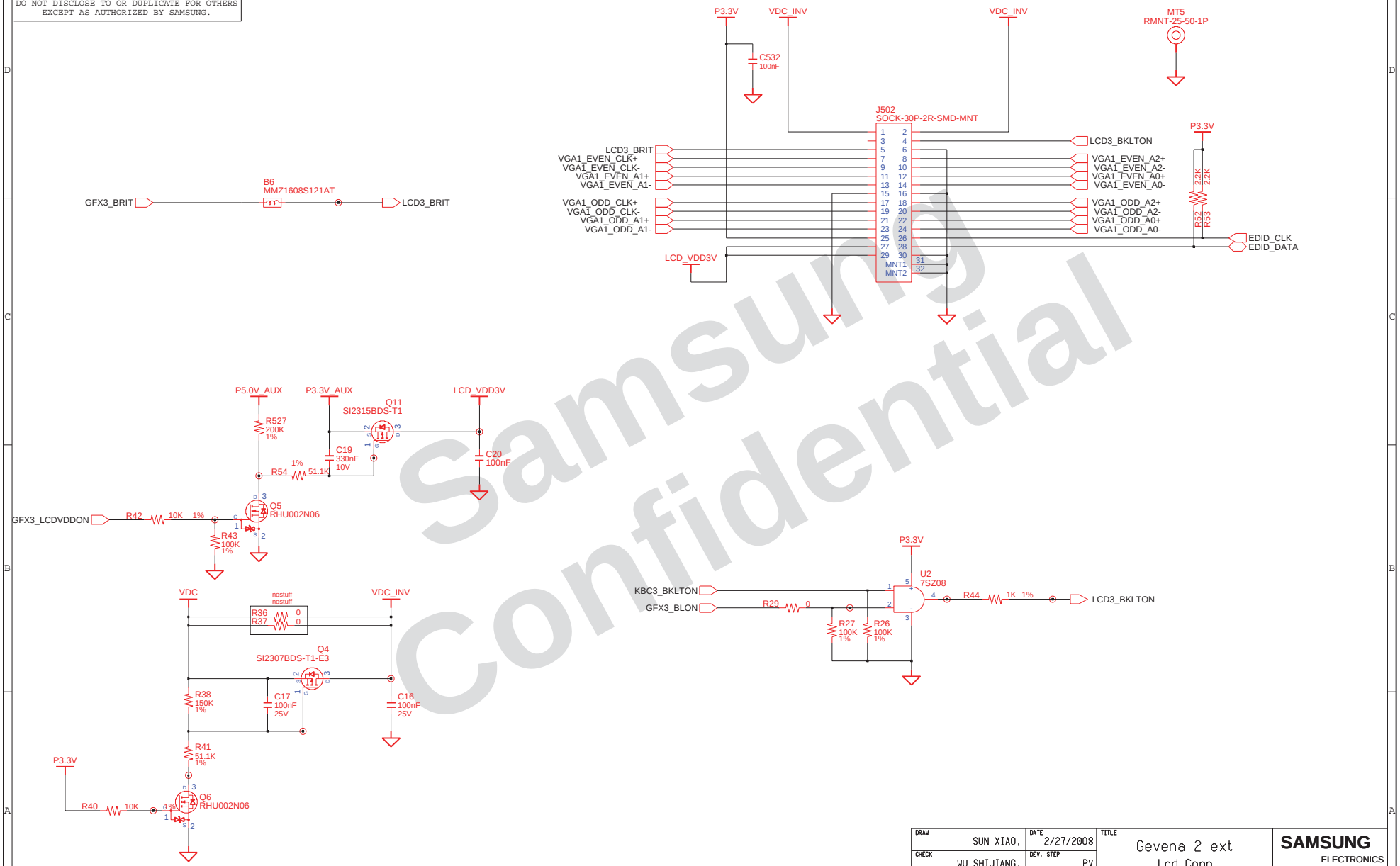

DRAW: SUN XIAO,	DATE: 2/27/2008	TITLE: Gevena 2 ext Lcd Conn	SAMSUNG ELECTRONICS
CHECK: WU SHIJIANG,	DEV. STEP: PV		
APPROVAL: BYEONGCHANG LEE,	REV: 1.0		PART NO. BA41-####A
MODULE CODE: undefined	LAST EDIT: May 08, 2008 19:01:59 PM		PAGE 1 OF 1

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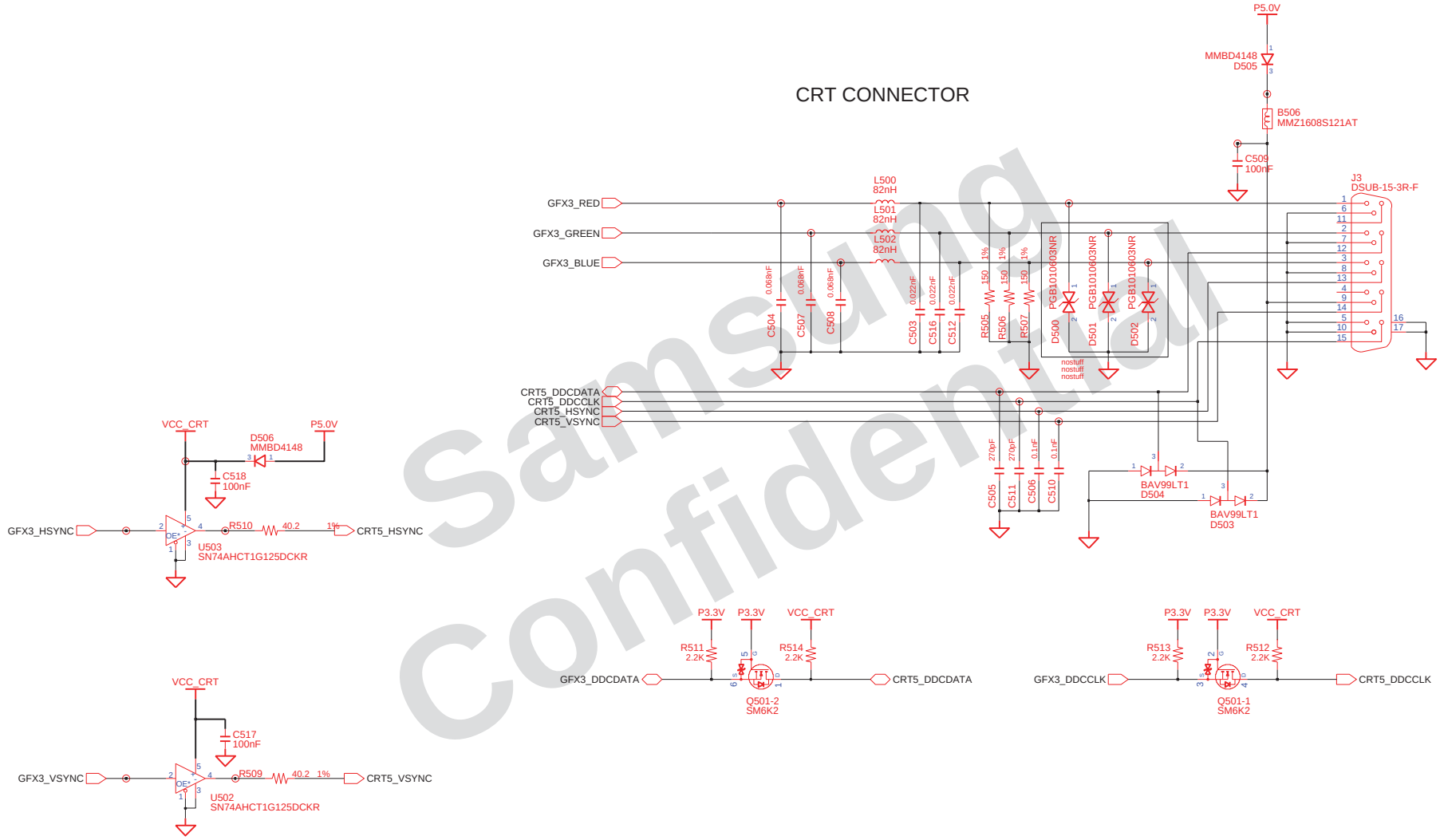
CRT CONNECTOR



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DRAW: SUN XIAO,	DATE: 2/27/2008	TITLE: Gevena 2 ext Interface_Circuit Graphics_IF_CRT	SAMSUNG ELECTRONICS
CHECK: WU SHIJIANG,	DEV. STEP: PV		
APPROVAL: BYEONGCHANG LEE,	REV: 1.0		PART NO. BA41-####A
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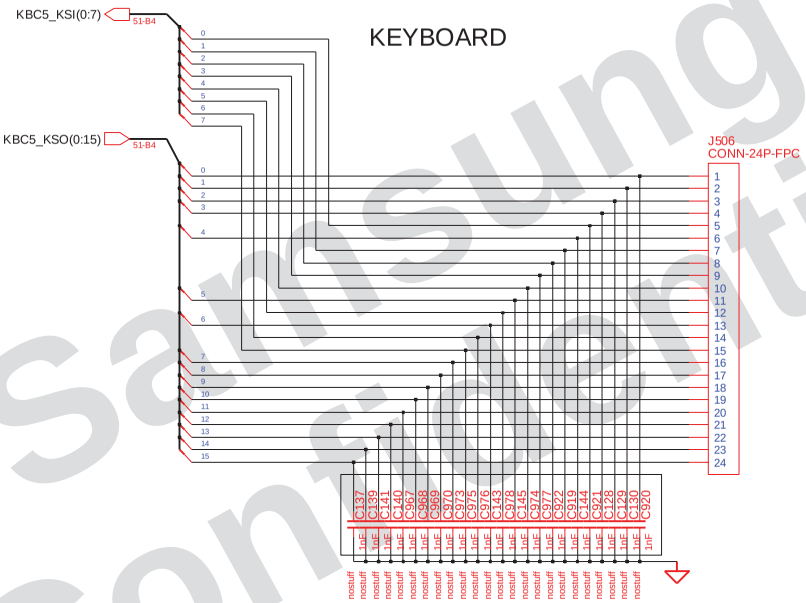

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DRAW SUN XIAO,	DATE 2/27/2008	TITLE Gevena 2 ext	SAMSUNG ELECTRONICS
CHECK WU SHIJIANG,	DEV. STEP PV	KBD_IF_Conn	
APPROVAL BYEONGCHANG LEE,	REV 1.0	KBD_IF_Conn	PART NO. BA41-####A
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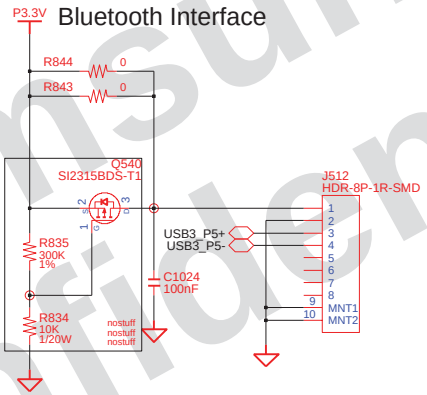
Bluetooth Interface



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DRAW SUN XIAO,	DATE 2/27/2008	TITLE Gevena 2 ext	SAMSUNG ELECTRONICS
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APPROVAL BYEONGCHANG LEE,	REV 1.0	Bluetooth_IF_Conn	PART NO. BA41-####A
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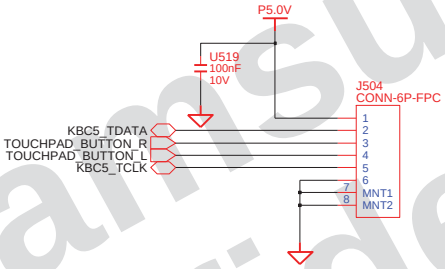
TOUCHPAD CONNECTOR



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DRAW SUN XIAO,	DATE 2/27/2008	TITLE Gevena 2 ext	SAMSUNG ELECTRONICS
CHECK WU SHIJIANG,	DEV. STEP PV	Touchpad_IF_Conn	
APPROVAL BYEONGCHANG LEE,	REV 1.0	Touchpad_IF_Conn	PART NO. BA41-####A
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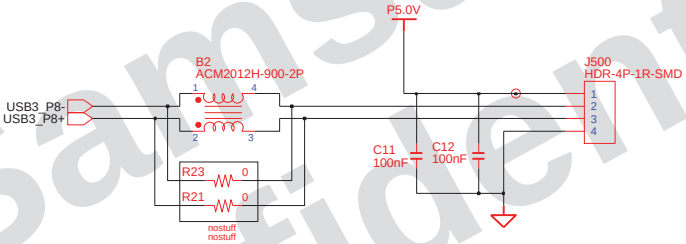
USB CAMERA FUNCTION



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DRAW SUN XIAO,	DATE 2/27/2008	TITLE Gevena 2 ext Camera_IF_Conn Camera_IF_Conn	SAMSUNG ELECTRONICS
CHECK WU SHIJIANG,	DEV. STEP PV		
APPROVAL BYEONGCHANG LEE,	REV 1.0		PART NO. BA41-####A
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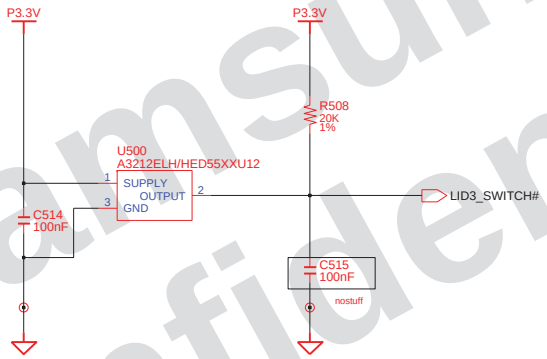
LID_SWITCH



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DRAW SUN XIAO,	DATE 2/27/2008	TITLE Gevena 2 ext LID_Switch LID_Switch	SAMSUNG ELECTRONICS
CHECK WU SHIJIANG,	DEV. STEP PV		
APPROVAL BYEONGCHANG LEE,	REV 1.0		PART NO. BA41-####A
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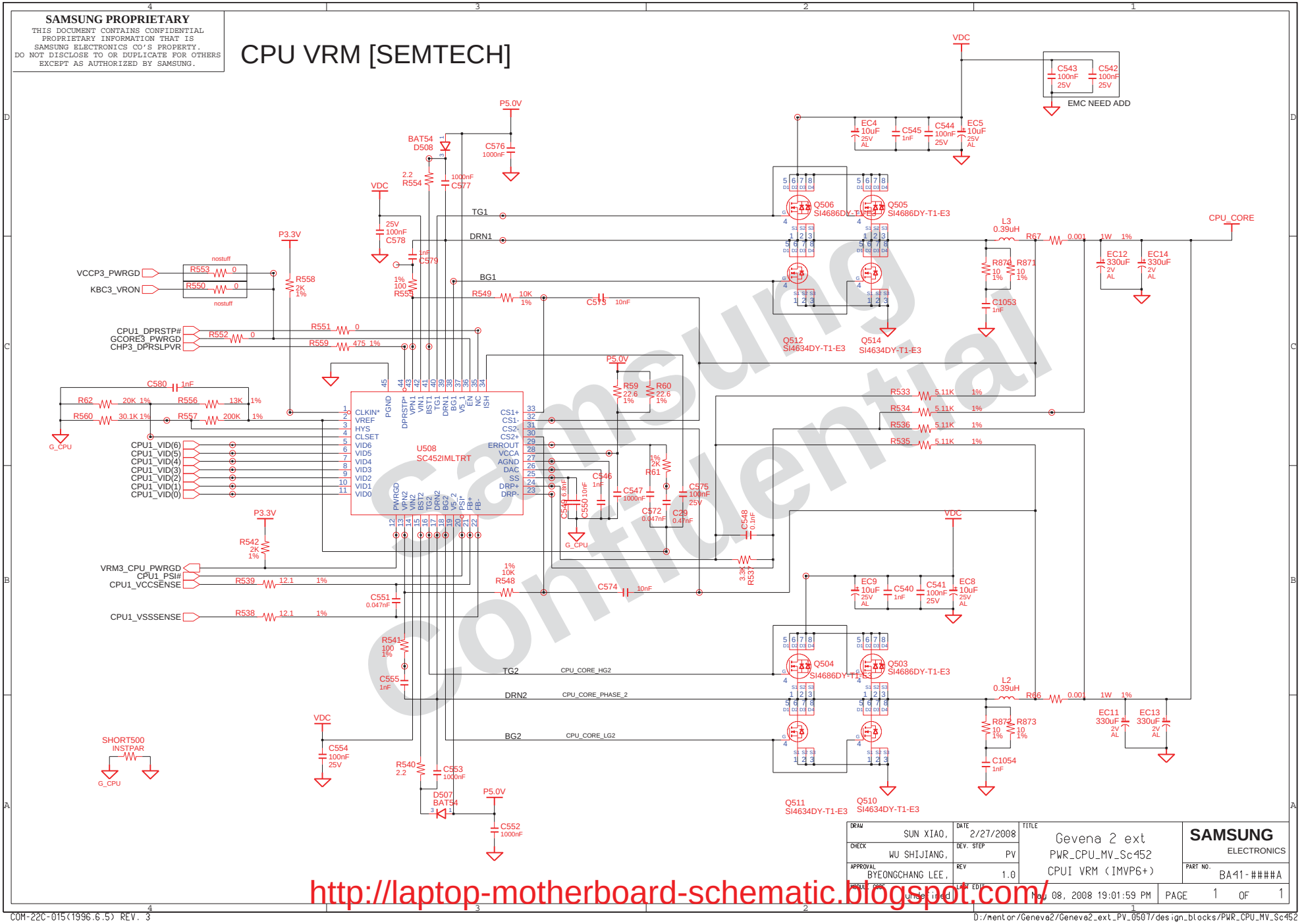
CPU VRM [SEMTECH]



DRAW: SUN XIAO,	DATE: 2/27/2008	TITLE: Gevena 2 ext PWR_CPU_MV_Sc452 CPUI VRM (IMVP6+)	SAMSUNG ELECTRONICS
CHECK: WU SHIJIANG,	DEV. STEP: PV		
APPROVAL: BYEONGCHANG LEE,	REV: 1.0		PART NO. BA41-####A
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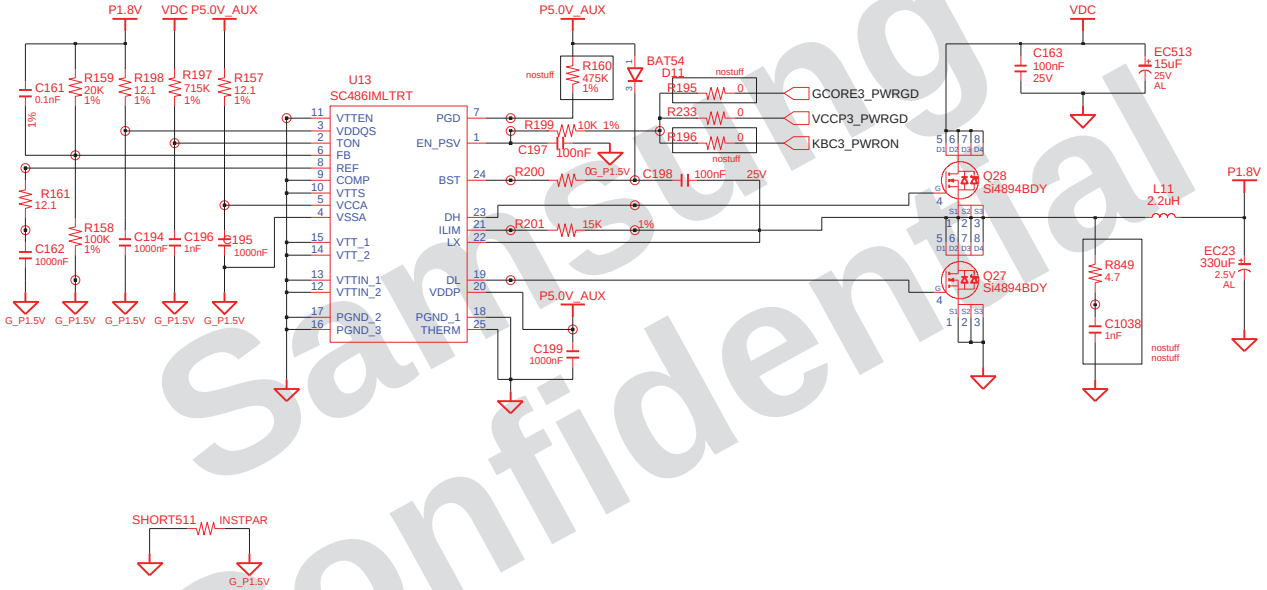
P1.8V



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DRAW: SUN XIAO,	DATE: 2/27/2008	TITLE: Gevena 2 ext PWR_Gfx_MV_Ext Ext Gfx Memory(SC486)	SAMSUNG ELECTRONICS
CHECK: WU SHIJIANG,	DEV. STEP: PV		
APPROVAL: BYEONGCHANG LEE,	REV: 1.0		PART NO. BA41-####A
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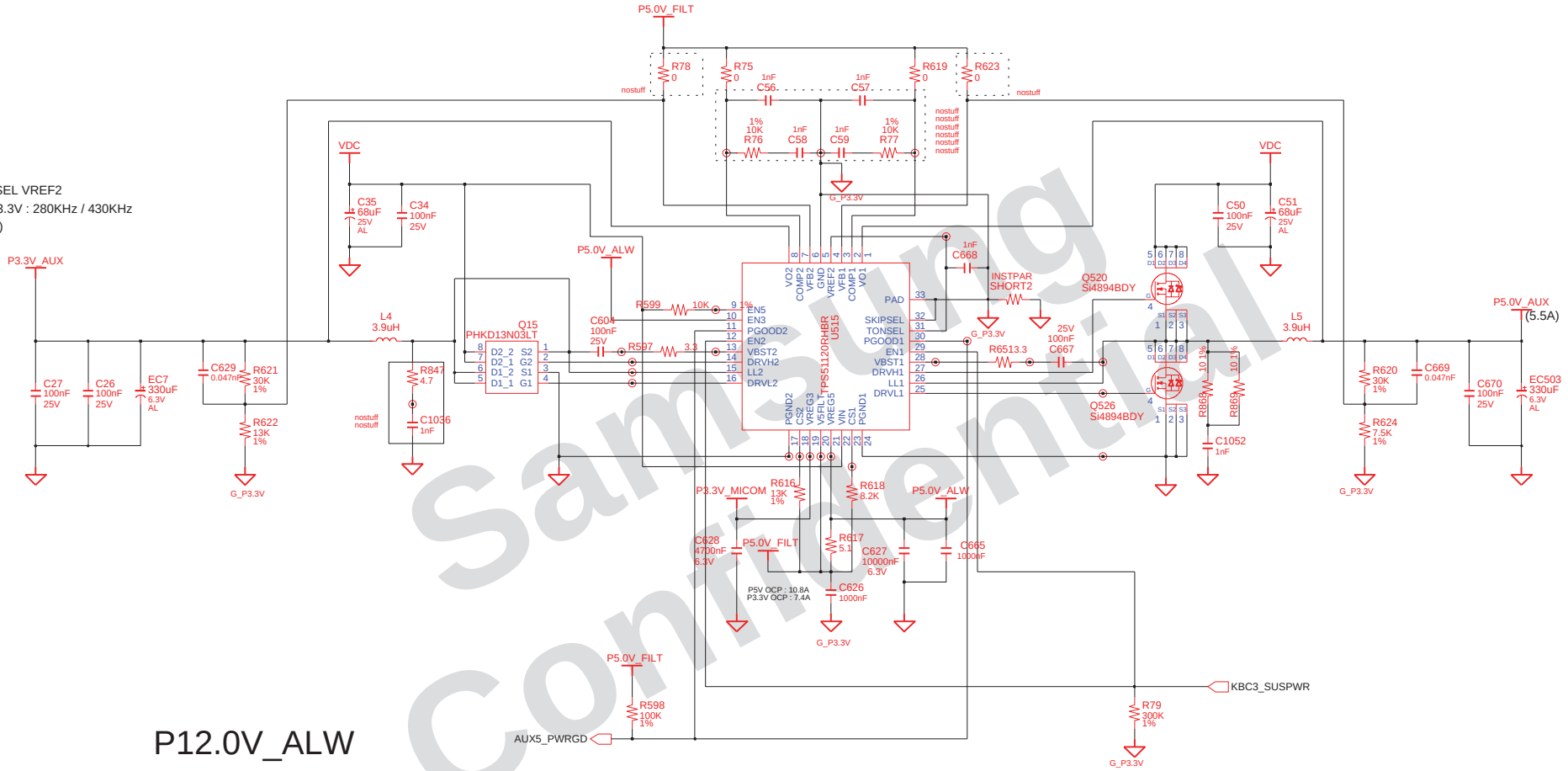
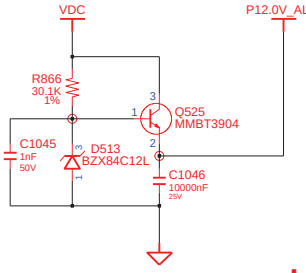
P3.3V_AUX & P5.0V_AUX

TONSEL VREF2
5V / 3.3V : 280KHz / 430KHz
(4.5A)



P12.0V_ALW



DRAW: SUN XIAO,	DATE: 2/27/2008	TITLE: Gevena 2 ext PWR_MV_3V_5V P3.3V_AUX / P5.0V_AUX	SAMSUNG ELECTRONICS
CHECK: WU SHIJIANG,	DEV. STEP: PV		
APPROVAL: BYEONGCHANG LEE,	REV: 1.0		PART NO.: BA41-####A
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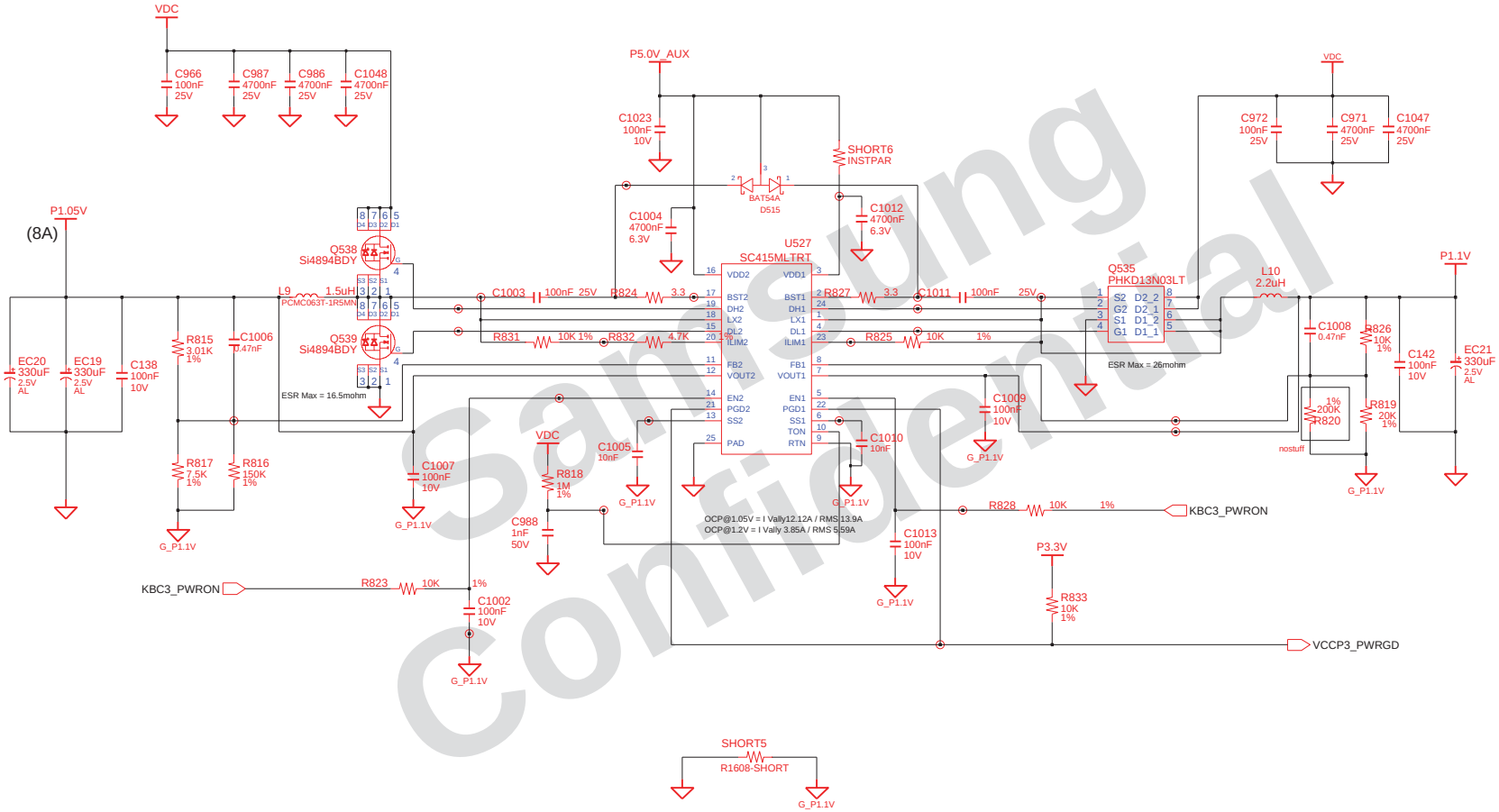
CHIPSET POWER(P1.05V & P1.1V)



DRAW SUN XIAO,	DATE 2/27/2008	TITLE Gevena 2 ext PWR_MV_Cantiga Chipset Power (P1.05V_M,P1.1V)	SAMSUNG ELECTRONICS
CHECK WU SHIJIANG,	DEV. STEP PV		
APPROVAL BYEONGCHANG LEE,	REV 1.0		PART NO. BA41-####A
MODEL CODE Unpublished	LAST EDIT May 08, 2008 19:01:59 PM		PAGE 1 OF 1

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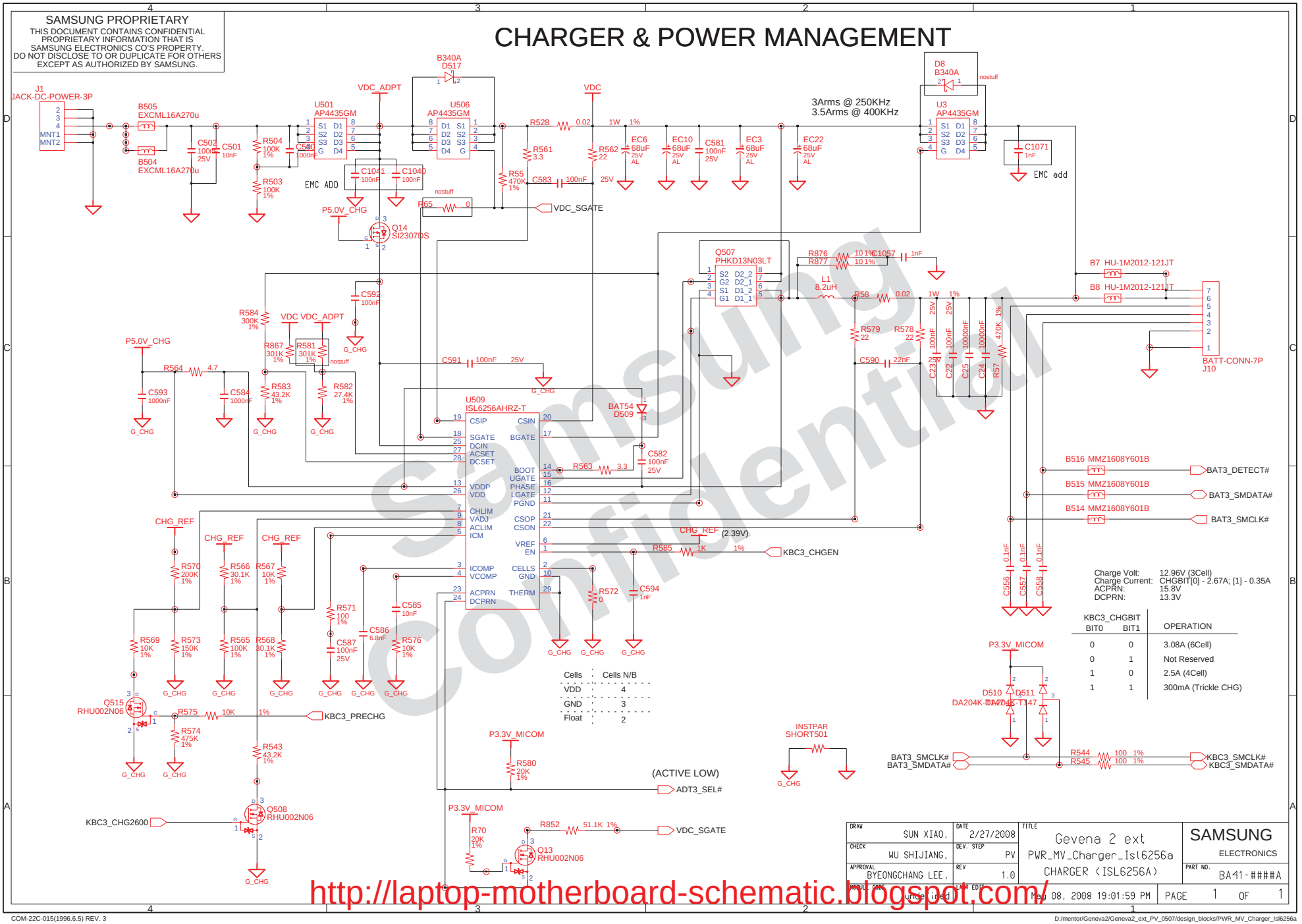
CHARGER & POWER MANAGEMENT



KBC3_CHGBIT BIT0	BIT1	OPERATION
0	0	3.08A (6Cell)
0	1	Not Reserved
1	0	2.5A (4Cell)
1	1	300mA (Trickle CHG)

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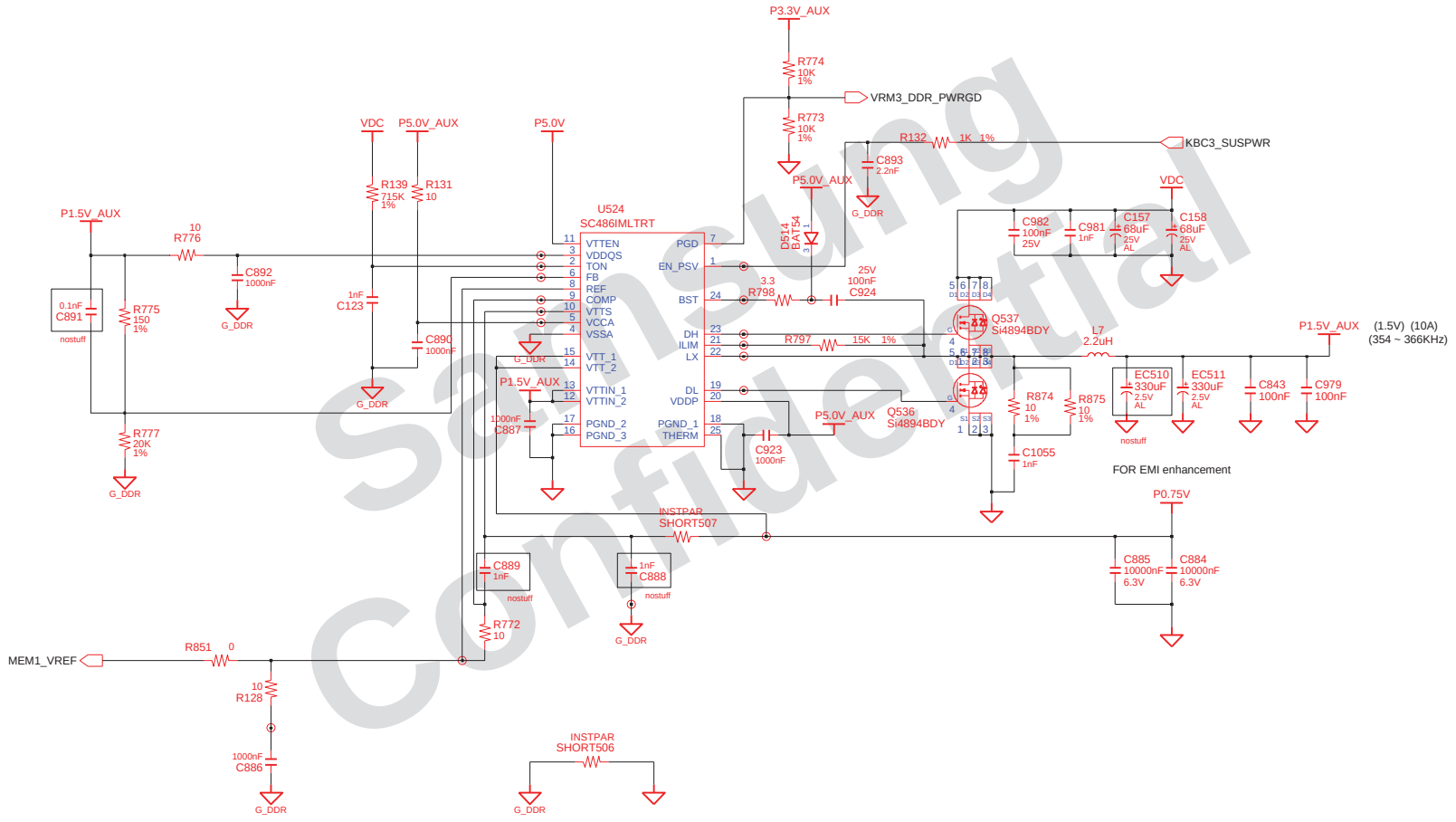
DDR3 Power



DRAW SUN XIAO,	DATE 2/27/2008	TITLE Gevena 2 ext PWR_MV_MeMory DDR3 POWER (P1.5V_AUX)	SAMSUNG ELECTRONICS
CHECK WU SHIJIANG,	DEV. STEP PV		
APPROVAL BYEONGCHANG LEE,	REV 1.0		PART NO. BA41-####A
MODULE CODE Unclassified	LAST EDIT May 08, 2008 19:01:59 PM		PAGE 1 OF 1

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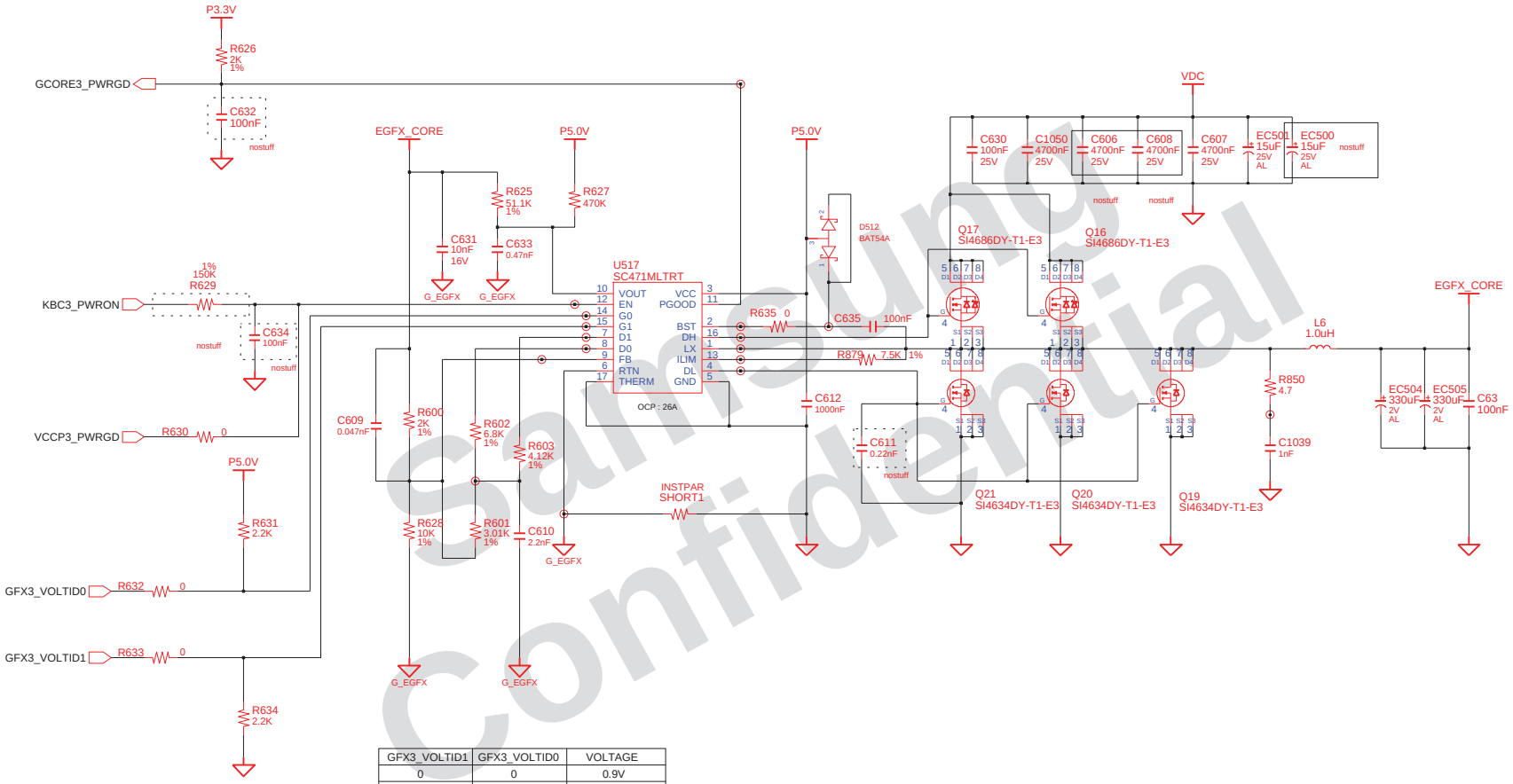
Graphic Core Power



GFX3_VOLTID1	GFX3_VOLTID0	VOLTAGE
0	0	0.9V
0	1	1.09V
1	0	1.17V
1	1	RESERVED

DRAW: SUN XIAO,	DATE: 2/27/2008	TITLE: Gevena 2 ext PWR_Gfx_MV_Ext Ext Gfx Core(SC471)	SAMSUNG ELECTRONICS
CHECK: WU SHIJIANG,	DEV. STEP: PV		
APPROVAL: BYEONGCHANG LEE,	REV: 1.0		PART NO.: BA41-####A
MODULE CODE:	LAST EDIT: May 08, 2008 19:01:59 PM		PAGE 2 OF 2

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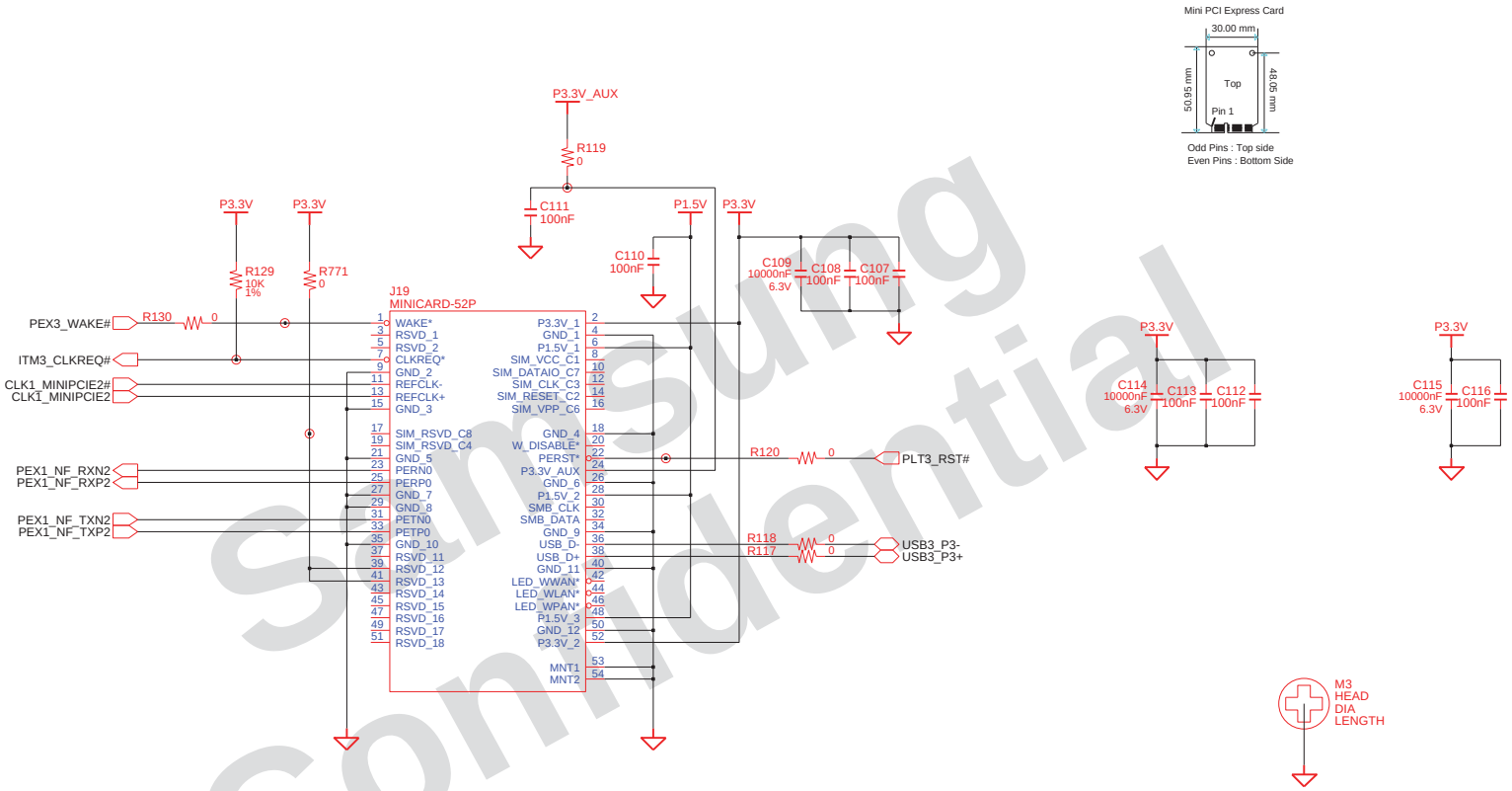
MINI CARD FOR ROBSON



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DRAW SUN XIAO,	DATE 2/27/2008	TITLE Gevena 2 ext Robson_PCIE Robson_PCIE	SAMSUNG ELECTRONICS
CHECK WU SHIJIANG,	DEV. STEP PV		
APPROVAL BYEONGCHANG LEE,	REV 1.0		PART NO. BA41-####A
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