

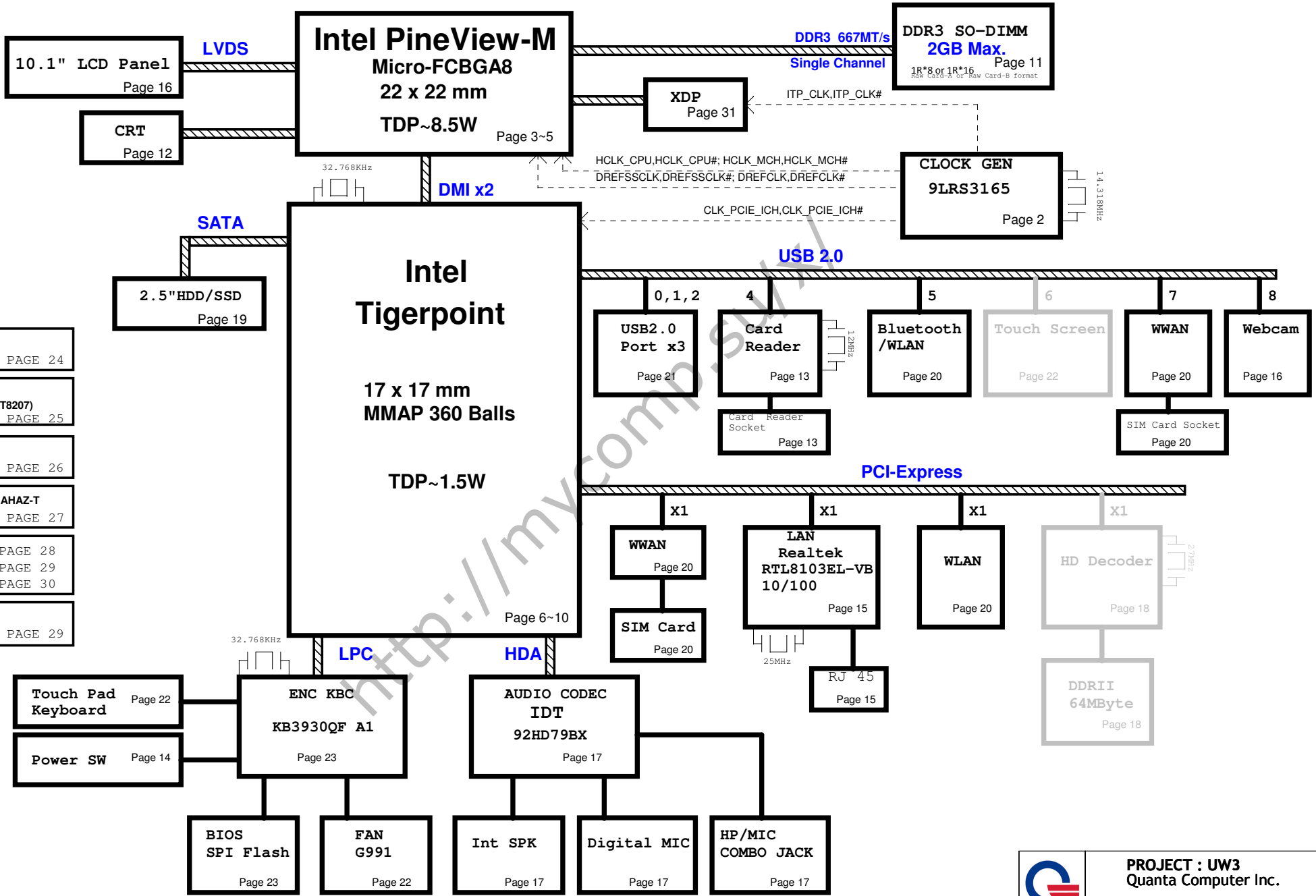
UW3 Block Diagram

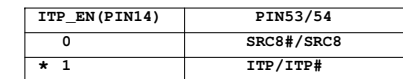
01

PCB STACK UP

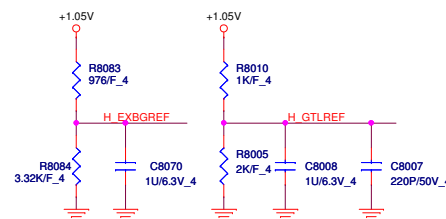
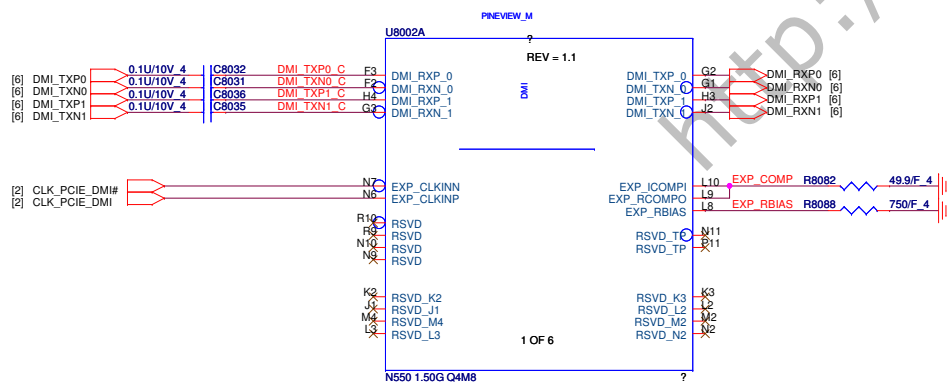
6L

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT





 NB5	PROJECT : UW3 Quanta Computer Inc.		
	Size	Document Number	Rev
	Clock Gen		1A
Date: Thursday, September 02, 2010 Sheet 2 of 32			

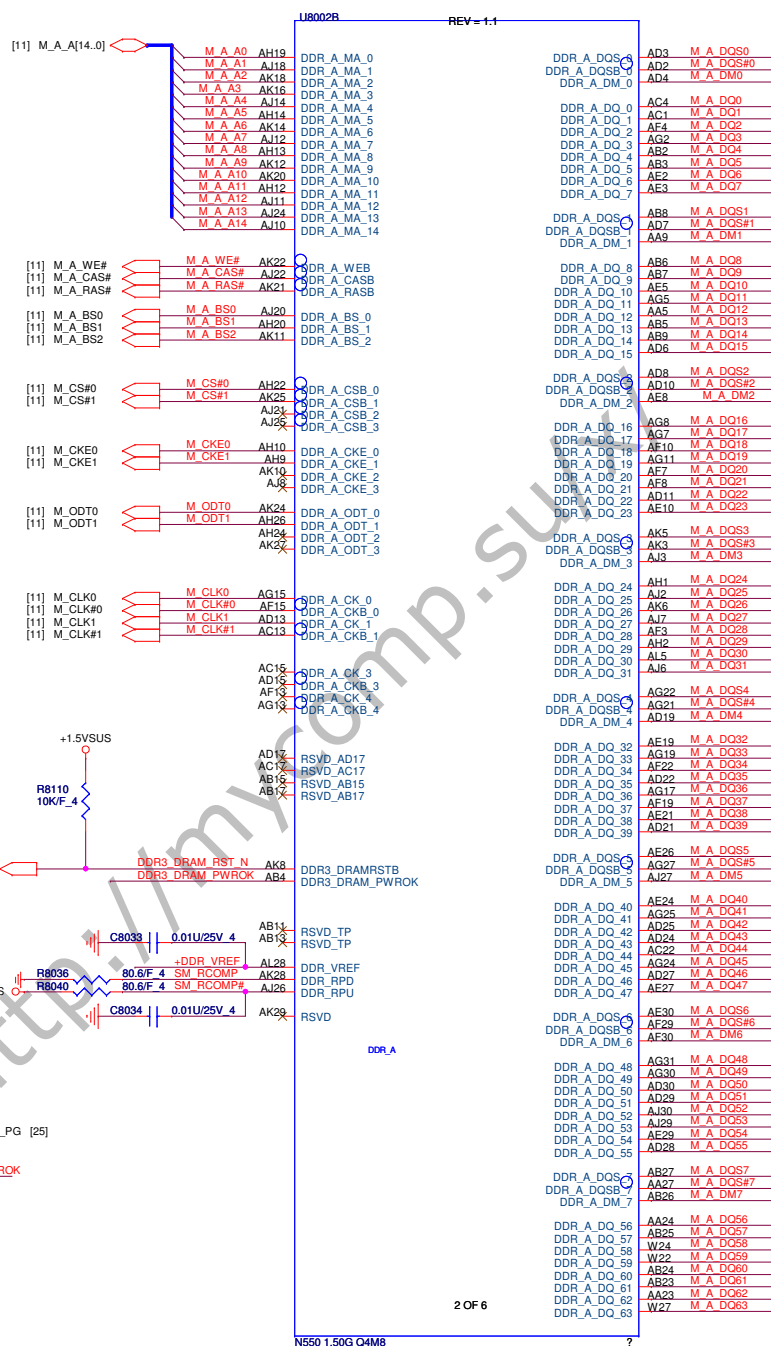


+1.5VSUS [5,11,25,28,29,30]
+0.75VSMVREF [11,25]

PINEVIEW_M



Intel CRB



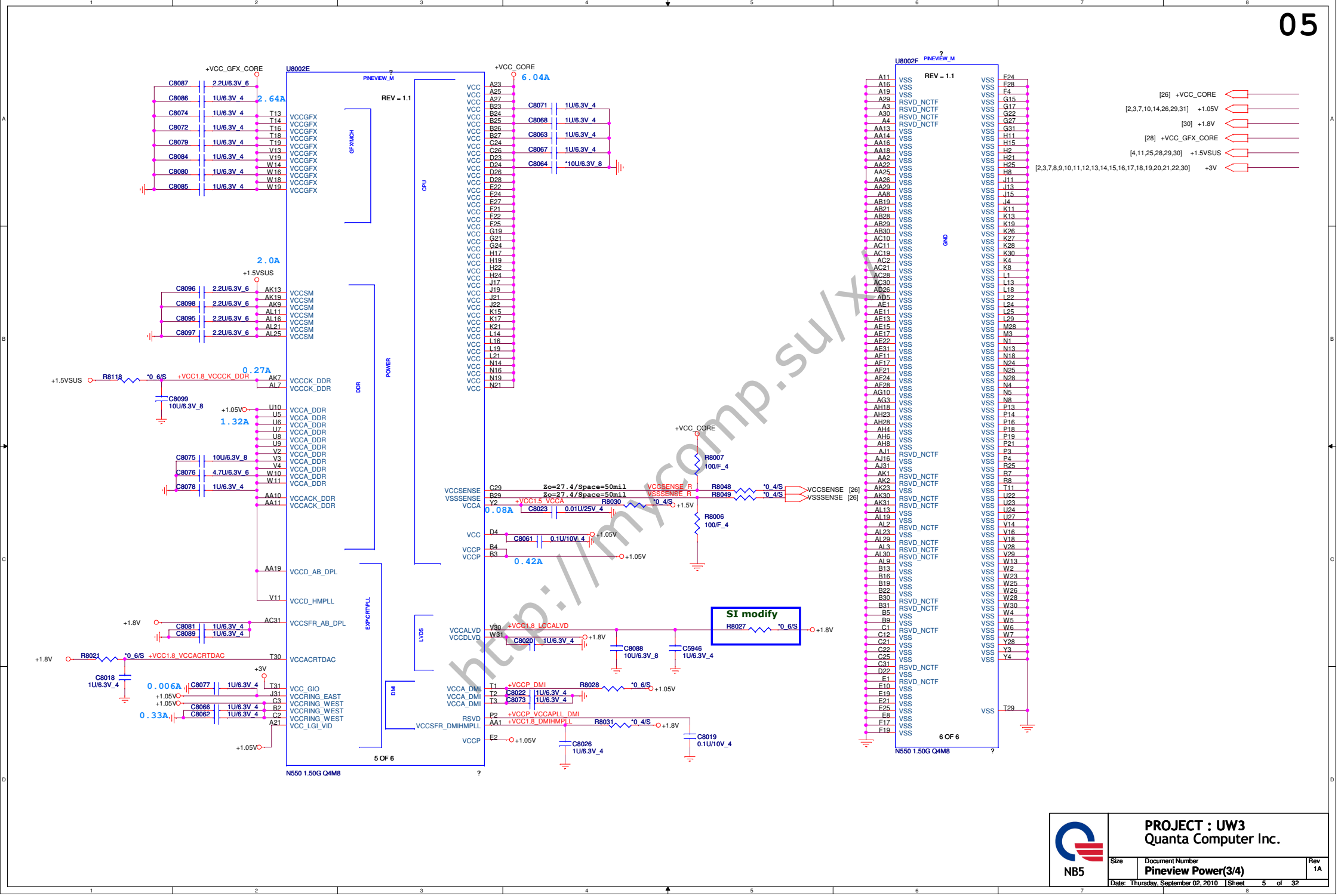
M_A_DQ[63:0] [11]
M_A_DM[7:0] [11]
M_A_DQS[7:0] [11]
M_A_DQS#[7:0] [11]



PROJECT : UW3
Quanta Computer Inc.

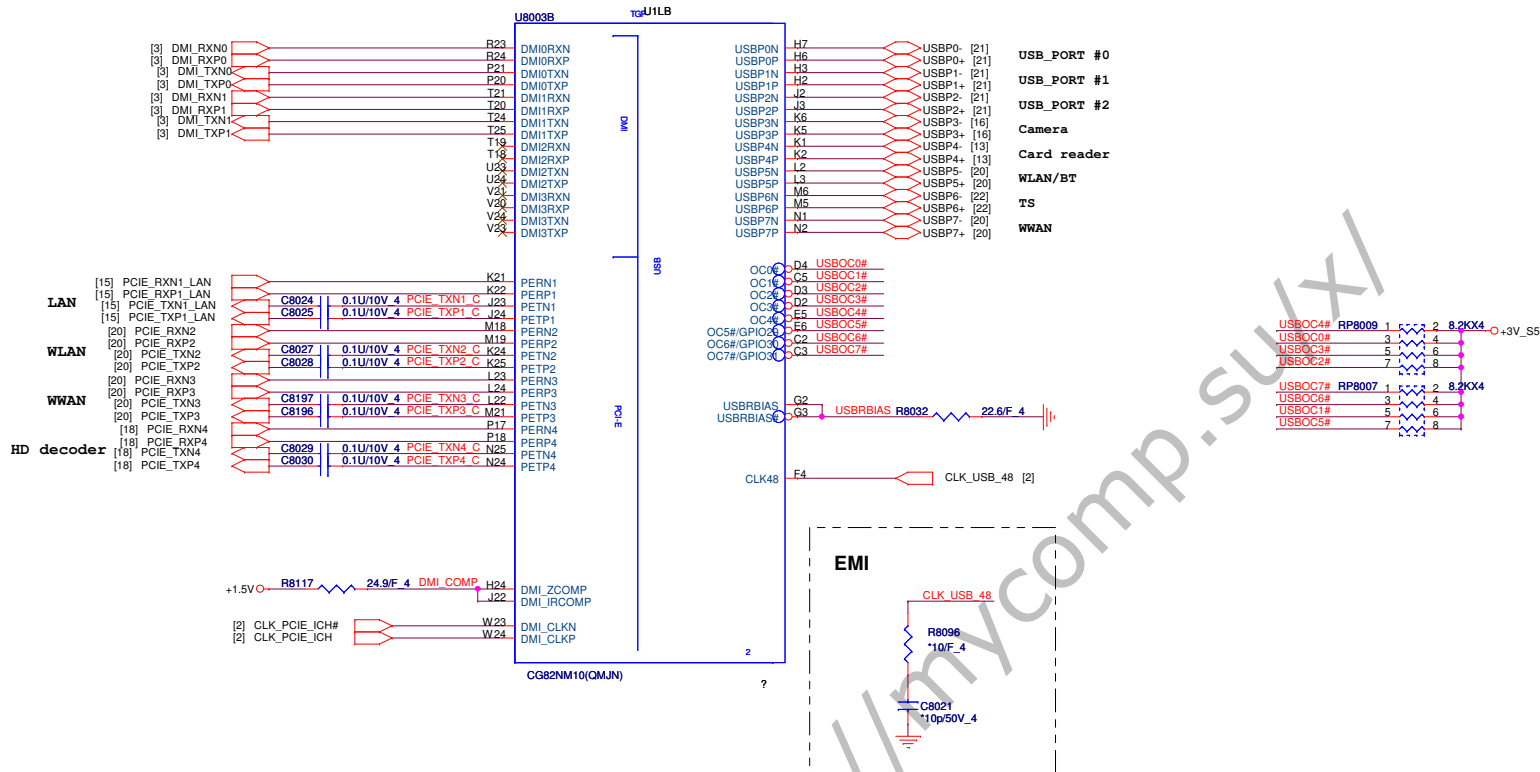
Size Document Number
Pineview DDR(2/4)
Date: Thursday, September 02, 2010 1 Sheet 4 of 32

Rev
1A

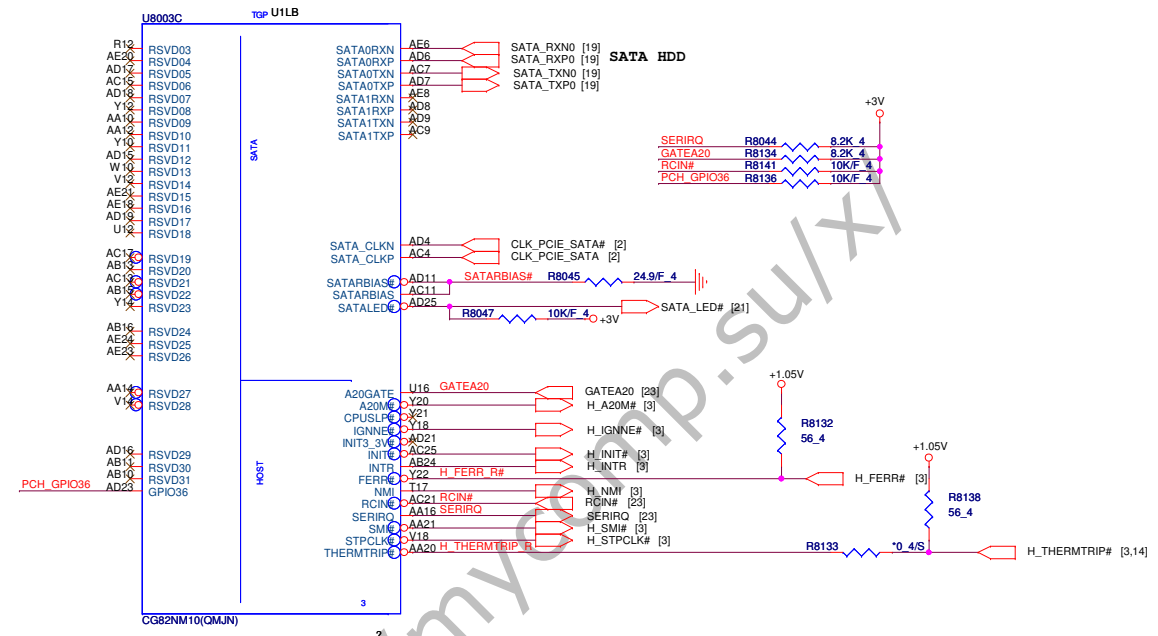


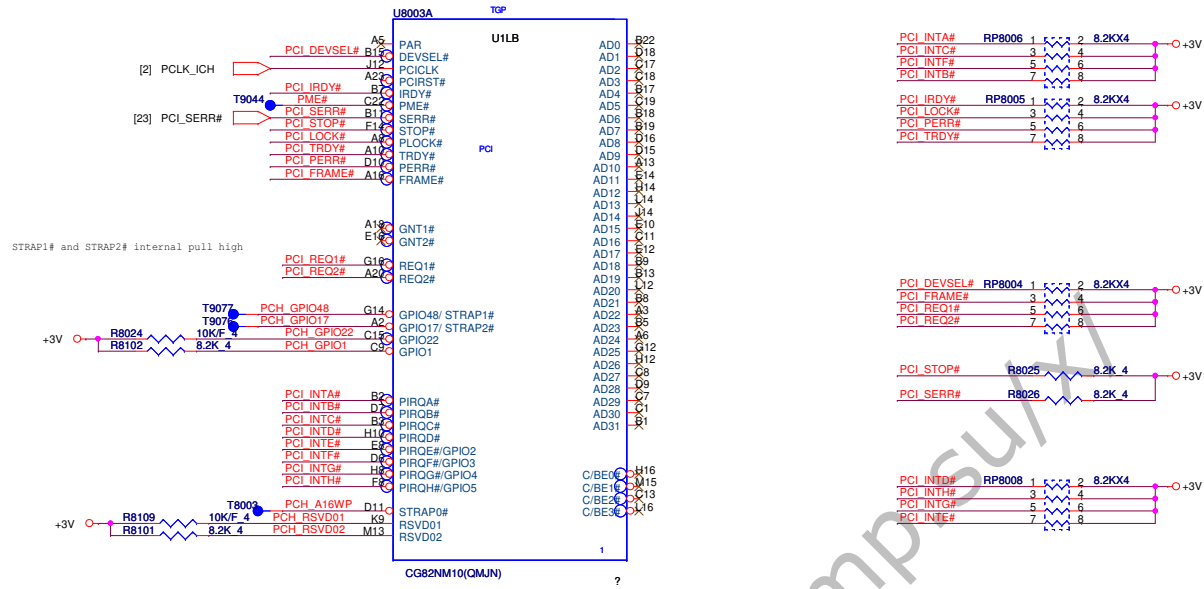
[5,10,18,20,30] +1.5V

[9,10,30] +3V_S5



+3V [2,3,5,8,9,10,11,12,13,14,15,16,17,18,19,20,21,22,30]
+1.05V [2,3,5,10,14,26,29,31]





ICH Boot BIOS select

PCH_GPIO17 (INT PU)	PCH_GPIO48 (INT PU)	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC (Default)

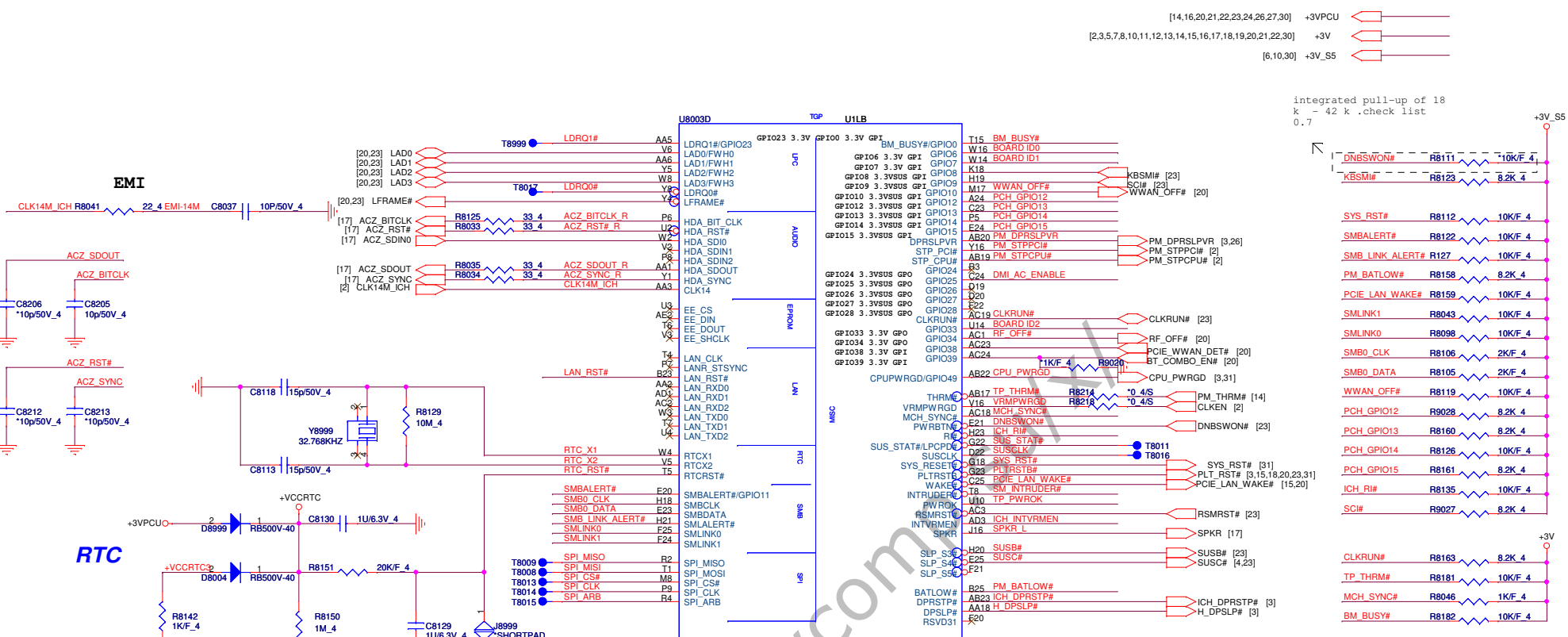
A16 SWAP Override strap

PCH_A16WP (INT PU)	Low = A16 swap override enabled High = Default
-----------------------	---

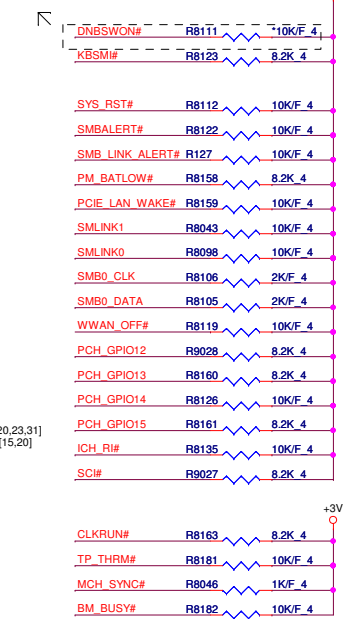
IRQ	Description
PIRQA	USB UHCI Controller #1, #4
PIRQB	AC'97 codec; option for SMBUS
PIRQC	USB UHCI Controller #3; SATA/IDE Native Mode
PIRQD	USB UHCI Controller #2
PIRQE	Internal LAN; Option for SCI, TCO, HPET#0,1,2
PIRQF	Option for SCI, TCO, HPET#0,1,2
PIRQG	Option for SCI, TCO, HPET#0,1,2
PIRQH	USB EHCI Controller; Option for SCI, TCO, HPET#0,1,2

PCI_GNT#2	Internal PU Should not be PD
-----------	---------------------------------





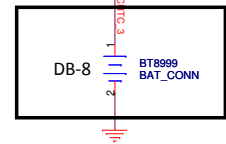
integrated pull-up of 18 k - 42 k .check list 0.7



INTRVMEN	
Enable (default)	1
Disable	0

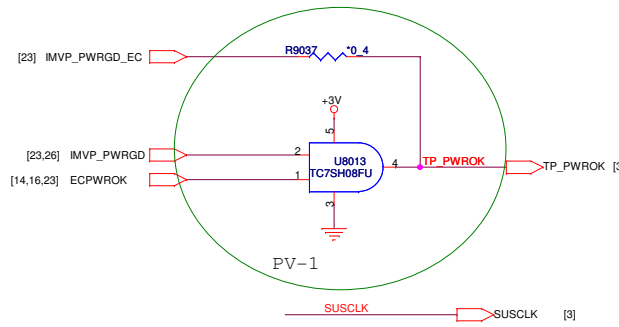
CG82NM10(QMJN)			
Board ID	ID0	ID1	ID2
R8223	0	0	0
R8225	1	0	0
R8227	0	1	0
R8228	1	1	0

ACZ_SDOUIT (INT PD)	ACZ_SYNC (INT PD)	Description
0	0	* 4 x 1s
1	0	Reserved
0	1	Reserved
1	1	1 x 4s(1 port/4 lanes)

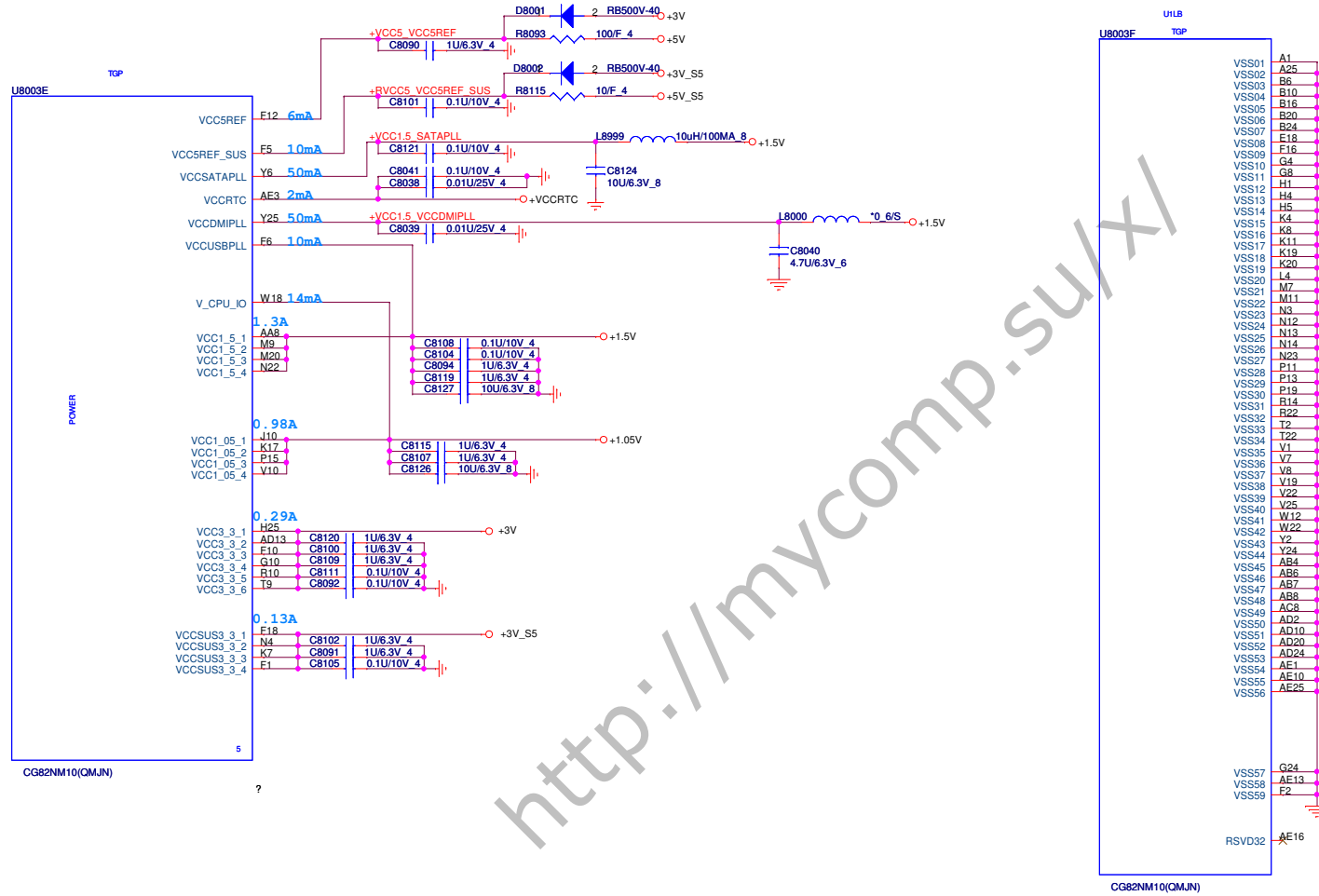


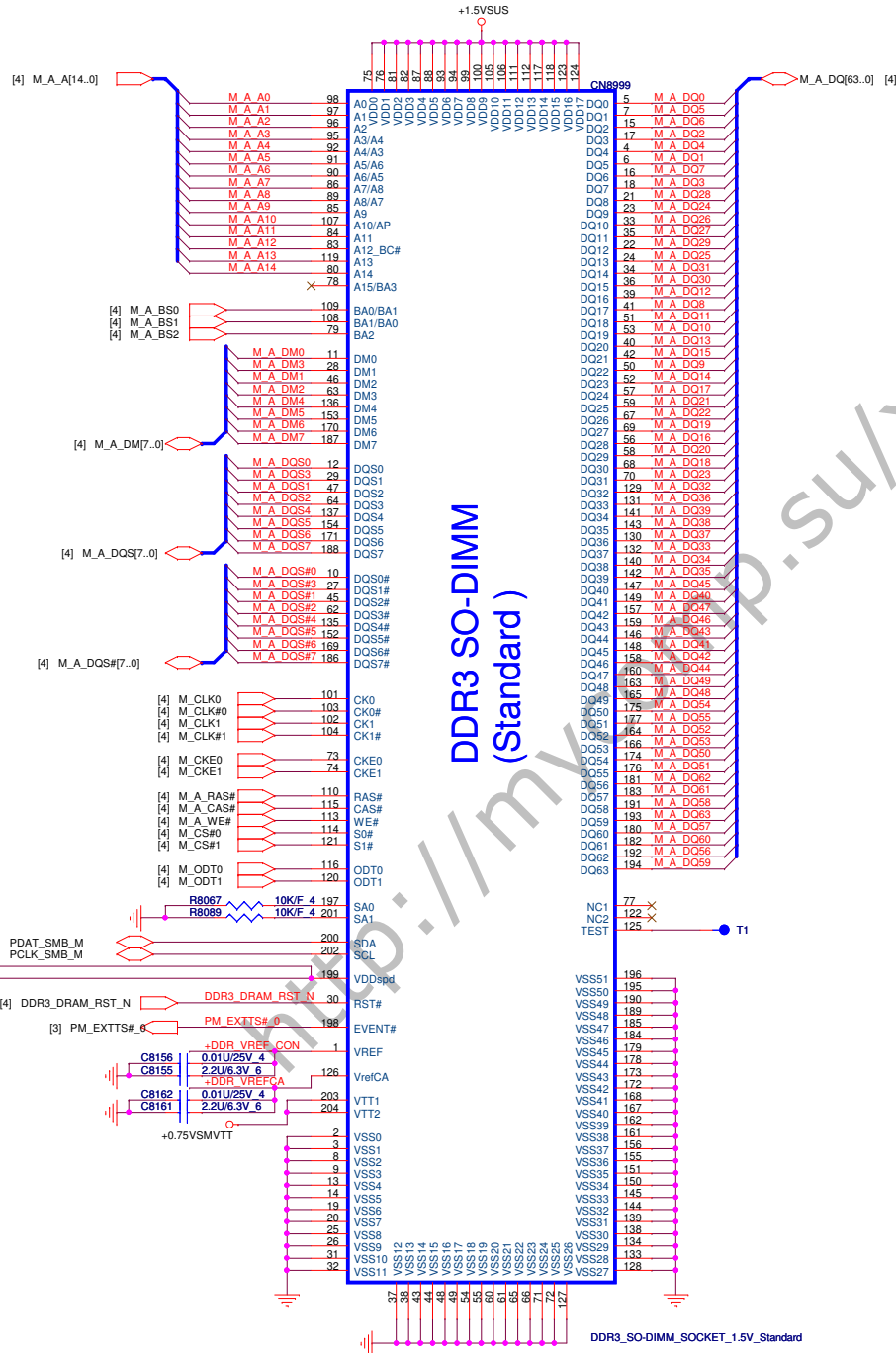
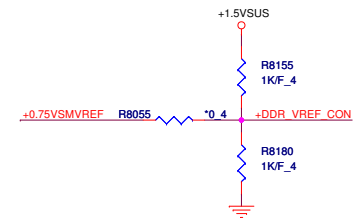
GPIO25 This signal has a weak internal pull-up. If the signal is sampled high, the DMI interface is strapped to operate in DC coupled mode (No coupling capacitors are required on DMI differential pairs). If the signal is sampled low, the DMI interface is strapped to operate in AC coupled mode (Coupling capacitors are required on DMI differential pairs). NOTE: Board designer must ensure that DMI implementation matches the strap selection.

DMI AC_ENABLE R8108 1K/F 4



[2,3,5,7,8,9,11,12,13,14,15,16,17,18,19,20,21,22,30]	+3V	
[12,16,17,19,20,22,30]	+5V	
[5,6,18,20,30]	+1.5V	
[2,3,5,7,14,26,29,31]	+1.05V	
[6,9,30]	+3V_S5	
[4,30]	+5V_S5	



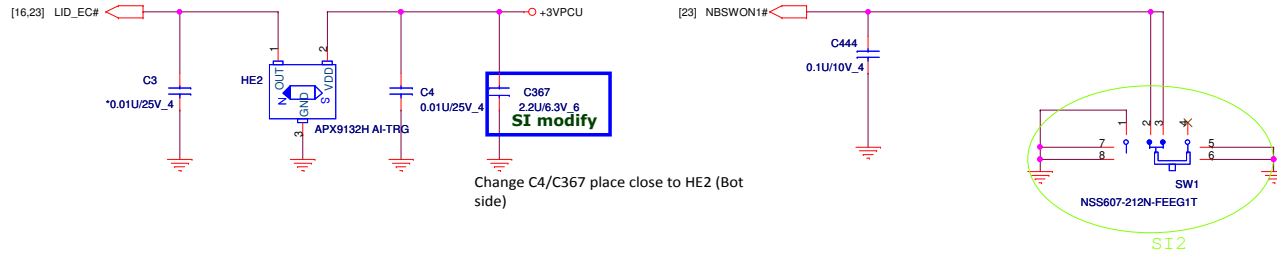




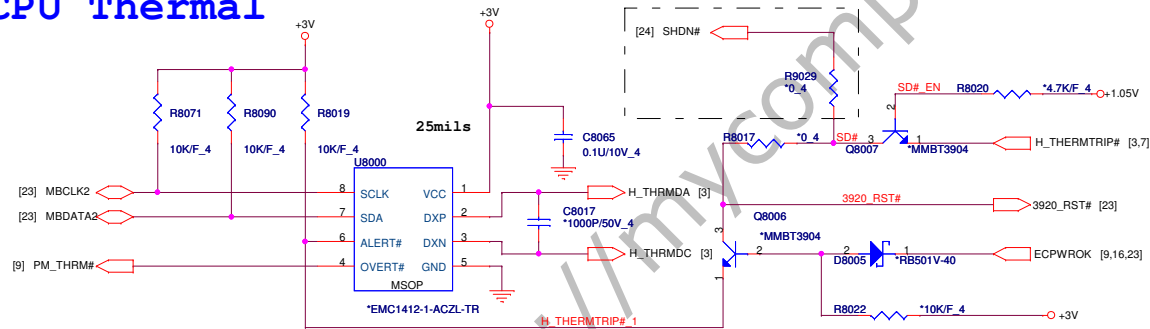


LID Switch

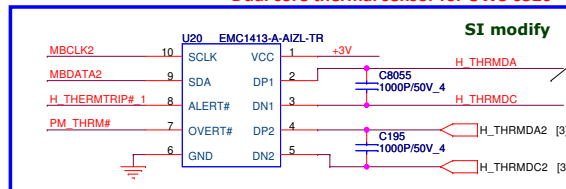
+3VPCU [9,16,20,21,22,23,24,26,27,30]
 +3V [2,3,5,7,8,9,10,11,12,13,15,16,17,18,19,20,21,22,30]
 +1.05V [2,3,5,7,10,26,29,31]



CPU Thermal

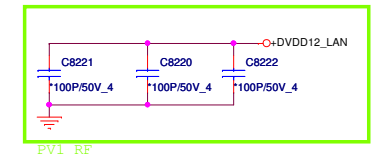
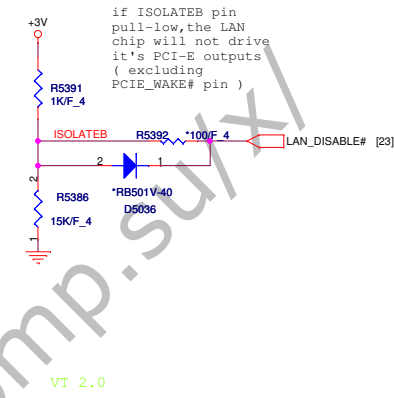
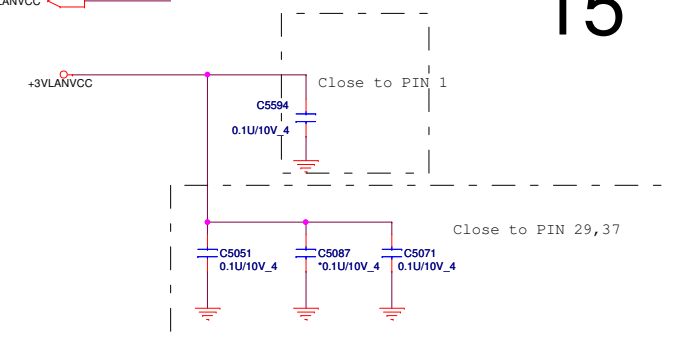
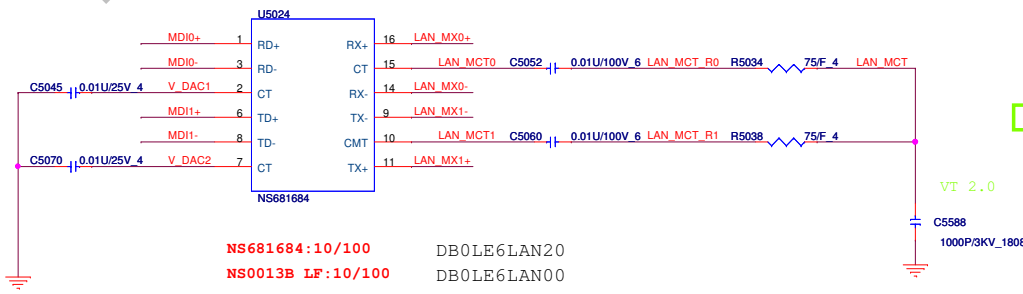


Dual core thermal sensor for UW3 0520

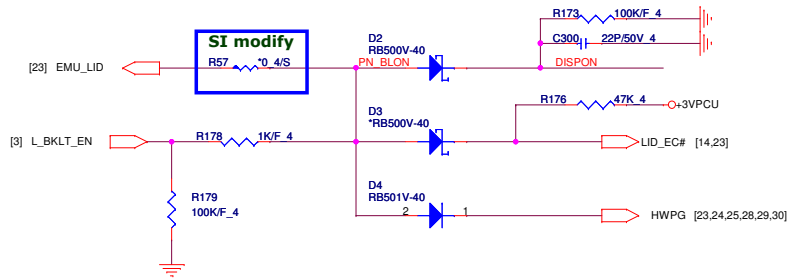


C8055 Place close to U20#2,3
SI modify

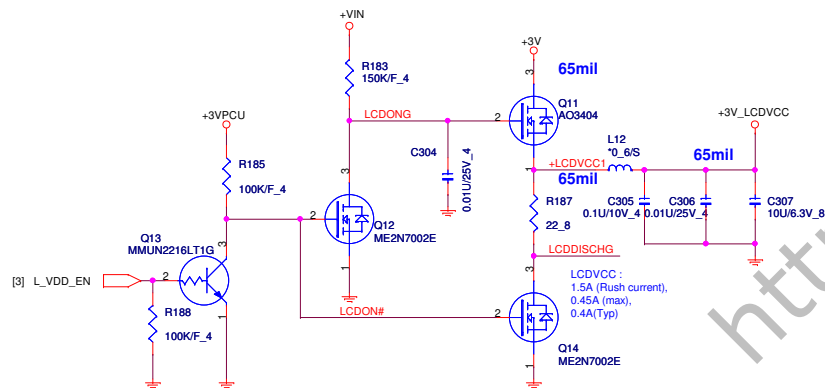
SMSC
 Single Code: C8055 non-Staff, C8017 Staff
 AL001412003 EMC1412-1-ACZL-TR
 Dual Code: AL001413002 EMC1413-A-AIZL-TR
 C8055 staff, C8017 non-Staff

[illegible]

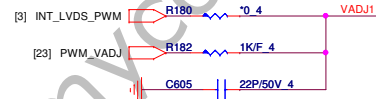
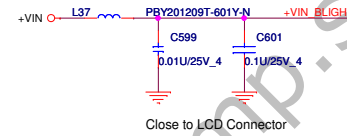
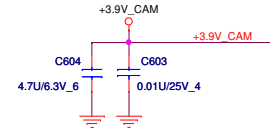
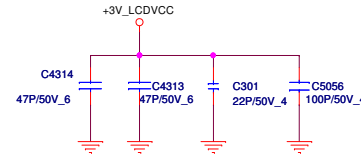
Backlight Control(LDS)



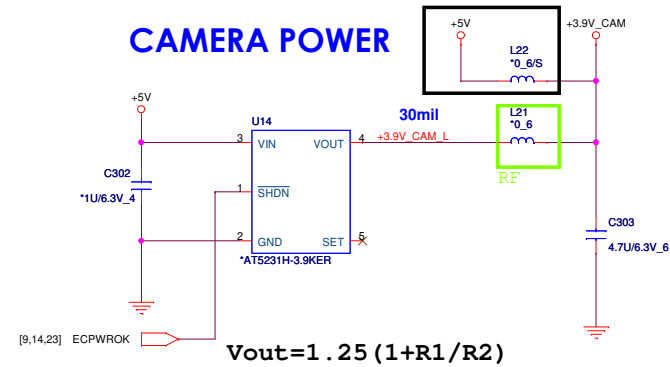
LCD POWER SWITCH



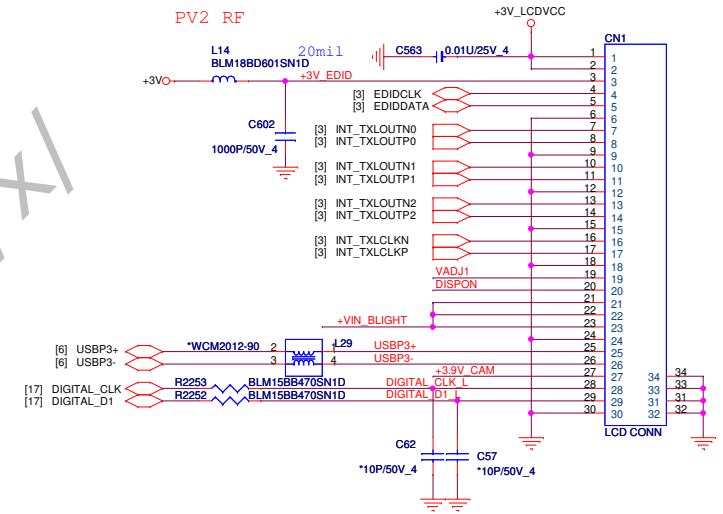
Request by HP RF (47Px2)

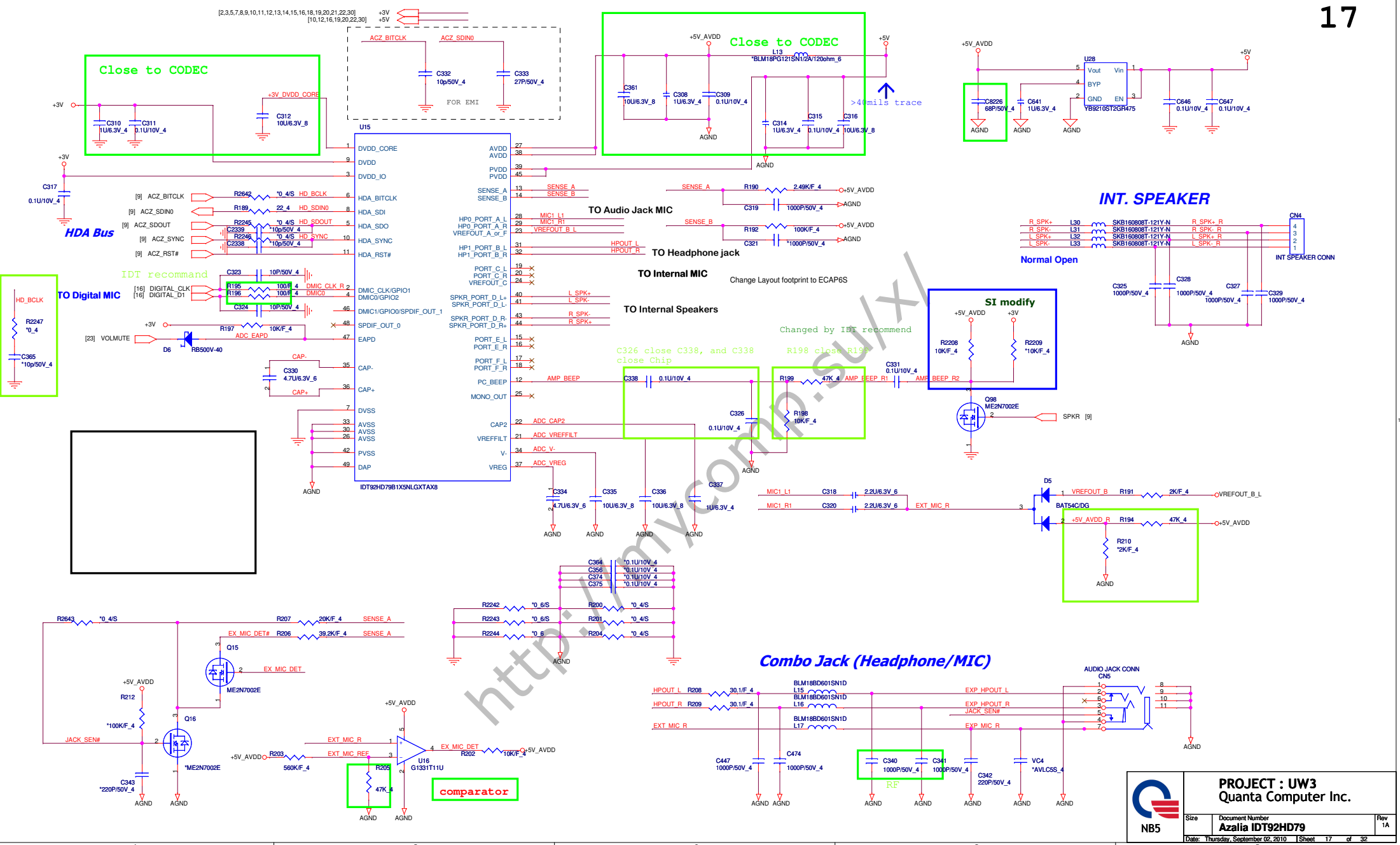


CAMERA POWER



LED Panel(LDS)

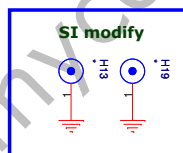
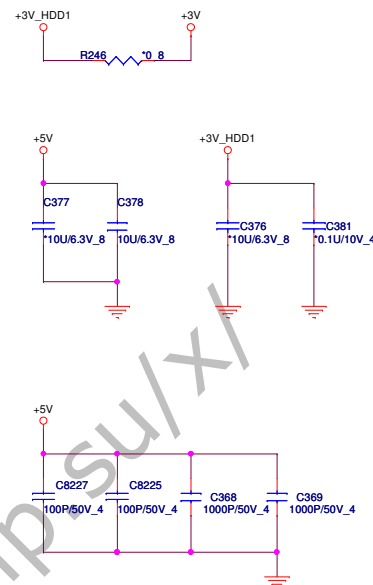
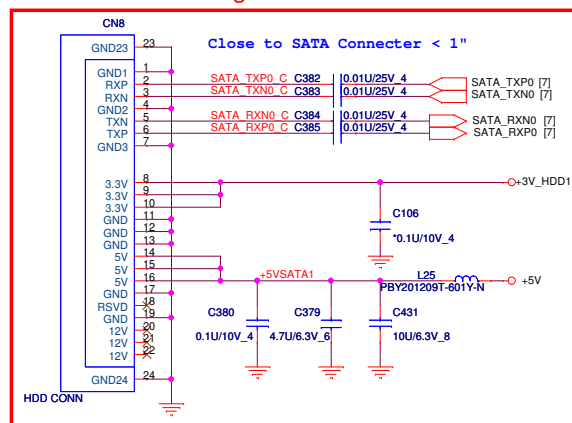




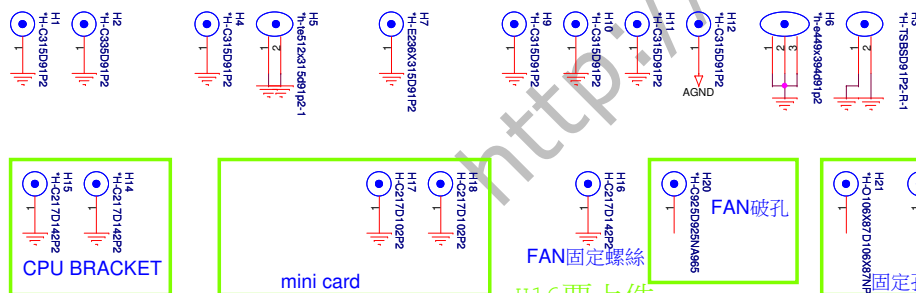
2.5" SATA HDD OR SSD(TOSHIBA)

DC Current rating: 0.5 A

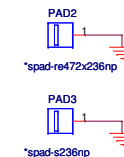
change for UW3 0520



M/B Screw Hole



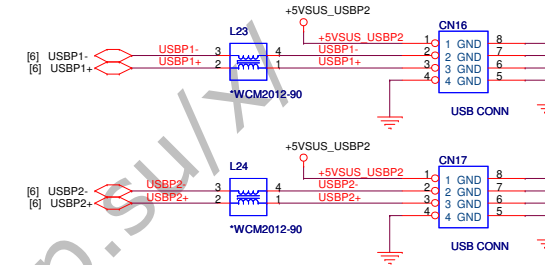
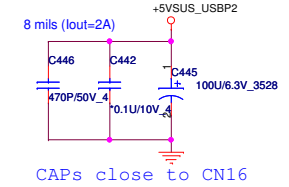
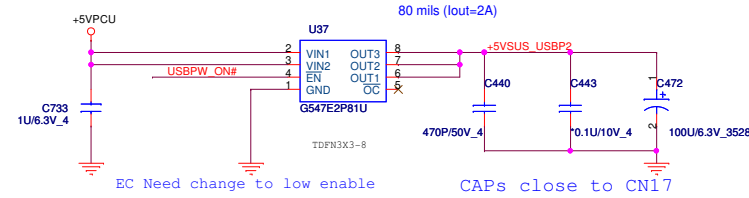
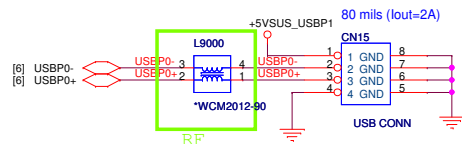
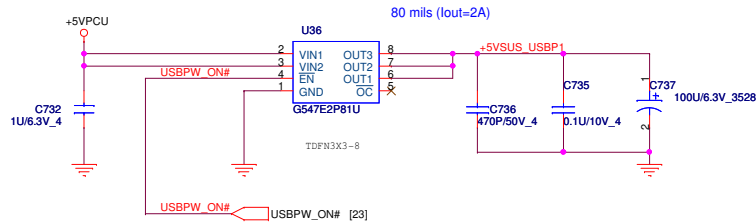
EMI spring



1x Left side USB port supports Keyed USB.

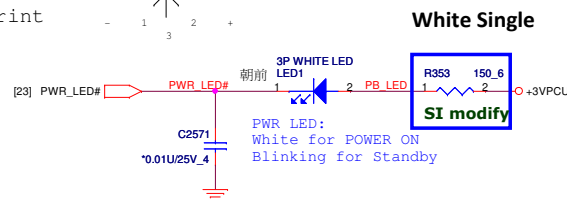
For Right 2xUSB Ports PWR

21



PWR Button/LED

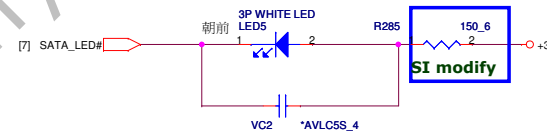
Footprint



SATA/LED

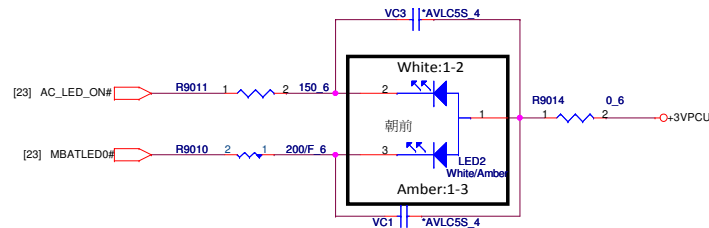
Change R285,R353 to 150 ohm

White Single



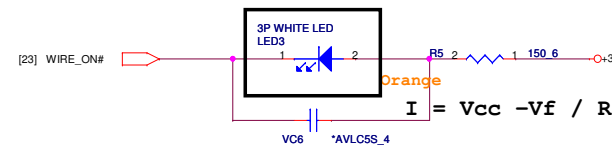
Charging & Discharging/LED

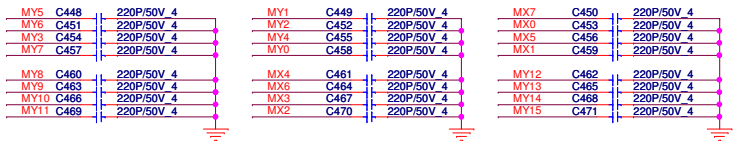
Footprint



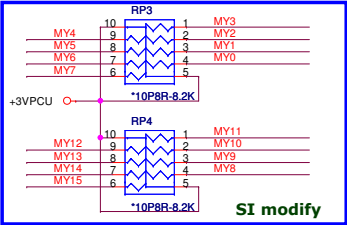
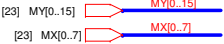
WLAN/BLUETOOTH & WWAN LED

White Single

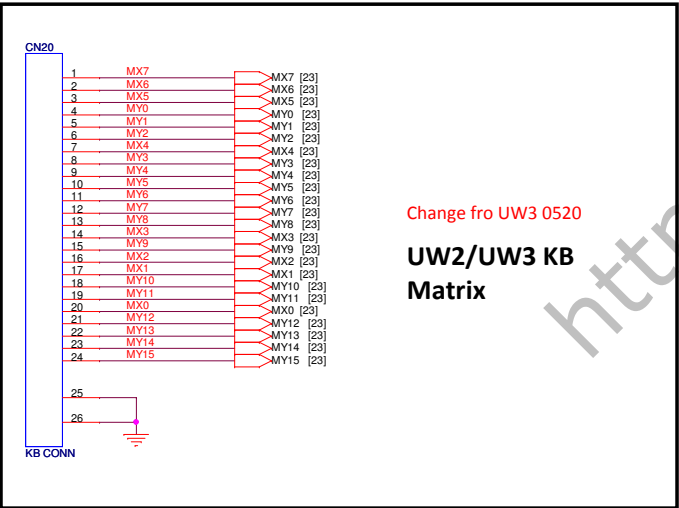




KEYBOARD PULL-UP



SI modify

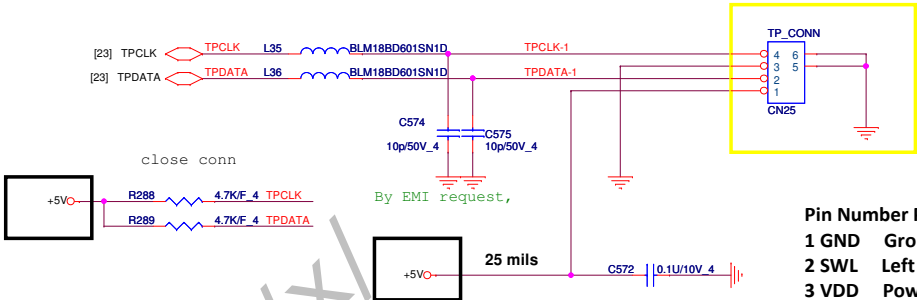


Change fro UW3 0520

UW2/UW3 KB Matrix

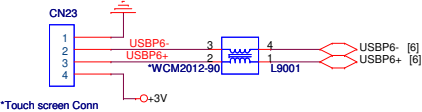
TOUCH PAD CONNECTOR

Change CN25 Pin-define and footprint

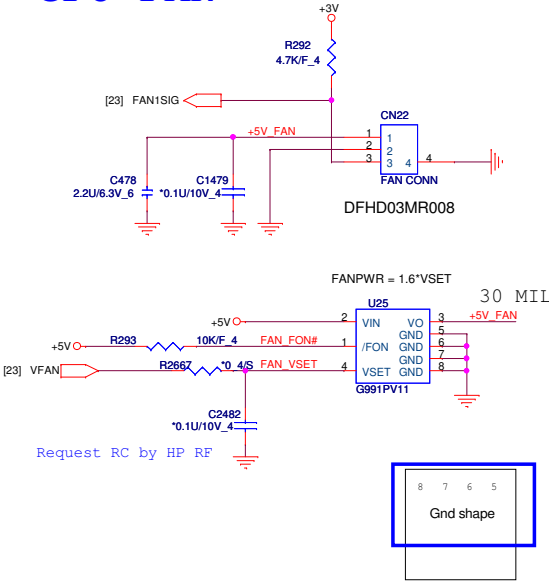


Pin Number	Pin Name	Description
1	GND	Ground Power
2	SWL	Left Button
3	VDD	Power Supply Voltage
4	DATA	Data
5	CLK	Clock
6	SWR	Right Button

TOUCH SCREEN



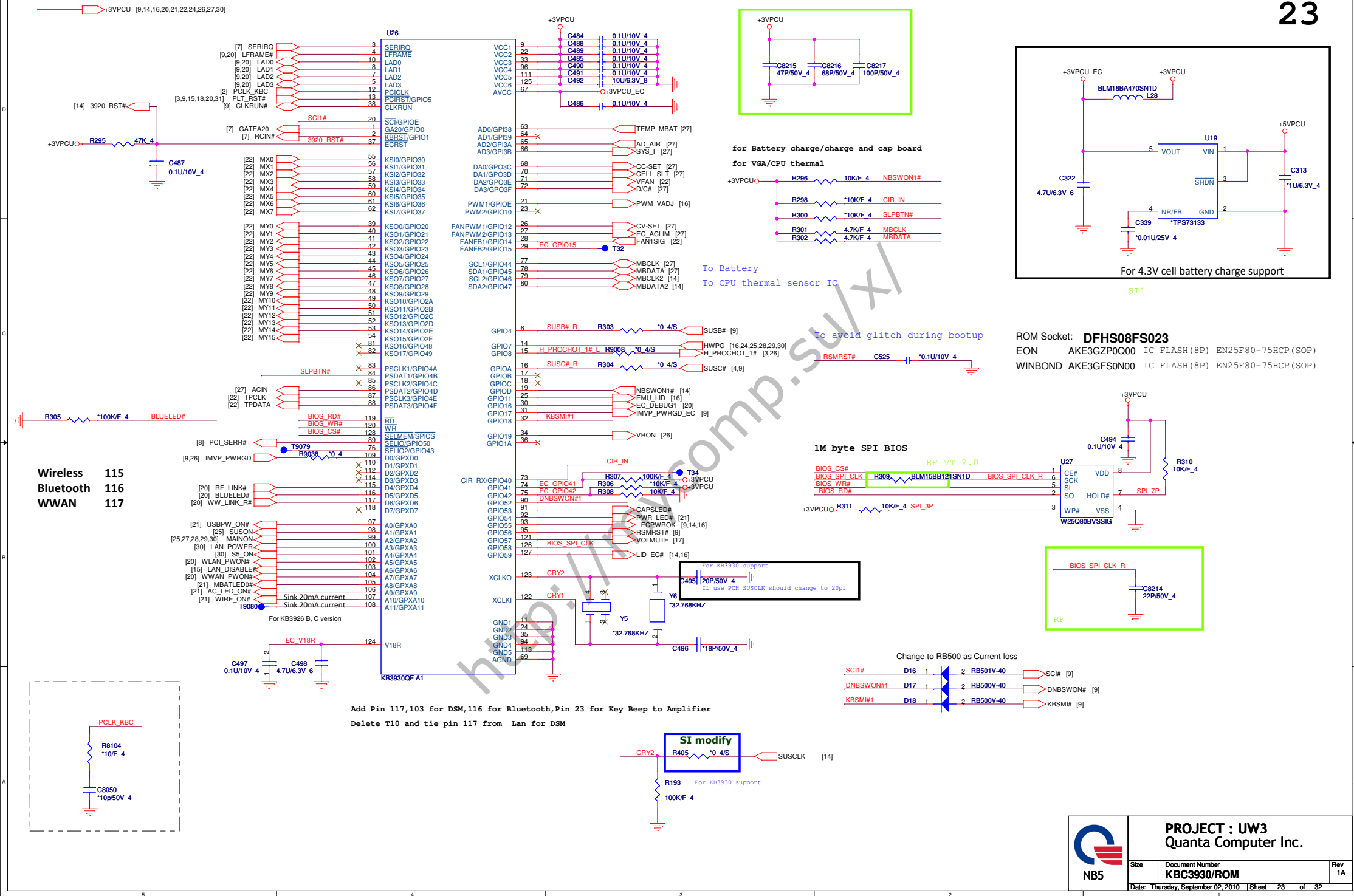
CPU FAN





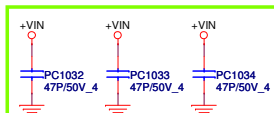
PROJECT : UW3
Quanta Computer Inc.

Size	Document Number	Rev
	KB/TP/BT/CPU FAN/TP SCREEN	1A
Date: Thursday, September 02, 2010 Sheet 22 of 32		

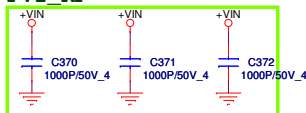


DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

SI2_RF

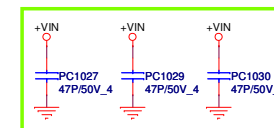


PV1_RF

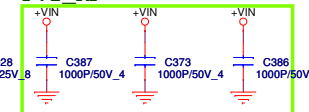


+5VPCU Volt +/- 5%
Continue current:4A
Peak current:5.5A
OCP minimum 6A

SI2_RF

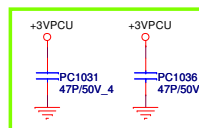


PV1_RF

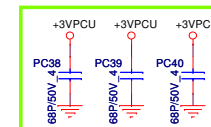


+3VPCU Volt +/- 5%
Continue current:4A
Peak current:5.5A
OCP minimum 6A

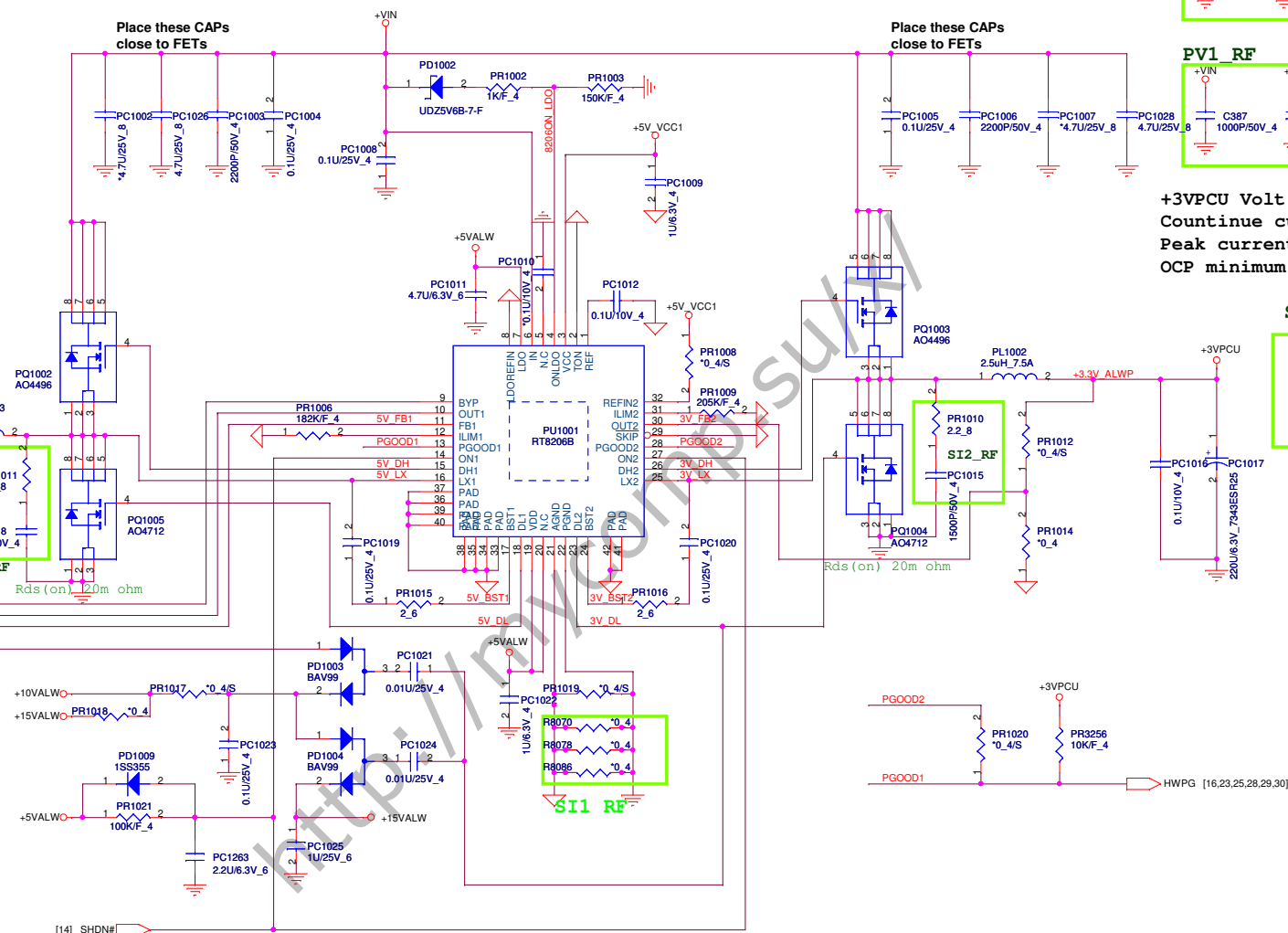
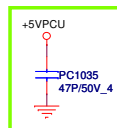
SI2_RF



NM6 1.1 RF
suggestion

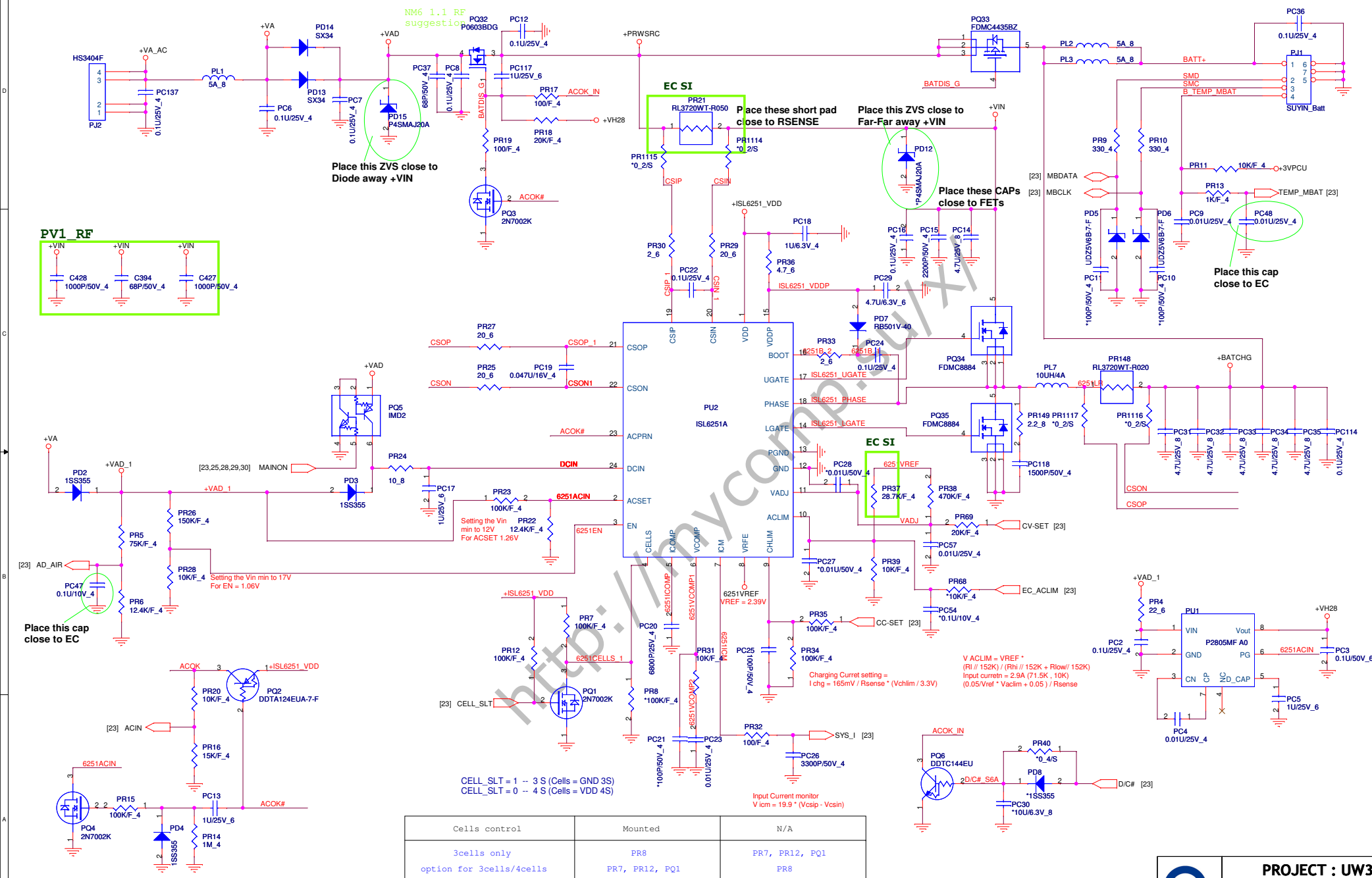


SI2_RF

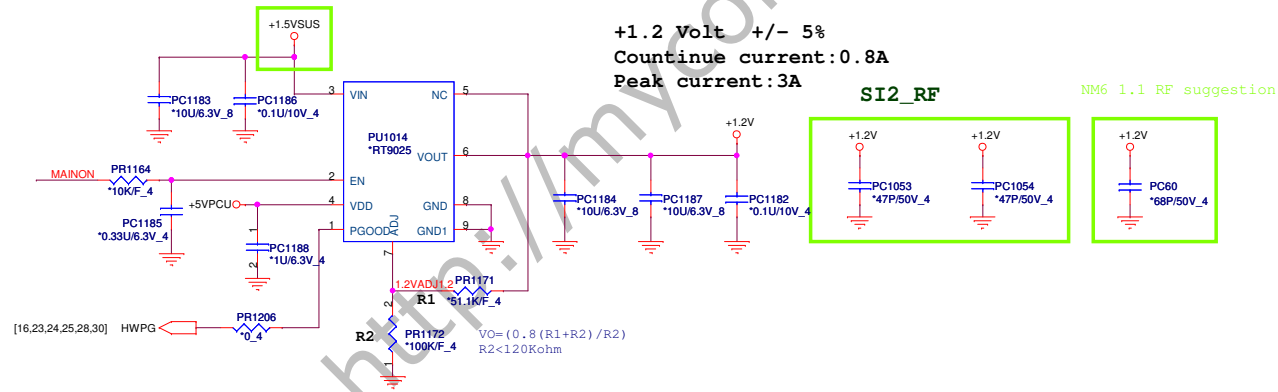
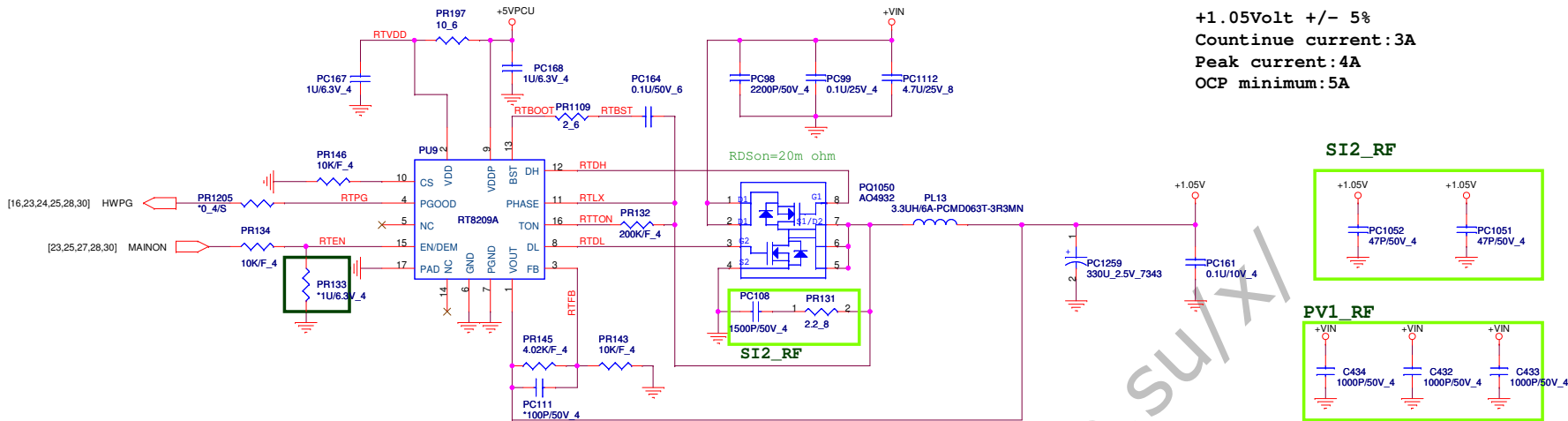


[14] SHDN#

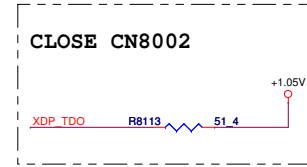
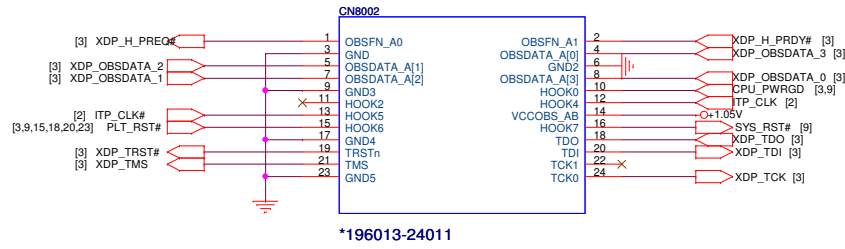




Cells control	Mounted	N/A
3cells only option for 3cells/4cells	PR8 PR7, PR12, PQ1	PR7, PR12, PQ1 PR8



CPU XDP



<http://mycomp.su/xl>

Power up sequence

