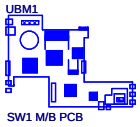

SW1-INTEGRATED GFX

RUN POWER SW PG 41

SYSTEM RESET CIRCUIT PG 41

AC/BATT CONNECTOR PG 36

BATT CHARGER PG 36

Yonah (478 Micro-FCPGA) PG 3,4

533/667 MHz FSB

DC/DC +3VPCU +5VPCU PG 40

1.8V & 0.9V PG 37

CPU VR PG 39

CLOCKS ICS954310 PG 17

Panel Connector PG 18

LVDS

DDR2-SODIMM1 PG 15,16

533/667 MHZ DDR II

DDR2-SODIMM2 PG 15,16

533/667 MHZ DDR II

Calistoga 1466 uFCBGA PG 5,6,7,8,9,10

SDVO

CH7307 PG 19

DVI

DVI Connector PG 19

VGA

CRT Connector PG 20

S-Video

I/O Board Connector PG 28

DMI interface

SATA - HDD PG 20

SATA

PATA HDD/ODD PG 20

IDE

Bluetooth PG 27

USB2.0 (P5)

AC97/Azalia

ICH7-M 652 BGA PG 11,12,13,14

USB2.0 (P2) (EXT Left Side)

USB2.0 (P0,P1) (EXT Right Side)

USB2.0 (P4)

USB PG 26

LAN

88E8036/53 PG 33

RJ45/Magnetics PG 34

33MHz PCI

PCIEx2

USB2.0 (P6,P7)

1394/Card Reader PCI7402 PG 21,22

MINI-PCI (Debug) PG 42

1394

Port Replicator PG 35

AUDIO PG 30,31

MODEM PG 32

LPC

KBC PC97551VPC PG 25

H/P to DOCK PG 31

Audio Jacks PG 31

EXPRESS-CARD MINI-CARD WLAN & WWAN PG 23,24

FWH

PS/2

Flash PG 25

Keyboard S/W&Led PG 28

Touchpad PG 27

USER INTERFACE PG 31

FAN & THERMAL PG 29

PROJECT : SW1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Schematic Block Diagram1	1A

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INDEX

Pg#	Description	DNI LIST
1	Schematic Block Diagram	
2	Front Page	
3-4	Yonah	
5-10	Calistoga	
11-14	ICH7	
15-16	DDRII SO-DIMM(200P)	
17	Clock Generator	
18-21	VGA	
22	LCD Conn. & SSP	
23	CRT Conn	
24	SATA & IDE Conn	
25	PCCARD/Conn & 1394	
26	Express Card & Smart Card	
27	Mini Card	
28	MDC Conn.	
29	SIO (MEC5004)	
30	SIO (MEC5018)	
31	SERIAL PORT & USB	
32	Flash ROM	
33	TP,BT & FIR	
34	Switch,Keyboard & LED	
35	FAN & Thermal	
36-37	Audio CODEC(STAC9200)/Phone Jack	
38-39	LOM (BCM5752)/Switch	
40-41	Docking Conn/Q-Switch	
42	System Reset Circuit	
43-44	Battery Selector & Charger	
45	DDR2_1.8VSUS, 0.9V	
46	1.5VSUS,1.05V(VTT)	
47	CPU Power	
48	D/D Power	
49	RUN Power Switch	
50	VGA DC/DC	
51	DCIN/Batt Conn.	
52	PAD& SCREW	
53	SMBUS BlOCK	

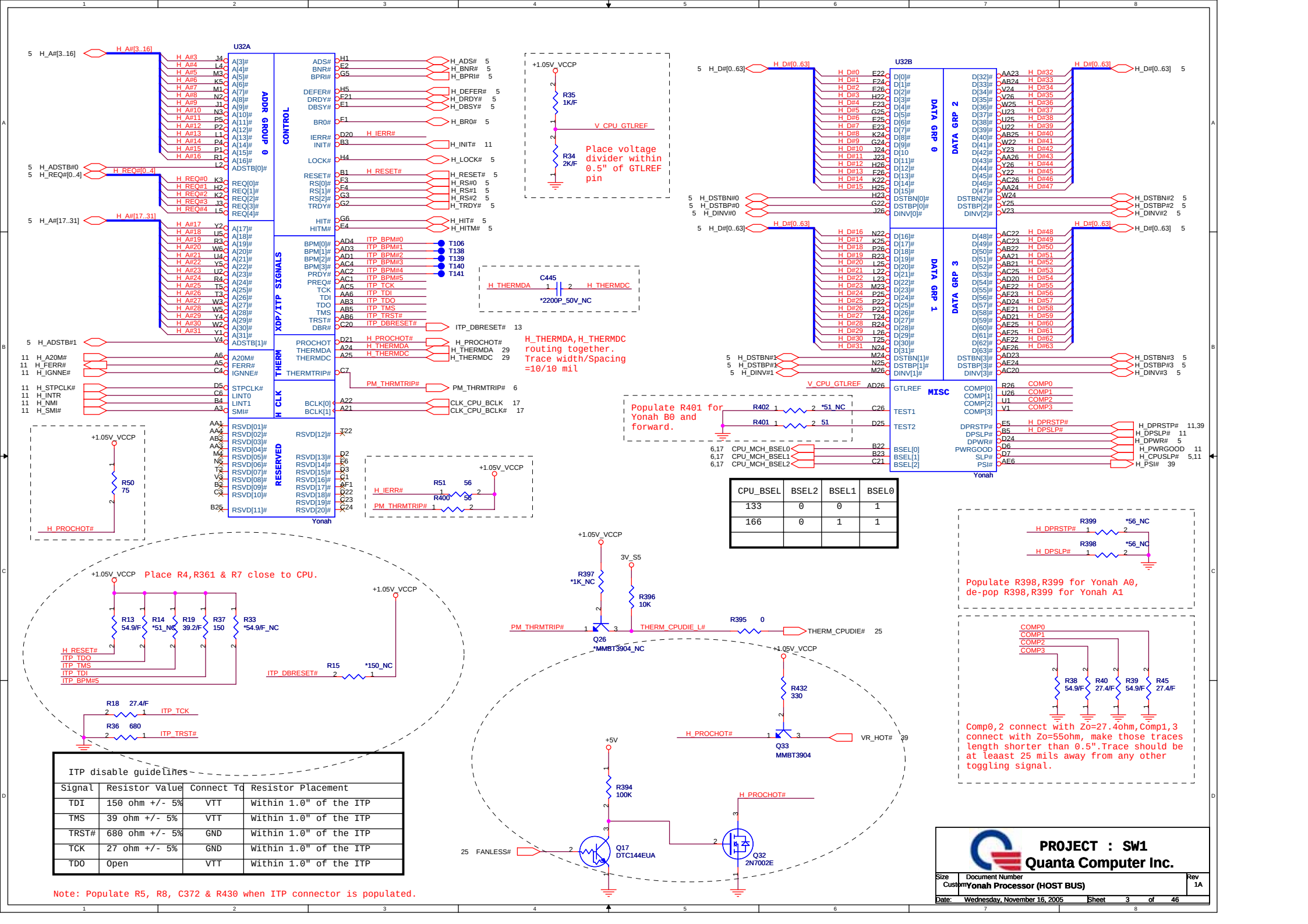
Power & Ground

Label	Pg#	Description	Control Signal
DC_IN+		AC ADAPTER (20V)	
PBATT+		MAIN BATTERY + (10~17V)	
PWR_SRC		MAIN POWER (10~20V)	
RTC_PWR3_3V		RTC & PCL POWER (3_3V)	
+12V		+12V	DRUNPWROK
VHCORE		CPU CORE POWER (1.25/1.15V)	RUNPWROK
V1_2RUN		AGTL+ POWER (1.2V)	RUNPWROK
+3VRUN		SLP_S3# CTRLD POWER	RUN_ON
+3VSUS		SLP_S5# CTRLD POWER	SUS_ON
+5VALW		8051 POWER (5V)	
+5VRUN		SLP_S3# CTRLD POWER	RUN_ON
+5VSUS		SLP_S5# CTRLD POWER	SUS_ON
+5VHDD		HDD POWER (5V)	HDDC_EN#
+5VMOD		MODULE POWER (5V)	MODC_EN#
STRB#/5V		EXTERNAL FDD POWER (5V)	FDD/LPT#
+5VFAN1, +5VFAN2		FAN POWER (5V)	FAN_OFF/ON#
VDDA		AUDIO ANALOG POWER (5V)	RUN_ON
1_8VSUS		RESUME WELL IN ICH	
1_8VRUN		SLP_S3# CTRLD POWER	
+3VALW		8051 POWER (3V)	
V1_5RUN		AGP I/O POWER	
GND	ALL PAGES	DIGITAL GROUND	
GNDP		CPU POWER GND	
CGNDP		CHARGER GND	
DGNDP		DC/DC POWER GND	
LANGND		COMBO CONN GND	

PROJECT : SW1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Index, DNI, Power & Ground	1A

Date: Wednesday, November 16, 2005 Sheet 2 of 46



CPU_BSEL	BSEL2	BSEL1	BSEL0
133	0	0	1
166	0	1	1

ITP disable guidelines

Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 1.0" of the ITP
TMS	39 ohm +/- 5%	VTT	Within 1.0" of the ITP
TRST#	680 ohm +/- 5%	GND	Within 1.0" of the ITP
TCK	27 ohm +/- 5%	GND	Within 1.0" of the ITP
TDO	Open	VTT	Within 1.0" of the ITP

Note: Populate R5, R8, C372 & R430 when ITP connector is populated.

PROJECT : SW1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Yonah Processor (HOST BUS)	1A
Date: Wednesday, November 16, 2005	Sheet 3 of 46	

All use 22U 4V(+-20%,X6S,0805)Pb-Free.

+VCC_CORE
C459 22U_4V
C458 22U_4V
C457 22U_4V
C72 22U_4V
C73 22U_4V

+VCC_CORE
C456 22U_4V
C455 22U_4V
C454 22U_4V
C71 22U_4V
C452 22U_4V

+VCC_CORE
C67 22U_4V
C451 22U_4V
C70 22U_4V
C69 22U_4V
C68 22U_4V

+VCC_CORE
C89 22U_4V
C88 22U_4V
C447 22U_4V
C58 22U_4V
C86 22U_4V

+VCC_CORE
C92 22U_4V
C91 22U_4V
C59 22U_4V
C90 22U_4V
C87 22U_4V

+VCC_CORE
C448 22U_4V
C450 22U_4V
C74 22U_4V
C97 22U_4V
C96 22U_4V

+VCC_CORE
C449 22U_4V
C93 22U_4V

8 inside cavity, north side, secondary layer.
8 inside cavity, south side, secondary layer.
6 inside cavity, north side, primary layer.
6 inside cavity, south side, primary layer.

+1.05V_VCCP
C77 0.1U_10V
C81 0.1U_10V
C82 0.1U_10V
C76 0.1U_10V
C78 0.1U_10V
C80 0.1U_10V

Total caps = 2633 uF.
ESR = 15m ohm/5 // 5m ohm/25 // 5m ohm/15.
Place these inside socket cavity on North side secondary.

+VCC_CORE

U32C

A7	VCC[001]	VCC[068]	AB20		
A9	VCC[002]	VCC[069]	AB7		
A10	VCC[003]	VCC[070]	AC7		
A12	VCC[004]	VCC[071]	AC9		
A13	VCC[005]	VCC[072]	AC12		
A15	VCC[006]	VCC[073]	AC13		
A17	VCC[007]	VCC[074]	AC15		
A18	VCC[008]	VCC[075]	AC17		
A20	VCC[009]	VCC[076]	AC18		
B7	VCC[010]	VCC[077]	AD7		
B9	VCC[011]	VCC[078]	AD9		
B10	VCC[012]	VCC[079]	AD10		
B12	VCC[013]	VCC[080]	AD12		
B14	VCC[014]	VCC[081]	AD14		
B15	VCC[015]	VCC[082]	AD15		
B17	VCC[016]	VCC[083]	AD17		
B18	VCC[017]	VCC[084]	AD18		
B20	VCC[018]	VCC[085]	AE9		
C9	VCC[019]	VCC[086]	AE10		
C10	VCC[020]	VCC[087]	AE12		
C12	VCC[021]	VCC[088]	AE13		
C13	VCC[022]	VCC[089]	AE15		
C15	VCC[023]	VCC[090]	AE17		
C17	VCC[024]	VCC[091]	AE18		
C18	VCC[025]	VCC[092]	AE20		
D9	VCC[026]	VCC[093]	AE9		
D10	VCC[027]	VCC[094]	AE10		
D12	VCC[028]	VCC[095]	AE12		
D14	VCC[029]	VCC[096]	AE14		
D15	VCC[030]	VCC[097]	AE15		
D17	VCC[031]	VCC[098]	AE17		
D18	VCC[032]	VCC[099]	AE18		
E7	VCC[033]	VCC[100]	AE20		
E9	VCC[034]				
E10	VCC[035]	VCCP[01]	V6		
E12	VCC[036]	VCCP[02]	G21		
E13	VCC[037]	VCCP[03]	J6		
E15	VCC[038]	VCCP[04]	K6		
E17	VCC[039]	VCCP[05]	M6		
E18	VCC[040]	VCCP[06]	J21		
E20	VCC[041]	VCCP[07]	K21		
F7	VCC[042]	VCCP[08]	M21		
F9	VCC[043]	VCCP[09]	N21		
F10	VCC[044]	VCCP[10]	N6		
F12	VCC[045]	VCCP[11]	R21		
F14	VCC[046]	VCCP[12]	R6		
F15	VCC[047]	VCCP[13]	T21		
F17	VCC[048]	VCCP[14]	T6		
F18	VCC[049]	VCCP[15]	V21		
F20	VCC[050]	VCCP[16]	W21		
AA7	VCC[051]				
AA9	VCC[052]	VCCA	B26		
AA10	VCC[053]				
AA12	VCC[054]				
AA13	VCC[055]	VID[0]	AD6	VID0	39
AA15	VCC[056]	VID[1]	AE5	VID1	39
AA17	VCC[057]	VID[2]	AE5	VID2	39
AA18	VCC[058]	VID[3]	AF4	VID3	39
AA20	VCC[059]	VID[4]	AE3	VID4	39
AB9	VCC[060]	VID[5]	AF2	VID5	39
AC10	VCC[061]	VID[6]	AE2	VID6	39
AB10	VCC[062]				
AB12	VCC[063]				
AB14	VCC[064]				
AB15	VCC[065]	VCCSENSE	AF7	VCCSENSE	39
AB17	VCC[066]				
AB18	VCC[067]	VSSSENSE	AF7	VSSSENSE	39

Yonah

+VCC_CORE

+1.05V_VCCP
C84 +270U_2V_NC

Place C27 near PIN B26

+1.5V_RUN
C444 0.01U_25V
C446 10U_4V

Route VCCSENSE and VSSSENSE traces at 27.4ohms with 7mil spacing and 25mil away from any other signals. Place PU and PD within 2 inch of CPU.

+VCC_CORE
R429 100/F
VCCSENSE
VSSSENSE
R428 100/F

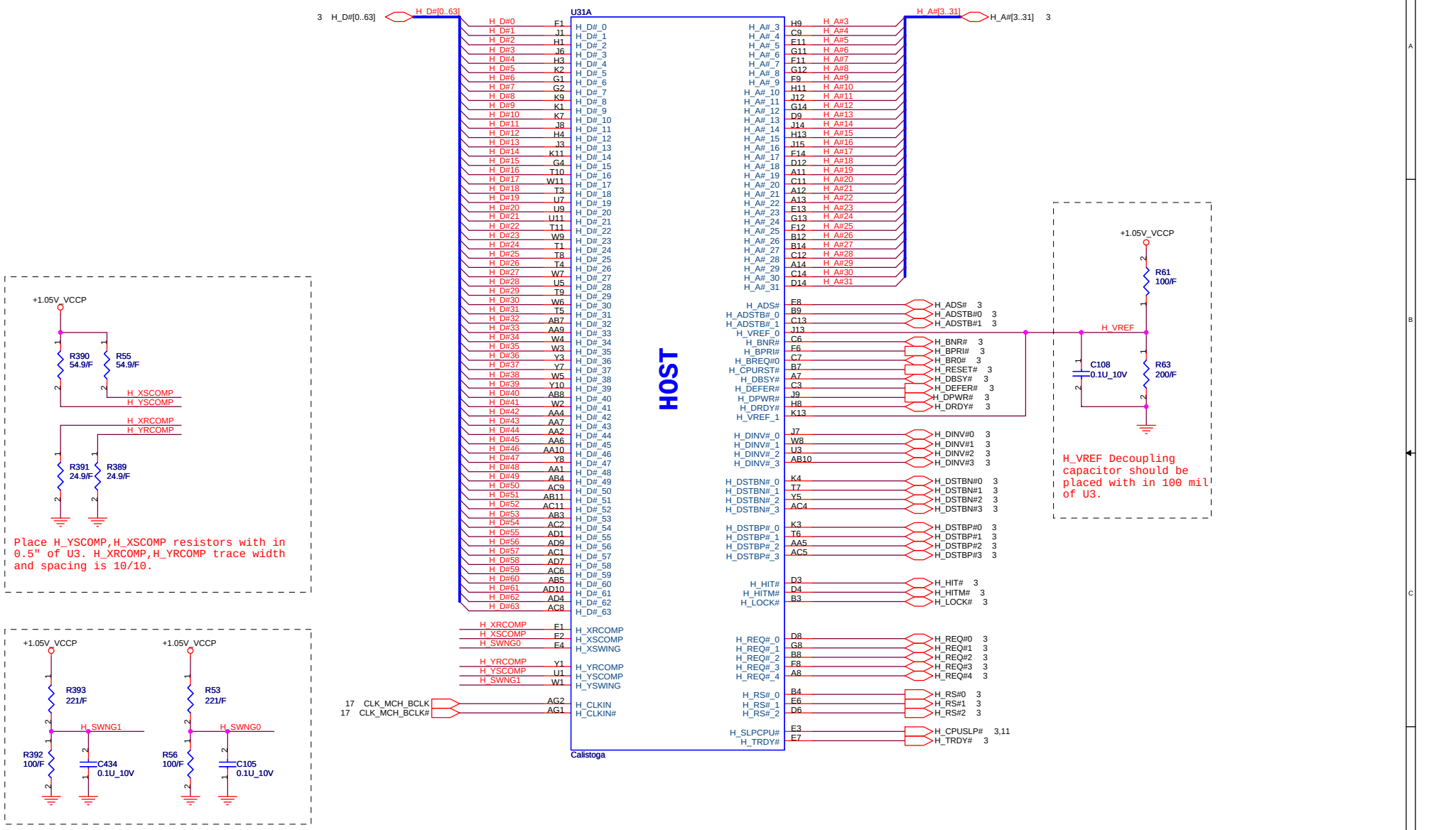
U32D

A4	VSS[001]	VSS[082]	P6
A8	VSS[002]	VSS[083]	P21
A11	VSS[003]	VSS[084]	P24
A14	VSS[004]	VSS[085]	R2
A16	VSS[005]	VSS[086]	R5
A19	VSS[006]	VSS[087]	R22
A23	VSS[007]	VSS[088]	R25
A26	VSS[008]	VSS[089]	T1
B6	VSS[009]	VSS[090]	T4
B8	VSS[010]	VSS[091]	T23
B11	VSS[011]	VSS[092]	T26
B13	VSS[012]	VSS[093]	U3
B16	VSS[013]	VSS[094]	U6
B19	VSS[014]	VSS[095]	U21
B21	VSS[015]	VSS[096]	U24
B24	VSS[016]	VSS[097]	V2
C5	VSS[017]	VSS[098]	V5
C8	VSS[018]	VSS[099]	V22
C11	VSS[019]	VSS[100]	V25
C14	VSS[020]	VSS[101]	W1
C16	VSS[021]	VSS[102]	W4
C19	VSS[022]	VSS[103]	W23
C2	VSS[023]	VSS[104]	W26
C22	VSS[024]	VSS[105]	Y3
C25	VSS[025]	VSS[106]	Y6
D1	VSS[026]	VSS[107]	Y21
D4	VSS[027]	VSS[108]	Y24
D8	VSS[028]	VSS[109]	AA2
D11	VSS[029]	VSS[110]	AA5
D13	VSS[030]	VSS[111]	AA8
D16	VSS[031]	VSS[112]	AA11
D19	VSS[032]	VSS[113]	AA14
D23	VSS[033]	VSS[114]	AA16
D26	VSS[034]	VSS[115]	AA19
E3	VSS[035]	VSS[116]	AA22
E6	VSS[036]	VSS[117]	AA25
E8	VSS[037]	VSS[118]	AB1
E11	VSS[038]	VSS[119]	AB4
E14	VSS[039]	VSS[120]	AB8
E16	VSS[040]	VSS[121]	AB11
E19	VSS[041]	VSS[122]	AB13
F21	VSS[042]	VSS[123]	AB16
F24	VSS[043]	VSS[124]	AB19
F5	VSS[044]	VSS[125]	AB23
F8	VSS[045]	VSS[126]	AB26
F11	VSS[046]	VSS[127]	AC3
F13	VSS[047]	VSS[128]	AC6
F16	VSS[048]	VSS[129]	AC8
F19	VSS[049]	VSS[130]	AC11
F2	VSS[050]	VSS[131]	AC14
F22	VSS[051]	VSS[132]	AC16
F25	VSS[052]	VSS[133]	AC19
G4	VSS[053]	VSS[134]	AC21
G1	VSS[054]	VSS[135]	AC24
G23	VSS[055]	VSS[136]	AD2
G26	VSS[056]	VSS[137]	AD5
H3	VSS[057]	VSS[138]	AD8
H6	VSS[058]	VSS[139]	AD11
H21	VSS[059]	VSS[140]	AD13
H24	VSS[060]	VSS[141]	AD16
J2	VSS[061]	VSS[142]	AD19
J5	VSS[062]	VSS[143]	AD22
J22	VSS[063]	VSS[144]	AD25
J25	VSS[064]	VSS[145]	AE1
K1	VSS[065]	VSS[146]	AE4
K4	VSS[066]	VSS[147]	AE8
K23	VSS[067]	VSS[148]	AE11
K26	VSS[068]	VSS[149]	AE14
L3	VSS[069]	VSS[150]	AE16
L6	VSS[070]	VSS[151]	AE19
L21	VSS[071]	VSS[152]	AE23
L24	VSS[072]	VSS[153]	AE26
M2	VSS[073]	VSS[154]	AF3
M5	VSS[074]	VSS[155]	AF6
M22	VSS[075]	VSS[156]	AF8
M25	VSS[076]	VSS[157]	AF11
N1	VSS[077]	VSS[158]	AF13
N4	VSS[078]	VSS[159]	AF16
N23	VSS[079]	VSS[160]	AF19
N26	VSS[080]	VSS[161]	AF21
P3	VSS[081]	VSS[162]	AF24

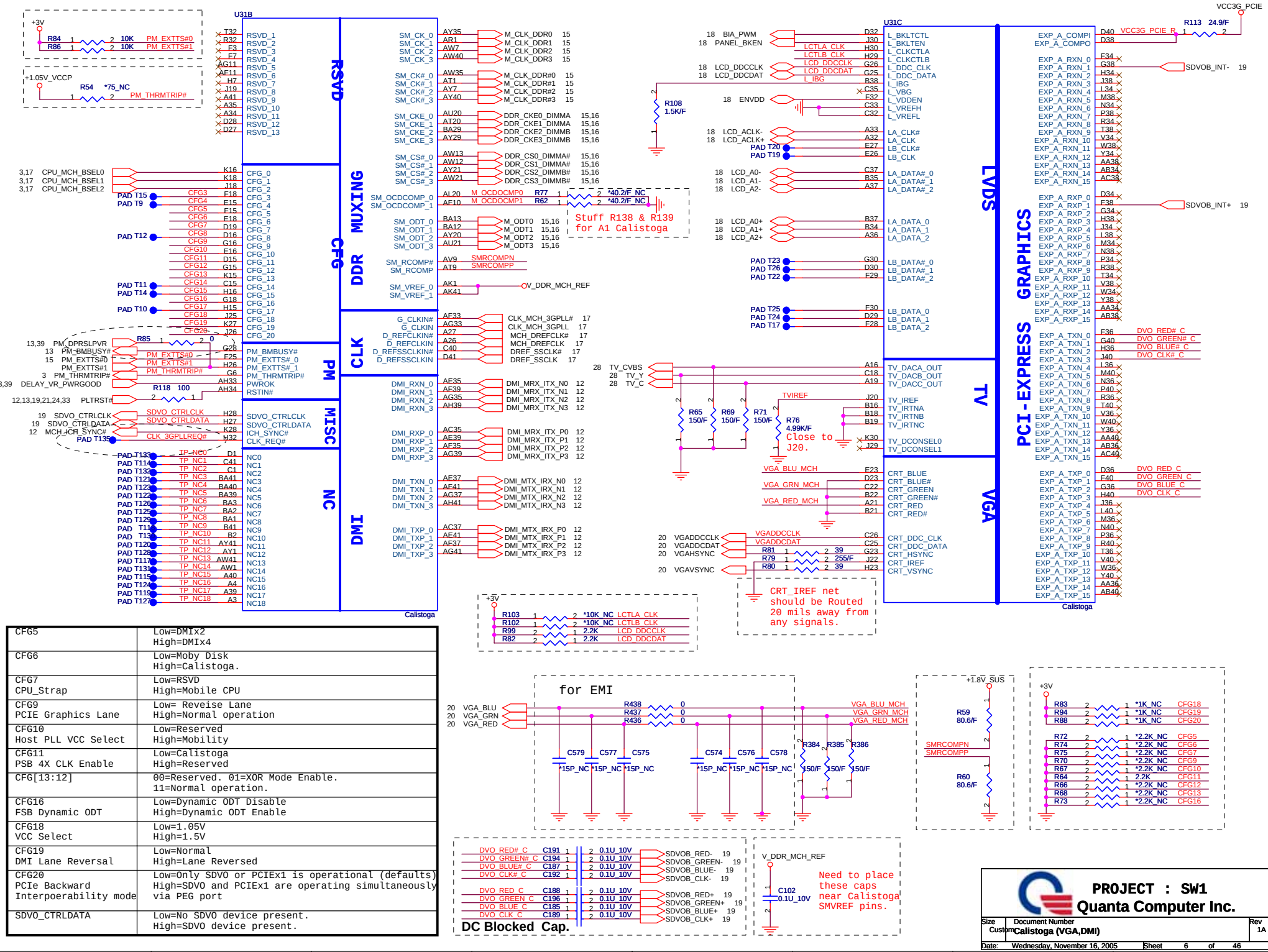
Yonah

PROJECT : SW1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Yonah Processor (POWER)	1A
Date: Wednesday, November 16, 2005	Sheet 4 of 46	



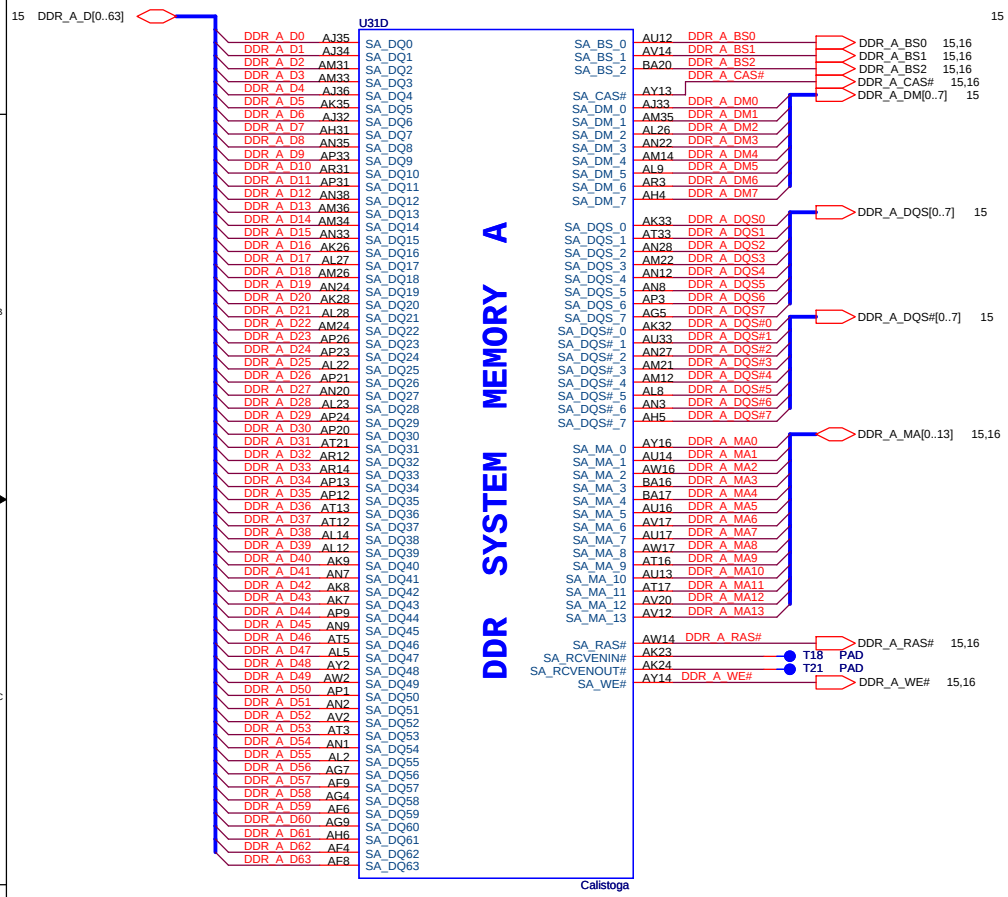
PROJECT : SW1		
Quanta Computer Inc.		
Size: Custom	Document Number: Calistoga (HOST)	Rev: 1A
Date: Wednesday, November 16, 2005	Sheet 5 of 46	

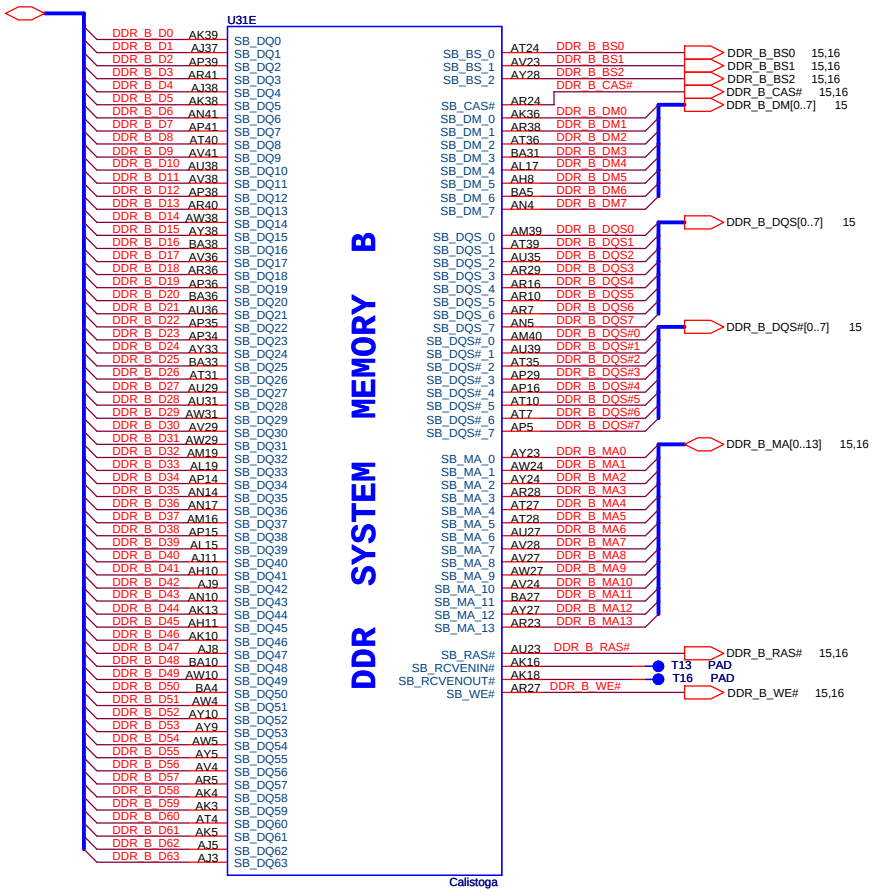


CFG5	Low=DMIx2 High=DMIx4
CFG6	Low=Moby Disk High=Calistoga.
CFG7 CPU_Strap	Low=RSVD High=Mobile CPU
CFG9 PCIE Graphics Lane	Low= Reveise Lane High=Normal operation
CFG10 Host PLL VCC Select	Low=Reserved High=Mobility
CFG11 PSB 4X CLK Enable	Low=Calistoga High=Reserved
CFG[13:12]	00=Reserved. 01=XOR Mode Enable. 11=Normal operation.
CFG16 FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable
CFG18 VCC Select	Low=1.05V High=1.5V
CFG19 DMI Lane Reversal	Low=Normal High=Lane Reversed
CFG20 PCIe Backward Interpoerability mode	Low=Only SDVO or PCIEx1 is operational (defaults) High=SDVO and PCIEx1 are operating simultaneously via PEG port
SDVO_CTRLDATA	Low=No SDVO device present. High=SDVO device present.

PROJECT : SW1
Quanta Computer Inc.

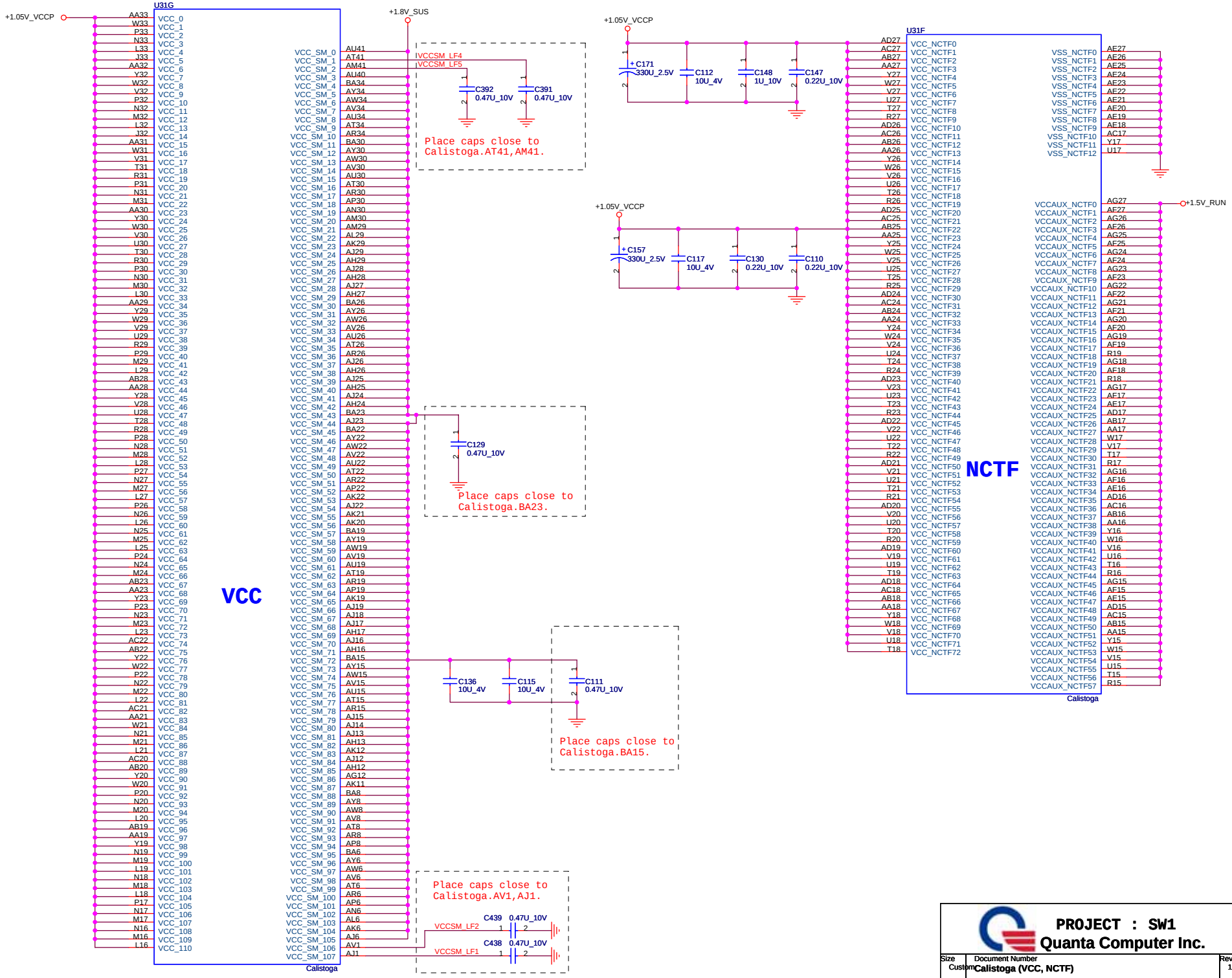
Size	Document Number	Rev
Custom	Calistoga (VGA,DMI)	1A
Date: Wednesday, November 16, 2005	Sheet 6 of 46	





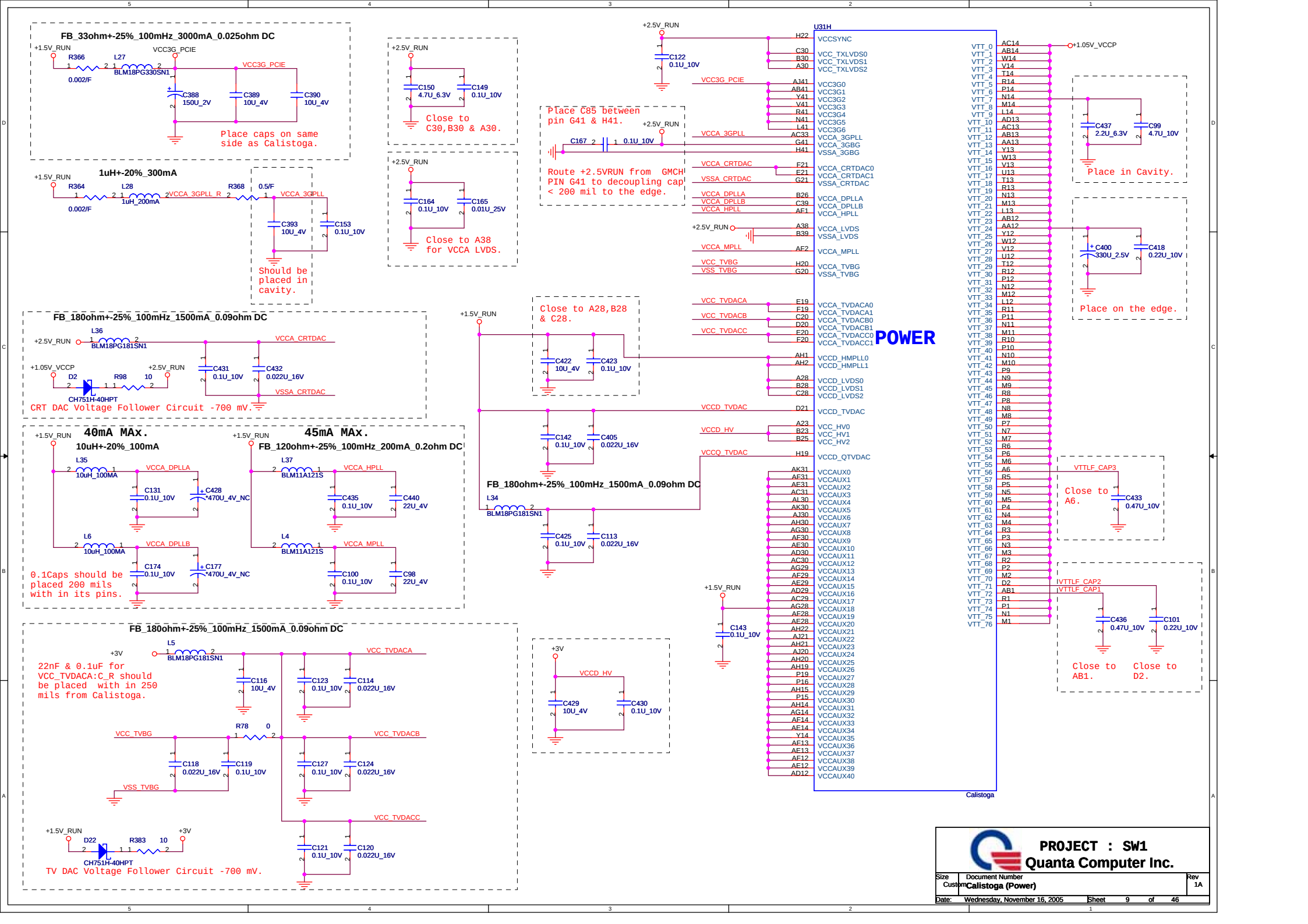
PROJECT : SW1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Calistoga (DDR2)	1A
Date: Wednesday, November 16, 2005	Sheet 7 of 46	



PROJECT : SW1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Calistoga (VCC, NCTF)	1A
Date: Wednesday, November 16, 2005	Sheet 8 of 46	


FB_33ohm+-25%_100mHz_3000mA_0.025ohm DC
+1.5V_RUN
R366
0.002/F
L27
BLM18PG330SN1
VCC3G_PCIE
C388
150U_2V
C389
10U_4V
C390
10U_4V
Place caps on same side as Calistoga.
+2.5V_RUN
C150
4.7U_6.3V
C149
0.1U_10V
Close to C30,B30 & A30.
+2.5V_RUN
C164
0.1U_10V
C165
0.01U_25V
Close to A38 for VCCA LVDS.
1uH+-20%_300mA
+1.5V_RUN
R364
0.002/F
L28
1uH_200mA
VCCA_3GPLL_R
R368
0.5/F
VCCA_3GPLL
C393
10U_4V
C153
0.1U_10V
Should be placed in cavity.
FB_180ohm+-25%_100mHz_1500mA_0.09ohm DC
+2.5V_RUN
L36
BLM18PG181SN1
VCCA_CRTDAC
+1.05V_VCCP
D2
CH751H-40HPT
R98
10
+2.5V_RUN
C431
0.1U_10V
C432
0.022U_16V
VSSA_CRTDAC
CRT DAC Voltage Follower Circuit -700 mV.
40mA MAx.
10uH+-20%_100mA
+1.5V_RUN
L35
10uH_100MA
VCCA_DPLLA
C131
0.1U_10V
C428
*470U_4V_NC
L6
10uH_100MA
VCCA_DPLLB
C174
0.1U_10V
C177
*470U_4V_NC
45mA MAx.
FB_120ohm+-25%_100mHz_200mA_0.2ohm DC
+1.5V_RUN
L37
BLM11A121S
VCCA_HPLL
C435
0.1U_10V
C440
22U_4V
L4
BLM11A121S
VCCA_MPLL
C100
0.1U_10V
C98
22U_4V
0.1Caps should be placed 200 mils with in its pins.
FB_180ohm+-25%_100mHz_1500mA_0.09ohm DC
+3V
L5
BLM18PG181SN1
VCC_TVDACA
22nF & 0.1uF for VCC_TVDACA:C_R should be placed with in 250 mils from Calistoga.
C116
10U_4V
C123
0.1U_10V
C114
0.022U_16V
VCC_TVBG
R78
0
VCC_TVDACB
C118
0.022U_16V
C119
0.1U_10V
VSS_TVBG
C127
0.1U_10V
C124
0.022U_16V
VCC_TVDACC
+1.5V_RUN
D22
CH751H-40HPT
R383
10
+3V
C121
0.1U_10V
C120
0.022U_16V
TV DAC Voltage Follower Circuit -700 mV.
+2.5V_RUN
C122
0.1U_10V
Place C85 between pin G41 & H41.
+2.5V_RUN
C167
0.1U_10V
Route +2.5VRUN from GMCH PIN G41 to decoupling cap < 200 mil to the edge.
+1.5V_RUN
Close to A28,B28 & C28.
C422
10U_4V
C423
0.1U_10V
C142
0.1U_10V
C405
0.022U_16V
FB_180ohm+-25%_100mHz_1500mA_0.09ohm DC
L34
BLM18PG181SN1
C425
0.1U_10V
C113
0.022U_16V
+1.5V_RUN
C143
0.1U_10V
+3V
VCCD_HV
C429
10U_4V
C430
0.1U_10V
U31H
VCCSYNC
VCC_TXLVDS0
VCC_TXLVDS1
VCC_TXLVDS2
VCC3G0
VCC3G1
VCC3G2
VCC3G3
VCC3G4
VCC3G5
VCC3G6
VCCA_3GPLL
VCCA_3GBG
VSSA_3GBG
VCCA_CRTDAC0
VCCA_CRTDAC1
VSSA_CRTDAC
VCCA_DPLLA
VCCA_DPLLB
VCCA_HPLL
VCCA_LVDS
VSSA_LVDS
VCCA_MPLL
VCC_TVBG
VSS_TVBG
VCCA_TVDACA0
VCCA_TVDACA1
VCCA_TVDACB0
VCCA_TVDACB1
VCCA_TVDACC0
VCCA_TVDACC1
VCCD_HMPLL0
VCCD_HMPLL1
VCCD_LVDS0
VCCD_LVDS1
VCCD_LVDS2
VCCD_TVDAC
VCC_HV0
VCC_HV1
VCC_HV2
VCCD_QTVDAC
VCCAUX0
VCCAUX1
VCCAUX2
VCCAUX3
VCCAUX4
VCCAUX5
VCCAUX6
VCCAUX7
VCCAUX8
VCCAUX9
VCCAUX10
VCCAUX11
VCCAUX12
VCCAUX13
VCCAUX14
VCCAUX15
VCCAUX16
VCCAUX17
VCCAUX18
VCCAUX19
VCCAUX20
VCCAUX21
VCCAUX22
VCCAUX23
VCCAUX24
VCCAUX25
VCCAUX26
VCCAUX27
VCCAUX28
VCCAUX29
VCCAUX30
VCCAUX31
VCCAUX32
VCCAUX33
VCCAUX34
VCCAUX35
VCCAUX36
VCCAUX37
VCCAUX38
VCCAUX39
VCCAUX40
Calistoga
POWER
+1.05V_VCCP
C437
2.2U_6.3V
C99
4.7U_10V
Place in Cavity.
C400
330U_2.5V
C418
0.22U_10V
Place on the edge.
VTTLF_CAP3
Close to A6.
C433
0.47U_10V
VTTLF_CAP2
VTTLF_CAP1
C436
0.47U_10V
C101
0.22U_10V
Close to AB1.
Close to D2.
PROJECT : SW1
Quanta Computer Inc.
Size
Custom
Document Number
Calistoga (Power)
Rev
1A
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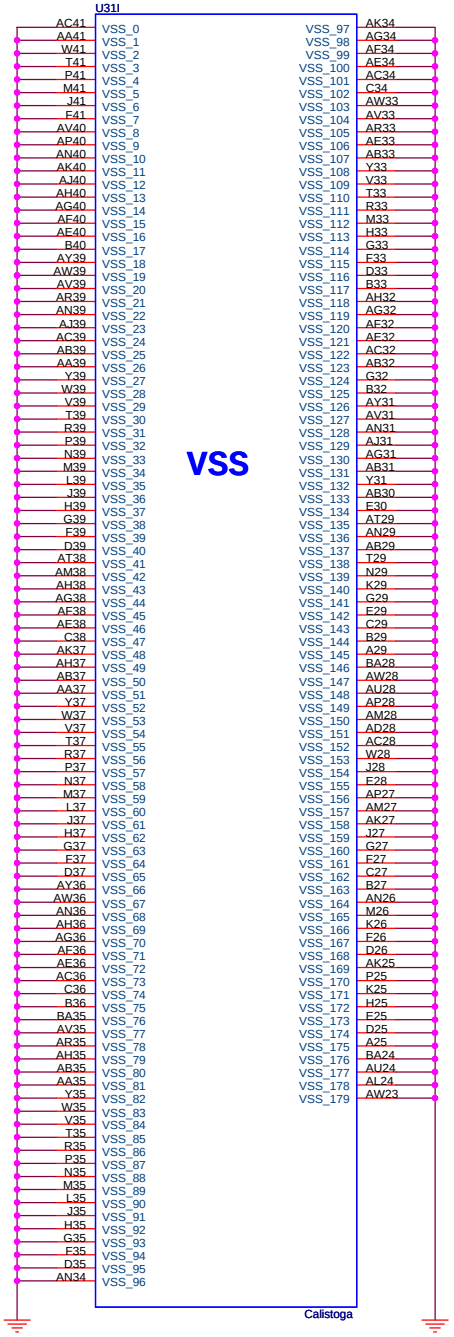

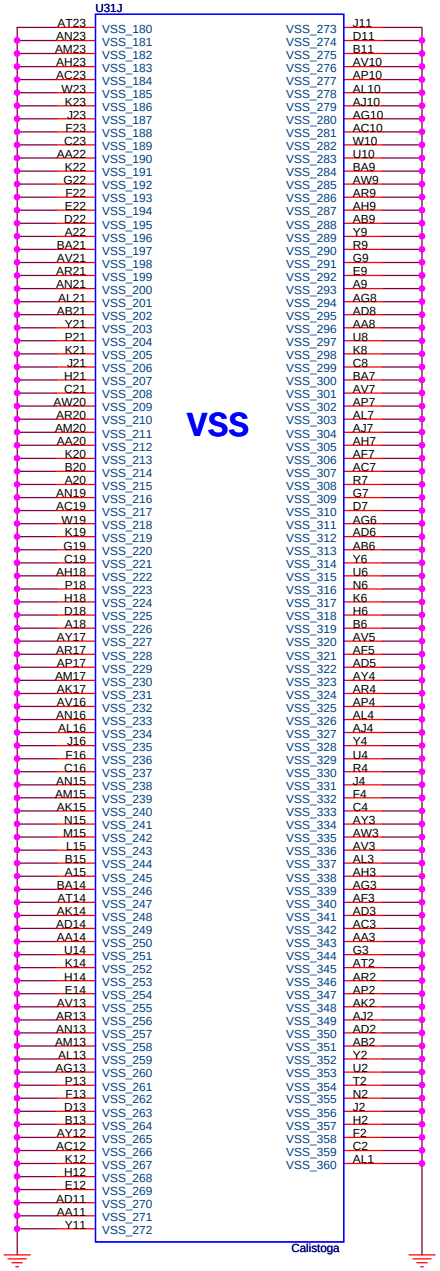

PROJECT : SW1
Quanta Computer Inc.

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Custom	Calistoga (VSS)	1A
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RTC

Pop R123 & no pop R125
to enable internal VR.

32.768KHZ R365 10M W1 ICH_RTCX1 ICH_RTCX2 C381 15P_50V 32.768KHZ C383 15P_50V

3VPCU D3 CH500H-40 +RTC_CELL VCCRTC_2 D4 CH500H-40 R111 1K C178 1U_10V R126 1M R123 332K/F R128 20K +COINCELL BT1 BAT_CONN R125 *0_NC C181 1U_10V

5VPCU 20MIL 20MIL R109 1.2K VCCRTC_1 R110 1K VCCRTC_3 Q8 MMBT3904 R107 4.7K R105 15K

U30A

RTC: RTXC1 RTXC2 RTCRST# INTRUDER# INTVRMEN

LPC: LAD0 LAD1 LAD2 LAD3 LDRQ0# LDRQ1#/GPIO23 LFRAME#

LAN: EE_CS EE_SHCLK EE_DOUT EE_DIN LAN_CLK LAN_RSTSYNC LAN_RXD0 LAN_RXD1 LAN_RXD2 LAN_TXD0 LAN_TXD1 LAN_TXD2

CPU: A20GATE A20M# CPUSLP# TP1/DPRSTP# TP2/DPSLP# FERR# GPIO49/CPUPWRGD IGNNE# INIT3_3V# INIT# INTR RCIN# NMI SMI# STPCLK# THERMTRIP#

AC-97/AZALIA: ACZ_BIT_CLK ACZ_SYNC ACZ_RST# ACZ_SDIN0 ACZ_SDIN1 ACZ_SDIN2 ACZ_SDOUT

SATA: SATALED# SATA0RXN SATA0RXP SATA0TXN SATA0TXP SATA2RXN SATA2RXP SATA2TXN SATA2TXP SATA_CLKN SATA_CLKP SATARBIASN SATARBIASP

IDE: DD0 DD1 DD2 DD3 DD4 DD5 DD6 DD7 DD8 DD9 DD10 DD11 DD12 DD13 DD14 DD15 DIOR# DIOW# DDACK# IDEIRQ IORDY DDREQ DA0 DA1 DA2 DCS1# DCS3#

ICH7-M

T36 PAD T43 PAD T48 PAD T47 PAD T50 PAD T41 PAD T34 PAD T39 PAD T44 PAD T109 PAD

30 ICH_AZ_CODEC_SDIN0

21 SATA_TX0- C396 3900P_25V SATA_TX0- C
21 SATA_TX0+ C395 3900P_25V SATA_TX0+ C

Distance between the ICH-7 M and cap on the "P" signal should be identical distance between the ICH-6 M and cap on the "N" signal for same pair.

21 SATA_RX0- 21 SATA_RX0+ SATA_TX0- C SATA_TX0+ C

28 SATA_LED#

17 CLK_PCIE_SATA# 17 CLK_PCIE_SATA

Place within 500mils of ICH7 ball

R379 24.9/F SATABIAS

21 IDE_DIOR# 21 IDE_DIOW# 21 IDE_DDACK# 21 IDE_IRQ 21 IDE_IORDY 21 IDE_DDREQ

R378 8.2K +3V

LAD0/FWH0 24,25 LAD1/FWH1 24,25 LAD2/FWH2 24,25 LAD3/FWH3 24,25

LDRQ#0 25 (T37) LFRAME#/FWH4 24,25

GATEA20 25 H_A20M# 3

R369 *0_NC H_CPUSLP# 3,5

R131 0 H_DPRSTP# 3,39 R370 0 H_DPSLP# 3

H_FERR# 3

H_PWRGOOD 3

H_IGNNE# 3 H_INIT# 3 H_INTR 3

RCIN# 25

H_NMI 3 R132 0 H_SMI# 3

H_STPCLK# 3

THERMTRIP# ICH

IDE_DD[0..15] IDE_DD[0..15] 21

IDE_DA0 21 IDE_DA1 21 IDE_DA2 21

IDE_DCS1# 21 IDE_DCS3# 21

+3V R133 10K R371 10K GATEA20 RCIN#

+1.05V_VCCP R129 56 R124 *56_NC R122 *56_NC H_FERR# H_DPRSTP# H_DPSLP#

Depop R369 if the MCH is driving CPUSLP# to the CPU. Place the resistors from ICH & MCH close together minimize stubs for either pop option.

+1.05V_VCCP R130 56 THERMTRIP# ICH C179 *0.1U_10V_NC

R130 & C179 should be placed as close as possable to ICH ball.

30 ICH_AZ_CODEC_BITCLK R145 33 ACZ_BIT_CLK C205 *27P_50V_NC

30 ICH_AZ_CODEC_SYNC R161 33 ACZ_SYNC
30 ICH_AZ_CODEC_RST# R158 33 ACZ_RST#
30 ICH_AZ_CODEC_SDOUT R157 33 ACZ_SDOUT

PROJECT : SW1
Quanta Computer Inc.

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Custom	ICH7-M (CPU,IDE,SATA,LPC,AC97)	1A

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Place TX DC blocking caps close ICH7.

24	PCIE_TX1-	C240	0.1U_10V	PCIE_TXN1_C	
24	PCIE_TX1+	C237	0.1U_10V	PCIE_TXP1_C	
24	PCIE_TX2-	C234	0.1U_10V	PCIE_TXN2_C	
24	PCIE_TX2+	C229	0.1U_10V	PCIE_TXP2_C	
33	PCIE_TX3-	C223	0.1U_10V	PCIE_TXN3_C	
33	PCIE_TX3+	C217	0.1U_10V	PCIE_TXP3_C	

Express Card

MiniWLAN

82573 GLAN

U30D

PCI-Express / Direct Media Interface

24	PCIE_RX1-	F26	PERn1	DMI0RXN	V26
24	PCIE_RX1+	F25	PERp1	DMI0RXP	V25
	PCIE_TXN1_C	E28	PETn1	DMI0TXN	U28
	PCIE_TXP1_C	E27	PETp1	DMI0TXP	U27
24	PCIE_RX2-	H26	PERn2	DMI1RXN	Y26
24	PCIE_RX2+	H25	PERp2	DMI1RXP	Y25
	PCIE_TXN2_C	G28	PETn2	DMI1TXN	W28
	PCIE_TXP2_C	G27	PETp2	DMI1TXP	W27
33	PCIE_RX3-	K26	PERn3	DMI2RXN	AB26
33	PCIE_RX3+	K25	PERp3	DMI2RXP	AB25
	PCIE_TXN3_C	J28	PETn3	DMI2TXN	AA28
	PCIE_TXP3_C	J27	PETp3	DMI2TXP	AA27
T59	PAD	M26	PERn4	DMI3RXN	AD25
T57	PAD	M25	PERp4	DMI3RXP	AD24
T64	PAD	L28	PETn4	DMI3TXN	AC28
T58	PAD	L27	PETp4	DMI3TXP	AC27
		P26	PERn5	DMI_CLKN	AE28
		P25	PERp5	DMI_CLKP	AE27
		N28	PETn5		
		N27	PETp5	DMI_ZCOMP	C25
		T25	PERn6	DMI_IRCOMP	D25
		T24	PERp6		
		R28	PETn6		
		R27	PETp6		

DMI_MTX_IRX_N0	6	DMI_MTX_IRX_P0 6
DMI_MTX_ITX_N0	6	DMI_MRX_ITX_P0 6
DMI_MTX_IRX_N1	6	DMI_MTX_IRX_P1 6
DMI_MRX_ITX_N1	6	DMI_MRX_ITX_P1 6
DMI_MTX_IRX_N2	6	DMI_MTX_IRX_P2 6
DMI_MRX_ITX_N2	6	DMI_MRX_ITX_P2 6
DMI_MTX_IRX_N3	6	DMI_MTX_IRX_P3 6
DMI_MRX_ITX_N3	6	DMI_MRX_ITX_P3 6
CLK_PCIE_ICH#	17	
CLK_PCIE_ICH	17	

R180 24.9/F — +1.5V_RUN — Place within 500mils of ICH7

Place series terms close to source.

+3V — R163 10K — R162 10K — R160 10K

T108	PAD	SPI_CLK	R2	SPI_CLK
T56	PAD	SPI_CS#	P6	SPI_CS#
T107	PAD	NVM_ARB	P1	SPI_ARB
T61	PAD	SPI_MOSI	P5	SPI_MOSI
T53	PAD	SPI_MISO	P2	SPI_MISO

SPI / USB

		OC0#	D3	OC0#
		OC1#	C4	OC1#
		OC2#	D5	OC2#
		OC3#	D4	OC3#
		OC4#	E5	OC4#
		OC5#	C3	OC5#/GPIO29
		OC6#	A2	OC6#/GPIO30
		OC7#	B3	OC7#/GPIO31

		USBP0N	F1	USBP0- 26
		USBP0P	F2	USBP0+ 26
		USBP1N	G4	USBP1- 26
		USBP1P	G3	USBP1+ 26
		USBP2N	H1	USBP2- 26
		USBP2P	H2	USBP2+ 26
		USBP3N	J4	USBP3- PAD T69
		USBP3P	J3	USBP3+ PAD T68
		USBP4N	K1	USBP4- 35
		USBP4P	K2	USBP4+ 35
		USBP5N	L4	USBP5- 27
		USBP5P	L5	USBP5+ 27
		USBP6N	M1	USBP6- 24
		USBP6P	M2	USBP6+ 24
		USBP7N	N4	USBP7- 24
		USBP7P	N3	USBP7+ 24
		USBRBIAS#	D2	
		USBRBIAS	D1	USBRBIAS

Ext Right Side Top
Ext Right Side
Ext Left Side
Dock
Bluetooth
Mini Card
Express Card

ICH7-M

RP32 — 10P8R-10K — 3VSUS

OC2#	6	5	OC5#
OC4#	7	4	OC0#
OC1#	8	3	OC7#
OC3#	9	2	OC6#
3VSUS	10	1	

Short D2 and D1 at the package and keep length to less than 500mils. Trace Impedance should be 60ohms +/- 15%.

R338 22.6/F

PCI Pullups

RP28 — 10P8R-8.2K — +3V

ICH_GPIO2_PIRQE#	6	5	PCI_PERR#
ICH_GPIO5_PIRQH#	7	4	PCI_SERR#
ICH_GPIO4_PIRQG#	8	3	PCI_PLOCK#
PCI_REQ5#	9	2	
+3V	10	1	

RP27 — 10P8R-8.2K — +3V

PCI_REQ4#	6	5	PCI_STOP#
PCI_TRDY#	7	4	PCI_FRAME#
PCI_DEVSEL#	8	3	PCI_REQ1#
PCI_REQ3#	9	2	PCI_REQ2#
+3V	10	1	

RP29 — 10P8R-8.2K — +3V

PCI_PIRQC#	6	5	PCI_PIRQD#
PCI_PIRQB#	7	4	ICH_GPIO3_PIRQF#
PCI_PIRQA#	8	3	PCI_IRDY#
	9	2	PCI_REQ0#
+3V	10	1	

U30B

PCI

PCI_AD0	E18	AD0	REQ0#	D7	PCI_REQ0#
PCI_AD1	C18	AD1	GNT0#	E7	PCI_GNT0#
PCI_AD2	A16	AD2	REQ1#	C16	PCI_REQ1#
PCI_AD3	E18	AD3	GNT1#	D16	PCI_GNT1#
PCI_AD4	E16	AD4	REQ2#	C17	PCI_REQ2#
PCI_AD5	A18	AD5	GNT2#	D17	PCI_GNT2#
PCI_AD6	E17	AD6	REQ3#	E13	PCI_REQ3#
PCI_AD7	A17	AD7	GNT3#	F13	PCI_GNT3#
PCI_AD8	A15	AD8	REQ4#/GPIO22	A13	PCI_REQ4#
PCI_AD9	C14	AD9	GNT4#/GPIO48	A14	PCI_GNT4#
PCI_AD10	E14	AD10	GPIO1/REQ5#	C8	PCI_REQ5#
PCI_AD11	D14	AD11	GPIO17/GNT5#	D8	PCI_GNT5#
PCI_AD12	B12	AD12			
PCI_AD13	C13	AD13	C/BE0#	B15	PCI_C_BE0#
PCI_AD14	G15	AD14	C/BE1#	C12	PCI_C_BE1#
PCI_AD15	G13	AD15	C/BE2#	D12	PCI_C_BE2#
PCI_AD16	E12	AD16	C/BE3#	C15	PCI_C_BE3#
PCI_AD17	C11	AD17			
PCI_AD18	D11	AD18	IRDY#	A7	PCI_IRDY#
PCI_AD19	A11	AD19	PAR	E10	
PCI_AD20	A10	AD20	PCIRST#	B18	PCI_RST#_G
PCI_AD21	F11	AD21	DEVSEL#	A12	PCI_DEVSEL#
PCI_AD22	F10	AD22	PERR#	C9	PCI_PERR#
PCI_AD23	E9	AD23	PLOCK#	E11	PCI_PLOCK#
PCI_AD24	D9	AD24	SERR#	B10	PCI_SERR#
PCI_AD25	B9	AD25	STOP#	E15	PCI_STOP#
PCI_AD26	A8	AD26	TRDY#	E14	PCI_TRDY#
PCI_AD27	A6	AD27	FRAME#	E16	PCI_FRAME#
PCI_AD28	C7	AD28			
PCI_AD29	B6	AD29	PLTRST#	C26	PCI_PLTRST#
PCI_AD30	E6	AD30	PCICLK	A9	CLK_PCI_ICH
PCI_AD31	D6	AD31	PME#	B19	

22,42 PCI_AD[0..31]

REQ2 : 1394/Media Card

R175 *1K_NC — R314 *1K_NC

Interrupt I/F

42	PCI_PIRQA#	PCI_PIRQA#	A3	PIRQA#	GPIO2/PIRQE# G8 ICH_GPIO2_PIRQE#
42	PCI_PIRQB#	PCI_PIRQB#	B4	PIRQB#	GPIO3/PIRQF# E7 ICH_GPIO3_PIRQF#
22	PCI_PIRQC#	PCI_PIRQC#	C5	PIRQC#	GPIO4/PIRQG# F8 ICH_GPIO4_PIRQG#
22	PCI_PIRQD#	PCI_PIRQD#	B5	PIRQD#	GPIO5/PIRQH# G7 ICH_GPIO5_PIRQH#

PCI_PIRQC: 1394/Media Card
PCI_PIRQD: for 1394

MISC

T28	PAD	AE5	RSVD[1]	RSVD[6]	AE9 PAD T27
T33	PAD	AD5	RSVD[2]	RSVD[7]	AG8 PAD T112
T113	PAD	AG4	RSVD[3]	RSVD[8]	AH8
T116	PAD	AH4	RSVD[4]	RSVD[9]	F21
T29	PAD	AD9	RSVD[5]	MCH_SYNC#	AH20 MCH_ICH_SYNC# 6

ICH7-M

		GNT5#	GNT4#
LPC	11	No stuff	No stuff
PCI	10	No stuff	Stuff
SPI	01	Stuff	No stuff

DOCK	REQ0	GNT0	PIRQA
Cardbus or Cardbus/1394	REQ1	GNT1	PIRQD
1394/MediaCard	REQ2	GNT2	PIRQC PIRQD
LOM(4401)	REQ3	GNT3	PIRQB

CLK_PCI_ICH — R320 *10_NC — C367 *8.2P_16V_NC

Reserved for EMI. Place resister and cap close to ICH.

Add Buffers as needed for Loading and fanout concerns.

C364 0.047U_10V — U28 7SH32 — PCI_RST# G — PCI_RST# 22,42

C246 0.047U_10V — U14 7SH32 — PCI_PLTRST# — PLTRST# 6,13,19,21,24,33

PROJECT : SW1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH7-M (USB,DMI,PCIE,PCI)	1A
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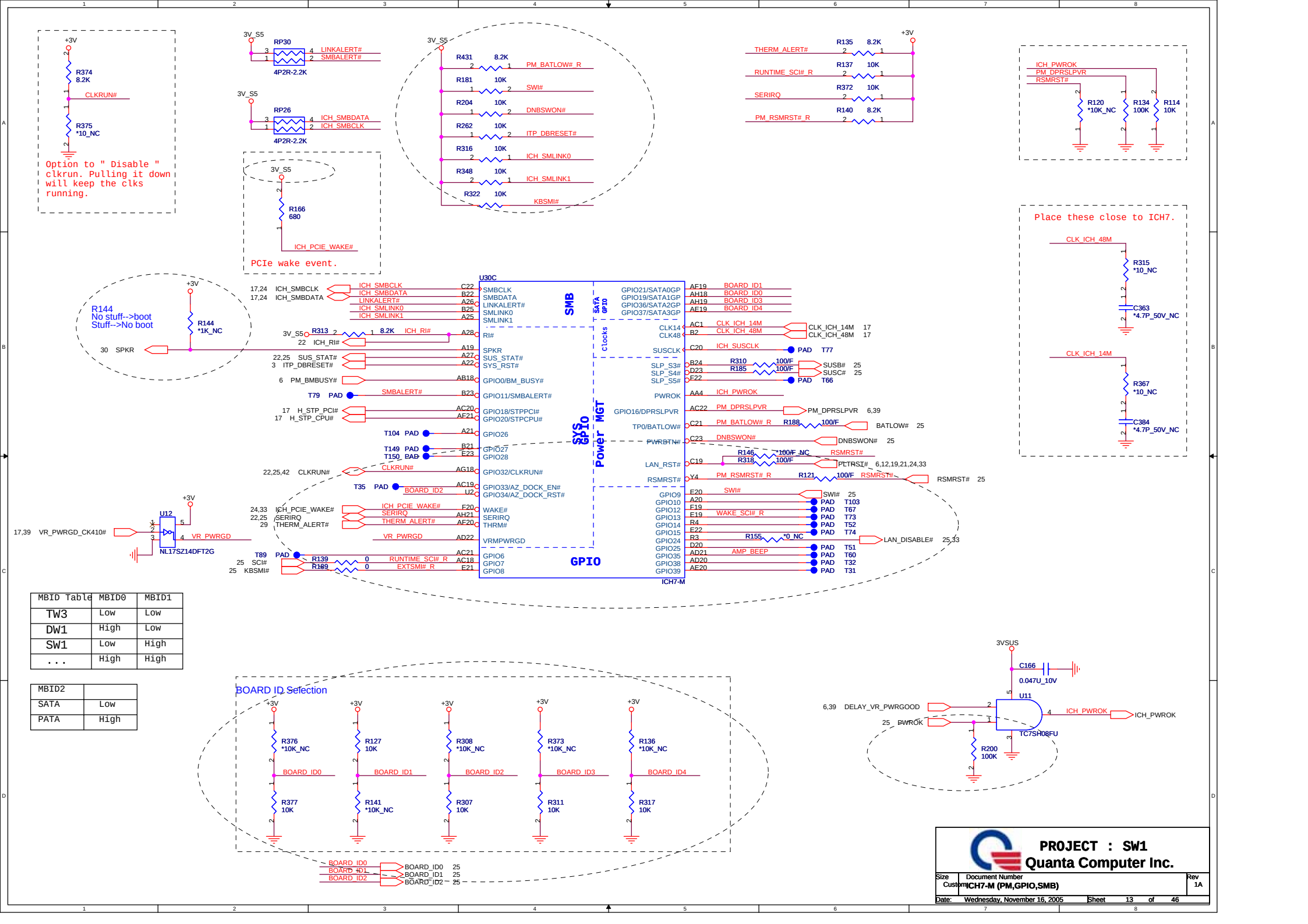

MBID Table	MBID0	MBID1
TW3	Low	Low
DW1	High	Low
SW1	Low	High
...	High	High

MBID2	
SATA	Low
PATA	High

PROJECT : SW1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH7-M (PM,GPIO,SMB)	1A

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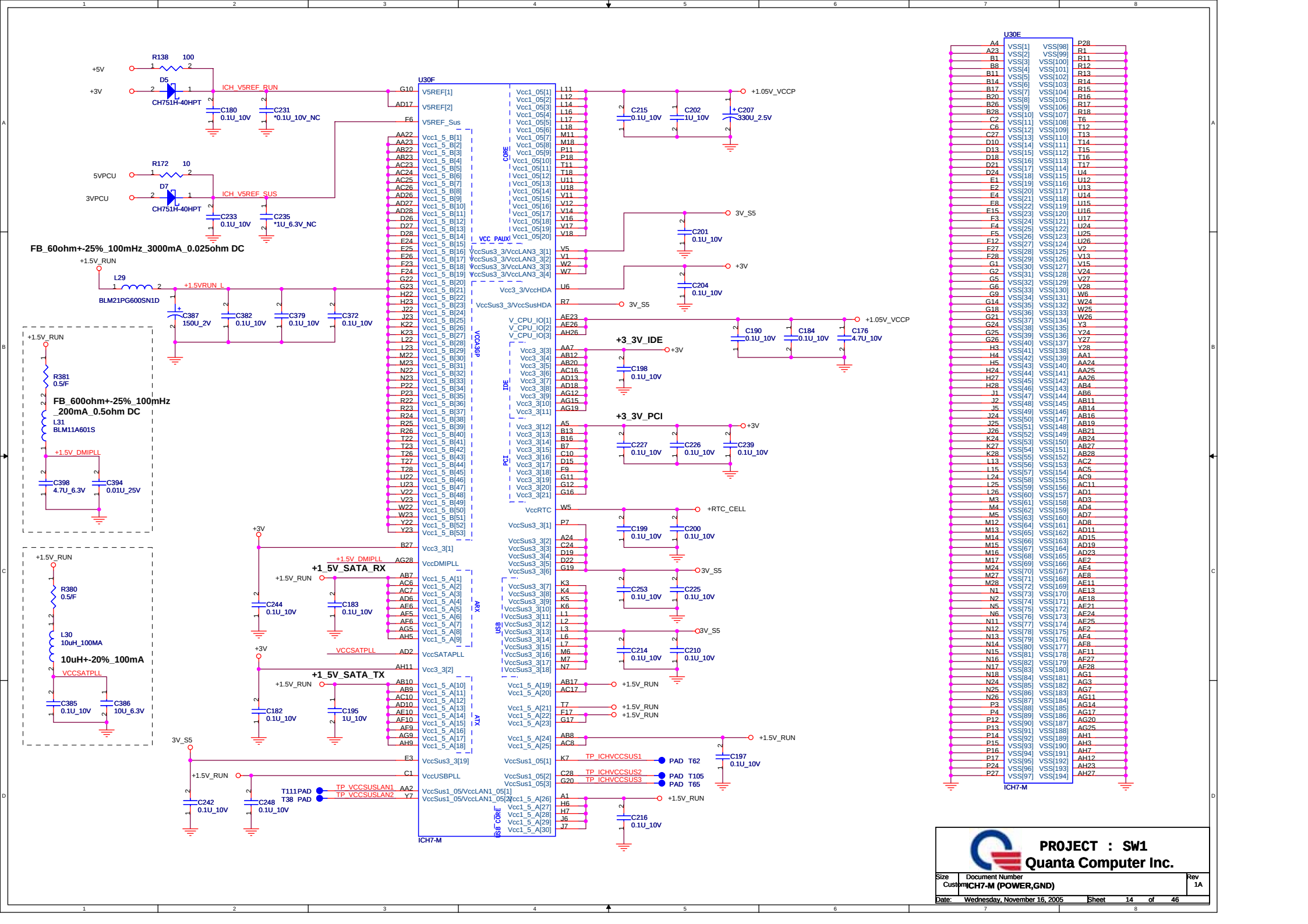
R138 100
+5V
+3V
D5
CH751H-40HPT
ICH_V5REF_RUN
C180 0.1U_10V
C231 *0.1U_10V_NC
R172 10
5VPCU
3VPCU
D7
CH751H-40HPT
ICH_V5REF_SUS
C233 0.1U_10V
C235 *1U_6.3V_NC
FB_60ohm+-25%_100mHz_3000mA_0.025ohm DC
+1.5V_RUN
L29
BLM21PG600SN1D
+1.5VRUN_L
C387 150U_2V
C382 0.1U_10V
C379 0.1U_10V
C372 0.1U_10V
+1.5V_RUN
R381 0.5/F
FB_600ohm+-25%_100mHz _200mA_0.5ohm DC
L31
BLM11A601S
+1.5V_DMIPLL
C398 4.7U_6.3V
C394 0.01U_25V
+1.5V_RUN
R380 0.5/F
L30
10uH_100MA
10uH+-20%_100mA
VCCSATPLL
C385 0.1U_10V
C386 10U_6.3V
U30F
V5REF[1]
V5REF[2]
V5REF_Sus
Vcc1_5_B[1]
Vcc1_5_B[2]
Vcc1_5_B[3]
Vcc1_5_B[4]
Vcc1_5_B[5]
Vcc1_5_B[6]
Vcc1_5_B[7]
Vcc1_5_B[8]
Vcc1_5_B[9]
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Vcc1_5_B[52]
Vcc1_5_B[53]
Vcc3_3[1]
VccDMIPLL
Vcc1_5_A[1]
Vcc1_5_A[2]
Vcc1_5_A[3]
Vcc1_5_A[4]
Vcc1_5_A[5]
Vcc1_5_A[6]
Vcc1_5_A[7]
Vcc1_5_A[8]
Vcc1_5_A[9]
VccSATAPLL
Vcc3_3[2]
Vcc1_5_A[10]
Vcc1_5_A[11]
Vcc1_5_A[12]
Vcc1_5_A[13]
Vcc1_5_A[14]
Vcc1_5_A[15]
Vcc1_5_A[16]
Vcc1_5_A[17]
Vcc1_5_A[18]
VccSus3_3[19]
VccUSBPLL
VccSus1_05/VccLAN1_05[1]
VccSus1_05/VccLAN1_05[2]
VCCA3GP
CORE
VCC_PAUX
VccSus3_3/VccLAN3_3[1]
VccSus3_3/VccLAN3_3[2]
VccSus3_3/VccLAN3_3[3]
VccSus3_3/VccLAN3_3[4]
Vcc3_3/VccHDA
VccSus3_3/VccSusHDA
V_CPU_IO[1]
V_CPU_IO[2]
V_CPU_IO[3]
IDE
Vcc3_3[3]
Vcc3_3[4]
Vcc3_3[5]
Vcc3_3[6]
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Vcc3_3[21]
VccRTC
VccSus3_3[1]
VccSus3_3[2]
VccSus3_3[3]
VccSus3_3[4]
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VccSus3_3[17]
VccSus3_3[18]
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ATX
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Vcc1_5_A[20]
Vcc1_5_A[21]
Vcc1_5_A[22]
Vcc1_5_A[23]
Vcc1_5_A[24]
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VccSus1_05[1]
VccSus1_05[2]
VccSus1_05[3]
Vcc1_5_A[26]
Vcc1_5_A[27]
Vcc1_5_A[28]
Vcc1_5_A[29]
Vcc1_5_A[30]
USB_CORE
ICH7-M
L11
L12
L14
L16
L17
L18
M11
M18
P11
P18
T11
T18
U11
U18
V11
V12
V14
V16
V17
V18
V5
V1
W2
W7
U6
R7
AE23
AE26
AH26
AA7
AB12
AB20
AC16
AD13
AD18
AG12
AG15
AG19
A5
B13
B16
B7
C10
D15
F9
G11
G12
G16
W5
P7
A24
C24
D19
D22
G19
K3
K4
K5
K6
L1
L2
L3
L6
L7
M6
M7
N7
AB17
AC17
T7
F17
G17
AB8
AC8
K7
C28
G20
A1
H6
H7
J6
J7
+1.05V_VCCP
C215 0.1U_10V
C202 1U_10V
C207 330U_2.5V
3V_S5
C201 0.1U_10V
+3V
C204 0.1U_10V
3V_S5
+1.05V_VCCP
C190 0.1U_10V
C184 0.1U_10V
C176 4.7U_10V
+3_3V_IDE
+3V
C198 0.1U_10V
+3_3V_PCI
+3V
C227 0.1U_10V
C226 0.1U_10V
C239 0.1U_10V
+RTC_CELL
C199 0.1U_10V
C200 0.1U_10V
3V_S5
C253 0.1U_10V
C225 0.1U_10V
3V_S5
C214 0.1U_10V
C210 0.1U_10V
+1.5V_RUN
+1.5V_RUN
+1.5V_RUN
C197 0.1U_10V
TP_ICHVCCSUS1
PAD T62
TP_ICHVCCSUS2
TP_ICHVCCSUS3
PAD T105
PAD T65
+1.5V_RUN
C216 0.1U_10V
+1.5V_DMIPLL
+1.5V_RUN
+1_5V_SATA_RX
C244 0.1U_10V
C183 0.1U_10V
VCCSATPLL
+1.5V_RUN
+1_5V_SATA_TX
C182 0.1U_10V
C195 1U_10V
3V_S5
+1.5V_RUN
C242 0.1U_10V
C248 0.1U_10V
T111 PAD
T38 PAD
TP_VCCSUSLAN1
TP_VCCSUSLAN2
U30E
VSS[1]
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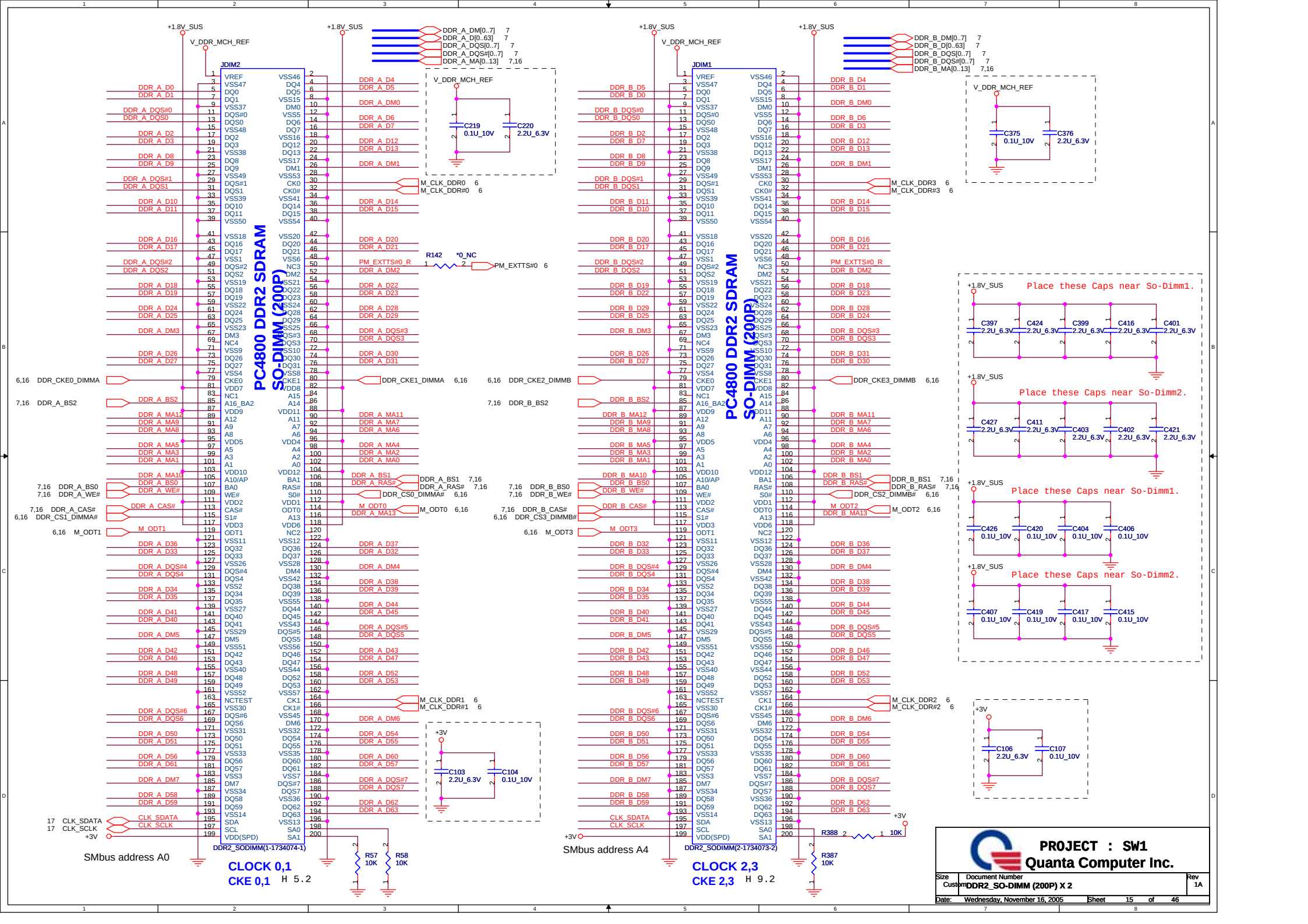
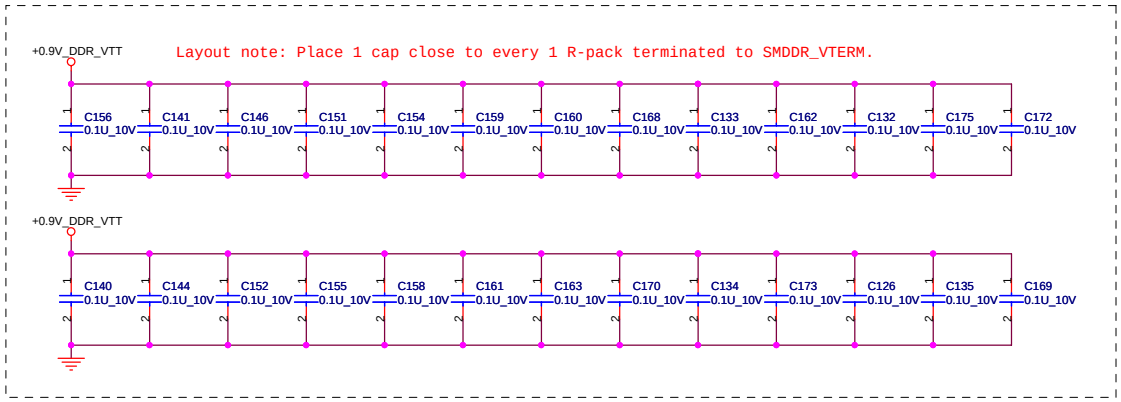
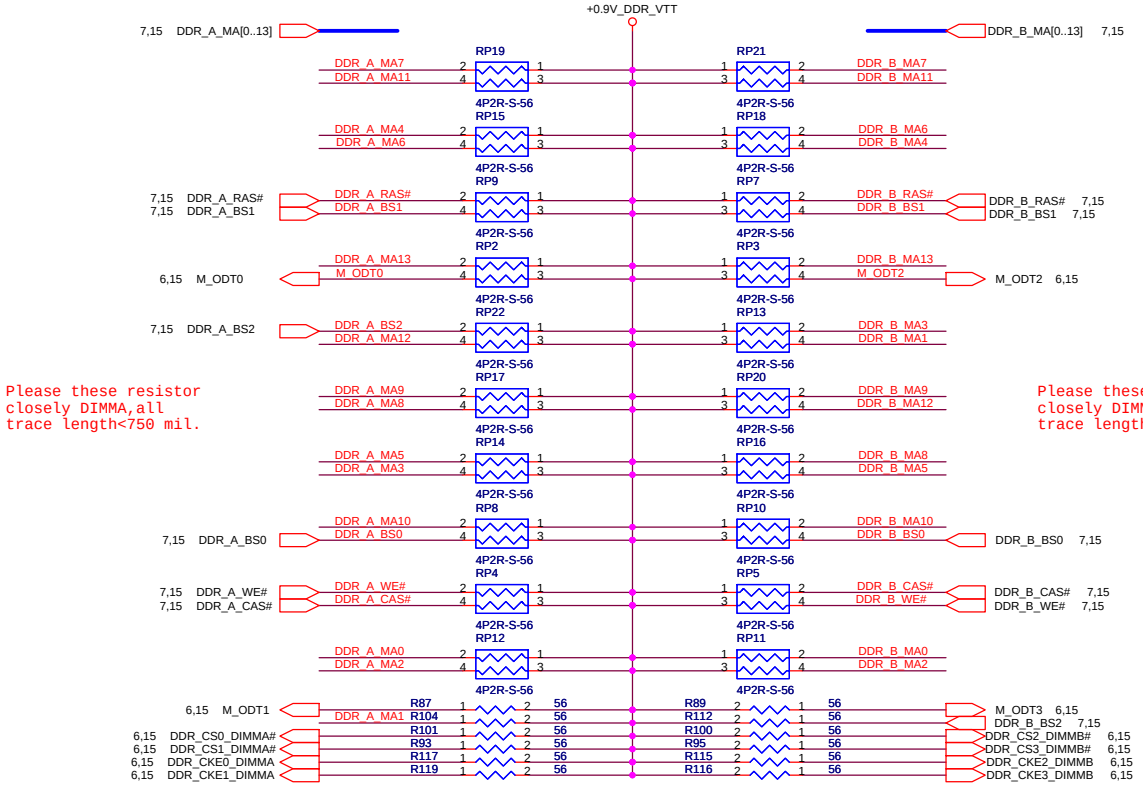
P28
R1
R11
R12
R13
R14
R15
R16
R17
R18
T6
T12
T13
T14
T15
T16
T17
U4
U12
U13
U14
U15
U16
U17
U24
U25
U26
V2
V13
V15
V24
V27
V28
W6
W24
W25
W26
Y3
Y24
Y27
Y28
AA1
AA24
AA25
AA26
AB4
AB6
AB11
AB14
AB16
AB19
AB21
AB24
AB27
AB28
AC2
AC5
AC9
AC11
AD1
AD3
AD4
AD7
AD8
AD11
AD15
AD19
AD23
AE2
AE4
AE8
AE11
AE13
AE18
AE21
AE24
AE25
AF2
AF4
AF8
AF11
AF27
AF28
AG1
AG3
AG7
AG11
AG14
AG17
AG20
AG25
AH1
AH3
AH7
AH12
AH23
AH27
ICH7-M
PROJECT : SW1
Quanta Computer Inc.
Size Custom
Document Number ICH7-M (POWER,GND)
Rev 1A
Date: Wednesday, November 16, 2005
Sheet 14 of 46


JDIM2
PC4800 DDR2 SDRAM SO-DIMM (200P)
DDR2_SODIMM(1-1734074-1)
JDIM1
PC4800 DDR2 SDRAM SO-DIMM (200P)
DDR2_SODIMM(2-1734073-2)
SMbus address A0
SMbus address A4
CLOCK 0,1
CKE 0,1 H 5.2
CLOCK 2,3
CKE 2,3 H 9.2
Place these Caps near So-Dimm1.
Place these Caps near So-Dimm2.
Place these Caps near So-Dimm1.
Place these Caps near So-Dimm2.
PROJECT : SW1
Quanta Computer Inc.
DDR2_SO-DIMM (200P) X 2
Wednesday, November 16, 2005





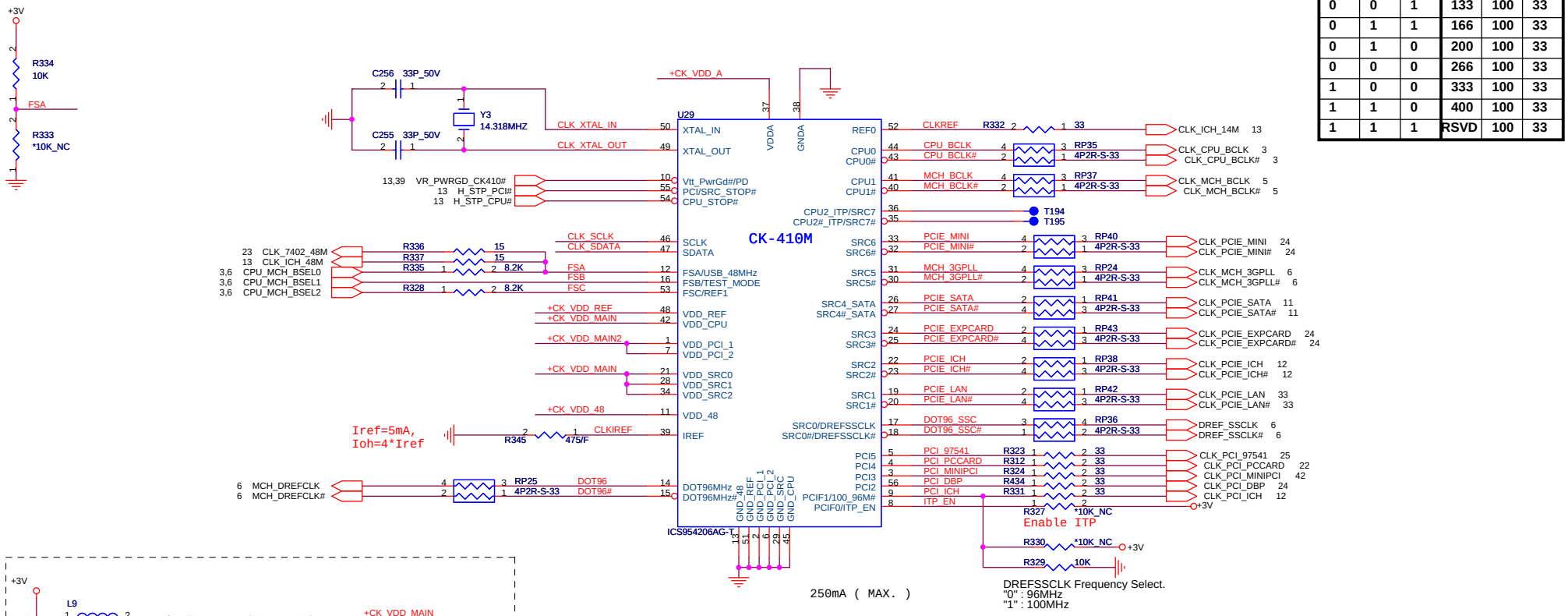
Please these resistor closely DIMMA,all trace length<750 mil.

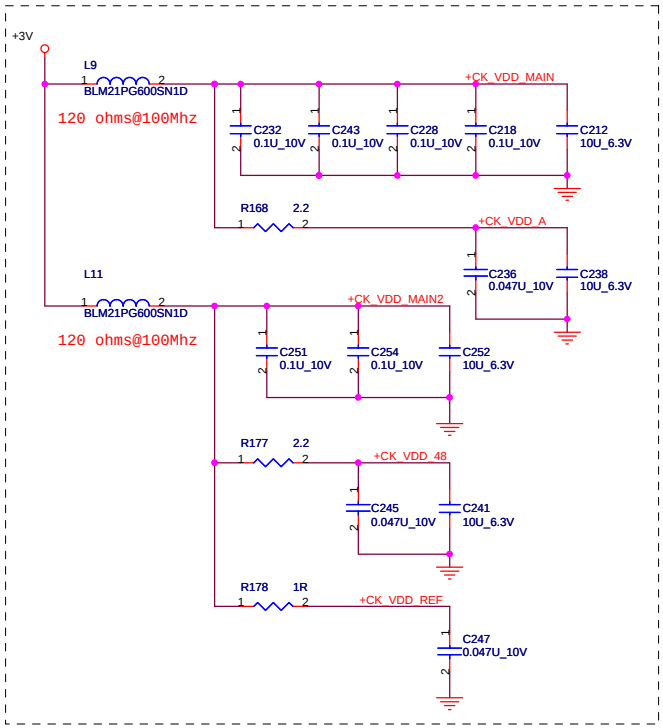
Please these resistor closely DIMMB,all trace length<750 mil.

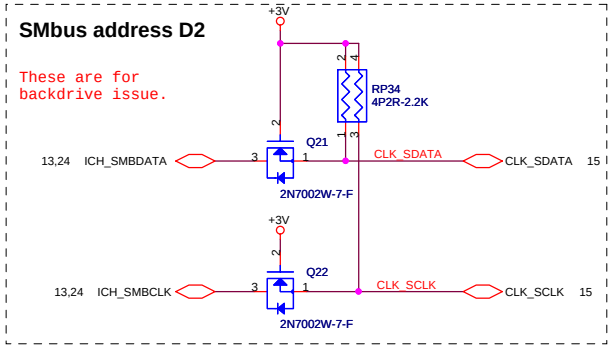
PROJECT : SW1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR2 RES.ARRAY	1A
Date: Wednesday, November 16, 2005	Sheet 16 of 46	

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33







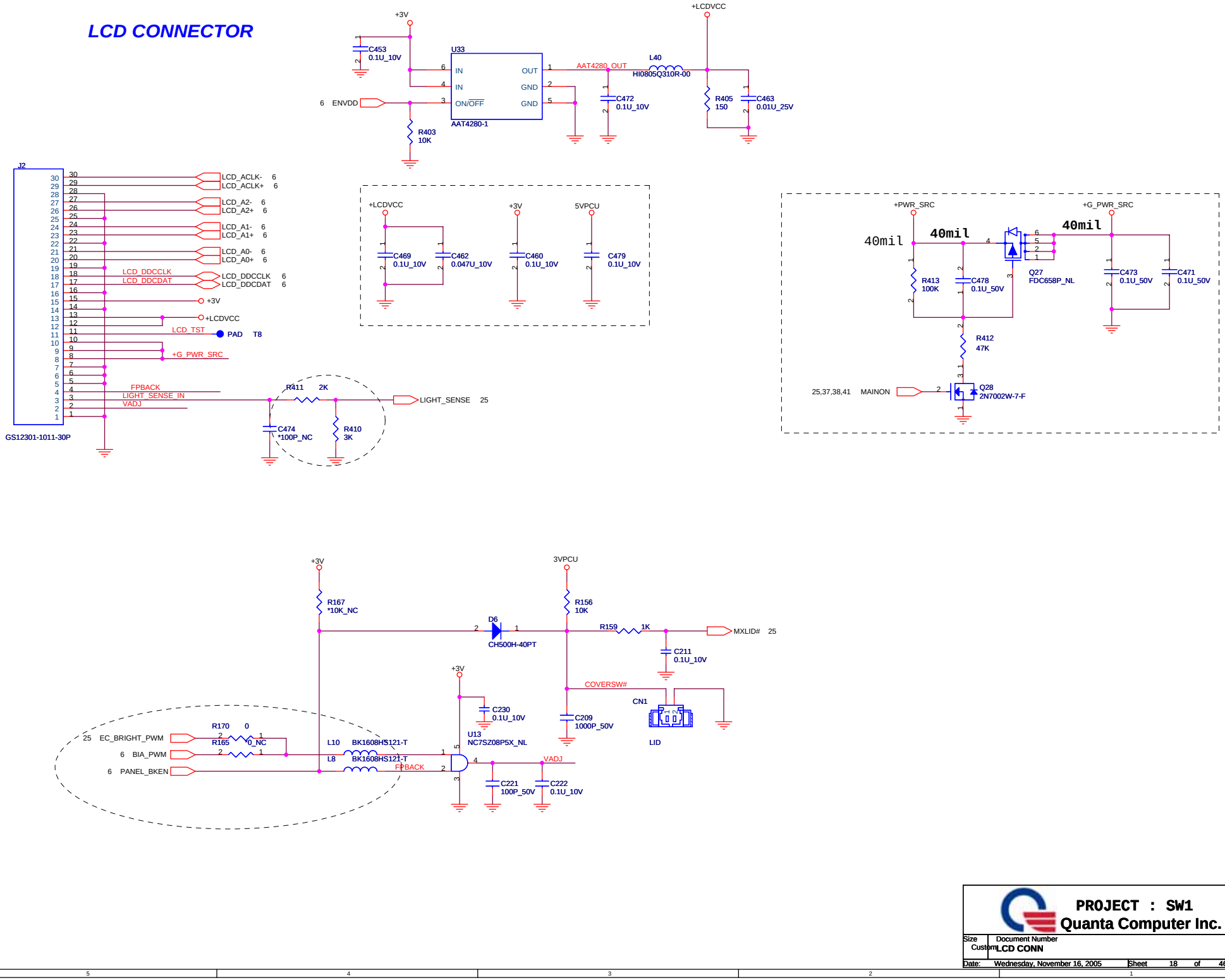
Place these termination close to CK410M.

PROJECT : SW1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CLOCK GENERATOR	1A

Date: Wednesday, November 16, 2005 Sheet 17 of 46

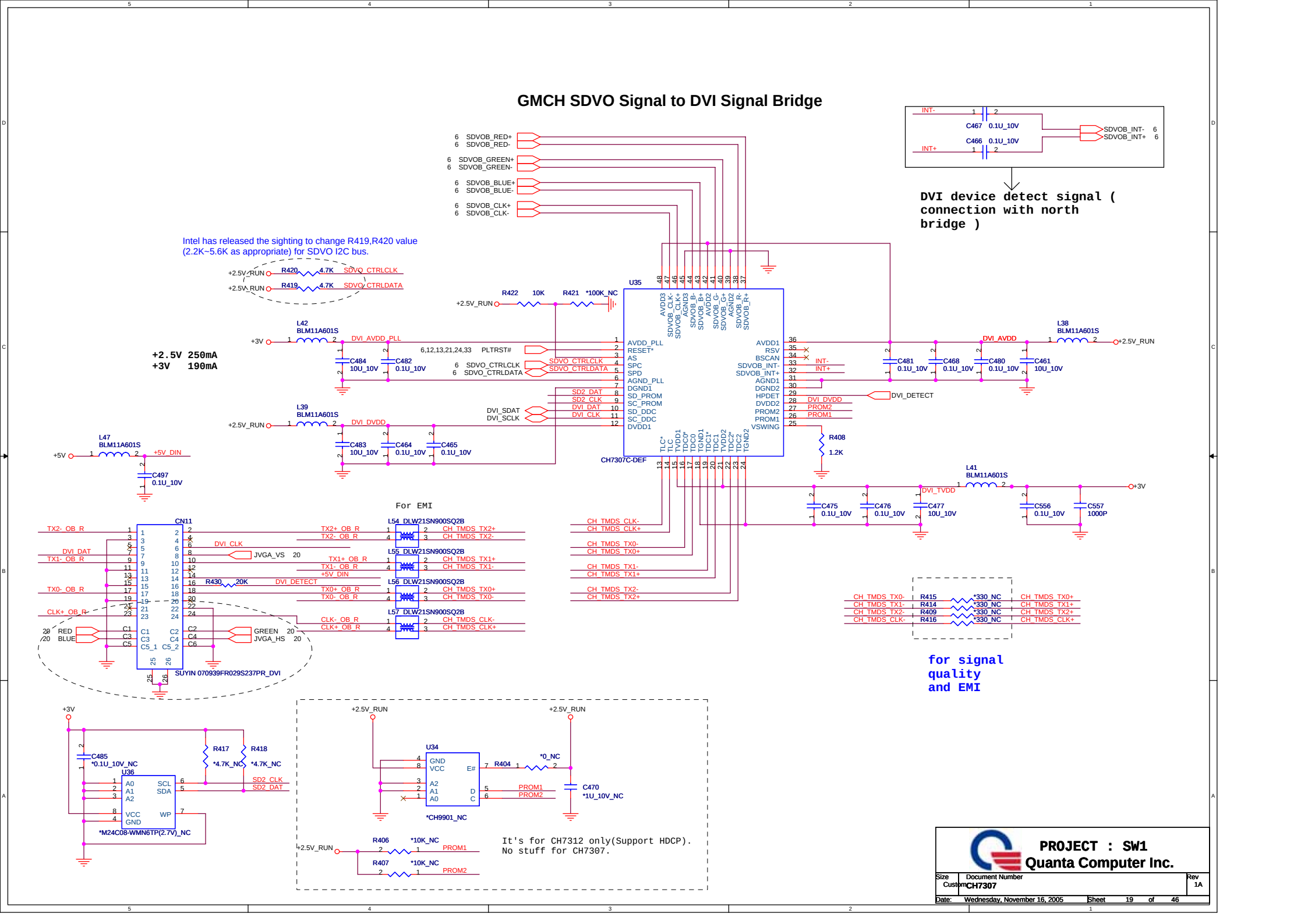
LCD CONNECTOR



PROJECT : SW1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN	1A
Date: Wednesday, November 16, 2005	Sheet 18 of 46	

GMCH SDVO Signal to DVI Signal Bridge



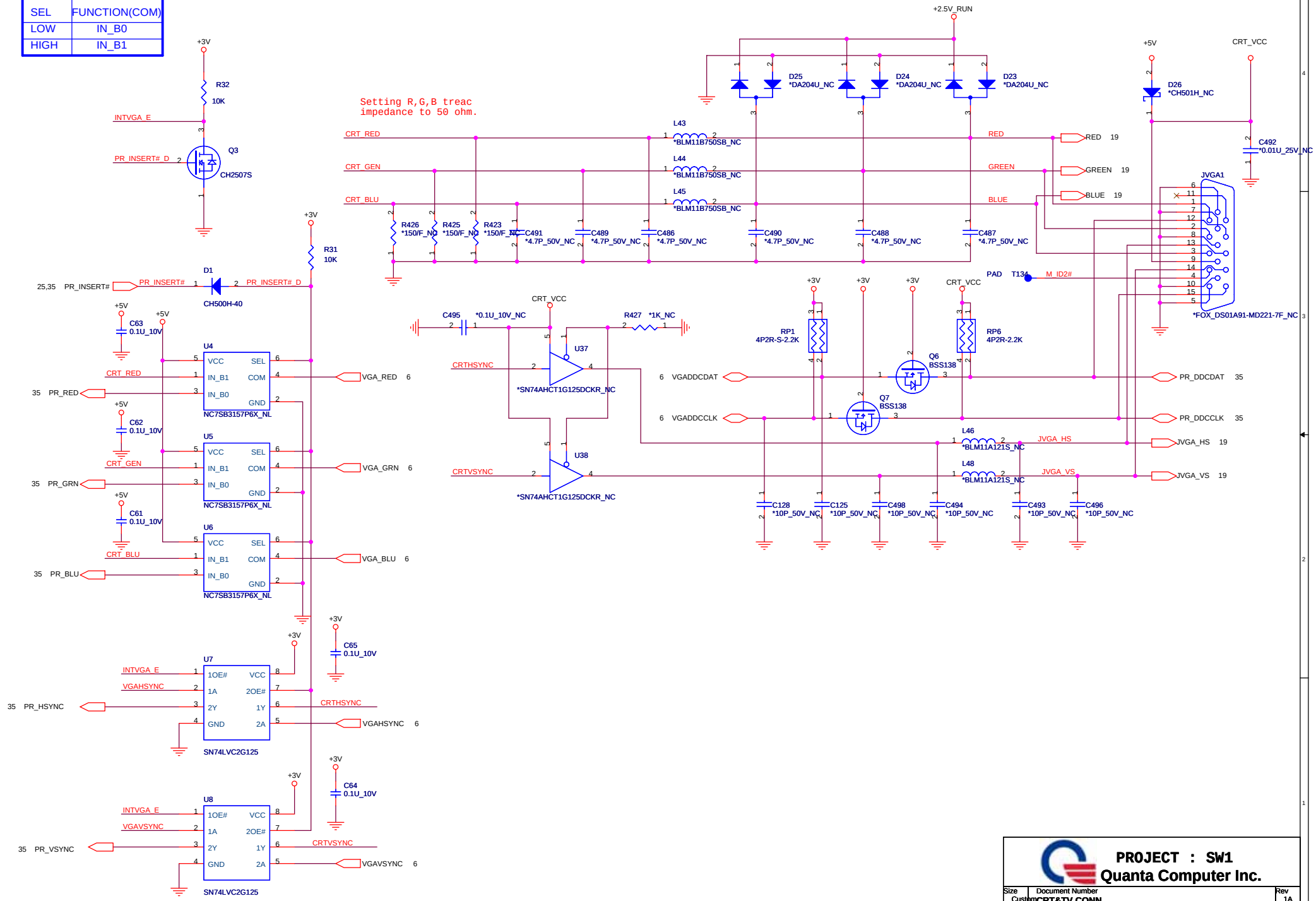
PROJECT : SW1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CH7307	1A

Date: Wednesday, November 16, 2005 Sheet 19 of 46

CRT SWITCH

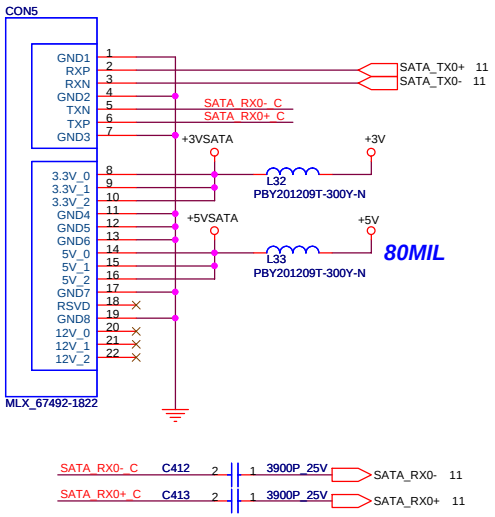
SEL	FUNCTION(COM)
LOW	IN_B0
HIGH	IN_B1



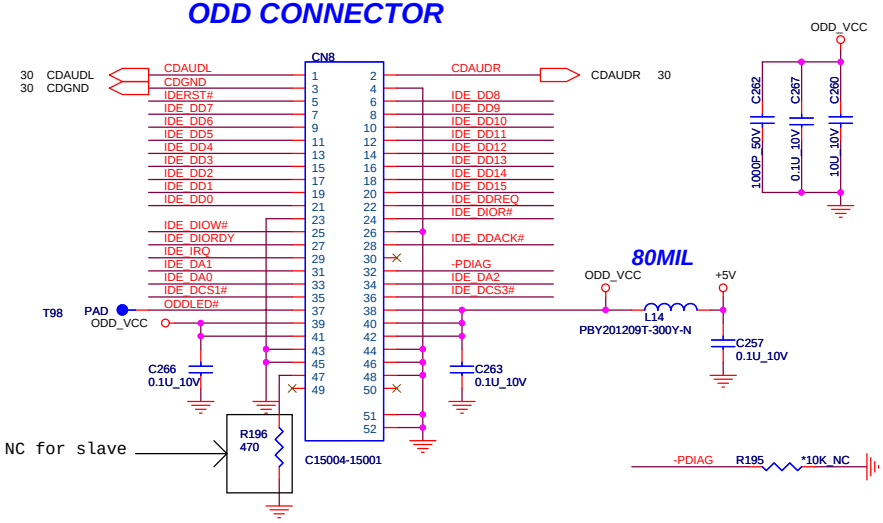
PROJECT : SW1
Quanta Computer Inc.

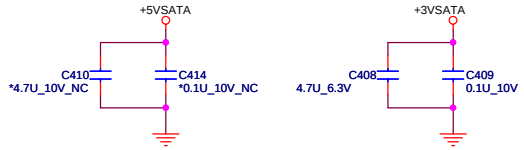
Size	Document Number	Rev
Custom	CRT&TV CONN	1A
Date: Wednesday, November 16, 2005	Sheet 20 of 46	

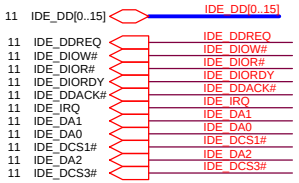
SATA Connector.



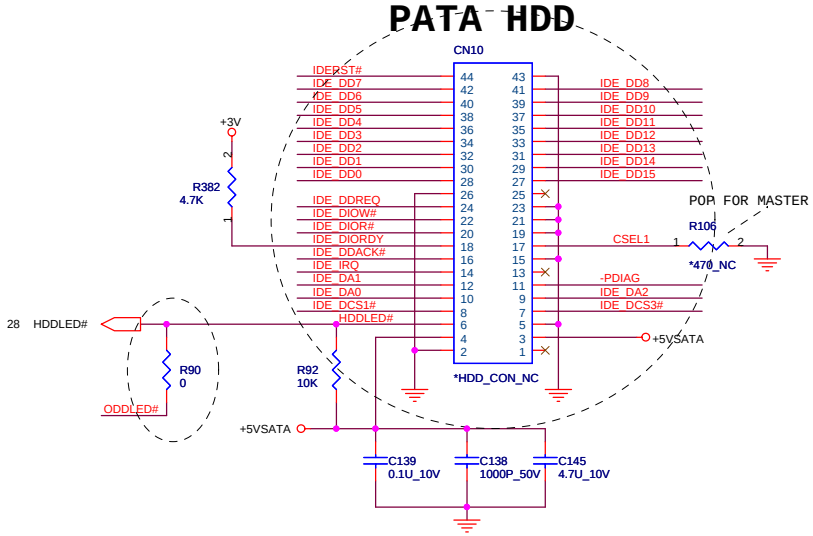
ODD CONNECTOR

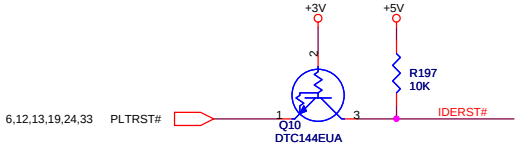




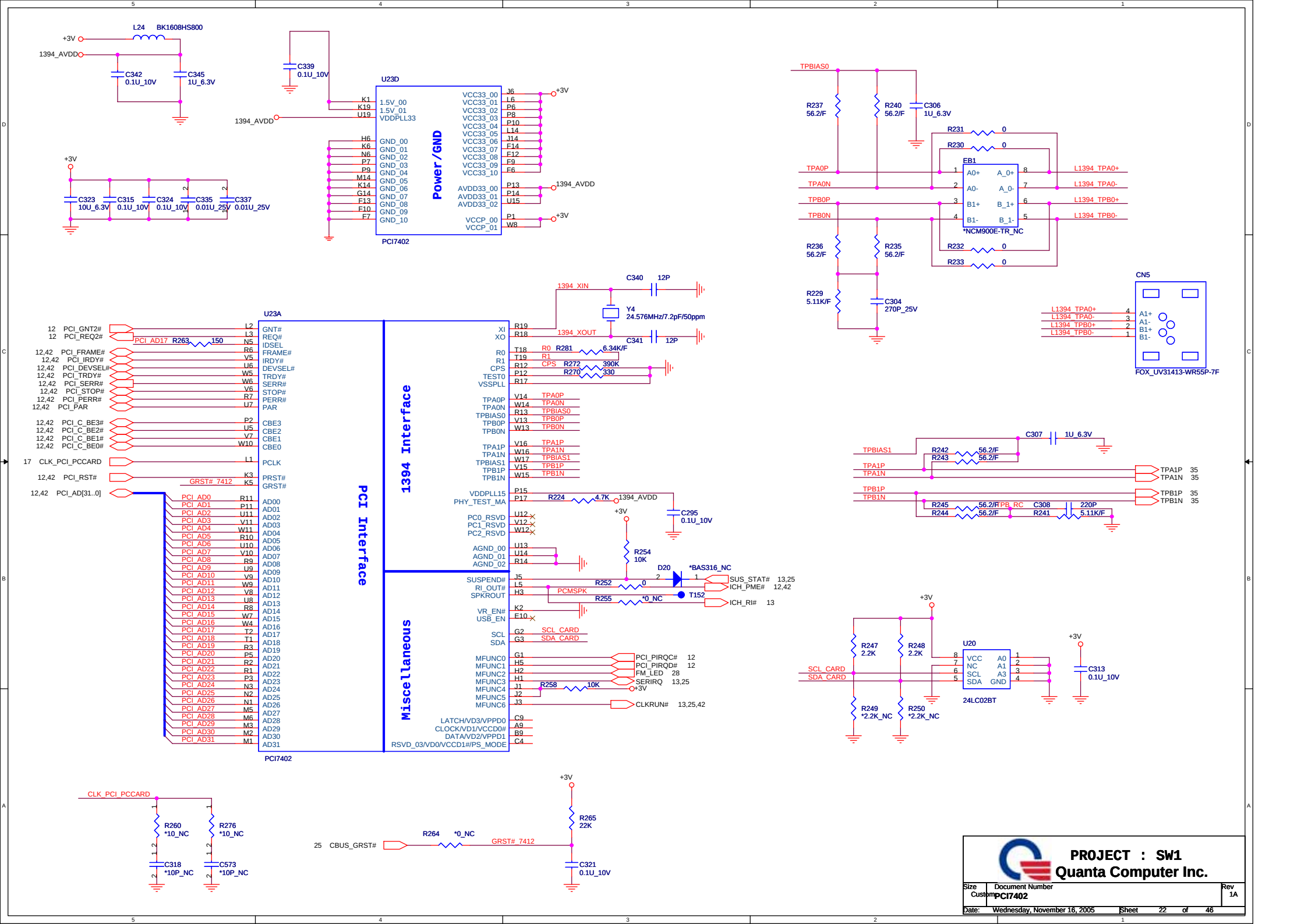


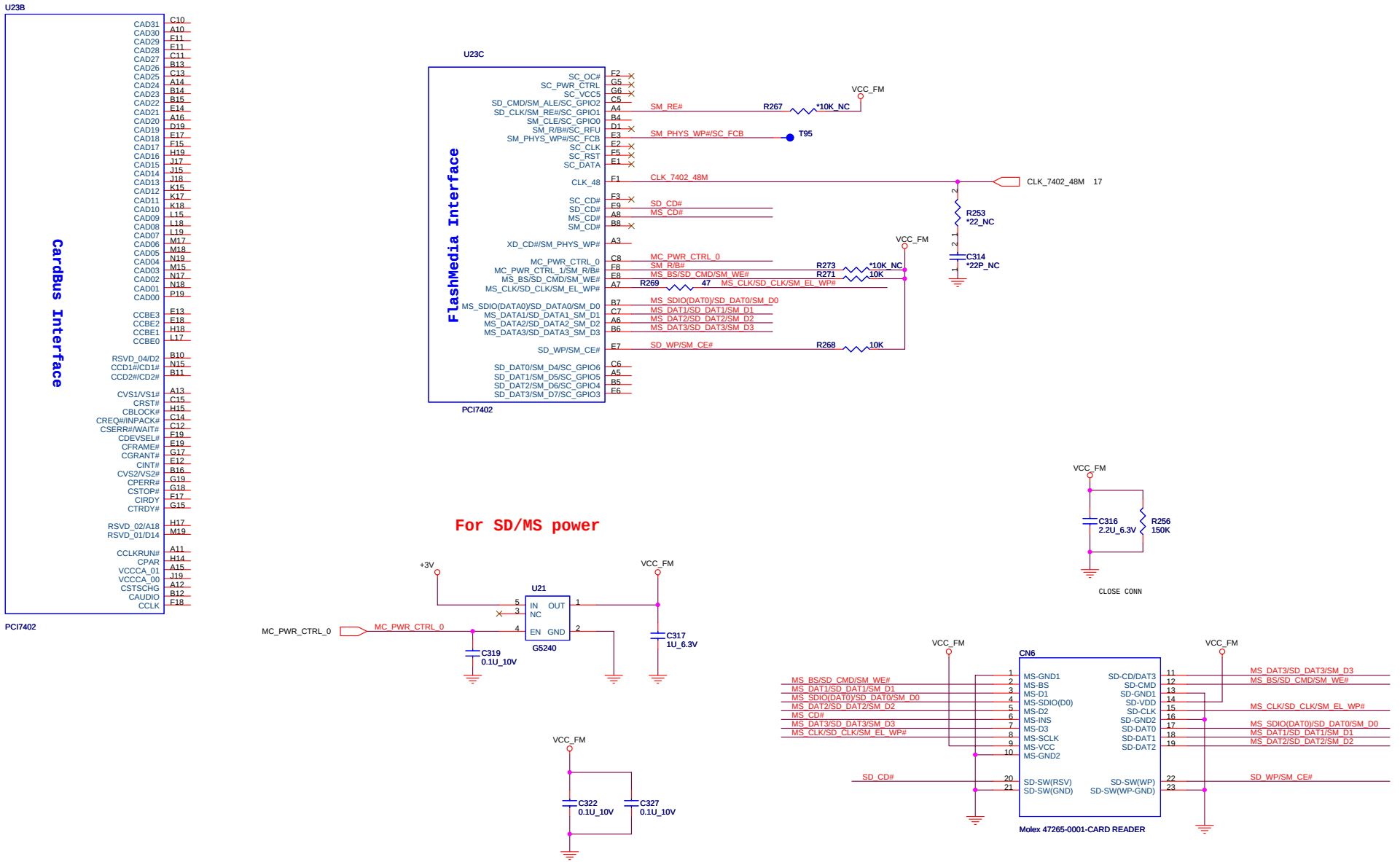
PATA HDD





PROJECT : SW1			
Quanta Computer Inc.			
Size: Custom	Document Number: SATA HDD & PATA ODD		Rev: 1A
Date: Wednesday, November 16, 2005	Sheet 21 of 46		


L24 BK1608HS800
+3V
1394_AVDD
C342 0.1U_10V
C345 1U_6.3V
C339 0.1U_10V
U23D
Power/GND
PCI7402
C323 10U_6.3V
C315 0.1U_10V
C324 0.1U_10V
C335 0.01U_25V
C337 0.01U_25V
TPBIAS0
R237 56.2/F
R240 56.2/F
C306 1U_6.3V
R231 0
R230 0
EB1
*NCM900E-TR_NC
TPA0P
TPA0N
TPB0P
TPB0N
L1394_TPA0+
L1394_TPA0-
L1394_TPB0+
L1394_TPB0-
R236 56.2/F
R235 56.2/F
R232 0
R233 0
R229 5.11K/F
C304 270P_25V
CN5
FOX_UV31413-WR55P-7F
U23A
PCI Interface
1394 Interface
Miscellaneous
PCI7402
1394_XIN
1394_XOUT
Y4 24.576MHz/7.2pF/50ppm
C340 12P
C341 12P
R281 6.34K/F
R272 390K
R270 330
C307 1U_6.3V
TPBIAS1
R242 56.2/F
R243 56.2/F
R245 56.2/F
R244 56.2/F
C308 220P
R241 5.11K/F
R224 4.7K
C295 0.1U_10V
R254 10K
D20 *BAS316_NC
R252 0
R255 *0_NC
T152
SUS_STAT#
ICH_PME#
ICH_RI#
PCMSPK
SERIRQ
CLKRUN#
SCL_CARD
SDA_CARD
U20
24LC02BT
R247 2.2K
R248 2.2K
R249 *2.2K_NC
R250 *2.2K_NC
C313 0.1U_10V
R258 10K
R260 *10_NC
R276 *10_NC
C318 *10P_NC
C573 *10P_NC
R264 *0_NC
R265 22K
C321 0.1U_10V
CBUS_GRST#
GRST# 7412
CLK_PCI_PCCARD
PROJECT : SW1
Quanta Computer Inc.
PCI7402
Custom
Rev 1A
Wednesday, November 16, 2005
Sheet 22 of 46



PROJECT : SW1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	IEEE 1394	1A
Date: Wednesday, November 16, 2005	Sheet 23 of 46	

Express Card

+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.

L23 *DLW21SN900SQ2B_NC
R283 0
R282 0
C332 0.1U_10V
C333 0.1U_10V
Please the cap near connector.
C343 0.1U_10V
C336 0.1U_10V
C338 10U_6.3V
Please the cap near connector.

CN4 EXPRESSCARD-SD-TMJS-001-26P
JAE PX10FS16PH-26P

PCI-Express TX and RX direct to connector.

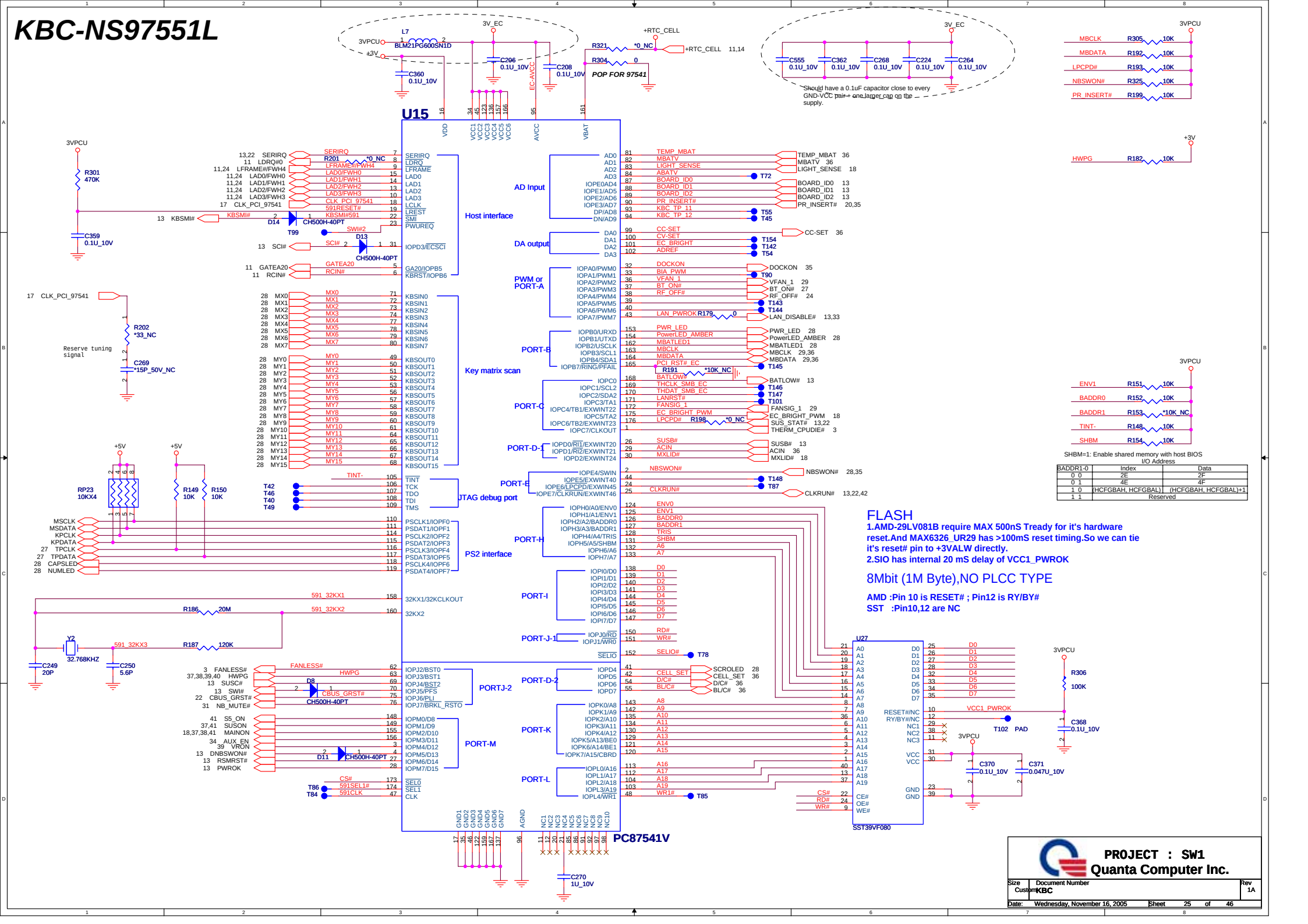
U24 R5538D001-TR-F
R285 100K
R284 100K
R280 100K
R279 100K
C346 0.1U_10V
Please the cap near pin 12 & 14(1.5VIN).
C347 0.1U_10V
Please the cap near pin 2 & 4 (3.3VIN).
C349 0.1U_10V
Please the cap near pin 17 (AUXIN).
C348 0.1U_10V
Please the cap near pin 15 (AUXOUT).
C334 0.1U_10V
Please the cap near pin 3 & 5 (3.3VOUT).
C344 0.1U_10V
Please the cap near pin 11 & 13(1.5VOUT).

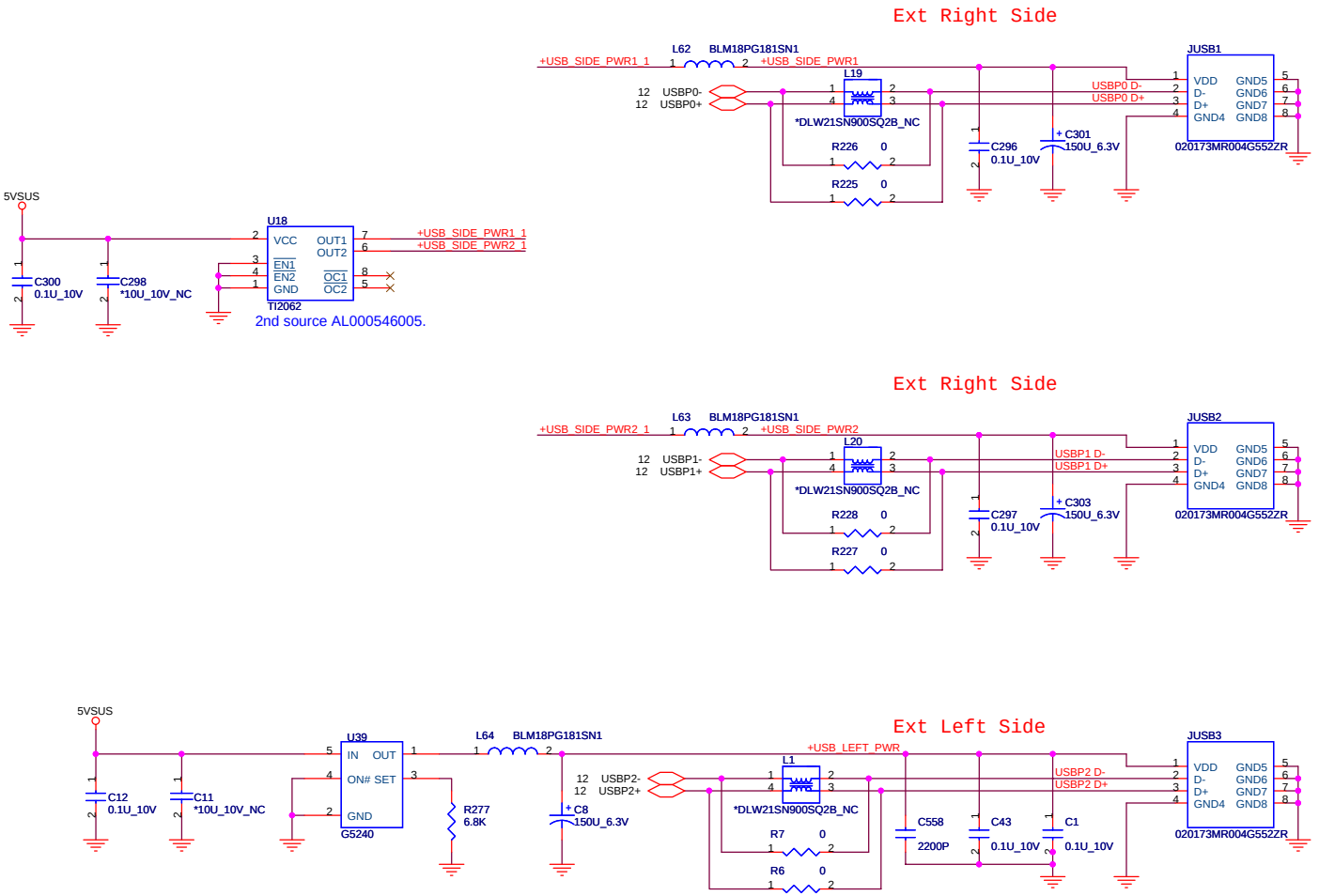
MiniCard WLAN connector

J5 MLX_48099-5700
J6 MLX_67910-5700
PCI-Express TX and RX direct to connector
R309 0
R319 0
R433 0
R341 0
RP48 0_4P2R_S
RP49 0_4P2R_S
LPC Debug
R363 10K
R355 10K
Q24 IRLML5103
Q23 IRLML5103
R350 0
R360 *0_NC
R435 *10_NC
C331 *10P_NC
Place caps close to connector.
C374 0.047U_10V
C369 0.047U_10V
C373 0.1U_10V
C378 0.1U_10V
C380 0.047U_10V
C366 0.1U_10V
C377 0.047U_10V
C365 4.7U_6.3V

PROJECT : SW1
Quanta Computer Inc.
Size: Custom | Document Number: Mini Card | Rev: 1A
Date: Wednesday, November 16, 2005 | Sheet 24 of 46

KBC-NS97551L

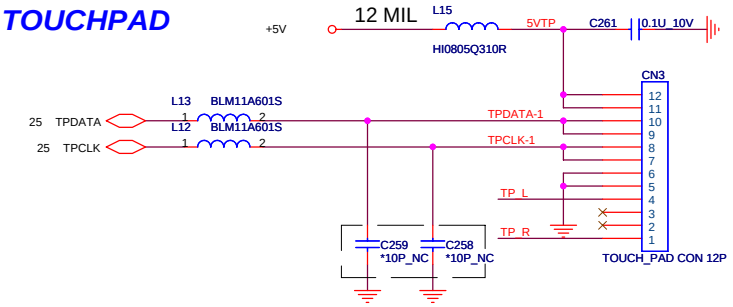


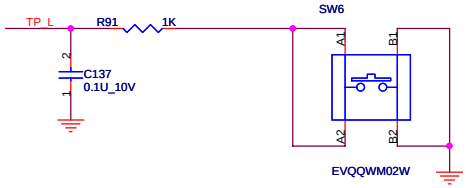


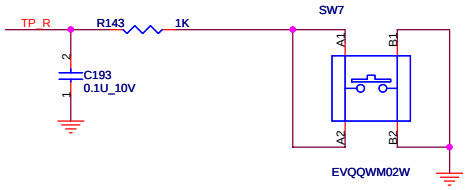
PROJECT : SW1
Quanta Computer Inc.

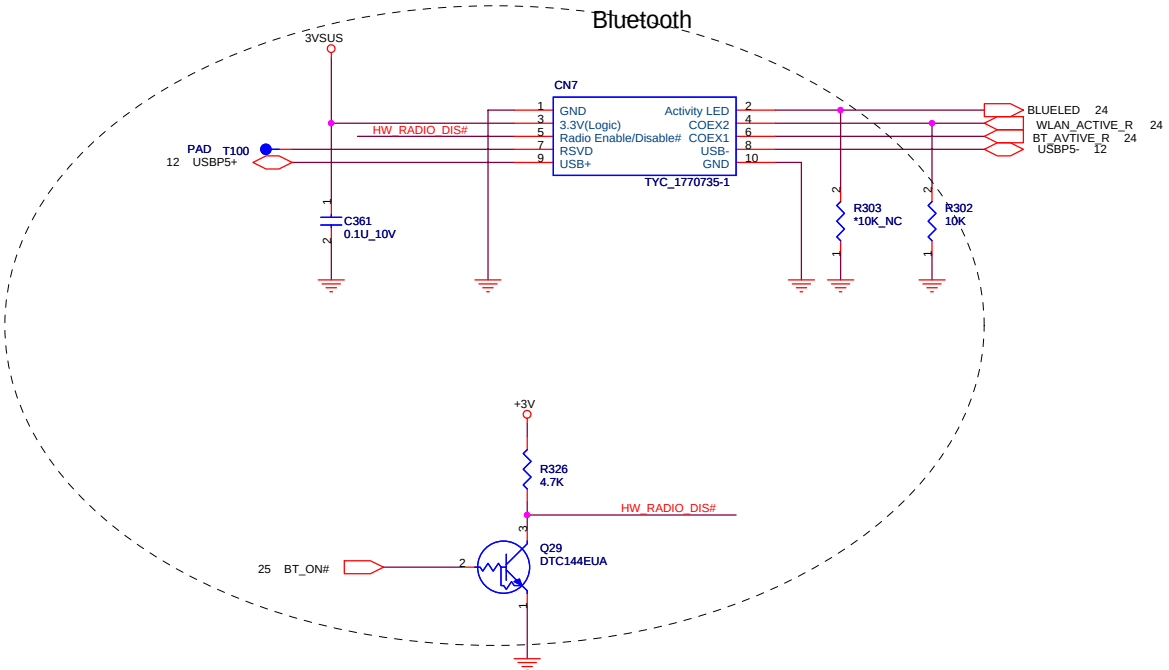
Size	Document Number	Rev
Custom	SERIAL PORT & USB	1A
Date: Wednesday, November 16, 2005	Sheet 26 of 46	

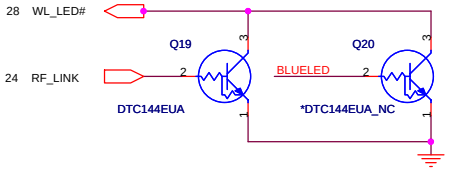
TOUCHPAD











PROJECT : SW1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	TOUCH PAD & BULE TOOTH	1A

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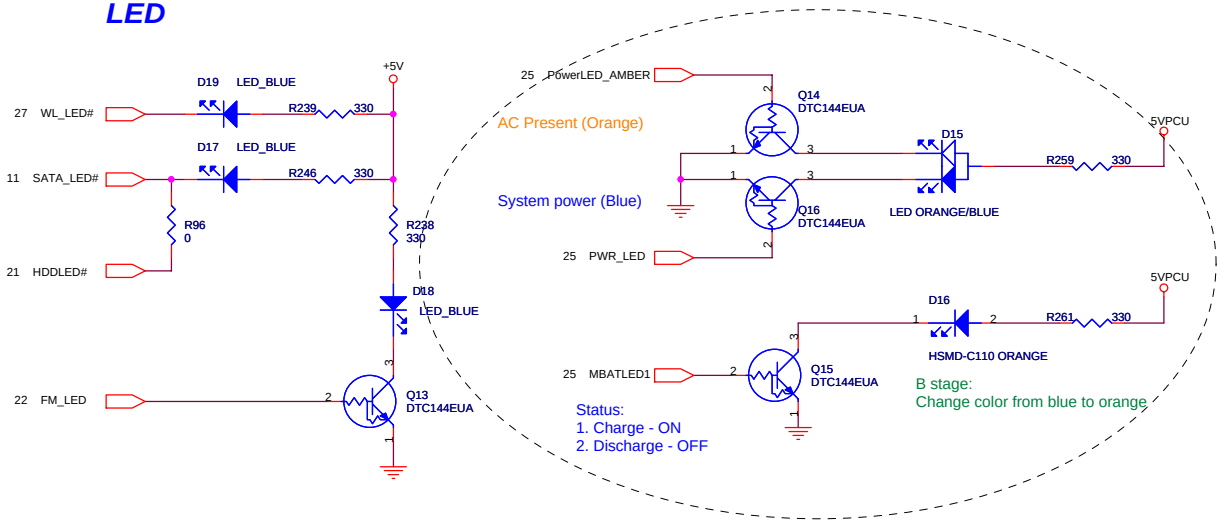
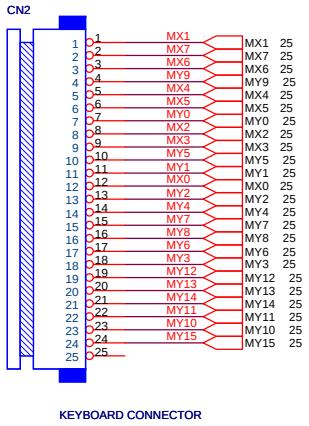
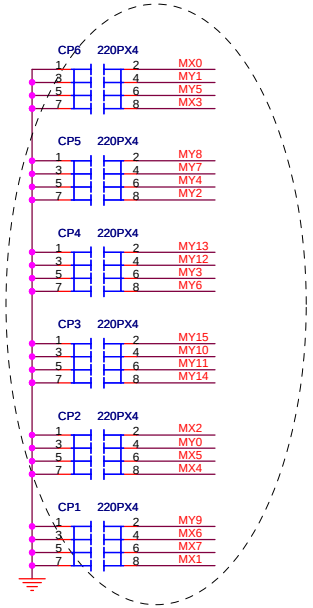
LED

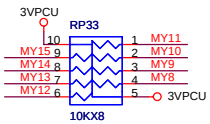


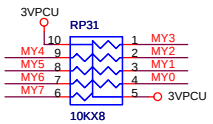
KEYBOARD

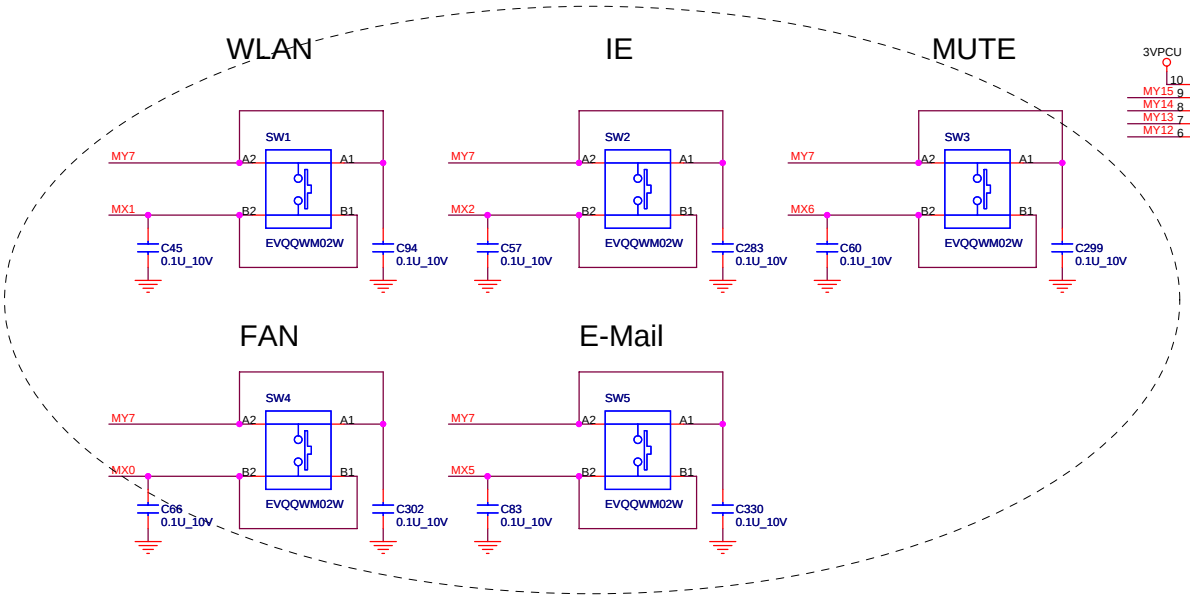


KEYBOARD CONNECTOR

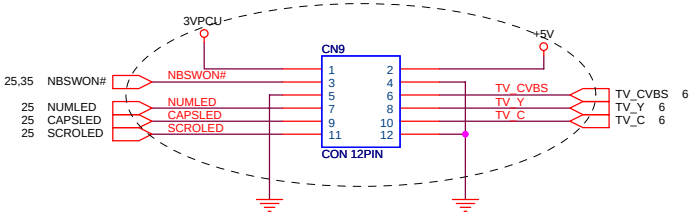








I/O Board CONN



PROJECT : SW1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SWITCH, KEYBOARD & LED	1A
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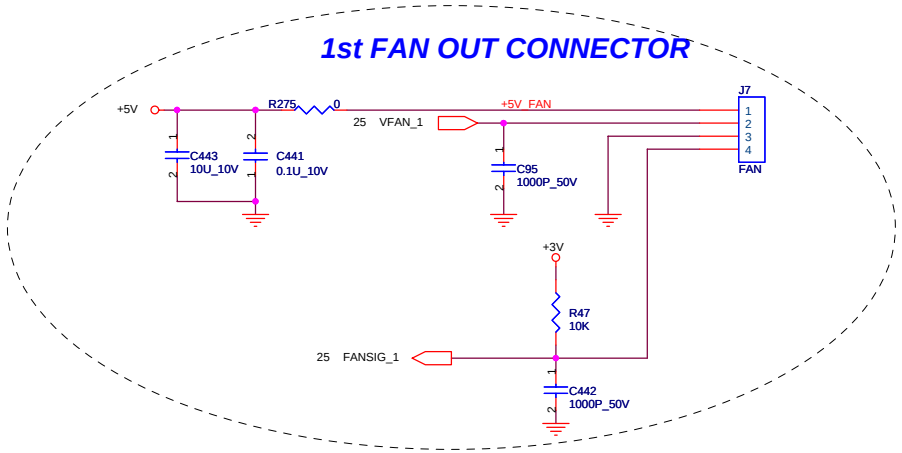
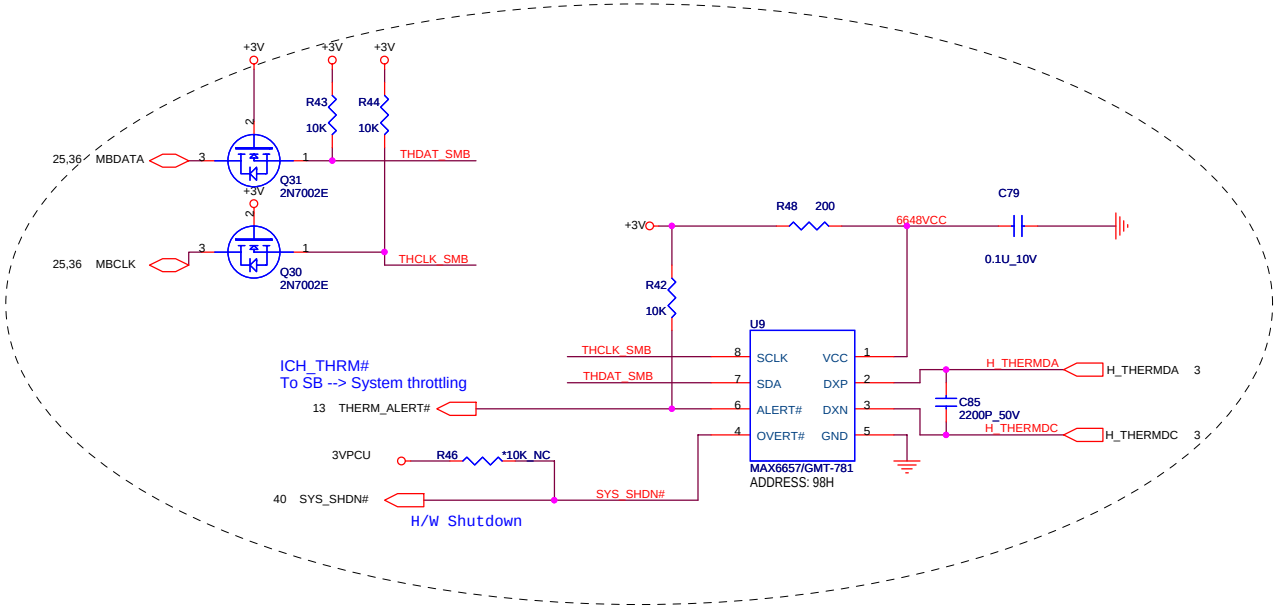
1st FAN OUT CONNECTOR





PROJECT : SW1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	FAN & THERMAL	1A

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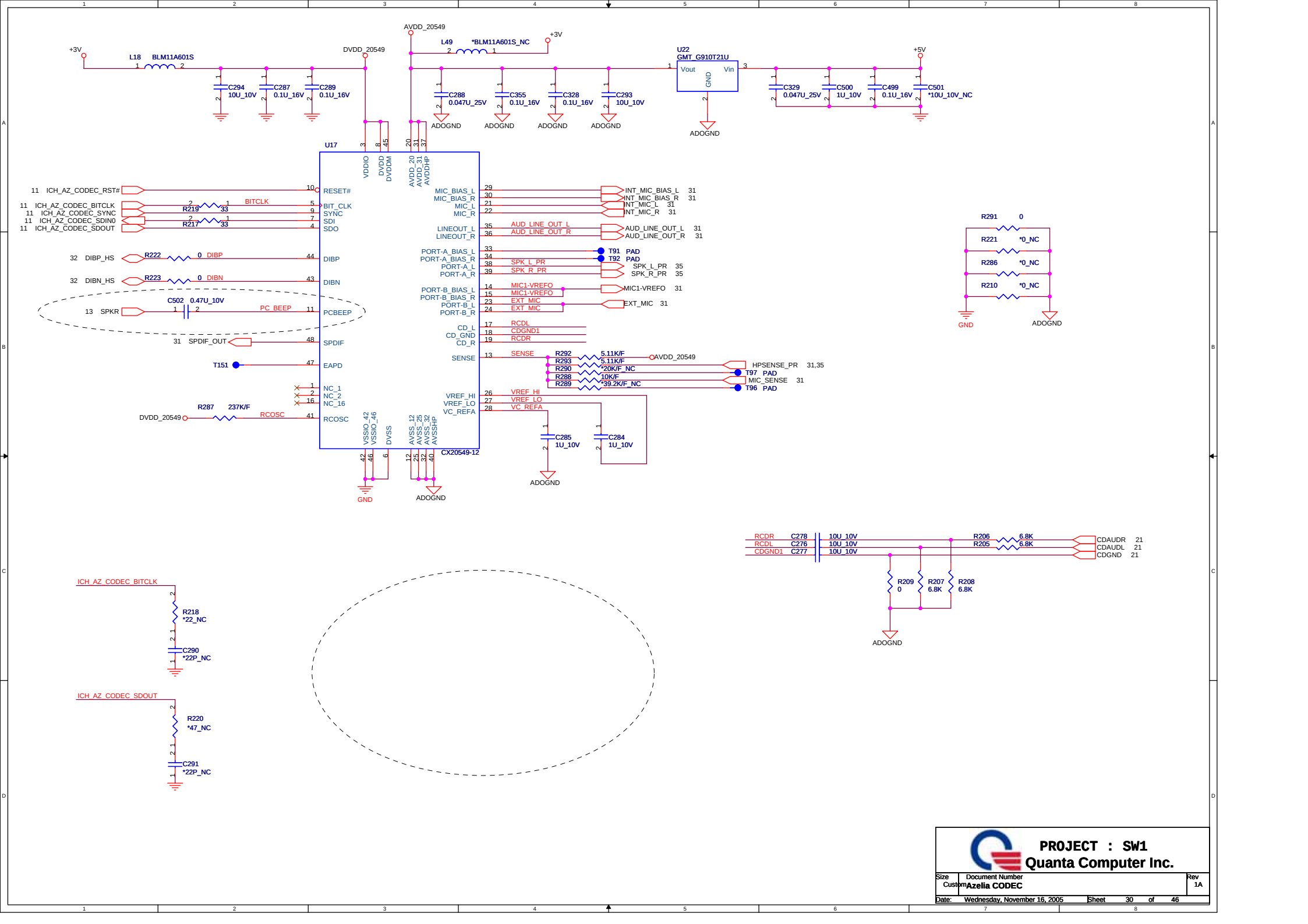
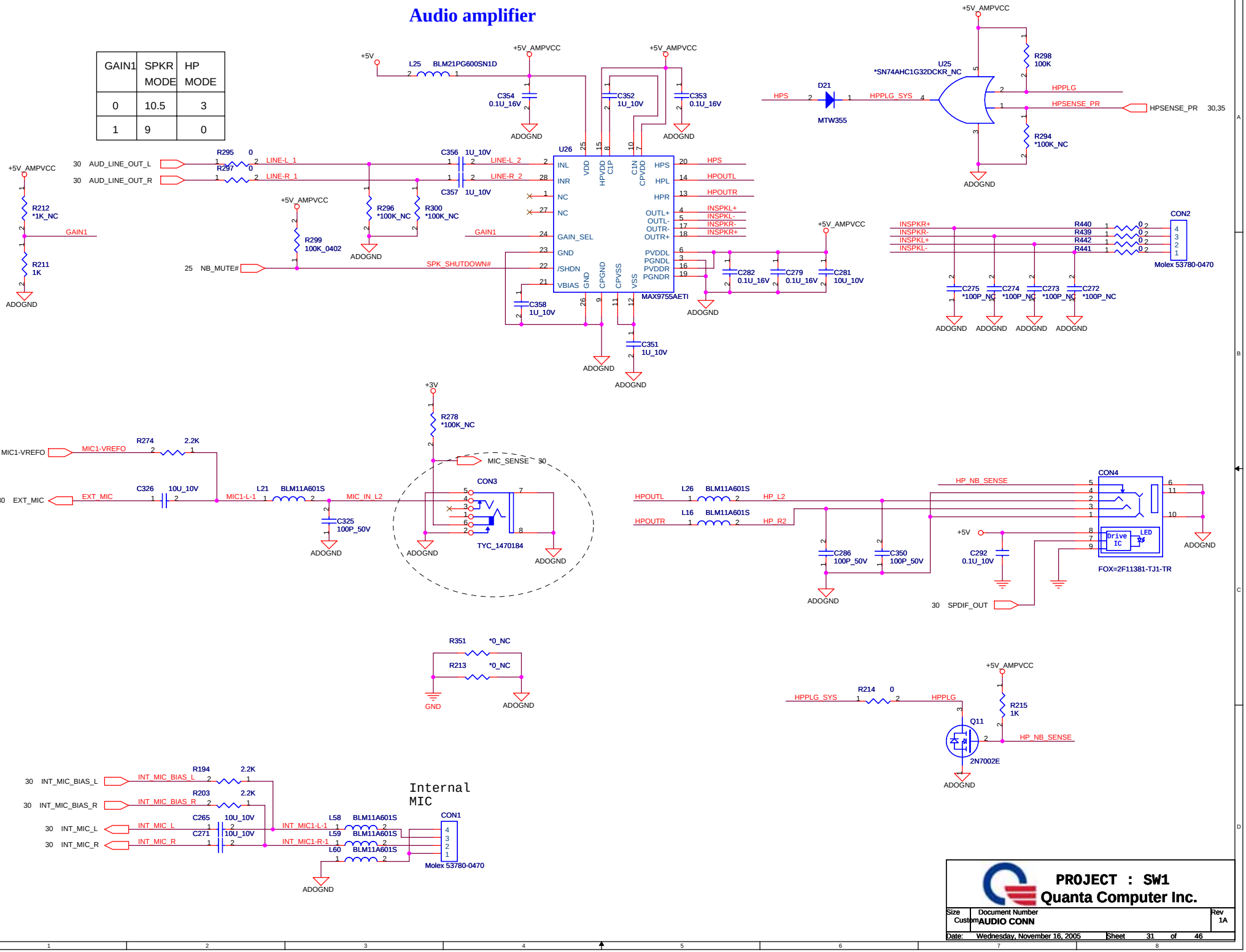


PROJECT : SW1		
Quanta Computer Inc.		
Size: Custom	Document Number: Azelia CODEC	Rev: 1A
Date: Wednesday, November 16, 2005	Sheet 30 of 46	

Audio amplifier

GAIN1	SPKR MODE	HP MODE
0	10.5	3
1	9	0



PROJECT : SW1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	AUDIO CONN	1A
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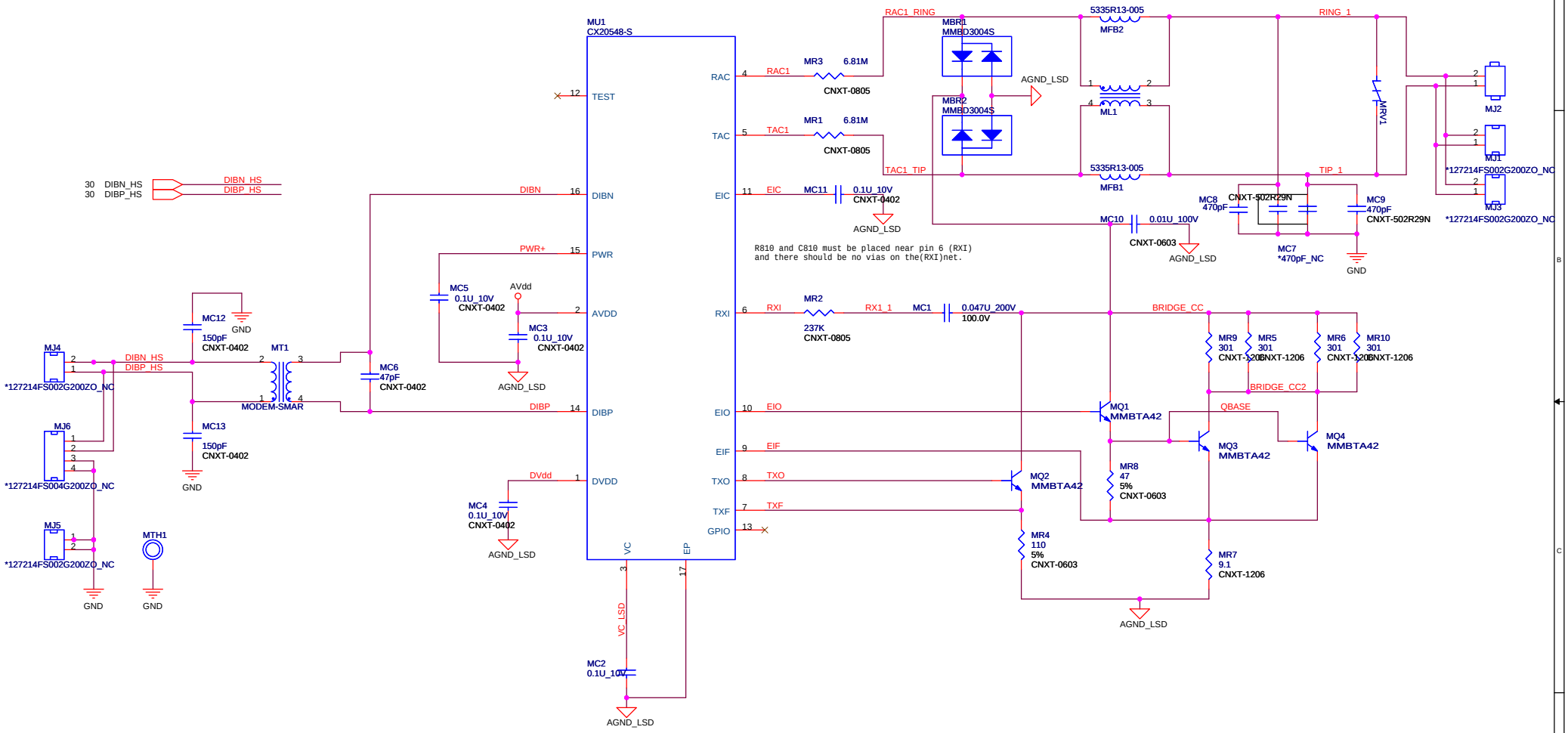

PROJECT : SW1			
Quanta Computer Inc.			
Size: Custom	Document Number: MDC		Rev: 1A
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C: 88E8053 LF PN: AJ080530010 (20050414)
1Mbits

C: Add 9 X GND Pad for LAN controller. (20050411)

C: Add these GND pin for via hole to GND Plane.

C: Add RC (R37 change to 200K, Add C101) delay to control LOM_DISABLE#. (20050411)

C: Reserve R36. Change LANRST# to PCIRST# source from MB option modify.(2005/04/11)

DELAY PIN10 AT LEAST 150ms

Populate R21 for 10/100
Populate R22 for 10/100/1000

A1A:Place termination resistors and caps as close to LAN controller as possible

PLACEMENT CLOSE TO EACH OTHER

C: Widen to 20 mils. AVDD25 to 20 mils.(20050411)

C: Widen to 20 mils. VDD to 20 mils.(20050411)

0804 REDUCING THE LANVCC NOISE

88E8036/88E8053

M24C08-WMN6TP(2.7V)

88E8038/88E8055

PROJECT : SW1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LAN(82562/82573)	1A

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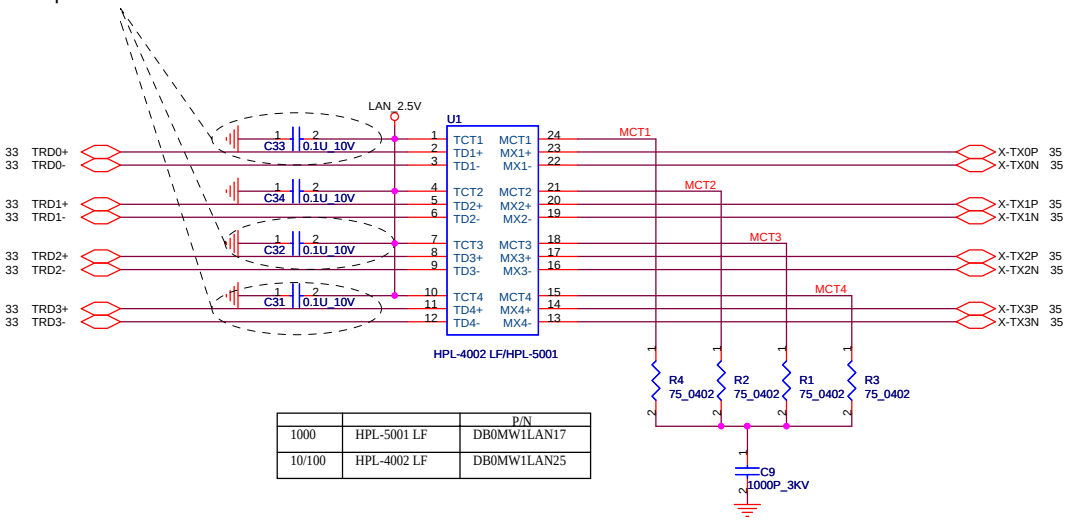
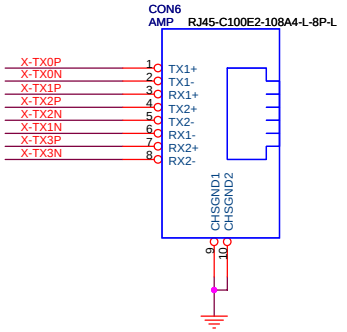
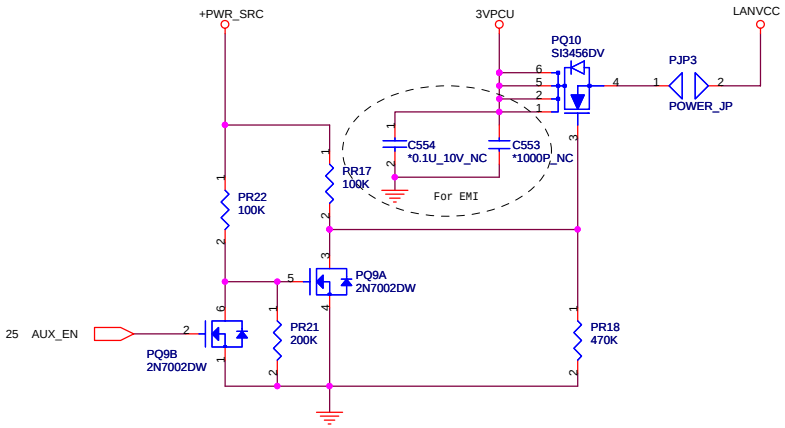
Populate for 82573



		P/N
1000	HPL-5001 LF	DB0MW1LAN17
10/100	HPL-4002 LF	DB0MW1LAN25





PROJECT : SW1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LAN RJ45	1A

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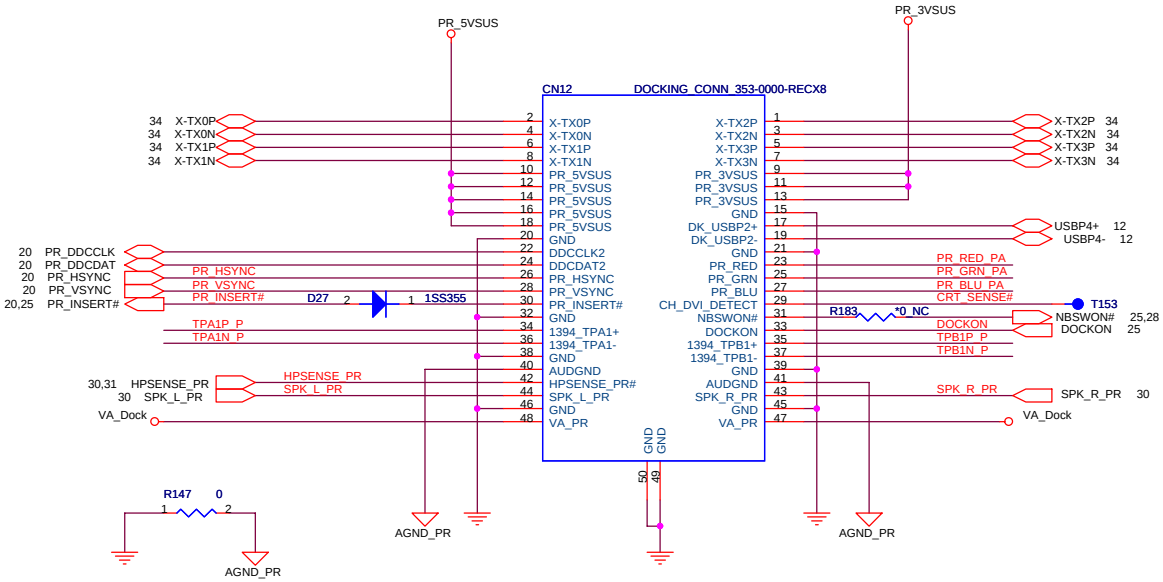
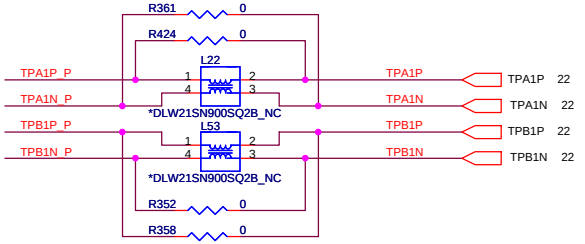
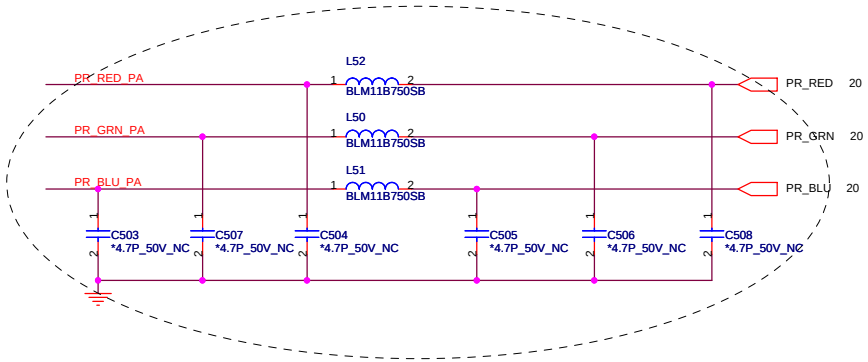
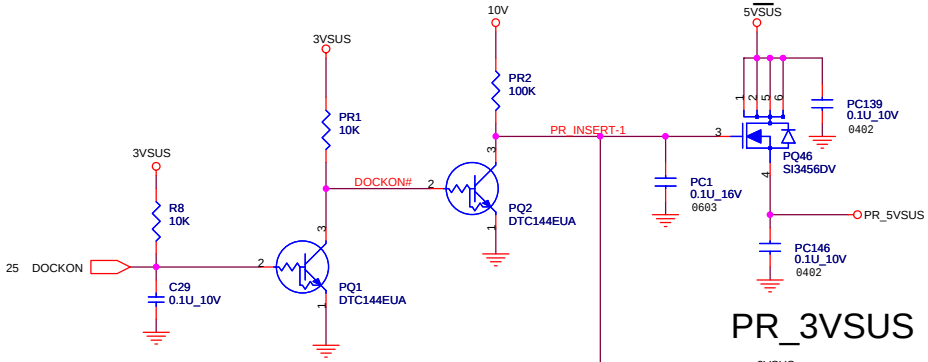
CABLE DOCKING CONNECTOR

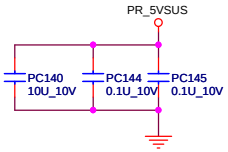




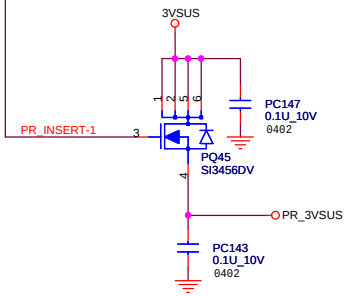


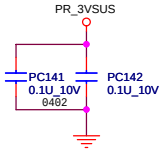
PR_5VSUS





PR_3VSUS





0402

PROJECT : SW1		
Quanta Computer Inc.		
Size: Custom	Document Number: PORT REPLICATOR	Rev: 1A
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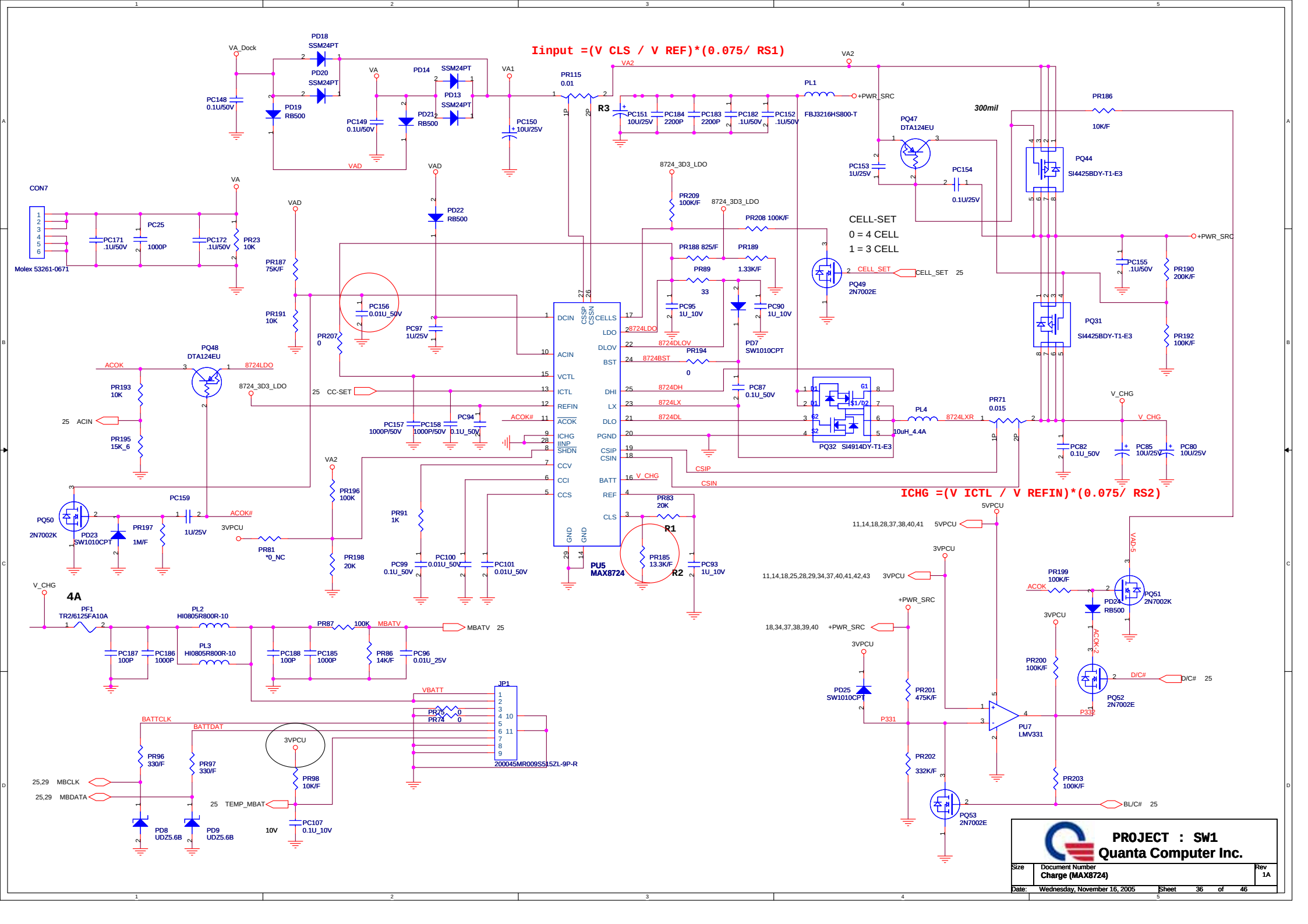
Iinput =(V CLS / V REF)*(0.075/ RS1)
ICHG =(V ICTL / V REFIN)*(0.075/ RS2)
CELL-SET
0 = 4 CELL
1 = 3 CELL
300mil
4A
PU5
MAX8724
PROJECT : SW1
Quanta Computer Inc.
Charge (MAX8724)
Wednesday, November 16, 2005
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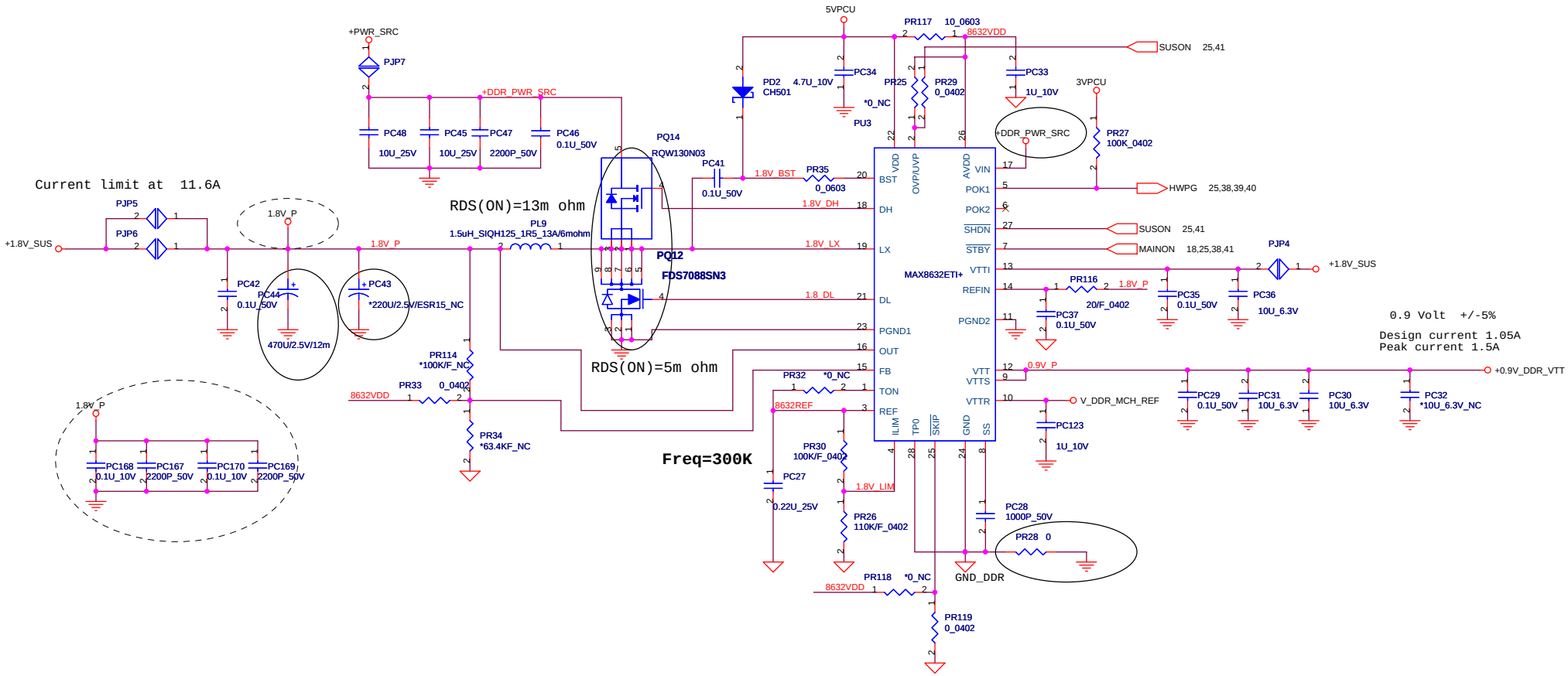
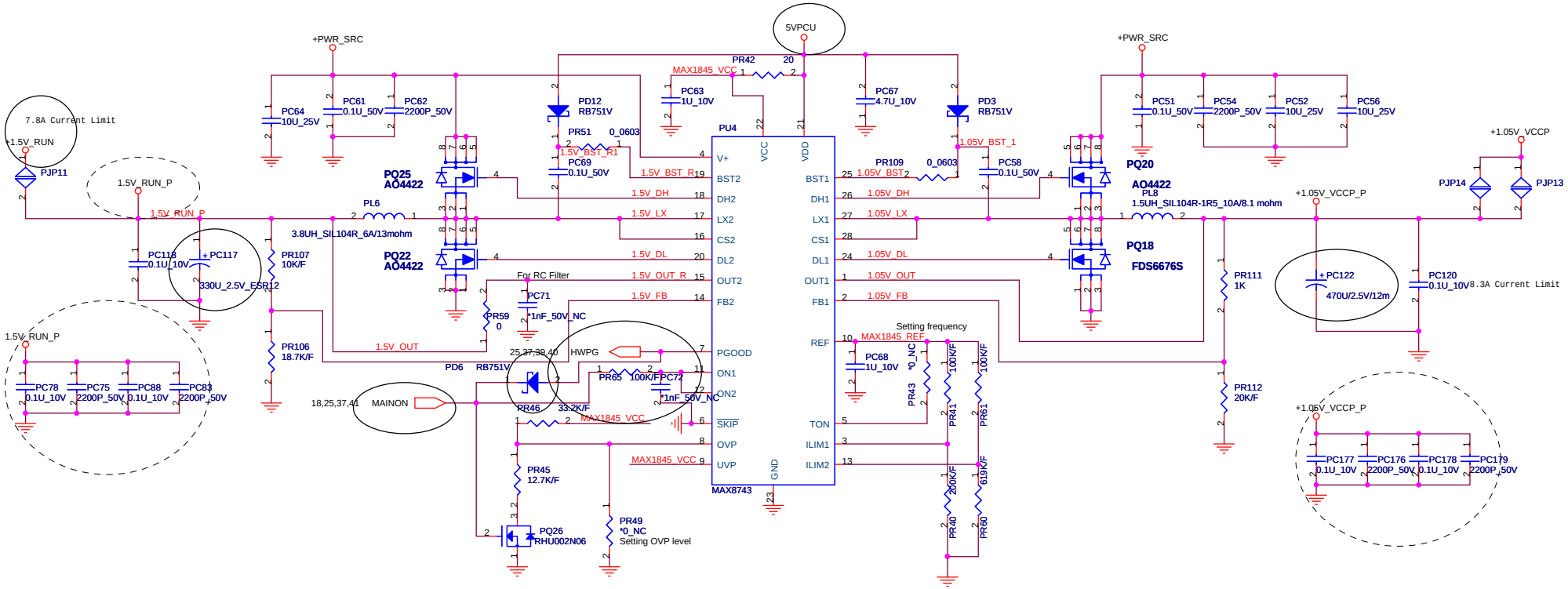

Current limit at 11.6A
RDS(ON)=13m ohm
RDS(ON)=5m ohm
Freq=300K
0.9 Volt +/-5%
Design current 1.05A
Peak current 1.5A
MAX8632ETI+
FDS7088SN3
RQW130N03
1.5uH_SIQH125_1R5_13A/6mohm
5VPCU
3VPCU
+PWR_SRC
+DDR_PWR_SRC
+1.8V_SUS
1.8V_P
1.8V_BST
1.8V_DH
1.8V_LX
1.8_DL
1.8V_LIM
8632VDD
8632REF
0.9V_P
+0.9V_DDR_VTT
V_DDR_MCH_REF
GND_DDR
SUSON 25,41
HWPG 25,38,39,40
MAINON 18,25,38,41
PJP5
PJP6
PJP7
PJP4
PL9
PQ12
PQ14
PU3
PD2 CH501 4.7U_10V
PR117 10_0603
PR25 *0_NC
PR29 0_0402
PR27 100K_0402
PR35 0_0603
PR116 20/F_0402
PR32 *0_NC
PR33 0_0402
PR34 *63.4KF_NC
PR114 *100K/F_NC
PR30 100K/F_0402
PR26 110K/F_0402
PR28 0
PR118 *0_NC
PR119 0_0402
PC27 0.22U_25V
PC28 1000P_50V
PC29 0.1U_50V
PC30 10U_6.3V
PC31 10U_6.3V
PC32 *10U_6.3V_NC
PC33 1U_10V
PC34 *0_NC
PC35 0.1U_50V
PC36 10U_6.3V
PC37 0.1U_50V
PC41 0.1U_50V
PC42 0.1U_50V
PC43 *220U/2.5V/ESR15_NC
PC44 470U/2.5V/12m
PC45 10U_25V
PC46 0.1U_50V
PC47 2200P_50V
PC48 10U_25V
PC123 1U_10V
PC168 0.1U_10V
PC167 2200P_50V
PC170 0.1U_10V
PC169 2200P_50V
PROJECT : SW1
Quanta Computer Inc.
Document Number
1.8V, 0.9V (MAX8632)
Rev 1A
Date: Wednesday, November 16, 2005
Sheet 37 of 46



PROJECT : SW1
Quanta Computer Inc.

Size	Document Number	Rev
	1.5V, 1.05V (MAX8743)	1A

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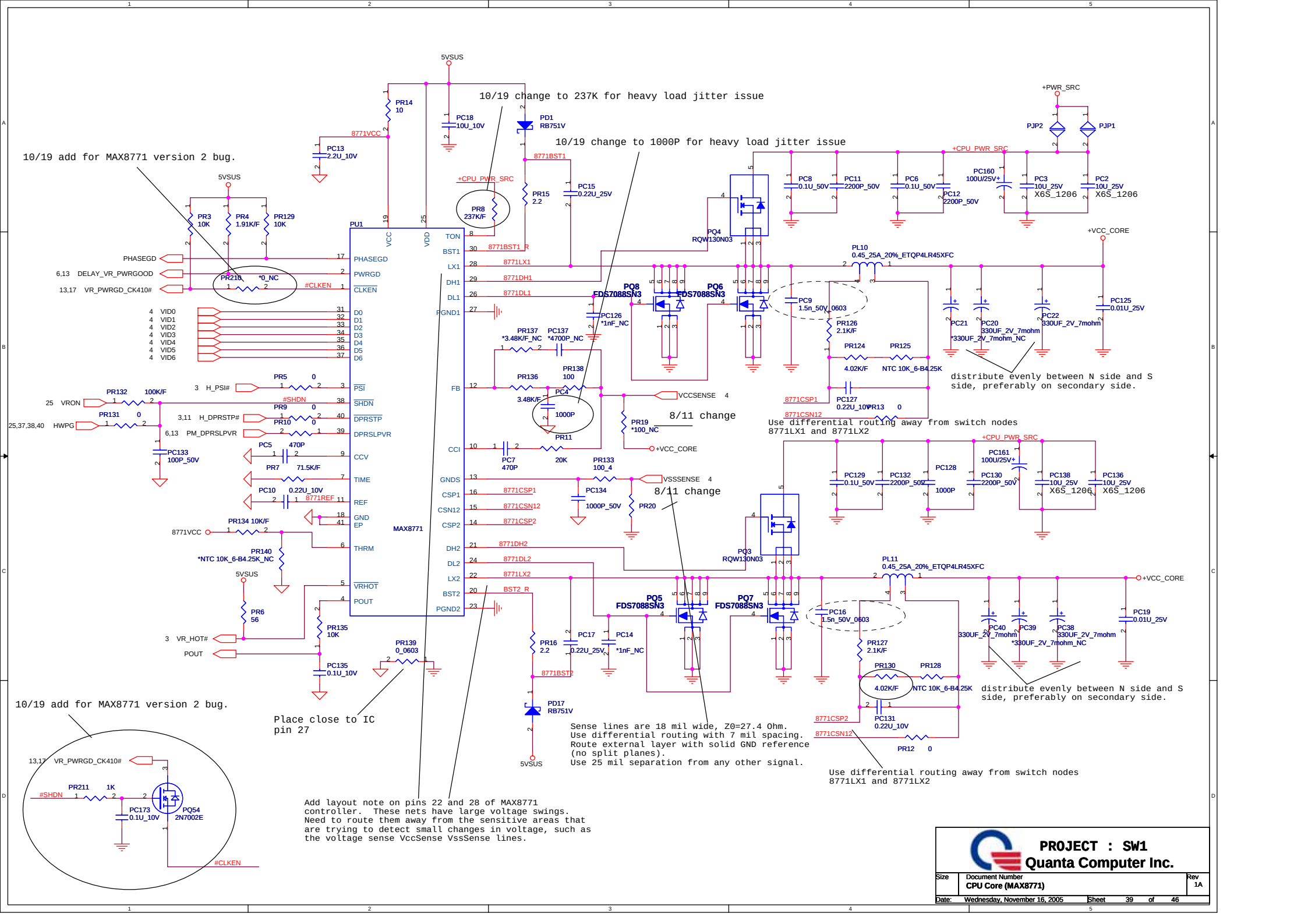
10/19 add for MAX8771 version 2 bug.
10/19 change to 237K for heavy load jitter issue
10/19 change to 1000P for heavy load jitter issue
8/11 change
8/11 change
Use differential routing away from switch nodes 8771LX1 and 8771LX2
distribute evenly between N side and S side, preferably on secondary side.
Place close to IC pin 27
Sense lines are 18 mil wide, Z0=27.4 Ohm.
Use differential routing with 7 mil spacing.
Route external layer with solid GND reference (no split planes).
Use 25 mil separation from any other signal.
Add layout note on pins 22 and 28 of MAX8771 controller. These nets have large voltage swings. Need to route them away from the sensitive areas that are trying to detect small changes in voltage, such as the voltage sense VccSense VssSense lines.
MAX8771
PROJECT : SW1
Quanta Computer Inc.
CPU Core (MAX8771)
Rev 1A
Wednesday, November 16, 2005
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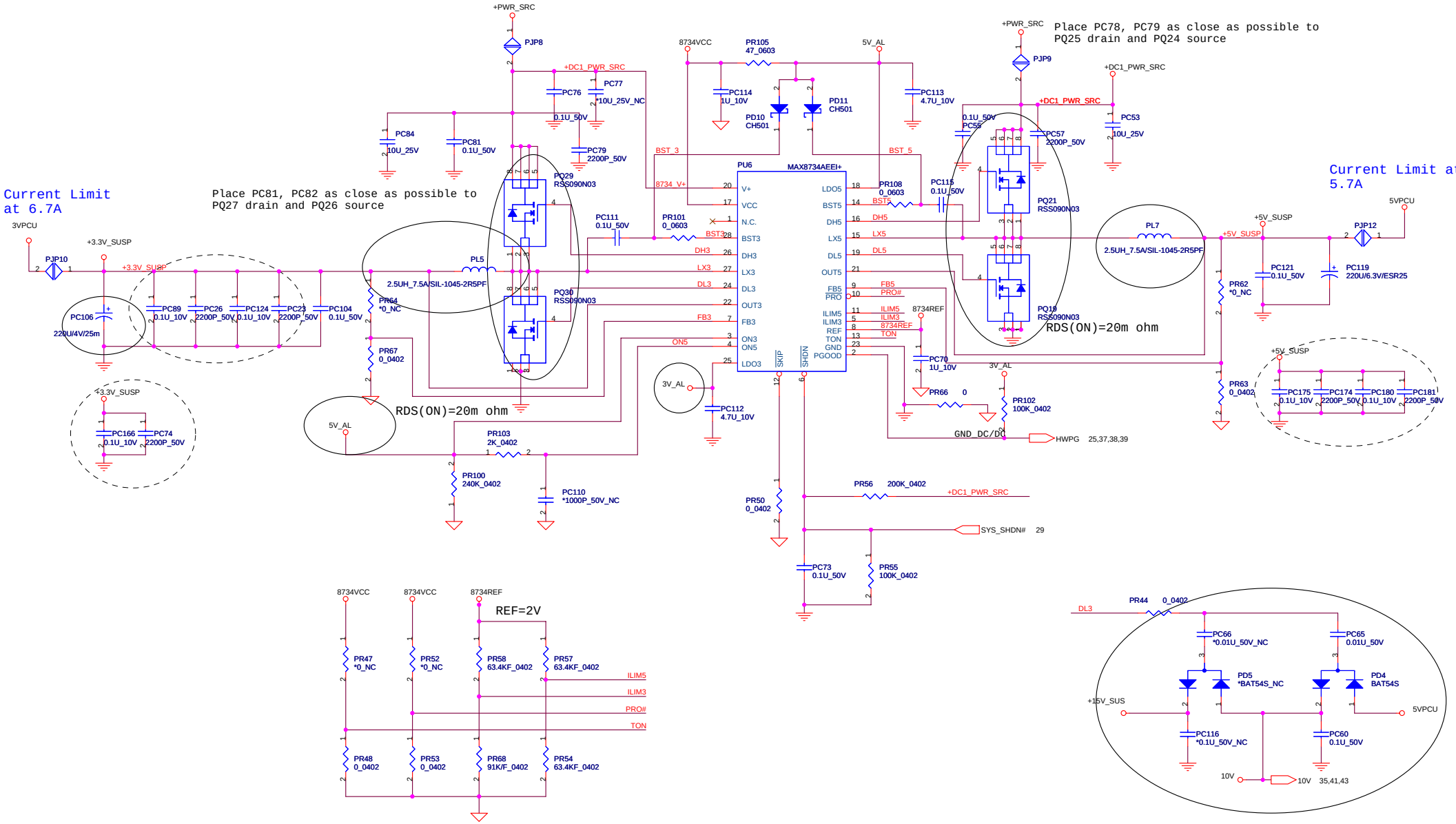

PROJECT : SW1		
Quanta Computer Inc.		
Size	Document Number: 5V,3V (MAX8734)	Rev: 1A
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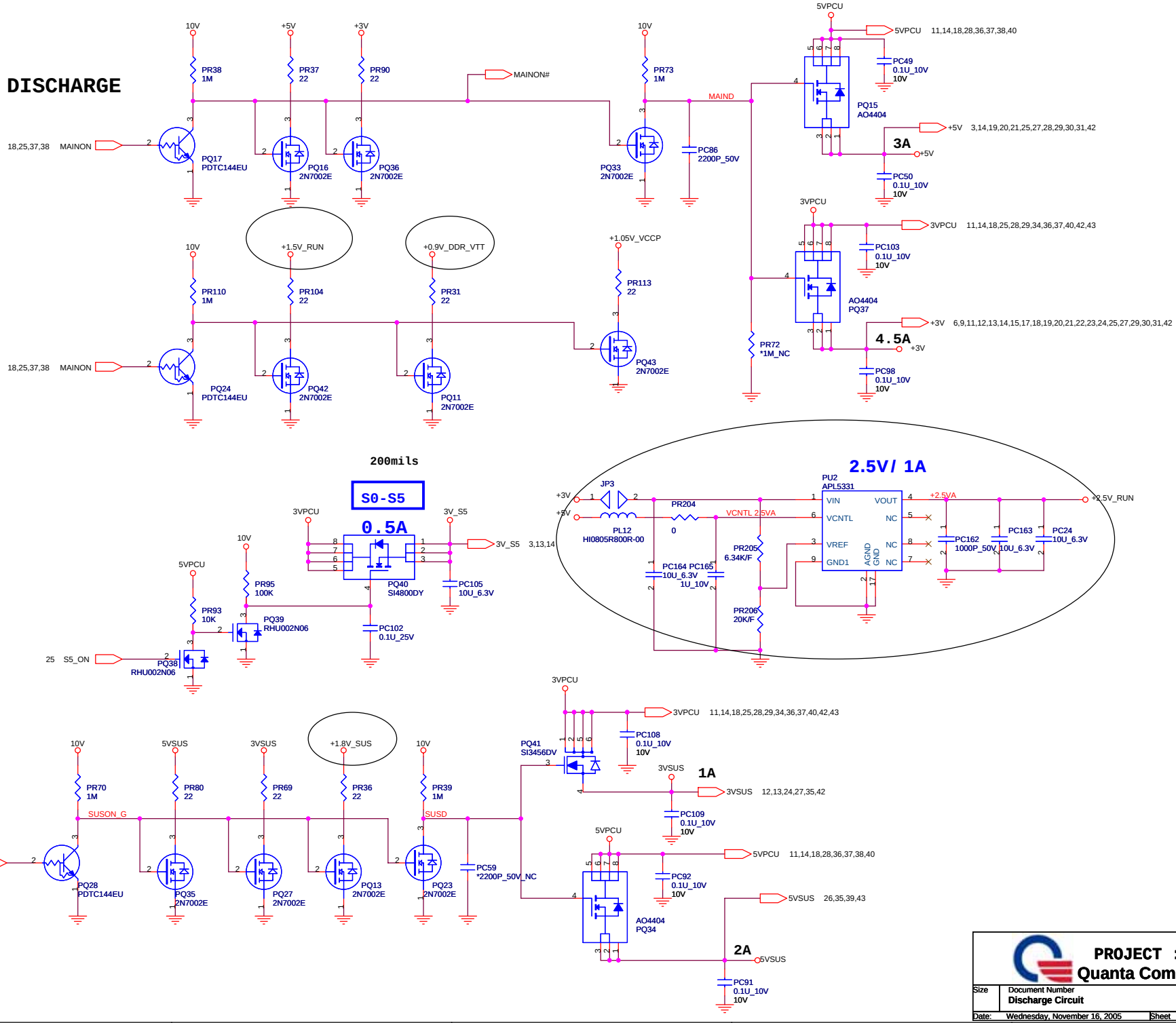
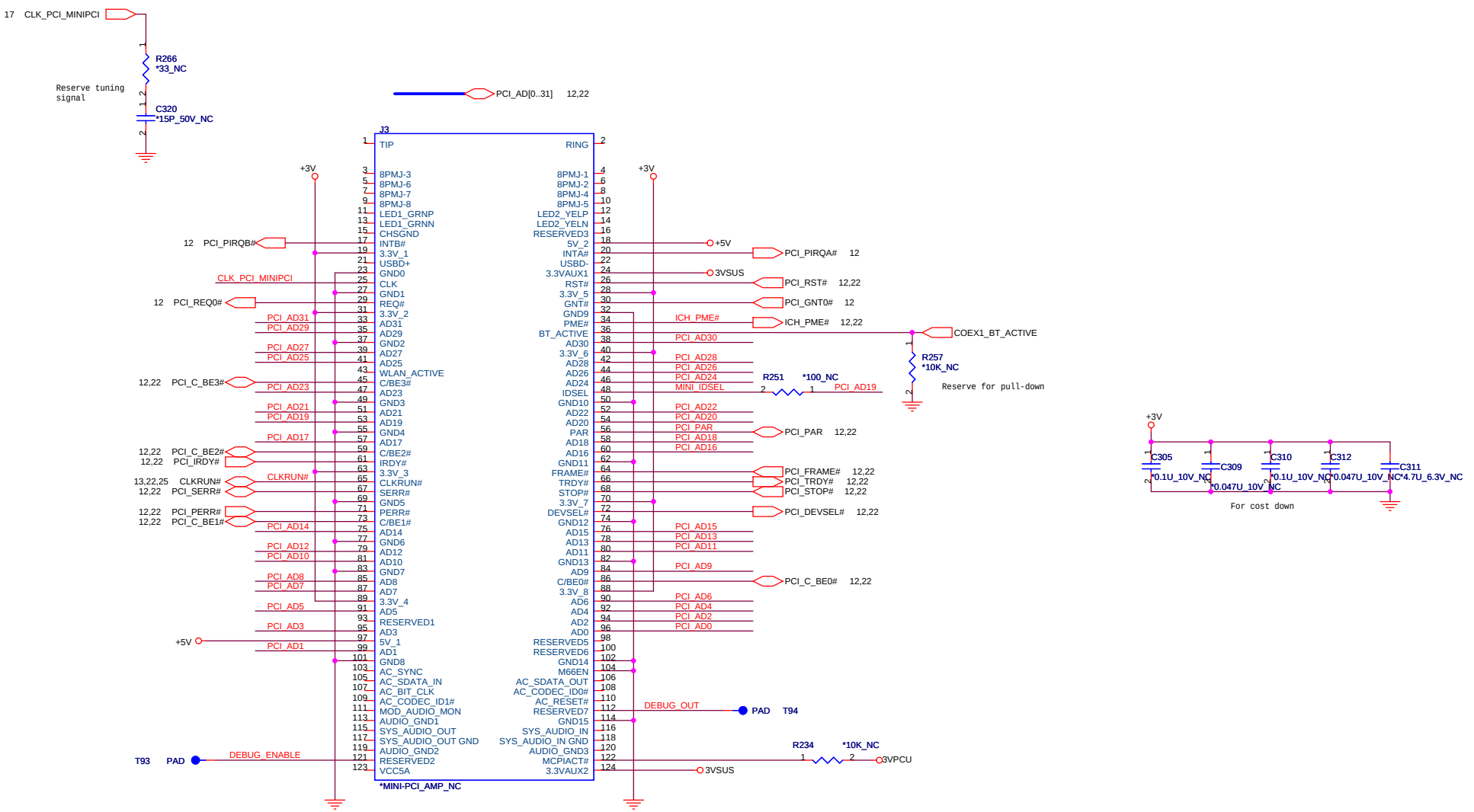
DISCHARGE

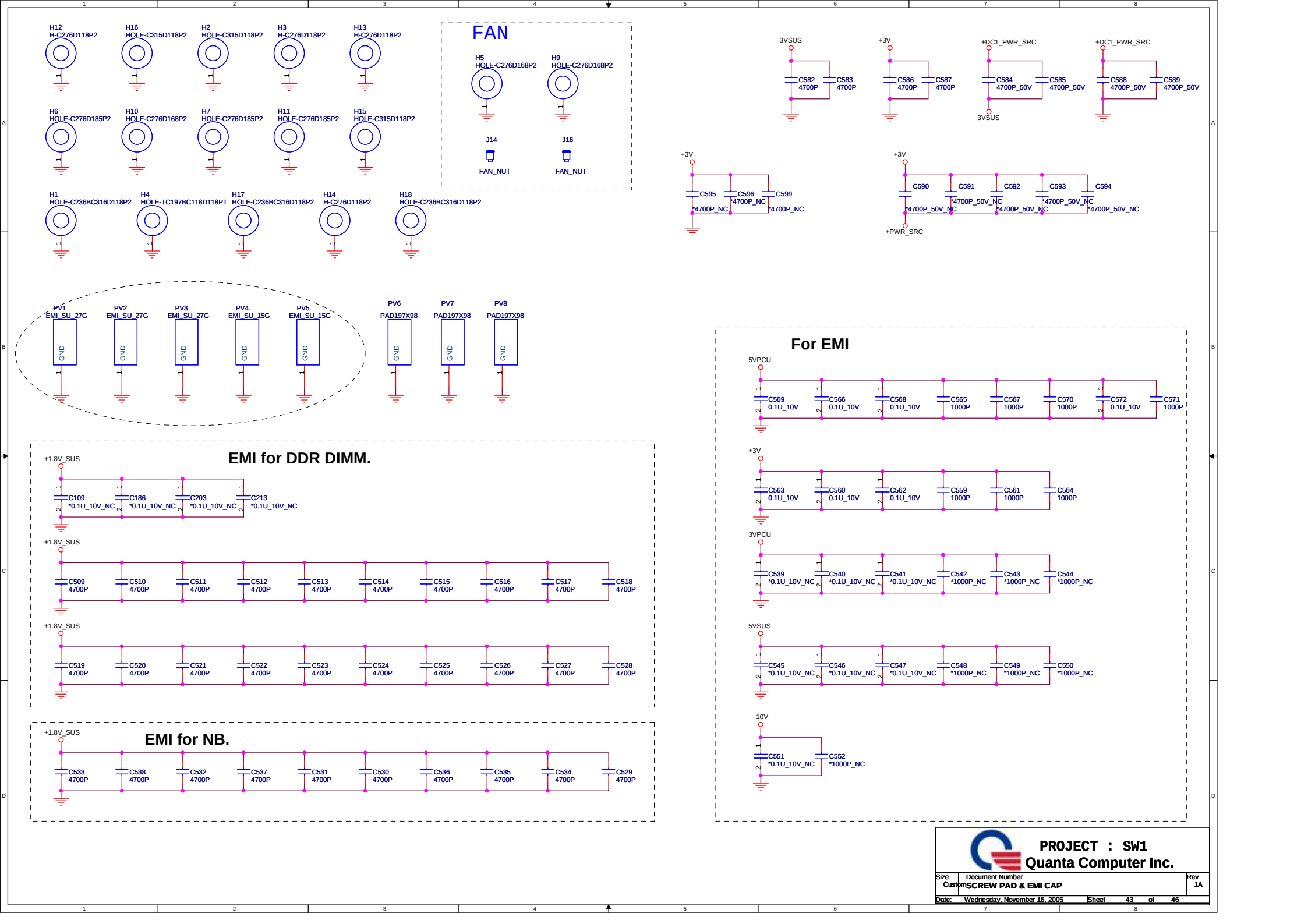


PROJECT : SW1
Quanta Computer Inc.

Size	Document Number	Rev
	Discharge Circuit	1A
Date: Wednesday, November 16, 2005	Sheet 41 of 46	



QUANTA COMPUTER		
Title: MINI-PCI &MDC		
Size	Document Number: JM5B	Rev: 3C
Date: Wednesday, November 16, 2005	Sheet 42 of 46	


H12 H-C276D118P2
H16 HOLE-C315D118P2
H2 HOLE-C315D118P2
H3 H-C276D118P2
H13 H-C276D118P2
H6 HOLE-C276D185P2
H10 HOLE-C276D168P2
H7 HOLE-C276D185P2
H11 HOLE-C276D185P2
H15 HOLE-C315D118P2
H1 HOLE-C236BC316D118P2
H4 HOLE-TC197BC118D118PT
H17 HOLE-C236BC316D118P2
H14 H-C276D118P2
H18 HOLE-C236BC316D118P2
FAN
H5 HOLE-C276D168P2
H9 HOLE-C276D168P2
J14 FAN_NUT
J16 FAN_NUT
3VSUS
C582 4700P
C583 4700P
+3V
C586 4700P
C587 4700P
+DC1_PWR_SRC
C584 4700P_50V
C585 4700P_50V
3VSUS
+DC1_PWR_SRC
C588 4700P_50V
C589 4700P_50V
+3V
C595 *4700P_NC
C596 *4700P_NC
C599 *4700P_NC
+3V
C590 *4700P_50V_NC
C591 *4700P_50V_NC
C592 *4700P_50V_NC
C593 *4700P_50V_NC
C594 *4700P_50V_NC
+PWR_SRC
PV1 EMI_SU_27G
PV2 EMI_SU_27G
PV3 EMI_SU_27G
PV4 EMI_SU_15G
PV5 EMI_SU_15G
PV6 PAD197X98
PV7 PAD197X98
PV8 PAD197X98
GND
EMI for DDR DIMM.
+1.8V_SUS
C109 *0.1U_10V_NC
C186 *0.1U_10V_NC
C203 *0.1U_10V_NC
C213 *0.1U_10V_NC
+1.8V_SUS
C509 4700P
C510 4700P
C511 4700P
C512 4700P
C513 4700P
C514 4700P
C515 4700P
C516 4700P
C517 4700P
C518 4700P
+1.8V_SUS
C519 4700P
C520 4700P
C521 4700P
C522 4700P
C523 4700P
C524 4700P
C525 4700P
C526 4700P
C527 4700P
C528 4700P
EMI for NB.
+1.8V_SUS
C533 4700P
C538 4700P
C532 4700P
C537 4700P
C531 4700P
C530 4700P
C536 4700P
C535 4700P
C534 4700P
C529 4700P
For EMI
5VPCU
C569 0.1U_10V
C566 0.1U_10V
C568 0.1U_10V
C565 1000P
C567 1000P
C570 1000P
C572 0.1U_10V
C571 1000P
+3V
C563 0.1U_10V
C560 0.1U_10V
C562 0.1U_10V
C559 1000P
C561 1000P
C564 1000P
3VPCU
C539 *0.1U_10V_NC
C540 *0.1U_10V_NC
C541 *0.1U_10V_NC
C542 *1000P_NC
C543 *1000P_NC
C544 *1000P_NC
5VSUS
C545 *0.1U_10V_NC
C546 *0.1U_10V_NC
C547 *0.1U_10V_NC
C548 *1000P_NC
C549 *1000P_NC
C550 *1000P_NC
10V
C551 *0.1U_10V_NC
C552 *1000P_NC
PROJECT : SW1
Quanta Computer Inc.
Size Custom
Document Number SCREW PAD & EMI CAP
Rev 1A
Date: Wednesday, November 16, 2005
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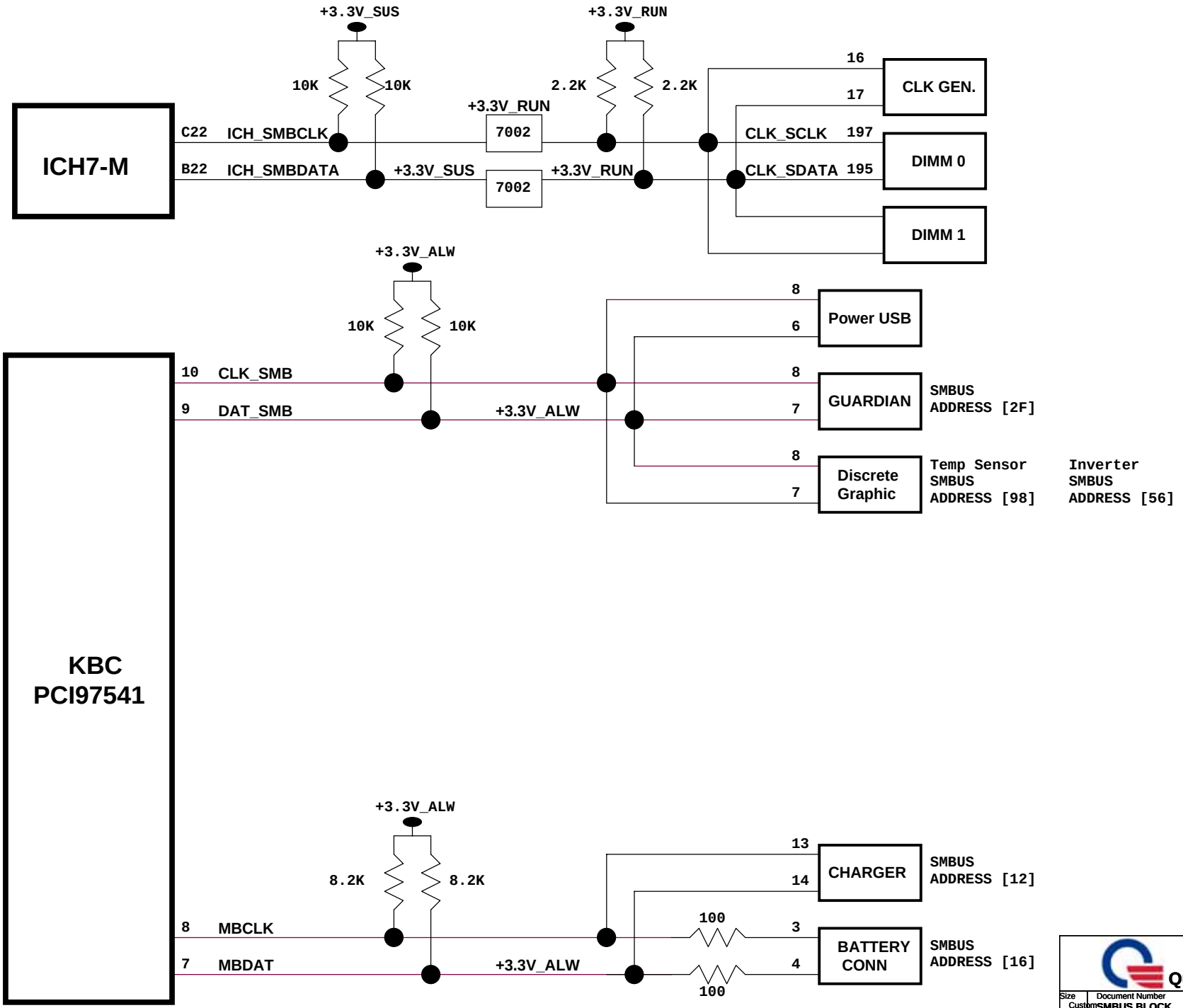

PROJECT : SW1
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