QL4 (15.6W) BLOCK DIAGRAM

01

PCB STACK UP
8L Dis. & UMA

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1
- LAYER 4 : VCC
- LAYER 5 : IN2
- LAYER 6 : IN3
- LAYER 7 : SGND2
- LAYER 8 : BOT

- UMA GPU CORE (RT8152A) PAGE 32
- SYSTEM POWER RT8206B PAGE 33
- VCCP +1.1VTT(RT8208A) AND PCH 1.05V(RT8204) PAGE 34
- CPU CORE ISL6288 PAGE 35
- VGACORE(1.025V) RT8208A PAGE 36
- DDR III SMDDR_VTERM 1.5V/1.5VSUS(RT8207) PAGE 37
- SYSTEM CHARGER(ISL6251AHAZ-T) PAGE 39

DDRIII-SODIMM1 PAGE 12 — DDRIII 800/1066 MT/s, 1333MT/s CFD only
DDRIII-SODIMM2 PAGE 13 — DDRIII 800/1066 MT/s, 1333MT/s CFD only

CPU
Auburndale 35W
Clarksfield 45W
PAGE 3~6

DMI LINK

27MHz

PCI-Express 16X

nVIDIA (40nm)
N10M-GE
N10P-GE
128 Bit
969p
PAGE 41~42

Switchable IC
PAGE 32~33

- HDMI CON PAGE 22
- CRT PAGE 22
- LCD CONN PAGE 21

32.768KHz 25MHz

SATA - HDD PAGE 31 — SATA0 150MB
SATA - CD-ROM PAGE 31 — SATA1 150MB
E-SATA PAGE 30 — SATA5 150MB

HDMI
CRT
LVDS

PCH
Ibex-M
PAGE 7~11

CLOCK GEN
9LRS3197
PAGE 2
14.318MHz

Mini PCI-E Card x2
Express Card x1
7,10,11

USB2.0

- 0,1,2 — USB2.0 Ports X3 PAGE 24
- 8 — BlueTooth PAGE 24
- 9 — Webcam PAGE 21
- 6 — RTS5159 PAGE 23

PCI-E

- X1 — Mini PCI-E Card WWAN/TV PAGE 30
- X1 — LAN Atheros PCIE-LAN AR8131(M) GagaLAN PAGE 26
- X1 — Express Card PAGE 27

25MHz

RJ45 PAGE 26

Azalia

Analog ALC272 PAGE 24

AUDIO Amplifier TPA6017A2 PAGE 25

- microphone PAGE 24
- Audio Jacks (Phone/ MIC) PAGE 24
- Jack to Speaker PAGE 25

32.768KHz

Keyboard PAGE 28
Touch Pad PAGE 27

ENE KBC
KB3926 C0
PAGE 29

LPC

- GMT G9931P1U FAN PAGE 28
- SPI PAGE 29

ONFI

- Braidwood PAGE 31
- SPI PAGE 7
- MDC CONN PAGE 26

NB5

PROJECT : QL4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	E

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CLOCK GENERATOR

+1.05V L23 HCB1608KF-181T15_6 +VDDIO_CLK

C459 .1U/10V_4
C453 .1U/10V_4
C450 10U/6.3V_6S
C458 10U/6.3V_6S

Place each 0.1uF cap as close as possible to each VDD IO pin. Place the 10uF caps on the VDD_IO plane.

U19 RTM875N-632-GRT (QFN32)

+3V

C451 4.7U/6.3V_6
C471 4.7U/6.3V_6
C452 .1U/10V_4
C454 .1U/10V_4
C470 .1U/10V_4
C469 .1U/10V_4
C464 .1U/10V_4

+VDDIO_CLK

VDD_USB, VDD_LCD, VDD_SRC, VDD_CPU, VDD_REF
VDD_CPU_IO, VDD_SRC_IO
SDATA, SCLK
CPU_STOP#, REF_0/CPU_SEL
CK_PWRGD/PD#_3.3
XOUT, XIN
VSS_SATA, VSS_USB, VSS_LCD

CPU-0, CPU-0#
CPU-1, CPU-1#
DOT96T_LPR, DOT96C_LPR
SRC-1, SRC-1#
SATA, SATA#
27MHz_nonSS, 27MHz_SS
GND, VSS_REF, VSS_CPU, VSS_SRC

[8,12,13,27,30] CGDAT_SMB
[8,12,13,27,30] CGCLK_SMB

[8] CLK_ICH_14M — R296 10K/F_4 — R300 33_4 — CPU_SEL — C465 10P/50V_4

Place the 33 ohm resistors close to the CK 505

CK_PWRGD_R

XTAL_OUT, XTAL_IN

CLK_BUF_BCLK_P [8]
CLK_BUF_BCLK_N [8]
133 or 100 Mhz output to PCH

CLK_BUF_DREFCLK [8]
CLK_BUF_DREFCLK# [8]
96Mhz output for generate 48Mhz (USB) and 24 Mhz (HDA)clk

CLK_BUF_PCIE_3GPLL [8]
CLK_BUF_PCIE_3GPLL# [8]
100Mhz output for DMI reference clk

CLK_BUF_DREFSSCLK [8]
CLK_BUF_DREFSSCLK# [8]
100Mhz output for SATA reference clk

CLK_VGA_27M_NOSS R308 33_4 → CLK_27M_NONSS [16]
CLK_VGA_27M_SS R309 33_4 → CLK_27M_SS [16]

Discrete and Hybrid

+3V R295 1K/F_4 CK_PWRGD_R

Q10 2N7002E

[37] VR_PWRGD_CLKEN# — R297 100K/F_4

Y3 14.318MHZ
C461 33P/50V_4
C457 33P/50V_4

+3V R303 *10K/F_4 CPU_SEL R306 10K/F_4

	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

CPU bracket Hole.

H5 H6 H10 H11 *H-tc295bc220d161p2

B-stage change

VGA bracket Hole.

H8 H12 H13 *H-tc295bc220d161p2

B-stage change

PAD and HOLE

H1 *H-tj4-1
H7 *H-c315d106p2
H2 *H-c315d106p2
H22 *H-tj4-3
H25 *H-C315D106P2
H15 *H-c315d106p2
H16 *H-c315d106p2
H18 *H-tC130bc197d130pb
H14 *O-O236X669D236X669N
H17 *H-tc421x335bc315d106p2
H23 *H-c315d106p2
H4 *H-C315D106P2
H9 *H-tj4-2
H3 *H-C315D130P2
H24 *H-TC130BC197D130PB

PAD2 MDC_SPRING
PAD1 MDC_SPRING

PAD3 PAD4 PAD5 *EMI_PAD
PAD6 PAD7 PAD8 *EMI_PAD

MINI CARD Hole.

H26 H30 H27 H29 *H-tc67bc276d67p2
H-TC161BC276D161P2
H28 *H-tc67bc276d67p2
H20 *H-TC161BC276D161P2

H31 *EMIPAD236X591B
H32 *emipad472x1220
H33 *emipad236x591b

[7,8,9,11,29,34,36,42] +1.05V
[3,7,8,9,10,11,12,13,21,22,23,24,25,26,27,28,29,30,31,32,33,37,40,42] +3V

MDC Hole.

H21 H19 *H-tc148bc256d148p2

EMI solution.

B-stage change

C773 .1U/25V_4 +VIN
C966 .1U/25V_4 +VIN
LAN_AGND1 R796 0_4

NB5

PROJECT : QL4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CLOCK & Screw Holes	E

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	DIS	UMA
Ra	NA	0 ohm
Rb	0 ohm	NA
Rc	0 ohm	NA

U29A

DMI

Intel(R) FDI

PCI EXPRESS -- GRAPHICS

IC,AUB_CFD_rPGA,R1P0

2.7GT/s data rate

U29B

MISC

THERMAL

CLOCKS

DDR3 MISC

PWR MANAGEMENT

JTAG & BPM

IC,AUB_CFD_rPGA,R1P0

PV 0616 DEL debug Con.

JTAG MAPPING

Scan Chain (Default)	STUFF -> R97, R89, R90 NO STUFF -> R84, R512
CPU Only	STUFF -> R97, R84 NO STUFF -> R89, R512, R90
GMCH Only	STUFF -> R512, R90 NO STUFF -> R97, R84, R89

Use a voltage divider with VDDQ (1.5V) rail (ON in S3) and resistor combination of 4.75K (to VDDQ)/12K(to GND) to generate the required voltage.
Note: CRB uses a 3.3V (always ON) rail with 2K and 1K combination.

NB5

PROJECT : QL4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSER 1/4(HOST&PEX)	E

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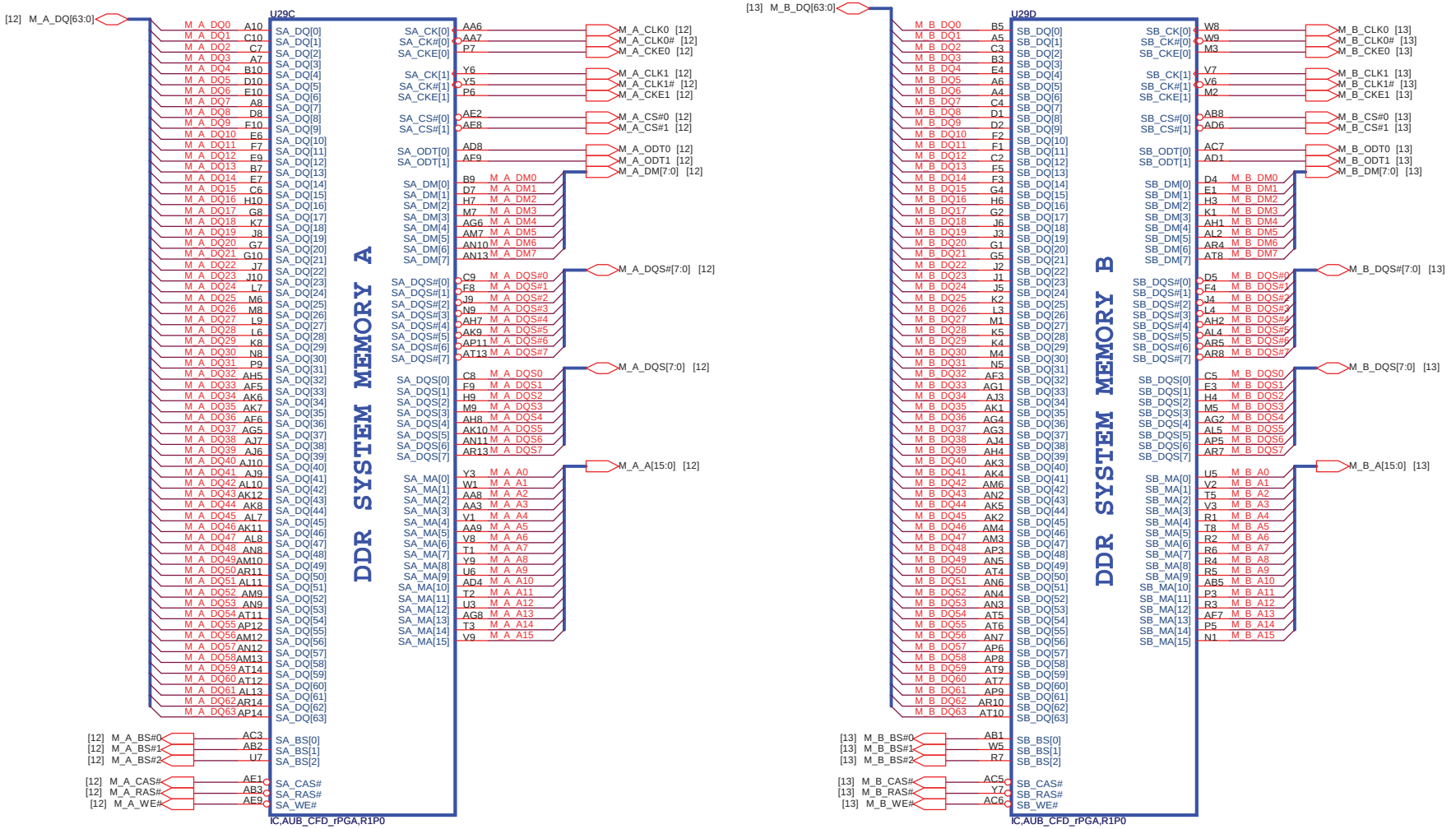
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



PROJECT : QL4 Quanta Computer Inc.		
NB5	Size: Custom; Document Number: PROCESSER 2/4(DDR)	Rev: E
	Date: Friday, October 09, 2009	Sheet 4 of 44

	DIS	UMA
Rc	NA	4.7K
Rd	NA	0 ohm
Re	NA	0 ohm
Rf	NA	NA

	DIS	UMA
Ra	0 ohm	NA

U29F

POWER

CPU CORE SUPPLY

1.1V RAIL POWER

CPU VIDS

SENSE LINES

IC,AUB_CFD_rPGA,R1P0

Please note that +VCC_GFX_CORE should be 1.05V in Auburndale

VTT Rail Values are
Auburndal VTT=1.05V
Clarksfield VTT=1.1V

H_VTTVID1=Low, 1.1V
H_VTTVID1=High, 1.05V

U29G

POWER

GRAPHICS

SENSE LINES

GRAPHICS VIDs

DDR3 - 1.5V RAILS

FDI

PEG & DMI

1.1V

1.8V

IC,AUB_CFD_rPGA,R1P0

HFM_VID : Max 1.4V
LFM_VID : Min 0.65V

Q3 AON6426L

Q34 BSS138

PROJECT : QL4
Quanta Computer Inc.

NB5

Size: Custom | Document Number: PROCESSER 3/4(POWER) | Rev: E

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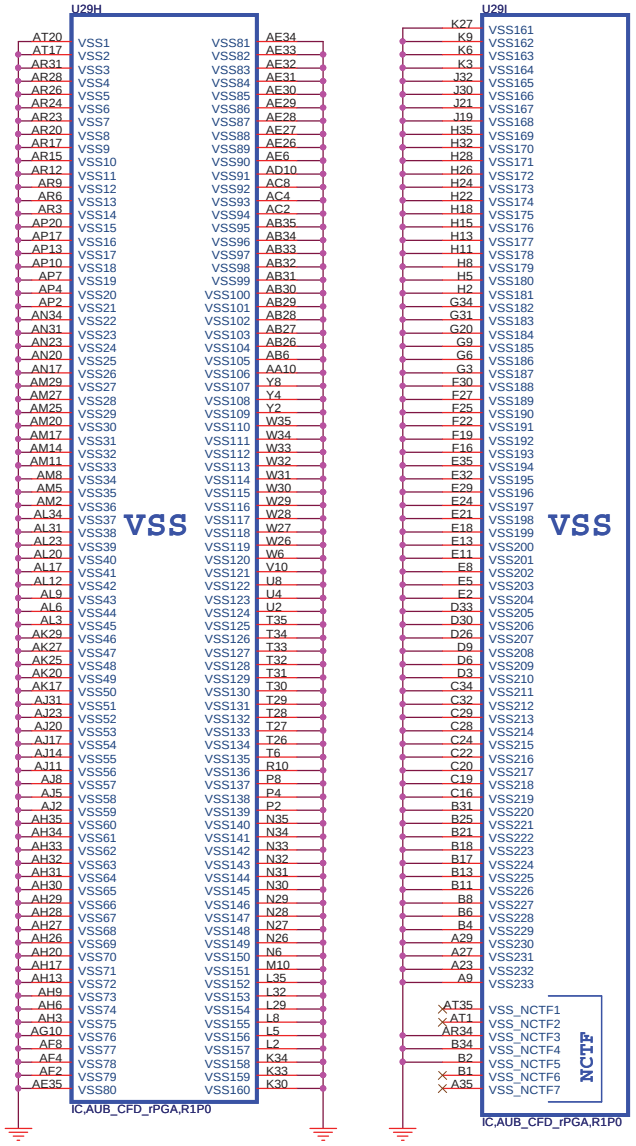
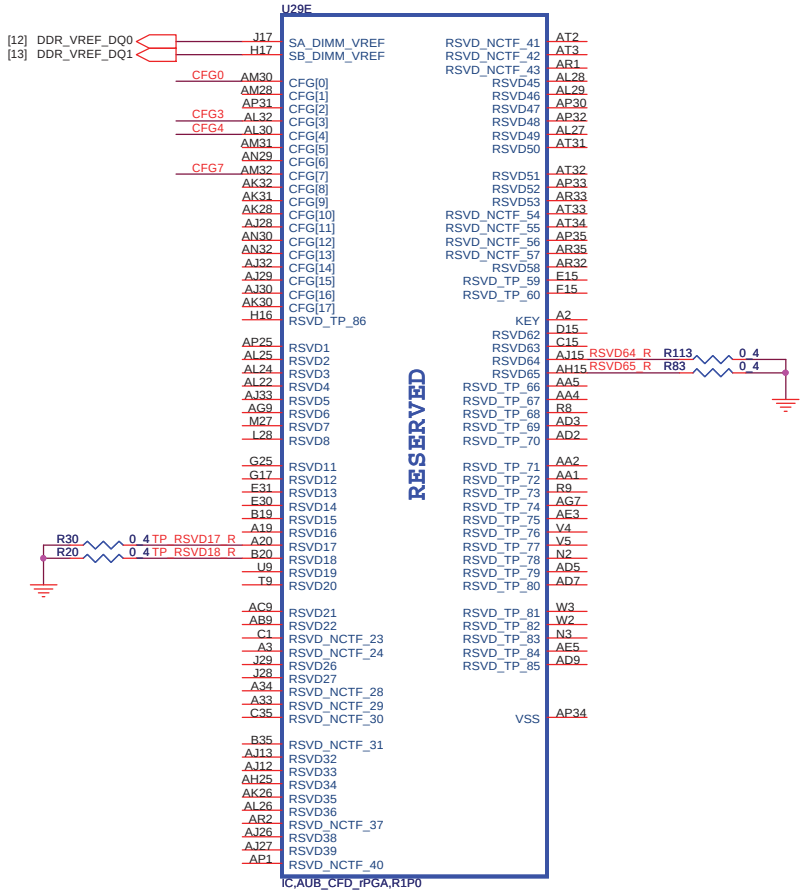
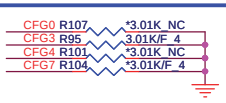
AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)





For Discrete only

```
CFG[ 1:0 ] - PCI_Epress Configuration Select
* 11= 1 x 16 PEG
* 10= 2 x 8 PEG
```

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

NB5

PROJECT : QL4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSER 4/4(GND)	E
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INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

IBEX PEAK-M (HDA,JTAG,SATA)

U35A

Ibex-M 1 OF 10

RTC: RTCX1, RTCX2, RTCRST#, SRTCRST#, INTRUDER#, INTVRMEN

IHDA: HDA_BCLK, HDA_SYNC, SPKR, HDA_RST#, HDA_SDIN0, HDA_SDIN1, HDA_SDIN2, HDA_SDIN3, HDA_SDO, HDA_DOCK_EN# / GPIO33 (+3V), HDA_DOCK_RST# / GPIO13 (+3V_S5)

JTAG: JTAG_TCK, JTAG_TMS, JTAG_TDI, JTAG_TDO, TRST#

must add test point.

SPI: SPI_CLK, SPI_CS0#, SPI_CS1#, SPI_MOSI, SPI_MISO

LPC: FWH0 / LAD0, FWH1 / LAD1, FWH2 / LAD2, FWH3 / LAD3, FWH4 / LFRAME#, LDRQ0#, (+3V) LDRQ1# / GPIO23, SERIRQ

SATA: SATA0RXN, SATA0RXP, SATA0TXN, SATA0TXP, SATA1RXN, SATA1RXP, SATA1TXN, SATA1TXP, SATA2RXN, SATA2RXP, SATA2TXN, SATA2TXP, SATA3RXN, SATA3RXP, SATA3TXN, SATA3TXP, SATA4RXN, SATA4RXP, SATA4TXN, SATA4TXP, SATA5RXN, SATA5RXP, SATA5TXN, SATA5TXP, SATAICOMPO, SATAICOMPI, SATALED#, (+3V) SATA0GP / GPIO21, (+3V_S5) SATA1GP / GPIO19

SATA HDD1

SATA ODD

Port2 and Port3 HM55 not support

E-SATA

IbexPeak-M_Rev1_0

IBEX PEAK-M (LVDS,DDI)

U35D

Ibex-M 4 OF 10

LVDS--A: L_BKLTEN, L_VDD_EN, L_BKLTCTL, L_DDC_CLK, L_DDC_DATA, L_CTRL_CLK, L_CTRL_DATA, LVD_IBG, LVD_VBG, LVD_VREFH, LVD_VREFL, LVDSA_CLK#, LVDSA_CLK, LVDSA_DATA#0, LVDSA_DATA#1, LVDSA_DATA#2, LVDSA_DATA#3, LVDSA_DATA0, LVDSA_DATA1, LVDSA_DATA2, LVDSA_DATA3

LVDS--B: LVDSB_CLK#, LVDSB_CLK, LVDSB_DATA#0, LVDSB_DATA#1, LVDSB_DATA#2, LVDSB_DATA#3, LVDSB_DATA0, LVDSB_DATA1, LVDSB_DATA2, LVDSB_DATA3

CRT: CRT_BLUE, CRT_GREEN, CRT_RED, CRT_DDC_CLK, CRT_DDC_DATA, CRT_HSYNC, CRT_VSYNC, DAC_IREF, CRT_IRTN

SDVO: SDVO_TVCLKINN, SDVO_TVCLKINP, SDVO_STALLN, SDVO_STALLP, SDVO_INTN, SDVO_INTP, SDVO_CTRLCLK, SDVO_CTRLDATA

Digital Display Interface

DISPLAY PORT B: DDPB_AUXN, DDPB_AUXP, DDPB_HPD, DDPB_0N, DDPB_0P, DDPB_1N, DDPB_1P, DDPB_2N, DDPB_2P, DDPB_3N, DDPB_3P

DISPLAY PORT C: DDPC_CTRLCLK, DDPC_CTRLDATA, DDPC_AUXN, DDPC_AUXP, DDPC_HPD, DDPC_0N, DDPC_0P, DDPC_1N, DDPC_1P, DDPC_2N, DDPC_2P, DDPC_3N, DDPC_3P

DISPLAY PORT D: DDPD_CTRLCLK, DDPD_CTRLDATA, DDPD_AUXN, DDPD_AUXP, DDPD_HPD, DDPD_0N, DDPD_0P, DDPD_1N, DDPD_1P, DDPD_2N, DDPD_2P, DDPD_3N, DDPD_3P

IbexPeak-M_Rev1_0

Stuff on Hybrid and UMA

R783 *2.2K_4 EDIDCLK_PCH
R785 *2.2K_4 EDIDDATA_PCH

UMA and Hybird_LVDS & CRT signals

No stuff on Hybrid

No stuff on Hybrid

UMA HDMI signals

Q4 *2N7002K

DPB_HPD_Q → HDMI_HPD_CON [33]

R159 *100K_4, R158 *0_4

DPB_CTRL_CLK, DPB_CTRL_DATA, DPB_LANE0_N, DPB_LANE0_P, DPB_LANE1_N, DPB_LANE1_P, DPB_LANE2_N, DPB_LANE2_P, DPB_LANE3_N, DPB_LANE3_P → SDVO_CLK, SDVO_DATA, IN_D2#, IN_D2, IN_D1#, IN_D1, IN_D0#, IN_D0, IN_CLK#, IN_CLK

[32] LVDS_BLON_PCH, DISP_ON_PCH, DPST_PWM_PCH, EDIDCLK_PCH, EDIDDATA_PCH, CRT_B_PCH, CRT_G_PCH, CRT_R_PCH, DDCCLK_PCH, DDCDATA_PCH, HSYNC_PCH, VSYNC_PCH

1205 The SATALED# signal is open-collector and requires a weak external pull-up (8.2 k to 10 k) to +V3.3.

R557 10K/F_4 SATA_LED#

R270 *10K/F_4 SATA_DET0#
R559 *10K/F_4 SATA_DET1#
R274 10K/F_4
R632 10K/F_4

For AUDIO

[24] ACZ_RST#_AUDIO, [24] ACZ_SDOUT_AUDIO, [24] ACZ_SYNC_AUDIO, [24] BIT_CLK_AUDIO

PV 0616

For MDC

[25] ACZ_RST#_MDC, [25] ACZ_SDOUT_MDC, [25] ACZ_SYNC_MDC, [25] BIT_CLK_MDC

RTC

+RTC_CELL, +3VPCU, +3VRTC_2, RB500V-40, D27, D26, C655 1U/6.3V_4, R482 20K/F_4, C660 1U/6.3V_4 *SHORT_PAD1, R487 20K/F_4, C664 1U/6.3V_4 *SHORT_PAD1, R476 1M_4, R489 1K/F_4 +3VRTC_1, BT1 BAT_CONN

RTC_RST#, SRTC_RST#, SM_INTRUDER#

2M byte SPI ROM for ME

U40 AKE38FP0Z00

SPI_CS0#, SPI_CLK, SPI_SI, SPI_SO_R, SPI_HOLD#, SPI_WP#

2M SPI ROM
AKE38FP0Z00
X6179-10XXXX-8P-SOCKET

2M byte SPI ROM for ME

MXIC: AKE38FP0Z00
WINBOND: AKE38FP0N01
AIT: AKE38ZN0800

SPI ROM Socket

DG008000031

[2,8,9,11,29,34,36,42] +1.05V
[2,3,8,9,10,11,12,13,21,22,23,24,25,26,27,28,29,30,31,32,33,37,40,42] +3V
[3,21,25,28,29,30,34,35,36,38,40,41,42] +3VPCU

NB5

PROJECT : QL4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 1/5 (SATA,HDA,LPC)	E
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IBEX PEAK-M (GND)

U35I

AY7	VSS[159]	VSS[259]	H49
B11	VSS[160]	VSS[260]	H5
B15	VSS[161]	VSS[261]	J24
B19	VSS[162]	VSS[262]	K11
B23	VSS[163]	VSS[263]	K43
B31	VSS[164]	VSS[264]	K47
B35	VSS[165]	VSS[265]	K7
B39	VSS[166]	VSS[266]	L14
B43	VSS[167]	VSS[267]	L18
B47	VSS[168]	VSS[268]	L2
B7	VSS[169]	VSS[269]	L22
BG12	VSS[170]	VSS[270]	L32
BB12	VSS[171]	VSS[271]	L36
BB16	VSS[172]	VSS[272]	L40
BB20	VSS[173]	VSS[273]	L52
BB24	VSS[174]	VSS[274]	M12
BB30	VSS[175]	VSS[275]	M16
BB34	VSS[176]	VSS[276]	M20
BB38	VSS[177]	VSS[277]	N38
BB42	VSS[178]	VSS[278]	M34
BB49	VSS[179]	VSS[279]	M38
BB5	VSS[180]	VSS[280]	M42
BC10	VSS[181]	VSS[281]	M46
BC14	VSS[182]	VSS[282]	M49
BC18	VSS[183]	VSS[283]	M5
BC2	VSS[184]	VSS[284]	M8
BC22	VSS[185]	VSS[285]	N24
BC32	VSS[186]	VSS[286]	P11
BC36	VSS[187]	VSS[287]	AD15
BC40	VSS[188]	VSS[288]	P22
BC44	VSS[189]	VSS[289]	P30
BC52	VSS[190]	VSS[290]	P32
BH9	VSS[191]	VSS[291]	P34
BD48	VSS[192]	VSS[292]	P42
BD49	VSS[193]	VSS[293]	P45
BD5	VSS[194]	VSS[294]	P47
BE12	VSS[195]	VSS[295]	R2
BE16	VSS[196]	VSS[296]	R52
BE20	VSS[197]	VSS[297]	T12
BE24	VSS[198]	VSS[298]	T41
BE30	VSS[199]	VSS[299]	T46
BE34	VSS[200]	VSS[300]	T49
BE38	VSS[201]	VSS[301]	T5
BE42	VSS[202]	VSS[302]	T8
BE46	VSS[203]	VSS[303]	U30
BE48	VSS[204]	VSS[304]	U31
BE50	VSS[205]	VSS[305]	U32
BE6	VSS[206]	VSS[306]	U34
BE8	VSS[207]	VSS[307]	P38
BF3	VSS[208]	VSS[308]	V11
BF49	VSS[209]	VSS[309]	P16
BF51	VSS[210]	VSS[310]	V19
BG18	VSS[211]	VSS[311]	V20
BG24	VSS[212]	VSS[312]	V22
BG4	VSS[213]	VSS[313]	V30
BG50	VSS[214]	VSS[314]	V31
BH11	VSS[215]	VSS[315]	V32
BH15	VSS[216]	VSS[316]	V34
BH19	VSS[217]	VSS[317]	V35
BH23	VSS[218]	VSS[318]	V38
BH31	VSS[219]	VSS[319]	V43
BH35	VSS[220]	VSS[320]	V45
BH39	VSS[221]	VSS[321]	V46
BH43	VSS[222]	VSS[322]	V47
BH47	VSS[223]	VSS[323]	V49
BH7	VSS[224]	VSS[324]	V5
C12	VSS[225]	VSS[325]	V7
C50	VSS[226]	VSS[326]	V8
D51	VSS[227]	VSS[327]	W2
E12	VSS[228]	VSS[328]	W52
E16	VSS[229]	VSS[329]	Y11
E20	VSS[230]	VSS[330]	Y12
E24	VSS[231]	VSS[331]	Y15
E30	VSS[232]	VSS[332]	Y19
E34	VSS[233]	VSS[333]	Y23
E38	VSS[234]	VSS[334]	Y28
E42	VSS[235]	VSS[335]	Y30
E46	VSS[236]	VSS[336]	Y31
E48	VSS[237]	VSS[337]	Y32
E6	VSS[238]	VSS[338]	Y38
E8	VSS[239]	VSS[339]	Y43
F49	VSS[240]	VSS[340]	Y46
F5	VSS[241]	VSS[341]	P49
G10	VSS[242]	VSS[342]	Y5
G14	VSS[243]	VSS[343]	Y6
G18	VSS[244]	VSS[344]	Y8
G2	VSS[245]	VSS[345]	P24
G22	VSS[246]	VSS[346]	T43
G32	VSS[247]	VSS[347]	AD51
G36	VSS[248]	VSS[348]	AT8
G40	VSS[249]	VSS[349]	AD47
G44	VSS[250]	VSS[350]	Y47
G52	VSS[251]	VSS[351]	AT12
AF39	VSS[252]	VSS[352]	AM6
H16	VSS[253]	VSS[353]	AT13
H20	VSS[254]	VSS[354]	AM5
H30	VSS[255]	VSS[355]	AK45
H34	VSS[256]	VSS[356]	AK39
H38	VSS[257]	VSS[366]	AV14
H42	VSS[258]		

IbexPeak-M_Rev1_0

IBEX PEAK-M (PCI-E,SMBUS,CLK)

U35B

Ibex-M 2 OF 10

PCI-E*

[WLAN]
[30] PCIE_RXN0 — PCIE_RXN0 BG30
[30] PCIE_RXP0 — PCIE_RXP0 BJ30
[30] PCIE_TXN0 — C649 .1U/10V_4 — C654 .1U/10V_4 — PCIE_TXN0_C BF29
[30] PCIE_TXP0 — PCIE_TXP0_C BH29

[LAN]
[26] PCIE_RXN1_LAN — AW30
[26] PCIE_RXP1_LAN — BA30
[26] PCIE_TXN1_LAN — C371 .1U/10V_4 — C358 .1U/10V_4 — PCIE_TXN1_C BC30
[26] PCIE_TXP1_LAN — PCIE_TXP1_C BD30

Robson
[30] PCIE_RXN4 — PCIE_RXN4 BA32
[30] PCIE_RXP4 — PCIE_RXP4 BB32
[30] PCIE_TXN4 — C343 .1U/10V_4 — C349 .1U/10V_4 — PCIE_TXN4_C BD32
[30] PCIE_TXP4 — PCIE_TXP4_C BE32

[New Card]
[27] PCIE_RXN6 — PCIE_RXN6 BF33
[27] PCIE_RXP6 — PCIE_RXP6 BH33
[27] PCIE_TXN6 — C644 .1U/10V_4 — C640 .1U/10V_4 — PCIE_TXN6_C BG32
[27] PCIE_TXP6 — PCIE_TXP6_C BJ32

PERN1 PERP1 PETN1 PETP1
PERN2 PERP2 PETN2 PETP2
PERN3 PERP3 PETN3 PETP3
PERN4 PERP4 PETN4 PETP4
PERN5 PERP5 PETN5 PETP5
PERN6 PERP6 PETN6 PETP6
PERN7 PERP7 PETN7 PETP7
PERN8 PERP8 PETN8 PETP8

Port7 and Port8 HM55 not support

MiniWLAN
[30] CLK_PCIE_WLAN# — AM43 CLKOUT_PCIE1N
[30] CLK_PCIE_WLAN — AM45 CLKOUT_PCIE1P
[30] PCIE_CLK_REQ1# — R558 short0402 *0_4/S — CLK1_OE# — U4 PCIECLKRQ1# / GPIO18 (+3V)

WWAN
[30] CLK_PCIE_WWAN# — AM47 CLKOUT_PCIE2N
[30] CLK_PCIE_WWAN — AM48 CLKOUT_PCIE2P
[30] PCIE_CLK_REQ2# — R555 short0402 *0_4/S — CLK2_OE# — N4 PCIECLKRQ2# / GPIO20 (+3V)

LAN
[26] CLK_PCIE_LAN# — AH42 CLKOUT_PCIE3N
[26] CLK_PCIE_LAN — AH41 CLKOUT_PCIE3P
[26] PCIE_CLK_REQ3# — R528 short0402 *0_4/S — PCIE_CLK_REQ3#_R — A8 PCIECLKRQ3# / GPIO25 (+3V_S5)

Express Card
[27] CLK_PCIE_NEW# — AM51 CLKOUT_PCIE4N
[27] CLK_PCIE_NEW — AM53 CLKOUT_PCIE4P
[27] PCIE_CLK_REQ4# — PCIE_CLK_REQ4# — M9 PCIECLKRQ4# / GPIO26 (+3V_S5)

AJ50 CLKOUT_PCIE5N
AJ52 CLKOUT_PCIE5P
PCIE_CLK_REQ5# — H6 PCIECLKRQ5# / GPIO44 (+3V_S5)

AK53 CLKOUT_PEG_B_N
AK51 CLKOUT_PEG_B_P
PCIE_CLK_REQB#_R — P13 PEG_B_CLKRQ# / GPIO56 (+3V_S5)

PCIE_CLK_REQ0# — P9 PCIECLKRQ0# / GPIO73 (+3V_S5)

IbexPeak-M_Rev1_0

SMBus

(+3V_S5) SMBALERT# / GPIO11 — B9 SMBALERT# — 10K/F_4 — R509
SMBCLK — H14 PCLK_SMB — 2.2K_4 — R217
SMBDATA — C8 PDAT_SMB — 2.2K_4 — R219
(+3V_S5) SML0ALERT# / GPIO60 — J14 SMBL0ALERT# — 10K/F_4 — R212
SML0CLK — C6 SMB_CLK_ME0 — 4.7K_4 — R264
SML0DATA — G8 SMB_DATA_ME0 — 4.7K_4 — R533
(+3V_S5) SML1ALERT# / GPIO74 — M14 SML1ALERT# — 10K/F_4 — R211
(+3V_S5) SML1CLK / GPIO58 — E10 SMB_CLK_ME1 — 4.7K_4 — R222
(+3V_S5) SML1DATA / GPIO75 — G12 SMB_DATA_ME1 — 4.7K_4 — R223

+3VS5

SMB_CLK_ME0 — SMB_CLK_ME0 [26]
SMB_DATA_ME0 — SMB_DATA_ME0 [26]
FOR LAN IC

Controller Link

CL_CLK1 — T13
CL_DATA1 — T11
CL_RST1# — T9

PEG

(+3V_S5) PEG_A_CLKRQ# / GPIO47 — H1 PEG_CLKREQ# — PEG_CLKREQ# [14]
CLKOUT_PEG_A_N — AD43 — CLK_PCIE_VGA# [14]
CLKOUT_PEG_A_P — AD45 — CLK_PCIE_VGA [14]
CLKOUT_DMI_N — AN4 — CLK_PCIE_3GPLL# [3]
CLKOUT_DMI_P — AN2 — CLK_PCIE_3GPLL [3]

From CLK BUFFER

CLKOUT_DP_N / CLKOUT_BCLK1_N — AT1 — DREFSSCLK# [3]
CLKOUT_DP_P / CLKOUT_BCLK1_P — AT3 — DREFSSCLK [3]
CLKIN_DMI_N — AW24 — CLK_BUF_PCIE_3GPLL# [2]
CLKIN_DMI_P — BA24 — CLK_BUF_PCIE_3GPLL [2]
CLKIN_BCLK_N — AP3 — CLK_BUF_BCLK_N [2]
CLKIN_BCLK_P — AP1 — CLK_BUF_BCLK_P [2]
CLKIN_DOT_96N — F18 — CLK_BUF_DREFCLK# [2]
CLKIN_DOT_96P — E18 — CLK_BUF_DREFCLK [2]
CLKIN_SATA_N / CKSSCD_N — AH13 — CLK_BUF_DREFSSCLK# [2]
CLKIN_SATA_P / CKSSCD_P — AH12 — CLK_BUF_DREFSSCLK [2]
REFCLK14IN — P41 — CLK_ICH_14M [2]
CLKIN_PCILOOPBACK — J42 CLK_PCI_FB — CLK_PCI_FB [9]
XTAL25_IN — AH51 PCH_XT25MHZ_IN
XTAL25_OUT — AH53 PCH_XT2MHZ_OUT
XCLK_RCOMP — AF38 XCLK_RCOMP — R174 90.9/F_4 — +1.05V

Clock Flex

(+3V) CLKOUTFLEX0 / GPIO64 — T45 CLK_FLEX0 — T4
(+3V) CLKOUTFLEX1 / GPIO65 — P43 CLK_FLEX1 — T5
(+3V) CLKOUTFLEX2 / GPIO66 — T42 CLK_FLEX2 — T6
(+3V) CLKOUTFLEX3 / GPIO67 — N50 CLK_FLEX3 — R149 22_4 — CLK_48M_CR [23]
C272 *18P/50V_4

1203 Intel EDS1.0 spec change to no support 27and 24MHZ

+3V
CLK1_OE# — R546 10K/F_4
CLK2_OE# — R542 10K/F_4

+3VS5
PCIE_CLK_REQ0# — R226 10K/F_4
PCIE_CLK_REQ4# — R228 10K/F_4
PCIE_CLK_REQB#_R — R210 10K/F_4
PCIE_CLK_REQ5# — R247 10K/F_4
R531 *10K/F_4
PCIE_CLK_REQ3#_R — R529 10K/F_4
PEG_CLKREQ# — R537 10K/F_4

SMB_CLK_ME1 — Q11 2N7002E — MBCLK2 [17,28,29]
R304 2.2K_4
+3V
R307 2.2K_4
SMB_DATA_ME1 — Q12 2N7002E — MBDATA2 [17,28,29]
PDAT_SMB — Q8 2N7002E — CGDAT_SMB [2,12,13,27,30]
R289 10K/F_4
+3V
R290 10K/F_4
PCLK_SMB — Q9 2N7002E — CGCLK_SMB [2,12,13,27,30]

+3VS5
U18 *MC74VHC1G08DFT2G
C425 *.1U/10V_4
[9] PLT_RST-R# — PLT_RST-R# — PLTRST# [3,14,26,27,29,30,32]
R280 100K/F_4
R281 0_4
R282 *100K/F_4

R480 *1M_4
PCH_XT2MHZ_OUT — Y7 *25MHZ — PCH_XT25MHZ_IN
C786 *18P/50V_4
C787 *18P/50V_4

[2,7,9,11,29,34,36,42] +1.05V
[2,3,7,9,10,11,12,13,21,22,23,24,25,26,27,28,29,30,31,32,33,37,40,42] +3V
[9,10,11,14,27,40] +3VS5

NB5

PROJECT : QL4
Quanta Computer Inc.

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IBEX PEAK-M (PCI,USB,NVRAM)

For Switchable only

[29,32] DGPU_HOLD_RST# — R798 *0_4 SATA2GP — SATA2GP [10]
[29,42] DGPU_PWR_EN — R773 *0_4 REQ1#
[29,32,33] DGPU_SELECT# — R775 *0_4 REQ2#
[29,32] EDID_SELECT# — R774 *0_4 REQ3#
[32] PWM_SELECT# — R781 *0_4 PCI_GNT2#
[14,29,32] DGPU_PWROK — R799 *0_4 SATA3GP — SATA3GP [10]

+3VS5
PCH_GPIO61 — R771 — 10K/F_4

Discrete Only

FDI_INT — R491 — 1K/F_4
FDI_FSYNC0 — R500 — 1K/F_4
FDI_FSYNC1 — R496 — 1K/F_4
FDI_LSYNC0 — R498 — 1K/F_4
FDI_LSYNC1 — R494 — 1K/F_4

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PCI

AD0–AD31 (H40, N34, C44, A38, C36, J34, A40, D45, E36, H48, E40, C40, M48, M45, F53, M40, M43, J36, K48, F40, C42, K46, M51, J52, K51, L34, F42, J40, G46, F44, M47, H36)
C/BE0# (J50), C/BE1# (G42), C/BE2# (H47), C/BE3# (G34)
PCI_PIRQA# (G38), PCI_PIRQB# (H51), PCI_PIRQC# (B37), PCI_PIRQD# (A44) — PIRQA#, PIRQB#, PIRQC#, PIRQD#
REQ0# (F51), REQ1# (A46), REQ2# (B45), REQ3# (M53) — REQ0#, REQ1# / GPIO50 (+5V), REQ2# / GPIO52 (+5V), REQ3# / GPIO54 (+5V)
[10] GNT0# (F48), [10] GNT1# (K45), PCI_GNT2# (F36), [10,30] GNT3# (H53) — GNT0#, GNT1# / GPIO51 (+3V), GNT2# / GPIO53 (+3V), GNT3# / GPIO55 (+3V)
[17] DGPU_IDLE_INT# — R776 *0_4 — PIRQE# (B41)
PIRQE# / GPIO2 (+5V), PIRQF# / GPIO3 (+5V), PIRQG# / GPIO4 (+5V), PIRQH# / GPIO5 (+5V)
PCIRST# (K6)
[29] PCI_SERR# — PCI_SERR# (E44)
PCI_PERR# (E50) — SERR#, PERR#
PCI_IRDY# (A42), PCI_DEVSEL# (H44), PCI_FRAME# (F46) — IRDY#, PAR, DEVSEL#, FRAME#
PCI_PLOCK# (C46) — PLOCK#
PCI_STOP# (D49), PCI_TRDY# (D41) — STOP#, TRDY#
TP6 — PME# (C48) — PME#
[8] PLT_RST-R# — PLT_RST-R# (M7) — PLTRST#
[30] CLK_33M_DEBUG — R456 33_4 CLK_33M_DEBUG_R (D5)
[29] CLK_33M_KBC — R443 33_4 CLK_33M_KBC_R (N52)
[8] CLK_PCI_FB — R442 22_4 CLK_PCI_FB_C (P53)
CLKOUT_PCI0 (P46), CLKOUT_PCI1 (P51), CLKOUT_PCI2 (P48), CLKOUT_PCI3, CLKOUT_PCI4
B-stage change to 33 Ohm

NVRAM

NV_CE#0 (AY9), NV_CE#1 (BD1), NV_CE#2 (AP15), NV_CE#3 (BD8) — NV_CE#0 [31], NV_CE#1 [31], NV_CE#2 [31], NV_CE#3 [31]
NV_DQS0 (AV9), NV_DQS1 (BG8) — NV_DQS0 [31], NV_DQS1 [31]
NV_DQ0 / NV_IO0 (AP7), NV_DQ1 / NV_IO1 (AP6), NV_DQ2 / NV_IO2 (AT6), NV_DQ3 / NV_IO3 (AT9), NV_DQ4 / NV_IO4 (BB1), NV_DQ5 / NV_IO5 (AV6), NV_DQ6 / NV_IO6 (BB3), NV_DQ7 / NV_IO7 (BA4), NV_DQ8 / NV_IO8 (BE4), NV_DQ9 / NV_IO9 (BB6), NV_DQ10 / NV_IO10 (BD6), NV_DQ11 / NV_IO11 (BB7), NV_DQ12 / NV_IO12 (BC8), NV_DQ13 / NV_IO13 (BJ8), NV_DQ14 / NV_IO14 (BJ6), NV_DQ15 / NV_IO15 (BG6) — NV_DQ0–NV_DQ15 [31]
NV_ALE (BD3), NV_CLE (AY6) — NV_ALE [10,31], NV_CLE [10,31]
NV_RCOMP (AU2) — NV_RCOMP R536 32.4/F_4
NV_RB# (AV7) — NV_RB# [31]
NV_WR#0_RE# (AY8), NV_WR#1_RE# (AY5) — NV_WR#_RE#0 [31], NV_WR#_RE#1 [31]
NV_WE#_CK0 (AV11), NV_WE#_CK1 (BF5) — NV_WE#_CK0 [31], NV_WE#_CK1 [31]

USB

USBP0N (H18), USBP0P (J18) — USBP0- [24], USBP0+ [24] — USB
USBP1N (A18), USBP1P (C18) — USBP1- [24], USBP1+ [24] — USB
USBP2N (N20), USBP2P (P20) — USBP2- [28], USBP2+ [28] — ESATA-USB
USBP3N (J20), USBP3P (L20)
USBP4N (F20), USBP4P (G20) — USBP4- [23], USBP4+ [23] — Card reader
USBP5N (A20), USBP5P (C20) — USBP5- [28], USBP5+ [28] — Camera
USBP6N (M22), USBP6P (N22), USBP7N (B21), USBP7P (D21)
Port6 and Port7 HM55 not support
USBP8N (H22), USBP8P (J22) — USBP8- [27], USBP8+ [27] — NEWCARD
USBP9N (E22), USBP9P (F22)
USBP10N (A22), USBP10P (C22) — USBP10- [30], USBP10+ [30] — WLAN
USBP11N (G24), USBP11P (H24) — USBP11- [30], USBP11+ [30] — WWAN
USBP12N (L24), USBP12P (M24) — USBP12- [24], USBP12+ [24] — Blue tooth
USBP13N (A24), USBP13P (C24)
USBRBIAS (B25) — USB_BIAS R479 22.6/F_4
USBRBIAS (D25)
(+3V_S5) OC0# / GPIO59 (N16), OC1# / GPIO40 (J16), OC2# / GPIO41 (F16), OC3# / GPIO42 (L16), OC4# / GPIO43 (E14), OC5# / GPIO9 (G16), OC6# / GPIO10 (F12), OC7# / GPIO14 (T15)
USB_OC0#, USB_OC1#, USB_OC2#, USB_OC3#, USB_OC4#, USB_OC5#, USB_OC6#, USB_OC7#
PV 0616 DEL debug Con.

IbexPeak-M_Rev1_0

EMI

CLK_33M_DEBUG — C620 *33P/50V_4
CLK_33M_KBC — C618 *33P/50V_4
CLK_PCI_FB — C617 *33P/50V_4
C90 *10P/50V_4 — USBP0-
C95 *10P/50V_4 — USBP0+
C648 *10P/50V_4 — USBP1-
C650 *10P/50V_4 — USBP1+
C671 *10P/50V_4 — USBP4-
C775 *10P/50V_4 — USBP4+
C666 *10P/50V_4 — USBP8-
C670 *10P/50V_4 — USBP8+
C780 *10P/50V_4 — USBP10-
C781 *10P/50V_4 — USBP10+
C782 *10P/50V_4 — USBP11-
C783 *10P/50V_4 — USBP11+
C778 *10P/50V_4 — USBP12-
C779 *10P/50V_4 — USBP12+

IBEX PEAK-M (DMI,FDI,GPIO)

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DMI

[3] DMI_RXN0 (BC24), [3] DMI_RXN1 (BJ22), [3] DMI_RXN2 (AW20), [3] DMI_RXN3 (BJ20) — DMI0RXN, DMI1RXN, DMI2RXN, DMI3RXN
[3] DMI_RXP0 (BD24), [3] DMI_RXP1 (BG22), [3] DMI_RXP2 (BA20), [3] DMI_RXP3 (BG20) — DMI0RXP, DMI1RXP, DMI2RXP, DMI3RXP
[3] DMI_TXN0 (BE22), [3] DMI_TXN1 (BF21), [3] DMI_TXN2 (BD20), [3] DMI_TXN3 (BE18) — DMI0TXN, DMI1TXN, DMI2TXN, DMI3TXN
[3] DMI_TXP0 (BD22), [3] DMI_TXP1 (BH21), [3] DMI_TXP2 (BC20), [3] DMI_TXP3 (BD18) — DMI0TXP, DMI1TXP, DMI2TXP, DMI3TXP
+1.05V — R208 49.9/F_4 — DMI_COMP (BH25) — DMI_ZCOMP, DMI_IRCOMP (BF25)

FDI

FDI_RXN0 (BA18), FDI_RXN1 (BH17), FDI_RXN2 (BD16), FDI_RXN3 (BJ16), FDI_RXN4 (BA16), FDI_RXN5 (BE14), FDI_RXN6 (BA14), FDI_RXN7 (BC12) — FDI_TXN0–FDI_TXN7 [3]
FDI_RXP0 (BB18), FDI_RXP1 (BF17), FDI_RXP2 (BC16), FDI_RXP3 (BG16), FDI_RXP4 (AW16), FDI_RXP5 (BD14), FDI_RXP6 (BB14), FDI_RXP7 (BD12) — FDI_TXP0–FDI_TXP7 [3]
FDI_INT (BJ14), FDI_FSYNC0 (BF13), FDI_FSYNC1 (BH13), FDI_LSYNC0 (BJ12), FDI_LSYNC1 (BG14) — FDI_INT [3], FDI_FSYNC0 [3], FDI_FSYNC1 [3], FDI_LSYNC0 [3], FDI_LSYNC1 [3]

System Power Management

[3] XDP_DBRESET# — T6
[37] IMVP_PWRGD — R262 0_4 — M6
[29] ECPWROK — R263 *0_4 — PCH_PWROK — B17
RSV_ICH_LAN_RST# — A10
[3] PM_DRAM_PWRGD — D9
[29] RSMRST# — C16
[29] DNBSWON# — R272 short0402 *0_4/S — K5
PM_PWRBTN#_R — P5
PM_RI# — F14
[26,27,30] PCIE_WAKE# — J12
[3] PM_SYNC — BJ10

SYS_RESET#, SYS_PWROK, PWROK, MEPWROK, LAN_RST#, DRAMPWROK, RSMRST#, PWRBTN#, RI#, WAKE#, PMSYNCH

SLP_S3# (P12), SLP_S4# (H7) — SUSB# [29], SUSC# [29]
SLP_M# (K8) — TP4
TP23 (N2)
(+3V_S5) SUS_PWR_DN_ACK / GPIO30 (M1) — SUS_PWR_ACK [29]
(+3V_S5) ACPRESENT / GPIO31 (P7) — AC_PRESENT — AC_PRESENT [29]
(+3V) CLKRUN# / GPIO32 (Y1) — CLKRUN# [29]
(+3V_S5) SUS_STAT# / GPIO61 (P8) — PCH_GPIO61
(+3V_S5) SUSCLK / GPIO62 (F3) — SUSCLK — TP47
(+3V_S5) SLP_S5# / GPIO63 (E4) — SLP_S5# — TP39
(+3V_S5) BATLOW# / GPIO72 (A6) — PM_BATLOW# — PM_BATLOW# [29]
(+3V_S5) SLP_LAN# / GPIO29 (F6) — BOARD_ID6 [10]

IbexPeak-M_Rev1_0

RP33 (10P8R-8.2K)

GNT3# — R190 *1K/F_4
+3V
PCI_IRDY# (5), PCI_STOP# (4), PCI_PIRQA# (3), PCI_PIRQC# (2), (1) — PCI_PIRQD# (6), PCI_SERR# (7), REQ1# (8), PCI_FRAME# (9), (10) +3V

RP38 (10P8R-8.2K)

+3VS5
USB_OC4# (5), USB_OC5# (4), USB_OC6# (3), USB_OC7# (2), (1) — USB_OC0# (6), USB_OC1# (7), USB_OC2# (8), USB_OC3# (9), (10) +3VS5

RP32 (10P8R-8.2K)

+3V
REQ3# (5), PCI_DEVSEL# (4), PCI_TRDY# (3), INTH# (2), (1) — PCI_PLOCK# (6), PCI_PERR# (7), REQ0# (8), PCI_PIRQB# (9), (10) +3V

REQ2# — R166 8.25K/F_4 — PIRQE#
R165 8.25K/F_4 — PIRQF#
R460 8.25K/F_4 — PIRQG#
R179 8.25K/F_4 — +3V
11/17
CLKRUN# — R549 8.25K/F_4 — XDP_DBRESET# — R259 1K/F_4
+3VS5
PM_RI# — R215 10K/F_4
PM_BATLOW# — R530 10K/F_4
PCIE_WAKE# — R221 1K/F_4
SUS_PWR_ACK — R541 10K/F_4
AC_PRESENT — R233 10K/F_4
11/17
RSMRST# — R209 10K/F_4
RSV_ICH_LAN_RST# — R499 10K/F_4
PCH_PWROK — R484 10K/F_4

[2,7,8,11,29,34,36,42] +1.05V
[2,3,7,8,10,11,12,13,21,22,23,24,25,26,27,28,29,30,31,32,33,37,40,42] +3V
[8,10,11,14,27,40] +3VS5

NB5

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Quanta Computer Inc.

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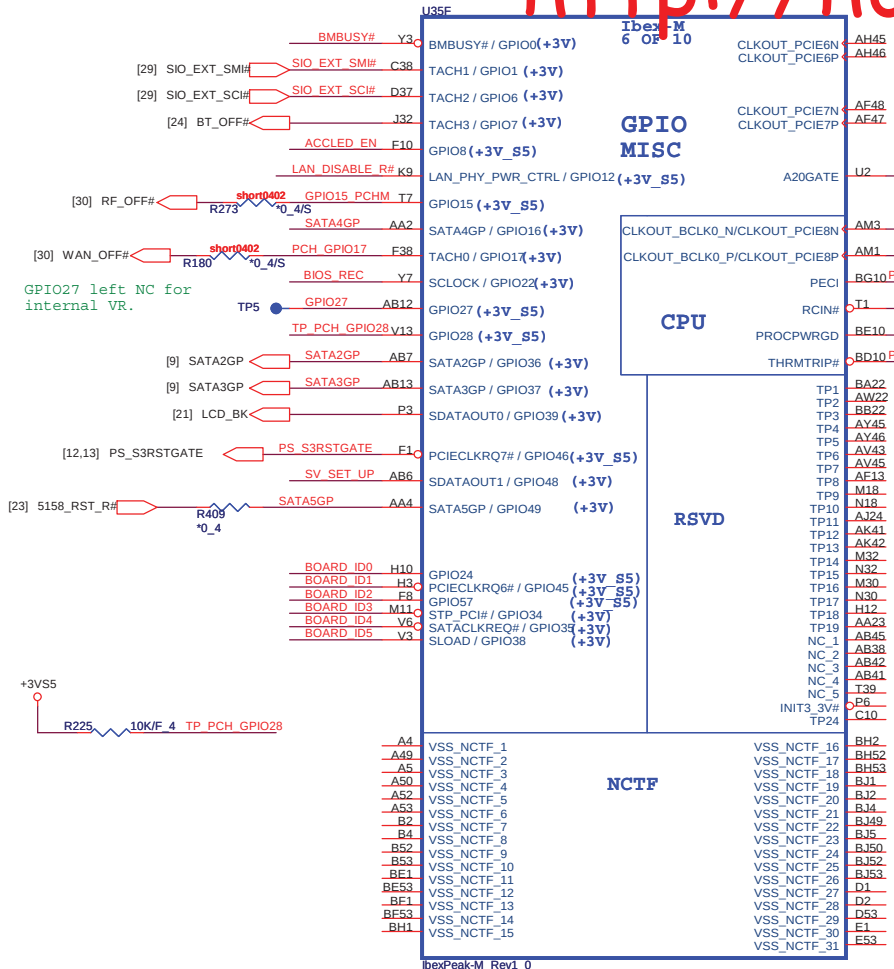
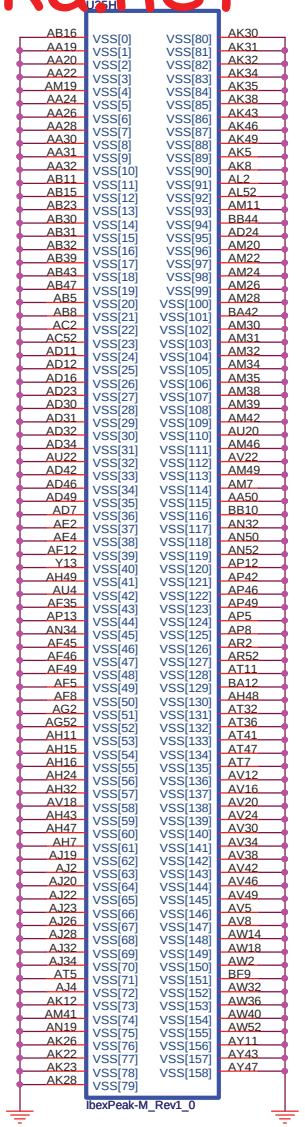
IBEX PEAK-M (GPIO, VSS_NCTF, RSVD)



IBEX PEAK-M (GND)



+3VS5
PS_S3RSTGATE R265 10K/F_4

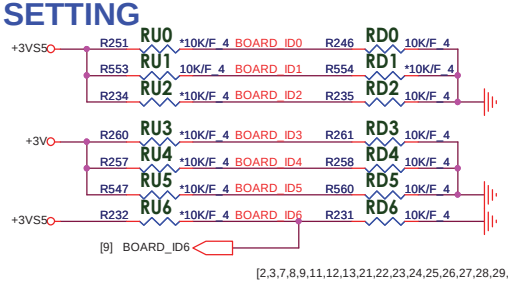
+3V
BIOS_REC R256 10K/F_4
BIOS RECOVERY
HIGH : DISABLE
LOW : ENABLE

+3V
RCIN# R544 10K/F_4
GATEA20 R545 10K/F_4
SATA2GP R269 10K/F_4
SATA3GP R216 10K/F_4
SATA4GP R561 10K/F_4
SATA5GP R550 10K/F_4
BMBUSY# R548 10K/F_4
SIO_EXT_SMI# R178 10K/F_4
SIO_EXT_SCI# R177 10K/F_4
BT_OFF# R193 10K/F_4
LCD_BK R543 10K/F_4
PCH_GPIO17 R171 10K/F_4
1204 (need to pull up to 3V from check list request)

+3VS5
ACCLED_EN R224 10K/F_4
RF_OFF# R200 1K/F_4
LAN_DISABLE_R# R230 10K/F_4
1204 (need to pull up to 3V_S5 from check list request)

Board ID	ID0	ID1	ID2	ID3	ID4	ID5	ID6
LG/CB	0=LG 1=CB						
UMA/Dis.		0=UMA 1=Dis.					
15.6"/ 14"			0=QL4/TW9 1=QL2/SW9				
Switchable						1=YES 0=NO	

BOARD ID SETTING



Board ID	ID6	ID5	ID4	ID3	ID2	ID1	ID0
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RD1 (0)	RU0 (1)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RU1 (1)	RD0 (0)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RU1 (1)	RU0 (1)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RD1 (0)	RD0 (0)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RD1 (0)	RU0 (1)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RU1 (1)	RD0 (0)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RU1 (1)	RU0 (1)

[3,5,11,34,38] +1.1V_VTT
[5,11,31,36,40,42] +1.8V
[2,3,7,8,9,11,12,13,21,22,23,24,25,26,27,28,29,30,31,32,33,37,40,42] +3V
[8,9,11,14,27,40] +3VS5

[9,30] GNT3# R461 *10K_NC

A16 swap override Strap/Top-Block Swap Override jumper	
GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

SV_SET_UP R271 10K/F_4 +3V

SV_SET_UP	1-X High = Strong (Default)

[9] GNT0#
[9] GNT1#
GNT0# R155 *1K/F_4
GNT1# R157 *1K/F_4

Boot BIOS Strap		
PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

[9,31] NV_ALE
[9,31] NV_CLE
R534 *1K/F_4
R535 *1K/F_4
+1.8V
11/17

Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

No Reboot Strap

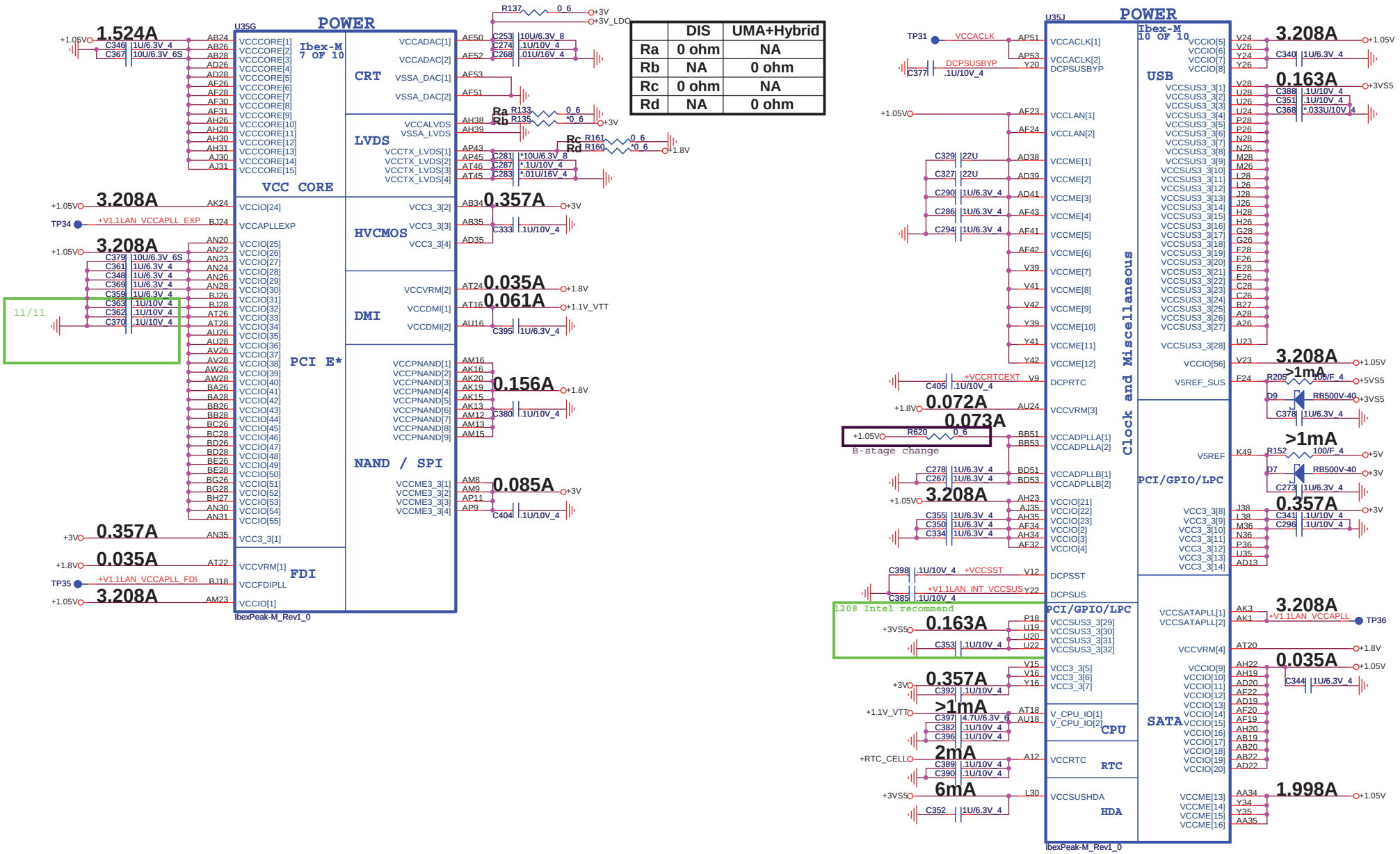
[7,24] SPKR
SPKR *1K/F_4 R556 +3V

[7] PCH_GPIO33
R194 *100K/F_4

NB5

PROJECT : QL4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 4/5 (GPIO & Strap)	E
Date: Friday, October 09, 2009	Sheet 10 of 44	



	DIS	UMA+Hybrid
Ra	0 ohm	NA
Rb	NA	0 ohm
Rc	0 ohm	NA
Rd	NA	0 ohm

PROJECT : QL4
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	PCH 5/5 (POWER)	E

Date: Friday, October 09, 2009 | Sheet 11 of 44

+1.5VSUS → C152 .1U/10V_4, C160 .1U/10V_4, C175 .1U/10V_4, C332 .1U/10V_4 → +1.5VSUS_CPU

SO-DIMMA SPD Address is 0XA0
SO-DIMMA TS Address is 0X30

JDIM2A — PC2100 DDR3 SDRAM SO-DIMM (204P) — DDR3-DIMM0

[4] M_A_A[15:0] → M_A_A0..M_A_A15 → A0..A15, A10/AP, A12/BC#
[4] M_A_BS#0, M_A_BS#1, M_A_BS#2 → BA0, BA1, BA2
[4] M_A_CS#0, M_A_CS#1 → S0#, S1#
[4] M_A_CLK0 → CK0
[4] M_A_CLK0# → CK0#
[4] M_A_CLK1 → CK1
[4] M_A_CLK1# → CK1#
[4] M_A_CKE0 → CKE0
[4] M_A_CKE1 → CKE1
[4] M_A_CAS# → CAS#
[4] M_A_RAS# → RAS#
[4] M_A_WE# → WE#
R196 10K/F_4 DIMM0_SA0 → SA0
R195 10K/F_4 DIMM0_SA1 → SA1
[2,8,13,27,30] CGCLK_SMB → SCL
[2,8,13,27,30] CGDAT_SMB → SDA
[4] M_A_ODT0 → ODT0
[4] M_A_ODT1 → ODT1
[4] M_A_DM[7:0] → M_A_DM0..M_A_DM7 → DM0..DM7
[4] M_A_DQS[7:0] → M_A_DQS0..M_A_DQS7 → DQS0..DQS7
[4] M_A_DQS#[7:0] → M_A_DQS#0..M_A_DQS#7 → DQS#0..DQS#7
M_A_DQ[63:0] [4] → M_A_DQ0..M_A_DQ63 → DQ0..DQ63

SMDDR_VREF_DIMM [13] → short0402 → R128 *0_4/S → DDR_VTTREF [39]

JDIM2B — PC2100 DDR3 SDRAM SO-DIMM (204P) — DDR3-DIMM0

+1.5VSUS → VDD1..VDD18
+3V → VDDSPD
NC1, NC2, NCTEST
+3V → R204 *10K/F_4 → PM_EXTTS#0
[3,13] PM_EXTTS#0 → EVENT#
[13] C_DDR3_DRAMRST# → RESET#
SMDDR_VREF_DQ0_M2 → R18 *0_4/S short0402 → SMDDR_VREF_DQ0
SMDDR_VREF_DIMM → VREF_DQ, VREF_CA
VSS1..VSS52
VTT1, VTT2 → +0.75V_DDR_VTT
GND, GND

+0.75V_DDR_VTT → R64 27_6 → DS_0.75VS
[5,40] MAINON_G → Q36 BSS138

C_DDR3_DRAMRST# → C973 68PF/50V_4
+1.5VSUS → R253 1K/F_4
[3] DDR3_DRAMRST# → R100 *0_4 → Q39 BSS138
R96 100K/F_4
C232 4700P/25V_4 → PS_S3RSTGATE

C224 470P/50V_4 SMDDR_VREF_DQ0_M2
R127 1K/F_4, R122 1K/F_4 → +1.5VSUS

[6] DDR_VREF_DQ0 → R26 *0_4 → SMDDR_VREF_DQ0
Q37 AO3402
R103 100K/F_4
PS_S3RSTGATE → PS_S3RSTGATE [10,13]

[13,39] +0.75V_DDR_VTT
[5,13,39,40,42] +1.5VSUS
[2,3,7,8,9,10,11,13,21,22,23,24,25,26,27,28,29,30,31,32,33,37,40,42] +3V
[3,7,21,25,28,29,30,34,35,36,38,40,41,42] +3VPCU
[29,34,35,36,37,38,39,40] +5VPCU

Place these Caps near So-Dimm0.

+1.5VSUS
C127 10U/6.3V_6S
C174 10U/6.3V_6S
C159 10U/6.3V_6S
C113 10U/6.3V_6S
C137 10U/6.3V_6S
C196 10U/6.3V_6S
C146 1U
C209 1U
C176 1U
C126 1U
C138 1U
B-stage change

+0.75V_DDR_VTT
C364 1U/6.3V_4
C402 1U/6.3V_4
C400 1U/6.3V_4
C365 1U/6.3V_4
C411 *10U/6.3V_8
C407 *10U/6.3V_8
C391 10U/6.3V_6S

SMDDR_VREF_DQ0
C38 .1U/10V_4
C37 2.2U/6.3V_6

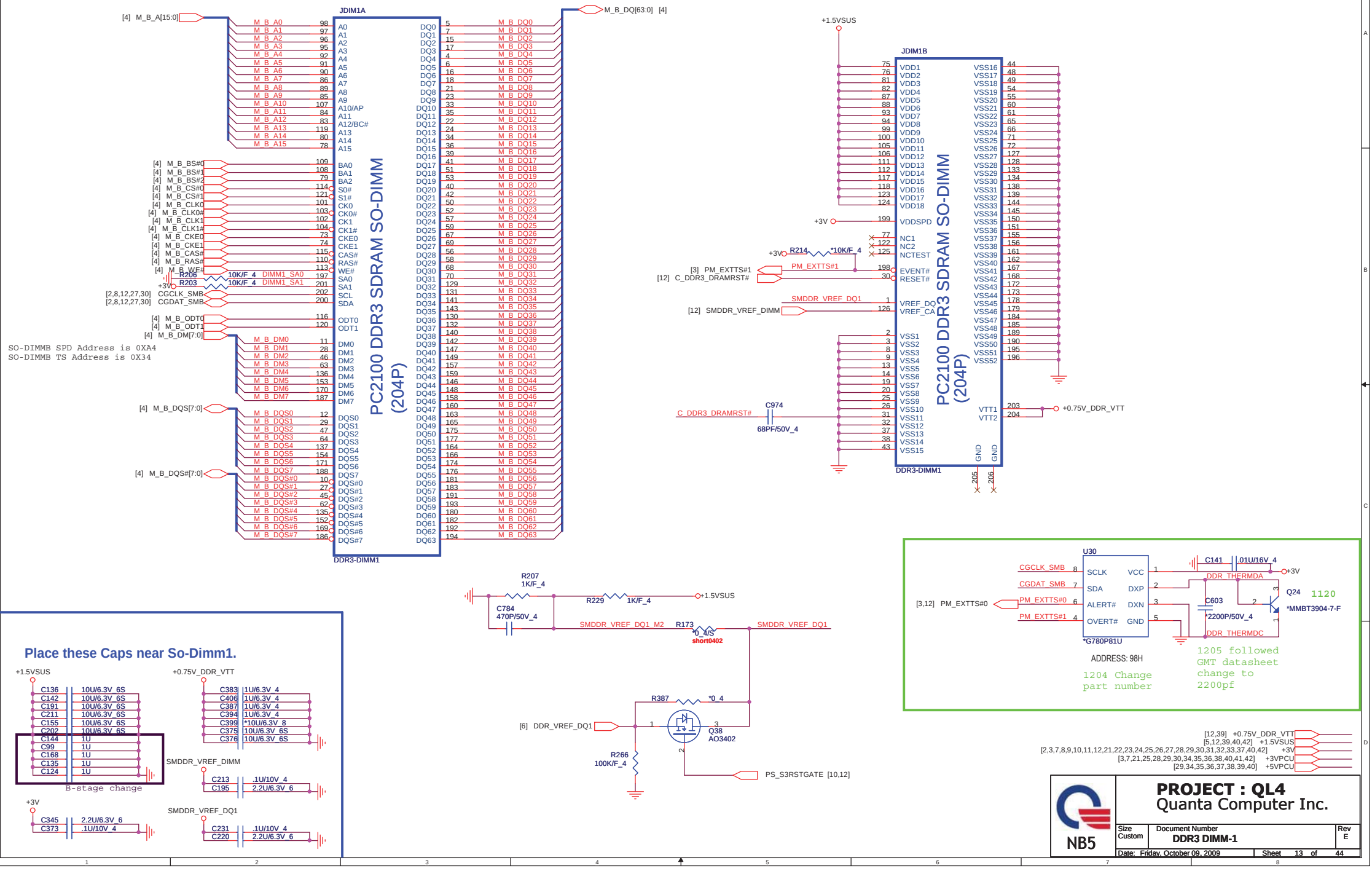
+3V
C354 2.2U/6.3V_6
C338 .1U/10V_4

SMDDR_VREF_DIMM
C180 .1U/10V_4
C187 2.2U/6.3V_6

NB5

PROJECT : QL4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM-0	E
Date: Friday, October 09, 2009	Sheet 12 of 44	



[12,39] +0.75V_DDR_VTT
[5,12,39,40,42] +1.5VSUS
[2,3,7,8,9,10,11,12,21,22,23,24,25,26,27,28,29,30,31,32,33,37,40,42] +3V
[3,7,21,25,28,29,30,34,35,36,38,40,41,42] +3VPCU
[29,34,35,36,37,38,39,40] +5VPCU

NB5	**PROJECT : QL4** Quanta Computer Inc.	
Size: Custom	Document Number: DDR3 DIMM-1	Rev: E
Date: Friday, October 09, 2009	Sheet 13 of 44	

PEX_IOVDD+PEX_IOVDDQ+PEX_PLLVDD >2.2A

~ 500mA

1600mA

Near BGA

12~16 mils width

110mA

12~16 mils width

B-stage change to 100nH

U33A
BGA969-NVIDIA-NB9P-GS
COMMON

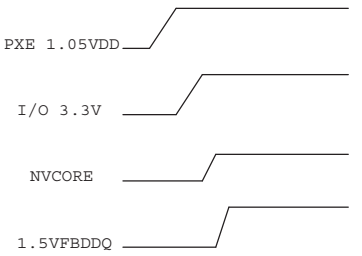
PCI EXPRESS

1211 for Nvidia request
add transition cap

R450 un-mount for switchable function

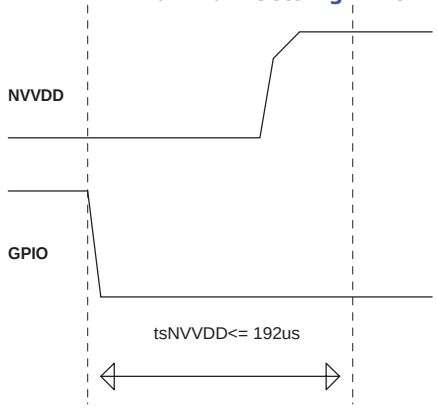
Only for Hybrid

power up sequence

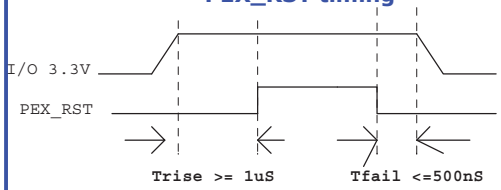


NB9M: VGACORE +0.90V (Normal) , +1.09V

NVVDD Maximum Settling Time



PEX_RST timing



[15,16,32,42] +1.05V_GFX
[16,17,22,32,33,38,42] +3V_GFX

NB5	PROJECT : QL4 Quanta Computer Inc.	
Size: Custom	Document Number: N10M-GE (PCIE I/F) 1/5	Rev: E
Date: Friday, October 09, 2009	Sheet 14 of 44	

U33B
BGA969-NVIDIA-NB9P-GS
COMMON

12/02 modify
package for N10

MEMORY I/F A

MEMORY I/F C

All need stuff for N10P

For Debug only

15mils width

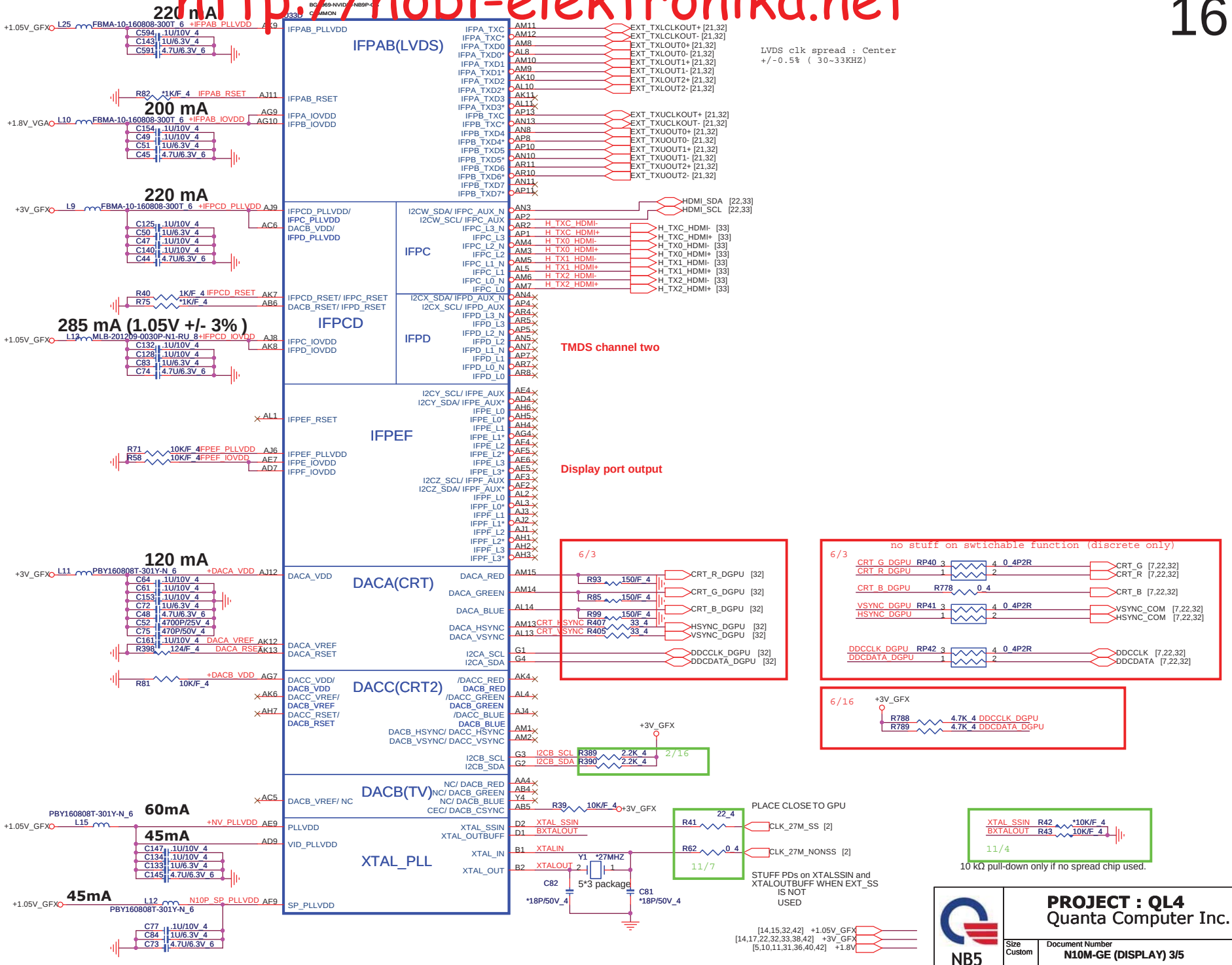
2/16

12/16 Modified
11/4

R92 no stuff

PROJECT : QL4	
Quanta Computer Inc.	
Size: Custom	Document Number: N10M-GE (MEMORY I/F) 2/5
Rev: E	
Date: Friday, October 09, 2009	Sheet 15 of 44

NB5



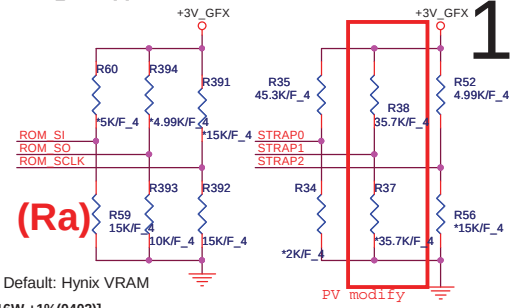
CHIP	PCI_DEVID:	STRAP2	ROM_SCLK
N10P-GE	0x0A38	1000 PU 5K	0000 PD 15K
N10M-GE	0x0A38	1000 PU 5K	0000 PD 15K

CHIP	PCI_DEVID:	STRAP2	ROM_SCLK
N11P-GS1	0x0CAF	1111 PU 45K	0010 PD 15K
N11M-GS1	0x0A35	0101 PD 30K	1010 PU 15K

PCI_DEVID[4]/SUBVENDOR

Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



Default: Hynix VRAM

4.99K/F_4: CS24992FB26 [RES CHIP 4.99K 1/16W +1%(0402)]
10K/F_4: CS31002FB26 [RES CHIP 10K 1/16W +1% (0402)]
15K/F_4: CS31502FB24 [RES CHIP 15K 1/16W +1% (0402)]
30.1K/F_4: CS33012FB18 [RES CHIP 30.1K 1/16W +-1%(0402)]
35.7K/F_4: CS33572FB13 [RES CHIP 35.7K 1/16W +-1%(0402)]
45.3K/F_4: CS34532FB18 [RES CHIP 45.3K 1/16W +-1% (0402)]
20K/F_4: CS32002FB29 RES CHIP 20K 1/16W +-1%(0402)

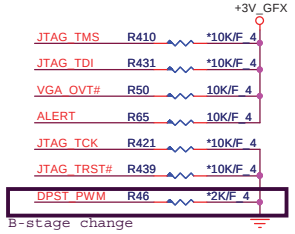
	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO NB10X	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1000
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0001
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

VRAM Configuration Table

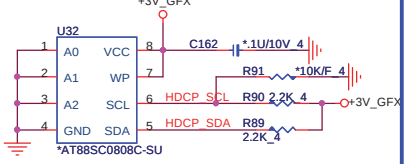
RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
0000		Reserved		
0001	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Qimonda	IDGH1G-04A1F1C-16X	PD 10K
0010	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Hynix	H5TQ1G63BFR-12C	PD 15K
0011	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Samsung	K4W1G1646E-HC12	PD 20K
0101		Reserved		
0110				
XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Hynix	H5TQ1G63AFR-14C	
XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Samsung	K4W1G1646D-EC12	

AKD58GGT^01
AKD5LZGTW00
AKD5LGGT502

(Ra)



HDCP ROM



Fill U36 to correct p/n as Top B/S P/N(AR0QT6VB002)

DHCP ROM	
HDCP_SCL	Low: Crypto ROM Hi: I2C ROM

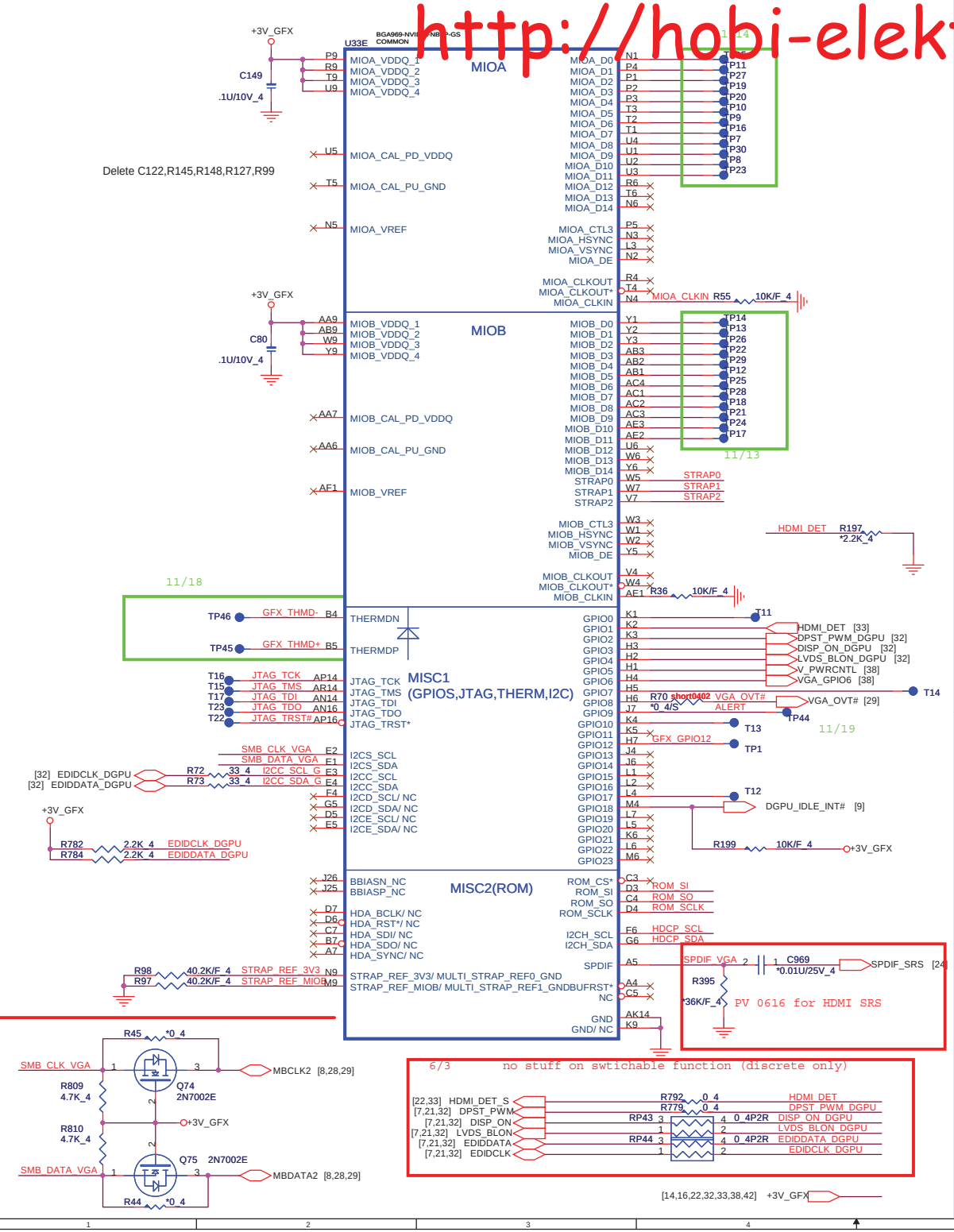
GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	NVVDD VID2 11/13
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL 11/13
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

NB5

PROJECT : QL4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N10M-GE (GPIO&STRAPS) 4/5	E
Date: Friday, October 09, 2009	Sheet 17 of 44	



U33F

BGA969-NVIDIA-NB9P-GS
COMMON

+VGACORE

+VGACORE

NVVDD

AB11	VDD_001	VDD_057	P21	AB13	VDD_002
AB15	VDD_003	VDD_058	P23	AB17	VDD_004
AB19	VDD_005	VDD_059	P25	AB21	VDD_006
AB23	VDD_007	VDD_060	R11	AB25	VDD_008
AC11	VDD_009	VDD_061	R12	AC12	VDD_010
AC13	VDD_011	VDD_062	R13	AC14	VDD_012
AC15	VDD_013	VDD_063	R14	AC16	VDD_014
AC17	VDD_015	VDD_064	R15	AC18	VDD_016
AC19	VDD_017	VDD_065	R16	AC20	VDD_018
AC21	VDD_019	VDD_066	R17	AC22	VDD_020
AC23	VDD_021	VDD_067	R18	AC24	VDD_022
AC25	VDD_023	VDD_068	R19	AD12	VDD_024
AD14	VDD_025	VDD_069	R20	AD16	VDD_026
AD18	VDD_027	VDD_070	R21	AD22	VDD_028
AD24	VDD_029	VDD_071	R22	L11	VDD_030
L12	VDD_031	VDD_072	R23	L13	VDD_032
L14	VDD_033	VDD_073	R24	L15	VDD_034
L16	VDD_035	VDD_074	R25	L17	VDD_036
L18	VDD_037	VDD_075	T12	L19	VDD_038
L20	VDD_039	VDD_076	T14	L21	VDD_040
L22	VDD_041	VDD_077	T16	L23	VDD_042
L24	VDD_043	VDD_078	T18	L25	VDD_044
M12	VDD_045	VDD_079	T20	M14	VDD_046
M16	VDD_047	VDD_080	T22	M18	VDD_048
M20	VDD_049	VDD_081	T24	M22	VDD_050
M24	VDD_051	VDD_082	V11	P11	VDD_052
P13	VDD_053	VDD_083	V13	P15	VDD_054
P17	VDD_055	VDD_084	V15	P19	VDD_056
		VDD_085	V17		
		VDD_086	V19		
		VDD_087	V21		
		VDD_088	V23		
		VDD_089	V25		
		VDD_090	W11		
		VDD_091	W12		
		VDD_092	W13		
		VDD_093	W14		
		VDD_094	W15		
		VDD_095	W16		
		VDD_096	W17		
		VDD_097	W18		
		VDD_098	W19		
		VDD_099	W20		
		VDD_100	W21		
		VDD_101	W22		
		VDD_102	W23		
		VDD_103	W24		
		VDD_104	W25		
		VDD_105	Y12		
		VDD_106	Y14		
		VDD_107	Y16		
		VDD_108	Y18		
		VDD_109	Y20		
		VDD_110	Y22		
		VDD_111	Y24		

U33G

BGA969-NVIDIA-NB9P-GS
COMMON

GROUND

AA11	GND_1	GND_096	E15	AA12	GND_2
AA13	GND_3	GND_097	E18	AA14	GND_4
AA15	GND_5	GND_098	E24	AA16	GND_6
AA17	GND_7	GND_099	E27	AA18	GND_8
AA19	GND_9	GND_100	E30	AA2	GND_10
AA20	GND_11	GND_101	E6	AA21	GND_12
AA22	GND_13	GND_102	E9	AA23	GND_14
AA24	GND_15	GND_103	F2	AA25	GND_16
AA34	GND_17	GND_104	F31	AA5	GND_18
AB12	GND_19	GND_105	F34	AB14	GND_20
AB16	GND_21	GND_106	F5	AB18	GND_22
AB20	GND_23	GND_107	J2	AB22	GND_24
AB24	GND_25	GND_108	J31	AC9	GND_26
AD11	GND_27	GND_109	J34	AD13	GND_28
AD15	GND_29	GND_110	J5	AD17	GND_30
AD2	GND_31	GND_111	L9	AD21	GND_32
AD23	GND_33	GND_112	M11	AD25	GND_34
AD31	GND_35	GND_113	M13	AD34	GND_36
AD5	GND_37	GND_114	M15	AE11	GND_38
AE12	GND_39	GND_115	M17	AE13	GND_40
AE14	GND_41	GND_116	M19	AE15	GND_42
AE16	GND_43	GND_117	M2	AE17	GND_44
AE18	GND_45	GND_118	M21	AE19	GND_46
AE20	GND_47	GND_119	M23	AE21	GND_48
AE22	GND_49	GND_120	M25	AE23	GND_50
AE24	GND_51	GND_121	M31	AE25	GND_52
AG2	GND_53	GND_122	M34	AG31	GND_54
AG34	GND_55	GND_123	M5	AG5	GND_56
AK2	GND_57	GND_124	N11	AK31	GND_58
AK34	GND_59	GND_125	N12	AK5	GND_60
AL12	GND_61	GND_126	N13	AL15	GND_62
AL18	GND_63	GND_127	N14	AL21	GND_64
AL24	GND_65	GND_128	N15	AL27	GND_66
AL30	GND_67	GND_129	N16	AL6	GND_68
AL9	GND_69	GND_130	N17	AN2	GND_70
AN34	GND_71	GND_131	N18	AP12	GND_72
AP15	GND_73	GND_132	N19	AP18	GND_74
AP21	GND_75	GND_133	N20	AP24	GND_76
AP27	GND_77	GND_134	N21	AP3	GND_78
AP30	GND_79	GND_135	N22	AP33	GND_80
AP6	GND_081	GND_136	N23	AP9	GND_082
B12	GND_083	GND_137	N24	B15	GND_084
B21	GND_085	GND_138	N25	B24	GND_086
B27	GND_087	GND_139	P12	B3	GND_088
B30	GND_089	GND_140	P14	B33	GND_090
B6	GND_091	GND_141	P16	B9	GND_092
C2	GND_093	GND_142	P18	C34	GND_094
E12	GND_095	GND_143	P20		
		GND_144	P22		
		GND_145	P24		
		GND_146	R2		
		GND_147	R31		
		GND_148	R34		
		GND_149	R5		
		GND_150	T11		
		GND_151	T13		
		GND_152	T15		
		GND_153	T17		
		GND_154	T19		
		GND_155	T21		
		GND_156	T23		
		GND_157	T25		
		GND_158	U11		
		GND_159	U12		
		GND_160	U13		
		GND_161	U14		
		GND_162	U15		
		GND_163	U16		
		GND_164	U17		
		GND_165	U18		
		GND_166	U19		
		GND_167	U20		
		GND_168	U21		
		GND_169	U22		
		GND_170	U23		
		GND_171	U24		
		GND_172	U25		
		GND_173	V12		
		GND_174	V14		
		GND_175	V16		
		GND_176	V18		
		GND_177	V2		
		GND_178	V20		
		GND_179	V22		
		GND_180	V24		
		GND_181	V31		
		GND_182	V5		
		GND_183	V9		
		GND_184	Y11		
		GND_185	Y13		
		GND_186	Y15		
		GND_187	Y17		
		GND_188	Y19		
		GND_189	Y21		
		GND_190	Y23		
		GND_191	Y25		

NVVDD Decoupling

+VGACORE

2/16

PLACE UNDER BALLS

C235	.01U/16V_4
C226	.01U/16V_4
C164	.01U/16V_4
C179	.01U/16V_4
C223	.01U/16V_4
C193	.01U/16V_4
C158	.033U/10V_4
C199	.033U/10V_4
C166	.033U/10V_4
C227	.047U/25V_4
C200	.047U/25V_4
C212	.047U/25V_4
C165	.1U/10V_4
C182	1U/6.3V_4
C170	1U/6.3V_4
C163	1U/6.3V_4

PLACE NEAR BALLS

C169	4.7U/6.3V_6
C215	10U/6.3V_8
C184	10U/6.3V_8

C131 330U/2.5V_6032

[38] +VGACORE

NB5

PROJECT : QL4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N10M-GE (POWER & GND) 5/5	E

Date: Friday, October 09, 2009 | Sheet 18 of 44

CHANNEL A: 256MBX32/512MB DDR3

[15] VMA_DQ[31..0]
[15] VMA_DM[7..0]
[15] VMA_WDQS[7..0]
[15] VMA_RDQS[7..0]

U15

SWAP

VREFC_VMA1
VREFD_VMA1

[15] FBA_CMD19
[15] FBA_CMD25
[15] FBA_CMD22
[15] FBA_CMD24
[15] FBA_CMD0
[15] FBA_CMD2
[15] FBA_CMD21
[15] FBA_CMD16
[15] FBA_CMD23
[15] FBA_CMD20
[15] FBA_CMD17
[15] FBA_CMD9
[15] FBA_CMD14
[15] FBA_CMD26

[15] FBA_CMD12
[15] FBA_CMD3
[15] FBA_CMD27

[15] VMA_CLK0
[15] VMA_CLK0#
[15] FBA_CMD18

[15] FBA_CMD30
[15] FBA_CMD29
[15] FBA_CMD1
[15] FBA_CMD10
[15] FBA_CMD11

11/12
VMA_WDQS2
VMA_RDQS2

VMA_DM2
VMA_DM0

11/12
VMA_WDQS0
VMA_RDQS0

[15] FBA_CMD15

VMA_ZQ1

R464
243/F_4

Should be 240 Ohms +-1%

DQU7 DQU6 DQU5 DQU4 DQU3 DQU2 DQU1 DQU0
VMA_DQ16 VMA_DQ22 VMA_DQ18 VMA_DQ23 VMA_DQ19 VMA_DQ20 VMA_DQ17 VMA_DQ21
VMA_DQ7 VMA_DQ2 VMA_DQ5 VMA_DQ1 VMA_DQ6 VMA_DQ0 VMA_DQ4 VMA_DQ3

+1.5V_GFX

96-BALL SDRAM DDR3
VRAM _DDR3

U37

SWAP

VREFC_VMA1
VREFD_VMA1

FBA_CMD19
FBA_CMD25
FBA_CMD22
FBA_CMD24
FBA_CMD0
FBA_CMD2
FBA_CMD21
FBA_CMD16
FBA_CMD23
FBA_CMD20
FBA_CMD17
FBA_CMD9
FBA_CMD14
FBA_CMD26

FBA_CMD12
FBA_CMD3
FBA_CMD27

VMA_CLK0
VMA_CLK0#
FBA_CMD18

FBA_CMD30
FBA_CMD29
FBA_CMD1
FBA_CMD10
FBA_CMD11

11/12
VMA_WDQS3
VMA_RDQS3

VMA_DM3
VMA_DM1

11/12
VMA_WDQS1
VMA_RDQS1

FBA_CMD15

VMA_ZQ2

R524
243/F_4

Should be 240 Ohms +-1%

DQU7 DQU6 DQU5 DQU4 DQU3 DQU2 DQU1 DQU0
VMA_DQ30 VMA_DQ26 VMA_DQ29 VMA_DQ28 VMA_DQ31 VMA_DQ25 VMA_DQ27 VMA_DQ24
VMA_DQ12 VMA_DQ10 VMA_DQ15 VMA_DQ8 VMA_DQ13 VMA_DQ11 VMA_DQ14 VMA_DQ9

+1.5V_GFX

96-BALL SDRAM DDR3
VRAM _DDR3

U16

SWAP

VREFC_VMA3
VREFD_VMA3

FBA_CMD19
FBA_CMD25
[15] FBA_CMD4
FBA_CMD4
FBA_CMD6
FBA_CMD5
[15] FBA_CMD13
FBA_CMD13
FBA_CMD21
FBA_CMD16
FBA_CMD23
FBA_CMD20
FBA_CMD17
FBA_CMD9
FBA_CMD14
FBA_CMD26

[15] FBA_CMD4
[15] FBA_CMD6
[15] FBA_CMD5
[15] FBA_CMD13

FBA_CMD12
FBA_CMD3
FBA_CMD27

[15] VMA_CLK1
[15] VMA_CLK1#
[15] FBA_CMD7

FBA_CMD7

[15] FBA_CMD28
[15] FBA_CMD8

FBA_CMD28
FBA_CMD8
FBA_CMD1
FBA_CMD10
FBA_CMD11

VMA_WDQS5
VMA_RDQS5
11/17 Swap

VMA_DM5
VMA_DM4

VMA_WDQS4
VMA_RDQS4

FBA_CMD15

VMA_ZQ3

R516
243/F_4

Should be 240 Ohms +-1%

DQU7 DQU6 DQU5 DQU4 DQU3 DQU2 DQU1 DQU0
VMA_DQ45 VMA_DQ43 VMA_DQ44 VMA_DQ41 VMA_DQ47 VMA_DQ40 VMA_DQ46 VMA_DQ42
VMA_DQ36 VMA_DQ39 VMA_DQ32 VMA_DQ38 VMA_DQ33 VMA_DQ37 VMA_DQ34 VMA_DQ35

+1.5V_GFX

96-BALL SDRAM DDR3
VRAM _DDR3

U36

SWAP

VREFC_VMA3
VREFD_VMA3

FBA_CMD19
FBA_CMD25
FBA_CMD4
FBA_CMD6
FBA_CMD5
FBA_CMD13
FBA_CMD21
FBA_CMD16
FBA_CMD23
FBA_CMD20
FBA_CMD17
FBA_CMD9
FBA_CMD14
FBA_CMD26

FBA_CMD12
FBA_CMD3
FBA_CMD27

VMA_CLK1
VMA_CLK1#
FBA_CMD7

FBA_CMD28
FBA_CMD8
FBA_CMD1
FBA_CMD10
FBA_CMD11

VMA_WDQS7
VMA_RDQS7
11/17 Swap

VMA_DM7
VMA_DM6

VMA_WDQS6
VMA_RDQS6

FBA_CMD15

VMA_ZQ4

R463
243/F_4

Should be 240 Ohms +-1%

DQU7 DQU6 DQU5 DQU4 DQU3 DQU2 DQU1 DQU0
VMA_DQ58 VMA_DQ63 VMA_DQ56 VMA_DQ61 VMA_DQ59 VMA_DQ57 VMA_DQ60 VMA_DQ62
VMA_DQ51 VMA_DQ53 VMA_DQ50 VMA_DQ52 VMA_DQ48 VMA_DQ54 VMA_DQ49 VMA_DQ55

+1.5V_GFX

96-BALL SDRAM DDR3
VRAM _DDR3

2/19
VMA_CLK0
R511
243/F_4
VMA_CLK0#

11/11 +1.5V_GFX
R520 1.33K/F_4
VREFC_VMA1
R521 1.33K/F_4
C676 .1U/10V_4

11/11 +1.5V_GFX
R526 1.33K/F_4
VREFD_VMA1
R525 1.33K/F_4
C677 .1U/10V_4

2/19
VMA_CLK1
R510
243/F_4
VMA_CLK1#

11/11 +1.5V_GFX
R518 1.33K/F_4
VREFC_VMA3
R517 1.33K/F_4
C674 .1U/10V_4

11/11 +1.5V_GFX
R512 1.33K/F_4
VREFD_VMA3
R513 1.33K/F_4
C673 .1U/10V_4

+1.5V_GFX
C271 1U/6.3V_4
C663 1U/6.3V_4
C639 1U/6.3V_4
C615 1U/6.3V_4

+1.5V_GFX
C697 10U/6.3V_6S
C635 .1U/10V_4
C266 .1U/10V_4
C612 .1U/10V_4
C609 .1U/10V_4
C636 .1U/10V_4

+1.5V_GFX
C624 .1U/10V_4
C616 .1U/10V_4
C625 .1U/10V_4
C228 .1U/10V_4
C623 .1U/10V_4
C607 .1U/10V_4
C695 .1U/10V_4
C680 .1U/10V_4

+1.5V_GFX
C634 .1U/10V_4
C638 .1U/10V_4
C619 .1U/10V_4
C637 .1U/10V_4
C693 .1U/10V_4
C236 .1U/10V_4
C685 .1U/10V_4
C692 .1U/10V_4

+1.5V_GFX
C683 .1U/10V_4
C678 .1U/10V_4
C686 .1U/10V_4
C675 .1U/10V_4

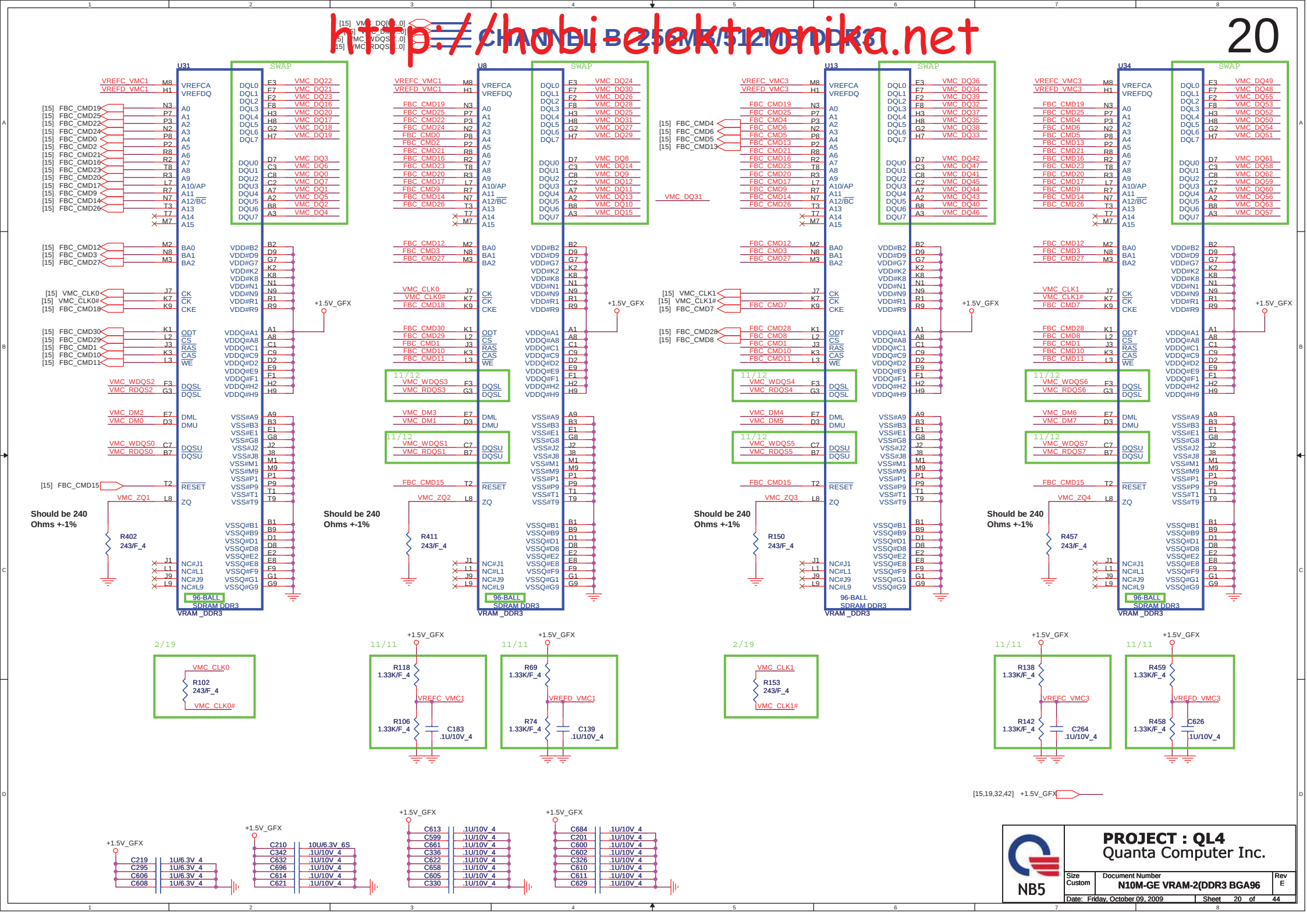
1211 for Nvidia request add transition cap

[15,20,32,42] +1.5V_GFX

NB5

PROJECT : QL4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N10M-GE VRAM-1(DDR3 BGA96	E
Date: Friday, October 09, 2009	Sheet 19 of 44	



PROJECT : QL4	
Quanta Computer Inc.	
NB5	
Size: Custom	Document Number: N10M-GE VRAM-2(DDR3 BGA96)
Rev: E	
Date: Friday, October 09, 2009	Sheet 20 of 44

1. If LCD connector near GPU, then place these series Resistors near GPU
2. If LCD connector near N/B, then place these series Resistors near N/B

OPTION SIGNAL FROM NB FOR UMA VGA

[7,32] LA_CLK#	RP8	3	4	*0_4P2R	TXLCLKOUT-
[7,32] LA_CLK		1	2		TXLCLKOUT+
[7,32] LA_DATAP0	RP2	1	2	*0_4P2R	TXLOUT0+
[7,32] LA_DATAN0		3	4		TXLOUT0-
[7,32] LA_DATAP1	RP4	1	2	*0_4P2R	TXLOUT1+
[7,32] LA_DATAN1		3	4		TXLOUT1-
[7,32] LA_DATAN2	RP6	3	4	*0_4P2R	TXLOUT2-
[7,32] LA_DATAP2		1	2		TXLOUT2+
[7,32] LB_CLK	RP16	1	2	*0_4P2R	TXUCLKOUT+
[7,32] LB_CLK#		3	4		TXUCLKOUT-
[7,32] LB_DATAN0	RP10	3	4	*0_4P2R	TXUOUT0-
[7,32] LB_DATAP0		1	2		TXUOUT0+
[7,32] LB_DATAP1	RP12	3	4	*0_4P2R	TXUOUT1-
[7,32] LB_DATAN1		1	2		TXUOUT1+
[7,32] LB_DATAP2	RP14	1	2	*0_4P2R	TXUOUT2+
[7,32] LB_DATAN2		3	4		TXUOUT2-

OPTION SIGNAL FROM Nvidia to VGA

[16,32] EXT_TXLCLKOUT-	RP7	1	2	0_4P2R	TXLCLKOUT-
[16,32] EXT_TXLCLKOUT+		3	4		TXLCLKOUT+
[16,32] EXT_TXLOUT0-	RP1	1	2	0_4P2R	TXLOUT0-
[16,32] EXT_TXLOUT0+		3	4		TXLOUT0+
[16,32] EXT_TXLOUT1+	RP3	3	4	0_4P2R	TXLOUT1+
[16,32] EXT_TXLOUT1-		1	2		TXLOUT1-
[16,32] EXT_TXLOUT2-	RP5	1	2	0_4P2R	TXLOUT2-
[16,32] EXT_TXLOUT2+		3	4		TXLOUT2+
[16,32] EXT_TXUCLKOUT-	RP15	1	2	0_4P2R	TXUCLKOUT-
[16,32] EXT_TXUCLKOUT+		3	4		TXUCLKOUT+
[16,32] EXT_TXUOUT0-	RP9	1	2	0_4P2R	TXUOUT0-
[16,32] EXT_TXUOUT0+		3	4		TXUOUT0+
[16,32] EXT_TXUOUT1+	RP11	3	4	0_4P2R	TXUOUT1+
[16,32] EXT_TXUOUT1-		1	2		TXUOUT1-
[16,32] EXT_TXUOUT2+	RP13	3	4	0_4P2R	TXUOUT2+
[16,32] EXT_TXUOUT2-		1	2		TXUOUT2-

CN2

+3VLCD_CON, C4 1000P/50V_4, +3V

[7,17,32] EDIDCLK
[7,17,32] EDIDDATA

B-stage change

[32] TXLOUT0-	TXLOUT0-
[32] TXLOUT0+	TXLOUT0+
[32] TXLOUT1-	TXLOUT1-
[32] TXLOUT1+	TXLOUT1+
[32] TXLOUT2-	TXLOUT2-
[32] TXLOUT2+	TXLOUT2+
[32] TXLCLKOUT-	TXLCLKOUT-
[32] TXLCLKOUT+	TXLCLKOUT+
[32] TXUOUT0-	TXUOUT0-
[32] TXUOUT0+	TXUOUT0+
[32] TXUOUT1-	TXUOUT1-
[32] TXUOUT1+	TXUOUT1+
[32] TXUOUT2-	TXUOUT2-
[32] TXUOUT2+	TXUOUT2+
[32] TXUCLKOUT-	TXUCLKOUT-
[32] TXUCLKOUT+	TXUCLKOUT+

[7,17,32] DPST_PWM
[29] PWM_VADJ
R5 0_4
R4 *0_4
C6 *4.7U/6.3V_6
C8 *.1U/10V_4
BLON_CON
+VIN_BLIGHT

FOX-GS12401-1011

+5VSUS, 14.5v, +15VALW, +3V

R377 100K/F_4
R375 330K_6
AO3404 ID current 5.8A
C542 .1U/10V_4

Q18 AO3404
LCDONG
+3VLCD
+3VLCD_CON
L1 PBY201209T-4A/08
C1 *.01U/25V_4
C3 .1U/10V_4
C2 *10U/6.3V_8
R374 22_8
LCDDISCHG

Q21 2N7002E
C541 .027U/25V_6
LCDON#
Q19 2N7002E
Q20 DTC144EUA
[7,17,32] DISP_ON

Delete in PV 0622

DISP_ON
LVDS_BLON
R376 100K/F_4
R9 100K/F_4

B-stage change to 100k Ohm

+VIN_BLIGHT
+VIN
L2 FBM2125 HM330-T +VIN_BLIGHT
C7 .1U/50V_6
C9 *10U/25V_12
C10 .1U/50V_6
C11 .01U/16V_4

R6 100K/F_4
C12 22P/50V_4
PN_BLON
BLON_CON
D2 RB500V-40

Close to EC

[7,17,32] LVDS_BLON
R8 1K/F_4
R7 47K_4
+3VPCU
D3 RB500V-40
D14 *RB501V-40
LID_EC# [28,29]
HWPG [3,29,34,35,36,38,39]

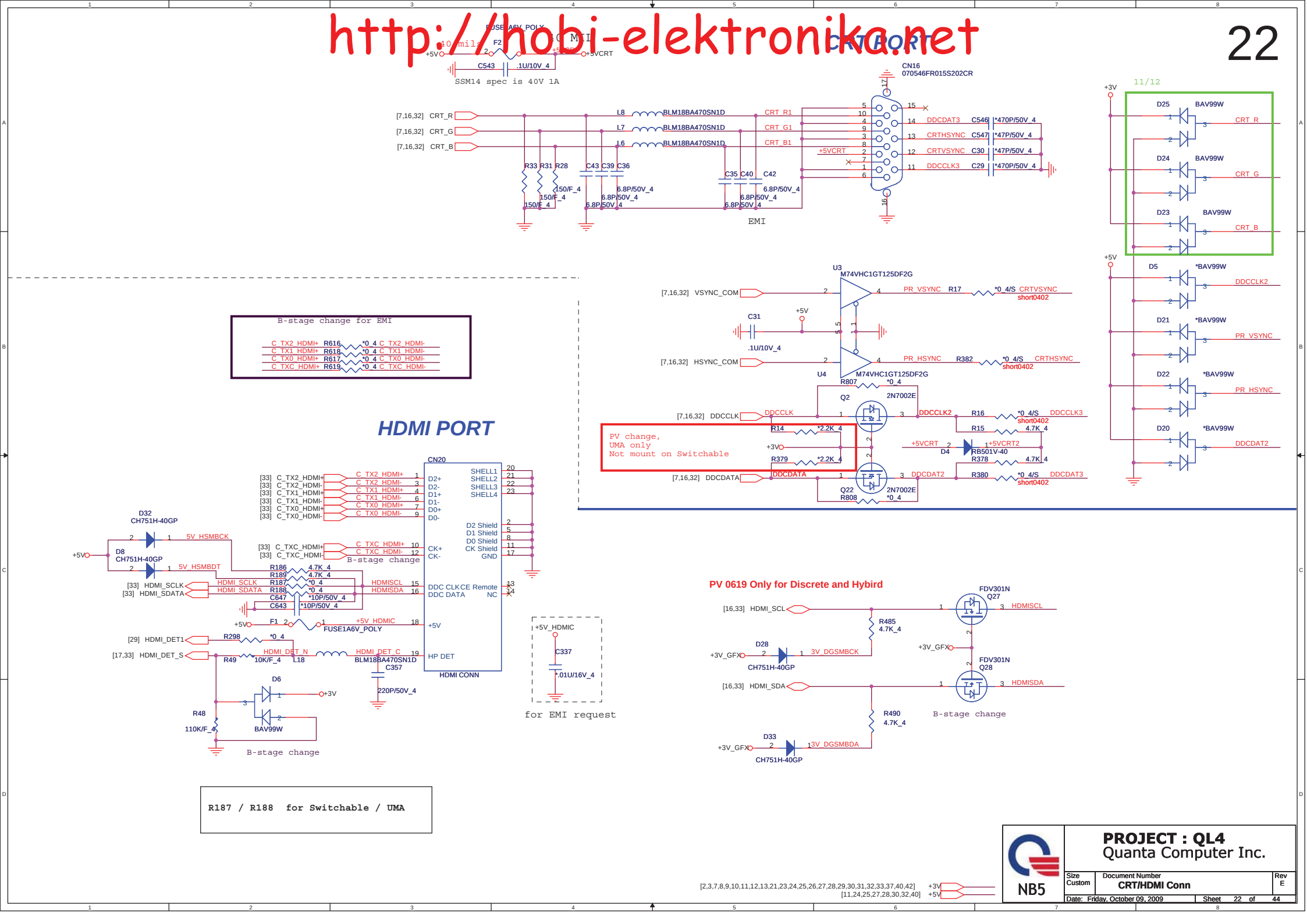
[10] LCD_BK
Q1 DTC144EUA

[2,3,7,8,9,10,11,12,13,22,23,24,25,26,27,28,29,30,31,32,33,37,40,42] +3V
[3,7,25,28,29,30,34,35,36,38,40,41,42] +3VPCU
[11,22,24,25,27,28,30,32,40] +5V
[24,27,28,40] +5VSUS
[35,40] +15VALW
[2,34,35,36,37,38,39,40,41,42] +VIN

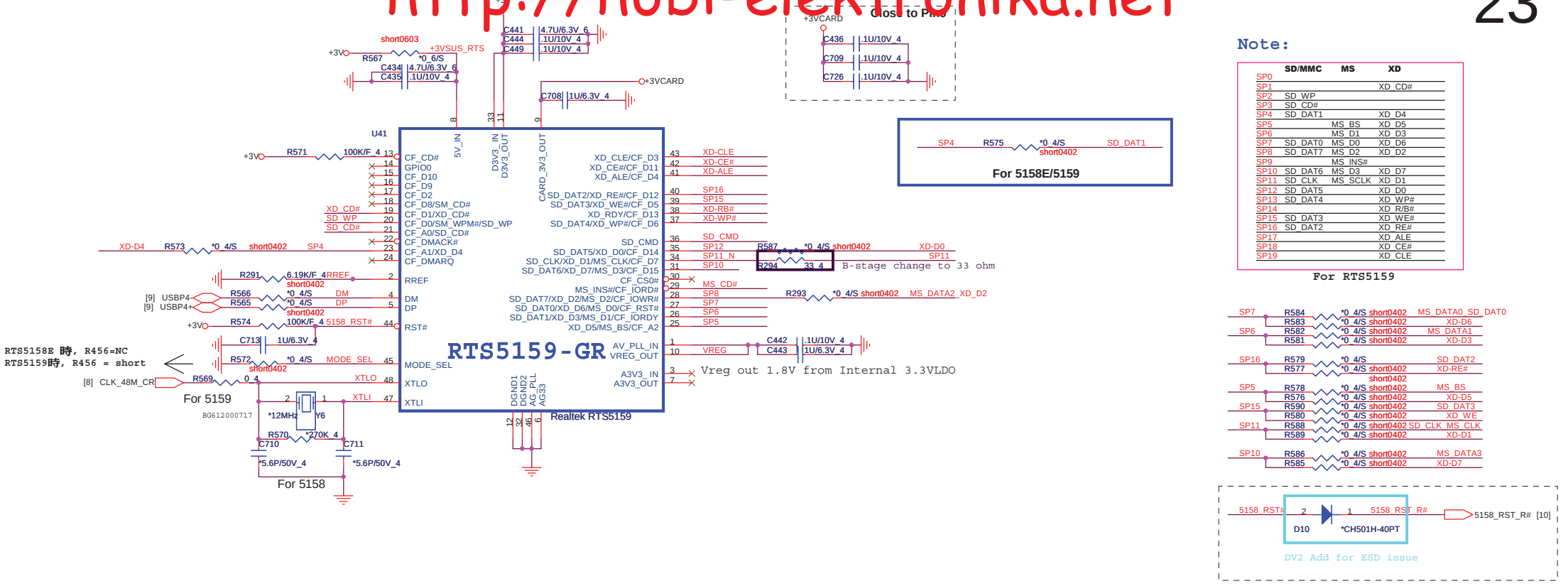
NB5

PROJECT : QL4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN	E
Date: Friday, October 09, 2009	Sheet 21 of 44	



NB5	PROJECT : QL4 Quanta Computer Inc.
Size: Custom	Document Number: CRT/HDMI Conn
Rev: E	
Date: Friday, October 09, 2009	Sheet 22 of 44

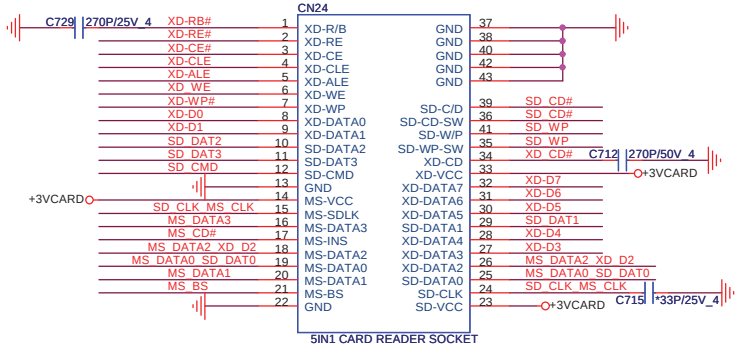


Note:

	SD/MMC	MS	XD
SP0			
SP1			XD_CD#
SP2	SD_WP		
SP3	SD_CD#		
SP4	SD_DAT1		XD_D4
SP5		MS_BS	XD_D5
SP6		MS_D1	XD_D3
SP7	SD_DAT0	MS_D0	XD_D6
SP8	SD_DAT7	MS_D2	XD_D2
SP9		MS_INS#	
SP10	SD_DAT6	MS_D3	XD_D7
SP11	SD_CLK	MS_SCLK	XD_D1
SP12	SD_DAT5		XD_D0
SP13	SD_DAT4		XD_WP#
SP14			XD_R/B#
SP15	SD_DAT3		XD_WE#
SP16	SD_DAT2		XD_RE#
SP17			XD_ALE
SP18			XD_CE#
SP19			XD_CLE

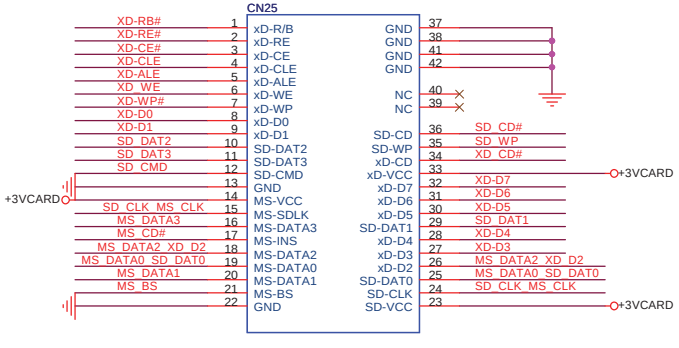
For RTS5159

5 IN1 CARD READER
XD,MMC/SD,MS/MSP

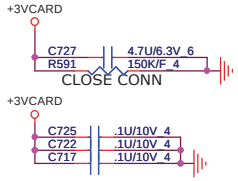


PV change footprint

DV2 add 2'nd source

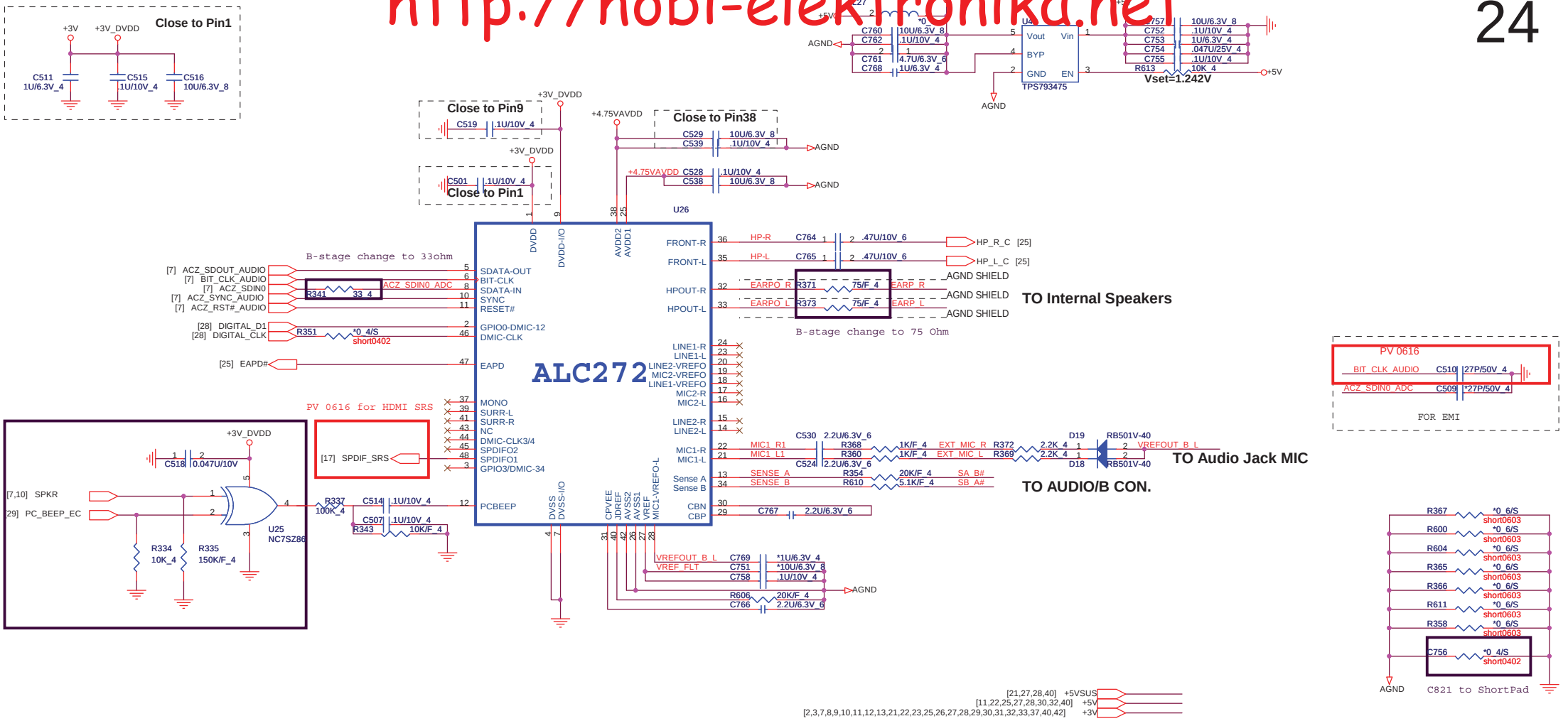


PV change footprint



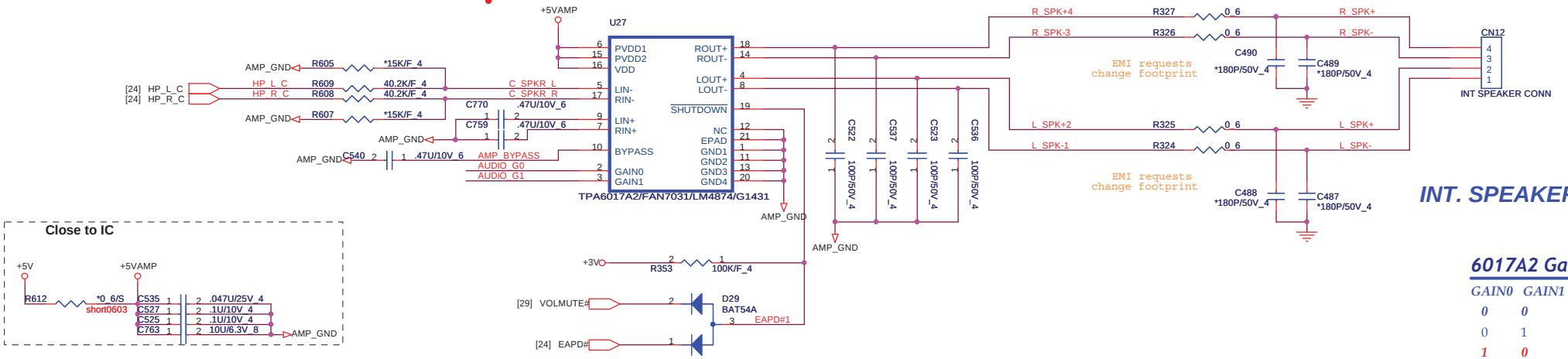
[2,3,7,8,9,10,11,12,13,21,22,24,25,26,27,28,29,30,31,32,33,37,40,42] +3V

NB5	PROJECT : QL4 Quanta Computer Inc.	
Size: Custom	Document Number: RTS5159 &CR SOCKET	Rev: E
Date: Friday, October 09, 2009	Sheet 23 of 44	



NB5	PROJECT : QL4 Quanta Computer Inc.	
Size: Custom	Document Number: Azalia ALC272/BT CONN	Rev: E
Date: Friday, October 09, 2009	Sheet 24 of 44	

AUDIO AMPLIFIER



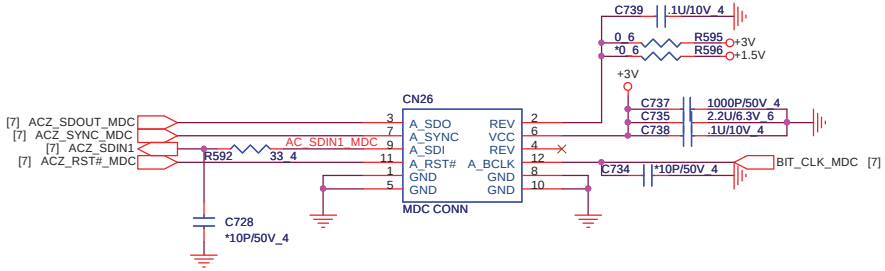
INT. SPEAKER

AL001431K04
AL6017A2K12
APA2031 ,AL002031K00

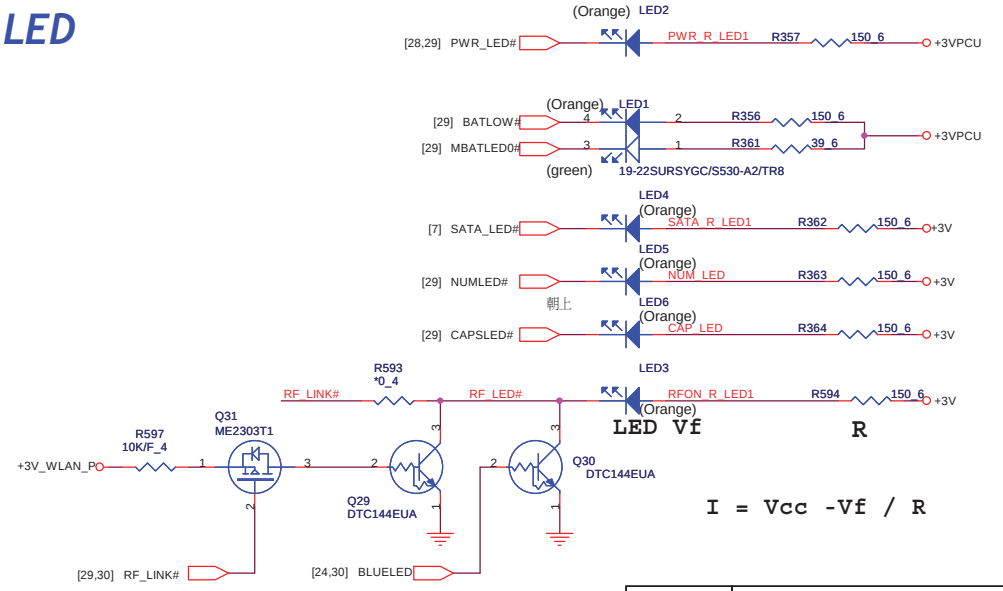
6017A2 Gain Table

GAIN0	GAIN1	AV(INV)
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

MDC CONNECTOR



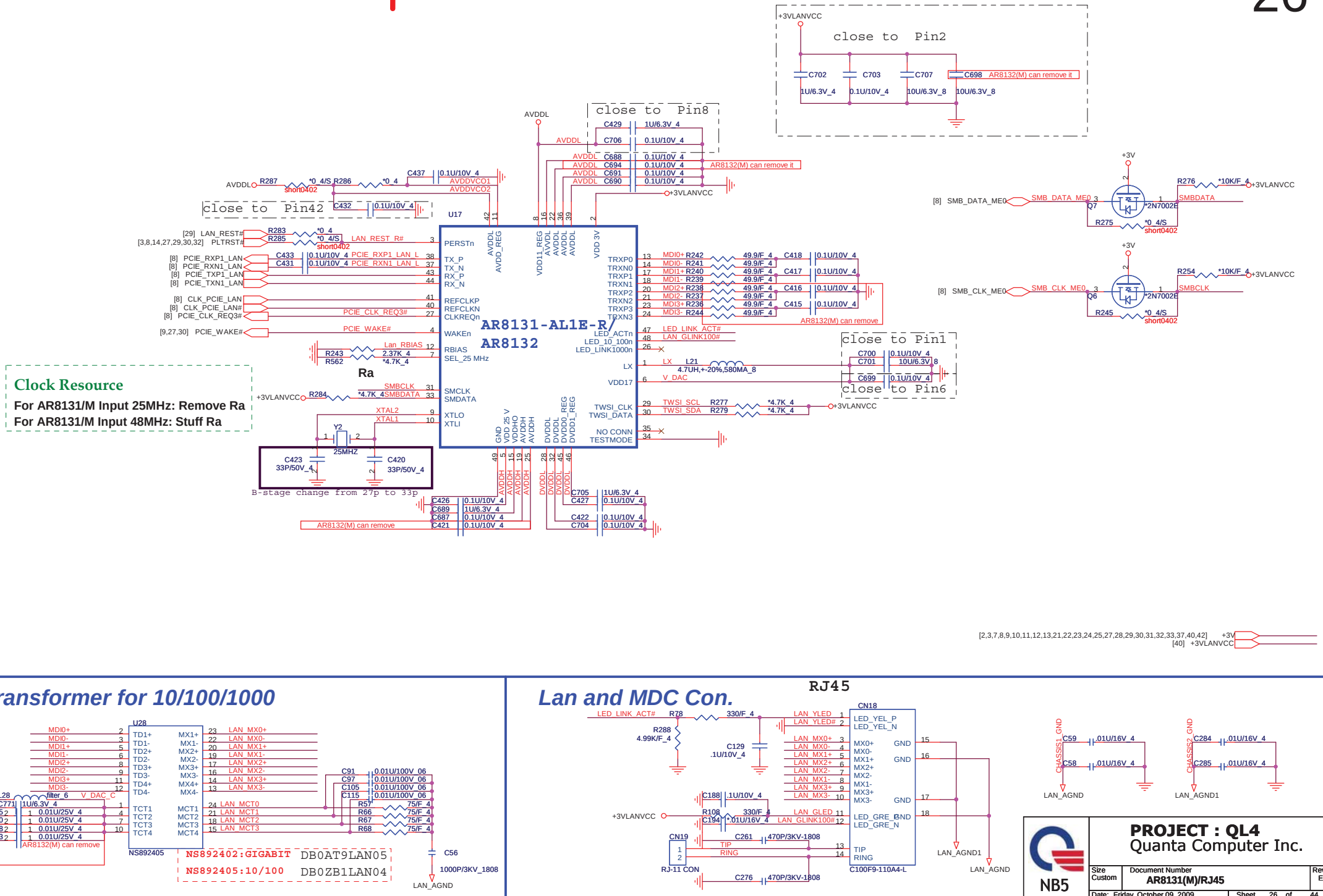
LED



[11,22,24,27,28,30,32,40] +5V
[3,7,21,28,29,30,34,35,36,38,40,41,42] +3VPCU
[2,3,7,8,9,10,11,12,13,21,22,23,24,26,27,28,29,30,31,32,33,37,40,42] +3V

PROJECT : QL4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	AMP_TPA6017/SPK/MDC/LED	E
NB5	Date: Friday, October 09, 2009	Sheet 25 of 44



Clock Resource

For AR8131/M Input 25MHz: Remove Ra

For AR8131/M Input 48MHz: Stuff Ra

Transformer for 10/100/1000

Lan and MDC Con.

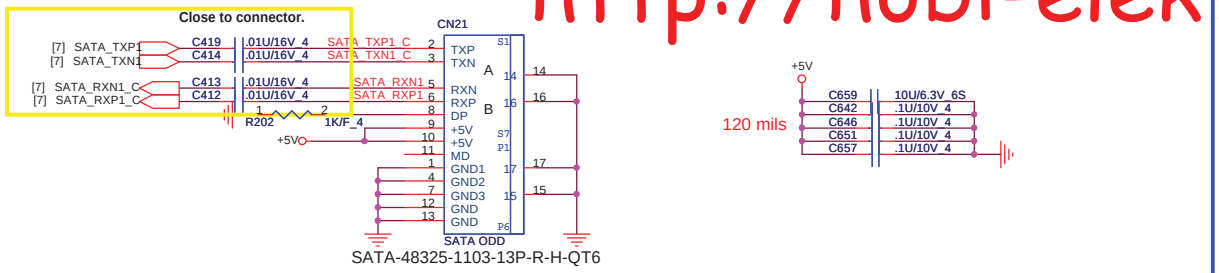
RJ45

NB5

PROJECT : QL4
Quanta Computer Inc.

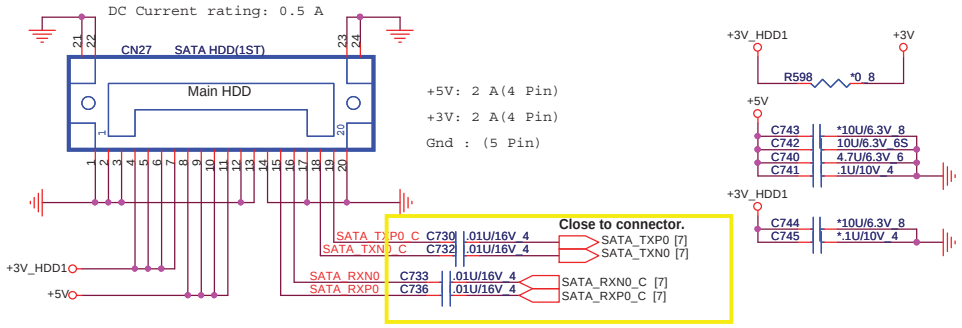
Size	Document Number	Rev
Custom	AR8131(M)/RJ45	E
Date: Friday, October 09, 2009	Sheet 26 of 44	

SATA ODD

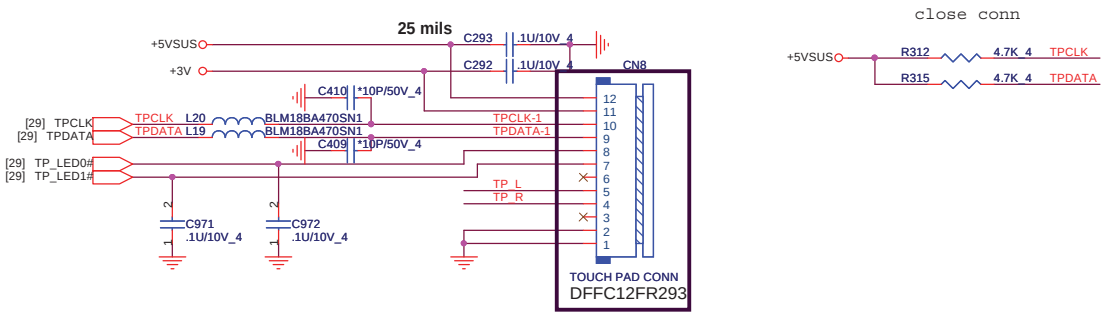


SATA-48325-1103-13P-R-H-QT6

SATA_1 CONNECTOR

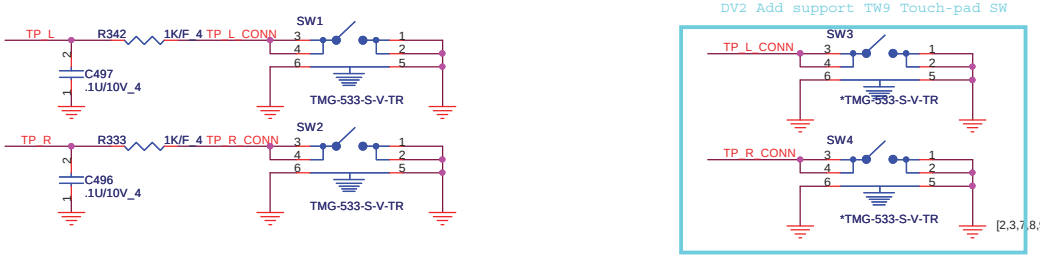


TOUCH PAD CONNECTOR

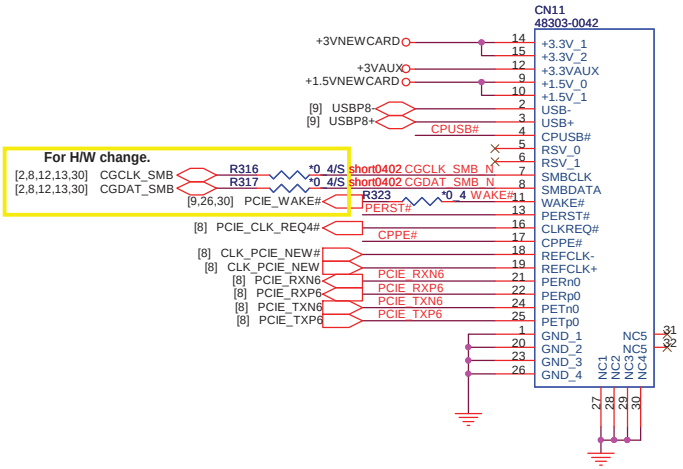


B-stage change footprint to BL121-12R-TAND-12P-L

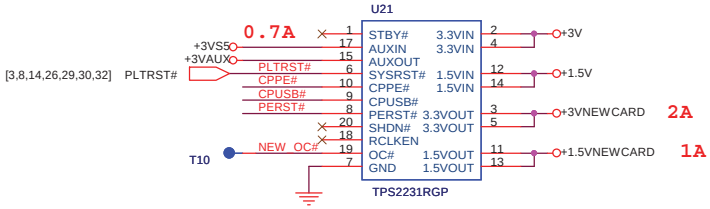
TOUCH PAD L/R SW1,SW2 in QL4 use, SW3,SW4 in TW9 use



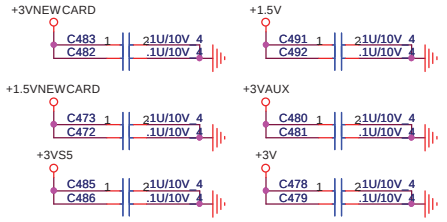
NEWCARD (PCIEXPRESS*1 + USB*1)

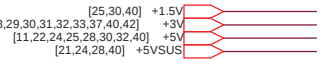


Change CN15#31,32 as ME request for Hole pad
expcard-48303-0042-26p-1-qt6 as ME modify Pad size(pin31,32)
Move CN15#29,30 Pin as ME request(Molex confirm drawing)



Change net name from 3V_NEWAUX to 3VAUX



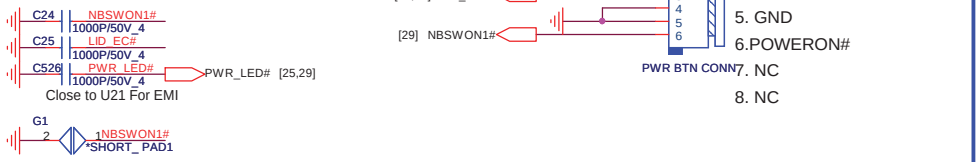


NB5

PROJECT : QL4
Quanta Computer Inc.

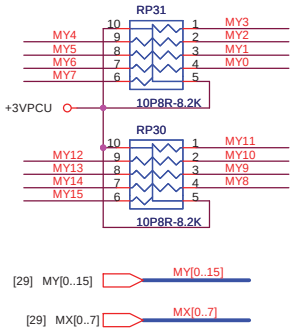
Size	Document Number	Rev
Custom	ODD/HDD/NEW CARD/TP	E
Date: Friday, October 09, 2009	Sheet 27 of 44	

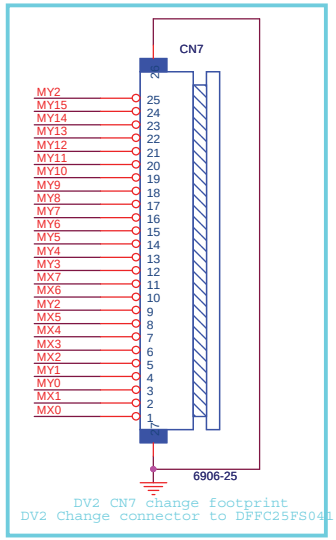
POWER BOTTON CONNECT



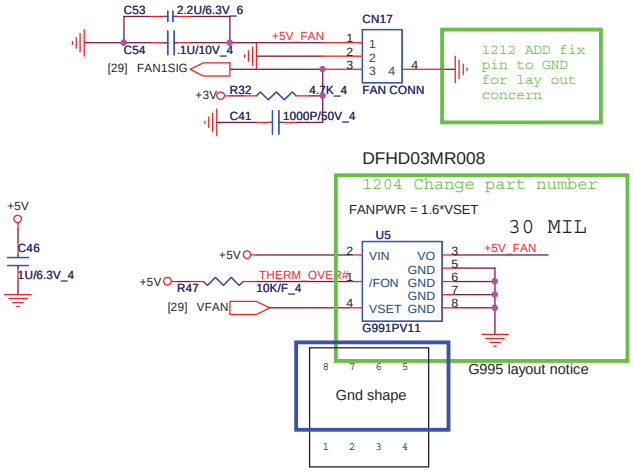
KEYBOARD CON.

KEYBOARD PULL-UP

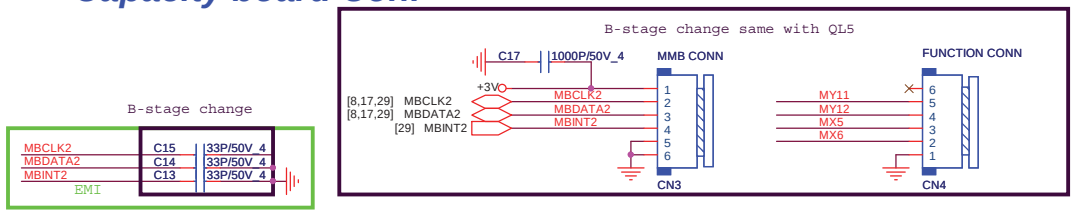




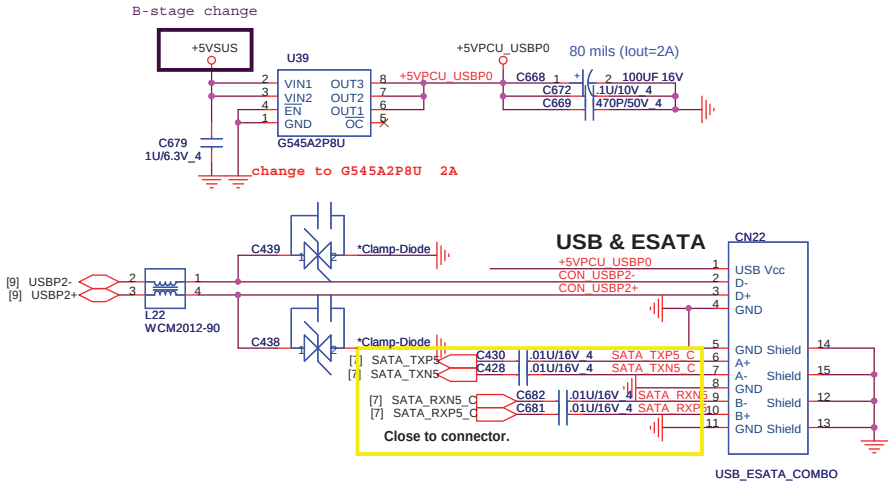
CPU FAN



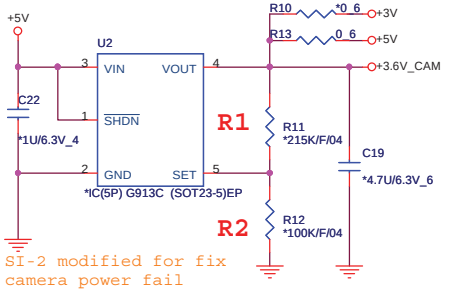
Capacity board Con.

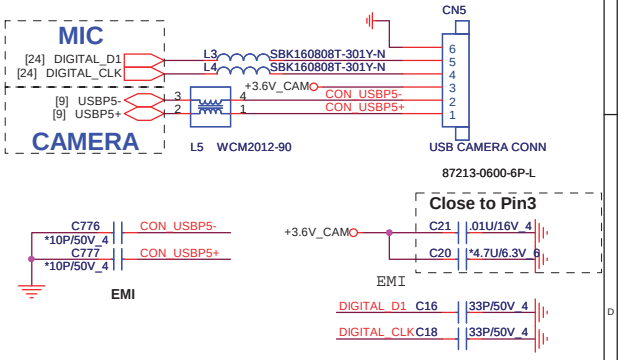


E-SATA/USB COMBO



USB CAMERA POWER



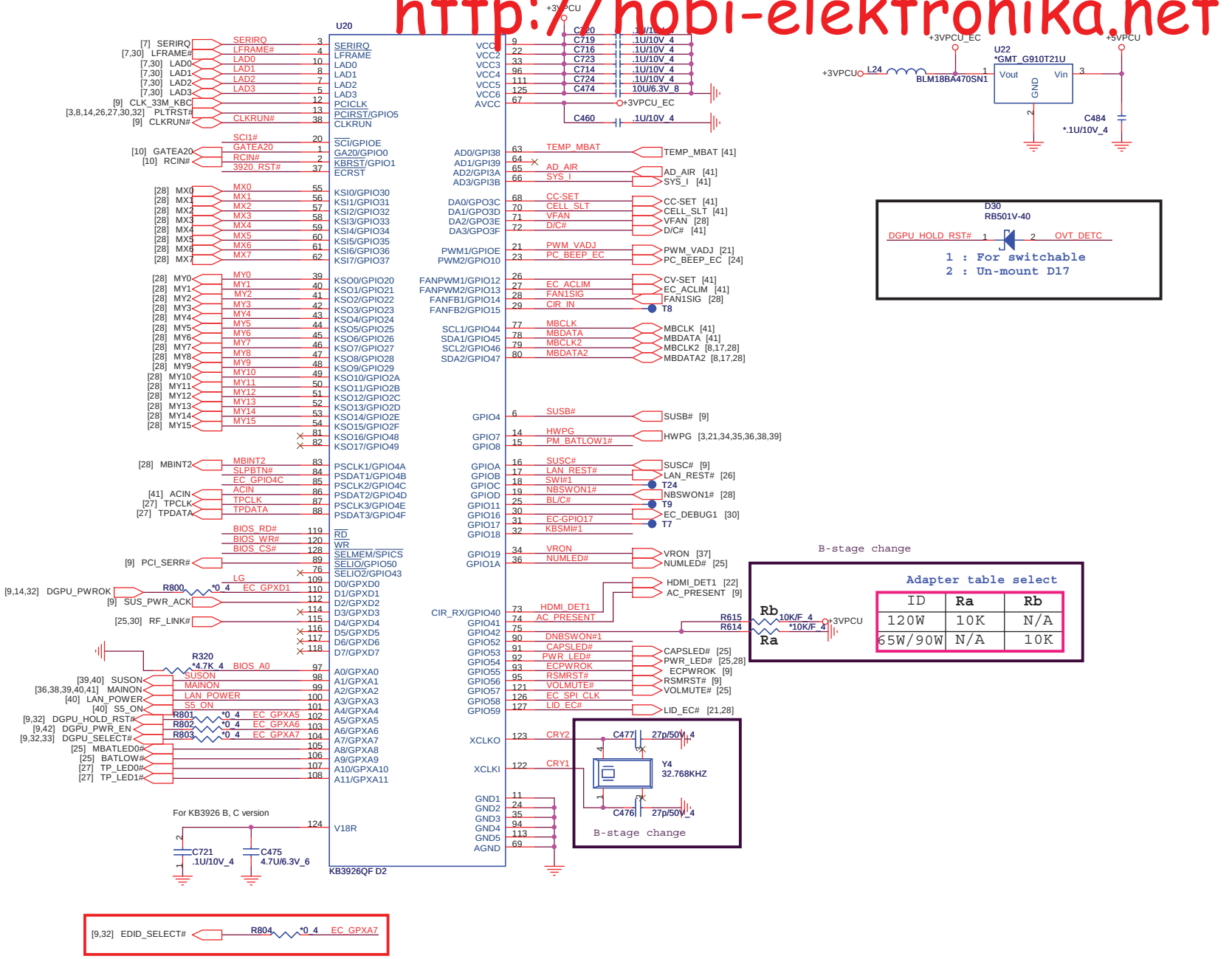


[11,22,24,25,27,30,32,40] +5V
[2,3,7,8,9,10,11,12,13,21,22,23,24,25,26,27,29,30,31,32,33,37,40,42] +3V
[3,7,21,25,29,30,34,35,36,38,40,41,42] +3VPCU
[29,34,35,36,37,38,39,40] +5VPCU

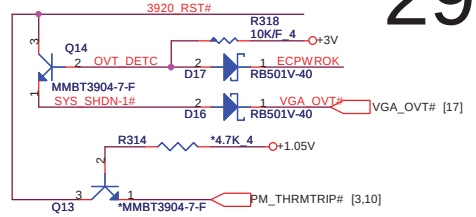
PROJECT : QL4
Quanta Computer Inc.

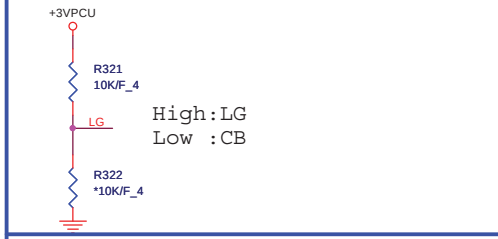
NB5

Size	Document Number	Rev
Custom	KB/PWR/ESATA/FAN/CAM/MIC	E
Date: Friday, October 09, 2009	Sheet 28 of 44	



thermal shutdown circuit

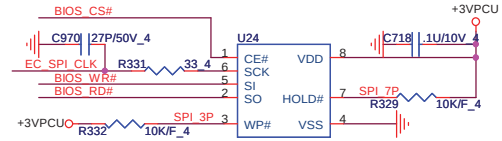


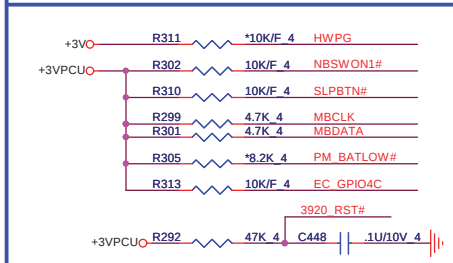


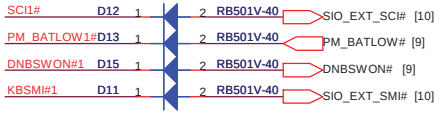
SPI BIOS

512K byte SPI ROM for EC — **SPI ROM Socket**

MXIC: AKE3KZP0001 DG008000031
WINBOND: AKE37ZN0N00
AIT: AKE37ZN0800







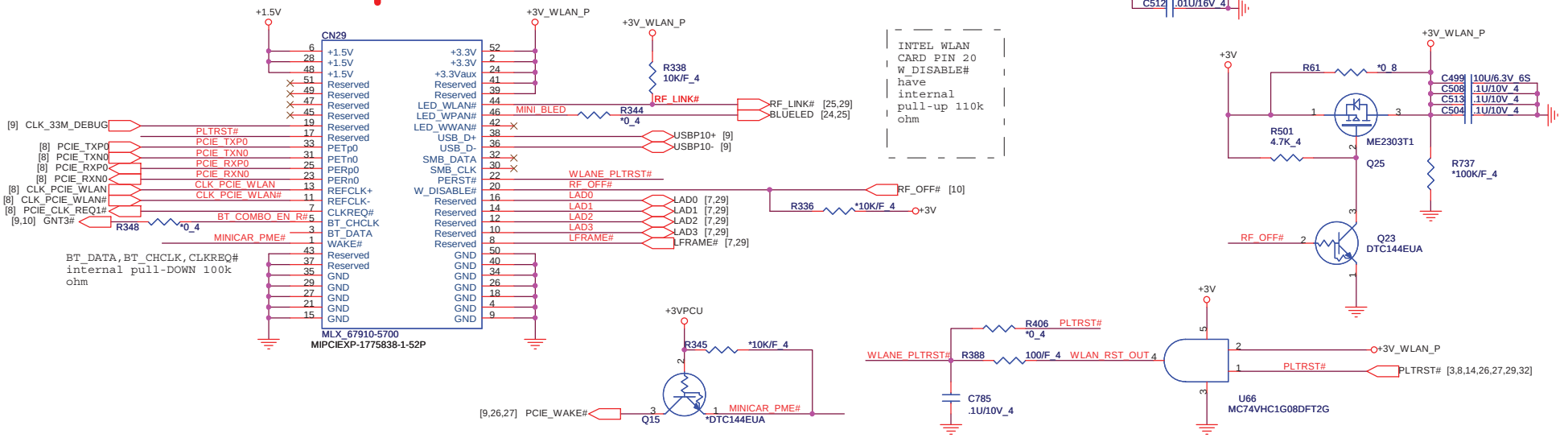
NB5

PROJECT : QL4
Quanta Computer Inc.

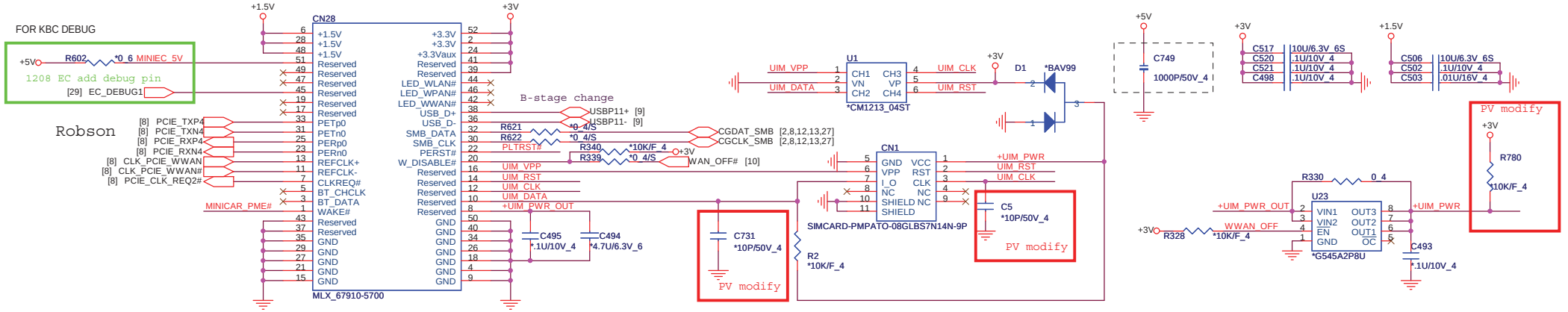
Size	Document Number	Rev
Custom	KB3926/ROM/TP	E

Date: Friday, October 09, 2009 Sheet 29 of 44

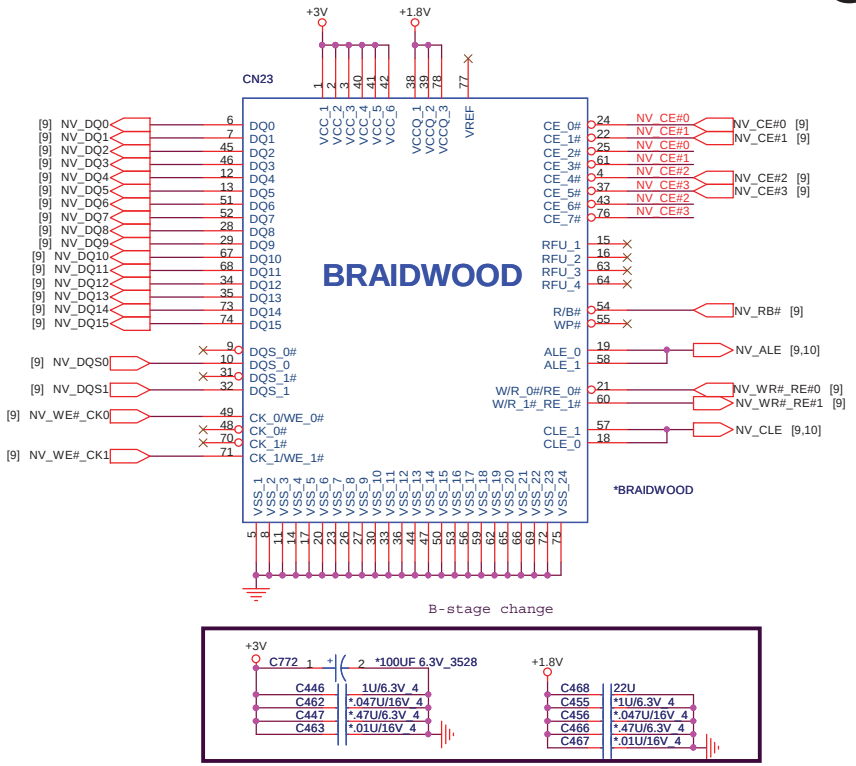
Mini PCI-E Card 1
WLAN



Mini PCI-E Card 2
WWAN& Robson



PV 0616 DEL debug Con.



PV 0616 DEL debug Con.

[3,5,10,11,34,38] +1.1V_VTT
[2,7,8,9,11,29,34,36,42] +1.05V
[5,10,11,36,40,42] +1.8V
[2,3,7,8,9,10,11,12,13,21,22,23,24,25,26,27,28,29,30,32,33,37,40,42] +3V
[8,9,10,11,14,27,40] +3VS5

NB5

PROJECT : QL4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	XDP/BRAIDWOOD	E
Date: Friday, October 09, 2009	Sheet 31 of 44	

LVDS Channel Switch

DGPU_Channel-A/B

IGPU_Channel-A /B

U38

PI3LVD1012

To LVDS Conn.

To LVDS Conn.

BKLTCTL_PWM

BKLTEN / LVDDEN

SEL	FUNCTION
LOW	DGPU
HIGH	IGPU

SELx	Ay
LOW	B1
HIGH	B2

LVDS/CRT DDC Switch

U59

74CBT3257

VGA SWITCH

U62

PI3V512

U65

74LVC1G3157GW

S	Yn
0	B0
1	B1

U63 MC74VHC1G08DFT2G

Q67 MMBT3904-7-F

Q70 MMBT3904-7-F

Q69 MMBT3904-7-F

Q71 MMBT3904-7-F

Q73 *MMBT3904-7-F

PROJECT : QL4
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	HDMI Switch / Power CRTL	E
Date: Friday, October 09, 2009	Sheet 32 of 44	

DGPU_HDMI

[16] H_TXC_HDMI+ C374 .1U/10V_4 DGPU_TXC_HDMI+
[16] H_TXC_HDMI- C360 .1U/10V_4 DGPU_TXC_HDMI-
[16] H_TX0_HDMI+ C386 .1U/10V_4 DGPU_TX0_HDMI+
[16] H_TX0_HDMI- C381 .1U/10V_4 DGPU_TX0_HDMI-
[16] H_TX1_HDMI+ C401 .1U/10V_4 DGPU_TX1_HDMI+
[16] H_TX1_HDMI- C393 .1U/10V_4 DGPU_TX1_HDMI-
[16] H_TX2_HDMI+ C403 .1U/10V_4 DGPU_TX2_HDMI+
[16] H_TX2_HDMI- C408 .1U/10V_4 DGPU_TX2_HDMI-

HDMISwitch

U64 PI3HDMI201

DGPU_TXC_HDMI- 55 CLK-A
DGPU_TXC_HDMI+ 56 CLK+A
DGPU_TX0_HDMI- 2 D0-A
DGPU_TX0_HDMI+ 3 D0+A
DGPU_TX1_HDMI- 5 D1-A
DGPU_TX1_HDMI+ 6 D1+A
DGPU_TX2_HDMI- 8 D2-A
DGPU_TX2_HDMI+ 9 D2+A

+3V → VDD (41, 35, 19, 13, 7, 1)

HPD_SINK 47 HDMI_DET_S → HDMI_DET_S [17,22]
SDA_SINK 46 → HDMI_SDATA [22]
SCL_SINK 45 → HDMI_SCLK [22]

[17] HDMI_DET 51 HPDA
[16,22] HDMI_SDA 52 SDAA
[16,22] HDMI_SCL 53 SCLA
[7] HDMI_HPD_CON 23 HPDB
[7] SDVO_DATA 24 SDAB
[7] SDVO_CLK 25 SCLB

CLK- 43 → C_TXC_HDMI- [22]
CLK+ 42 → C_TXC_HDMI+ [22]
D0- 40 → C_TX0_HDMI- [22]
D0+ 39 → C_TX0_HDMI+ [22]
D1- 37 → C_TX1_HDMI- [22]
D1+ 36 → C_TX1_HDMI+ [22]
D2- 34 → C_TX2_HDMI- [22]
D2+ 33 → C_TX2_HDMI+ [22]

PAD_GND 57
GND 4, 10, 16, 22, 32, 38, 44, 54

[7] IN_CLK# 11 CLK-B
[7] IN_CLK 12 CLK+B
[7] IN_D0# 14 D0-B
[7] IN_D0 15 D0+B
[7] IN_D1# 17 D1-B
[7] IN_D1 18 D1+B
[7] IN_D2# 20 D2-B
[7] IN_D2 21 D2+B

EQ_S1, EQ_S0, OC_S2, OC_S1, OC_S0, OE, SEL2, SEL1

HSW_EQS1 26
HSW_EQS0 28
HSW_OCS2 29
HSW_OCS1 30
HSW_OCS0 31
HSW_ON# 50
HSW_SEL2 27
HSW_SEL1 49

To HDMI Conn.

IGPU_HDMI

+3V
R507 2.2K/F_4 SDVO_DATA
R508 2.2K/F_4 SDVO_CLK

+3V
C955 0.1U/10V_4
C954 0.1U/10V_4
C945 0.1U/10V_4
C950 0.1U/10V_4

OC SETTING
S2 S1 S0 = 1 : 1 : 1 500mV 0dB Defualt
S2 S1 S0 = 1 : 1 : 0 750mV 0dB
S2 S1 S0 = 1 : 0 : 1 1000mV 0dB
S2 S1 S0 = 1 : 0 : 0 600mV 0dB
S2 S1 S0 = 0 : 1 : 1 500mV 0dB
S2 S1 S0 = 0 : 1 : 0 500mV 1.5dB
S2 S1 S0 = 0 : 0 : 1 500mV 3.5dB
S2 S1 S0 = 0 : 0 : 0 500mV 6dB

EQ SETTING
S1 S0 = 1 : 1 3dB Defualt
S1 S0 = 1 : 0 8dB
S1 S0 = 0 : 1 3dB
S1 S0 = 0 : 0 15dB

OE#	SEL2	SEL1	Ay
0	X	1	A
0	1	0	B

HSW_EQS1 R629 *4.7K_4
HSW_EQS0 R628 *4.7K_4
HSW_OCS2 R627 *4.7K_4
HSW_OCS1 R626 *4.7K_4
HSW_OCS0 R624 *4.7K_4
HSW_ON# R623 4.7K_4

+3V
R630 4.7K_4
HSW_SEL1
R793 *4.7K_4
Q33 DTC144EUA
DGPU_SELECT# → DGPU_SELECT# [9,29,32]
R631 0_4 HSW_SEL2
R794 *4.7K_4
+3V

Mount R793 and R794 for UMA only

Only for NVIDIA

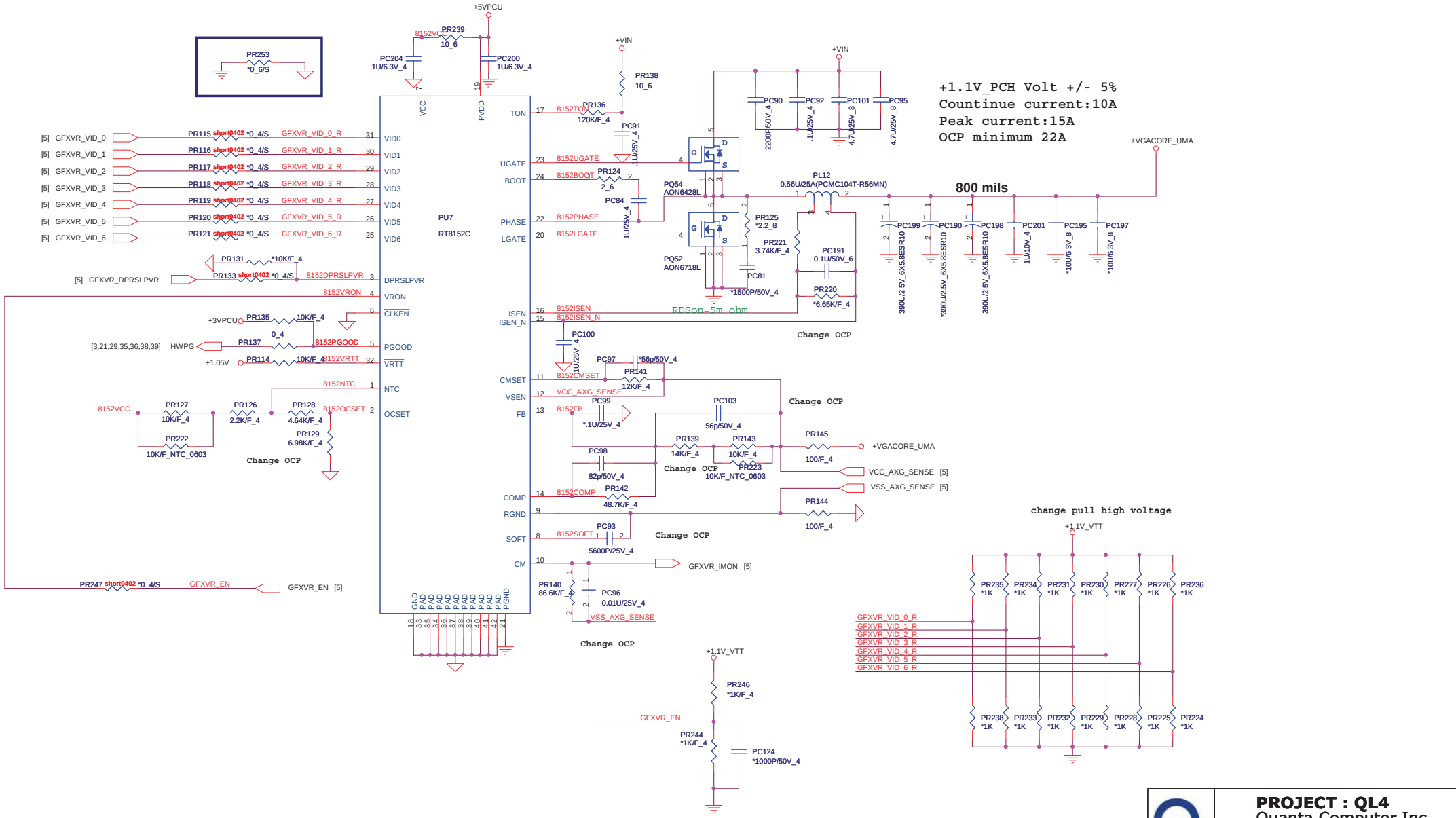
+3V_GFX
Q26 2N7002E

R493 499/F_4 DGPU_TXC_HDMI+
R495 499/F_4 DGPU_TXC_HDMI-
R488 499/F_4 DGPU_TX0_HDMI+
R486 499/F_4 DGPU_TX0_HDMI-
R483 499/F_4 DGPU_TX1_HDMI+
R481 499/F_4 DGPU_TX1_HDMI-
R478 499/F_4 DGPU_TX2_HDMI+
R475 499/F_4 DGPU_TX2_HDMI-

DGPU_TXC_HDMI- RP19 0_4P2R C_TXC_HDMI-
DGPU_TXC_HDMI+ C_TXC_HDMI+
DGPU_TX0_HDMI- RP18 0_4P2R C_TX0_HDMI-
DGPU_TX0_HDMI+ C_TX0_HDMI+
DGPU_TX1_HDMI- RP20 0_4P2R C_TX1_HDMI-
DGPU_TX1_HDMI+ C_TX1_HDMI+
DGPU_TX2_HDMI+ RP17 0_4P2R C_TX2_HDMI+
DGPU_TX2_HDMI- C_TX2_HDMI-

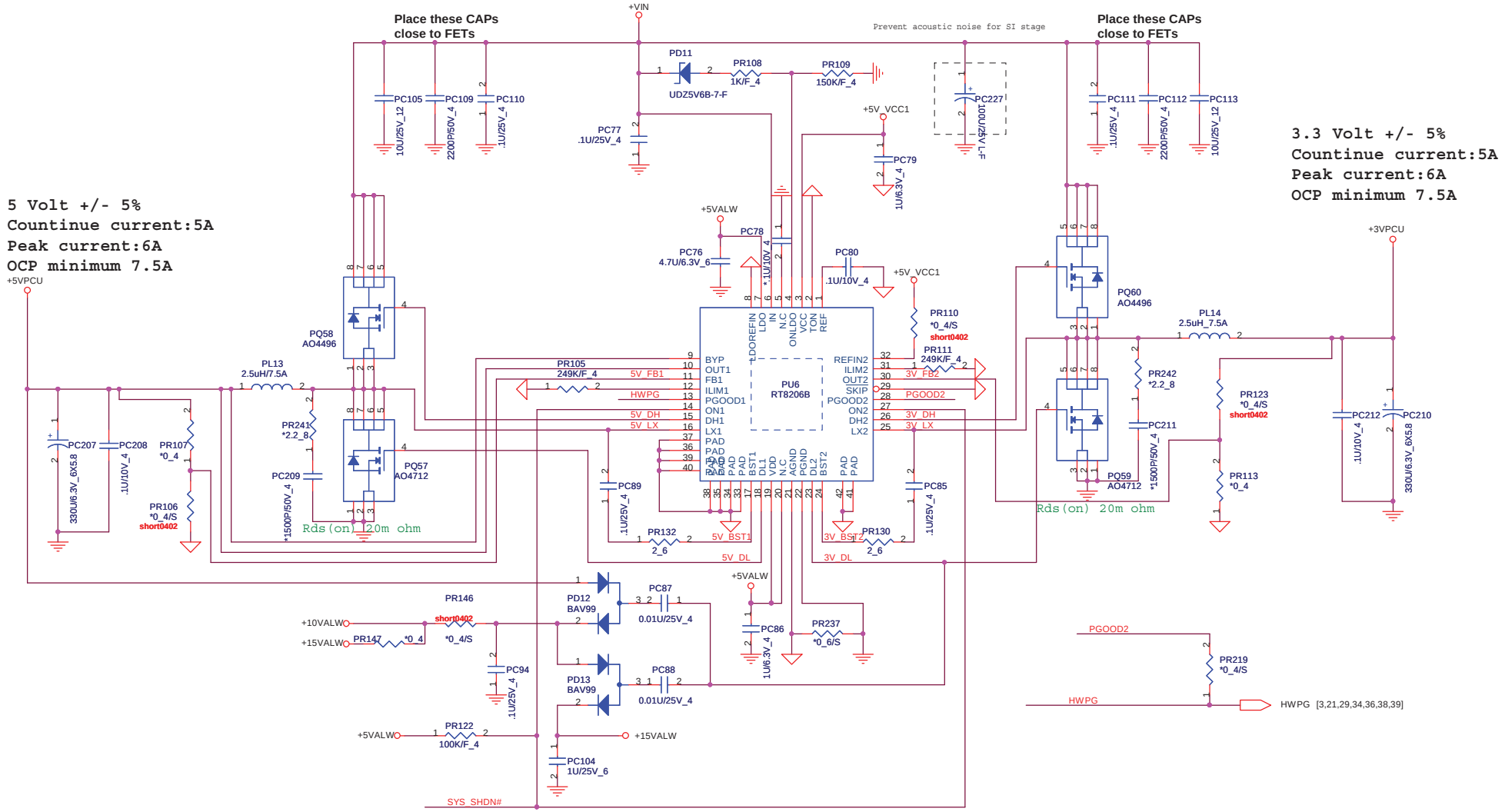
Un-mount for switchable function

NB5	**PROJECT : QL4** Quanta Computer Inc.	
Size A3	Document Number **HDMI Switch / Power CRTL**	Rev E
Date: Friday, October 09, 2009	Sheet 33 of 44	

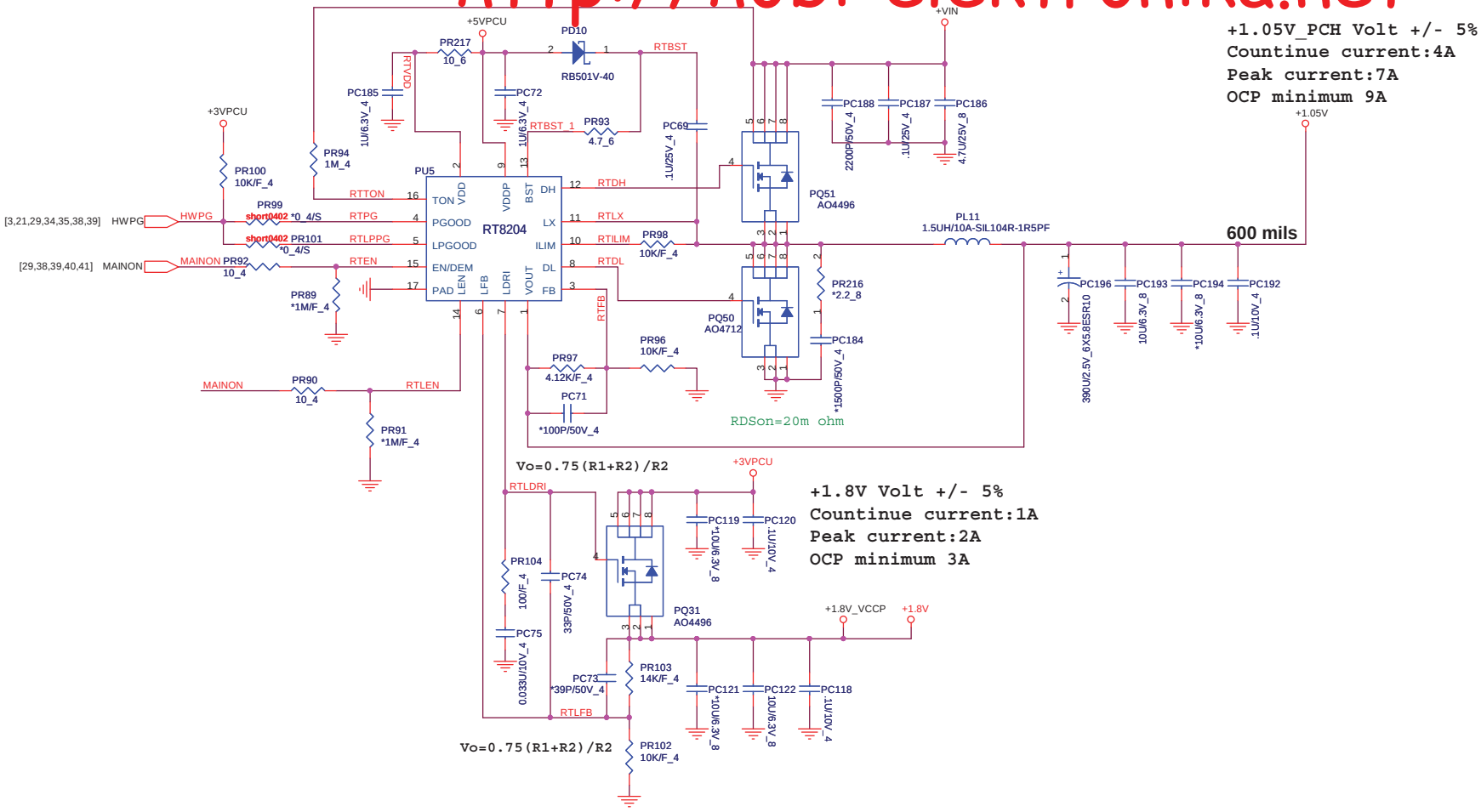


PROJECT : QL4
Quanta Computer Inc.

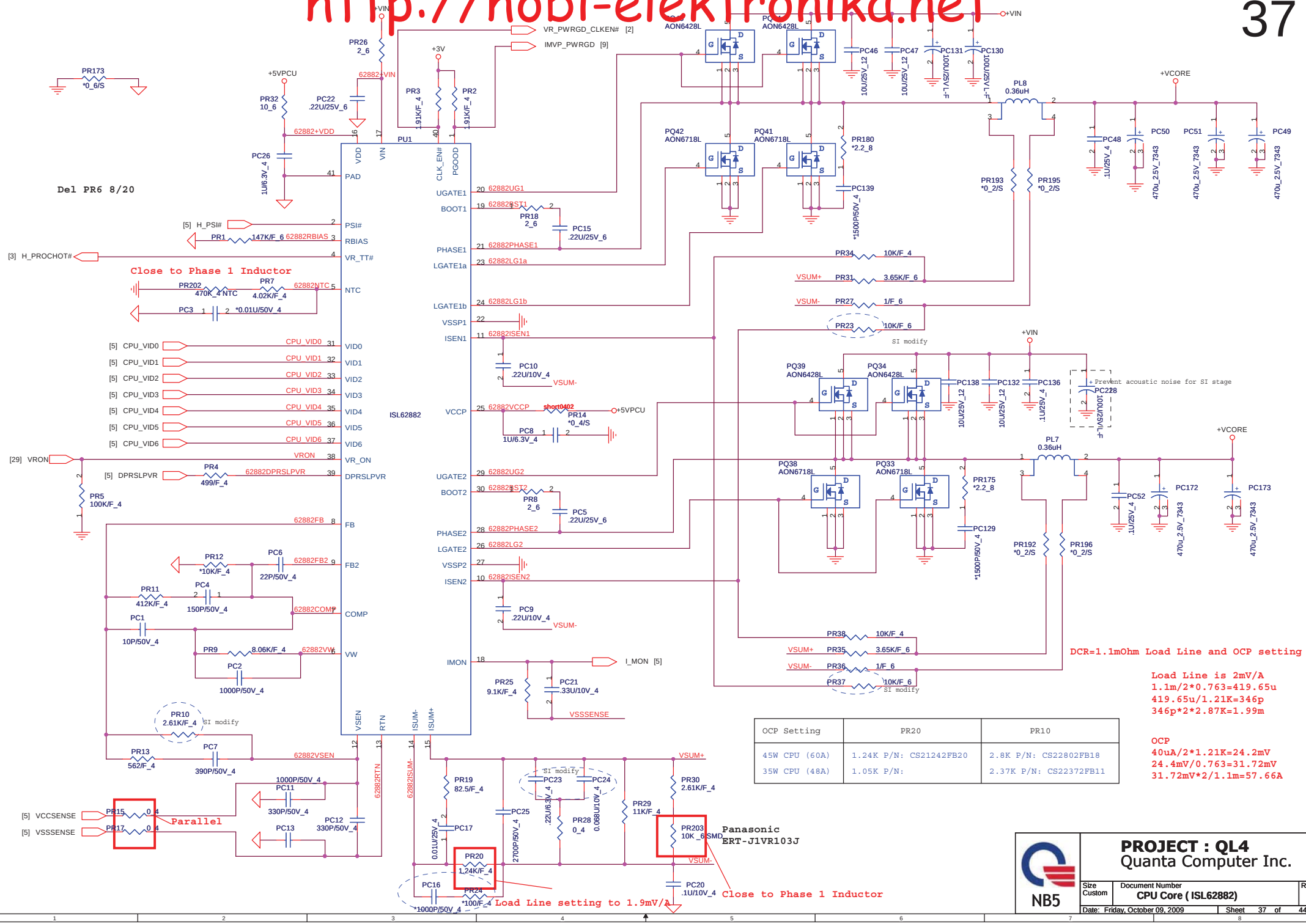
Size	Document Number	Rev
Custom	UMA GPU CORE (RT8152A)	E
NB5	Date: Friday, October 09, 2009	Sheet 34 of 44



NB5	PROJECT : QL4 Quanta Computer Inc.	
Size: Custom	Document Number: +5V/+3V (RT8206B)	Rev: E
Date: Friday, October 09, 2009	Sheet 35 of 44	



NB5	PROJECT : QL4 Quanta Computer Inc.		
	Size: Custom	Document Number: PCH +1.05V (RT8204)	Rev: E
	Date: Friday, October 09, 2009	Sheet 36 of 44	



OCP Setting	PR20	PR10
45W CPU (60A)	1.24K P/N: CS21242FB20	2.8K P/N: CS22802FB18
35W CPU (48A)	1.05K P/N:	2.37K P/N: CS22372FB11

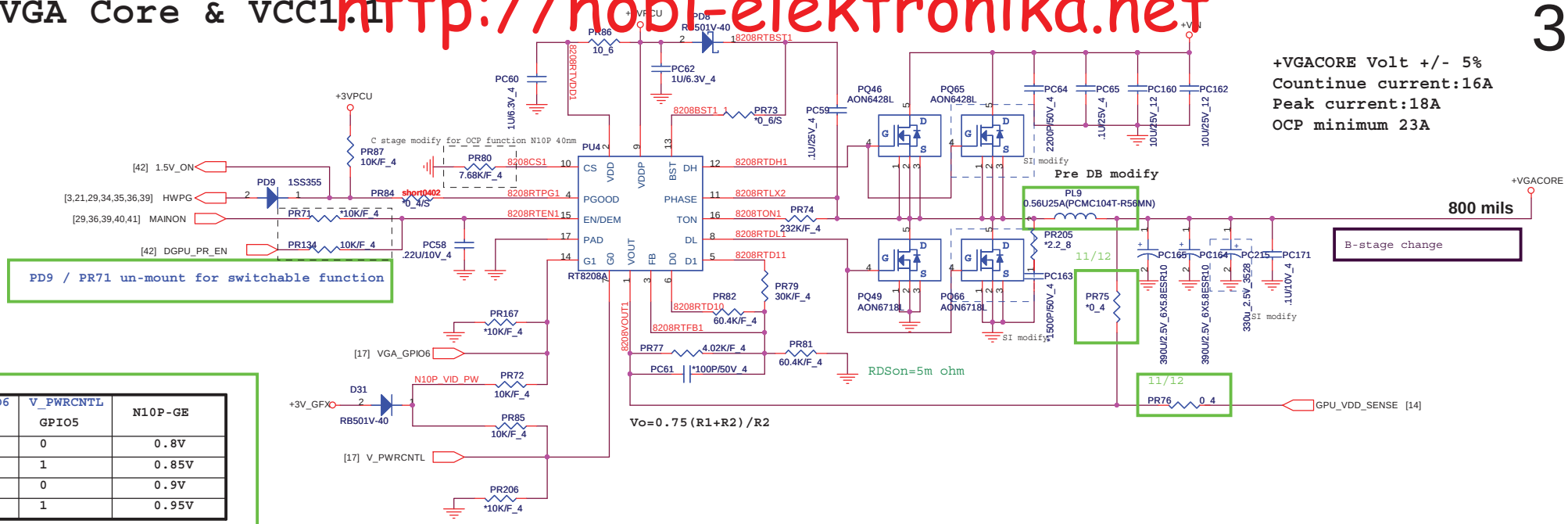
PROJECT : QL4
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	CPU Core (ISL62882)	E
Date: Friday, October 09, 2009	Sheet 37 of 44	

VGA Core & VCC1.1

+VGACORE Volt +/- 5%
Countinue current:16A
Peak current:18A
OCP minimum 23A

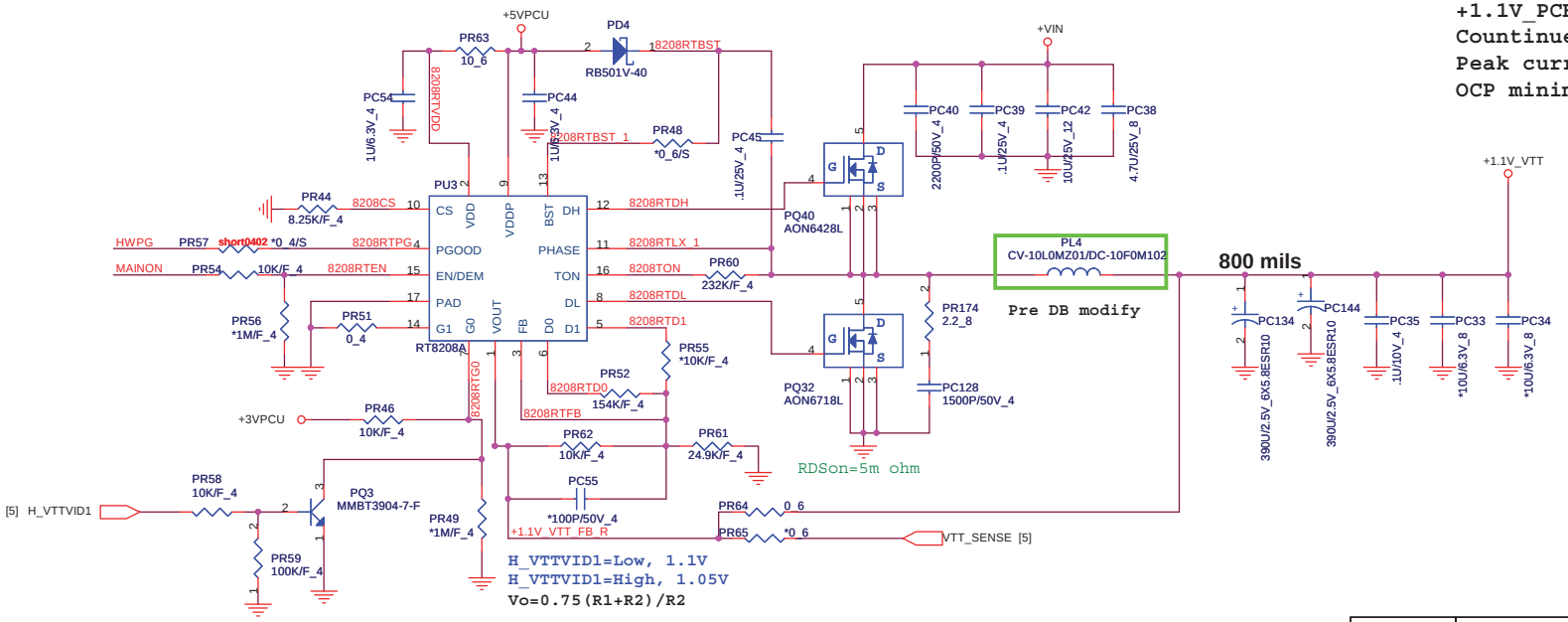


PD9 / PR71 un-mount for switchable function

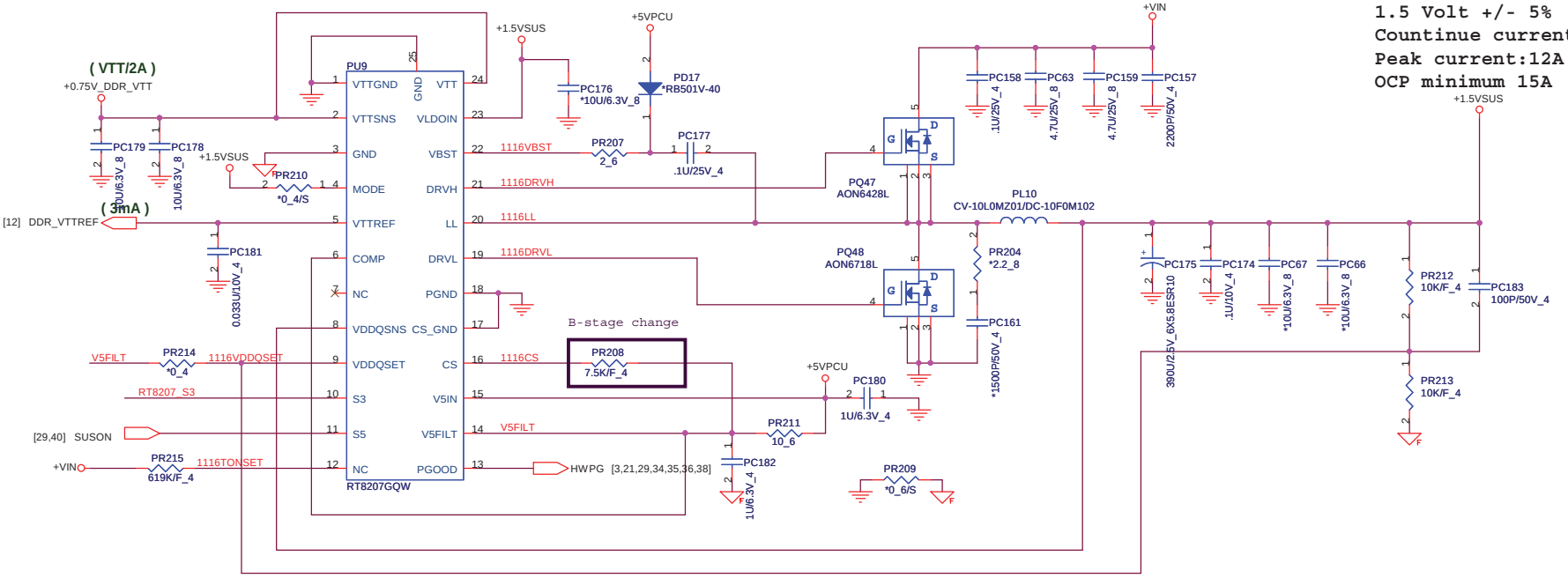
11/13

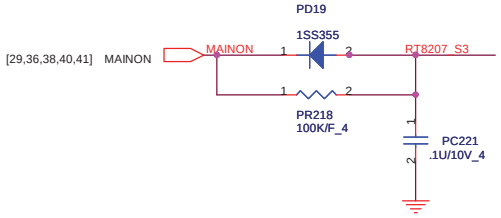
VGA_GPIO6	V_PWRCNTL	N10P-GE
GPIO6	GPIO5	
0	0	0.8V
0	1	0.85V
1	0	0.9V
1	1	0.95V

+1.1V_PCH Volt +/- 5%
Countinue current:12A
Peak current:15A
OCP minimum 18A



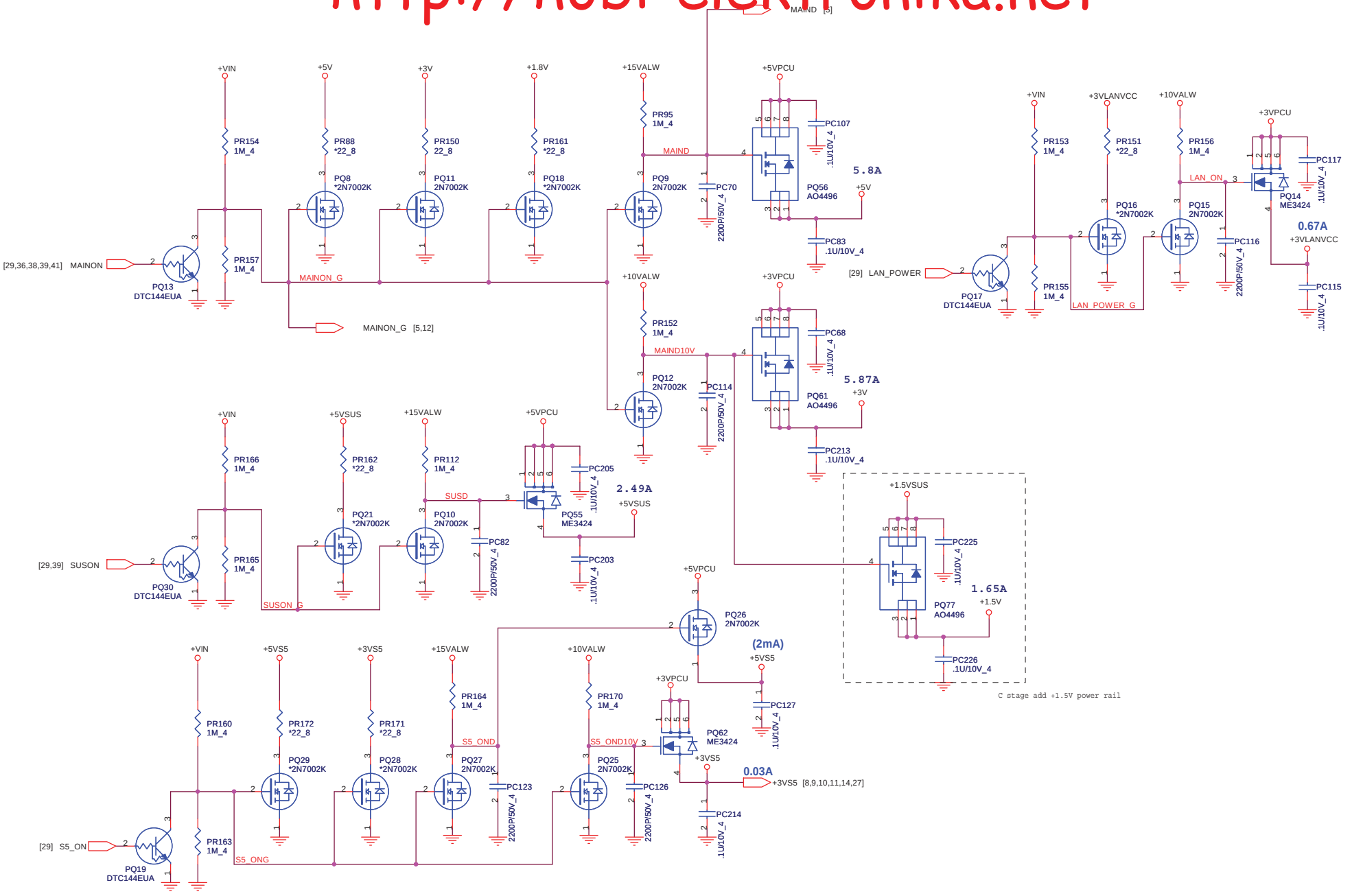
NB5	PROJECT : QL4 Quanta Computer Inc.		
	Size: Custom	Document Number: +1.1V_VTT/VGA Core RT820A	Rev: E
	Date: Friday, October 09, 2009	Sheet 38 of 44	





PROJECT : QL4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 (RT8207)	E
NB5	Date: Friday, October 09, 2009	Sheet 39 of 44



NB5	**PROJECT : QL4** Quanta Computer Inc.	
	Size: Custom Document Number: DISCHARGE/3VS5/5VS5/LAN	Rev: E
	Date: Friday, October 09, 2009	Sheet 40 of 44

PV 0616 for EMI

BATT+	C967	1	2	.1U/25V_4
+BATCHG	C968	1	2	.1U/25V_4

Place these short pad close to RSENSE

Place this ZVS close to Far-Far away +VIN

Place this ZVS close to Diode away +VIN

Power	PR187 P/N
65W/90W	CS+020AFR00
120W	CS+015AFR01

Place these CAPs close to FETs

Place this cap close to EC

Place this cap close to EC

Place this cap close to EC

Setting the Vin min to 12V For ACSET 1.26V

Setting the Vin min to 17V For EN = 1.06V

V ACLIM = VREF * (RI // 152K) / (Rhi // 152K + Rlow// 152K) Input curretn = 2.9A (71.5K , 10K) (0.05/Vref * Vaclim + 0.05) / Rsense

Charging Curret setting = I chg = 165mV / Rsense * (Vchlim / 3.3V)

CELL_SLT = 1 -- 3 S (Cells = GND 3S)
CELL_SLT = 0 -- 4 S (Cells = VDD 4S)

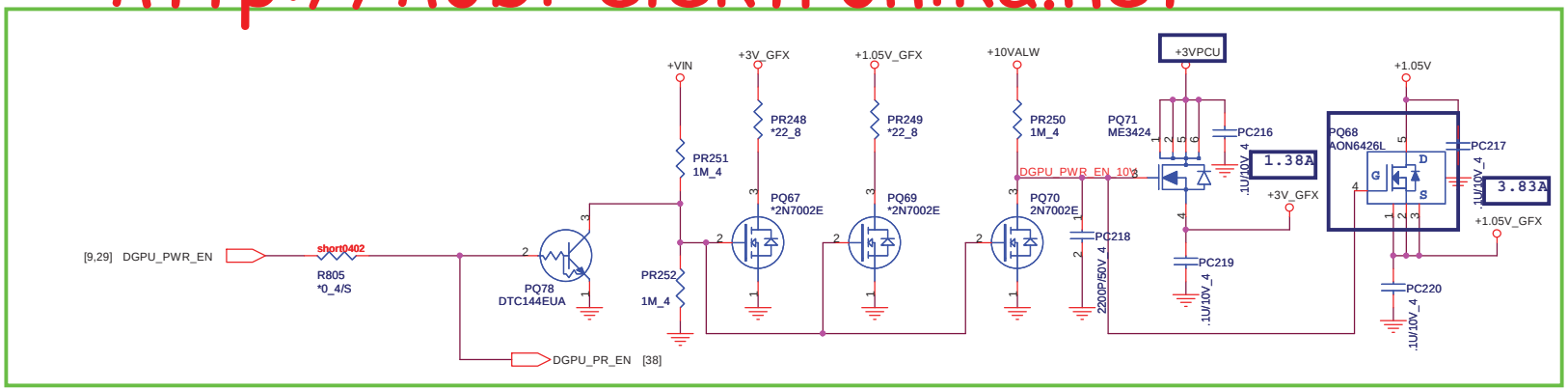
Input Current monitor V icm = 19.9 * (Vcsip - Vcsin)

Size	Mounted	N/A
16"	PR185	PR184, PR186, PQ59
17.3"	PR184, PR186, PQ59	PR185

NB5

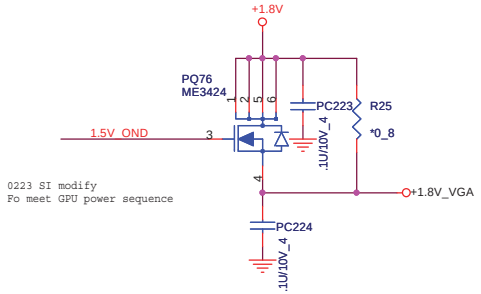
PROJECT : QL4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Charger (ISL6251)	E
Date: Friday, October 09, 2009	Sheet 41 of 44	

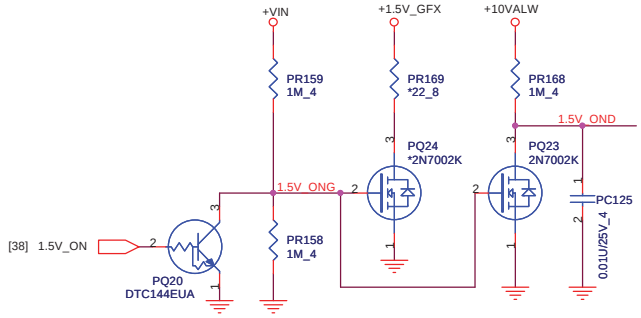


For Discrete or switchable Only

+1.8 Volt +/- 0.1V
Countinue current:0.3A
Peak current:1A

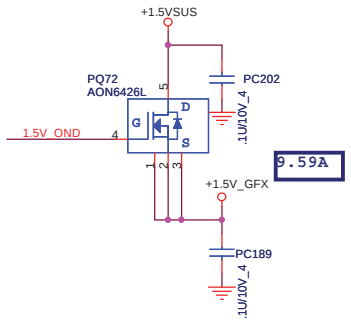


For Discrete or switchable Only



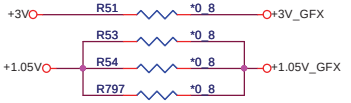
Change PC119 to 0.01u/25v as Discrete power sequence

For Discrete or switchable Only



R51 co-lay PQ71
R53/R54 co-lay PQ68

For Discrete Only



SEL	FUNCTION
LOW	DGPU
HIGH	IGPU

For Hybrid DGPU Power Rails Sequence
1. +3V_GFX, +1.05V_GFX
2. +VGA_CORE -> DGPU_PG
3. 1.5V_GFX, +1.8V_GFX

PROJECT : QL4
Quanta Computer Inc.

NB5

Size	Document Number	Rev
A3	Switchable Power	E
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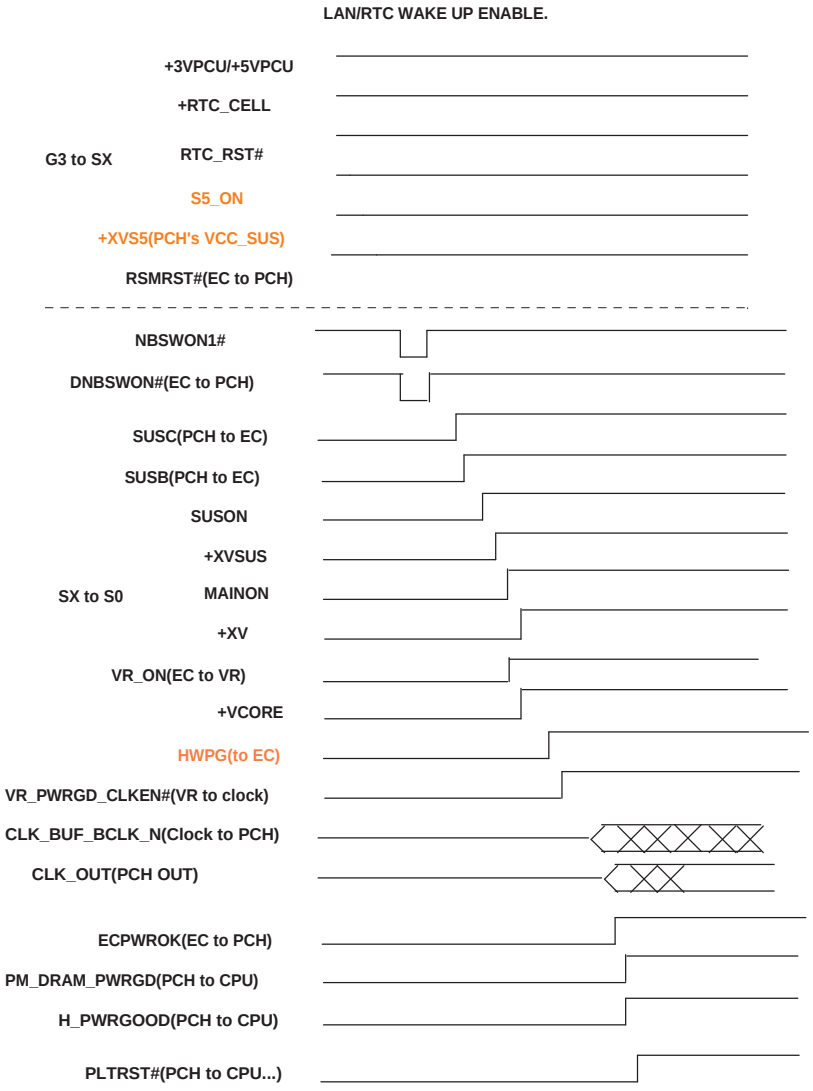
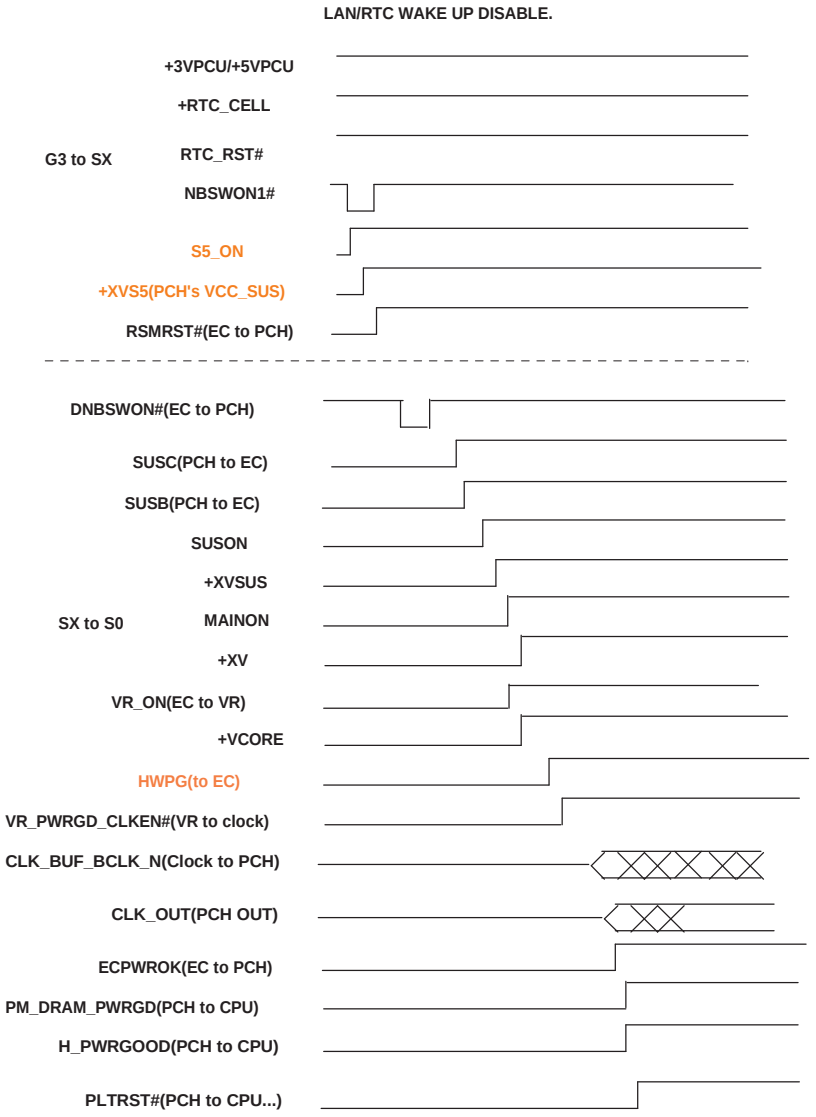
Power up sequence





NB5	PROJECT : QL4 Quanta Computer Inc.	
Size: Custom	Document Number: Power up sequence	Rev: E
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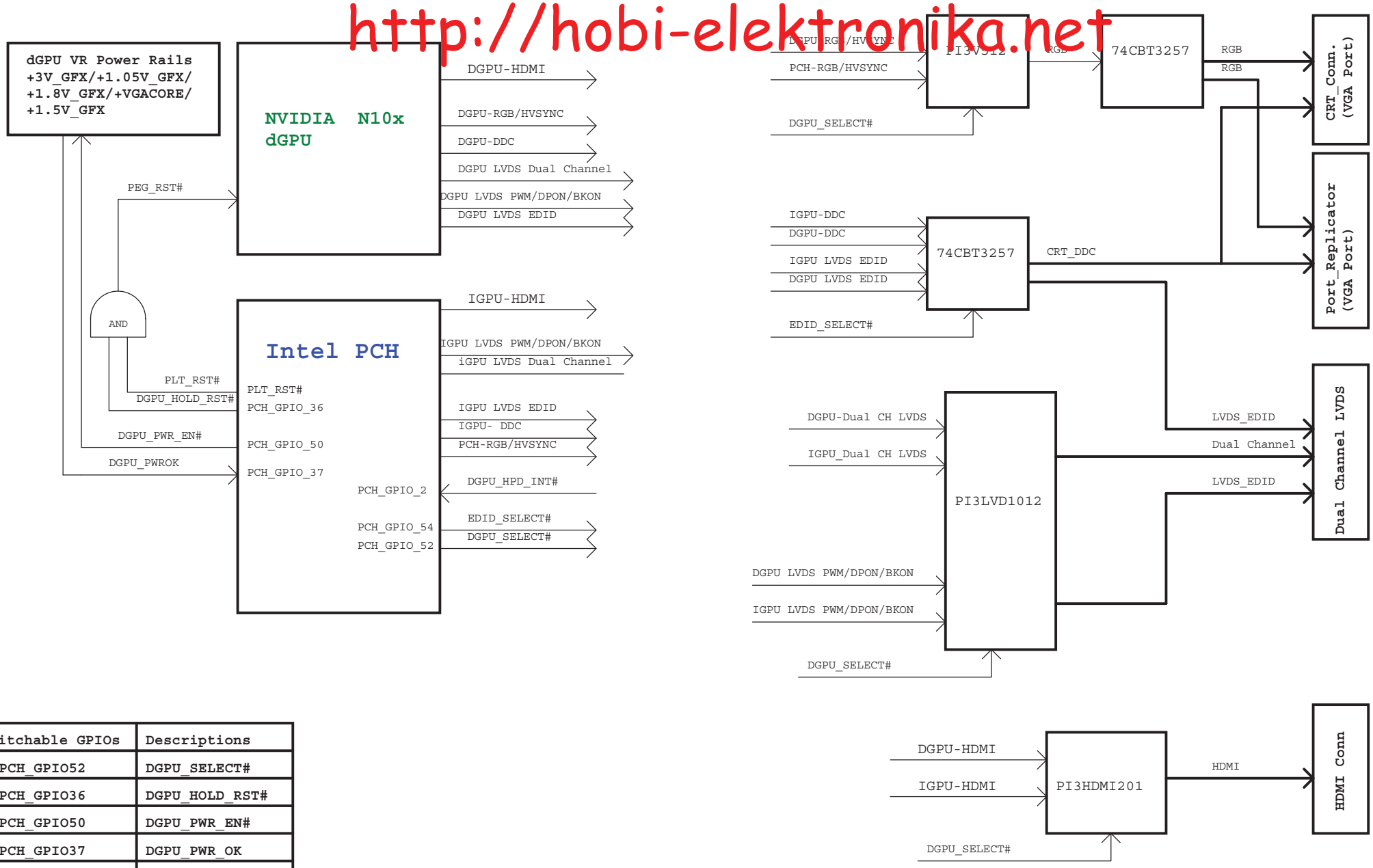

Switchable GPIOs	Descriptions
PCH_GPIO52	DGPU_SELECT#
PCH_GPIO36	DGPU_HOLD_RST#
PCH_GPIO50	DGPU_PWR_EN#
PCH_GPIO37	DGPU_PWR_OK
PCH_GPIO54	EDID_ELECT#

NB5

PROJECT : QL4
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Size	Document Number	Rev
Custom	Switch Blockdiagram	E

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