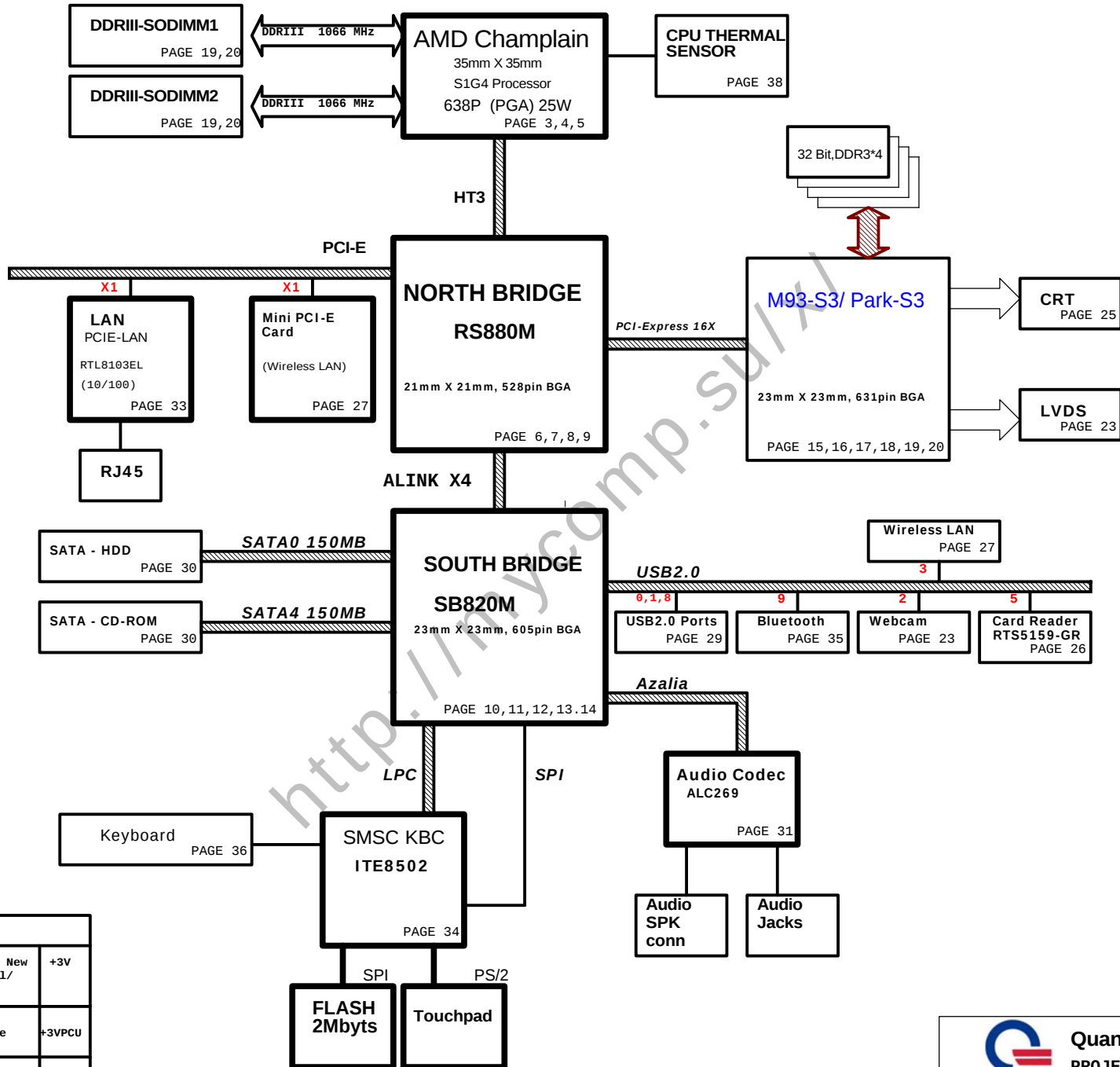


FK1 SYSTEM DIAGRAM

01

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT



SYSTEM CHARGER(bq24740)
PAGE 44, 45

3/5V5 RT8206B
PAGE 43

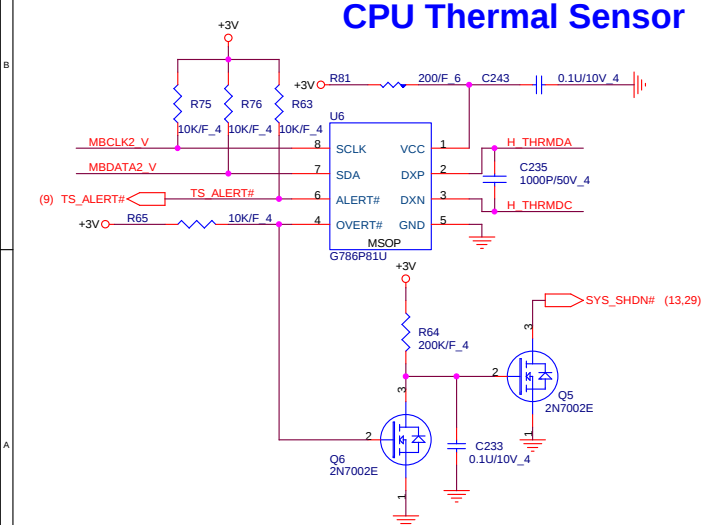
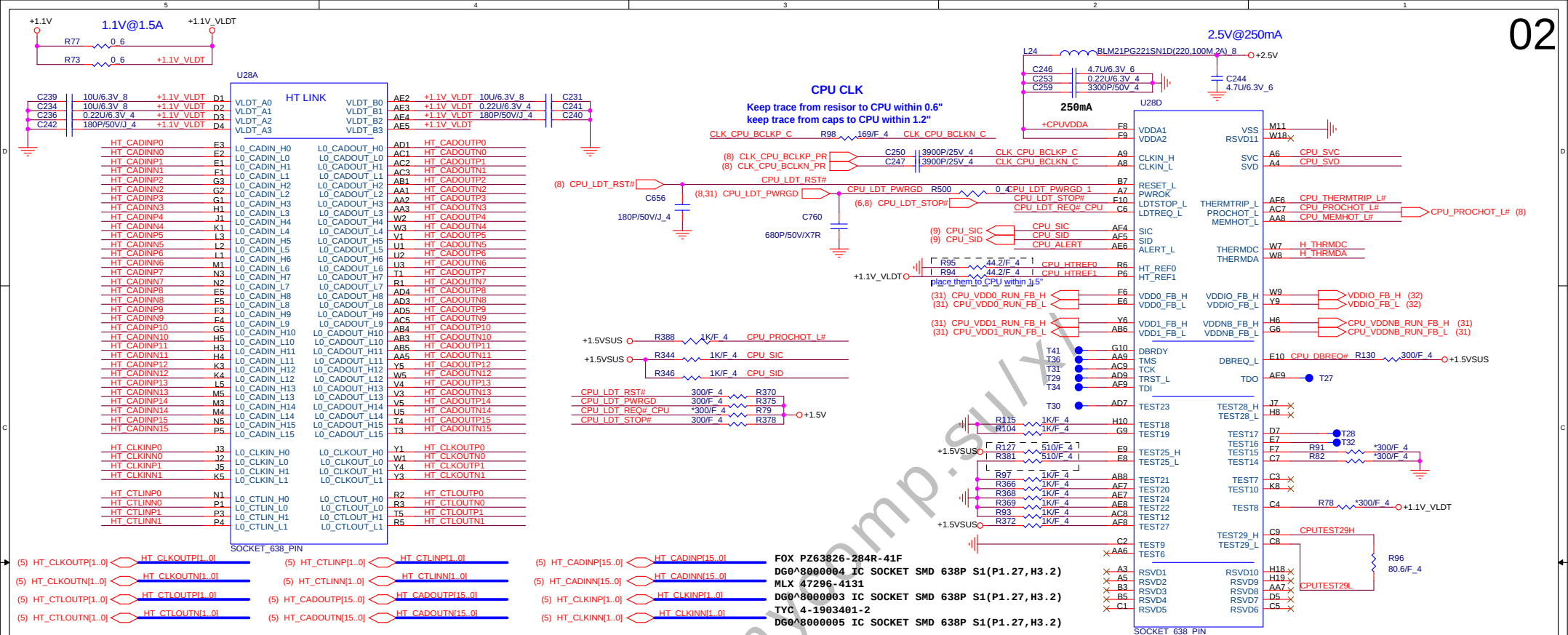
+1.1V(RT8029)/+1.1VS5/+1.8V
PAGE 41

DDR3 (RT8207)/+1.0V_VGA
PAGE 42

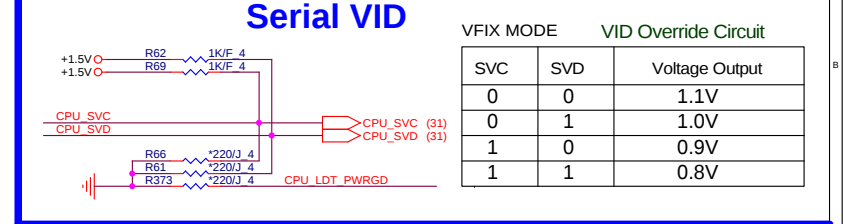
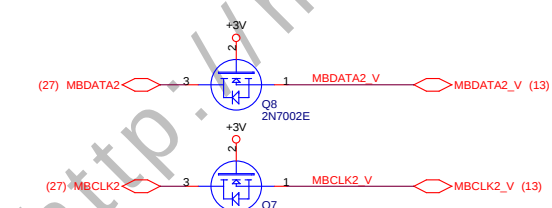
VGACORE(1.1V~0.9V)RT8028A
PAGE 40

CPU_CORE ISL6265
PAGE 39

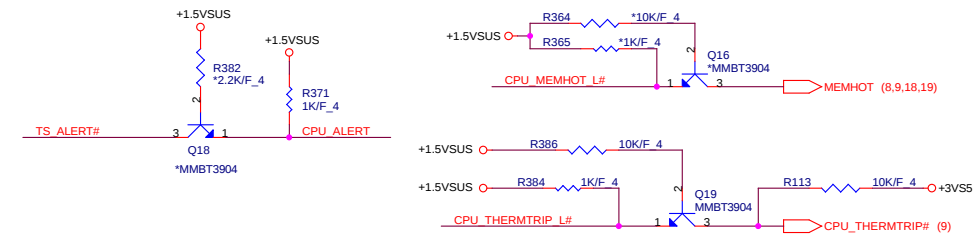
SMBUS TABLE		
SB--SCL0/SD0	Clock gen/ wireless LAN/ New card/ DDR3/ DDR3 thermal/ Accelerometer/system thermal	+3V
EC -- AB1A	Battery charge/discharge	+3VPCU
EC -- AB2A	VGA thermal	+3V



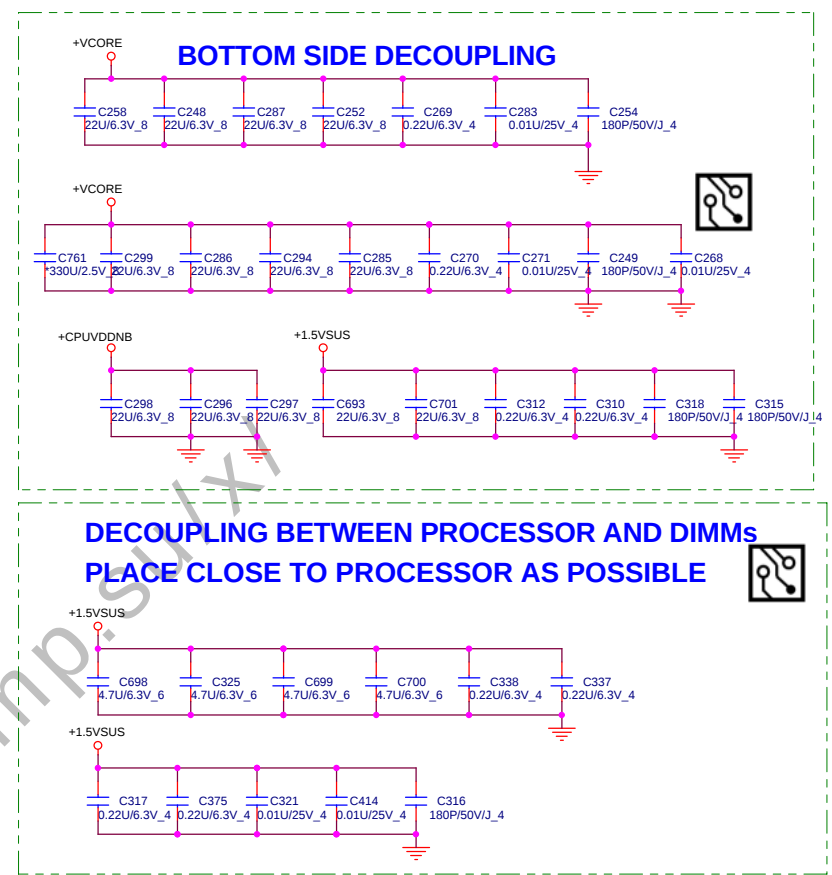
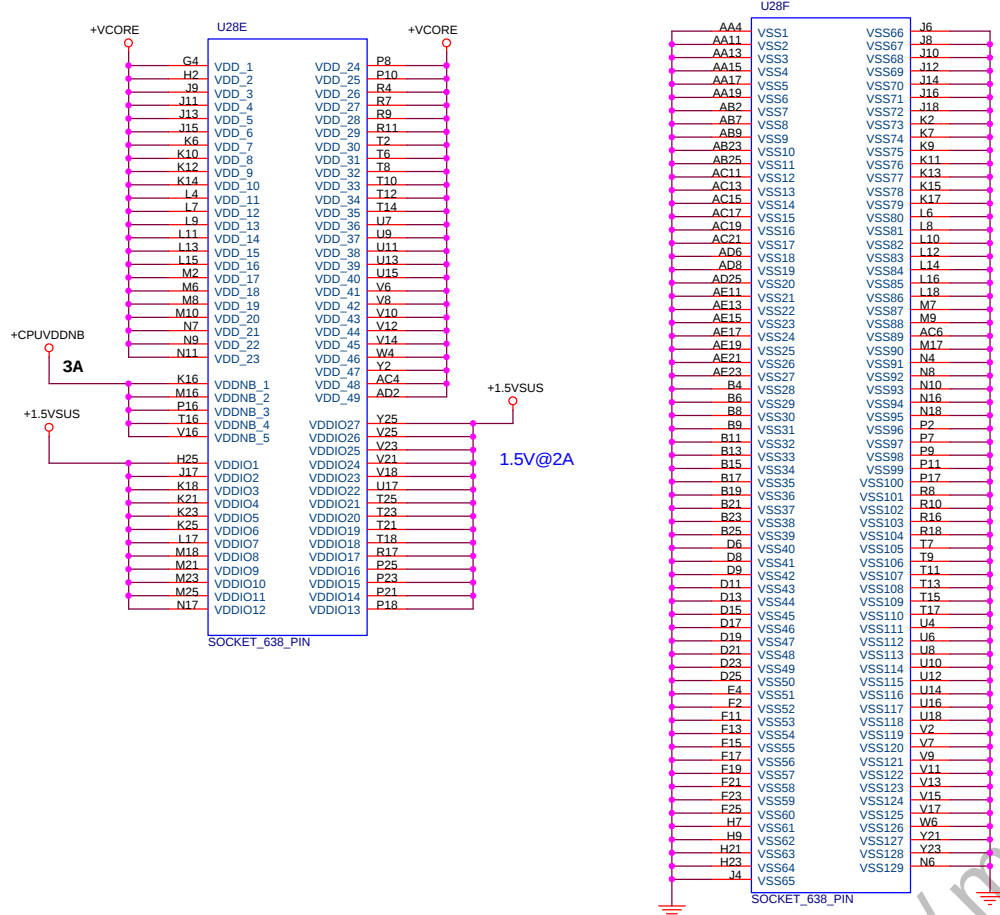
MBCLK2/MBDATA2	
G786P81U	1001 100X
G781-1P8	1001 101X



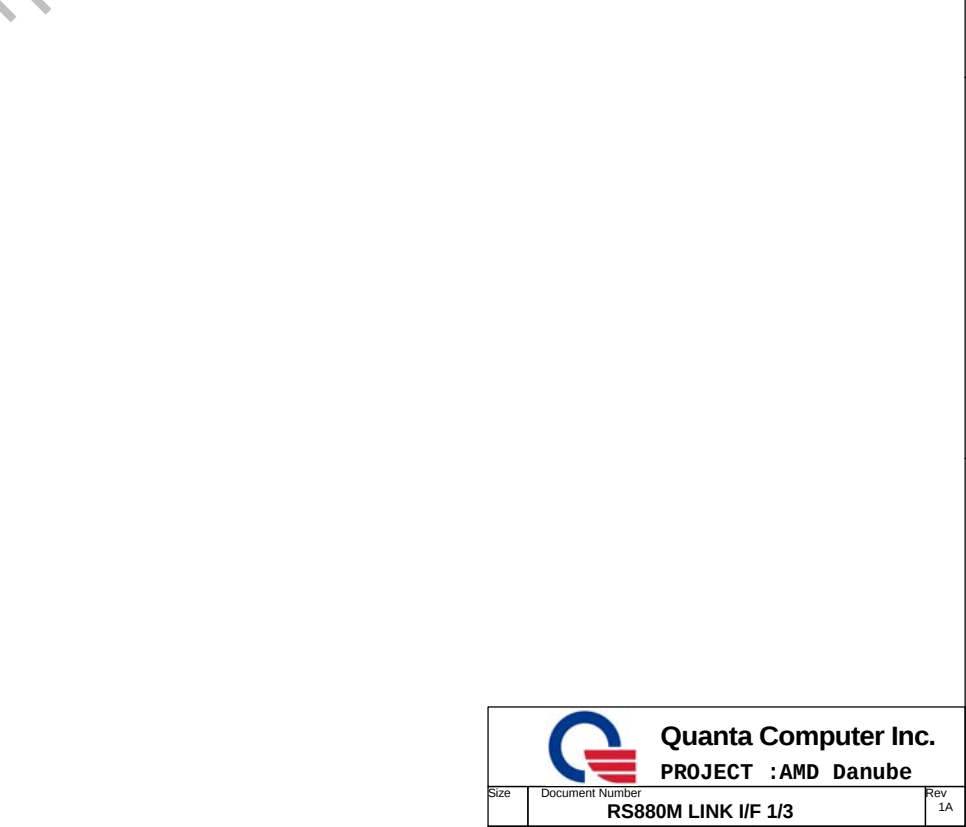
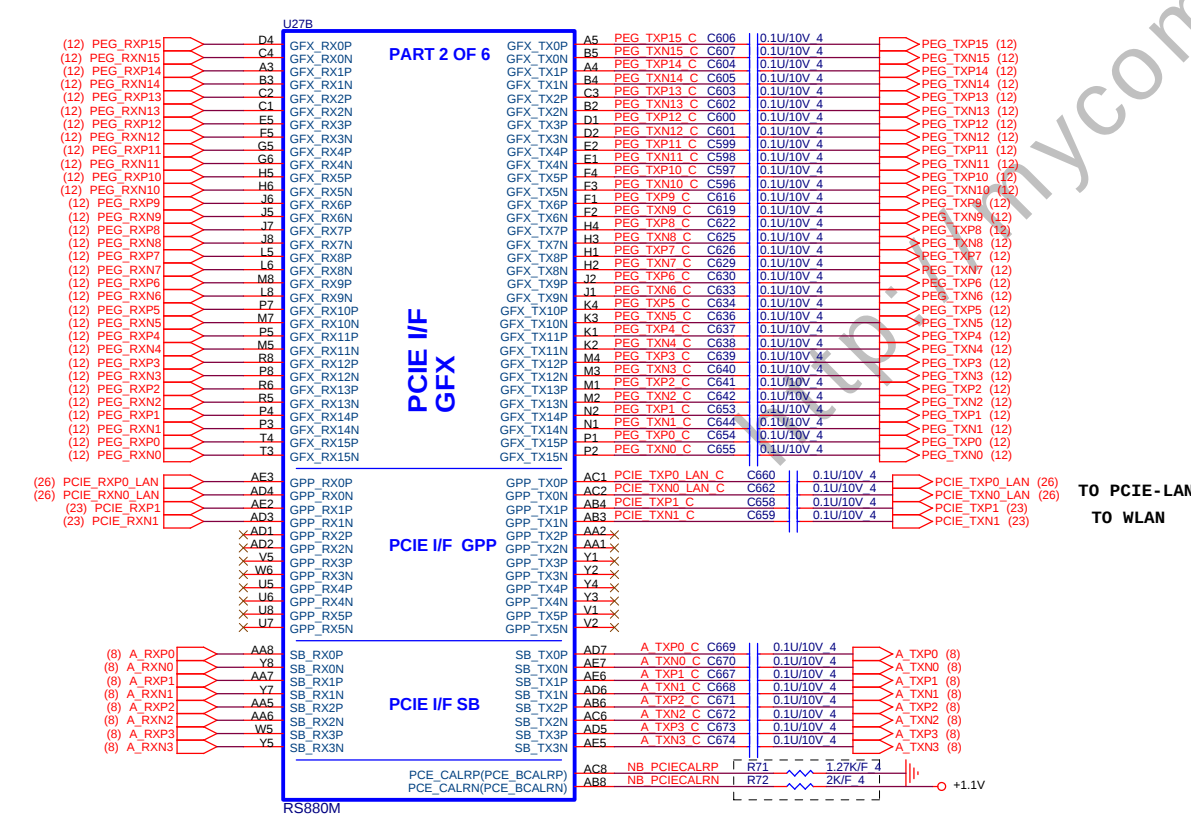
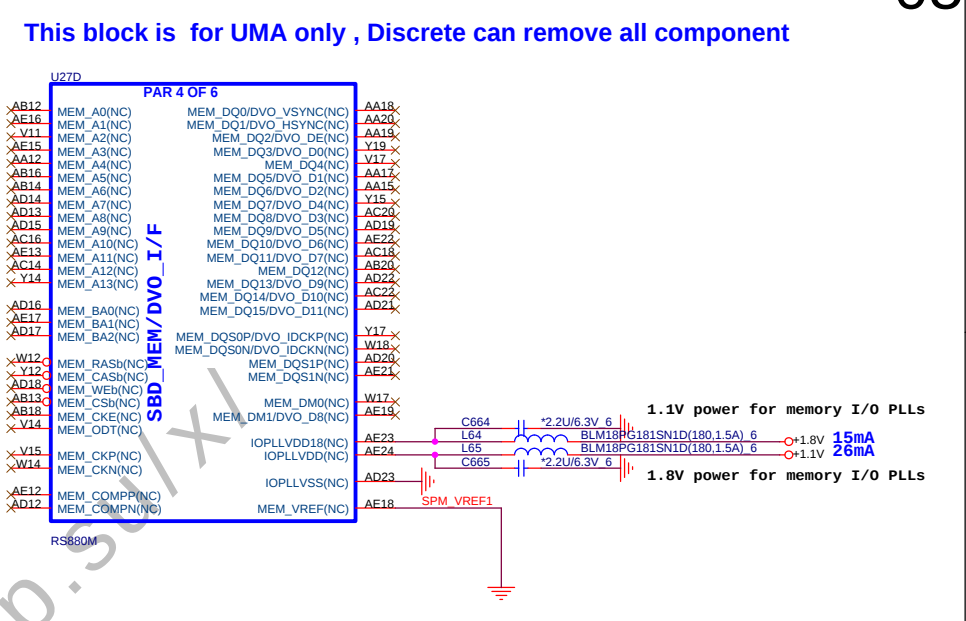
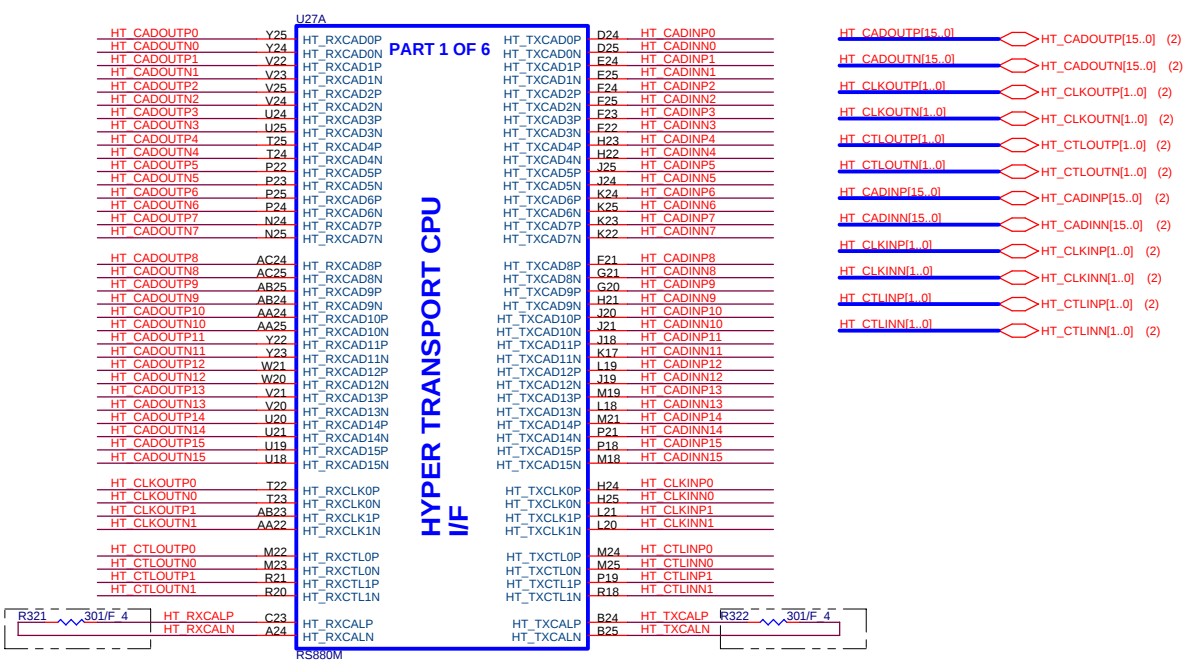
SVC	SVD	Voltage Output
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

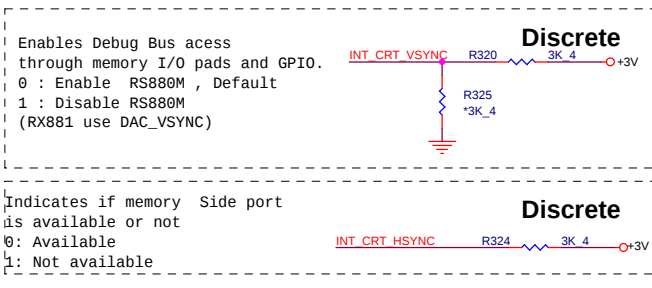


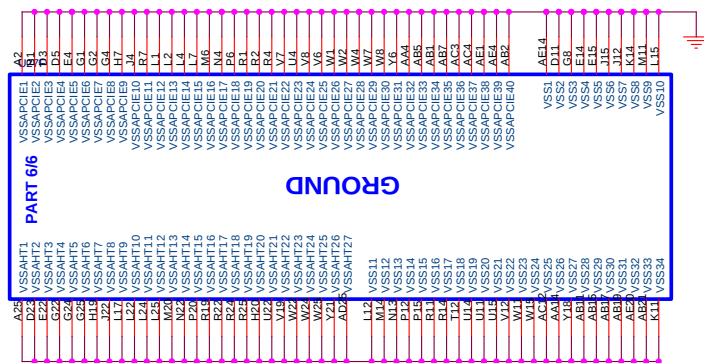




PROCESSOR POWER AND GROUND

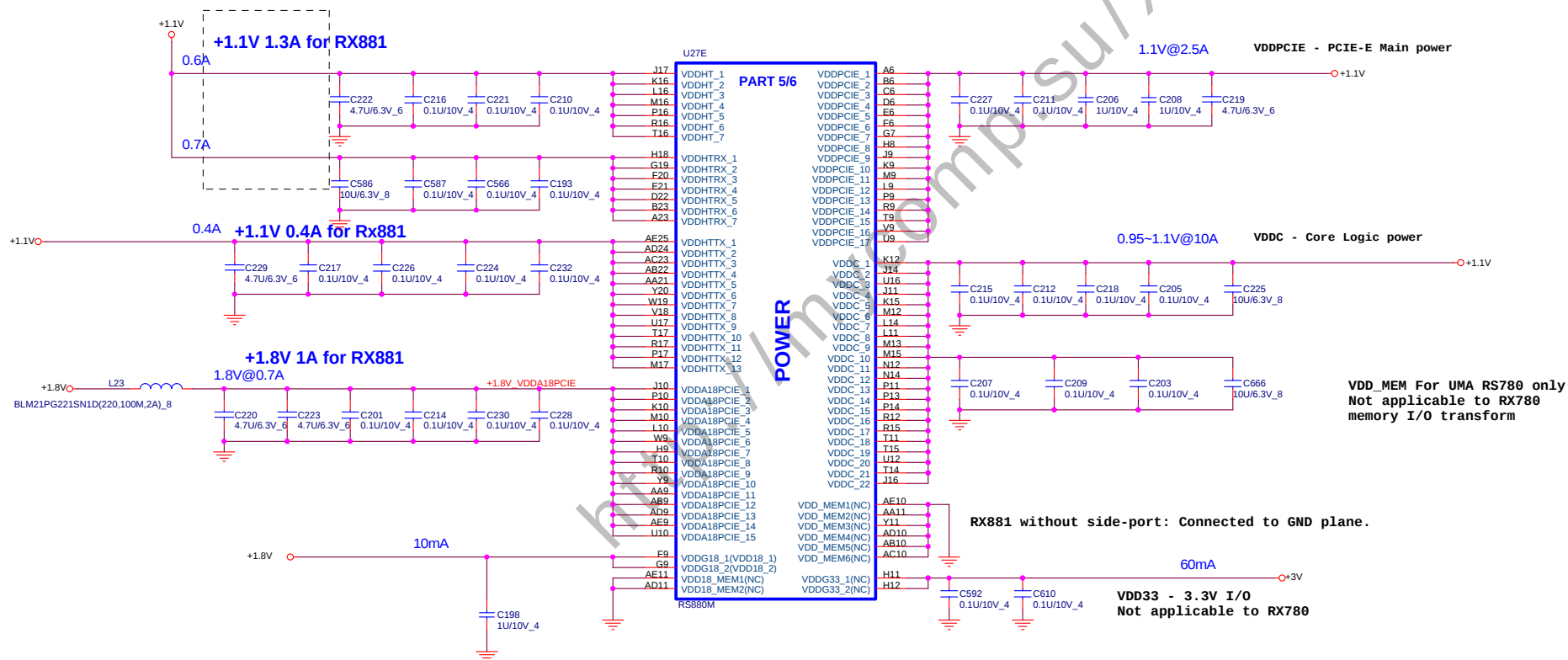






RX881/RS880 POWER DIFFERENCE TABLE

PIN NAME	RX881	RS880	PIN NAME	RX881	RS880
VDDHT	+1.1V	+1.1V	IOPLLVD	+1.1V	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	GND	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDI	GND	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	GND	+1.8V
VDDG18	+1.8V	+1.8V	PLLVD	GND	+1.1V
VDD18_MEM	GND	+1.8V	PLLVD18	GND	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	GND	+1.8V/1.5V	VDDLTP18	GND	+1.8V
VDDG33	+3.3V	+3.3V	VDDLTP18	GND	+1.8V
IOPLLVD18	+1.8V	+1.8V	VDDLTP33	NC	NC

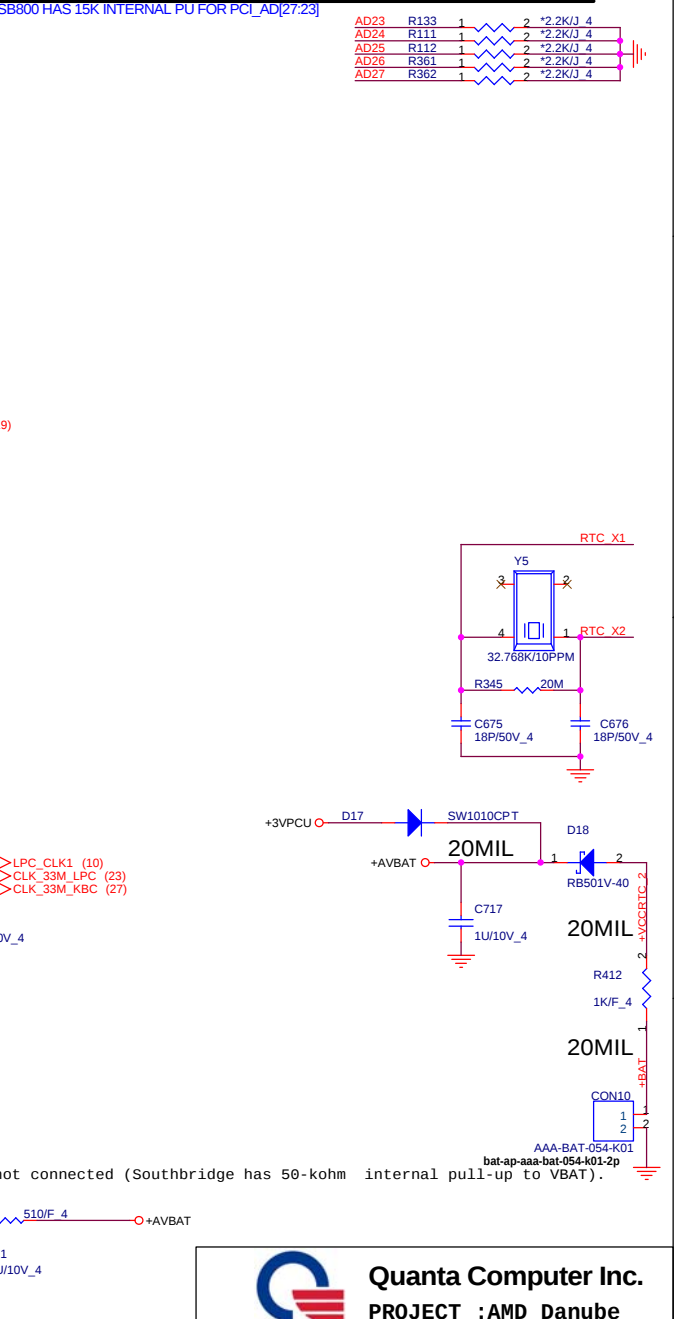
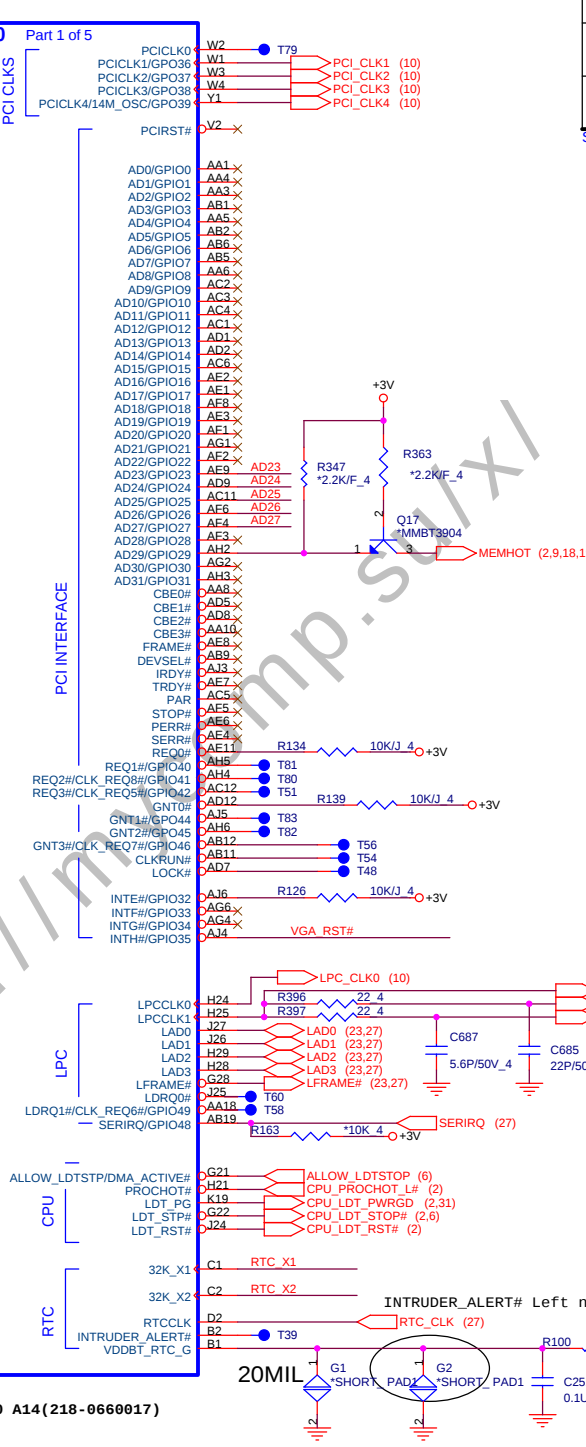
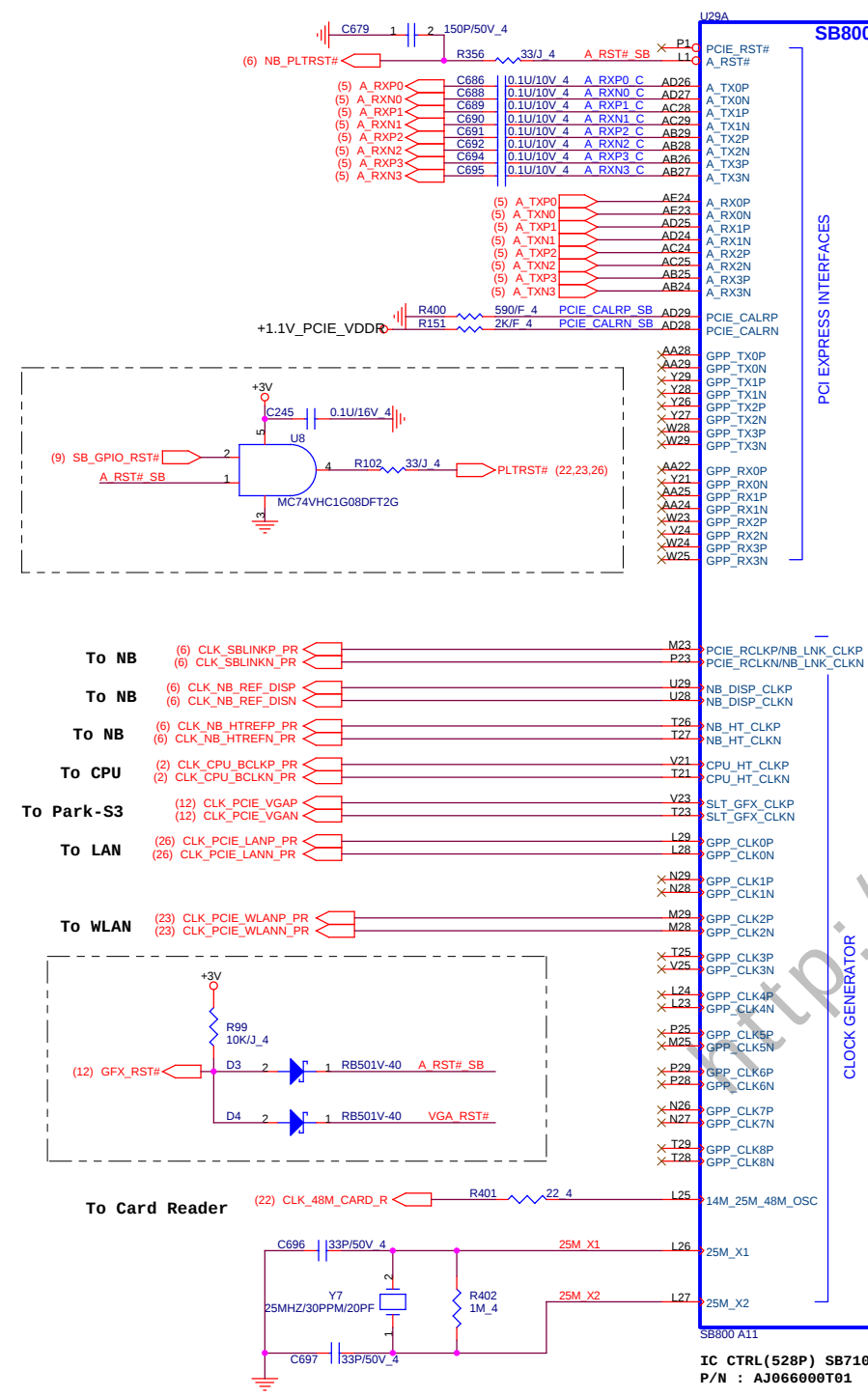


Quanta Computer Inc.
PROJECT :AMD Danube

Size: Document Number: **RS880M-POWER5 3/3** Rev: 1A
Date: Wednesday, March 24, 2010 Sheet: 7 of 37

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL	DISABLE ILA AUTORUN	USE FC PLL	USE DEFAULT PCIE STRAPS	DISABLE PCI MEM BOOT
PULL LOW	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT
	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



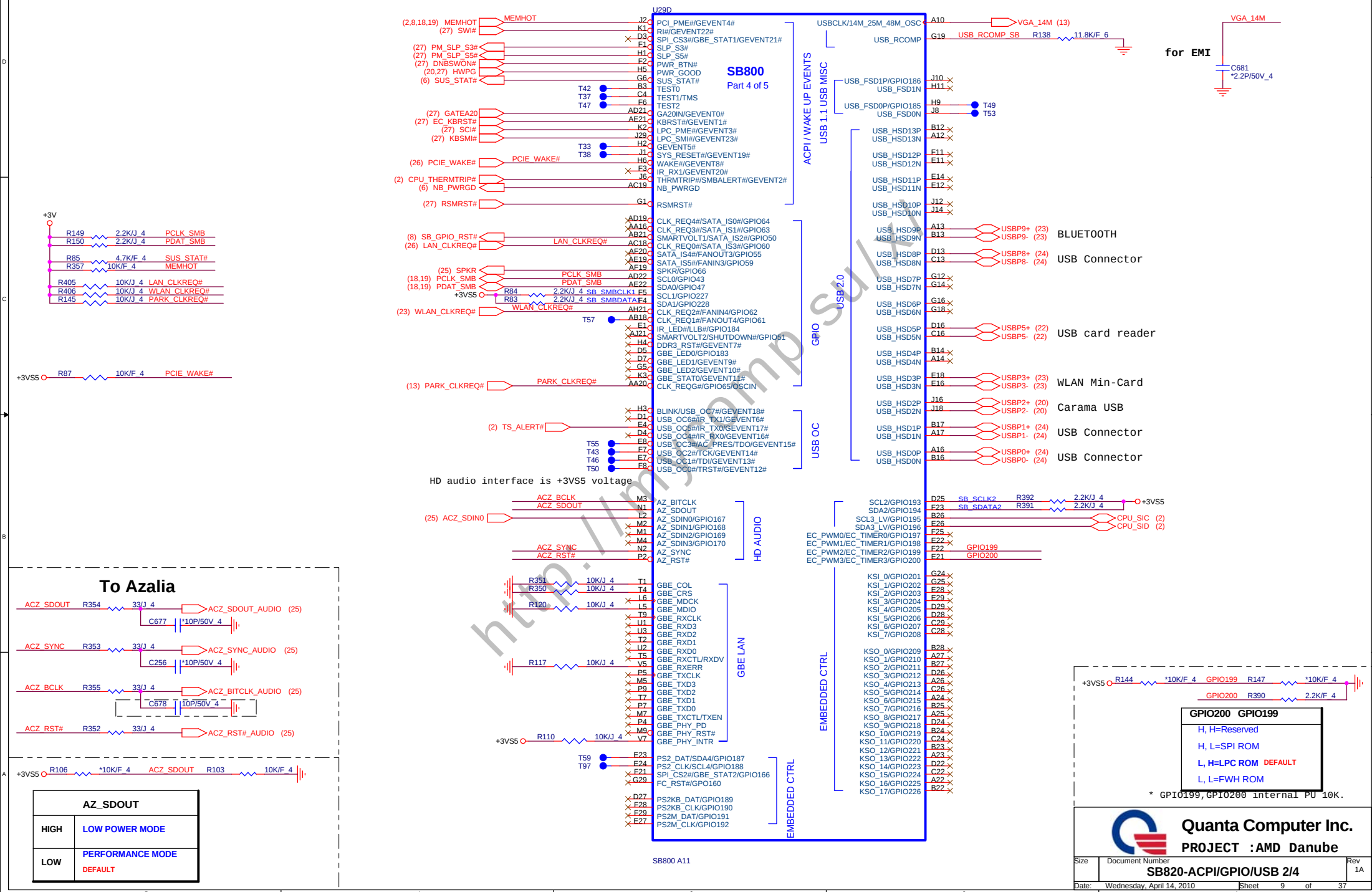


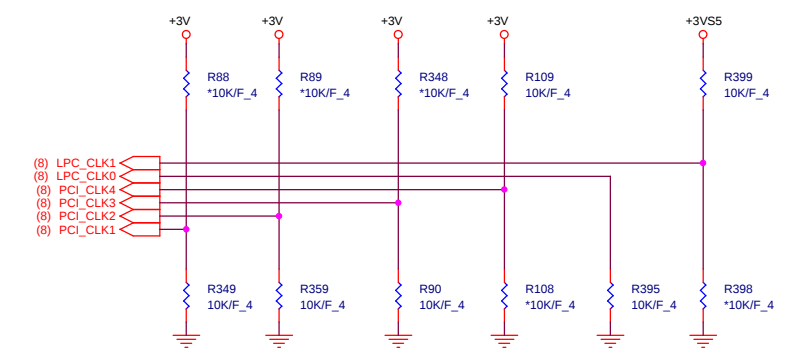
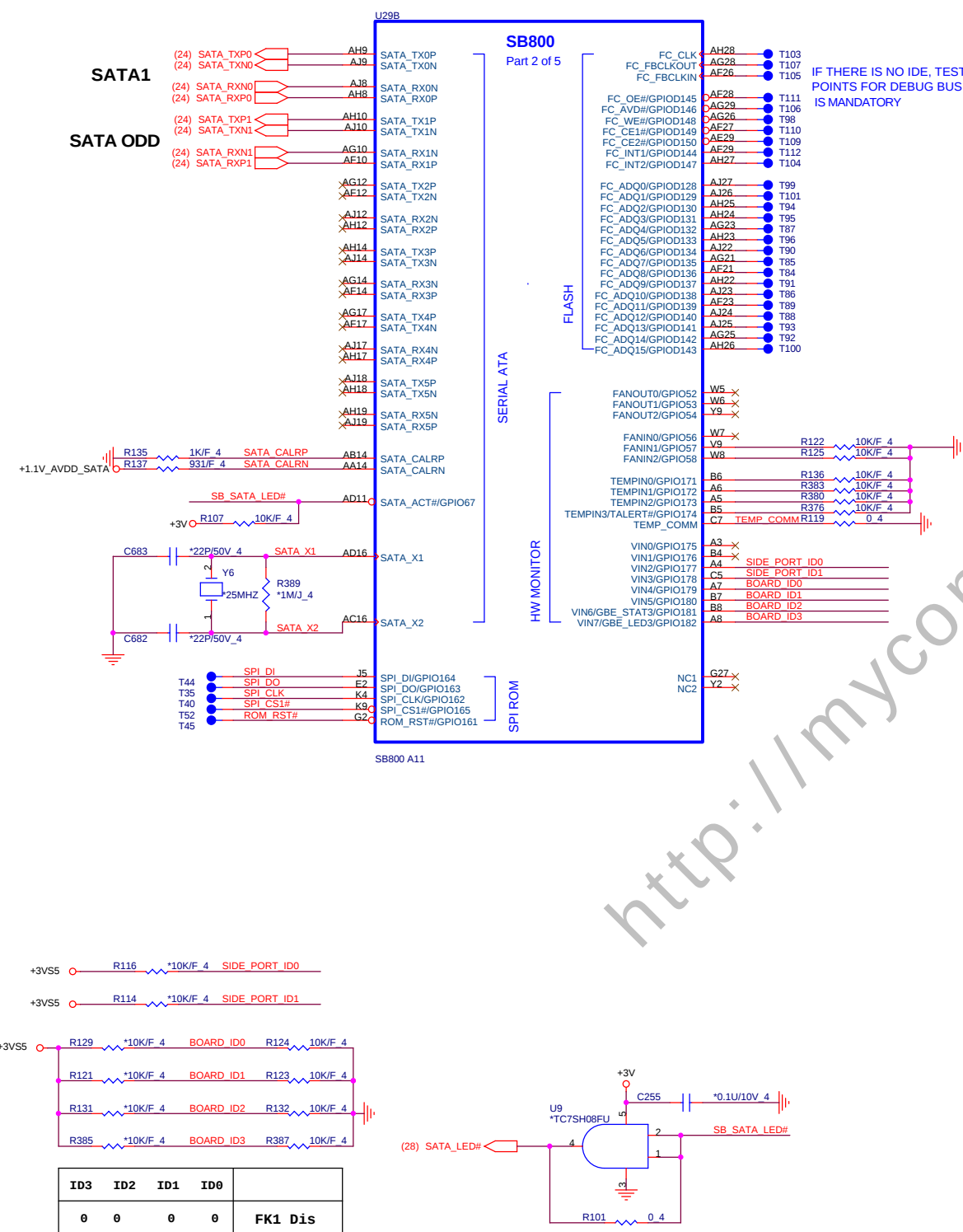
Quanta Computer Inc.
PROJECT :AMD Danube

Size	Document Number	Rev
	SB820-PCIE/PCI/CPU/LPC 1/4	1A
Date:	Monday, April 19, 2010	Sheet 8 of 37

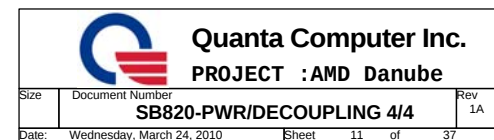
IC CTRL(528P) SB710 A14(218-0660017)
P/N : AJ066000T01

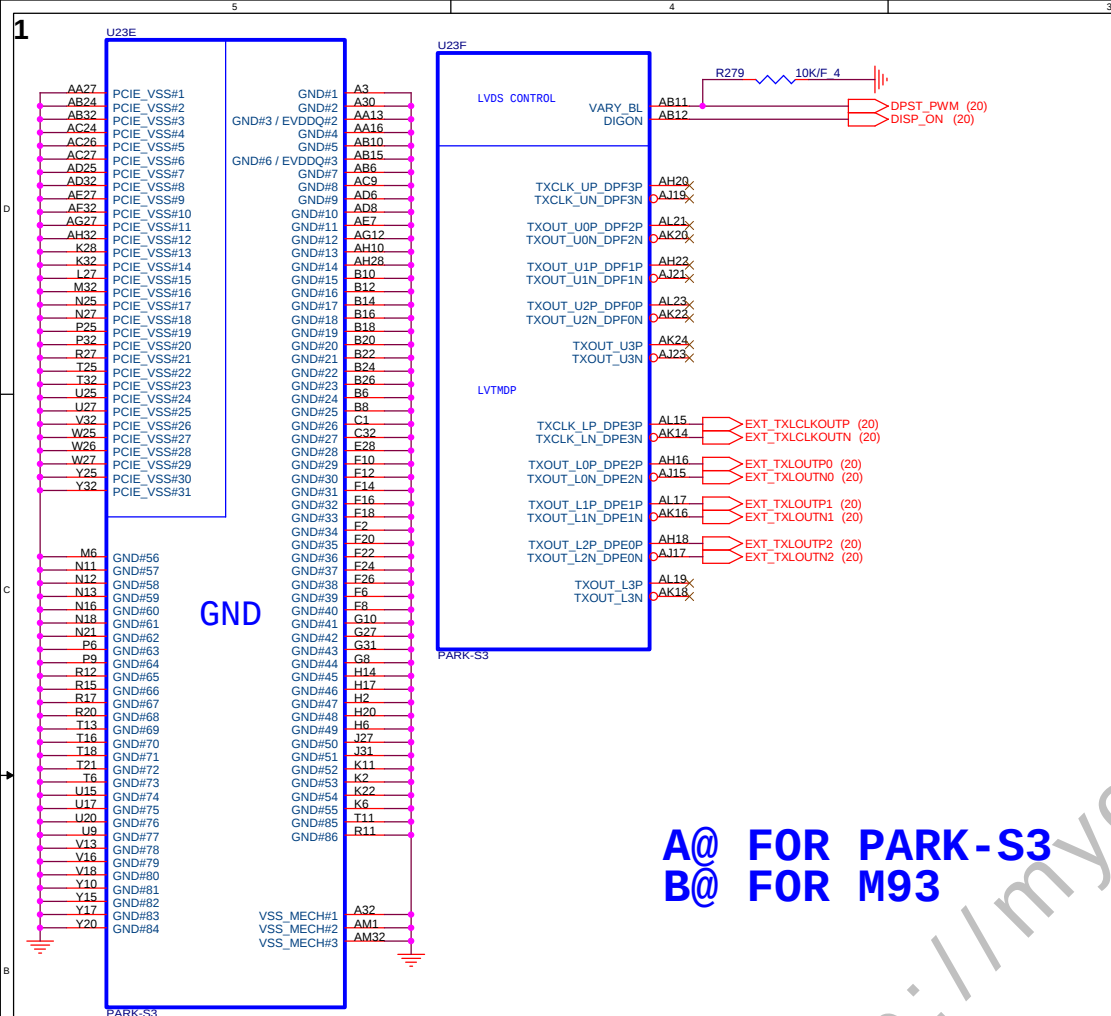
0412 add G2 for RTC clean





	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1
PULL HIGH	ALLOW PCIE Gen2	Watchdog Timer Enable	USE DEBUG STRAPS	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT
PULL LOW	FORCE PCIE Gen1 DEFAULT	Watchdog Timer Disable DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED



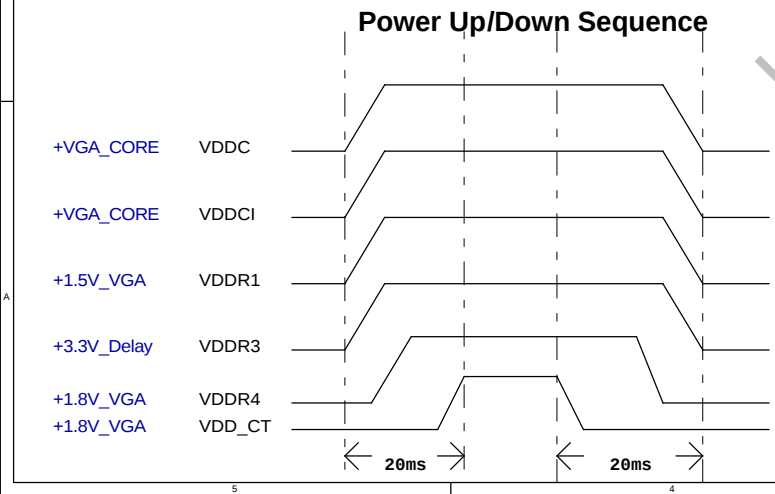


14

CONFIGURATION STRAPS			RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET			
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

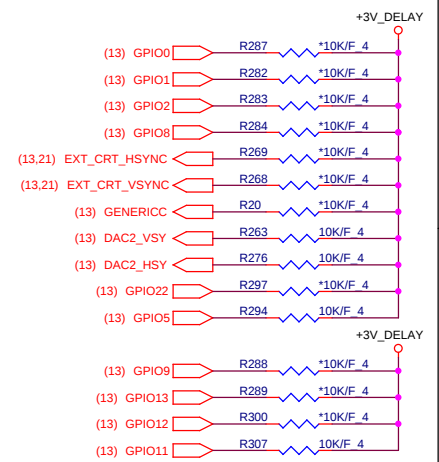
AMD RESERVED CONFIGURATION STRAPS	
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET	
H2SYNC	GENERICC
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET	
GPIO21_BB_EN	

A@ FOR PARK-S3
B@ FOR M93



Memory Aperture size				
GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	512M	0	0	1

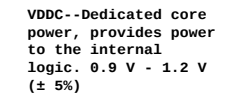
Memory Aperture Size 512MB and 256MB GPIO setting is the same
It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.



NBS/RD2

PROJECT : AX2 / 7
Quanta Computer Inc.

Size Custom	Document Number PARK_GND / LVDS/ Straps	Rev 1A
Date: Tuesday, April 20, 2010	Sheet 14 of 37	



PCIE_VDDC--PCI-E
Digital Power
Supply (Either 1.0
V or 1.1 V) 1.0 V
-5% to 1.1 V +5%

A@ FOR PARK-S3
B@ FOR M93

(17) VMA_WDQS[7..0] $\Rightarrow$ VMA_WDQS[7..0]
 (17) VMA_RDQS[7..0] $\Rightarrow$ VMA_RDQS[7..0]
 (17) VMA_DM[7..0] $\Rightarrow$ VMA_DM[7..0]
 (17) VMA_DQ[63..0] $\Rightarrow$ VMA_DQ[63..0]
 (17) VMA_MA[13..0] $\Rightarrow$ VMA_MA[13..0]

VMA_DQ0 K27
 VMA_DQ1 J29
 VMA_DQ2 H30
 VMA_DQ3 H32
 VMA_DQ4 G29
 VMA_DQ5 F28
 VMA_DQ6 F32
 VMA_DQ7 F30
 VMA_DQ8 C30
 VMA_DQ9 F27
 VMA_DQ10 A28
 VMA_DQ11 C28
 VMA_DQ12 E27
 VMA_DQ13 G26
 VMA_DQ14 D26
 VMA_DQ15 F25
 VMA_DQ16 A25
 VMA_DQ17 C25
 VMA_DQ18 E25
 VMA_DQ19 D24
 VMA_DQ20 E23
 VMA_DQ21 F23
 VMA_DQ22 D22
 VMA_DQ23 E21
 VMA_DQ24 F21
 VMA_DQ25 D20
 VMA_DQ26 F19
 VMA_DQ27 A19
 VMA_DQ28 D18
 VMA_DQ29 F17
 VMA_DQ30 A17
 VMA_DQ31 C17
 VMA_DQ32 E17
 VMA_DQ33 D16
 VMA_DQ34 F15
 VMA_DQ35 A15
 VMA_DQ36 D14
 VMA_DQ37 F13
 VMA_DQ38 A13
 VMA_DQ39 C13
 VMA_DQ40 E11
 VMA_DQ41 A11
 VMA_DQ42 C11
 VMA_DQ43 F11
 VMA_DQ44 A9
 VMA_DQ45 C8
 VMA_DQ46 E9
 VMA_DQ47 D8
 VMA_DQ48 E7
 VMA_DQ49 A7
 VMA_DQ50 C7
 VMA_DQ51 E7
 VMA_DQ52 A5
 VMA_DQ53 E5
 VMA_DQ54 C3
 VMA_DQ55 E1
 VMA_DQ56 G7
 VMA_DQ57 G6
 VMA_DQ58 G1
 VMA_DQ59 G3
 VMA_DQ60 J6
 VMA_DQ61 J1
 VMA_DQ62 J3
 VMA_DQ63 J5

U23C

DQA_0
 DQA_1
 DQA_2
 DQA_3
 DQA_4
 DQA_5
 DQA_6
 DQA_7
 DQA_8
 DQA_9
 DQA_10
 DQA_11
 DQA_12
 DQA_13
 DQA_14
 DQA_15
 DQA_16
 DQA_17
 DQA_18
 DQA_19
 DQA_20
 DQA_21
 DQA_22
 DQA_23
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 DQA_26
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 DQA_46
 DQA_47
 DQA_48
 DQA_49
 DQA_50
 DQA_51
 DQA_52
 DQA_53
 DQA_54
 DQA_55
 DQA_56
 DQA_57
 DQA_58
 DQA_59
 DQA_60
 DQA_61
 DQA_62
 DQA_63

MEMORY INTERFACE

MAA_0 K17
 MAA_1 J20
 MAA_2 H23
 MAA_3 G23
 MAA_4 G24
 MAA_5 H24
 MAA_6 J19
 MAA_7 K19
 MAA_8 J14
 MAA_9 K14
 MAA_10 J11
 MAA_11 J13
 MAA_12 H11
 G11 VMA_BA2
 J16 VMA_BA0
 MAA_14/BA0 VMA_BA0 (17)
 MAA_15/BA1 VMA_BA1 (17)

E32 VMA_DM0
 E30 VMA_DM1
 A21 VMA_DM2
 C21 VMA_DM3
 E13 VMA_DM4
 D12 VMA_DM5
 E3 VMA_DM6
 F4 VMA_DM7

H28 VMA_RDQS0
 C27 VMA_RDQS1
 A23 VMA_RDQS2
 E19 VMA_RDQS3
 E15 VMA_RDQS4
 D10 VMA_RDQS5
 D6 VMA_RDQS6
 G5 VMA_RDQS7

H27 VMA_WDQS0
 A27 VMA_WDQS1
 C23 VMA_WDQS2
 C19 VMA_WDQS3
 C15 VMA_WDQS4
 E9 VMA_WDQS5
 C5 VMA_WDQS6
 H4 VMA_WDQS7

L18 VMA_ODT0
 K16 VMA_ODT1
 H26 VMA_CLKP0
 H25 VMA_CLKN0
 G9 VMA_CLKP1
 H9 VMA_CLKN1

RASA0B VMA_RAS0#
 RASA1B VMA_RAS1#
 G22 VMA_CAS0#
 G16 VMA_CAS1#
 G19 VMA_CS0#
 G16 VMA_CS1#

CSA0B_0 VMA_CKE0
 CSA0B_1 VMA_CKE1
 K20 VMA_WE0#
 J17 VMA_WE1#

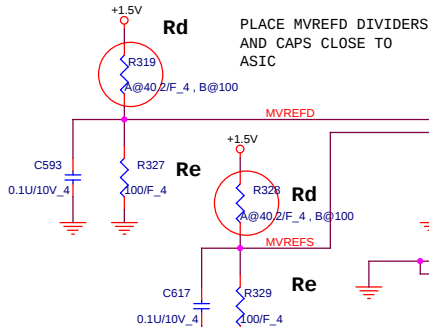
WEA0B VMA_WE0#
 WEA1B VMA_WE1#
 PX_EN VMA_MA13
 RSVD#2
 RSVD#3

VMA_BA2 (17)
 VMA_BA0 (17)
 VMA_BA1 (17)

support 16bit VRAM (64M X 16)

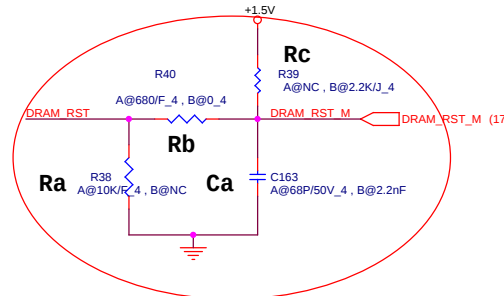
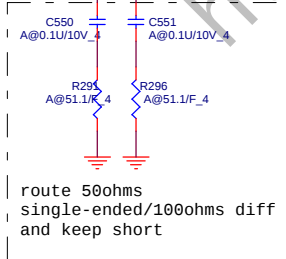
A@ FOR PARK-S3
 B@ FOR M93

For PARK-S3 only
 For M9X-S2/S3 with
 DDR3: this pin is
 not in use.



Do not Install for
 M9X-S2/S3
 Install 240 Ohms
 0.5% Resistor
 for PARK-S3

DIVIDER RESISTORS	M93	PARK
MVREF TO 1.8V (Rd)	100R	40.2R
MVREF TO GND (Re)	100R	100R



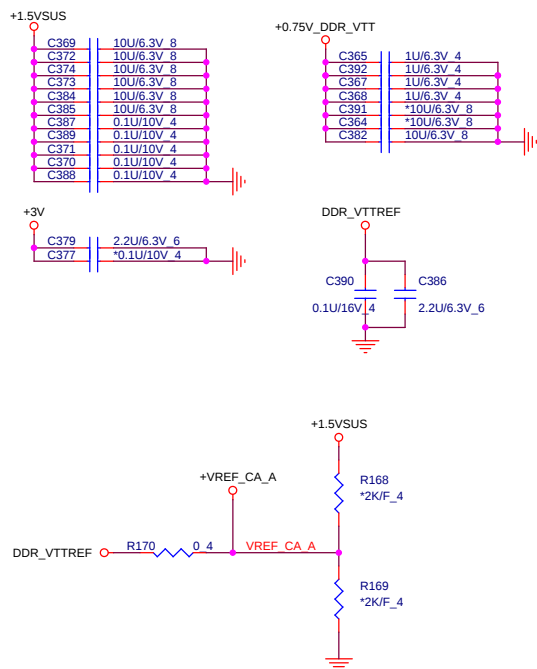
Designator	M9X-S2 and M93-S3	Park-S3
Ra	DNI	10K
Rb	0R/Short	680R
Rc	2.2K	DNI
Ca	2.2nF	68pF



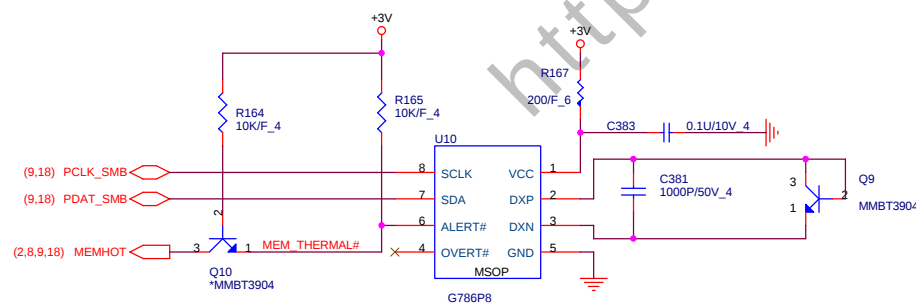
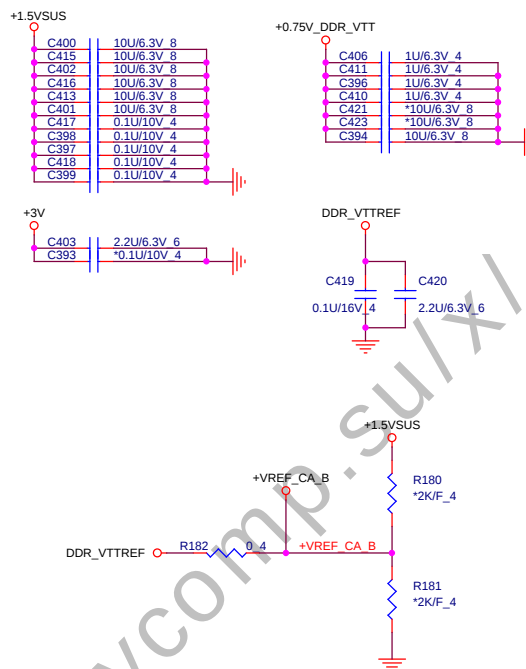
PROJECT : AX2 / 7
 Quanta Computer Inc.

Size	Document Number	Rev
Custom	PARK/MEM_Interface	1A
Date	Wednesday, February 24, 2010	Sheet 16 of 37

Place these Caps near So-Dimm0

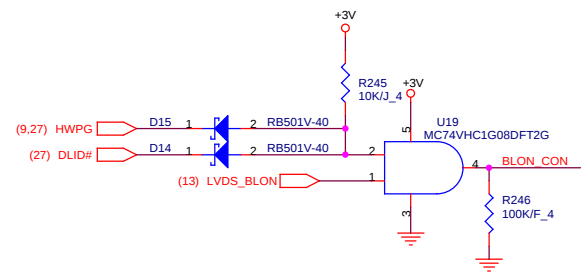


Place these Caps near So-Dimm1



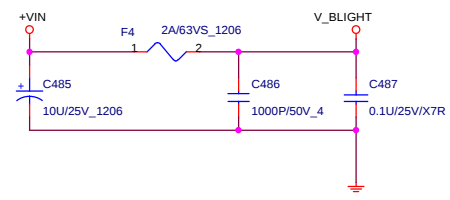
Quanta Computer Inc.
PROJECT :AMD Danube

Backlight Control(LVDS)

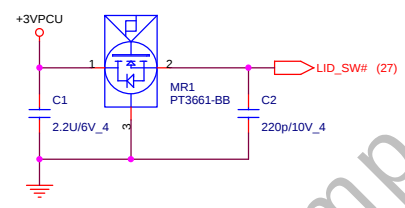


BACKLIGHT POWER

80mils

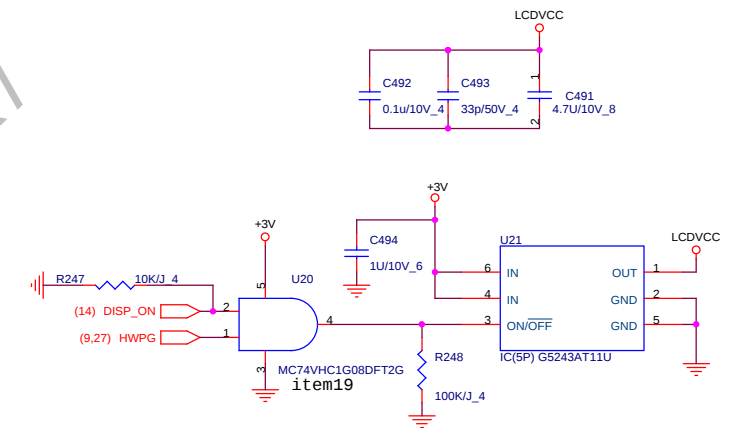


LID SW

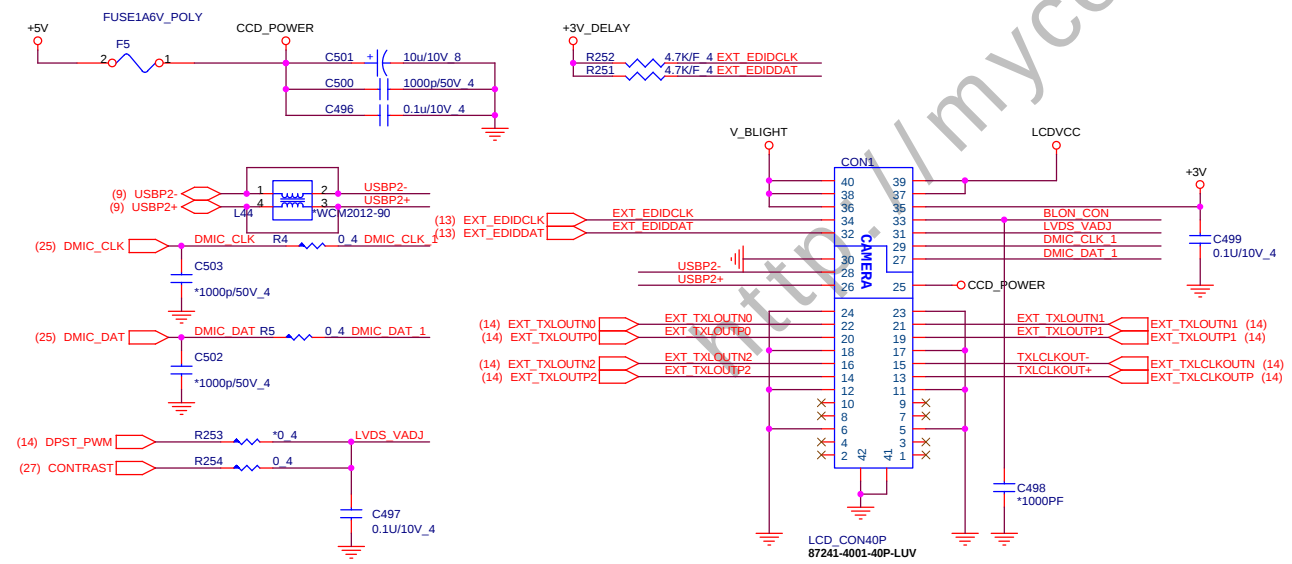


LED Panel POWER SWITCH(LVDS)

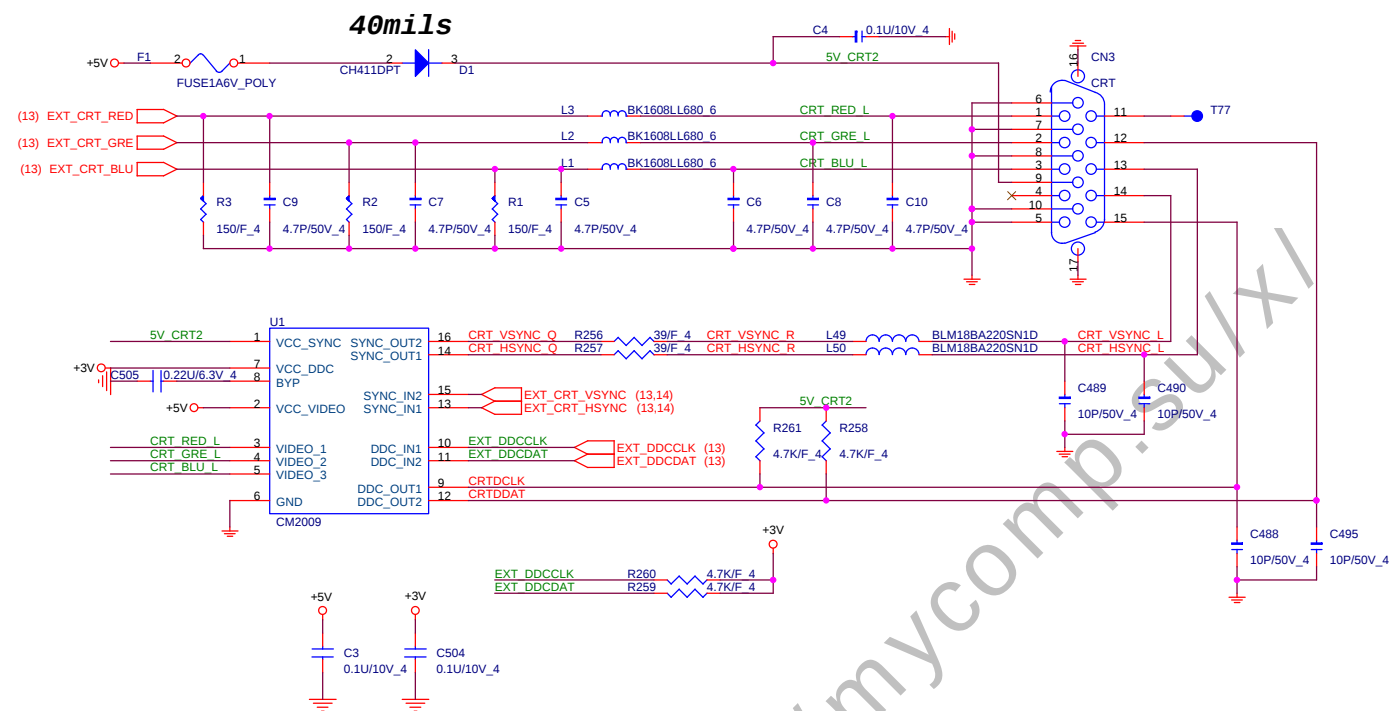
80mils



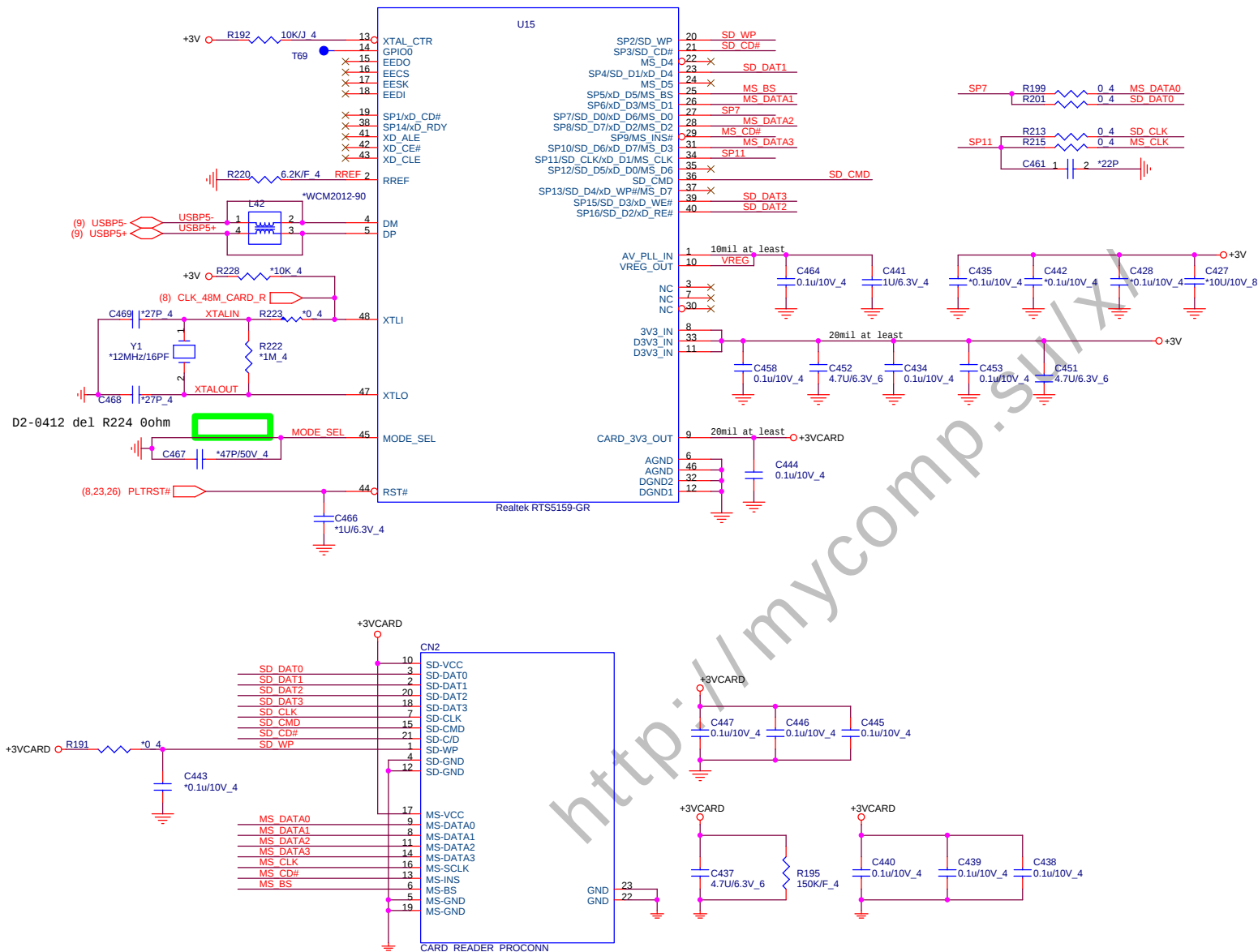
LVDS/CCD



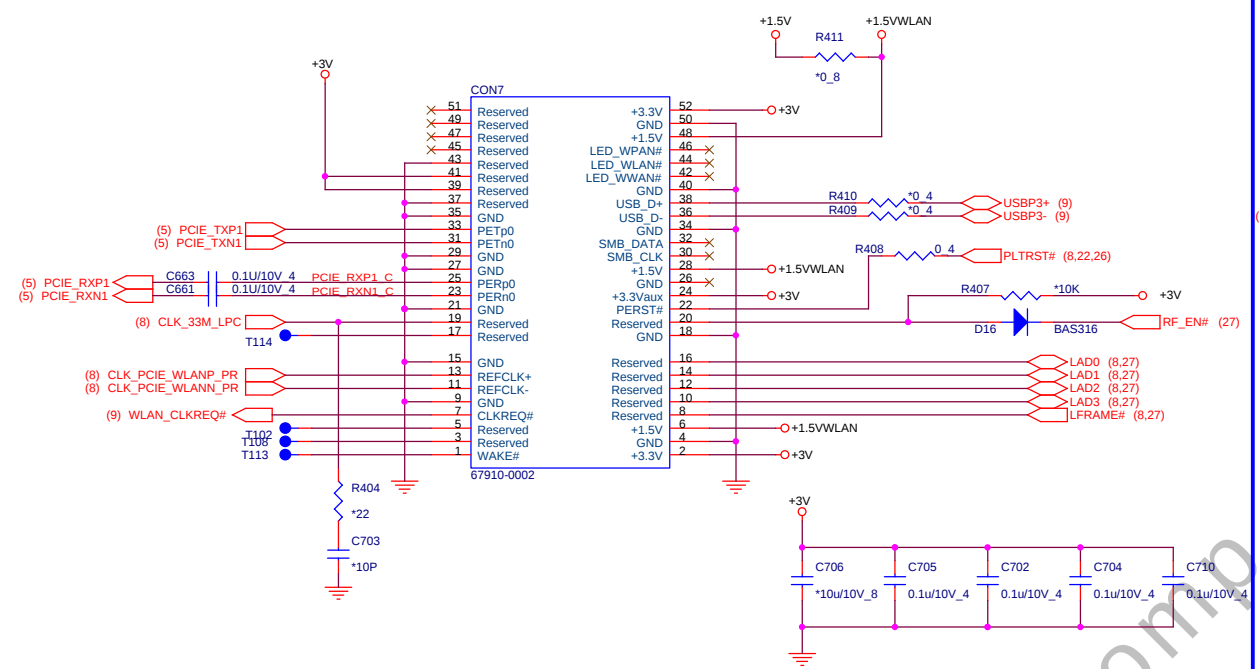
CRT PORT



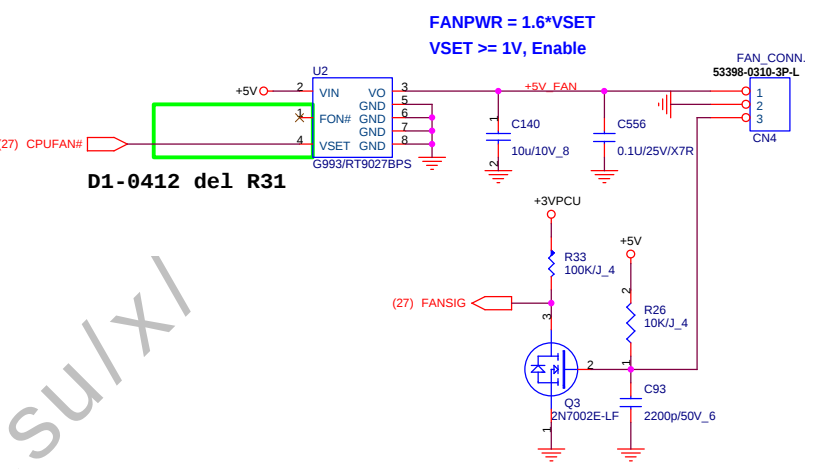
Card Reader



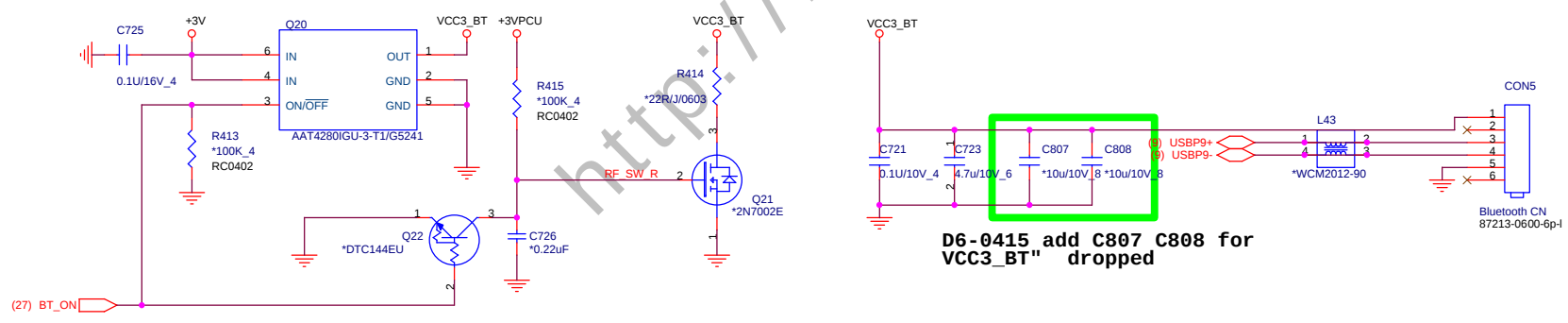
MINI CARD (WLAN)



CPU FAN CTRL

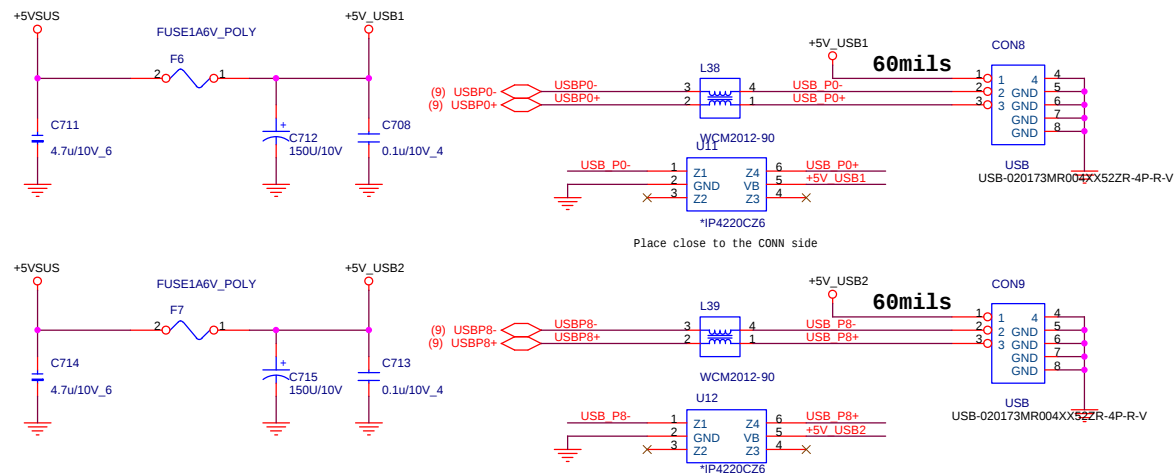


BuleTooth (BTM)

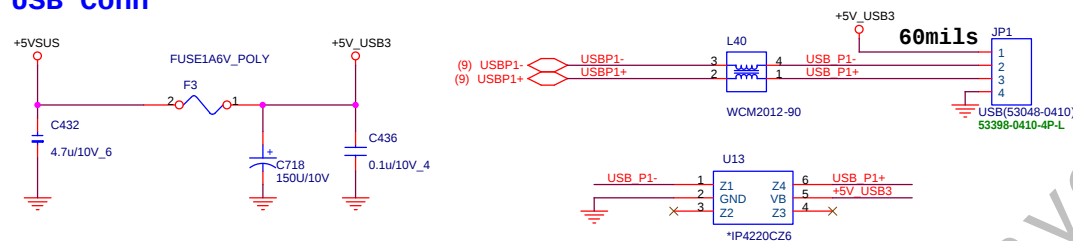


D6-0415 add C807 C808 for VCC3_BT" dropped

USB PORTX2

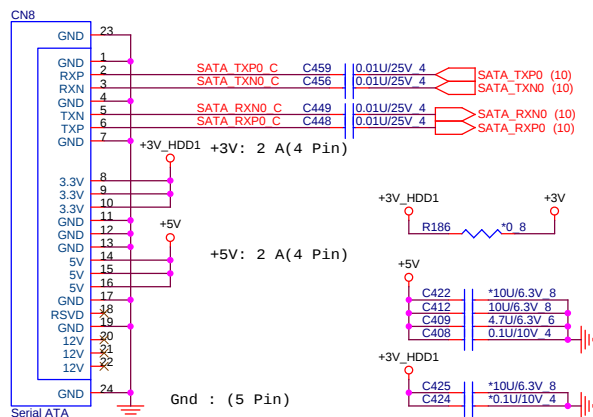


USB Conn



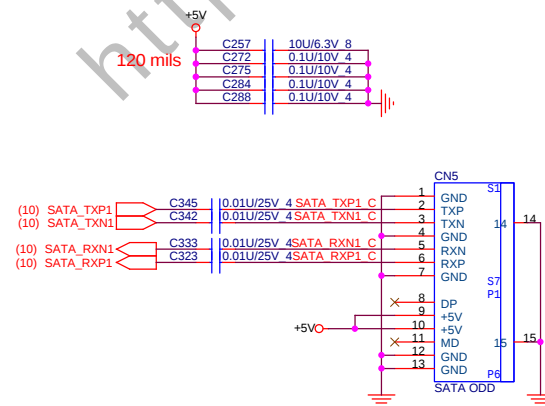
SATA HDD CONNECTOR

DC Current rating: 0.5 A



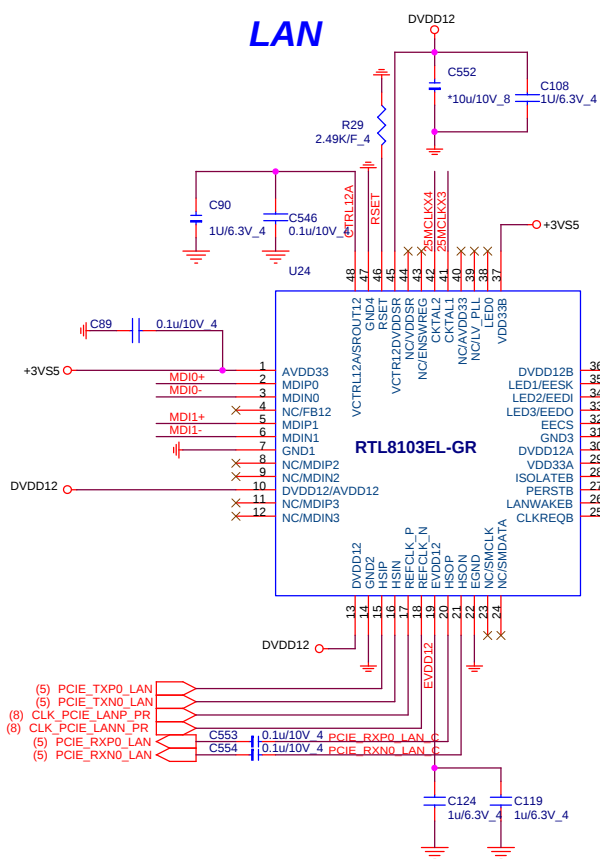
SATA CD-ROM

3V RUN Power.
Need Check
Net Name

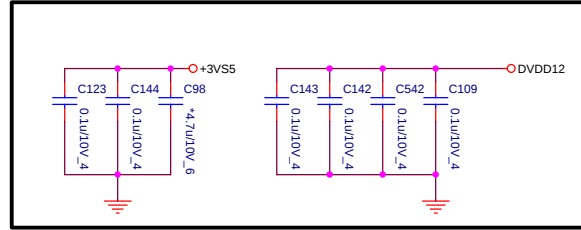


Quanta Computer Inc.
PROJECT : AMD Danube

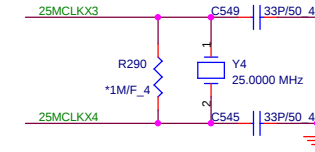
LAN



Placement close to LAN chip

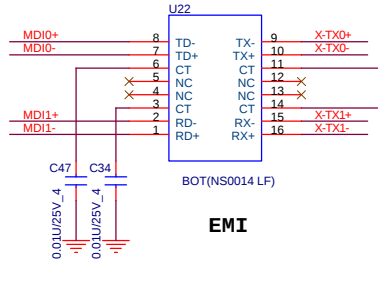


X'tal 25MHz

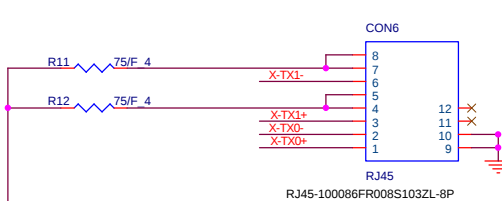


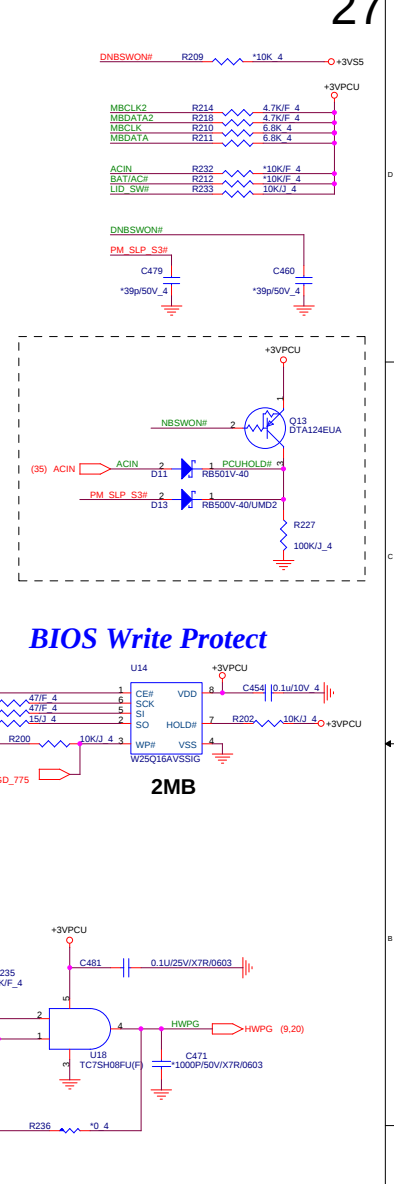
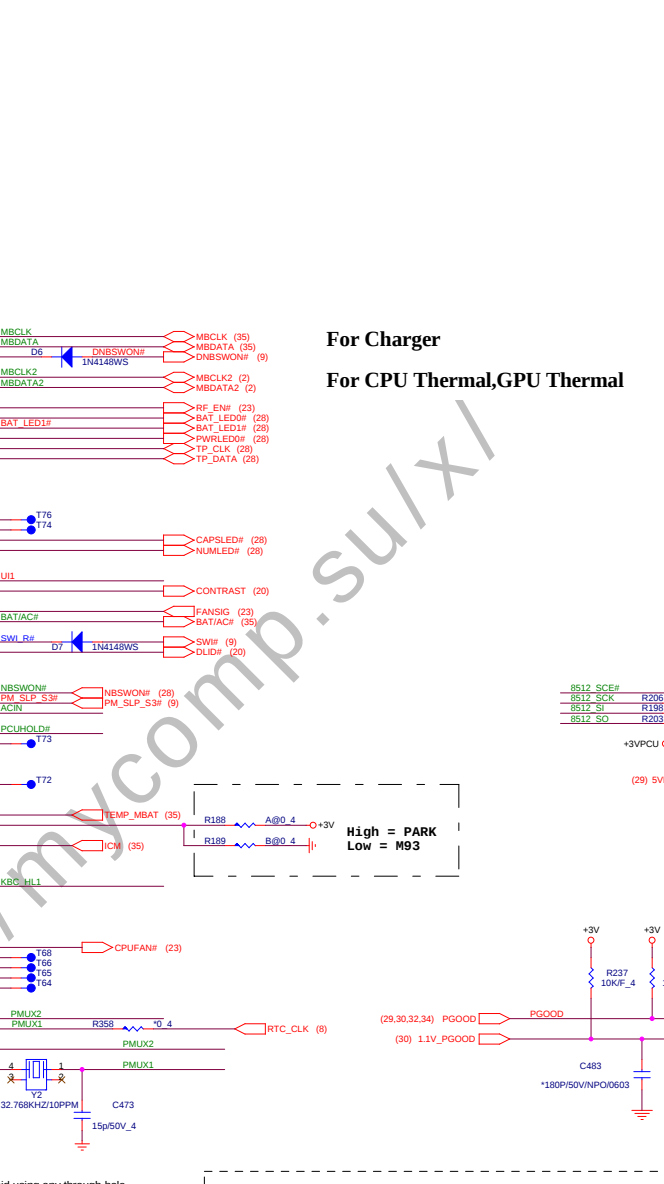
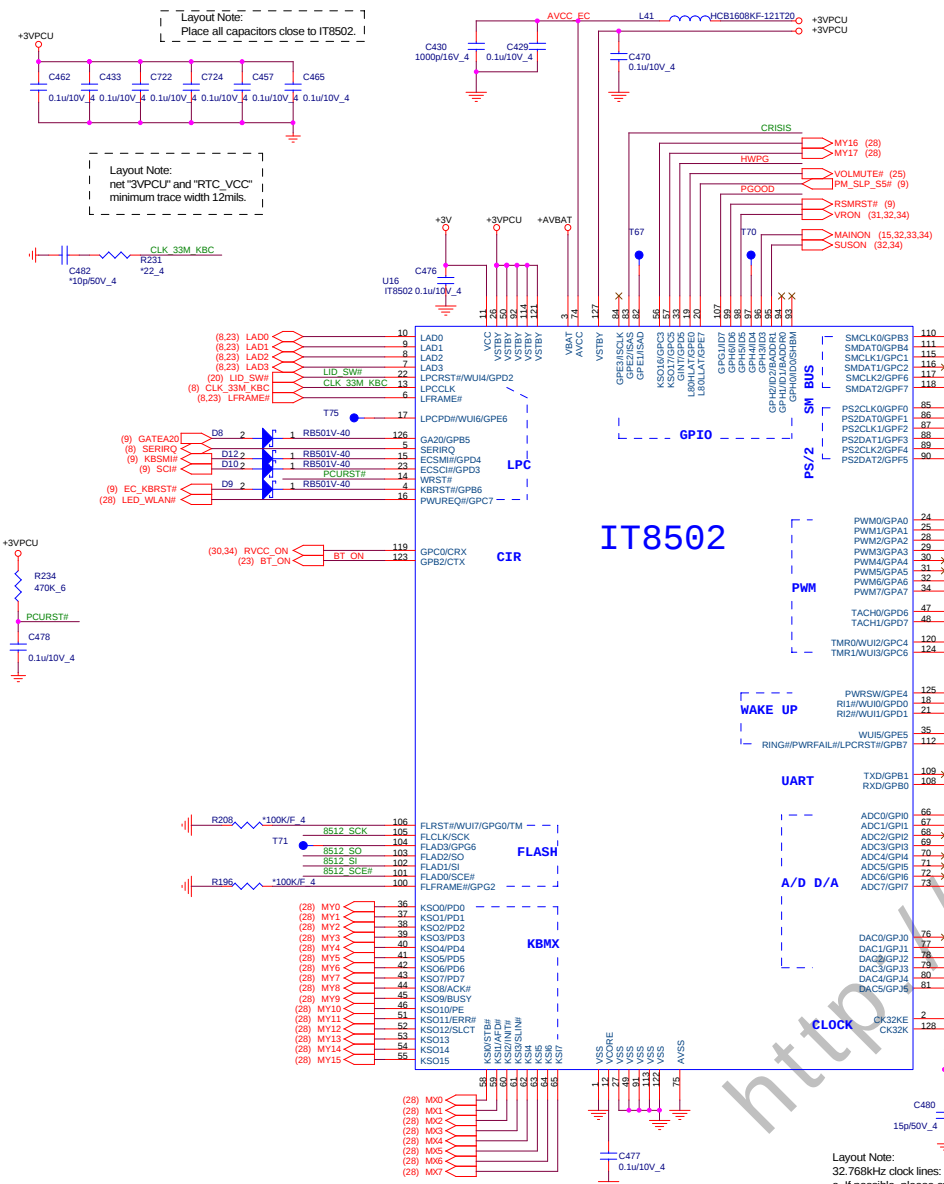
26

10/100 Transformer



RJ45

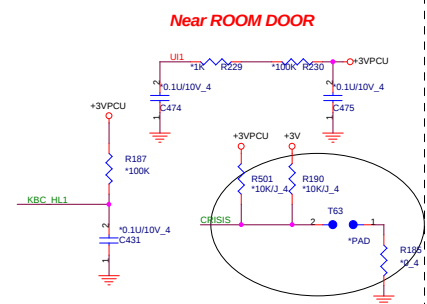




For Charger
For CPU Thermal, GPU Thermal

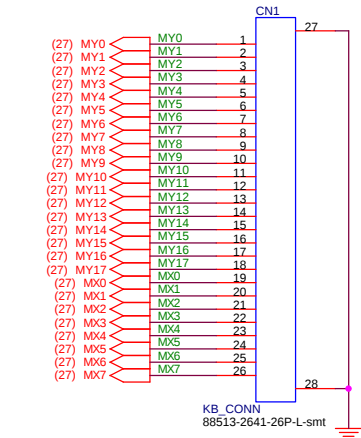
BIOS Write Protect

High = PARK
Low = M93



0415, reserve circuit but
SMT not mount

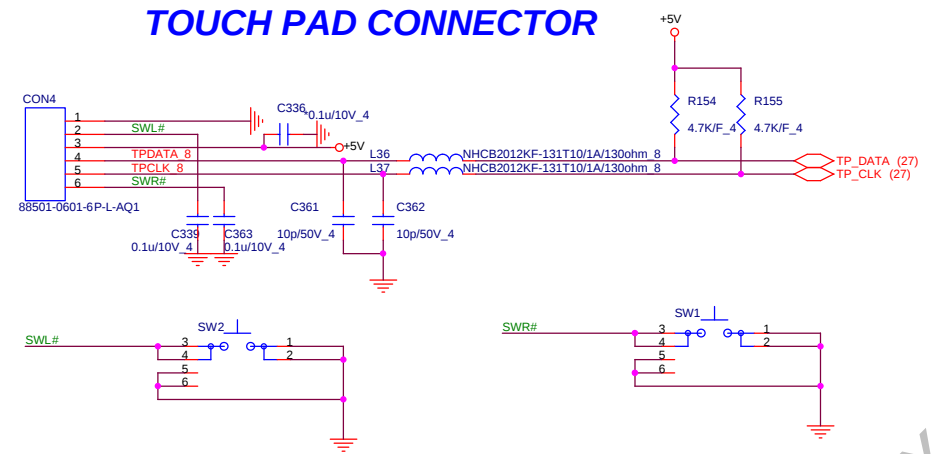
KEY BOARD



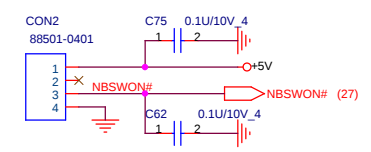
For EMI Reserve Caps for debug

MY3	C575	*10p/50V_4	C578	MX7
MY2	C576	*10p/50V_4	C579	MX6
MY1	C577	*10p/50V_4	C580	MX5
MY0	C558	*10p/50V_4	C581	MX4
MY15	C561	*10p/50V_4	C570	MY8
MY14	C562	*10p/50V_4	C569	MY9
MY13	C563	*10p/50V_4	C568	MY10
MY12	C564	*10p/50V_4	C567	MY11
MX0	C585	*10p/50V_4	C574	MY4
MX1	C584	*10p/50V_4	C573	MY5
MX2	C583	*10p/50V_4	C572	MY6
MX3	C582	*10p/50V_4	C571	MY7
MY16	C560	*10p/50V_4	C559	MY17

TOUCH PAD CONNECTOR

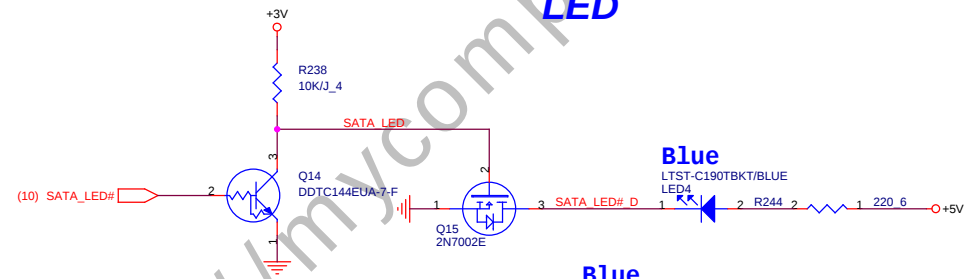


SW BOARD CON



LED

HDD/ODD



CAPS LED



NUM LED



WLAN

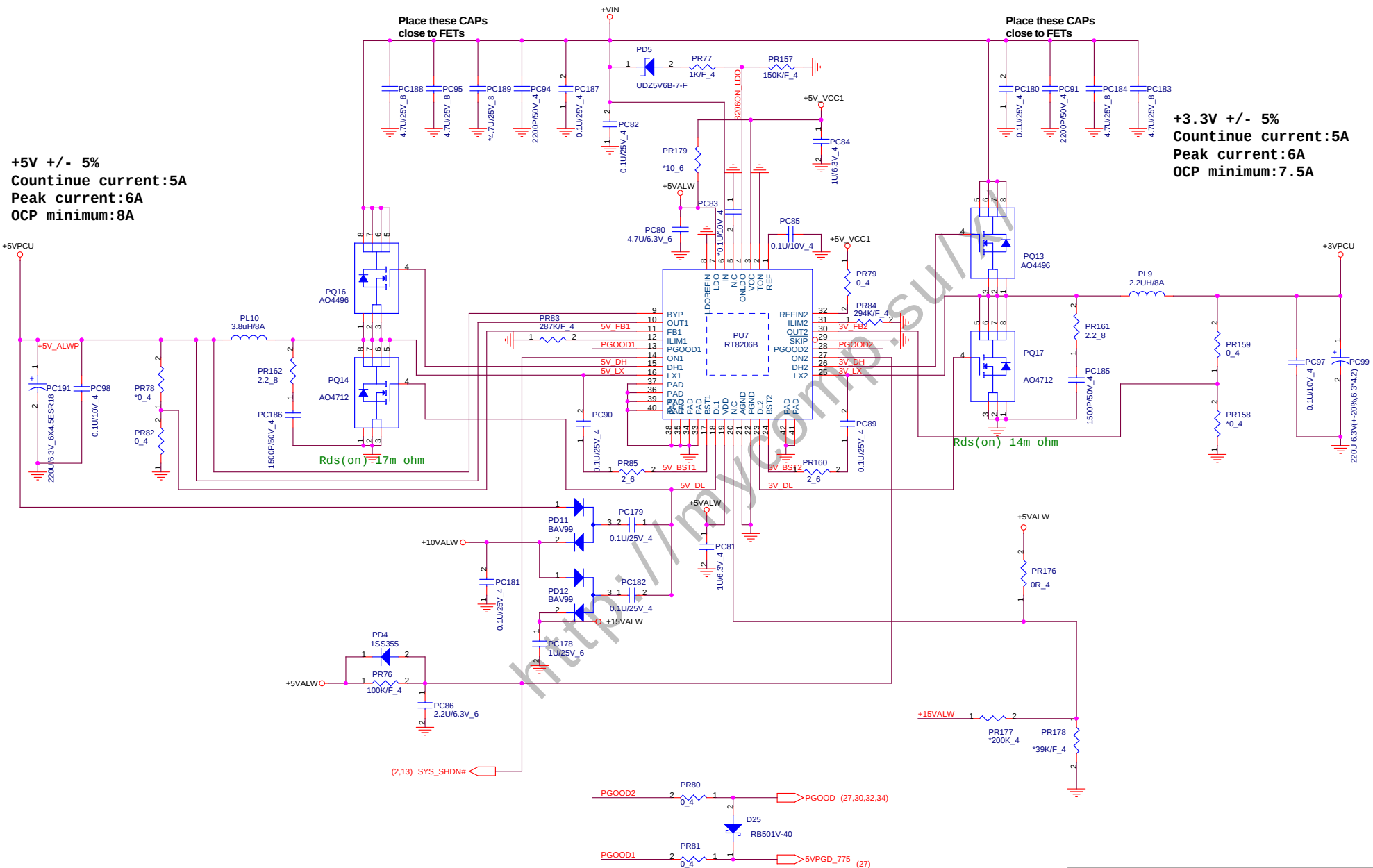


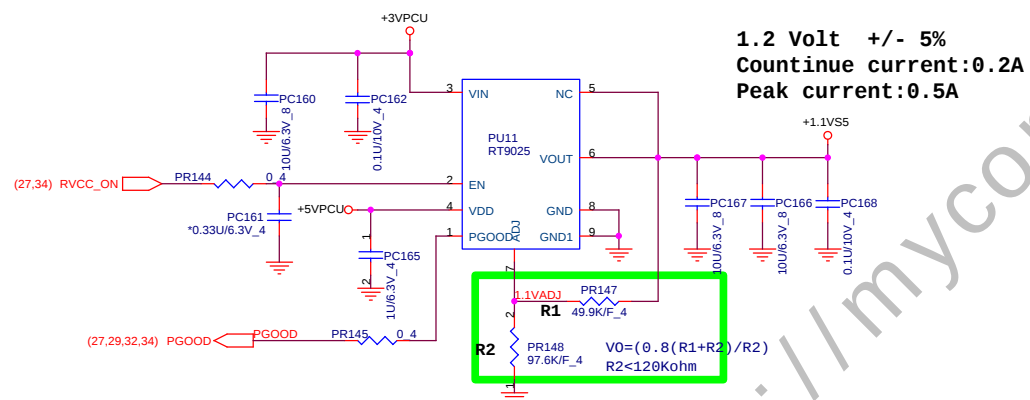
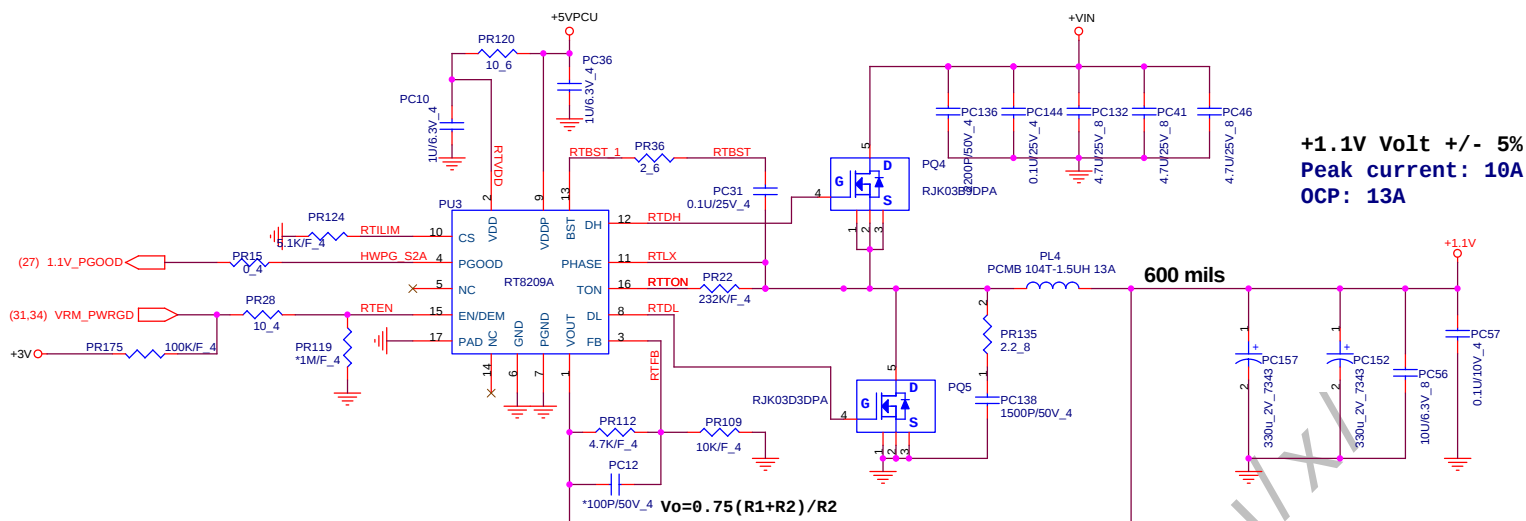
Battery



Power Status



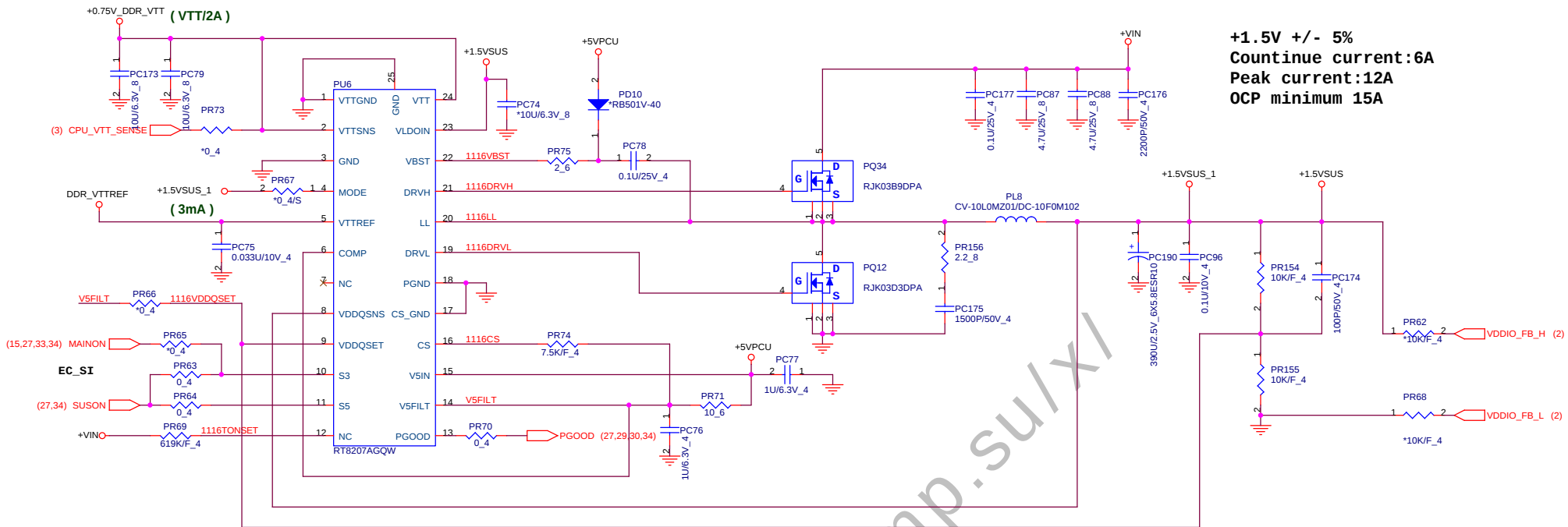




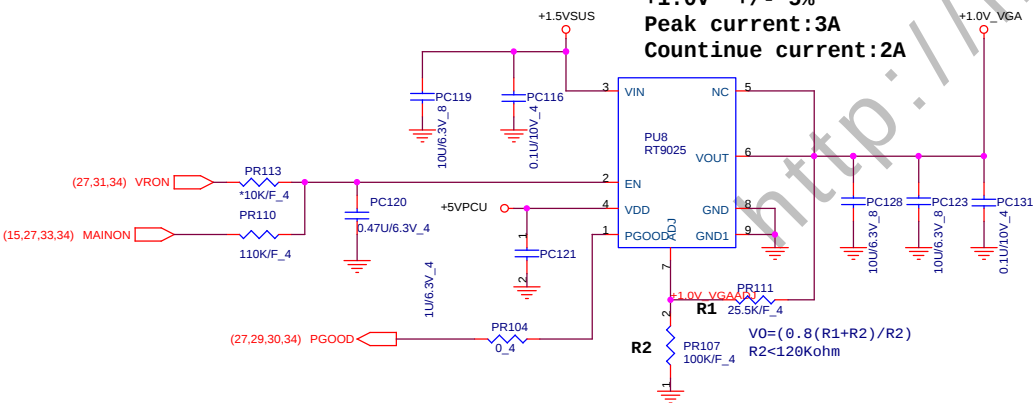
D4-0412 FOR AMD SB820M USB hold time issue on all
 Danubechange PR147 38.7K to 49.9K ohm
 change PR148 100K to 97.6K ohm



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PROJECT : FK1

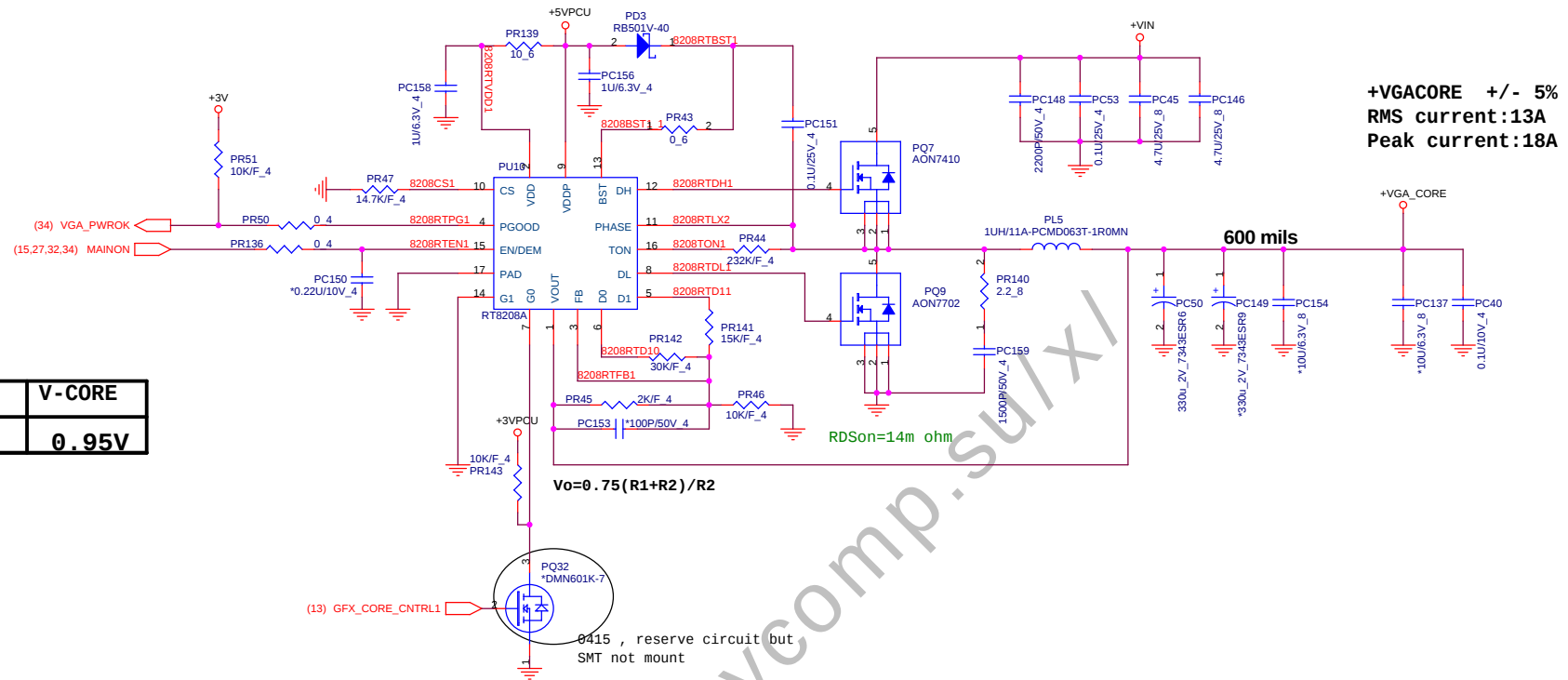


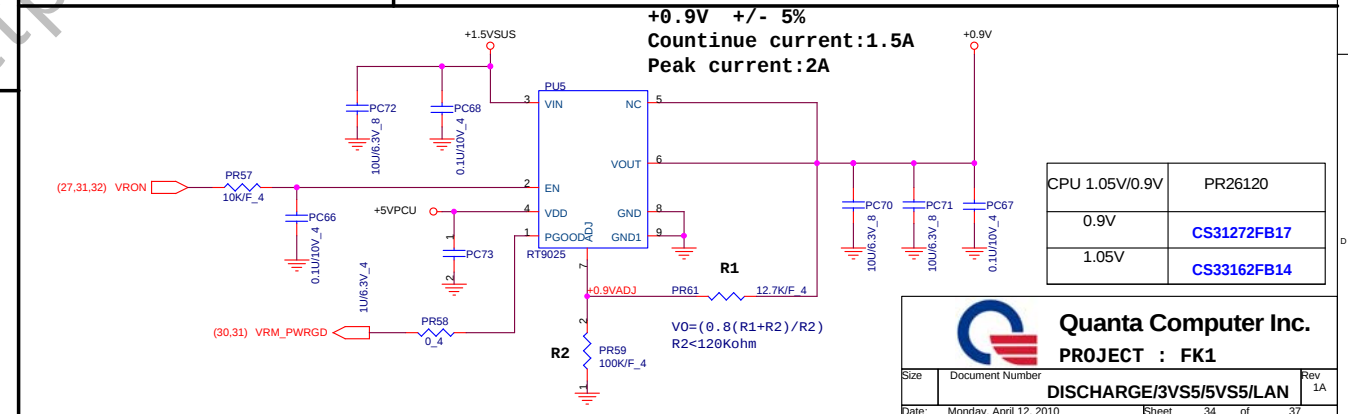
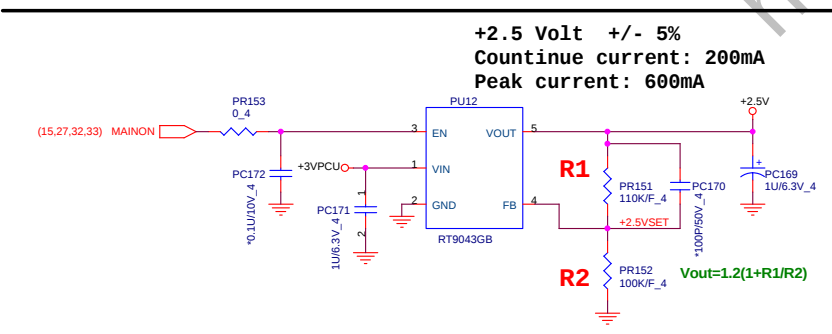
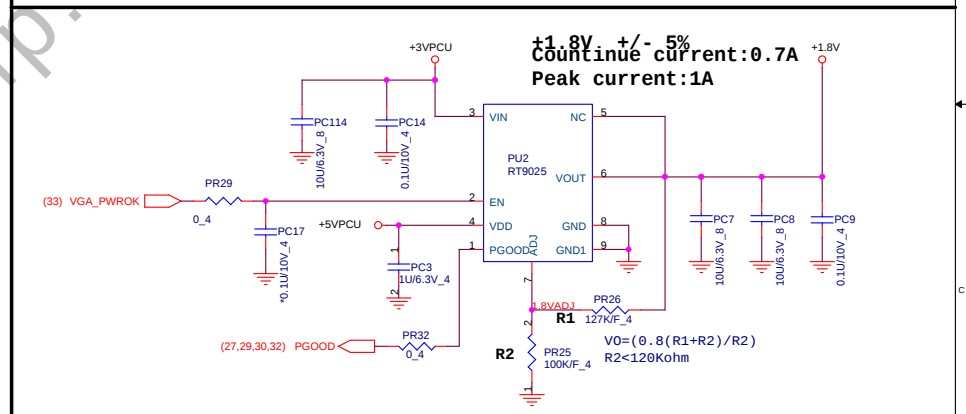
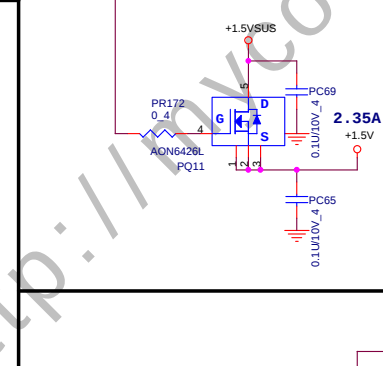
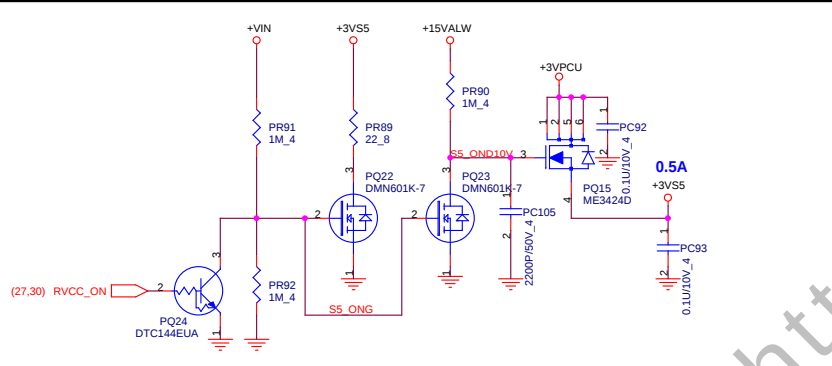
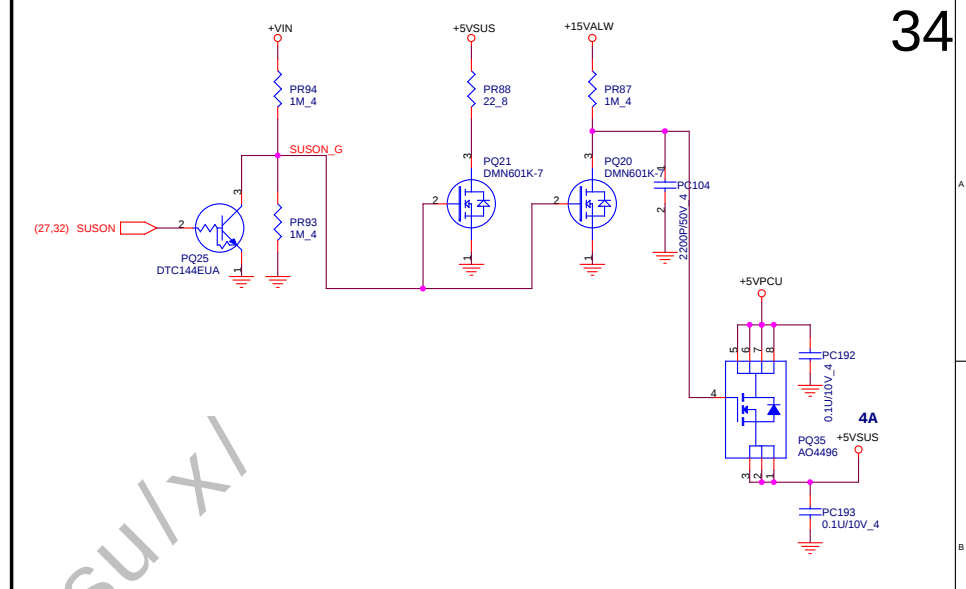
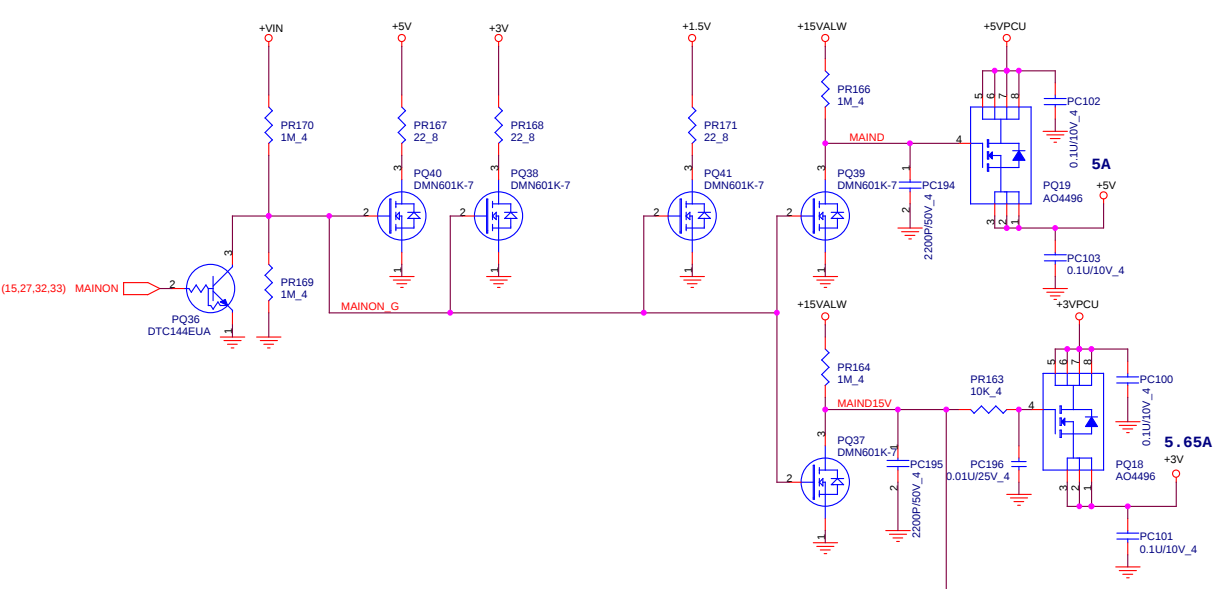
+1.0V +/- 5%
Peak current:3A
Countinue current:2A



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CPU 1.05V/0.9V	PR26120
0.9V	CS31272FB17
1.05V	CS33162FB14

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PROJECT : FK1

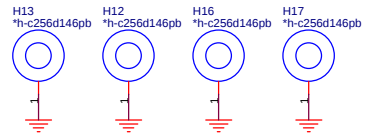
Size	Document Number	Rev
		1A

DISCHARGE/3VS5/5VS5/LAN

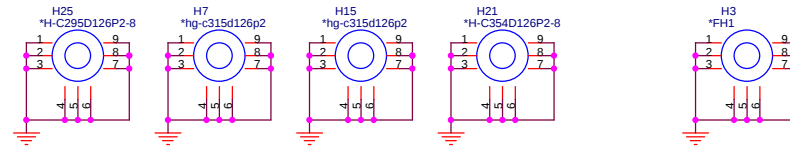
Date: Monday, April 12, 2010 Sheet 34 of 37

Hole

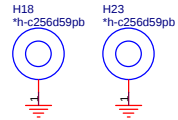
CPU Nut



Hole for ESD



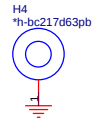
MINI CARD



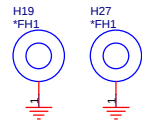
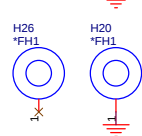
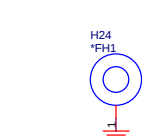
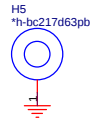
Antenna Hole



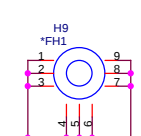
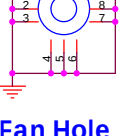
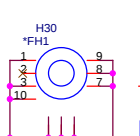
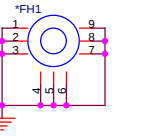
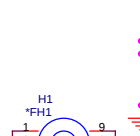
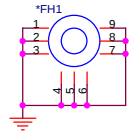
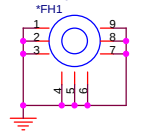
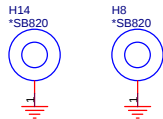
Thermal Module



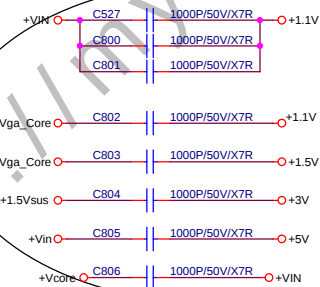
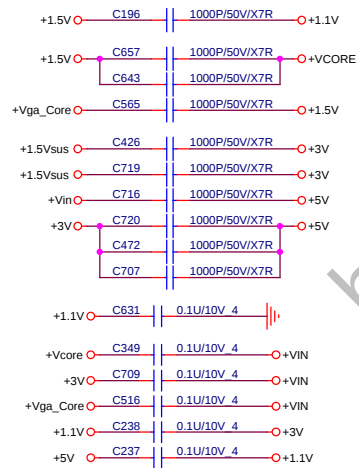
VGA Nut



SB820



Fan Hole



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PROJECT :AMD Danube

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Hole, Nuts		
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Change list from A to B stage

- P25 PR173,PR165 change to 68 ohm.
- P29 Add PR176,PR177,PR178
- P34 PR163 change from 0 to 10K ohm.(For power on timing)
- P34 Add PC196 0.01uF.(For power on timing)
- P34 PR29 change value from 49.9K to 0 ohm.(For Power on timing)
- P34 PC17 change value from 0.1u to NC.(Power on Timing)
- P36 Add C800 , C801 , C802 , C803 , C804 , C805, C806
- P2 Add C760 , R500
- P29 delete PR86
- P30 PR124 ,PL4, PC31 change to 5.1K ,1.5uH ,0.1u for OCP 13A
- P31 PR4 change to NC
- P32 PC174 Mount
- P32 modify circuit for VDDIO_FB_H and VDDIO_FB_L
- P32 PR62 change to NC , delete PR123
- P33 PC153 Mount
- P34 Mount PR171 ,PQ41 ,PR88 ,PQ21 ,PR89 , PQ22 for discharge
- P34 delete PR10 , PR60
- P35 Mount PR14 , PR19 change form 10K to 100K
- P27 Add R501
- P27 Add D25

Change list from B to C stage

- P2 delete 0ohm R367 , R360 , R342
- P5 delete 0ohm R70
- P6 delete 0ohm R313 , R312 , R315 , R54
- P9 delete 0ohm R343 , R393 , R394
- P8 delete 0ohm RP1 , RP2 , RP3 , RP4 , RP5 , RP6 , RP7
- P20 delete 0ohm R250 , R249
- P22 delete 0ohm R219 , R205 , R225
- P26 delete 0ohm R203 , R301
- P25 delete 0ohm AR25
- Page 29,PC99 from Polymer capacitor change to E/C
- Page31,PQ8 and PQ31 low side Mosfet part number correct is RJK03D3DPA
- Page35 PL1 from 0805/5A change to 1206/6A
- P7 delete 0ohm L21 , L61 , L22 , R55 , R318 , R68 , R67
- P11 delete 0ohm R105 , R143 , L35 , R146 , L35 , R146 , R152
- P13 delete 0ohm R270 , R272 , R274
- P14 delete 0ohm R278 , R262
- P22 delete 0ohm R221 , R226 , R204 , R193 , R194 , R197 , R207
- P32 delete 0ohm PR72
- P20 C1 change form 0.1u to 2.2u
- P24 ADD L38,L39,L40 for EMI issue

Change list from C to MP stage

- D1-P23 Delete R31 10Kohm , Delete U2 PIN1 trace
- D2-P22 Delete R224 0ohm
- D3-P25 change AU2 pin5 , AU3 pin5 , R416 pin1 , AU1 pin5 form +3VS5 to +3V
- D4-P30 FOR AMD SB820M USB hold time issue on all Danube change PR147 38.7K to 49.9K ohm change PR148 100K to 97.6K ohm
- D5-P25 change AC17 form 10uF to 1uF
- D6-P23 add C807 C808 10uF for VCC3_BT" dropped



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Size	Document Number	Rev
Change List		1A
Date:	Monday, April 19, 2010	Sheet 37 of 37