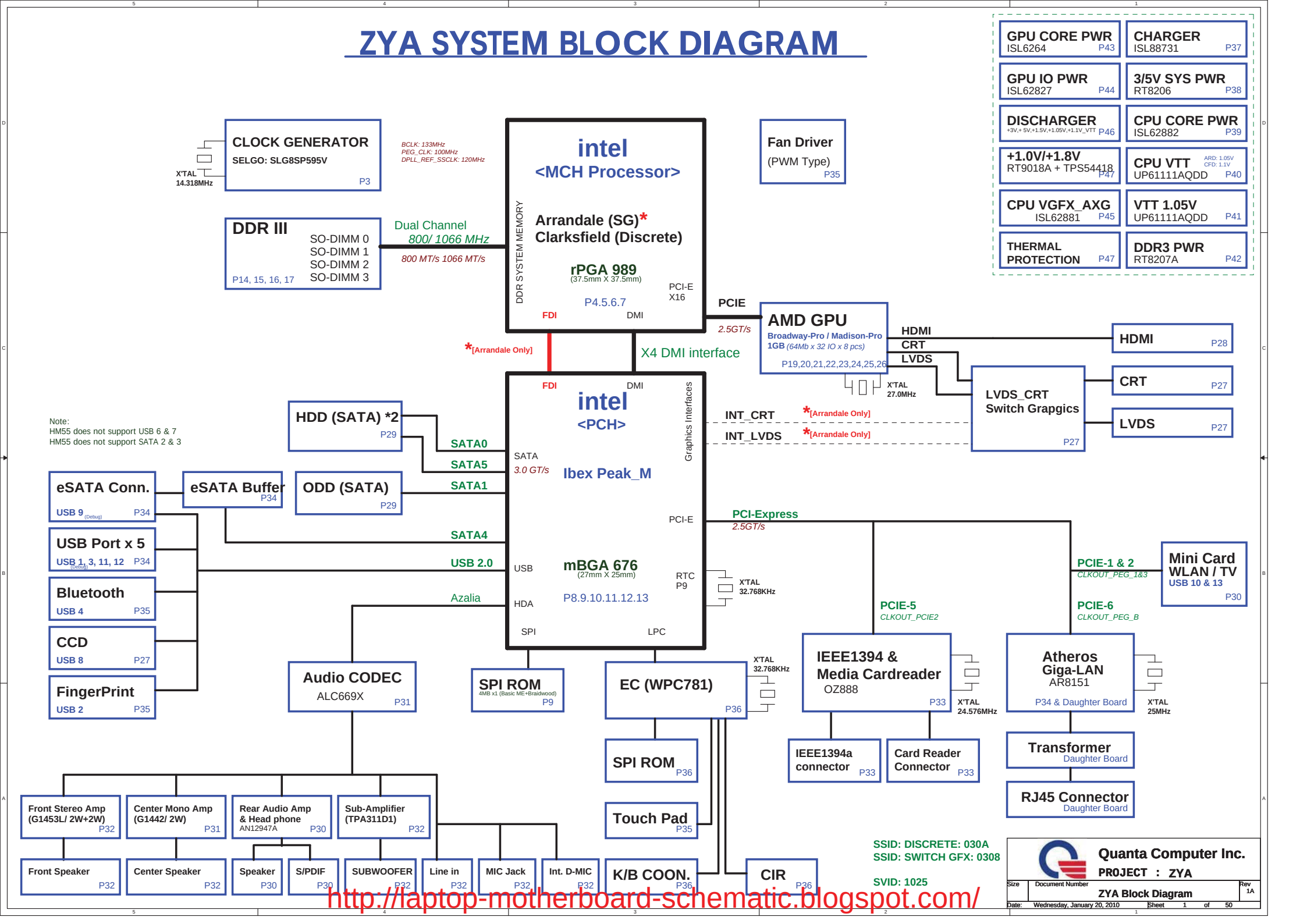
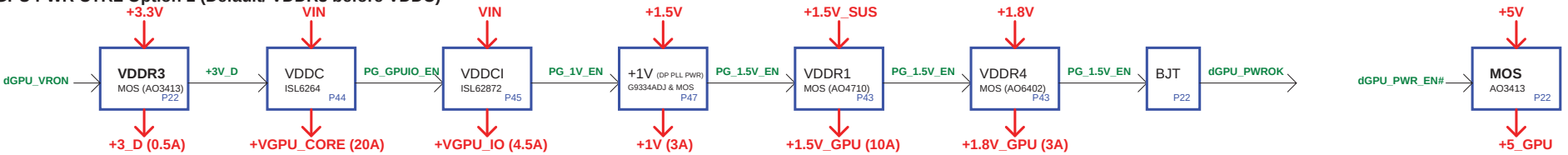
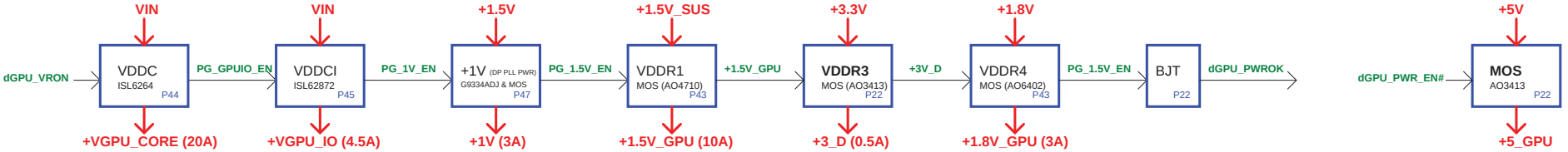
ZYA SYSTEM BLOCK DIAGRAM



GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



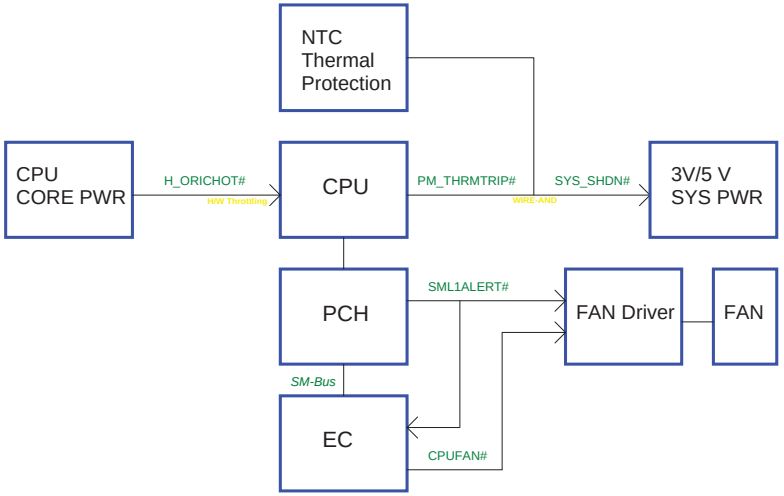
GPU PWR CTRL Option 2 (VDDR3 after VDDR1)



Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+5V_GPU	+5V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN#	Discrete enable
+GPU_CORE	+0.9V~+1.1V	GPU CORE POWER	+3V_D	Discrete enable
+GPU_IO	+0.9V~+1.1V	GPU I/O POWER	PG_GPUIO_EN	Discrete enable
+1.5V_GPU	+1.5V	VRAM CORE POWER	PG_1.5V_EN	Discrete enable
+1.8V_GPU	+1.8V	GPU_CRE/LVDS/PLL POWER	+1.5V_GPU	Discrete enable
+1V	+1V	DP/PEG POWER	PG_1V_EN	Discrete enable

Thermal Follow Chart



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REV : B chenge pin define for B-test

+1.5V **150mA(20mil)** C10050 close L35

L26 BLM18AG601/0.2A_6

180ohm/1.5A

R402 *0_6

C579 *10u/6.3V_8 | C575 .1u/16V_4 | C535 .1u/16V_4 | C565 .1u/16V_4

+1.5V_CLK

+3V

L31 BLM18AG601/0.2A_6

+3V_CLK

C10000 close L72

C584 10u/6.3V_8 | C533 0.1u/10V_4 | C560 0.1u/10V_4

[10] CLK_ICH_14M R381 33_4 CPU_SEL

C556 33p_4 | C546 33p_4

Y2 14.318MHZ

XTAL_IN | XTAL_OUT

U20

1	VDD_DOT	VDD_SRC_I/O	15
17	VDD_SRC	VDD_CPU_I/O	18
24	VDD_CPU		
5	VDD_27	DOT_96	3
29	VDD_REF	DOT_96#	4
31	SDA	27M	6
32	SCL	27M_SS	7
30	REF_0/CPU_SEL	SRC_1/SATA	10
		SRC_1#/SATA#	11
28	XTAL_IN	SRC_2	13
27	XTAL_OUT	SRC_2#	14
		*CPU_STOP#	16
2	VSS_DOT	CPU_1	20
8	VSS_27	CPU_1#	19
9	VSS_SATA	CPU_0	23
12	VSS_SRC	CPU_0#	22
21	VSS_CPU		
26	VSS_REF	CKPWRGD/PD#	25
33	GND		

SLG8LV595V

CLK_SDATA 31
CLK_SCLK 32

+VDDIO_CLK

CLK_BUF_DREFCLK [10]
CLK_BUF_DREFCLK# [10]

R395 B@0_4
R396 *0_4
27M_CLK [20]
For ATI suggest

CLK_BUF_DREFSSCLK [10]
CLK_BUF_DREFSSCLK# [10]
CLK_BUF_PCIE_3GPLL [10]
CLK_BUF_PCIE_3GPLL# [10]

Switch CLK_BUF_DREFSSCLK and CLK_BUF_PCIE_3GPLL on ver B(SATA)

R354 10K_4 +3V

TP23 TP21

CLK_BUF_BCLK [10]
CLK_BUF_BCLK# [10]

CK_PWRGD_R

80mA(20mil) C465 close L36 +1.05V

BKP1608HS181T_6_1.5A L29

C534 .1u/16V_4 | C558 .1u/16V_4 | C557 10u/Y5V_8

SLG8SP595V	STUFF L35 (default)
SLG8SP585V	STUFF R10000

For EMI

CLK_ICH_14M C561 *10p/50V_4
27M_CLK C580 *10p/50V_4

CPU_CLK select

+1.05V

R386 *4.7K_4

CPU_SEL

R388 4.7K_4

	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

SMBus

+3V

R399 4.7K_4

[10] ICH_SMBDATA — Q23 2N7002K — CLK_SDATA — CLK_SDATA [14,15,16,17,30]

+3V

R400 4.7K_4

[10] ICH_SMBCLK — Q24 2N7002K — CLK_SCLK — CLK_SCLK [14,15,16,17,30]

CLK Enable

+3V

R343 1K/F_4

CK_PWRGD_R

Q20 2N7002K

[39] VR_PWRGD_CK505# — R345 100K/F_4

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	Clock Generator	1A

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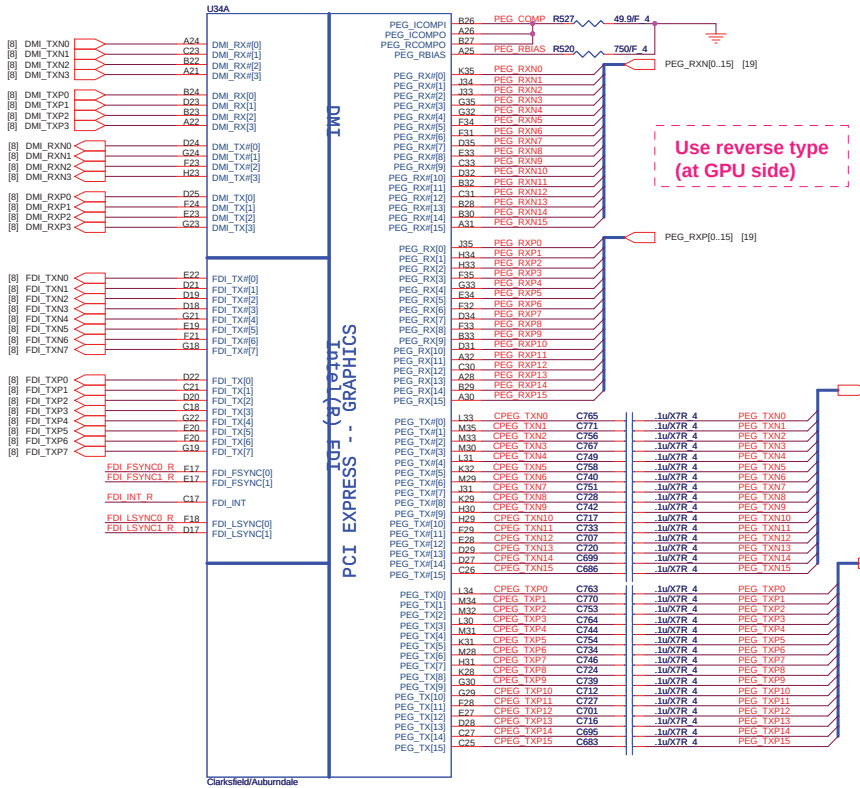
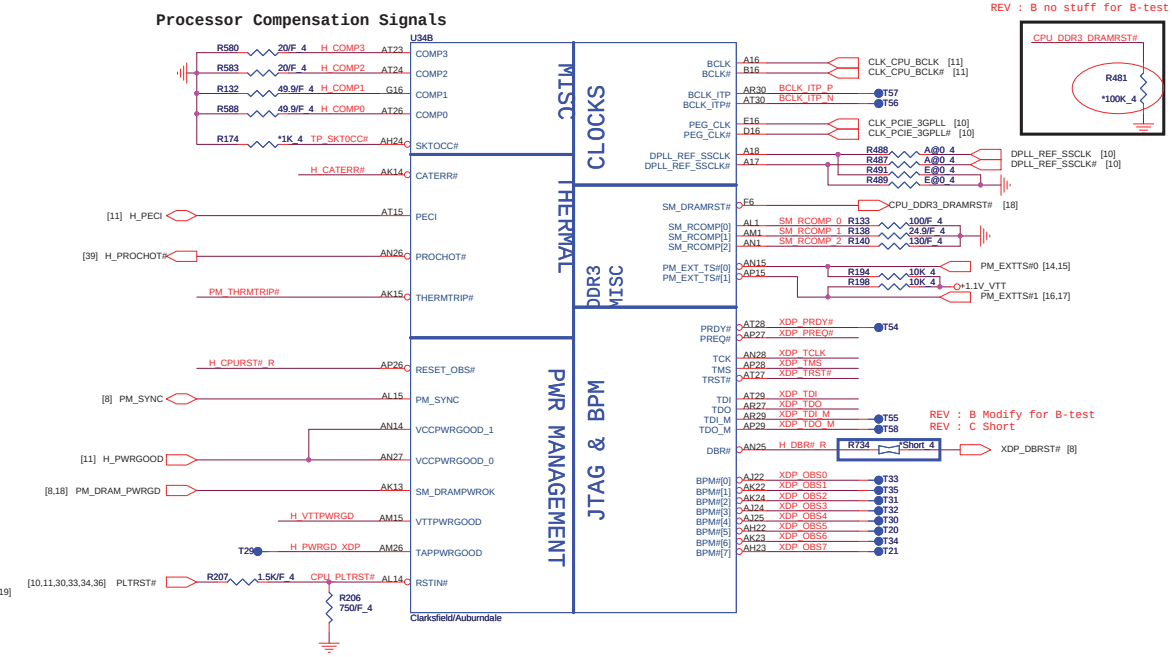
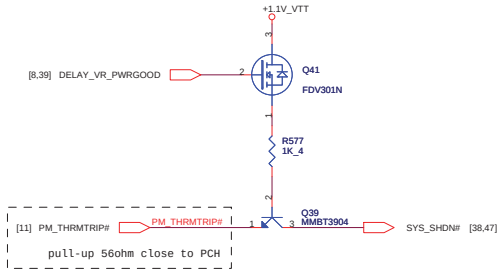
AUBURNDALE/CLARKSFIELD PROCESSOR (DMI,PEG,FDI)



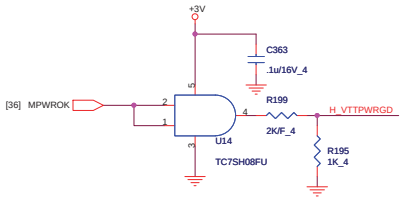
AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)



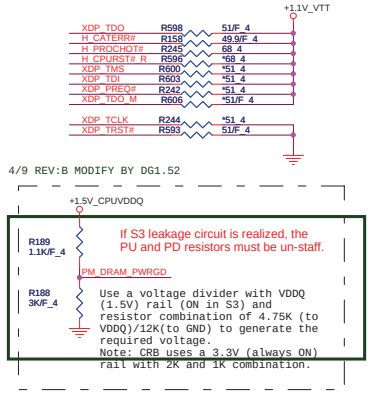
Thermaltrip protect

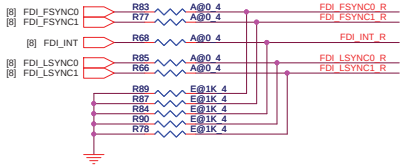


VTT PWR_Good



Processor pull-up





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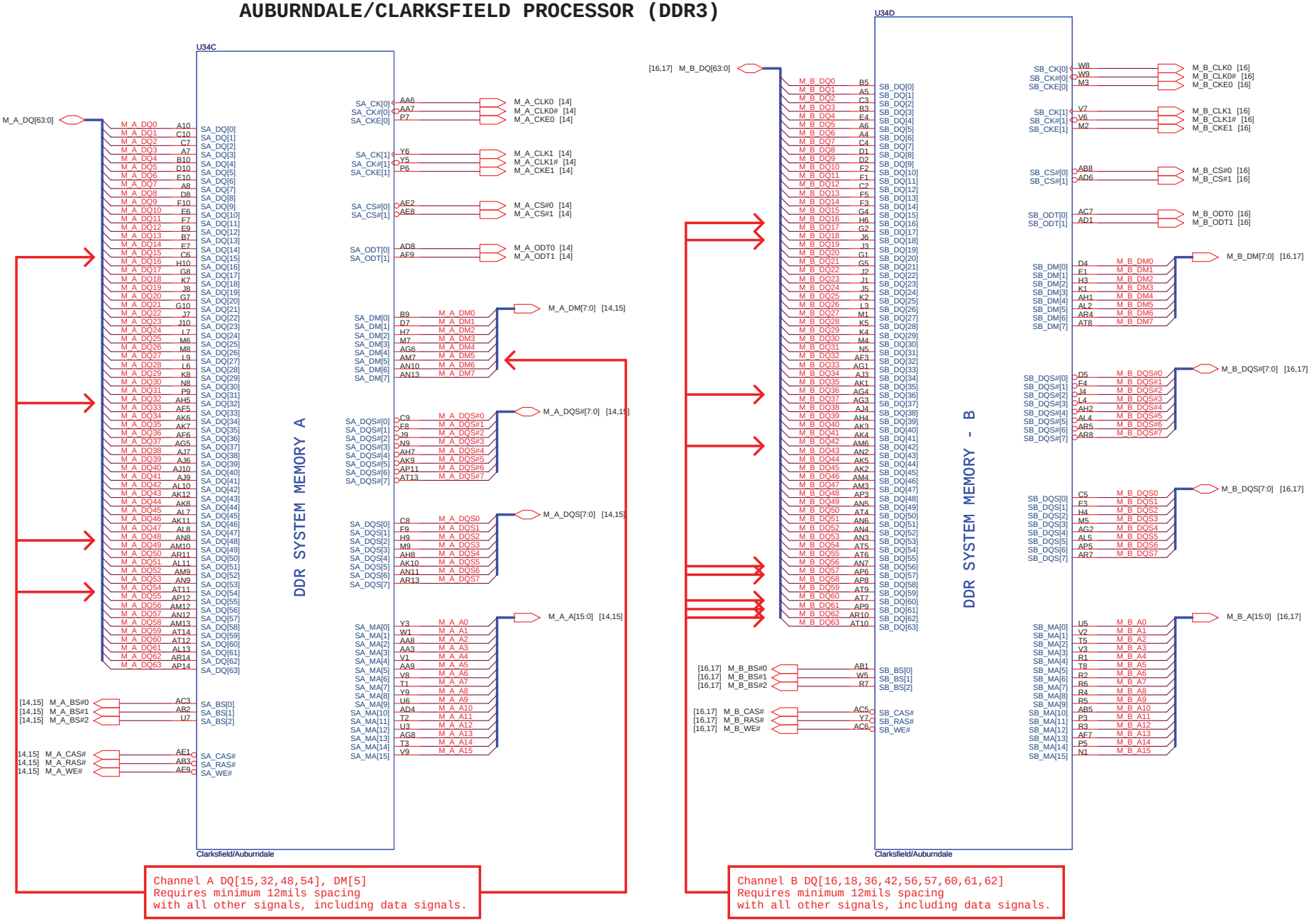
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



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PROJECT : ZYA			
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	AUBURNDA 2/4		1A
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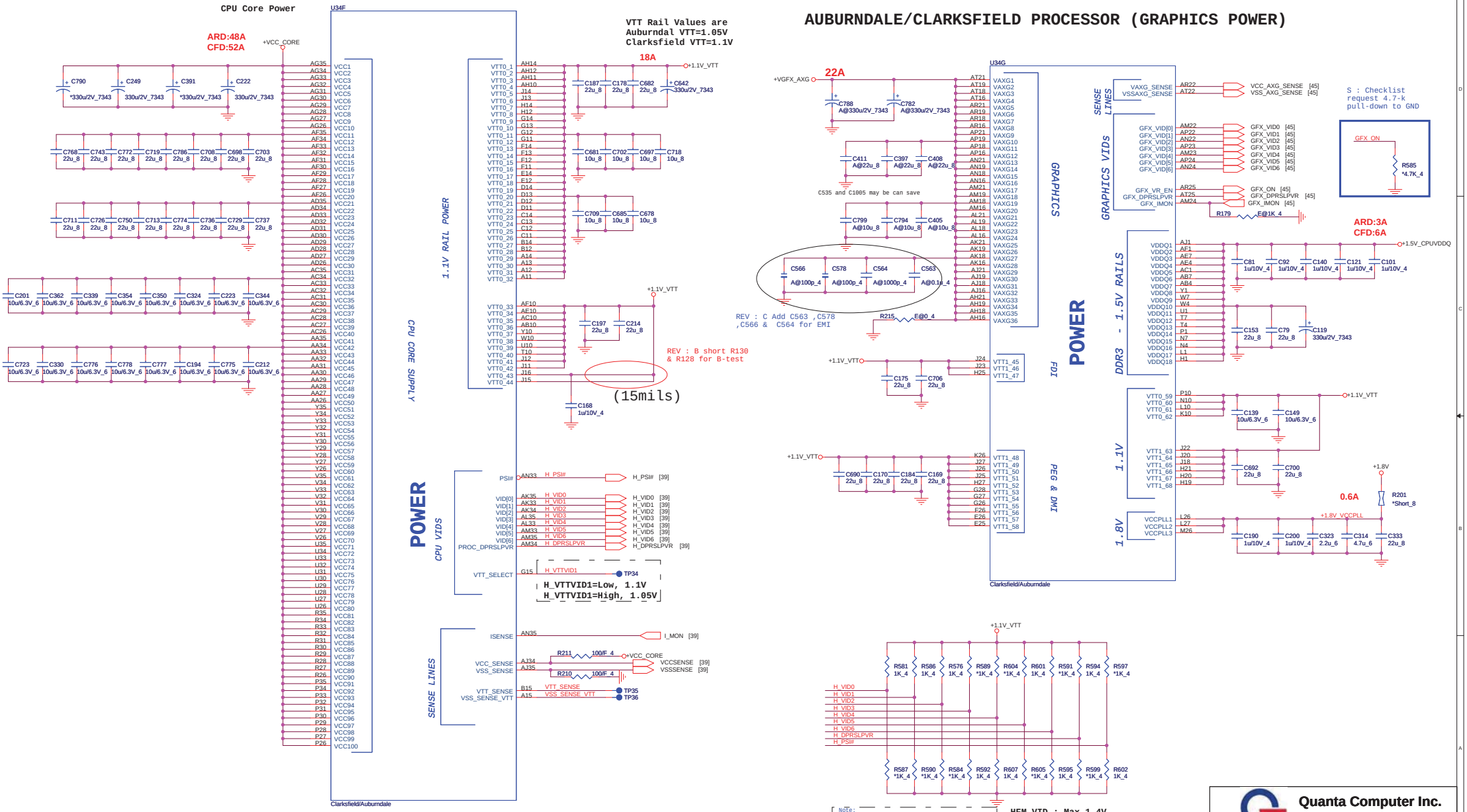
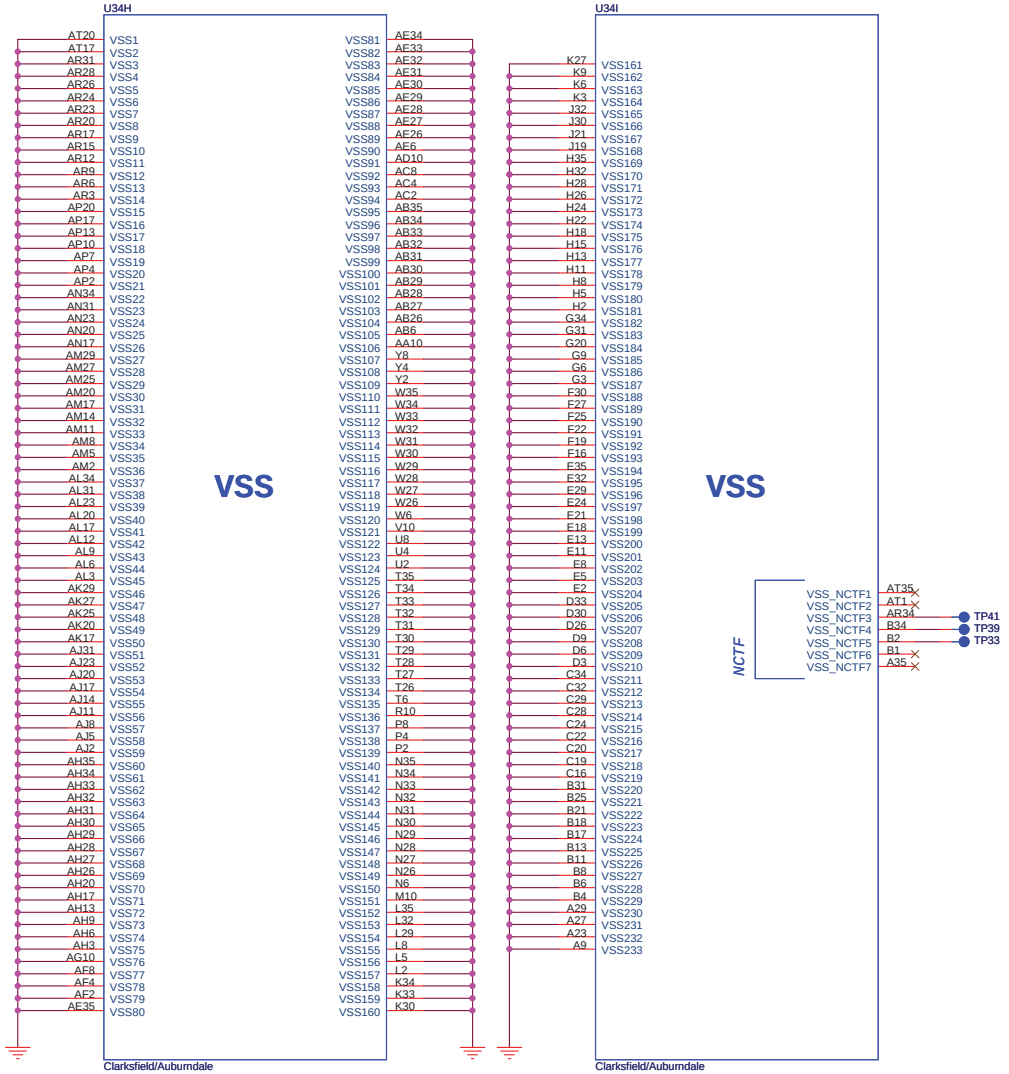
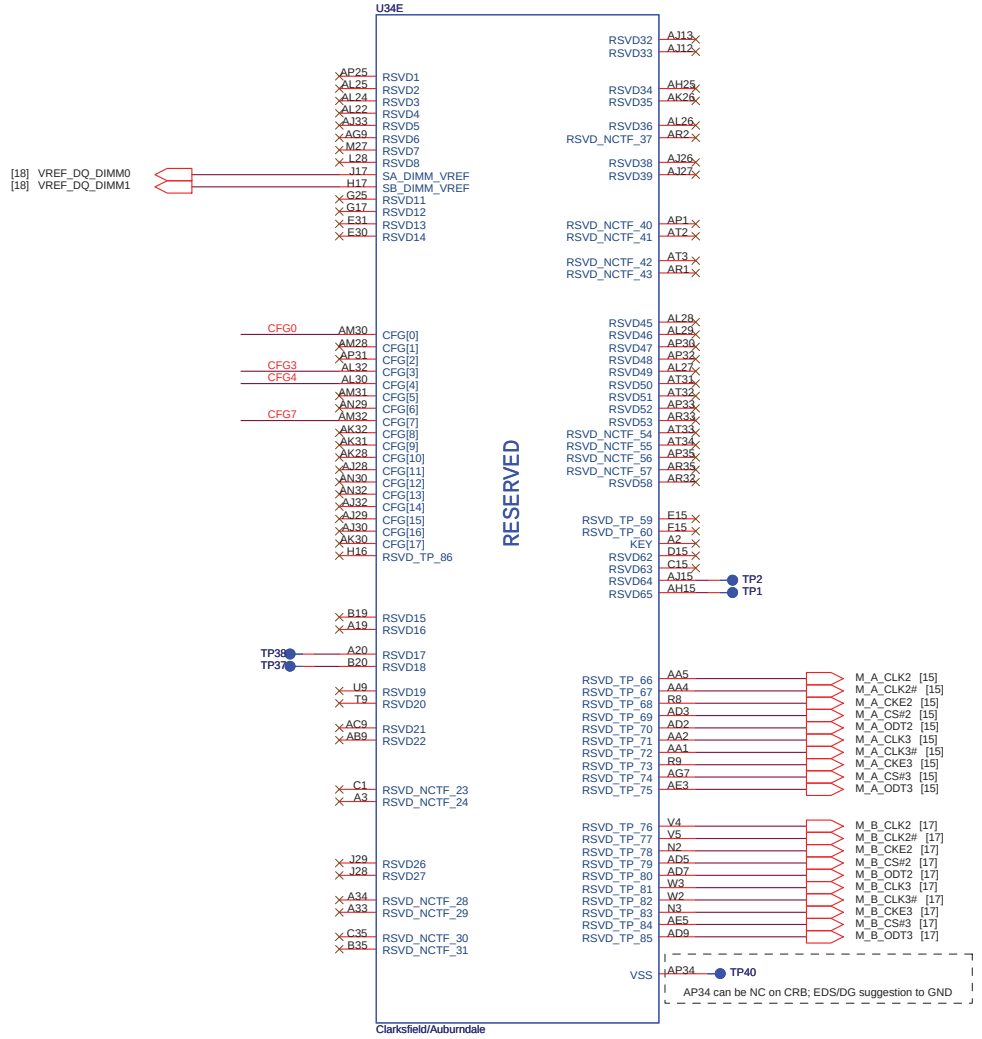


AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

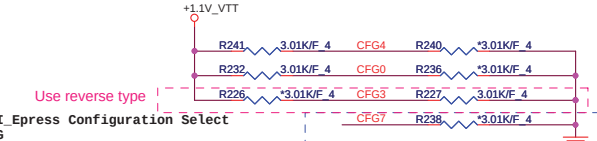


AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



Processor Strapping

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed



CFG[1:0] - PCI_Epress Configuration Select
* 11= 1 x 16 PEG
* 10= 2 x 8 PEG

S: The CFG signals have a default value of '1' if not terminated on the board.

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.(ES1 only)

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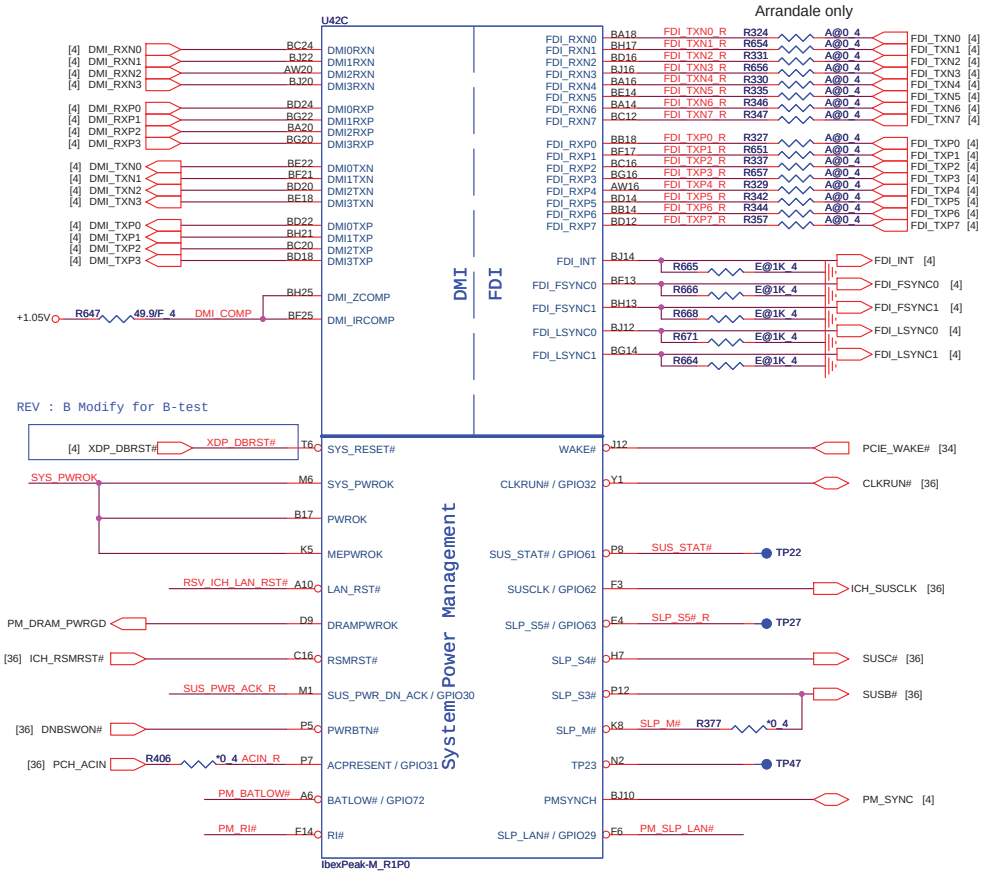
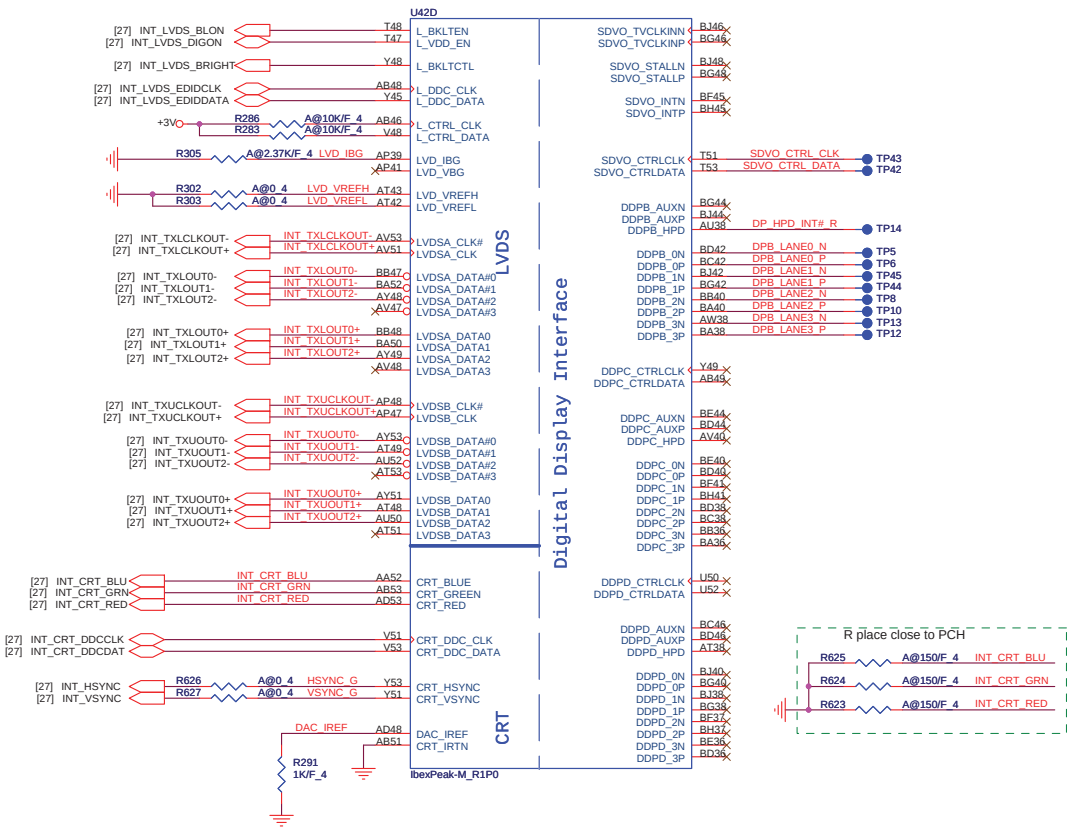
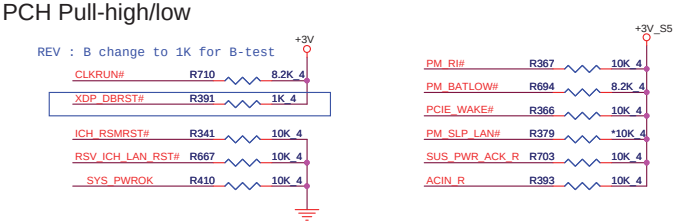
IBEX PEAK-M (DMI,FDI,GPIO)



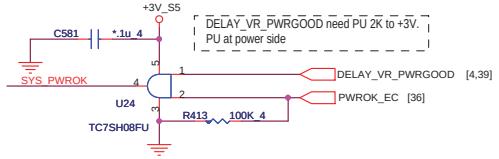
IBEX PEAK-M (LVDS,DDI)



PCH Pull-high/low



System PWR_OK



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	IBEX PEAK-M 1/6	1A

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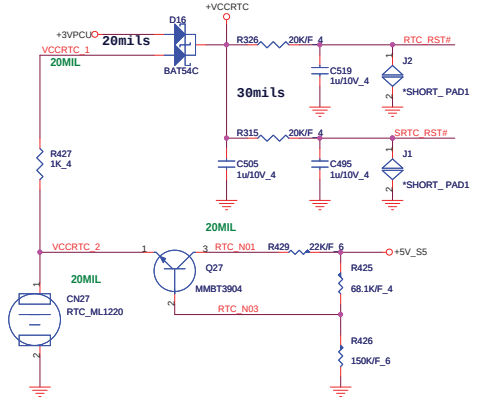
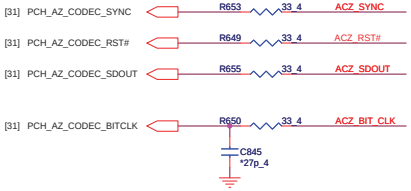
RTC Circuitry

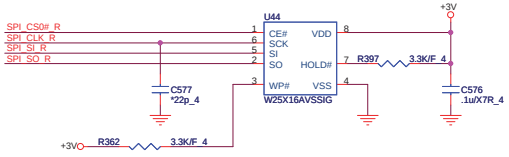


HDA Bus



Place all series terms close to PCH except for SDIN input lines,which should be close to source.Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

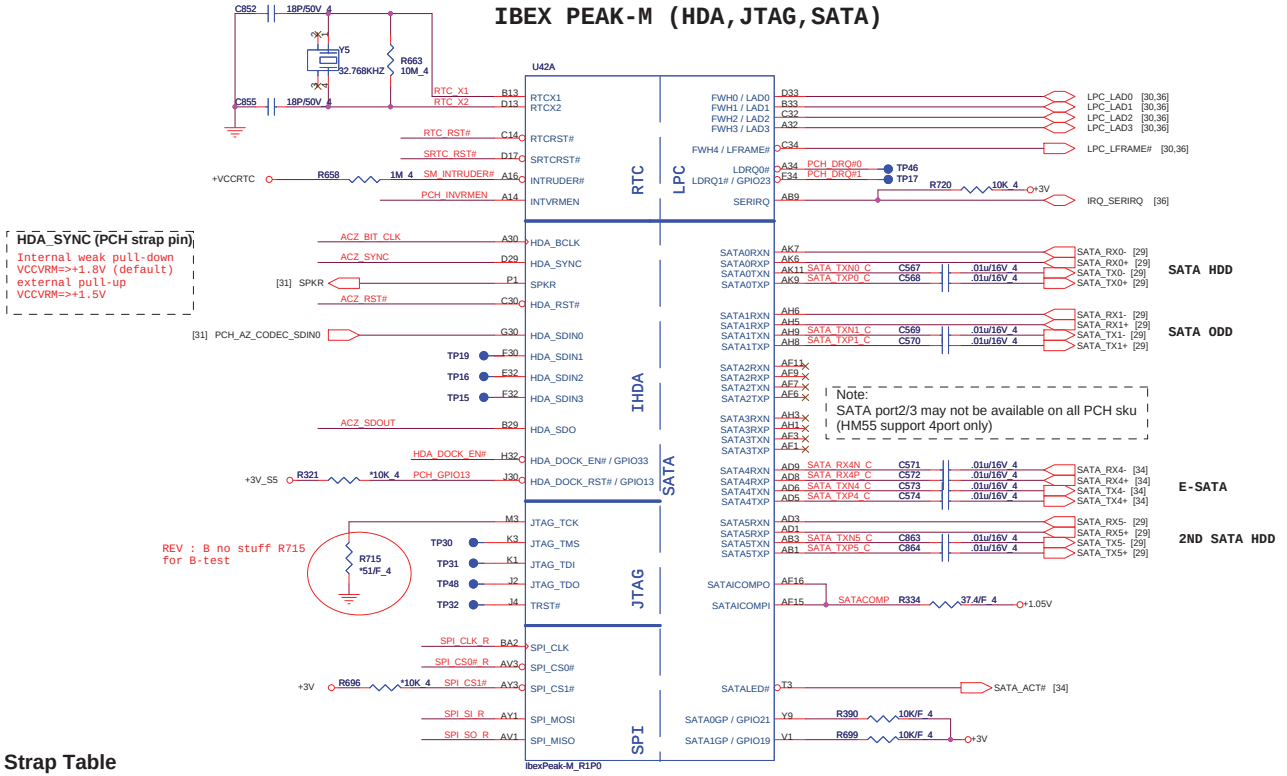
PCH SPI



At 11/24 add

Winbond W25X16AVSSIG		AKE38ZP0N01
EON	EN25F16-100HIP	AKE38ZA0Q00
AMIC	A25L016	AKE38ZN0800

IBEX PEAK-M (HDA,JTAG,SATA)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	ZY9B note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V R725 *10K_4 SPKR
INIT3_3V	Reserved	PWROK	1 = Default (weak pull-up 20K) Should not be pull-down	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R274 *10K_4 PCI_GNT3# [10]
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+VCCRTC R660 330K_4 PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location: 1 / 1 / SPI 1 / 0 / PCI 0 / 0 / LPC	Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS] +3V R288 *1K_4 R290 *1K_4 R287 1K_4 R301 1K_4 PCI_GNT0# [10] PCI_GNT1# [10]
GNT0#	Boot BIOS Selection 0 [bit-0]	PWROK		
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 32ohm)	+1.8V R695 *1K_4 NV_ALE NV_ALE [10]
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 32ohm	+1.8V R692 *1K_4 NV_CLE NV_CLE [10]
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	+3V R311 *1K_4 R309 *10K_4 HDA_DOCK_EN#
SPI_MOSI	iTPM function Disable	MEPWROK	0 = Default (weak pull-down 20K) 1 = Enable	+3V R398 *1K_4 SPI_SI_R
HDA_SDO	Reserved	RSMRST#	Should not be pull-up (weak pull-down 20K)	
GPIO8	Reserved	RSMRST#	Should not be pull-down (weak pull-up 20K)	+3V_S5 R382 10K_4 RSV_GPIO8 [11]
GPIO27	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (weak pull-up 20K)	
HDA_SYNC	On-die PLL PWR supply select	RSMRST#	0 = 1.8V supply (weak pull-down 20K) 1 = 1.5V supply	use defaul (0 = 1.8V supply)
GPIO15	Reserved	RSMRST#	0 = TLS no Confidentiality 1 = TLS Confidentiality	+V R392 1K_4 [illegible] [11]

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

Boot BIOS Strap		
GNT0#	GNT1#	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

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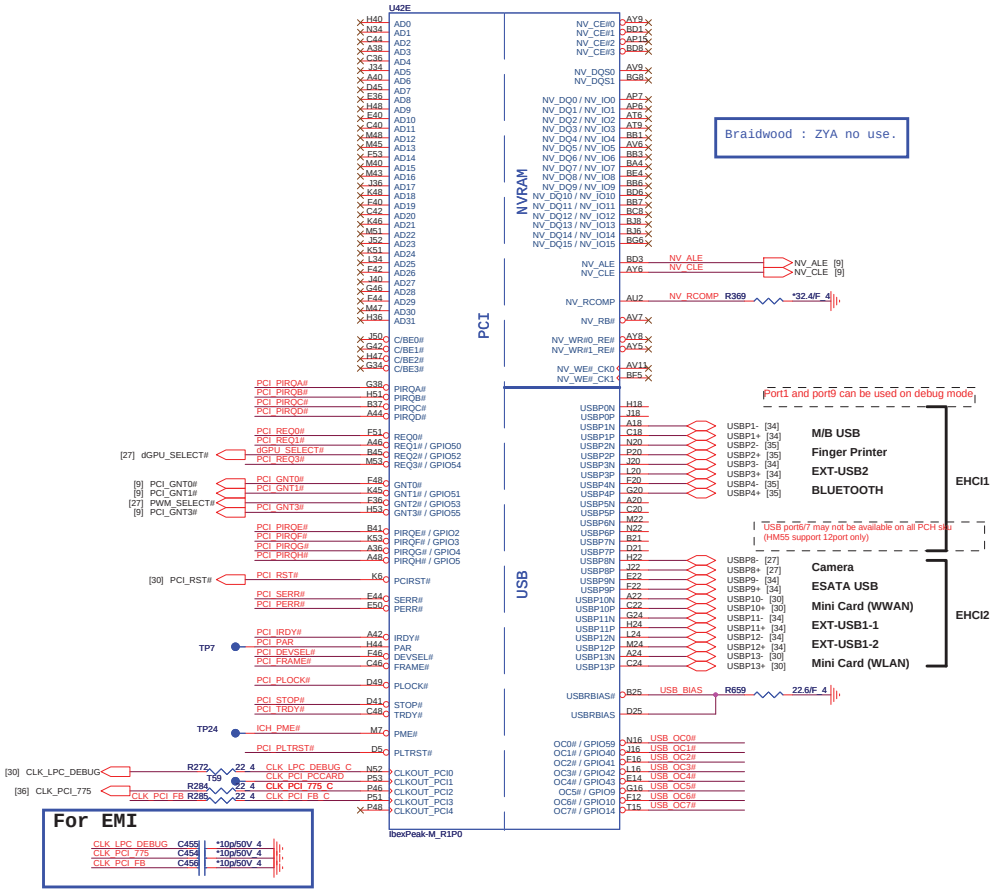
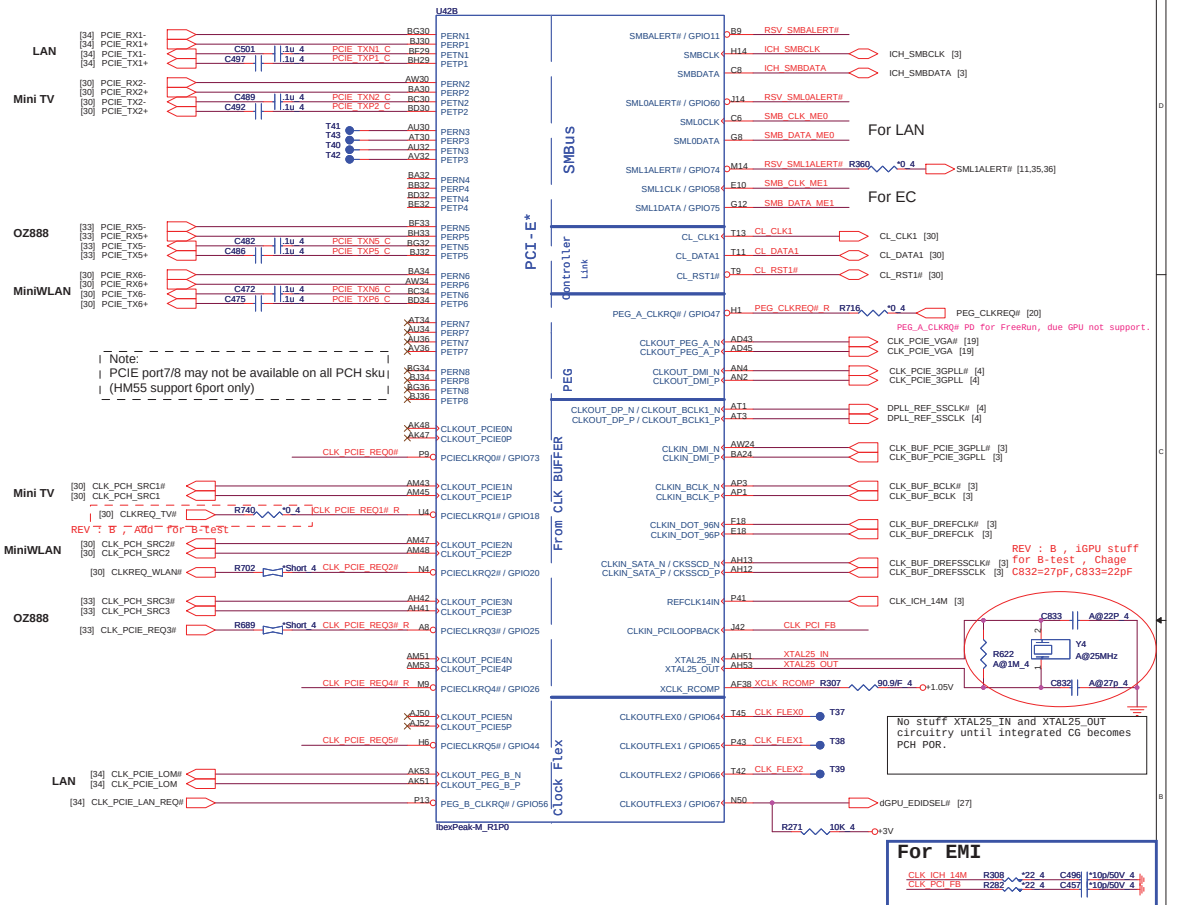
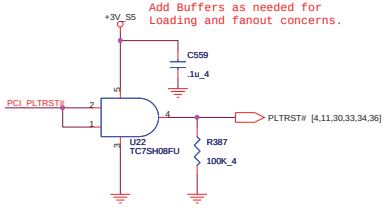
IBEX PEAK-M (PCI,USB,NVRAM)



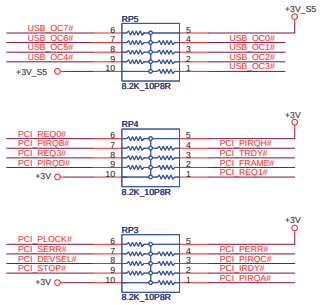
IBEX PEAK-M (PCI-E,SMBUS,CLK)



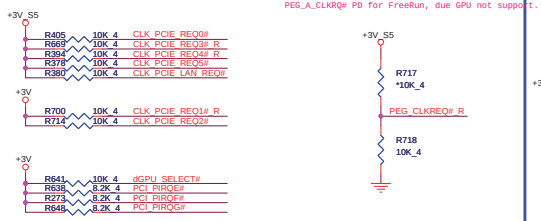
PLTRST#



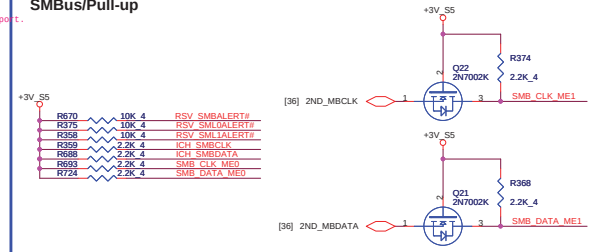
PCI/USBOC# Pull-up



CLK_REQ/Strap Pin



SMBus/Pull-up



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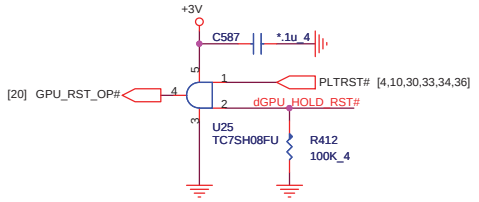
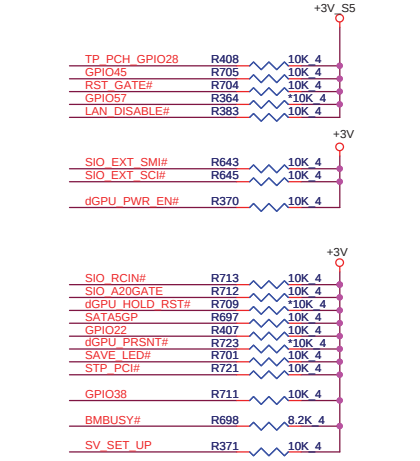
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

SATA5GP / GPIO49 / TEMP_ALERT# is used to alert for EC when CPU or Graph/Memory controllers' temperature go out of limit. So connecting GPIO49 to EC and avoid this pin to be used for other purpose

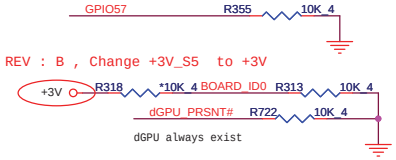
GPU RST#



GPIO Pull-up/Pull-down



SV_SET_UP	1-X High = Strong (Default)



Integrated Clock Chip Enable	
BOARD_ID0	High = Discrete Low = SW
RSV_GPIO8	High = Disable Low = Enable

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	IBEX PEAK-M 4/6	1A
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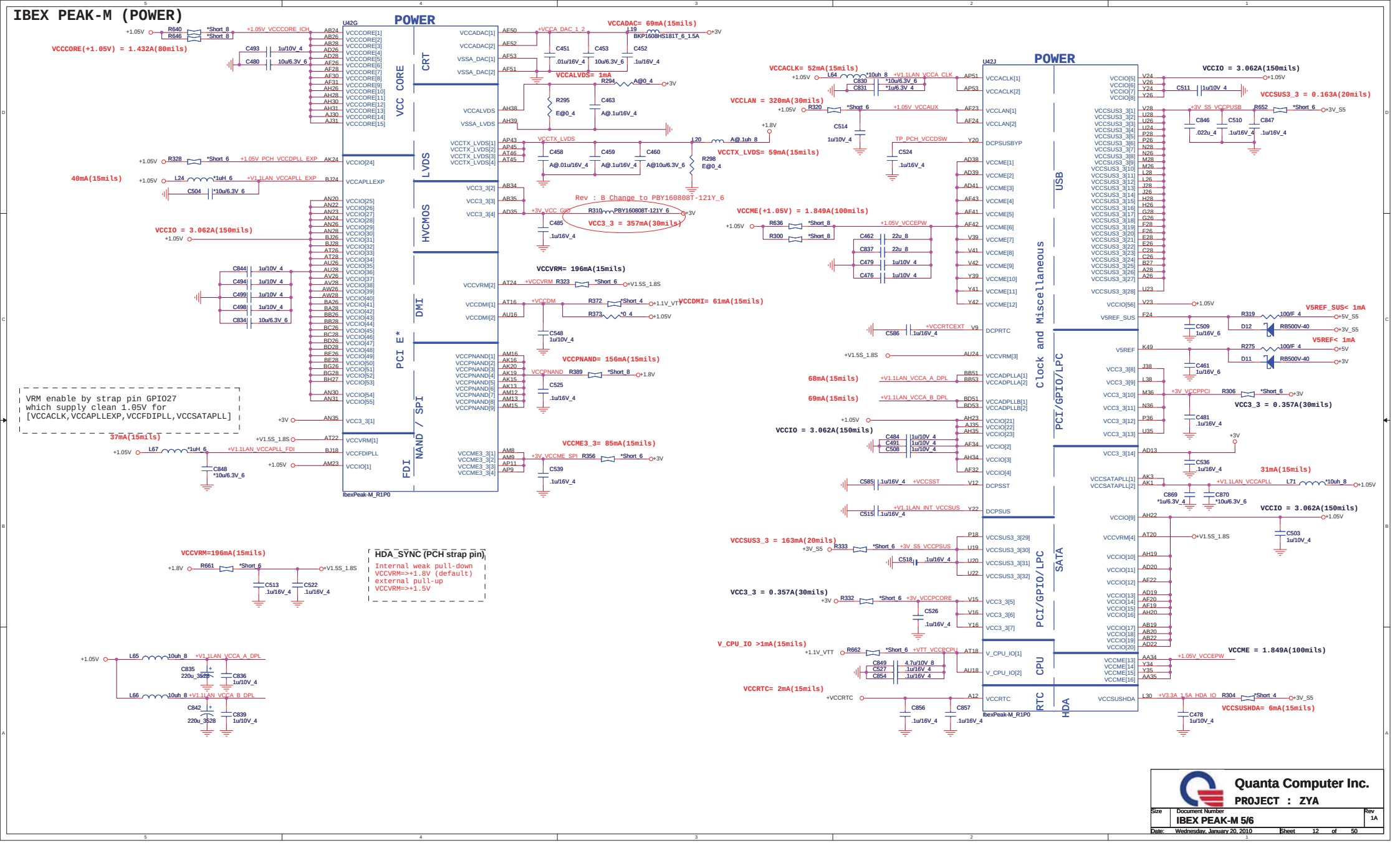
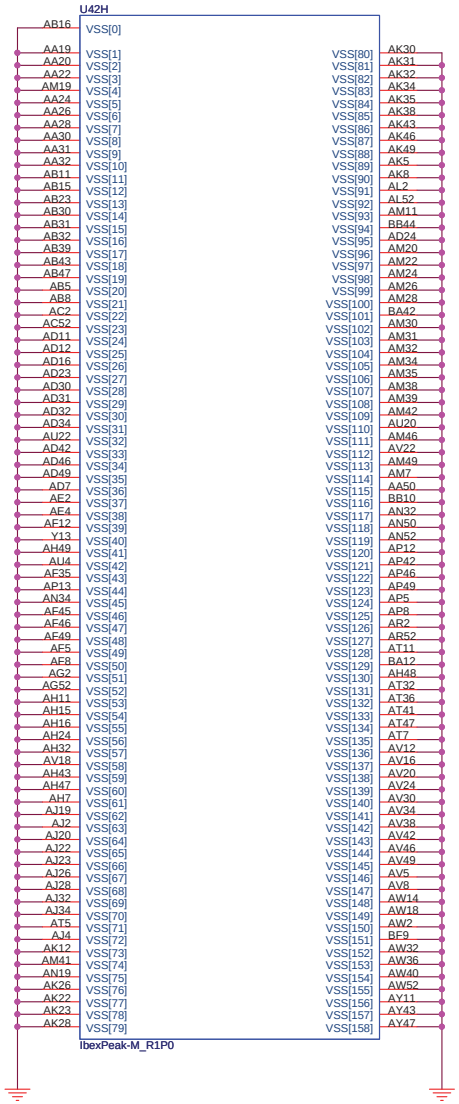
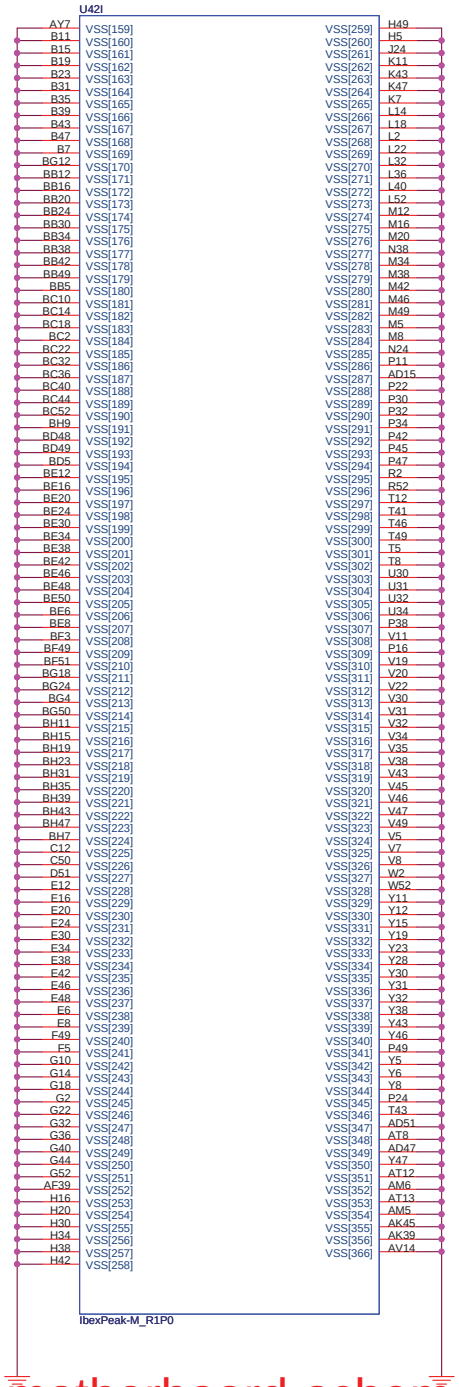


IBEX PEAK-M (GND)





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Size	Document Number	Rev
	IBEX PEAK-M 6/6	1A
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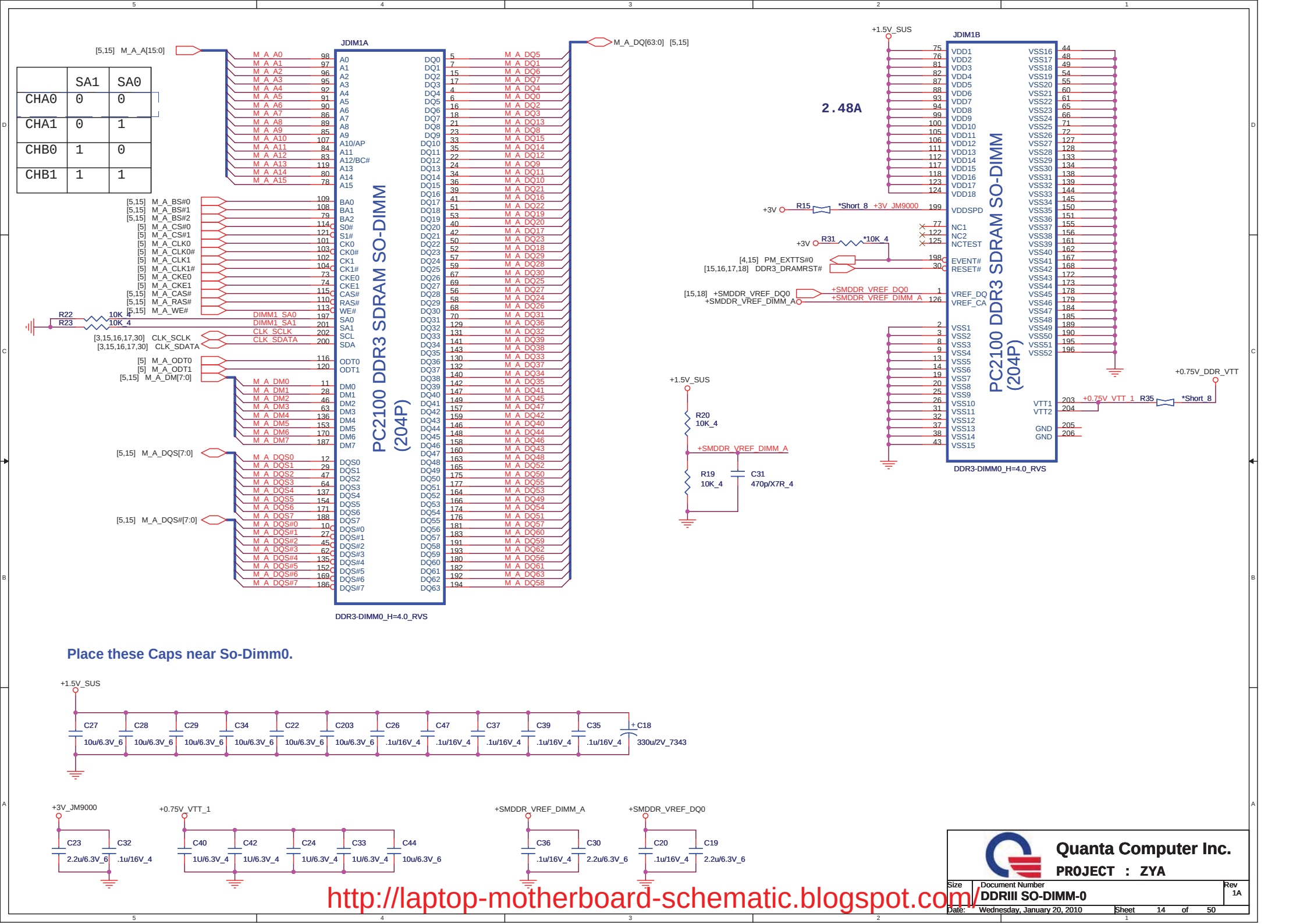
JDIM1A
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM0_H=4.0_RVS
JDIM1B
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM0_H=4.0_RVS
2.48A
SA1 SA0
CHA0 0 0
CHA1 0 1
CHB0 1 0
CHB1 1 1
Place these Caps near So-Dimm0.
+1.5V_SUS
+3V_JM9000
+0.75V_VTT_1
+SMDDR_VREF_DIMM_A
+SMDDR_VREF_DQ0
+0.75V_DDR_VTT
Quanta Computer Inc.
PROJECT : ZYA
Document Number DDRIII SO-DIMM-0
Rev 1A
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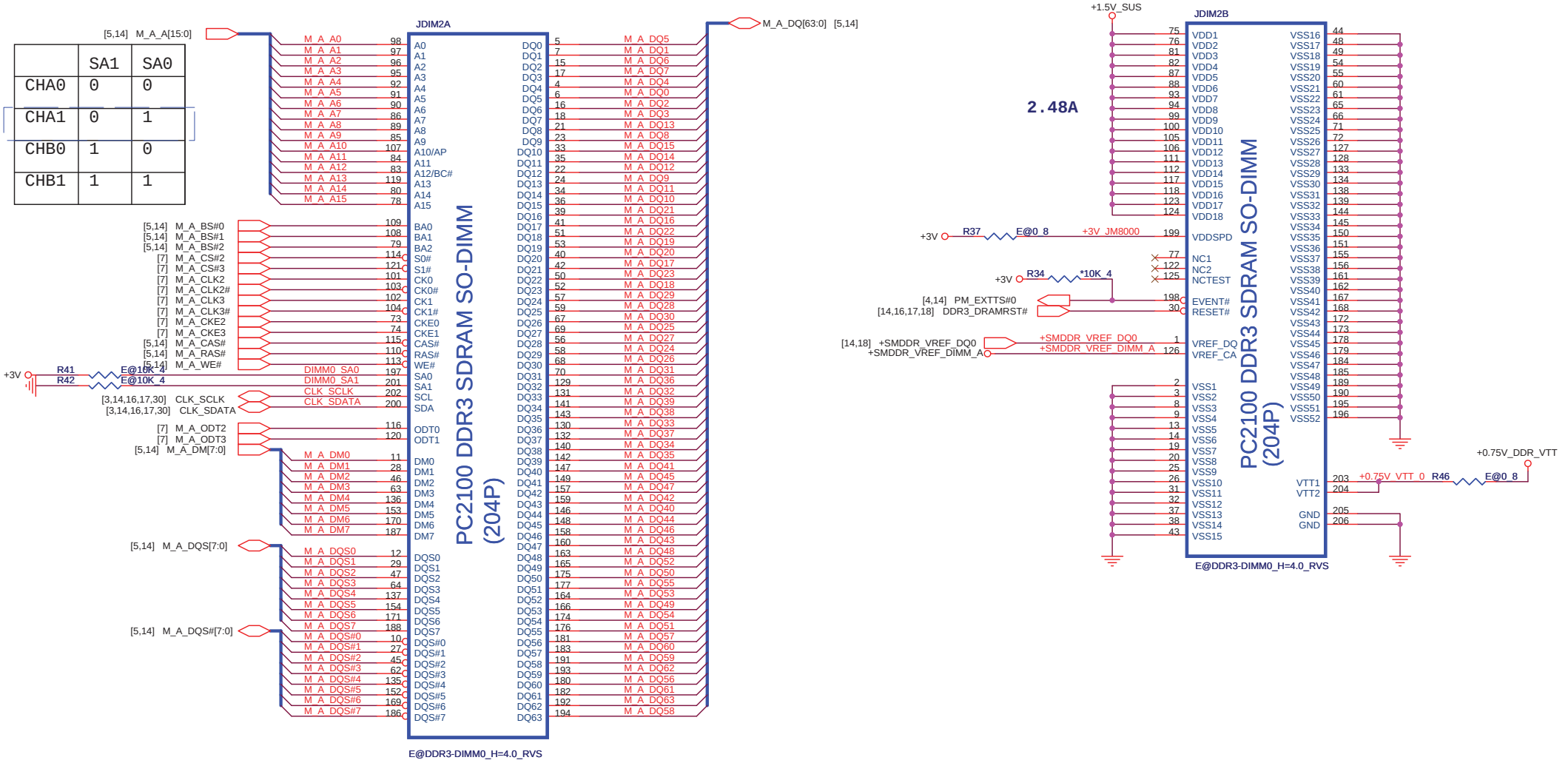
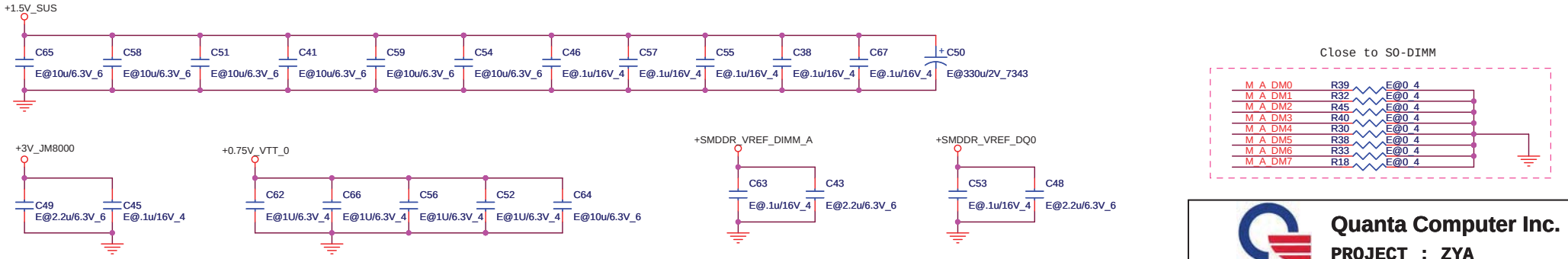
http://laptop-motherboard-schematic.blogspot.com/

	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1



Place these Caps near So-Dimm0.



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Size	Document Number	Rev
	DDRIII SO-DIMM-0	1A
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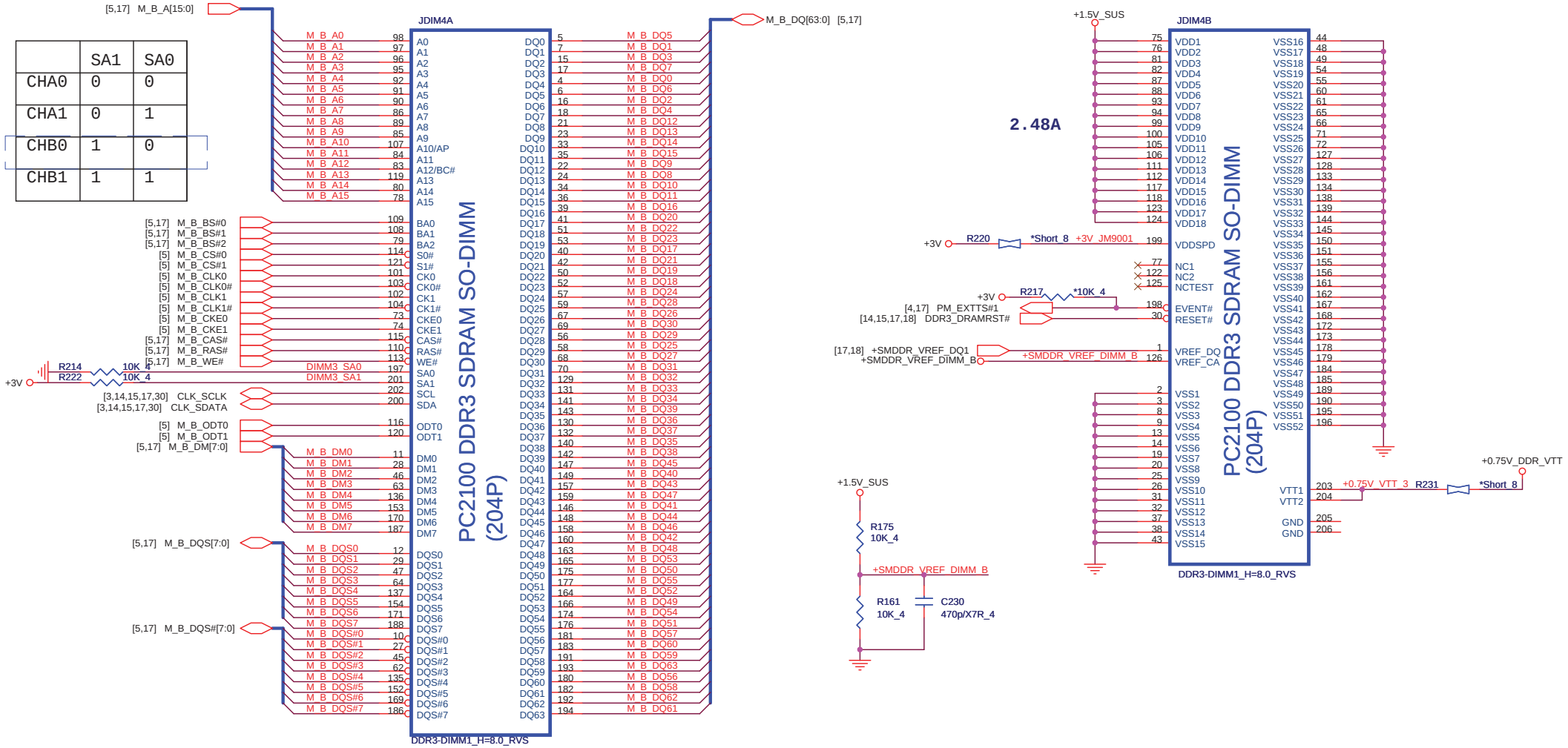
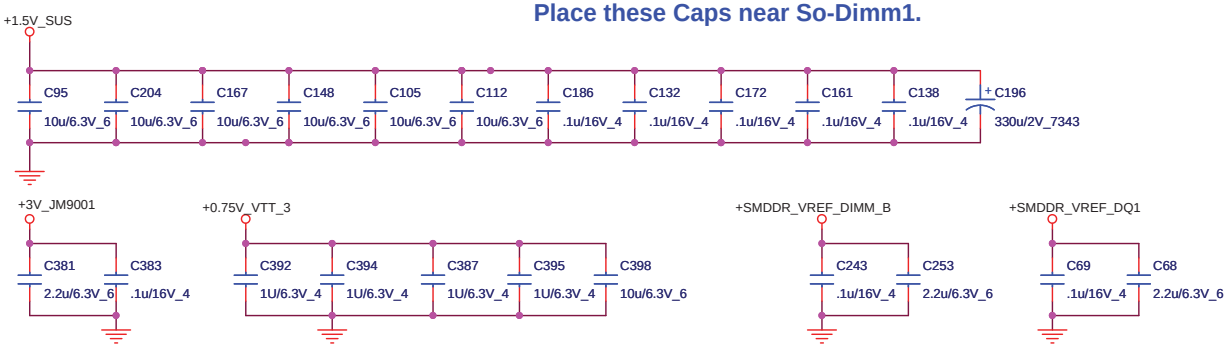


	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

Place these Caps near So-Dimm1.



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Size	Document Number	Rev
	DDRIII SO-DIMM-1	1A

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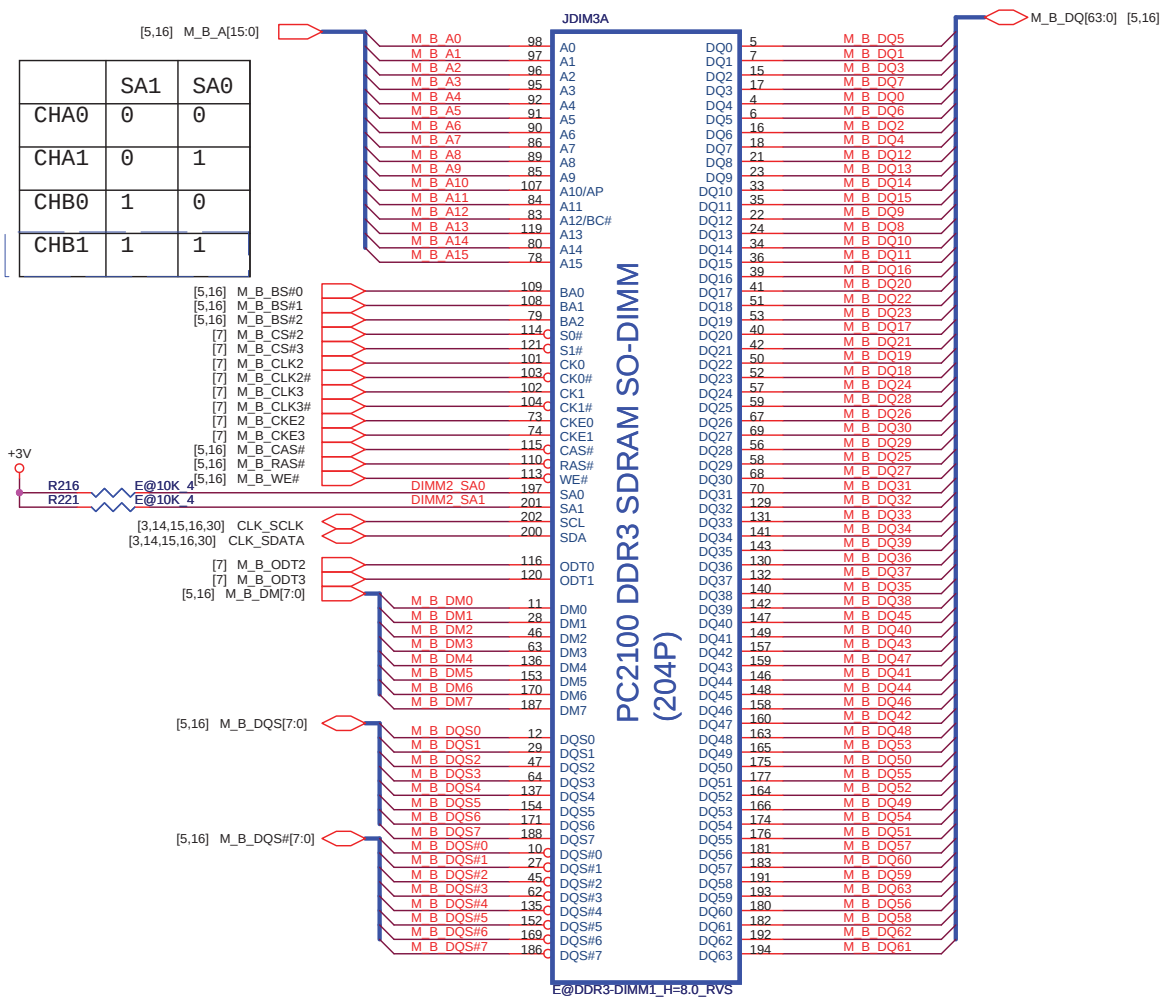
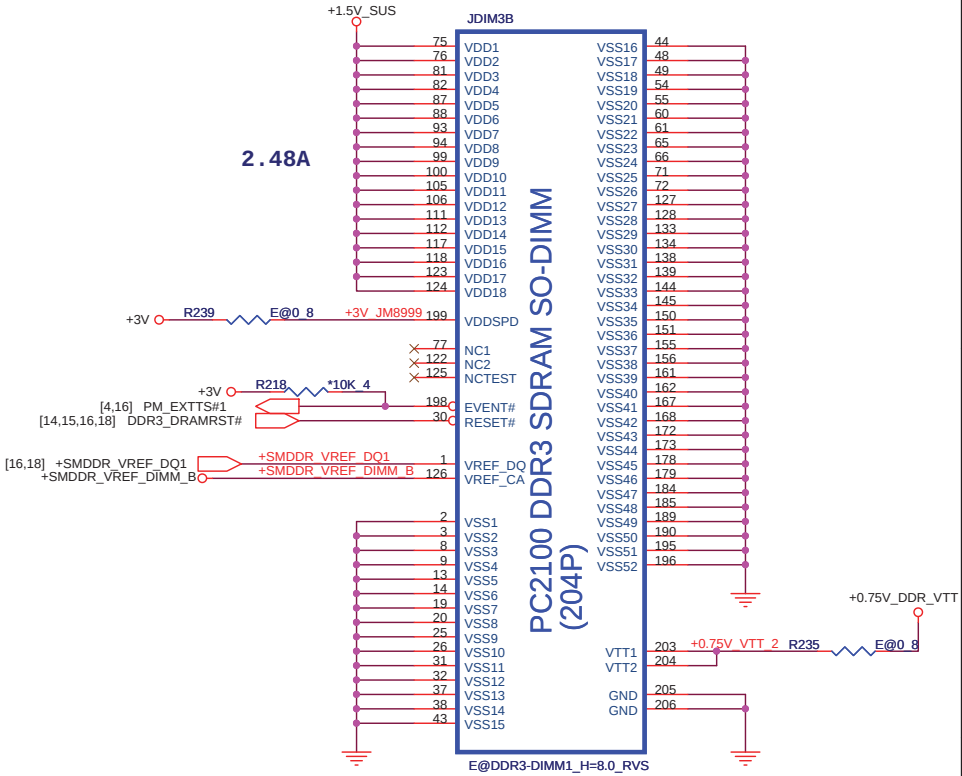
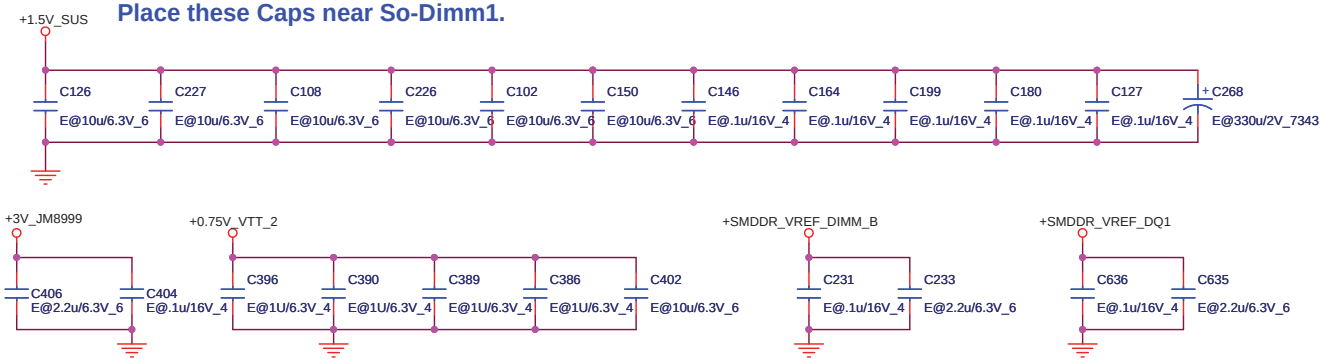
	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

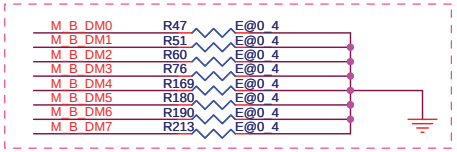




Place these Caps near So-Dimm1.



Close to SO-DIMM



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	DDRIII SO-DIMM-1	1A
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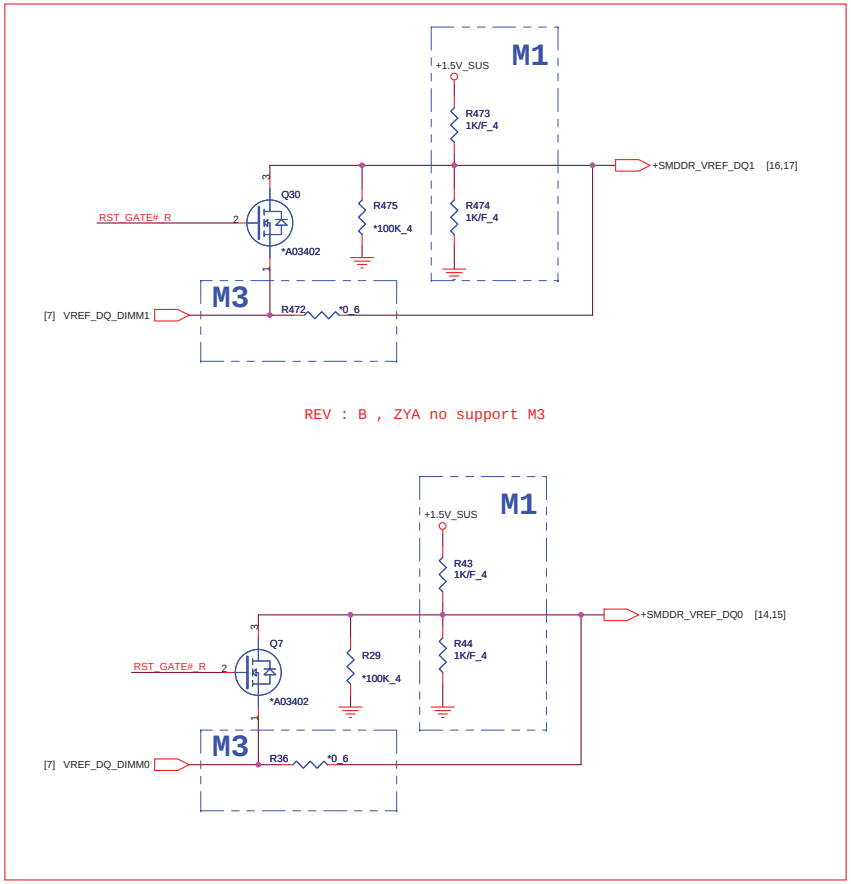
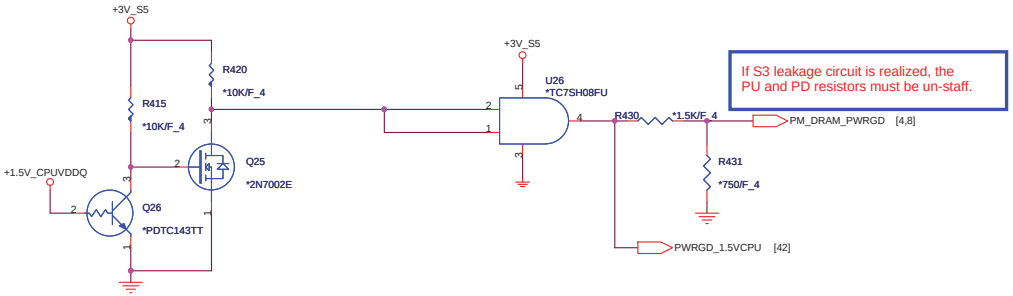
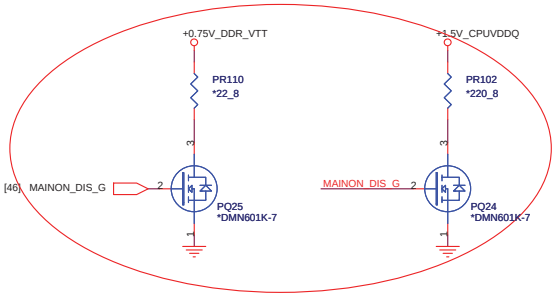
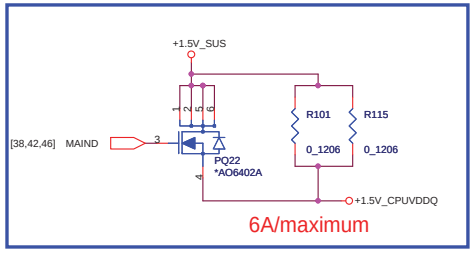
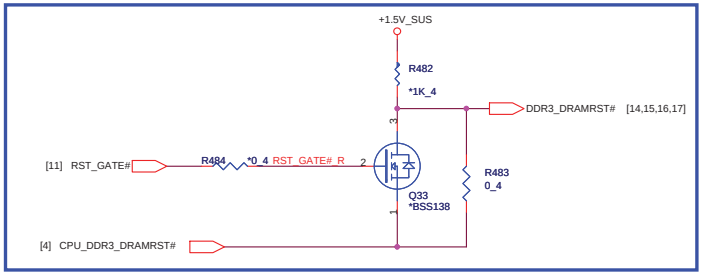




REV : B , No stuff for B-test







Quanta Computer Inc.
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Size	Document Number	Rev
	XDP	1A

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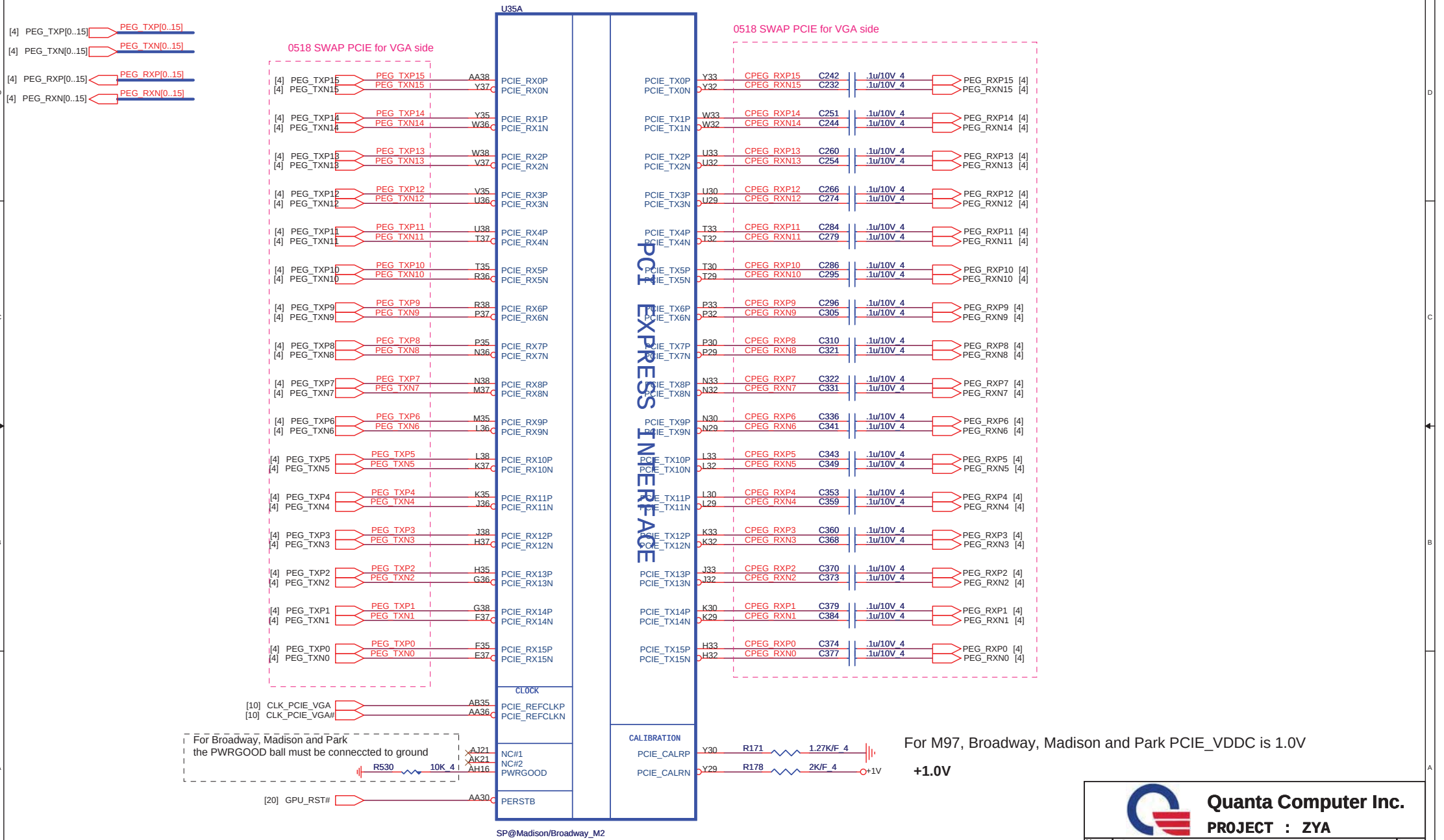

GPU Power-on sequence

1 => +3V_D
2 => +VGPU_CORE
3 => +VGPU_IO
4 => +1V
5 => +1.5V_GPU
6 => +1.8V_GPU
7 => dGPU_PWROK

1.8V GPIO

3.3V GPIO

U35B

MUTI GFX

DVPCNTL_MVP_0
DVPCNTL_MVP_1
DVPCNTL_0
DVPCNTL_1
DVPCNTL_2
DVPCLK
DVPDATA_0
DVPDATA_1
DVPDATA_2
DVPDATA_3
DVPDATA_4
DVPDATA_5
DVPDATA_6
DVPDATA_7
DVPDATA_8
DVPDATA_9
DVPDATA_10
DVPDATA_11
DVPDATA_12
DVPDATA_13
DVPDATA_14
DVPDATA_15
DVPDATA_16
DVPDATA_17
DVPDATA_18
DVPDATA_19
DVPDATA_20
DVPDATA_21
DVPDATA_22
DVPDATA_23

[24] RAM_STRAP0
[24] RAM_STRAP1
[24] RAM_STRAP2
T44

DPA
TXCAP_DPA3P AU24 — EXT_HDMICLK+ [28]
TXCAM_DPA3N AV23 — EXT_HDMICLK- [28]
TX0P_DPA2P AT25 — EXT_HDMITX0P [28]
TX0M_DPA2N AR24 — EXT_HDMITX0N [28]
TX1P_DPA1P AU26 — EXT_HDMITX1P [28]
TX1M_DPA1N AV25 — EXT_HDMITX1N [28]
TX2P_DPA0P AT27 — EXT_HDMITX2P [28]
TX2M_DPA0N AR26 — EXT_HDMITX2N [28]

DPB
TXCBP_DPB3P AR39
TXCBM_DPB3N AT39
TX3P_DPB2P AV31
TX3M_DPB2N AU30
TX4P_DPB1P AR32
TX4M_DPB1N AT31
TX5P_DPB0P AT33
TX5M_DPB0N AU32

DPC
TXCCP_DPC3P AU14 — T50
TXCCM_DPC3N AV13 — T47
TX0P_DPC2P AT15 — T51
TX0M_DPC2N AR14 — T52
TX1P_DPC1P AU16 — T53
TX1M_DPC1N AV15 — T45
TX2P_DPC0P AT17 — T49
TX2M_DPC0N AR16 — T46

DPD
TXCDP_DPD3P AU29
TXCDM_DPD3N AT19
TX3P_DPD2P AT21
TX3M_DPD2N AR29
TX4P_DPD1P AU22
TX4M_DPD1N AV21
TX5P_DPD0P AT23
TX5M_DPD0N AR22

U35G

LVDS CONTROL
VARY_BL AK27 — EV_LVDS_BRIGHT [27]
DIGON AJ27 — EV_LVDS_VDDEN [27]
TXCLK_UP_DPF3P AK35 — EV_TXUCLKOUT+ [27]
TXCLK_UN_DPF3N AL36 — EV_TXUCLKOUT- [27]
TXOUT_U0P_DPF2P AJ38 — EV_TXUOUT0+ [27]
TXOUT_U0N_DPF2N AK37 — EV_TXUOUT0- [27]
TXOUT_U1P_DPF1P AH35 — EV_TXUOUT1+ [27]
TXOUT_U1N_DPF1N AJ36 — EV_TXUOUT1- [27]
TXOUT_U2P_DPF0P AG38 — EV_TXUOUT2+ [27]
TXOUT_U2N_DPF0N AH37 — EV_TXUOUT2- [27]
TXOUT_U3P AF35
TXOUT_U3N AG36

LVTMDP
TXCLK_LP_DPE3P AP34 — EV_TXLCLKOUT+ [27]
TXCLK_LN_DPE3N AR34 — EV_TXLCLKOUT- [27]
TXOUT_L0P_DPE2P AW37 — EV_TXLOUT0+ [27]
TXOUT_L0N_DPE2N AU35 — EV_TXLOUT0- [27]
TXOUT_L1P_DPE1P AR37 — EV_TXLOUT1+ [27]
TXOUT_L1N_DPE1N AU39 — EV_TXLOUT1- [27]
TXOUT_L2P_DPE0P AP35 — EV_TXLOUT2+ [27]
TXOUT_L2N_DPE0N AR35 — EV_TXLOUT2- [27]
TXOUT_L3P AN36
TXOUT_L3N AP37

SP@Madison/Broadway_M2

I2C
SCL AK26
SDA AJ26
+3V_D
R104 10K/F_4
R105 10K/F_4

GENERAL PURPOSE I/O
GPIO_0 AH20 — [24] GPU_GPIO0
GPIO_1 AH18 — [24] GPU_GPIO1
GPIO_2 AN16 — [24] GPU_GPIO2
GPIO_3_SMBDATA AH23 — [24] GPIO3_SMBDAT
GPIO_4_SMBCLK AJ23 — [24] GPIO4_SMBCLK
GPIO_5_AC_BATT AH17 — [43] PWR_PSI#
GPIO_6 AJ17 — [44] IO_VID0
GPIO_7_BLON AK17 — [27] EV_LVDS_BLON
GPIO_8_ROMSO AJ13 — [24] SOUT_GPIO8
GPIO_9_ROMSI AH15 — [24] SIN_GPIO9
GPIO_10_ROMSCK AJ16 — [24] SCLK_GPIO10
GPIO_11 AK16 — [24] GPU_GPIO11
GPIO_12 AL16 — [24] GPU_GPIO12
GPIO_13 AM16 — [24] GPU_GPIO13
GPIO_14_HPD2 AM14 — T15 — [43] GPU_VID2
GPIO_15_PWRCNTL_0 AM13 — [43] GPU_VID1
GPIO_16_SSIN AK14 — [24] ALT#_GPIO17
GPIO_17_THERMAL_INT AC30
GPIO_18_HPD3 AN14 — T48 — [43] GPU_VID3
GPIO_19_CTF AM17
GPIO_20_PWRCNTL_1 AL13 — T11 — [24] SCS#_GPIO22
GPIO_21_BB_EN AJ14
GPIO_22_ROMCSB AK13
GPIO_23_CLKREQB AN13
JTAG_TRSTB AM23 — R152 B@10K/F_4 — GPIO24_TRSTB
JTAG_TDI AN23 — R14 *10K/F_4
JTAG_TCK AK23 — [3] 27M_CLK — 27M_CLK — T10
JTAG_TMS AL24 — R125 B@10K/F_4
JTAG_TDO AM24 — T8
GENERICA AJ19
GENERICB AK19
GENERICC AJ20
GENERICD AK20
GENERICE_HPD4 AJ24
GENERICF AH26
GENERICG AH24

For EMI
C193 *10p/50V_4 R154 *10K/F_4 27M_CLK

[28] EXT_HDMI_HPD
HPD1 AK24

VREFG AH13
+1.8V_GPU
R517 499/F_4
R529 249/F_4
C667 .1u_4

PLL/CLOCK
DPLL_PVDD AM32
DPLL_PVSS AN32
DPLL_VDDC AN31
XTALIN AV33
XTALOUT AU34
DPLUS AF29 — [24] GPU_D+
DMINUS AG29 — [24] GPU_D-
THERMAL
TS_FDO AK32
TSVDD AJ32
TSVSS AJ33
T17 — TS_VDD

DAC1
R AD39
RB AD37
G AE36
GB AD35
B AE37
BB AE38
EXT_CRT_RED [27]
EXT_CRT_GRN [27]
EXT_CRT_BLU [27]
HSYNC AC36 — EXT_HSYNC [24,27]
VSYNC AC38 — EXT_VSYNC [24,27]
R540 150/F_4
R541 150/F_4
R542 150/F_4
RSET AB34 R167 499/F_4
AVDD AD34
AVSSQ AE34
VDD1DI AC33
VSS1DI AC34

DAC2
R2 AC39
R2B AC31
G2 AD39
G2B AD31
B2 AE39
B2B AE31
C AC32
Y AD32
COMP AE32
H2SYNC AD29 — T19
V2SYNC AC29 — V2SYNC [24]
VDD2DI AG31
VSS2DI AG32
A2VDD AG33 — +3V_D (3.3V@130mA A2VDD)
A2VDDQ AD33
A2VSSQ AE33
C209 .1u/10V_4
R2SET AA29 R165 715/F_4

DDC/AUX
DDC1CLK AM26 — EV_HDMI_DDCCK [28]
DDC1DATA AN26 — EV_HDMI_DDCDAT [28] — HDMI
AUX1P AM27 — T16
AUX1N AL27 — T9
DDC2CLK AM19
DDC2DATA AL19 — Display Port
AUX2P AN20
AUX2N AM20 — T7
DDCCLK_AUX3P AL30 — T14
DDCDATA_AUX3N AM30
DDCCLK_AUX4P AL29
DDCDATA_AUX4N AM29
DDCCLK_AUX5P AN21 — EV_LVDS_DDCCLK [27] — LVDS
DDCDATA_AUX5N AM21 — EV_LVDS_DDCDAT [27]
DDC6CLK AJ30 — EV_CRTDCLK [27] — CRT
DDC6DATA AJ31 — EV_CRTDDAT [27]
NC_DDCCLK_AUX7P AK30
NC_DDCDATA_AUX7N AK29

SP@Madison/Broadway_M2

+3V_D
R496 *10K_4
R497 10K/F_4
R93 *10K_4
R103 *10K_4
[10] PEG_CLKREQ#

+1.8V_GPU
(1.8V@70mA AVDD)
AVDD — L15 BLM15BD121SN1_4 (120 ohm/300mA)
C210 .1u/10V_4
C211 1u/6.3V_4
C207 10u/6.3V_6
(1.8V@100mA VDD1DI)
VDD1DI — L8 BLM15BD121SN1_4 (120 ohm/300mA)
C123 .1u/10V_4
C122 1u/6.3V_4
C117 10u/6.3V_6
(1.8V@2mA A2VDDQ)
A2VDDQ — L12 BLM15BD121SN1_4 (120 ohm/300mA)
C188 .1u/10V_4
C189 1u/6.3V_4

+3V_D_ZY9B
C88 *.1u_4
U3 *74AHC125PW
GPIO24_TRSTB — R96 *7.5K_4 — C91 *100p/50V_6 — C85 *100p/50V_6 — R86 *7.5K_4
TESTEN [21]
[11] GPU_RST_OP#
R106 *Short_4
[19] GPU_RST#
R110 *7.5K_4
C93 *100p/50V_6

+1.8V_GPU
+1.8V(75mA) — L47 BLM15BD121SN1_4 (120 ohm/300mA) — DPLL_PVDD — C654 10u_6 — C676 1u_4 — C666 .1u_4
+1.0V(125mA) — L46 BLM15BD121SN1_4 (120 ohm/300mA) — DPLL_VDDC — C653 10u_6 — C665 1u_4 — C675 .1u_4
+1.8V(5mA) — L11 BLM15BD121SN1_4 (120 ohm/300mA) — TS_VDD — C173 10u_6 — C174 .1u_4

Change C612/C613 from 18p to 27p at B-test
C670 27p/50V_4 — Y3 27MHZ — C671 27p/50V_4 — R521 1M/F_4

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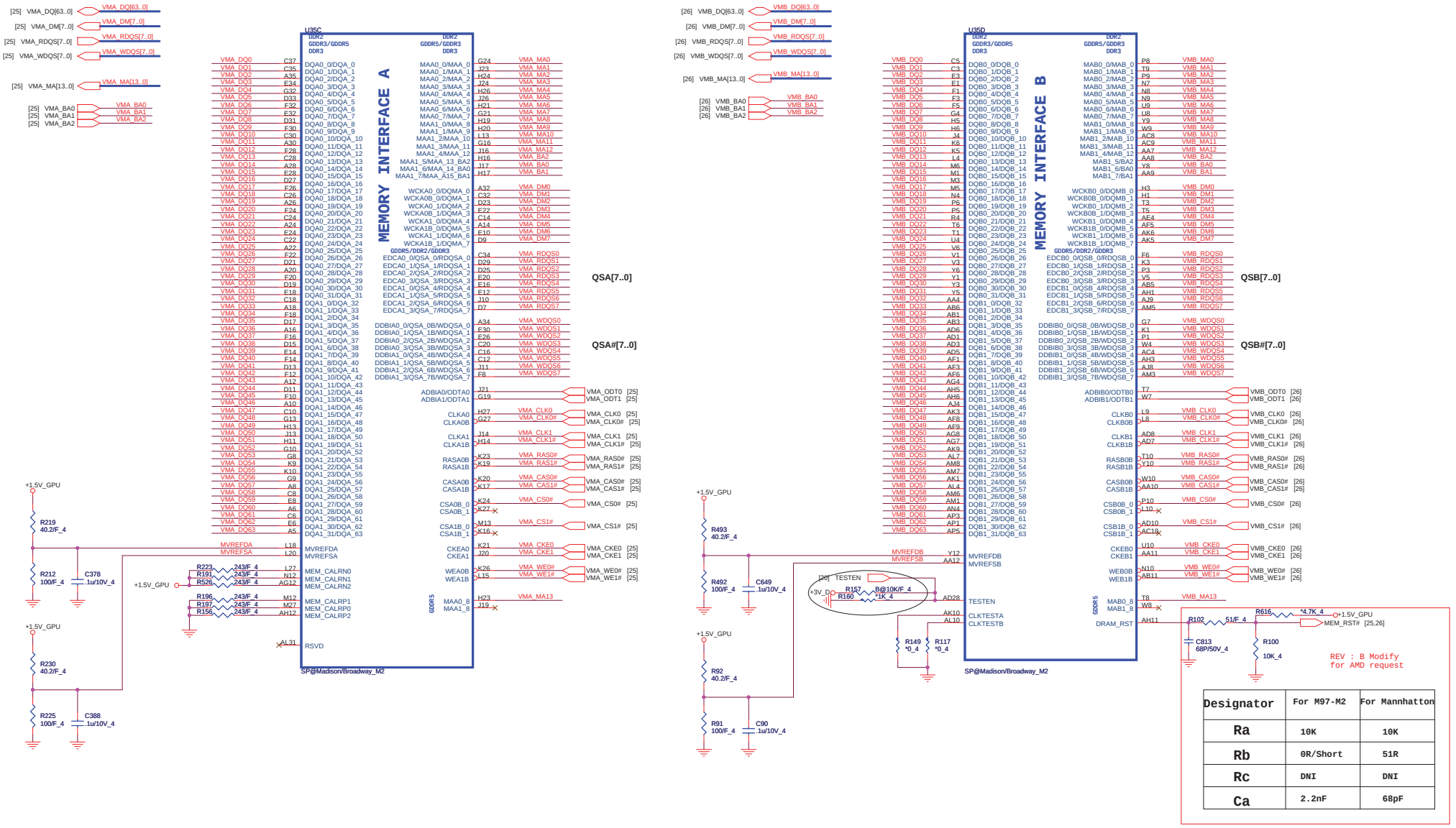

Designator	For M97-M2	For Mannhatton
Ra	10K	10K
Rb	0R/Short	51R
Rc	DNI	DNI
Ca	2.2nF	68pF

Quanta Computer Inc.
PROJECT : ZYA
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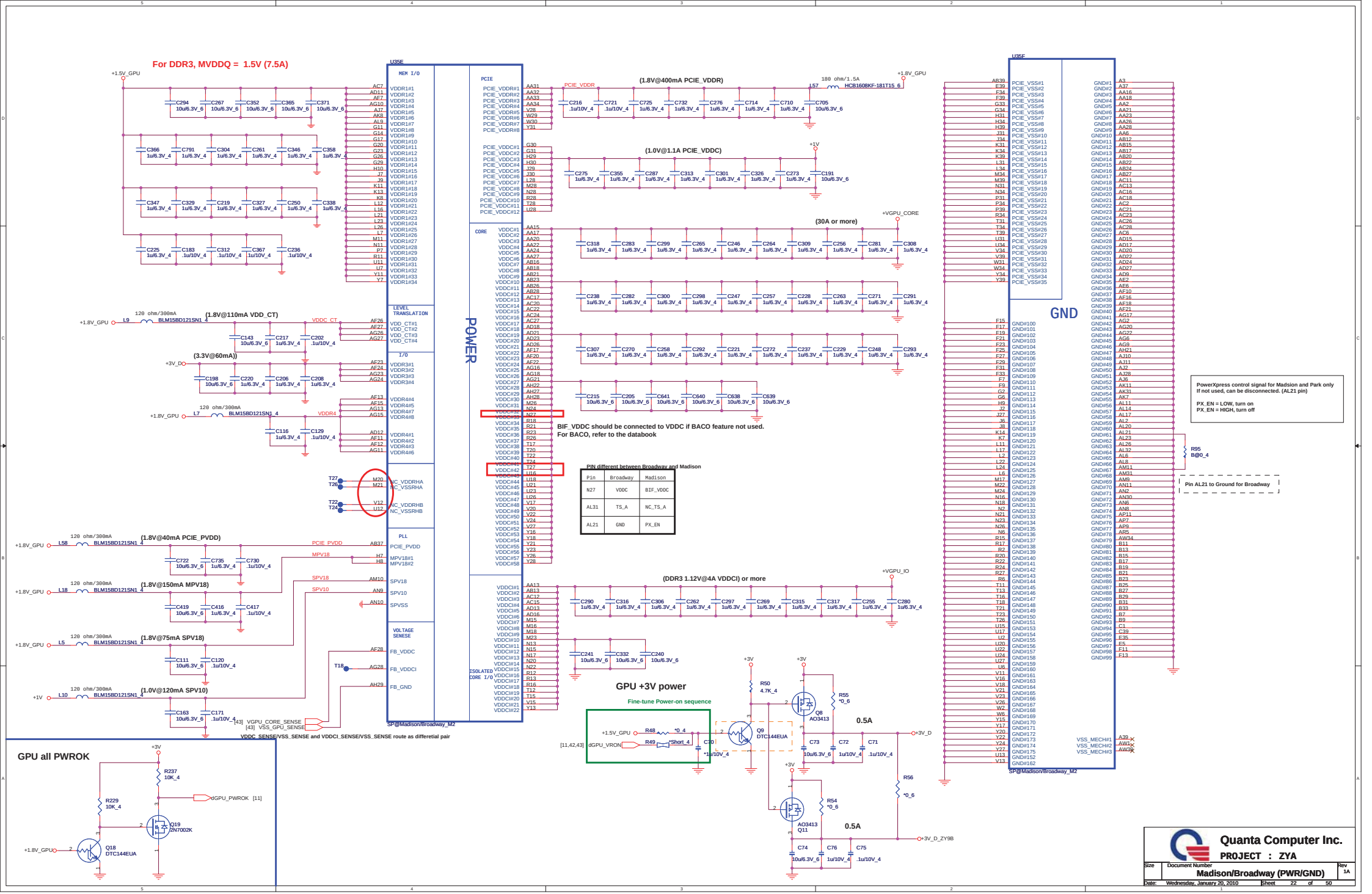
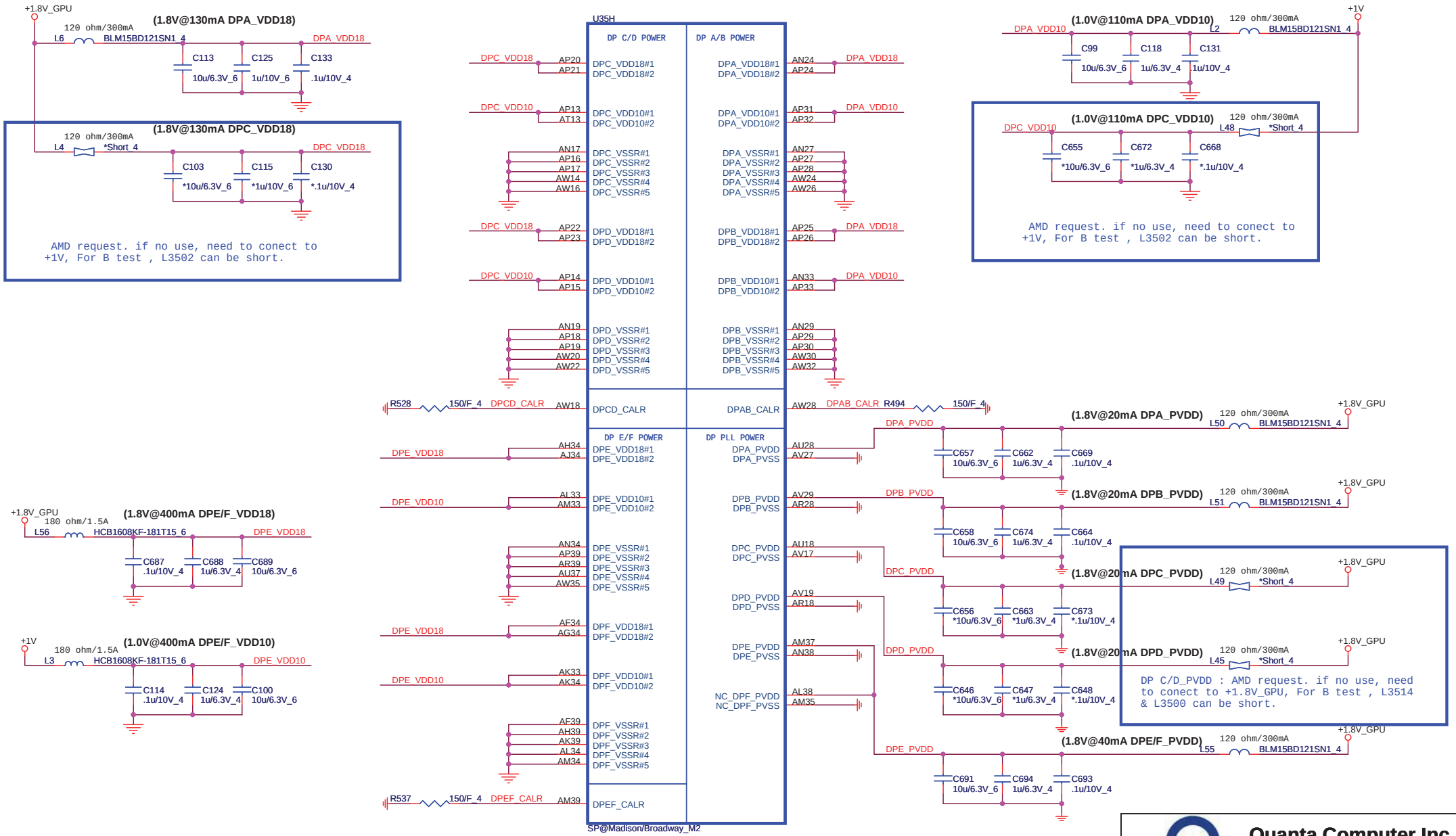
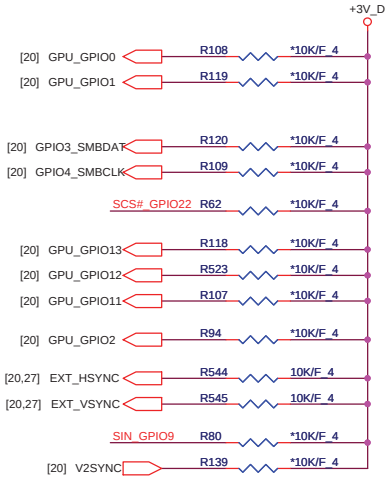
Madison/Broadway-MEM I/F
Date: Wednesday, January 20, 2010 | Sheet 21 of 50





PIN STRAPS



Memory Aperture size	
GPIO[13:11]	Size
000	128MB
001	256MB
010	64MB
011	32MB

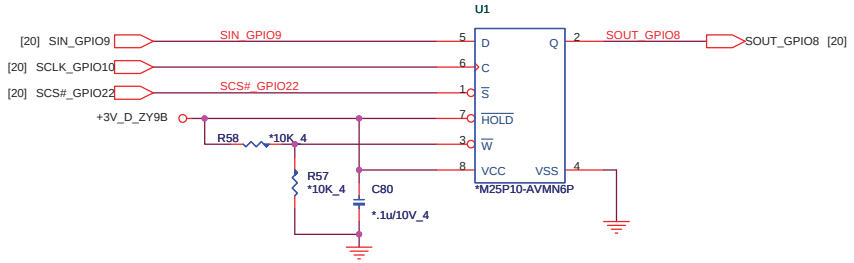
Audio Table		
EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by detect
1	0	DP only
1	1	Both DP & HDMI

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	000	See Memory Aperture size
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

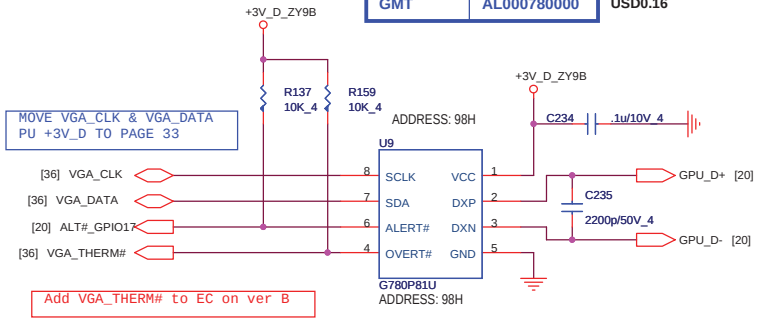
EEPROM



Thermal Sensor

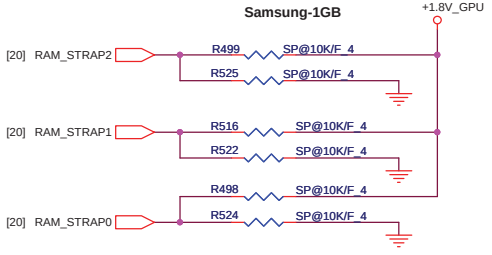
Vendor	P/N
WINDBOND	AL83L771K01
GMT	AL000780000

USD0.16



DDR3 VRAM SIZE Strap

DDR3 VRAM size						
Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	512MB	1	1	0
			1GB	1	0	0
			2GB	1	0	1
Samsung	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)				
			1GB	0	0	0
	K4W2G1646B-HC12	AKD5MGGT500	2GB	0	0	1
AMD	23EY2387MA-12	AKD5LGGT700	1GB	0	1	0

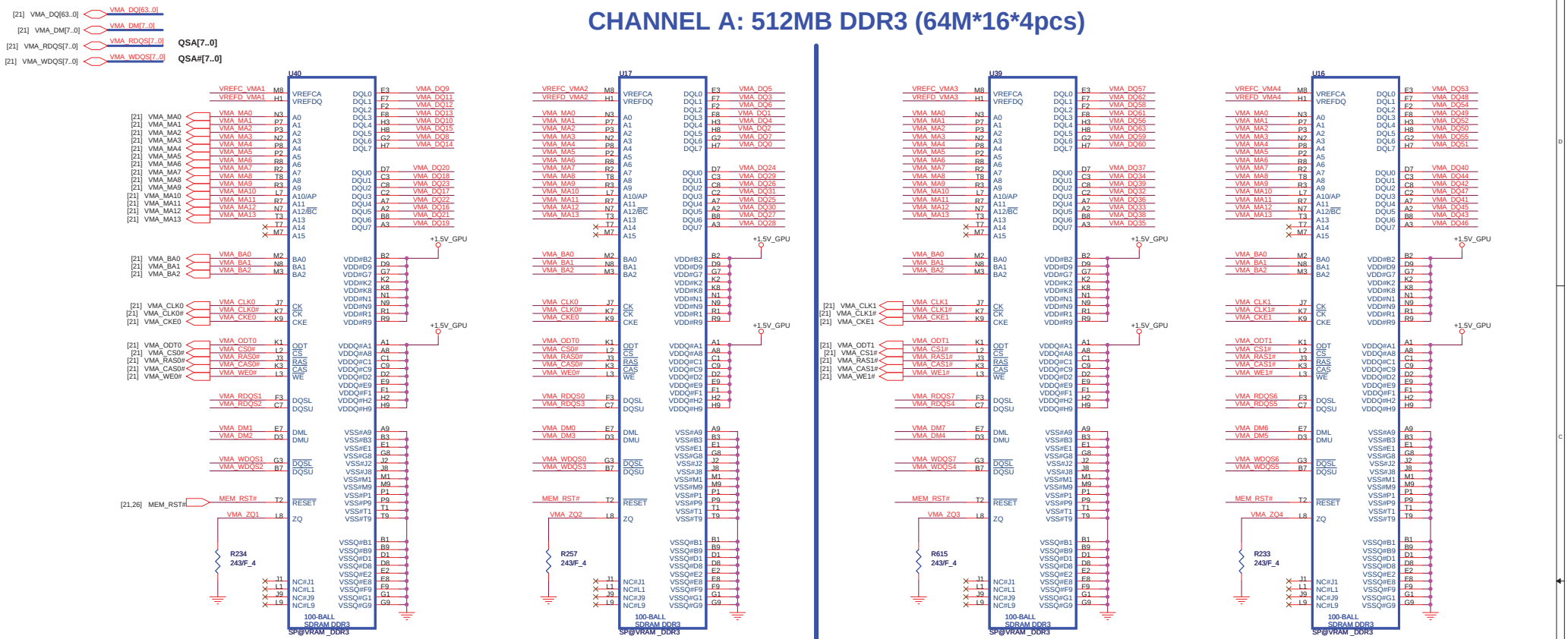


RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.

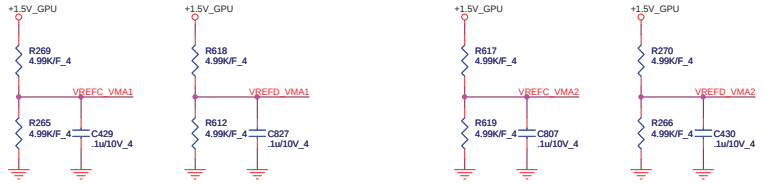
Quanta Computer Inc.
PROJECT : ZYA

Size	Document Number	Rev
	Strip/Thermal	1A
Date: Wednesday, January 20, 2010	Sheet 24 of 50	

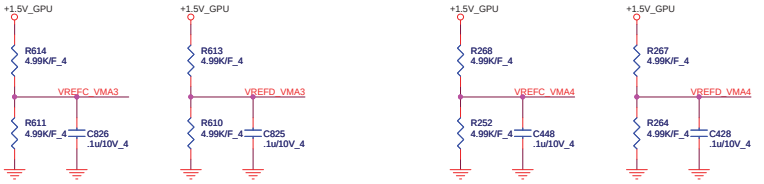
CHANNEL A: 512MB DDR3 (64M*16*4pcs)



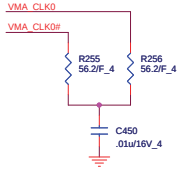
Group-A0 VREF



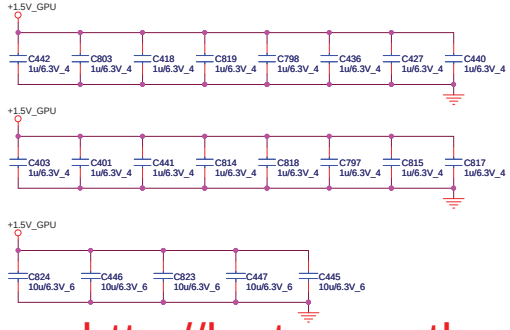
Group-A1 VREF



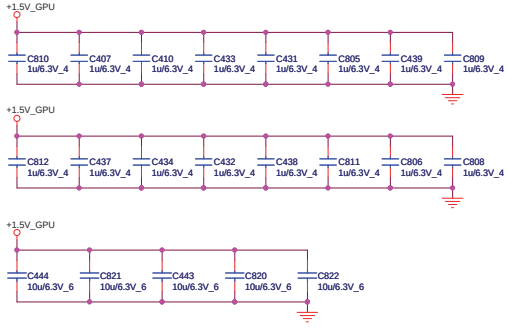
MEM_A0 CLK



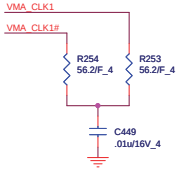
Group-A0 decoupling CAP



Group-A1 decoupling CAP



MEM_A1 CLK

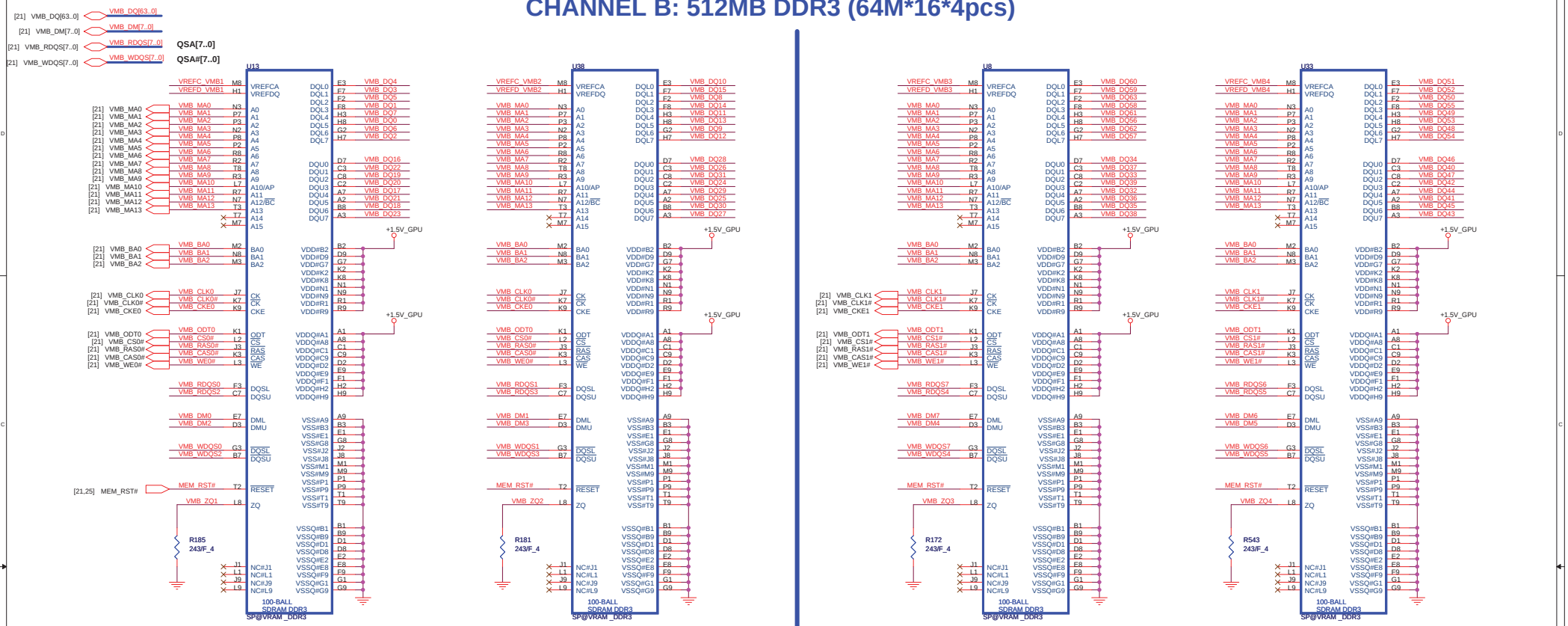


Quanta Computer Inc.
PROJECT : ZYA

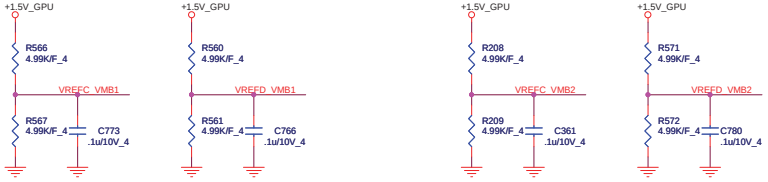
Size	Document Number	Rev
	MEMORY 1 channel A	1A

Date: Wednesday, January 20, 2010 Sheet 25 of 50

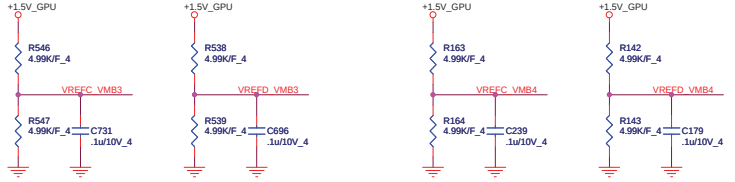
CHANNEL B: 512MB DDR3 (64M*16*4pcs)



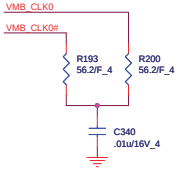
Group-B0 VREF



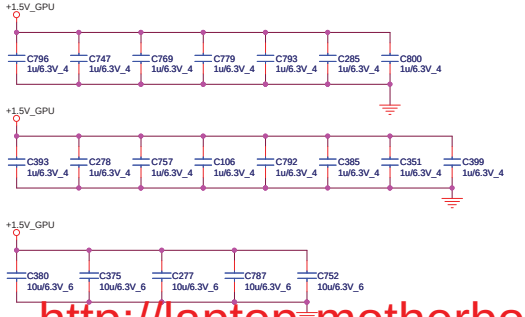
Group-B1 VREF



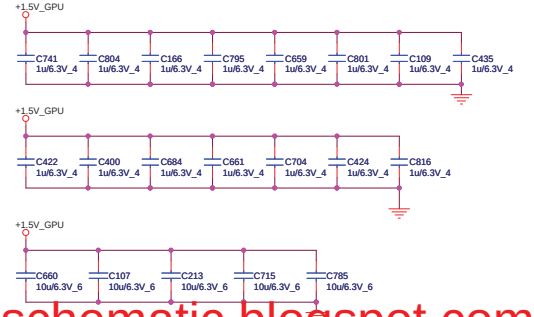
MEM_B0 CLK



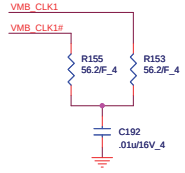
Group-B0 decoupling CAP



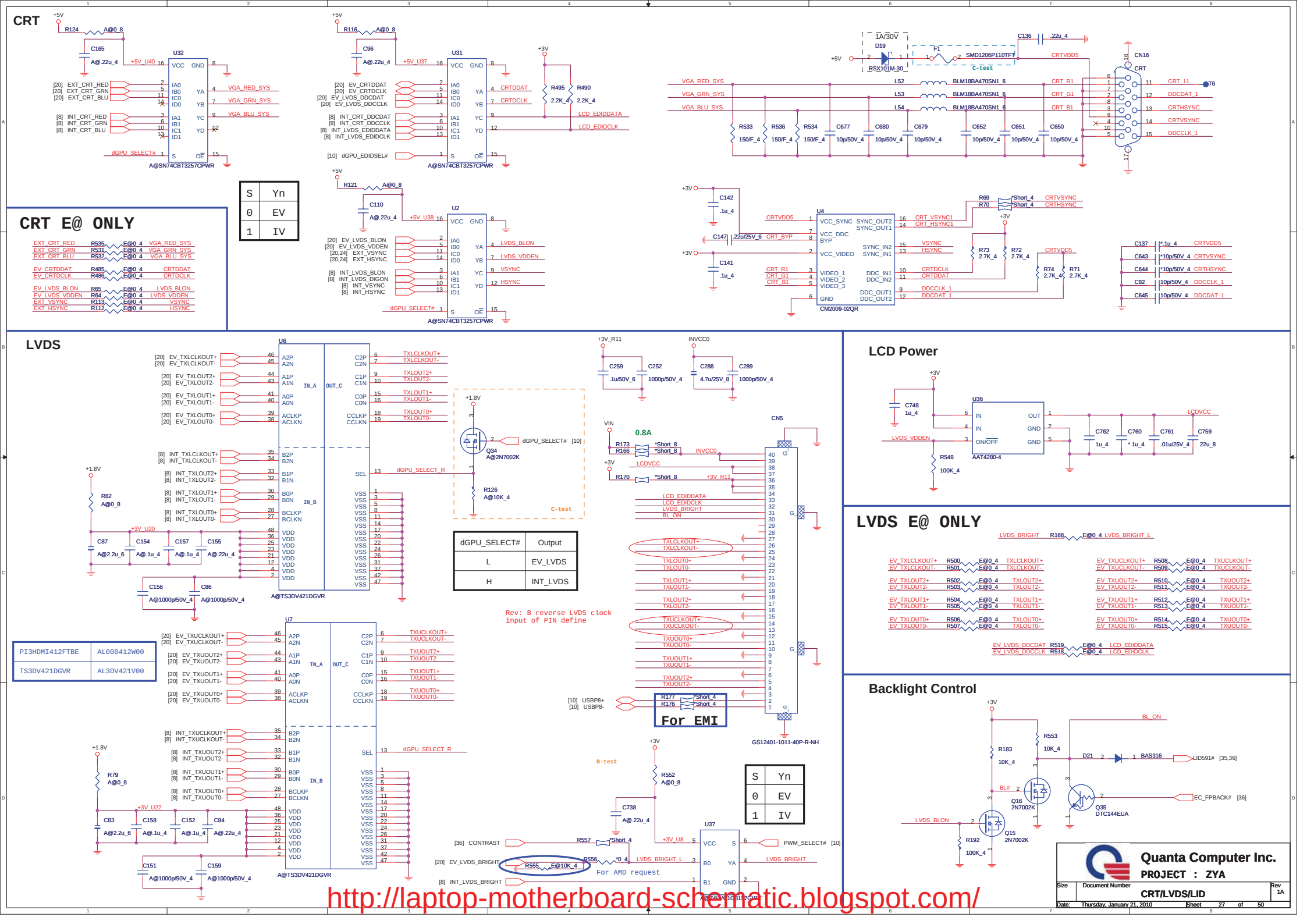
Group-B1 decoupling CAP



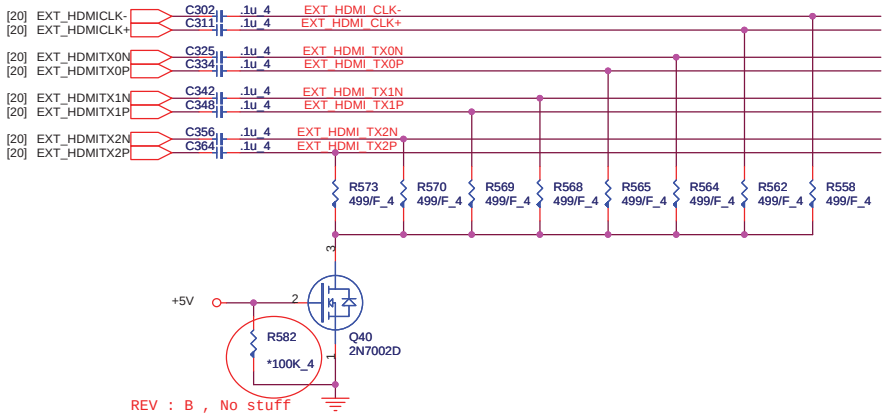
MEM_B1 CLK



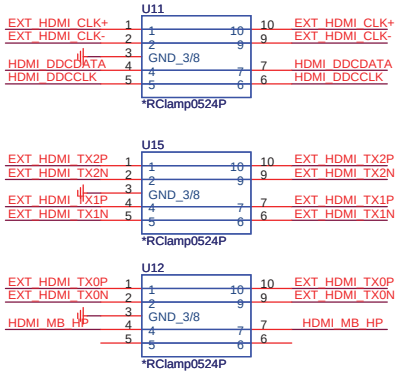
Quanta Computer Inc.		
PROJECT : ZYA		
Size	Document Number	Rev
	MEMORY 2 channel B	1A
Date: Wednesday, January 20, 2010	Sheet 26 of 50	


CRT
CRT E@ ONLY
LVDS
LCD Power
LVDS E@ ONLY
Backlight Control
For EMI
For AMD request
Rev: B reverse LVDS clock input of PIN define
Quanta Computer Inc.
PROJECT : ZYA
CRT/LVDS/LID
Thursday, January 21, 2010
http://laptop-motherboard-schematic.blogspot.com/

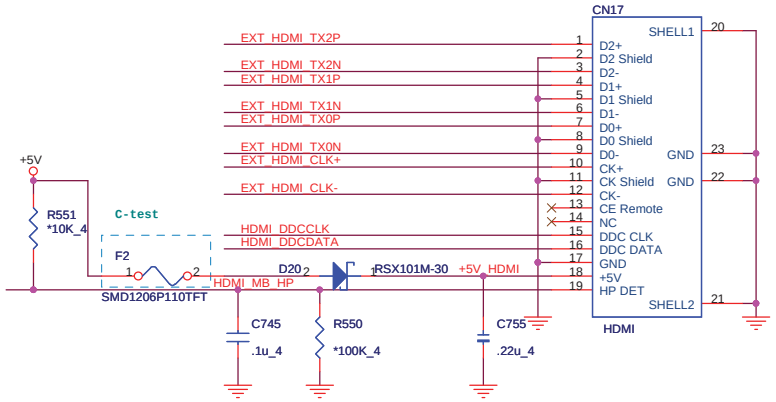
HDMI



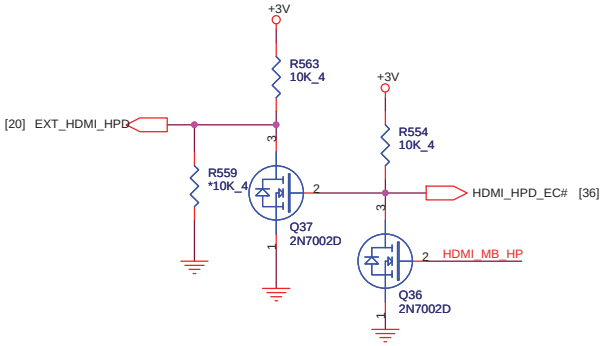
ESD Protect



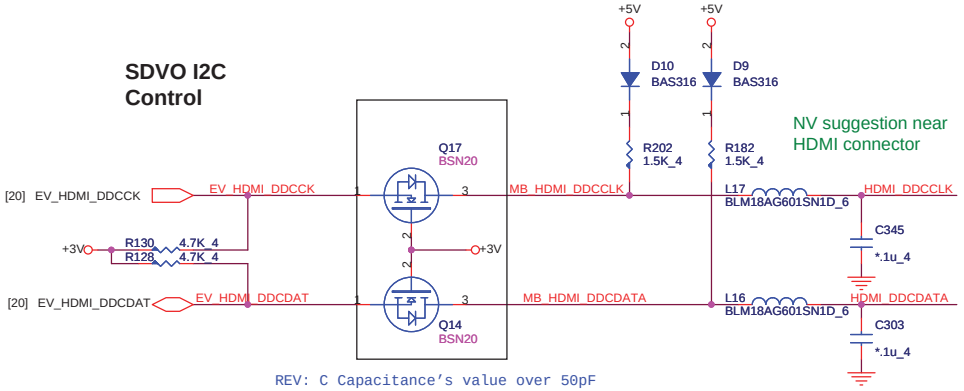
HDMI connector



HDMI Hot-PLUG to EC and GPU



SDVO I2C Control



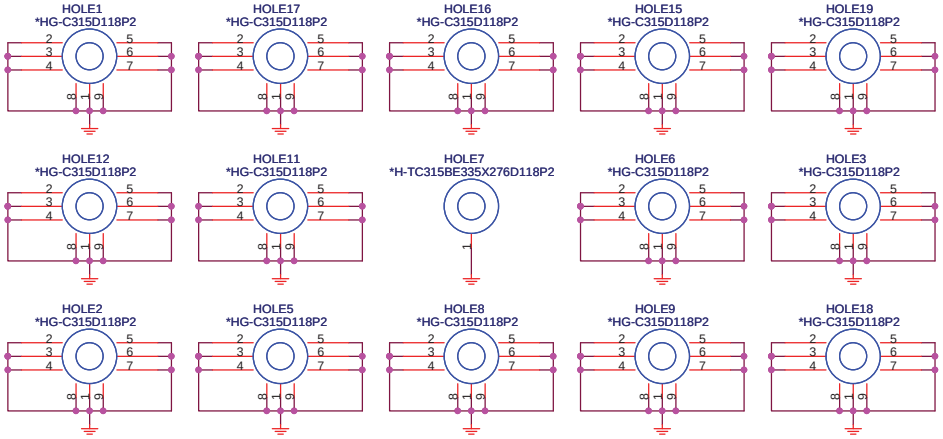
NV suggestion near HDMI connector

EXT_HDMI_CLK-	R1006	*100_4	EXT_HDMI_CLK+
EXT_HDMI_TX2N	R1007	*100_4	EXT_HDMI_TX2P
EXT_HDMI_TX1N	R1009	*100_4	EXT_HDMI_TX1P
EXT_HDMI_TX0N	R1008	*100_4	EXT_HDMI_TX0P

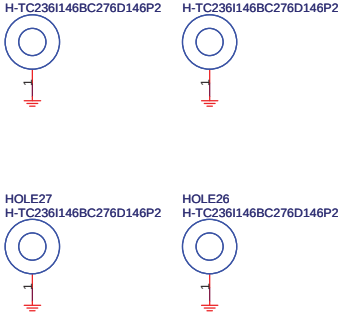
REV : B HDMI reserve 100 ohm parallel resister for EMI

REV: C Capacitance's value over 50pF

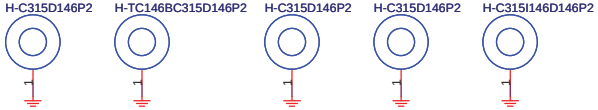
SCREW HOLE



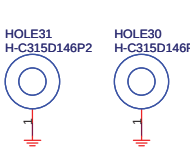
CPU NUT



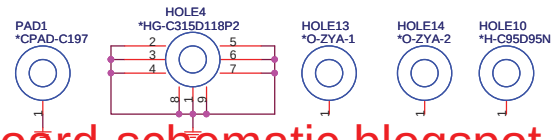
PCH & GPU NUT



PCH NUT



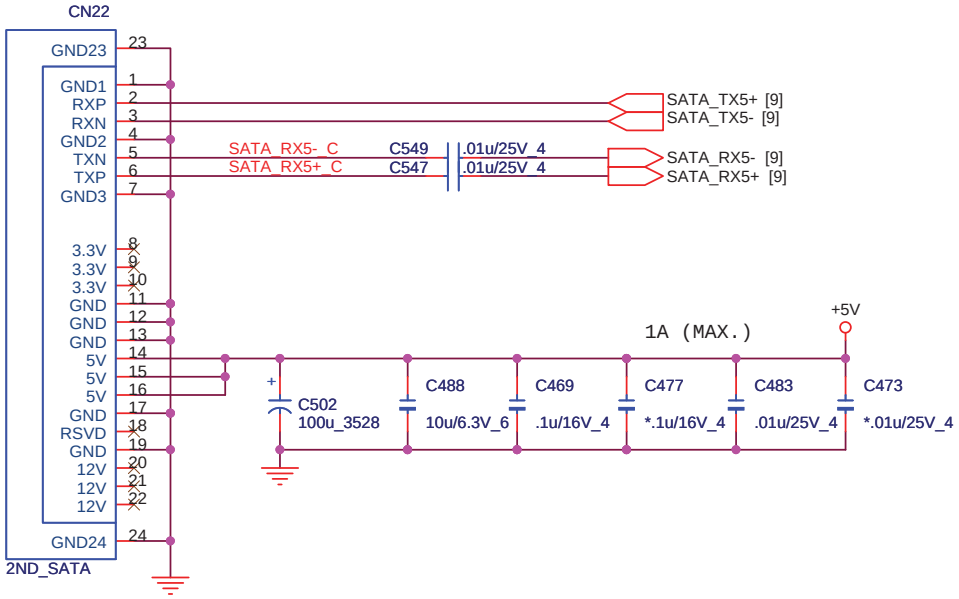
MINI CARD NUT



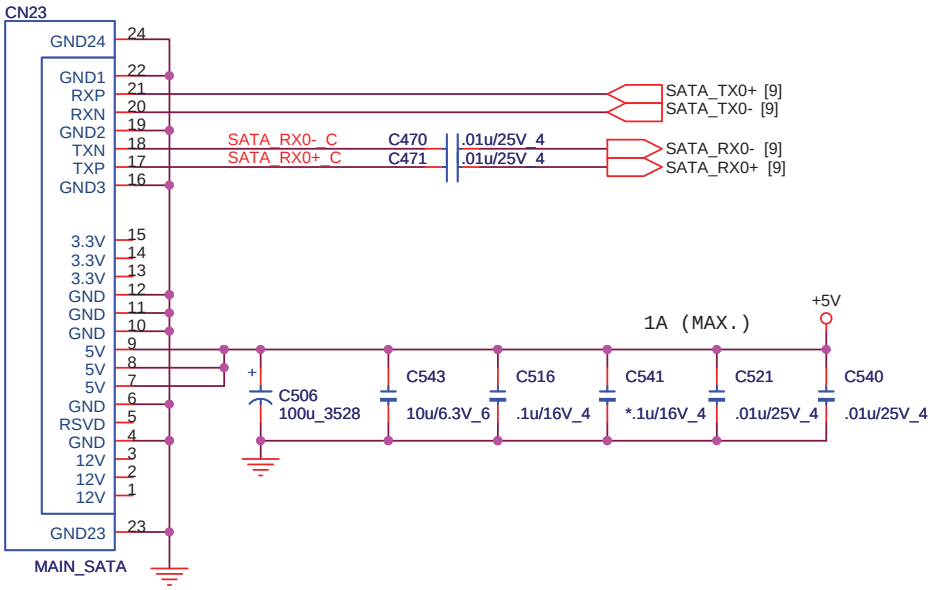
Quanta Computer Inc.
PROJECT : ZYA

Size	Document Number	Rev
	HDMI/DP	1A
Date: Thursday, January 21, 2010	Sheet 28 of 50	

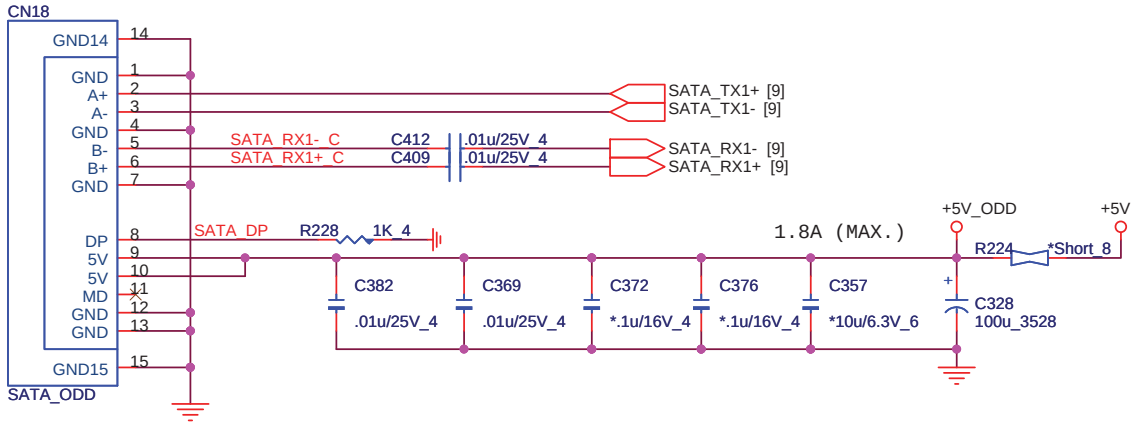
2nd SATA HDD (edge of board)



MAIN SATA HDD



ODD (SATA)

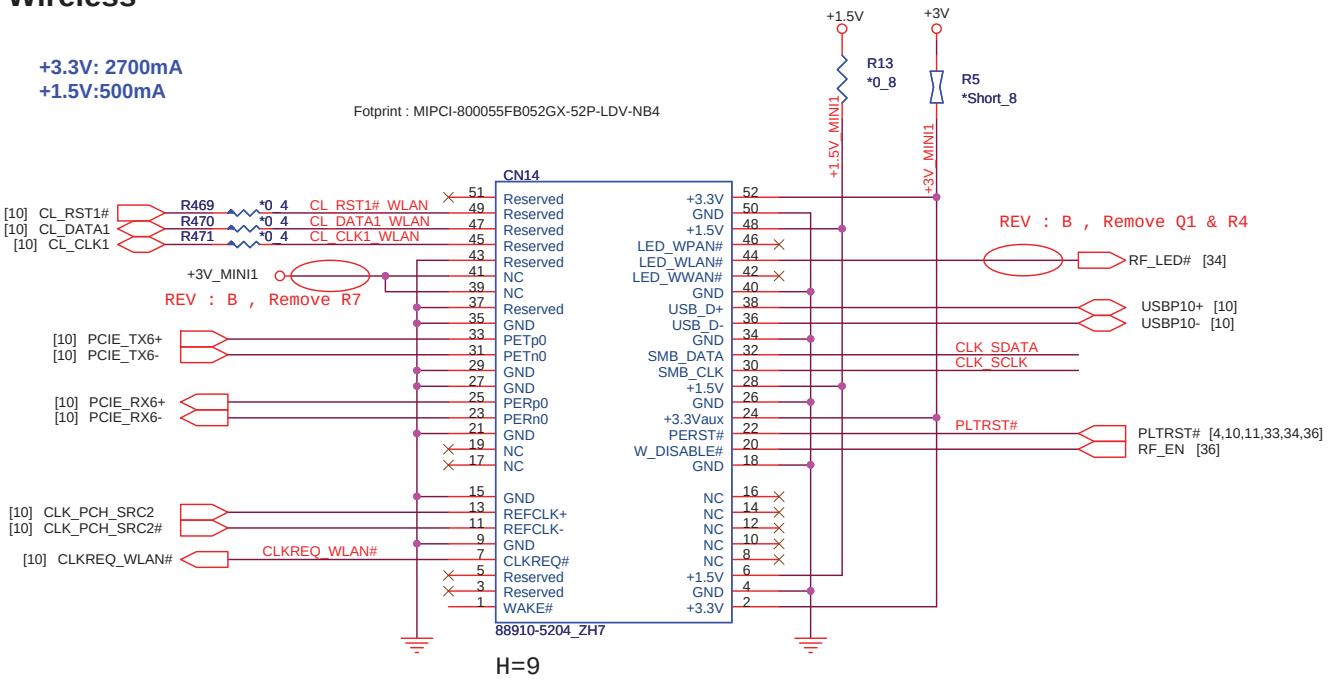


Quanta Computer Inc.		
PROJECT : ZYA		
Size	Document Number	Rev
	SATA-HDD/ODD	1A
Date: Wednesday, January 20, 2010	Sheet 29 of 50	

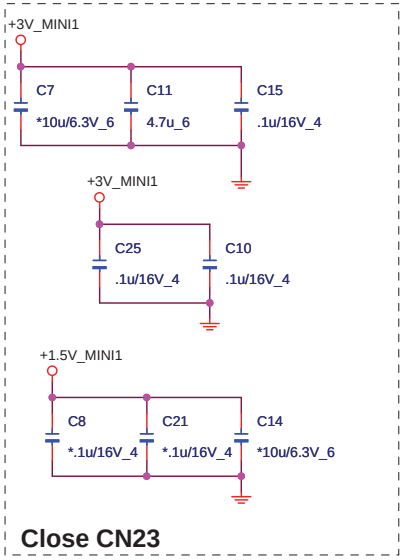
Wireless

+3.3V: 2700mA
+1.5V:500mA

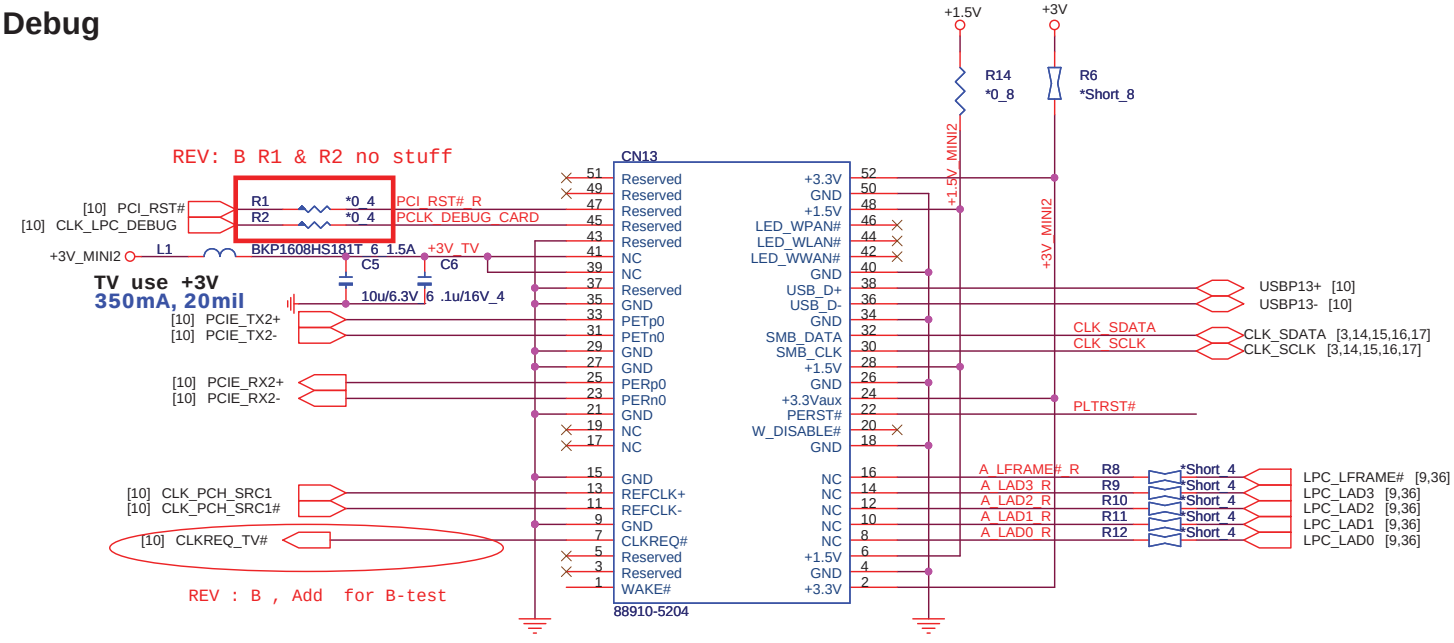
Fotprint : MIPCI-800055FB052GX-52P-LDV-NB4



H=9



TV and Debug



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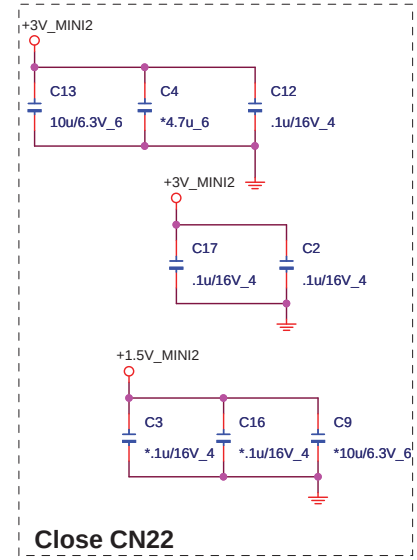
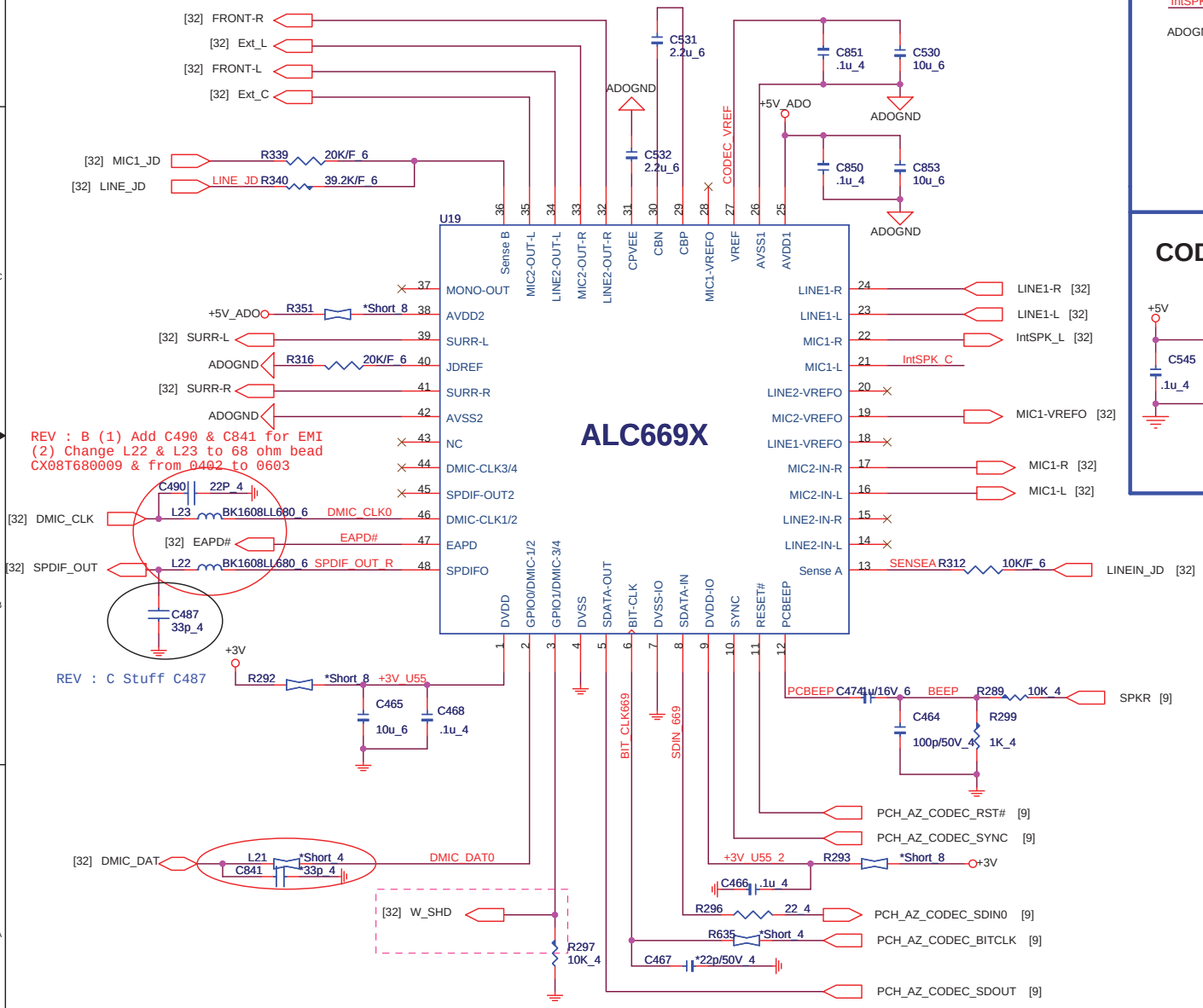


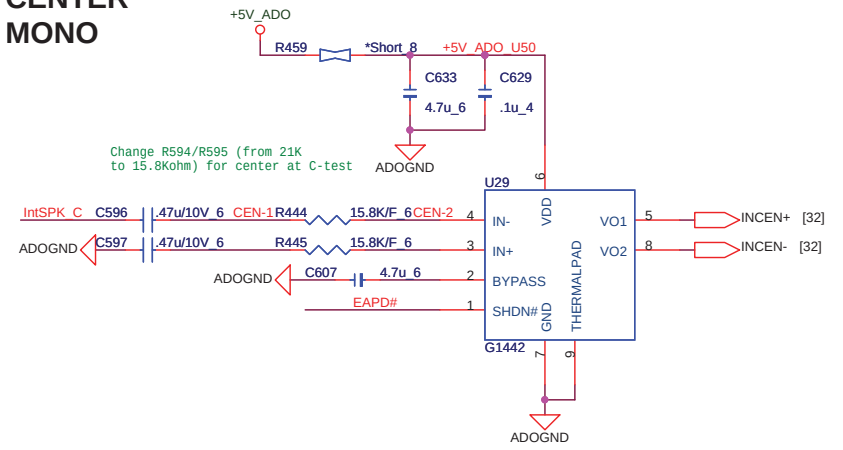
Quanta Computer Inc.
PROJECT : ZYA

Size	Document Number	Rev
	MINI PCI-E card/TV	1A
Date: Wednesday, January 20, 2010	Sheet 30 of 50	

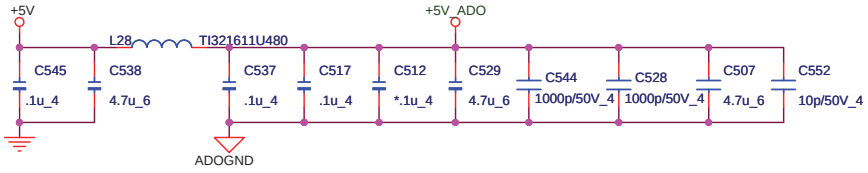
CODEC(ALC669X)

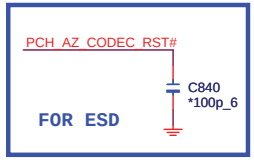


CENTER MONO



CODEC/AMP Power

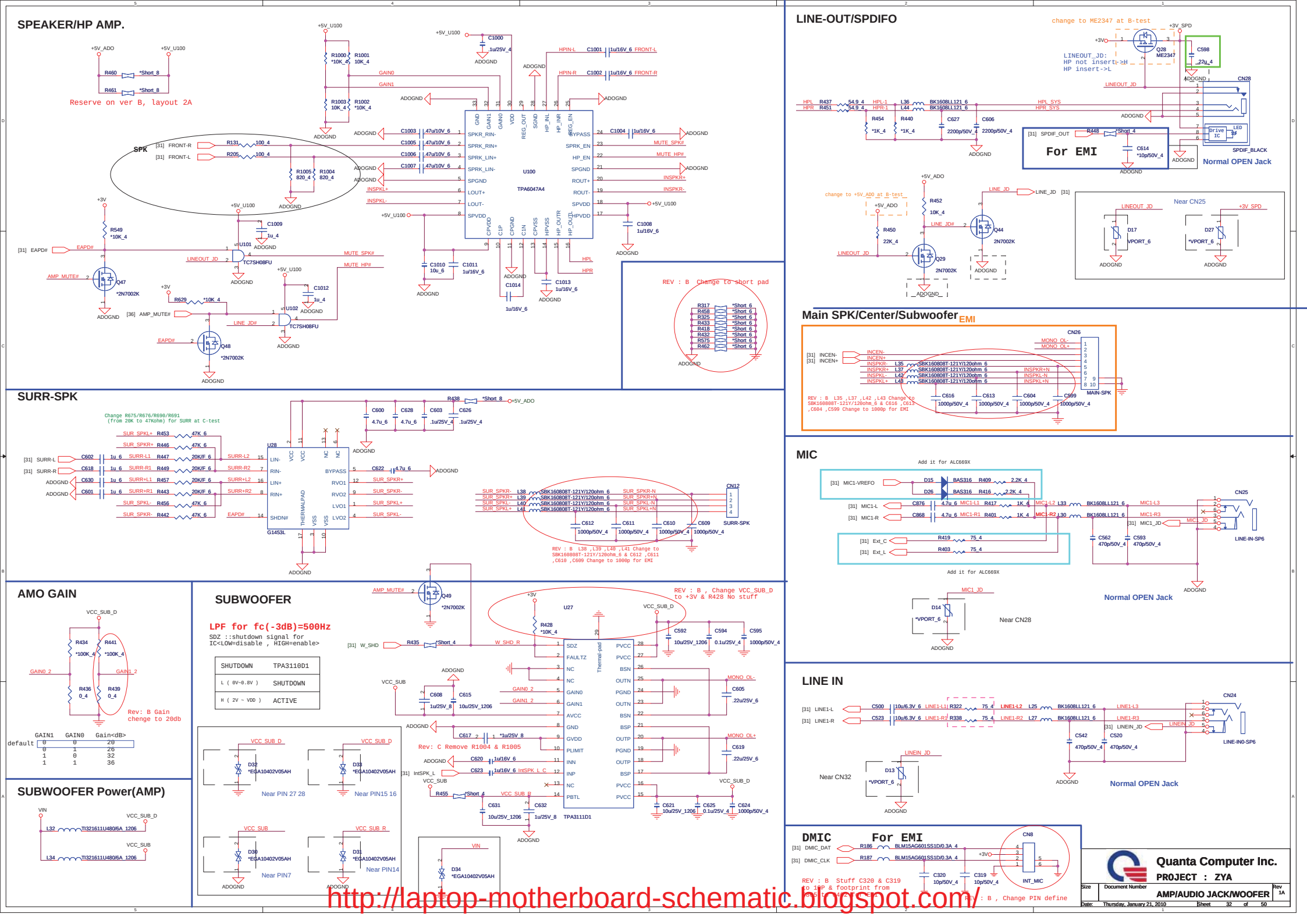




Quanta Computer Inc.
PROJECT : ZYA

Size	Document Number	Rev
	REALTEK ALC889X/MONO-AMP	1A

Date: Wednesday, January 20, 2010 Sheet 31 of 50



Remove R734

Each power pin is 100mA

REV : B , Remove L73 , L74

REV : B , Change to 0 ohm

REV : B , remove 0 ohm

REV : B , Remove the U46 circuit (LDO)

OZ888GS0L3N

OZ888GS0L3N-C1
vqfn64-8x8-4-65p

As close as possible to OZ888GS0LN

As close as possible to OZ888GS0LN

As close as possible to CN35 Pin12

These 1394 signals are high speed differential pairs and must be kept equal length with a differential impedance (Zo) of 110ohms.

These 1394 signals are high speed differential pairs and must be kept equal length with a differential impedance (Zo) of 110ohms.

H=1.2mm Better than 50ppm

CONN_CARDREADER

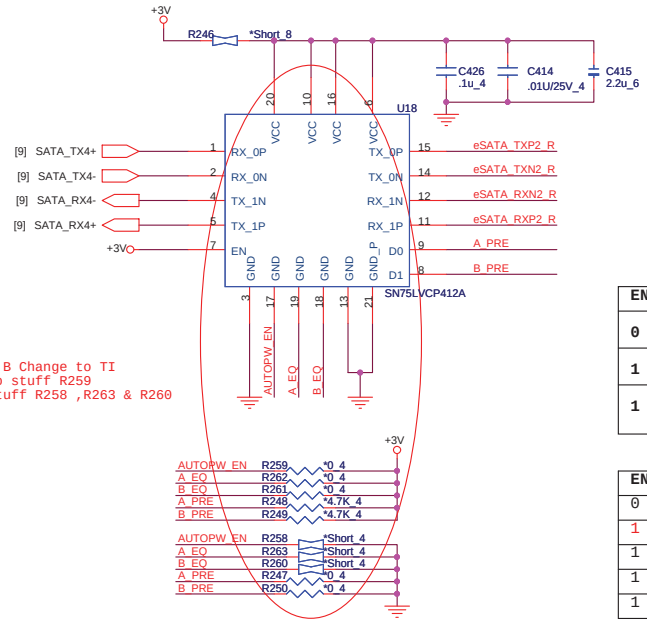
1394/STD

1394 [FIW]

Quanta Computer Inc.
PROJECT : ZYA

Size	Document Number	Rev
	OZ888 Card Reader & 1394	1A
Date: Wednesday, January 20, 2010	Sheet 33 of 50	

ESATA & USB



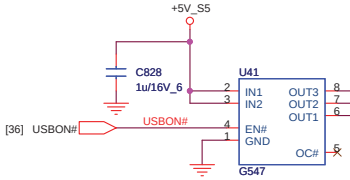
Rev : B Change to TI
(1) No stuff R259
(2) Stuff R258 ,R263 & R260

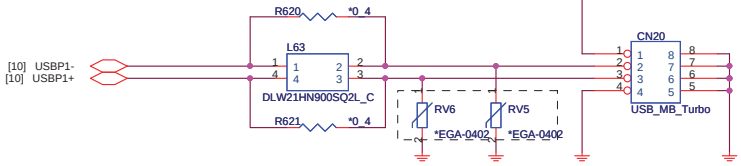
AL008511001

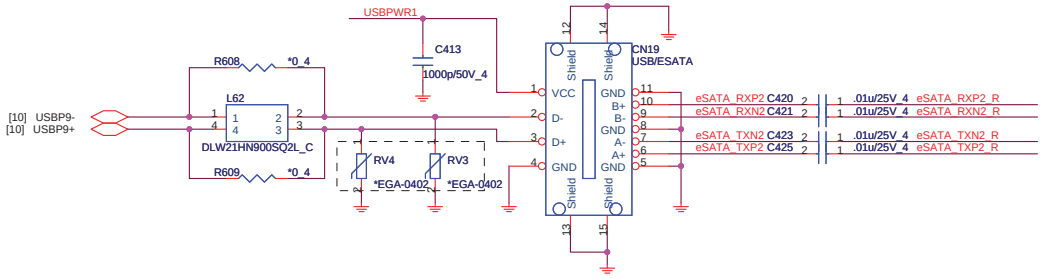
EN	A_PRE	B_PRE	dB
0	X	X	Power down mode
1	0	0	Pre-emphasis disable
1	1	1	Pre-emphasis enable

ALLVC412000

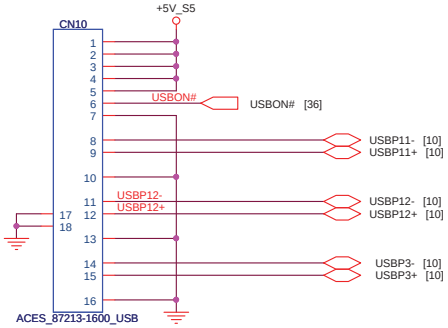
EN	D0	D1	CH-0	CH-1
0	X	X	Standby	Standby
1	0	0	0dB	0dB
1	1	0	Pre-emphasis (5dB)	0dB
1	0	1	0dB	Pre-emphasis (5dB)
1	1	1	Pre-emphasis (5dB)	Pre-emphasis (5dB)

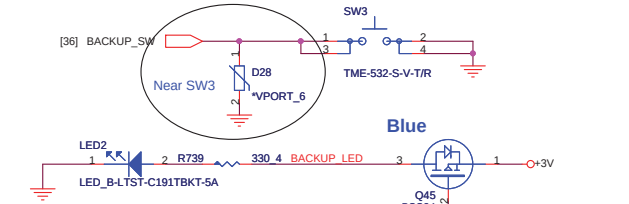


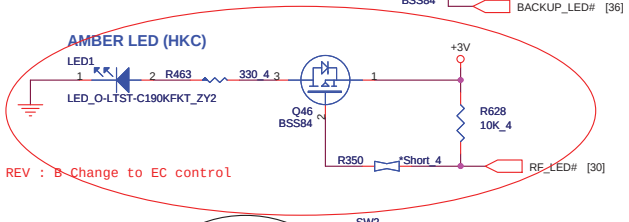


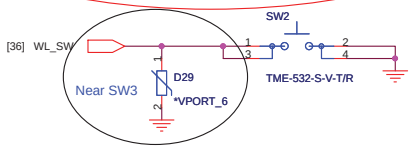


To USB/B

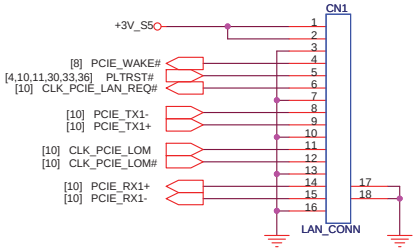




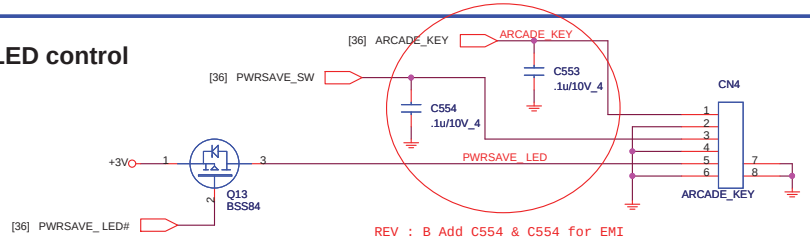


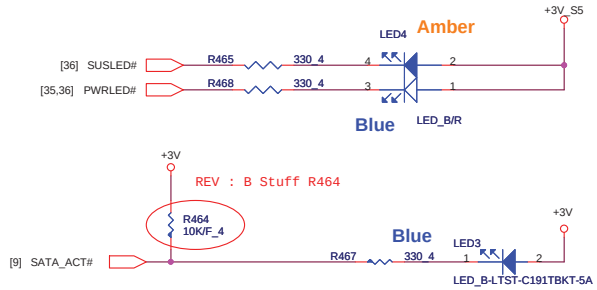


To LAN/B



Keyboard LED control





Quanta Computer Inc.
PROJECT : ZYA

Size	Document Number	Rev
	USB/eSATA/TP_Screen	1A
Date: Wednesday, January 20, 2010	Sheet 34 of 50	

INT K/B

CP6 CP5 CP1 CP2 CP3 CP4 *100p_8P4C
C60 *100p_4 MY16
C61 *100p_4 MY17

CN3 — KB

AMBER LED (HKC)
CAPSLED R53 330_4 Q10 BSS84 CAPSLED# [36]

AMBER LED (HKC)
NUMLED R52 330_4 Q12 BSS84 NUMLED# [36]

TOUCHPAD

+5V R578 10K_4 R579 10K_4
L61 BLM21P300S_8 20mil +TPVDD
C784 .1u/16V_4
[36] TPDATA L59 LZA10-2ACB104MT TPDATA_R
[36] TPCLK L60 LZA10-2ACB104MT TPCLK_R
C783 *.01u/25V_4 C781 *.01u/25V_4
+3VPCU CN7 TP & VR_8P
[27,36] LID591# [36] DIGVOL_UP [36] DIGVOL_DN

Finger-Printer

[10] USBP2- [10] USBP2+ RP2 R184 0X2_4 *Short_8
USBP2- R USBP2+ R CN9 Finger Printer
RV2 *EGA-0402 RV1 *EGA-0402

BLUETOOTH

Rev: B (1) del. R575
(2)change C789 from .33u to 2.2u
(3)Change R574 from 4.7K to short pad

+3V C789 2.2u/6.3V_6 Q38 AO3413
C335 *2.2u_6 C337 1000p/50V_4
BT_POWER 30mil CN6 BT_CONN
[10] USBP4+ [10] USBP4-
[36] BT_POWERON# R574 4.7K_4 C555 *1000p_4

CPU FAN

REV : B Stuff C637 for EMI

+3V R476 *10K_4 R478 10K_4 FAN_PWM_E
Q31 MMBT3904 Q32 MMBT3904
[10,11,36] SML1ALERT# [36] CPUFAN#
+3V +5V R477 10K_4 R479 10K_4
+3V R480 10K_4 [36] FANSIG
+5V For EMI C637 .01u/16V_4 CN15 FAN CONN
FAN_PWM_CN 30mil
REV : B reverse PIN define.

POWER BOARD

+3VPCU R21 *10K_4 R16 10K_4 R17 *Short_4 BATLED1#_R
Q3 *2N7002D Q2 2N7002D
[36] BATLED1#

+3VPCU R27 *10K_4 R24 10K_4 R26 *Short_4 BATLED0#_R
Q6 *2N7002D Q4 2N7002D
[36] BATLED0#

REV : B Change to +3V_S5 & Add PU

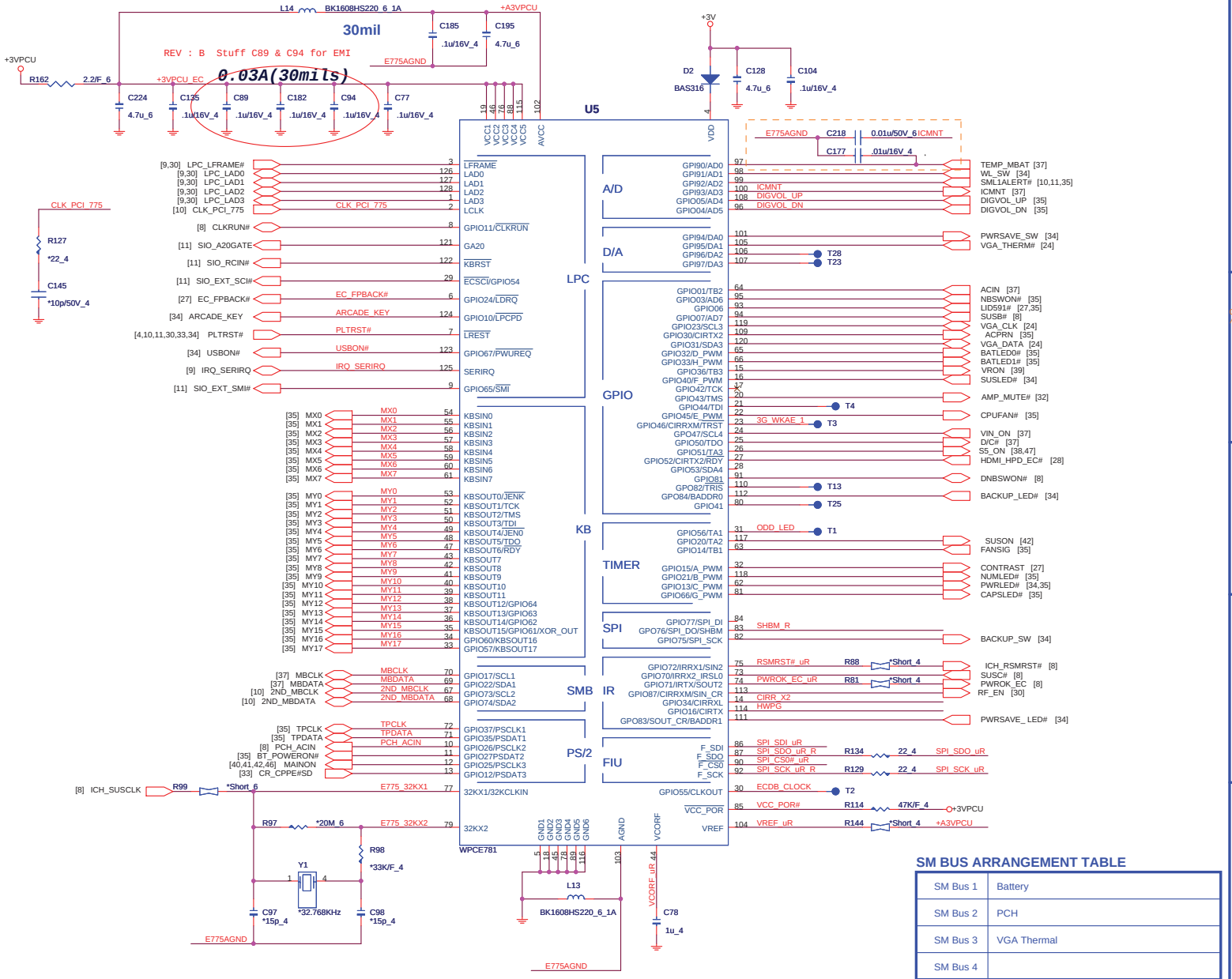
+3VPCU +3V_S5 R123 *10K_4 R25 *Short_4 R28 *0_4 Q5 BSS84
[34,36] PWRLED# [36] ACPRN PWR_LED

+3VPCU L74 FBMA-11-160808-121A20 C551 .1u/10V_4
D1 BAS316 L73 FBMA-11-160808-121A20 C550 .1u/10V_4
[36] NBSWON# PWR_LED
BATLED0# R BATLED1# R CN2 POWER/B_CONN

REV : B Add L73 L74 C551 & C550 for EMI

Quanta Computer Inc.
PROJECT : ZYA
Size | Document Number KB/FAN/TP+FP/BT | Rev 1A
Date: Wednesday, January 20, 2010 | Sheet 35 of 50

EC



I/O ADDRESS SETTING

	I/O Address	
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

SHBM R111 10K_4

1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

SM BUS PU

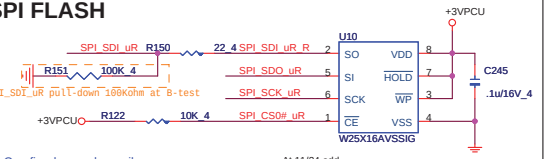
Change pull-up resistor (R148 /R154) from 10K to 4.7Kohm

MBCLK R75 4.7K_4
MBDATA R67 4.7K_4
2ND_MBCLK R61 10K_4
2ND_MBDATA R63 10K_4
REV : B Change from +3V to +3V_S5
VGA_CLK R135 10K_4
VGA_DATA R136 10K_4

INTERNAL KEYBOARD STRIP SET

MY0 R59 10K_4

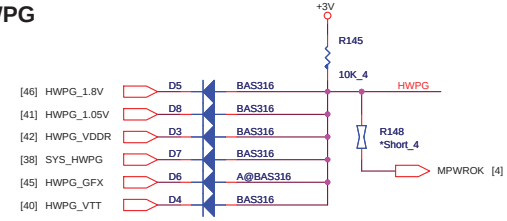
SPI FLASH



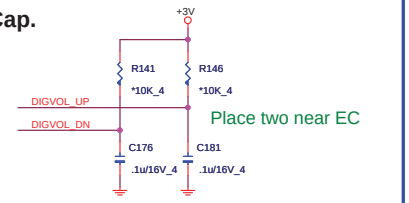
1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

At 11/24 add
Winbond W25X16AVSSIG AKE38ZP0N01
EON EN25F16-100HIP AKE38ZA0Q00
AMIC A25L016 AKE38ZN0800

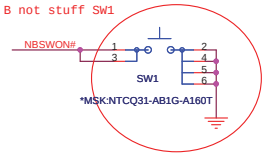
HWPG



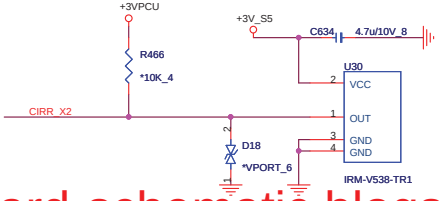
VR Cap.



POWER-ON Switch



CIR



Quanta Computer Inc.
PROJECT : ZYA

Size	Document Number	Rev
	WPCE775C_0DG & FLASH	1A
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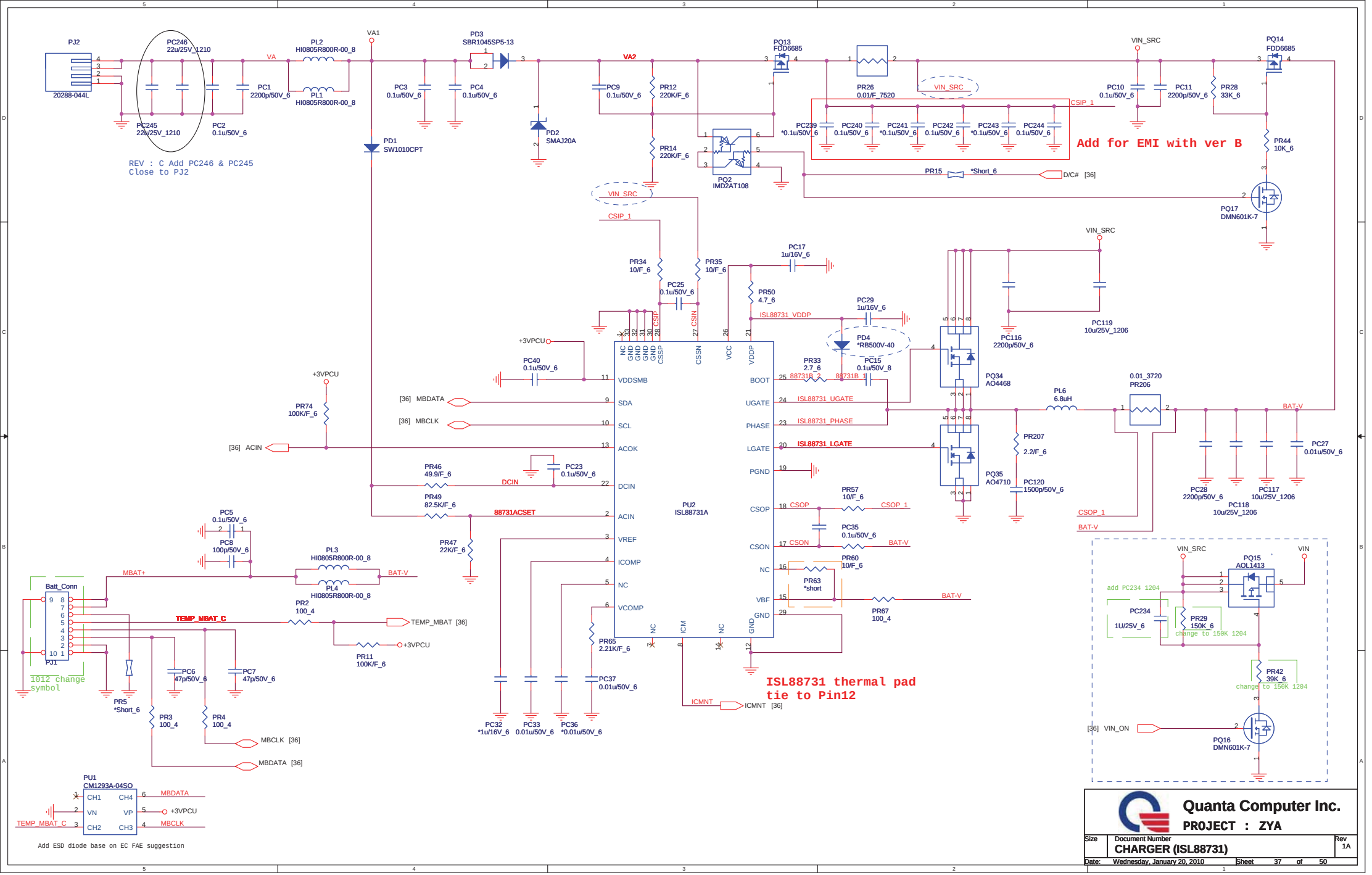
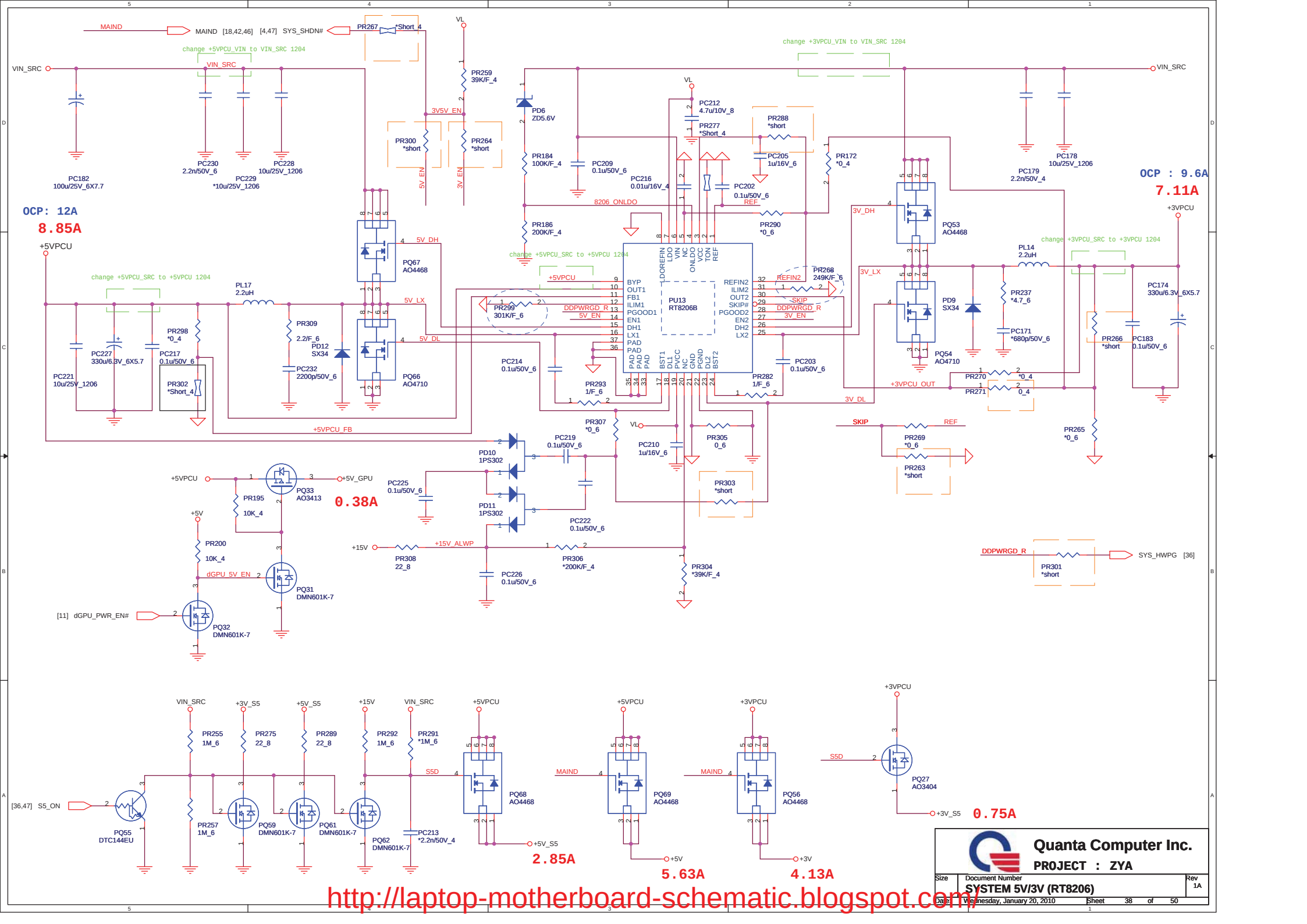




[PWM]

VID 1.2875V

Rev: B checnge footprint for SMT request

Close to Phase 1 Inductor

Parallel

Panasonic ERT-J1VR103J

Close to Phase 1 Inductor

Load Line setting to 1.9mV/A

1019 change 9.76k ohm and 33PF

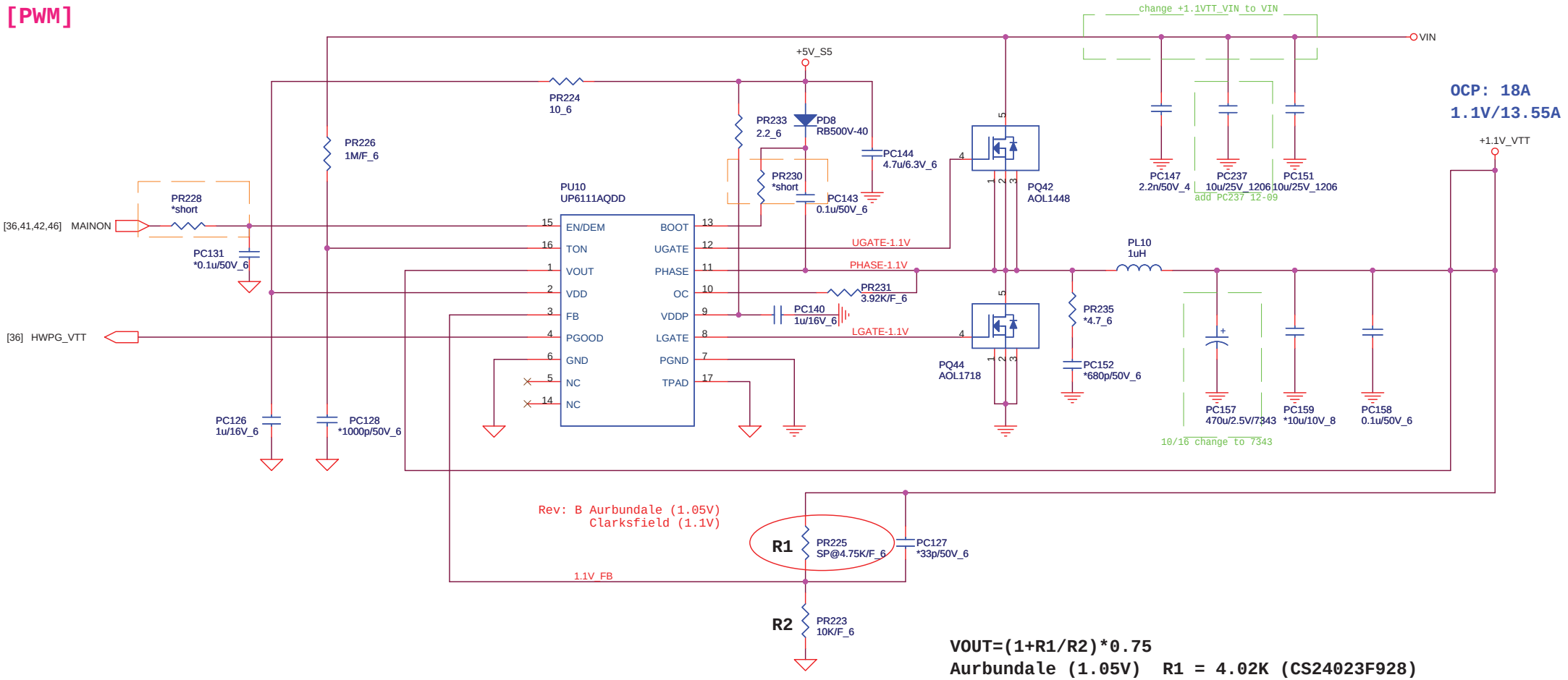
change VCC_CORE_SRC1 to VIN

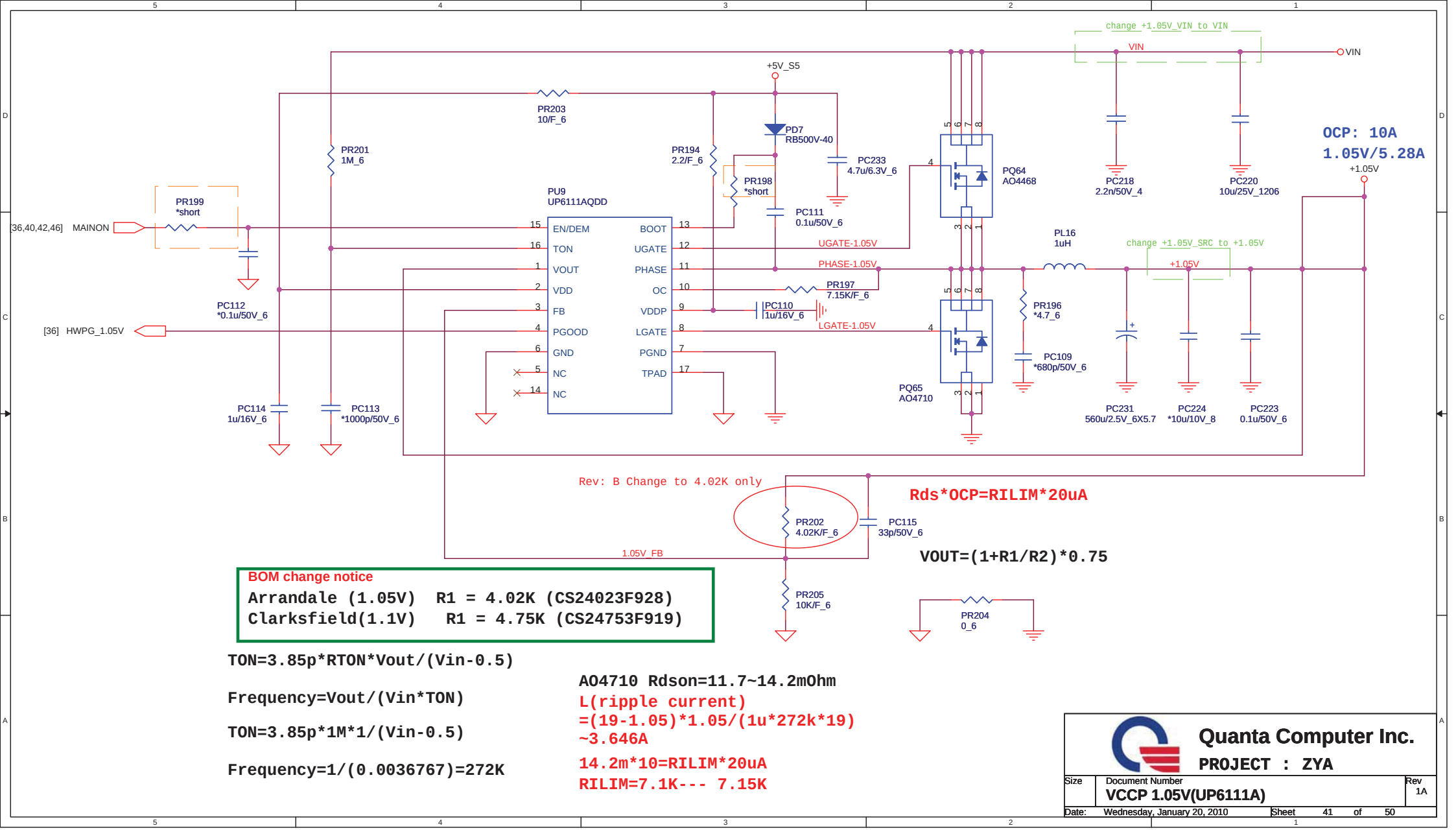
change VCC_CORE_SRC2 to VIN

20A

20A

Quanta Computer Inc.
PROJECT : ZYA
Size | Document Number: CPU Core (ISL62882) | Rev: 1A
Date: Wednesday, January 20, 2010 | Sheet 39 of 50





BOM change notice

Arrandale (1.05V) R1 = 4.02K (CS24023F928)
Clarksfield(1.1V) R1 = 4.75K (CS24753F919)

TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

AO4710 Rdson=11.7~14.2mOhm

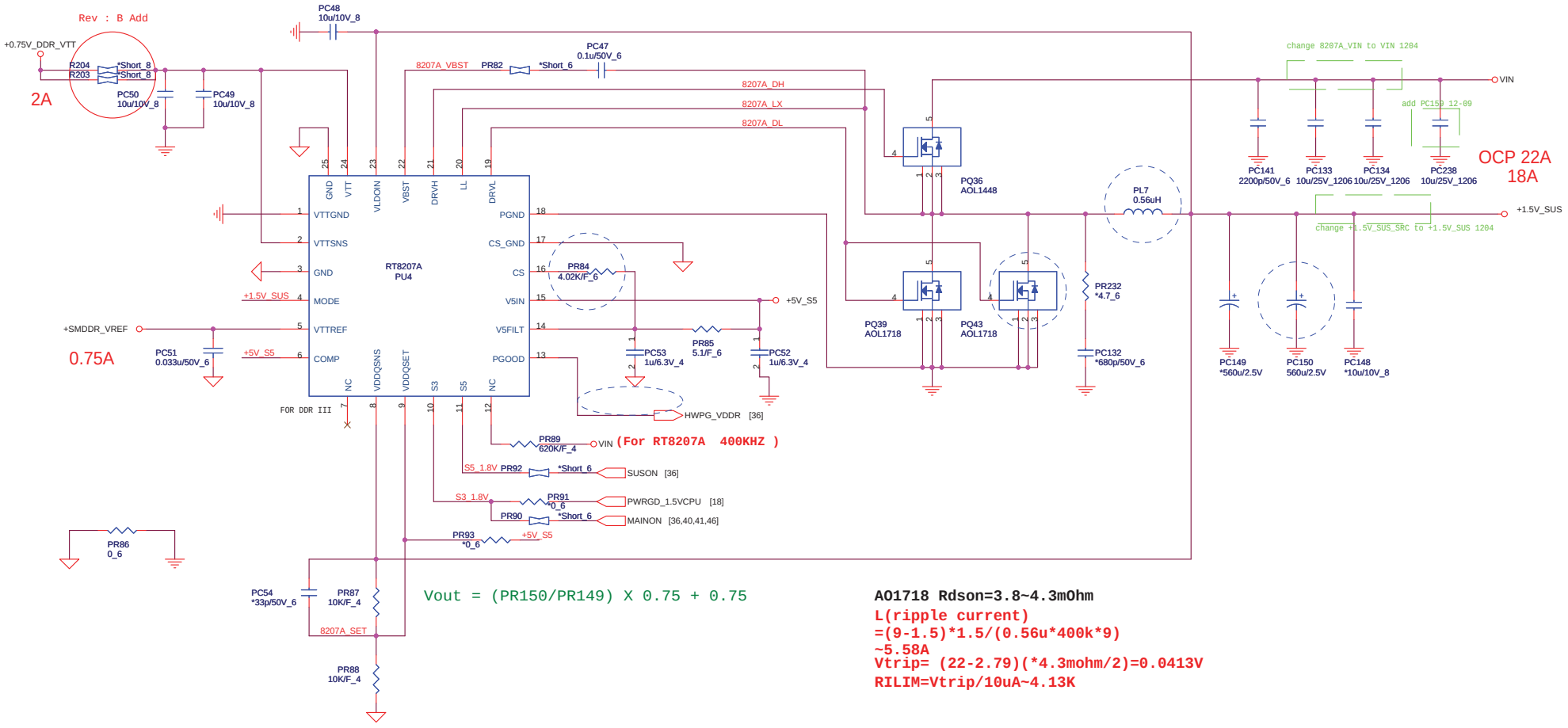
L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.646A

14.2m*10=RILIM*20uA
RILIM=7.1K--- 7.15K

Quanta Computer Inc.
PROJECT : ZYA

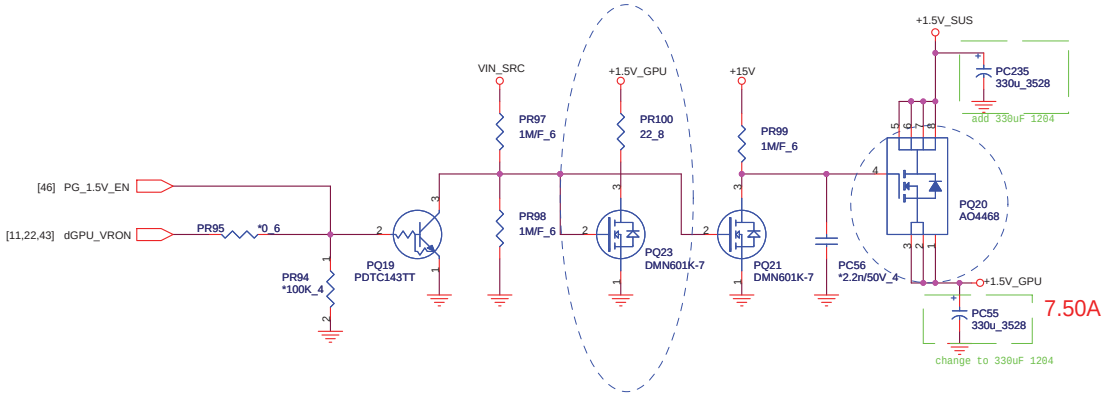
Size	Document Number	Rev
	VCCP 1.05V(UP6111A)	1A
Date: Wednesday, January 20, 2010	Sheet 41 of 50	

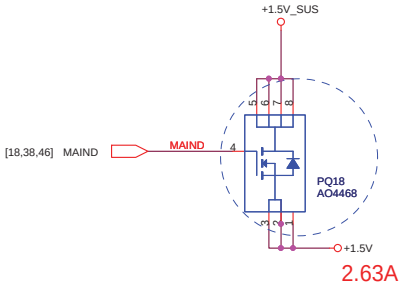
[PWM]



Vout = (PR150/PR149) X 0.75 + 0.75

AO1718 Rdson=3.8~4.3mOhm
L(ripple current)
=(9-1.5)*1.5/(0.56u*400k*9)
~5.58A
Vtrip= (22-2.79)(*4.3mohm/2)=0.0413V
RILIM=Vtrip/10uA~4.13K

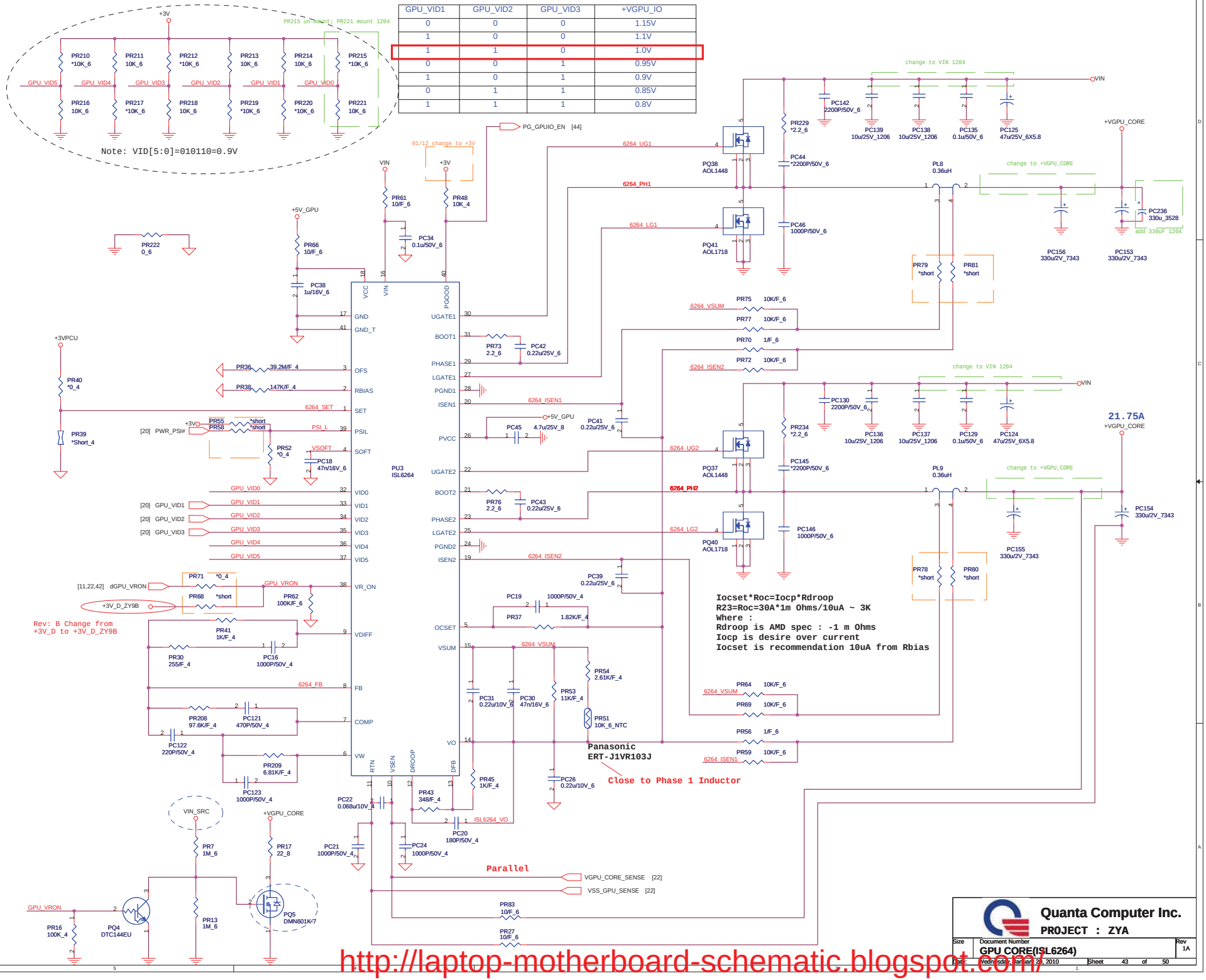


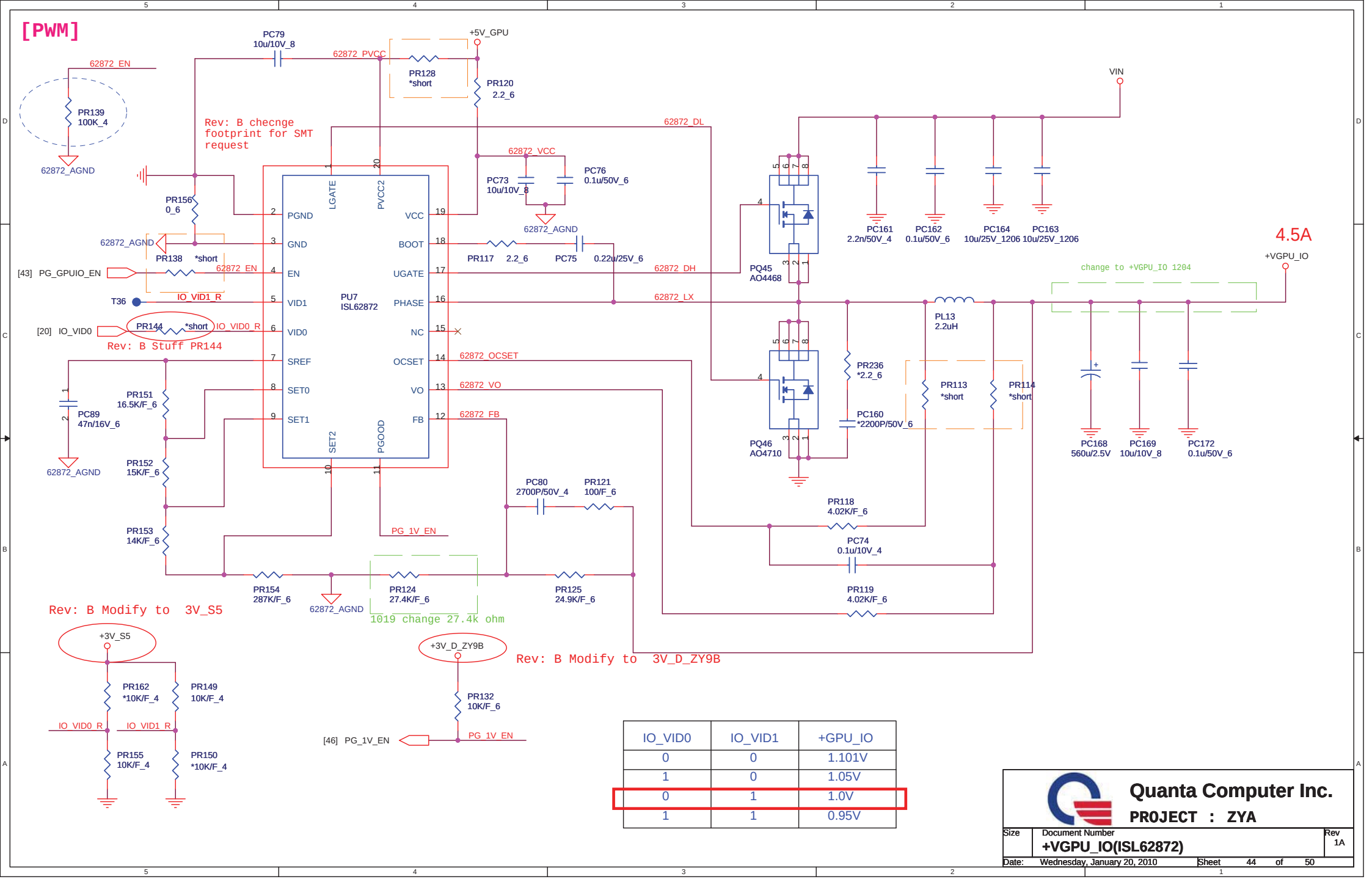


Quanta Computer Inc.
PROJECT : ZYA

Size	Document Number	Rev
	DDR 1.5V(TPS51116)	1A
Date: Wednesday, January 20, 2010	Sheet 42 of 50	

GPU_VID1	GPU_VID2	GPU_VID3	+VGPU_IO
0	0	0	1.15V
1	0	0	1.1V
1	1	0	1.0V
0	0	1	0.95V
1	0	1	0.9V
0	1	1	0.85V
1	1	1	0.8V





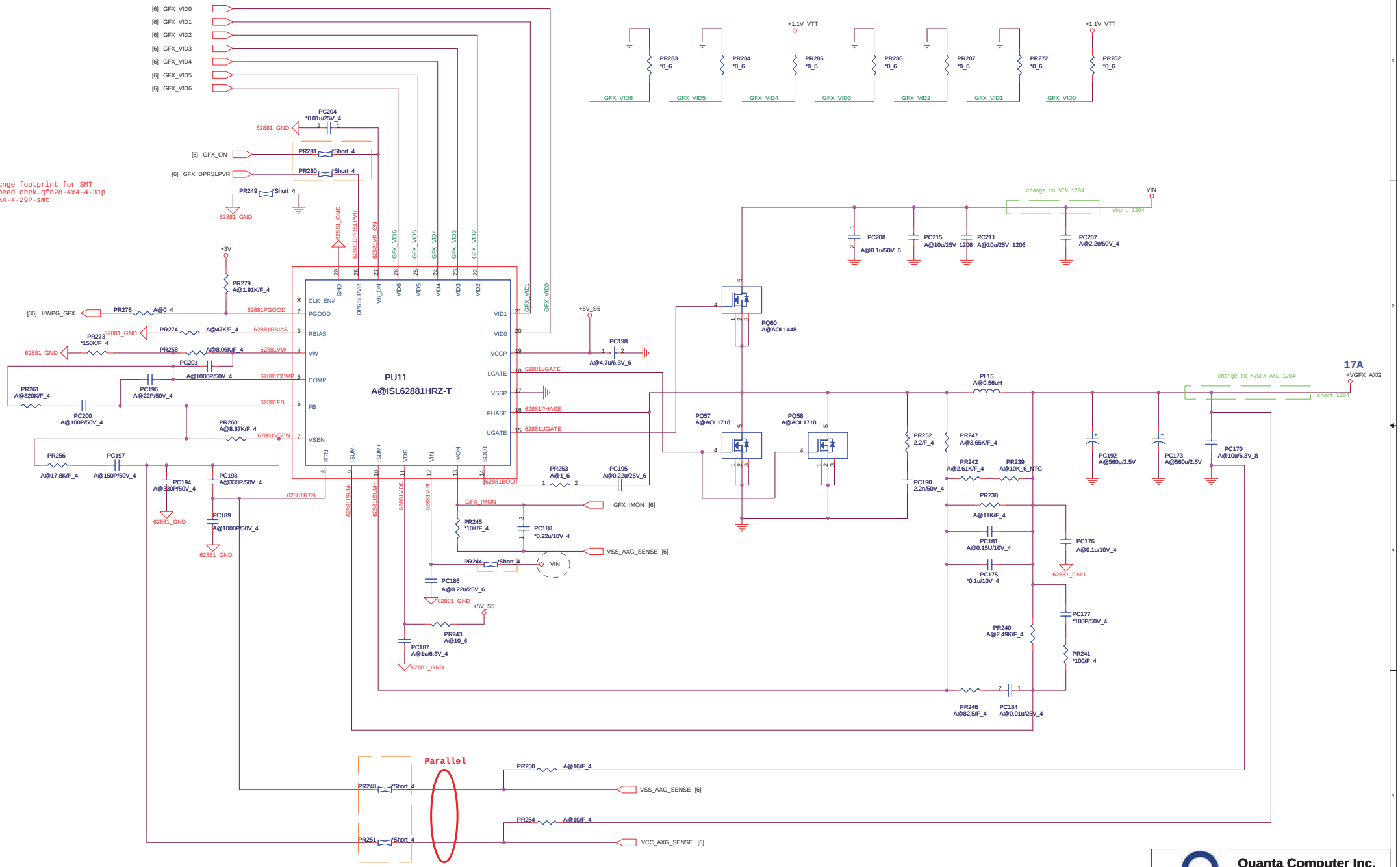
IO_VID0	IO_VID1	+GPU_IO
0	0	1.101V
1	0	1.05V
0	1	1.0V
1	1	0.95V

Quanta Computer Inc.
PROJECT : ZYA

Size	Document Number	Rev
	+VGPU_IO(ISL62872)	1A
Date: Wednesday, January 20, 2010	Sheet 44 of 50	

Int_VGA [PWM]

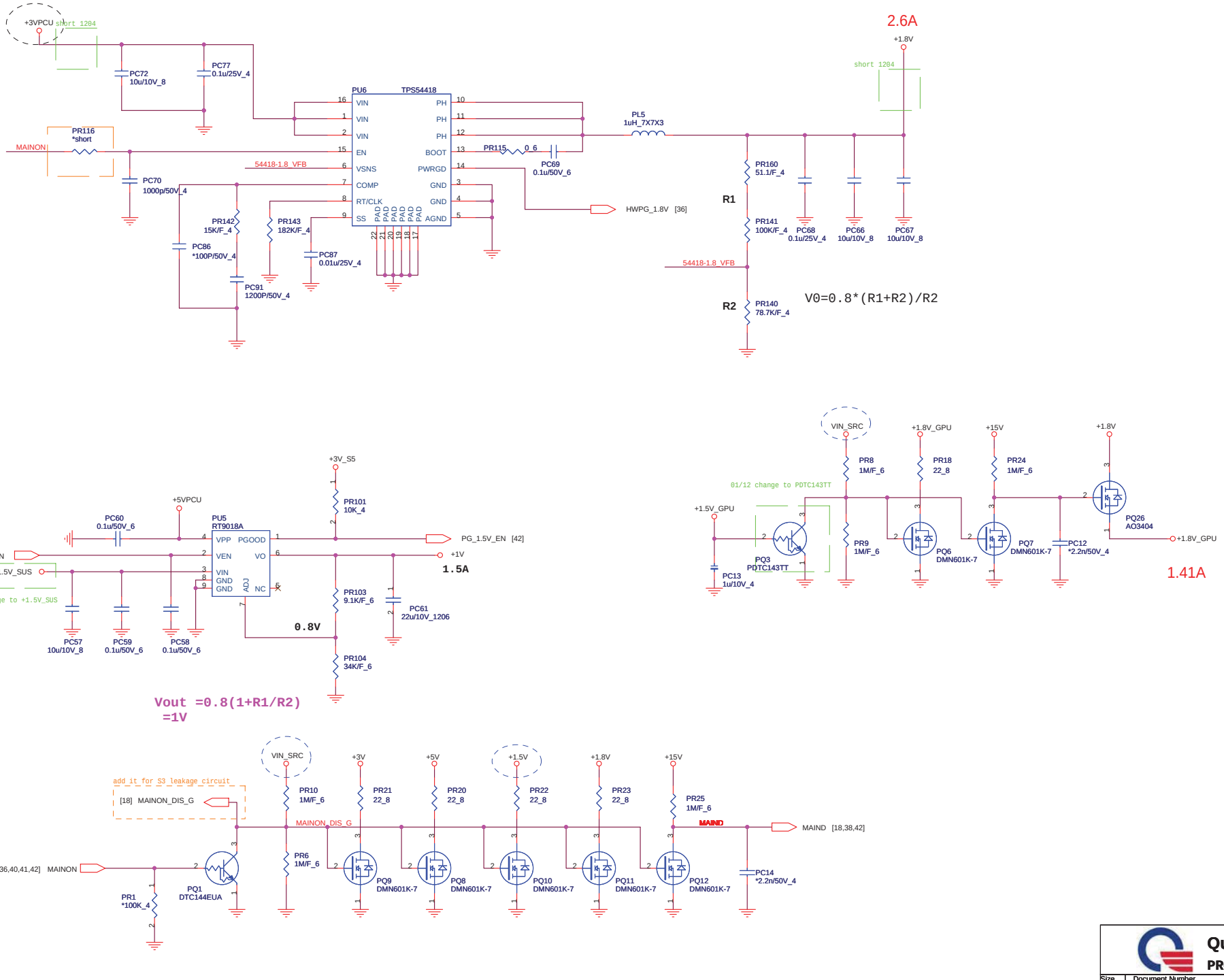
Rev: B checnge footprint for SMT
request , need chek.qfn28-4x4-4-31p
to QFN28-4X4-4-29P-smt



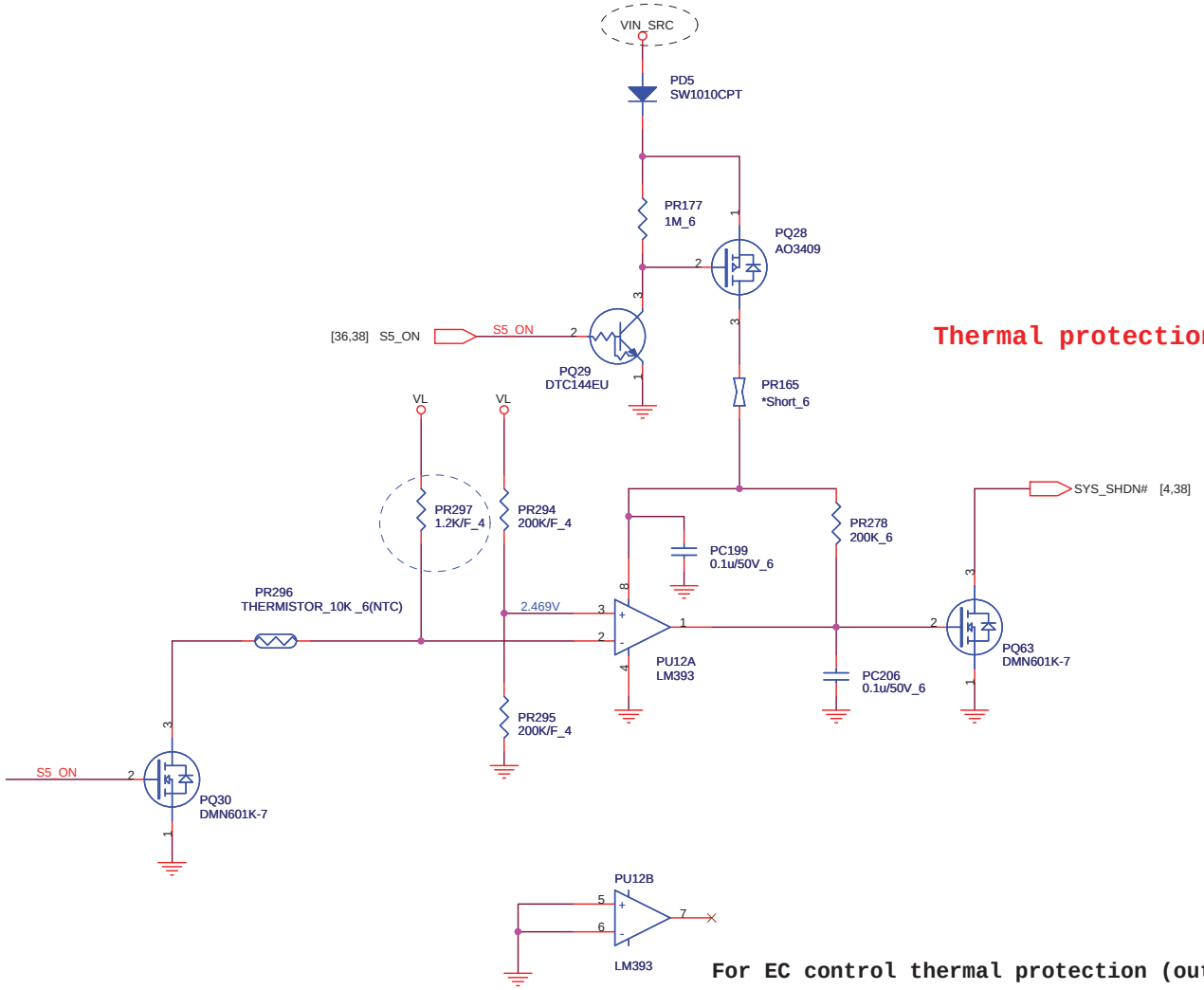
1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

Quanta Computer Inc.
PROJECT : ZYA

Size	Document Number	Rev
	+VGFX_AXG (ISL62881)	1A
Date: Wednesday, January 20, 2010	Sheet 45 of 50	



Quanta Computer Inc.		
PROJECT : ZYA		
Size	Document Number: Discharge/+1.8V/+1V	Rev: 1A
Date: Wednesday, January 20, 2010	Sheet 46 of 50	



Thermal protection

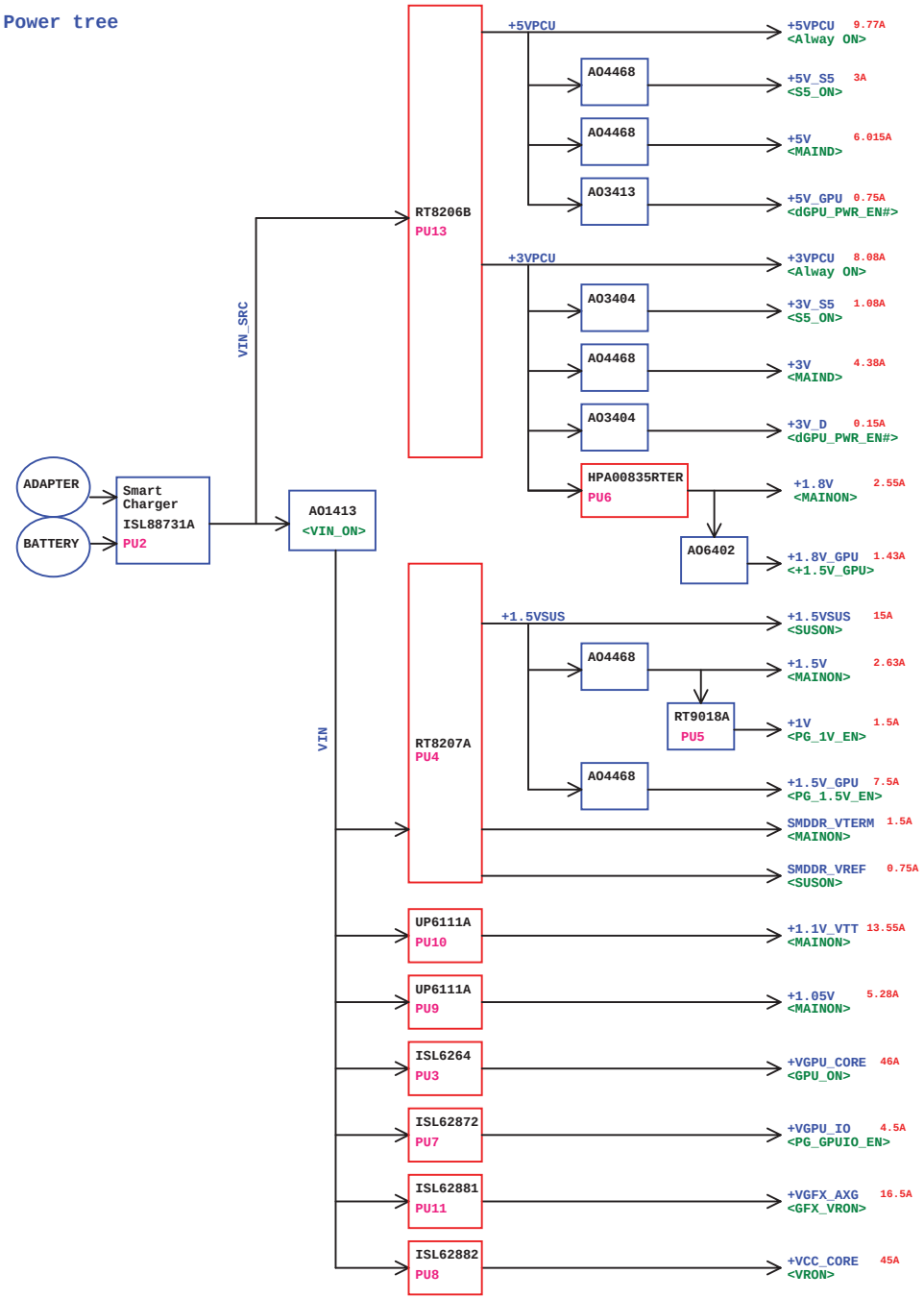
For EC control thermal protection (output 3.3V)

Quanta Computer Inc.

PROJECT : ZYA

Size	Document Number	Rev
	Thermal protect	1A
Date: Wednesday, January 20, 2010	Sheet 47 of 50	

ZYB Power tree



PROJECT : ZYB & ZYBA
Quanta Computer Inc.

Size	Document Number	Rev
	ZYA/B Power tree	1A
Date: Wednesday, January 20, 2010	Sheet 48 of 49	

Model	REV	CHANGE LIST
ZY9B MB	1A	FIRST RELEASED
	2A	Page 3 : U20 Change pin define Page 4 : Not stuff R481 Page 4 : Add XDP_DBRST# contact CPU to PCH Page 6 : Short , Remove R130 & R128 Page 9 : No stuff R715 Page 10 : Add R740 for TV funation Page 10 : Add Y4(25 MHZ) for internal VGA & C832=27pF,C833=22pF Page 11 : R318 Change PU from +3V_S5 to +3V for leakage Page 18 : For ZYA no support M3, No stuff R472 & R36 , stuff R473 ,R474 ,R43 & R44 Page 18 : No stuff PR102 , PQ24 ,PR110 & PQ25 for leakage Page 18 : Remove R131 & R123 for leakage Page 18 : Modify DRAM_RST for AMD request Page 27 : Reverse LVDS clock input of PIN define for design error Page 28 : No stuff R582 for leakage Page 28 : HDMI reserve 100 ohm parallel resister for EMI Page 29 : Mpdify CN23 of symbol Page 30 : Short , Remove R7 Page 30 : Remove Q1 , R4 ,R1 & R2 Page 31 : Add C490 & C487 for EMI Page 31 : Change L22 & L23 to 68 ohm bead CX08T680009 & from 0402 to 0603 for EMI Page 32 : Change AMP for buyer request Page 32 : No stuff R428 amd PU to +3V Page 32 : Change Audio conn. (CN24 & CN25) to normal open Page 32 : Change PIN define of DMIC(CN8) Page 32 : Stuff C320 & C319 to 10P & footprint from 0805 to 0402 for EMI Page 32 : L35 ,L37 ,L42 ,L43 Change to SBK160808T-121Y/120ohm_6 & C616 ,C613 ,C604 ,C599 Change to 1000p for EMI Page 32 : L38 ,L39 ,L40 ,L41 Change to SBK160808T-121Y/120ohm_6 & C612 ,C611 ,C610 ,C609 Change to 1000p for EMI Page 33 : Change R726 to 0 ohm for card reader funation Page 33 : Remove the U46 circuit (LDO) Page 33 : Short 0 ohm for cost down Page 34 : Add R349 (Change to EC control) & reserve R350 Page 34 : Add C554 & C554 for EMI Page 34 : Add L75 ,L76 & L77 for EMI Page 34 : Stuff L63 & L62 & not stuff R620 ,R621 ,R608 & R609 for EMI Page 35 : (1) Reserve R123 & PU to +3VPCU (2)Cahnge Q5.3 PU from +3VPCU to +3V_S5 Page 35 : Change design for bluetooth Page 35 : CN15 change pin define Page 35 : Add L73 ,L74 , C551 & C550 for EMI Page 35 : Stuff C637 for EMI Page 35 : Change to short pad Page 36 : No stuff SW1 Page 36 : U5.80 Change to WLAN_LED Page 36 : R61 & R63 Change PU from +3V to +3V_S5 for leakage Page 36 : Stuff C89 & C94 for EMI Page 39 : PU8 change footprint for SMT request Page 40 : PR225 (+1.1V_VTT) chage to SP@(Aurbundale (1.05V) ,Clarksfield (1.1V)) Page 41 : PR202 Change to 4.02K ohm Page 43 : PR68 Change PU from +3V_D to +3V_D_ZY9B for VGA Sequenc Page 44 : PU7 change footprint for SMT request Page 44 : Stuff PR144 Page 43 : PR149 Change PU from +3V_D to +3V_S5 Page 44 : PR132 Change PU from +3V_D to +3V_D_ZY9B Page 45 : PU11 change footprint for SMT request
	3A	All Page :Change Location: R395 ,R734 ,R201 ,R702 ,R689 ,R708 ,R640 ,R646 ,R328 ,R661 ,R323 ,R372 ,R389 ,R456 ,R320 ,R636 ,R300 ,R333 ,R332 ,R662 ,R652 ,R306 ,R304 ,R15 ,R35 ,R220 ,R231 ,R106 ,R49 ,L4 ,L48 ,L49 ,L45 ,R69 ,R70 ,R173 ,R166 ,R170 ,R177 ,R176 ,R557 ,R224 ,R5 ,R6 ,R8 ,R9 ,R10 ,R11 ,R12 ,R351 ,R292 ,L21 ,R635 ,R738 ,R726 ,R736 ,R733 ,,R293 ,R459 ,R460 ,R461 ,R438 ,R435 ,R455 ,R448 ,R186 ,R187 ,R246 ,R258 ,R263 ,R260 ,R350 , R17 ,R26 ,R25 ,R184 ,R99 ,R128 ,R88 ,R81 ,R144 ,R148 ,R204 ,R203 to short pad Page 27 : Add fuse Location : F1 for safety requirement Page 27 : circuitry update Location : Q34 & R126 for leakage current Page 28 : Add fuse Location : F2 for safety requirement Page 28 : circuitry update Location : Q14 & Q17 , Add R128 & R130 for capacitance's value over 50pF Page 28 : HOLE4 contact to GND Page 29 : Remove 0 ohm Location : R314 ,R336 for cost down. Page 30 : Remove Q100 ,Q101 ,R1004 ,R1005 Page 30 : C622 change from 1u_0402 to 4.7u _0603 Page 30 : Add D27 for ESD Page 33 : Remove 0 ohm Location : R644 ,R639 ,R633 ,R630 f, R349 for cost down. Page 34 : Add D28 & D29 for ESD
	3C	

MODEL	ZY9B	
	FROM	To
	X	1A
	X	1A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
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	3A	3B
	3A	3B
	3A	3B

DOC NO.	PROJECT MODEL :	ZY9B	APPROVED BY:		DATE:	2009/05/??
	PART NUMBER:		DRAWING BY:		REVISON:	1A

Quanta Computer Inc.

PROJECT : ZYA

Size	Document Number	Rev
	Change list	1A
Date: Wednesday, January 20, 2010	Sheet 49 of 50	

EC GPIO Setting

Pin Name	Net Name	Setting	Description
GPIO1	ACIN	GPI	EC Detect AC Adapter State
GPIO3	NBSWON#	GPI	Pwer switch in
GPIO4/AD5	DIGVOL_DN	GPI	Digital Volume wheel.
GPIO5/AD4	DIGVOL_UP	GPI	Digital Volume wheel.
GPIO6	LID591#	GPI	Reserved for Lid function
GPIO7	SUSB#	GPI	S.B sleep S3 pin
GPIO10/LPCPD#	ARCADE_KEY	GPI	Arcade Button switch
GPIO11/CLKRUN#	CLKRUN#	O	Clock Run
GPIO12/PSDAT3	CR_CPPE#SD	GPI	OZ888 Wake indicator
GPIO13/C_PWM	PWRLED#	O	Power on LED drive
GPIO14/TB1	FANSIG	GPI	To detect FAN speed
GPIO15/A_PWM	CONTRAST	O	EC PWM for Panel Brightness
GPIO16/CIRTX	HWPG	GPI	
GPIO17/SCL1	MBCLK	O	SMBus Clock for M/B
GPIO20/TA2	SUSON	GPO	S3 Power Panel
GPIO21/B_PWM	NUMLED#	O	Number Lock LED drive
GPIO22/SDA1	MBDATA	I/O	SMBus Data for M/B
GPIO23/SCL3	VGA_CLK	O	SMBus Clock for acer ID flash
GPIO24/LDRQ#	EC_FPBACK#	GPO	Panel back light control
GPIO25/PSCLK3	MAINON	GPO	Turn On/Off main power
GPIO26/PSCLK2	PCH_ACIN	GPI	
GPIO27/PSDAT2	BT_POWERON#	GPO	Turn On/Off bule tooth power
GPIO30/CIRTX2	ACPRN	GPI	
GPIO31/SDA3	VGA_DATA	I/O	SMBus Data for acer ID flash
GPIO32/D_PWM	BATLED0#	GPO	Battery status LED drive
GPIO33/H_PWM	BATLED1#	GPO	Battery status LED drive
GPIO34/CIRRXL	CIRR_X2	GPI	CIR signal
GPIO35/PSDAT1	TPDATA	O	PS/2 data for touch pad
GPIO36/TB3	VRON	GPO	Turn On/Off CPU Power
GPIO37/PSCLK1	TPCLK	O	PS/2 clock for touch pad
GPIO40/F_PWM	SUSLED	GPO	S3 state LED drive
GPIO41		GPI	No used
GPIO42/TCK		GPI	No used
GPIO43/TMS	AMP_MUTE#	GPO	Turn On/Off Audio Amplier
GPIO44/TDI		GPI	No used
GPIO45/E_PWM	CPUFAN#	O	EC PWM for Fan Module
GPIO46/cirrxm/trst#		GPI	No used
GPO47/SCL4	VIN_ON	GPI	Turn On/Off VIN_SRC Power plane
GPIO50/TDO	D/C#	GPO	Battery charge / discharge control
GPIO51/TA3	S5_ON	GPO	Turn On/Off S5 Power plane
GPIO52/cirtx2/trdy#	HDMI_HPD_EC#	GPI	EC Detect HDMI State
GPIO53/SDA4		O	No used
GPIO54/ECSCI#	SIO_EXT_SCI#	GPI	EC SCI
GPIO55/CLKOUT	ECDB_CLOCK	GPI	EC core clock
GPIO56/TA1		GPI	No used
GPIO57/KBSOUT17	MY17	O	Keyboard scan output
GPIO60/KBSOUT16	MY16	O	Keyboard scan output
GPIO61/KBSOUT15	MY15	O	Keyboard scan output
GPIO62/KBSOUT14	MY14	O	Keyboard scan output
GPIO63/KBSOUT13	MY13	O	Keyboard scan output
GPIO64/KBSOUT12	MY12	O	Keyboard scan output
GPIO65/SMI#	SIO_EXT_SMI#	O	EC SMI
GPIO66/G_PWM	CAPSLED#	O	Caps Lock LED drive
GPIO67/PWUREQ	USBON#	GPO	USB power enable/disable
GPIO70/IRRX2_IRSL0	SUSC#	GPI	S.B sleep S4 pin
GPIO71/IRTX/SOUT2	PWROK_EC	GPO	System Power Good for PCI Reset
GPIO72/IRRX1/SIN2	ICH_RSMRST#	GPO	S.B Resume Power Reset
GPIO73/SCL2	2ND_MBCLK	O	SMBus Clock for CPU thermal
GPIO74/SDA2	2ND_MBDATA	I/O	SMBus Data for CPU thermal
GPIO75/SPI_SCK	BACKUP_SW	GPO	Backup Switch
GPO76/SPI_DO/SHBM	SHBM_R	GPO	Using SPI flash for BIOS and EC firmware
GPIO77/SPI_DI		GPI	No used
GPIO81	DNBSWON#	GPO	S.B Power button Event
GPO82/TRIS		GPI	No used
GPO83/SOUT_CR/BADDR1	PWRSAVE_LED#	GPI	Power Save LED
GPO84/BADDR0	BACKUP_LED#	GPI	Backup LED
GPIO87/CIRRRXM/SIN_CR	RF_EN	GPO	Mini card 1 (WLAN) enable/disable
GPI90/AD0	TEMP_MBAT	I	EC detect battery state
GPI91/AD1	WL_SW	GPI	Wireless Switch
GPI92/AD2	SML1ALERT#	GPI	Touchpad temperature / PCH thermal Hot
GPI93/AD3	ICMNT	I	EC detect system current in AC mode
GPI94/DA0	PWRSAVE_SW	GPI	Power Save (Battery) Button Switch
GPI95/DA1		GPI	No used
GPI96/DA2		GPI	No used
GPI97/DA3		GPI	No used

PCH GPIO Setting

Pin Name	Power	PCH Default	Net Name	Description	Setting	Internal PU/PD	External PU/PD
GPIO0 / BMBUSY#	Core	GPI	BMBUSY#	No used	GPO		PU 8.2KΩ to +3V
GPIO1 / TACH1	Core	GPI	SIO_EXT_SMI#	EC SMI	GPI		PU 10KΩ to +3V
GPIO2 / PIRQE#	Core	GPI	PCI_PIRQE#	No used	GPO		PU 8.2KΩ to +3V
GPIO3 / PIRQF#	Core	GPI	PCI_PIRQF#	No used	GPO		PU 8.2KΩ to +3V
GPIO4 / PIRQG	Core	GPI	PCI_PIRQG#	No used	GPO		PU 8.2KΩ to +3V
GPIO5 / PIRQH#	Core	GPI	PCI_PIRQH#	No used	GPO		PU 8.2KΩ to +3V
GPIO6 / TACH2	Core	GPI	SIO_EXT_SCI#	EC SCI interrupt	GPI		PU 10KΩ to +3V
GPIO7 / TACH3	Core	GPI	BOARD_ID0	M/B ID Setting	GPI		PD 10K to GND & PU to +3V
GPIO8	S5	GPO	RSV_GPIO8	No used	GPO		PU 10KΩ to +3V_S5
GPIO9 / OC5#	S5	Native	USB_OC5#	No used	Native		PU 8.2KΩ to +3V_S5
GPIO10 / OC6#	S5	Native	USB_OC6#	No used	Native		PU 8.2KΩ to +3V_S5
GPIO11 / SMBALERT#	S5	Native	RSV_SMBALERT#	No used	GPO		PU 10KΩ to +3V_S5
GPIO12 / LAN_PHY_PWR_CTRL	S5	Native	LAN_DISABLE#	No used	GPI		PU 10KΩ to +3V_S5
GPIO13 / HDA_DOCK_RST#	S5	GPI	PCH_GPIO13	No used	GPI		RV PU 10KΩ to +3V_S5
GPIO14 / OC7#	S5	Native	USB_OC7#	No used	Native		PU 8.2KΩ to +3V_S5
GPIO15	S5	GPO	CR_WAKE#	No used	GPO	PU 20KΩ	PU 1KΩ to +3V_S5
GPIO16 / SATA4GP	Core	GPI	dGPU_HOLD_RST#	GPU Reset	GPO		PD 100K to G RV PU 10K to +3V
GPIO17 / TACH0	Core	GPI	dGPU_PWROK	GPU Power OK	GPI		PU 10KΩ to +3V
GPIO18 / PCIECLKRQ1#	Core	Native	CLK_PCIE_REQ1#_R	No used	GPO		PU 10KΩ to +3V
GPIO19 / SATA1GP	Core	GPI		No used	GPO		PU 10KΩ to +3V
GPIO20 / PCIECLKRQ2#	Core	Native	CLK_PCIE_REQ2#	Clock Request for PCIE Clocks	Native		PU 10KΩ to +3V
GPIO21 / SATA0GP	Core	GPI		No used	GPO		PU 10KΩ to +3V
GPIO22 / SCLOCK	Core	GPI	GPIO22	No used	GPO		PU 10KΩ to +3V
GPIO23 / LDRQ1#	Core	Native		No used	GPO		
GPIO24	S5	GPO		No used	GPO		
GPIO25 / PCIECLKRQ3#	S5	Native	CLK_PCIE_REQ3#_R	Clock Request for PCIE Clocks	Native		PU 10KΩ to +3V_S5
GPIO26 / PCIECLKRQ4#	S5	Native	CLK_PCIE_REQ4#_R	No used	GPO		PU 10KΩ to +3V_S5
GPIO27	S5	GPO		No used	GPO		
GPIO28	S5	GPI	TP_PCH_GPIO28	No used	GPO		PU 10KΩ to +3V_S5
GPIO29 / SLP_LAN#	S5	GPI	PM_SLP_LAN#	No used	GPO		RV PU 10KΩ to +3V_S5
GPIO30 / SUS_PWR_DN_ACK	S5	GPI	SUS_PWR_ACK_R	No used	GPO		PU 10KΩ to +3V_S5
GPIO31 / ACPRESENT	S5	GPI	ACIN_R	No used	GPO		PU 10KΩ to +3V_S5
GPIO32 / CLKRUN#	Core	GPO , Native	CLKRUN#	PCI Clock Run	Native		PU 8.2KΩ to +3V
GPIO33 / HDA_DOCK_EN#	Core	GPO	HDA_DOCK_EN#	No used	GPO	PU 20KΩ	RV PU 10K to +3V & 1K to GND
GPIO34 / STP_PCI#	Core	GPI	STP_PCI#	No used	GPO		PU 10KΩ to +3V
GPIO35 / SATACLKREQ#	Core	GPO	dGPU_VRON	GPU Voltage Regulator Enable	GPO		
GPIO36 / SATA2GP	Core	GPI	dGPU_PWR_EN#	GPU Power Enable	GPO		PU 10KΩ to +3V
GPIO37 / SATA3GP	Core	GPI	dGPU_PRSNT#	No used	GPI		PD 10KΩ to GND
GPIO38 / SLOAD	Core	GPI	GPIO38	No used	GPO		PU 10KΩ to +3V
GPIO39 / SDATAOUT0	Core	GPI	SAVE_LED#	No used	GPO		PU 10KΩ to +3V
GPIO40/OC1#	S5	Native	USB_OC1#	No used	Native		PU 8.2KΩ to +3V_S5
GPIO41/OC2#	S5	Native	USB_OC2#	No used	Native		PU 8.2KΩ to +3V_S5
GPIO42/OC3#	S5	Native	USB_OC3#	No used	Native		PU 8.2KΩ to +3V_S5
GPIO43/OC4#	S5	Native	USB_OC4#	No used	Native		PU 8.2KΩ to +3V_S5
GPIO44 / PCIECLKRQ5#	S5	Native	CLK_PCIE_REQ5#	No used	Native		PU 10KΩ to +3V_S5
GPIO45 / PCIECLKRQ6#	S5	Native	GPIO45	No used	GPO		PU 10KΩ to +3V_S5
GPIO46 / PCIECLKRQ7#	S5	Native	RST_GATE#	S3 Power Reduction	GPO		PU 10KΩ to +3V_S5
GPIO47 / PEG_A_CLKRQ#	S5	Native	PEG_CLKREQ#_R	Clock Request Signals for PEG	Native		PD 10KΩ to GND
GPIO48 / SDATAOUT1	Core	GPI	SV_SET_UP	No used	GPO		PU 10KΩ to +3V
GPIO49 / SATA5GP	Core	GPI	SATA5GP	CPU alert for EC	GPO		PU 10KΩ to +3V
GPIO50 / REQ1#	Core	Native	PCI_REQ1#	No used	GPO		PU 8.2KΩ to +3V
GPIO51 / GNT1#	Core	Native	PCI_GNT1#	Boot BIOS Selection	Native		PD 1K to GND RV PU 1K to +3V
GPIO52 / REQ2#	Core	Native	dGPU_SELECT#	GPU Output Select	GPO		PU 10KΩ to +3V
GPIO53 / GNT2#	Core	Native	PWM_SELECT#	LVDS_BRIGHT Select	GPO		
GPIO54 / REQ3#	Core	Native	PCI_REQ3#	No used	GPO		PU 8.2KΩ to +3V
GPIO55 / GNT3#	Core	Native	PCI_GNT3#	No used	Native		PU 8.2KΩ to +3V
GPIO56 / PEG_B_CLKRQ#	S5	Native	CLK_PCIE_LAN_REQ#	Clock Request Signals for PEG	Native		PU 10KΩ to +3V_S5
GPIO57	S5	GPI	GPIO57	No used	GPI		PD 10KΩ to GND
GPIO58 / SML1CLK	S5	Native	SMB_CLK_ME1	SMBus Clock for EC	Native		PU 2.2KΩ to +3V_S5
GPIO59 / OC0#	S5	Native	USB_OC0#	No used	Native		PU 8.2KΩ to +3V_S5
GPIO60 / SML0ALERT#	S5	Native	RSV_SML0ALERT#	No used	Native		PU 10KΩ to +3V_S5
GPIO61 / SUS_STAT#	S5	Native	SUS_STAT#	No used	GPO		
GPIO62 / SUSCLK	S5	Native	ICH_SUSCLK	Suspend Clock	Native		
GPIO63 / SLP_S5#	S5	Native	SLP_S5# _R	No used	GPO		
GPIO64 / CLKOUTFLEX0	Core	Native	CLK_FLEX0	No used	GPO		
GPIO65 / CLKOUTFLEX1	Core	Native	CLK_FLEX1	No used	GPO		
GPIO66 / CLKOUTFLEX2	Core	Native	CLK_FLEX2	No used	GPO		
GPIO67 / CLKOUTFLEX3	Core	Native	dGPU_EDIDSEL#	GPU EDID Select	GPO		PU 10KΩ to +3V
GPIO72 / BATLOW#	S5	Native	PM_BATLOW#	No used	GPO		PU 8.2KΩ to +3V_S5
GPIO73 / PCIECLKRQ0#	S5	Native	CLK_PCIE_REQ0#	No used	GPO		PU 10KΩ to +3V_S5
GPIO74 / SML1ALERT#	S5	Native	RSV_SML1ALERT#	No used	GPO		PU 10KΩ to +3V_S5
GPIO75 / SML1DATA	S5	Native	SMB_DATA_ME1	SMBus Data for EC	Native		PU 2.2KΩ to +3V_S5

CK595 Clock Setting Table

Differential CPU Clock

Pin Name	Pin	Net Name	Description
CPU_0	23	CLK_BUF_BCLK	
CPU_0#	22	CLK_BUF_BCLK#	Differential CPU clock

CK595 PCI Express Clock

Pin Name	Pin	Net Name	Description
DOT96	3	CLK_BUF_DREFCLK	
DOT96#	4	CLK_BUF_DREFCLK#	96MHz DOT clock for PCH
SRC_2	13	CLK_BUF_DREFSSCLK	
SRC_2#	14	CLK_BUF_DREFSSCLK#	Clock output for PCH graphic contoller
SRC_1/SATA	10	CLK_BUF_PCIE_3GPLL	
SRC_1#/SATA#	11	CLK_BUF_PCIE_3GPLL#	Differential Serial Reference Clock for PCH

PCH PCI Express Clock

Pin Name	Pin	Net Name	Description
CLKOUT_BCLK0_P	AM3	CLK_CPU_BCLK	
CLKOUT_BCLK0_N	AM1	CLK_CPU_BCLK#	Differential Serial Reference Clock for CPU
CLKOUT_DP_P	AT1	DPLL_REF_SSCLK	
CLKOUT_DP_N	AT3	DPLL_REF_SSCLK#	Differential Serial Reference Clock for CPU
CLKOUT_DMI_P	AN2		
CLKOUT_DMI_N	AN4	CLK_PCIE_3GPLL#	Differential Serial Reference Clock for CPU
CLKOUT_PEG_A_P	AD43	CLK_PCIE_VGA	Differential Serial Reference Clock for PCI-Express
CLKOUT_PEG_A_N	AD45	CLK_PCIE_VGA#	Graphics device
CLKOUT_PCIE0P	AK47		
CLKOUT_PCIE0N	AK48		No use
CLKOUT_PCIE1P	AM45	CLK_PCH_SRC1	
CLKOUT_PCIE1N	AM43	CLK_PCH_SRC1#	Differential Serial Reference Clock for MINI CARD 2
CLKOUT_PCIE2P	AM48	CLK_PCH_SRC2	
CLKOUT_PCIE2N	AM47	CLK_PCH_SRC2#	Differential Serial Reference Clock for MINI CARD 1
CLKOUT_PCIE3P	AH41	CLK_PCH_SRC3	
CLKOUT_PCIE3N	AH42	CLK_PCH_SRC3#	Differential Serial Reference Clock for OZ888
CLKOUT_PCIE4P	AM53		
CLKOUT_PCIE4N	AM51		No use
CLKOUT_PCIE5P	AJ52		
CLKOUT_PCIE5N	AJ50		No use
CLKOUT_PEG_B_P	AK51	CLK_PCIE_LOM	
CLKOUT_PEG_B_N	AK53	CLK_PCIE_LOM#	Differential Serial Reference Clock for on board LAN

Other Clock

Pin Name	Pin	Net Name	Description
27M	6	27M_CLK	27MHz for GPU
27M_SS	7		
REF	30	CLK_ICH_14M	14.318MHz for PCH

Clock Request Table	
CLKREQ#	Control
PEG_A_CLKRQ#	GPU
PCIECLKRQ0#	N/A
PCIECLKRQ1#	MINI2
PCIECLKRQ2#	MINI1
PCIECLKRQ3#	OZ888
PCIECLKRQ4#	N/A
PCIECLKRQ5#	N/A
PEG_B_CLKRQ#	LAN

QUANTA COMPUTER

Title: **Schematic Setting**

Size	Document Number	Rev
	ZH7	1A

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