ZY2 SYSTEM BLOCK DIAGRAM

BOM MARK

E@ EXT VGA 要打
268@ AUDIO 268 要打
D@ DOCK
D2@ DDR2 要打
SP@ 特殊(EXT VGA OR DDR2)
LC@ LOW COST 要打
ED2@ EXT VGA & DDR2 要打
CB@ CARDBUS 要打
NSF@ Non ASF 要打

I@ INT VGA 要打
888@ AUDIO 888要打
D3@ DDR3 要打
ND@ NON DOCK 要打
NLC@ NON LOW COST 要打
TPM@ INT TPM
ID2@ INT VGA & DDR2 要打
ED3@ EXT VGA & DDR3 要打
ID3@ INT VGA & DDR3 要打
ASF@ ASF 要打
NCB@ NON CARDBUS 要打

LOW COST
1. MINI CARD 1 SLOT
2. NON DOCK
3. NON CARDBUS
4. NON ASF
5. NON HDMI

X'TAL 14.318MHZ
CLOCK GENERATOR
ICS: ICS9LPRS365BGLFT
SELGO: SLG8SP512K05
P2

Penryn 479 uFCPGA P3,P4
CPU Thermal Sensor P3
FSB 667/800/1067 Mhz

DDRII SO-DIMM 0 SO-DIMM 1 P16
Dual Channel DDR2 667/800 MHz
DDRIII SO-DIMM 0 SO-DIMM 1 P17
Dual Channel DDR3 667/800 MHz

NB Cantiga PM965 P5,P6,P7,P8,P9,P10,P11

PCIE
MXM-NB8P-GS (nVidia) VRAM 256M VRAM 512M P18
EXT_LVDS
EXT_CRT
EXT_DVI
INT_LVDS
INT_CRT
LVDS
RGB
SWITCH CIRCUIT
CRT Page:19
LVDS Page:19
HDMI Page:20
DVI Level Shift IC PI3VDP411LSZDE Page:20
INT_DVI
DOCKING/DVI Page: 31

X4 DMI interface

HDD (SATA)*2 P25
ODD (SATA) P25
SATA0
SATA1
SATA4

SB ICH9M P12,P13,P14,P15

PCI-Express
PCIE-1
New Card P23
USB5
PCIE-4
Mini Card / WLAN / TV P23
USB6
PCIE-6
X'TAL 25M
BROADCOM 10/100/1G LAN 5764M P21
SWITCH CIRCUIT Page:22
DOCK/LAN Page: 33
Transformer P22
RJ45 P22

PCI Bus
Cardreader Controller OZ601T P29
Media Card Reader P29

USB 2.0
Bluetooth USB4 P22
USB Port x 4 USB0~3 P25
CCD USB7 P19

Azalia
Int MIC P27
Azalia Audio Controller ALC268 & 888 P27
Audio Amplifier P27 & 28
MDC 1.5 P27

X'TAL 32.768KHZ

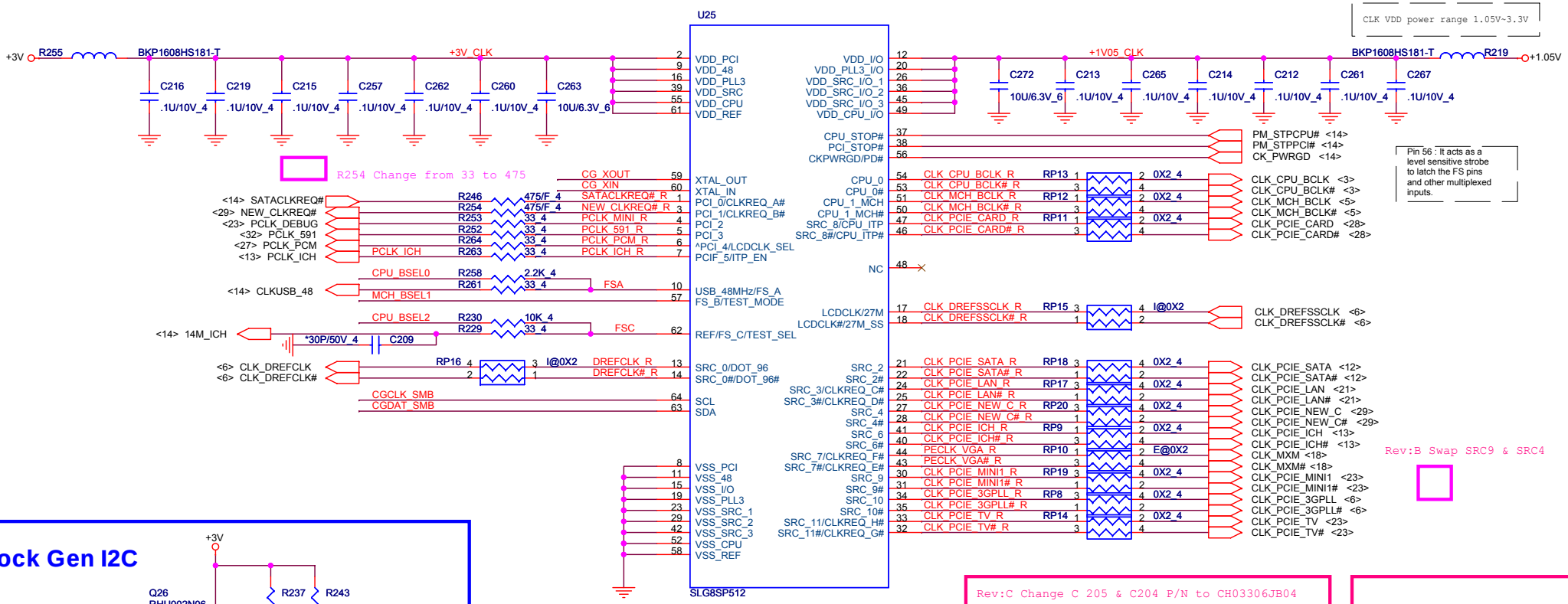
LPC
EC (WPC8769LDG) P32
X'TAL 32.768K
TPM P23
SPI ROM P32
Touch Pad P32
K/B COON. P32
VR P27
CIR P32
Fan Header P31

Connector
Speaker P28
Phone Jack P28
SPDIF P28
Line in P28
MIC Jack P28
SUBWOOFER P28

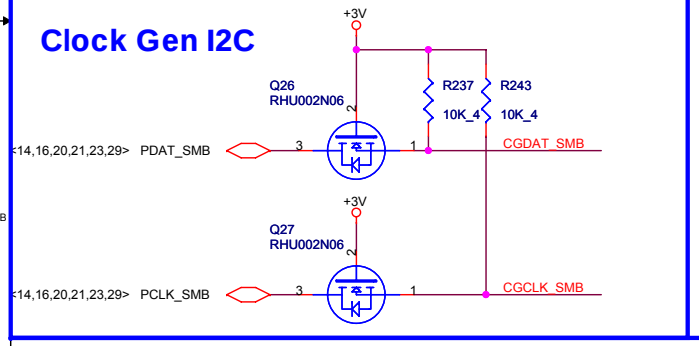
Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	Block Diagram	1A
Date: Tuesday, April 08, 2008	Sheet 1 of 40	

Clock Generator

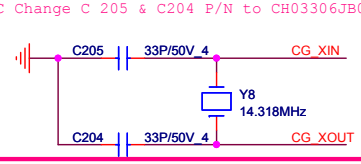


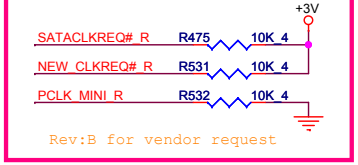
Clock Gen I2C



	QCI P/N
SLG8SP512	AL8SP512K05
ICS9LPRS365BGLFT	ALPRS365K13

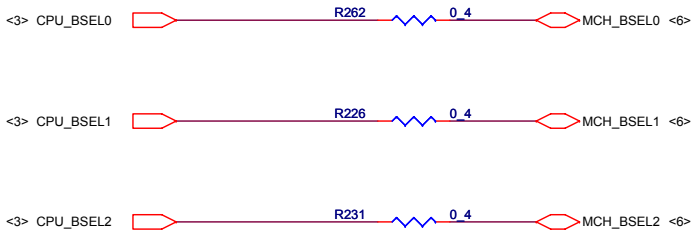
Rev:C Change C 205 & C204 P/N to CH03306JB04





CPU Clock select

Pin 10/57/62 : For Pin CPU frequency selection

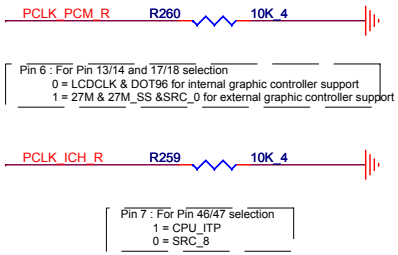


CRB Rev0.7 : 110(CBA)

BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz

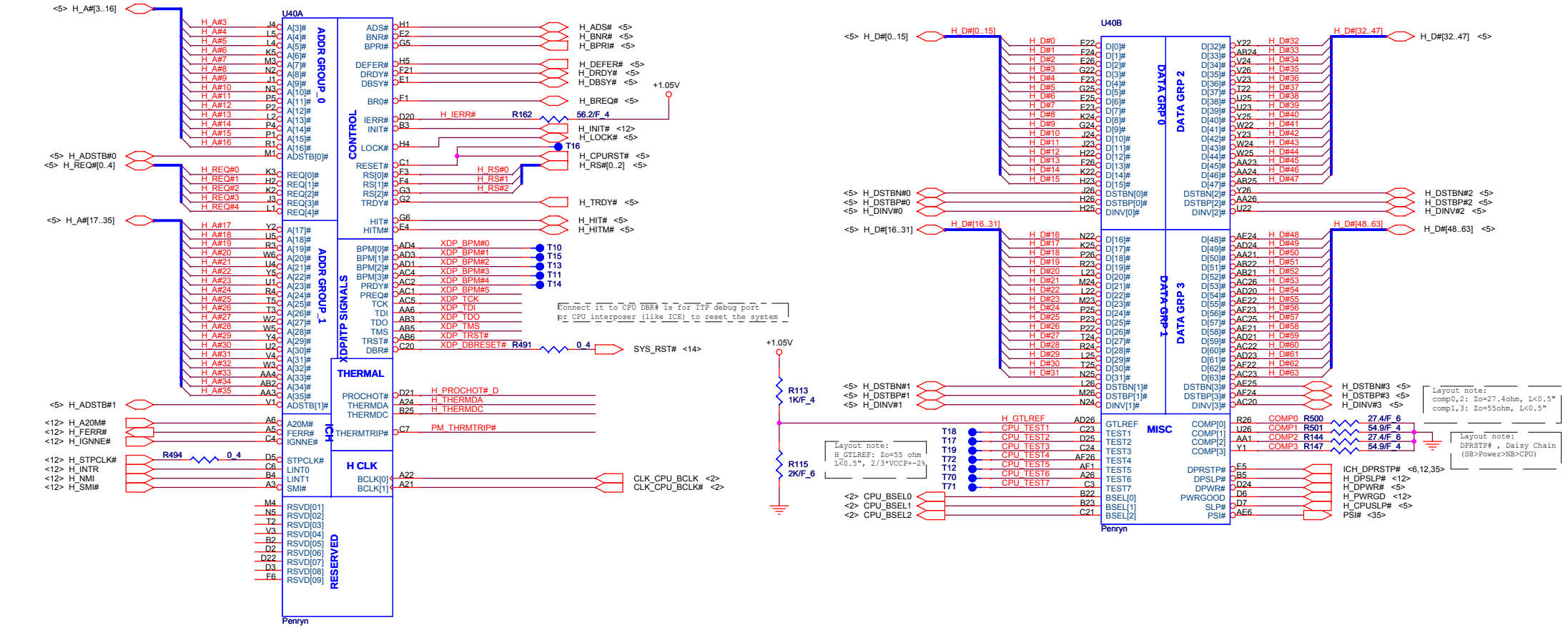
Strap table



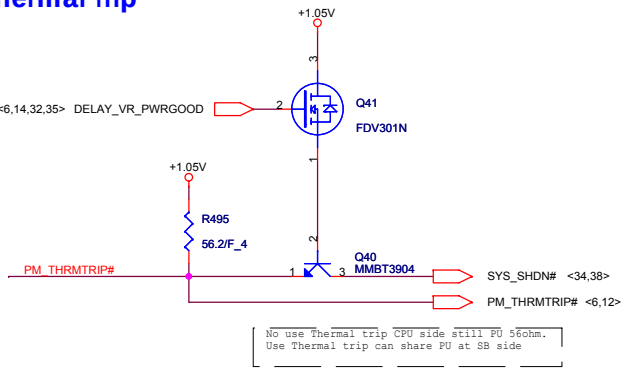
Quanta Computer Inc.

PROJECT : ZY2 & ZY6

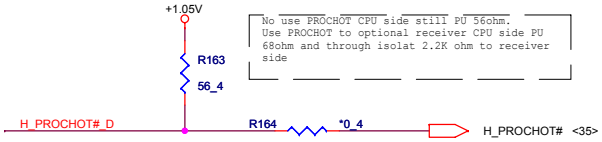
Size	Document Number	Rev
	CLOCK GENERATOR CK505 W/REGULATOR	1A
Date: Tuesday, April 08, 2008	Sheet 2 of 40	



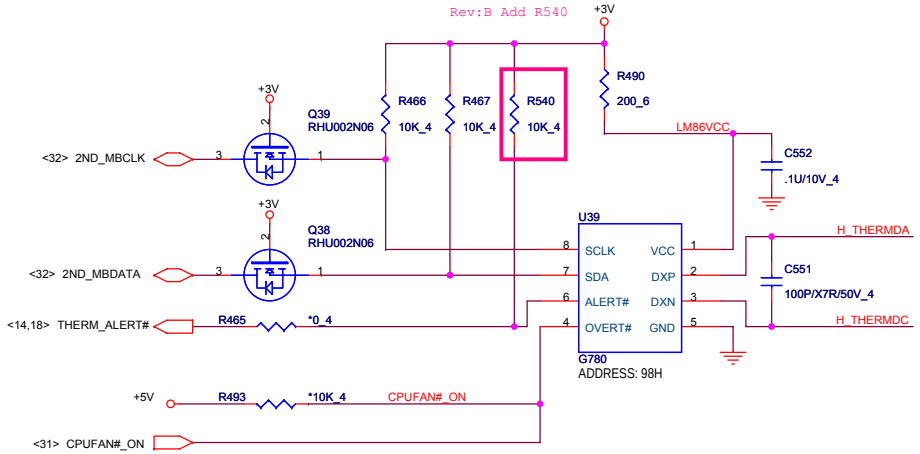
Thermal Trip



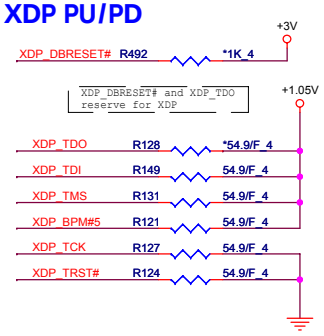
Processor hot



CPU Thermal monitor

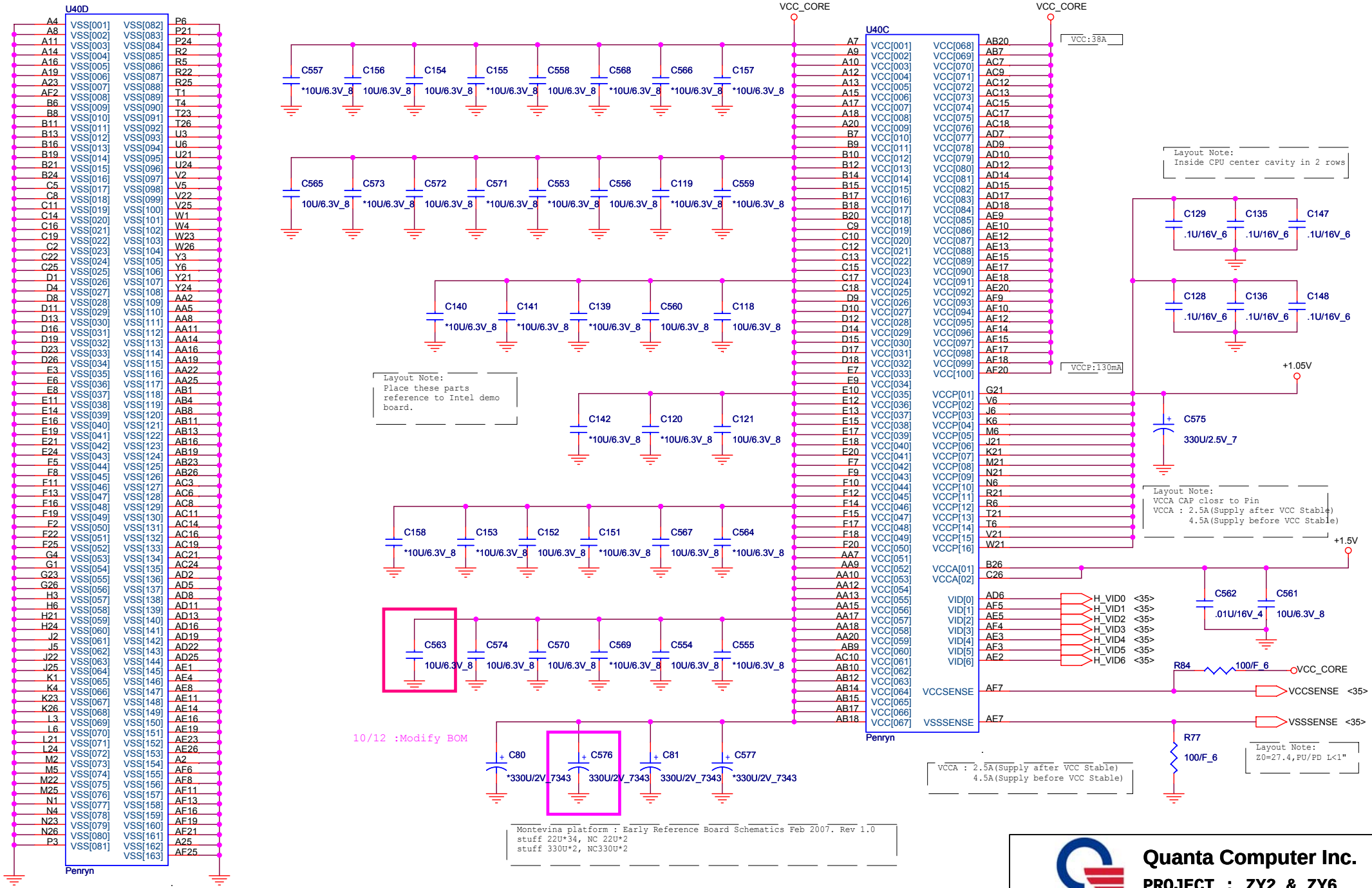


XDP PU/PD



Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	CPU Host Bus	1A
Date: Tuesday, April 08, 2008	Sheet 3 of 40	

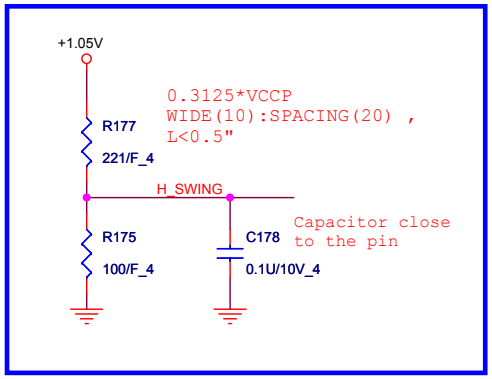


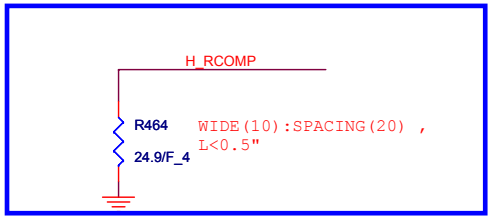
Quanta Computer Inc.

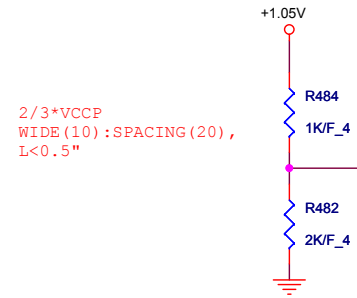
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	CPU Power	1A
Date: Tuesday, April 08, 2008	Sheet 4 of 40	

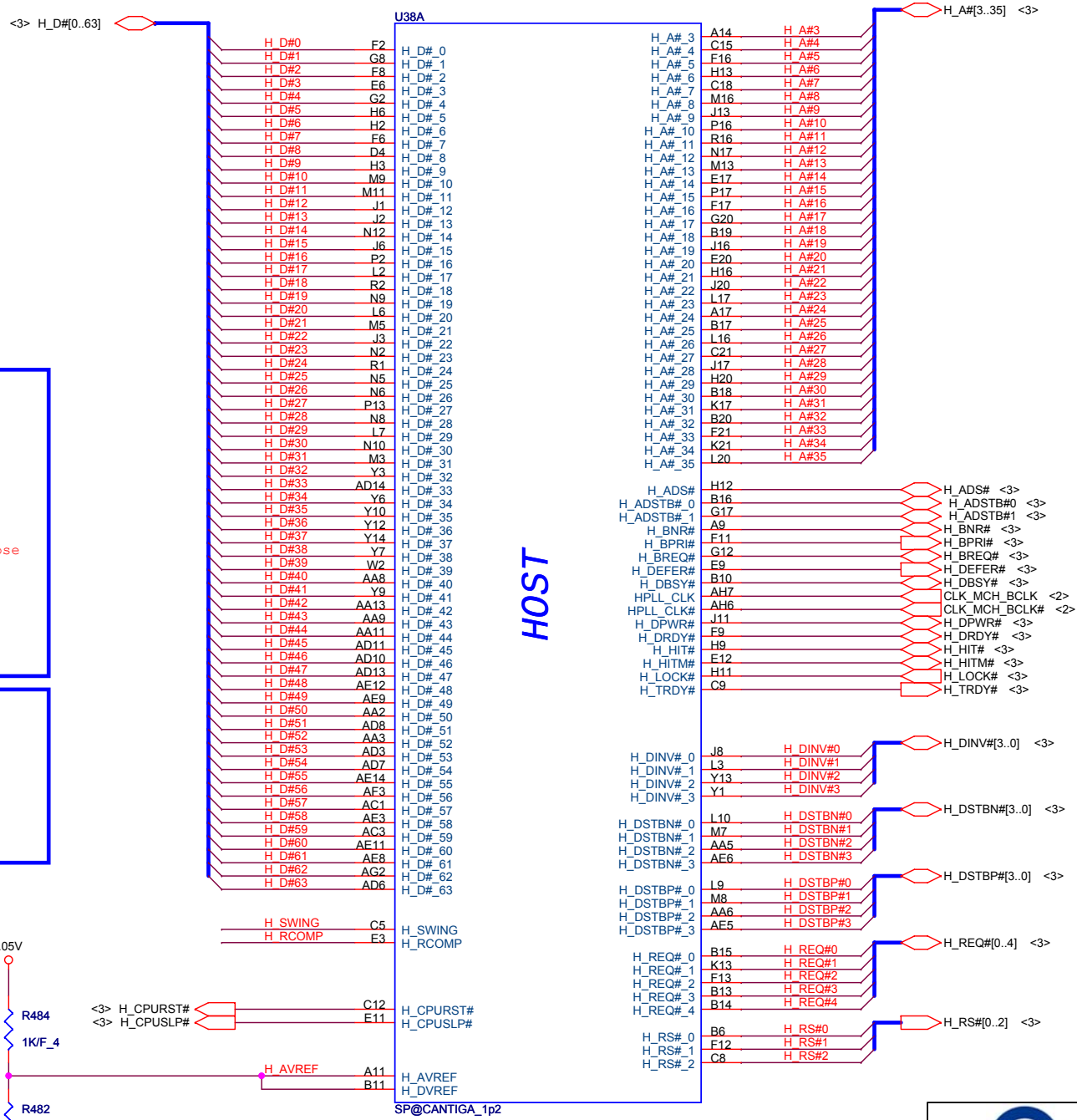
	QCI P/N
Intel Cantiga (G)M	AJ0QT620T01
Intel Cantiga (P)M	AJ0QT780T03







2/3*VCCP
WIDE(10):SPACING(20),
L<0.5"



Quanta Computer Inc.

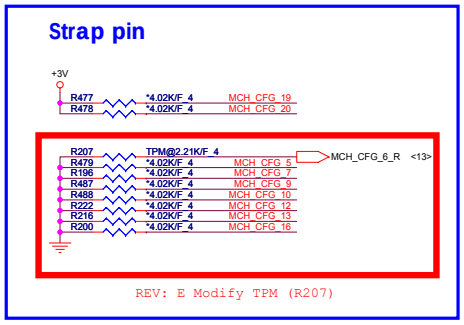
PROJECT : ZY2 & ZY6

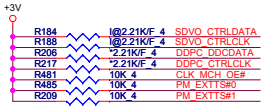
Size	Document Number	Rev
	GMCH HOST	1A
Date: Tuesday, April 08, 2008	Sheet 5 of 40	

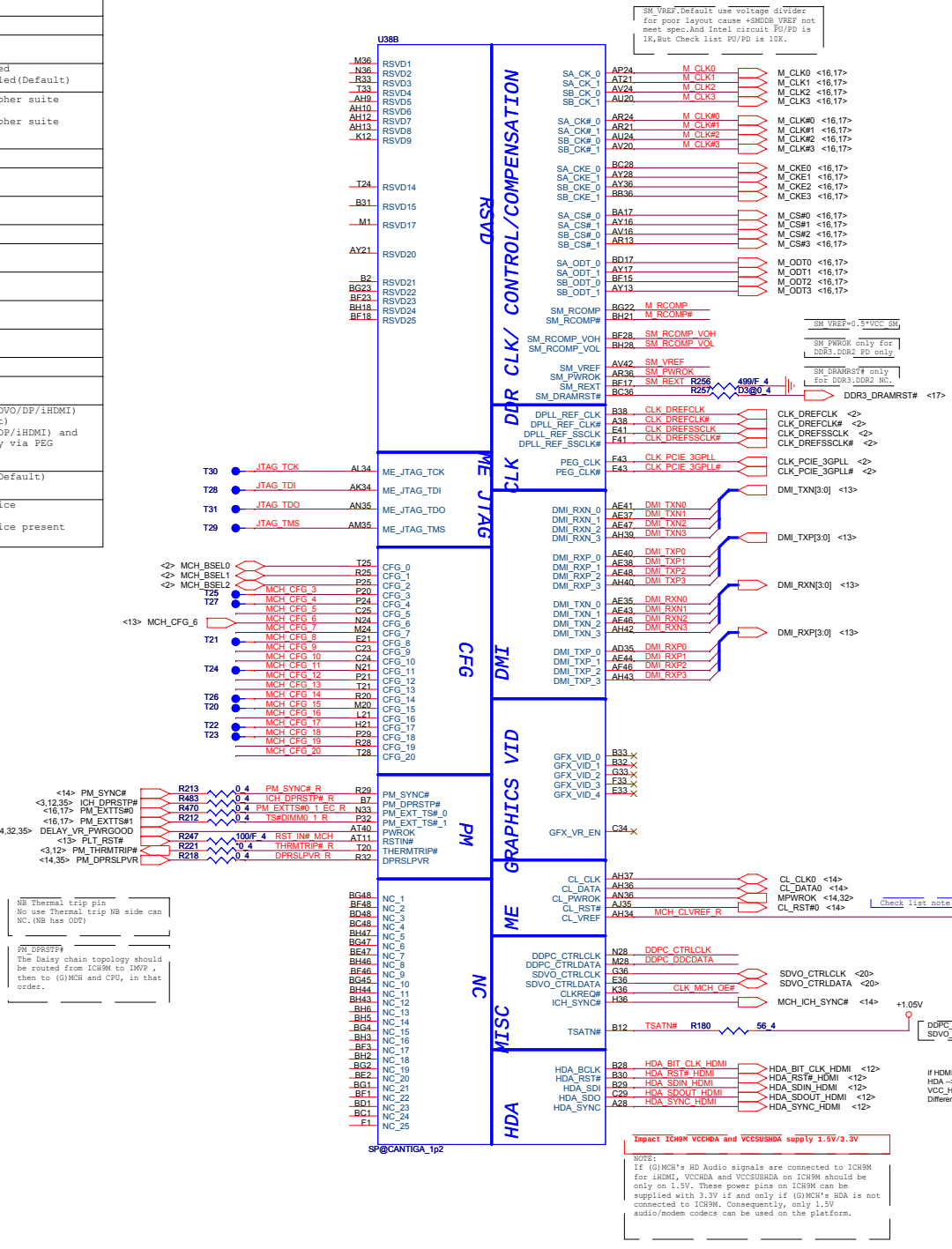
Strap table

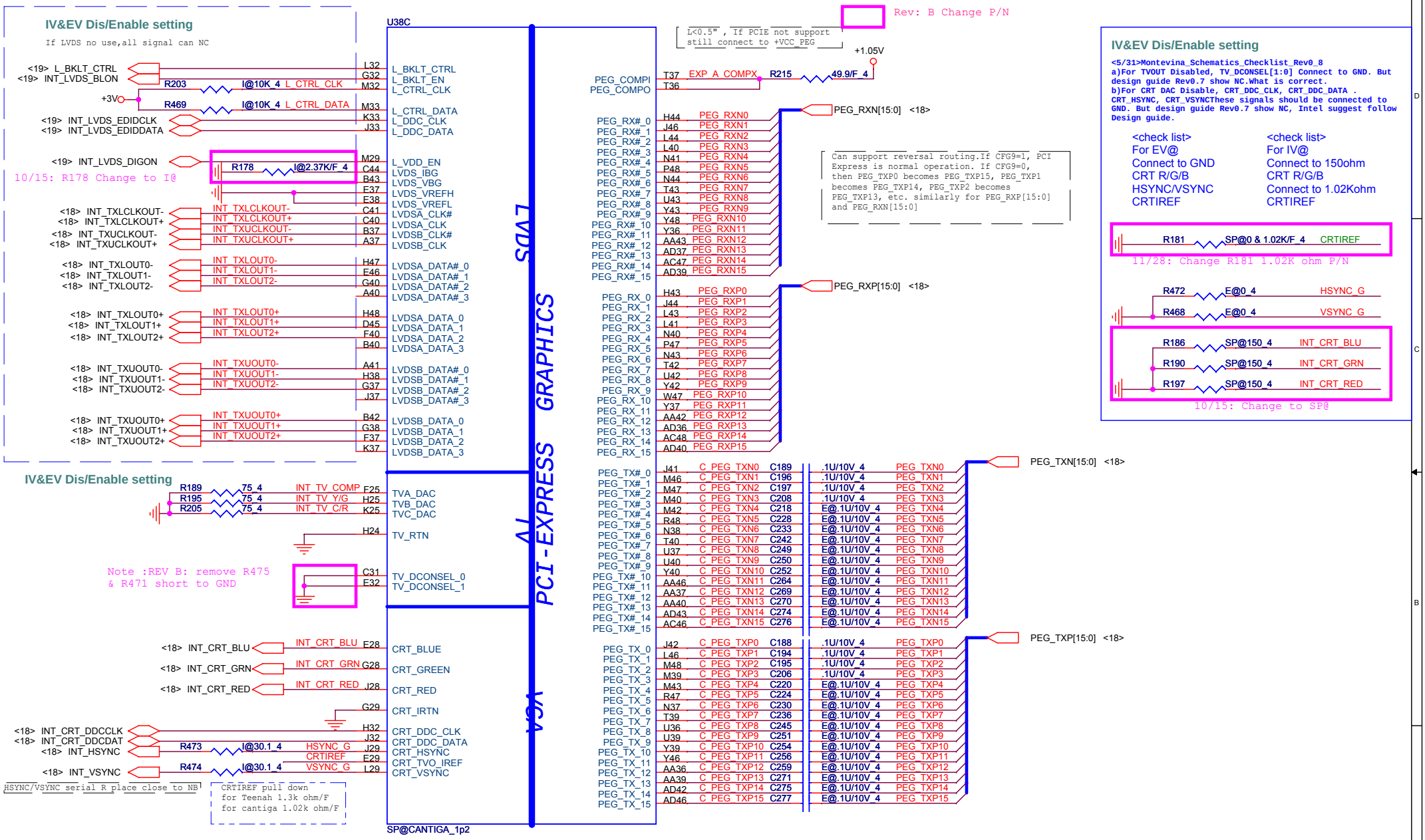
Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	000= FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)
CFG7	ME TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)
CFG8	Reserved	
CFG9	PCIE Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG10	PCIE Loopback enable	0 = Enabled 1 = Disabled (Default)
CFG11	Reserved	
CFG12	ALLZ	0 = ALLZ mode enable 1 = disable(Default)
CFG13	XOR	0 = XOR mode enable 1 = disable(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display port (SDVO/DP/iHDMI) or PCIE is operational (Default) 1 = Digital Display port (SDVO/DP/iHDMI) and PCIE are operating simultaneously via PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/HDMI Device Present(Default) 1 = SDVO/HDMI Device present
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent(Default) 1 = Digital display(HDMI/DP) device present

Strap pin







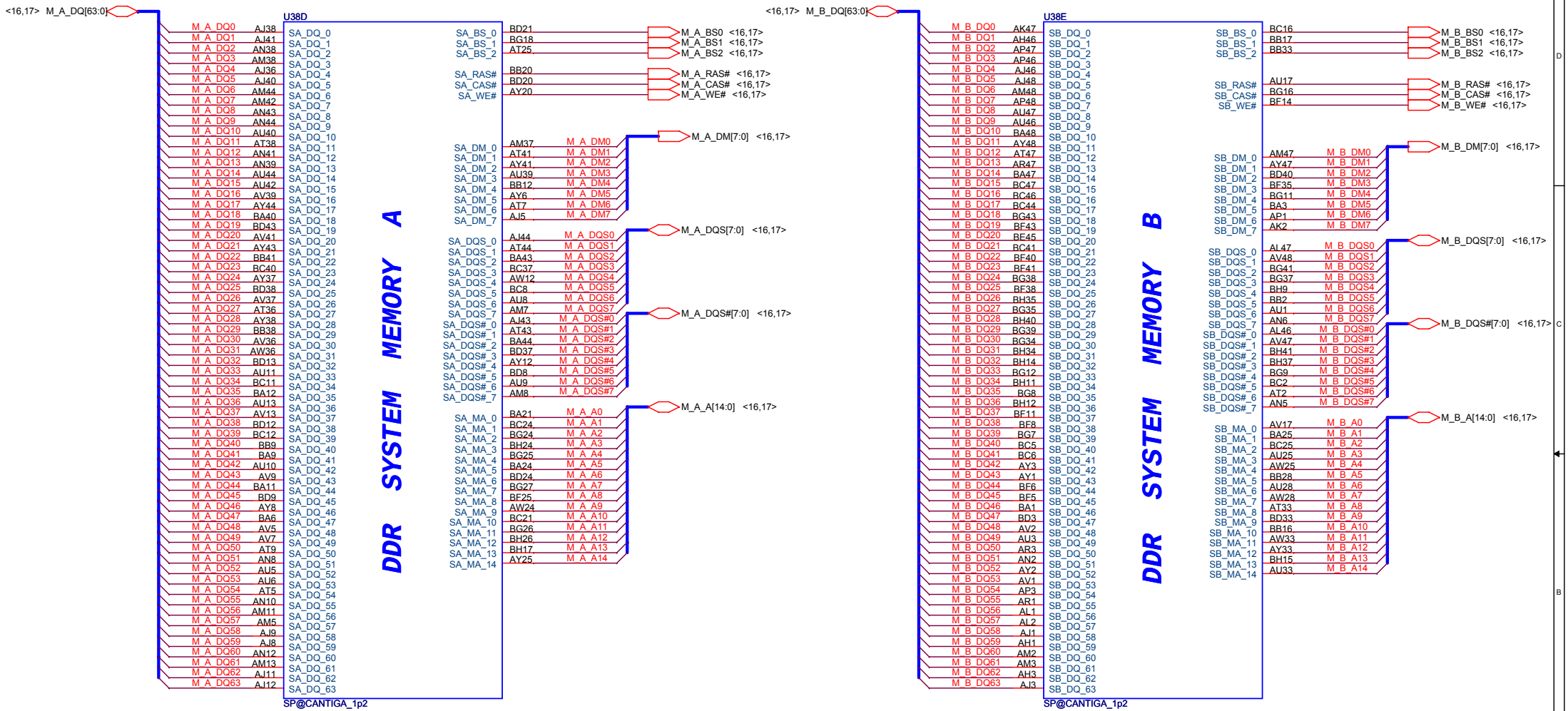


Quanta Computer Inc.

PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	GMCH VGA	1A

Date: Tuesday, April 08, 2008 Sheet 7 of 40



Quanta Computer Inc.

PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	GMCH DDRII	1A
Date: Tuesday, April 08, 2008	Sheet 8 of 40	

Power consumption reference to Intel
644135 Cantiga chipset EDS Volume1.
Section 10

GM TDP 10.5~12W
GS TDP 7~8W
PM TDP 7W

VCC
VCC_NCTF
1210.34mA_EV
1930.4mA_IV
ME Engine
508.12mA
Total Max=2438.52mA

Intel check list(Rev 0.8)
270U*1 near to power(+V1.05M).
270U*2 near to NB
Intel CRB(Rev 0.7)
270U*3 near to power(+V1.05M).
270U*1 near to NB
ESR=12m ohm

Intel check list(Rev 0.8)
No description for VCC_SM bulk CAP
Intel CRB(Rev 0.7)
330U*1 Reserve near to power
330U*1 near to NB

+VDR_SUS
C519 22U/6V_8
C521 22U/6V_8
C244 0.1U/10V_4
C518 330U/2.5V_7
Place on the edga

U38G

VCC_SM(1.8V)
DDR2(800M)
3000mA_S0 , 1mA_S3
DDR2(667M) : 2600mA_S0
DDR3(1067M) : 4140mA_S0

VCC SM POWER
VCC_SM_1 … VCC_SM_42/NC

VCC GFX NCTF
VCC_AXG_NCTF_1 … VCC_AXG_NCTF_60

+1.05V_AXG

1.05V
Graphics core
VCC_AXG
VCC_AXG_NCTF
6326.84mA

Voltage regulator is shared between the Graphics Core Rail, VCCA_HPLL, VCCA_MPLL, VCCA_PEG_PLL/VCCD_PEG_PLL, VCCA_SM_CK, VCCA_DPLLA, VCCA_DPLLB, VCCD_HPLL, VCCA_SM, VCC_AXF

VCC GFX
VCC_AXG_1 … VCC_AXG_42

R242 I@10/F_4
R238 I@10/F_4
VCC_AXG_SENSE
VSS_AXG_SENSE

1. Route VCC_AXG_SENSE and VSS_AXG_SENSE differentially
2. VCC_AXG_SENSE PU to +VGFX_CORE_INT with 10ohm
and VSS_AXG_SENSE PD with 10ohm for Intel suggest

SP@CANTIGA_1p2

VCC SM LF
VCC_SM_LF1 … VCC_SM_LF7

1.8V
Internal connect to power

C268 .1U/10V_4
C239 .1U/10V_4
C255 .22U/6V_4
C253 .22U/6V_4
C238 .47U/6V_4
C266 1U/6V_4
C258 1U/6V_4

+1.05V
C231 .1U/10V_4
C225 .22U/6V_4
C226 .22U/6V_4
C210 22U/6V_8
C524 330U/2.5V_7
Place close to the GMCH

U38F
VCC CORE POWER
VCC_1 … VCC_35
SP@CANTIGA_1p2

VCC NCTF
VCC_NCTF_1 … VCC_NCTF_44

+1.05V
R227 I@0_8
R228 I@0_8

IV&EV Dis/Enable setting
SP@:INT 1 U
EXT 0 ohm
Design guide(Table 72)
For INT VGA disable.VCC_AXG power can connect to GND

C191 I@330U/2.5V_7343
C192 I@330U/2.5V_7343
C200 I@.47U/6V_4
C237 SP@0_6
C217 I@10U/10V_8
C201 I@22U/6V_8
C247 I@.1U/10V_4
C203 I@.1U/10V_4
Place close to the GMCH
Cavity Capacitors

Intel check list(Rev 0.8)
220U*2 near to NB(ESR=15m ohm)
Intel CRB(Rev 0.7)
270U*4 near to power(+V1.05S).
330U*2 near to NB

Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	GMCH VCC,NCTF	1A

Date: Tuesday, April 08, 2008 Sheet 9 of 40

Power consumption reference to Intel 644135 Cantiga chipset EDS Volume1. Section 10

IV&EV Dis/Enable setting Design guide Table 72

External Graphics (GMCH Integrated Graphics Disable)

VCCSYNC_CRT	GND
VCCA_CRT_DAC	GND
VCCD_LVDS	GND
VCC_TX_LVDS	GND
VCCA_LVDS	GND
VCCA_TVDAC	GND
VCCD_QDAC	GND
VCCA_DAC_BG	GND
VCC_AXG	GND
VCC_AXG_NCTF	GND

U38H

CRT: VCCA_CRT_DAC_1, VCCA_CRT_DAC_2, VCCA_DAC_BG, VSSA_DAC_BG

PLL: VCCA_DPLLA, VCCA_DPLLB, VCCA_HPLL, VCCA_MPLL

A LVDS: VCCA_LVDS, VSSA_LVDS

A PEG: VCCA_PEG_BG, VCCA_PEG_PLL

A SM: VCCA_SM_1 … VCCA_SM_9

A CK: VCCA_SM_CK_1, VCCA_SM_CK_2, VCCA_SM_CK_3, VCCA_SM_CK_4, VCCA_SM_CK_5, VCCA_SM_CK_NCTF_1, VCCA_SM_CK_NCTF_2, VCCA_SM_CK_NCTF_3, VCCA_SM_CK_NCTF_4, VCCA_SM_CK_NCTF_5, VCCA_SM_CK_NCTF_6, VCCA_SM_CK_NCTF_7, VCCA_SM_CK_NCTF_8

TV: VCCA_TV_DAC_1, VCCA_TV_DAC_2

HDA: VCC_HDA

D TV/CRT: VCCD_TVDAC, VCCD_QDAC, VCCD_HPLL, VCCD_PEG_PLL

LVDS: VCCD_LVDS_1, VCCD_LVDS_2

VTT: VTT_1 … VTT_25

AXF: VCC_AXF_1, VCC_AXF_2, VCC_AXF_3

SM CK: VCC_SM_CK_1 … VCC_SM_CK_4

HV: VCC_HV_1, VCC_HV_2, VCC_HV_3

PEG: VCC_PEG_1 … VCC_PEG_5

DMI: VCC_DMI_1 … VCC_DMI_4

VTTLF: VTTLF1, VTTLF2, VTTLF3

SP@CANTIGA_1p2

POWER

3.3V 73mA

1.05V 64.8mA for A/B

Design guide table 72 VCCA_DPLLA/B always keep to +1.05V(If no use IV dynamic core power)

3.3V 2.68mA

1.8V 13.2mA

1.5V 414uA

1.05V 24mA

1.05V 139.2mA

1.05V 50mA

1.05V DDR2-800 720mA

1.05V DDR2-800 26mA

3.3V 24.15mA for VCCA_TVA_DAC 39.48mA for VCCA_TVB_DAC 24.15mA for VCCA_TVC_DAC Total 87.78mA

1.5V 50mA

1.5V 58.67mA

1.5V 48.363mA for CRT 5mA for TV

1.05V 157.2mA

VCCD_QDAC share to TV and CRT

1.05V 50mA

1.8V 60.31mA

1.05V FSB-1067 852mA

1.05V 321.35mA

1.8V DDR2-800 124mA

3.3V 105.3mA

1.8V 118.8mA

1.05V 1782mA

1.05V 456mA

1.05V Internal connect to power

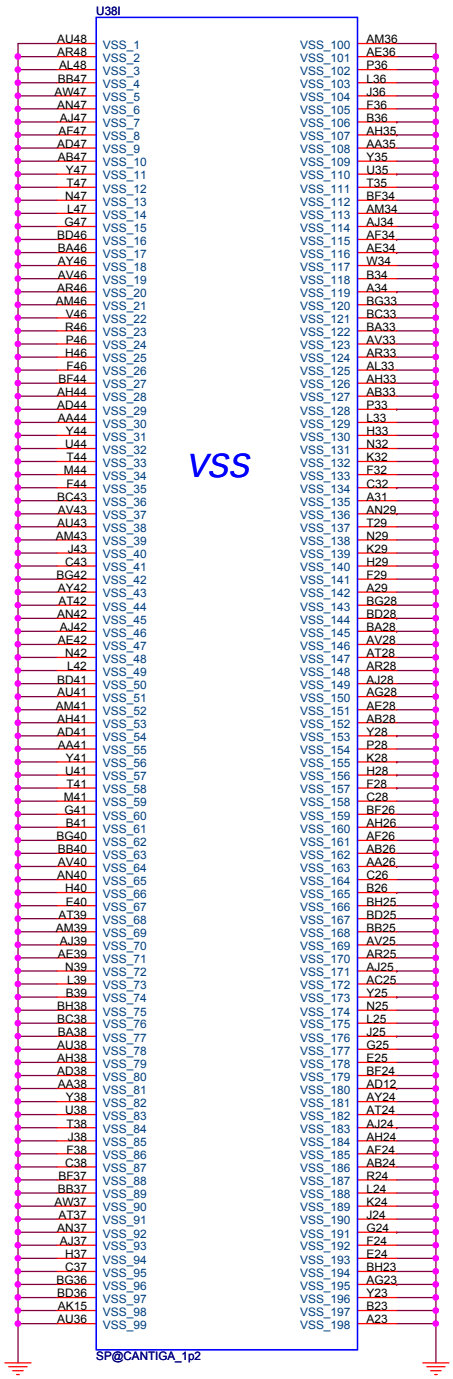
Power Rail Differences between the Teenah and Cantiga Chipset Family

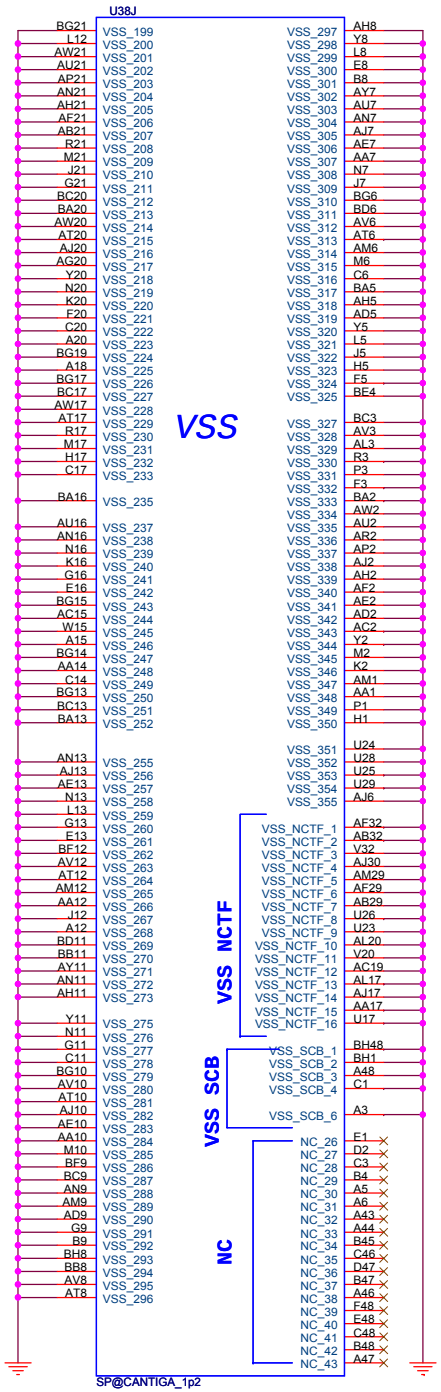
Power Net Name	Cantiga(V)	Tennah(V)	Tennah Current
VCC_AXG_# VCC_AXG_NCTF_#	1.05V	1.25V	6326.84mA Cantiga use
VCCA_PEG_BG	1.5V	3.3V	400uA
VCCA_DPLLA	1.05V	1.25V	100mA
VCCA_DPLLB	1.05V	1.25V	100mA
VCCA_SM_#	1.05V	1.25V	1065mA
VCCA_HPLL	1.05V	1.25V	50mA
VCCA_MPLL	1.05V	1.25V	150mA
VCCA_SM_CK_#	1.05V	1.25V	35mA
VCCA_PEG_PLL	1.05V	1.25V	100mA
VCC_AXF_#	1.05V	1.25V	495mA
VCCD_HPLL	1.05V	1.25V	250mA
VCCD_PEG_PLL	1.05V	1.25V	100mA

Quanta Computer Inc.
PROJECT : ZY2 & ZY6

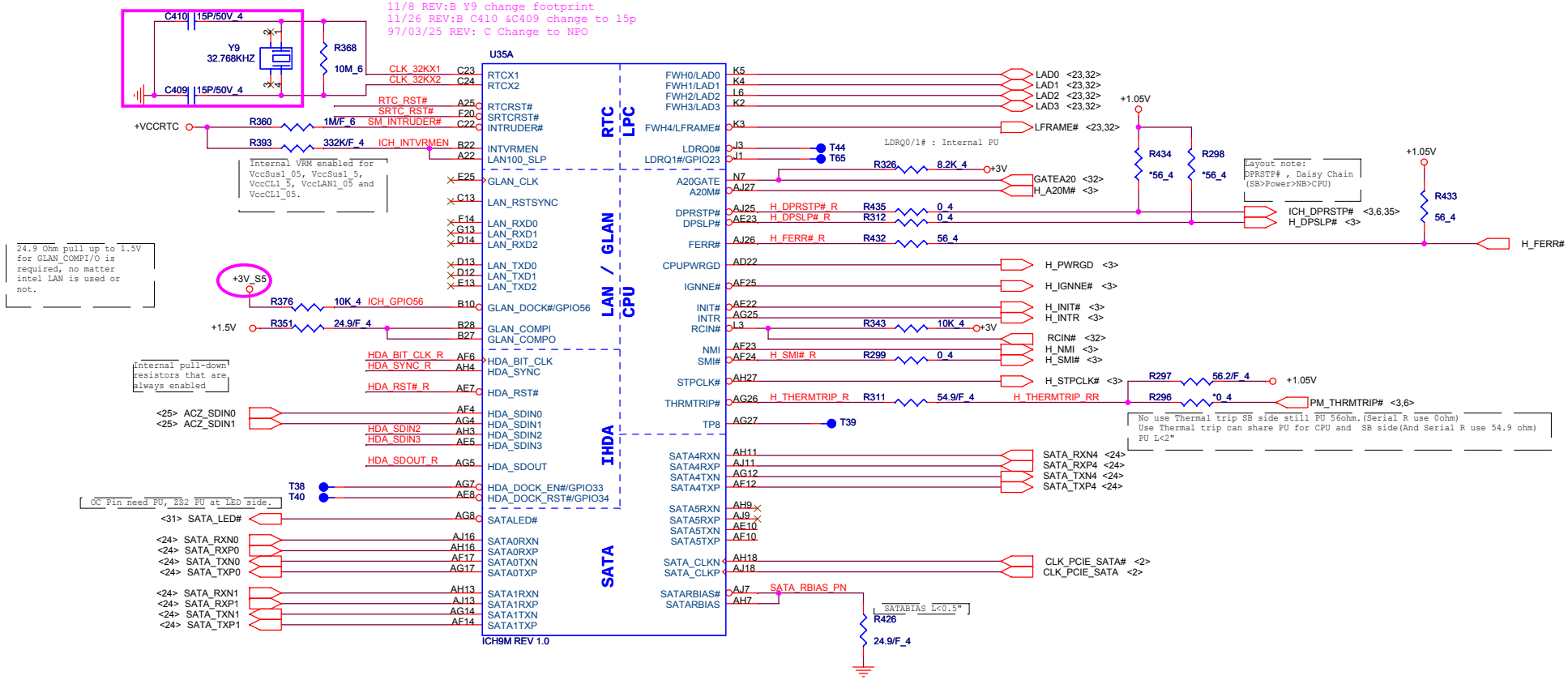
Size	Document Number	Rev
	GMCH POWER	1A

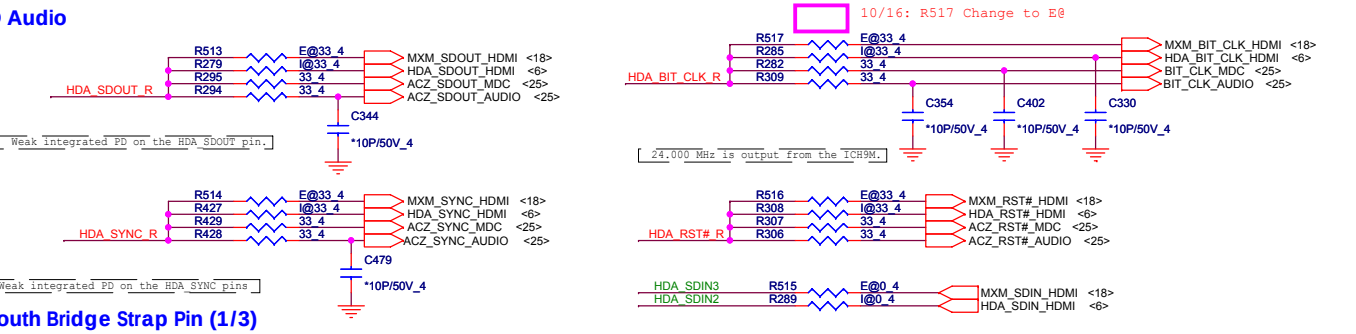
Date: Tuesday, April 08, 2008 Sheet 10 of 40





Quanta Computer Inc.	
PROJECT : ZY2 & ZY6	
Size	Document Number: GMCH VSS
Rev	1A
Date: Tuesday, April 08, 2008	Sheet 11 of 40

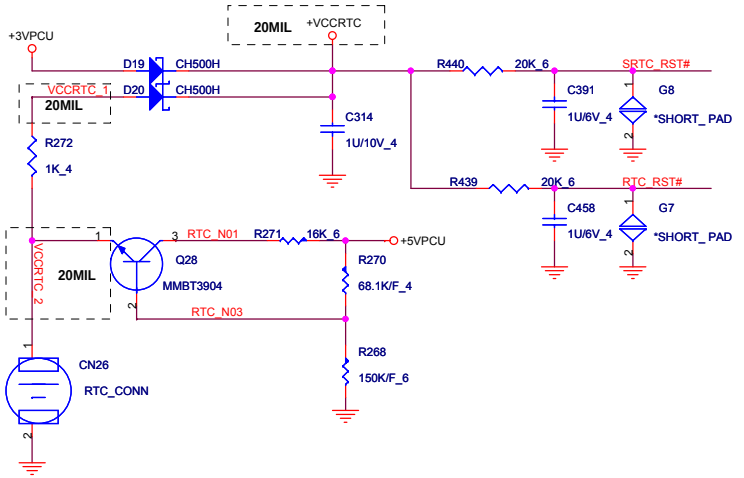




South Bridge Strap Pin (1/3)

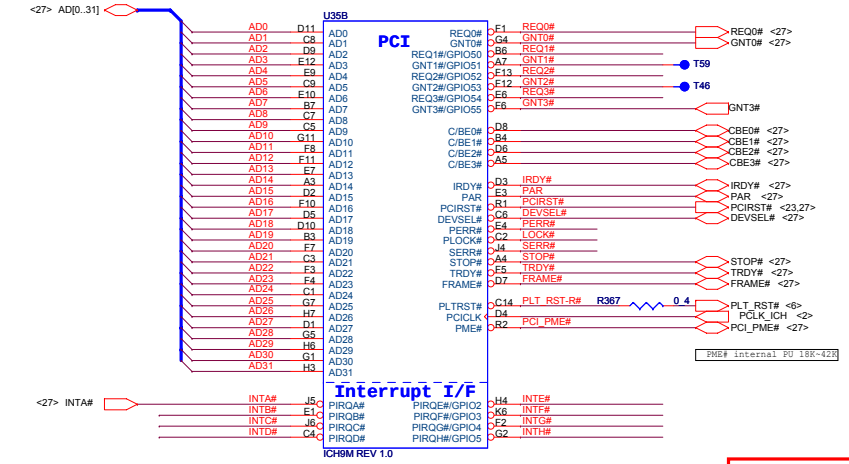
Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect	This strap should only be enabled in manufacturing environments using an external pull-up resistor.
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU	
TP3	XOR Chain Entrance	PWROK	ICH_TP3 / HDA_SDOUT / Description 0 / 0 / RSVD 0 / 1 / Enter XOR Chain 1 / 0 / Normal opration(Default) 1 / 1 / Set PCIE port config bit 1	<14> ICH_TP3 — ICH_TP3 — R406 — *1K_4
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK		HDA_SDOUT_R — R310 — *1K_4 — +3V

RTC

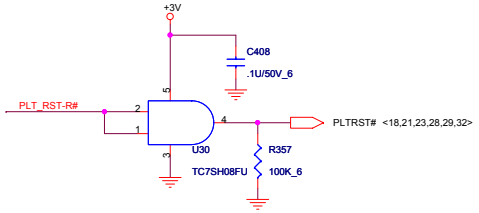


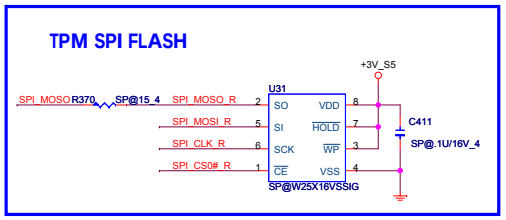
Quanta Computer Inc.
PROJECT : ZY2 & ZY6

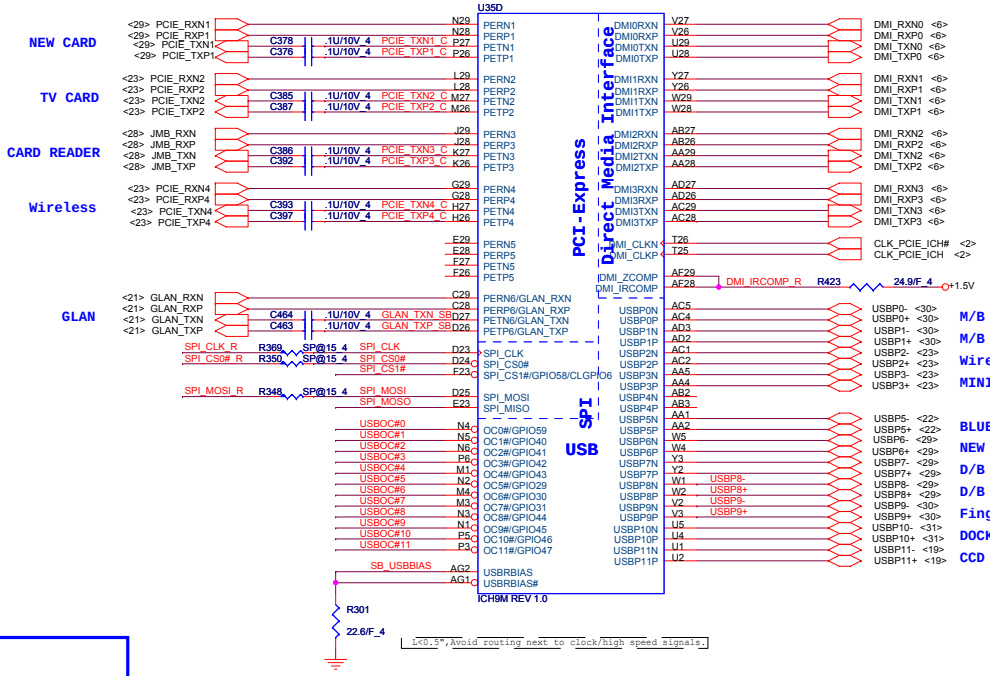
Size	Document Number	Rev
	ICH9M HOST	1A
Date: Tuesday, April 08, 2008	Sheet 12 of 40	



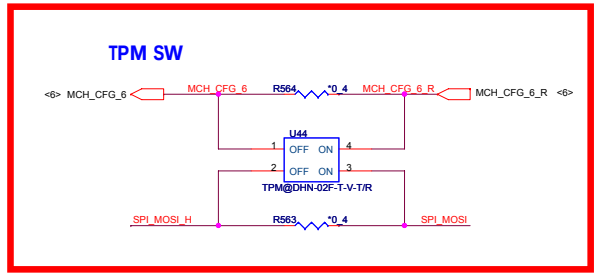
TM & AS	Y
LOW COST	N





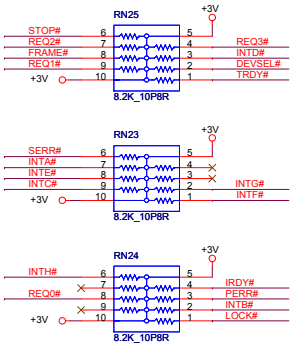


PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD20	INTA#	OZ601T



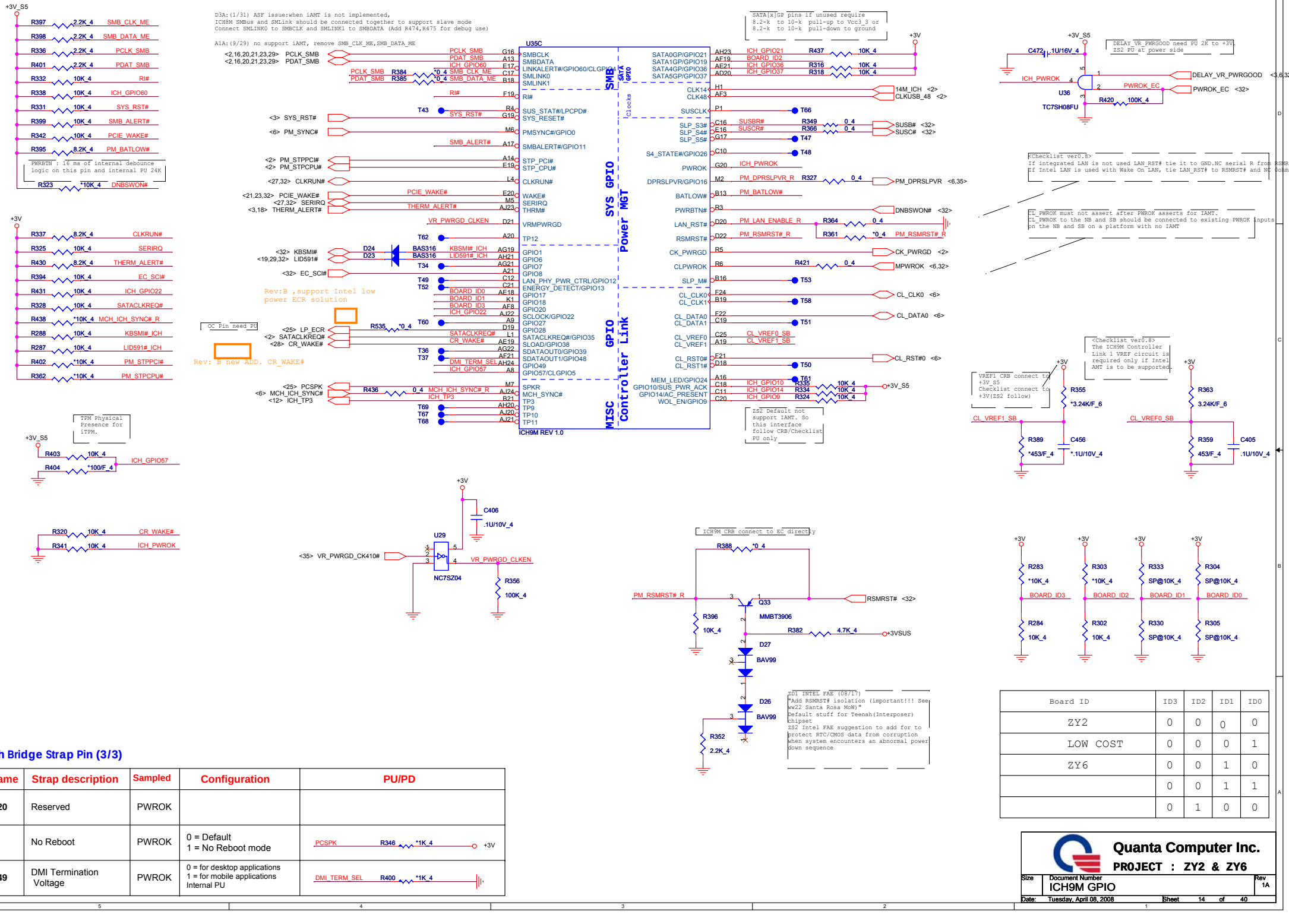
South Bridge Strap Pin (2/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0	
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default	
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default	GNT3# R347 *1K_4
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable	SPI_MOSI_H R329 TPM@10K_4 +3V_S5
GNT0#	Boot BIOS Selection 0	PWROK	PCI_GNT#0 / SPI_CS#1 / Boot Location 0 / 1 / SPI(Default) 1 / 0 / PCI 1 / 1 / LPC	GNT0# R344 *1K_4
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK		SPI_CS1# R340 *1K_4



Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	ICH9M PCIE / PCI / USB	1A
Date: Wednesday, April 09, 2008	Sheet 13 of 40	



South Bridge Strap Pin (3/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
SPKR	No Reboot	PWROK	0 = Default 1 = No Reboot mode	PCSPK R346 *1K_4 +3V
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	DMI_TERM_SEL R400 *1K_4

Board ID	ID3	ID2	ID1	ID0
ZY2	0	0	0	0
LOW COST	0	0	0	1
ZY6	0	0	1	0
	0	0	1	1
	0	1	0	0

Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	ICH9M GPIO	1A

Date: Tuesday, April 08, 2008 Sheet 14 of 40

Power consumption reference to Intel
642879 ICH9 Family EDS Rev 1.5

2~3.456v
3.6uA_G3

5V
2mA

5V
2mA_S0
1mA_S3/S4/S5

1.5V
646mA

1.5V
47mA

VCC1_5_A
1.5V
1342mA

1.5V
11mA

1.05V , Powered by VCC1_05 in S0

3.3V
19mA_S0 ,
78mA_S3/S4/S5

1.5V
23mA

1.5V
80mA

3.3V
1mA

1.05V
1634mA

1.5V
23mA

1.05V
50mA

VCCP
2mA

VCC3_3
3.3V
308mA

1.5V / 3.3V
11mA

1.5V / 3.3V
11mA_S0 , 1mA_S3/S4/S5

VCCSUS1_05 power by VCC1_05 in S0 / VCCSUS3_3 in S3/S4/S5
VCCSUS1_5 power by VCC1_5_A in S0 / VCCSUS3_3 in S3/S4/S5

3.3V
212mA_S0 , 53mA_S3/S4/S5

VCCCL1_05 power by VCC1_05_A in S0
VCCCL1_5 power by VCC1_5_A in S0

3.3V
19mA_S0 , 73mA_S3/S4/S5

If use SB MAC for LAN function. And support wake up need connect to relation power.

ZS2 Default not support INT HDMI interface

Impact ICH9M VCCHDA and VCCSUSHDA supply 1.5V/3.3V

Support INT HDMI HDA interface. These power only support 1.5V.Device must to meet.

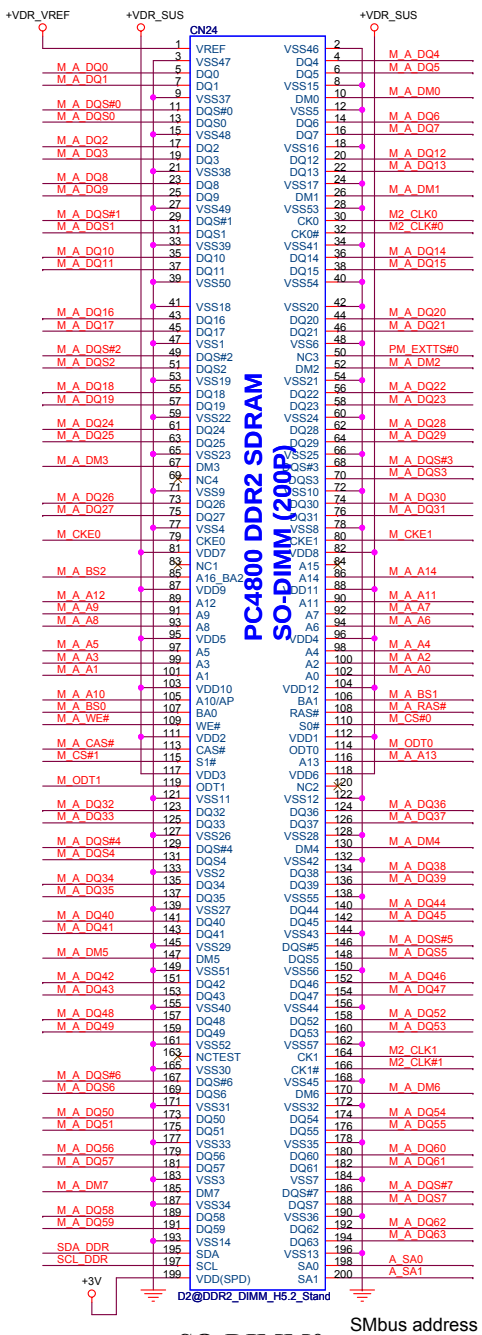
NOTE:
If (G)MCH's HD Audio signals are connected to ICH9M for iHDMI, VCCHDA and VCCSUSHDA on ICH9M should be only on 1.5V. These power pins on ICH9M can be supplied with 3.3V if and only if (G)MCH's HDA is not connected to ICH9M. Consequently, only 1.5V audio/modem codecs can be used on the platform.

U35F — ICH9M REV 1.0

U35E — ICH9M REV 1.0

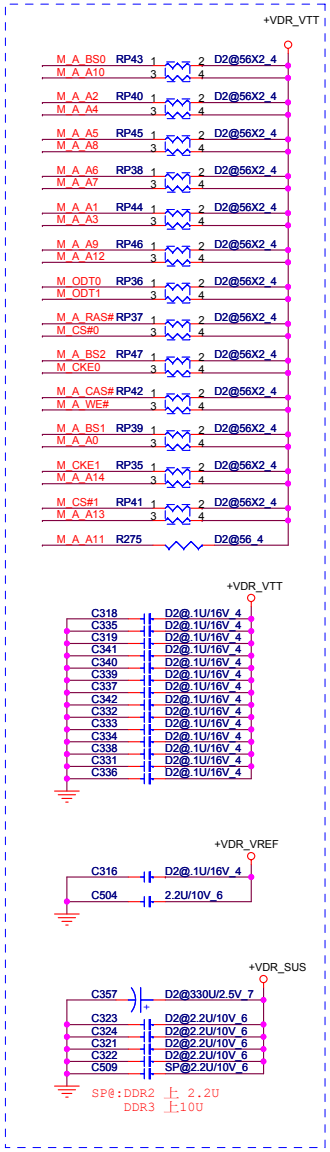
Quanta Computer Inc.		
PROJECT : ZY2 & ZY6		
Size	Document Number: ICH9 POWER	Rev: 1A
Date: Tuesday, April 08, 2008	Sheet 15 of 40	

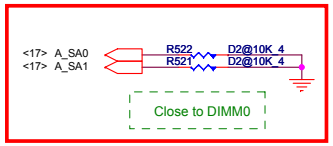
FOR DDR2



SMbus address A0

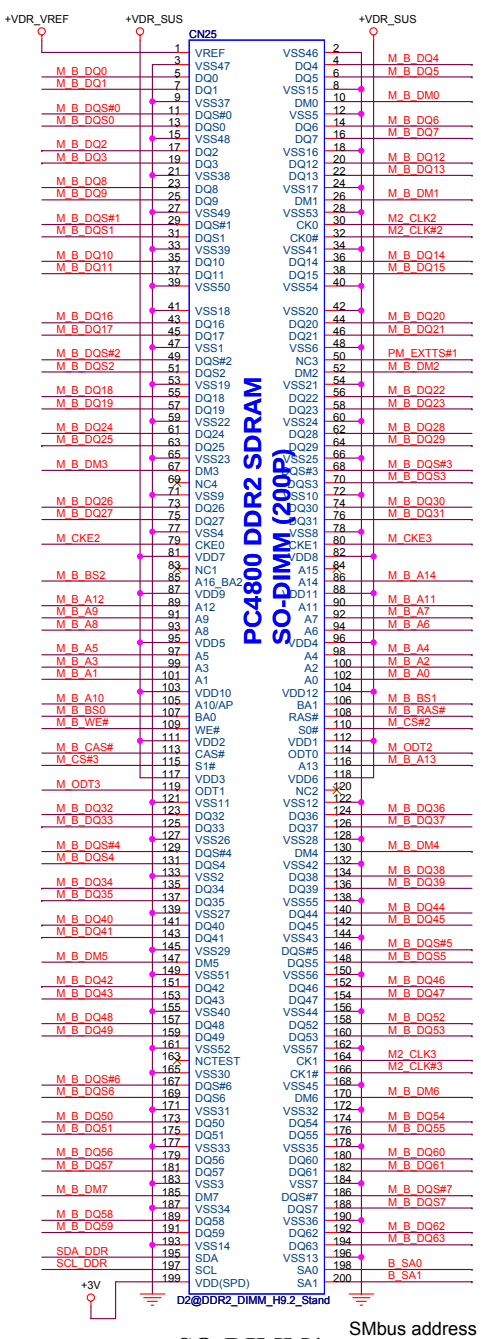
SO-DIMM0





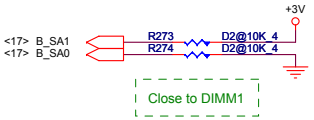
NOTE:Place one cap close to every 2 pull-up resistors terminated to +SMDDR_VTERM

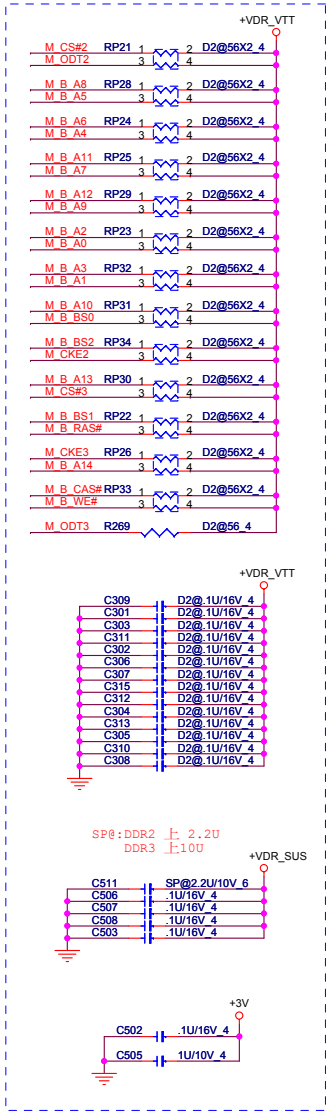
10/16: Change to D2@

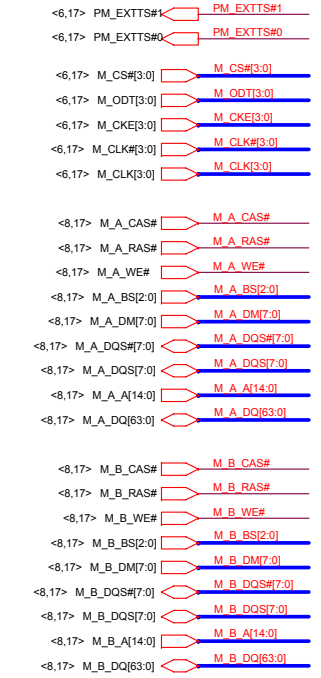


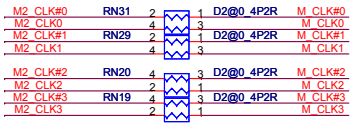
SMbus address A2

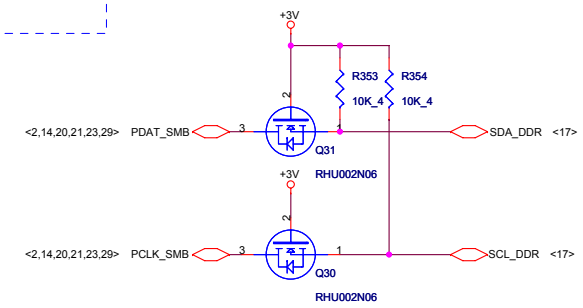
SO-DIMM1



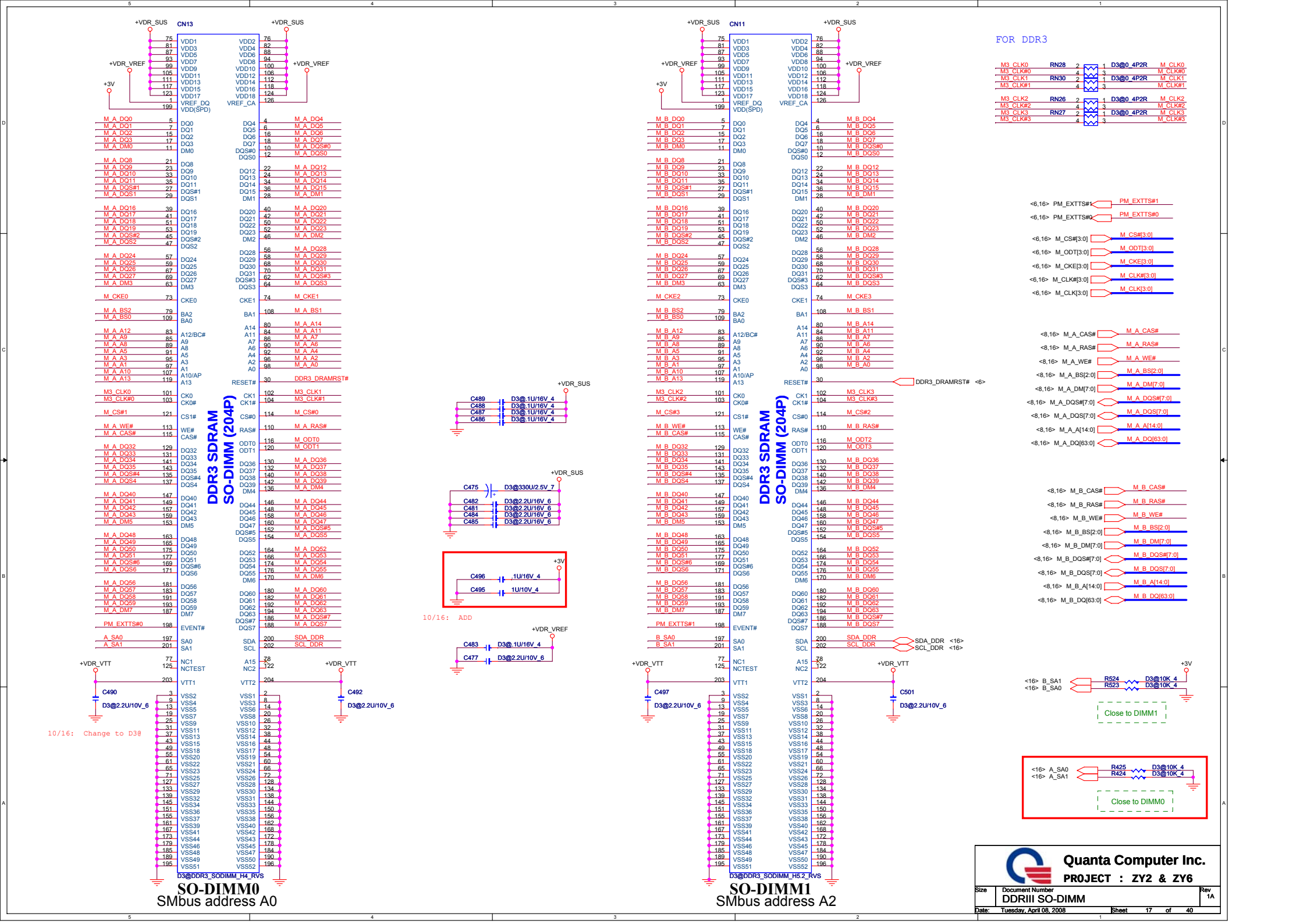


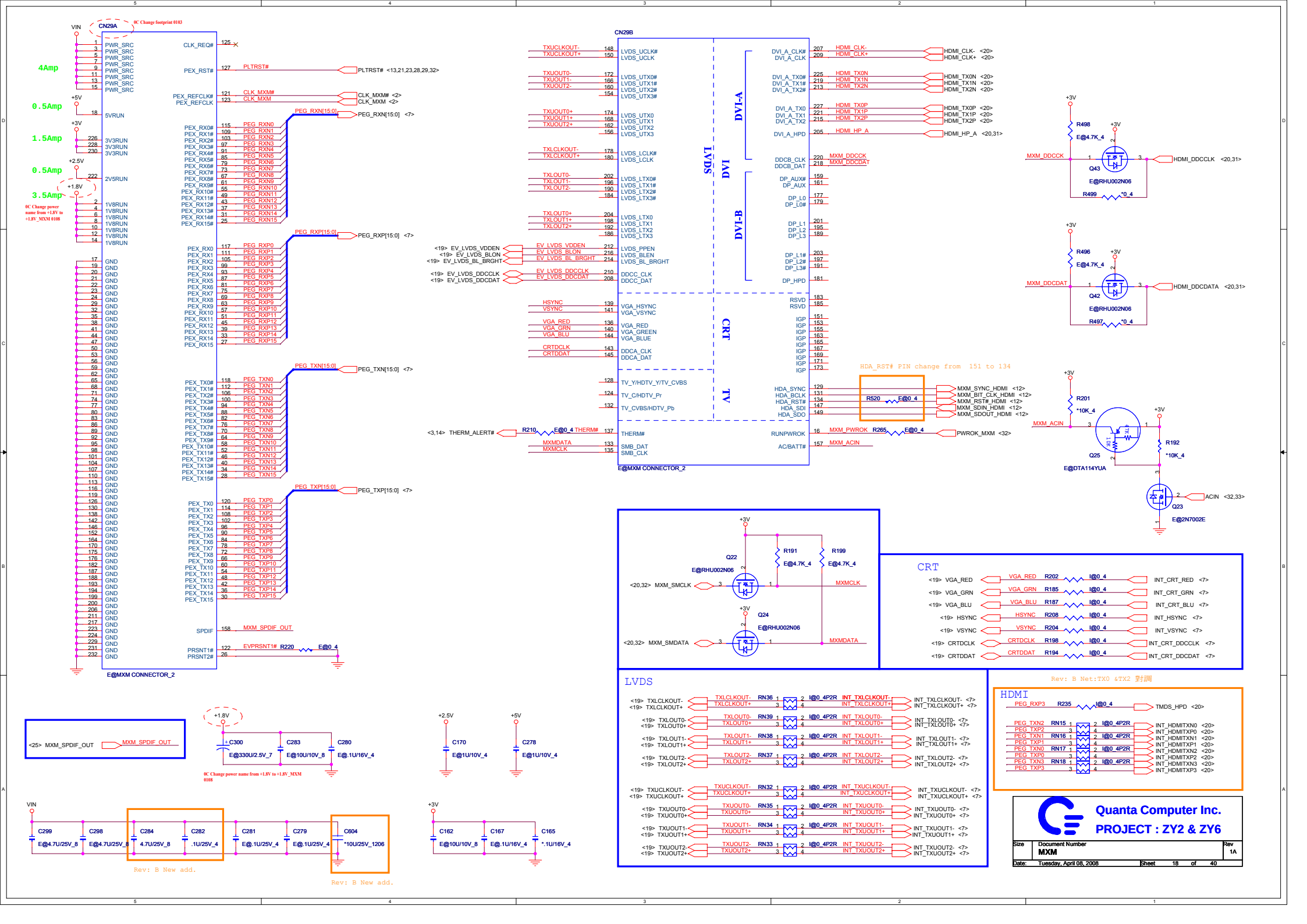






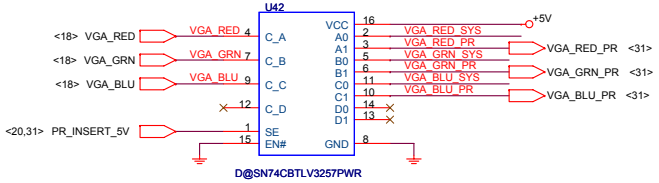
Quanta Computer Inc.		
PROJECT : ZY2 & ZY6		
Size	Document Number: DDRII SO-DIMM	Rev: 1A
Date: Tuesday, April 08, 2008	Sheet 16 of 40	


CN13
CN11
DDR3 SDRAM
SO-DIMM (204P)
+VDR_SUS
+VDR_VREF
+3V
+VDR_VTT
FOR DDR3
M3_CLK0
M3_CLK#0
M3_CLK1
M3_CLK#1
M3_CLK2
M3_CLK#2
M3_CLK3
M3_CLK#3
RN28
RN30
RN26
RN27
D3@0_4P2R
M_CLK0
M_CLK#0
M_CLK1
M_CLK#1
M_CLK2
M_CLK#2
M_CLK3
M_CLK#3
PM_EXTTS#1
PM_EXTTS#0
M_CS#[3:0]
M_ODT[3:0]
M_CKE[3:0]
M_CLK#[3:0]
M_CLK[3:0]
M_A_CAS#
M_A_RAS#
M_A_WE#
M_A_BS[2:0]
M_A_DM[7:0]
M_A_DQS#[7:0]
M_A_DQS[7:0]
M_A_A[14:0]
M_A_DQ[63:0]
M_B_CAS#
M_B_RAS#
M_B_WE#
M_B_BS[2:0]
M_B_DM[7:0]
M_B_DQS#[7:0]
M_B_DQS[7:0]
M_B_A[14:0]
M_B_DQ[63:0]
DDR3_DRAMRST#
SDA_DDR
SCL_DDR
B_SA1
B_SA0
A_SA0
A_SA1
R524
R523
R425
R424
D3@10K_4
Close to DIMM1
Close to DIMM0
C489
C488
C487
C486
D3@1U/16V_4
C475
D3@330U/2.5V_7
C482
C481
C484
C485
D3@2.2U/16V_6
C496
.1U/16V_4
C495
1U/10V_4
10/16: ADD
C483
D3@.1U/16V_4
C477
D3@2.2U/10V_6
C490
C492
C497
C501
10/16: Change to D3@
D3@DDR3_SODIMM_H4_RVS
D3@DDR3_SODIMM_H5.2_RVS
SO-DIMM0
SMbus address A0
SO-DIMM1
SMbus address A2
Quanta Computer Inc.
PROJECT : ZY2 & ZY6
Size
Document Number
DDRIII SO-DIMM
Rev
1A
Date: Tuesday, April 08, 2008
Sheet 17 of 40


CN29A
0C Change footprint 0103
4Amp
0.5Amp
1.5Amp
0.5Amp
3.5Amp
0C Change power name from +1.8V to +1.8V_MXM 0108
E@MXM CONNECTOR_2
CN29B
LVDS
DVI
DVI-A
DVI-B
CRT
TV
E@MXM CONNECTOR_2
HDA_RST# PIN change from 151 to 134
E@RHU002N06
E@DTA114YUA
E@2N7002E
CRT
LVDS
HDMI
Rev: B Net:TX0 &TX2 對調
Quanta Computer Inc.
PROJECT : ZY2 & ZY6
Size
Document Number
MXM
Rev
1A
Date: Tuesday, April 08, 2008
Sheet 18 of 40
0C Change power name from +1.8V to +1.8V_MXM 0108
Rev: B New add.
Rev: B New add.

CRT Select

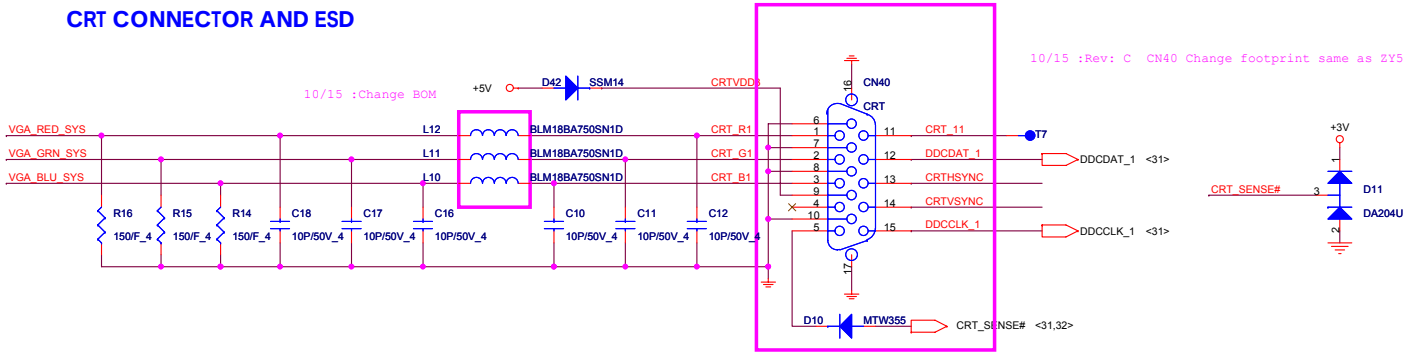
CRT SWITCH

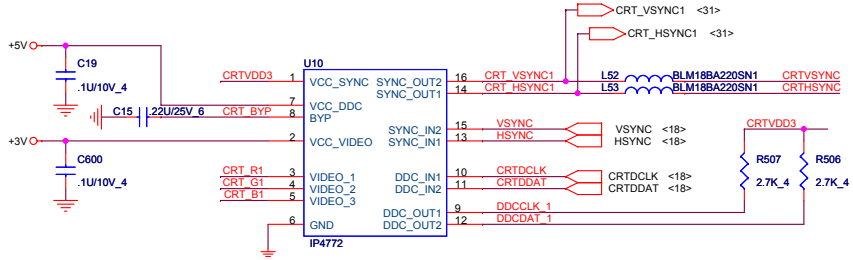


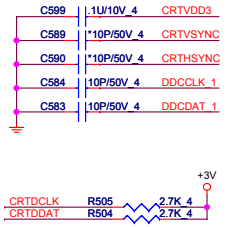
CRT CONNECTOR AND ESD

10/15 :Change BOM

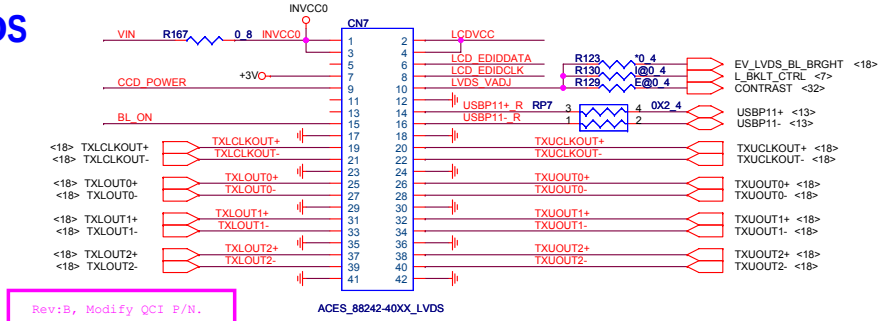
10/15 :Rev: C CN40 Change footprint same as ZY5



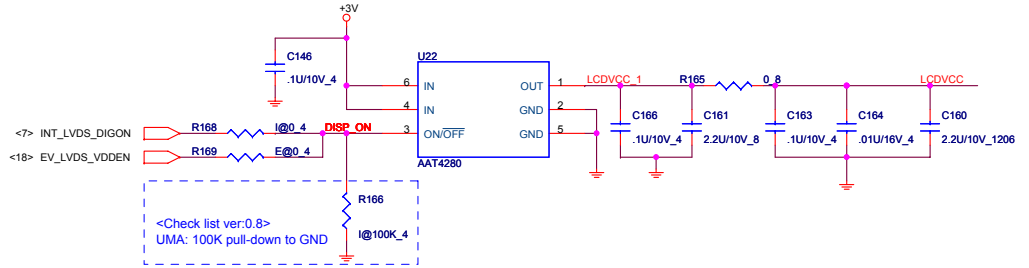




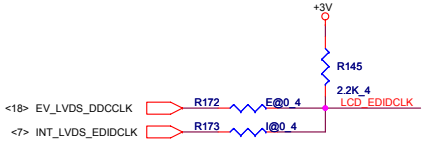
LVDS

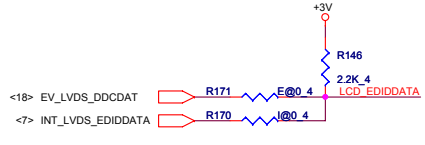


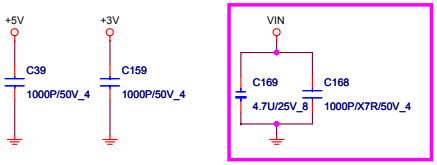
Rev:B, Modify QCI P/N.



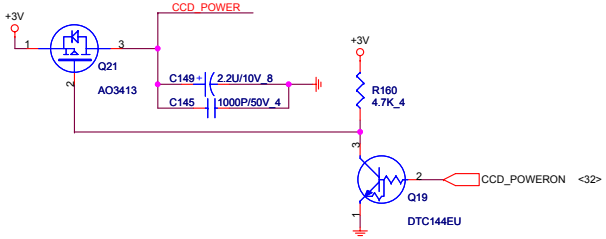
Rev:C, Change to 4.7U 0805



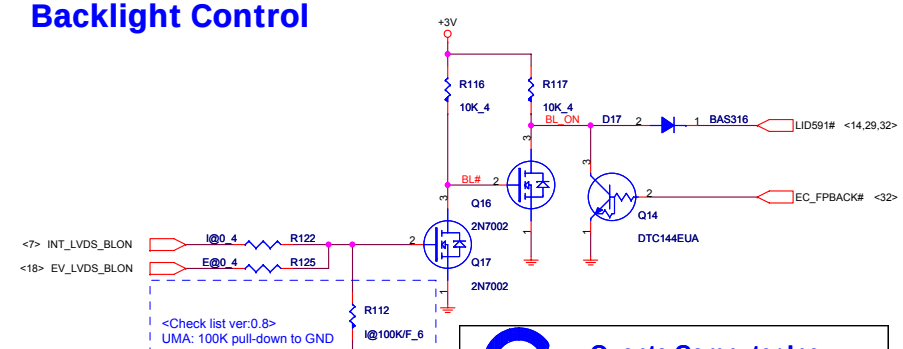




CAMERA MODULE CONNECTOR



Backlight Control

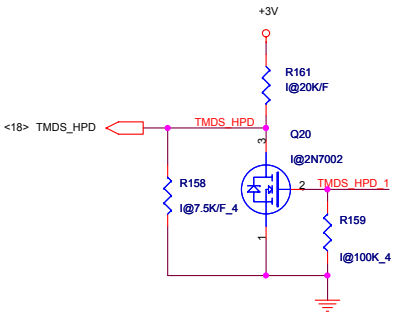


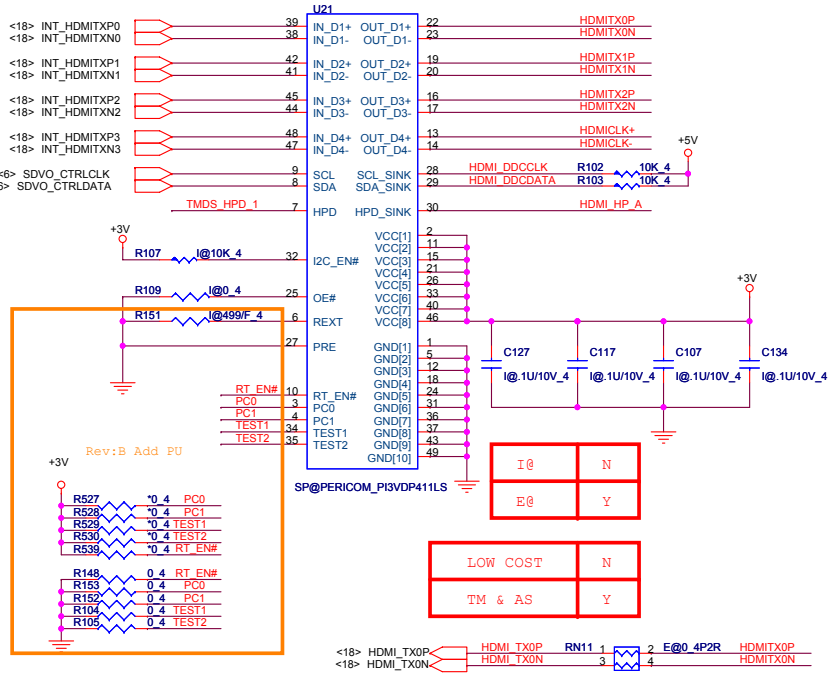
Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	CRT	1A
Date: Tuesday, April 08, 2008	Sheet 19 of 40	

DVI-I CONNECTOR (DVI-D)

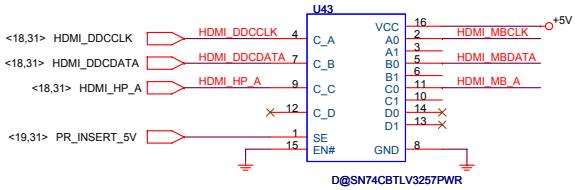
	QCI P/N
PI3VDP411LS	ALP411LS000
Ch7318A	AL007318000
PS8101	

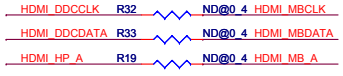


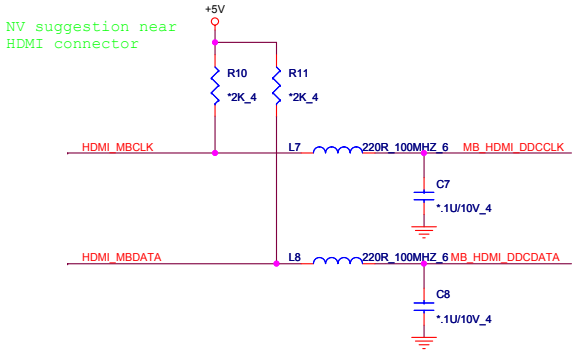


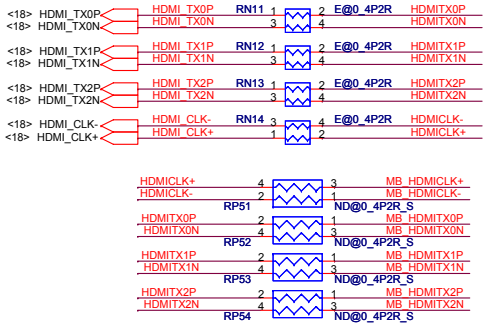
I@	N
E@	Y

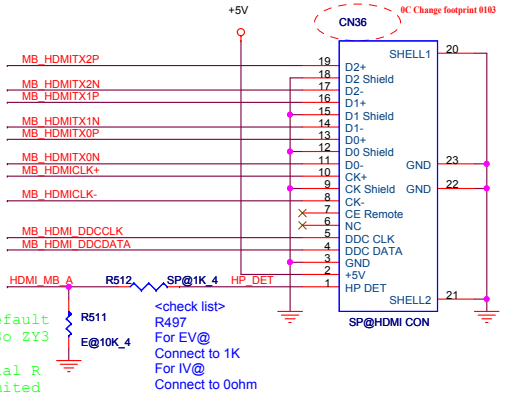
LOW COST	N
TM & AS	Y

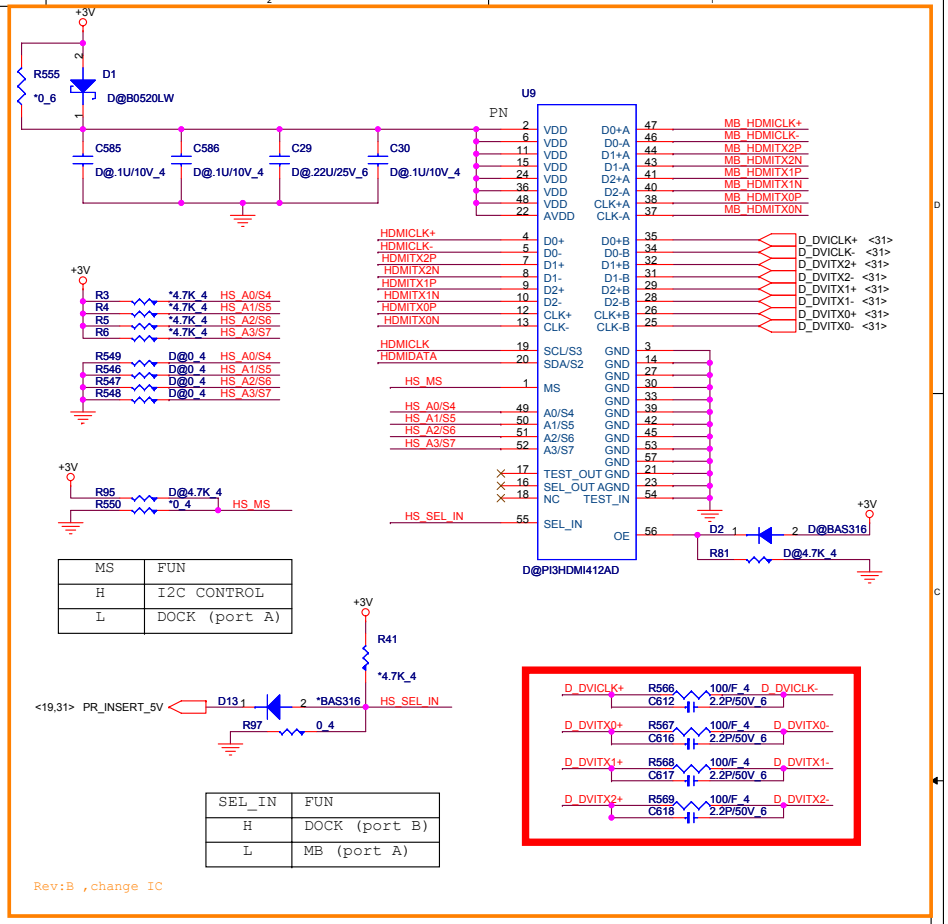






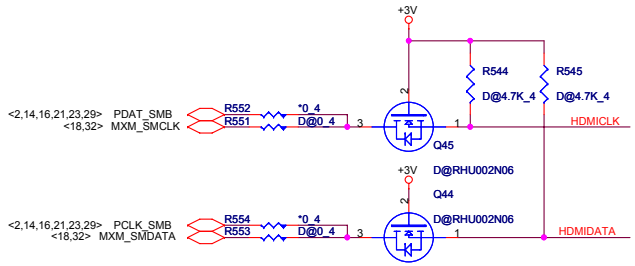




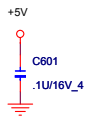


MS	FUN
H	I2C CONTROL
L	DOCK (port A)

SEL_IN	FUN
H	DOCK (port B)
L	MB (port A)



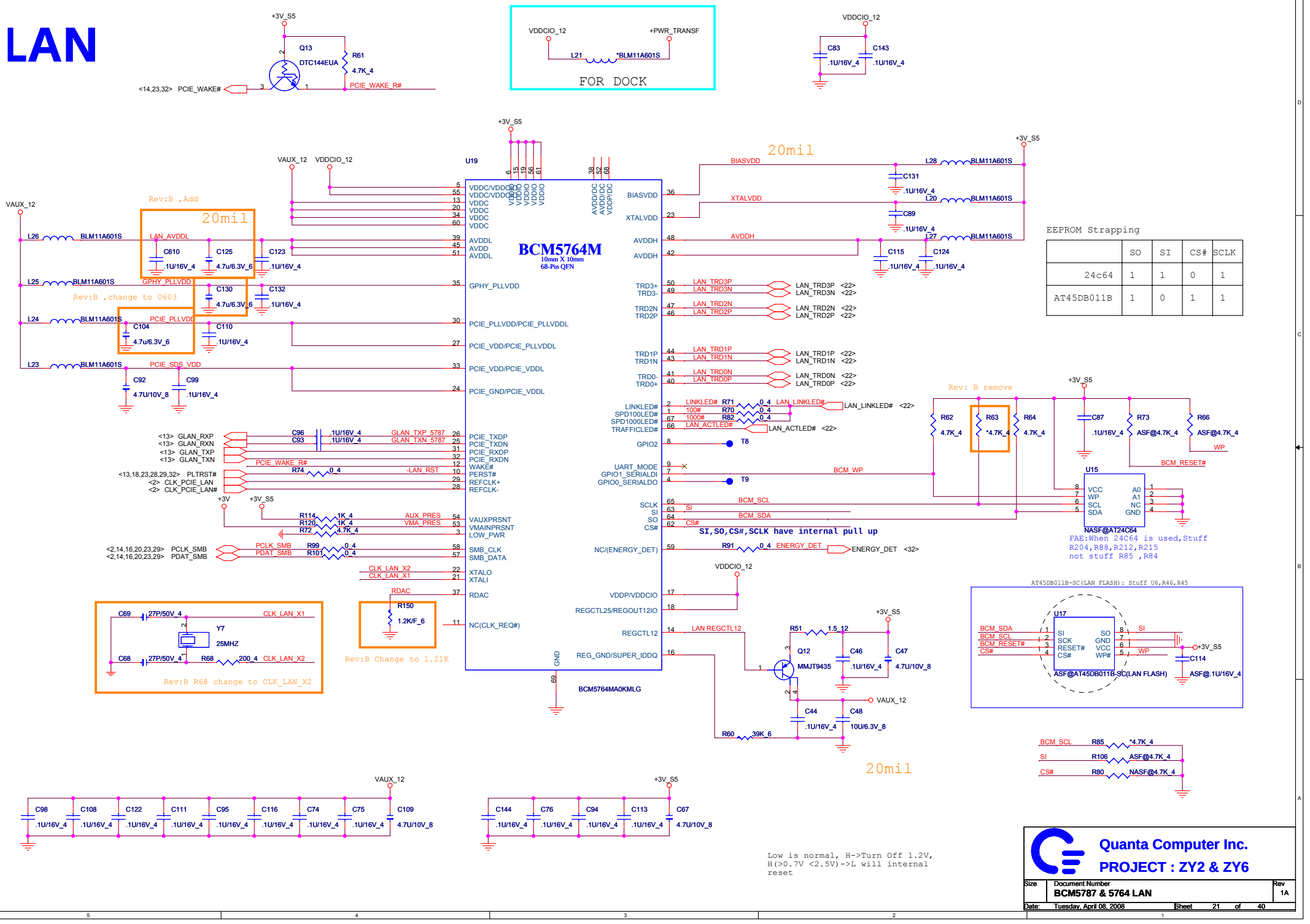
LOW COST	N
TM & AS	Y



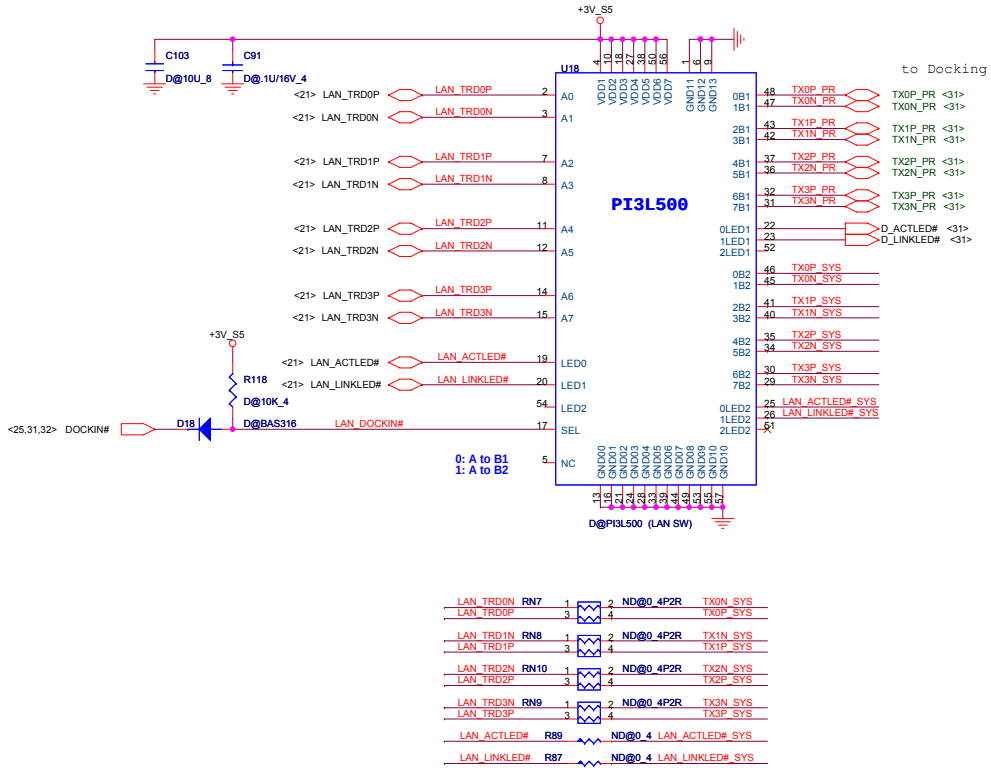
Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	LVDS/HDMI/CAMERA/LID	1A
Date: Wednesday, April 09, 2008	Sheet 20 of 40	

LAN

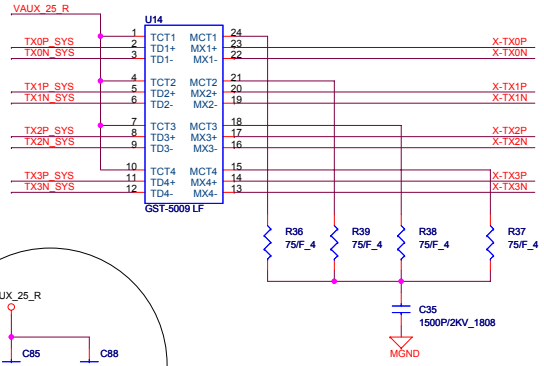

+3V_S5
Q13
DTC144EUA
R61
4.7K_4
<14,23,32> PCIE_WAKE#
PCIE_WAKE_R#
VDDCIO_12
+PWR_TRANSF
L21
*BLM11A601S
FOR DOCK
VDDCIO_12
C83
C143
.1U/16V_4
.1U/16V_4
U19
BCM5764M
10mm X 10mm
68-Pin QFN
BCM5764MA0KMLG
VAUX_12
VDDCIO_12
+3V_S5
20mil
Rev:B ,Add
Rev:B ,change to 0603
LAN_AVDDL
GPHY_PLLVDD
PCIE_PLLVDD
PCIE_SDS_VDD
L26 BLM11A601S
L25 BLM11A601S
L24 BLM11A601S
L23 BLM11A601S
C610 .1U/16V_4
C125 4.7u/6.3V_6
C123 .1U/16V_4
C130 4.7u/6.3V_6
C132 .1U/16V_4
C104 4.7u/6.3V_6
C110 .1U/16V_4
C92 4.7U/10V_8
C99 .1U/16V_4
BIASVDD
XTALVDD
AVDDH
L28 BLM11A601S
L20 BLM11A601S
L27 BLM11A601S
C131 .1U/16V_4
C89 .1U/16V_4
C115 .1U/16V_4
C124 .1U/16V_4
LAN_TRD3P
LAN_TRD3N
LAN_TRD2N
LAN_TRD2P
LAN_TRD1P
LAN_TRD1N
LAN_TRD0N
LAN_TRD0P
EEPROM Strapping
SO SI CS# SCLK
24c64 1 1 0 1
AT45DB011B 1 0 1 1
Rev: B remove
R62 4.7K_4
R63 *4.7K_4
R64 4.7K_4
C87 .1U/16V_4
R73 ASF@4.7K_4
R66 ASF@4.7K_4
WP
BCM_RESET#
U15
NASF@AT24C64
FAE:When 24C64 is used,Stuff
R204,R88,R212,R215
not stuff R85 ,R84
BCM_WP
BCM_SCL
BCM_SDA
SI,SO,CS#,SCLK have internal pull up
LINKLED#
100#
1000#
LAN_ACTLED#
GPIO2
T8
T9
ENERGY_DET
PCIE_WAKE_R#
-LAN_RST
PCLK_SMB
PDAT_SMB
AUX_PRES
VMA_PRES
CLK_LAN_X1
CLK_LAN_X2
RDAC
R150 1.2K/F_6
Rev:B Change to 1.21K
C69 27P/50V_4
C68 27P/50V_4
Y7
25MHZ
R68 200_4
Rev:B R68 change to CLK_LAN_X2
R114 1K_4
R120 1K_4
R72 4.7K_4
R99 0_4
R101 0_4
R74 0_4
R91 0_4
R51 1.5_12
Q12 MMJT9435
C46 .1U/16V_4
C47 4.7U/10V_8
C44 .1U/16V_4
C48 10U/6.3V_8
R60 39K_6
LAN REGCTL12
AT45DB011B-SC(LAN FLASH): Stuff U6,R46,R45
U17
ASF@AT45DB011B-SC(LAN FLASH)
C114 ASF@.1U/16V_4
BCM_SCL R85 *4.7K_4
SI R106 ASF@4.7K_4
CS# R80 NASF@4.7K_4
C98 C108 C122 C111 C95 C116 C74 C75 C109 .1U/16V_4 4.7U/10V_8
C144 C76 C94 C113 C67 .1U/16V_4 4.7U/10V_8
Low is normal, H->Turn Off 1.2V,
H(>0.7V <2.5V)->L will internal
reset
Quanta Computer Inc.
PROJECT : ZY2 & ZY6
Size
Document Number
BCM5787 & 5764 LAN
Rev
1A
Date: Tuesday, April 08, 2008
Sheet 21 of 40

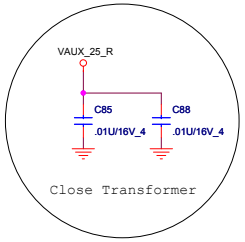
LAN SWITCH

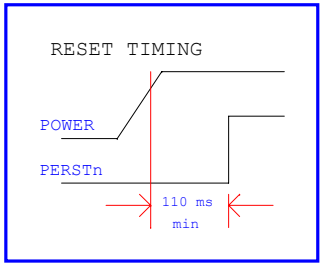


Transfomer

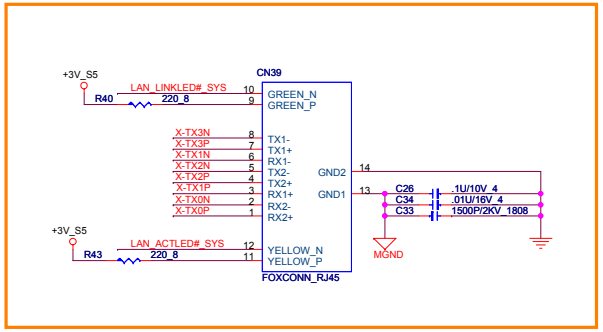
Source 1: DELTA LFE9249 DB0ZR1LAN11
Source 2: Bothand GST5009 DBKN1NLAN03





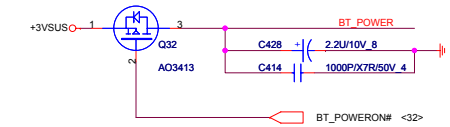


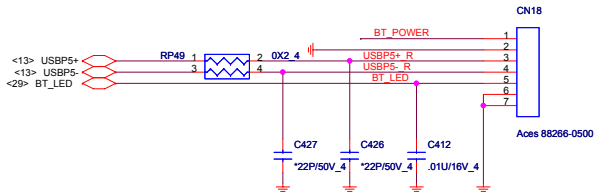
RJ45-11



9/29: change footprint
11/27 :change footprint
11/28 : R43 & R40 Change to 0805
1/31 :Rev: C change PIN define about 9,10,11 & 12

BLUETOOTH MODULE CONNECTOR





Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	BT/CCD/RJ45-11/CIR/2nd FAN	1A
Date: Tuesday, April 08, 2008	Sheet 22 of 40	

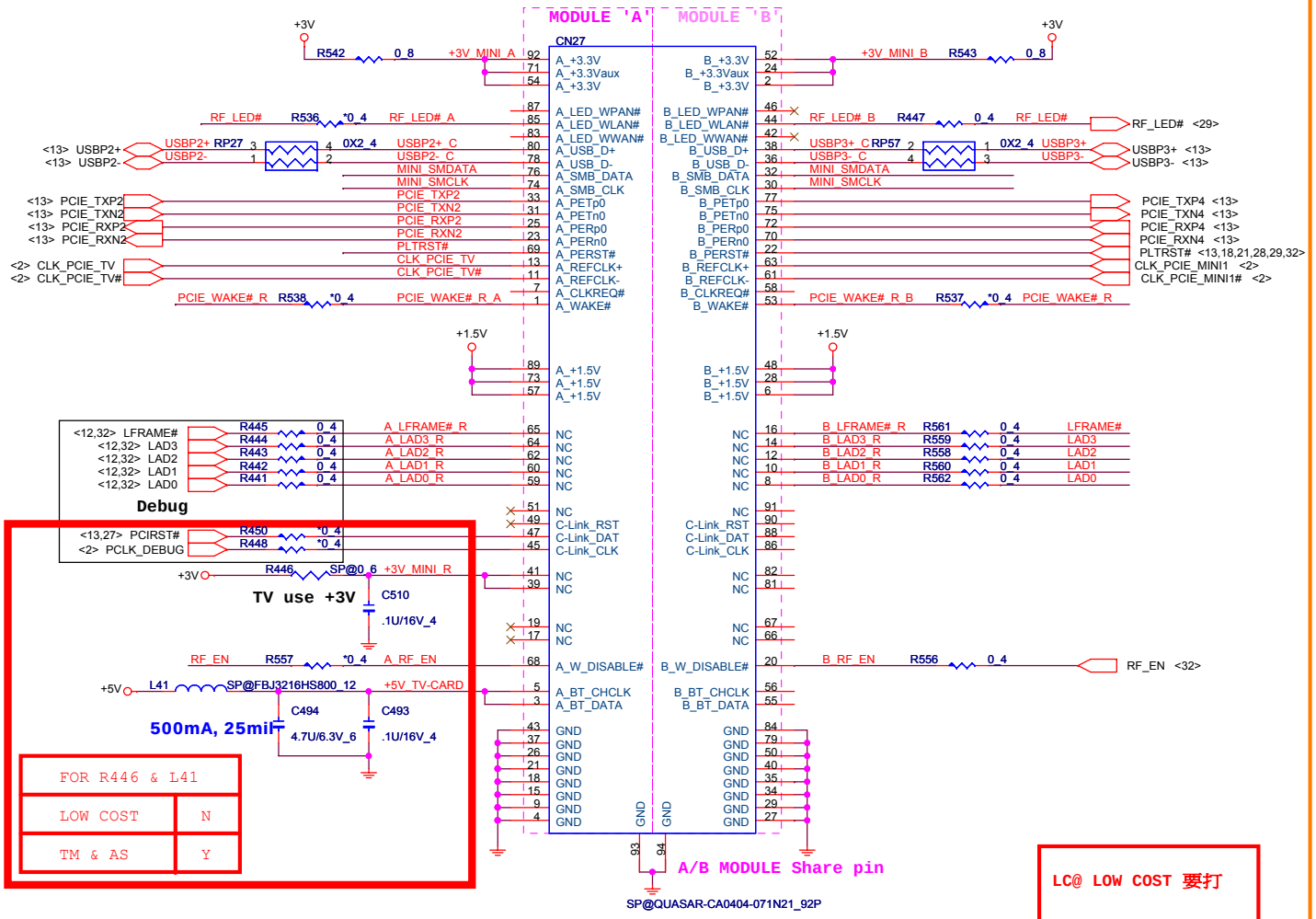
MINI-CARD

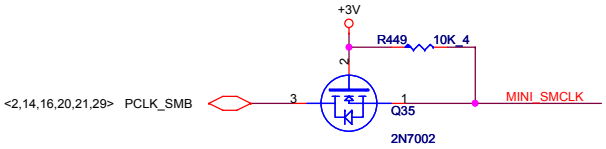
MODULE 'A' TV card

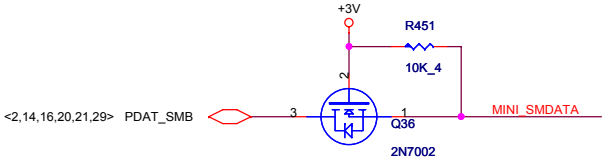
MODULE 'B' Wireless card

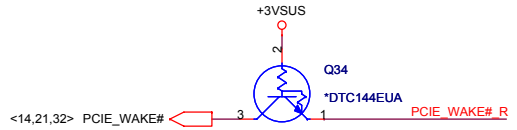
Double Stack MINI CARD

Rev:B PIN36,38 Add USB3
PIN69 Add R536
PIN1, 53 Add R537 & R538

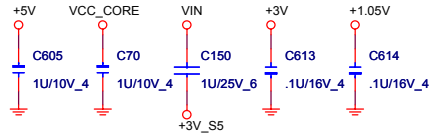


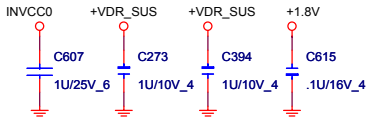




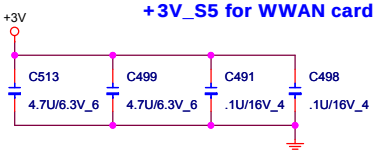


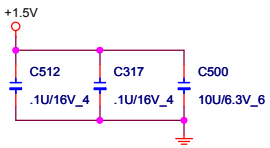
FOR EMI





+3V_S5 for WWAN card is 2.75A





Quanta Computer Inc.
PROJECT : ZY2 & ZY6

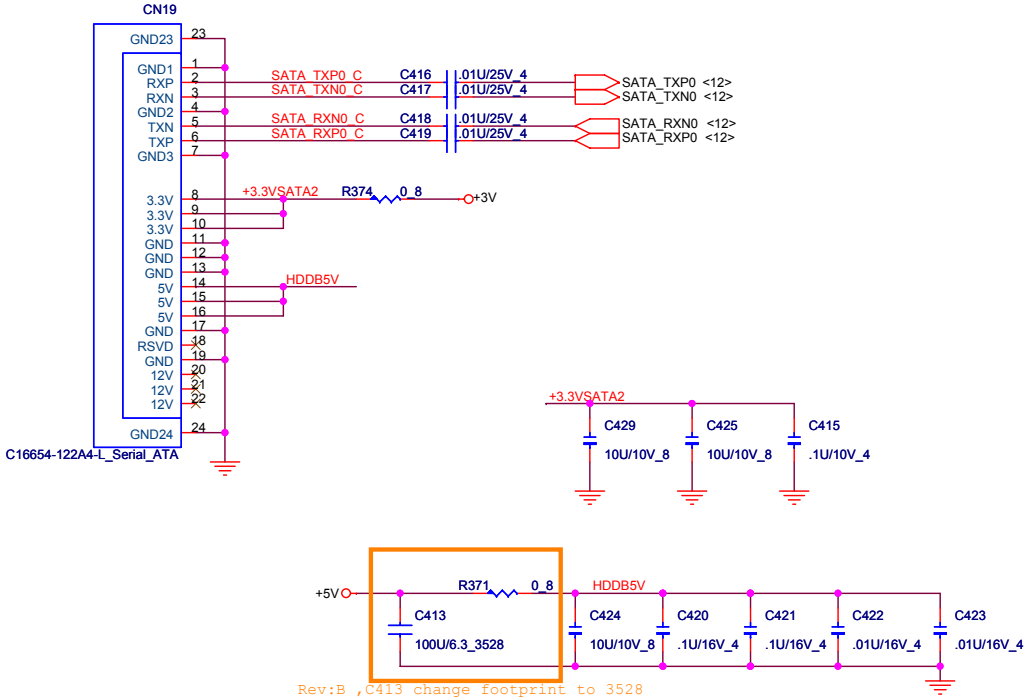
Size	Document Number	Rev
	MINI PCI-E card/TV/TPM	1A

Date: Tuesday, April 08, 2008 Sheet 23 of 40

SATA HDD

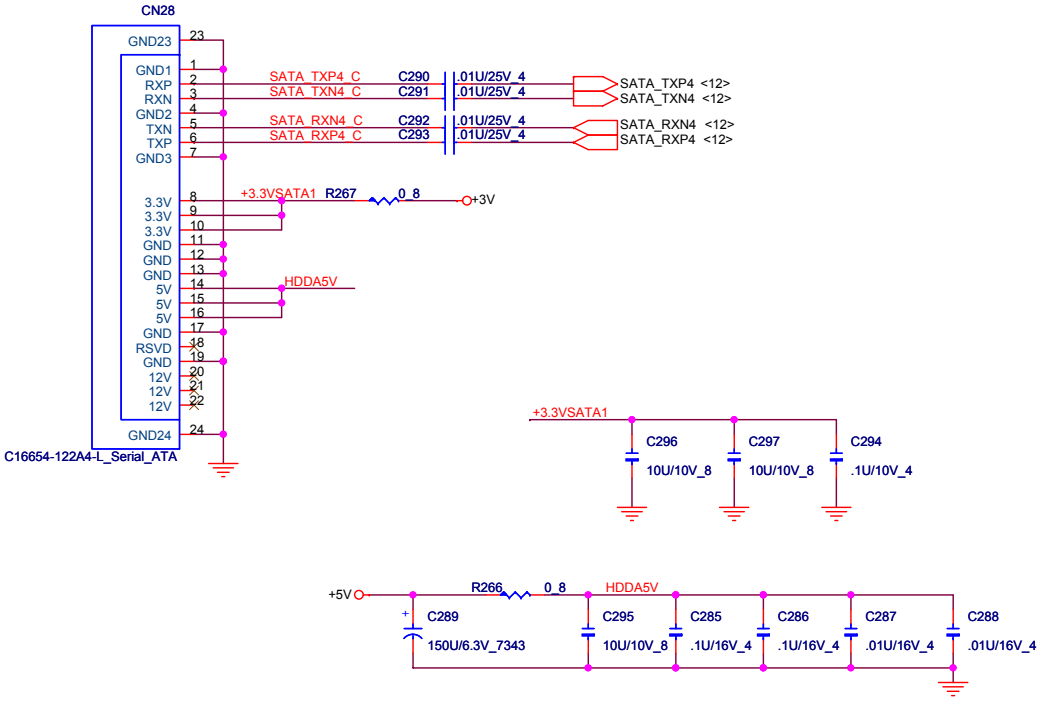
11/8 REV:B Conn. 掉對調 CN28 & CN19

Main

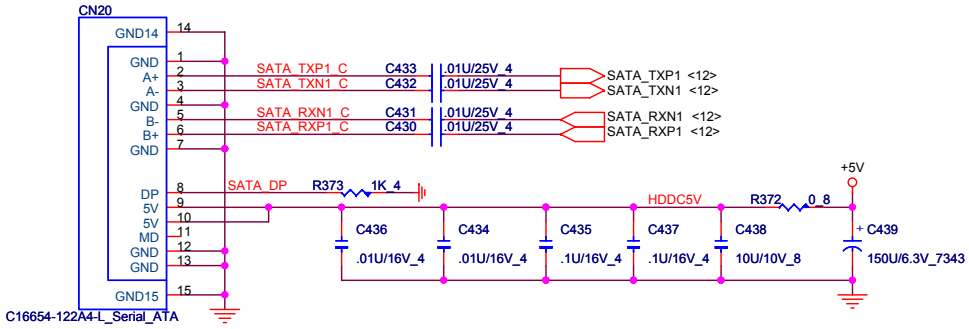


Rev:B ,C413 change footprint to 3528

2ND SATA HDD



ODD (SATA)



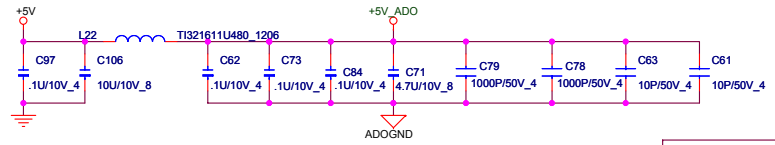
Quanta Computer Inc.

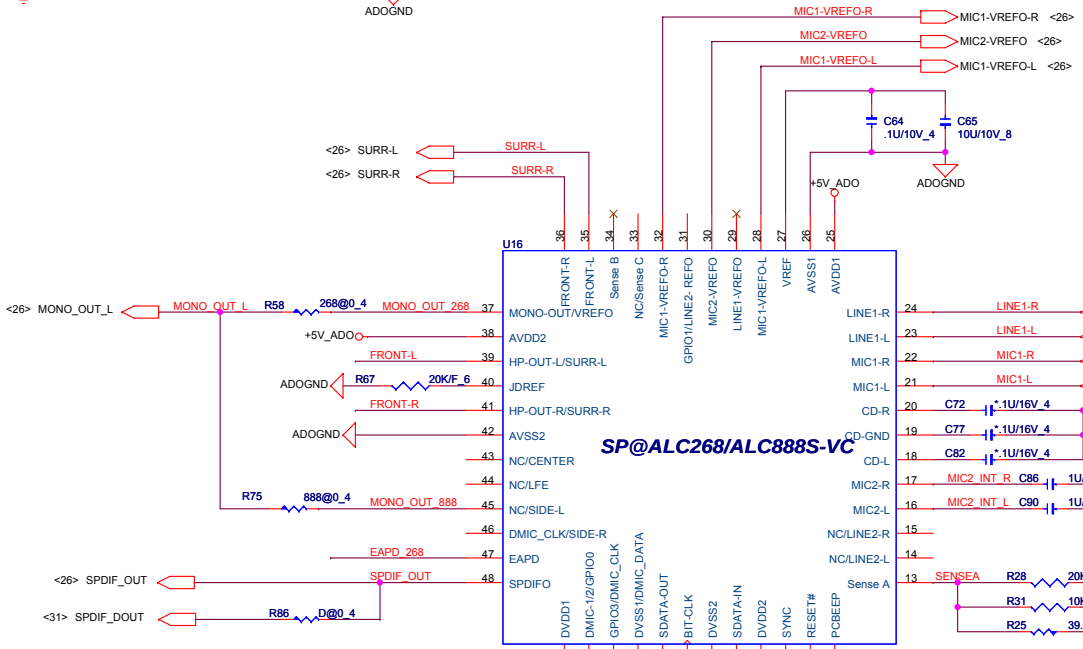
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	SATA-HDD & ODD	1A

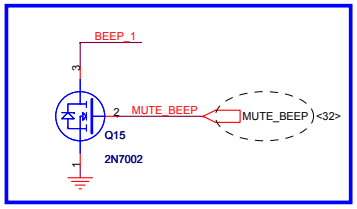
Date: Tuesday, April 08, 2008 Sheet 24 of 40

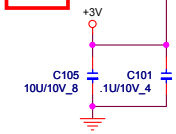
CODEC(ALC268)

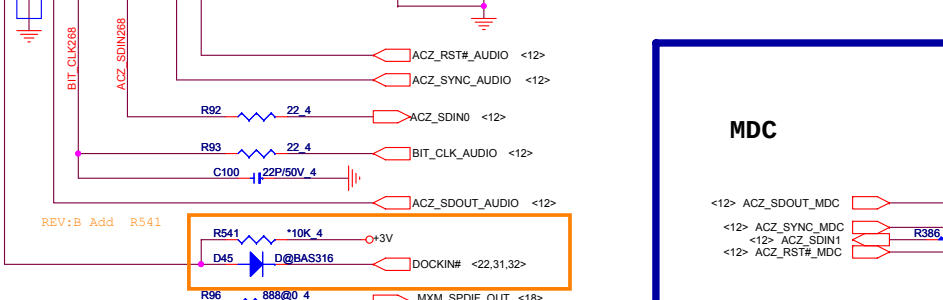


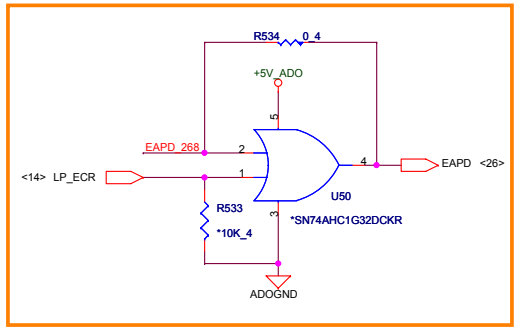


11/8 REV:B Remove R97, R98



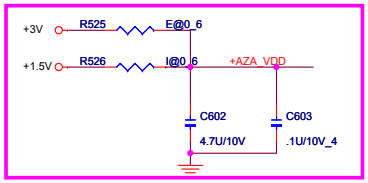






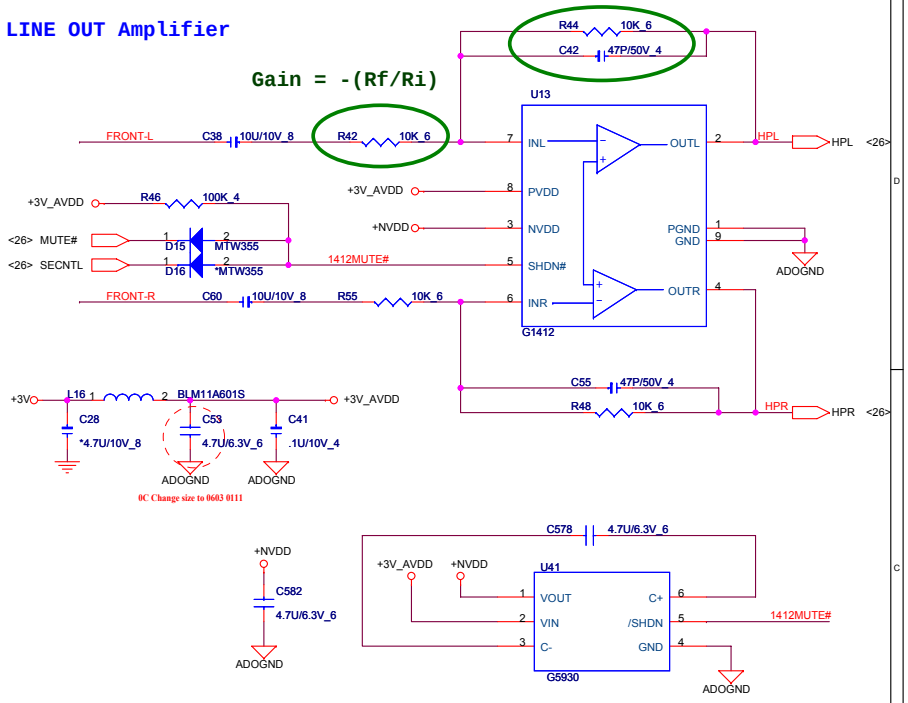
10/10 : ADD. FOR NO CARDBUS

REV:B, Please modify U16.PIN9.same as ZD1



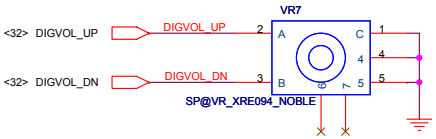
LINE OUT Amplifier

Gain = -(Rf/Ri)

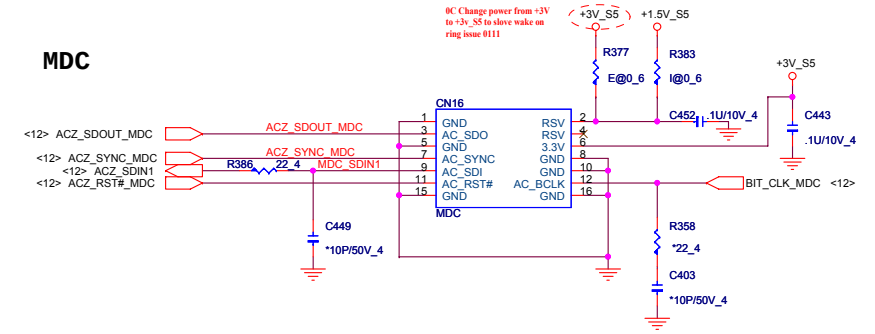


VR

TM	N
AS & LOW COST	Y



MDC



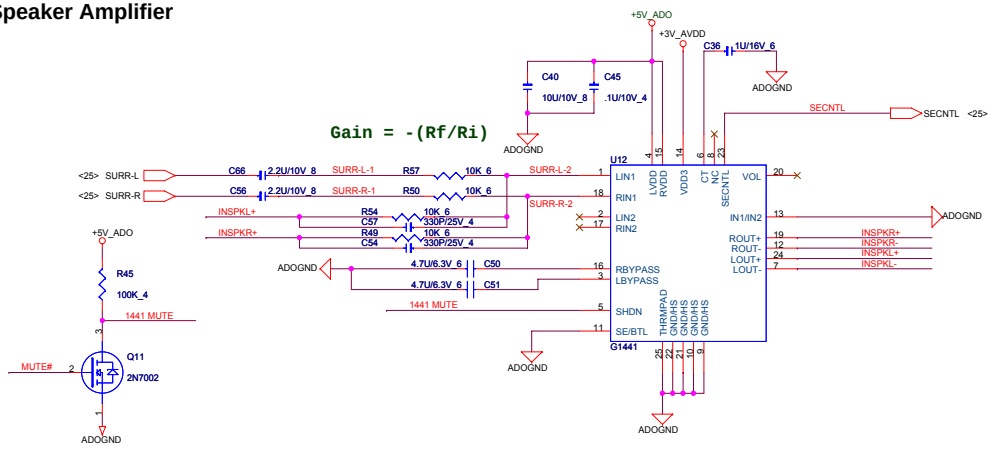
Quanta Computer Inc.

PROJECT : ZY2 & ZY6

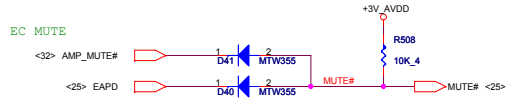
Size	Document Number	Rev
	REALTEK ALC268&888/MDC/VR	1A

Date: Tuesday, April 08, 2008 Sheet 25 of 40

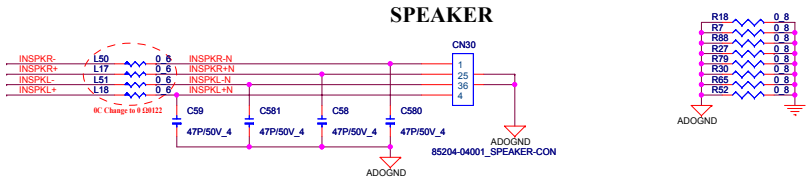
Speaker Amplifier



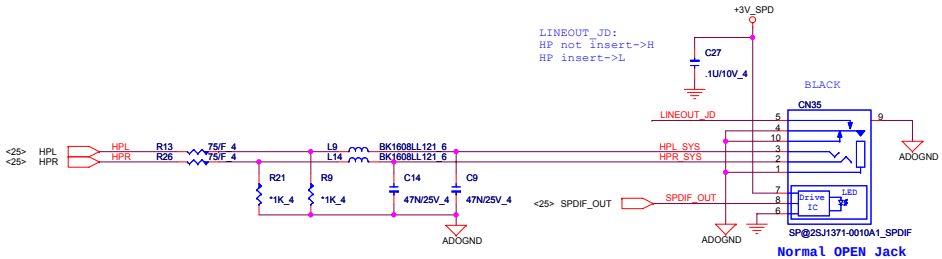
EC MUTE

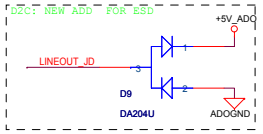


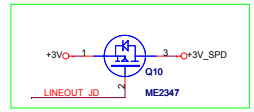
SPEAKER



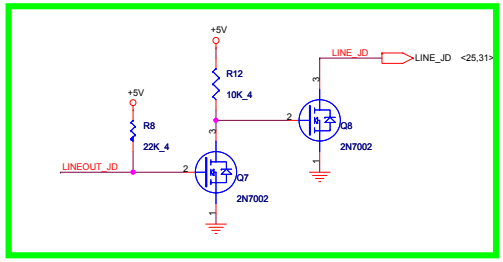
SYSTEM LINE OUT/SPDIF



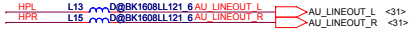




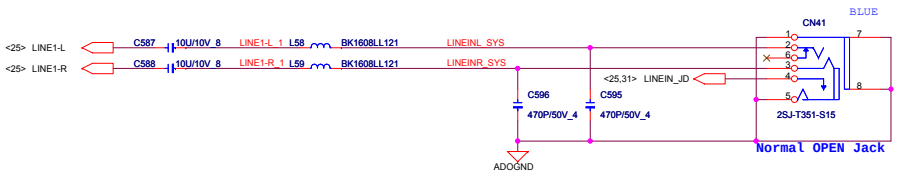
Foxconn DFTJ10FR470 2FB5441-BKMC-7F
Singatron DFTJ10FR437 2SJ1371-0010A1



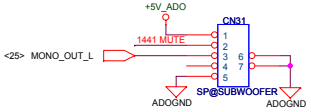
Docking LINE OUT/SPDIF



SYSTEM LINE IN/SUBWOOFER

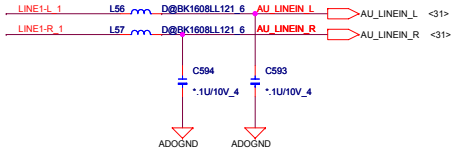


Singatron DFTJ06FR732 2SJ-T351-S15
Foxconn DFTJ06FRA21 JA6233L-U3T4-7F
Alltop DFTJ06FR902 C12107-906A9-L

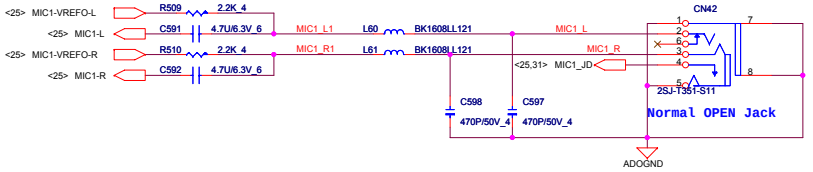


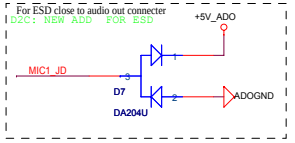
TM & LOW COST	N
AS	Y

Docking LINE IN



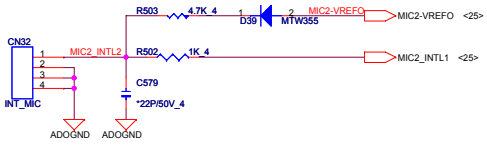
MIC





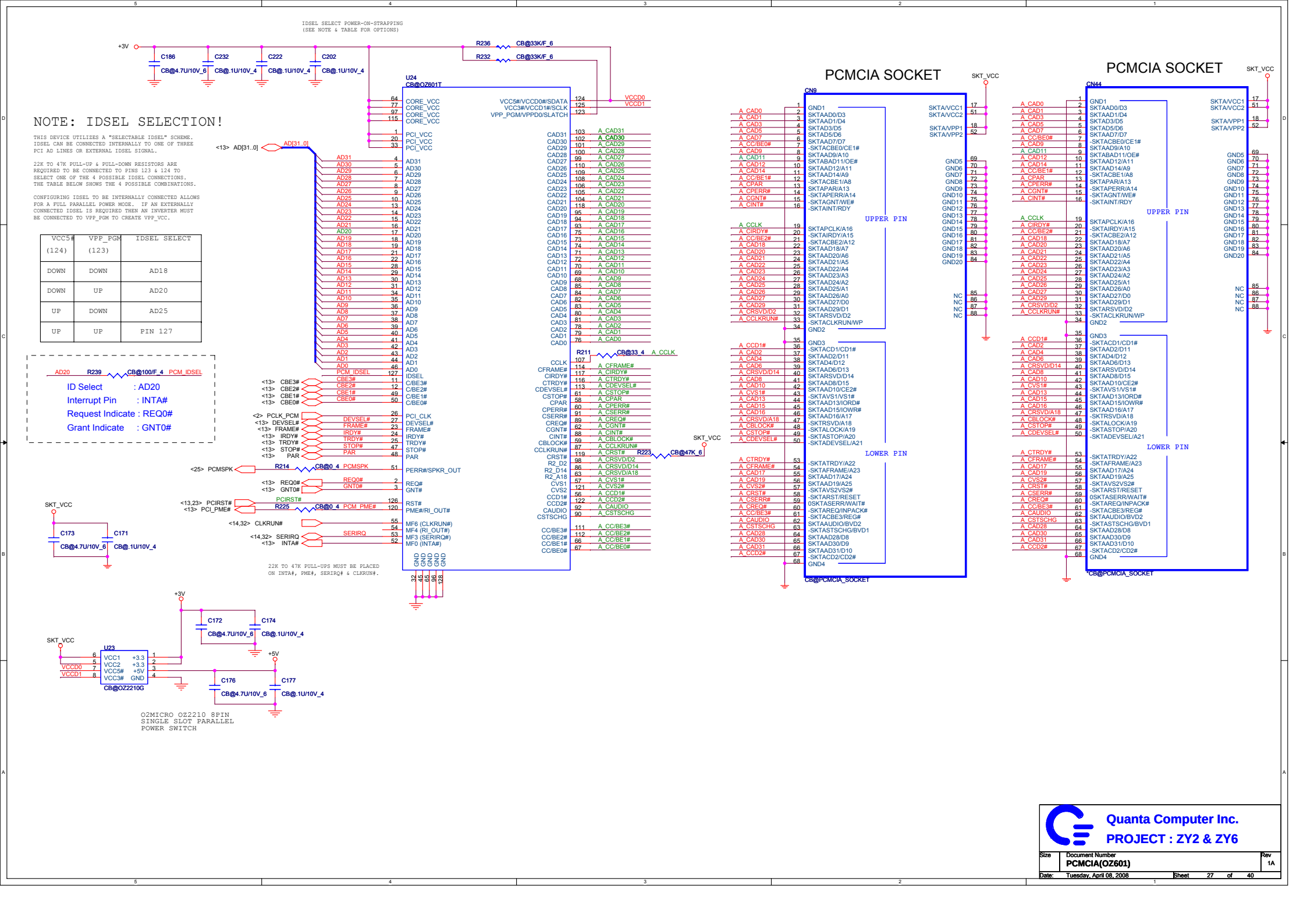
Singatron DFTJ06FR741 2SJ-T351-S11
Foxconn DFTJ06FRA39 JA6233L-P3T4-7F
Alltop DFTJ06FR899 C12107-D06A9-L

INT MIC array

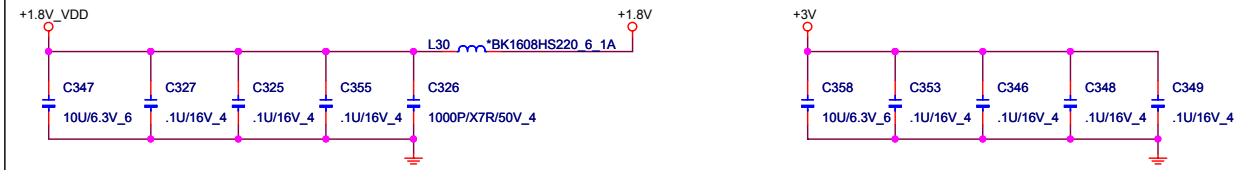


Quanta Computer Inc.
PROJECT : ZY2 & ZY6

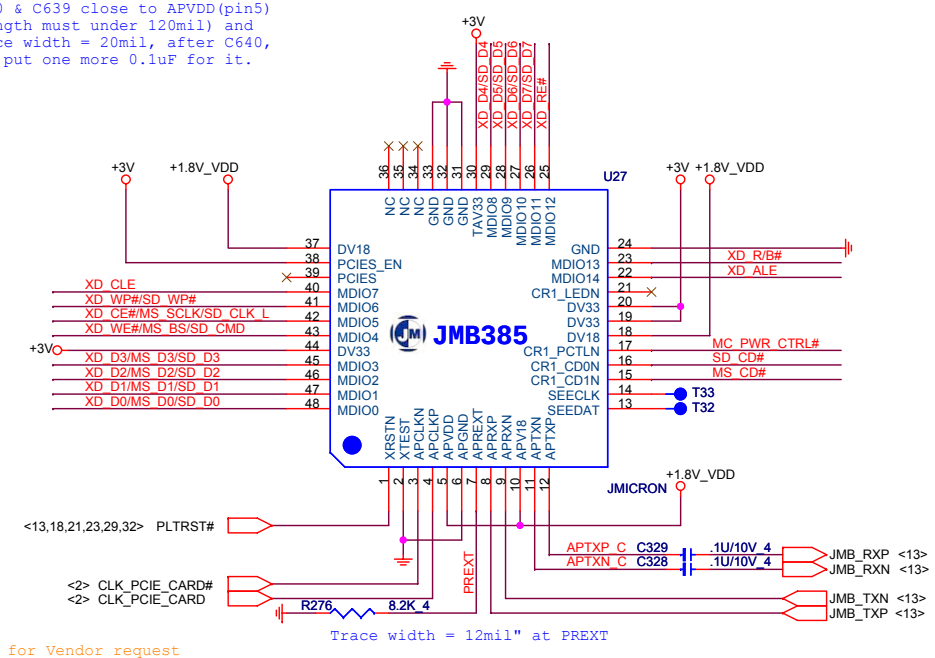
Size	Document Number	Rev
	AMP /AUDIO JACK CONN	1A
Date: Tuesday, April 08, 2008	Sheet 26 of 40	


IDSEL SELECT POWER-ON-STRAPPING
(SEE NOTE & TABLE FOR OPTIONS)
NOTE: IDSEL SELECTION!
THIS DEVICE UTILIZES A "SELECTABLE IDSEL" SCHEME.
IDSEL CAN BE CONNECTED INTERNALLY TO ONE OF THREE
PCI AD LINES OR EXTERNAL IDSEL SIGNAL.
22K TO 47K PULL-UP & PULL-DOWN RESISTORS ARE
REQUIRED TO BE CONNECTED TO PINS 123 & 124 TO
SELECT ONE OF THE 4 POSSIBLE IDSEL CONNECTIONS.
THE TABLE BELOW SHOWS THE 4 POSSIBLE COMBINATIONS.
CONFIGURING IDSEL TO BE INTERNALLY CONNECTED ALLOWS
FOR A FULL PARALLEL POWER MODE. IF AN EXTERNALLY
CONNECTED IDSEL IS REQUIRED THEN AN INVERTER MUST
BE CONNECTED TO VPP_PGM TO CREATE VPP_VCC.
VCC5# (124) | VPP_PGM (123) | IDSEL SELECT
DOWN | DOWN | AD18
DOWN | UP | AD20
UP | DOWN | AD25
UP | UP | PIN 127
ID Select : AD20
Interrupt Pin : INTA#
Request Indicate : REQ0#
Grant Indicate : GNT0#
U24
CB@OZ601T
PCMCIA SOCKET
CN9
CB@PCMCIA_SOCKET
PCMCIA SOCKET
CN44
CB@PCMCIA_SOCKET
UPPER PIN
LOWER PIN
U23
CB@OZ2210G
O2MICRO OZ2210 8PIN
SINGLE SLOT PARALLEL
POWER SWITCH
22K TO 47K PULL-UPS MUST BE PLACED
ON INTA#, PME#, SERIRQ# & CLKRUN#.
Quanta Computer Inc.
PROJECT : ZY2 & ZY6
Size
Document Number
PCMCIA(OZ601)
Rev
1A
Date: Tuesday, April 08, 2008
Sheet 27 of 40

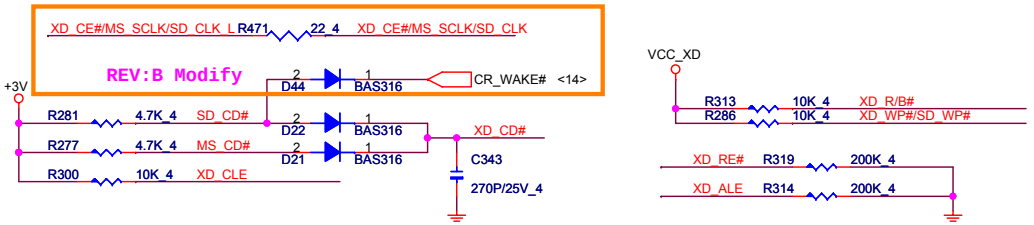
7 IN 1 CARD READER

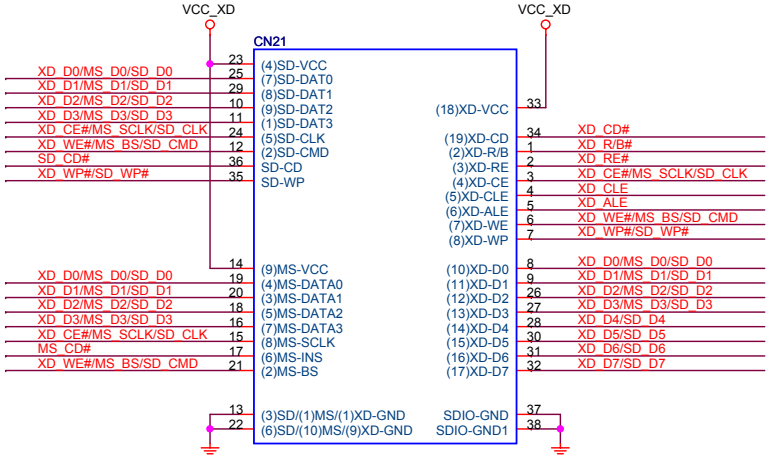


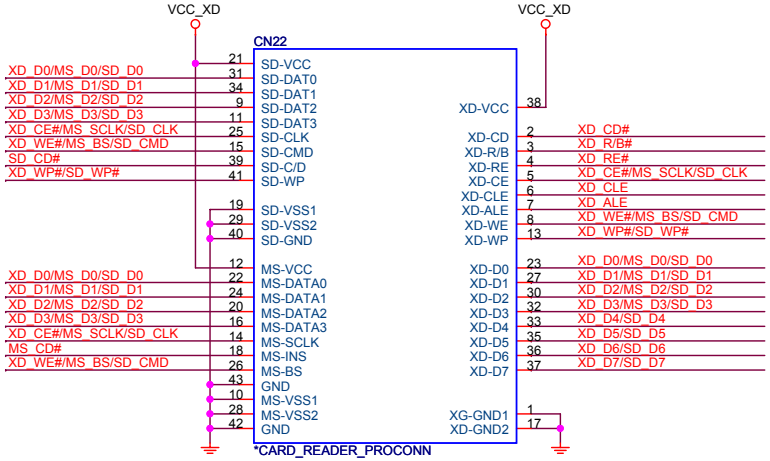
C640 & C639 close to APVDD(pin5) (length must under 120mil) and trace width = 20mil, after C640, pls put one more 0.1uF for it.



Rev: B Add. for Vendor request

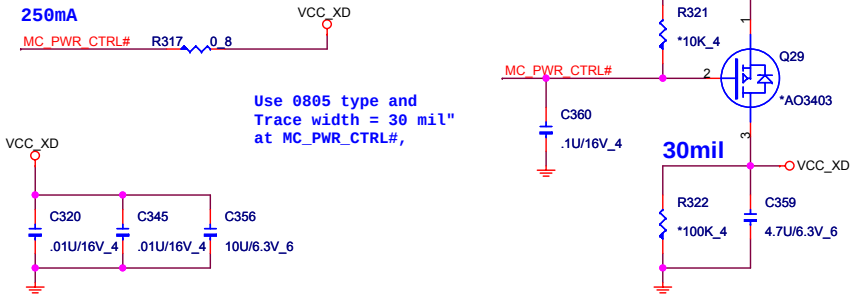






Memory Card Power Supply

10/12 : BOM modify



Quanta Computer Inc.

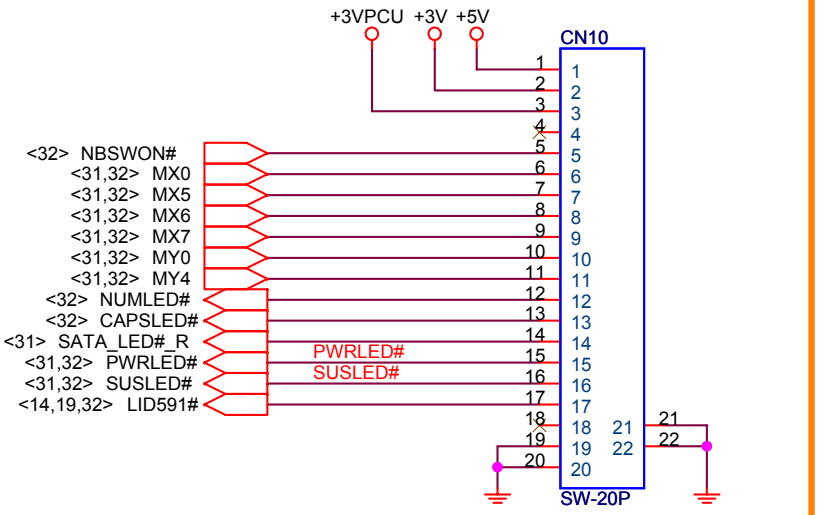
PROJECT : ZY2 & ZY6

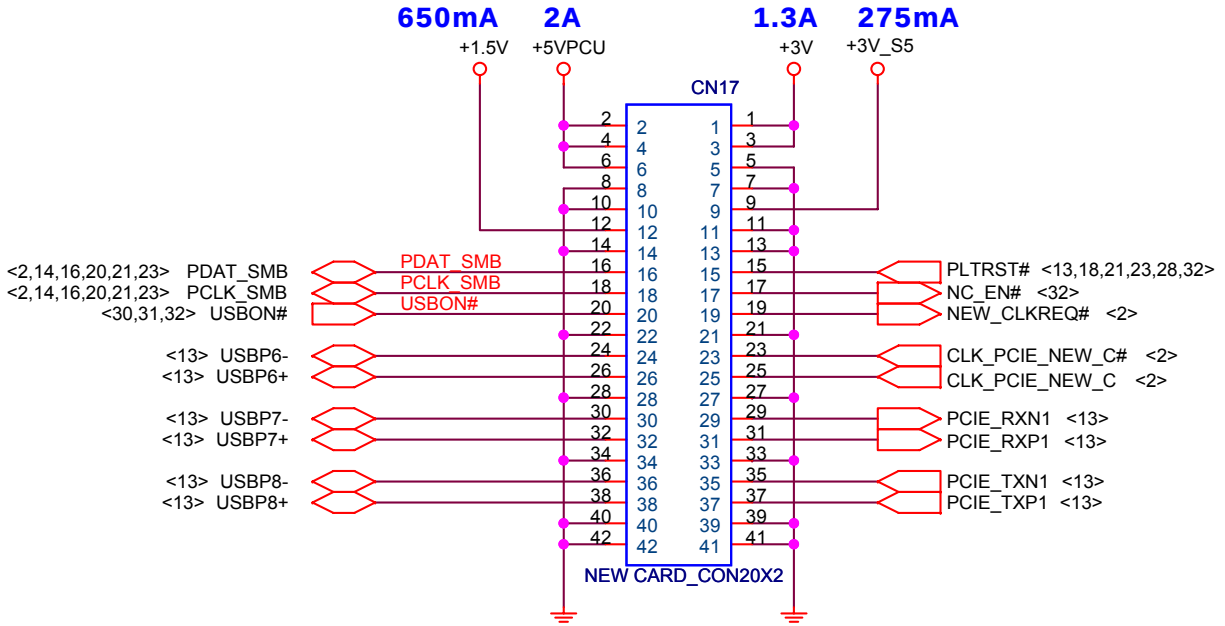
Size	Document Number	Rev
	CARD READER JMB385	1A

Date: Tuesday, April 08, 2008 Sheet 28 of 40

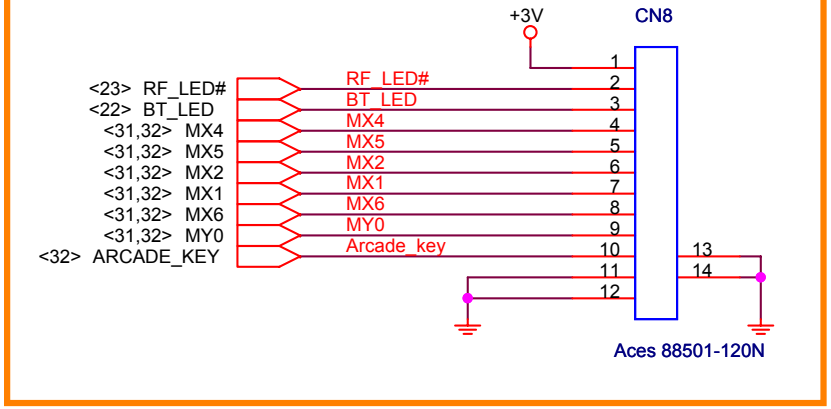
To NEW-CARD & EXT. USB

REV:B, CN10 change footprint

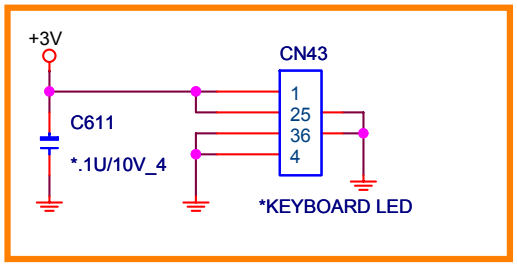




REV:B, Please change PIN define.same as ZY5
CN8 change footprint



Fnction	Keyboard Matrix
E-KEY	MX0/ MY0
E-Mail	MX1/ MY0
E-WWW	MX2/ MY0
3G/TV	MX3/ MY0
Wireless	MX4/ MY0
BlueTooth	MX5/ MY0
P-KEY	MX6/ MY0
Presentation	MX5/ MY4
Lock	MX6/ MY4
Sync	MX7/ MY4



Rev:B Add CN43 For backlight KB

Rev:B Change to 圓 to 方PAD
C255,C234,C221,C199,R217,C198,R183,
R182,R174,R257,R324,R335,R334,R349,C395

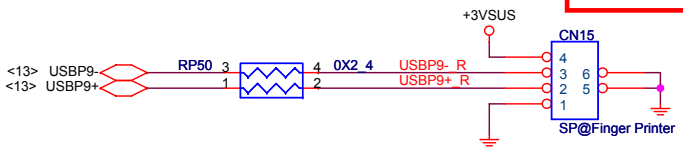
Quanta Computer Inc.

PROJECT : ZY2 & ZY6

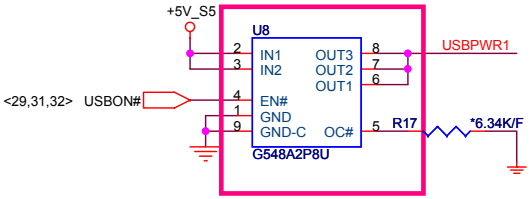
Size	Document Number	Rev
	BTB CONN.	1A
Date: Tuesday, April 08, 2008	Sheet 29 of 40	

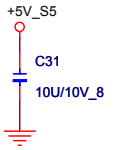
Finger Printer

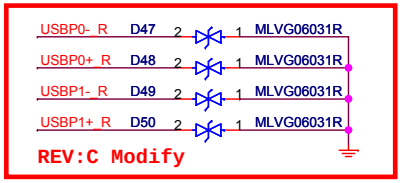
TM & AS	Y
LOW COST	N



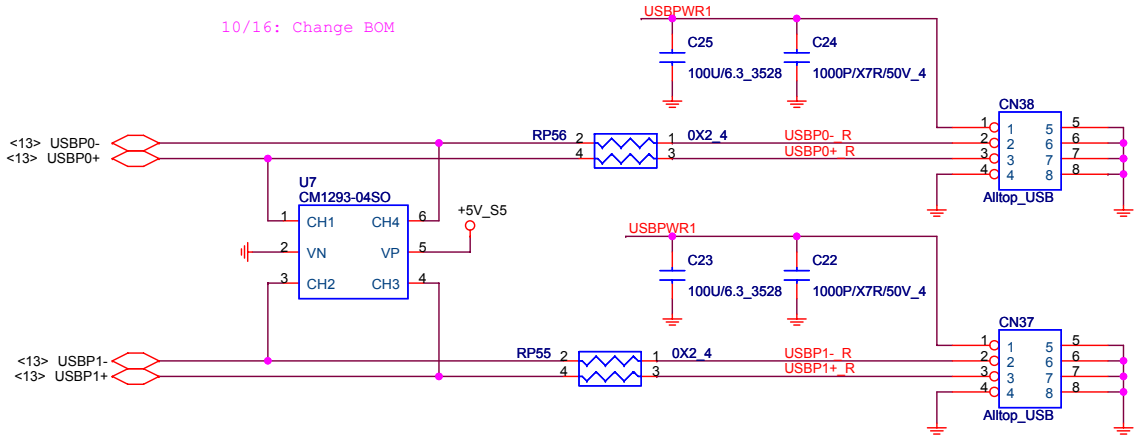
USB





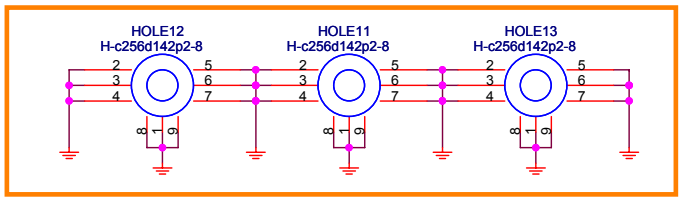


10/16: Change BOM

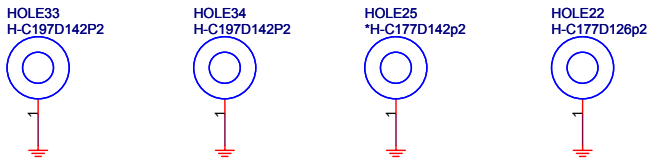


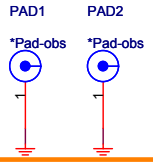
HOLES

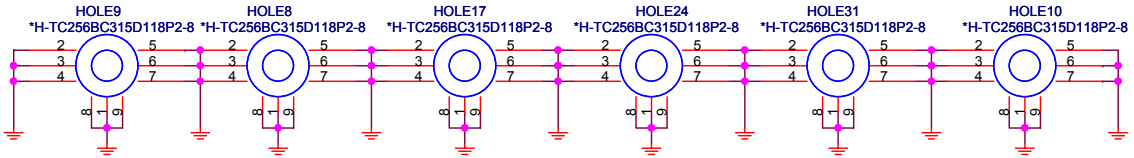
CPU NUT (BOT)



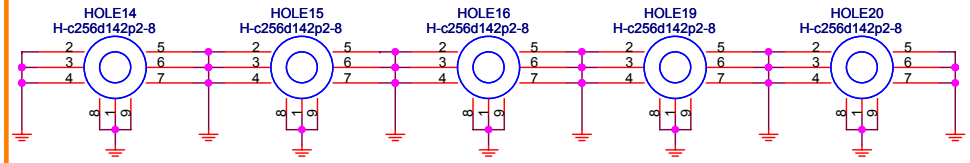
Rev : B Add MINI NUT

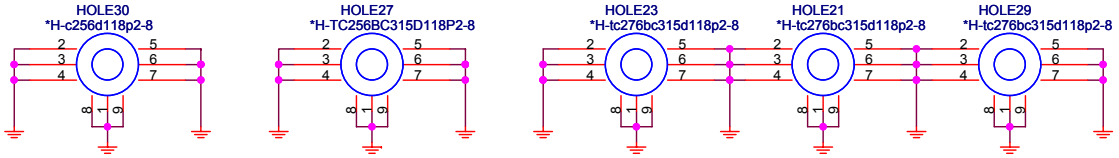




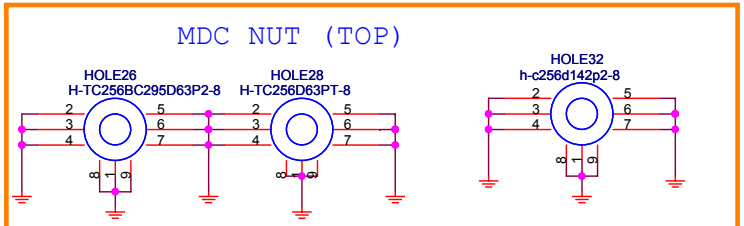


MXM NUT (BOT)

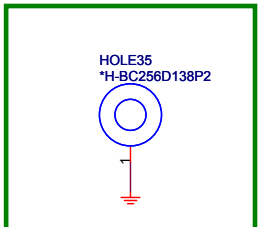




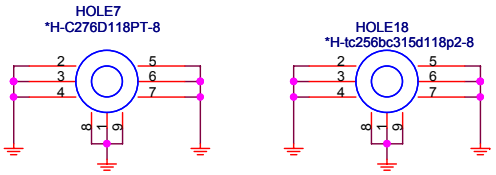
MDC NUT (TOP)



Rev:B New add HOLE32
HOLE26 & 28 Change footprint



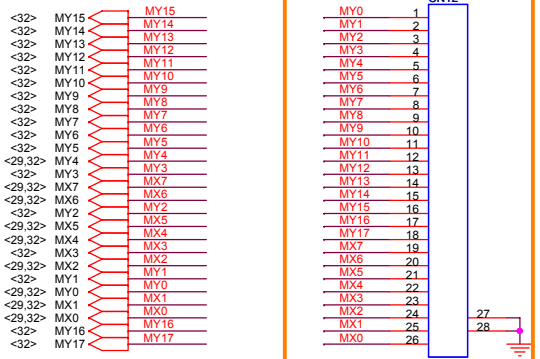
HOLE35 要搬到BOT去



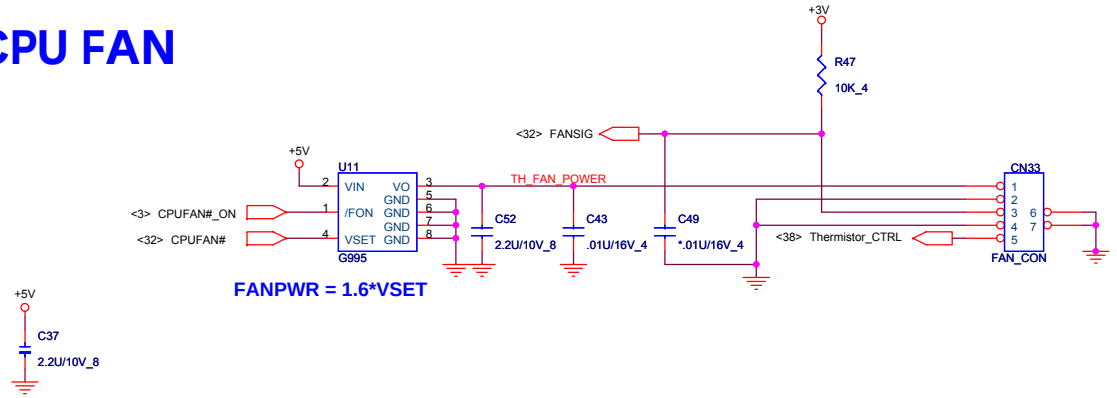
Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	USB/FINGER PRINTER	1A
Date: Wednesday, April 09, 2008	Sheet 30 of 40	

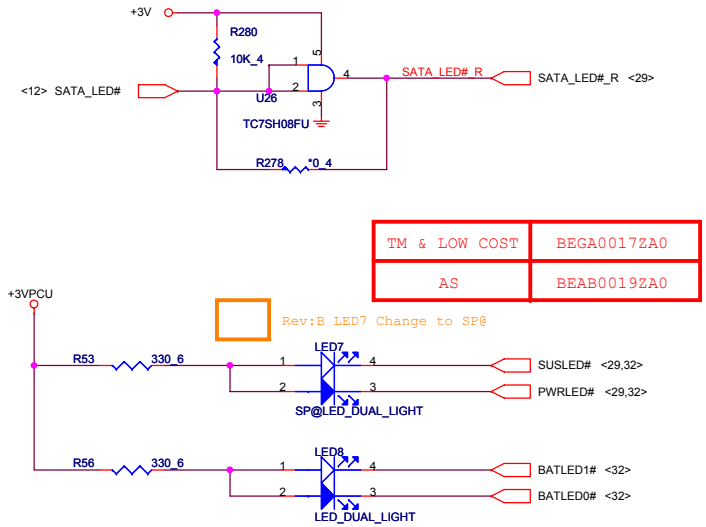
INT K/B



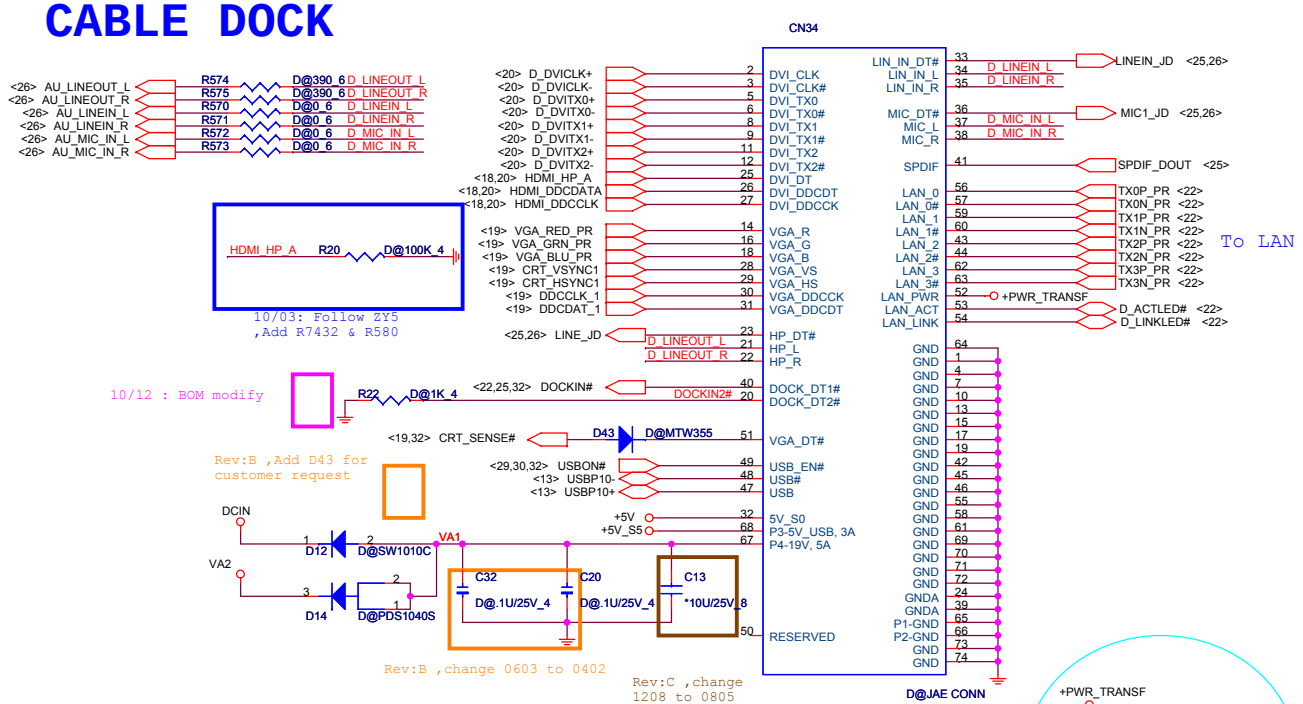
CPU FAN



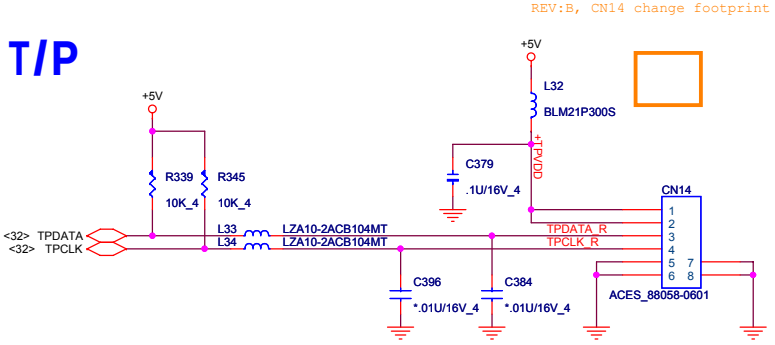
LED

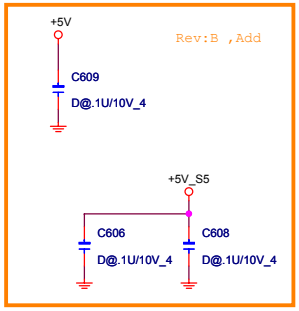


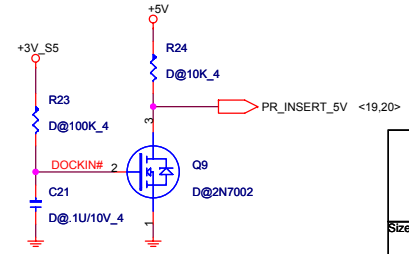
CABLE DOCK

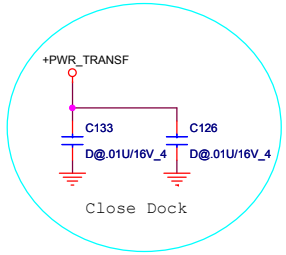


T/P



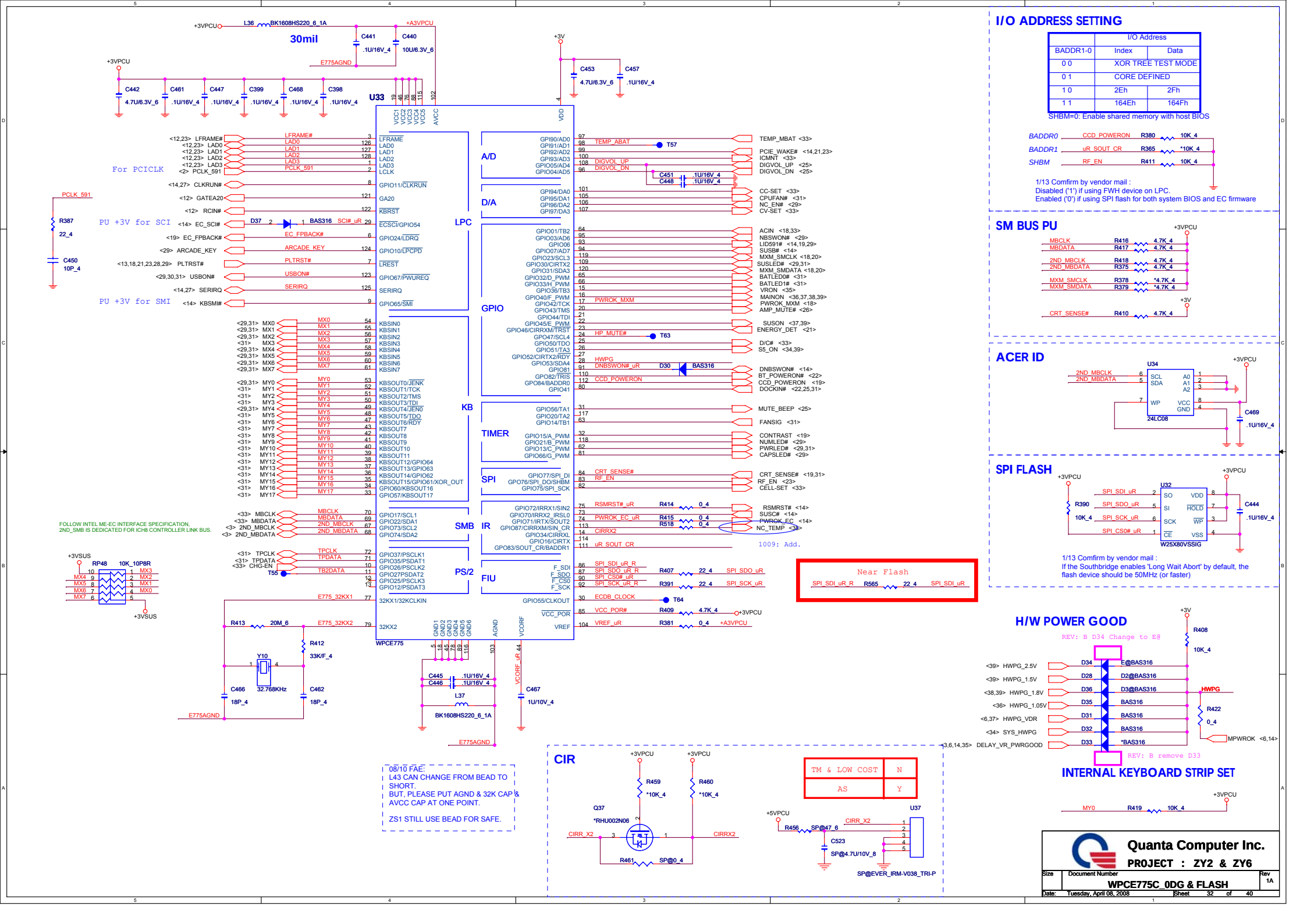


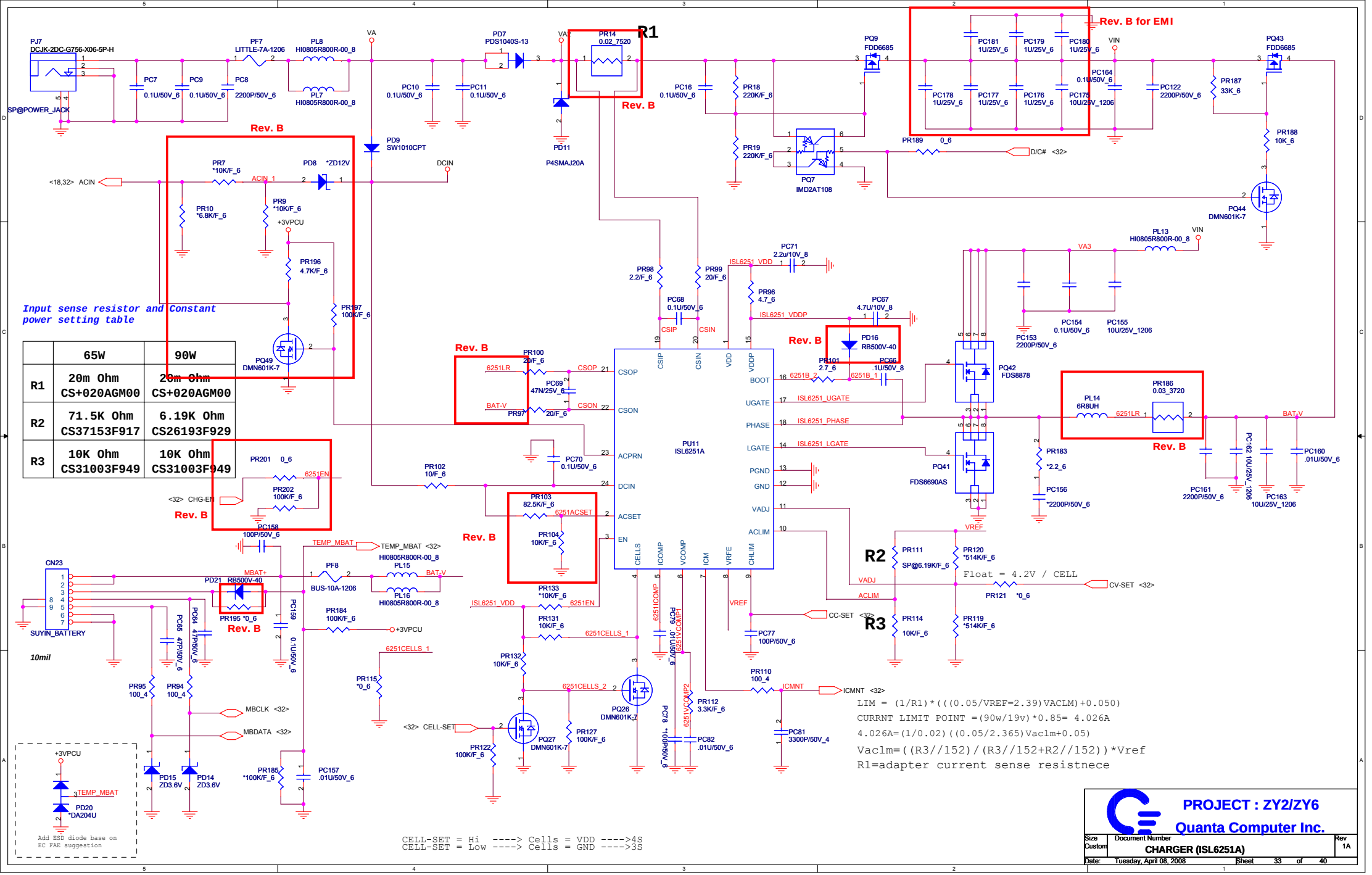


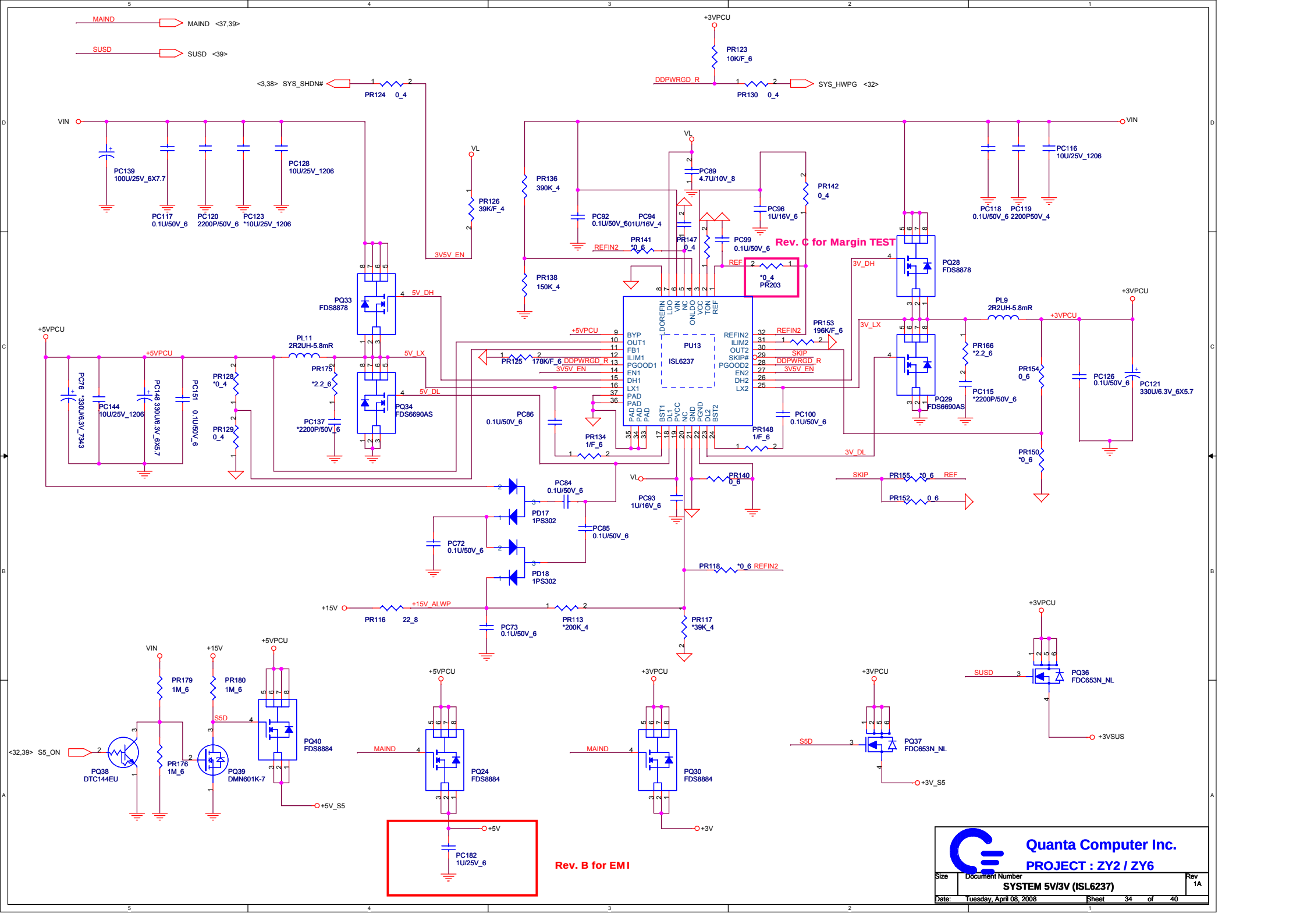


Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	FAN,LED,KB,DEBUG PORT,TP	1A
Date: Wednesday, April 09, 2008	Sheet 31 of 40	


U33
WPCE775
LPC
A/D
D/A
GPIO
KB
TIMER
SPI
SMB
IR
PS/2
FIU
LFRAME
LAD0
LAD1
LAD2
LAD3
LCLK
GPIO11/CLKRUN
GA20
KBRST
ECSCI/GPIO54
GPIO24/LDRQ
GPIO10/LPCPD
LRESET
GPIO67/PWUREQ
SERIRQ
GPIO65/SMI
KBSIN0
KBSIN1
KBSIN2
KBSIN3
KBSIN4
KBSIN5
KBSIN6
KBSIN7
KBSOUT0/JENK
KBSOUT1/TCK
KBSOUT2/TMS
KBSOUT3/TDI
KBSOUT4/JEN0
KBSOUT5/TDO
KBSOUT6/RDY
KBSOUT7
KBSOUT8
KBSOUT9
KBSOUT10
KBSOUT11
KBSOUT12/GPIO64
KBSOUT13/GPIO63
KBSOUT14/GPIO62
KBSOUT15/GPIO61/XOR_OUT
GPIO60/KBSOUT16
GPIO57/KBSOUT17
GPIO17/SCL1
GPIO22/SDA1
GPIO73/SCL2
GPIO74/SDA2
GPIO37/PSCLK1
GPIO35/PSDAT1
GPIO26/PSCLK2
GPIO27PSDAT2
GPIO25/PSCLK3
GPIO12/PSDAT3
32KX1/32KCLKIN
32KX2
GPIO90/AD0
GPIO91/AD1
GPIO92/AD2
GPIO93/AD3
GPIO05/AD4
GPIO04/AD5
GPI94/DA0
GPI95/DA1
GPI96/DA2
GPI97/DA3
GPIO01/TB2
GPIO03/AD6
GPIO06
GPIO07/AD7
GPIO23/SCL3
GPIO30/CIRTX2
GPIO31/SDA3
GPIO32/D_PWM
GPIO33/H_PWM
GPIO36/TB3
GPIO40/F_PWM
GPIO42/TCK
GPIO43/TMS
GPIO44/TDI
GPIO45/E_PWM
GPIO46/CIRRXM/TRST
GPO47/SCL4
GPIO50/TDO
GPIO51/TA3
GPIO52/CIRTX2/RDY
GPIO53/SDA4
GPIO81
GPO82/TRIS
GPO84/BADDR0
GPIO41
GPIO56/TA1
GPIO20/TA2
GPIO14/TB1
GPIO15/A_PWM
GPIO21/B_PWM
GPIO13/C_PWM
GPIO66/G_PWM
GPIO77/SPI_DI
GPO76/SPI_DO/SHBM
GPIO75/SPI_SCK
GPIO72/IRRX1/SIN2
GPIO70/IRRX2_IRSL0
GPIO71/IRTX/SOUT2
GPIO87/CIRRX/SIN_CR
GPIO34/CIRRXL
GPIO16/CIRTX
GPO83/SOUT_CR/BADDR1
F_SDI
F_SDO
F_CS0
F_SCK
GPIO55/CLKOUT
VCC_POR
VREF
VCC1
VCC2
VCC3
VCC4
VCC5
AVCC
VDD
GND1
GND2
GND3
GND4
GND5
GND6
AGND
VCORF
+3VPCU
+A3VPCU
+3V
+3VSUS
L36 BK1608HS220_6_1A
30mil
C441 .1U/16V_4
C440 10U/6.3V_6
E775AGND
C442 4.7U/6.3V_6
C461 .1U/16V_4
C447 .1U/16V_4
C399 .1U/16V_4
C468 .1U/16V_4
C398 .1U/16V_4
C453 4.7U/6.3V_6
C457 .1U/16V_4
For PCICLK
PU +3V for SCI
PU +3V for SMI
R387 22_4
C450 10P_4
D37 BAS316
SCI# uR
FOLLOW INTEL ME-EC INTERFACE SPECIFICATION,
2ND_SMB IS DEDICATED FOR ICH8 CONTROLLER LINK BUS.
RP48 10K_10P8R
T55
R413 20M_6
R412 33K/F_4
Y10 32.768KHz
C466 18P_4
C462 18P_4
L37 BK1608HS220_6_1A
C445 .1U/16V_4
C446 .1U/16V_4
C467 1U/10V_4
T57
T63
T64
D30 BAS316
C451 .1U/16V_4
C448 .1U/16V_4
R414 0_4
R415 0_4
R518 0_4
R407 22_4
R391 22_4
R409 4.7K_4
R381 0_4
Near Flash
SPI_SDI_uR_R R565 22_4 SPI_SDI_uR
1009: Add.
08/10 FAE:
L43 CAN CHANGE FROM BEAD TO SHORT.
BUT, PLEASE PUT AGND & 32K CAP & AVCC CAP AT ONE POINT.
ZS1 STILL USE BEAD FOR SAFE.
CIR
Q37 *RHU002N06
R459 *10K_4
R460 *10K_4
R461 SP@0_4
TM & LOW COST N
AS Y
U37
R456 SP@47_6
C523 SP@4.7U/10V_8
SP@EVER_IRM-V038_TRI-P
I/O ADDRESS SETTING
BADDR1-0 | I/O Address: Index | Data
0 0 | XOR TREE TEST MODE
0 1 | CORE DEFINED
1 0 | 2Eh | 2Fh
1 1 | 164Eh | 164Fh
SHBM=0: Enable shared memory with host BIOS
BADDR0 CCD_POWERON R380 10K_4
BADDR1 uR_SOUT_CR R365 *10K_4
SHBM RF_EN R411 10K_4
1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware
SM BUS PU
MBCLK R416 4.7K_4
MBDATA R417 4.7K_4
2ND_MBCLK R418 4.7K_4
2ND_MBDATA R375 4.7K_4
MXM_SMCLK R378 *4.7K_4
MXM_SMDATA R379 *4.7K_4
CRT_SENSE# R410 4.7K_4
ACER ID
U34 24LC08
C469 .1U/16V_4
SPI FLASH
U32 W25X80VSSIG
C444 .1U/16V_4
R390 10K_4
1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)
H/W POWER GOOD
REV: B D34 Change to E@
R408 10K_4
D34 E@BAS316
D28 D2@BAS316
D36 D3@BAS316
D35 BAS316
D31 BAS316
D32 BAS316
D33 *BAS316
R422 0_4
REV: B remove D33
INTERNAL KEYBOARD STRIP SET
MY0 R419 10K_4
Quanta Computer Inc.
PROJECT : ZY2 & ZY6
Size
Document Number
WPCE775C_0DG & FLASH
Rev 1A
Date: Tuesday, April 08, 2008
Sheet 32 of 40

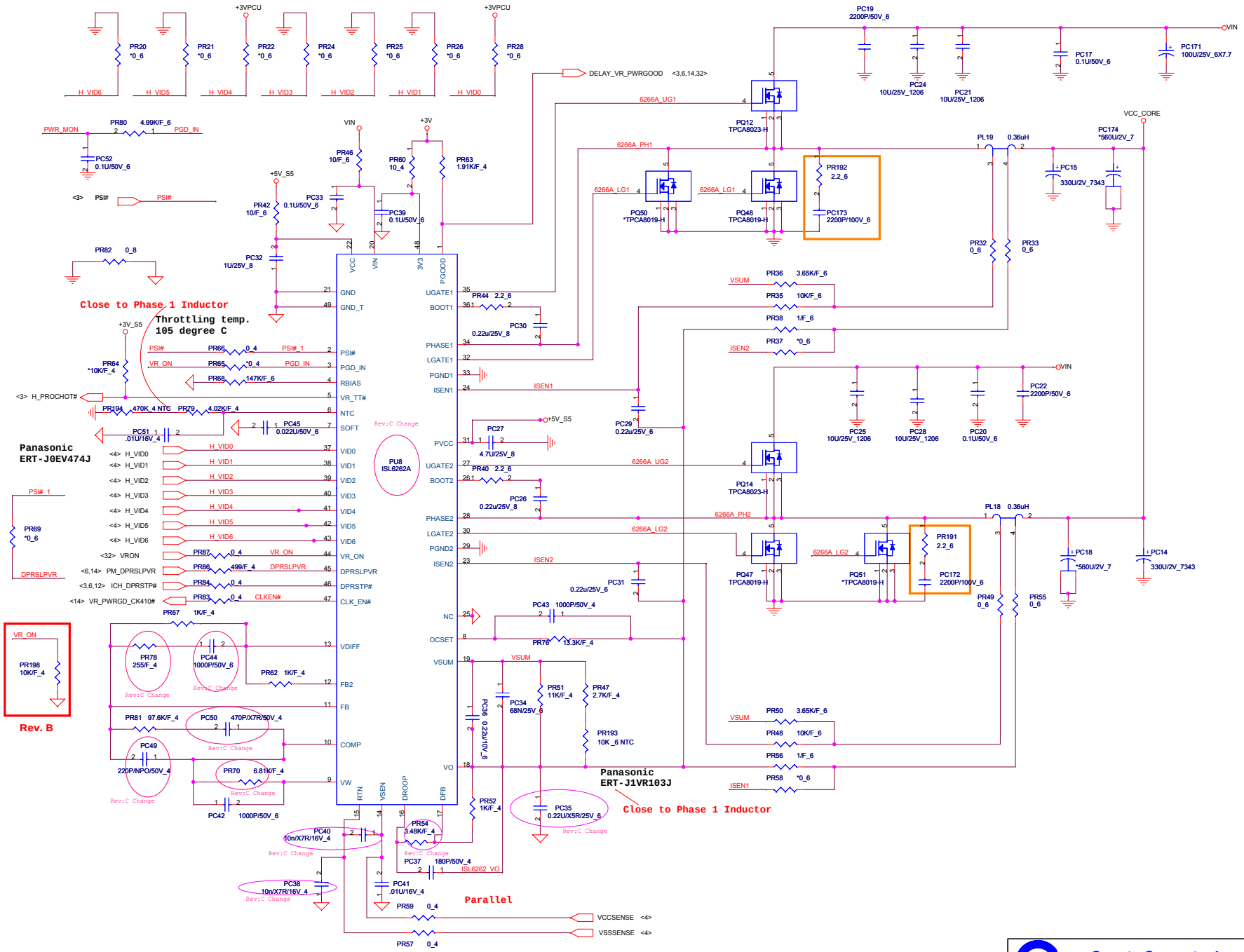

R1
Rev. B
Rev. B for EMI
Input sense resistor and Constant power setting table
65W
90W
R1
20m Ohm CS+020AGM00
20m Ohm CS+020AGM00
R2
71.5K Ohm CS37153F917
6.19K Ohm CS26193F929
R3
10K Ohm CS31003F949
10K Ohm CS31003F949
R2
R3
Float = 4.2V / CELL
LIM = (1/R1)*(((0.05/VREF=2.39)VACLM)+0.050)
CURRNT LIMIT POINT =(90w/19v)*0.85= 4.026A
4.026A=(1/0.02)((0.05/2.365)Vaclm+0.05)
Vaclm=((R3//152)/(R3//152+R2//152))*Vref
R1=adapter current sense resistnece
CELL-SET = Hi ----> Cells = VDD ---->4S
CELL-SET = Low ----> Cells = GND ---->3S
Add ESD diode base on EC FAE suggestion
PROJECT : ZY2/ZY6
Quanta Computer Inc.
CHARGER (ISL6251A)
Tuesday, April 08, 2008
Sheet 33 of 40

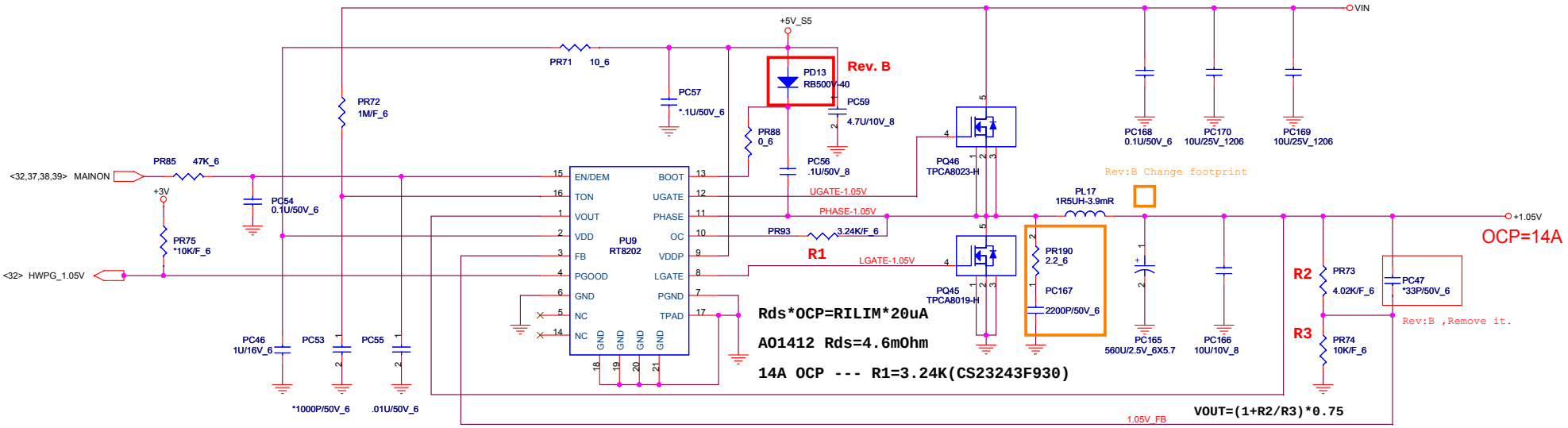


Quanta Computer Inc.

PROJECT : ZY2 / ZY6

Size	Document Number	Rev
	SYSTEM 5V/3V (ISL6237)	1A
Date: Tuesday, April 08, 2008	Sheet 34 of 40	


Close to Phase 1 Inductor
Throttling temp.
105 degree C
Panasonic
ERT-J0EV474J
Rev. B
Panasonic
ERT-J1VR103J
Close to Phase 1 Inductor
Parallel
PU8
ISL6262A
Rev:C Change
DELAY_VR_PWRGOOD
VCC_CORE
VIN
+3VPCU
+3V
+5V_S5
PSI#
VR_ON
PGD_IN
H_PROCHOT#
VSUM
ISEN1
ISEN2
6266A_UG1
6266A_LG1
6266A_PH1
6266A_UG2
6266A_LG2
6266A_PH2
VCCSENSE
VSSSENSE
ISL6262_VO



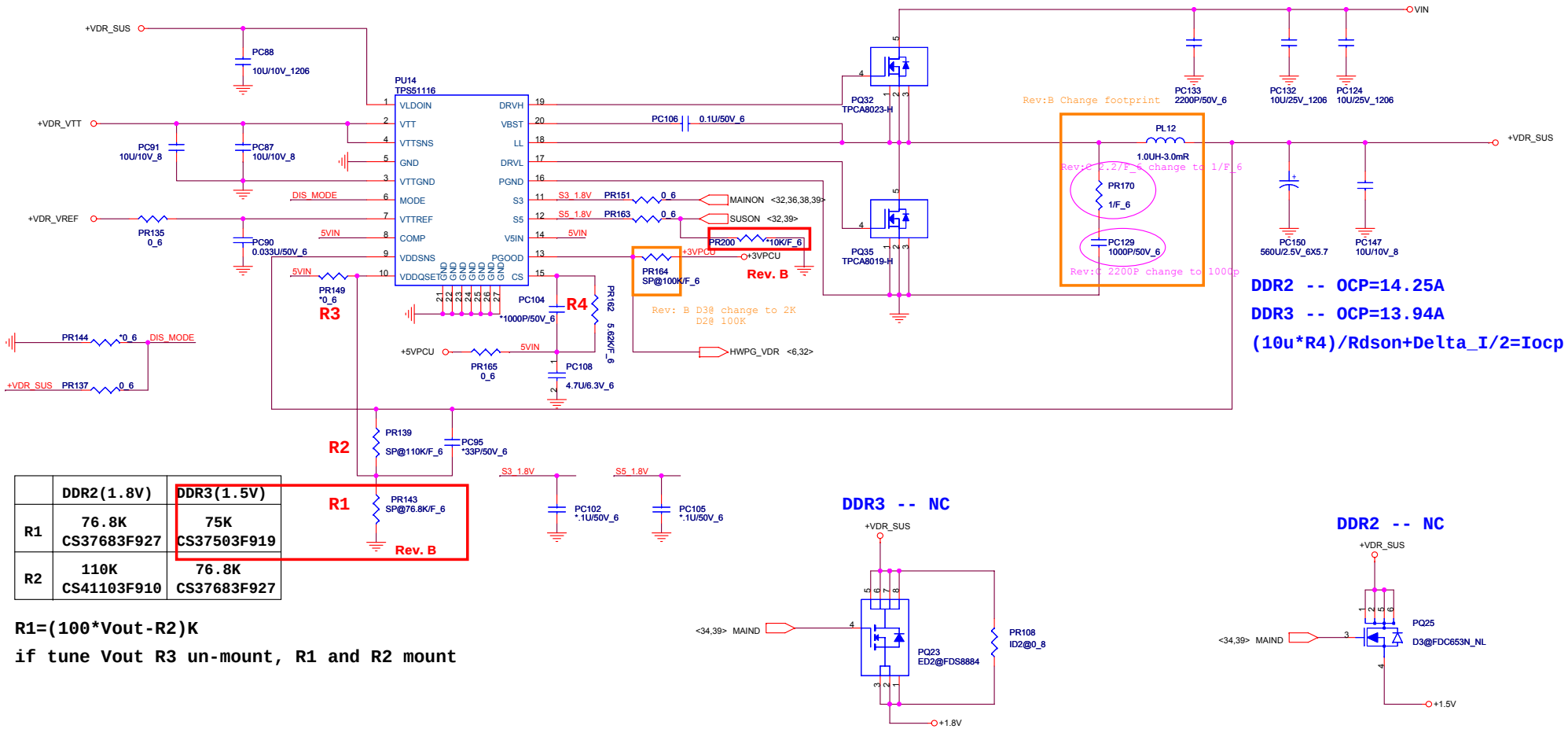
TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

Quanta Computer Inc.

PROJECT : ZY2 / ZY6

Size	Document Number	Rev
	VTT 1.05V (RT8202)	1A
Date: Tuesday, April 08, 2008	Sheet 36 of 40	

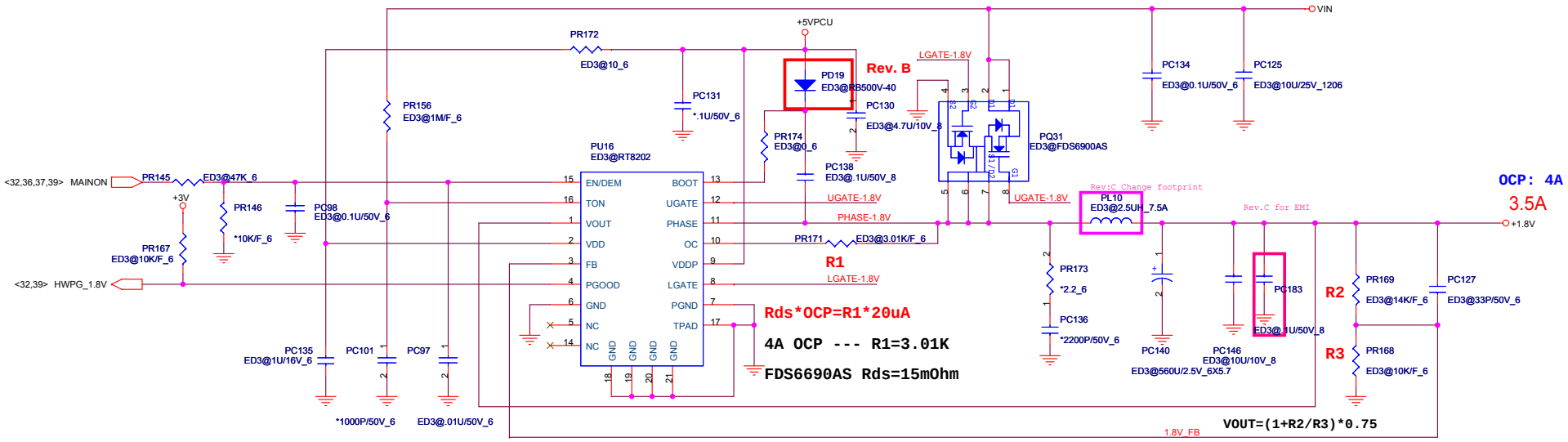


	DDR2(1.8V)	DDR3(1.5V)
R1	76.8K CS37683F927	75K CS37503F919
R2	110K CS41103F910	76.8K CS37683F927

R1=(100*Vout-R2)K

if tune Vout R3 un-mount, R1 and R2 mount

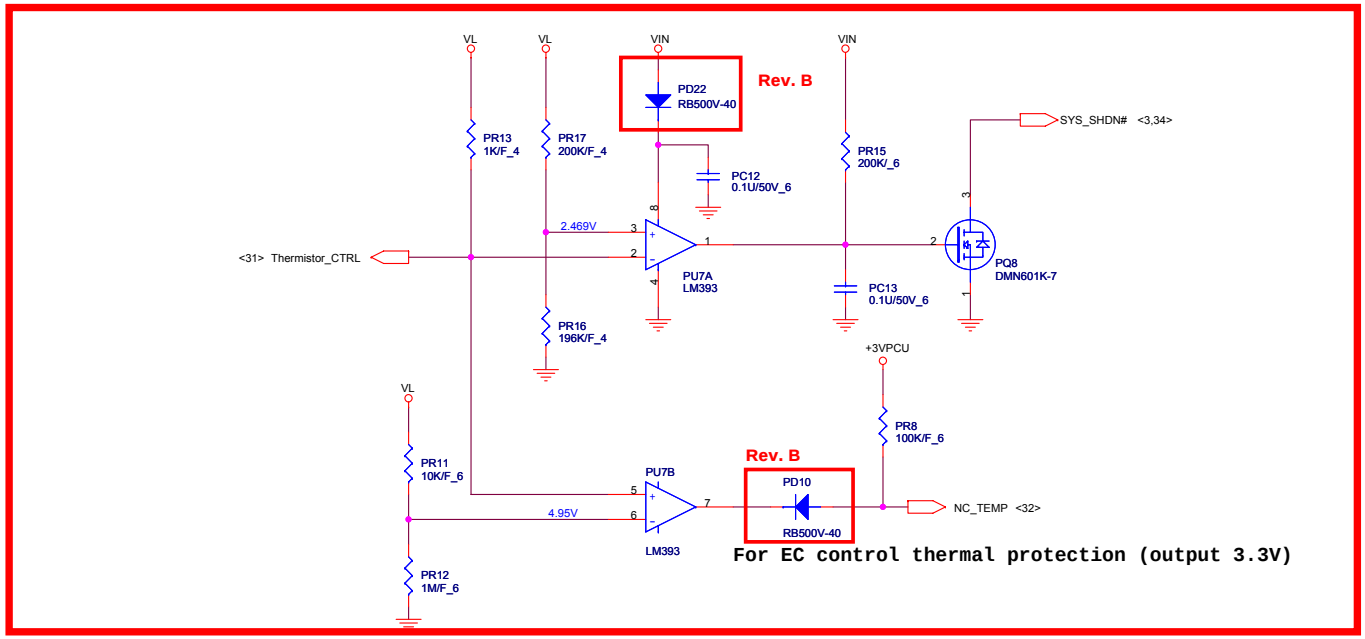
Quanta Computer Inc.		
PROJECT : ZY2 / ZY6		
Size	Document Number VDR (TPS51116)	Rev 1A
Date: Tuesday, April 08, 2008	Sheet 37 of 40	



TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

thermal protection --0928

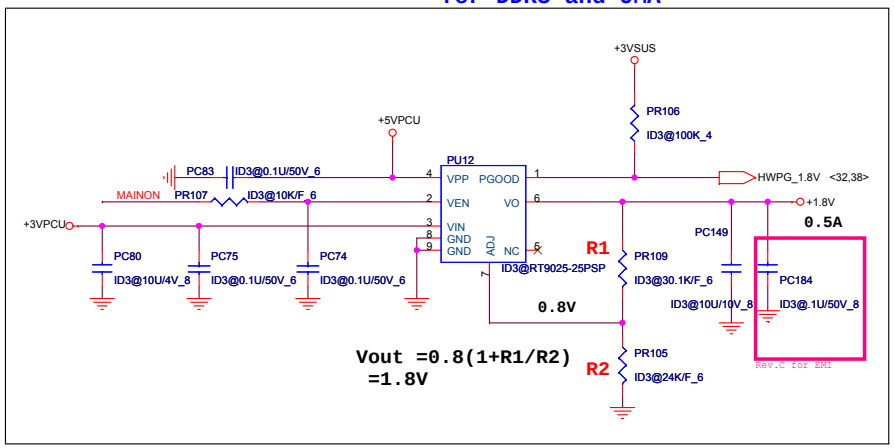


Quanta Computer Inc.

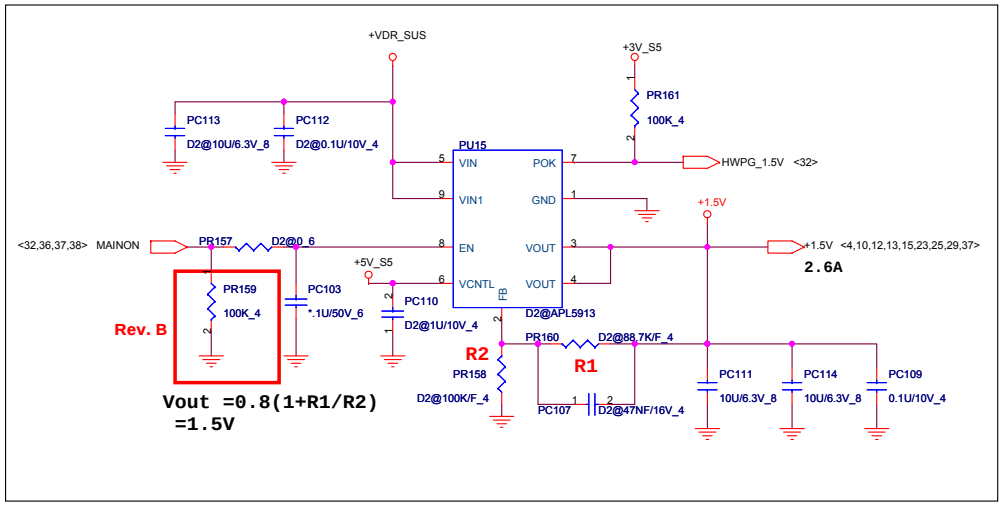
PROJECT : ZY2 / ZY6

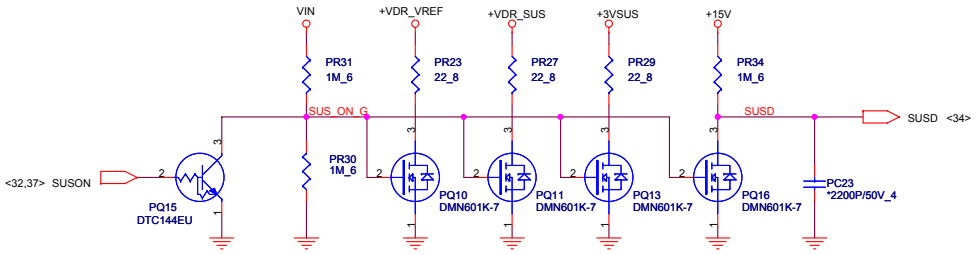
Size	Document Number	Rev
	1.8V (RT8202)	1A
Date: Tuesday, April 08, 2008	Sheet 38 of 40	

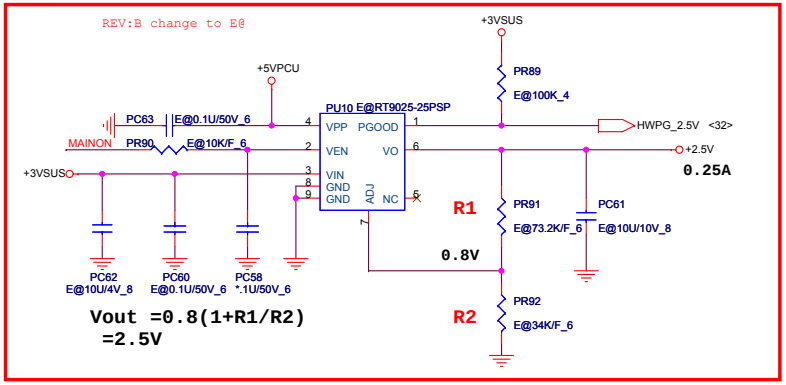
for DDR3 and UMA

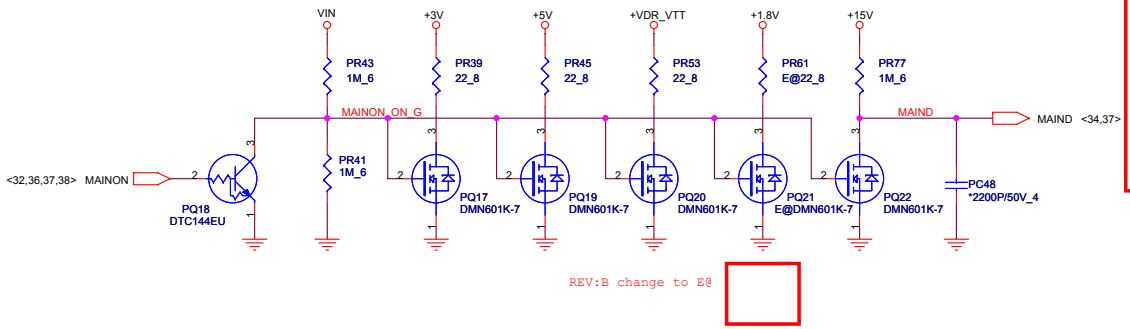


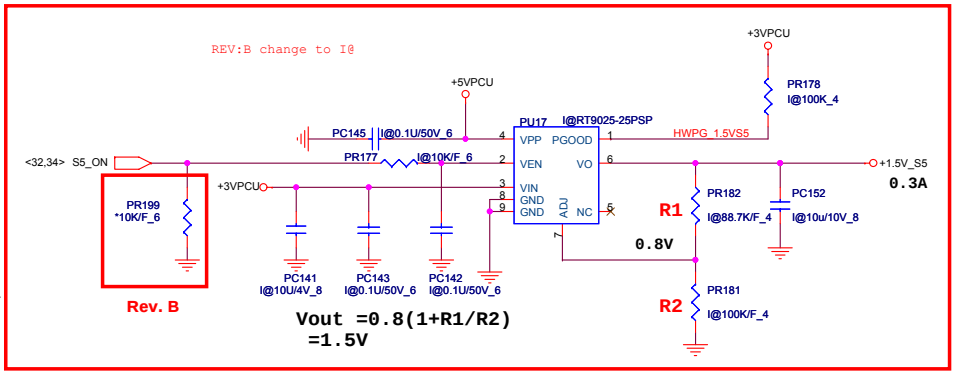
DDR3 -- NC









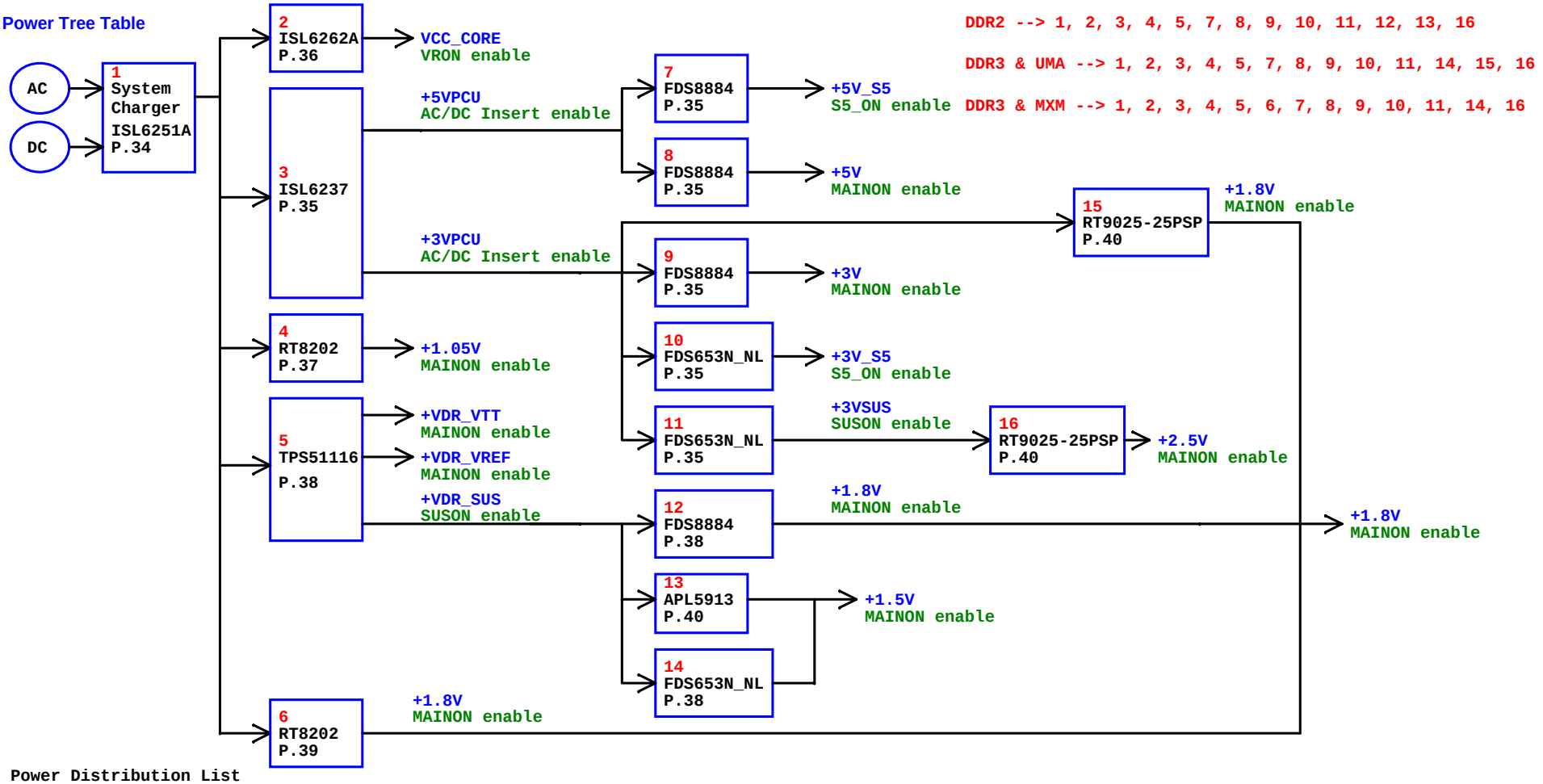


Quanta Computer Inc.

PROJECT : ZY2 / ZY6

Size	Document Number	Rev
	Discharge (2.5V/1.5V)	1A
Date: Tuesday, April 08, 2008	Sheet 39 of 40	

Power Tree Table



Power Distribution List

Power	Distribution
VCC_CORE	CPU
+5VPCU	ICH8M, RJ45/USB /B, USB/eSATA, Satellite LED, CIR
+3VPCU	RTC, HALL SENSOR, KB, TP/FP/LED /B, Power /B, Kill SW, EC, ID, SPI Flash, CIR
+1.5V	CPU, GMCH, ICH9M, Mini Card, New Card
+VDR_SUS	GMCH, DDR
+VDR_VREF	GMCH, DDR
+VDR_VTT	DDR
+1.05V	CPU, CLK, Thermal Trip, GMCH, ICH8M
+5V_S5	ICH8M, G-SENSOR, Felica, USB/eSATA
+5V	CPU, ICH8M, VGA, Camera, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, TP/FP/LED /B, EC, Speaker, Headphone
+3V	CLK, CPU Thermal Monitor, FAN, GMCH, DDR, ICH8M, VGA, LCD/LED Panel, HALL SENSOR, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, Cardreader (OZ129T) Mini Card, KB, TP/FP/LED /B, RJ45/USB /B, Bluetooth, MMB, New Card, PC BEEP, EC, Codec (CX20561), VR, Headphone, MDC
+3V_S5	ICH8M, Mini Card, RJ45/USB /B, New Card
+3VSUS	ICH8M, FP
+1.8V	Cardreader
+2.5V	MXM

Quanta Computer Inc.
PROJECT : ZY2 & ZY6
Size | Document Number: Power Tree Table | Rev: 1A
Date: Tuesday, April 08, 2008 | Sheet 40 of 40

CHANGE LIST

Model	REV	
ZY2 MB	1A	FIRST RELEASED: E200610-3793 (PCB:)
	1B	Page2 : Add R475 ,531 & R532 to avoid active error. (follow CK505 design guideline) Page2 : Swap SRC4 & SRC9, because NEW_CLKREQ# is only to control SRC1 or 4 Page3 : Add R540 to avoid active error. (CPU Thermal monitor) Page6 : Follow DDR3 spec R251 change to 10K. Page18 : POP C282 &C284 and RSVD. C604 for DDR3 PCB boot issue. Page18 : HDA_RST# PIN change from 151 to 134 for customer request. Page18 : Swap Net:TX0 &TX2 (RN15 & RN17) For HDMI no function issue. Page20 : Add R527 ,R528 ,R529 ,R530 ,R539 ,R148 ,R153 ,R152 ,R104 & R105 for vendor request.(HDMI level shifter) Page20 : Change HDMI SW IC (U9) & schematic Page23 : Add R536 ,R542 ,R538 ,RP57 ,R537 customer request.(MINI PCI-E card function) Page25 : add Intel Low Power ECR Solution(Audio) Page28 : Add part for D3 Enhanced (D3E).(cerd reader) Page29 : Add Keyboard LED function for customer request. Page30 : Location :C25 & C23 change to 100U & POP it for customer request.(USB) Page31 : Add D43 for customer request(FOR Dock :CRT _SENSE#) Page31 : CN12 & CN14 change footprint.(K/B & T/P CONN.) Page31 : Add C609 ,C606 & C608.(FOR DOCK : +5V & +5V_S5)
	2A	Page19 : change U22 LVDS PWR SW IC to TI for display isuue Page21 : remove 5787 schematic Page23 : Add C605 ,C70 ,C150 ,C613 &C614 for EMI request Page23 : Change CN27 CONN. & schematic for intel WL burnout issue Page25 :change U13 packing from TQFN to TDFN for vendor request
	2B	Page20 : Add

MODEL	ZY2 FROM	ZY2 To
	X	1A
	X	1A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	2A	2B
	2A	2B
	2A	2B
	2A	2B
	2A	2B
	2A	2B
	2A	2B
	2A	2B
	2B	3A
	2B	3A
	2B	3A
	2B	3A
	2B	3A
	2B	3A
	2B	3A

PROJECT : ZY2
Quanta Computer Inc.

Size	Document Number	Rev
	Change list	1A

Date: Wednesday, April 09, 2008 Sheet 41 of 41

DOC NO.	PROJECT MODEL :	ZY2	APPROVED BY:		DATE:	2007/ 2/15
	PART NUMBER:		DRAWING BY:		REVISON:	3A