ZRA SYSTEM DIAGRAM

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : IN3
LAYER 7 : GND
LAYER 8 : BOT

DDR3-SODIMM1 PAGE 7 — DDR3 channel A
DDR3-SODIMM2 PAGE 8 — DDR3 channel B

AMD Champlain
35mm X 35mm
S1G4 Processor
638P (PGA)45W/35W
PAGE 4,5,6

CPU THERMAL SENSOR PAGE 6

From SB Option

14.318MHz

CLOCK GEN
ICS9LPRS476AKLFT-->HP
SLG8SP628VTR-->HP
RTM880N-796 -->HP
PAGE 3

CPU_CLK
NBGFX_CLK
NBGPP_CLK
SBLINK_CLK

HT3

PCI-E

NORTH BRIDGE
RS880
A12
21mm X 21mm, 528pin BGA
PAGE 9,10,11,12

PCI-Express 16X

ATI
Madison LP
128-bit M2 Pkg
29mm X 29mm
PAGE 18,19,20,21,22,23

800MHz
VRAM DDR3
64MX16X8,128bit
128MX16X8,128 bit
PAGE 24,25

VGA
Madison/Park

X1 Port 0
LAN
BCM 57760
PCIE-LAN
(10/100/1000)
PAGE 27

X1 Port 2
Mini PCI-E Card
(Wireless LAN)
PAGE 28

1 to 2 Switch

Lan_PCIE1
Lan_PCIE2

Docking

RJ45
PAGE 27

DVI
LVDS
CRT

MUXs (S.G)

1 to 2 Switch

On board LVDS
On board CRT

ALINK X4

SOUTH BRIDGE
SB820
21mm X 21mm, 528pin BGA
4.5W(Ext)
4.3W(Int)
PAGE 13,14,15,16,17

USB2.0 x 1
Lan_PCIE1

Docking
PAGE 36

CRT connector
DVI connector
USB connector x 3
RJ45 connector
MIC
Line out
Line in

USB2.0
Finger print PAGE 32
BT PAGE 32

MIC to Docking
Line out to Docking
Line in from Docking

SATA0 150MB
SATA - HDD1 PAGE 29

SATA1 150MB
SATA - CD-ROM PAGE 29

USB2.0 Ports X1 PAGE 32
Webcam PAGE 26
CardReader AU6437 PAGE 31
WLAN conn PAGE 28

TPM PAGE 28

LPC
Azalia

Winbond KBC
NPCE781L
PAGE 35

Codec CX20672-11Z
PAGE 30

MIC to Docking
Line out to Docking
Line in from Docking

MDC
PAGE 30

USB BOARD
USB2.0 Ports x3
PAGE 32

Power BOARD
PAGE 33

Keyboard PAGE 34
Touch Pad PAGE 32

CPU FAN PAGE 34

SPI PAGE 35

Digital MIC PAGE 30

AUDIO CONN (Phone/ MIC) PAGE 30

Speaker PAGE 30

AMD CPU CORE (ISL6265) PAGE 39
NB_CORE (UP6111AQDD) PAGE 41
+VGPU_CORE (MAX8792ETD) PAGE 43
1.1V (UP6111AQDD) PAGE 40
1.8V/GPU_Power/+2.5V PAGE 44
DDR 1.5V(RT8207) PAGE 42
SYSTEM 5V/3V (RT8206) PAGE 38
1V/CPU_VDDR/Discharage PAGE 45
Charger (ISL88731) PAGE 37

Quanta Computer Inc.
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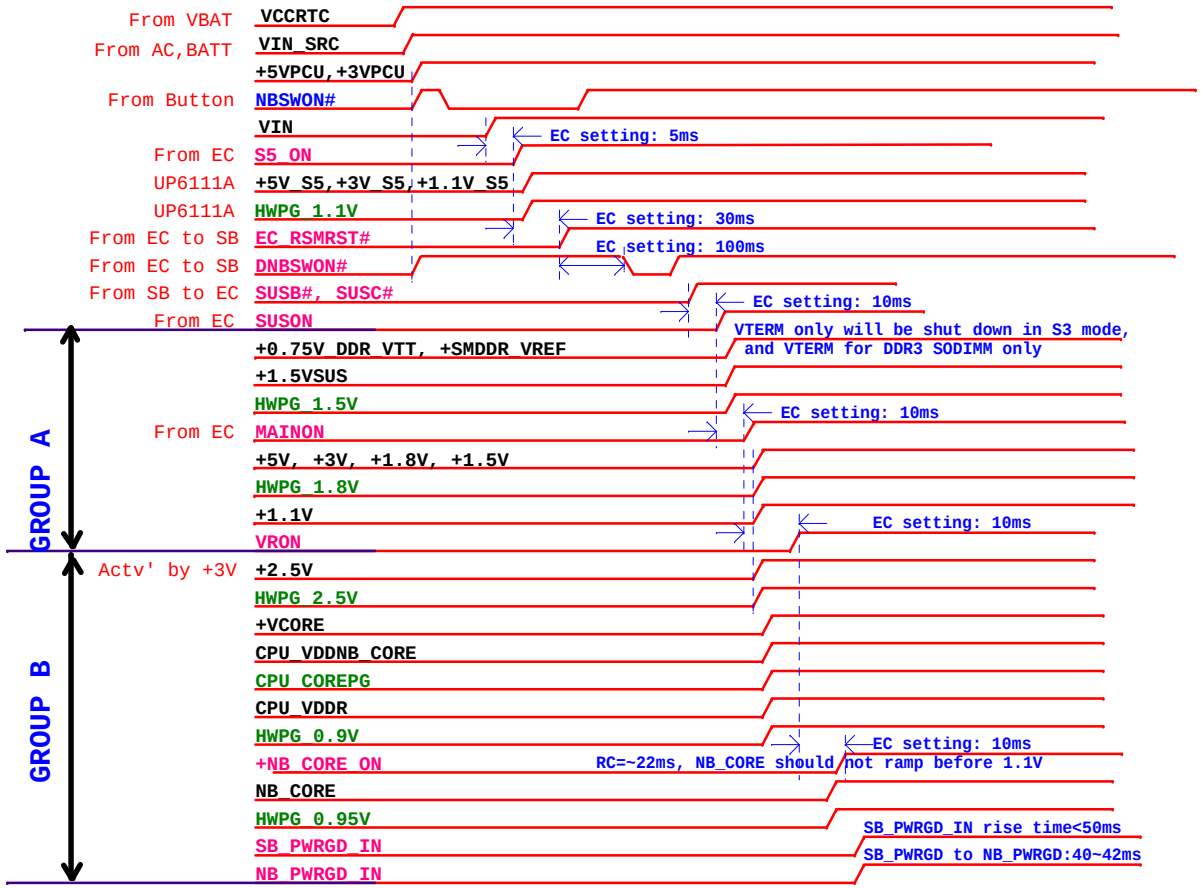
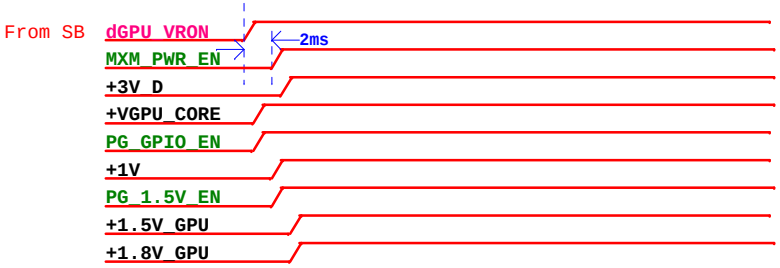
Date: Monday, March 29, 2010 | Sheet 1 of 48

Danube Power On Sequence



Notice:
1.CPU_LDT_RST# msut be asserted a minimum of 1ms prior to the assertion of CPU_PWRGD
2.CPU_CLKP/N must be within specification a minimum of 1ms prior to the assertion of CPU_PWRGD
3.CPU_PWRGD remains deasserted at least 1ms after both CPU_CLKP/N and all voltages to the processor are within specification for operation
4.all NB power rails(1.8V/1.2V/1.1V) valid before NB_PWRGD at least 1ms
5.stable input clocks from CLKGEN(HT_REFCLKP/N) to NB before NB_PWRGD at least 1ms

Danube GPU Power Sequence



Power on sequence required:

SB800:
1.+3.3V_S5 ramp before +1.1_S5
2.+3.3V ramp before +1.8V
3.+1.8V ramp before +1.1V
4.+3.3V ramp before +1.1V
5.+3.3V_S5 ramping down time>300us
6.All power rails rise time >= 50us, except +3.3V_S5<=40ms
7.100us<=+3.3V_S5 rise time<=40ms
9.VBAT (VCCRTC) must ramp at least 5 seconds before the S5 rails to allow start time for the internal RTC

(only in SB820M NB_PWRGD signal)
40ms <= SB PWRGOOD to NB_PWRGD delay <= 42ms

RS880:
1.0<(+3.3V)-(+1.8V)<2.1
2.+1.8V ramp before +1.1V
3.+1.1V ramp before CPU_VDDNB_CORE

BOM naming rule

Items	Function	Name	Description
1	Internal CLK GEN	SGN@	
2	External CLK GEN	GN@	
3	iGPU	IV@	
4	dGPU	SW@	
5	iGPU & dGPU notice	SP@	

SB SMBUS Table

	CLK GEN	RAM	Mini Card (WLAN)
(SB_DA0)/(SB_CL0) (+3V)	V	V	V
Power Plane	+3V	+3V	+3V
MOS CKT (Level shift)	X	X	X*

*Reserve: There is not SMBUS function in AVL

EC SMBUS Table

	Battery	CPU thermal Sensor
EC775 SDA1 / SCL1 (+3VPCU)	V	
EC775 SDA2 / SCL2 (+3V)		V
EC775 SDA3 / SCL3 ()		
Power Plane	+3VPCU	+3V
MOS CKT (Level shift)	X	X

Quanta Computer Inc.
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S1G4

1.1V@1.5A

+1.1V → R486 0_6 → +1.1V_VLDT

R483 0_6

P/N: DG0^8000005
DG0^8000009
DG0^80000013
DG0^80000014

SI Change from AMD request

8 HT_CADINP[15..0] HT_CADINP[15..0]
8 HT_CADINN[15..0] HT_CADINN[15..0]
8 HT_CLKINP[1..0] HT_CLKINP[1..0]
8 HT_CLKINN[1..0] HT_CLKINN[1..0]
8 HT_CTLINP[1..0] HT_CTLINP[1..0]
8 HT_CTLINN[1..0] HT_CTLINN[1..0]
8 HT_CADOUTP[15..0] HT_CADOUTP[15..0]
8 HT_CADOUTN[15..0] HT_CADOUTN[15..0]
8 HT_CLKOUTP[1..0] HT_CLKOUTP[1..0]
8 HT_CLKOUTN[1..0] HT_CLKOUTN[1..0]
8 HT_CTLOUTP[1..0] HT_CTLOUTP[1..0]
8 HT_CTLOUTN[1..0] HT_CTLOUTN[1..0]

BLM21PG221SN1D(220 100M2A)_8

+2.5V → L44 → +CPUVDDA

2.5V@250mA

C781 4.7u/6.3V_6 LS0805-100M-N
C483 4.7u/6.3V_6
C459 0.22u/6.3V_4
C463 3300P/50V_4
C469 *10u/6.3V_8

W/S= 15 mil/20mil

U30A

HT LINK

VLDT_A0 VLDT_A1 VLDT_A2 VLDT_A3
VLDT_B0 VLDT_B1 VLDT_B2 VLDT_B3

C450 10u/6.3V_8 +1.1V_VLDT D1
C746 10u/6.3V_8 +1.1V_VLDT D2
C453 0.22u/6.3V_4 +1.1V_VLDT D3
C314 180P/50V_4 +1.1V_VLDT D4

AE2 +1.1V_VLDT 10u/6.3V_8 C449
AE3 +1.1V_VLDT 0.22u/6.3V_4 C318
AE4 +1.1V_VLDT 180P/50V_4 C448
AE5 +1.1V_VLDT

HT_CADINP0 E3 L0_CADIN_H0 L0_CADOUT_H0 AD1 HT_CADOUTP0
HT_CADINN0 E2 L0_CADIN_L0 L0_CADOUT_L0 AC1 HT_CADOUTN0
HT_CADINP1 F1 L0_CADIN_H1 L0_CADOUT_H1 AC2 HT_CADOUTP1
HT_CADINN1 F1 L0_CADIN_L1 L0_CADOUT_L1 AC3 HT_CADOUTN1
HT_CADINP2 G3 L0_CADIN_H2 L0_CADOUT_H2 AB1 HT_CADOUTP2
HT_CADINN2 G2 L0_CADIN_L2 L0_CADOUT_L2 AA1 HT_CADOUTN2
HT_CADINP3 G1 L0_CADIN_H3 L0_CADOUT_H3 AA2 HT_CADOUTP3
HT_CADINN3 H1 L0_CADIN_L3 L0_CADOUT_L3 AA3 HT_CADOUTN3
HT_CADINP4 J1 L0_CADIN_H4 L0_CADOUT_H4 W2 HT_CADOUTP4
HT_CADINN4 K1 L0_CADIN_L4 L0_CADOUT_L4 W3 HT_CADOUTN4
HT_CADINP5 L3 L0_CADIN_H5 L0_CADOUT_H5 V1 HT_CADOUTP5
HT_CADINN5 L2 L0_CADIN_L5 L0_CADOUT_L5 U1 HT_CADOUTN5
HT_CADINP6 L1 L0_CADIN_H6 L0_CADOUT_H6 U2 HT_CADOUTP6
HT_CADINN6 M1 L0_CADIN_L6 L0_CADOUT_L6 U3 HT_CADOUTN6
HT_CADINP7 N3 L0_CADIN_H7 L0_CADOUT_H7 T1 HT_CADOUTP7
HT_CADINN7 N2 L0_CADIN_L7 L0_CADOUT_L7 R1 HT_CADOUTN7
HT_CADINP8 E5 L0_CADIN_H8 L0_CADOUT_H8 AD4 HT_CADOUTP8
HT_CADINN8 F5 L0_CADIN_L8 L0_CADOUT_L8 AD3 HT_CADOUTN8
HT_CADINP9 F3 L0_CADIN_H9 L0_CADOUT_H9 AD5 HT_CADOUTP9
HT_CADINN9 F4 L0_CADIN_L9 L0_CADOUT_L9 AC5 HT_CADOUTN9
HT_CADINP10 G5 L0_CADIN_H10 L0_CADOUT_H10 AB4 HT_CADOUTP10
HT_CADINN10 H5 L0_CADIN_L10 L0_CADOUT_L10 AB3 HT_CADOUTN10
HT_CADINP11 H3 L0_CADIN_H11 L0_CADOUT_H11 AB5 HT_CADOUTP11
HT_CADINN11 H4 L0_CADIN_L11 L0_CADOUT_L11 AA5 HT_CADOUTN11
HT_CADINP12 K3 L0_CADIN_H12 L0_CADOUT_H12 Y5 HT_CADOUTP12
HT_CADINN12 K4 L0_CADIN_L12 L0_CADOUT_L12 W5 HT_CADOUTN12
HT_CADINP13 L5 L0_CADIN_H13 L0_CADOUT_H13 V4 HT_CADOUTP13
HT_CADINN13 M5 L0_CADIN_L13 L0_CADOUT_L13 V3 HT_CADOUTN13
HT_CADINP14 M3 L0_CADIN_H14 L0_CADOUT_H14 V5 HT_CADOUTP14
HT_CADINN14 M4 L0_CADIN_L14 L0_CADOUT_L14 U5 HT_CADOUTN14
HT_CADINP15 N5 L0_CADIN_H15 L0_CADOUT_H15 T4 HT_CADOUTP15
HT_CADINN15 P5 L0_CADIN_L15 L0_CADOUT_L15 T3 HT_CADOUTN15

HT_CLKINP0 J3 L0_CLKIN_H0 L0_CLKOUT_H0 Y1 HT_CLKOUTP0
HT_CLKINN0 J2 L0_CLKIN_L0 L0_CLKOUT_L0 W1 HT_CLKOUTN0
HT_CLKINP1 J5 L0_CLKIN_H1 L0_CLKOUT_H1 Y4 HT_CLKOUTP1
HT_CLKINN1 K5 L0_CLKIN_L1 L0_CLKOUT_L1 Y3 HT_CLKOUTN1

HT_CTLINP0 N1 L0_CTLIN_H0 L0_CTLOUT_H0 R2 HT_CTLOUTP0
HT_CTLINN0 P1 L0_CTLIN_L0 L0_CTLOUT_L0 R3 HT_CTLOUTN0
HT_CTLINP1 P3 L0_CTLIN_H1 L0_CTLOUT_H1 T5 HT_CTLOUTP1
HT_CTLINN1 P4 L0_CTLIN_L1 L0_CTLOUT_L1 R5 HT_CTLOUTN1

SOCKET_638_PIN

CPU CLK

12 CLK_CPU_BCLKP_PR → CLK_CPU_BCLKP_PR
12 CLK_CPU_BCLKN_PR → CLK_CPU_BCLKN_PR

Keep trace from resisor to CPU within 0.6"
keep trace from caps to CPU within 1.2"

CLK_CPU_BCLKP_C R516 169/F_4 CLK_CPU_BCLKN_C

CLK_CPU_BCLKP_PR C780 3900P/25V_4 CLK_CPU_BCLKP_C
CLK_CPU_BCLKN_PR C779 3900P/25V_4 CLK_CPU_BCLKN_C

B-TEST 0205

+1.5VSUS → R490 1K_4 R488 1K_4 R487 1K_4

5 SIC
5 SID
5 ALERT_L

SideBand-Temp sense I2C

S1G4 +1.1V_VLDT → R220 44.2/F_4 CPU_HTREF0
R218 44.2/F_4 CPU_HTREF1
place them to CPU within 1.5"

38 CPU_VDD0_FB_H
38 CPU_VDD0_FB_L

38 CPU_VDD1_FB_H
38 CPU_VDD1_FB_L

4,5,6,7,15,29,38,41,43,44 +1.5VSUS
27,29,41,44 +1.5V
8,9,10,11,15,39 +1.1V
43 +2.5V

+1.5VSUS +1.5V +1.1V +2.5V

SB check list tide to CPUVDDIO (+1.5VSUS)

CPU_PWRGD 300_4 R514
CPU_LDT_RST# 300_4 R509
CPU_LDT_STOP# 300_4 R243
CPU_LDT_REQ#_CPU *300_4 R505
→ +1.5V

+CPUVDDA 250mA

W/S= 15 mil/20mil

U30D

VDDA1 VDDA2 F8 F9 +CPUVDDA +CPUVDDA
CLKIN_H A9 CLK_CPU_BCLKP_C
CLKIN_L A8 CLK_CPU_BCLKN_C
RESET_L B7 CPU_LDT_RST#
PWROK A7 CPU_PWRGD
LDTSTOP_L F10 CPU_LDT_STOP#
LDTREQ_L C6 CPU_LDT_REQ#_CPU
SIC AF4
SID AF5
ALERT_L AE6
HT_REF0 R6
HT_REF1 P6
VDD0_FB_H F6
VDD0_FB_L E6
VDD1_FB_H Y6
VDD1_FB_L AB6
DBRDY G10 CPU_DBRDY
TMS AA9 CPU_TMS
TCK AC9 CPU_TCK
TRST_L AD9 CPU_TRST#
TDI AF9 CPU_TDI
TEST23 AD7 CPUTEST23
TEST18 H10 CPUTEST18
TEST19 G9 CPUTEST19
TEST25_H E9 CPUTEST25H
TEST25_L E8 CPUTEST25L
TEST21 AB8 CPUTEST21
TEST20 AF7 CPUTEST20
TEST24 AE7 CPUTEST24
TEST22 AE8 CPUTEST22
TEST12 AC8 CPUTEST12
TEST27 AF8 CPUTEST27
TEST9 C2 TEST9
TEST6 AA6
RSVD1 A3
RSVD2 A5
RSVD3 B3
RSVD4 B5
RSVD5 C1
VSS M11
RSVD11 W18
SVC A6 CPU_SVC_R
SVD A4 CPU_SVD_R
THERMTRIP_L AF6 CPU_THERMTRIP_L#
PROCHOT_L AC7 CPU_PROCHOT_L#
MEMHOT_L AA8 CPU_MEMHOT_L#
THERMDC W7 H_THRMDC 5
THERMDA W8 H_THRMDA 5
VDDIO_FB_H W9 VDDIO_FB_H
VDDIO_FB_L Y9 VDDIO_FB_L
VDDNB_FB_H H6 CPU_VDDNB_FB_H 38
VDDNB_FB_L G6 CPU_VDDNB_FB_L 38
DBREQ_L E10 CPU_DBREQ# R520 300_4 +1.5VSUS
TDO AE9 CPU_TDO
TEST28_H J7
TEST28_L H8
TEST17 D7 CPUTEST17 T30
TEST16 E7 CPUTEST16 T29
TEST15 F7 CPUTEST15 T28
TEST14 C7 CPUTEST14 T33
TEST7 C3
TEST10 K8
TEST8 C4
TEST29_H C9 CPUTEST29H T72
TEST29_L C8
RSVD10 H18
RSVD9 H19
RSVD8 AA7 CPUTEST29L
RSVD7 D5
RSVD6 C5
R511 80.6/F_4 T73

SOCKET_638_PIN

S1G4

FOX PZ63826-284R-41F
DG0^8000004 IC SOCKET SMD 638P S1(P1.27,H3.2)
MLX 47296-4131
DG0^8000003 IC SOCKET SMD 638P S1(P1.27,H3.2)
TYC 4-1903401-2
DG0^8000005 IC SOCKET SMD 638P S1(P1.27,H3.2)

B-TEST 0205

+3V → R524 20K/F_4 → CNTR_VREF 5
C778 0.1u/10V_4
R529 34.8K/F_4 → CNTR_VREF

CPU_LDT_REQ# CPU → Q35 *BSS138_NL/SOT23 → CPU_LDT_REQ# 10
R508 *0_4

+3V → R532 4.7K_4 S1G4 → CPU_LDT_RST_HTPA#
CPU_LDT_RST# → Q36 BSS138_NL/SOT23

G2 *SHORT_PAD1 for debug only

The RS880 family does not support CLMC architecture
The LDTREQ# connection from the CPU to ALLOW_LDTSTOP
of the Northbridge is no longer required.

+1.5VSUS → Q33 FDV301N
16,38,39 CPU_COREPG
R459 *10K_4 D25 *BAS316
R460 100K_6
R461 10K_4
R467 1K_4
R455 0_4 → SYS_SHDN# 18,37,44
Q31 MMBT3904
CPU_THERMTRIP_L# R456 *0_4 → CPU_THERMTRIP# 13

+1.5VSUS → R466 *10K_4
R472 300_4 → Q30 *MMBT3904
CPU_PROCHOT_L# → CPU_PROCHOT# 12,14
R458 0_4

+1.5VSUS → R457 *10K_4
R464 *1K_4 S1G4 → Q32 *MMBT3904
CPU_MEMHOT_L# → CPU_MEMHOT# 6,7,12

S1g4 does not support MEMHOT#

Serial VID

SI Change from AMD request

+1.5VSUS +1.5V → R530 1K_4 R526 *1K_4
+1.5VSUS +1.5V → R531 1K_4 R527 *1K_4

CPU_SVC_R R513 *short_4
CPU_SVD_R R512 *short_4
CPU_PWRGD R515 *short_4

R523 *220_4
R522 *220_4
R525 *220_4

CPU_SVC 38
CPU_SVD 38
CPU_PWRGD_SVID_REG 38

VFIX MODE — VID Override Circuit

SVC	SVD	Voltage Output
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

S1G4

HDT Connector

+1.5VSUS → C484 *0.1u/10V_4

CPU_DBREQ#
CPU_DBRDY
CPU_TCK
CPU_TMS
CPU_TDI
CPU_TRST#
CPU_TDO

CPU_LDT_RST_HTPA#

KEY
*HDT_CONN
CN7

CPUTEST24 R475 1K_4
CPUTEST23 R473 *1K_4
CPUTEST20 R474 1K_4
CPUTEST22 R476 1K_4
CPUTEST12 R184 1K_4
CPUTEST15 R229 1K_4
CPUTEST14 R534 1K_4
CPUTEST19 R533 1K_4
CPUTEST18 R236 1K_4
CPUTEST21 R159 1K_4

S1G4

Quanta Computer Inc.
PROJECT : ZRA

Size	Document Number	Rev
	S1G4 HT,CTL I/F 1/3	1A
Date: Monday, March 29, 2010	Sheet 3 of 48	

Processor Memory Interface

VDDR=> 0.9V support 1066 / 800 DDR
VDDR= >1.05V support 1333 / 1066 / 800 DDR

CPU_VDDR VDDR=>1.75A

+1.5VSUS

PLACE THEM CLOSE TO CPU WITHIN 1"

R465 0_4

C739 10u/6.3V_8

S1G4

CPU_VDDR

U30B

MEM:CMD/CTRL/CLK

VDDR1 VDDR2 VDDR3 VDDR4 VDDR5 VDDR6 VDDR7 VDDR8 VDDR9

MEMZP MEMZN VDDR_SENSE

MA_RESET_L MEMVREF

MA0_ODT0 MA0_ODT1 MA1_ODT0 MA1_ODT1 MB0_ODT0 MB0_ODT1 MB1_ODT0

MA0_CS_L0 MA0_CS_L1 MA1_CS_L0 MA1_CS_L1 MB0_CS_L0 MB0_CS_L1 MB1_CS_L0

MA_CKE0 MA_CKE1 MB_CKE0 MB_CKE1

MA_CLK_H5 MA_CLK_L5 MA_CLK_H1 MA_CLK_L1 MA_CLK_H7 MA_CLK_L7 MA_CLK_H4 MA_CLK_L4 MB_CLK_H5 MB_CLK_L5 MB_CLK_H1 MB_CLK_L1 MB_CLK_H7 MB_CLK_L7 MB_CLK_H4 MB_CLK_L4

MA_ADD0 MA_ADD1 MA_ADD2 MA_ADD3 MA_ADD4 MA_ADD5 MA_ADD6 MA_ADD7 MA_ADD8 MA_ADD9 MA_ADD10 MA_ADD11 MA_ADD12 MA_ADD13 MA_ADD14 MA_ADD15 MB_ADD0 MB_ADD1 MB_ADD2 MB_ADD3 MB_ADD4 MB_ADD5 MB_ADD6 MB_ADD7 MB_ADD8 MB_ADD9 MB_ADD10 MB_ADD11 MB_ADD12 MB_ADD13 MB_ADD14 MB_ADD15

MA_BANK0 MA_BANK1 MA_BANK2 MB_BANK0 MB_BANK1 MB_BANK2

MA_RAS_L MA_CAS_L MA_WE_L MB_RAS_L MB_CAS_L MB_WE_L

SOCKET_638_PIN

+0.75V_DDR_VTT

+SMDDR_VREF

R482 *0_4

R182 *0_4

CPU_VTT_SENSE

MEMVREF_CPU

C369 0.1u/10V_4

C367 1000P/50V_4

M_B_DQ[0..63] 7

M_A_DQ[0..63] 6

M_B_RST# 7

M_B_ODT0 7

M_B_ODT1 7

M_B_CS#0 7

M_B_CS#1 7

M_B_CKE0 7

M_B_CKE1 7

M_B_CLKP1 7

M_B_CLKN1 7

M_B_CLKP2 7

M_B_CLKN2 7

M_B_A[0..15] 7

M_B_BANK0 7

M_B_BANK1 7

M_B_BANK2 7

M_B_RAS# 7

M_B_CAS# 7

M_B_WE# 7

6,7,41 +0.75V_DDR_VTT

6,7,41 +SMDDR_VREF

44 CPU_VDDR

3,5,6,7,15,29,38,41,43,44 +1.5VSUS

U30C

MEM:DATA

MB_DATA0 MB_DATA1 MB_DATA2 MB_DATA3 MB_DATA4 MB_DATA5 MB_DATA6 MB_DATA7 MB_DATA8 MB_DATA9 MB_DATA10 MB_DATA11 MB_DATA12 MB_DATA13 MB_DATA14 MB_DATA15 MB_DATA16 MB_DATA17 MB_DATA18 MB_DATA19 MB_DATA20 MB_DATA21 MB_DATA22 MB_DATA23 MB_DATA24 MB_DATA25 MB_DATA26 MB_DATA27 MB_DATA28 MB_DATA29 MB_DATA30 MB_DATA31 MB_DATA32 MB_DATA33 MB_DATA34 MB_DATA35 MB_DATA36 MB_DATA37 MB_DATA38 MB_DATA39 MB_DATA40 MB_DATA41 MB_DATA42 MB_DATA43 MB_DATA44 MB_DATA45 MB_DATA46 MB_DATA47 MB_DATA48 MB_DATA49 MB_DATA50 MB_DATA51 MB_DATA52 MB_DATA53 MB_DATA54 MB_DATA55 MB_DATA56 MB_DATA57 MB_DATA58 MB_DATA59 MB_DATA60 MB_DATA61 MB_DATA62 MB_DATA63

MA_DATA0 MA_DATA1 MA_DATA2 MA_DATA3 MA_DATA4 MA_DATA5 MA_DATA6 MA_DATA7 MA_DATA8 MA_DATA9 MA_DATA10 MA_DATA11 MA_DATA12 MA_DATA13 MA_DATA14 MA_DATA15 MA_DATA16 MA_DATA17 MA_DATA18 MA_DATA19 MA_DATA20 MA_DATA21 MA_DATA22 MA_DATA23 MA_DATA24 MA_DATA25 MA_DATA26 MA_DATA27 MA_DATA28 MA_DATA29 MA_DATA30 MA_DATA31 MA_DATA32 MA_DATA33 MA_DATA34 MA_DATA35 MA_DATA36 MA_DATA37 MA_DATA38 MA_DATA39 MA_DATA40 MA_DATA41 MA_DATA42 MA_DATA43 MA_DATA44 MA_DATA45 MA_DATA46 MA_DATA47 MA_DATA48 MA_DATA49 MA_DATA50 MA_DATA51 MA_DATA52 MA_DATA53 MA_DATA54 MA_DATA55 MA_DATA56 MA_DATA57 MA_DATA58 MA_DATA59 MA_DATA60 MA_DATA61 MA_DATA62 MA_DATA63

7 M_B_DM[0..7]

M_A_DM[0..7] 6

MB_DM0 MB_DM1 MB_DM2 MB_DM3 MB_DM4 MB_DM5 MB_DM6 MB_DM7

MA_DM0 MA_DM1 MA_DM2 MA_DM3 MA_DM4 MA_DM5 MA_DM6 MA_DM7

7 M_B_DQSP0 7 M_B_DQSN0 7 M_B_DQSP1 7 M_B_DQSN1 7 M_B_DQSP2 7 M_B_DQSN2 7 M_B_DQSP3 7 M_B_DQSN3 7 M_B_DQSP4 7 M_B_DQSN4 7 M_B_DQSP5 7 M_B_DQSN5 7 M_B_DQSP6 7 M_B_DQSN6 7 M_B_DQSP7 7 M_B_DQSN7

MB_DQS_H0 MB_DQS_L0 MB_DQS_H1 MB_DQS_L1 MB_DQS_H2 MB_DQS_L2 MB_DQS_H3 MB_DQS_L3 MB_DQS_H4 MB_DQS_L4 MB_DQS_H5 MB_DQS_L5 MB_DQS_H6 MB_DQS_L6 MB_DQS_H7 MB_DQS_L7

MA_DQS_H0 MA_DQS_L0 MA_DQS_H1 MA_DQS_L1 MA_DQS_H2 MA_DQS_L2 MA_DQS_H3 MA_DQS_L3 MA_DQS_H4 MA_DQS_L4 MA_DQS_H5 MA_DQS_L5 MA_DQS_H6 MA_DQS_L6 MA_DQS_H7 MA_DQS_L7

M_A_DQSP0 6 M_A_DQSN0 6 M_A_DQSP1 6 M_A_DQSN1 6 M_A_DQSP2 6 M_A_DQSN2 6 M_A_DQSP3 6 M_A_DQSN3 6 M_A_DQSP4 6 M_A_DQSN4 6 M_A_DQSP5 6 M_A_DQSN5 6 M_A_DQSP6 6 M_A_DQSN6 6 M_A_DQSP7 6 M_A_DQSN7 6

SOCKET_638_PIN

Place close to socket

CPU_VDDR

C472 4.7u/6.3V_6 C309 4.7u/6.3V_6 C471 4.7u/6.3V_6 C305 4.7u/6.3V_6 C306 0.22u/6.3V_4 C308 0.22u/6.3V_4 C302 0.22u/6.3V_4 C303 0.22u/6.3V_4

CPU_VDDR

C465 1000P/50V_4 C464 1000P/50V_4 C371 1000P/50V_4 C299 1000P/50V_4 C461 180P/50V_4 C470 180P/50V_4 C468 180P/50V_4 C460 180P/50V_4

Reserved for AMD suggest

+1.5VSUS

R470 0_4

+3VPCU

C734 *0.1u/10V_4

R462 1K/F_4

R469 1K/F_4

C741 *0.47u/10V_4

U27

*OPA343NA/3K

R471 *10_4

MEMVREF_CPU

R481 *10K_4

R468 *0_4

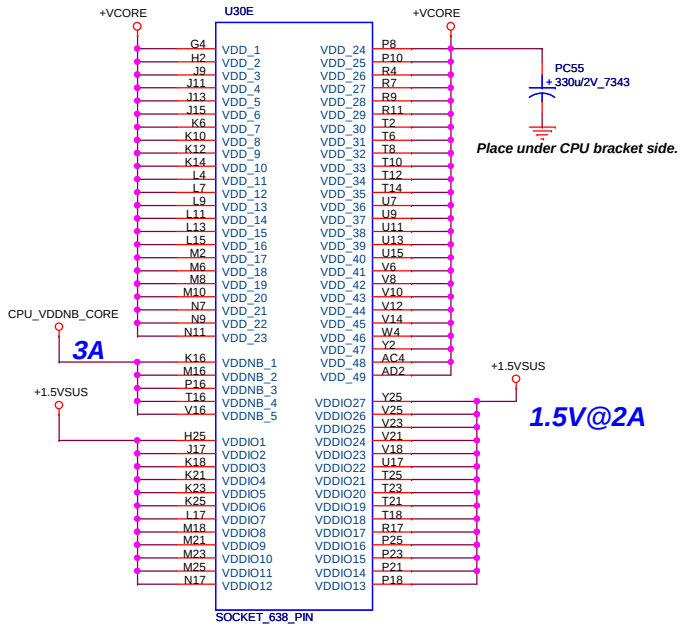
R463 *0_4

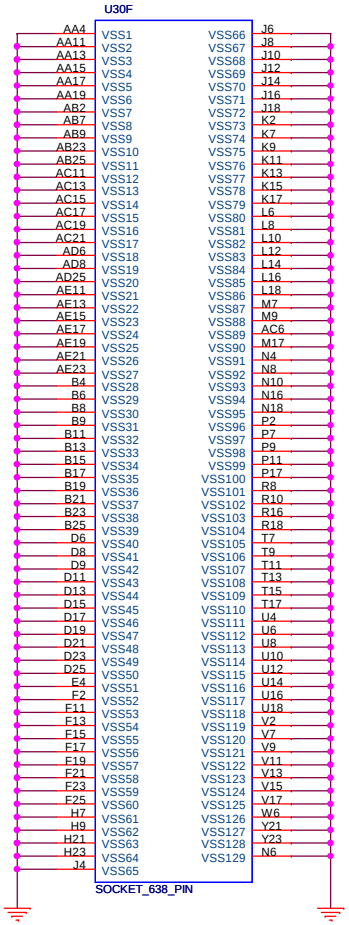
Quanta Computer Inc.

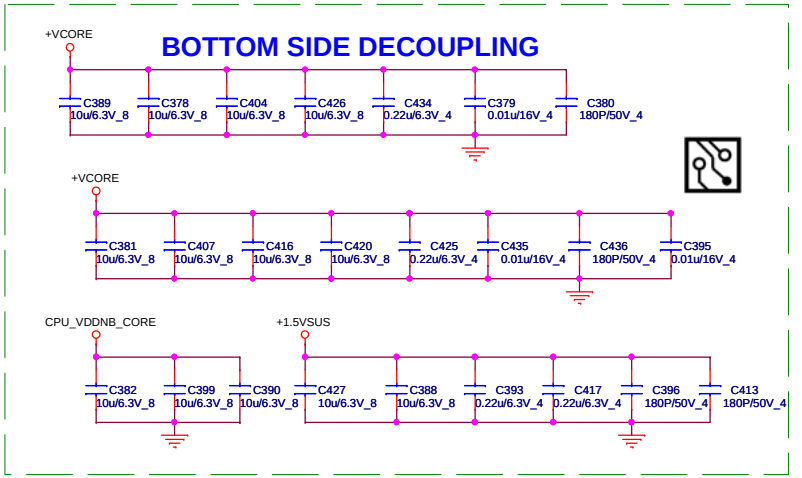
PROJECT : ZRA

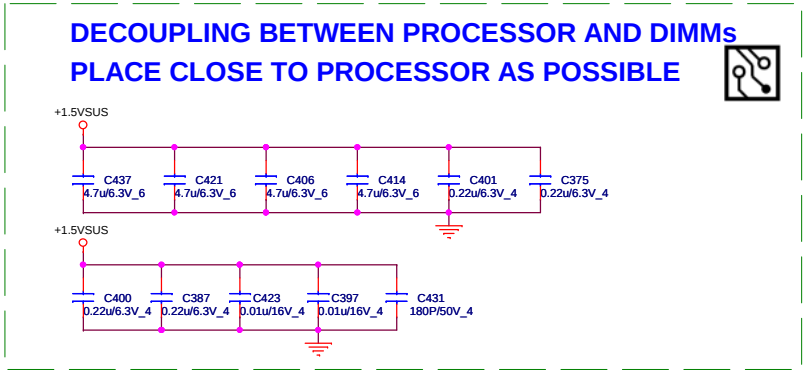
Size	Document Number	Rev
	S1G4 DDRIII MEMORY I/F 2/3	1A

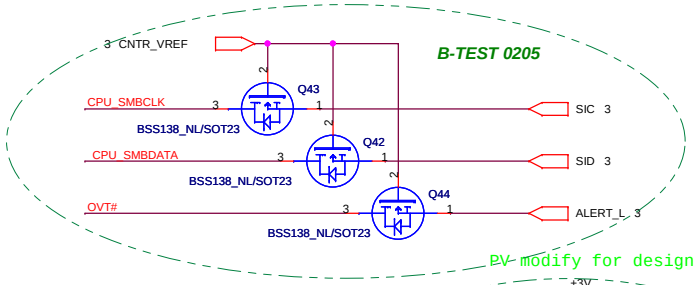
Date: Monday, March 29, 2010 Sheet 4 of 48





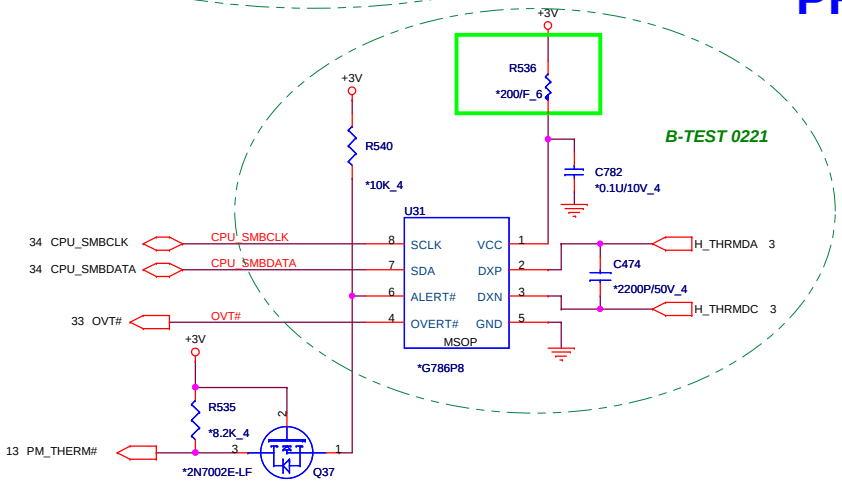






PROCESSOR POWER AND GROUND

PV modify for design

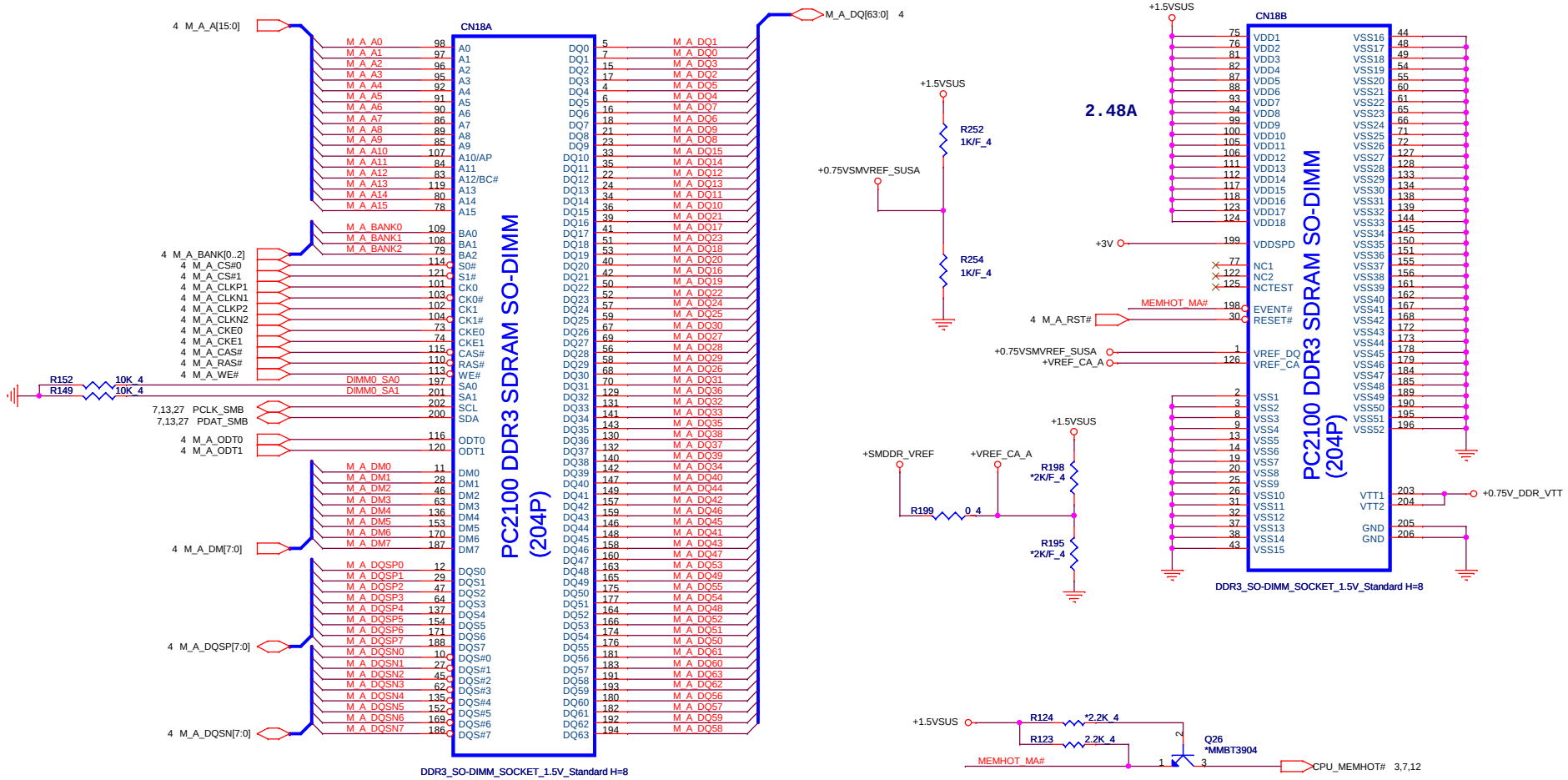


3,4,6,7,15,29,38,41,43,44 +1.5VSUS
38 CPU_VDDNB_CORE
38 +VCORE
12,13,15,16,26,27,29,32,35,37 +3V_S5
3,6,7,10,11,12,13,14,15,16,18,20,25,26,27,29,30,32,33,34,35,37,38,39,40,41,42,43,44 +3V

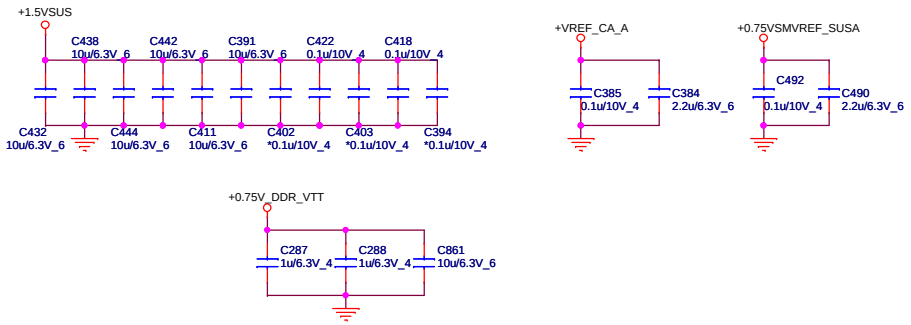
+1.5VSUS
CPU_VDDNB_CORE
+VCORE
+3V_S5
+3V

Quanta Computer Inc.
PROJECT : ZRA

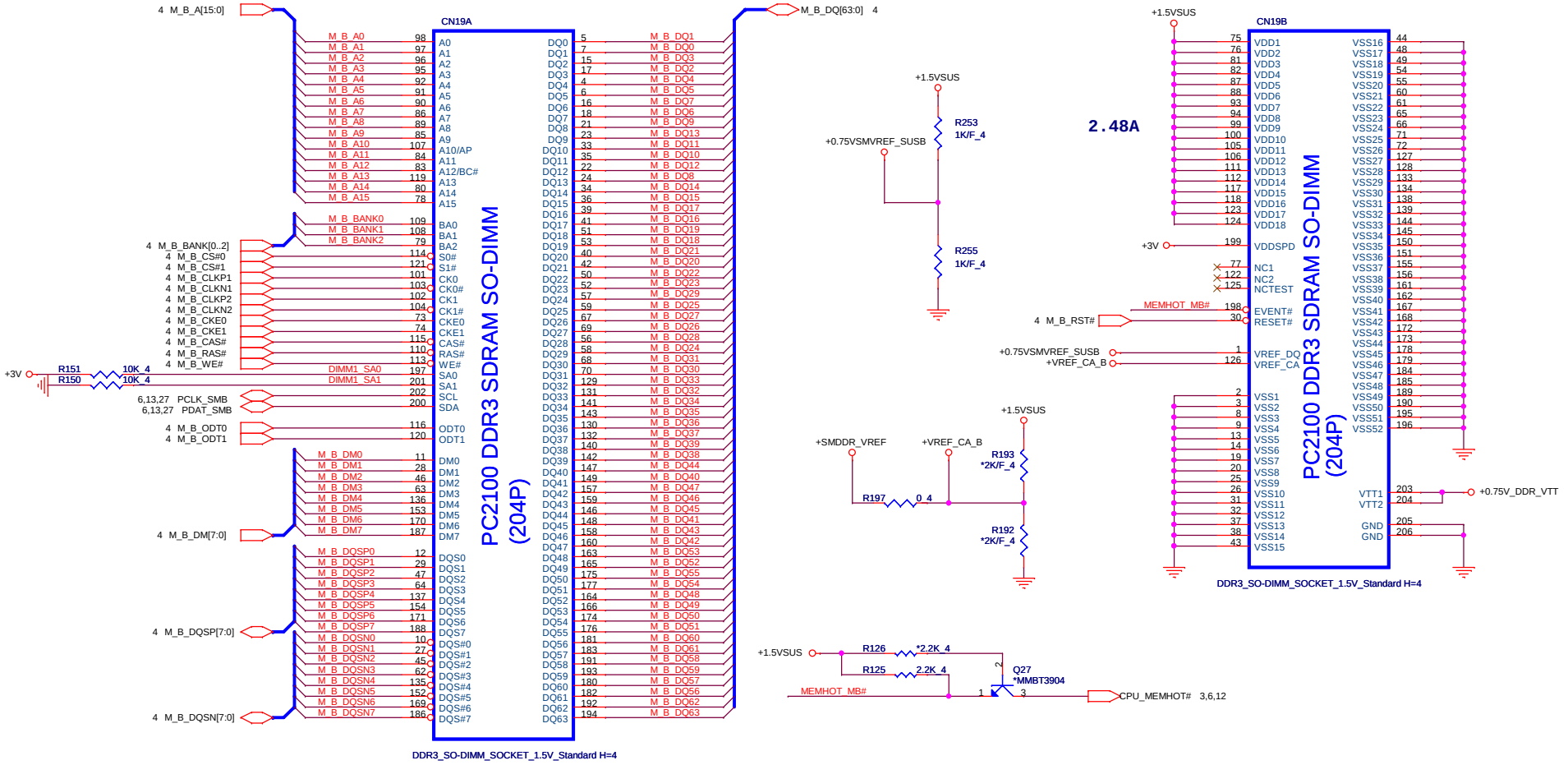
Size	Document Number	Rev
	S1G4 PWR & GND 3/3	1A
Date: Monday, March 29, 2010	Sheet 5 of 48	



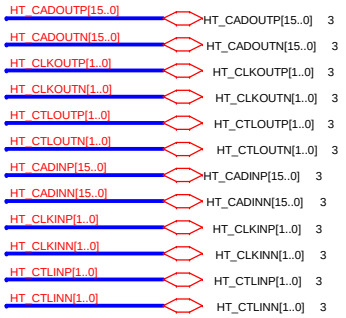
Place these Caps near So-Dimm0.



Quanta Computer Inc.		
PROJECT : ZRA		
Size	Document Number: DDR3 DIMMA-STD	Rev: 1A
Date: Monday, March 29, 2010	Sheet 6 of 48	



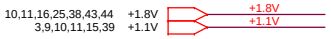
Quanta Computer Inc.		
PROJECT : ZRA		
Size	Document Number	Rev
	DDR3 DIMMB-STD	1A
Date: Monday, March 29, 2010	Sheet 7 of 48	

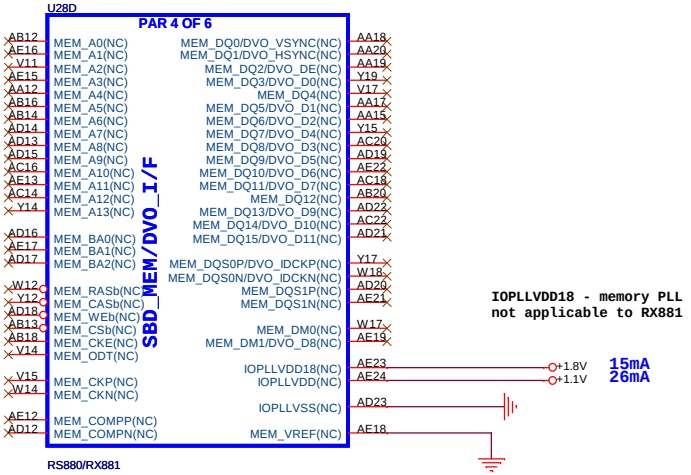


signals	RS880	RX880
HT_TXCALP	Ra 301 ohm 1%	Ra 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	Rb 301 ohm 1%	Rb 1.21k ohm 1%
HT_RXCALN		

RES CHIP 1.21K 1/16W +-1%(0402)
P/N : CS21212FB18

This block is for UMA only , Discrete can remove all component

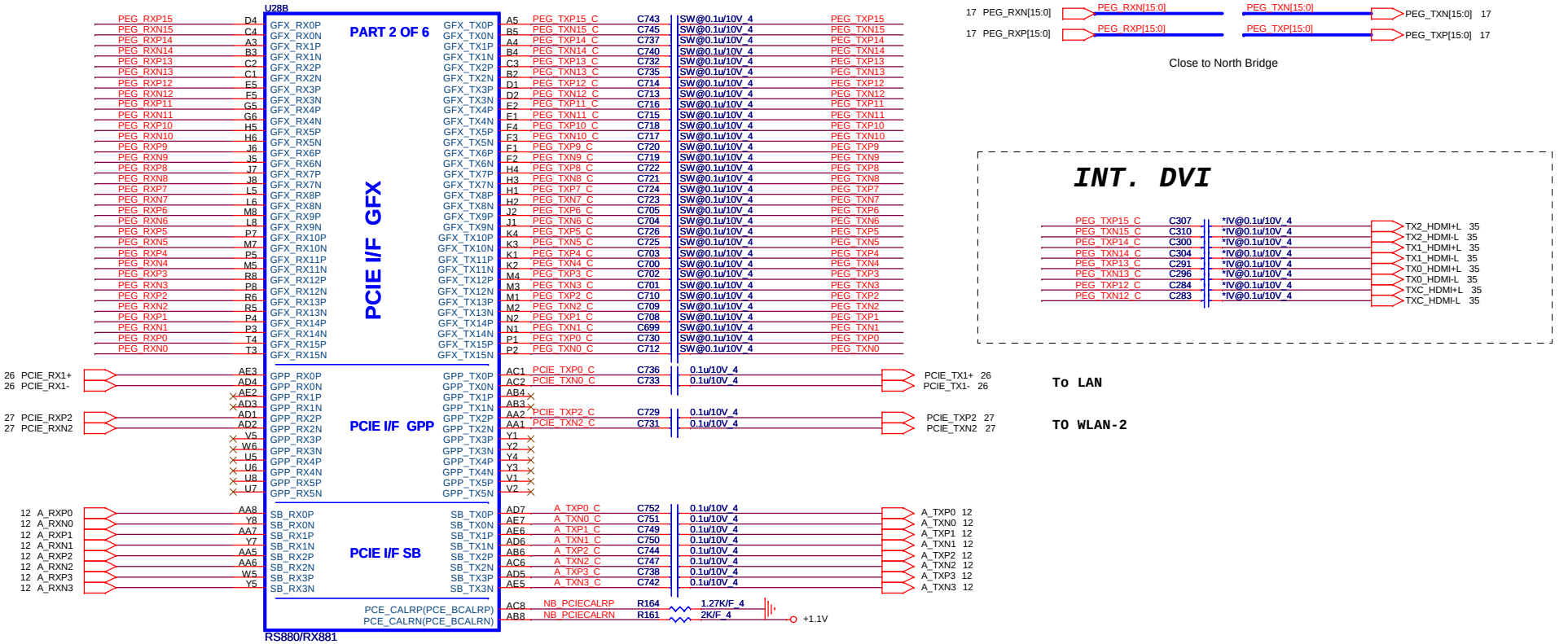




IOPLLVDD18 - memory PLL
not applicable to RX881

Quanta Computer Inc.
PROJECT : ZRA

Size	Document Number	Rev
	RS880M-HT LINK I/F 1/4	1A
Date: Monday, March 29, 2010	Sheet 8 of 48	



RS880 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

Quanta Computer Inc.
PROJECT : ZRA

Size	Document Number	Rev
	RS880M-PCIE I/F 2/4	1A
Date: Monday, March 29, 2010	Sheet 9 of 48	

All RS880 variants do not support analog TV-out functionality. As such, Y, C_Pr, and COMP_Pb

110mA
20mA
4mA

U28C — RS880/RX881 — PART 3 OF 6

CRT/TVOUT
PLL PWR
LVTM
PM
CLOCKs
MIS.

Only for UMA
VGA (Not applicable to RX881)

For Check list JTAG

For A11 version

B-TEST 0128

Reference clock input for the RS880M.

B-TEST 0128

15mA
300mA

STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.

RS880M
1 Disable
0 Enable

RS880M: Enables Side port memory

RS880M:INT_CRT_HSYNC

Selects if Memory SIDE PORT is available or not
1 = Memory Side port Not available
0 = Memory Side port available
Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]

For extrnal EEPROM Debug only

RS780/RX780/RS880

Display Port interface from PCIeGraphics (RS880/rs880M only)

RS880M --- ADD

AVDD-DAC Analog not applicable to RX780

PLLVDD - Graphics PLL not applicable to RX780

change R175 0ohm to bead(CX8PG221003) and C339 from 0.1uF to 2.2uF(CH52201K991), for monitor noise issue.

C-TEST 0322

AVDDI-DAC Digital not applicable to RX780

AVDDQ-DAC Bandgap Reference not applicable to RX780

PLLVDD18 - Graphics PLL not applicable to RX780

VDDLTP18 - LVDS or DVI/HDMI PLL not applicable to RX780

VDDLT18 - LVDS or DVI/HDMI digital not applicable to RX780

20mils width

VDDA18PCIEPLL -PCIE PLL

20mils width

VDDA18HTPLL -HT LINK PLL

DDR3 based CPU : Level shifted to 1.8 V on the Northbridge side using an open-drain buffer and pulled up to 1.8V_S0 through a 2.2k Ohm 5% resistor on the Northbridge side.

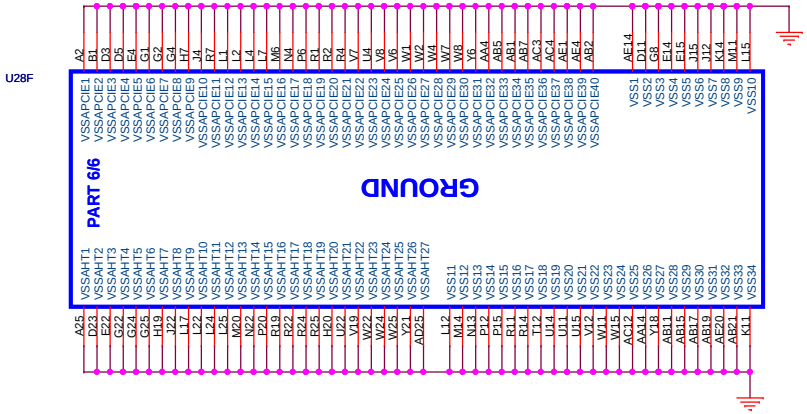
B-TEST 0225
2.2K => 300R , Accord with LDT riss time SPEC

The RS880 family does not support CLMC architecture
The LDTREQ# connection from the CPU to ALLOW_LDTSTOP of the Northbridge is no longer required.

Quanta Computer Inc.
PROJECT : ZRA

Size	Document Number	Rev
	RS880M-SYSTEM I/F 3/4	1A

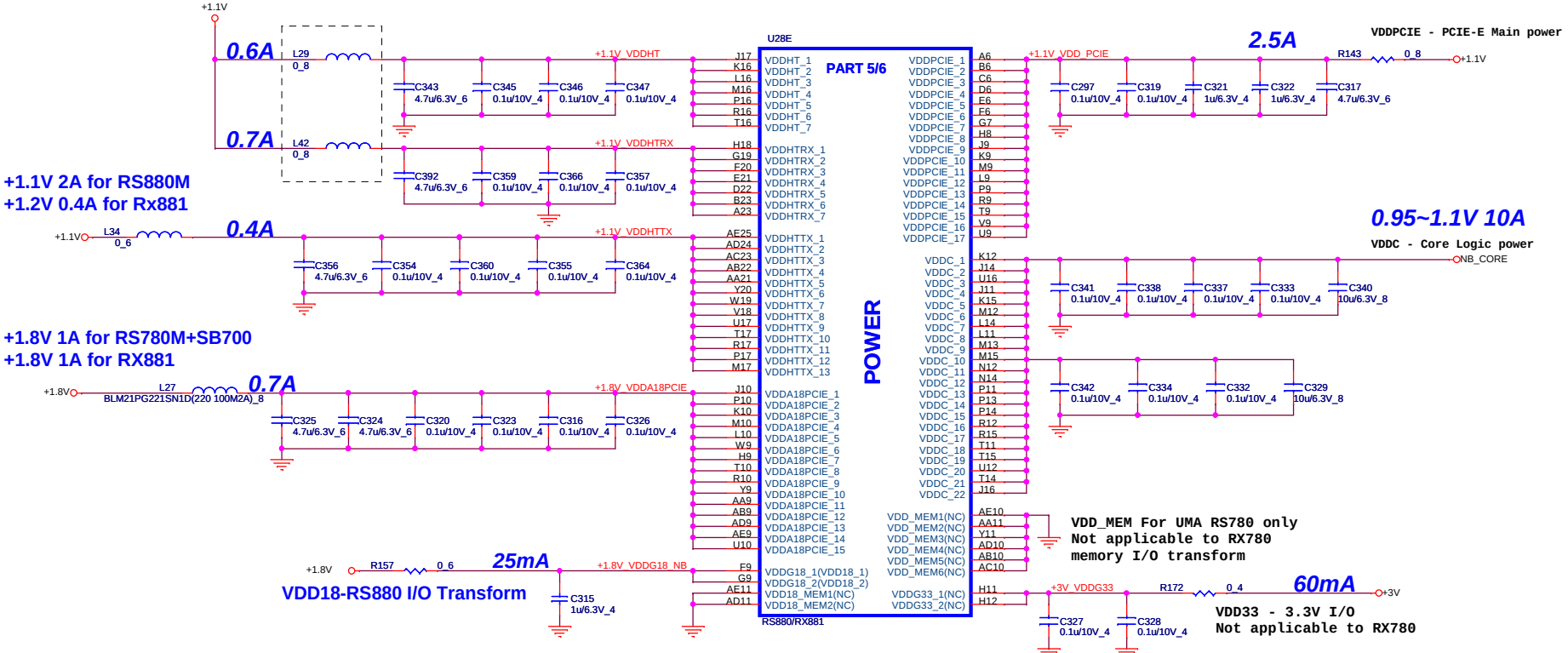
Date: Monday, March 29, 2010 Sheet 10 of 48



RX881/RS880 POWER DIFFERENCE TABLE

PIN NAME	RX881	RS880	PIN NAME	RX881	RS880
VDDHT	+1.1V	+1.1V	IOPLLVDD	+1.1V	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	GND	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	GND	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	GND	+1.8V
VDDG18	+1.8V	+1.8V	PLLVDD	GND	+1.1V
VDD18_MEM	GND	+1.8V	PLLVDD18	GND	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	GND	+1.8V/1.5V	VDDLTP18	GND	+1.8V
VDDG33	+3.3V	+3.3V	VDDLT18	GND	+1.8V
IOPLLVDD18	+1.8V	+1.8V	VDDLT33	NC	NC

+1.1V 2A for RS880M
+1.1V 1.3A for RX881

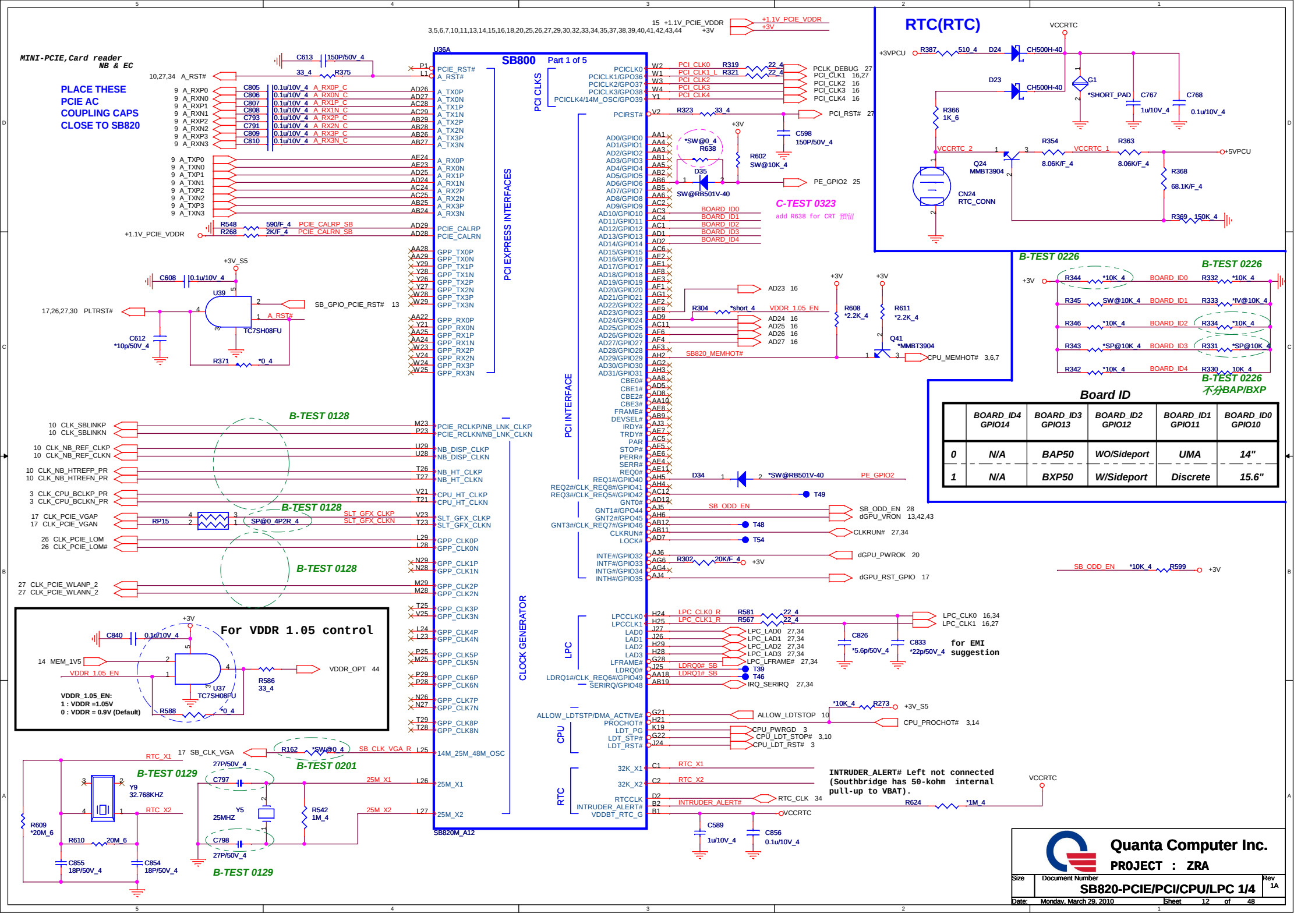


+1.1V
+1.8V
NB_CORE

+1.1V 3,8,9,10,15,39
+1.8V 8,10,16,25,38,43,44
NB_CORE 33,40

Quanta Computer Inc.
PROJECT : ZRA

Size	Document Number	Rev
	RS880M-POWER 4/4	1A
Date: Monday, March 29, 2010	Sheet 11 of 48	



	BOARD_ID4 GPIO14	BOARD_ID3 GPIO13	BOARD_ID2 GPIO12	BOARD_ID1 GPIO11	BOARD_ID0 GPIO10
0	N/A	BAP50	WO/Sideport	UMA	14"
1	N/A	BXP50	W/Sideport	Discrete	15.6"

Quanta Computer Inc.
PROJECT : ZRA

Size	Document Number	Rev
	SB820-PCIE/PCI/CPU/LPC 1/4	1A

Date: Monday, March 29, 2010 Sheet 12 of 48

NC only ,Can't be install

+3V_S5
R376 *2.2K_4 SB_TEST0
R373 *2.2K_4 SB_TEST1
R358 *2.2K_4 SB_TEST2

+3V
SCL0/SDATA0 is 3V tolerance
AMD datasheet define it
R276 2.2K_4 PCLK_SMB
R275 2.2K_4 PDAT_SMB
Clock gen/Robson/TV tuner /DDR2/DDR2 thermal/Accelerometer

+3V_S5
SCL2/SDATA2 is 3V/S5 tolerance
AMD datasheet define it
R278 2.2K_4 SB_SCLK2
R270 2.2K_4 SB_SDATA2

+3V
R329 4.7K_4 SUS_STAT#

B-TEST 0128
+3V
R289 SW@10K_4
dGPU_VRON 2ms
MXM_PWR_EN
20 MXM_PWREN
D13 SW@RB501V-40
MXM_PWR_EN 1 2
C564 SW@0.1u/10V_4
12,42,43 dGPU_VRON 1 2
D14 *SW@RB501V-40
>1mS delay is required between all MXM power rail stable and MXM_PWREN(enables the module internal power)

12,15,16,26,27,29,32,35,37 +3V_S5
3,5,6,7,10,11,12,14,15,16,18,20,25,26,27,29,30,32,33,34,35,37,38,39,40,41,42,43,44 +3V
+3V_S5
+3V

USBCLK/41M_25M_48M_OSC pin is CLK input
pin when EXT CLKGEN mode.
It is output CLK source when INT CLKGEN mode.

change R301 footprint from 0402 to 0603
P/N from CS00002JB38 to CX08T600102

C-TEST 0324
B-TEST 0223
CLK source change from exterior to SB

EMI
CLK_48M_USB
C-TEST 0324
del R300, stuff C581 for EMI
C581 10p/50V_4

U36D
SB800
Part 4 of 5

34 SUSB#
34 SUSC#
34 DNBSWON#
16,27 SB_PWRGD_IN
10 SUS_STAT#
SB_TEST0
SB_TEST1
SB_TEST2
34 SIO_A20GATE
34 SIO_RCIN#
LANLINK_STATE#
T99
34 SIO_EXT_SMI#
34 SIO_EXT_SCI#
R551 0_4
R378 0_4
SIO_EXT_SMI#_R
SIO_EXT_SCI#_R
T98
SYS_RST#
26 PCIE_WAKE#
PCIE_WAKE#
T59
IR_RX1
3 CPU_THERMTRIP#
16 NB_PWRGD_SB
34 ICH_RSMRST#

PCI_PME#/GEVENT4#
RI#/GEVENT22#
SPI_CS3#/GBE_STAT1/GEVENT21#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST0
TEST1/TMS
TEST2
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/GEVENT23#
GEVENT5#
SYS_RESET#/GEVENT19#
WAKE#/GEVENT8#
IR_RX1/GEVENT20#
THRMTRIP#/SMBALERT#/GEVENT2#
NB_PWRGD
RSMRST#

ACPI / WAKE UP EVENTS

12 SB_GPIO_PCIE_RST#
26 CLK_PCIE_LAN_REQ#
MXM_PWR_EN
T45
SB_GPIO59
29 SPKR
6,7,27 PCLK_SMB
6,7,27 PDAT_SMB
26 SB_SMBCLK1
26 SB_SMBDATA1
27 CLK_PCIE_2_REQ#
CRD_CLKREQ#
T47
18 SB_CLKREQG#
R272 *SW@0_4 CLKREQG#

CLK_REQ4#/SATA_IS0#/GPIO64
CLK_REQ3#/SATA_IS1#/GPIO63
SMARTVOLT1/SATA_IS2#/GPIO50
CLK_REQ0#/SATA_IS3#/GPIO60
SATA_IS4#/FANOUT3/GPIO55
SATA_IS5#/FANIN3/GPIO59
SPKR/GPIO66
SCL0/GPIO43
SDA0/GPIO47
SCL1/GPIO227
SDA1/GPIO228
CLK_REQ2#/FANIN4/GPIO62
CLK_REQ1#/FANOUT4/GPIO61
IR_LED#/LB#/GPIO184
SMARTVOLT2/SHUTDOWN#/GPIO51
DDR3_RST#/GEVENT7#
GBE_LED0/GPIO183
GBE_LED1/GEVENT9#
GBE_LED2/GEVENT10#
GBE_STAT0/GEVENT11#
CLK_REQG#/GPIO65/OSCIN

GPIO

31 OC_7#
31 OC_6#
5 PM_THERM#
31 OC_4#
R377 0_4
R315 0_4
SB_JTAG_TDO
SB_JTAG_TCK
SB_JTAG_TDI
SB_JTAG_RST#

BLINK/USB_OC7#/GEVENT18#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GEVENT17#
USB_OC4#/IR_RX0/GEVENT16#
USB_OC3#/AC_PRES/TDO/GEVENT15#
USB_OC2#/TCK/GEVENT14#
USB_OC1#/TDI/GEVENT13#
USB_OC0#/TRST#/GEVENT12#

USB OC

HD audio interface is +3VS5 voltage

16 ACZ_SDOUT
R622 *10K_4 ACZ_BCLK
ACZ_SDOUT
R328 *10K_4 ACZ_SDIN0
R327 *10K_4 ACZ_SDIN1
R630 *10K_4 ACZ_SDIN2
R317 *10K_4 ACZ_SDIN3
ACZ_SYNC
ACZ_RST#

AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO167
AZ_SDIN1/GPIO168
AZ_SDIN2/GPIO169
AZ_SDIN3/GPIO170
AZ_SYNC
AZ_RST#

HD AUDIO

+3V_S5
R619 10K_4 GBE_COL
R314 10K_4 GBE_CRS
R614 10K_4 GBE_MDIO
ZR8
R350 10K_4 GBE_RXERR
R351 10K_4 GBE_PHY_INTR

GBE_COL
GBE_CRS
GBE_MDCK
GBE_MDIO
GBE_RXCLK
GBE_RXD3
GBE_RXD2
GBE_RXD1
GBE_RXD0
GBE_RXCTL/RXDV
GBE_RXERR
GBE_TXCLK
GBE_TXD3
GBE_TXD2
GBE_TXD1
GBE_TXD0
GBE_TXCTL/TXEN
GBE_PHY_PD
GBE_PHY_RST#
GBE_PHY_INTR

GBE LAN

T40
ADP_PRES0

PS2_DAT/SDA4/GPIO187
PS2_CLK/SCL4/GPIO188
SPI_CS2#/GBE_STAT2/GPIO166
FC_RST#/GPO160
PS2KB_DAT/GPIO189
PS2KB_CLK/GPIO190
PS2M_DAT/GPIO191
PS2M_CLK/GPIO192

EMBEDDED CTRL

SB820M_A12

USBCLK/14M_25M_48M_OSC
USB_RCOMP
A10 CLK_48M_USB
R301 SBK160808T-600Y-N_6
CR_CLK 30
G19 USB_RCOMP_SB
R283 11.8K/F_6

USB 1.1 USB MISC

USB_FSD1P/GPIO186
USB_FSD1N
USB_FSD0P/GPIO185
USB_FSD0N
USB_FDS12P
USB_FSD12N
T51
T53

USB 2.0

USB_HSD13P
USB_HSD13N
USB_HSD12P
USB_HSD12N
USB_HSD11P
USB_HSD11N
USB_HSD10P
USB_HSD10N
USB_HSD9P
USB_HSD9N
USB_HSD8P
USB_HSD8N
USB_HSD7P
USB_HSD7N
USB_HSD6P
USB_HSD6N
USB_HSD5P
USB_HSD5N
USB_HSD4P
USB_HSD4N
USB_HSD3P
USB_HSD3N
USB_HSD2P
USB_HSD2N
USB_HSD1P
USB_HSD1N
USB_HSD0P
USB_HSD0N

USBP5+ 30
USBP5- 30
USBP12+ 31
USBP12- 31
USBP11+ 31
USBP11- 31
USBP10+ 31
USBP10- 31
USBP9+ 32
USBP9- 32
USBP8+ 25
USBP8- 25
USBP7+ 31
USBP7- 31
USBP4+ 27
USBP4- 27
USBP1+ 35
USBP1- 35
USBP0+ 31
USBP0- 31

USB card reader
USB board
USB board
USB board
BLUETOOTH
USB CAMERA
Finger Print
WLAN MINI CARD
DOCKING
On board USB connect
Only USB Port0 can be configured as debug port.

SCL2/GPIO193
SDA2/GPIO194
SCL3_LV/GPIO195
SDA3_LV/GPIO196
EC_PWM0/EC_TIMER0/GPIO197
EC_PWM1/EC_TIMER1/GPIO198
EC_PWM2/EC_TIMER2/GPIO199
EC_PWM3/EC_TIMER3/GPIO200
SB_SCLK2
SB_SDATA2
SB_GPIO195
SB_GPIO196
GPIO199 16
GPIO200 16

KSI_0/GPIO201
KSI_1/GPIO202
KSI_2/GPIO203
KSI_3/GPIO204
KSI_4/GPIO205
KSI_5/GPIO206
KSI_6/GPIO207
KSI_7/GPIO208
KSO_0/GPIO209
KSO_1/GPIO210
KSO_2/GPIO211
KSO_3/GPIO212
KSO_4/GPIO213
KSO_5/GPIO214
KSO_6/GPIO215
KSO_7/GPIO216
KSO_8/GPIO217
KSO_9/GPIO218
KSO_10/GPIO219
KSO_11/GPIO220
KSO_12/GPIO221
KSO_13/GPIO222
KSO_14/GPIO223
KSO_15/GPIO224
KSO_16/GPIO225
KSO_17/GPIO226

EMBEDDED CTRL

Check list
SB_GPIO195 R563 10K_4
SB_GPIO196 R549 10K_4

Azalia to AUDIO and MDC
ADD C873 C874 C875,L43 for EMI
C-TEST 0324

ACZ_SDOUT
C875 *10p/50V_4
R341 33_4 ACZ_SDOUT_MDC 29
R629 33_4 ACZ_SDOUT_AUDIO 29
C611 *10p/50V_4
C874 *10p/50V_4
ACZ_SYNC
R631 33_4 ACZ_SYNC_MDC 29
R618 33_4 ACZ_SYNC_AUDIO 29
C857 *10p/50V_4
BLM15AG121SS1_4 L43
C873 *10p/50V_4
ACZ_BCLK
R627 33_4 ACZ_BITCLK_MDC 29
R628 33_4 ACZ_BITCLK_AUDIO 29
C614 *10p/50V_4
ACZ_RST#
R621 33_4 ACZ_RST#_MDC 29
R620 33_4 ACZ_RST#_AUDIO 29
ACZ_SDIN0 ACZ_SDIN0 29 AUDIO CODE
ACZ_SDIN1 ACZ_SDIN1 29 MDC
If the VDDIO_AZ_S power rail is configured for 1.5V_S5 then AZ_SDIN[3:0] can not be connected to 3.3-V devices.

CN12
+3V_S5
C615 *10p/50V_4
SB_JTAG_TCK
SB_JTAG_TDO
SB_JTAG_TDI
SB_TEST1
SB_JTAG_RST#
*S/W_JTAG_DEBUG
SB JTAG

Quanta Computer Inc.
PROJECT : ZRA
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Document Number
SB820-ACPI/GPIO/USB 2/4
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SATA PORT 0,1,2,3
can support AHCI
mode

SATA HDD

SATA ODD

U36B

SB800
Part 2 of 5

28 SATA_TX0+ — C850 0.01u/16V_4 — SATA_TX0+_C — AH9 SATA_TX0P
28 SATA_TX0- — C849 0.01u/16V_4 — SATA_TX0-_C — AJ9 SATA_TX0N
28 SATA_RX0- — AJ8 SATA_RX0N
28 SATA_RX0+ — AH8 SATA_RX0P
28 SATA_TX1+ — C848 0.01u/16V_4 — SATA_TX1+_C — AH10 SATA_TX1P
28 SATA_TX1- — C847 0.01u/16V_4 — SATA_TX1-_C — AJ10 SATA_TX1N
28 SATA_RX1- — AG10 SATA_RX1N
28 SATA_RX1+ — AF10 SATA_RX1P
AG12 SATA_TX2P
AF12 SATA_TX2N
AJ12 SATA_RX2N
AH12 SATA_RX2P
AH14 SATA_TX3P
AJ14 SATA_TX3N
AG14 SATA_RX3N
AF14 SATA_RX3P
AG17 SATA_TX4P
AF17 SATA_TX4N
AJ17 SATA_RX4N
AH17 SATA_RX4P
AJ18 SATA_TX5P
AH18 SATA_TX5N
AH19 SATA_RX5N
AJ19 SATA_RX5P

SERIAL ATA

+1.1V_AVDD_SATA
R295 1K/F_4 — SATA_CALRP — AB14 SATA_CALRP
R290 931/F_4 — SATA_CALRN — AA14 SATA_CALRN

32 SATA_ACT# — AD11 SATA_ACT#/GPIO67

PLACE SATA_CAL
RES VERY CLOSE
TO BALL OF SB820

*22P/50V_4 — C845 — SATA_X1 — AD16 SATA_X1
Y7 *25MHZ
R587 *1M_4
C841 — SATA_X2 — AC16 SATA_X2
*22P/50V_4

T56 SB_GPIO164 — J5 SPI_DI/GPIO164
T61 SB_GPIO163 — E2 SPI_DO/GPIO163
T58 SB_GPIO162 — K4 SPI_CLK/GPIO162
T50 SB_GPIO165 — K9 SPI_CS1#/GPIO165
T60 SB_GPIO161 — G2 ROM_RST#/GPIO161

SPI ROM

NC1 G27
NC2 Y2

FC_CLK AH28 T80
FC_FBCLKOUT AG28 T78
FC_FBCLKIN AF26 T86
FC_OE#/GPIOD145 AF28 T77
FC_AVD#/GPIOD146 AG29 T76
FC_WE#/GPIOD148 AG26 T87
FC_CE1#/GPIOD149 AF27 T81
FC_CE2#/GPIOD150 AF29 T74
FC_INT1/GPIOD144 AF29 T75
FC_INT2/GPIOD147 AH27 T83
FC_ADQ0/GPIOD128 AJ27 T82
FC_ADQ1/GPIOD129 AJ26 T37
FC_ADQ2/GPIOD130 AH25 T85
FC_ADQ3/GPIOD131 AH24 T91
FC_ADQ4/GPIOD132 AG23 T90
FC_ADQ5/GPIOD133 AH23 T93
FC_ADQ6/GPIOD134 AJ22 T95
FC_ADQ7/GPIOD135 AG21 T96
FC_ADQ8/GPIOD136 AF21 T97
FC_ADQ9/GPIOD137 AH22 T94
FC_ADQ10/GPIOD138 AJ23 T89
FC_ADQ11/GPIOD139 AF23 T42
FC_ADQ12/GPIOD140 AJ24 T92
FC_ADQ13/GPIOD141 AJ25 T88
FC_ADQ14/GPIOD142 AG25 T84
FC_ADQ15/GPIOD143 AH26 T79

FLASH

IF THERE IS NO IDE, TEST
POINTS FOR DEBUG BUS
IS MANDATORY

FANOUT0/GPIO52 W5
FANOUT1/GPIO53 W6
FANOUT2/GPIO54 Y9 SB_PROCHOT#_C
FANIN0/GPIO56 W7 WWAN_DET# T55
FANIN1/GPIO57 V9 CPPE_NC1# T52
FANIN2/GPIO58 W8 CRD_REQ1# T57
TEMPIN0/GPIO171 B6 TEMPIN0
TEMPIN1/GPIO172 A6 TEMPIN1
TEMPIN2/GPIO173 A5 MB_THRMDA_SB
TEMPIN3/TALERT#/GPIO174 B5 SB_GPIO174
TEMP_COMM C7 TEMP_COMM
VIN0/GPIO175 A3 SB_GPIO175
VIN1/GPIO176 B4 SB_GPIO176
VIN2/GPIO177 A4 SIDE_PORT_ID0
VIN3/GPIO178 C5 SIDE_PORT_ID1
VIN4/GPIO179 A7 MEM_1V5 12
VIN5/GPIO180 B7 SB_GPIO180
VIN6/GBE_STAT3/GPIO181 B8 SB_GPIO181
VIN7/GBE_LED3/GPIO182 A8 SB_GPIO182

HW MONITOR

SB820M_A12

15 +1.1V_AVDD_SATA — +1.1V_AVDD_SATA
12,13,15,16,26,27,29,32,35,37 +3V_S5 — +3V_S5

+3V
R316 *10K_4
R306 *10K_4
Q23 *MMBT3904
3,12 CPU_PROCHOT#
SB_PROCHOT#_C

Check list

TEMPIN0	R597	10K_4
TEMPIN1	R598	10K_4
MB_THRMDA_SB	R601	10K_4
SB_GPIO174	R600	10K_4
SB_GPIO175	R606	10K_4
SB_GPIO176	R605	10K_4
SIDE_PORT_ID0	R603	10K_4
SIDE_PORT_ID1	R604	10K_4
SB_GPIO180	R596	10K_4
SB_GPIO181	R594	*10K_4
SB_GPIO182	R592	10K_4

Quanta Computer Inc.
PROJECT : ZRA

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	SB820-SATA/IDE/HWM/SPI 3/4	1A

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PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.

VDDQ--3.3V I/O power

VDD-- S/B CORE power

U36C

SB800

Part 3 of 5

POWER

SB820M_A12

SB820 without GBE: Connected to GND plane.

U36E

SB800

GROUND

Part 5 of 5

SB820M_A12

If the VDDIO_AZ_S power rail is configured for 1.5V_S5 then AZ_SDIN[3:0] can not be connected to 3.3-V devices.

B-TEST 0202

For support USB wakeup-->3V_S5

3,5,6,7,10,11,12,13,14,16,18,20,25,26,27,29,30,32,33,34,35,37,38,39,40,41,42,43,44	+3V
3,8,9,10,11,39	+1.1V
12,13,16,26,27,29,32,35,37	+3V_S5
39	+1.1V_S5

Quanta Computer Inc.

PROJECT : ZRA

Size	Document Number	Rev
	SB820-PWR/DECOUPLING 4/4	1A
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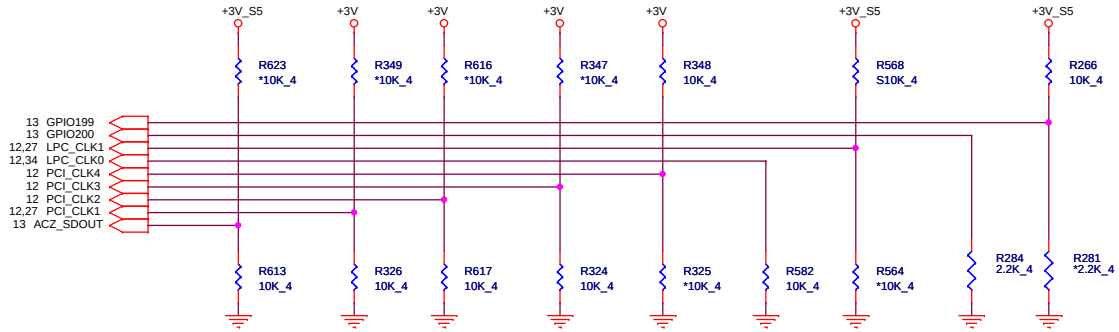
REQUIRED STRAPS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

SB820M is supported Gen1 mode only.

For internal clock GEN.



	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200 GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2	Watchdog Timer Enable	USE DEBUG STRAPS	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	INT. CLKGEN ENABLED DEFAULT	H, H=Reserved H, L=SPI ROM
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1 DEFAULT	Watchdog Timer Disable DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK MODE	EC DISABLED DEFAULT	EXT. CLKGEN ENABLE	L,H=LPC ROM DEFAULT L, L=FWH ROM

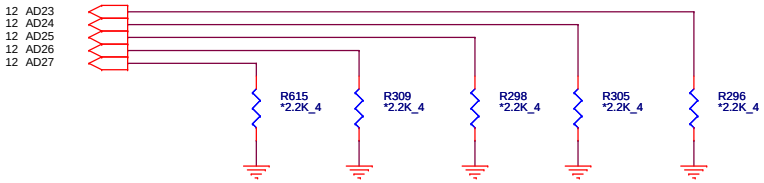
internal have pull Hi 10K

12,13,15,26,27,29,32,35,37 +3V_S5
8,10,11,25,38,43,44 +1.8V

+3V_S5
+1.8V

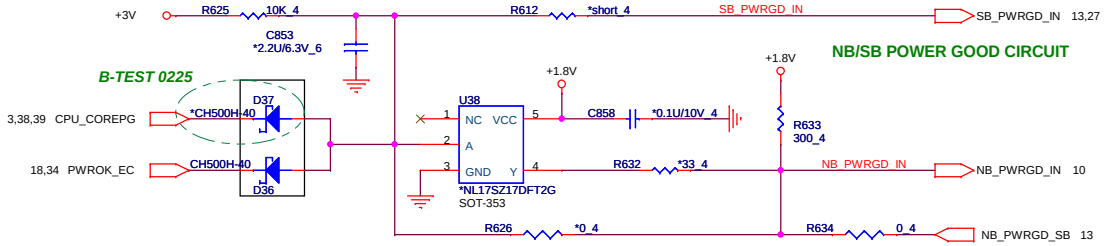
DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	DISABLE I2C ROM DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	ENABLE I2C ROM use REQ3# as SDA use GNT3# as SCL	ENABLE PCI MEM BOOT

NB_PWRGD_IN:
RS880/RX881 = 1.8V;
Do NOT share it with SB_PWRGD when use Internal Clk Gen (Need SB PLL initialize firstly)



AL17SZ17000	IC(5P) NL17SZ17DFT2G(SOT-353)	SOT-353
ALUC1G17000	IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5)	SOT23-5

Quanta Computer Inc.
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	SB820-STRAPS,PWRGD	1A
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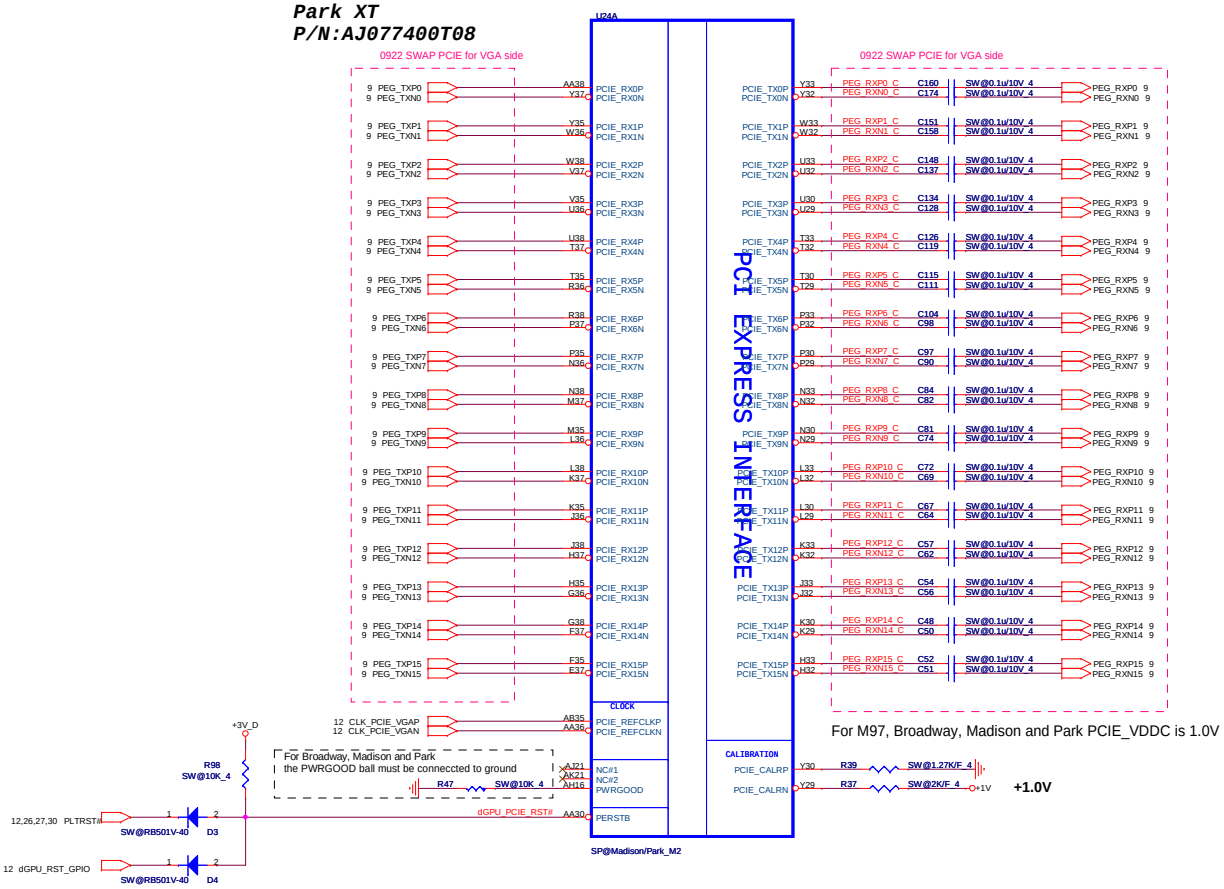
Park XT
P/N:AJ077400T08

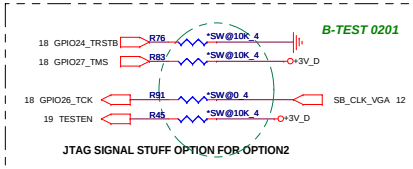


For M97, Broadway, Madison and Park PCIE_VDDC is 1.0V

+3V_D
+1V

+3V_D 18,20,22,25,35
+1V 18,20,21,44

B-TEST 0201



JTAG SIGNAL STUFF OPTION FOR OPTION2

SIGNALS	NORMAL MODE	JTAG MODE (DEBUG)
GPIO24_TRSTB	"0" (PD)	"1" (PU)
GPIO27_TMS	"1" (PU)	"1" (PU)
GPIO26_TCK	CLK	"1" (PU)
TESTEN	"1" (PU)	"1" (PU)

Quanta Computer Inc.
PROJECT : ZRA

Size	Document Number	Rev
	Madison/Broadway-PCIE I/F	1A

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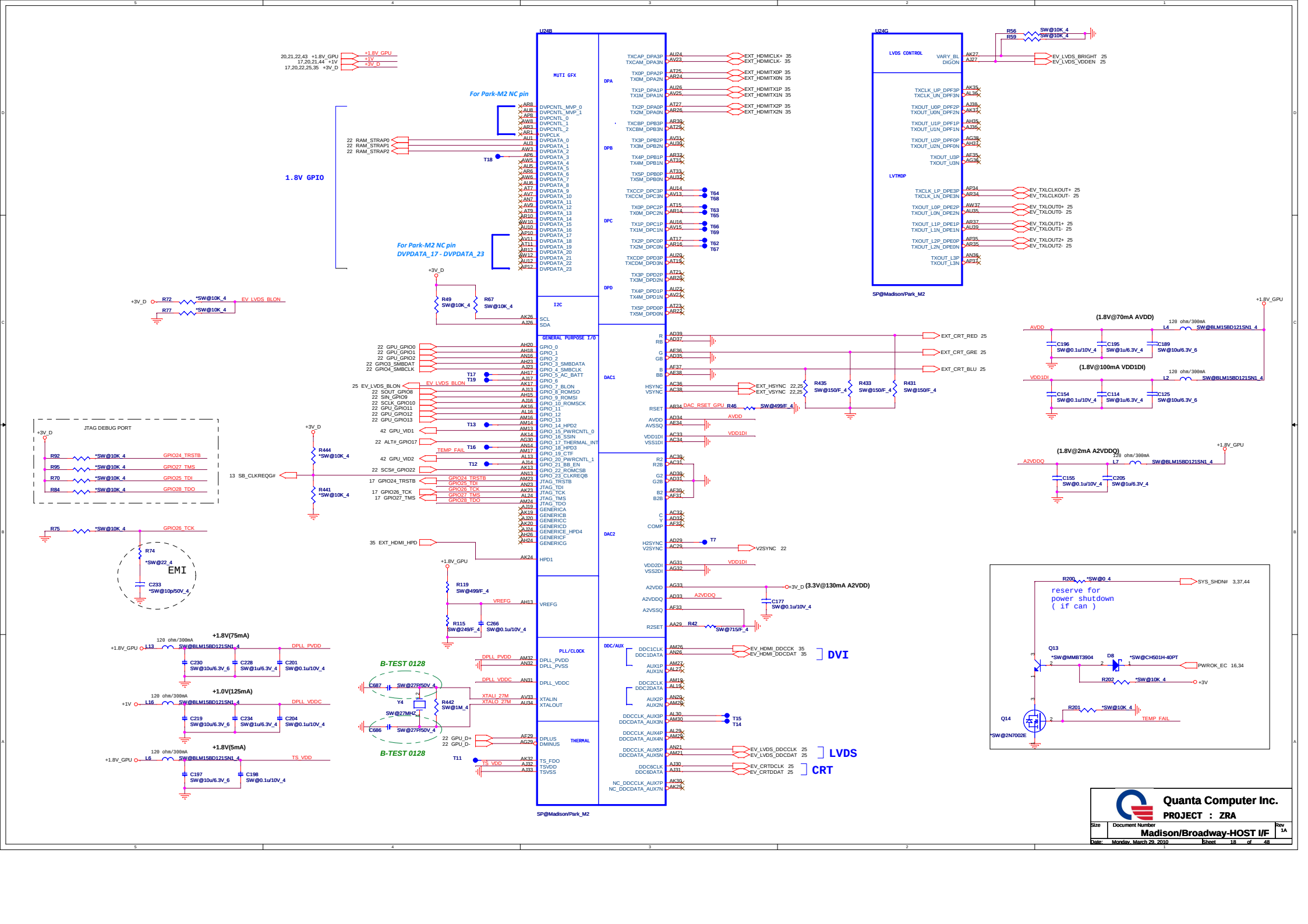
U24B
MUTI GFX
DPA
DPB
DPC
DPD
I2C
GENERAL PURPOSE I/O
DAC1
DAC2
PLL/CLOCK
THERMAL
DDC/AUX
SP@Madison/Park_M2
U24G
LVDS CONTROL
LVTMDP
SP@Madison/Park_M2
1.8V GPIO
For Park-M2 NC pin
For Park-M2 NC pin
DVPDATA_17 - DVPDATA_23
JTAG DEBUG PORT
EMI
B-TEST 0128
B-TEST 0128
+1.8V(75mA)
+1.0V(125mA)
+1.8V(5mA)
(1.8V@70mA AVDD)
(1.8V@100mA VDD1DI)
(1.8V@2mA A2VDDQ)
(3.3V@130mA A2VDD)
DVI
LVDS
CRT
reserve for
power shutdown
(if can)
Quanta Computer Inc.
PROJECT : ZRA
Madison/Broadway-HOST I/F
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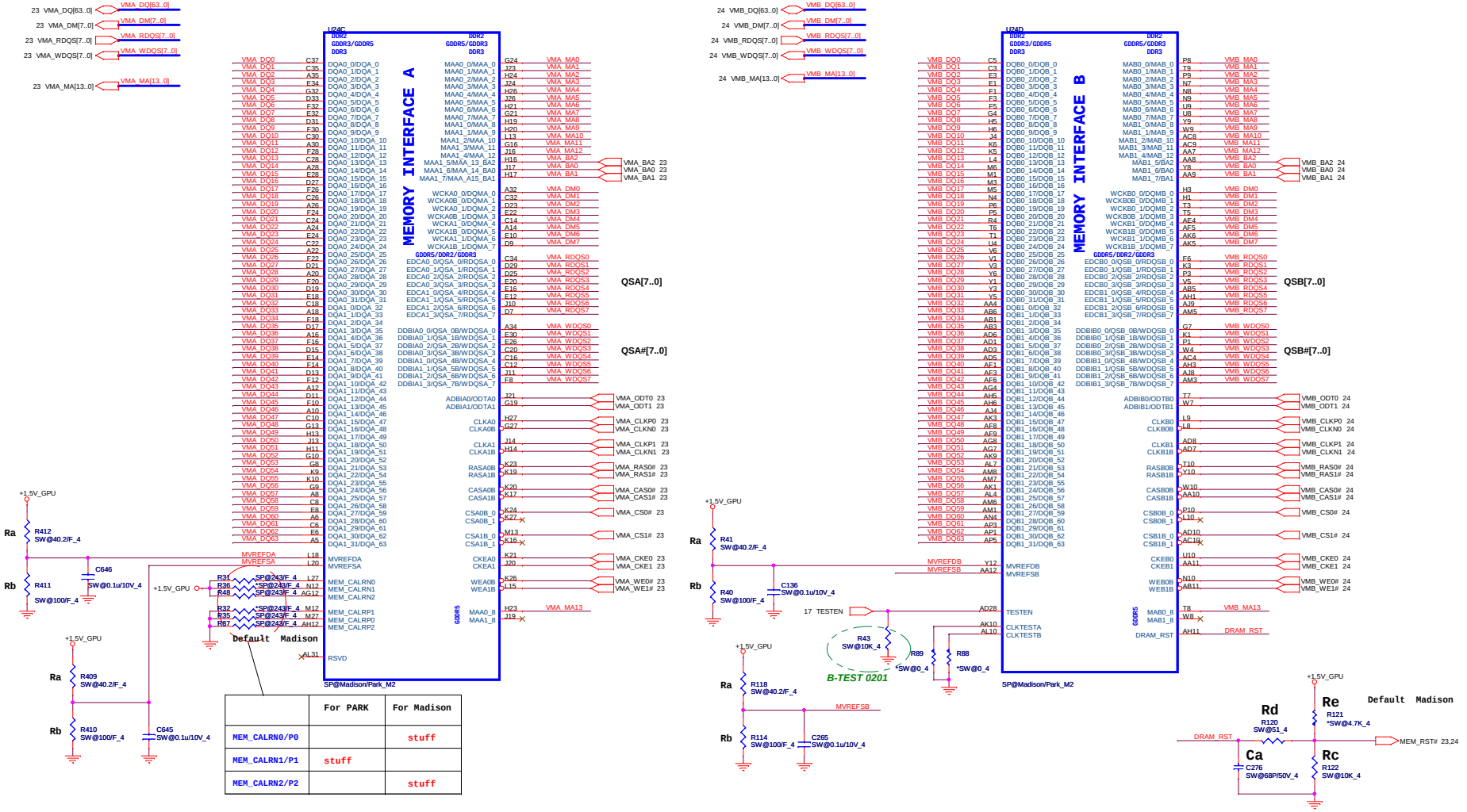

	For PARK	For Madison
MEM_CALRN0/P0		stuff
MEM_CALRN1/P1	stuff	
MEM_CALRN2/P2		stuff

DDR3/GDDR3 Memory Stuff Option

	GDDR5	GDDR3	DDR3(Default)
+1.5V_VGA	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

For SSTL-1.8/SSTL-2/DDR1/GDDR1: 0.5 * VDDR1.
For DDR3/GDDR3/GDDR4/GDDR5: 0.7 * VDDR1.

Designator	For M97-M2	For Mannhatton
Rc	10K	10K
Rd	0R/Short	51R
Re	DNI	DNI
Ca	2.2nF	68pF

Quanta Computer Inc.
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+1.5V_GPU
+1.8V_GPU
+1V
+VGPU_CORE
+VGPU_CORE
+3V

+1.5V_GPU 19,23,24,43
+1.8V_GPU 18,21,22,43
+1V 17,18,21,44
+VGPU_CORE 42
+VGPU_CORE 42
+3V 3,5,6,7,10,11,12,13,14,15,16,18,25,26,27,29,30,32,33,34,35,37,38,39,40,41,42,43,44

For DDR3, MVDDQ = 1.5V (7.5A)

+1.5V_GPU

C659 SW@10u/6.3V_6 C80 SW@10u/6.3V_6 C658 SW@10u/6.3V_6 C662 SW@10u/6.3V_6 C660 SW@10u/6.3V_6

C70 SW@10u/6.3V_4 C63 SW@10u/6.3V_4 C76 SW@10u/6.3V_4 C183 SW@10u/6.3V_4 C176 SW@10u/6.3V_4 C71 SW@10u/6.3V_4

C68 SW@10u/6.3V_4 C167 SW@10u/6.3V_4 C169 SW@10u/6.3V_4 C38 SW@10u/6.3V_4 C78 SW@10u/6.3V_4 C77 SW@10u/6.3V_4

C156 SW@10u/6.3V_4 C65 SW@0.1u/10V_4 C37 SW@0.1u/10V_4 C95 SW@0.1u/10V_4 C61 SW@0.1u/10V_4

U24E

MEM I/O

VDDR1#1 AC7
VDDR1#2 AD11
VDDR1#3 AE7
VDDR1#4 AG10
VDDR1#5 AJ7
VDDR1#6 AK8
VDDR1#7 AL9
VDDR1#8 G11
VDDR1#9 G14
VDDR1#10 G17
VDDR1#11 G20
VDDR1#12 G23
VDDR1#13 G26
VDDR1#14 G29
VDDR1#15 H10
VDDR1#16 J7
VDDR1#17 J9
VDDR1#18 K11
VDDR1#19 K13
VDDR1#20 K8
VDDR1#21 L12
VDDR1#22 L16
VDDR1#23 L21
VDDR1#24 L23
VDDR1#25 L26
VDDR1#26 L7
VDDR1#27 M11
VDDR1#28 N11
VDDR1#29 P7
VDDR1#30 R11
VDDR1#31 U11
VDDR1#32 U7
VDDR1#33 Y11
VDDR1#34 Y7

LEVEL TRANSLATION

VDD_CT#1 AF26
VDD_CT#2 AF27
VDD_CT#3 AG26
VDD_CT#4 AG27

I/O

VDDR3#1 AF23
VDDR3#2 AF24
VDDR3#3 AG23
VDDR3#4 AG24

VDDR4#4 AF13
VDDR4#5 AF15
VDDR4#7 AG13
VDDR4#8 AG15

VDDR4#1 AD12
VDDR4#2 AF11
VDDR4#3 AF12
VDDR4#6 AG11

NC_VDDRHA T4
NC_VSSRHA T3
NC_VDDRHB T6
NC_VSSRHB T5

PLL

PCIE_PVDD AB37
MPV18#1 H7
MPV18#2 H8
SPV18 AM10
SPV10 AN9
SPVSS AN10

VOLTAGE SENESE

FB_VDDC T9 AF28
FB_VDDCI T8 AG28
FB_GND T10 AH29

PCIE

PCIE_VDDR#1 AA31
PCIE_VDDR#2 AA32
PCIE_VDDR#3 AA33
PCIE_VDDR#4 AA34
PCIE_VDDR#5 V28
PCIE_VDDR#6 W29
PCIE_VDDR#7 W30
PCIE_VDDR#8 Y31

PCIE_VDDC#1 G30
PCIE_VDDC#2 G31
PCIE_VDDC#3 H29
PCIE_VDDC#4 H30
PCIE_VDDC#5 J29
PCIE_VDDC#6 J30
PCIE_VDDC#7 L28
PCIE_VDDC#8 M28
PCIE_VDDC#9 N28
PCIE_VDDC#10 R28
PCIE_VDDC#11 T28
PCIE_VDDC#12 U28

CORE

VDDC#1 AA15
VDDC#2 AA17
VDDC#3 AA20
VDDC#4 AA22
VDDC#5 AA24
VDDC#6 AA27
VDDC#7 AB16
VDDC#8 AB18
VDDC#9 AB21
VDDC#10 AB23
VDDC#11 AB26
VDDC#12 AB28
VDDC#13 AC17
VDDC#14 AC20
VDDC#15 AC22
VDDC#16 AC24
VDDC#17 AC27
VDDC#18 AD18
VDDC#19 AD21
VDDC#20 AD23
VDDC#21 AD26
VDDC#22 AF17
VDDC#23 AF20
VDDC#24 AF22
VDDC#25 AG16
VDDC#26 AG18
VDDC#27 AG21
VDDC#28 AH22
VDDC#29 AH27
VDDC#30 AH28
VDDC#31 M26
VDDC#32 N27
VDDC#33 N24
VDDC#34 R18
VDDC#35 R21
VDDC#36 R23
VDDC#37 R26
VDDC#38 T17
VDDC#39 T20
VDDC#40 T22
VDDC#41 T24
VDDC#42 T27
VDDC#43 U16
VDDC#44 U18
VDDC#45 U21
VDDC#46 U23
VDDC#47 U26
VDDC#48 V17
VDDC#49 V20
VDDC#50 V22
VDDC#51 V24
VDDC#52 V27
VDDC#53 Y16
VDDC#54 Y18
VDDC#55 Y21
VDDC#56 Y23
VDDC#57 Y26
VDDC#58 Y28

ISOLATED CORE I/O

VDDC#1 AA13
VDDC#2 AB13
VDDC#3 AC12
VDDC#4 AC15
VDDC#5 AD13
VDDC#6 AD16
VDDC#7 M15
VDDC#8 M16
VDDC#9 M18
VDDC#10 M23
VDDC#11 N13
VDDC#12 N15
VDDC#13 N17
VDDC#14 N20
VDDC#15 N22
VDDC#16 R12
VDDC#17 R13
VDDC#18 R16
VDDC#19 T12
VDDC#20 T15
VDDC#21 V15
VDDC#22 Y13

POWER

SP@Madison/Park_M2

+1.8V_GPU

(1.8V@110mA VDD_CT)

120 ohm/300mA L74 SW@BLM15BD121SN1_4

VDDC_CT

C698 SW@10u/6.3V_6 C184 SW@1u/6.3V_4 C173 SW@0.1u/10V_4

(3.3V@60mA))

+3V_D

C235 SW@10u/6.3V_6 C182 SW@1u/6.3V_4 C212 SW@1u/6.3V_4 C255 SW@1u/6.3V_4

+1.8V_GPU

120 ohm/300mA L23 SW@BLM15BD121SN1_4

VDDR4

C274 SW@1u/6.3V_4 C273 SW@0.1u/10V_4

(1.8V@40mA PCIE_PVDD)

+1.8V_GPU

120 ohm/300mA L69 SW@BLM15BD121SN1_4

PCIE_PVDD

C676 SW@10u/6.3V_6 C675 SW@1u/6.3V_4 C673 SW@0.1u/10V_4

(1.8V@150mA MPV18)

+1.8V_GPU

120 ohm/300mA L1 SW@BLM15BD121SN1_4

MPV18

C58 SW@10u/6.3V_6 C66 SW@1u/6.3V_4 C60 SW@0.1u/10V_4

(1.8V@75mA SPV18)

+1.8V_GPU

120 ohm/300mA L19 SW@BLM15BD121SN1_4

SPV18

C261 SW@10u/6.3V_6 C249 SW@0.1u/10V_4

(1.0V@120mA SPV10)

+1V

120 ohm/300mA L20 SW@BLM15BD121SN1_4

SPV10

C262 SW@10u/6.3V_6 C250 SW@0.1u/10V_4

+1.8V_GPU

180 ohm/1.5A L3 SW@HCB1608KF-181T15_6

PCIE_VDDR

(1.8V@400mA PCIE_VDDR)

C139 SW@0.1u/10V_4 C138 SW@0.1u/10V_4 C129 SW@1u/6.3V_4 C124 SW@1u/6.3V_4 C153 SW@1u/6.3V_4 C130 SW@1u/6.3V_4 C150 SW@1u/6.3V_4 C157 SW@10u/6.3V_6

+1V

(1.0V@1.1A PCIE_VDDC)

C99 SW@1u/6.3V_4 C218 SW@1u/6.3V_4 C79 SW@1u/6.3V_4 C241 SW@1u/6.3V_4 C112 SW@1u/6.3V_4 C73 SW@1u/6.3V_4 C94 SW@1u/6.3V_4 C229 SW@10u/6.3V_6

+VGPU_CORE

(30A or more)

C102 SW@1u/6.3V_4 C106 SW@1u/6.3V_4 C131 SW@1u/6.3V_4 C133 SW@1u/6.3V_4 C103 SW@1u/6.3V_4 C172 SW@1u/6.3V_4 C159 SW@1u/6.3V_4 C100 SW@1u/6.3V_4 C101 SW@1u/6.3V_4 C147 SW@1u/6.3V_4

C194 SW@1u/6.3V_4 C193 SW@1u/6.3V_4 C161 SW@1u/6.3V_4 C141 SW@1u/6.3V_4 C187 SW@1u/6.3V_4 C180 SW@1u/6.3V_4 C166 SW@1u/6.3V_4 C117 SW@1u/6.3V_4 C165 SW@1u/6.3V_4 C181 SW@1u/6.3V_4

C152 SW@1u/6.3V_4 C170 SW@1u/6.3V_4 C143 SW@1u/6.3V_4 C188 SW@1u/6.3V_4 C164 SW@1u/6.3V_4 C120 SW@1u/6.3V_4 C116 SW@1u/6.3V_4 C146 SW@1u/6.3V_4 C127 SW@1u/6.3V_4 C110 SW@1u/6.3V_4

C144 SW@10u/6.3V_6 C121 SW@10u/6.3V_6 C142 SW@10u/6.3V_6 C122 SW@10u/6.3V_6 C91 SW@10u/6.3V_6 C123 SW@10u/6.3V_6

BIF_VDDC should be connected to VDDC if BACO feature not used.
For BACO, refer to the databook
(Separate Core power for PCIe bus macros
Connector to VDDCin non-ower-Xpress desingns ZR8

PIN different between Broadway and Madison		
Pin	Broadway	Madison
VDDC#32 / BIF_VDDC (N27)	VDDC	BIF_VDDC
VDDC#42 / BIF_VDDC (T27)	VDDC	BIF_VDDC
GND#61 / PX_EN (AL21)	GND	PX_EN
(AL31)	TS_A	NC_TS_A

+VGPU_CORE

(DDR3 1.12V@4A VDDCI) or more

C93 SW@1u/6.3V_4 C132 SW@1u/6.3V_4 C109 SW@1u/6.3V_4 C85 SW@1u/6.3V_4 C162 SW@1u/6.3V_4 C92 SW@1u/6.3V_4

C171 SW@10u/6.3V_6 C135 SW@10u/6.3V_6 C149 SW@10u/6.3V_6 C87 SW@1u/6.3V_4 C108 SW@1u/6.3V_4 C89 SW@1u/6.3V_4 C86 SW@1u/6.3V_4

U24F

GND

PCIE_VSS#1 AB39
PCIE_VSS#2 E39
PCIE_VSS#3 F34
PCIE_VSS#4 F39
PCIE_VSS#5 G33
PCIE_VSS#6 G34
PCIE_VSS#7 H31
PCIE_VSS#8 H34
PCIE_VSS#9 H39
PCIE_VSS#10 J31
PCIE_VSS#11 J34
PCIE_VSS#12 K31
PCIE_VSS#13 K34
PCIE_VSS#14 K39
PCIE_VSS#15 L31
PCIE_VSS#16 L34
PCIE_VSS#17 M34
PCIE_VSS#18 M39
PCIE_VSS#19 N31
PCIE_VSS#20 N34
PCIE_VSS#21 P31
PCIE_VSS#22 P34
PCIE_VSS#23 P39
PCIE_VSS#24 R34
PCIE_VSS#25 T31
PCIE_VSS#26 T34
PCIE_VSS#27 T39
PCIE_VSS#28 U31
PCIE_VSS#29 U34
PCIE_VSS#30 V34
PCIE_VSS#31 V39
PCIE_VSS#32 W31
PCIE_VSS#33 W34
PCIE_VSS#34 Y34
PCIE_VSS#35 Y39

GND#100 F15
GND#101 F17
GND#102 F19
GND#103 F21
GND#104 F23
GND#105 F25
GND#106 F27
GND#107 F29
GND#108 F31
GND#109 F33
GND#110 F7
GND#111 F9
GND#112 G2
GND#113 G6
GND#114 H9
GND#115 J2
GND#116 J27
GND#117 J6
GND#118 J8
GND#119 K14
GND#120 K7
GND#121 L11
GND#122 L17
GND#123 L2
GND#124 L22
GND#125 L24
GND#126 L6
GND#127 M17
GND#128 M22
GND#129 M24
GND#130 N16
GND#131 N18
GND#132 N2
GND#133 N21
GND#134 N23
GND#135 N26
GND#136 N6
GND#137 R15
GND#138 R17
GND#139 R2
GND#140 R20
GND#141 R22
GND#142 R24
GND#143 R27
GND#144 R6
GND#145 T11
GND#146 T13
GND#147 T16
GND#148 T18
GND#149 T21
GND#150 T23
GND#151 T26
GND#152 U15
GND#153 U17
GND#154 U2
GND#155 U20
GND#156 U22
GND#157 U24
GND#158 U27
GND#159 U6
GND#160 V11
GND#161 V16
GND#163 V18
GND#164 V21
GND#165 V23
GND#166 V26
GND#167 W2
GND#168 W6
GND#169 Y15
GND#170 Y17
GND#171 Y20
GND#172 Y22
GND#173 Y24
GND#174 Y27
GND#175 U13
GND#152 V13

GND#1 A3
GND#2 A37
GND#3 AA16
GND#4 AA18
GND#5 AA2
GND#6 AA21
GND#7 AA23
GND#8 AA26
GND#9 AA28
GND#10 AA6
GND#11 AB12
GND#12 AB15
GND#13 AB17
GND#14 AB20
GND#15 AB22
GND#16 AB24
GND#17 AB27
GND#18 AC11
GND#19 AC13
GND#20 AC16
GND#21 AC18
GND#22 AC2
GND#23 AC21
GND#24 AC23
GND#25 AC26
GND#26 AC28
GND#27 AC6
GND#28 AD15
GND#29 AD17
GND#30 AD20
GND#31 AD22
GND#32 AD24
GND#33 AD27
GND#34 AD9
GND#35 AE2
GND#36 AE6
GND#37 AE10
GND#38 AE16
GND#39 AE18
GND#40 AF21
GND#41 AG2
GND#42 AG20
GND#43 AG22
GND#44 AG6
GND#45 AG9
GND#46 AH21
GND#47 AJ10
GND#48 AJ11
GND#49 AJ12
GND#50 AJ28
GND#51 AJ6
GND#52 AK11
GND#53 AK31
GND#54 AK7
GND#55 AL11
GND#56 AL14
GND#57 AL17
GND#58 AL2
GND#59 AL20
GND#60 AL21
GND#61 AL23
GND#62 AL26
GND#63 AL32
GND#64 AL6
GND#65 AL8
GND#66 AM11
GND#67 AM31
GND#68 AM9
GND#69 AN11
GND#71 AN2
GND#72 AN30
GND#73 AN6
GND#74 AN8
GND#75 AP11
GND#76 AP7
GND#77 AP9
GND#78 AR5
GND#79 AW34
GND#80 B11
GND#81 B13
GND#82 B15
GND#83 B17
GND#84 B19
GND#85 B21
GND#86 B23
GND#87 B25
GND#88 B27
GND#89 B29
GND#90 B31
GND#91 B33
GND#92 B7
GND#93 B9
GND#94 C1
GND#95 C39
GND#96 E35
GND#97 E5
GND#98 F11
GND#99 F13

VSS_MECH#1 A39
VSS_MECH#2 AW1
VSS_MECH#3 AW36

SP@Madison/Park_M2

GND#61/ PX_EN
PowerXpress control signal for Madsion and Park only
If not used, can be disconnected.
PX_EN = LOW, turn on
PX_EN = HIGH, turn off
PX_EN is used to turn ON/OFF some regulators for PowerXpress mode. An output high '3.3V' will turn the regulators OFF. An output low '0V' will turn the regulators ON. PX_EN outputs low (0V) by default.
If this signal is unused, it can be NC (not connected) or connected to ground.

R71 *SW@4.7K_4

B-TEST 0223

Pin AL21 to Ground for Broadway

GPU all PWROK

+3V

R112 SW@10K_4

dGPU_PWROK 12

R107 SW@10K_4

Q6 SW@2N7002K

+1.8V_GPU

Q4 SW@DTC144EUA

GPU +3V power

13 MXM_PWREN

R128 SW@0_4

+1.5V_GPU

R129 *SW@0_4

C279 *SW@1u/6.3V_4

R454 SW@4.7K_4

Q9 SW@ME2N7002E

B-TEST 0128

C-TEST 0323

Q9 change footprint from UMT_213-3-1_3 to SOT23_213-3_3-2

Q28 SW@AO3413

R449 *SW@0_6

0.5A

+3V_D

C697 SW@10u/6.3V_6 C694 SW@1u/6.3V_4 C696 SW@0.1u/10V_4

R450 *SP@0_6

Q29 SP@AO3413

R453 *SP@0_6

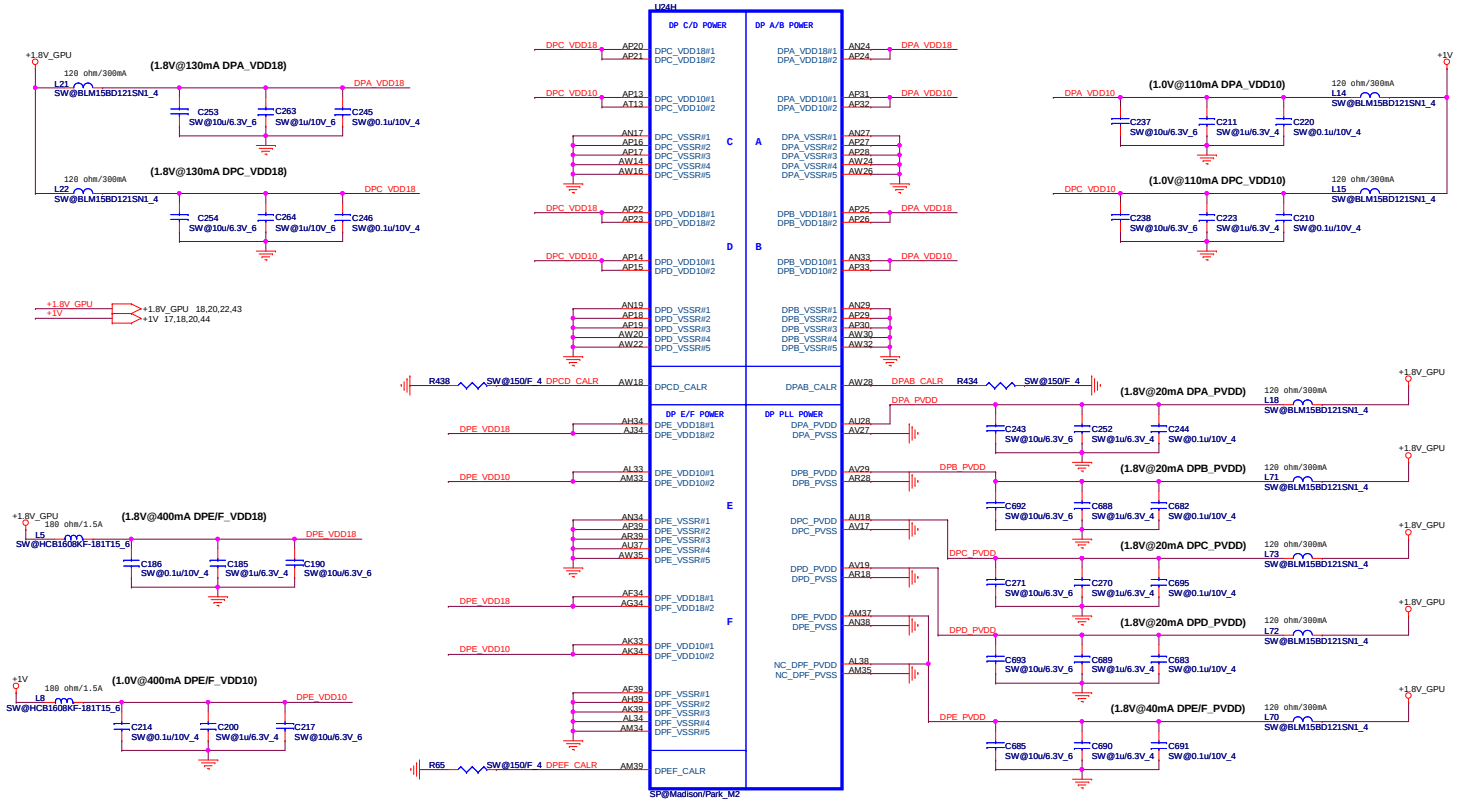
0.5A

+3V_D_EXT

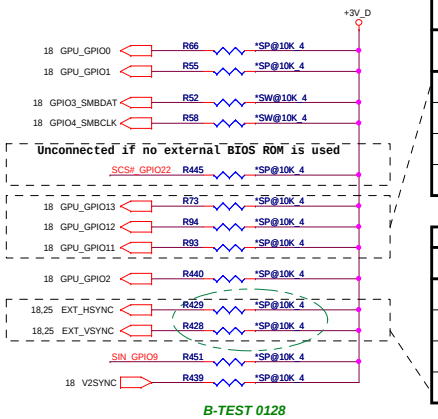
C727 SP@10u/6.3V_6 C711 SP@1u/6.3V_4 C728 SP@0.1u/10V_4

Quanta Computer Inc.
PROJECT : ZRA

Size	Document Number	Rev
	Madison/Broadway PWR_GND	1A
Date: Monday, March 29, 2010	Sheet 20 of 48	


U24H
DP C/D POWER
DP A/B POWER
DP E/F POWER
DP PLL POWER
SP@Madison/Park_M2
+1.8V_GPU
(1.8V@130mA DPA_VDD18)
(1.8V@130mA DPC_VDD18)
(1.8V@400mA DPE/F_VDD18)
(1.0V@400mA DPE/F_VDD10)
(1.0V@110mA DPA_VDD10)
(1.0V@110mA DPC_VDD10)
(1.8V@20mA DPA_PVDD)
(1.8V@20mA DPB_PVDD)
(1.8V@20mA DPC_PVDD)
(1.8V@20mA DPD_PVDD)
(1.8V@40mA DPE/F_PVDD)
+1V
+1.8V_GPU 18,20,22,43
+1V 17,18,20,44
Quanta Computer Inc.
PROJECT : ZRA
Madison/Broadway DPPW_GND
Rev 1A
Date: Monday, March 29, 2010
Sheet 21 of 48

PIN STRAPS



B-TEST 0128

Memory Aperture size	
GPIO[13:11]	Size
000	128MB
001	256MB
010	64MB
011	32MB

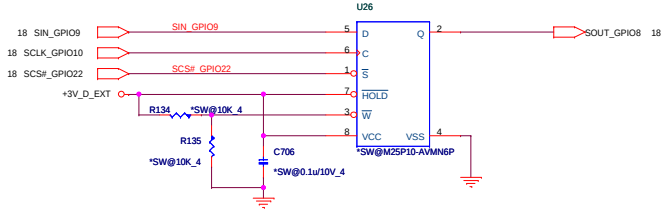
Function Table		
EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by dectec
1	0	DP only
1	1	Both DP & HDMI

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT NUMONYX M25P10A : 101	000	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	(Recommended setting as 5.0 GT/s capability will be controlled by software.)
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable 1 = VGA controller capacity disenable (The device will not be recognized as the system's VGA controller.)	0	
VIP_DEVICE_STRAP_DIS	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET. 1 = DRIVER would use the value sample on VHAD_0 during RESET.	0	

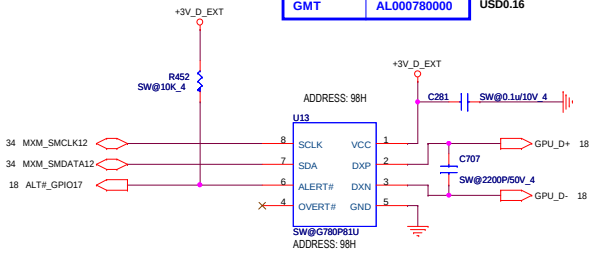
SERIAL ROM *Default don't put*



Thermal Sensor

Vendor	P/N
WINDBOND	AL83L771K01
GMT	AL000780000

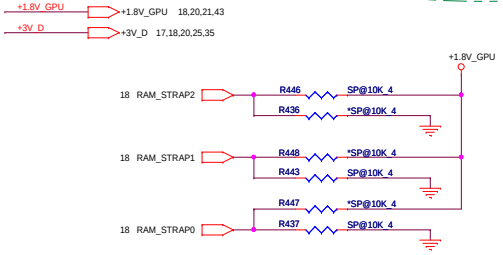
USD0.16



DDR3 Memory Aperture size

DDR3 Memory Aperture size						
Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix	H5TQ1G63BFR-12C		512Mb			
		AKD5LZGTW04 (64M*16)	1Gb	1	0	0
			2Gb			
Samsung	K4W1G1646E-HC12		512Mb			
		AKD5LGGT506 (64M*16)	1Gb	0	0	0
	K4W2G1646B-HC12	AKD5MGGT500	2Gb			
AMD	23EY2387MA12-SZ	AKD5LGGT700	1Gb	0	1	0

B-TEST 0128



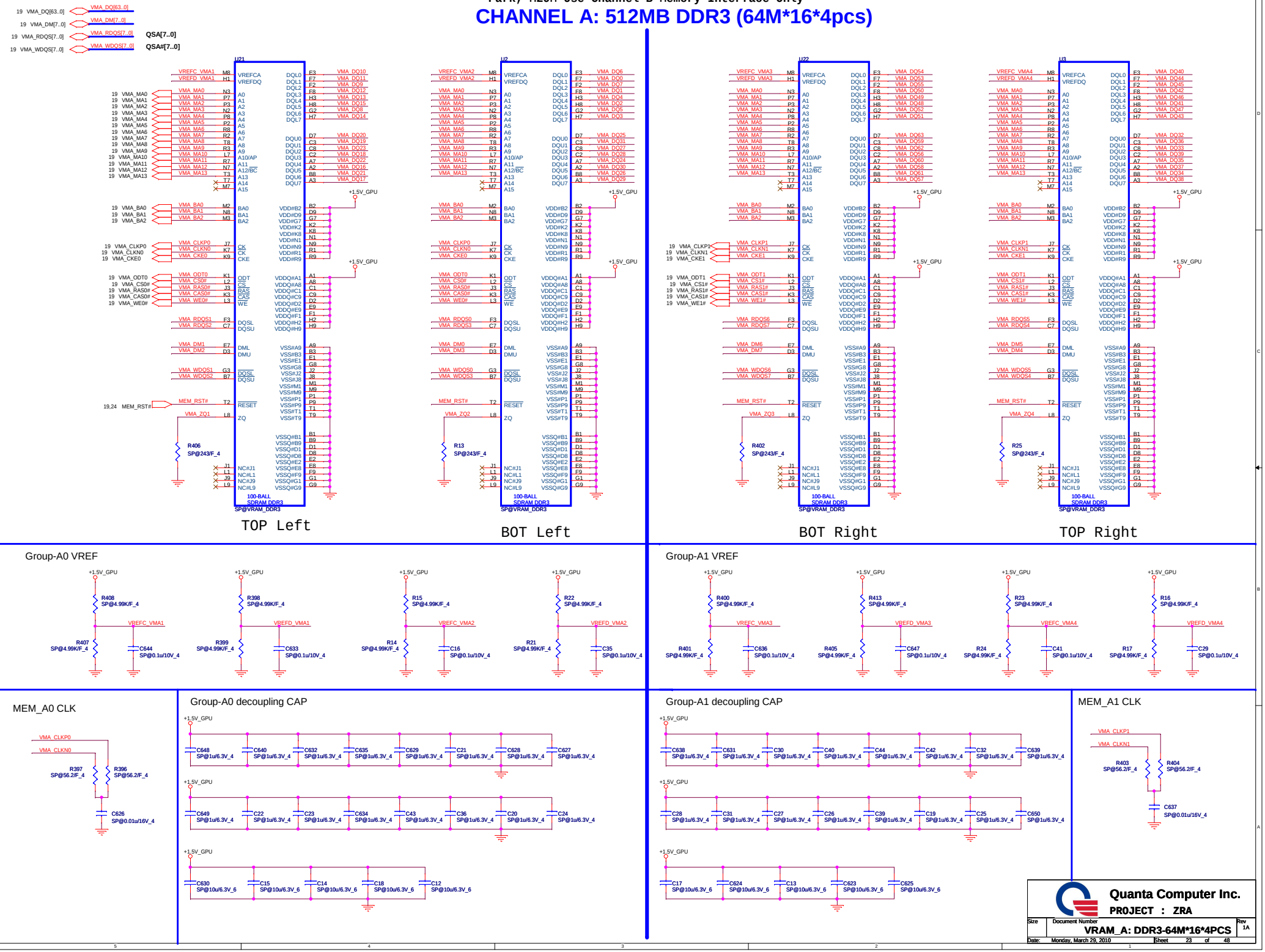
RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.

Quanta Computer Inc.
PROJECT : ZRA

Size	Document Number	Rev
	Memory strip/Thermal/HDCP	1A
Date: Monday, March 29, 2010	Sheet 22 of 48	

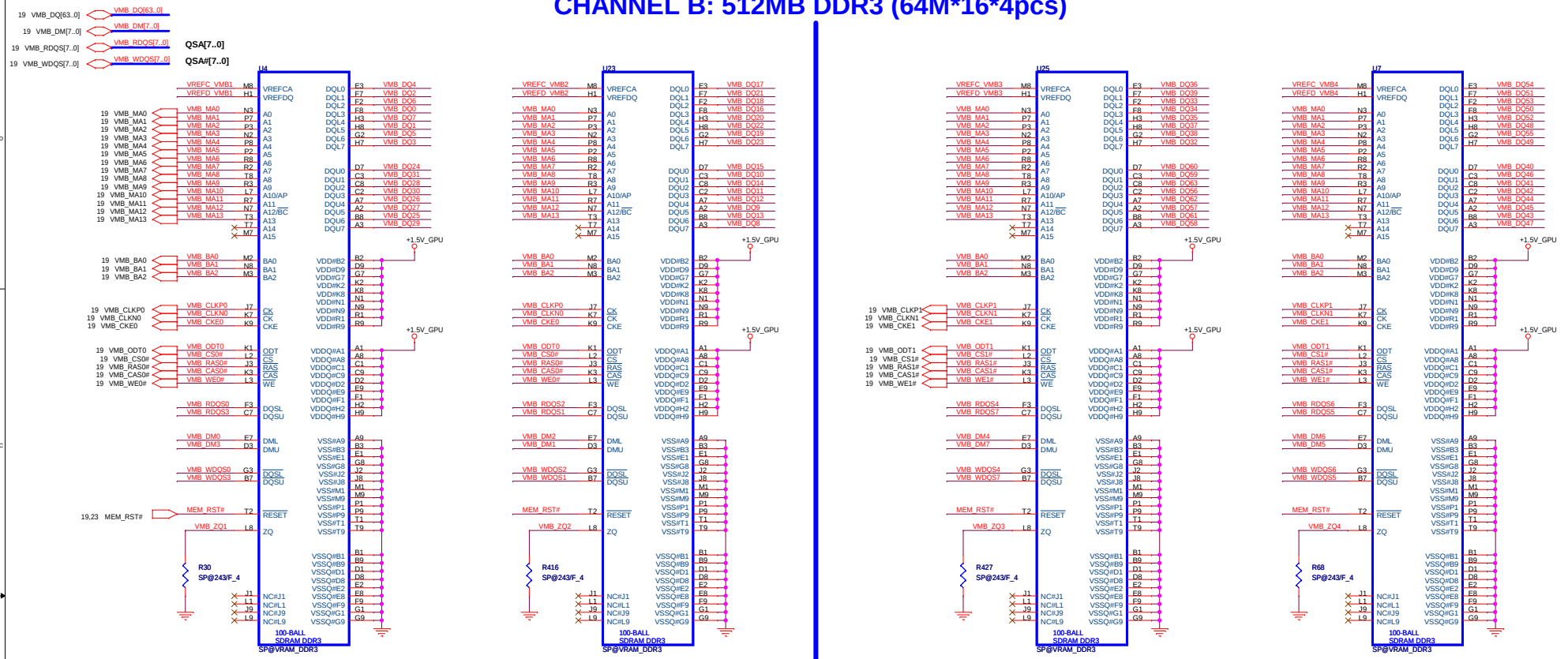
Park, M29M Use Channel B Memory Interface Only

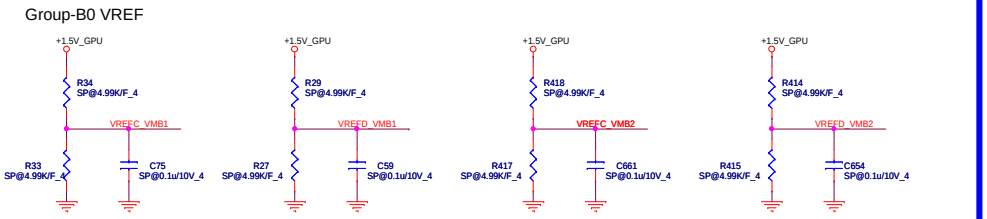
CHANNEL A: 512MB DDR3 (64M*16*4pcs)

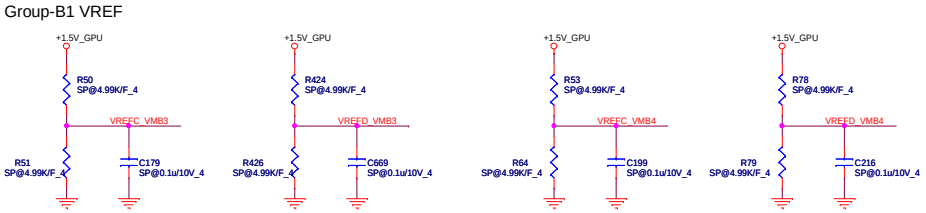


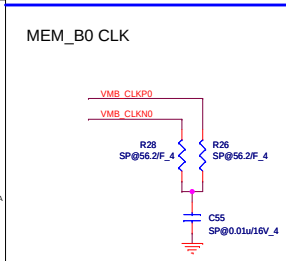
Quanta Computer Inc.	PROJECT : ZRA	
Size	Document Number: VRAM_A: DDR3-64M*16*4PCS	Rev: 1A
Date: Monday, March 29, 2010	Sheet 23 of 48	

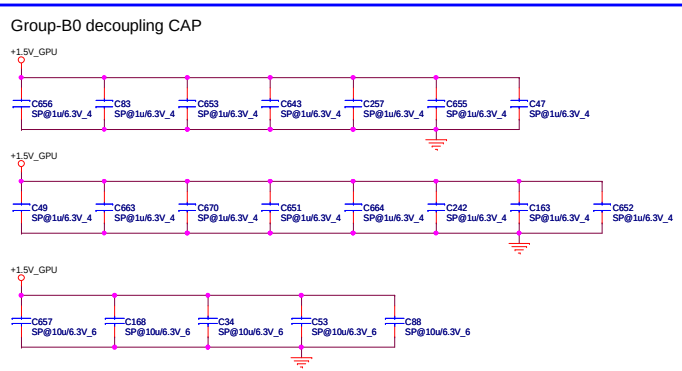
CHANNEL B: 512MB DDR3 (64M*16*4pcs)

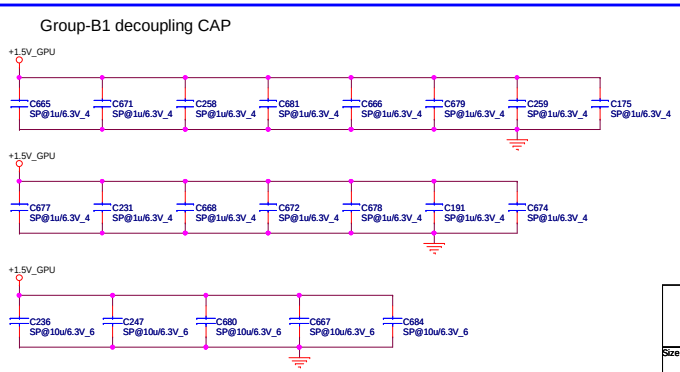


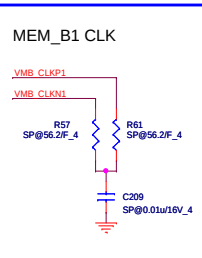












Quanta Computer Inc.

PROJECT : ZRA

Size	Document Number	Rev
	VRAM_B: DDR3-64M*16*4PCS	1A
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CRT MUXs / No MUXs

S	Yn
0	IV
1	SW(EV)

OPTION SIGNAL FROM NB to CRT for UMA

CRT LVDS MUXs / No MUXs

OPTION Back Light SIGNAL FROM NB to LVDS for UMA

OPTION LCDVCC SIGNAL FROM NB to LVDS for UMA

LVDS MUXs / No MUXs

B-TEST 0201

CRT LVDS MUXs / No MUXs

OPTION SIGNAL FROM NB to CRT for UMA

A-test 確認 R7467 R7468 R7295 R7469是否可以不上件

Follow AMD reference schematic change for reduce leakage to VDDR3 BUS.

CAMERA Module(CCD) / Digital MIC

C-TEST 0322

change R4 from 0R to PBY160808T-601Y-N FOR EMI

change R388 R390 footprint from RC0402 to short_4

EMI

stuff C1,C2

CRT SWITCH

B-TEST 0225

CRT

B-TEST 0210 B-TEST 0128

B-TEST 0210

CRT DDCCLK ,DDCDATA pull high resistor to +3v or +5v.
Due to RS880M and Madison DDC can support 5V tolerance

LVDS MUXs / No MUXs

TI	AL3DV421V00
Pericom	AL000412W00

PE_GPIO2	Output
L	INT_LVDS
H	EV_LVDS

IGPU_Channel-A

DGPU_Channel-A

OPTION SIGNAL FROM NB to LVDS for UMA

2~3pin share one cap

LCD Power

Backlight Control

Lid Switch (HSR)

AL006781000 no need pull high R. USD 0.053
AL003661003 need pull high 100K. USD 0.05
AL002648034 need pull high 100K. USD 0.048

Quanta Computer Inc. PROJECT : ZRA			
Size	Document Number		Rev
	CRT/LVDS/CCD/DIG MIC		1A
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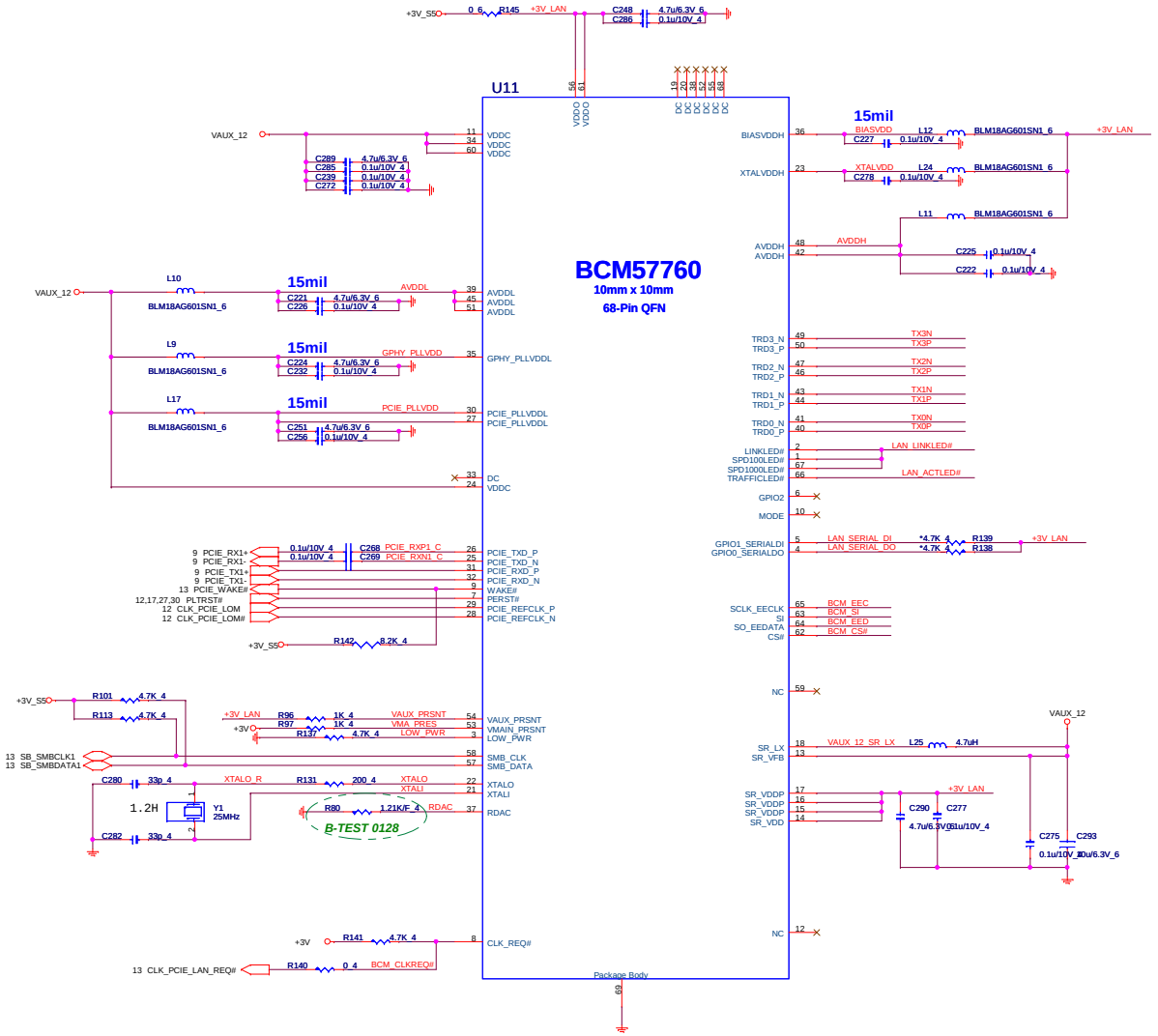
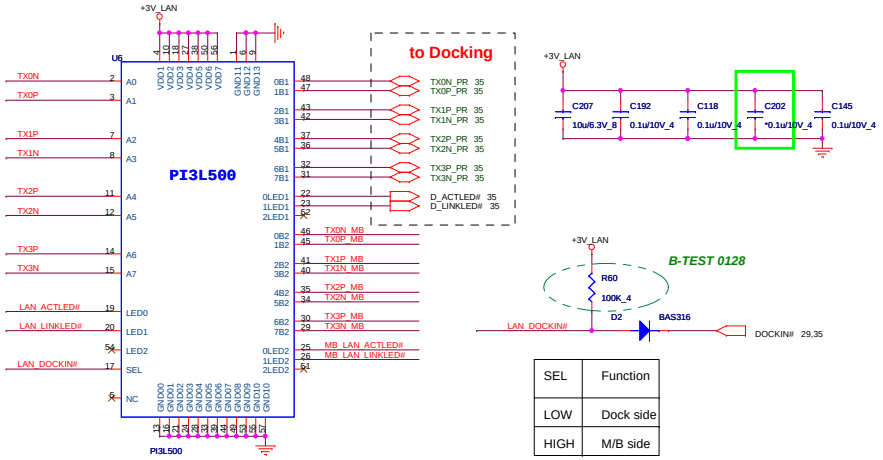
Giga-LAN BCM57760(LAN)

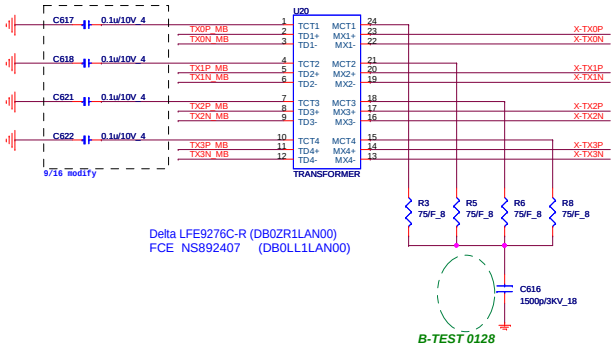


LAN SWITCH

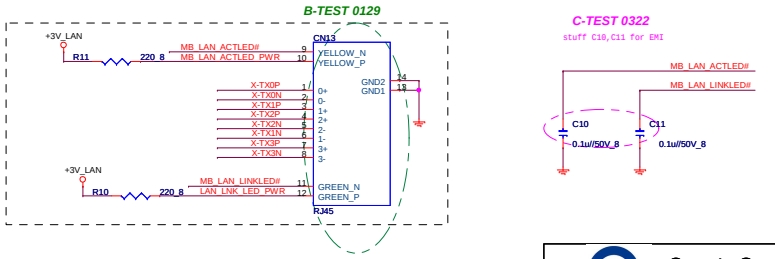


SEL	Function
LOW	Dock side
HIGH	M/B side

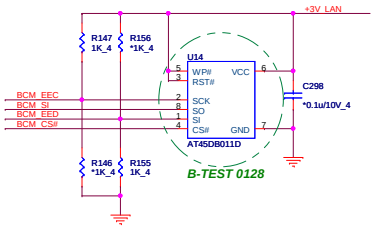
TRANSFORMER



RJ45(LAN)



Flash (1M) for ASF2.0



Quanta Computer Inc.		
PROJECT : ZRA		
Size	Document Number: LAN (BCM57760)	Rev 1A
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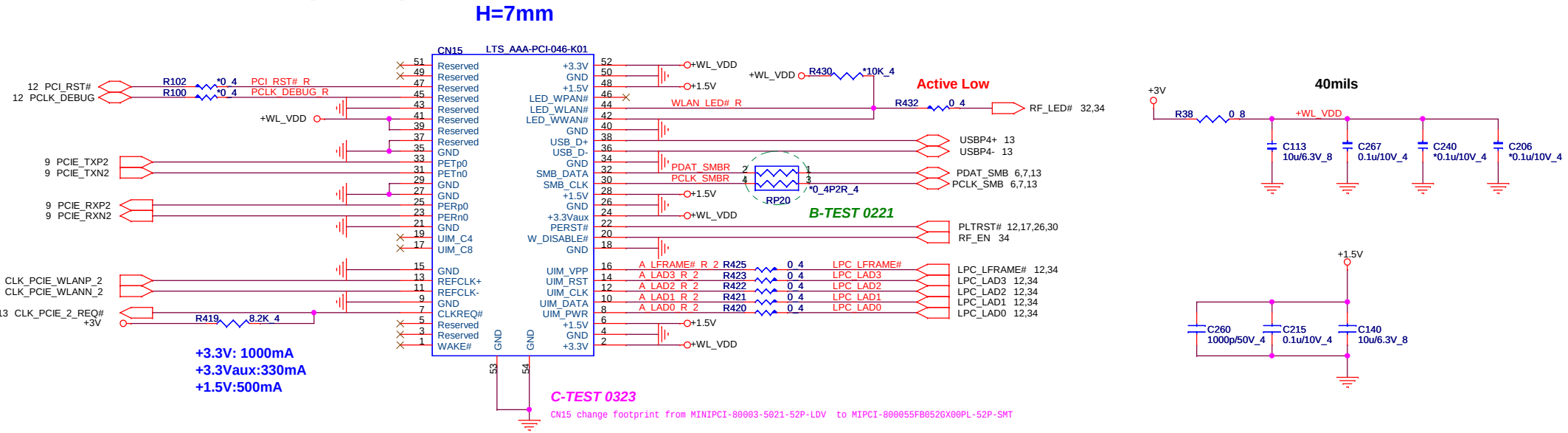
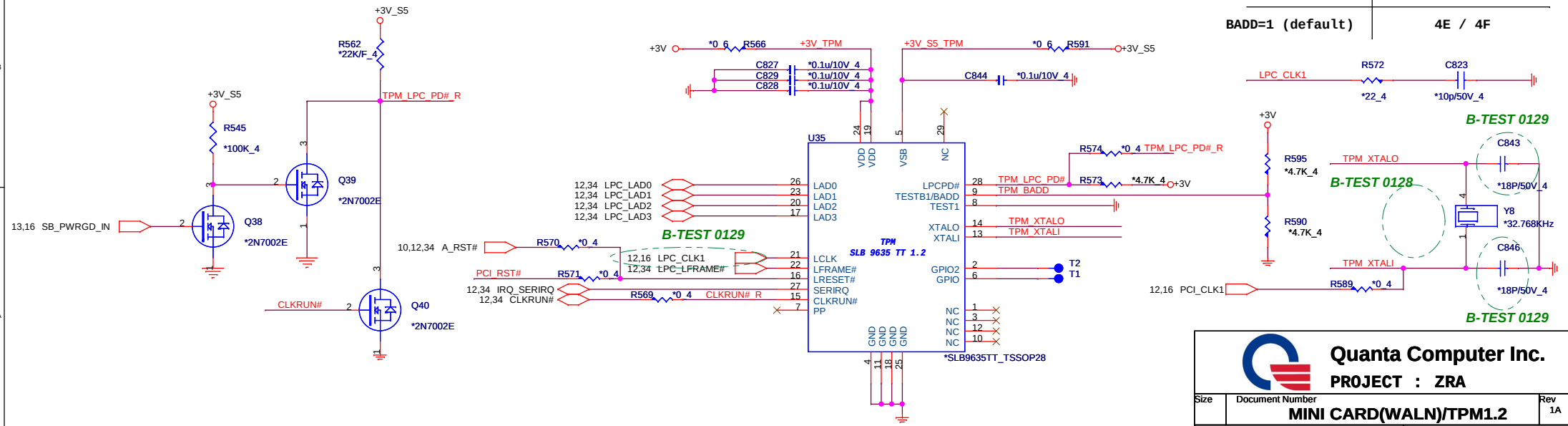
MINI-CARD WLAN(MPC)



TPM

Resiger Base Address	
BADD=0	2E / 2F
BADD=1 (default)	4E / 4F



Quanta Computer Inc.			
PROJECT : ZRA			
Size	Document Number		Rev
	MINI CARD(WALN)/TPM1.2		1A
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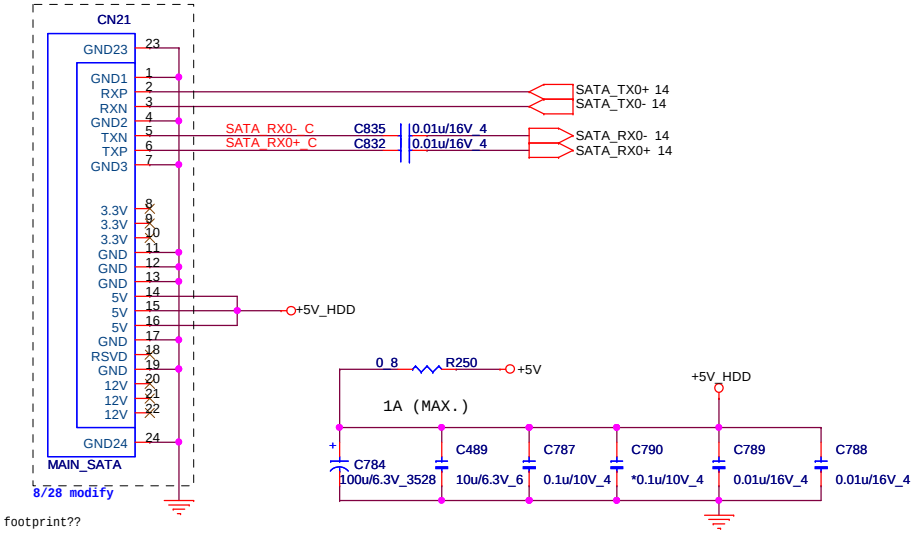
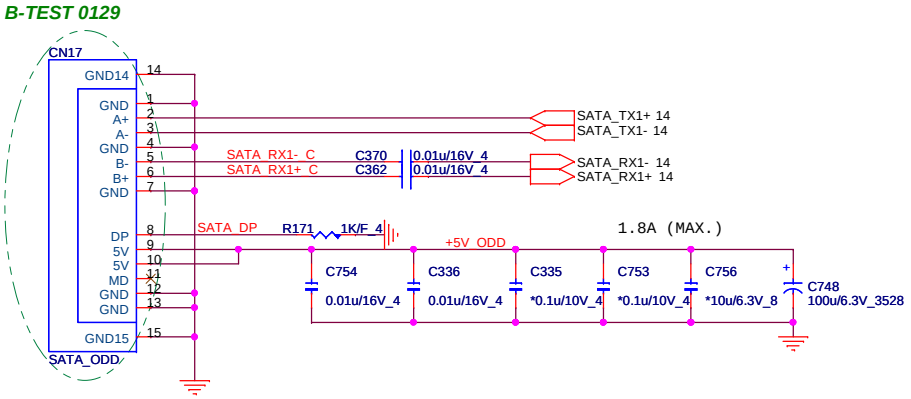
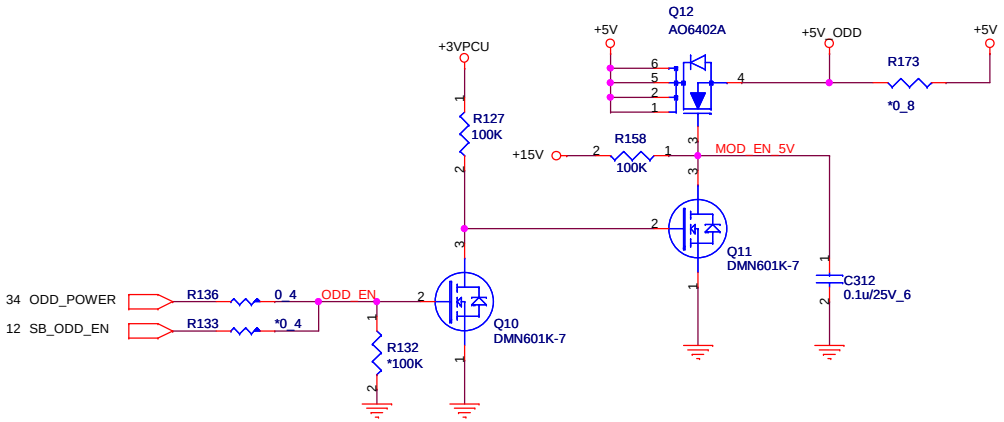
SATA HDD(HDD)



SATA ODD (ODD)



ODD POWER(ODD)



Quanta Computer Inc.		
PROJECT : ZRA		
Size	Document Number: SATA-HDD/ODD	Rev: 1A
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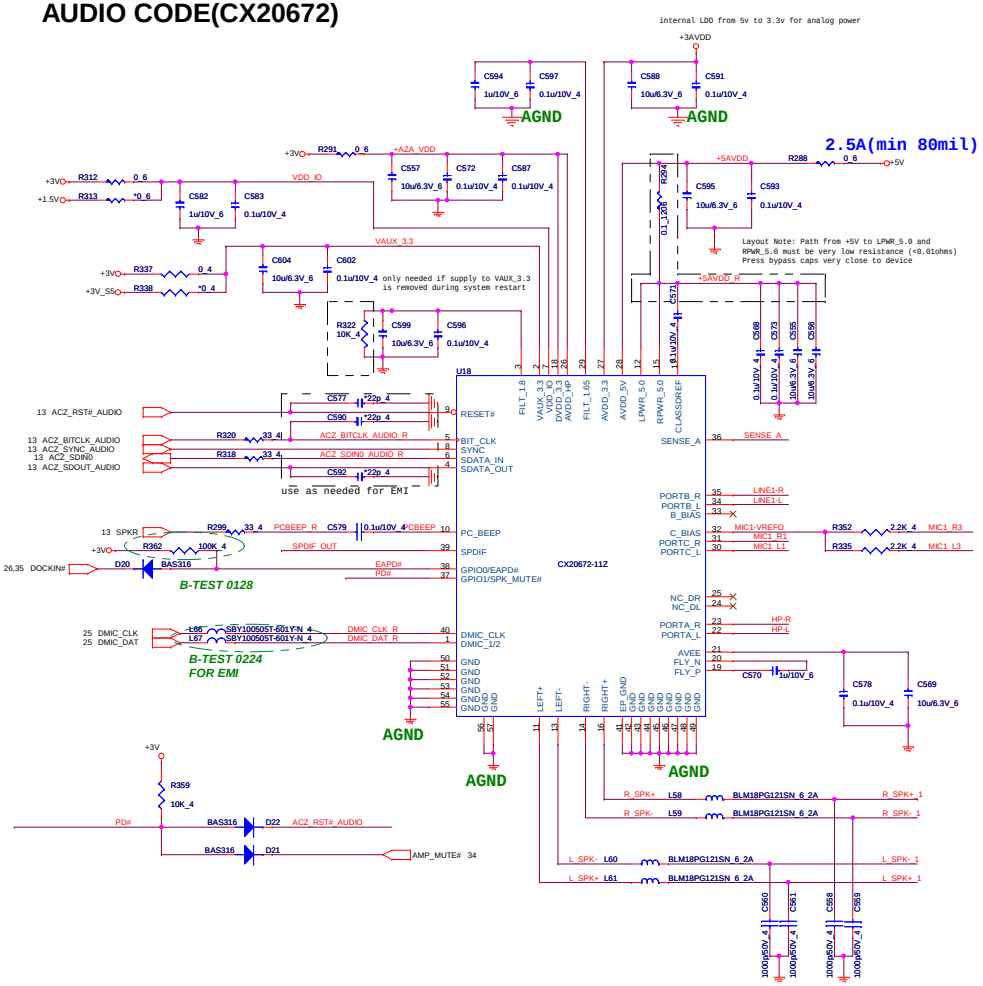
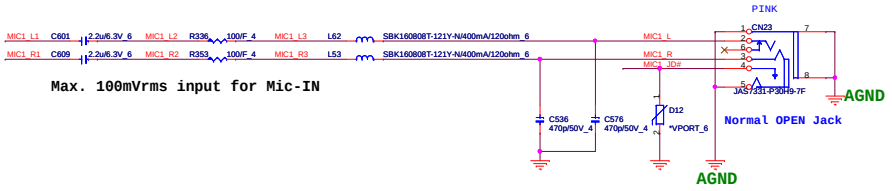
AUDIO CODE(CX20672)

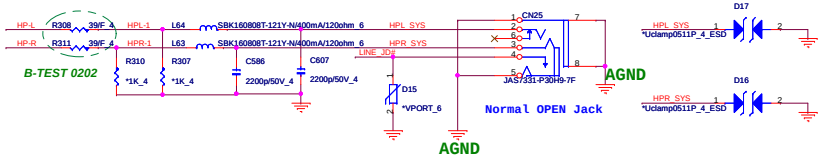


EXTERNAL MIC

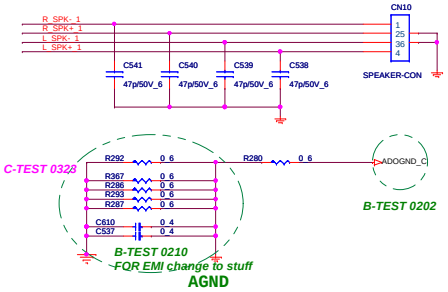


Max. 100mVrms input for Mic-IN

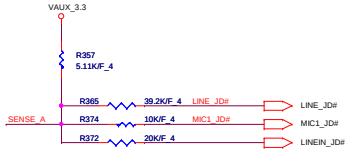
LINE-OUT/SPDIFO(AMP)



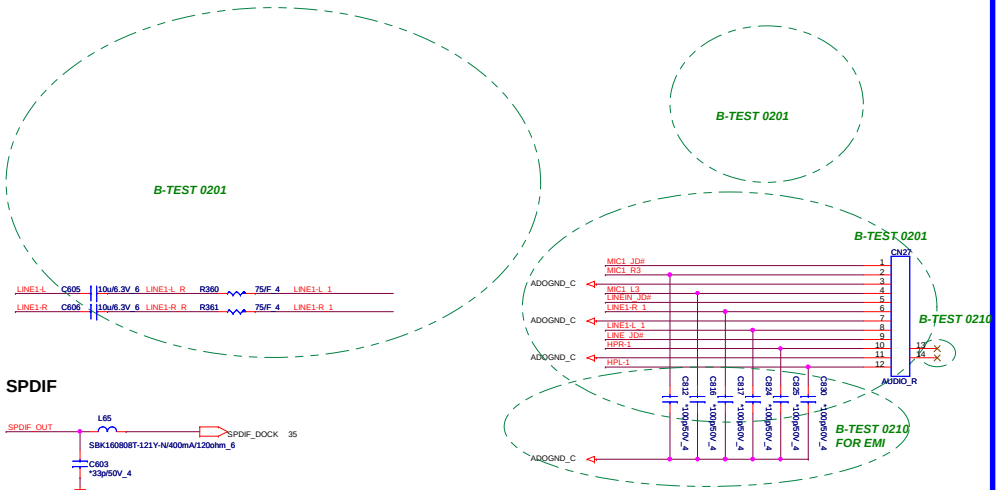
INT SPEAKER CONN



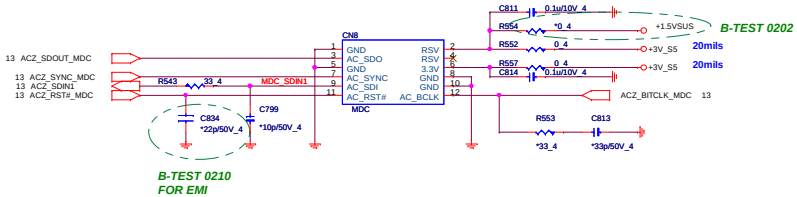
Jack Detect Resistor



SPDIF



MDC Module



Quanta Computer Inc.
PROJECT : ZRA

Size	Document Number	Rev
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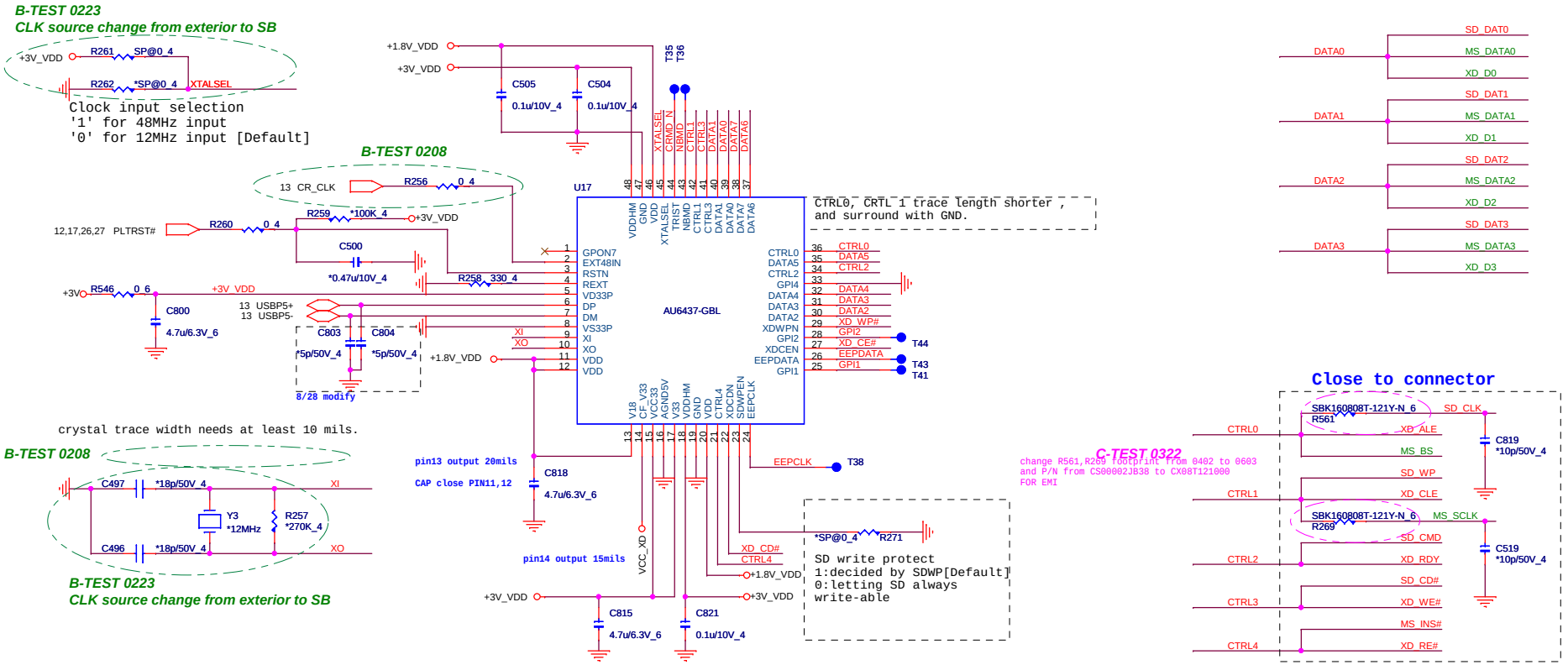
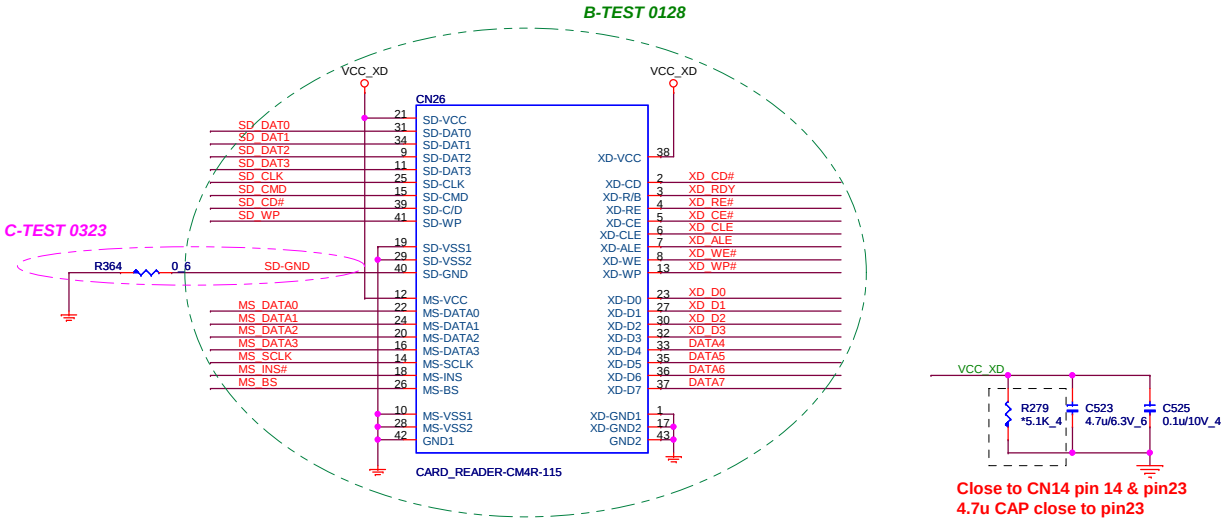
CARD READER (AU6437)



4 IN 1 CARD READER (MMC)



Quanta Computer Inc.		
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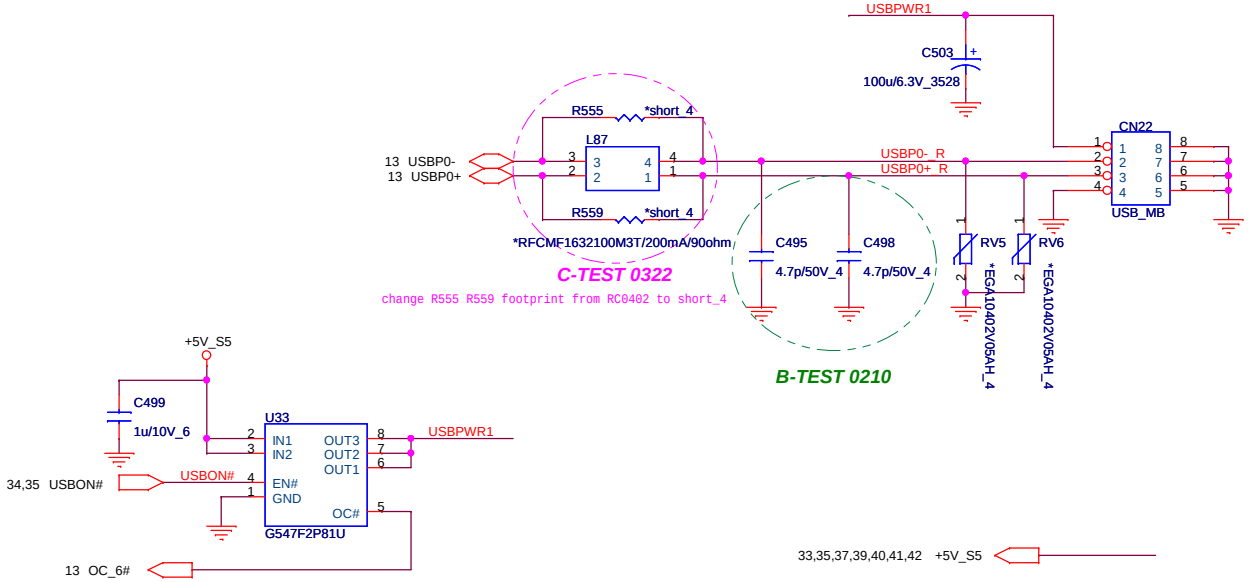
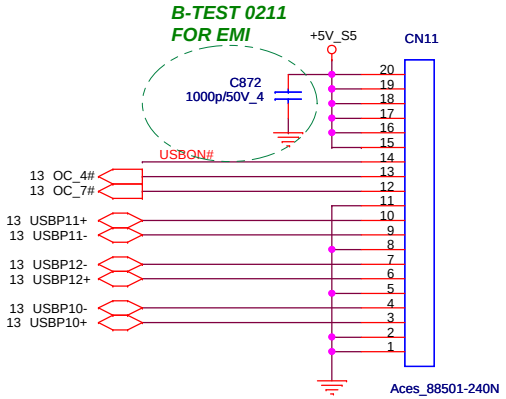
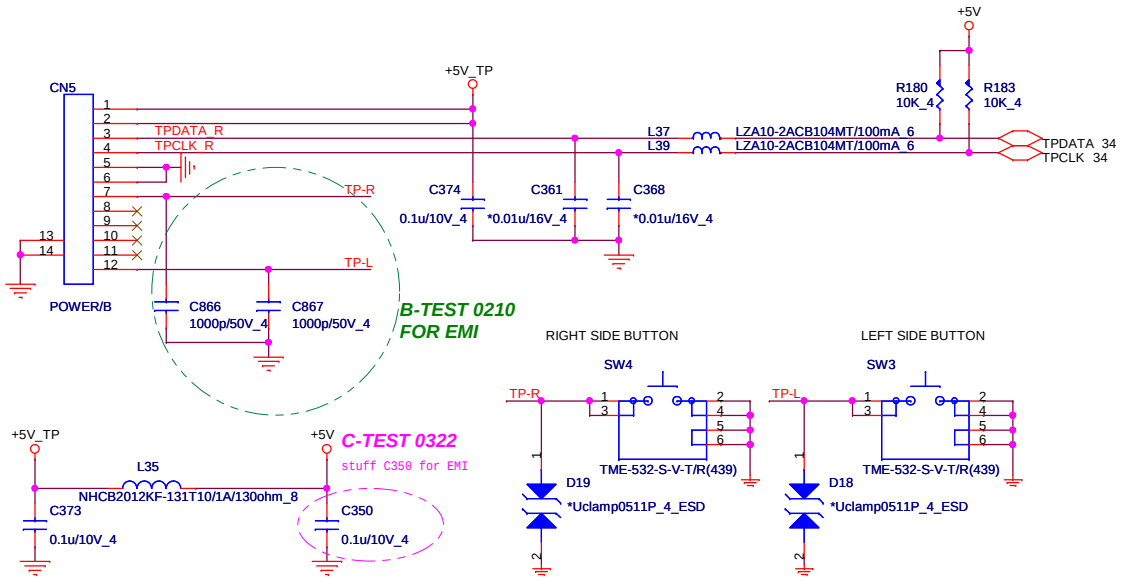
USB PORT(USB)



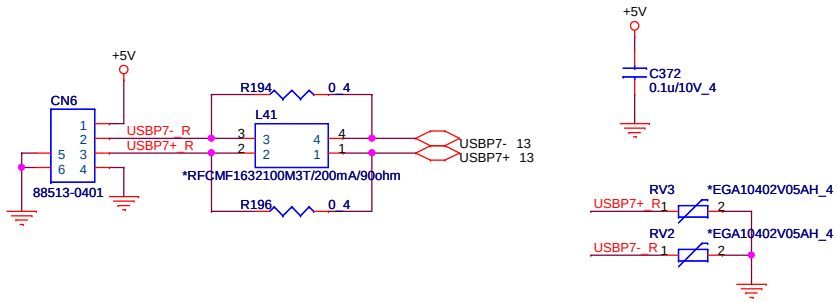
USB BOARD CONN(USB)



Touch Pad



Finger Print



Quanta Computer Inc.		
PROJECT : ZRA		
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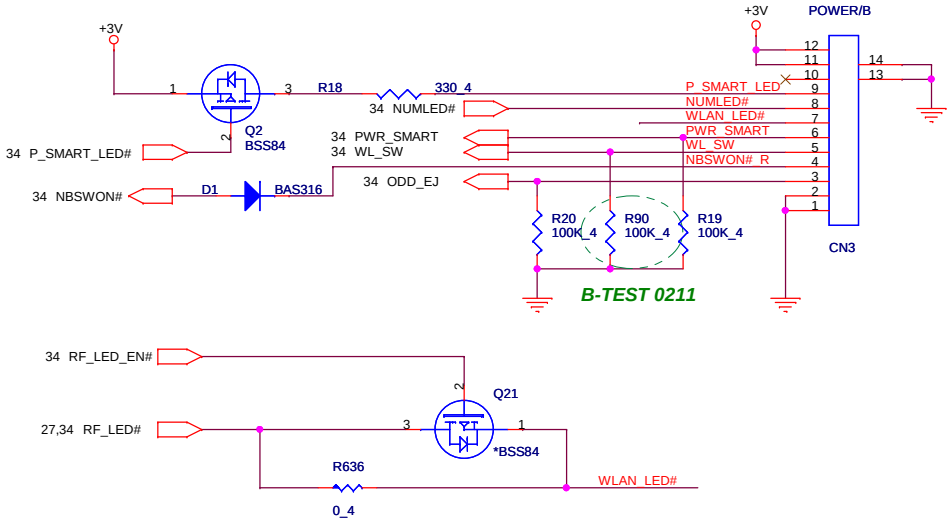
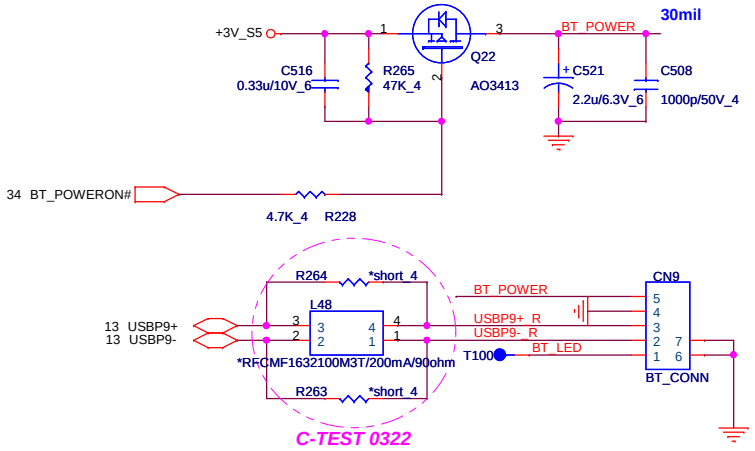
POWER DB CONN(UIF)

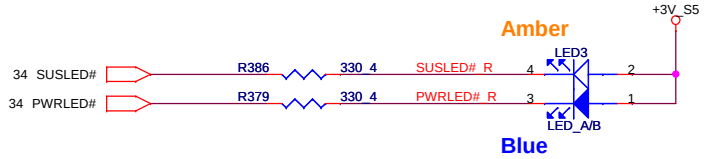


BLUETOOTH CONN(BTM)

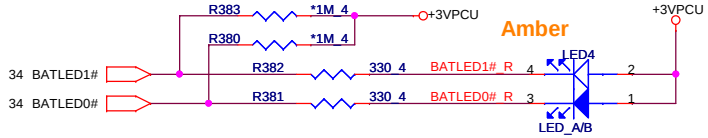


LED(UIF)

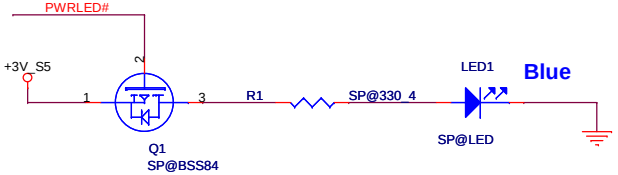
Power LED



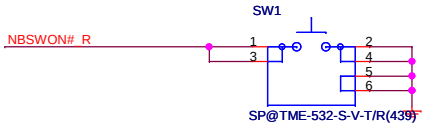
Battery LED



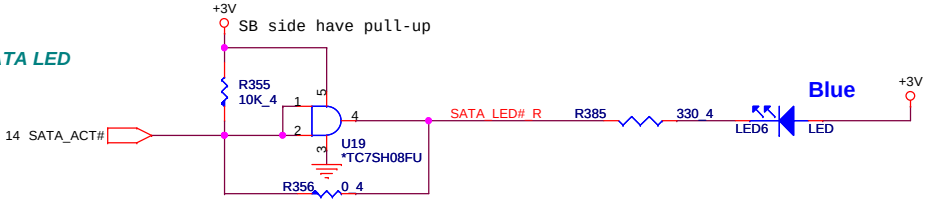
BXP Power LED



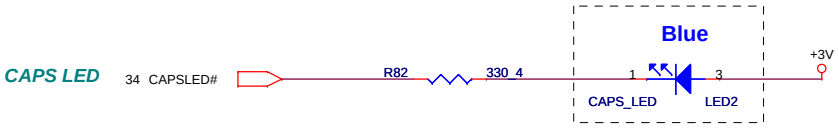
BXP Power SW

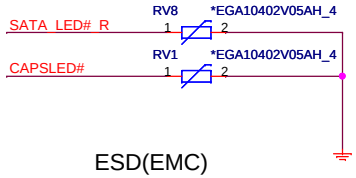


SATA LED



CAPS LED





ESD(EMC)

Quanta Computer Inc.

PROJECT : ZRA

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	PWR DB/BT/LED	1A
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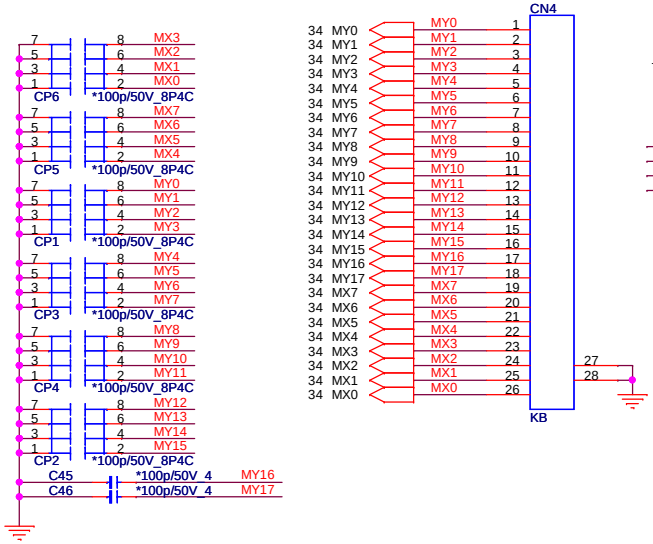
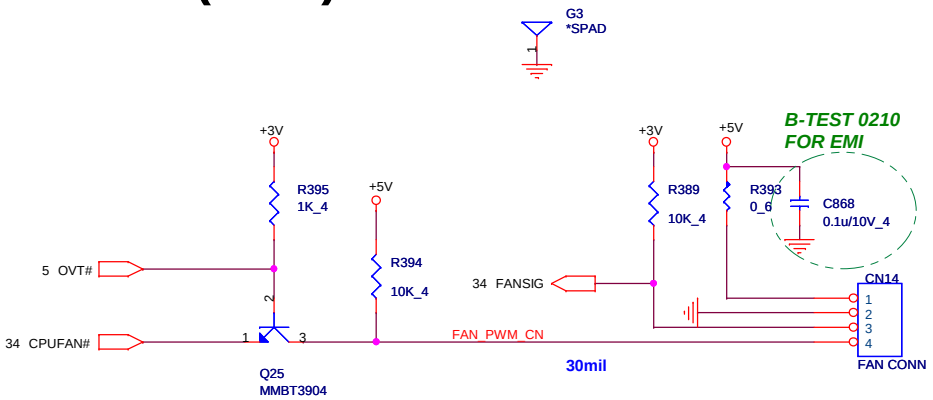
K/B(KBC)

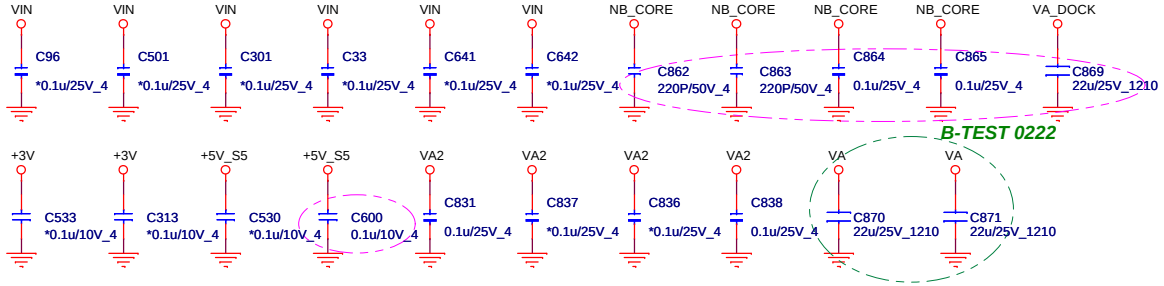


CPU FAN(THM)

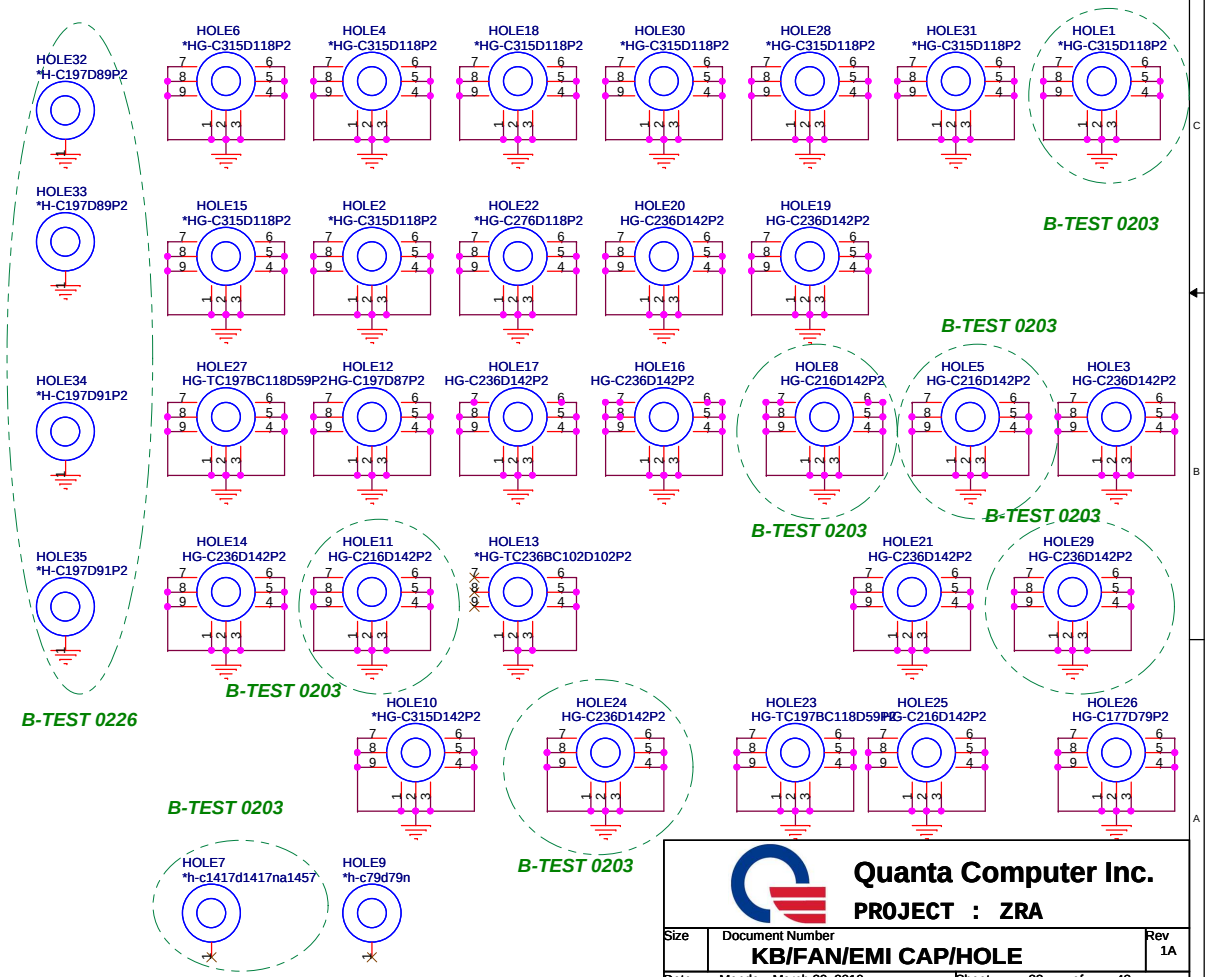


EMI CAP

C-TEST 0322 stuff C862,C863,C864,C865,C600,C869,C831,C838



HOLE(OTH)



Quanta Computer Inc.

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Size	Document Number	Rev
	KB/FAN/EMI CAP/HOLE	1A

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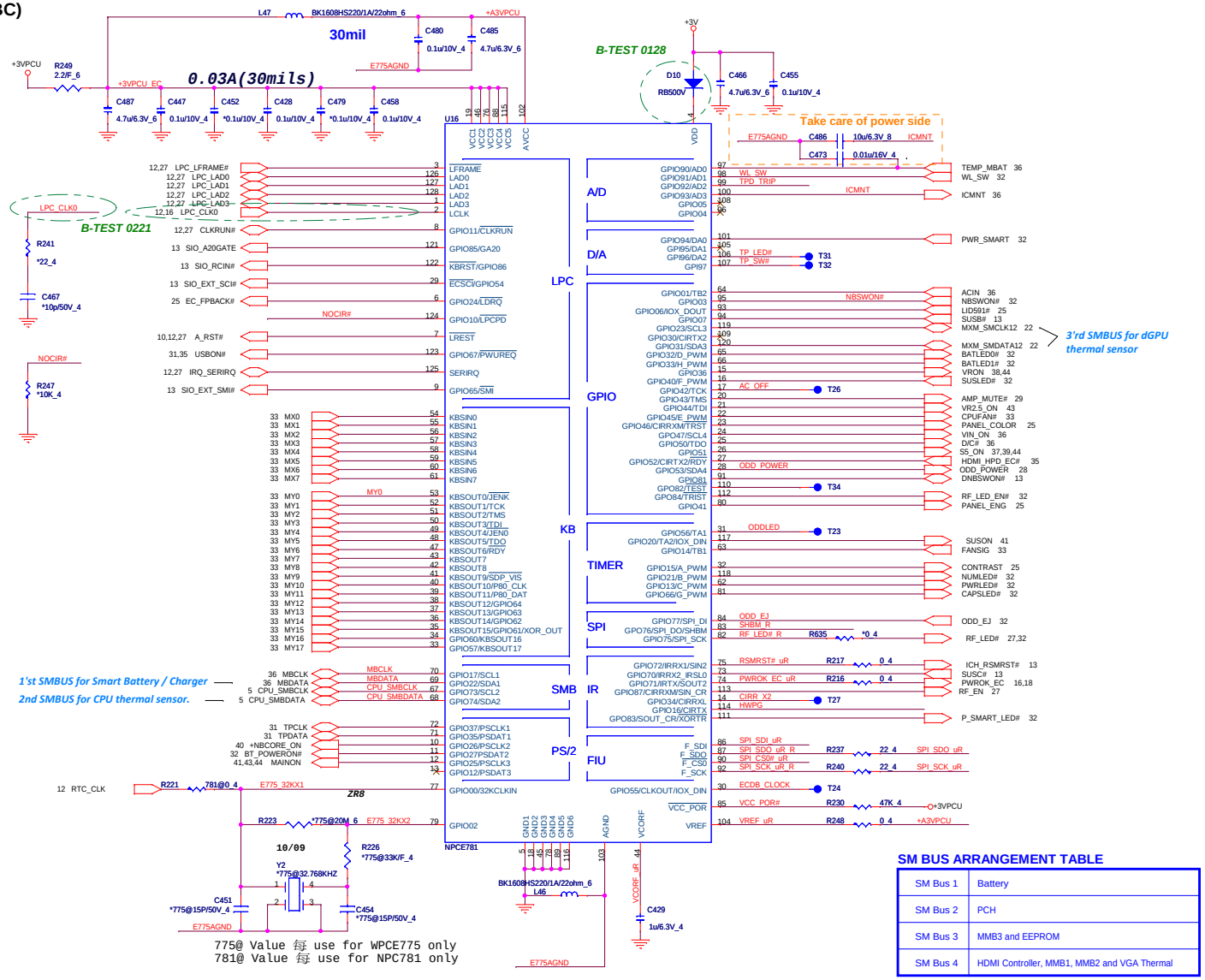
EC(KBC)



SM BUS ARRANGEMENT TABLE

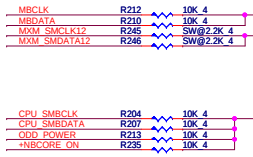
SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	MMB3 and EEPROM
SM Bus 4	HDMI Controller, MMB1, MMB2 and VGA Thermal

I/O ADDRESS SETTING(KBC)

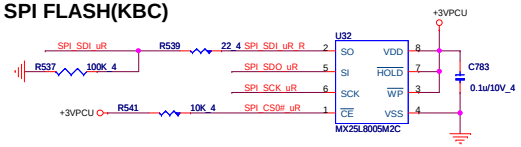
SHBM=0: Enable shared memory with host BIOS

Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

SM BUS PU(KBC)

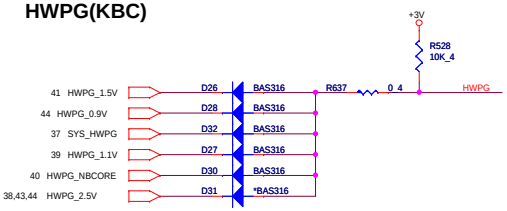


SPI FLASH(KBC)

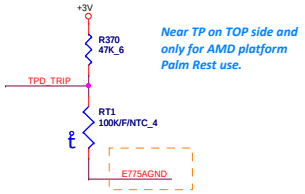


If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

HWPG(KBC)

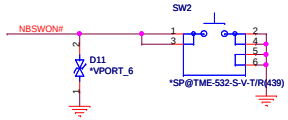


Palm Rest Thermal Sensor(THM)



Near TP on TOP side and only for AMD platform Palm Rest use.

POWER-ON Switch(KBC)



INTERNAL KEYBOARD STRIP SET(KBC)

Quanta Computer Inc.		
PROJECT : ZRA		
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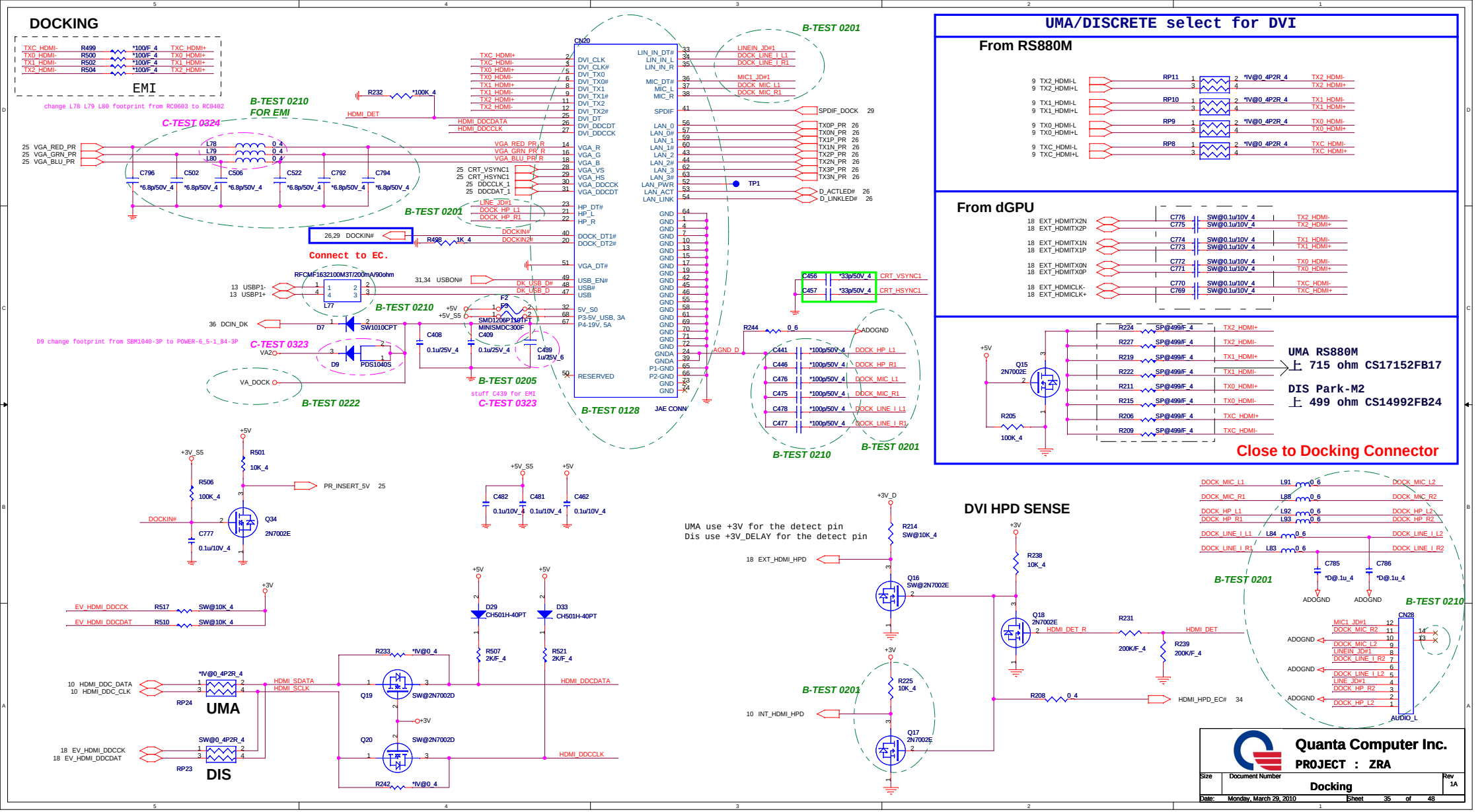
DOCKING
EMI
B-TEST 0210
FOR EMI
C-TEST 0324
B-TEST 0201
B-TEST 0210
C-TEST 0323
B-TEST 0205
B-TEST 0222
B-TEST 0128
JAE CONN
Connect to EC.
UMA/DISCRETE select for DVI
From RS880M
From dGPU
UMA RS880M
715 ohm CS17152FB17
DIS Park-M2
499 ohm CS14992FB24
Close to Docking Connector
DVI HPD SENSE
UMA use +3V for the detect pin
Dis use +3V_DELAY for the detect pin
UMA
DIS
Quanta Computer Inc.
PROJECT : ZRA
Docking
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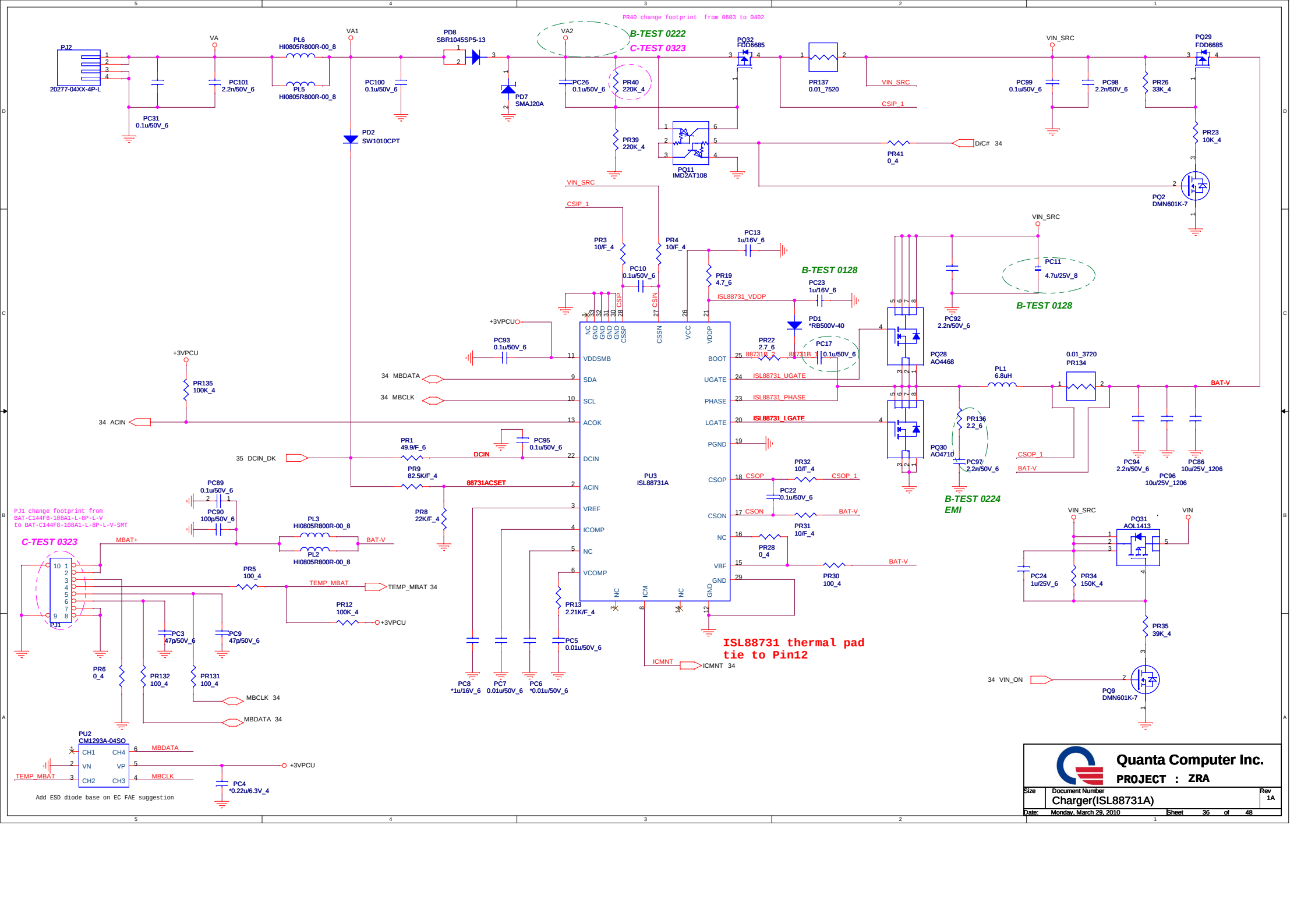
PR40 change footprint from 0603 to 0402
B-TEST 0222
C-TEST 0323
B-TEST 0128
B-TEST 0224
EMI
C-TEST 0323
PJ1 change footprint from BAT-C144F8-108A1-L-8P-L-V to BAT-C144F8-108A1-L-8P-L-V-SMT
ISL88731 thermal pad tie to Pin12
Add ESD diode base on EC FAE suggestion
PU3 ISL88731A
PJ2
20277-04XX-4P-L
PJ1
PU2 CM1293A-04SO
PQ2 DMN601K-7
PQ9 DMN601K-7
PQ28 AO4468
PQ30 AO4710
PQ31 AOL1413
PQ32 FDD6685
PQ29 FDD6685
PQ11 IMD2AT108
PD1 *RB500V-40
PD2 SW1010CPT
PD7 SMAJ20A
PD8 SBR1045SP5-13
PL1 6.8uH
PL2 HI0805R800R-00_8
PL3 HI0805R800R-00_8
PL5 HI0805R800R-00_8
PL6 HI0805R800R-00_8
PR137 0.01_7520
PR134 0.01_3720
Quanta Computer Inc.
PROJECT : ZRA
Charger(ISL88731A)
Size
Document Number
Rev 1A
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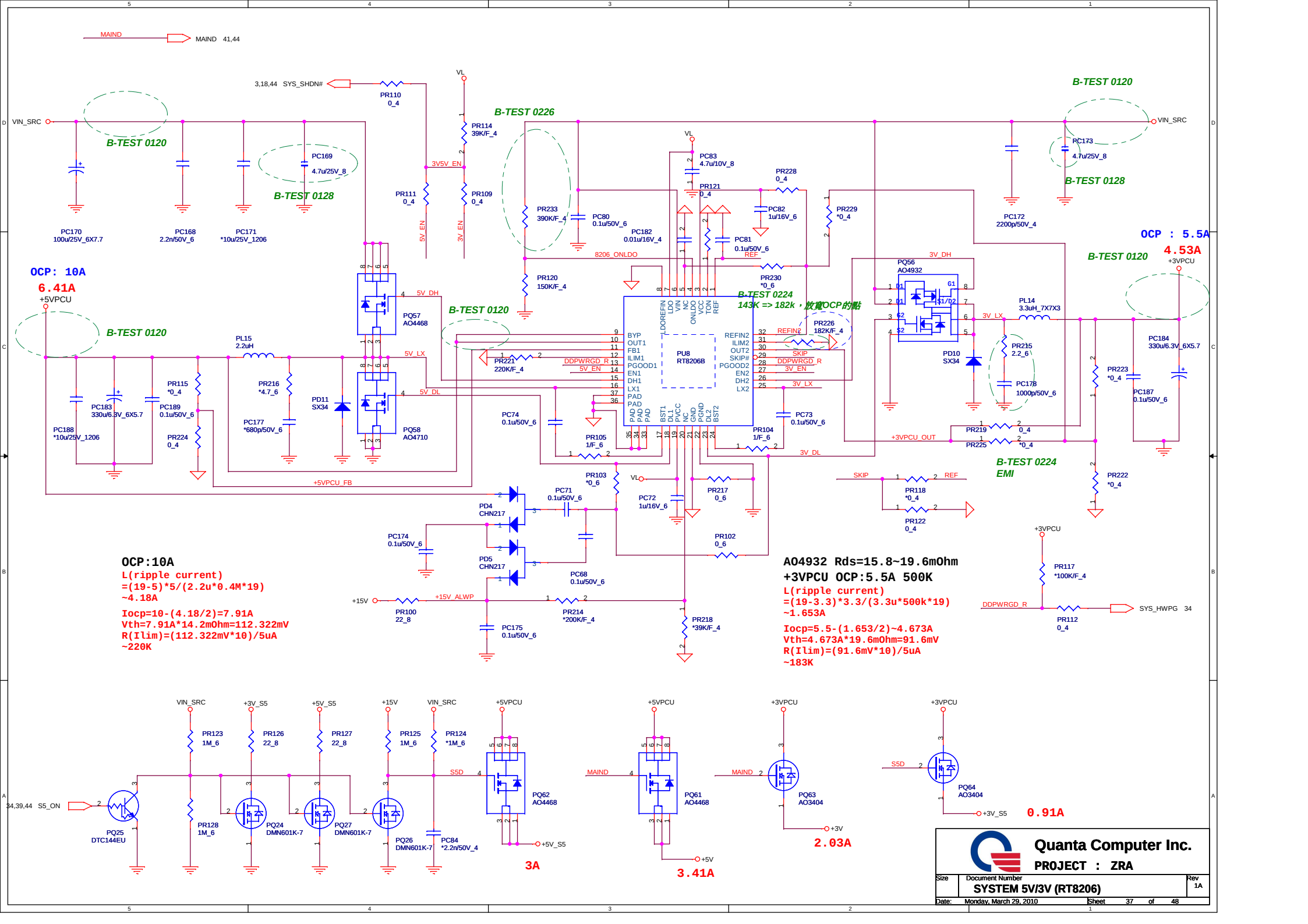
MAIND
MAIND 41,44
3,18,44 SYS_SHDN#
VIN_SRC
VL
PR110 0_4
PR114 39K/F_4
PR109 0_4
PR111 0_4
3V5V_EN
5V_EN
3V_EN
B-TEST 0226
B-TEST 0120
B-TEST 0128
PC169 4.7u/25V_8
PC170 100u/25V_6X7.7
PC168 2.2n/50V_6
PC171 *10u/25V_1206
PR233 390K/F_4
PC80 0.1u/50V_6
PC182 0.01u/16V_4
PC83 4.7u/10V_8
PR121 0_4
PR228 0_4
PC82 1u/16V_6
PC81 0.1u/50V_6
PR229 *0_4
PR230 *0_6
REF
8206_ONLDO
PR120 150K/F_4
B-TEST 0224
143K => 182k，放寬OCP的點
PR226 182K/F_4
REFIN2
SKIP
DDPWRGD_R
3V_EN
3V_LX
PR221 220K/F_4
PU8 RT8206B
LDOREFIN LDO VIN NC ONLDO VOO TON REF
BYP OUT1 FB1 ILIM1 PGOOD1 EN1 DH1 LX1 PAD PAD
REFIN2 ILIM2 OUT2 SKIP# PGOOD2 EN2 DH2 LX2
BST1 DL1 PVCC NC GND PGND DL2 BST2
PC74 0.1u/50V_6
PR105 1/F_6
PR104 1/F_6
PC73 0.1u/50V_6
3V_DL
PR103 *0_6
PC71 0.1u/50V_6
PC72 1u/16V_6
PR217 0_6
PR102 0_6
PD4 CHN217
PD5 CHN217
PC174 0.1u/50V_6
PC68 0.1u/50V_6
PC175 0.1u/50V_6
PR218 *39K/F_4
+15V
+15V_ALWP
PR100 22_8
PR214 *200K/F_4
PQ56 AO4932
PD10 SX34
PL14 3.3uH_7X7X3
PR215 2.2_6
PC178 1000p/50V_6
PR219 0_4
PR225 *0_4
+3VPCU_OUT
PR223 *0_4
PR222 *0_4
PC184 330u/6.3V_6X5.7
PC187 0.1u/50V_6
PR118 *0_4
PR122 0_4
B-TEST 0224
EMI
PR117 *100K/F_4
PR112 0_4
SYS_HWPG 34
PC172 2200p/50V_4
PC173 4.7u/25V_8
OCP : 5.5A
4.53A
OCP: 10A
6.41A
+5VPCU
+3VPCU
PL15 2.2uH
PR115 *0_4
PR216 *4.7_6
PR224 0_4
PC183 330u/6.3V_6X5.7
PC189 0.1u/50V_6
PC188 *10u/25V_1206
PC177 *680p/50V_6
PD11 SX34
PQ57 AO4468
PQ58 AO4710
5V_DH
5V_LX
5V_DL
+5VPCU_FB
OCP:10A
L(ripple current)
=(19-5)*5/(2.2u*0.4M*19)
~4.18A
Iocp=10-(4.18/2)=7.91A
Vth=7.91A*14.2mOhm=112.322mV
R(Ilim)=(112.322mV*10)/5uA
~220K
AO4932 Rds=15.8~19.6mOhm
+3VPCU OCP:5.5A 500K
L(ripple current)
=(19-3.3)*3.3/(3.3u*500k*19)
~1.653A
Iocp=5.5-(1.653/2)~4.673A
Vth=4.673A*19.6mOhm=91.6mV
R(Ilim)=(91.6mV*10)/5uA
~183K
VIN_SRC
+3V_S5
+5V_S5
+15V
PR123 1M_6
PR126 22_8
PR127 22_8
PR125 1M_6
PR124 *1M_6
S5D
34,39,44 S5_ON
PQ25 DTC144EU
PR128 1M_6
PQ24 DMN601K-7
PQ27 DMN601K-7
PQ26 DMN601K-7
PC84 *2.2n/50V_4
PQ62 AO4468
+5V_S5
3A
+5VPCU
MAIND
PQ61 AO4468
+5V
3.41A
+3VPCU
PQ63 AO3404
+3V
2.03A
PQ64 AO3404
+3V_S5
0.91A
Quanta Computer Inc.
PROJECT : ZRA
Size
Document Number
SYSTEM 5V/3V (RT8206)
Rev 1A
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OFS/VFIXEN	Offset & Droop	SVI	VFIX
GND	O	O	X
+3.3V	X	X	O
+5V	X	O	X

Metal VID Codes

SVC	SVD	Output
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8

3A

15A

15A

Pin 49 is GND Pin

Parallel

Close to CPU socket

Close to CPU socket

B-TEST 0120

B-TEST 0128

B-TEST 0224 EMI

B-TEST 0225

PU13 ISL6265A

Quanta Computer Inc.	
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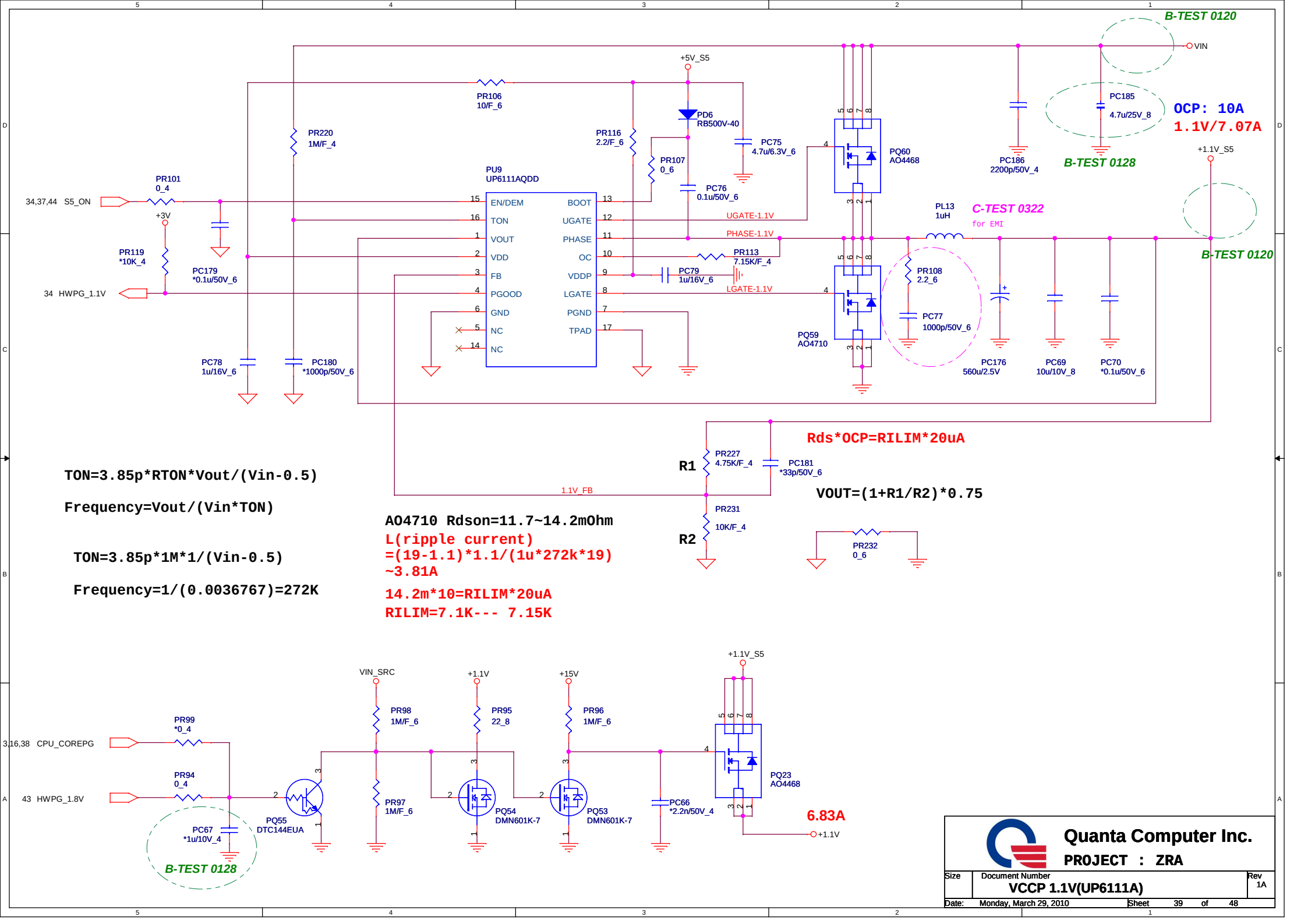
B-TEST 0120
VIN
+5V_S5
PR106
10/F_6
PD6
RB500V-40
PR220
1M/F_4
PR116
2.2/F_6
PC75
4.7u/6.3V_6
PR107
0_6
PC76
0.1u/50V_6
PU9
UP6111AQDD
PQ60
AO4468
PC185
4.7u/25V_8
OCP: 10A
1.1V/7.07A
PC186
2200p/50V_4
B-TEST 0128
+1.1V_S5
PR101
0_4
34,37,44 S5_ON
+3V
PR119
*10K_4
PC179
*0.1u/50V_6
34 HWPG_1.1V
EN/DEM
TON
VOUT
VDD
FB
PGOOD
GND
NC
NC
BOOT
UGATE
PHASE
OC
VDDP
LGATE
PGND
TPAD
UGATE-1.1V
PHASE-1.1V
LGATE-1.1V
PR113
7.15K/F_4
PC79
1u/16V_6
PL13
1uH
C-TEST 0322
for EMI
PR108
2.2_6
PC77
1000p/50V_6
PQ59
AO4710
PC176
560u/2.5V
PC69
10u/10V_8
PC70
*0.1u/50V_6
B-TEST 0120
PC78
1u/16V_6
PC180
*1000p/50V_6
Rds*OCP=RILIM*20uA
R1
PR227
4.75K/F_4
PC181
*33p/50V_6
1.1V_FB
VOUT=(1+R1/R2)*0.75
PR231
10K/F_4
R2
PR232
0_6
TON=3.85p*RTON*Vout/(Vin-0.5)
Frequency=Vout/(Vin*TON)
TON=3.85p*1M*1/(Vin-0.5)
Frequency=1/(0.0036767)=272K
AO4710 Rdson=11.7~14.2mOhm
L(ripple current)
=(19-1.1)*1.1/(1u*272k*19)
~3.81A
14.2m*10=RILIM*20uA
RILIM=7.1K--- 7.15K
VIN_SRC
+1.1V
+15V
+1.1V_S5
PR99
*0_4
3,16,38 CPU_COREPG
PR94
0_4
43 HWPG_1.8V
PR98
1M/F_6
PR95
22_8
PR96
1M/F_6
PQ55
DTC144EUA
PR97
1M/F_6
PQ54
DMN601K-7
PQ53
DMN601K-7
PC66
*2.2n/50V_4
PQ23
AO4468
PC67
*1u/10V_4
B-TEST 0128
6.83A
+1.1V
Quanta Computer Inc.
PROJECT : ZRA
Size
Document Number
VCCP 1.1V(UP6111A)
Rev
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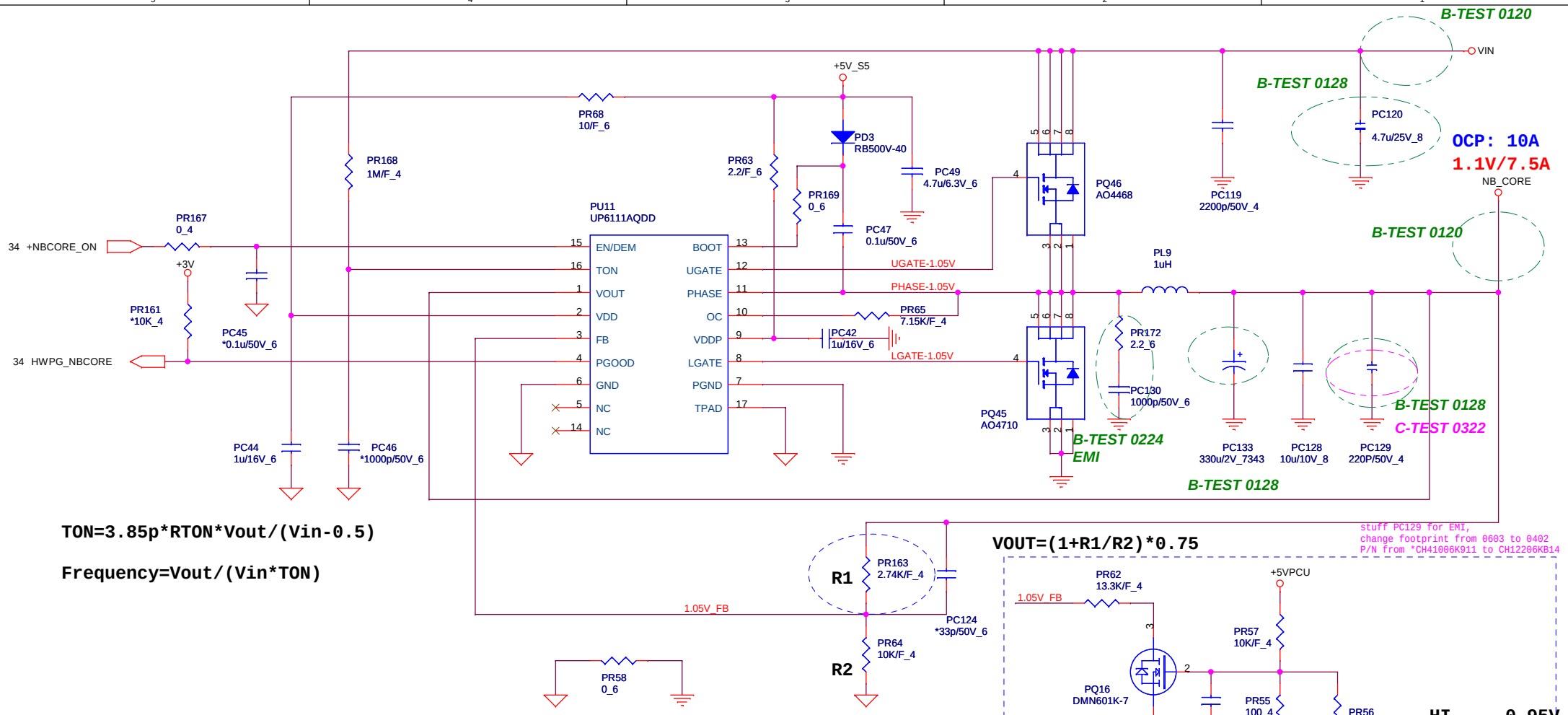

Quanta Computer Inc.

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Size	Document Number	Rev
	NB_CORE(UP6111A)	1A
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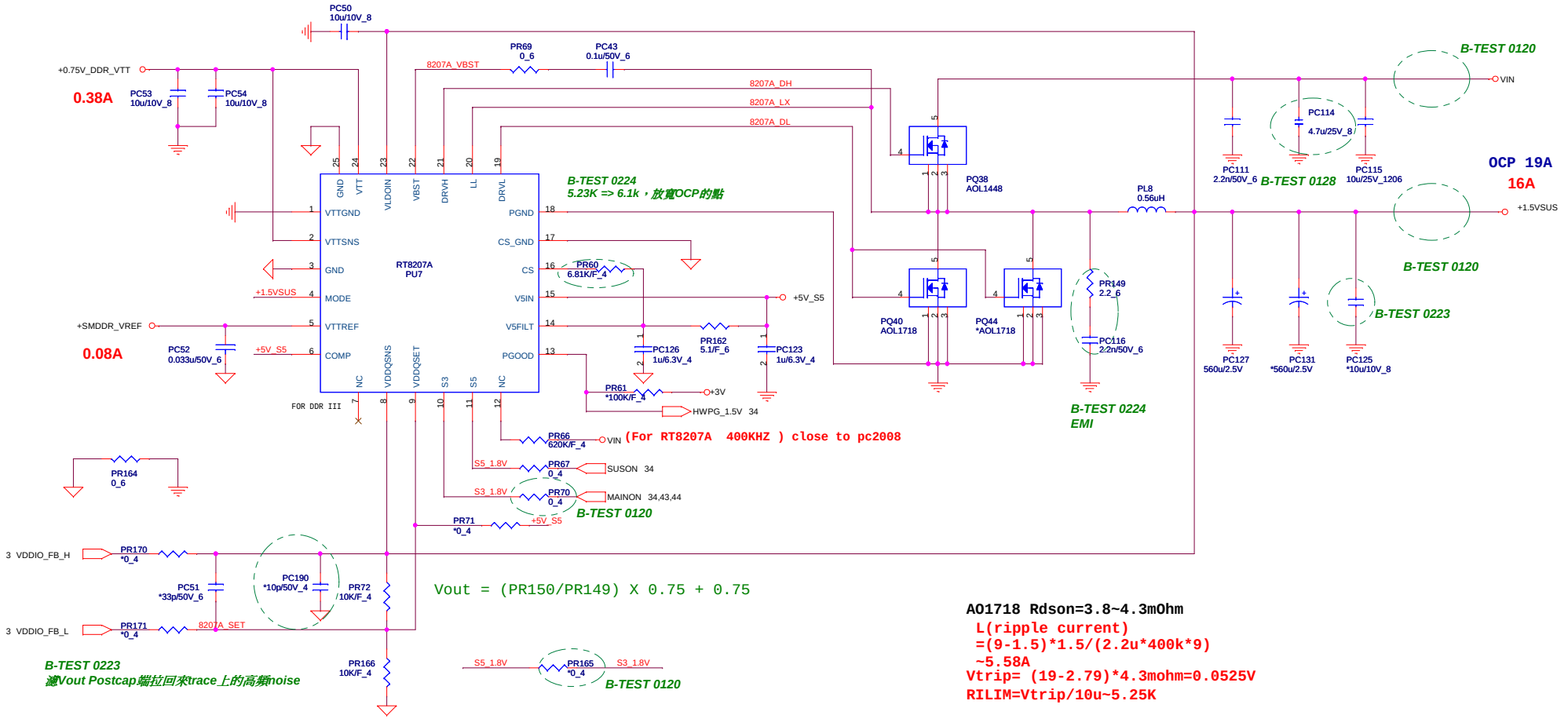
[PWM]



	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

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Size	Document Number	Rev
	DDR 1.5V(TPS51116)	1A

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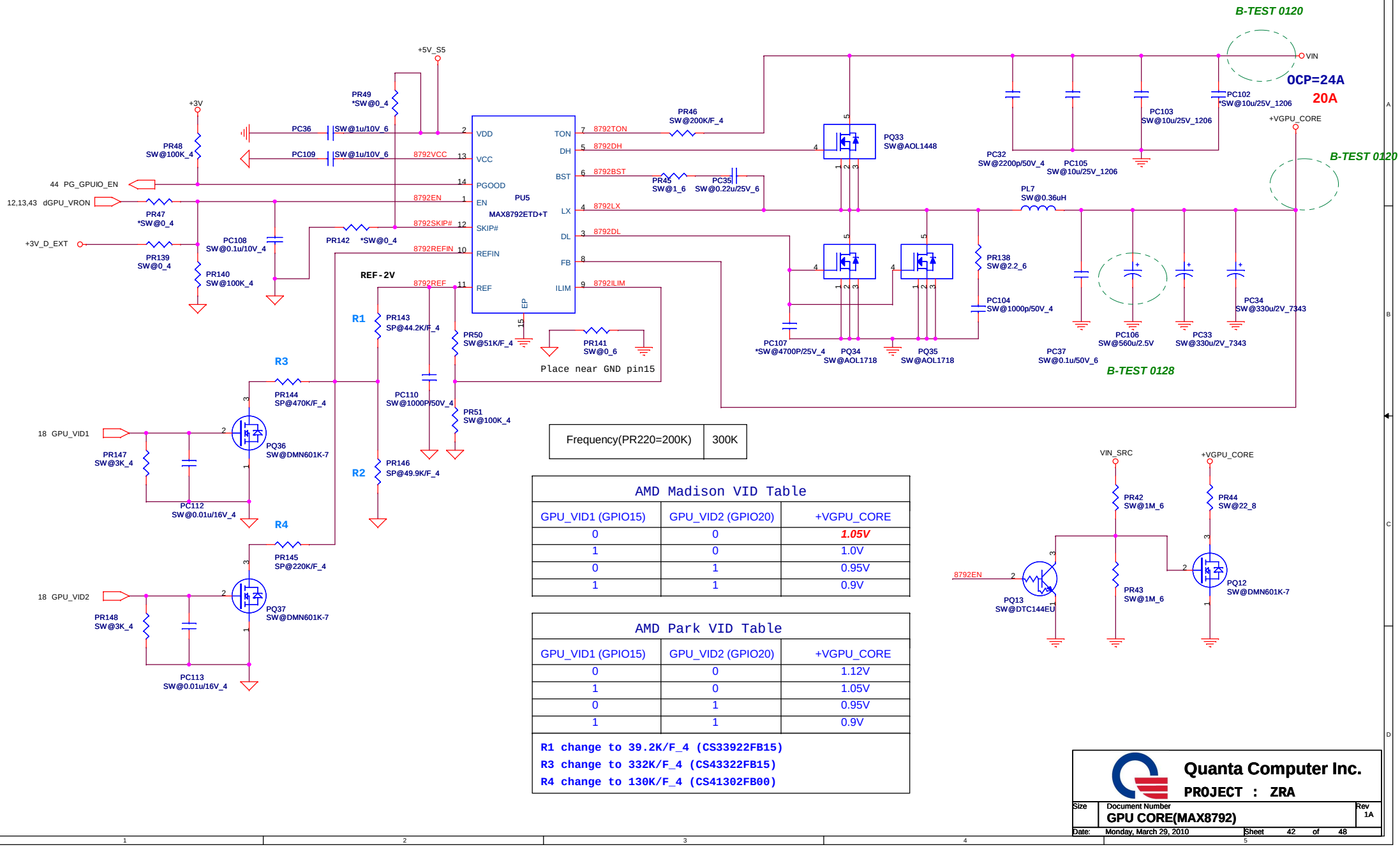

Frequency(PR220=200K)	300K

AMD Madison VID Table

GPU_VID1 (GPIO15)	GPU_VID2 (GPIO20)	+VGPU_CORE
0	0	***1.05V***
1	0	1.0V
0	1	0.95V
1	1	0.9V

AMD Park VID Table

GPU_VID1 (GPIO15)	GPU_VID2 (GPIO20)	+VGPU_CORE
0	0	1.12V
1	0	1.05V
0	1	0.95V
1	1	0.9V

R1 change to 39.2K/F_4 (CS33922FB15)
R3 change to 332K/F_4 (CS43322FB15)
R4 change to 130K/F_4 (CS41302FB00)

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	GPU CORE(MAX8792)	1A
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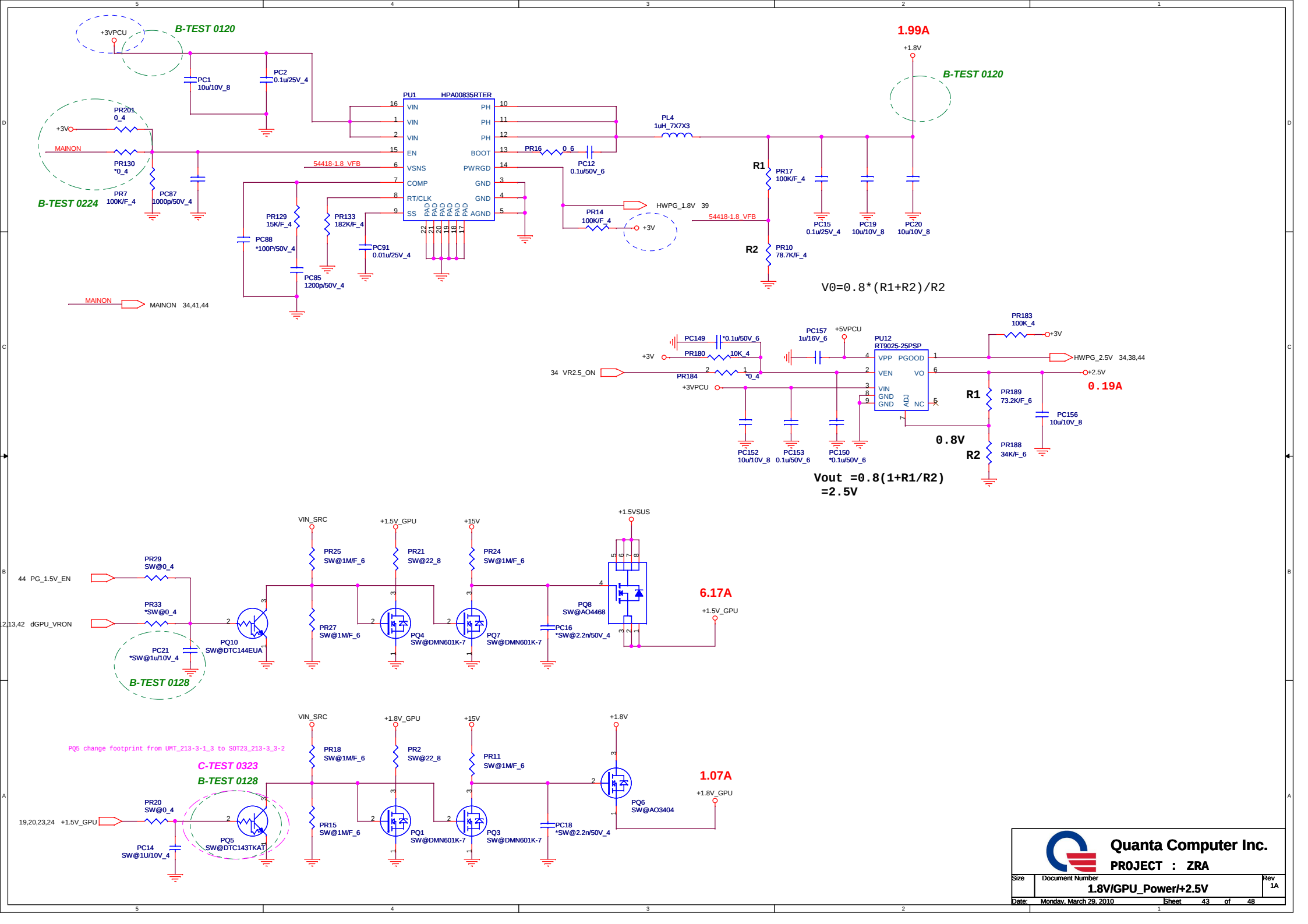
B-TEST 0120
+3VPCU
PC1
10u/10V_8
PC2
0.1u/25V_4
PR201
0_4
+3V
MAINON
PR130
*0_4
PR7
100K/F_4
PC87
1000p/50V_4
B-TEST 0224
PU1
HPA00835RTER
VIN
EN
VSNS
COMP
RT/CLK
SS
PH
BOOT
PWRGD
GND
AGND
PAD
54418-1.8_VFB
PR129
15K/F_4
PR133
182K/F_4
PC88
*100P/50V_4
PC85
1200p/50V_4
PC91
0.01u/25V_4
PR16
0_6
PC12
0.1u/50V_6
PL4
1uH_7X7X3
PR14
100K/F_4
HWPG_1.8V 39
MAINON 34,41,44
1.99A
+1.8V
B-TEST 0120
R1
PR17
100K/F_4
R2
PR10
78.7K/F_4
PC15
0.1u/25V_4
PC19
10u/10V_8
PC20
10u/10V_8
V0=0.8*(R1+R2)/R2
PR183
100K_4
PC149
*0.1u/50V_6
PR180
10K_4
PR184
*0_4
34 VR2.5_ON
PC157
1u/16V_6
+5VPCU
PU12
RT9025-25PSP
VPP
VEN
VIN
GND
PGOOD
VO
ADJ
NC
HWPG_2.5V 34,38,44
+2.5V
0.19A
PR189
73.2K/F_6
PC156
10u/10V_8
0.8V
PR188
34K/F_6
PC152
10u/10V_8
PC153
0.1u/50V_6
PC150
*0.1u/50V_6
Vout =0.8(1+R1/R2)
=2.5V
VIN_SRC
+1.5V_GPU
+15V
+1.5VSUS
PR29
SW@0_4
44 PG_1.5V_EN
PR33
*SW@0_4
2,13,42 dGPU_VRON
PC21
*SW@1u/10V_4
PQ10
SW@DTC144EUA
PR25
SW@1M/F_6
PR27
SW@1M/F_6
PR21
SW@22_8
PQ4
SW@DMN601K-7
PR24
SW@1M/F_6
PQ7
SW@DMN601K-7
PQ8
SW@AO4468
PC16
*SW@2.2n/50V_4
6.17A
+1.5V_GPU
B-TEST 0128
PQ5 change footprint from UMT_213-3-1_3 to SOT23_213-3_3-2
C-TEST 0323
B-TEST 0128
VIN_SRC
+1.8V_GPU
+15V
+1.8V
PR18
SW@1M/F_6
PR20
SW@0_4
19,20,23,24 +1.5V_GPU
PC14
SW@1U/10V_4
PQ5
SW@DTC143TKAT
PR15
SW@1M/F_6
PR2
SW@22_8
PQ1
SW@DMN601K-7
PR11
SW@1M/F_6
PQ3
SW@DMN601K-7
PQ6
SW@AO3404
PC18
*SW@2.2n/50V_4
1.07A
+1.8V_GPU
Quanta Computer Inc.
PROJECT : ZRA
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1.8V/GPU_Power/+2.5V
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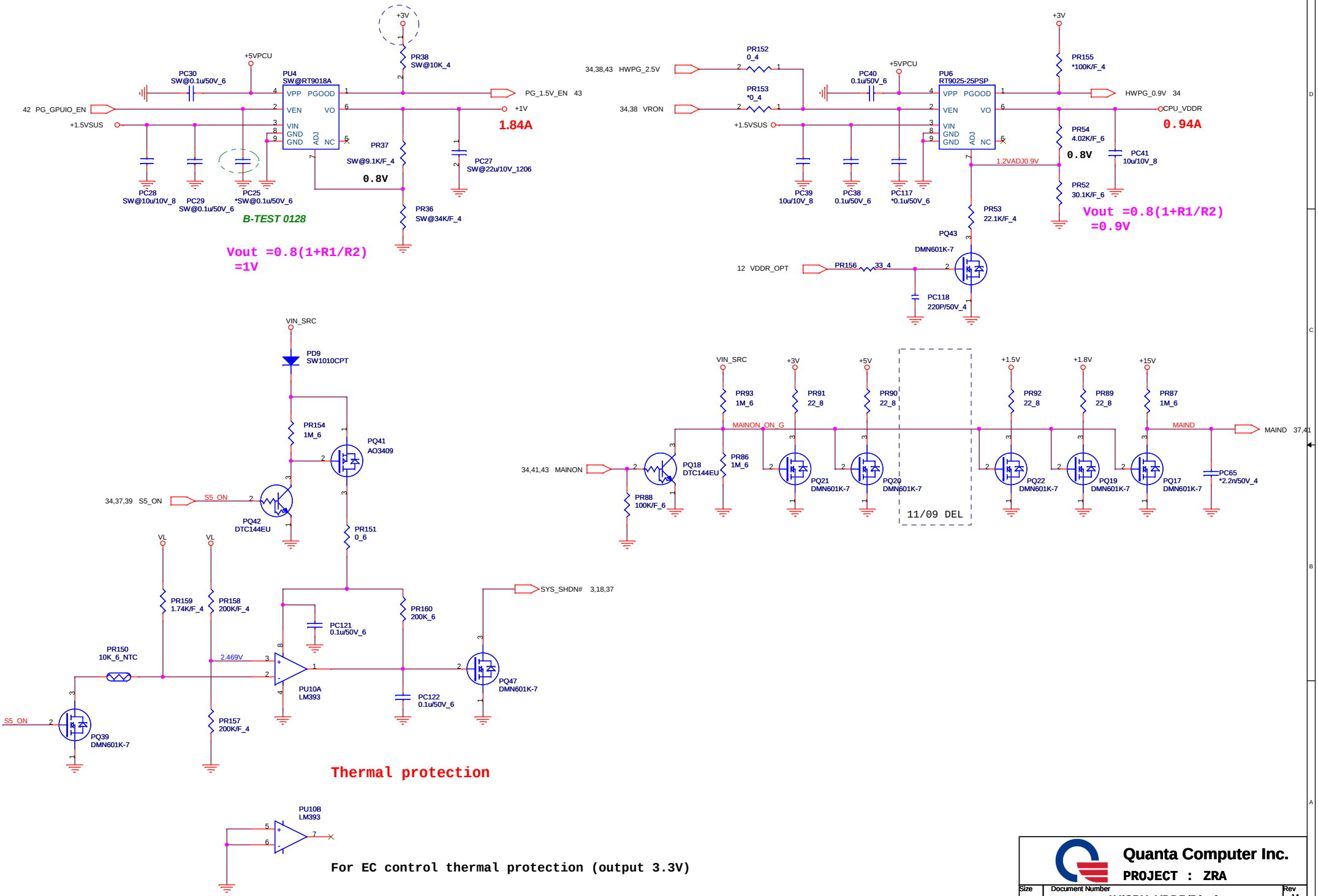

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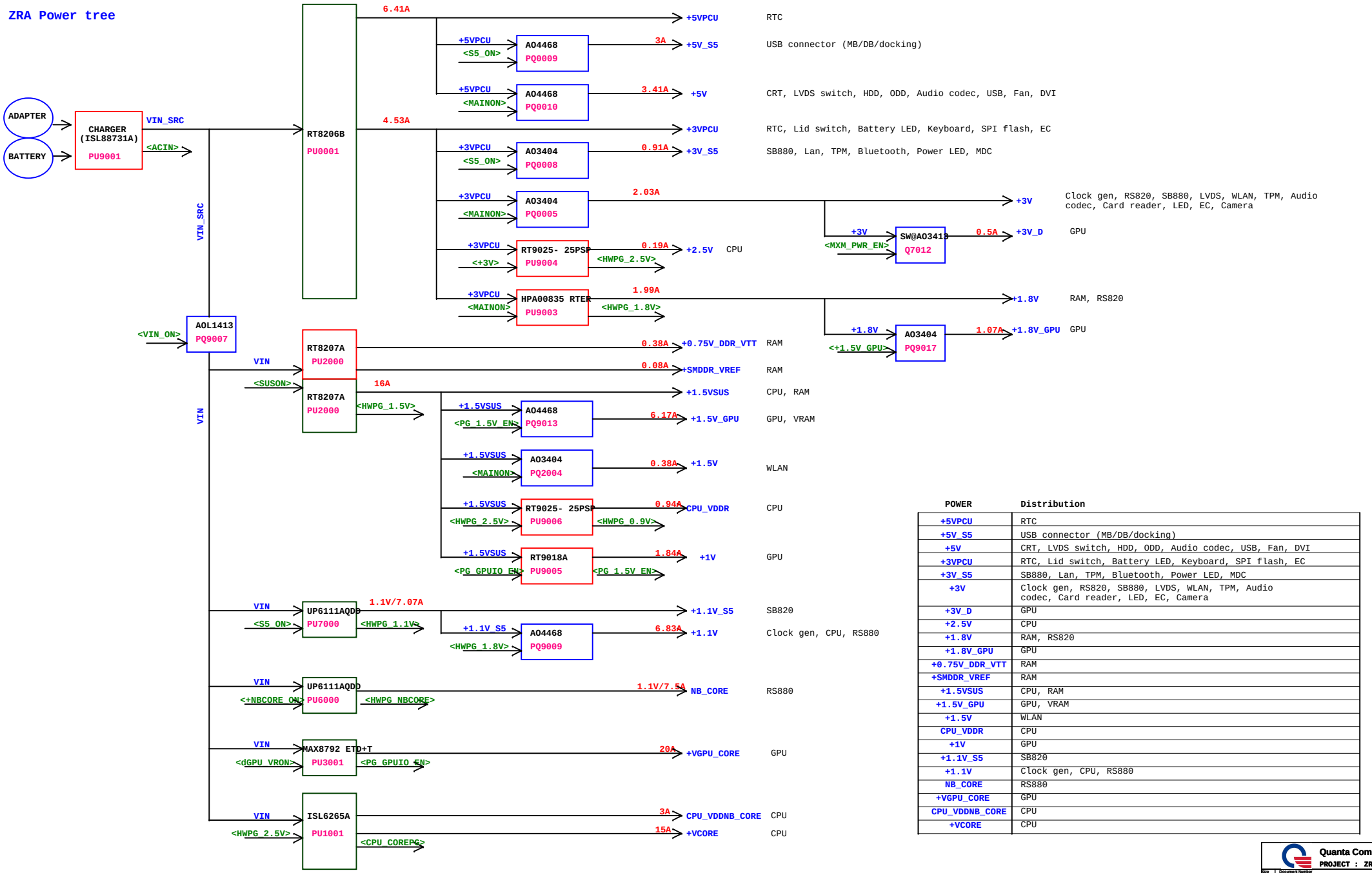
ZRA Power tree



POWER	Distribution
+5VPCU	RTC
+5V_S5	USB connector (MB/DB/docking)
+5V	CRT, LVDS switch, HDD, ODD, Audio codec, USB, Fan, DVI
+3VPCU	RTC, Lid switch, Battery LED, Keyboard, SPI flash, EC
+3V_S5	SB880, Lan, TPM, Bluetooth, Power LED, MDC
+3V	Clock gen, RS820, SB880, LVDS, WLAN, TPM, Audio codec, Card reader, LED, EC, Camera
+3V_D	GPU
+2.5V	CPU
+1.8V	RAM, RS820
+1.8V_GPU	GPU
+0.75V_DDR_VTT	RAM
+SMDDR_VREF	RAM
+1.5VSUS	CPU, RAM
+1.5V_GPU	GPU, VRAM
+1.5V	WLAN
CPU_VDDR	CPU
+1V	GPU
+1.1V_S5	SB820
+1.1V	Clock gen, CPU, RS880
NB_CORE	RS880
+VGPU_CORE	GPU
CPU_VDDNB_CORE	CPU
+VCORE	CPU

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Model	REV	DATE	CHANGE LIST	NOTE
ZRA	A1A	11/24	1.Change Hole31___P29(unguard hole) 2.Change CN9009___P32(ME modify T/B connector from 6pin to12 pin) 3.Del R7528、R7529___P28(for all acer project in 2010=>short the WLAN_LED and WWAN_LED)	ECN Release
		11/25	1.Add power tree___P46 2.Change CN7019 footprint___P29(NEW=>sata-c166h2-12204-l-22p-r) 3.Change PC9064、PR9021、PR9025 P/N___P37(PC9064=>CH5104K1900、PR9021=>CS41502JB10、PR9025=>CS33902JB01) 4.Stuff R7118、R7115___P11 (for NB REV:11 use) 5.Exchange R7105、C7228___P20(refence AMD design) 6.Del U7033A PINAA4 funcyion___P13(refence AMD design) 7.Rename U7033A PINAJ6 net name___P13(refence AMD design, change from PG_GPUIO_ENA to dGPU_PWROK)	
		11/26	1.Change R7029___P20(AMD suggest change from 1k to 10k) 2.no stuff R7060___P19 3.Change R7061、R7070、R7032___P18(AMD suggest change from 1k to 10k) 4.Change R7108、R9038___P18(AMD suggest change from 1k to 0R) 5.no stuff R7029___P20 6.Change GPU_VID1 net___P19(change from U7022B PIN AK14 to AM13) 7.Change GPU_VID2 net___P19(change from U7022B PIN AM13 to AL13) 8.Modify Board ID schematic___P13、P15(follow ZR8_B) 9.Add LED4、R9252、RV5___P33(SATA LED movie from DB to MB)	
		11/27	1.Change R9629 footprint___P28(from 0603 to 0402) 2.Change CN7022 H___P28(from H=5.6 to H=7) 3.Change PJ2 battery footprint___P37(new => bat-bhp-08afeb-8p-l-v) 4.Change PR3013、PR3017、PR3010 value___P43	
		12/01	1.Change L7031、L7060、L7026、L7035、L7032、L7061、L7021、L7033 value___P28(change to PBY160808T-221Y-N) 2.Modify Power tree	
		12/03	1.Change L9000 footprint___P27(from 0806 to 0805) 2.Change CN9007 P/N___P30(from DFHD12MS788 to DFHD12MS621)	
		12/08	1.Change C7343 value_P6(from 1000P to 2200P) 2.Change C9098、C9119、C9120、C9121、C9122、C9123 value_P34(from 0.1u/10V to 0.1u/25V) 3.Change R7437 value_P11(from 140 ohm to 133ohm ==> AMD suggest use docking need matching 133 ohm)	
		12/09	1.Change C7063 value_P21(from SPE@ to SW@) 2.Change C7404 value_P23(from SPE@ to SP@) 2.Add R9253 _P33	
		12/11	1.rename 2.Change PC24 P/N _P37(from CH5104K1900 to CH5104K9906) 3.Change PC55、PC56、PC57、PC58、PC139、PC140 P/N _P6/P39(from CH733RM8802 to CH733RY8802) 4.Change PL11 P/N _P39(from DC+18V0MZ04 to CV+18V0MZ04) 5.Change LED2 footprint _P33(change to ledltst-s326kgjskt-3p-nb4)	
		12/15	1.Change CN6 P/N _P32(from DFFC04FR014 to DFFC04FR018) 2.DEL R384、LED6、RV7 _P33(DEL BLUETOOTH LED function) 3.Add T100 _P33	
		12/16	1.Add Hole NUT P/N _P32 2.DEL CN20 PIN73/PIN74 _P36(change from GND to NA)	
	B1A	12/28	1.Modify power sequence_P2 2.Modify power tree_P46	
		01/20	1.Del JP15、JP16、JP20、JP21__P37 2.Del JP14、JP13、JP12、RP201、RP213、RP209、RP210__P38 3.no stuff PC141___P38 4.Change PL12 P/N to CV-2280MZ05、footprint to CHOKE-PCMC063T-3R3MN-smt___P38 5.Change PC154 and PC138 P/N to CC71004MZ01 and Value from 27uF to 100uF___P38 6.Del JP19、JP17、JP18__P39 7.Del JP7、JP8、JP10__P40 8.Del JP6、JP9、JP11__P41 9.no stuff PR165___P41 10.stuff PR70___P41 11.Del JP3、JP4、JP5__P42 12.Del JP2、JP1__P43	

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Model	REV	DATE	CHANGE LIST	NOTE
ZRA	B1A	01/28	1.Change Q9 P/N to BAM700200F6___P20 2.Change PC17 footprint to 0603 ___P36 3.Change PC11 Value from 10uF to 4.7uF，footprint form 1206 to 0805，P/N from CH61004M291 to CH5474KEA06 ___P36 4.Change PC169、PC173 Value from 10uF to 4.7uF，footprint form 1206 to 0805，P/N from CH61004M291 to CH5474KEA06 ___P37 5.Change PC158、PC62、PC142、PC143、PC135、PC136 Value from 10uF to 4.7uF，footprint form 1206 to 0805，P/N from CH61004M291 to CH5474KEA06 ___P38 6.Change PC185 Value from 10uF to 4.7uF，footprint form 1206 to 0805，P/N from CH61004M291 to CH5474KEA06 ___P39 7.no stuff PC67___P39 8.Change PC120 Value from 10uF to 4.7uF，footprint form 1206 to 0805，P/N from CH61004M291 to CH5474KEA06 ___P40 9.no stuff PC129___P40 10.Change PC114 Value from 10uF to 4.7uF，footprint form 1206 to 0805，P/N from CH61004M291 to CH5474KEA06 ___P41 11.no stuff PC21___P43 12.no stuff PC25___P44 13.Change PQ5 P/N from BA144EUAZ04 to BA001430Z31___P43 14.Change PC133 Value from 560uF to 330uF，footprint form ECAP6_3X6_1-7_2 to CC7343，P/N from CC7560JMZ15 to CH733RY8802 ___P40 15.Change PC106 Value from 560uF to 330uF，footprint form ECAP6_3X6_1-7_2 to CC7343，P/N from CC7560JMZ15 to CH733RY8802 ___P42 16.no stuff R148、R144___P10 17.Del Clock Generator ___P3 18.Del R166、R163、R162、R165、RP21 ___P10 19.Del RP26、RP14、RP13、RP27、RP33、RP30、RP29 ___P12 20.Del R274、R297 ___P13 21.Change R289 from 100K to 10K ___P13 22.Change C687、C686 from 18P to 27P ___P18 23.no stuff R428、R429___P22 24.Modify DDR3 Memory Aperture size table___P22 25.Add F1___P25 26.Change L32、L38、L40 from BLM18BA470SN1 to BLM18BA220SN1D ___P25 27.Change R80 from 1.24K to 1.21K ___P26 28.Change U14 footprint to soic8-8-1_27-at45db011d___P26 29.Change R60 from 100K to 10K ___P26 30.Del R2 ___P26 31.Del R593 ___P27 32.Modify CN16 schematic ___P30 33.Change D10 P/N to BCRB500VZ29___P34 34.Change CN20 footprint to DOCK-SP07-10207-19-64P-H-SMT___P35	ECN Release
		01/29	1.Change C797、C798 from 22P to 27P ___P12 2.Change CN13 footprint to rj45-130452-g-12p-v，P/N to DFTJ12FR154___P26 3.Change C843、C846 from 12P to 18P ___P27 4.Change U35 PIN21 netname to LPC_CLK0___P27	
		02/01	1.Add R162___P12 2.Del R90 ___P17 3.no stuff R76、R83、R91、R45___P17 4.Add C494、U34___P25 5.Add CN27___P29 6.Del L43、L45、L81、L82、L66、L67___P29 7.stuff R225、Q17 (Del IV)___P35 8.Add CN28、L91、L92、L93、L83、L84、L88、C785、C786___P35 9.Modify CN20 netname___P35 10.stuff R43___P17	
		02/02	1.Add R384___P15 2.Add R554___P29	
		02/05	1.Add Q43、Q42、Q44___P5 2.Add F2、F3___P35	
		02/08	1.Modify R256 schematic to U17 PIN2___P30	
		02/10	1.change L77 P/N to CX163210007，foot print to CHOKE-WCM3216-4P___P35 2.Add C495、C498___P31 3.no stuff C441、C446、C476、C475、C478、C477___P35 4.change CN28 PIN13、PIN14 from GND to NC___P35 5.change CN27 PIN13、PIN14 from GND to NC___P29 6.Change L32、L38、L40 P/N from BLM18BA220SN1D to BLM18BA470SN1___P25 7.Change C377、C363、C351、C349、C365、C376 value from 10p to 6.8p，P/N to CH-6806TB01___P25 8.add C796、C502、C506、C522、C792、C794___P35 9.change L78、L79、L80 P/N to CX8BA470003___P35	

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Model	REV	DATE	CHANGE LIST	NOTE
ZRA	B1A	02/10	10.Add C812、C816、C817、C824、C825、C830___P29 11.Add C834___P29 12.Add C831、C837、C836、C838、C862、C863、C864、C865、C869、C870、C871___P33 13.Add C866、C867___P31 14.Change R292,R364,R367,R286,R293,R287,C610,C537 footprint to short pad__P29 15.Add C868___P33	ECN Release
		02/11	1.Add C872___P31 2.Add R90___P32	
		02/21	1.Change netname LPC_CLK1 to LPC_CLK0___P34 2.no stuff R540、R536、C782、C474、U31___P3 3.no stuff RP20___P27	
		02/23	1.Change R308、R311 from 5.1R to 39R___P29 2.Change R71 from 0 ohm to 4.7k ohm and not stuff R71___P20 3.Change L78、L79、L80 from BEAD 47R TO 0R___P35 4.Change L91、L88、L92、L93、L84、L83 from BEAD 120R TO 0R___P35 5.No stuff R262、R257、Y3、C496、C497，and stuff R261、R256___P30 6.stuff R292、R364、R367、R286、R293、R287、C610、C537 to 0R___P29 7.ADD PC190 10pF___P41 8.No stuff PC125___P41 9.change PR226 from 143K => 182k，放寬OCP的點___P37 10.change PR60 from 5.23K => 6.1k，放寬OCP的點___P41 11.change R339、R340 to L66、L67，and change value from 0R to BEAD___P29	
		02/25	1.No stuff PR178___P41 2.change R130 from 2.2K => 300R， Accord with LDT riss time SPEC___P10 3.change U15 P/N from AL003257K28 to ALBT3257K18___P25	
		02/26	1.NO stuff R331（不分BAP/BXP）___P12	
		03/22	1.change R175 0ohm to bead(CX8PG221003) and C339 from 0.1uF to 2.2uF(CH52201K991), for monitor noise issue.___P10	

Quanta Computer Inc.

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