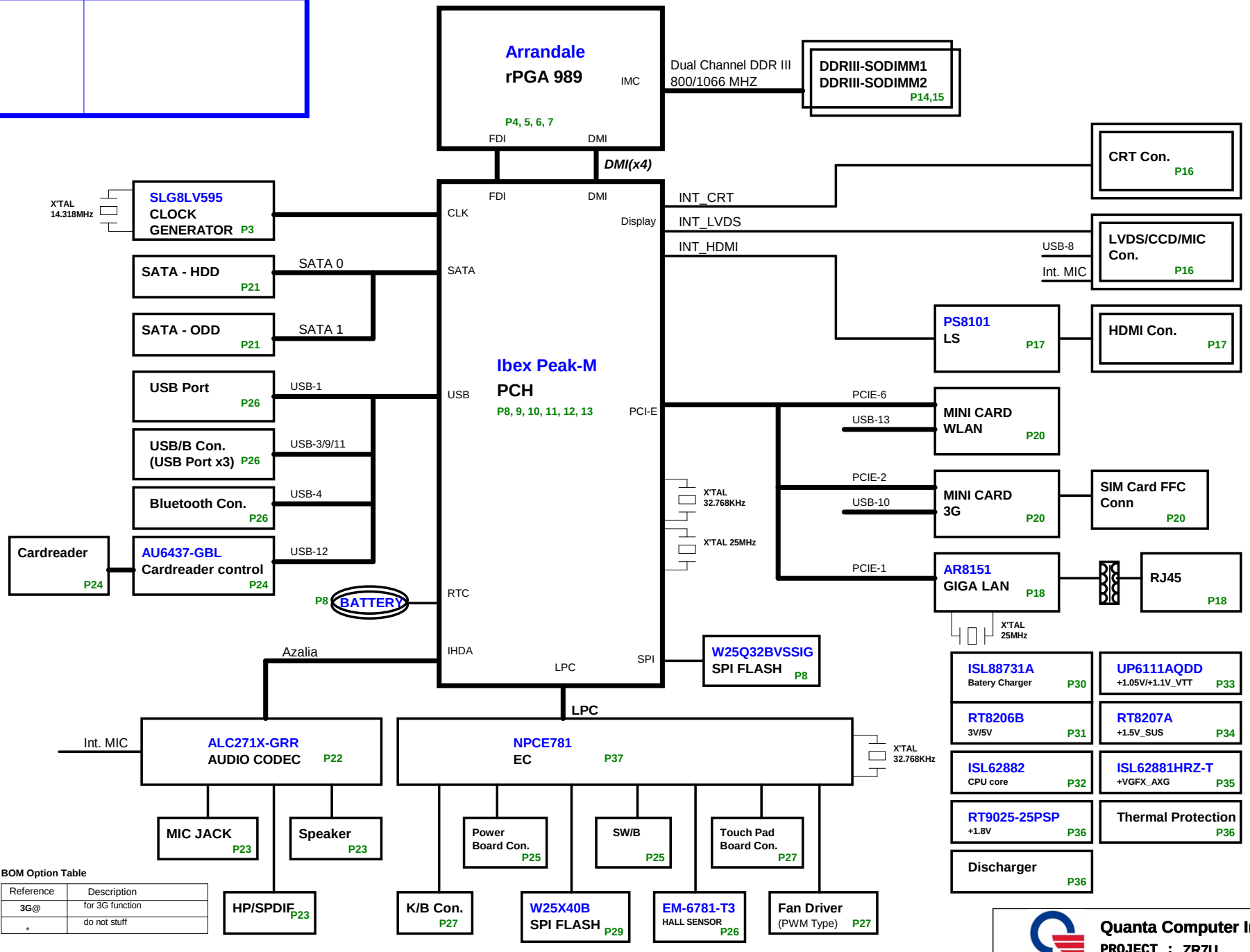
VER : 1A

| BOM P/N | Description |
|---|---|
| | |

# ZR7U SYSTEM BLOCK DIAGRAM




**BOM Option Table**

| Reference | Description |
|---|---|
| 3G@ | for 3G function |
| * | do not stuff |

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|---|---|---|
| | Block Diagram | 1A |

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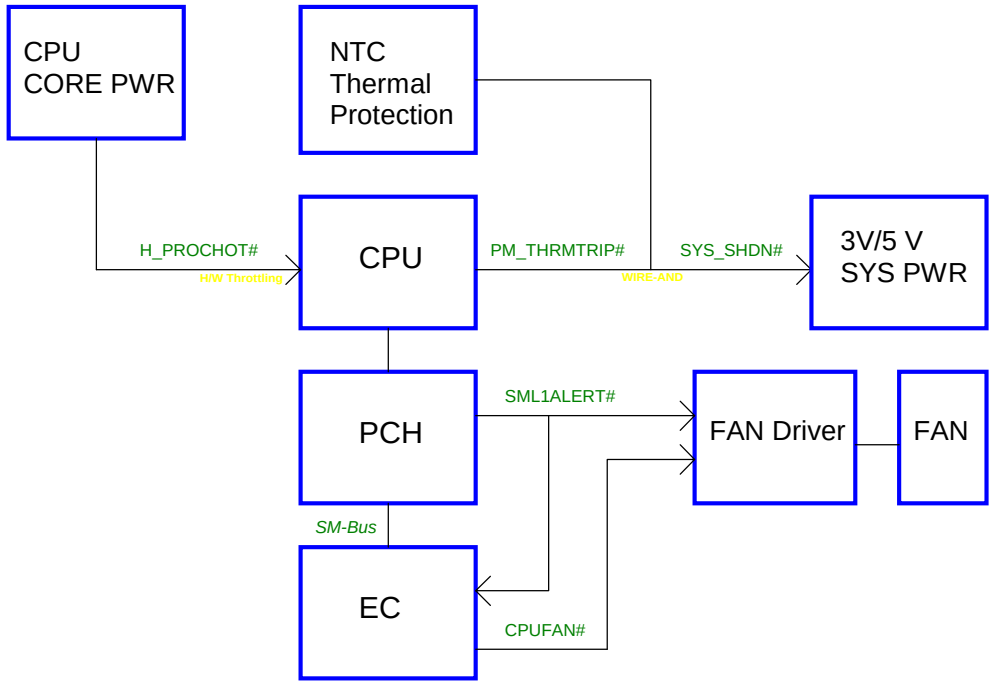
## Power States

| POWER PLANE | VOLTAGE | DESCRIPTION | CONTROL SIGNAL | ACTIVE IN |
|---|---|---|---|---|
| VIN | +10V~+19V | MAIN POWER | ALWAYS | ALWAYS |
| +VCCRTC | +3V~+3.3V | RTC POWER | ALWAYS | ALWAYS |
| +3VPCU | +3.3V | EC POWER | ALWAYS | ALWAYS |
| +5VPCU | +5V | CHARGE POWER | ALWAYS | ALWAYS |
| +15V | +15V | CHARGE PUMP POWER | ALWAYS | ALWAYS |
| +3V_S5 | +3.3V | LAN/BT/CIR POWER | S5_ON | S0-S5 |
| +5V_S5 | +5V | USB POWER | S5_ON | S0-S5 |
| +5V | +5V | HDD/ODD/Codec/TP/CRT/HDMI POWER | MAINON | S0 |
| +3V | +3.3V | PCH/GPU/Peripheral component POWER | MAINON | S0 |
| +1.5VSUS | +1.5V | CPU/SODIMM CORE POWER | SUSON | S0-S3 |
| +0.75V_DDR_VTT | +0.75V | SODIMM Termination POWER | MAINON | S0 |
| +VGFX_AXG | variation | Internal GPU POWER | GFX_ON | S0 |
| +1.8V | +1.8V | CPU/PCH/Braidwood POWER | MAINON | S0 |
| +1.5V | +1.5V | MINI CARD/NEW CARD POWER | MAINON | S0 |
| +1.05V | +1.05V | PCH CORE POWER | MAINON | S0 |
| +VCC_CORE | variation | CPU CORE POWER | VRON | S0 |
| LCDVCC | +3.3V | LCD POWER | LVDS_VDDEN | S0 |
| | | | | |

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|---|---|---|
| | PWR Status & GPU PWR CRL & THRM | 1A |

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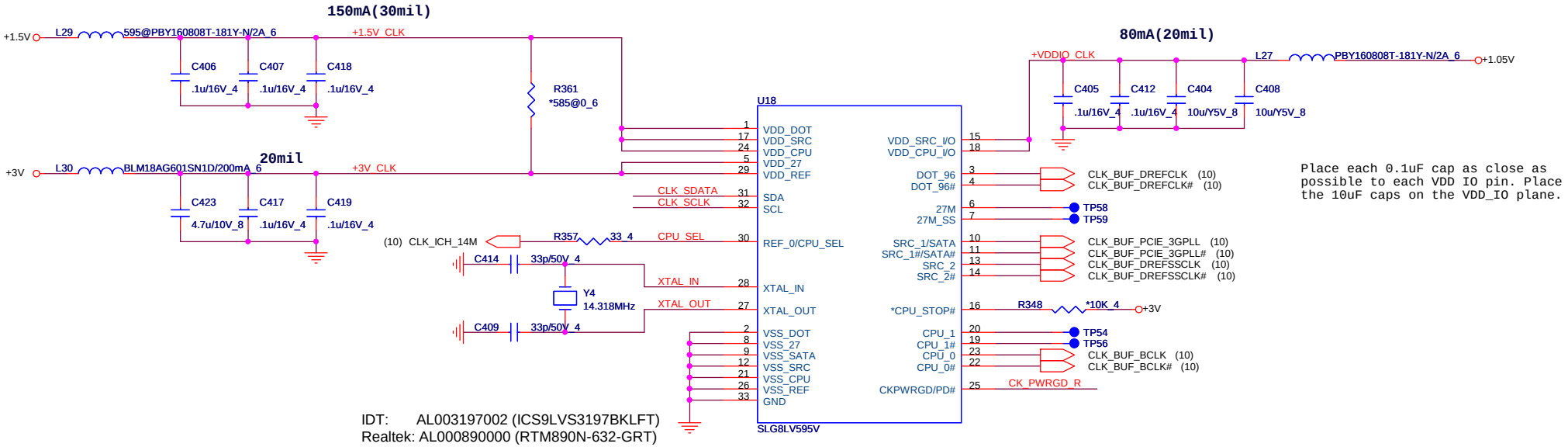
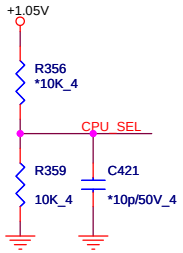



Place each 0.1uF cap as close as possible to each VDD IO pin. Place the 10uF caps on the VDD_IO plane.

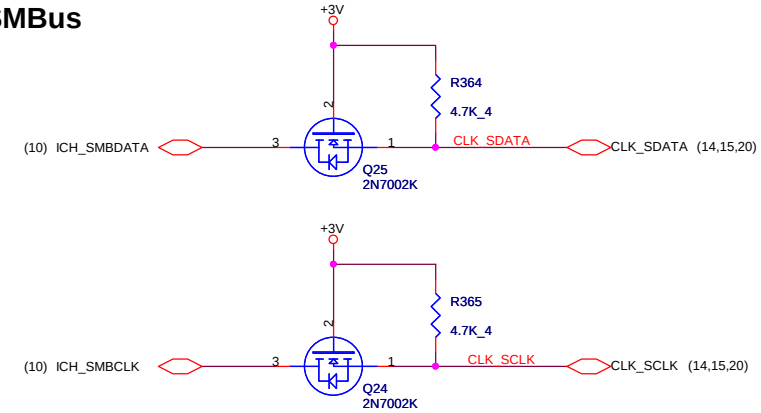
IDT: AL003197002 (ICS9LVS3197BKLFT)
Realtek: AL000890000 (RTM890N-632-GRT)
Silego: AL000595000 (SLG8LV595VTR)

## CPU_CLK select

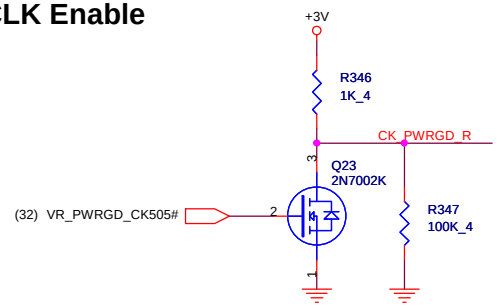



| | 0 | 1 |
|---|---|---|
| CPU_SEL | CPU0/1=133MHz (default) | CPU0/1=100MHz |

## SMBus




## CLK Enable

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| Size | Document Number | Rev |
|---|---|---|
| | Clock Generator | 1A |
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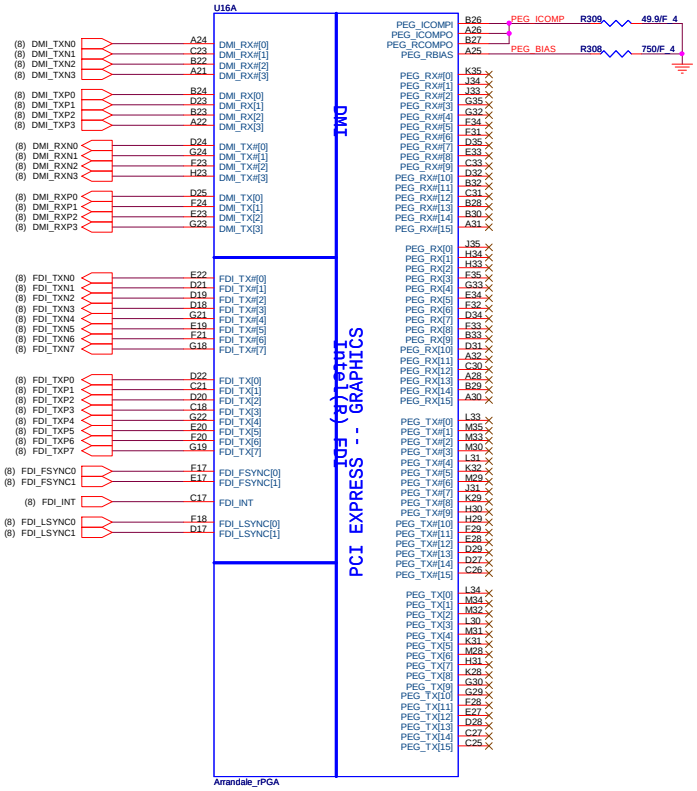
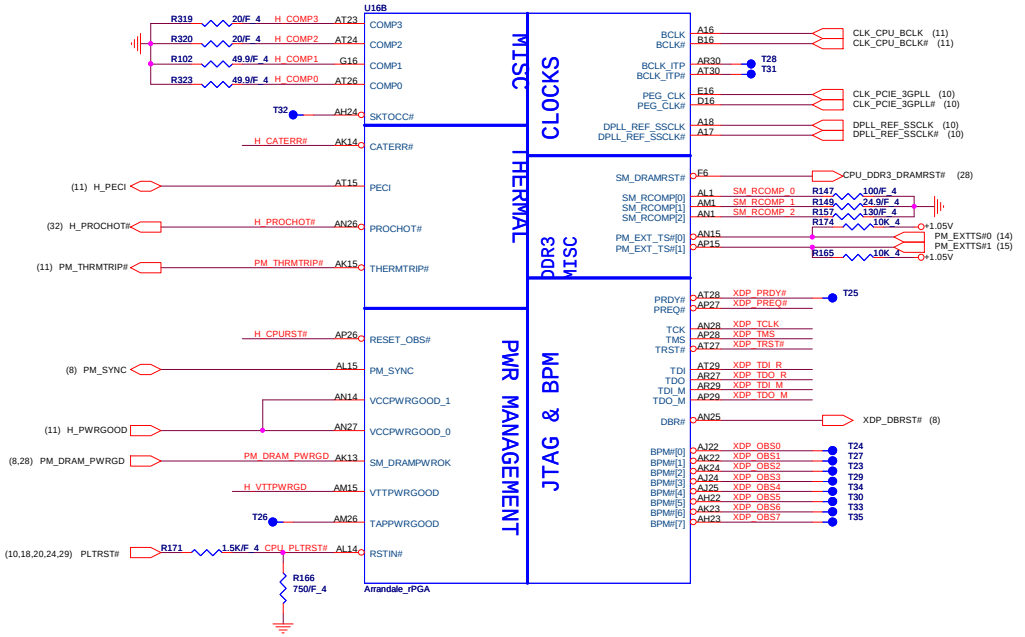
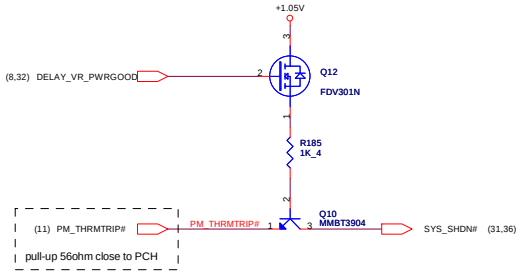
# AUBURNDALE/CLARKSFIELD PROCESSOR (DMI,PEG,FDI)



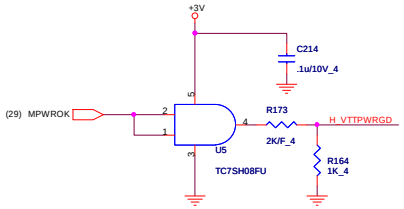

# AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)



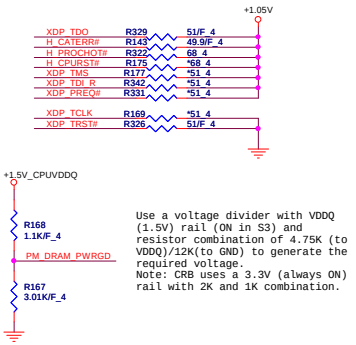

## Thermaltrip protect




## VTT PWR_Good

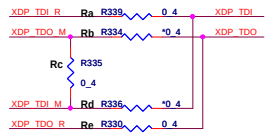



## Processor pull-up




Use a voltage divider with VDDQ (1.5V) rail (ON in S3) and resistor combination of 4.75K (to VDDQ)/12K(to GND) to generate the required voltage.
Note: CRB uses a 3.3V (always ON) rail with 2K and 1K combination.

## JTAG MAPPING




| Scan Chain (Default) | STUFF -> Ra, Rc, Re<br>NO STUFF -> Rb, Rd |
|---|---|
| CPU Only | STUFF -> Ra, Rb<br>NO STUFF -> Rc, Rd, Re |
| GMCH Only | STUFF -> Rd, Re<br>NO STUFF -> Ra, Rb, Rc |

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| | AUBURNDA 1/4 | 1A |

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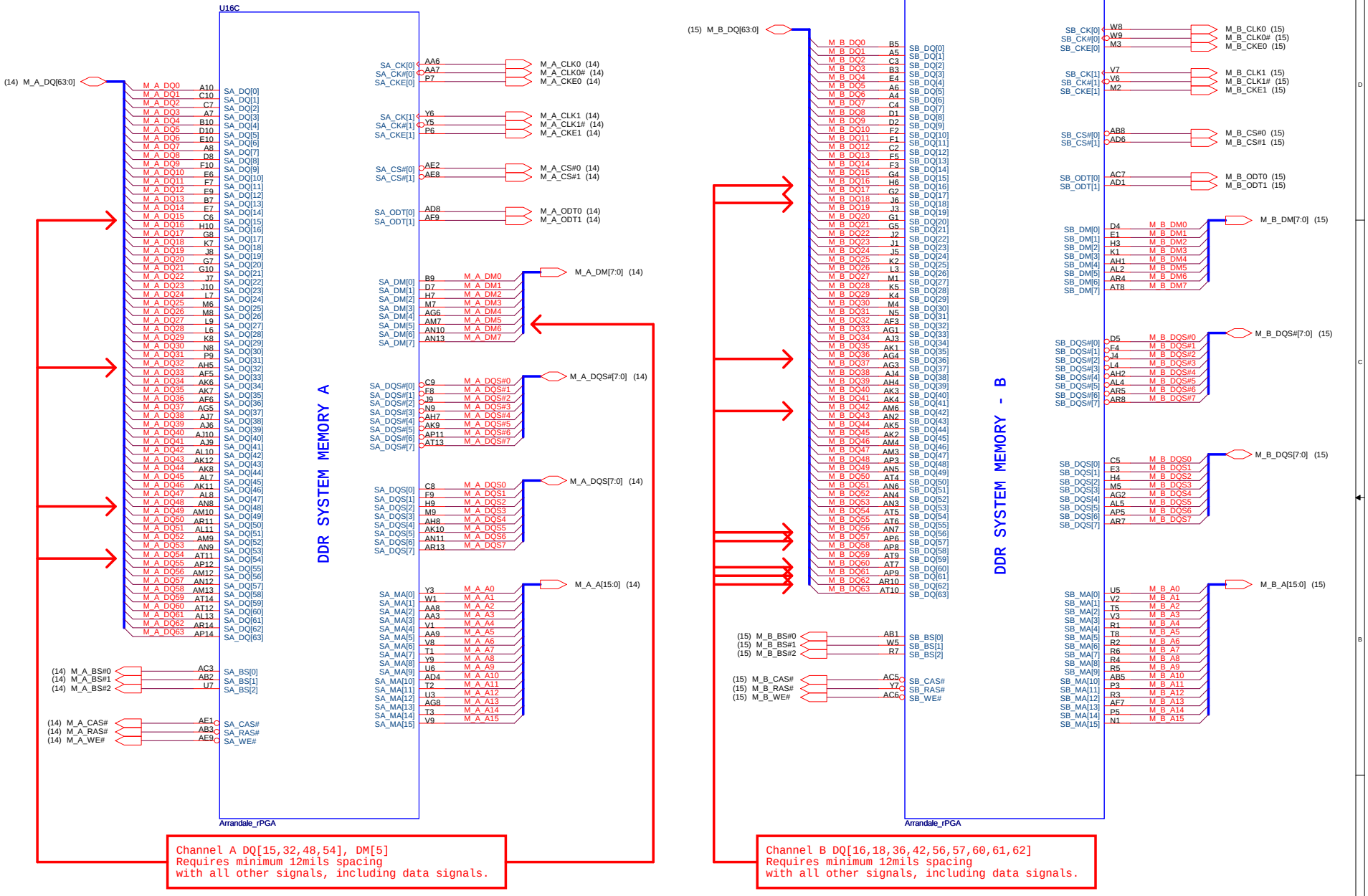
# AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

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|---|---|---|
| | AUBURNDA 2/4 | 1A |
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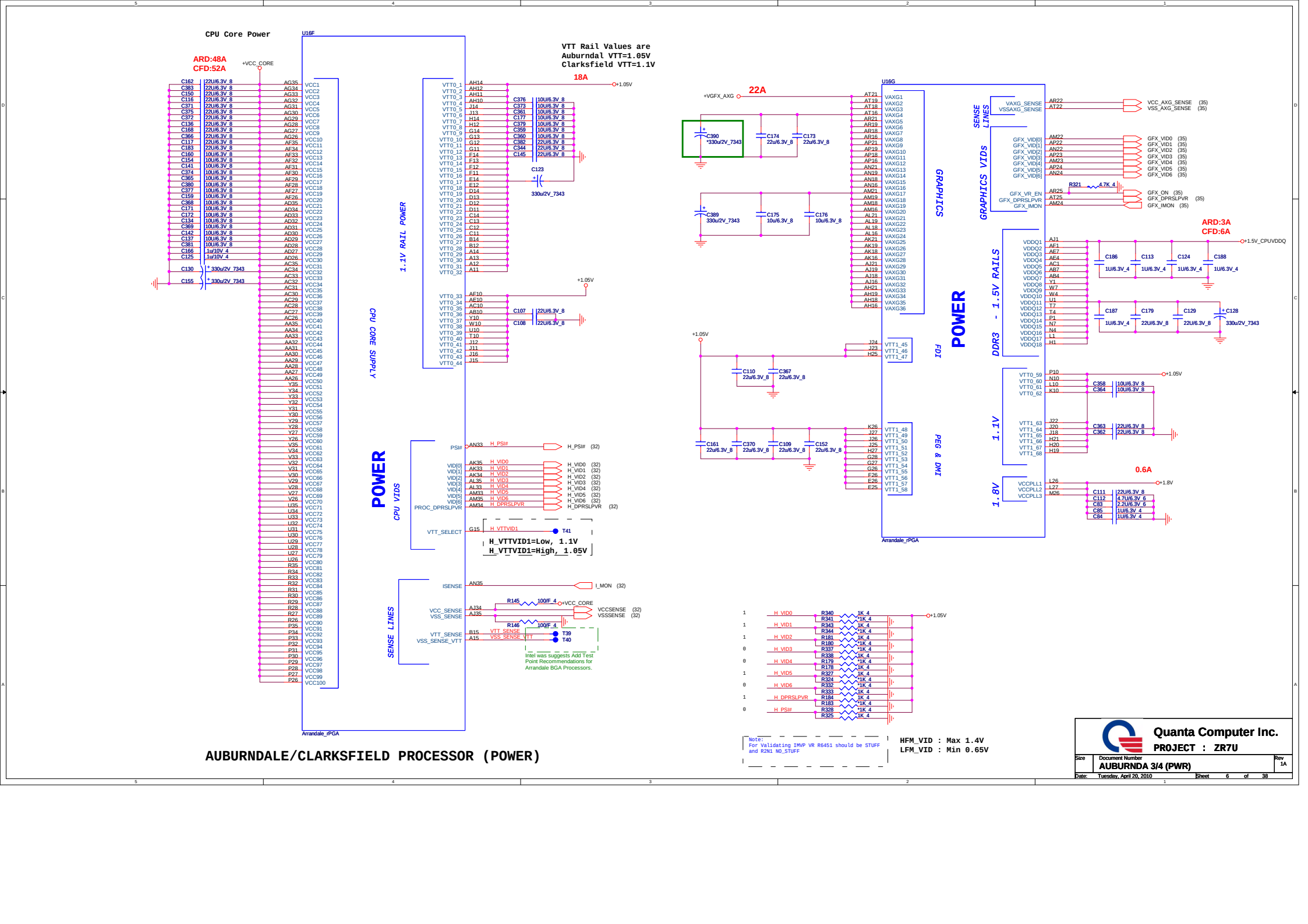
CPU Core Power
ARD:48A
CFD:52A
+VCC_CORE
U16F
VTT Rail Values are
Auburndal VTT=1.05V
Clarksfield VTT=1.1V
18A
1.1V RAIL POWER
CPU CORE SUPPLY
POWER
CPU VIDS
SENSE LINES
H_PSI#
H_VID0
H_VID1
H_VID2
H_VID3
H_VID4
H_VID5
H_VID6
H_DPRSLPVR
H_VTTVID1
T41
H_VTTVID1=Low, 1.1V
H_VTTVID1=High, 1.05V
I_MON
VCCSENSE
VSSSENSE
VTT_SENSE
VSS_SENSE_VTT
T39
T40
Intel was suggests Add Test Point Recommendations for Arrandale BGA Processors.
Arrandale_rPGA
22A
+VGFX_AXG
U16G
GRAPHICS
VAXG_SENSE
VSSAXG_SENSE
VCC_AXG_SENSE (35)
VSS_AXG_SENSE (35)
GRAPHICS VIDs
GFX_VID0 (35)
GFX_VID1 (35)
GFX_VID2 (35)
GFX_VID3 (35)
GFX_VID4 (35)
GFX_VID5 (35)
GFX_VID6 (35)
GFX_VR_EN
GFX_DPRSLPVR
GFX_IMON
GFX_ON (35)
GFX_DPRSLPVR (35)
GFX_IMON (35)
ARD:3A
CFD:6A
DDR3 - 1.5V RAILS
+1.5V_CPUVDDQ
FDI
DMI & PEG
1.1V
0.6A
1.8V
VCCPLL1
VCCPLL2
VCCPLL3
+1.8V
Arrandale_rPGA
Note:
For Validating IMVP VR R6451 should be STUFF and R2N1 NO_STUFF
HFM_VID : Max 1.4V
LFM_VID : Min 0.65V
AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)
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AUBURNDA 3/4 (PWR)
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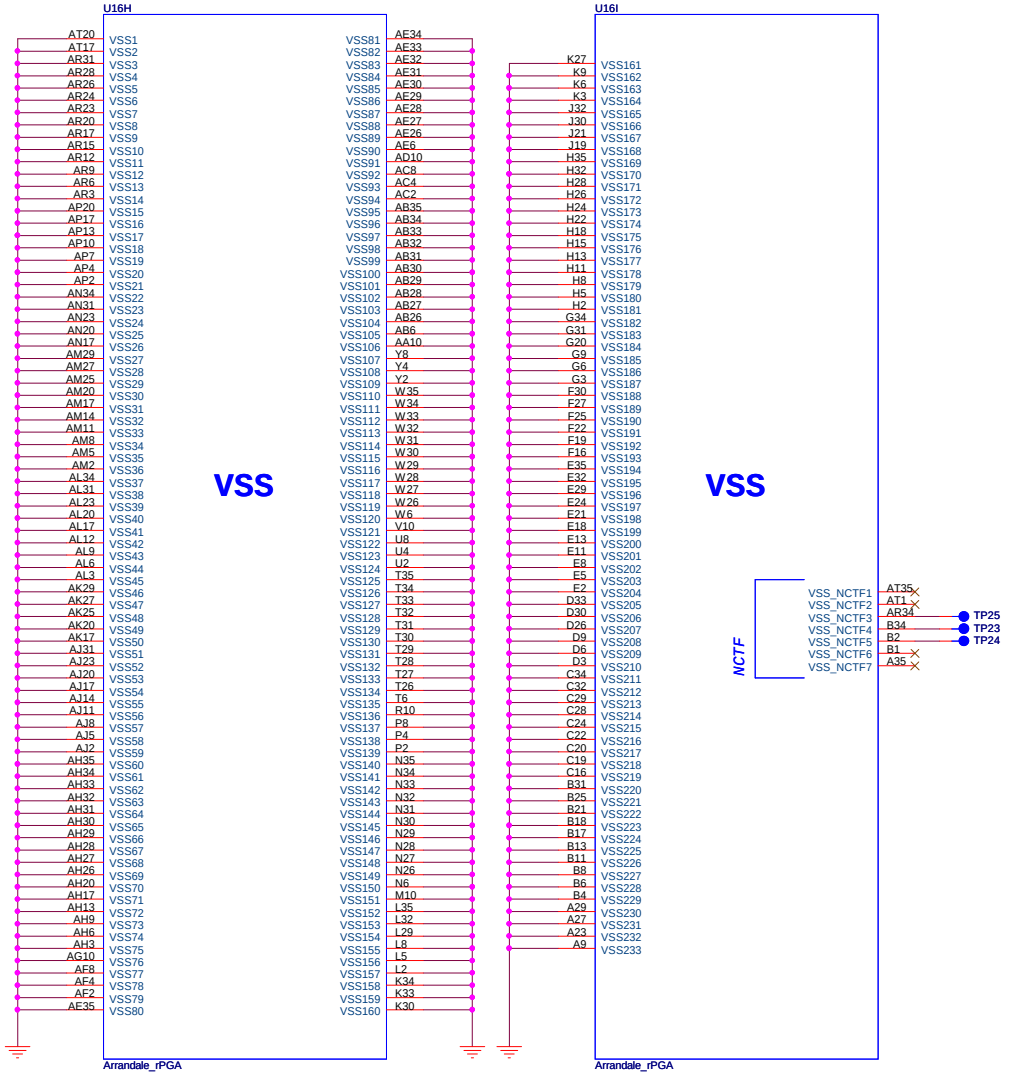
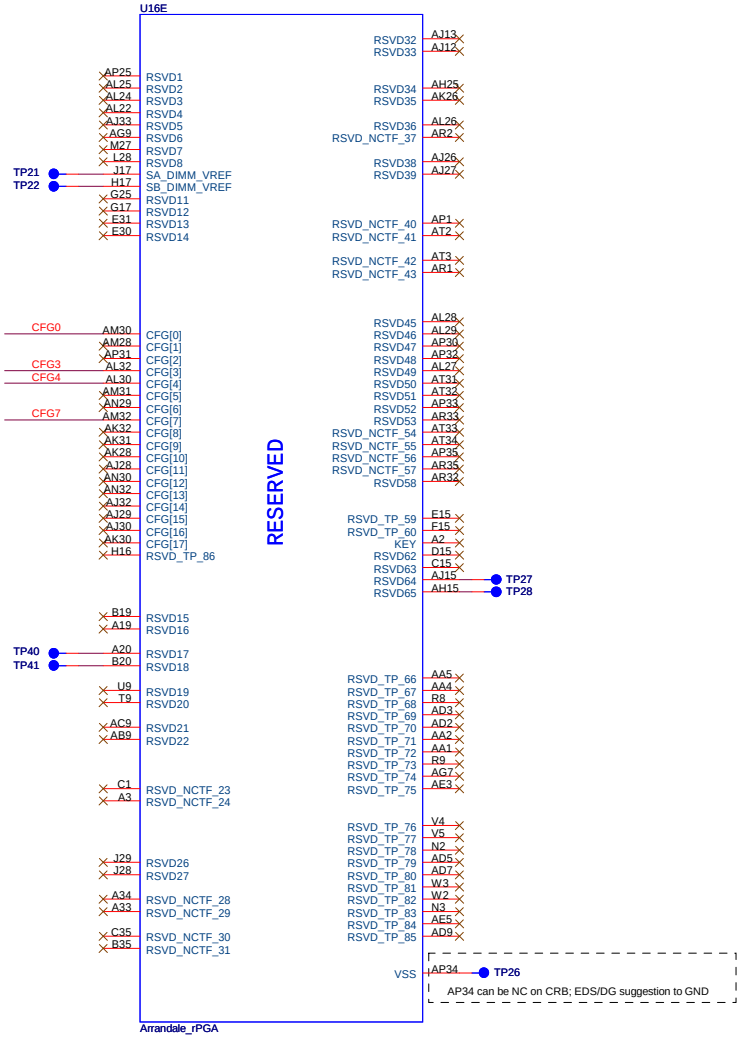
# AUBURNDALE/CLARKSFIELD PROCESSOR (GND)




# AUBURNDALE/CLARKSFIELD PROCESSOR( RESERVED, CFG)




## Processor Strapping

| | 1 | 0 | DEFAULT | |
|---|---|---|---|---|
| CFG0 (PCI-Epress Configuration Select) | Single PEG | Bifurcation enabled | No use | CFG0 R172 *3.01K/F_4 |
| CFG3 (PCI-Epress Static Lane Reversal) | Normal Operation | Lane Numbers Reversed | No use | CFG3 R156 *3.01K/F_4 |
| CFG4 (Embended Display Port Presence) | Disabled; No Physical Display Port attached to Embedded Diplay Port | Enabled; An external Display port device is connected to the Embedded Display port | No use | CFG4 R148 *3.01K/F_4 |
| T | | | | CFG7 R158 *3.01K/F_4 |

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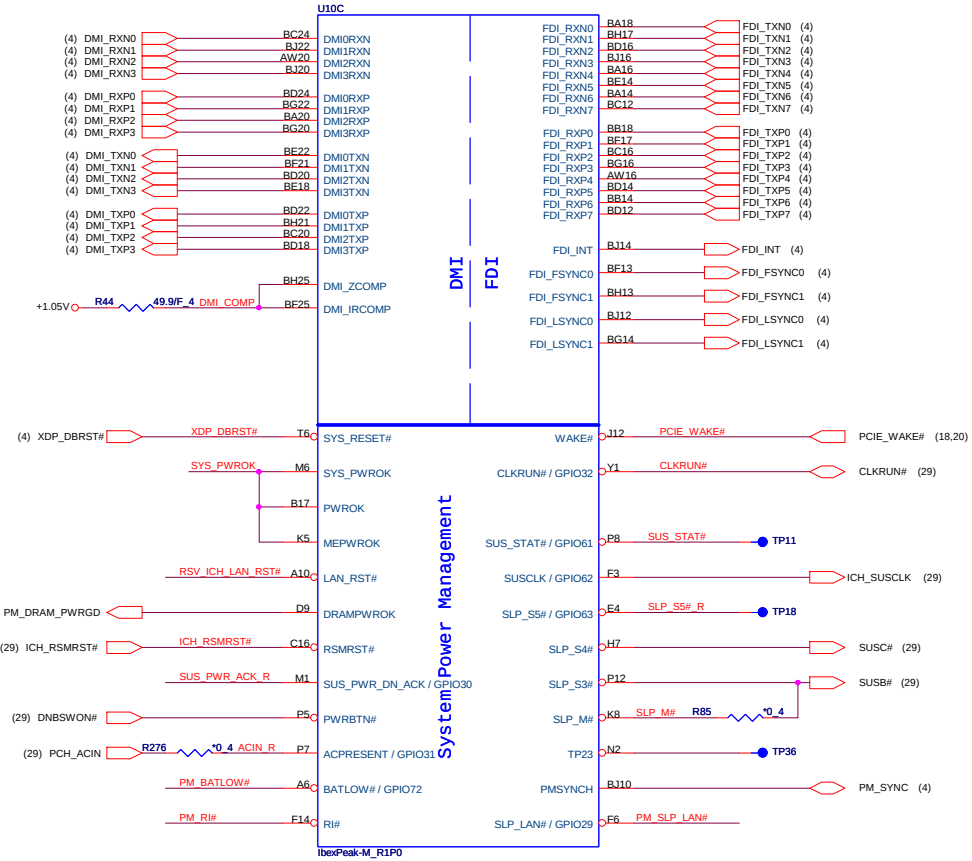
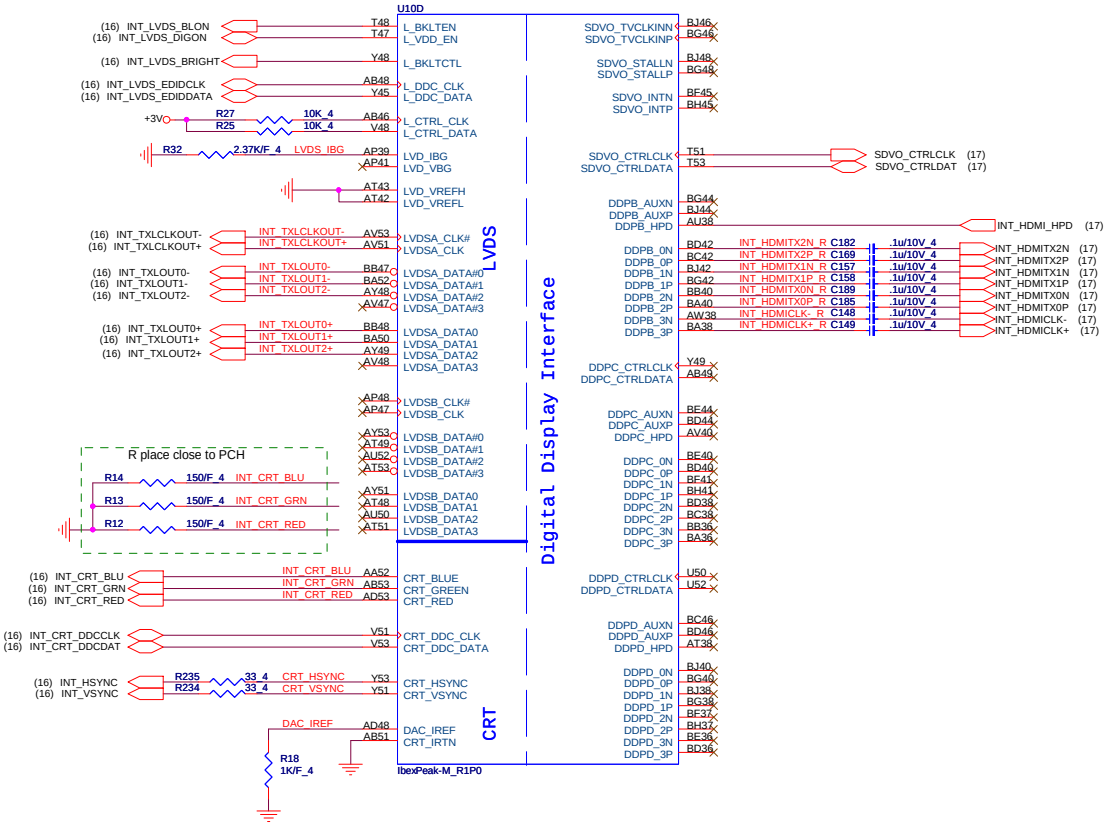
PCH1(CLG)

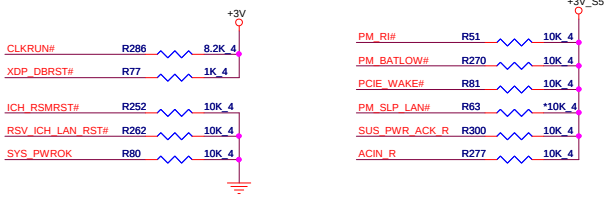
# IBEX PEAK-M (DMI,FDI,GPIO)



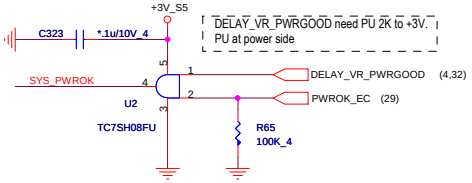

# IBEX PEAK-M (LVDS,DDI)




## PCH Pull-high/low(CLG)




## System PWR_OK(CLG)

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| | IBEX PEAK-M 1/6 | 1A |

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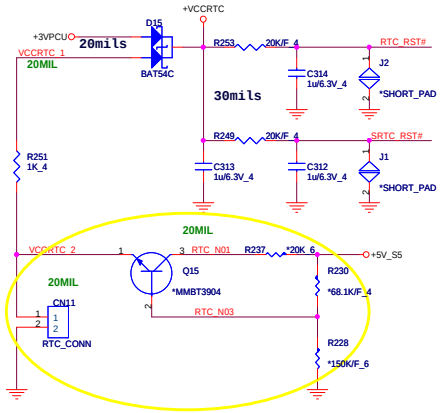
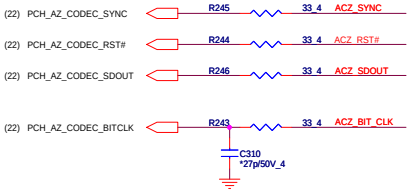
## RTC Circuitry(RTC)

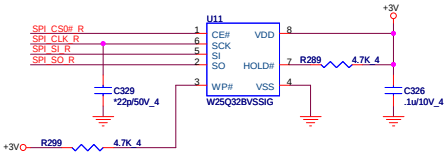



## HDA Bus(CLG)



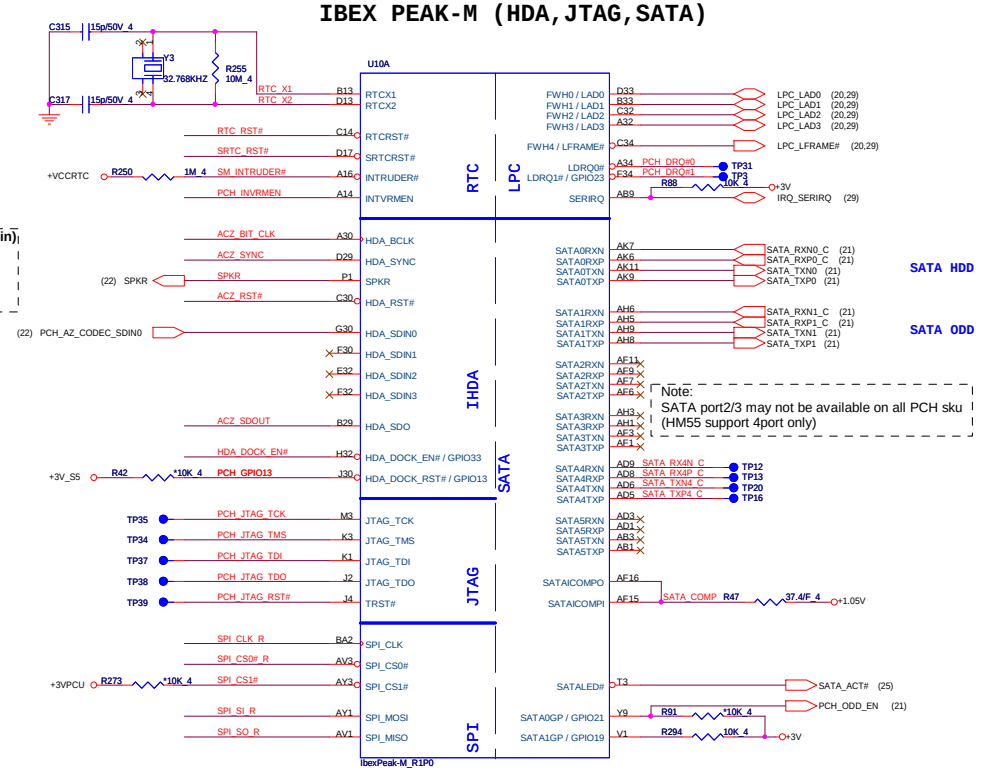

Place all series terms close to PCH except for SDIN input lines,which should be close to source.Placement of R should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

## PCH SPI(CLG)




## PCH2(CLG)

# IBEX PEAK-M (HDA,JTAG,SATA)




## PCH Strap Table

| Pin Name | Strap description | Sampled | Configuration | ZR7U note |
|---|---|---|---|---|
| **SPKR** | No reboot mode setting | PWROK | 0 = Default (weak pull-down 20K)<br>1 = Setting to No-Reboot mode | +3V R282 *10K_4 SPKR |
| **INIT3_3V** | Reserved | PWROK | 1 = Default (weak pull-up 20K)<br>Should not be pull-down | No use |
| **GNT3# / GPIO55** | Top-Block Swap Override | PWROK | 0 = "top-block swap" mode<br>1 = Default (weak pull-up 20K) | R231 *10K_4 PCI_GNT3# (10) |
| **INTVRMEN** | Integrated 1.05V VRM enable | ALWAYS | Should be always pull-up | +VCCRTC R254 330K_4 PCH_INVRMEN |
| **GNT1# / GPIO51** | Boot BIOS Selection 1 [bit-1] | PWROK | GNT1# / GNT0# / Boot Location<br>1 / 1 / SPI<br>1 / 0 / PCI<br>0 / 0 / LPC | +3V R22 1K_4 R6 1K_4 R21 *1K_4 R10 *1K_4 PCI_GNT0# (10) PCI_GNT1# (10) |
| **GNT0#** | Boot BIOS Selection 0 [bit-0] | PWROK | | |
| **GNT2# / GPIO53** | ESI strap (Server only) | PWROK | Should not be pull-down (weak pull-up 20K) | No use |
| **NV_ALE** | Intel Anti-Theft HDD protection | PWROK | 0 = Disable (Internal pull-down 32ohm) | +1.8V R265 *1K_4 NV_ALE NV_ALE (10) |
| **NV_CLE** | DMI Termination voltage | PWROK | weak pull-down 32ohm<br>Set to Vcc when LOW | +1.8V R261 *1K_4 NV_CLE NV_CLE (10) |
| **HDA_DOCK_EN#/GPIO33** | Flash Descriptor Security | PWROK | 0 = Override<br>1 = Default (weak pull-up 20K) | +3V R36 *1K_4 R37 *10K_4 HDA_DOCK_EN# |
| **SPI_MOSI** | iTPM function Disable | MEPWROK | 0 = Default (weak pull-down 20K)<br>1 = Enable | +3V R301 *1K_4 SPI_SI_R |
| **HDA_SDO** | Reserved | RSMRST# | Should not be pull-up (weak pull-down 20K) | |
| **GPIO8** | Reserved | RSMRST# | Should not be pull-down (weak pull-up 20K) | +3V_S5 R274 10K_4 RSV_GPIO8 (11) |
| **GPIO27** | On-die PLL Voltage Regulator | RSMRST# | 0 = Disable<br>1 = Enable (weak pull-up 20K) | On-die PLL voltage enable |
| **HDA_SYNC** | On-die PLL PWR supply select | RSMRST# | 0 = 1.8V supply (weak pull-down 20K)<br>1 = 1.5V supply | use default (0=1.8V supply) |
| **GPIO15** | Reserved | RSMRST# | 0 = TLS no Confidentiality (weak pull-down 20K)<br>1 = TLS Confidentiality | +3V_S5 R92 1K_4 CR_WAKE# (11) |

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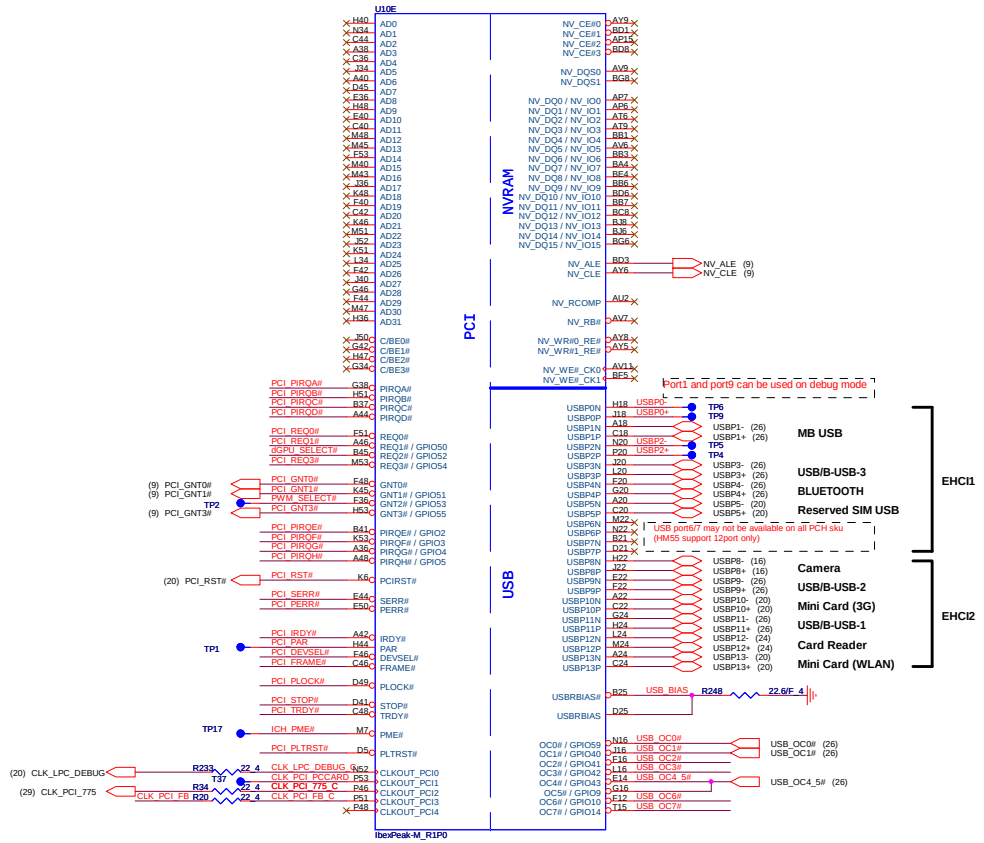
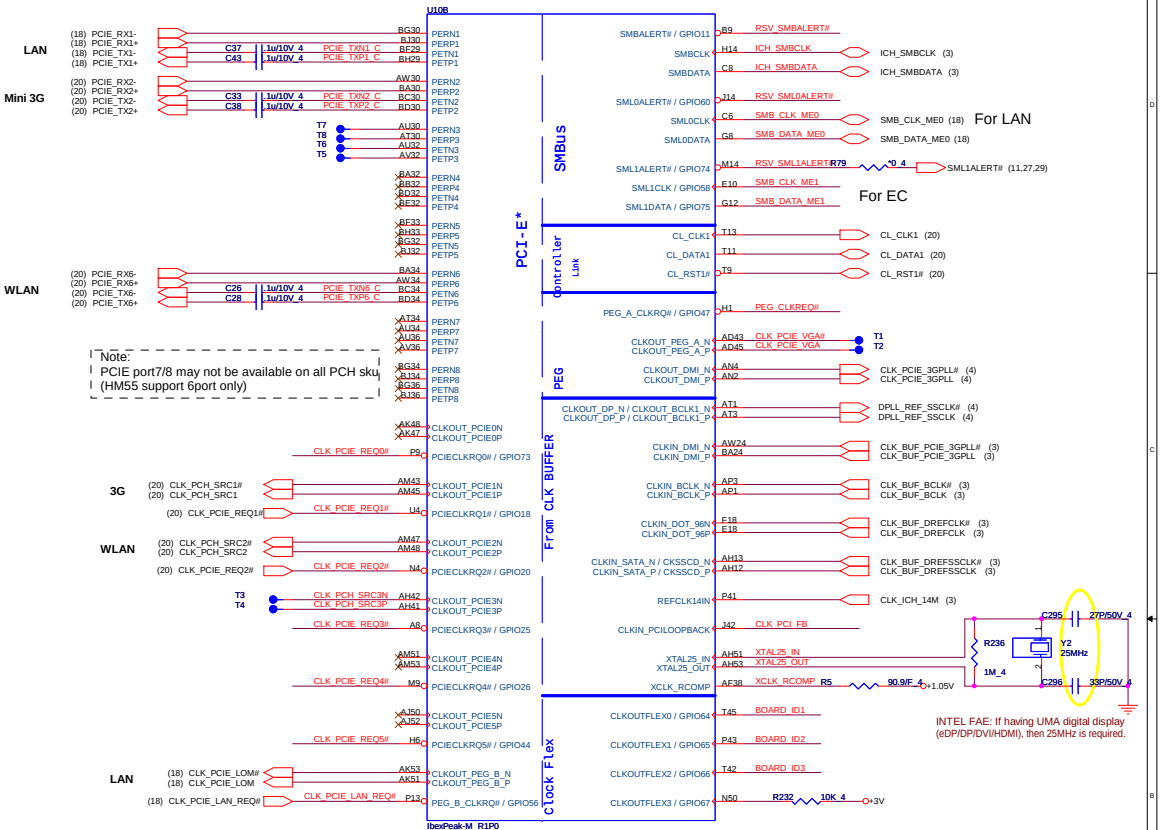
# PCH3(CLG)

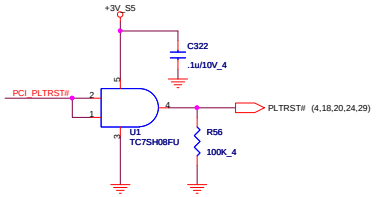
## IBEX PEAK-M (PCI,USB,NVRAM)



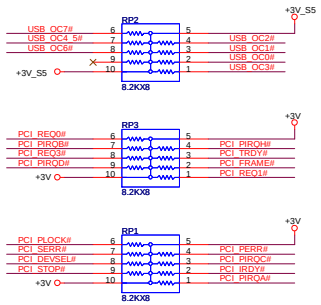

## IBEX PEAK-M (PCI-E,SMBUS,CLK)



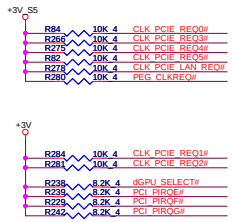

## PLTRST#(CLG)



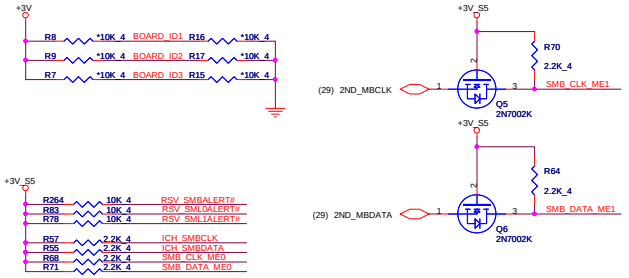

## PCI/USBOC# Pull-up(CLG)




## CLK_REQ/Strap Pin(CLG)



## SMBus/Pull-UP and Board ID



| | |
|---|---|
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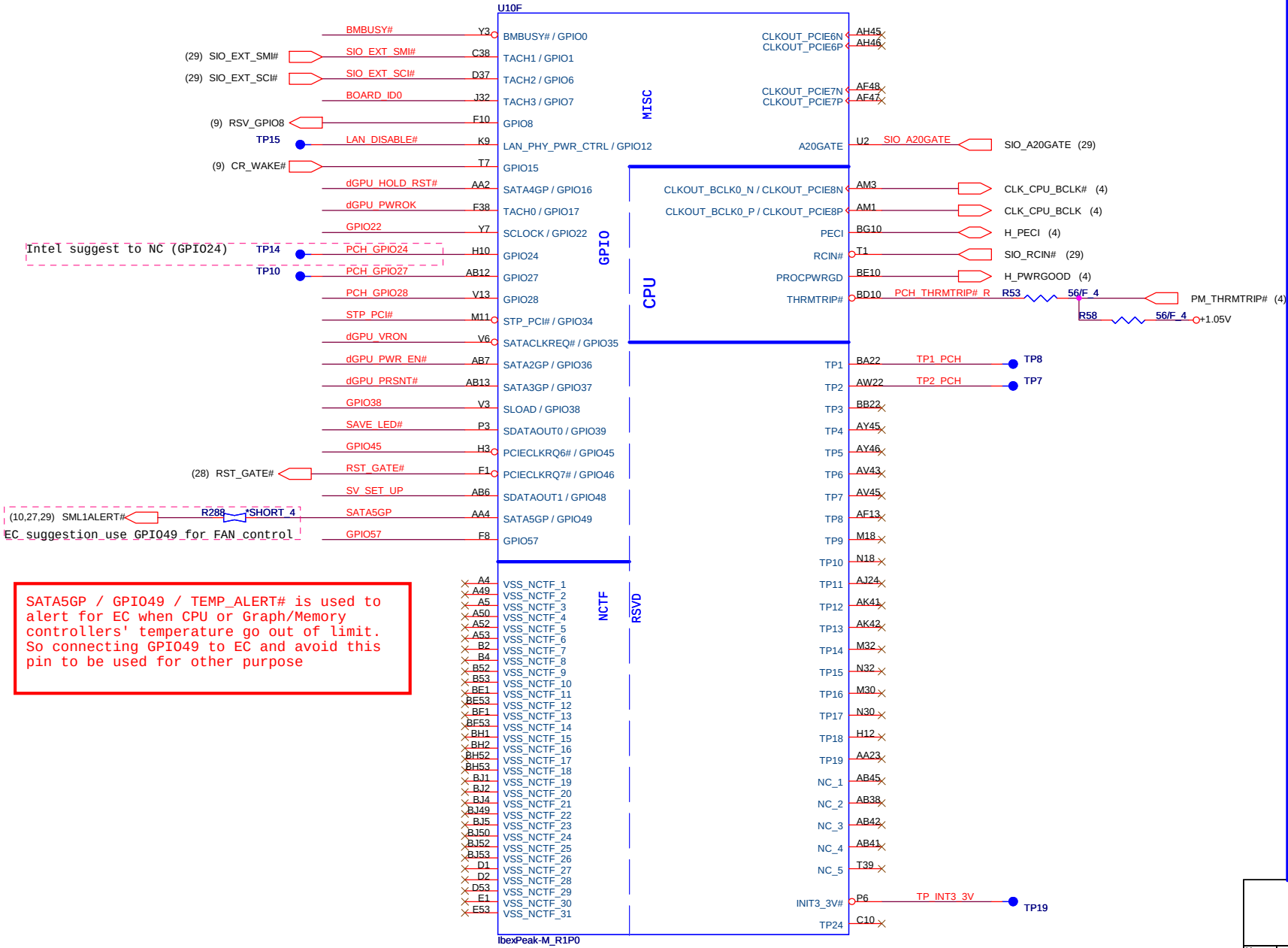
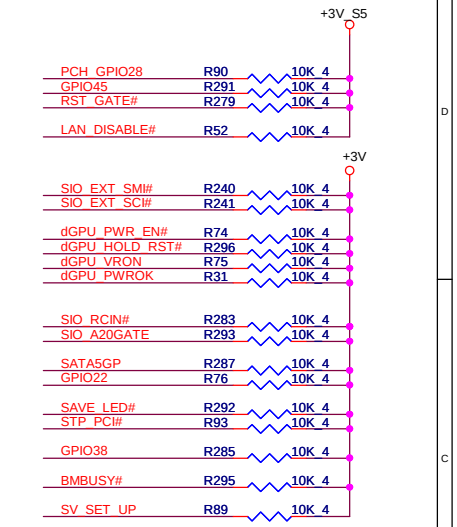
# IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



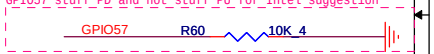

SATA5GP / GPIO49 / TEMP_ALERT# is used to alert for EC when CPU or Graph/Memory controllers' temperature go out of limit. So connecting GPIO49 to EC and avoid this pin to be used for other purpose

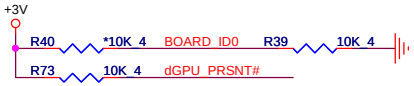
## GPIO Pull-up/Pull-down(CLG)




| SV_SET_UP | 1-X High = Strong (Default) |
|---|---|

GPIO57_stuff_PD and not_stuff_PU for_Intel suggestion




| BOARD_ID0 | High = JV41/JM41<br>Low = JM51 |
|---|---|
| RSV_GPIO8 | High = Disable<br>Low = Enable |

**Quanta Computer Inc.**
**PROJECT : ZR7U**

| Size | Document Number | Rev |
|---|---|---|
| | IBEX PEAK-M 4/6 | 1A |

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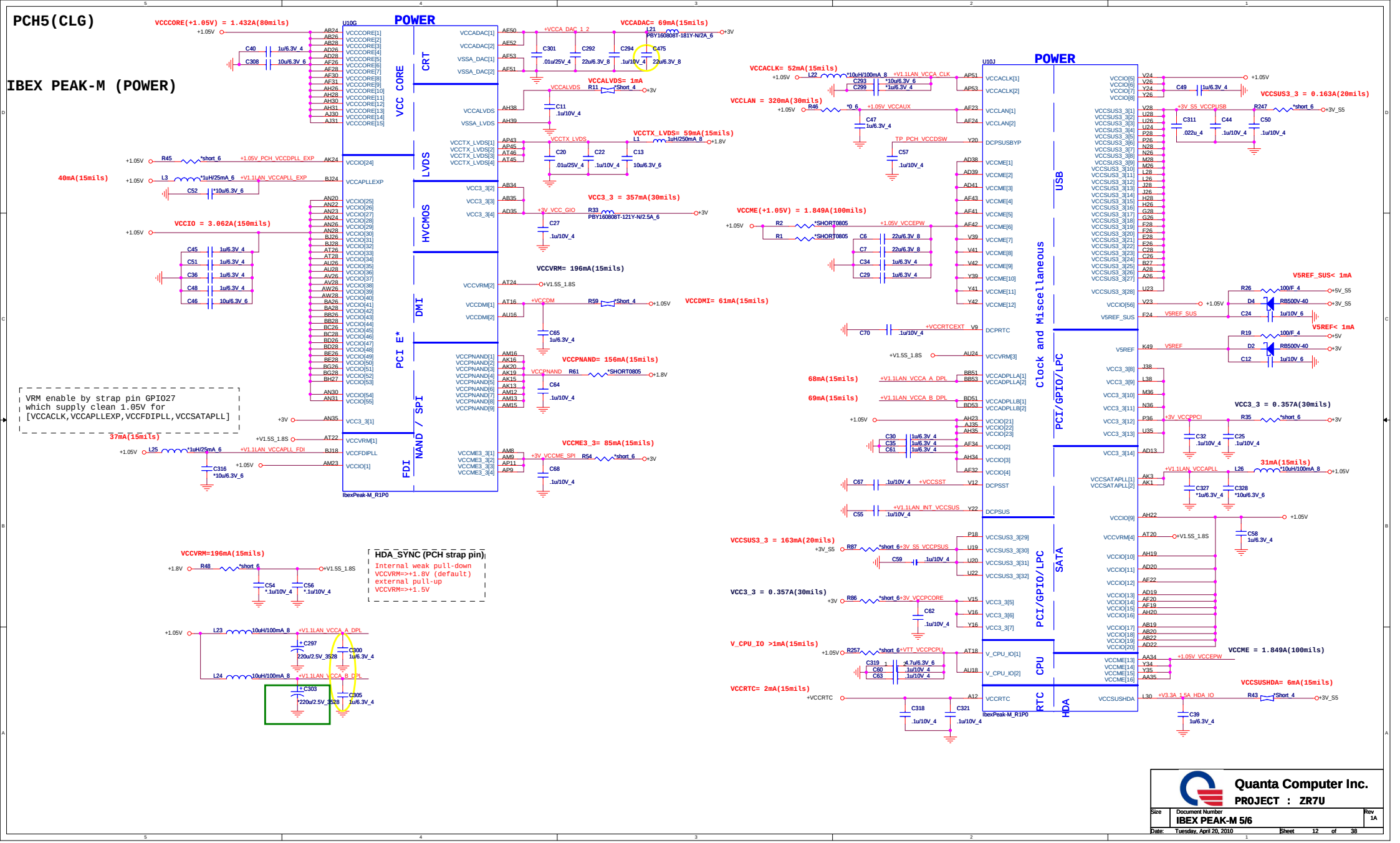
# PCH5(CLG)

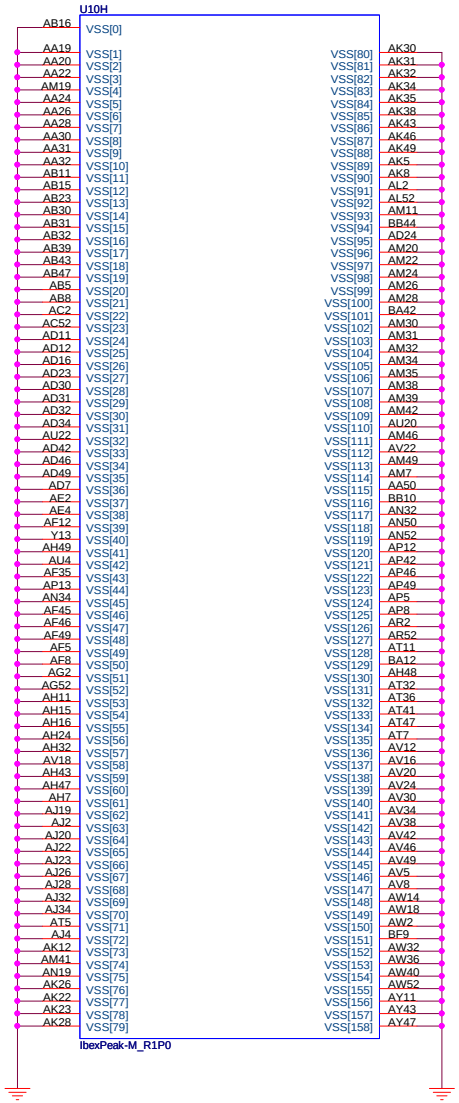
# IBEX PEAK-M (POWER)

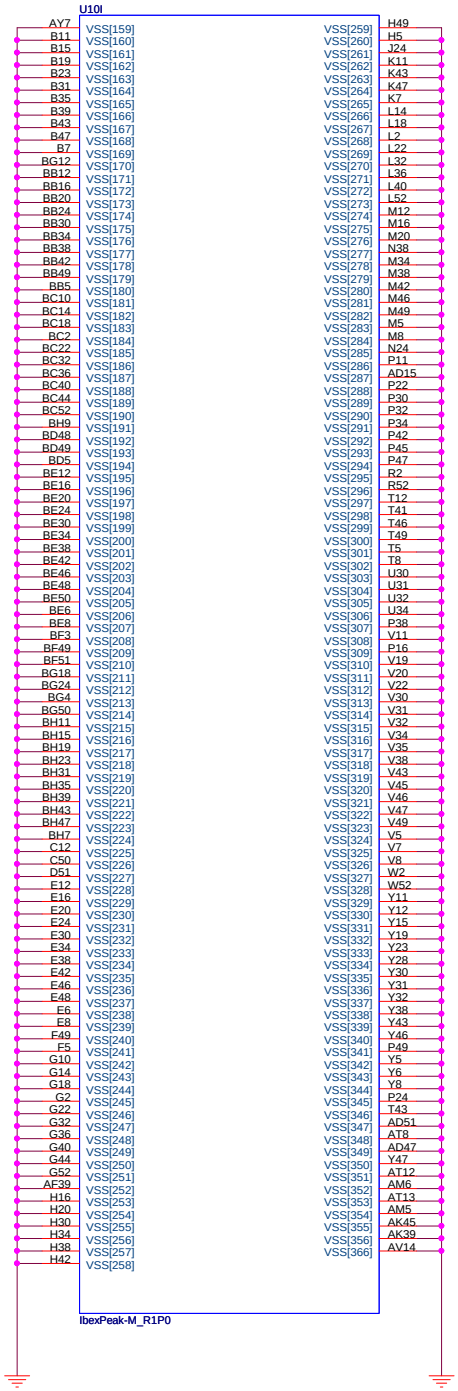



| | | | |
|---|---|---|---|
| Quanta Computer Inc. | | | |
| PROJECT : ZR7U | | | |
| Size | Document Number | | Rev |
| | IBEX PEAK-M 5/6 | | 1A |
| Date: Tuesday, April 20, 2010 | Sheet 12 of 38 | | |

# PCH6(CLG)

## IBEX PEAK-M (GND)

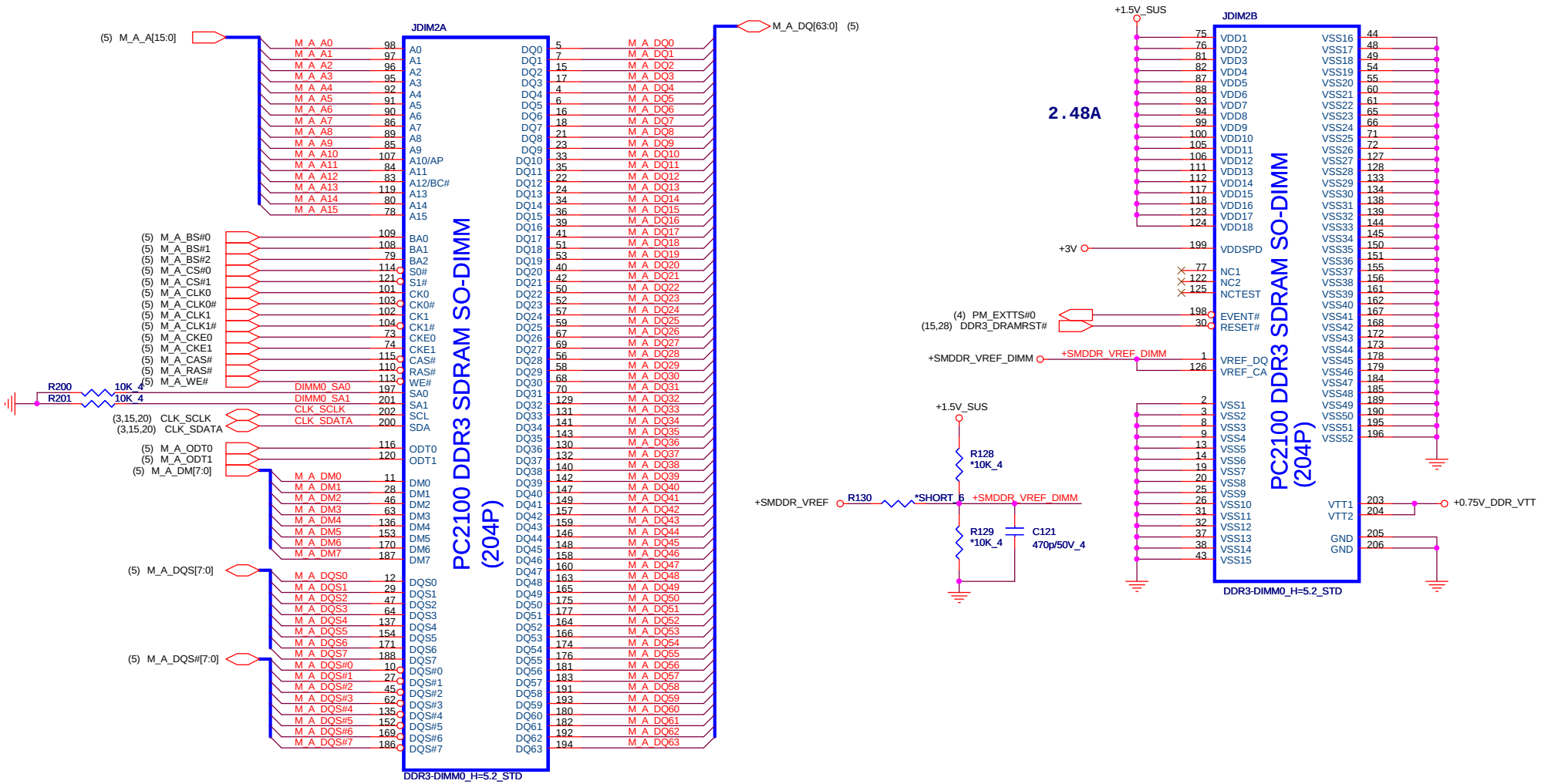


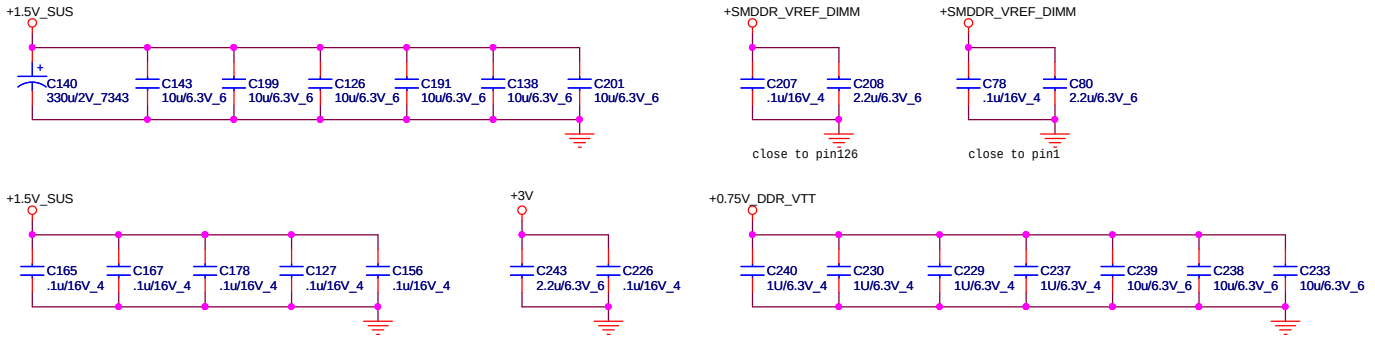

Quanta Computer Inc.

PROJECT : ZR7U

| Size | Document Number | Rev |
|---|---|---|
| | IBEX PEAK-M 6/6 | 1A |
| Date: Tuesday, April 20, 2010 | Sheet 13 of 38 | |



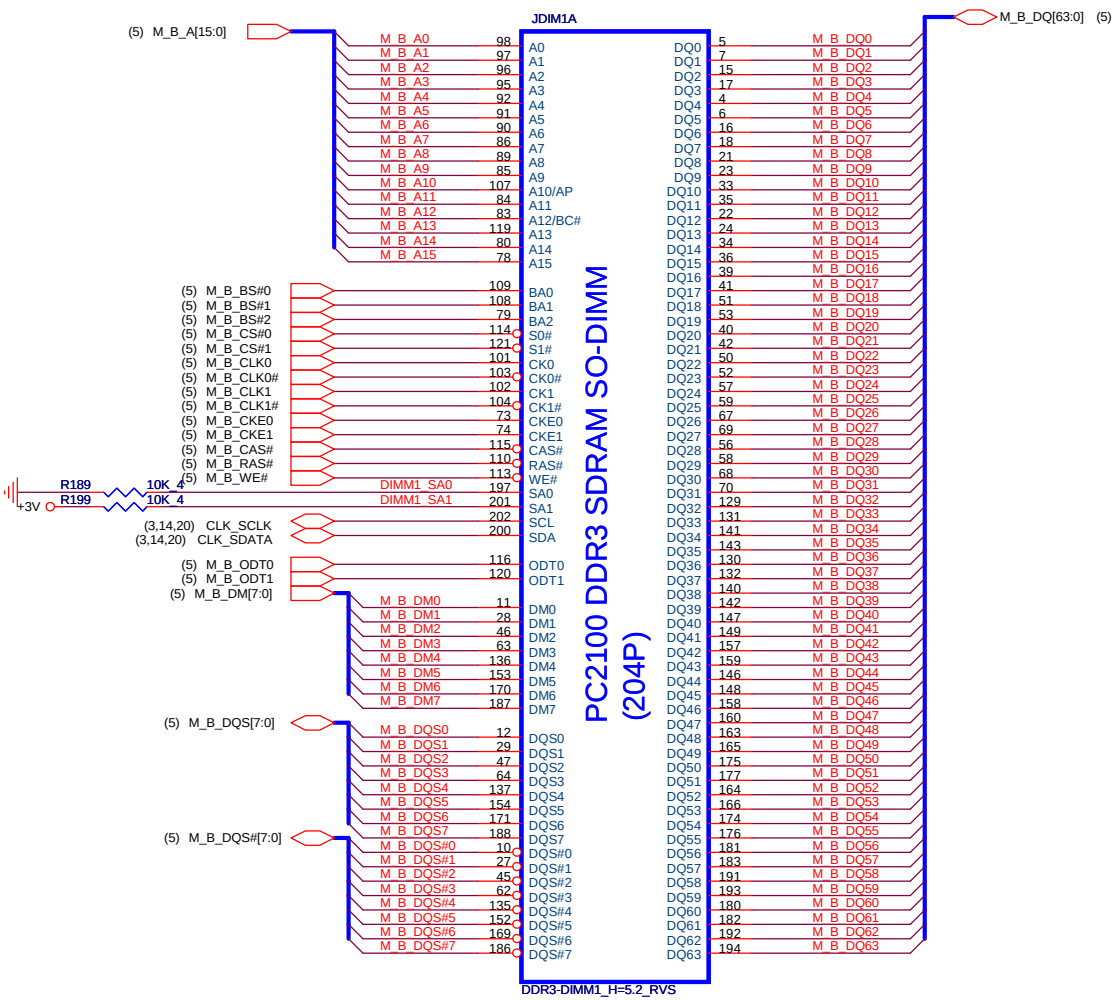

## DIMM decoupling CAP (near So-Dimm0)

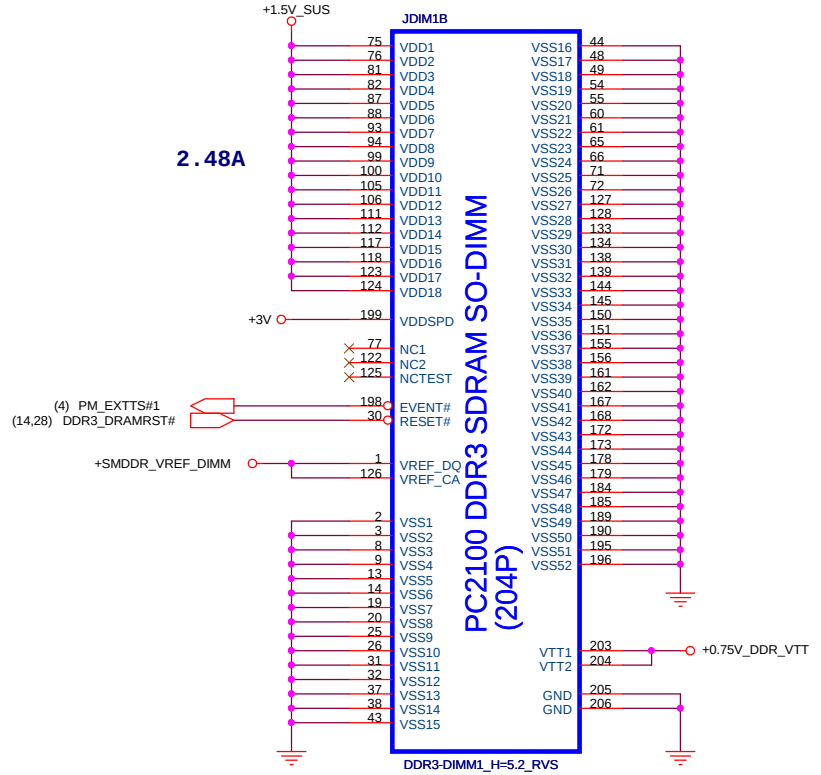



Quanta Computer Inc.

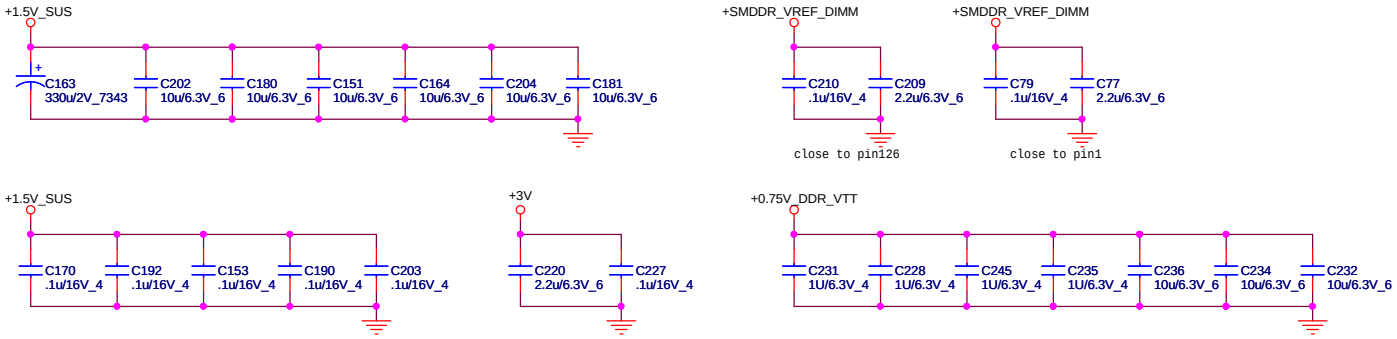
PROJECT : ZR7U

| Size | Document Number | Rev |
|---|---|---|
| | DDRIII SO-DIMM-0 | 1A |
| Date: Tuesday, April 20, 2010 | Sheet 14 of 38 | |



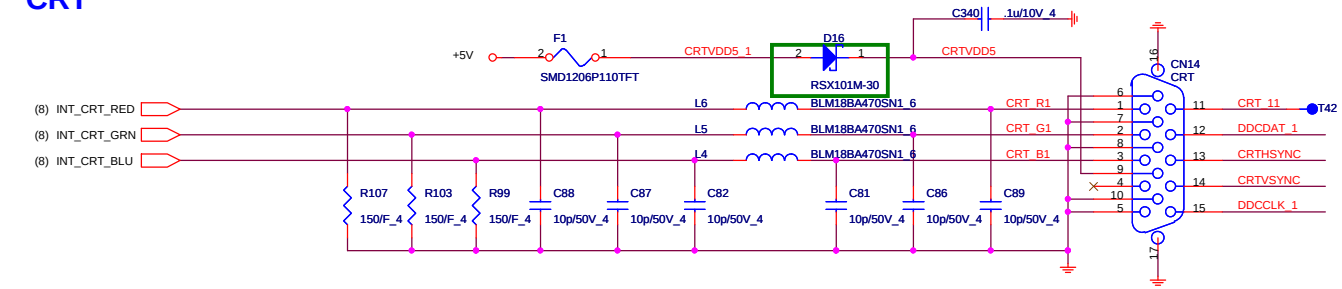

## DIMM decoupling CAP (near So-Dimm1)

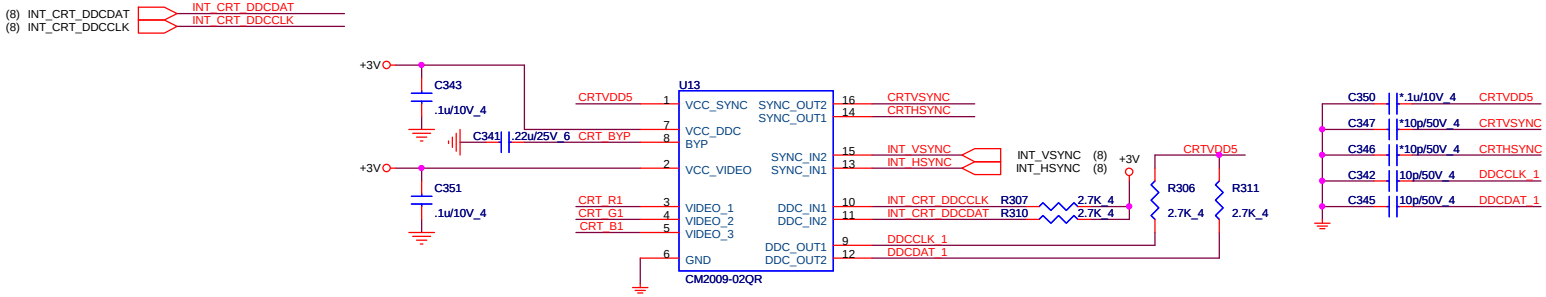



Quanta Computer Inc.
PROJECT : ZR7U

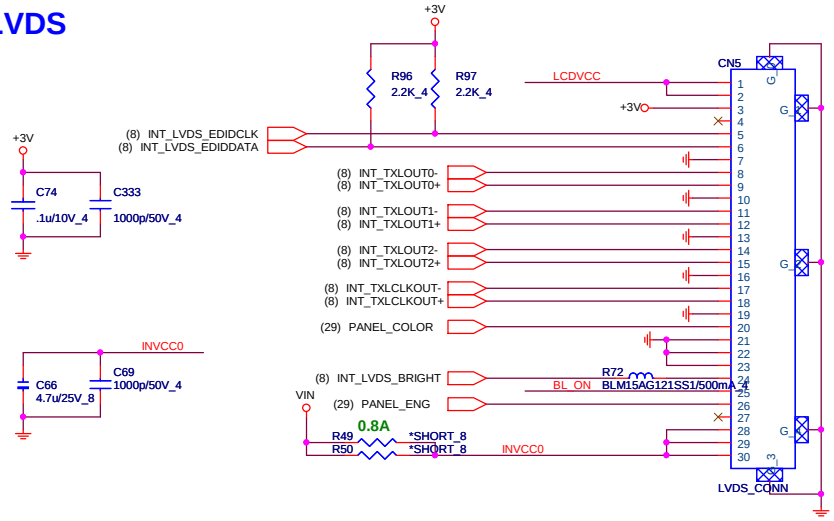
| Size | Document Number | Rev |
|---|---|---|
| | DDRIII SO-DIMM-1 | 1A |
| Date: Tuesday, April 20, 2010 | Sheet 15 of 38 | |

# CRT

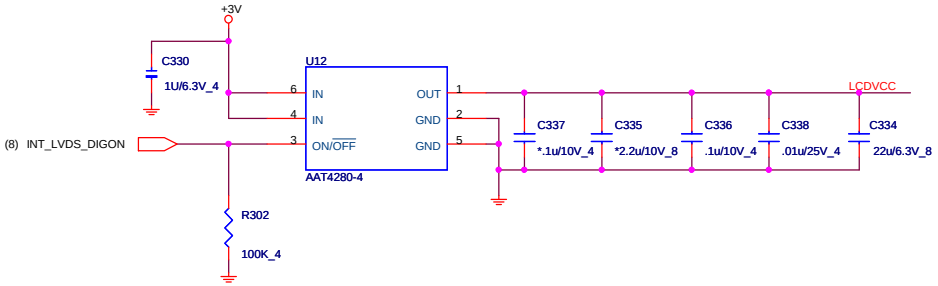


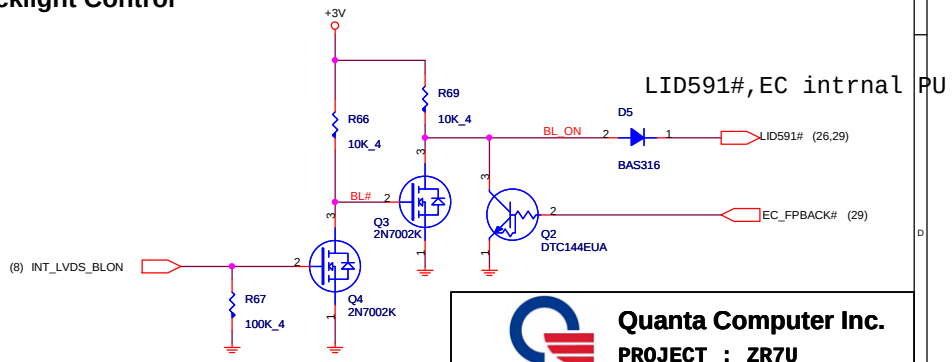

# LVDS




# LCD Power

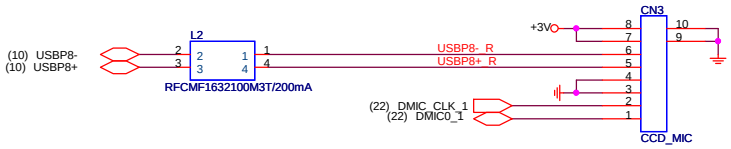



# Backlight Control



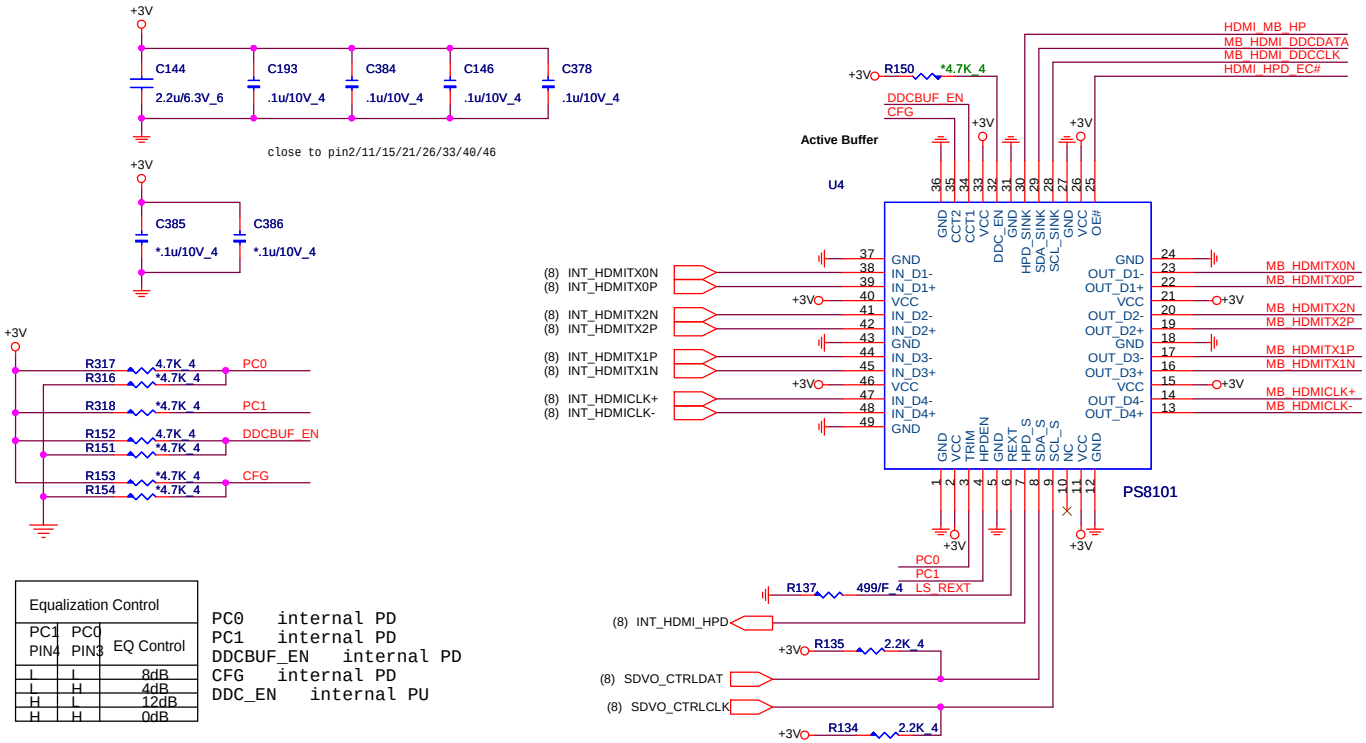

LID591#,EC intrnal PU

# CCD and MIC




| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : ZR7U | | |
| Size | Document Number: CRT/LVDS/CAMERA/LID | Rev: 1A |
| Date: Thursday, April 22, 2010 | Sheet 16 of 38 | |

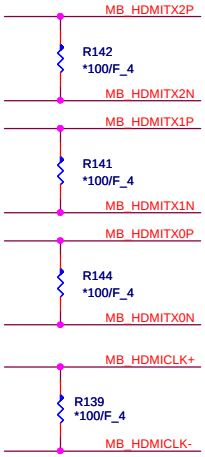
# HDMI LEVEL SHIFTER



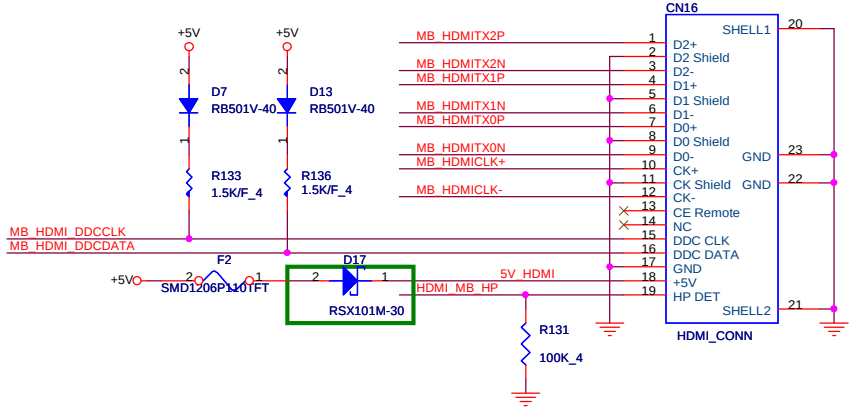

| Equalization Control | | |
|---|---|---|
| PC1 PIN4 | PC0 PIN3 | EQ Control |
| L | L | 8dB |
| L | H | 4dB |
| H | L | 12dB |
| H | H | 0dB |

PC0 internal PD
PC1 internal PD
DDCBUF_EN internal PD
CFG internal PD
DDC_EN internal PU

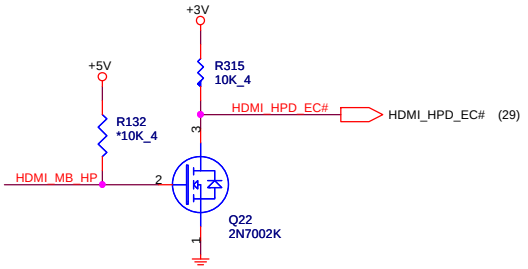
## EMI




## HDMI connector

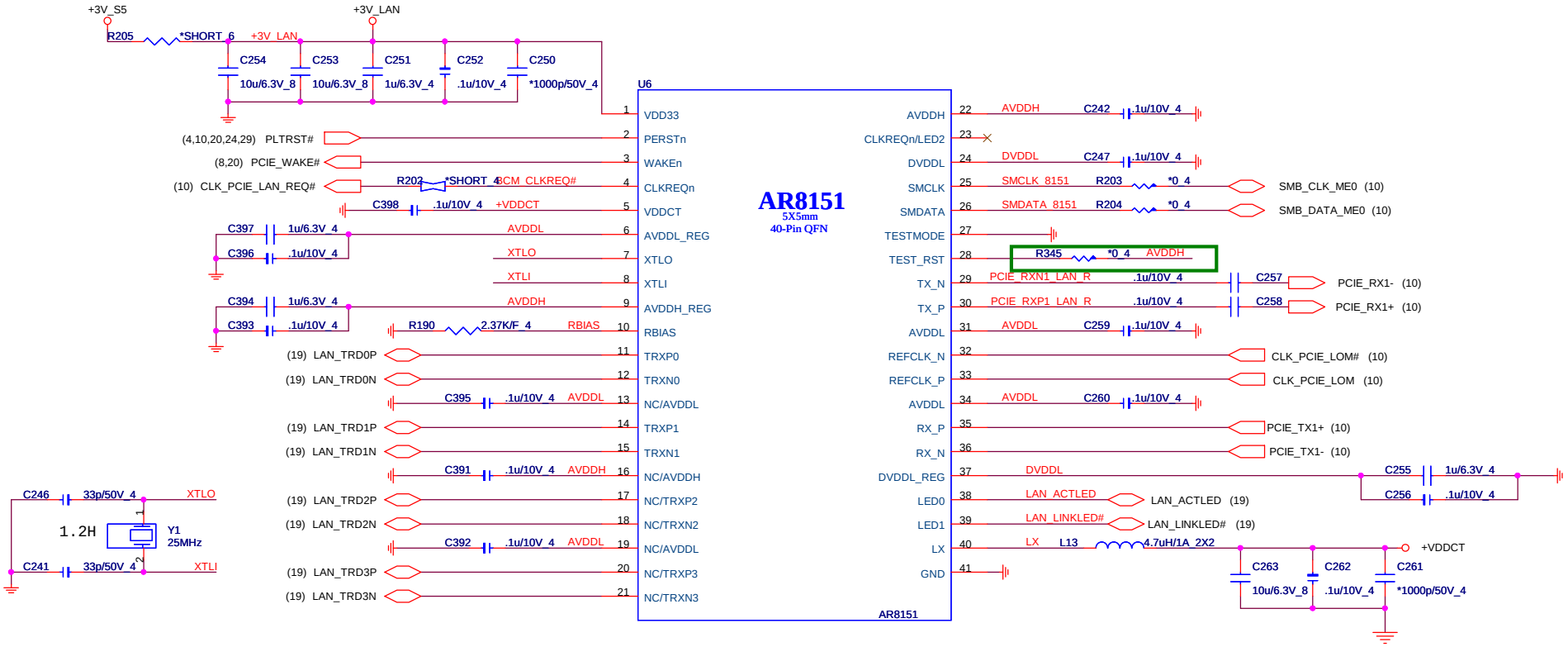


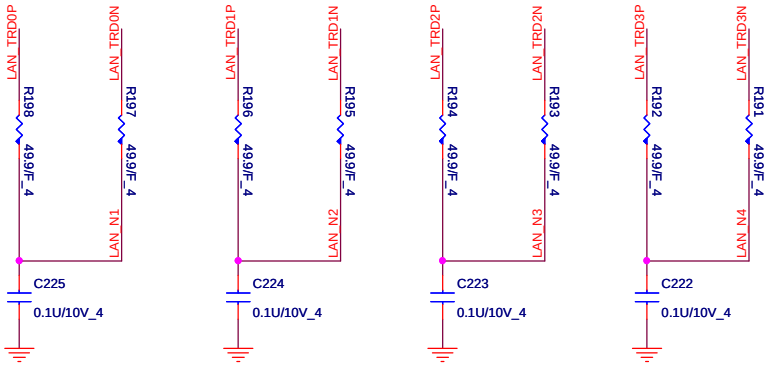

## HP-detect & OE# control



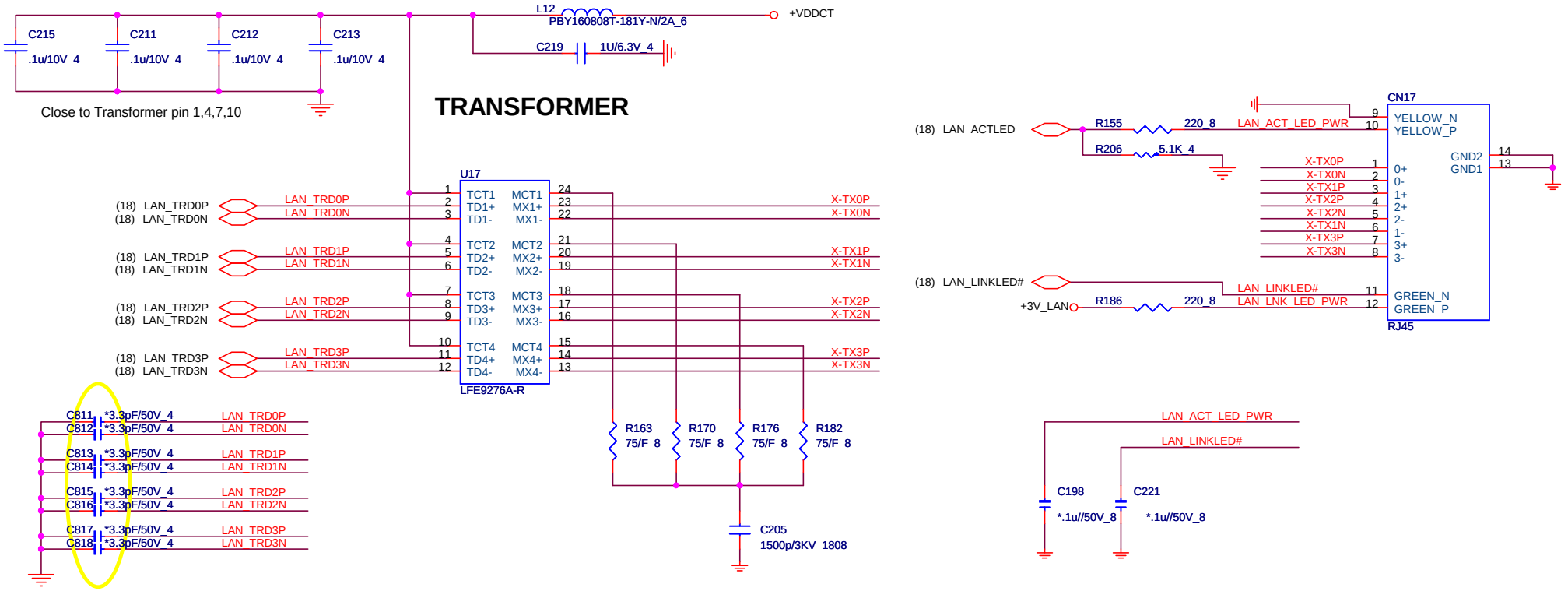

| Quanta Computer Inc. | | |
|---|---|---|
| PROJECT : ZR7U | | |
| Size | Document Number: HDMI (PS8101) | Rev 1A |
| Date: Tuesday, April 20, 2010 | Sheet 17 of 38 | |

# Giga-LAN AR8151




| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : ZR7U | | |
| Size | Document Number | Rev |
| | GLAN BCM57780 | 1A |
| Date: Thursday, April 22, 2010 | Sheet 18 of 38 | |







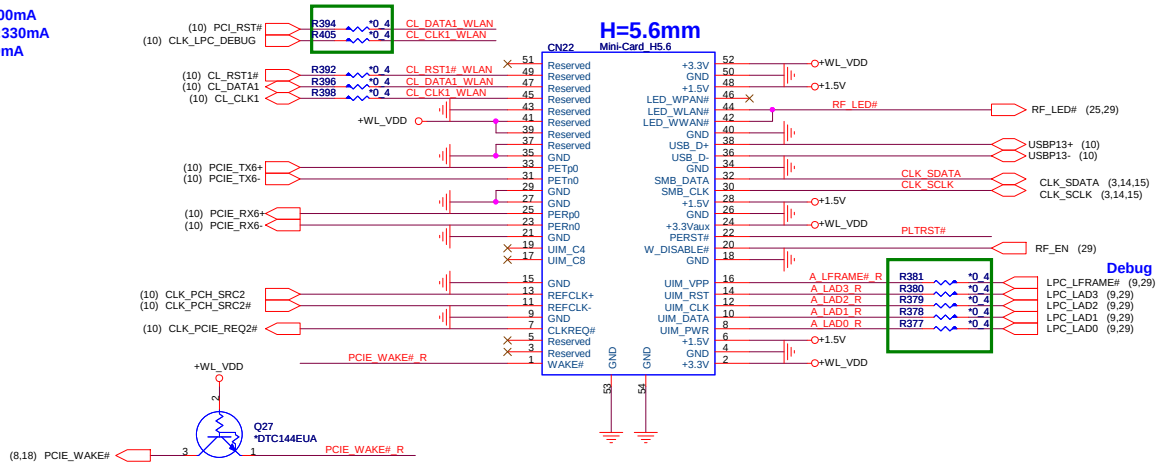
Delta LFE9276C-R (DB0ZR1LAN00)
FCE NS892407 (DB0LL1LAN00)
Bothhand GST5009B (DB0Z06LAN00)

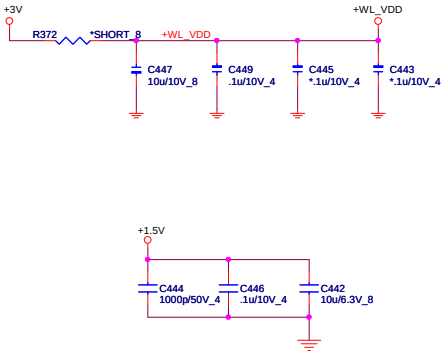
**Quanta Computer Inc.**
**PROJECT : ZR7U**

| Size | Document Number | Rev |
|---|---|---|
| | **LAN Transformer and RJ45** | 1A |
| Date: Tuesday, April 20, 2010 | Sheet 19 of 38 | |

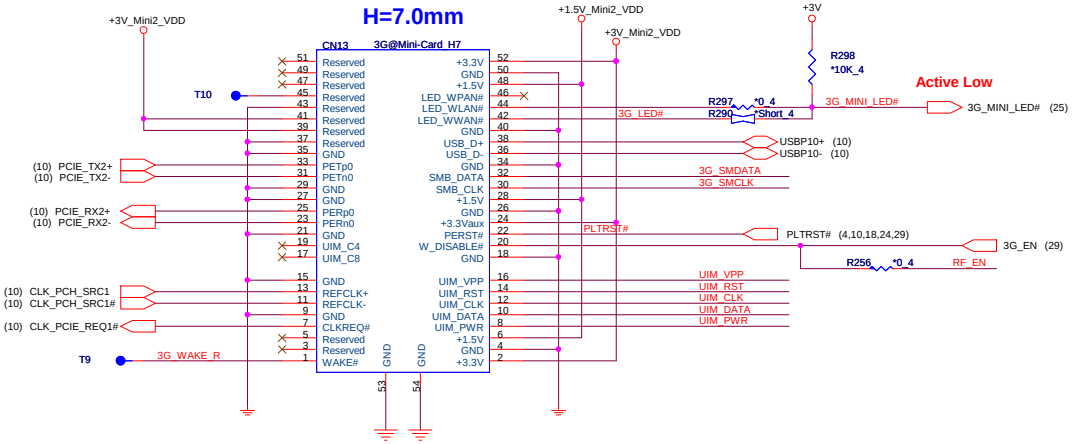
# MINI-CARD WLAN(MPC)

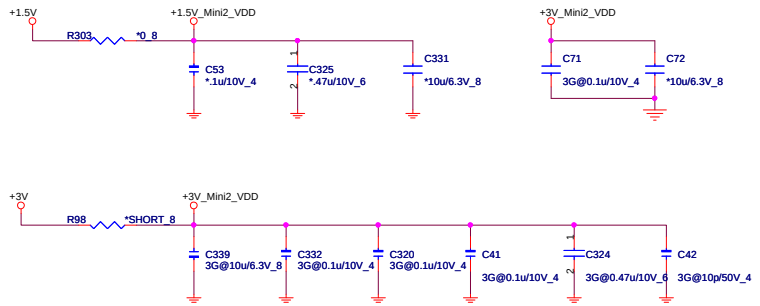
+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA



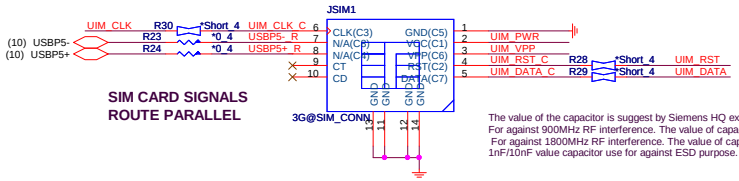




# MINI-CARD 3G(MNC)

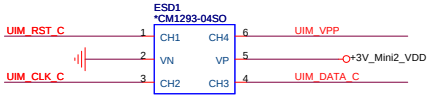


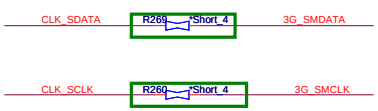



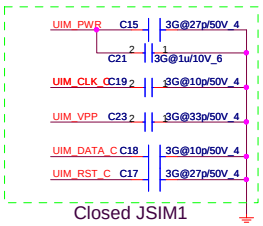

# SIM CARD(RFM)




The value of the capacitor is suggest by Siemens HQ expert.
For against 900MHz RF interference. The value of capacitor is 27pF.
For against 1800MHz RF interference. The value of capacitor is 10pF.
1nF/10nF value capacitor use for against ESD purpose.




Closed JSIM1

Quanta Computer Inc.
PROJECT : ZR7U

| Size | Document Number | Rev |
|---|---|---|
| | MINI PCI-E card/TV | 1A |

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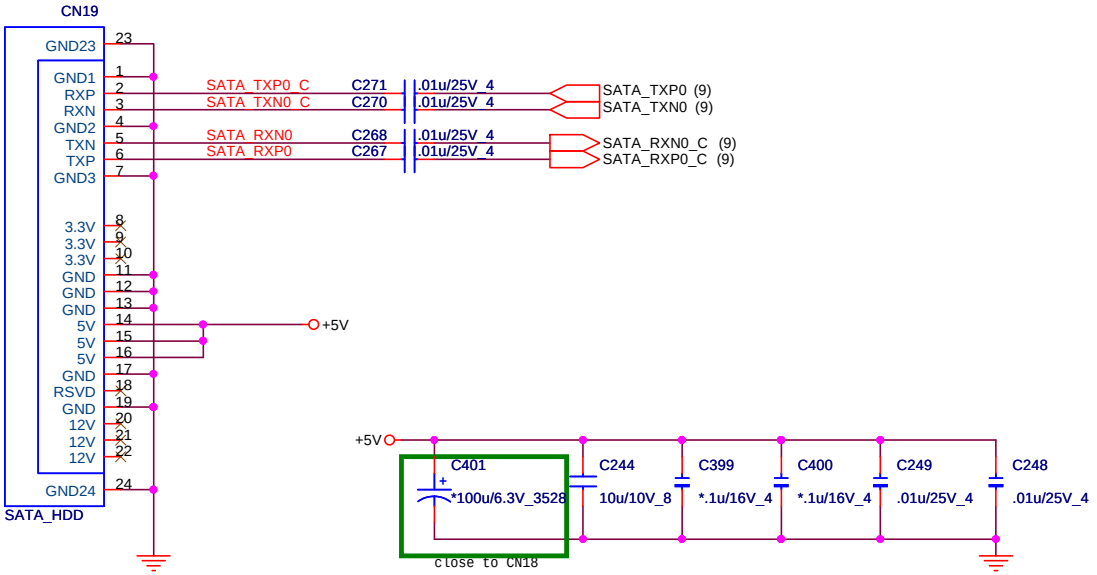
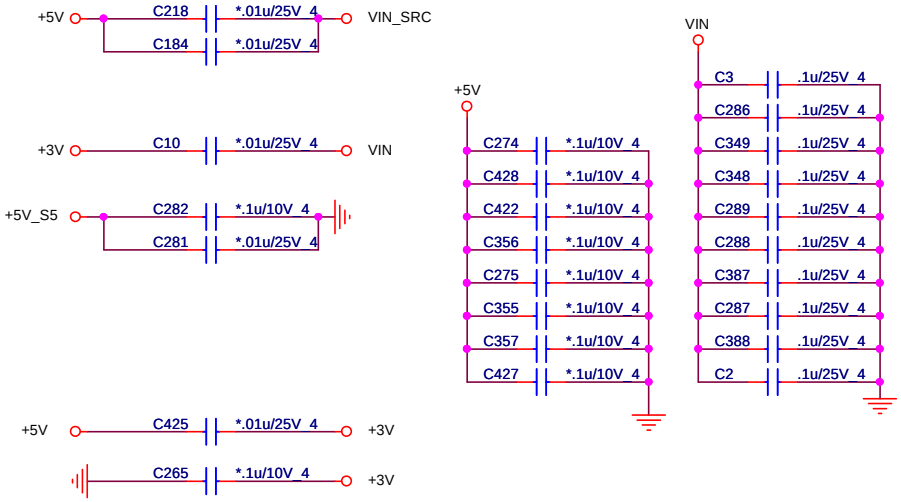
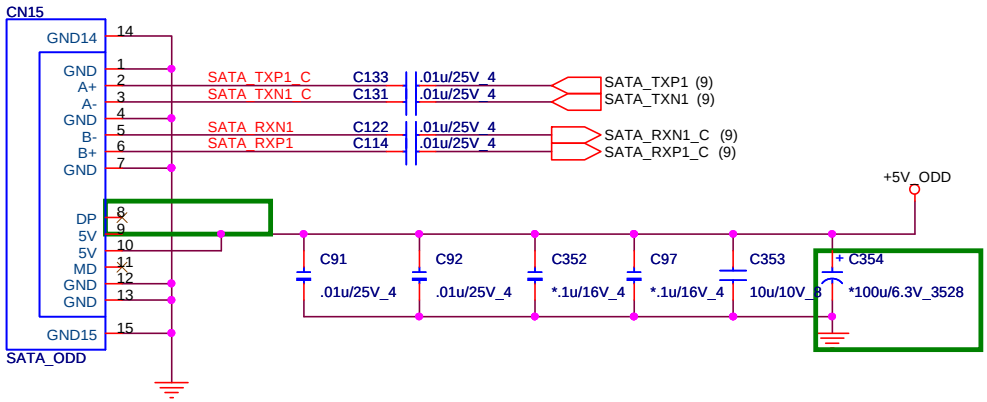
## MAIN SATA HDD



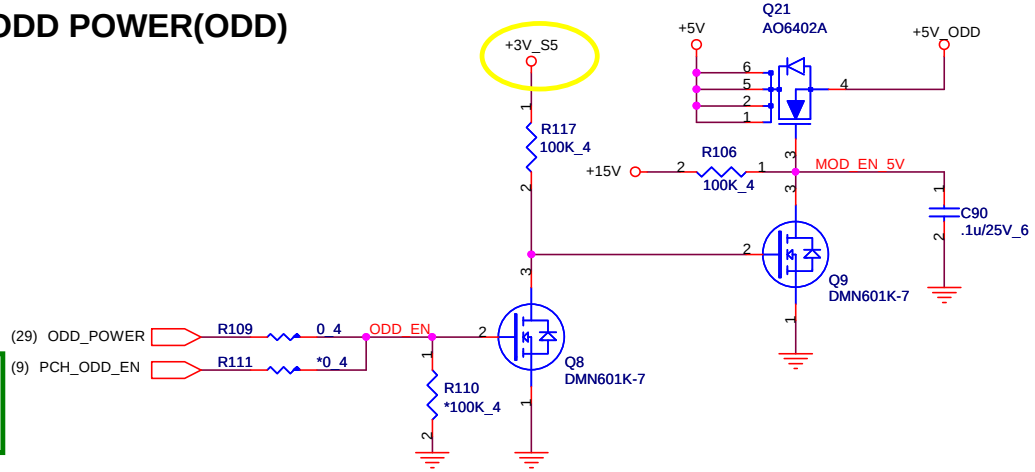

## EE RETURN-PATH CAPACITORS




## ODD (SATA)




## ODD POWER(ODD)

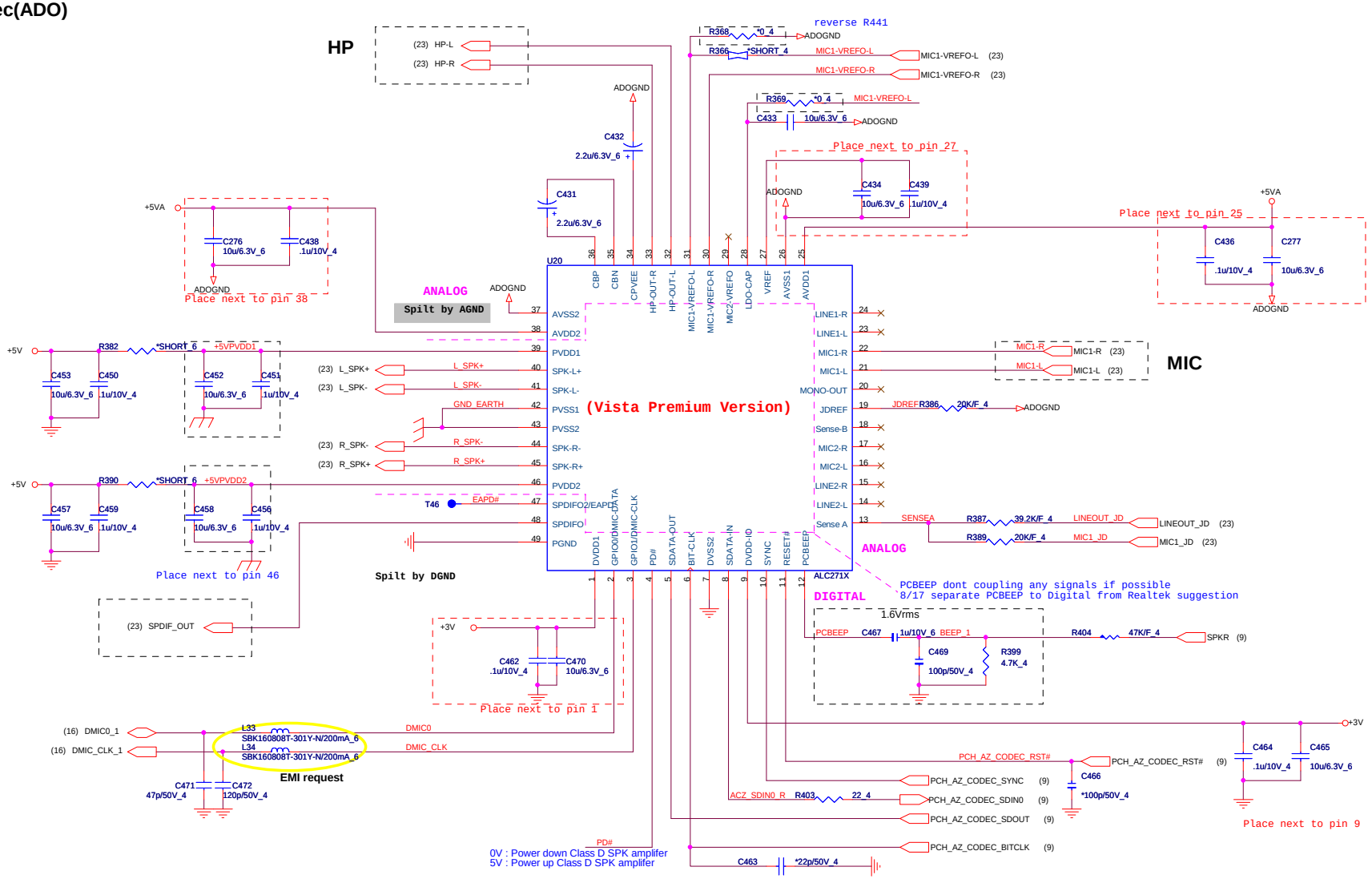



Quanta Computer Inc.

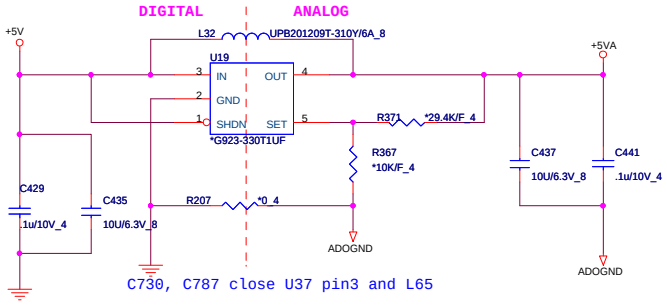
PROJECT : ZR7U

| Size | Document Number | Rev |
|---|---|---|
| | SATA-HDD/ODD/USB-ESATA | 1A |
| Date: Tuesday, April 20, 2010 | Sheet 21 of 38 | |

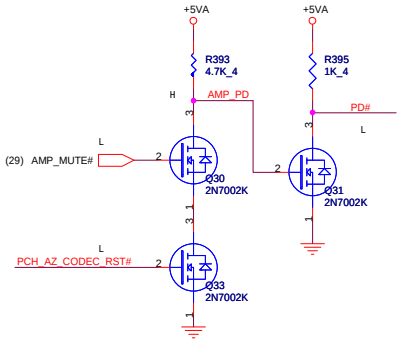
# Codec(ADO)




## Power (ADO)

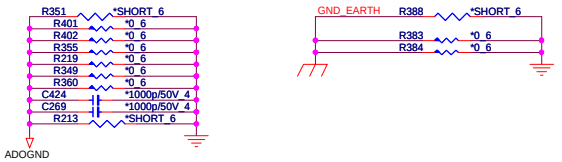



## Mute(ADO)



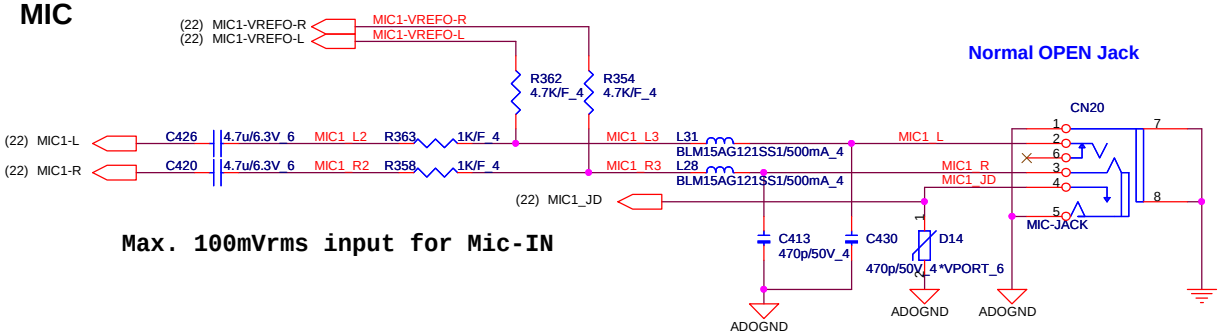

## Split-GND

GND_EARTH don't coupling AGND and SPK signals



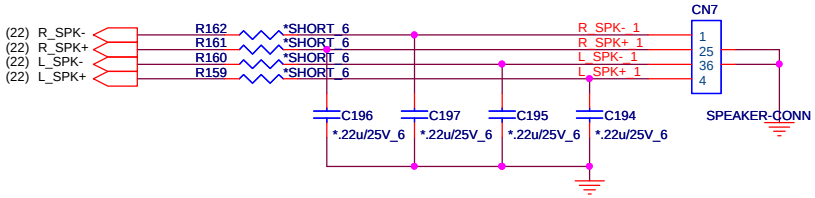

| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : ZR7U | | |
| Size | Document Number: REALTEK ALC663&888/MDC | Rev: 1A |
| Date: Thursday, April 22, 2010 | Sheet 22 of 38 | |

## MIC

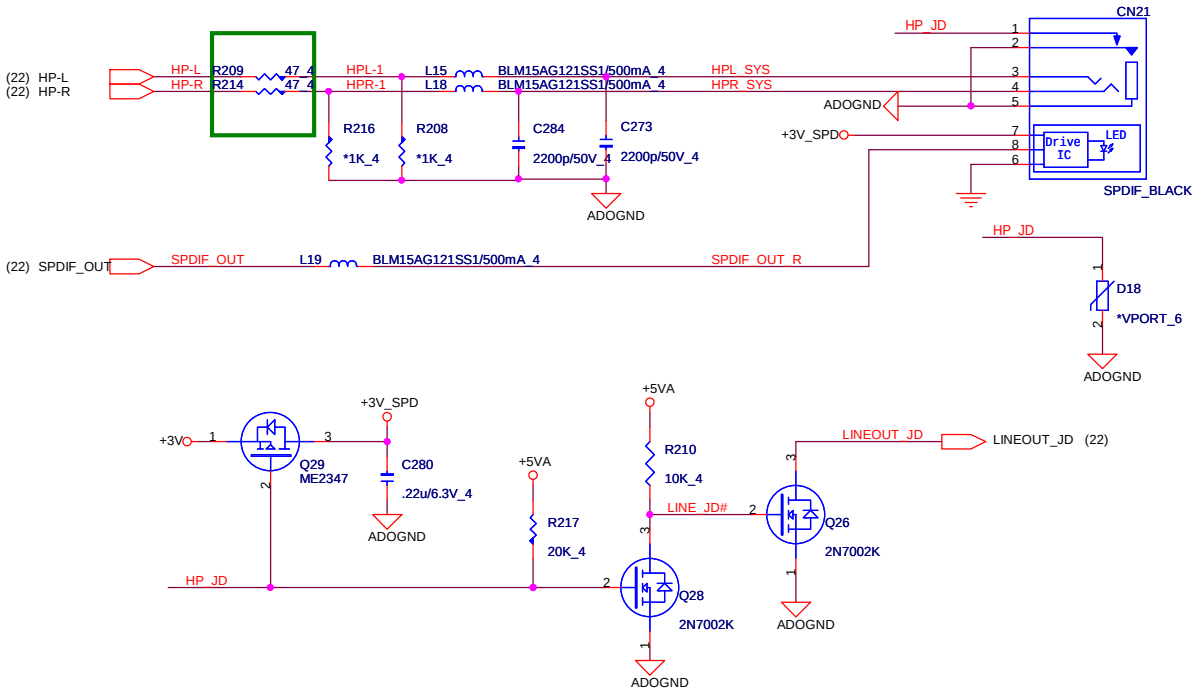



Max. 100mVrms input for Mic-IN

## Internal Speaker



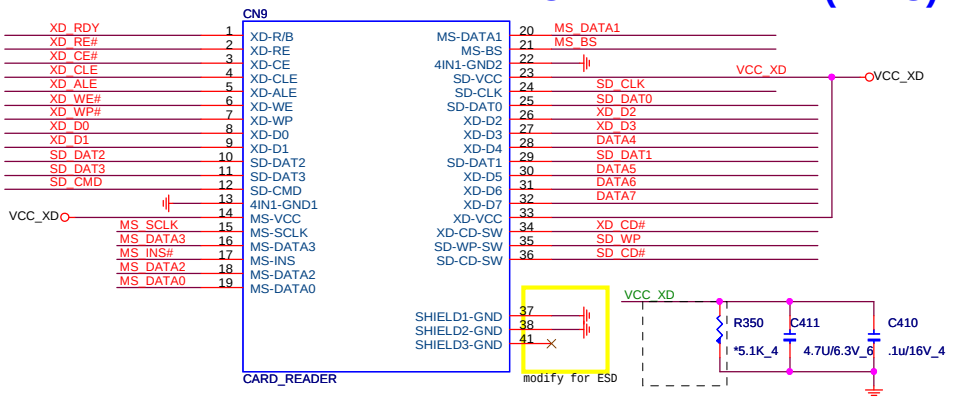

## HP/SPDIF



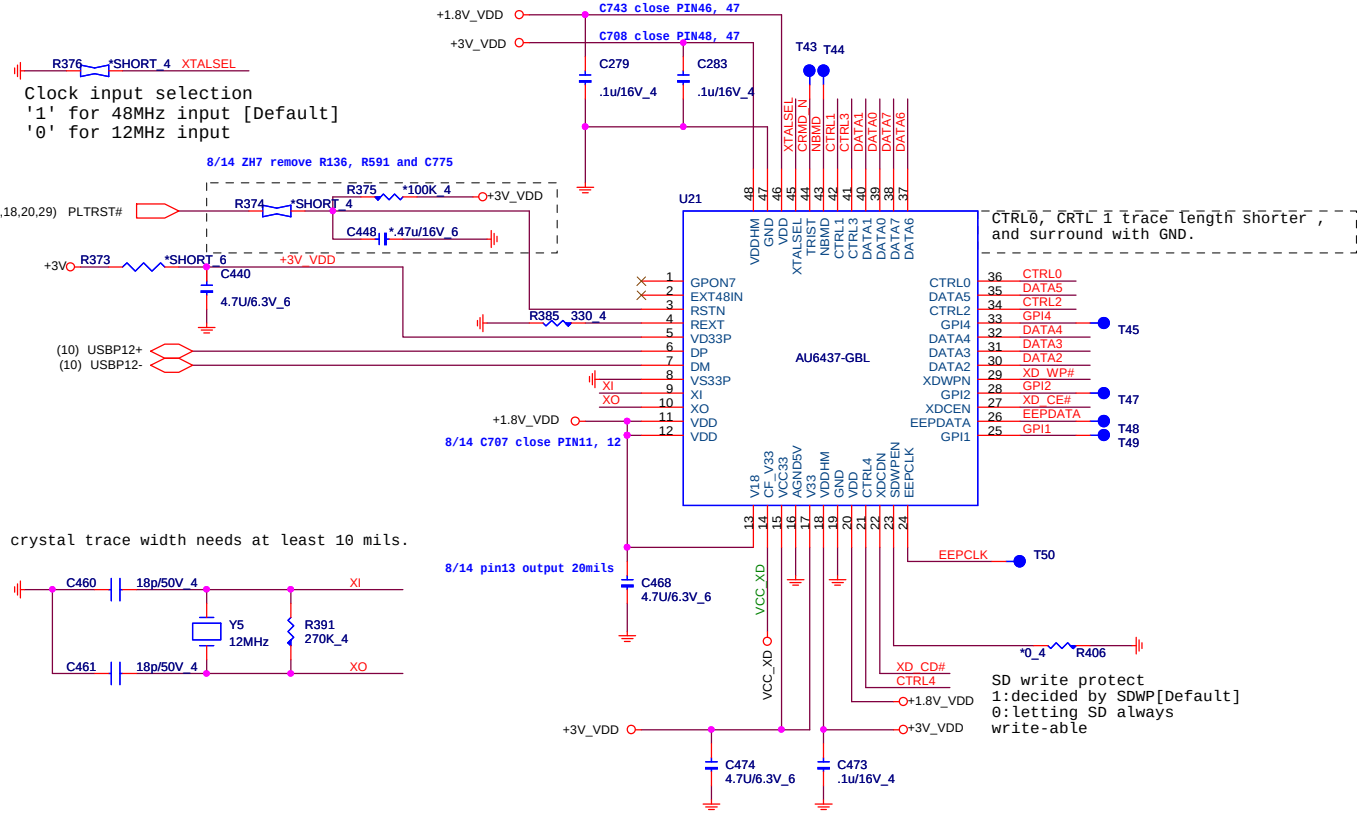

| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : ZR7U | | |
| Size | Document Number | Rev |
| | AMP /AUDIO JACK CONN | 1A |
| Date: Tuesday, April 20, 2010 | Sheet 23 of 38 | |

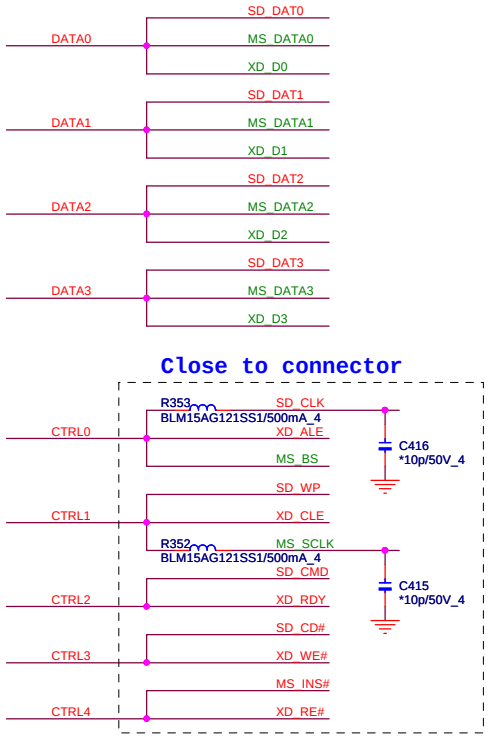
# CARD READER Controller

# 4 IN 1 CARD READER (MMC)



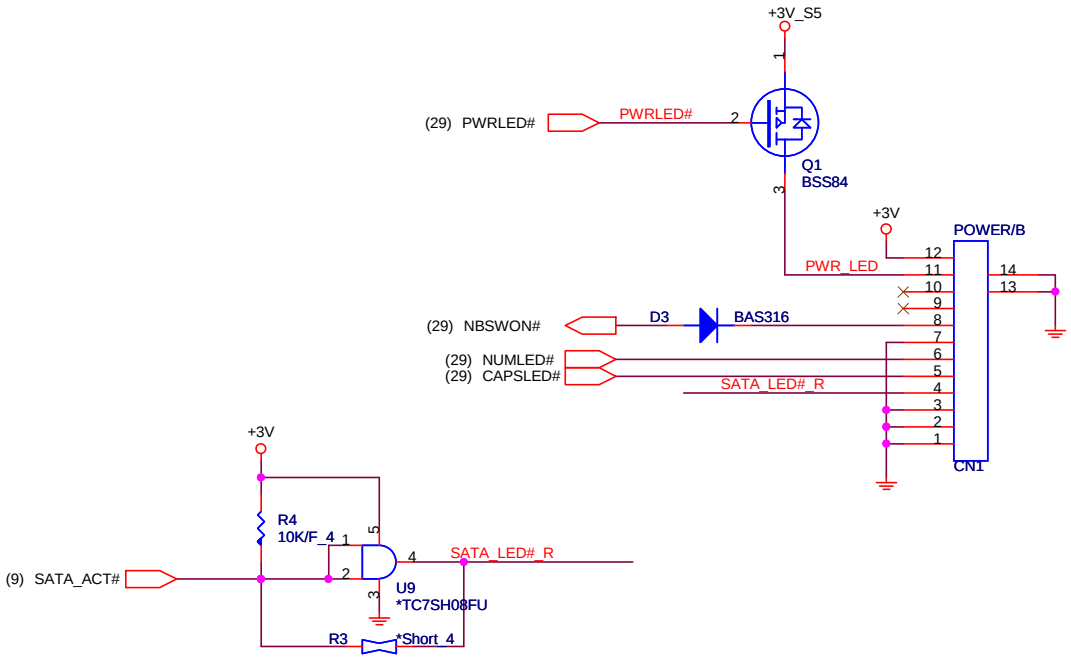

Close to CN14 pin 14 & pin23
4.7u CAP close to pin23



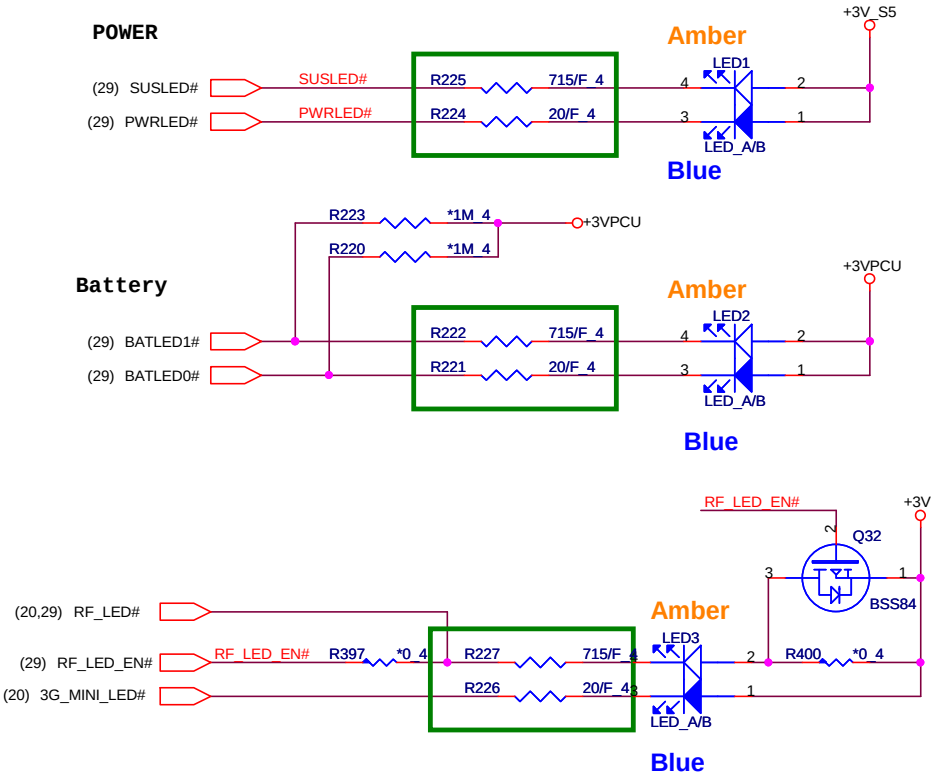




| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : ZR7U | | |
| Size | Document Number | Rev |
| | AU6433 CardReader | 1A |
| Date: Tuesday, April 20, 2010 | Sheet 24 of 38 | |

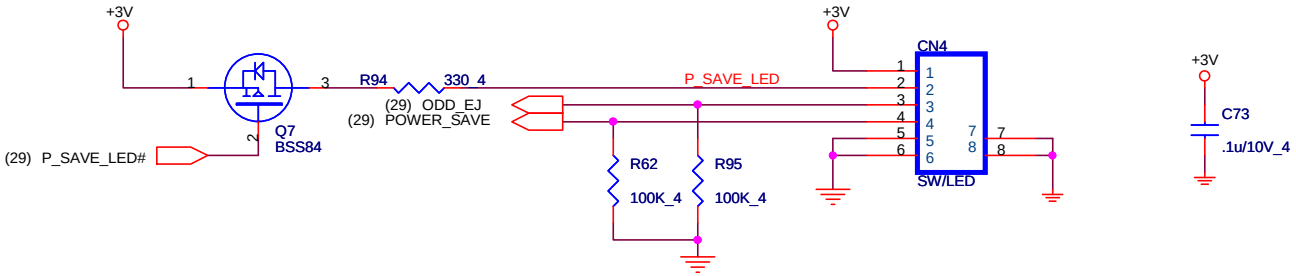
## POWER BOARD CONN(UIF)




## LED




## SW /B

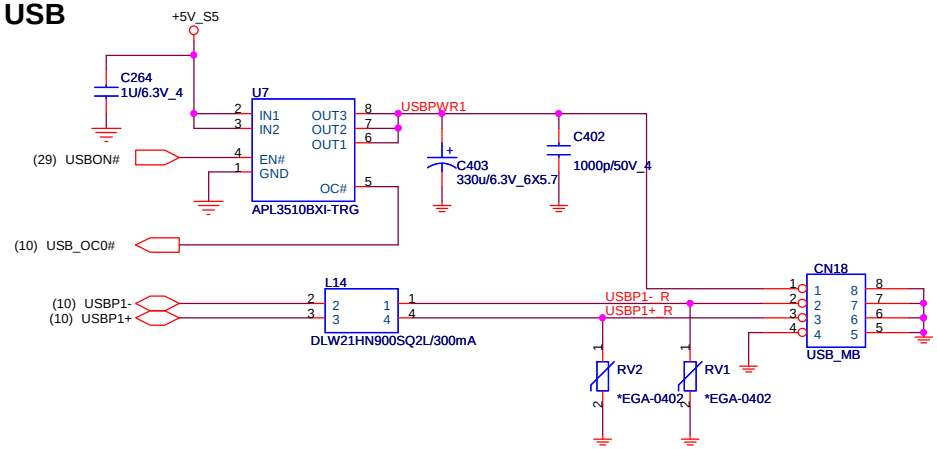



**Quanta Computer Inc.**

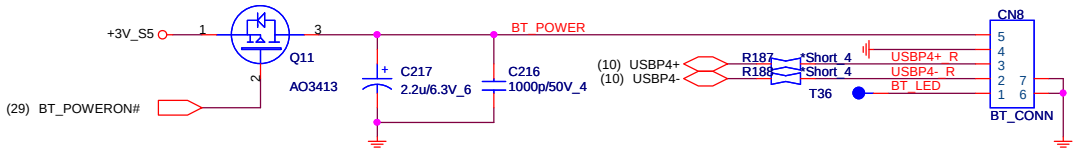
**PROJECT : ZR7U**

| Size | Document Number | Rev |
|---|---|---|
| | POWER/MMB/LAUNCH/LED | 1A |
| Date: Wednesday, April 21, 2010 | Sheet 25 of 38 | |

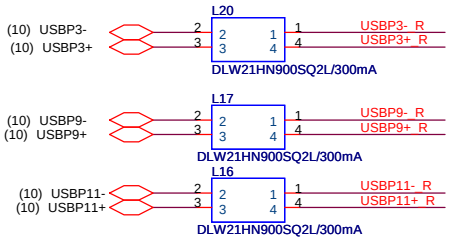
## USB

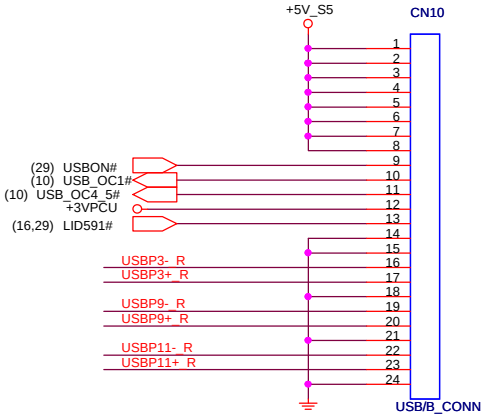



## BLUETOOTH CONNECTOR




## USB/B




Quanta Computer Inc.

PROJECT : ZR7U

| Size | Document Number | Rev |
|---|---|---|
| | USB/ BT | 1A |

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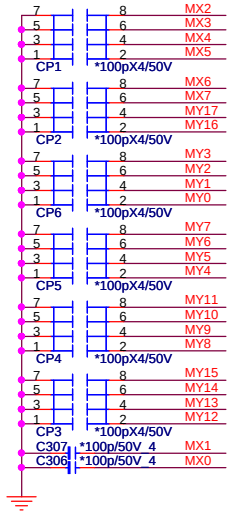
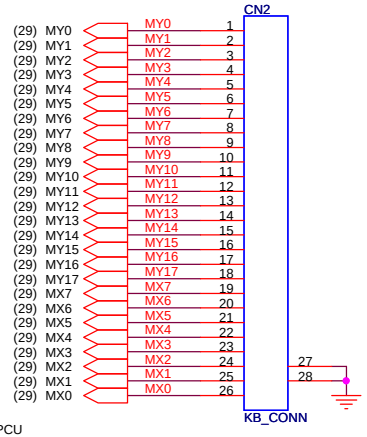
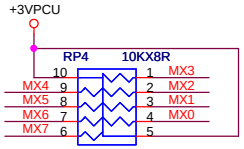
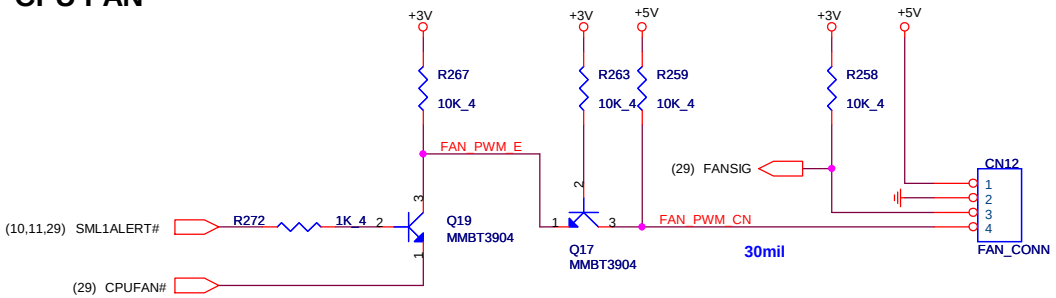
## K/B



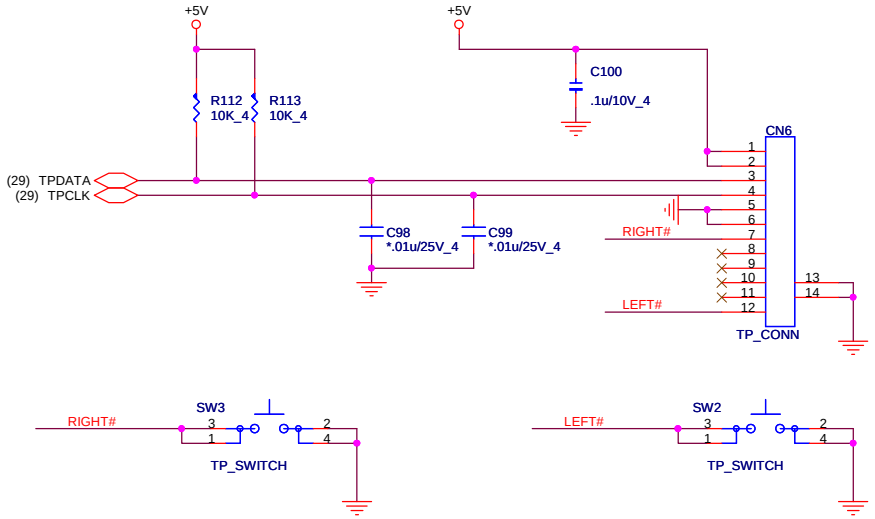



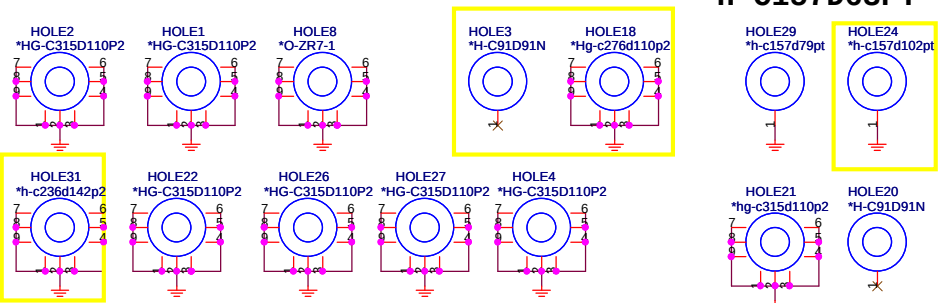

## CPU FAN



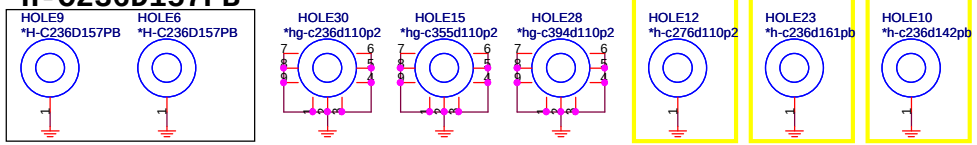

## TOUCHPAD & Switch CONN.



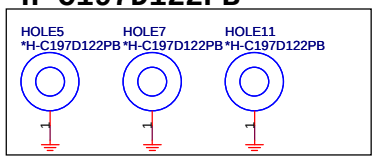

## H-C157D63PT



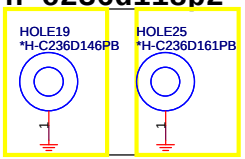

## H-C236D157PB



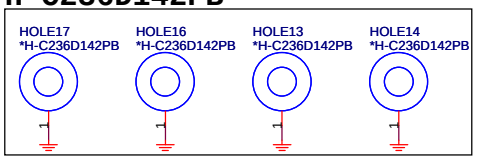

## H-C197D122PB




## h-c236d118p2




## H-C236D142PB




| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : ZR7U | | |
| Size | Document Number | Rev |
| | KB/FAN/TP+FP | 1A |
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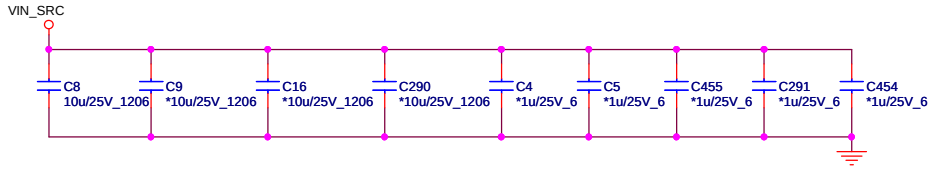
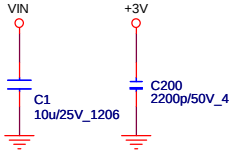
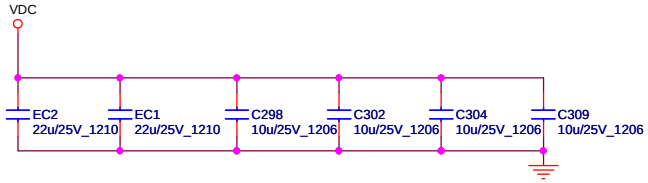
## EMI decoupling

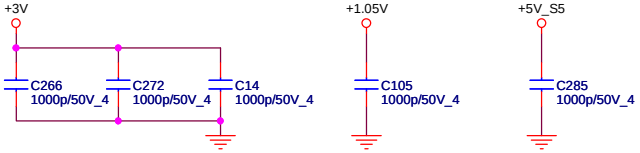


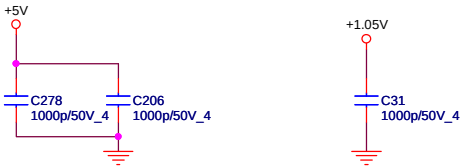




## EMI ISN solution

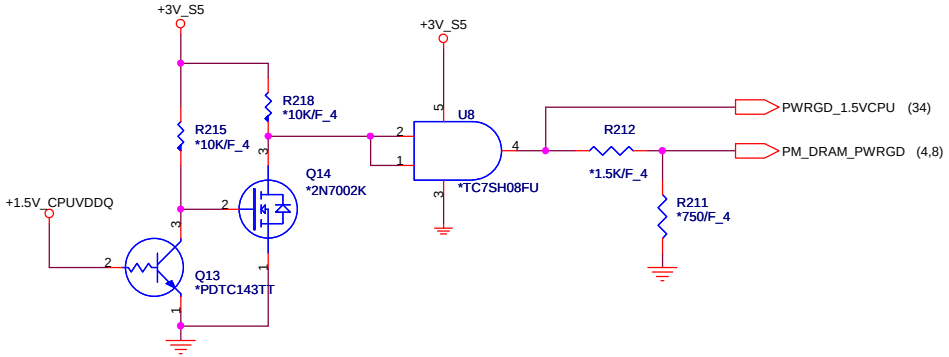


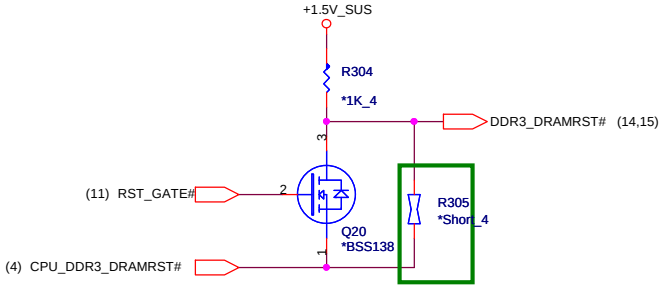

## EMI decoupling

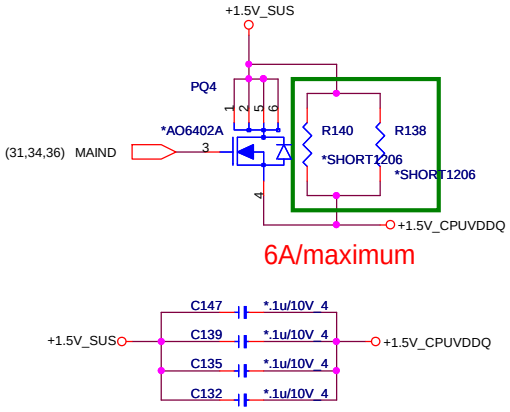


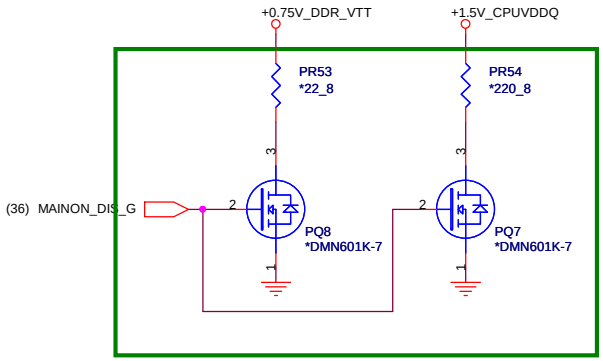




## Intel S3 leakage circuit



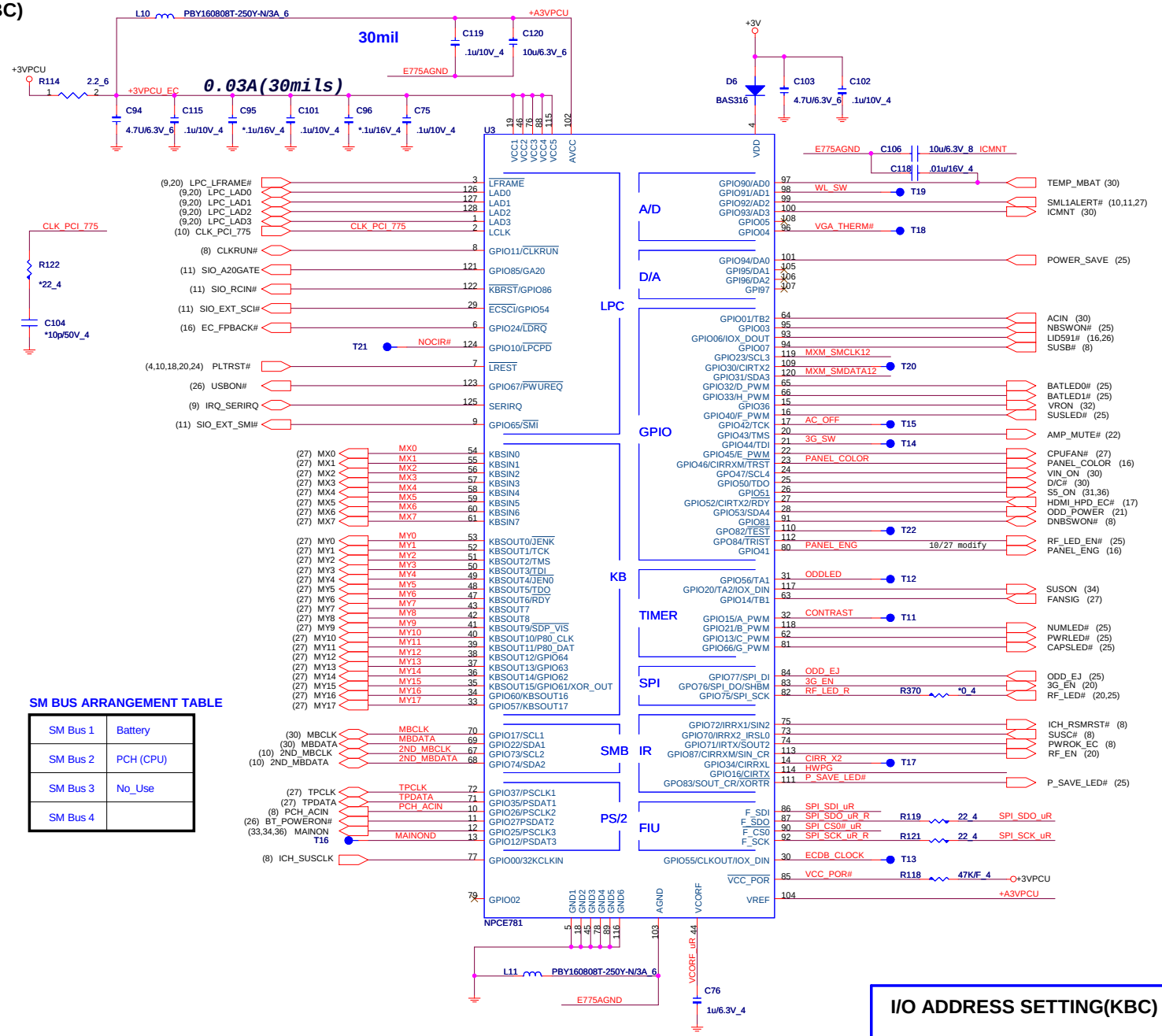




| | | |
|---|---|---|
| Quanta Computer Inc. PROJECT : ZR7U | | |
| Size | Document Number: S3 power saving | Rev: 1A |
| Date: Tuesday, April 20, 2010 | Sheet 28 of 38 | |

# EC(KBC)




## SM BUS ARRANGEMENT TABLE

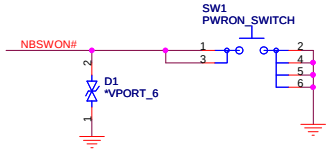
| | |
|---|---|
| SM Bus 1 | Battery |
| SM Bus 2 | PCH (CPU) |
| SM Bus 3 | No_Use |
| SM Bus 4 | |

## I/O ADDRESS SETTING(KBC)

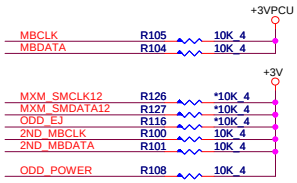
SHBM=0: Enable shared memory with host BIOS


Non-sharing ROM

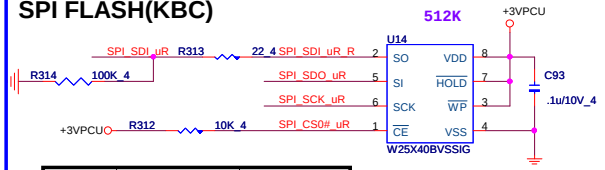
## POWER-ON Switch(KBC)




## SM BUS PU(KBC)

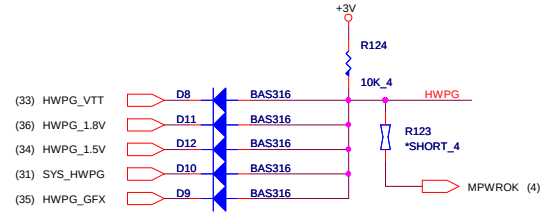



## SPI FLASH(KBC)




| Vendor | Vendor P/N | Quanta P/N |
|---|---|---|
| Winbond | W25X40BVSSIG | AKE37FN0N01 |
| EON | EN25F40-100HIP | AKE37ZN0Q00 |
| AMIC | A25L040 | AKE37ZN0800 |

## HWPG(KBC)




Quanta Computer Inc.

PROJECT : ZR7U

| Size | Document Number | Rev |
|---|---|---|
| | WPCE781 & FLASH | 1A |

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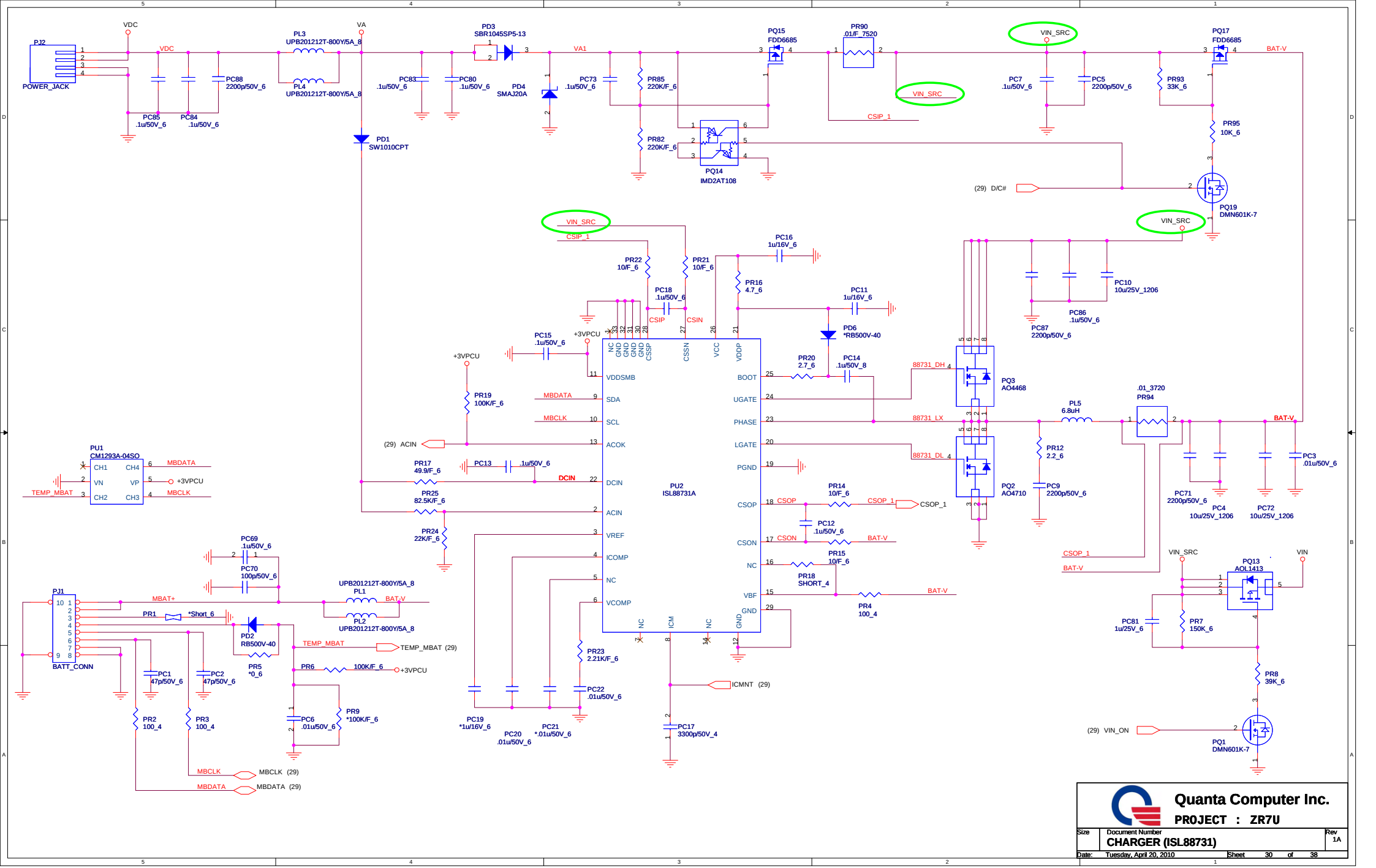
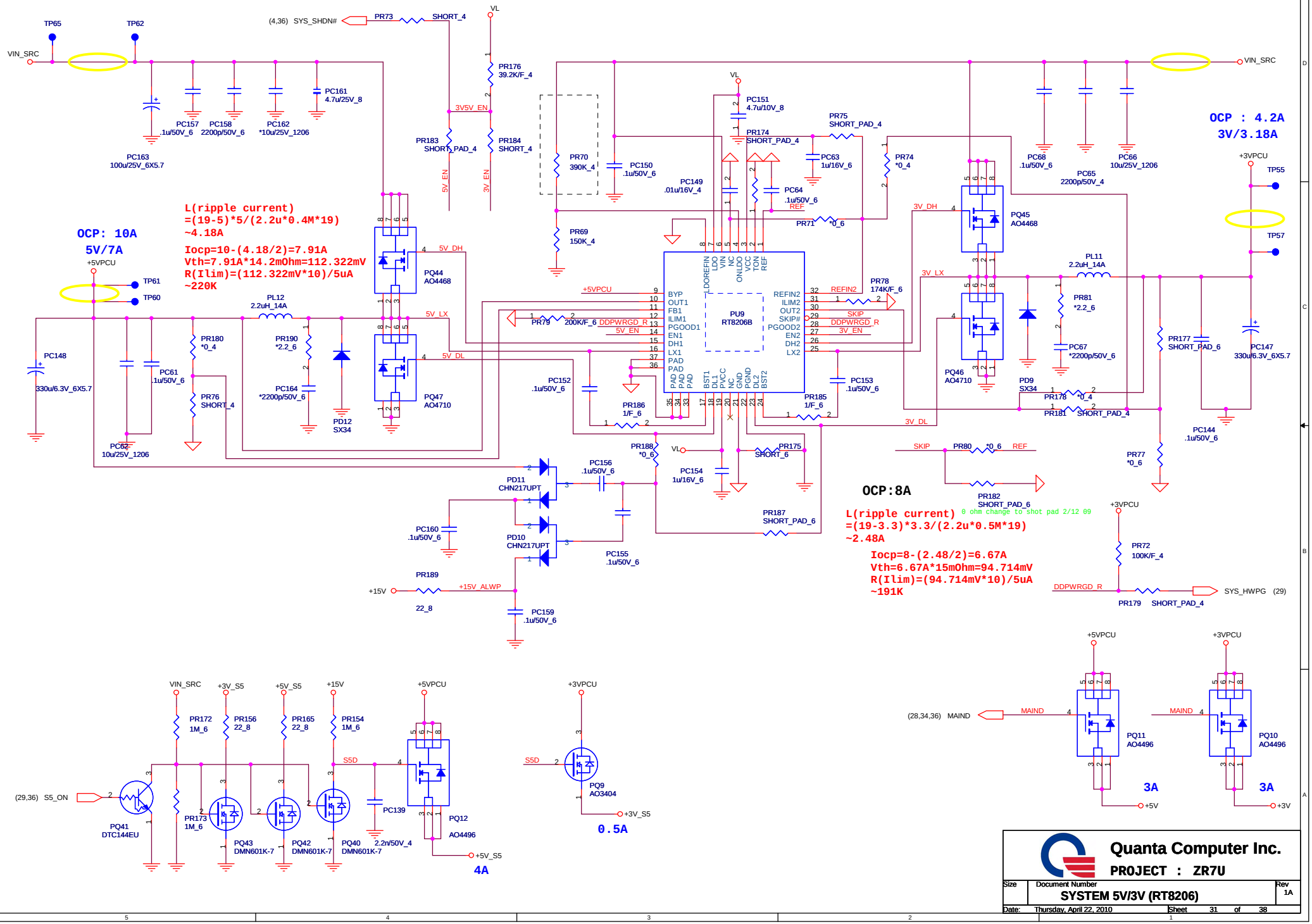



| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : ZR7U | | |
| Size | Document Number: CHARGER (ISL88731) | Rev: 1A |
| Date: Tuesday, April 20, 2010 | Sheet 30 of 38 | |


OCP : 4.2A
3V/3.18A
L(ripple current)
=(19-5)*5/(2.2u*0.4M*19)
~4.18A
Iocp=10-(4.18/2)=7.91A
Vth=7.91A*14.2mOhm=112.322mV
R(Ilim)=(112.322mV*10)/5uA
~220K
OCP: 10A
5V/7A
OCP:8A
L(ripple current)
=(19-3.3)*3.3/(2.2u*0.5M*19)
~2.48A
Iocp=8-(2.48/2)=6.67A
Vth=6.67A*15mOhm=94.714mV
R(Ilim)=(94.714mV*10)/5uA
~191K
0 ohm change to shot pad 2/12 09
PU9
RT8206B
PQ44
AO4468
PQ45
AO4468
PQ46
AO4710
PQ47
AO4710
PQ41
DTC144EU
PQ42
DMN601K-7
PQ43
DMN601K-7
PQ40
DMN601K-7
PQ12
AO4496
PQ9
AO3404
PQ11
AO4496
PQ10
AO4496
PD10
CHN217UPT
PD11
CHN217UPT
PD12
SX34
PD9
SX34
PL11
2.2uH_14A
PL12
2.2uH_14A
0.5A
3A
3A
4A
Quanta Computer Inc.
PROJECT : ZR7U
SYSTEM 5V/3V (RT8206)
Size
Document Number
Rev
1A
Date: Thursday, April 22, 2010
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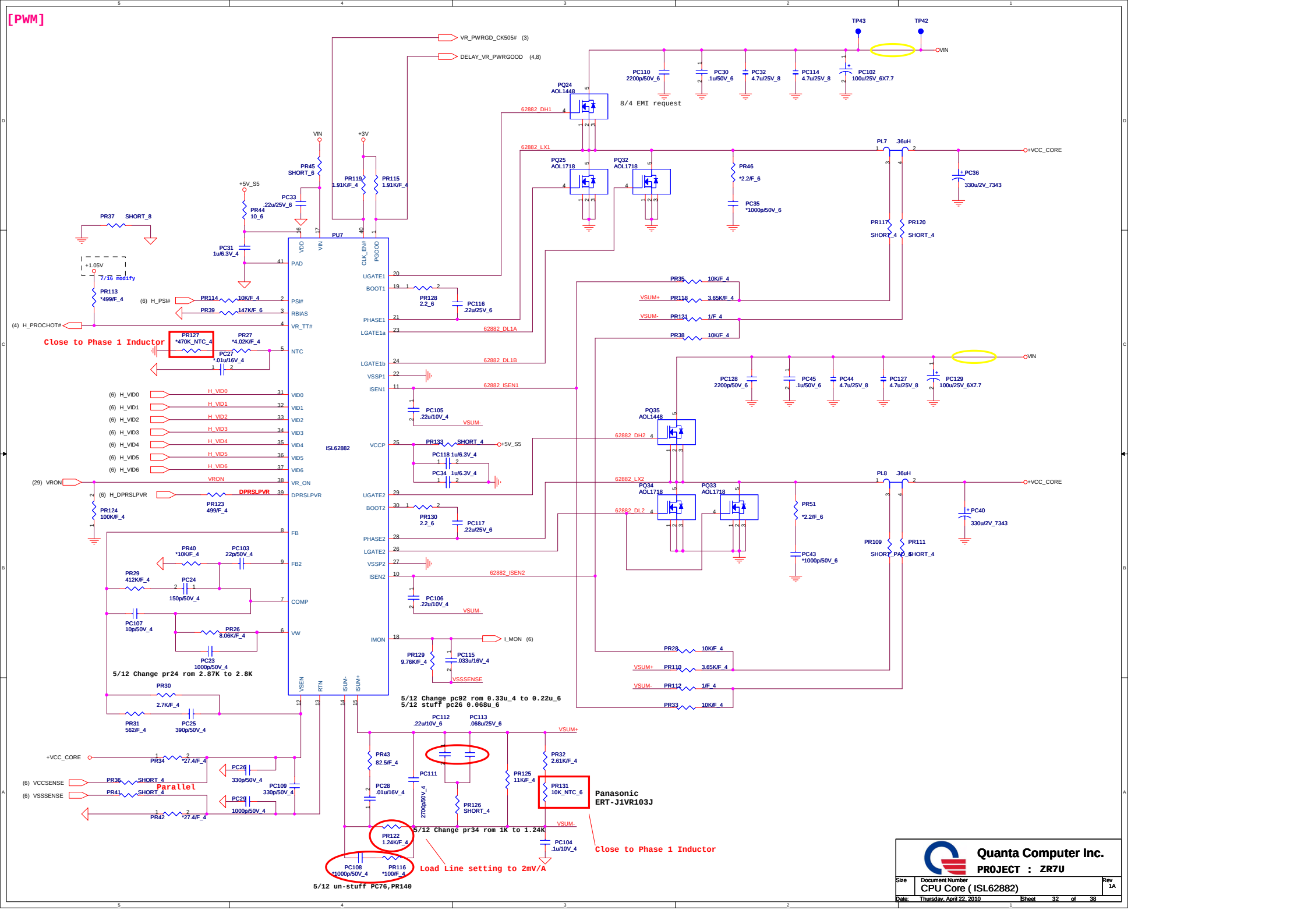
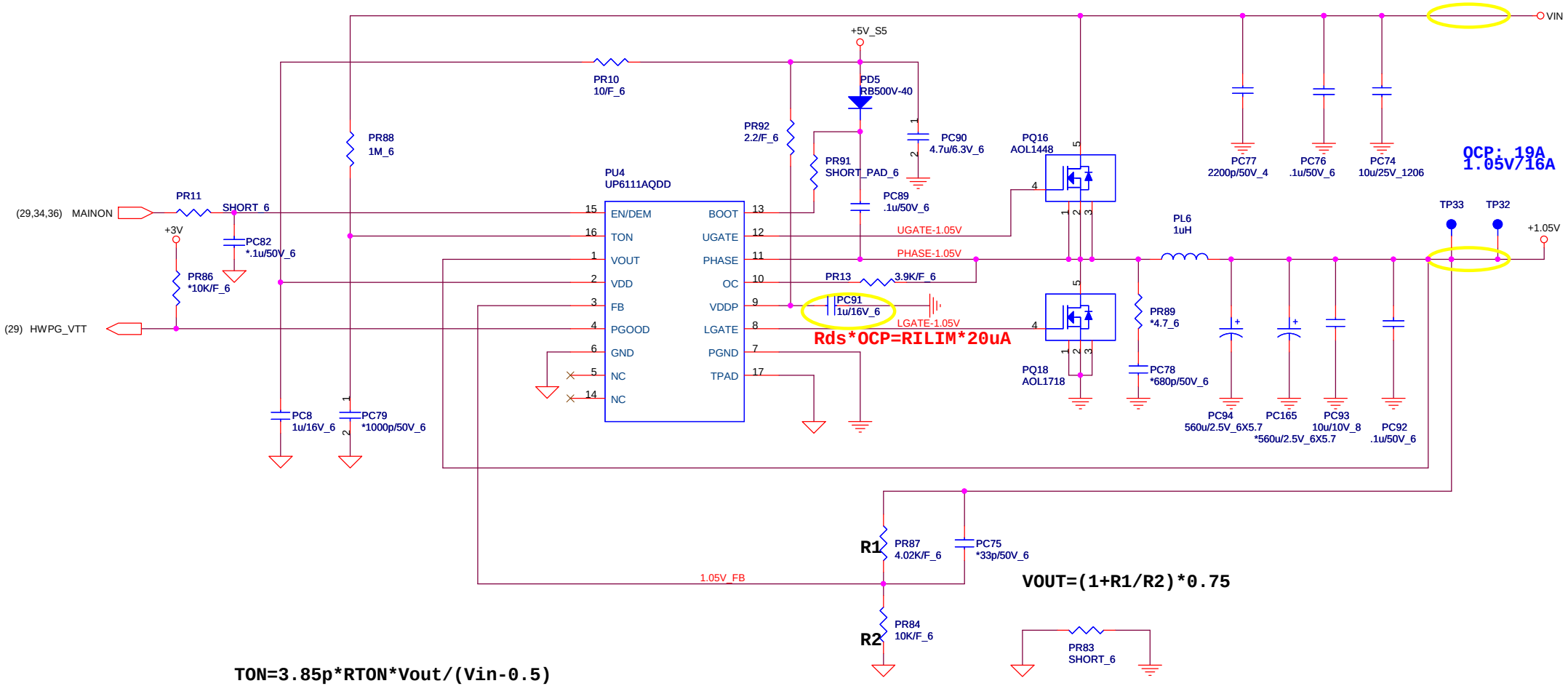

[PWM]
ISL62882
PU7
Close to Phase 1 Inductor
Parallel
Panasonic
ERT-J1VR103J
Close to Phase 1 Inductor
Load Line setting to 2mV/A
5/12 Change pr24 rom 2.87K to 2.8K
5/12 Change pc92 rom 0.33u_4 to 0.22u_6
5/12 stuff pc26 0.068u_6
5/12 Change pr34 rom 1K to 1.24K
5/12 un-stuff PC76,PR140
8/4 EMI request
7/16 modify
Quanta Computer Inc.
PROJECT : ZR7U
CPU Core ( ISL62882)
Thursday, April 22, 2010




TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

AO4710 Rdson=11.7~14.2mOhm

L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.646A

14.2m*10=RILIM*20uA
RILIM=7.1K--- 7.15K

| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : ZR7U | | |
| Size | Document Number: VCCP 1.05V(UP6111A) | Rev: 1A |
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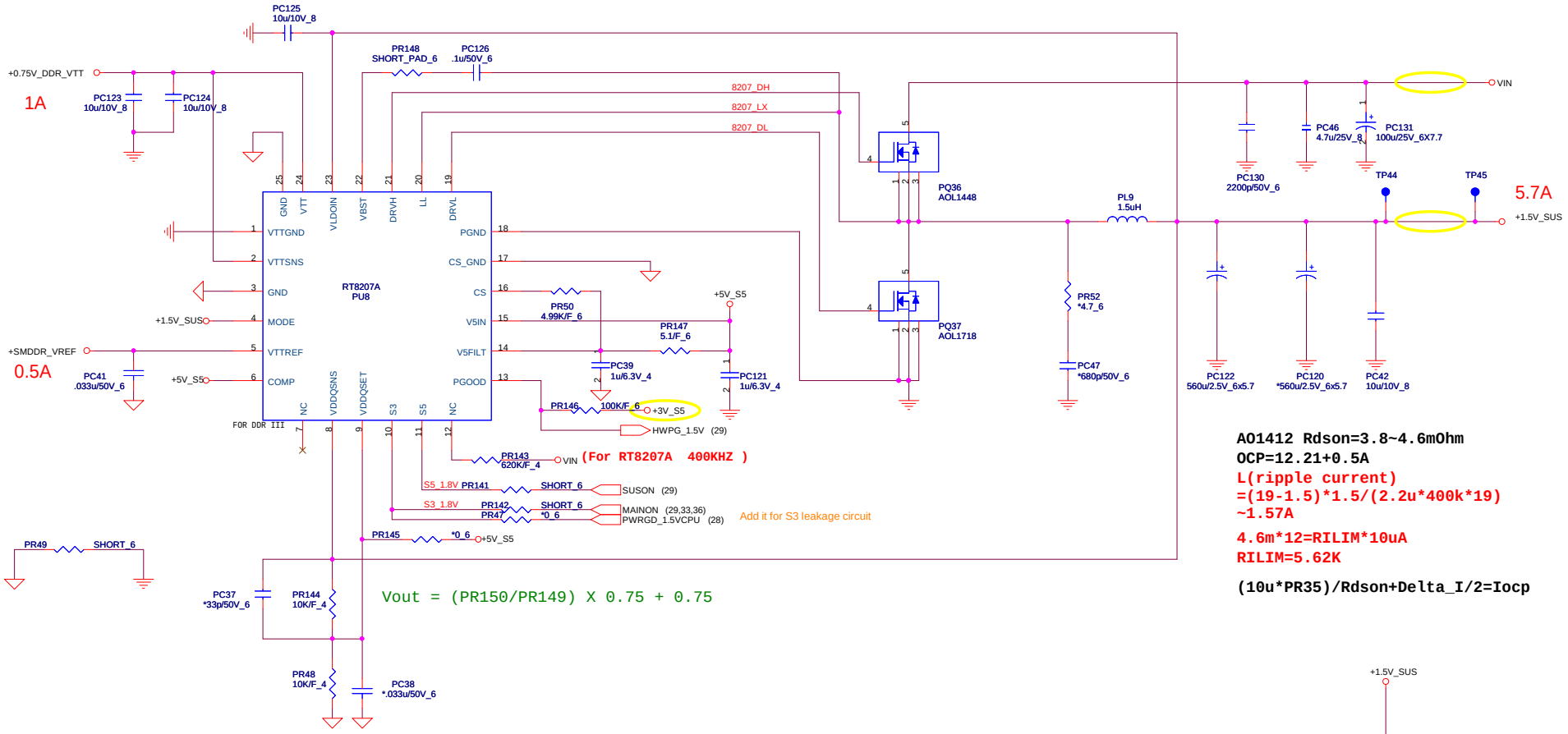
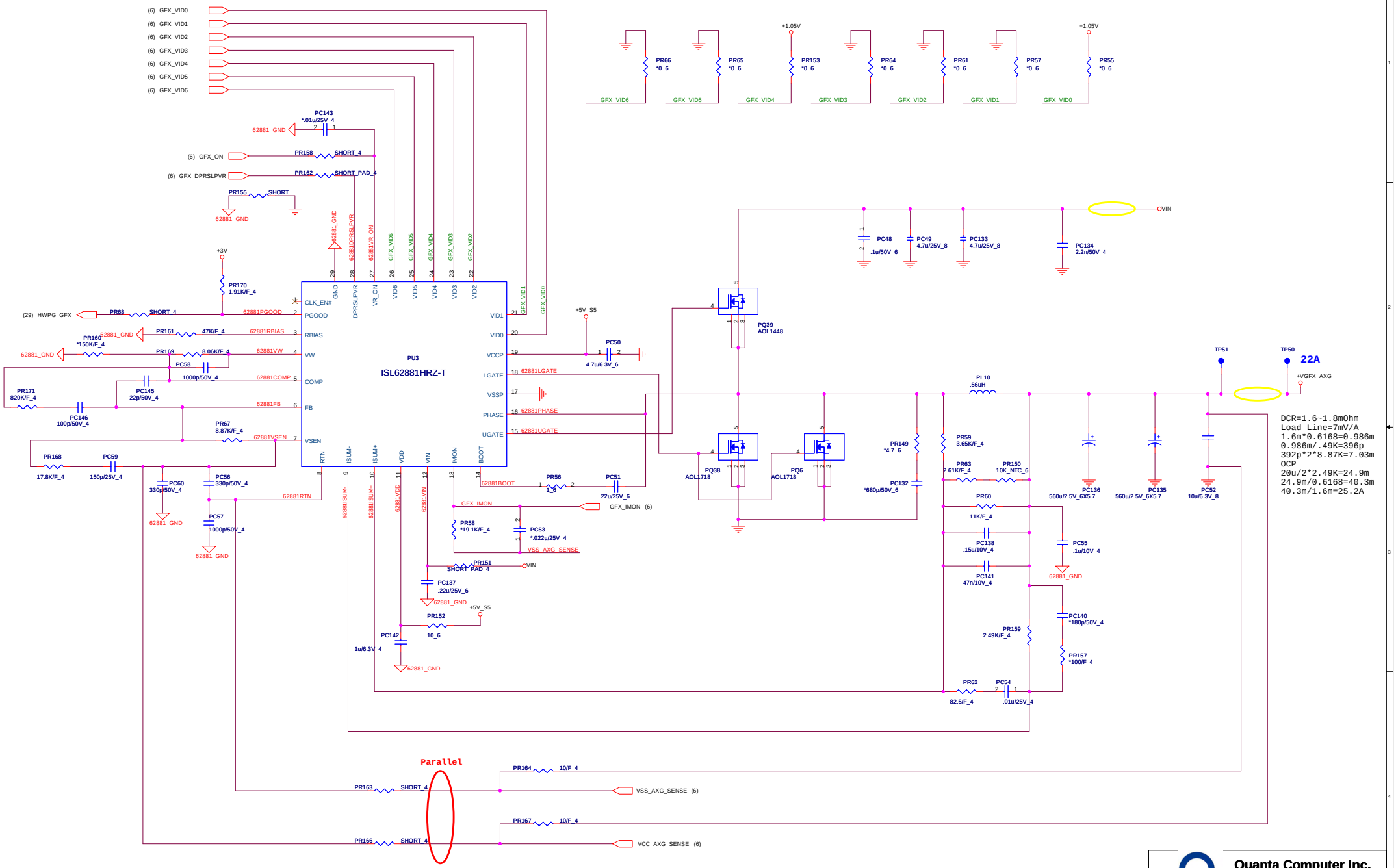



| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : ZR7U | | |
| Size | Document Number: DDR III 1.5V(TPS51116) | Rev: 1A |
| Date: Thursday, April 22, 2010 | Sheet 34 of 38 | |

# Int_VGA [PWM]




1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

Quanta Computer Inc.
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| Size | Document Number | Rev |
|---|---|---|
| | +VGFX_AXG (ISL62881) | 1A |

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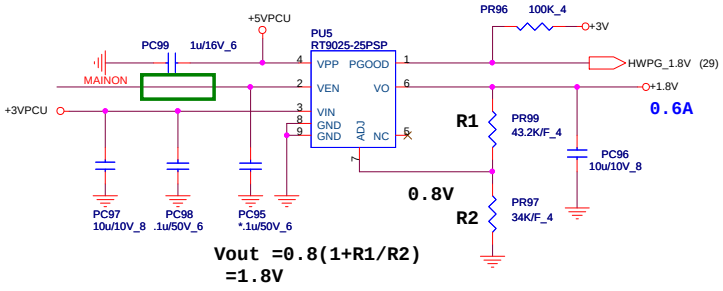


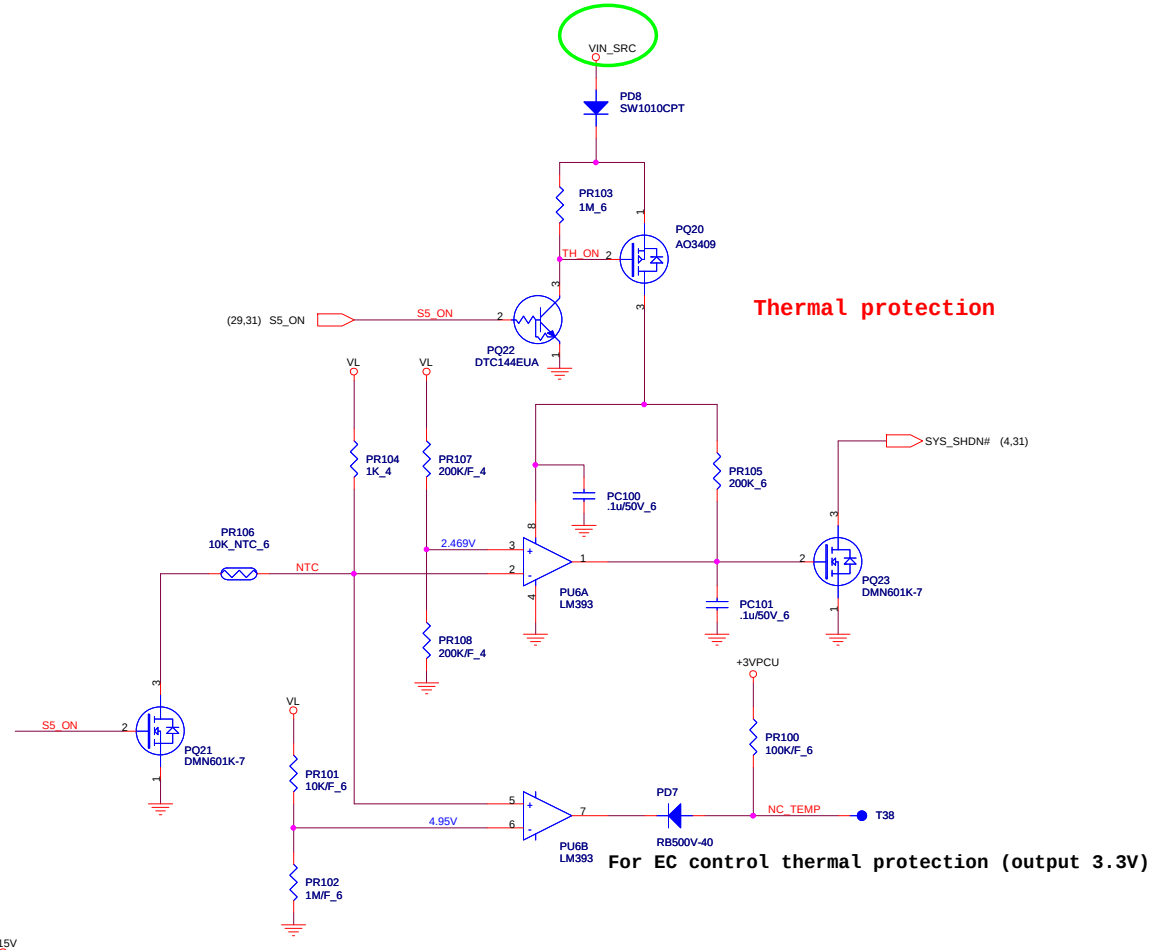


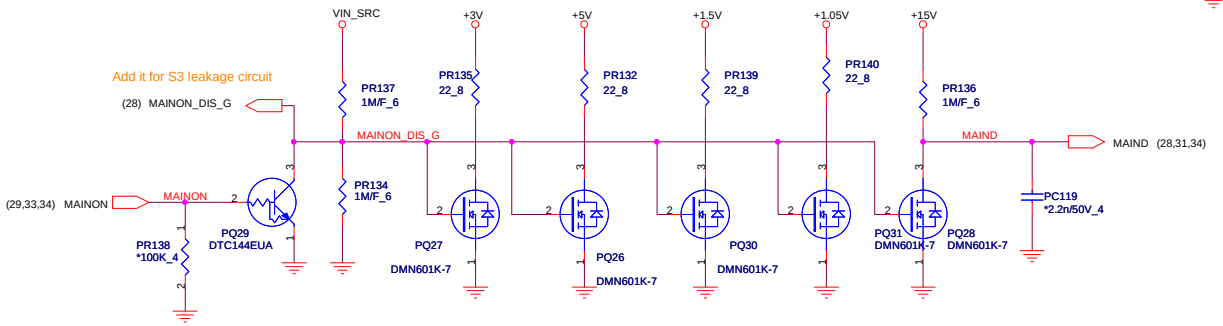


Quanta Computer Inc.

PROJECT : ZR7U

| Size | Document Number | Rev |
|---|---|---|
| | Discharge/1.8V/Thermal protection | 1A |

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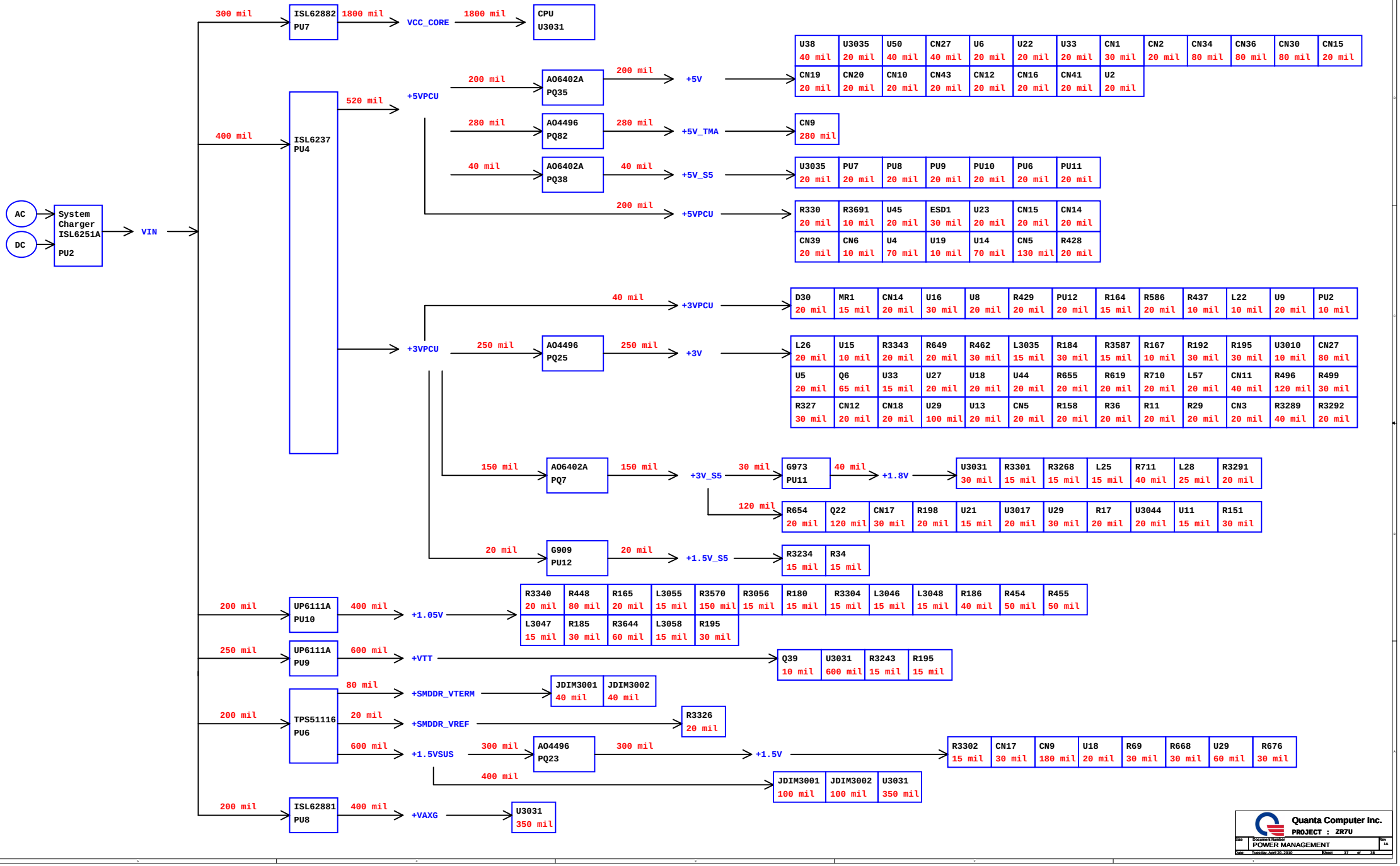
AC
DC
System Charger ISL6251A
PU2
VIN
300 mil
ISL62882 PU7
1800 mil
VCC_CORE
1800 mil
CPU U3031
400 mil
ISL6237 PU4
520 mil
+5VPCU
200 mil
AO6402A PQ35
200 mil
+5V
U38 40 mil
U3035 20 mil
U50 40 mil
CN27 40 mil
U6 20 mil
U22 20 mil
U33 20 mil
CN1 30 mil
CN2 20 mil
CN34 80 mil
CN36 80 mil
CN30 80 mil
CN15 20 mil
CN19 20 mil
CN20 20 mil
CN10 20 mil
CN43 20 mil
CN12 20 mil
CN16 20 mil
CN41 20 mil
U2 20 mil
280 mil
AO4496 PQ82
280 mil
+5V_TMA
CN9 280 mil
40 mil
AO6402A PQ38
40 mil
+5V_S5
U3035 20 mil
PU7 20 mil
PU8 20 mil
PU9 20 mil
PU10 20 mil
PU6 20 mil
PU11 20 mil
200 mil
+5VPCU
R330 20 mil
R3691 10 mil
U45 20 mil
ESD1 30 mil
U23 20 mil
CN15 20 mil
CN14 20 mil
CN39 20 mil
CN6 10 mil
U4 70 mil
U19 10 mil
U14 70 mil
CN5 130 mil
R428 20 mil
40 mil
+3VPCU
D30 20 mil
MR1 15 mil
CN14 20 mil
U16 30 mil
U8 20 mil
R429 20 mil
PU12 20 mil
R164 15 mil
R586 20 mil
R437 10 mil
L22 10 mil
U9 20 mil
PU2 10 mil
+3VPCU
250 mil
AO4496 PQ25
250 mil
+3V
L26 20 mil
U15 10 mil
R3343 20 mil
R649 20 mil
R462 30 mil
L3035 15 mil
R184 30 mil
R3587 15 mil
R167 10 mil
R192 30 mil
R195 30 mil
U3010 10 mil
CN27 80 mil
U5 20 mil
Q6 65 mil
U33 15 mil
U27 20 mil
U18 20 mil
U44 20 mil
R655 20 mil
R619 20 mil
R710 20 mil
L57 20 mil
CN11 40 mil
R496 120 mil
R499 30 mil
R327 30 mil
CN12 20 mil
CN18 20 mil
U29 100 mil
U13 20 mil
CN5 20 mil
R158 20 mil
R36 20 mil
R11 20 mil
R29 20 mil
CN3 20 mil
R3289 40 mil
R3292 20 mil
150 mil
AO6402A PQ7
150 mil
+3V_S5
30 mil
G973 PU11
40 mil
+1.8V
U3031 30 mil
R3301 15 mil
R3268 15 mil
L25 15 mil
R711 40 mil
L28 25 mil
R3291 20 mil
120 mil
R654 20 mil
Q22 120 mil
CN17 30 mil
R198 20 mil
U21 15 mil
U3017 20 mil
U29 30 mil
R17 20 mil
U3044 20 mil
U11 15 mil
R151 30 mil
20 mil
G909 PU12
20 mil
+1.5V_S5
R3234 15 mil
R34 15 mil
200 mil
UP6111A PU10
400 mil
+1.05V
R3340 20 mil
R448 80 mil
R165 20 mil
L3055 15 mil
R3570 150 mil
R3056 15 mil
R180 15 mil
R3304 15 mil
L3046 15 mil
L3048 15 mil
R186 40 mil
R454 50 mil
R455 50 mil
L3047 15 mil
R185 30 mil
R3644 60 mil
L3058 15 mil
R195 30 mil
250 mil
UP6111A PU9
600 mil
+VTT
Q39 10 mil
U3031 600 mil
R3243 15 mil
R195 15 mil
200 mil
TPS51116 PU6
80 mil
+SMDDR_VTERM
JDIM3001 40 mil
JDIM3002 40 mil
20 mil
+SMDDR_VREF
R3326 20 mil
600 mil
+1.5VSUS
300 mil
AO4496 PQ23
300 mil
+1.5V
R3302 15 mil
CN17 30 mil
CN9 180 mil
U18 20 mil
R69 30 mil
R668 30 mil
U29 60 mil
R676 30 mil
400 mil
JDIM3001 100 mil
JDIM3002 100 mil
U3031 350 mil
200 mil
ISL62881 PU8
400 mil
+VAXG
U3031 350 mil
Quanta Computer Inc.
PROJECT : ZR7U
Size
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POWER MANAGEMENT
Rev
1A
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| Model | REV | CHANGE LIST |
|---|---|---|
| ZR7U MB | 1A | 2/11 1. Del trace VREF_DQ_DIMM0/VREF_DQ_DIMM1, and R131,R127,R116,R129<br>2. Add two test point (TP35/TP36)<br>3. Remove D16, and connect to EC directly by Anda confirmed<br>2/12 1. Add Q44/Q45/R600 for AMP_PWR_DOWN function<br>2/22 1. Change C630/C516 to VIN_SRC<br>2. Change R489, R488 P/N to 5%<br>3. Change PL18 footprint by power engineer<br>4. Del R190,R217,R218 and Add JP1007<br>5. Change R7643, R7646 P/N to 4.7K 5%<br>6. Remove 0ohm and short PAD R482,R7575, R7576,R7562, R7565<br>2/23 1. Del C791,C794,T77,T79 for layout requirement<br>2. Swap USB_OC0#,USB_OC2# ,USB_OC6#,USB_OC4_5#for layout requirement<br>3. Change C763,C767 for cost down<br>4. Change Y7000 P/N and footprint for cost down<br>2/25 1. Stuff R166 for vender commend<br>2. Del R171,R203 for layout requirement<br>3. Add C781,C782,C785,C786,C787,C788,C791,C794 for EMI decoupling cap<br>3/02 1. Correct Function Code<br>2. Change C656,C702,C7798 P/N and Footprint<br>3/04 1. Change PC218,PC61,PC164,PC74,PC176,PC76,PC180,PC79,PC182 P/N and Footprint for Power design change<br>2. Layout reference rename |
| | | 3/22 1. Del TP63,TP64,TP46,TP47,TP29,TP48,TP49,TP53,TP30,TP52,<br>JP1,JP2,JP3,JP4,JP5JP6,JP7,JP8,JP9,JP10,JP11,JP12,JP13 for remove current test components_All<br>2. PR146, R117 link to +_3V_S5 for power sequence_P34<br>3. Unstuff SW1 on board power switch_P29<br>4. Change 0ohm to short pad R45,R48,R54,R247,R35,R87,R86,R257,R1,R2,R61,43,<br>R11,R59,R290.R30,R28,R29,R98,R3,R187,R188_All<br>5. Change netname +1.1V_VTT to +1.05V_All<br>6. Unstuff R237,R230,R228,Q15 and change CN11 for change RTC Battery type_P9<br>3/24 1. Reserve PC165 for +1.05V ripple_P33<br>2. PQ16 AOL1718 change to AOL1448_P33<br>3. PR78 182K/F change to 174K/F_P31<br>4. Add C475 for Monitor test_P12<br>5. Del U15 128k EEPROM_P29<br>3/25 1. Reserve C811,C812,C813,C814,C815,C816,C817,C818 for EMI 1G Hz_P19<br>2. Del R38, R41_P16 |
| | | 4/1 1. Change C295,C296 value to 27pF and 33pF for X'tal vender commend_P10<br>2. Add C300,C305 for HDMI signal quality_P12<br>3. Add C471,C472 to 47pF and 220pF for EMI solution _P22<br>4. Del C390,C354,C401,C303,C140 for cost down _All |
| | | 4/19 1. Change D16,D17 P/Nand fotprint for 5V power_P16,17<br>2. Remove R120 for don't need it _P21<br>3. Unstuff PQ7,PQ8,PR53,PR54 for leakage in S3 _P28<br>4. Remove 0 ohm:<br>* Remove PR98_P36<br>* Short R260,R269_P20<br>* Remove R377/R378/R379/R380/R381/R394/R405_P20<br>* Short L7,L8,L9<br>* Short R125<br>5. Change R209,R214 for Audio test_P23 |
| | | 4/20 1. Remove Q16/Q18/R268/R271 for no used_P20<br>2. Change R221,R222,R224,R225,R226,R227 value to fine turn the brightness_P25<br>3. Change C472 to 120pF for Audio requirement_P22 |

| MODEL | ZR7 FROM | ZR7 To |
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| DOC NO. | | | | | |
|---|---|---|---|---|---|
| | PROJECT MODEL : | ZR7U | APPROVED BY: | | DATE: 2010/? |
| | PART NUMBER: | | DRAWING BY: | | REVISON: 1A |

Quanta Computer Inc.
PROJECT : ZR7U
Change list
Size | Document Number | Rev 1A
Date: Thursday, April 22, 2010 | Sheet 38 of 38