ZQG SYSTEM DIAGRAM

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT

IV@ -----> iGPU / PWW control
SW@ -----> Switchable iGPU & dGPU
SWS@ -----> VRAM / Strap / BACO option
SP@ -----> Board ID / VBIOS option / CPU

DDR3- SODIMM2 PAGE 7
DDR3- SODIMM1 PAGE 6
DDR3 Channel A

AMD Brazos
Zacate TDP~18W
19mmX19mm 413pin BGA
PAGE 3,4,5

HDMI
CRT
LVDS
DIG
UMA/Muxless

HDMI PAGE 21
CRT PAGE 20
LVDS PAGE 20

PCI-Express 4X

ATI
Seymour XT
128-bit M2 Pkg
29mm X 29mm
PAGE 13~17

800MHz
VRAM DDR3
64MX16X4,64 bit
64MX16X8,128 bit
PAGE 19

VGA AMD Seymour XT

CPU (PROCHOT)
E.C. (CPUFAN#)
32.768KHz
25MHz

PWM FAN SCH. PAGE 30

CPU THERMAL SENSOR
(Reserve Only)
PAGE 4

CPU SideBand TemperatureSense I2C

HT3
1.8GHz

PCI-Expresss

AMD
Hudson-M1
23mmX23mm, 605pin BGA
TDP~4.7W
PAGE 8,9,10,11,12

P0 **LAN**
Atheros
AR8151L rev.B
(10/100/1000)
PAGE 22
25MHz

RJ45 PAGE 22

P2 **Mini PCI-E Card**
(Wireless LAN)
PAGE 23

SATA - HDD PAGE 24
SATA0 150MB
3 Gb/s

SATA - ODD PAGE 24
SATA1 150MB
3 Gb/s

P0 **USB2.0 Port**
on board x1
PAGE 28

P9 **Blue Tooth** PAGE 28

P13 **Web-Camera** PAGE 20

P44 **USB BOARD**
USB2.0 Ports x3
PAGE 28

P4 **Mini Card**
WLAN & Debug
PAGE 23

P10 **CardReader**
AU6437
PAGE 25
12MHz

PCLK_DEBUG

LPC
Azalia

CLK_PCI_775
Winbond KBC
NPCE791L
PAGE 31

CPU SideBand TemperatureSense I2C

Audio CODEC
Conexant 20584
PAGE 26

Keyboard TouchPad PAGE 30
SPI ROM PAGE 31
INT MIC PAGE 26
AUDIO CONN (H.P./ MIC) PAGE 27
Speaker CN PAGE 27

CHARGER (ISL88731A) PAGE 32
AMD CPU CORE (ISL6265) PAGE 34 — *CPU*
NB_CORE (UP6111AQDD) PAGE 36 — *NB*
0.9V/DDR 1.5V(RT8207) PAGE 37
SYSTEM 5V/3V (RT8206) PAGE 33
1.1V(UP6111AQDD) PAGE 35
Discharge /Thermal protec PAGE 40

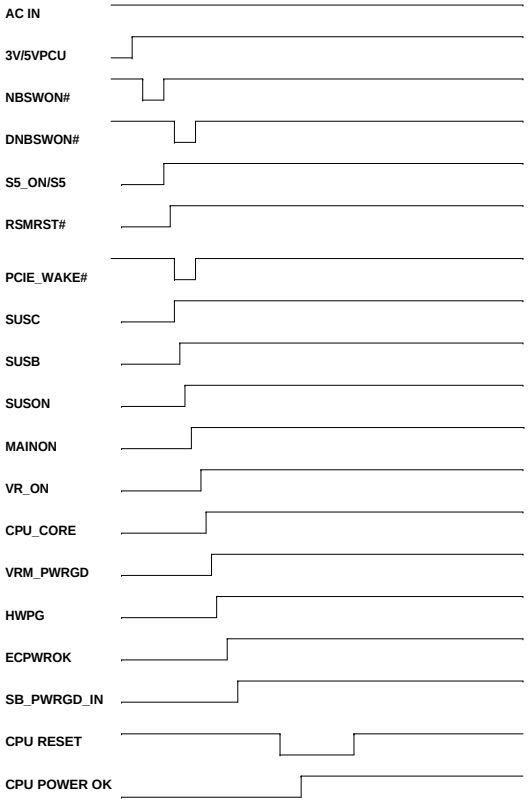
Quanta Computer Inc.
PROJECT : ZQG

Size	Document Number	Rev
	Block Diagram	1A

Date: Monday, November 01, 2010 Sheet 1 of 41

INDEX

Power Sequence



Hudson M1 SM BUS

SB820 SMBUS	Pin NO.	SMBUS Function Define
PCLK_SMB PDAT_SMB (+3V)	AD22 AE22	DDR / RFID
SB_SMBCLK1 SB_SMBDATA1 (+3V_S5)	F5 F4	not used
SB_SCLK2 SB_SDATA2 (+3V_S5)	D25 F23	not used
SB_SCLK3 SB_SDATA3 (+3V_S5)	B26 E26	not used
SB_SCLK3 SB_SDATA3 (+3V_S5)	B26 E26	not used

KBC(EC) SM BUS

KBC SMBUS	Pin NO.	SMBUS Function Define
MBCLK MBDATA (+3VPCU)	110 111	Battery
MBCLK_THRM MBDATA_THRM (+3VPCU)	115 116	Thermal

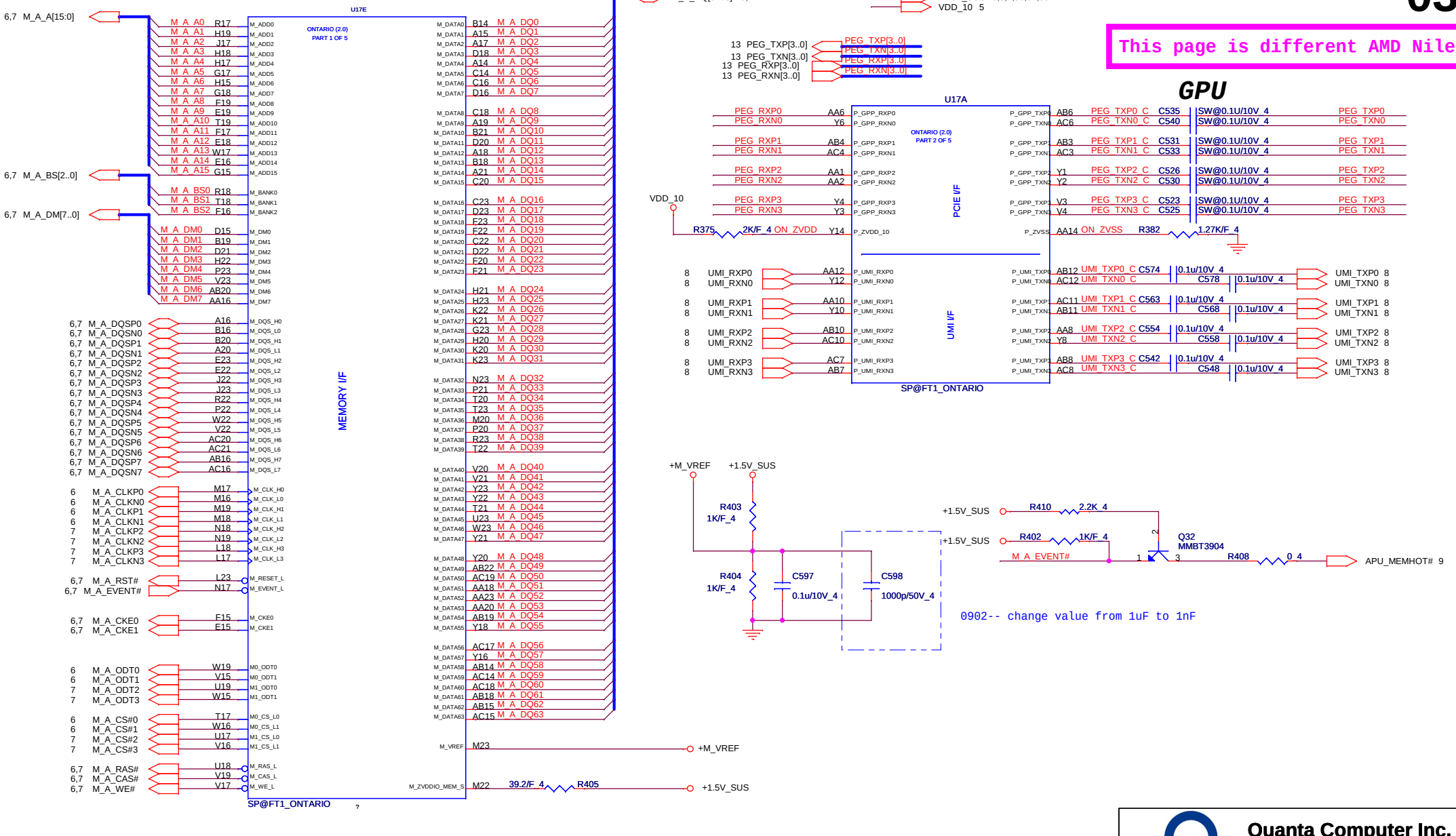
Quanta Computer Inc.
PROJECT : ZQ6

Size	Document Number	Rev
	System Information	1A

Date: Monday, November 01, 2010 Sheet 2 of 41

This page is different AMD Nile

GPU



Quanta Computer Inc.			
PROJECT : ZQG			
Size	Document Number		Rev
	ONTARIO MEM & PCIE I/F(1/3)		1A
Date: Monday, November 01, 2010		Sheet 3 of 41	

+1.8V 5,30,39,40
+3V 5,6,7,9,10,11,12,16,17,20,21,23,25,26,29,30,31,33,34,35,36,37,38,39,40

0901-- change from 2.2k to 2kohm

0906-- modify circuit

0831---follow AMD request for HDMI function

0830---add circuit

DIFFERENTIAL ROUTING

Can remove on MP------>LX

VID Override Circuit

for normal operation
open all switches

HDT+ Connector

HDT+ HEADER / PLACE ON TOP

SN74LVC2G07DCKR

Quanta Computer Inc.
PROJECT : ZQ6
ONTATIO DISPLAY/CLK/MI(2/3)
Size: Document Number: Rev: 1A
Date: Monday, November 01, 2010 Sheet 4 of 41

This page is different AMD Nile

+1.5V_SUS 3,6,7,30,37,39
+1V 30,36,39
+1.8V 4,30,39,40
+3V 4,6,7,9,10,11,12,16,17,20,21,23,25,26,29,30,31,33,34,35,36,37,38,39,40
+VCORE 30,34
+NBCORE 34
VDD_10 3

+VCORE
11A 440mil viax22
U17C
VDD_18 U8 W8 U6 U9 W6 T7 V7
2A 80mil viax4
1u/6.3V_4 C134
10u/6.3V_8 C135 C175 C544
0.1u/10V_4 C149 C148
1u/6.3V_4 C127
R371 0_8
+1.8V
+NBCORE
10A 400mil viax20
VDDCR_NB_1 E8
VDDCR_NB_2 E11
VDDCR_NB_3 E13
VDDCR_NB_4 F9
VDDCR_NB_5 F12
VDDCR_NB_6 G11
VDDCR_NB_7 G13
VDDCR_NB_8 H9
VDDCR_NB_9 H12
VDDCR_NB_10 K11
VDDCR_NB_11 K13
VDDCR_NB_12 L10
VDDCR_NB_13 L12
VDDCR_NB_14 L14
VDDCR_NB_15 M11
VDDCR_NB_16 M12
VDDCR_NB_17 M13
VDDCR_NB_18 N10
VDDCR_NB_19 N12
VDDCR_NB_20 N14
VDDCR_NB_21 P11
VDDCR_NB_22 P13
ONTARIO (2.0) PART 4 OF 5
POWER
+1.5V_SUS
2A 80mil viax4
VDDIO_MEM_S_1 G16
VDDIO_MEM_S_2 G19
VDDIO_MEM_S_3 E17
VDDIO_MEM_S_4 J16
VDDIO_MEM_S_5 L16
VDDIO_MEM_S_6 L19
VDDIO_MEM_S_7 N16
VDDIO_MEM_S_8 R16
VDDIO_MEM_S_9 R19
VDDIO_MEM_S_10 W18
VDDIO_MEM_S_11 U16
SP@FT1_ONTARIO
VDD_18_DAC W9
VDDAN_18_DAC
150mA 10mil viax1
C18
C674 10u/6.3V_8
C537 10u/6.3V_8
C188 1u/6.3V_4
L58 BLM18PG221SN1D(220_1.4A)_6
+1.8V
C19
T49
VDDPL_10 U11
200mA 10mil viax1
+1V
R103 0_6
C534 10u/6.3V_8
0.1u/10V_4 C192
C191 1u/6.3V_4
0901-- change R7037 P/N and footprint add R
VDD_10 U13 W13 V12 T12
5.5A 220mil viax11
R149 0_8
R144 0_8
+1V
10u/6.3V_8 C579
C280
0.1u/10V_4 C237 C236 C238 C235
1u/6.3V_4
+3V
VDD_33 A4
500mA 20mil viax1
C528 1u/6.3V_4
GND

+VCORE
10u/6.3V_8 C501 C170 C498 C499 C500 C141 C206 10u/6.3V_8
0.1u/10V_4 C131 C166 C168 C136 C130 C164 C169 C132 C167
+NBCORE
10u/6.3V_8 C155 C259 C147 C266 C231 10u/6.3V_8
0.1u/10V_4 C194 C181 C203 C199 C247 C251 C250 C214 C252
+1.5V_SUS
1u/6.3V_4 C269 C289 C321 C315
10u/6.3V_8 C351 C352
0.1u/10V_4 C272 C275 C311 C273 C271 C296 C319 C316 C350

+VCORE
1u/6.3V_4 C163 C138 C165 C129
+NBCORE
1u/6.3V_4 C195 C198 C233 C154 C197

U17D
ONTARIO (2.0) PART 5 OF 5
GROUND
VSS_1 A7
VSS_2 B7
VSS_3 B11
VSS_4 B17
VSS_5 B22
VSS_6 C4
VSS_7 D5
VSS_8 D7
VSS_9 D9
VSS_10 D11
VSS_11 D14
VSS_12 B15
VSS_13 D17
VSS_14 D19
VSS_15 E7
VSS_16 E9
VSS_17 E12
VSS_18 E20
VSS_19 F8
VSS_20 F11
VSS_21 F13
VSS_22 G4
VSS_23 G5
VSS_24 G7
VSS_25 G9
VSS_26 G12
VSS_27 G20
VSS_28 G22
VSS_29 H6
VSS_30 H11
VSS_31 H13
VSS_32 J4
VSS_33 J5
VSS_34 J7
VSS_35 J20
VSS_36 K10
VSS_37 K14
VSS_38 L4
VSS_39 L6
VSS_40 L8
VSS_41 L11
VSS_42 L13
VSS_43 L20
VSS_44 L22
VSS_45 M7
VSS_46 N4
VSS_47 N6
VSS_48 N8
VSS_49 N11
VSS_50 N13
VSS_51 N20
VSS_52 N22
VSS_53 P10
VSS_54 P14
VSS_55 R4
VSS_56 R7
VSS_57 R20
VSS_58 T6
VSS_59 T9
VSS_60 T11
VSS_61 T13
VSS_62 U4
VSS_63 U5
VSS_64 U7
VSS_65 U12
VSS_66 U20
VSS_67 U22
VSS_68 V8
VSS_69 V9
VSS_70 V11
VSS_71 V13
VSS_72 W1
VSS_73 W2
VSS_74 W4
VSS_75 W5
VSS_76 W7
VSS_77 W12
VSS_78 W20
VSS_79 Y5
VSS_80 Y7
VSS_81 Y9
VSS_82 Y11
VSS_83 Y13
VSS_84 Y15
VSS_85 Y17
VSS_86 Y19
VSS_87 AA4
VSS_88 AA22
VSS_89 AB2
VSS_90 AB5
VSS_91 AB9
VSS_92 AB13
VSS_93 AB17
VSS_94 AB21
VSS_95 AC5
VSS_96 AC9
VSS_97 AC13
VSSBG_DAC A11
SP@FT1_ONTARIO
GND

EMC CAPS
place capacitors under BGA
+1.5V_SUS C270 180P/25V_4 C303 180P/25V_4
+VCORE 180P/25V_4 C133 C128 180P/25V_4
+NBCORE C196 180P/25V_4 C232 180P/25V_4
+1.5V_SUS 0.1u/10V_4 C274 C320 0.1u/10V_4
VDD_18 C174 180P/25V_4 C153 180P/25V_4
VDDAN_18_DAC C187 180P/25V_4
VDD_10 C234 180P/25V_4
VDDPL_10 C190 180P/25V_4
+3V C521 0.1u/10V_4

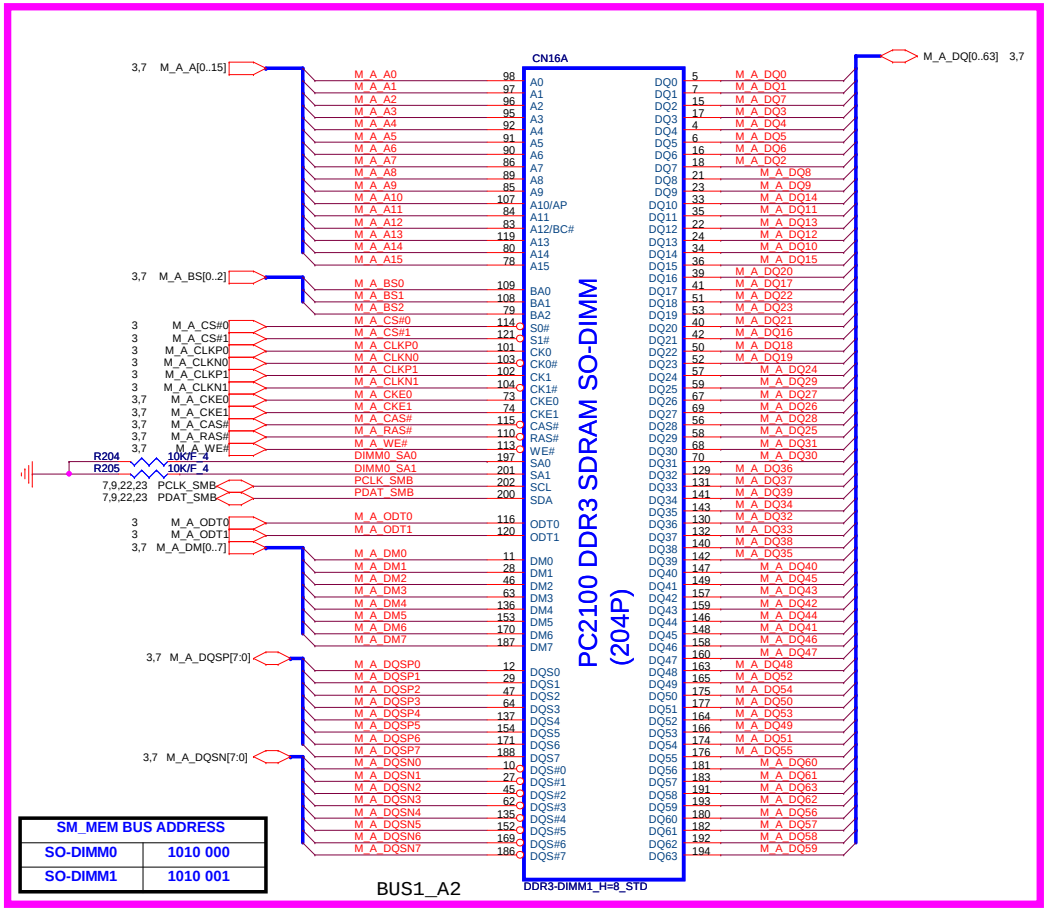
Quanta Computer Inc.
PROJECT : ZQG
Size | Document Number: ONTARIO POWER & DECOUP(3/3) | Rev 1A
Date: Monday, November 01, 2010 | Sheet 5 of 41

0830--P/N and footprint are follow ZR7B

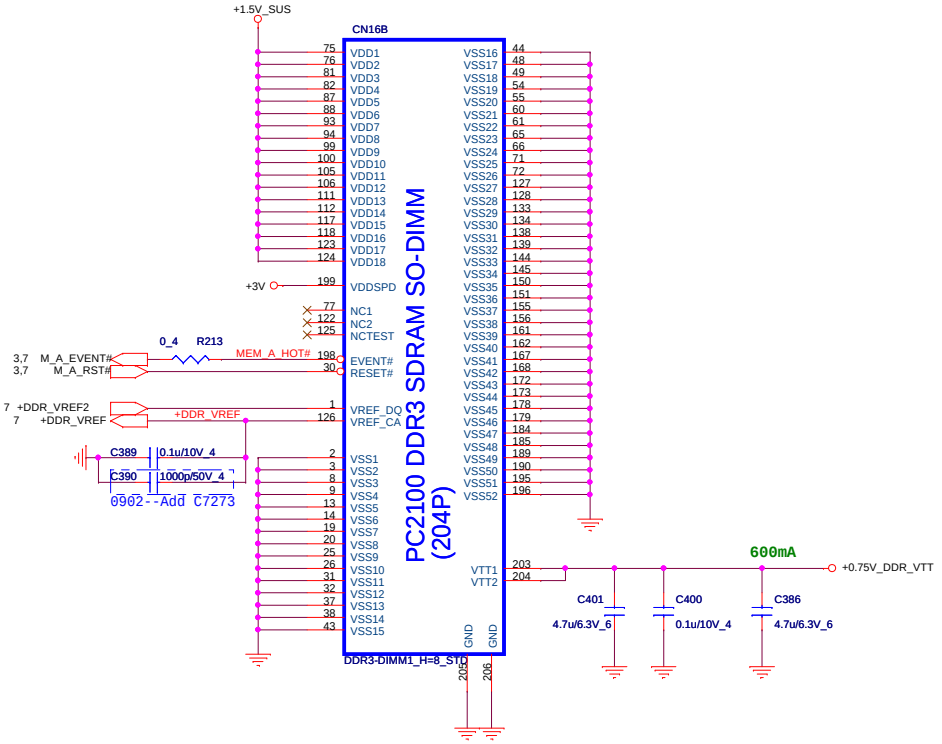
+1.5V_SUS 3,5,7,30,37,39

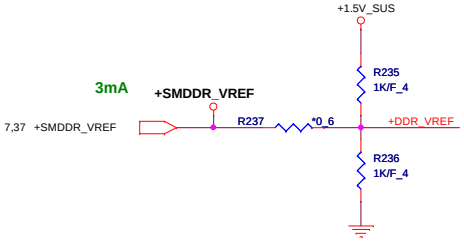
+0.75V_DDR_VTT 7,37

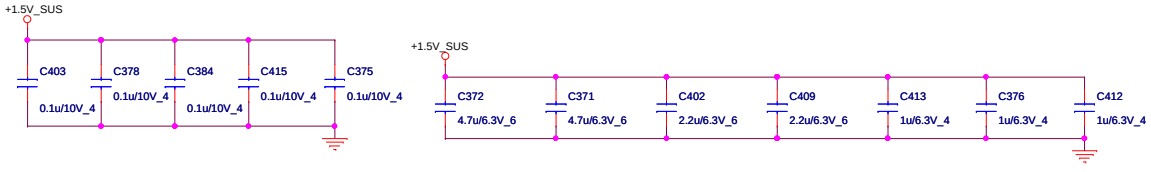
+3V 4,5,7,9,10,11,12,16,17,20,21,23,25,26,29,30,31,33,34,35,36,37,38,39,40

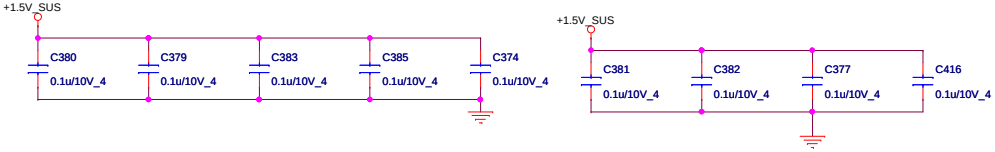


SM_MEM BUS ADDRESS	
SO-DIMM0	1010 000
SO-DIMM1	1010 001









Quanta Computer Inc.

PROJECT : ZQ6

Size	Document Number	Rev
	DDR3 SO-DIMM (STD)	1A

Date: Monday, November 01, 2010 Sheet 6 of 41

0830--P/N and footprint are follow ZR7B

+1.5V_SUS 3,5,6,30,37,39
+0.75V_DDR_VTT 6,37
+3V 4,5,6,9,10,11,12,16,17,20,21,23,25,26,29,30,31,33,34,35,36,37,38,39,40

CN20A

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDR3-DIMM0_H=4_Standard

BUS1_A2

SM_MEM BUS ADDRESS	
SO-DIMM0	1010 000
SO-DIMM1	1010 001

CN20B

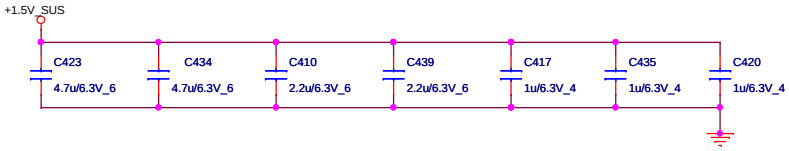
PC2100 DDR3 SDRAM SO-DIMM (204P)

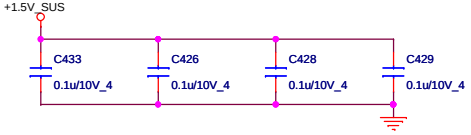
DDR3-DIMM0_H=4_Standard

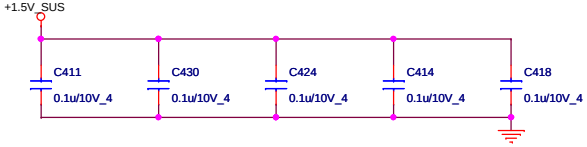
0902--Add C7274

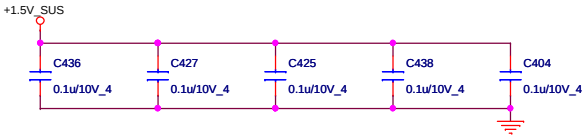
3mA

+SMDDR_VREF









Quanta Computer Inc.		
PROJECT : ZQG		
Size	Document Number: DDR3 SO-DIMM (STD)	Rev: 1A
Date: Monday, November 01, 2010	Sheet 7 of 41	

This page is different AMD Nile expect RTC circuit

PCIE_VDDR 11
+3V_S5 9,10,11,12,22,28,29,30,33
+3VPCU 20,29,30,31,32,33,39
+5VPCU 33,34,35,40

RTC

PLACE THESE PCIE AC COUPLING CAPS CLOSE TO U41

Hudson M1 Part 1 of 5

PCI CLKS
PCI EXPRESS INTERFACES
PCI INTERFACE
CLOCK GENERATOR
LPC
CPU
RTC

STRAP Function To EC

Debug STRAPS

All the PCI bus has build-in Pull-UP/Down resistors

LAN
WLAN
WWAN

CPU_CLK

To LAN Controller
To WLAN Controller
To WWAN Connector

To STRAPs Page

Del Q33,R434,R435,R444 from BOMs, ZQE no support RTC charge circuits.

CR2032 with cable
AHL03003004
AHL03003032
AHL03003037 , AHL03001044

CR2032 (Non-Chargeable)
AHL03003014
AHL030M0009

RTC_CLK must ready refore RSMRST#

INTRUDER_ALERT# Left not connected (Southbridge has 50-kohm internal pull-up to VBAT).

PCH_SUSCLK 31

Quanta Computer Inc.
PROJECT : ZQ6

Size	Document Number	Rev
	HUDSON PCIE/LPC/CPU IF(1/5)	1A
Date: Monday, November 01, 2010	Sheet 8 of 41	

This page is different AMD Nile

SCL0/SDATA0 is 3V tolerance
AMD datasheet define it

Clock gen/Robson/TV tuner
/DDR3/DDR3 thermal/Accelerometer

+3V R125 2.2K_4 PCLK_SMB
+3V R131 2.2K_4 PDAT_SMB

+3V R179 *10K/F_4 SUS_STAT#
+3V R133 4.7K_4 NB_PWRGD

+3V_S5 R175 10K/F_4 CPU_THERMTRIP#

SB/ PWR_GOOD / VDDIO_33_S

By AMD confirm

+3V_S5 R437 *10K/F_4 SYS_RST#
+3V R120 *10K/F_4 SIO_A20GATE

+3V_S5 R436 *10K/F_4 DNBSWON#
R189 10K/F_4 PCIE_WAKE#
R352 10K/F_4 SB_SCLK3
R353 10K/F_4 SB_SDATA3
R193 10K/F_4 SB_PWRGD_IN
R116 2.2K_4 SB_SCLK4
R102 2.2K_4 SB_SDATA4

+3V 4,5,6,7,10,11,12,16,17,20,21,23,25,26,29,30,31,33,34,35,36,37,38,39,40
+3V_S5 8,10,11,12,22,28,29,30,33

U18D

Hudson M1
Part 4 of 5

3 APU_MEMHOT# → RI# T163, SPI_CS3# T157
30,31 SUSB#
30,31 SUSC#
30,31 DNBSWON#
SB_PWRGD_IN
SUS_STAT#
SB_TEST0 T155
SB_TEST1 T97
SB_TEST2 T82
31 SIO_A20GATE
31 SIO_RCIN#
31 SIO_EXT_SCI#
31 SIO_EXT_SMI#
SYS_RST# T166
22,31 PCIE_WAKE# → C346 100p/50V_4
4 CPU_THERMTRIP# → CPU_THERMTRIP# NB_PWRGD T169
30,31 ICH_RSMRST#

ACPI / WAKE UP EVENTS
USB 1.1 USB MISC

PCI_PME#/GEVENT4#
RI#/GEVENT22#
SPI_CS3#/GBE_STAT1/GEVENT21#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST0
TEST1/TMS
TEST2
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/GEVENT23#
GEVENT5#
SYS_RESET#/GEVENT19#
WAKE#/GEVENT8#
IR_RX1/GEVENT20#
THRMTRIP#/SMBALERT#/GEVENT2#
NB_PWRGD
RSMRST#

USBCLK/14M_25M_48M_OSC A10 T144
USB_RCOMP G19 USB_RCOMP_SB R139 11.8K/F_4
USB_FSD1P/GPIO186 J10 T69
USB_FSD1N H11 T70
USB_FSD0P/GPIO185 H9 T76
USB_FSD0N J8 T85

GPIO

CLK_REQ4#/SATA_IS0#/GPIO64 T62
CLK_REQ3#/SATA_IS1#/GPIO63 T64
SMARTVOLT1/SATA_IS2#/GPIO50
CLK_REQ0#/SATA_IS3#/GPIO60
SATA_IS4#/FANOUT3/GPIO55
SATA_IS5#/FANIN3/GPIO59
SPKR/GPIO66
SCL0/GPIO43
SDA0/GPIO47
SCL1/GPIO227
SDA1/GPIO228
CLK_REQ2#/FANIN4/GPIO62
CLK_REQ1#/FANOUT4/GPIO61
IR_LED#/LLB#/GPIO184
SMARTVOLT2/SHUTDOWN#/GPIO51
DDR3_RST#/GEVENT7#
GBE_LED0/GPIO183
GBE_LED1/GEVENT9#
GBE_LED2/GEVENT10#
GBE_STAT0/GEVENT11#
CLK_REQG#/GPIO65/OSCIN

22 PCIE_REQ_LAN# R140 0_4 8 SB_GPIO_RST# → PCIE_REQ_LAN# R
16 dGPU_PWR_EN
0908--Add net
26 SPKR
6,7,22,23 PCLK_SMB
6,7,22,23 PDAT_SMB
+3V_S5 R184 10K/F_4 SB_SMBCLK1
R185 10K/F_4 SB_SMBDATA1
23 PCIE_REQ_WLAN2# R373 0_4 PCIE_REQ_WLAN2# R
23 PCIE_REQ_WLAN1# R142 0_4 PCIE_REQ_WLAN1# R
ACCLED_EN T168

USB 2.0

USB_HSD13P A12
USB_HSD13N
USB_HSD12P F11
USB_HSD12N E11
USB_HSD11P E14
USB_HSD11N E12
USB_HSD10P J12 → USBP10+ 23, USBP10- 23 WL2(3G)
USB_HSD10N J14
USB_HSD9P A13 → USBP9+ 23, USBP9- 23 WL1
USB_HSD9N B13
USB_HSD8P D13 → USBP8+ 28, USBP8- 28 EXT BLUETOOTH
USB_HSD8N C13
USB_HSD7P G12 → USBP7+ 28, USBP7- 28 BLUETOOTH
USB_HSD7N G14
USB_HSD6P G16 → USBP6+ 25, USBP6- 25 4 IN 1 CARD READER (MMC)
USB_HSD6N G18
USB_HSD5P D16 → USBP5+ 28, USBP5- 28 USB3 Connector (Daughter)
USB_HSD5N C16
USB_HSD4P B14
USB_HSD4N A14
USB_HSD3P E18
USB_HSD3N E16
USB_HSD2P J16 → USBP2+ 20, USBP2- 20 CCD
USB_HSD2N J18
USB_HSD1P B17 → USBP1+ 28, USBP1- 28 USB2 Connector (Daughter)
USB_HSD1N A17
USB_HSD0P A16 → USBP0+ 28, USBP0- 28 USB1 Connector (MB Side)
USB_HSD0N B16

T164 CPU_MEMHOT#_IN
28 OC_6#
+3V_S5 R187 *10K/F_4
28 OC_4#
T77 T84 T83 T78

USB OC

BLINK/USB_OC7#/GEVENT18#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GEVENT17#
USB_OC4#/IR_RX0/GEVENT16#
USB_OC3#/AC_PRES/TDO/GEVENT15#
USB_OC2#/TCK/GEVENT14#
USB_OC1#/TDI/GEVENT13#
USB_OC0#/TRST#/GEVENT12#

SCL2/SDATA2 is 3V/S5 tolerance
AMD datasheet define it

SB_SCLK2 D25 R360 10K/F_4 +3V_S5
SB_SDATA2 F23 R362 10K/F_4
SB_SCLK3 B26
SB_SDATA3 E26
F25 T53
E22 T125
SB_GPIO199 F22 R132 *2.2K_4
SB_GPIO200 E21 R134 2.2K_4

has checked with AMD FAE already--Allen

GPIO200	GPIO199
H,H = Reserved	
H,L = SPI ROM (DEFAULT)	
L,H = LPC ROM	
L,L = FWH ROM	

To Azalia

HD audio interface is 3.3S5 voltage

for EMI

26 ACZ_BITCLK_AUDIO C607 *10p/50V_4 R424 33_4 R412 *10K_4 ACZ_BITCLK_R
12 ACZ_SDOUT ACZ_SDOUT
26 ACZ_SDOUT_AUDIO R425 33_4
C608 *10p/50V_4
26 ACZ_SDIN0
C604 *10p/50V_4 R411 *10K_4
R414 33_4 ACZ_SYNC_R
26 ACZ_SYNC_AUDIO R416 33_4 ACZ_RST#_R
26 ACZ_RESET#_AUDIO
C605 *10p/50V_4

HD AUDIO

AZ_BITCLK M3
AZ_SDOUT N1
AZ_SDIN0/GPIO167 L2
AZ_SDIN1/GPIO168 M2
AZ_SDIN2/GPIO169 M1
AZ_SDIN3/GPIO170 M4
AZ_SYNC N2
AZ_RST# P2

R417 10K/F_4 GBE_COL
R428 10K/F_4 GBE_CRS
+3V_S5 R171 10K/F_4 GBE_MDIO
R169 10K/F_4 GBE_RXERR
+3V_S5 R161 10K/F_4 GBE_PHY_INTR

GBE LAN

GBE_COL T1
GBE_CRS T4
GBE_MDCK L6
GBE_MDIO L5
GBE_RXCLK T9
GBE_RXD3 U1
GBE_RXD2 U3
GBE_RXD1 T2
GBE_RXD0 U2
GBE_RXCTL/RXDV T5
GBE_RXERR V5
GBE_TXCLK P5
GBE_TXD3 M5
GBE_TXD2 P9
GBE_TXD1 T7
GBE_TXD0 P7
GBE_TXCTL/TXEN M7
GBE_PHY_PD P4
GBE_PHY_RST# M9
GBE_PHY_INTR V7

23 SB_SDATA4 SB_SDATA4 F23
23 SB_SCLK4 SB_SCLK4 E24
SB_GPIO166 F21
T58 T114 SB_GPIO160 G29
T116 AC_OK D27
T115 BAT_INT# F28
F29
E27

EMBEDDED CTRL

PS2_DAT/SDA4/GPIO187
PS2_CLK/SCL4/GPIO188
SPI_CS2#/GBE_STAT2/GPIO166
FC_RST#/GPIO160
PS2KB_DAT/GPIO189
PS2KB_CLK/GPIO190
PS2M_DAT/GPIO191
PS2M_CLK/GPIO192

EMBEDDED CTRL

SCL2/GPIO193
SDA2/GPIO194
SCL3_LV/GPIO195
SDA3_LV/GPIO196
EC_PWM0/EC_TIMER0/GPIO197
EC_PWM1/EC_TIMER1/GPIO198
EC_PWM2/EC_TIMER2/GPIO199
EC_PWM3/EC_TIMER3/GPIO200

KSI_0/GPIO201 G24
KSI_1/GPIO202 G25
KSI_2/GPIO203 E28
KSI_3/GPIO204 E29
KSI_4/GPIO205 D29
KSI_5/GPIO206 D28
KSI_6/GPIO207 C29
KSI_7/GPIO208 C28

KSO_0/GPIO209 B28
KSO_1/GPIO210 A27
KSO_2/GPIO211 B27
KSO_3/GPIO212 D26
KSO_4/GPIO213 A26
KSO_5/GPIO214 C26
KSO_6/GPIO215 A24
KSO_7/GPIO216 B25
KSO_8/GPIO217 A25
KSO_9/GPIO218 D24
KSO_10/GPIO219 B24
KSO_11/GPIO220 C24
KSO_12/GPIO221 B23
KSO_13/GPIO222 A23
KSO_14/GPIO223 D22
KSO_15/GPIO224 C22
KSO_16/GPIO225 A22
KSO_17/GPIO226 B22

Hudson M1

System PWR_OK(CLG)

+3V_S5 C349 *0.1u/10V_4
U8 TC7SH08FU
17,30 SB_PWRGD_IN → SB_PWRGD_IN
PWROK_EC → CPU_COREPG 30,34, PWROK_EC 30,31
R194 100K_4

Quanta Computer Inc.
PROJECT : ZQG

Size	Document Number	Rev
	HUDSON ACPI/GPIO/USB(2/5)	1A

Date: Monday, November 01, 2010 Sheet 9 of 41

SATA PORT 0,1,2,3 can support AHCI mode

PLACE SATA AC COUPLING CAPS CLOSE TO Hudson M1

AVDD_SATA 11
+3V 4,5,6,7,9,11,12,16,17,20,21,23,25,26,29,30,31,33,34,35,36,37,38,39,40
+3V_S5 8,9,11,12,22,28,29,30,33

This page is different AMD Nile

SATA HDD

24 SATA_TXP0 — C592 .01U/16V/X7R_4 — SATA_TXP0_C — AH9 SATA_TX0P
24 SATA_TXN0 — C590 .01U/16V/X7R_4 — SATA_TXN0_C — AJ9 SATA_TX0N
24 SATA_RXN0 — AJ8 SATA_RX0N
24 SATA_RXP0 — AH8 SATA_RX0P

SATA ODD

24 SATA_TXP1 — C588 .01U/16V/X7R_4 — SATA_TXP1_C — AH10 SATA_TX1P
24 SATA_TXN1 — C585 .01U/16V/X7R_4 — SATA_TXN1_C — AJ10 SATA_TX1N
24 SATA_RXN1 — AG10 SATA_RX1N
24 SATA_RXP1 — AF10 SATA_RX1P

AG12 SATA_TX2P
AF12 SATA_TX2N
AJ12 SATA_RX2N
AH12 SATA_RX2P
AH14 SATA_TX3P
AJ14 SATA_TX3N
AG14 SATA_RX3N
AF14 SATA_RX3P
AG17 SATA_TX4P
AF17 SATA_TX4N
AJ17 SATA_RX4N
AH17 SATA_RX4P
AJ18 SATA_TX5P
AH18 SATA_TX5N
AH19 SATA_RX5N
AJ19 SATA_RX5P

PLACE SATA_CAL RES VERY CLOSE TO BALL OF Hudson M1

XTLVDD_SATA-- SATA crystal power

PLVDD_SATA-- SATA PLL POWER

AVDD_SATA — R147 1K/F_4 — R143 931/F_4 — SATA_CALRP — SATA_CALRN — AB14 SATA_CALRP — AA14 SATA_CALRN

29 SATA_LED# — AD11 SATA_ACT#/GPIO67

C575 *22p/50V_4 — Y4 *25MHz_30PPM — R381 *1M/F_4 — C582 *22p/50V_4
SATA_X1 — AD16 SATA_X1
SATA_X2 — AC16 SATA_X2

T89 SPI_DI — J5 SPI_DI/GPIO164
T96 SPI_DO — E2 SPI_DO/GPIO163
T160 SPI_CLK — K4 SPI_CLK/GPIO162
T79 SPI_CS1# — K9 SPI_CS1#/GPIO165
T162 ROM_RST# — G2 ROM_RST#/GPIO161

U18B

Hudson M1

Part 2 of 5

SERIAL ATA

FLASH

FC_CLK AH28 T123
FC_FBCLKOUT AG28 T124
FC_FBCLKIN AF26 T47
FC_OE#/GPIOD145 AF28 T121
FC_AVD#/GPIOD146 AG29 T122
FC_WE#/GPIOD148 AG26 T128
FC_CE1#/GPIOD149 AF27 T119
FC_CE2#/GPIOD150 AE29 T118
FC_INT1/GPIOD144 AF29 T120
FC_INT2/GPIOD147 AH27 T129
FC_ADQ0/GPIOD128 AJ27 T126
FC_ADQ1/GPIOD129 AJ26 T133
FC_ADQ2/GPIOD130 AH25 T132
FC_ADQ3/GPIOD131 AH24 T137
FC_ADQ4/GPIOD132 AG23 T135
FC_ADQ5/GPIOD133 AH23 T134
FC_ADQ6/GPIOD134 AJ22 T138
FC_ADQ7/GPIOD135 AG21 T143
FC_ADQ8/GPIOD136 AF21 T139
FC_ADQ9/GPIOD137 AH22 T140
FC_ADQ10/GPIOD138 AJ23 T141
FC_ADQ11/GPIOD139 AF23 T131
FC_ADQ12/GPIOD140 AJ24 T136
FC_ADQ13/GPIOD141 AJ25 T130
FC_ADQ14/GPIOD142 AG25 T46
FC_ADQ15/GPIOD143 AH26 T127

HW MONITOR

FANOUT0/GPIO52 W5 BOARD_ID0
FANOUT1/GPIO53 W6 BOARD_ID1
FANOUT2/GPIO54 Y9 SB_PROCHOT#
FANIN0/GPIO56 W7 BOARD_ID2
FANIN1/GPIO57 V9 BOARD_ID3
FANIN2/GPIO58 W8 BOARD_ID4

0831--modify location

TEMPIN0/GPIO171 B6 TEMPIN0
TEMPIN1/GPIO172 A6 TEMPIN1
TEMPIN2/GPIO173 A5 TEMPIN2
TEMPIN3/TALERT#/GPIO174 B5 SB_TALERT#
TEMP_COMM C7 — SB_TALERT# 4

VIN0/GPIO175 A3 CPU_TYPE
VIN1/GPIO176 B4 SB_HOLE_TIME
VIN2/GPIO177 A4 CPU_SENSOR
VIN3/GPIO178 C5 VIN2 — R390 10K_4
VIN4/GPIO179 A7 VIN3 — R387 10K_4
VIN5/GPIO180 B7 VIN4 — R386 10K_4
VIN6/GBE_STAT3/GPIO181 B8 VIN5 — R383 10K_4
VIN7/GBE_LED3/GPIO182 A8 BOARD_ID5

SPI ROM

NC1 G27
NC2 Y2

4,8,31 H_PROCHOT# — H_PROCHOT# — D6 RB500V-40 — SB_PROCHOT#

0831--add circuit

Hudson M1

AMD recommand : TEMPIN0 / TEMPIN1 / TEMPIN2 can not maintain on floating stages when without usage. Do not care pull high or pull down.

TEMPIN2 — R388 10K_4
TEMPIN1 — R389 10K_4
TEMPIN0 — R391 10K_4

MB ID

CPU THERMAL	GPIO52
External	1
SB-TSI	0

	GPIO57
(Dis) SW	1
UMA	0

SB8XX Hold Time	GPIO53
1.2V	1
1.1V	0

	GPIO58
VRAM - 800	1
VRAM-900	0

DU1/MK2	GPIO56
MK2.0 AMD	1
DU1.0 AMD	0

	GPIO182
PX4.0	1
PX3.0	0

+3V

GPIO52
R182 10K_4 BOARD_ID0 R192 *10K_4
GPIO53
R181 10K_4 BOARD_ID1 R191 *10K_4
GPIO56
R180 10K_4 BOARD_ID2 R190 *10K_4
GPIO57
R158 *SP@10K_4 BOARD_ID3 R157 SP@10K_4
GPIO58
R418 *SP@10K_4 BOARD_ID4 R429 SP@10K_4

+3V_S5

GPIO182
R385 *SP@10K_4 BOARD_ID5 R384 SP@10K_4
R400 *10K/F_4 CPU_TYPE R399 10K/F_4
R395 *10K/F_4 CPU_SENSOR R394 10K/F_4
R398 *10K/F_4 SB_HOLE_TIME R397 10K/F_4

Quanta Computer Inc.
PROJECT : ZQG

Size	Document Number	Rev
	HUDSON SATA/BIDs(3/5)	1A

Date: Monday, November 01, 2010 Sheet 10 of 41

+3V 4,5,6,7,9,10,12,16,17,20,21,23,25,26,29,30,31,33,34,35,36,37,38,39,40
+1.1V 30,35
+3V_S5 8,9,10,12,22,28,29,30,33
+1.1V_S5 30,35
AVDD_SATA 10
VDDIO_AZ 12

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PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

GPIOD Interface Not Implemented connected to GND through a 0-Ω resistor

U18C Hudson M1 Part 3 of 5

POWER

42mA
150mA 10mil viax1
22mA
1115mA 50mil viax3
15mA 5mil vaix1
1354mA 60mil viax3
534mA 25mil viax2
88mA
790mA 35mil viax2
382mA 20mil viax1
49mA
165mA 10mil viax1
15mA
58mA
46mA
65mA
16mA
12mA
5mA

U18E Hudson M1 GROUND Part 5 of 5

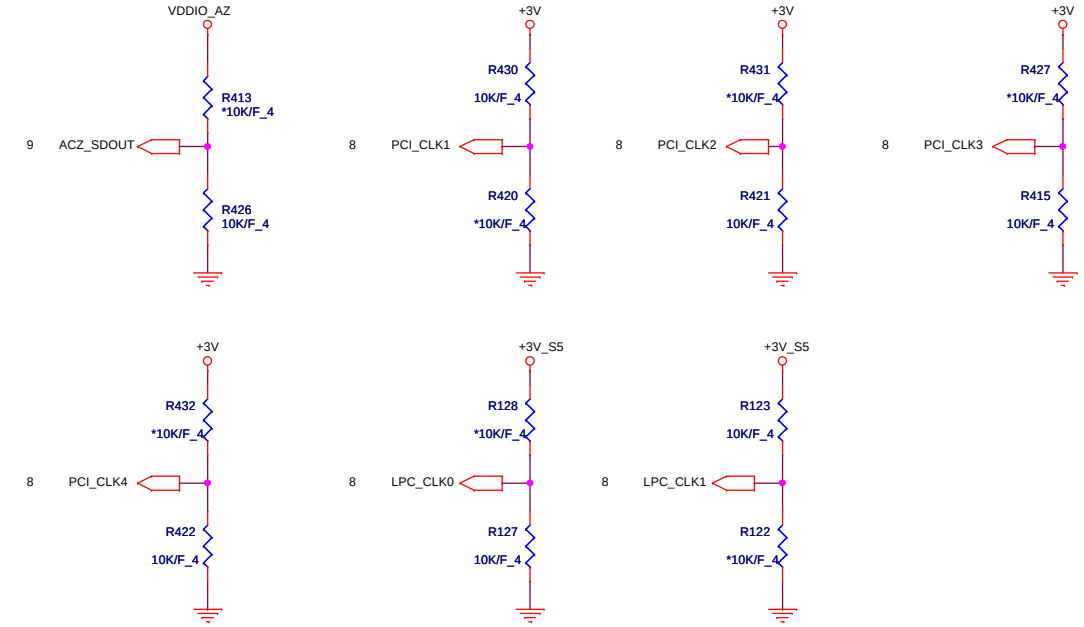
Quanta Computer Inc.
PROJECT : ZQG
Size | Document Number: HUDSON PWR/GND(4/5) | Rev: 1A
Date: Monday, November 01, 2010 | Sheet 11 of 41

VDDIO_AZ 11
+3V 4,5,6,7,9,10,11,16,17,20,21,23,25,26,29,30,31,33,34,35,36,37,38,39,40
+3V_S5 8,9,10,11,22,28,29,30,33

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

intermal have pull Hi 10K , confirm AMD ward this pull Hi not need

REQUIRED STRAPS



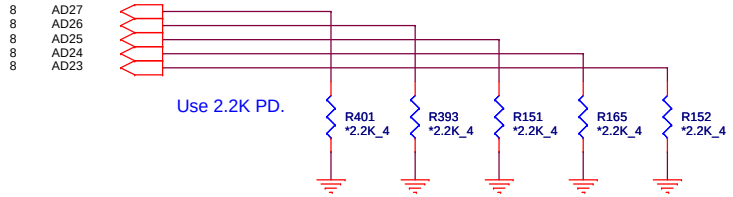
PCI_CLK4 CPU/NB HT Clock Selection
0 V – Reserved.
3.3 V – Required setting for integrated clock mode.
This strap is not used if the strap CLKGEN is configured for external clock generator mode.

REQUIRED STRAPS

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200 GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM (Default)
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM L,L = FWH ROM

DEBUG STRAPS

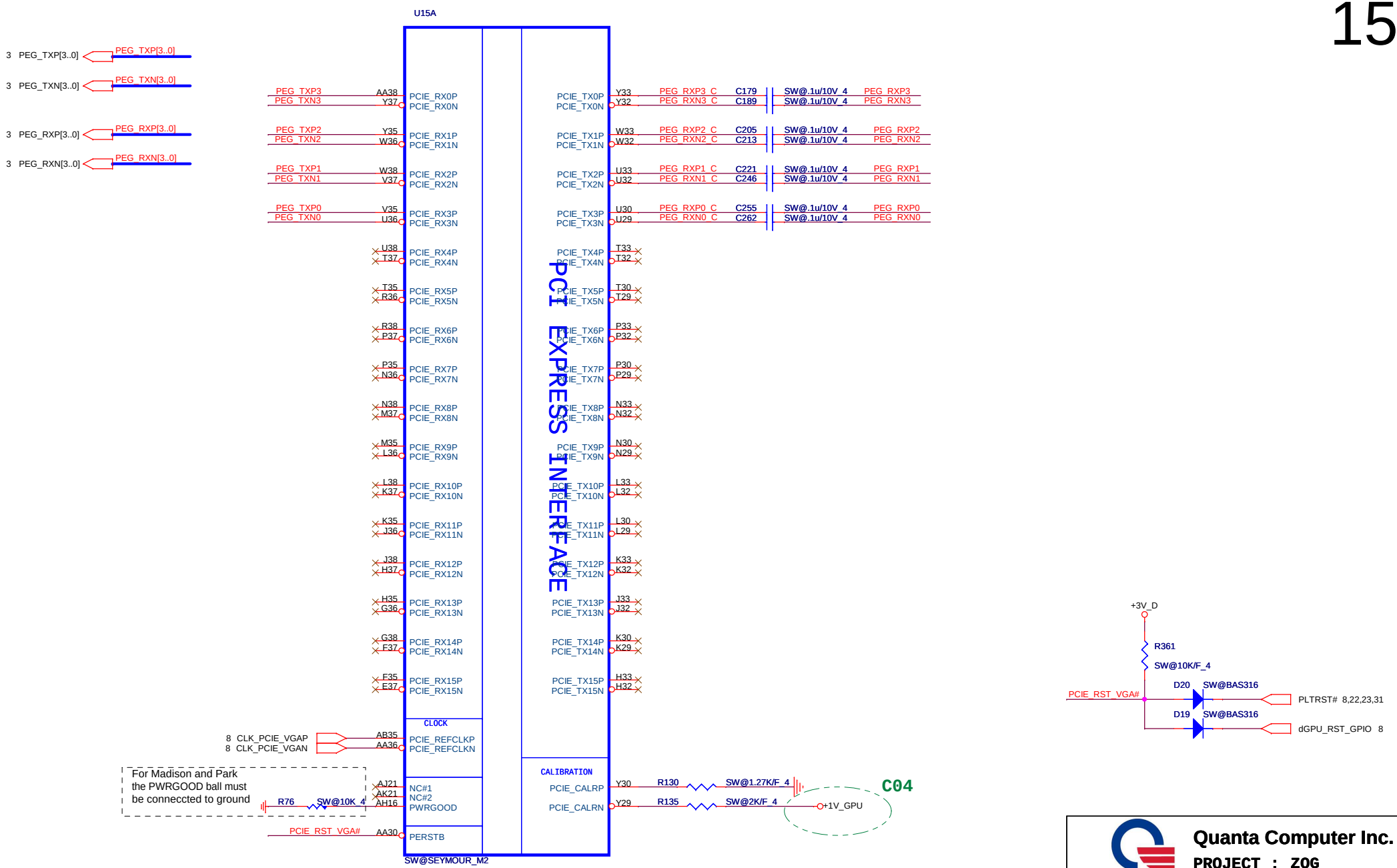
HUDSON-M1 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

Quanta Computer Inc.
PROJECT : ZQG

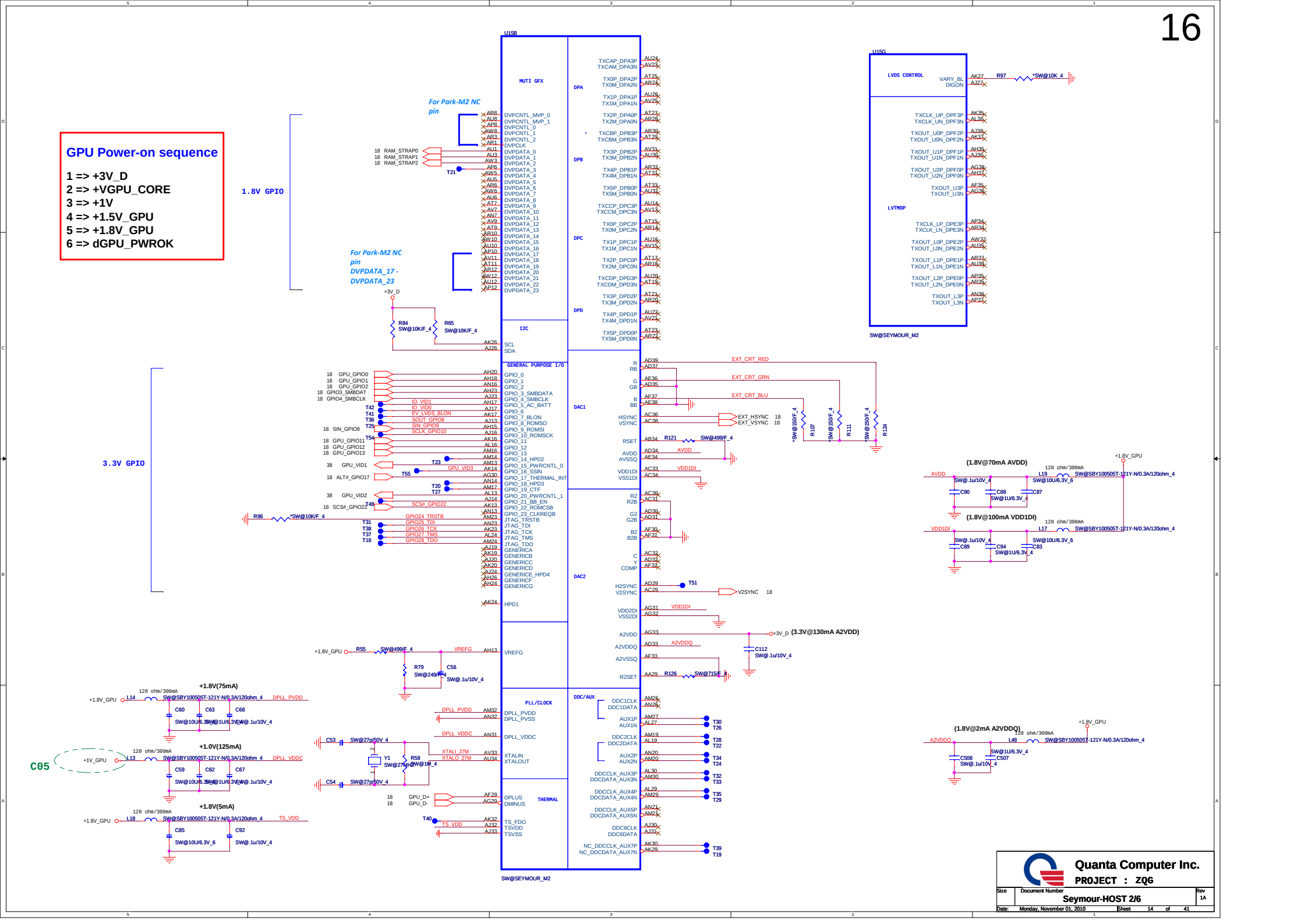
Size	Document Number	Rev
	HUDSON STRAPS/PWRGD(5/5)	1A
Date: Monday, November 01, 2010	Sheet 12 of 41	



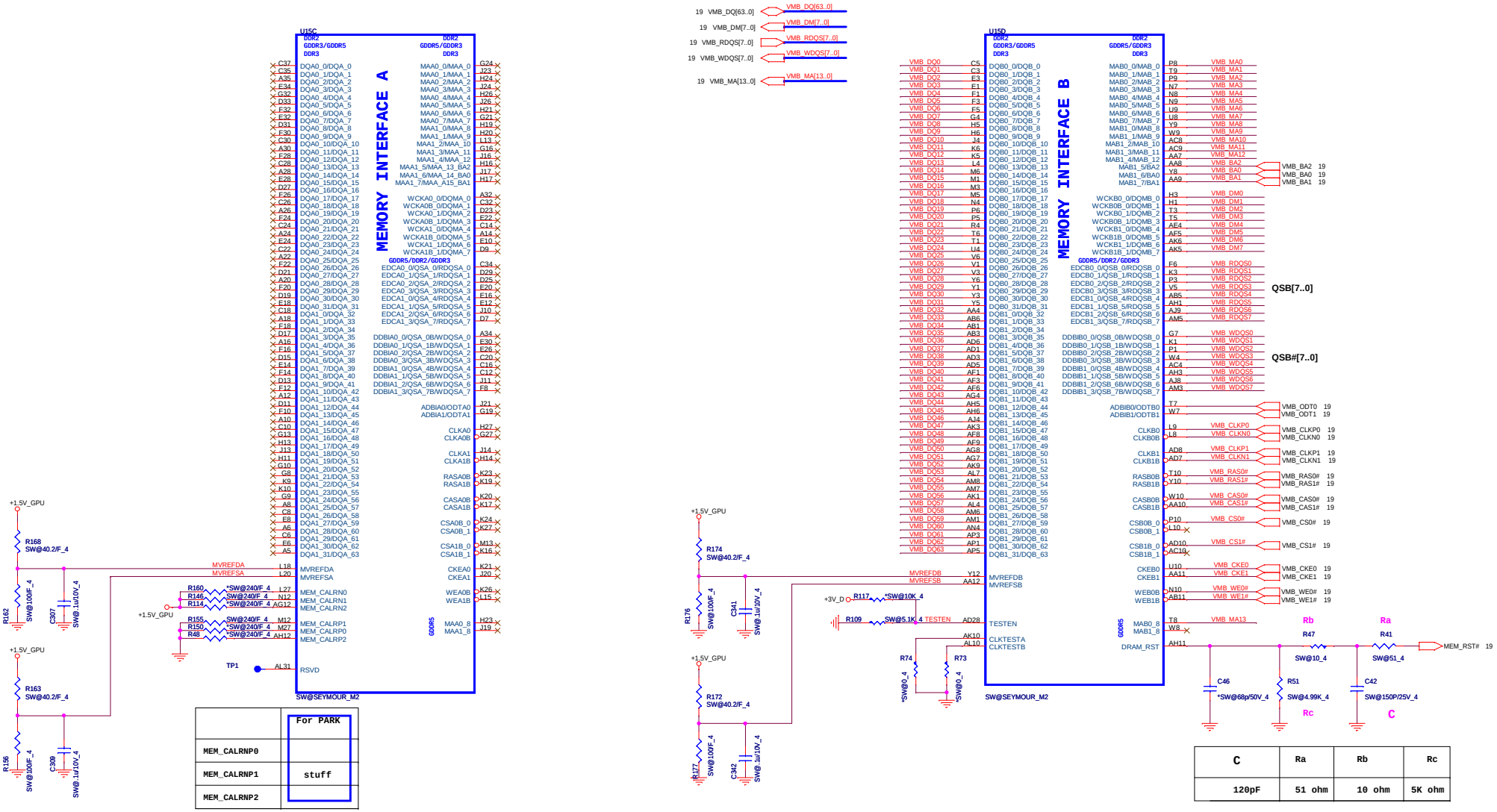
Quanta Computer Inc.		
PROJECT : ZQG		
Size	Document Number	Rev
	SeymourPCIE 1/6	1A
Date: Monday, November 01, 2010	Sheet 13 of 41	

GPU Power-on sequence

1 => +3V_D
2 => +VGPU_CORE
3 => +1V
4 => +1.5V_GPU
5 => +1.8V_GPU
6 => dGPU_PWROK



Quanta Computer Inc.
PROJECT : ZQG
Size | Document Number: Seymour-HOST 2/6 | Rev 1A
Date: Monday, November 01, 2010 | Sheet 14 of 41



	For PARK
MEM_CALRNP0	
MEM_CALRNP1	stuff
MEM_CALRNP2	

C	Ra	Rb	Rc
120pF	51 ohm	10 ohm	5K ohm

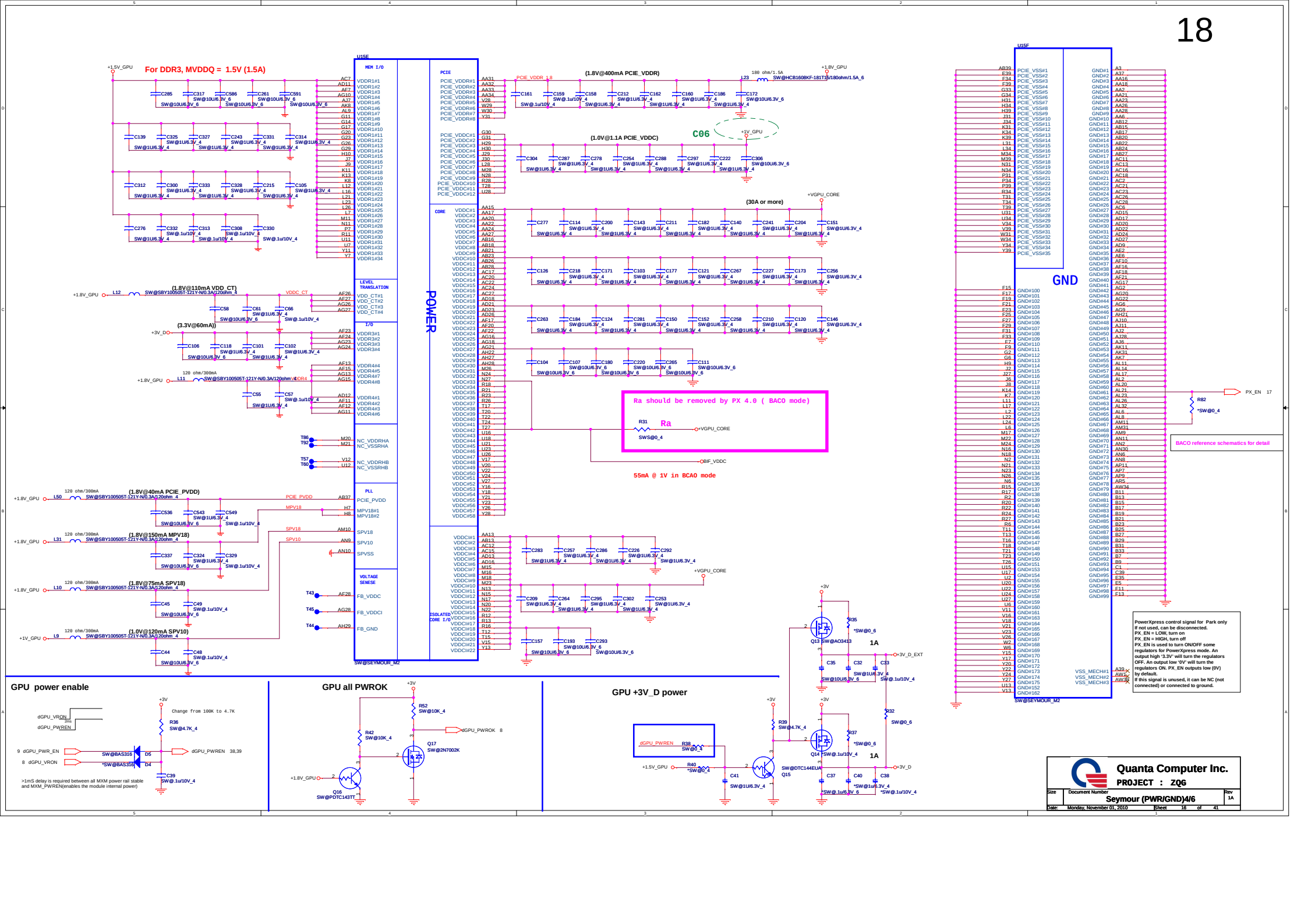
DDR3/GDDR3 Memory Stuff Option

	GDDR5	GDDR3	DDR3
+1.5V_VGA	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

Quanta Computer Inc.
PROJECT : ZQG

Size	Document Number	Rev
	Seymour-MEM 3/6	1A

Date: Monday, November 01, 2010 Sheet 15 of 41


For DDR3, MVDDQ = 1.5V (1.5A)
+1.5V_GPU
U15E
MEM I/O
VDDR#1
VDDR#2
VDDR#3
VDDR#4
VDDR#5
VDDR#6
VDDR#7
VDDR#8
VDDR#9
VDDR#10
VDDR#11
VDDR#12
VDDR#13
VDDR#14
VDDR#15
VDDR#16
VDDR#17
VDDR#18
VDDR#19
VDDR#20
VDDR#21
VDDR#22
VDDR#23
VDDR#24
VDDR#25
VDDR#26
VDDR#27
VDDR#28
VDDR#29
VDDR#30
VDDR#31
VDDR#32
VDDR#33
VDDR#34
LEVEL TRANSLATION
VDD_CT#1
VDD_CT#2
VDD_CT#3
VDD_CT#4
I/O
VDDR3#1
VDDR3#2
VDDR3#3
VDDR3#4
VDDR4#4
VDDR4#5
VDDR4#7
VDDR4#8
VDDR4#1
VDDR4#2
VDDR4#3
VDDR4#6
NC_VDDRHA
NC_VSSRHA
NC_VDDRHB
NC_VSSRHB
PLL
PCIE_PVDD
MPV18#1
MPV18#2
SPV18
SPV10
SPVSS
VOLTAGE SENESE
FB_VDDC
FB_VDDCI
FB_GND
POWER
SW@SEYMOUR_M2
(1.8V@110mA VDD_CT)
VDDC_CT
(3.3V@60mA)
(1.8V@40mA PCIE_PVDD)
(1.8V@150mA MPV18)
(1.8V@75mA SPV18)
(1.0V@120mA SPV10)
PCIE
PCIE_VDDR_L8
(1.8V@400mA PCIE_VDDR)
(1.0V@1.1A PCIE_VDDC)
C06
CORE
(30A or more)
+VGPU_CORE
ISOLATED CORE I/O
Ra should be removed by PX 4.0 (BACO mode)
Ra
+VGPU_CORE
OBIF_VDDC
55mA @ 1V in BCAO mode
U15F
GND
VSS_MECH#1
VSS_MECH#2
VSS_MECH#3
PX_EN 17
BACO reference schematics for detail
PowerXpress control signal for Park only
If not used, can be disconnected.
PX_EN = LOW, turn on
PX_EN = HIGH, turn off
PX_EN is used to turn ON/OFF some regulators for PowerXpress mode. An output high '3.3V' will turn the regulators OFF. An output low '0V' will turn the regulators ON. PX_EN outputs low (0V) by default.
If this signal is unused, it can be NC (not connected) or connected to ground.
GPU power enable
dGPU_VRON
dGPU_PWREN
dGPU_PWR_EN
dGPU_VRON
dGPU_PWREN 38,39
Change from 100K to 4.7K
>1mS delay is required between all MXM power rail stable and MXM_PWREN(enables the module internal power)
GPU all PWROK
dGPU_PWROK 8
GPU +3V_D power
dGPU_PWREN
+3V_D_EXT
+3V_D
Quanta Computer Inc.
PROJECT : ZQG
Seymour (PWR/GND)4/6
Rev 1A
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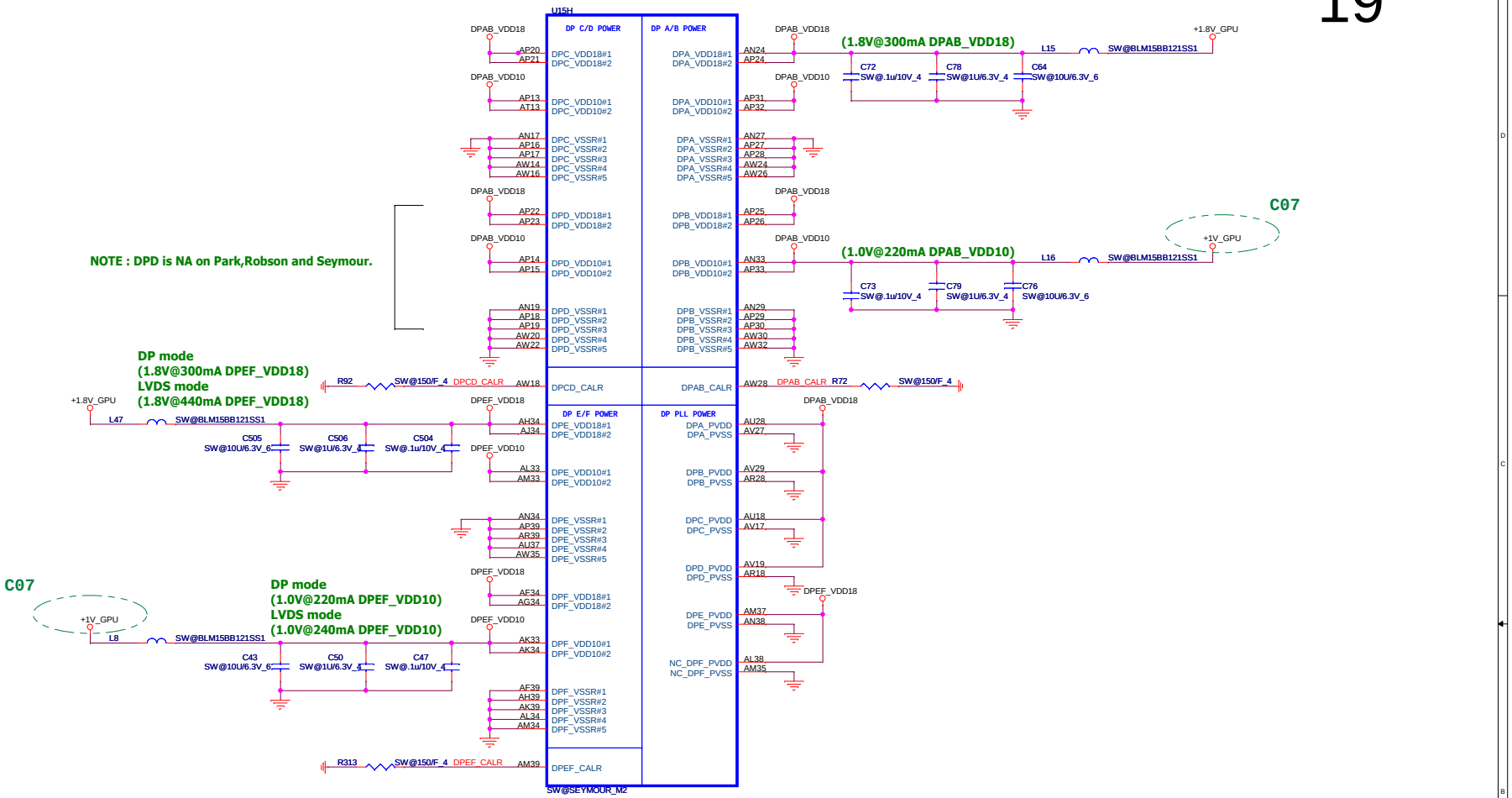
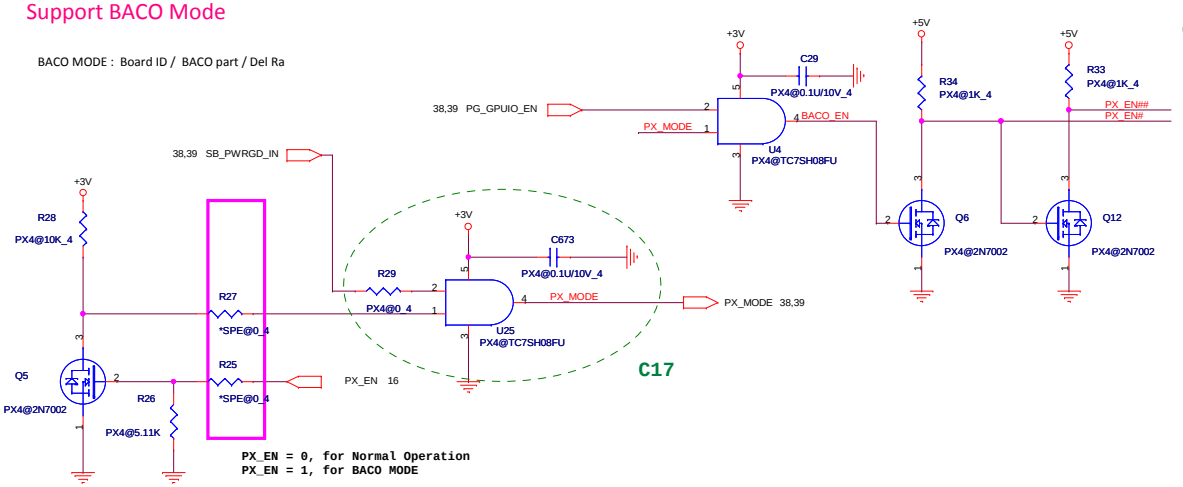
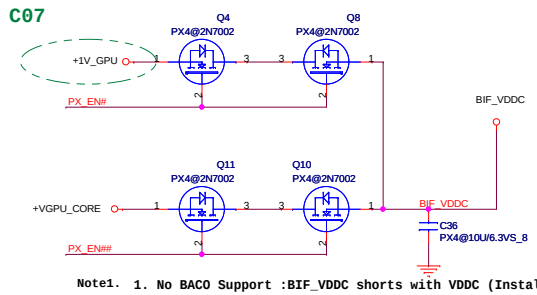


Support BACO Mode

BACO MODE : Board ID / BACO part / Del Ra





Note1. 1. No BACO Support :BIF_VDDC shorts with VDDC (Install Ra)

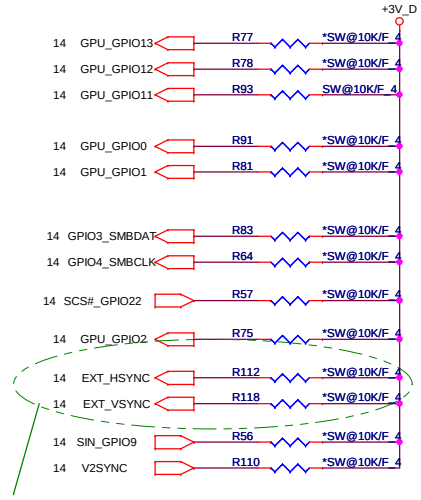
2. BACO Support: Refer to the BACO reference schematics/Application note for detail about BIF_VDDC Rail if BACO is Supported (Uninstall Ra)

Quanta Computer Inc.

PROJECT : ZQ6

Size	Document Number	Rev
	Seymour (DP_PWR/GND)5/6	1A
Date: Monday, November 01, 2010	Sheet 17 of 41	

PIN STRAPS



C08 : to slove the HDMI issue , remove R112,R118 from BOMs

Memory Aperture size	
GPIO[13:11]	Size
000	128MB
001	256MB
010	64MB
011	32MB

C02 : to slove the Power DVD issue , setting size to 256MB

ROM Table		
EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by dectec
1	0	DP only
1	1	Both DP & HDMI

CONFIGURATION STRAPS

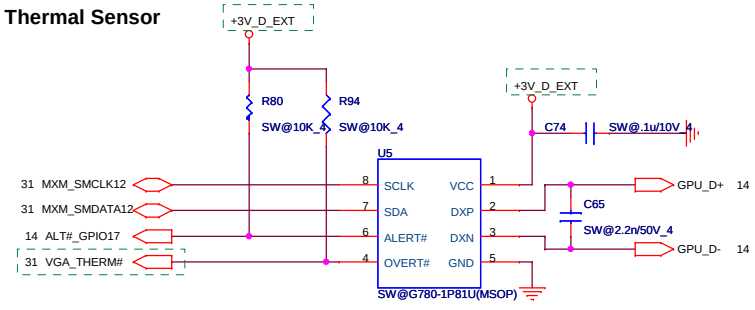
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT NUMONYX M25P10A : 101	000	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	00	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

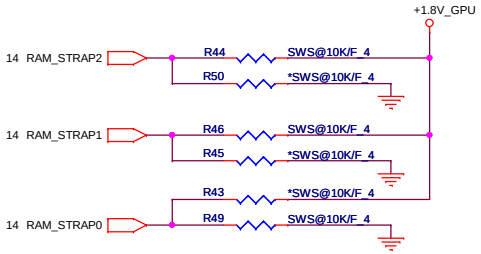
DDR3 Memory Aperture size

Vendor	Vendor P/N	STN B/S P/N	Total Memory Size	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0	ZQE/G
Hynix	H5TQ1G63DFR-11C	AKD5LZWTW05 (64M*16)	1GB (900 Mhz)	1	1	0	V
	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	1GB (800 Mhz)	1	0	0	V
	H5TQ2G63BFR-12C	AKD5MGGTW03 (128M*16)	2GB	1	1	1	V
Samsung	K4W1G1646G-BC11	AKD5EGGT503 (64M*16)	1GB	0	1	0	
	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	1GB (800 Mhz)	0	0	0	V
	K4W2G1646B-HC12	AKD5MGGT500	2GB	0	0	1	

Thermal Sensor



Address ID: 98H



RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.

Quanta Computer Inc.
PROJECT : ZQG

Size	Document Number	Rev
	Seymour Strip/Thermal 6/6	1A
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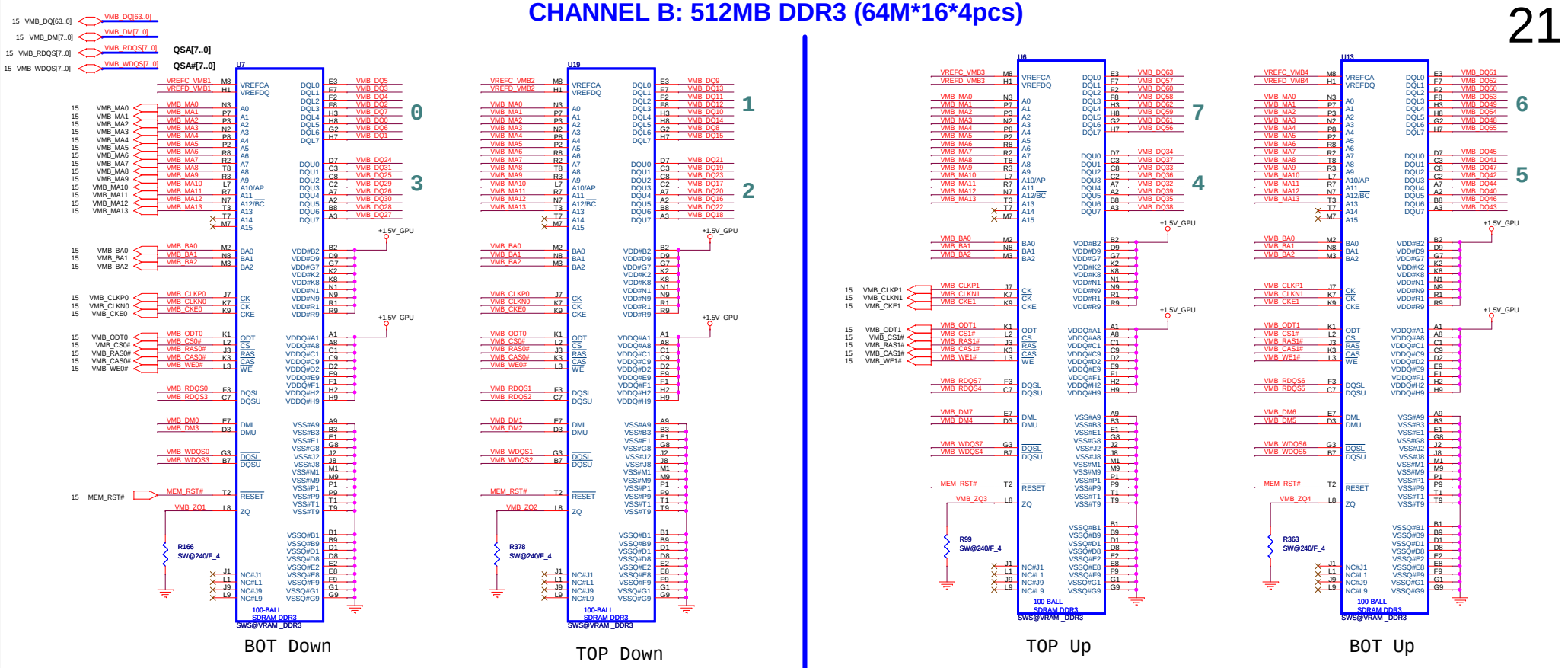
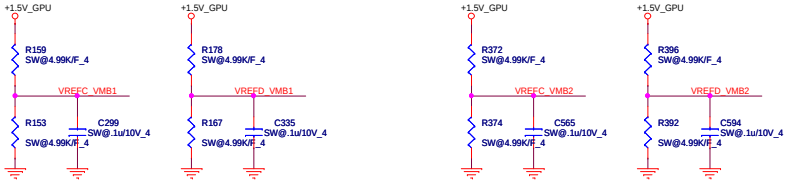
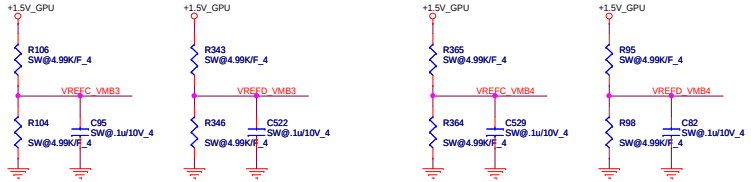
CHANNEL B: 512MB DDR3 (64M*16*4pcs)



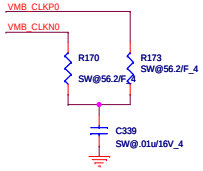
Group-B0 VREF



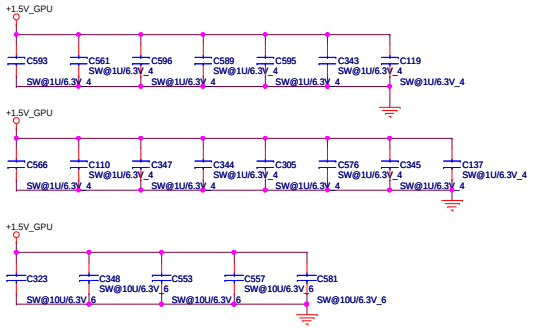
Group-B1 VREF



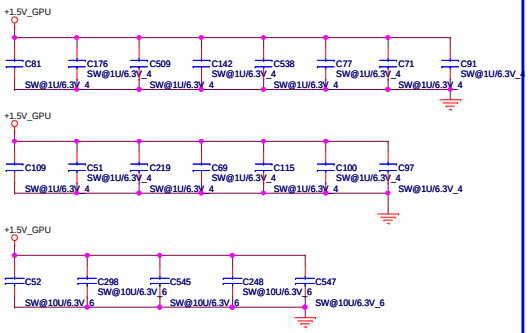
MEM_B0 CLK



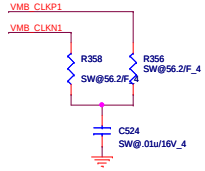
Group-B0 decoupling CAP



Group-B1 decoupling CAP



MEM_B1 CLK



Quanta Computer Inc.
PROJECT : ZQG

Size	Document Number	Rev
	MEMORY 2 channel B	1A
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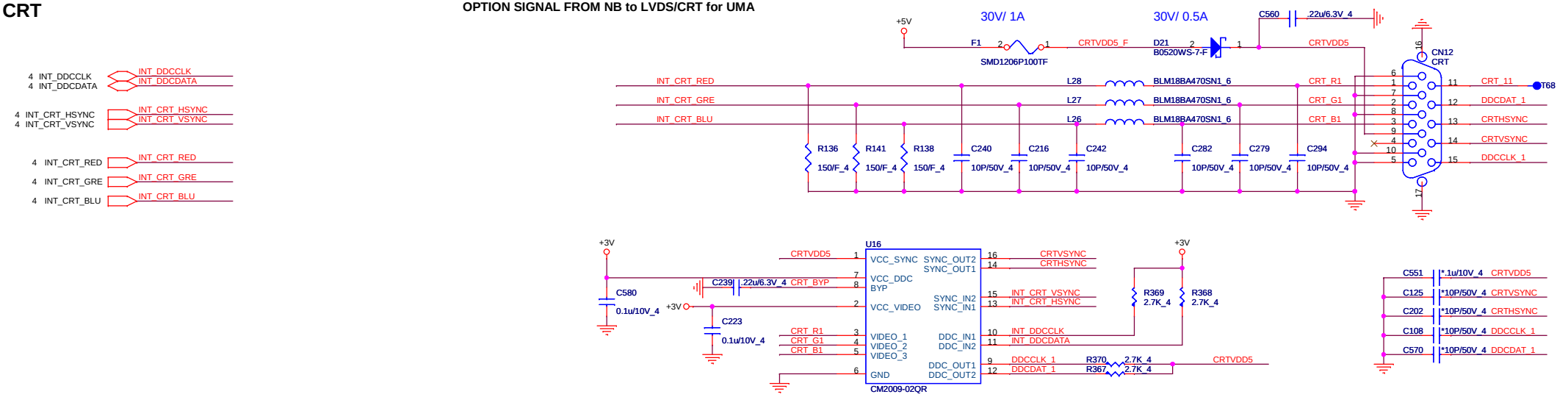
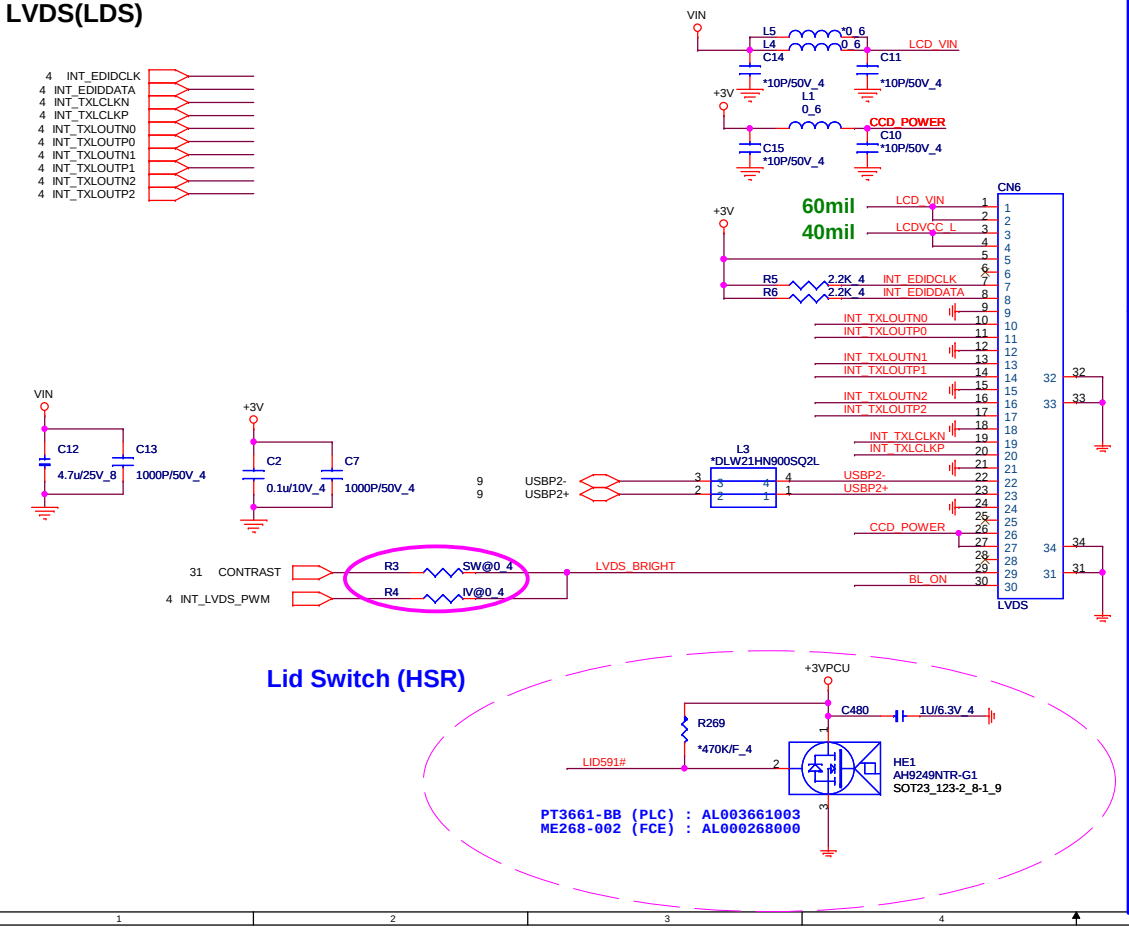
CRT

OPTION SIGNAL FROM NB to LVDS/CRT for UMA

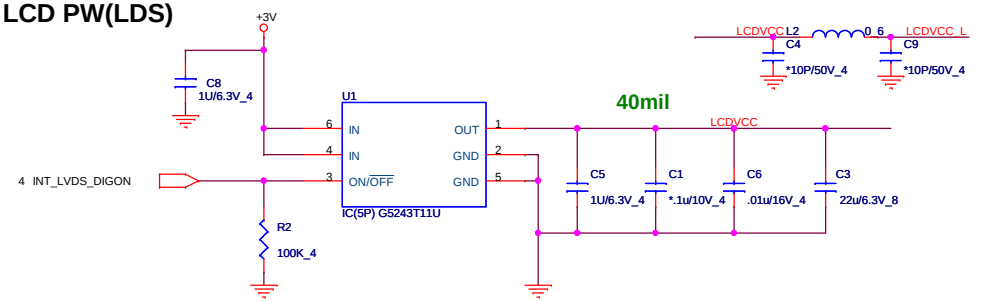


LVDS(LDS)

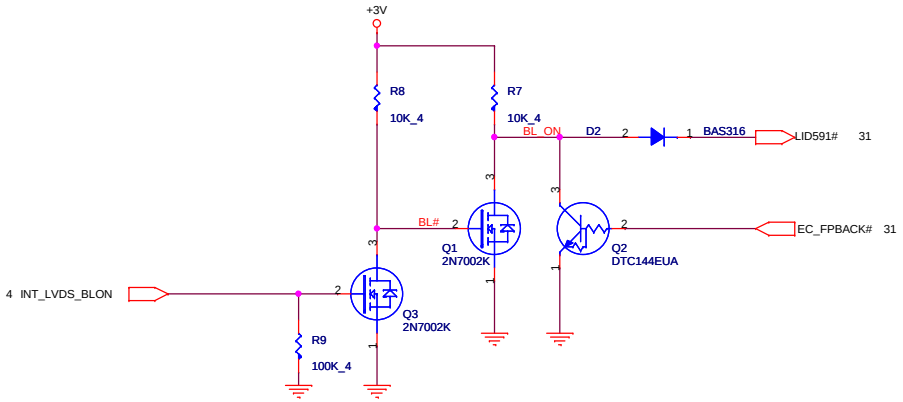


Lid Switch (HSR)

LCD PW(LDS)



Backlight Control(LDS)



Quanta Computer Inc.

PROJECT : ZQG

Size	Document Number	Rev
	CRT/LVDS/LID	1A

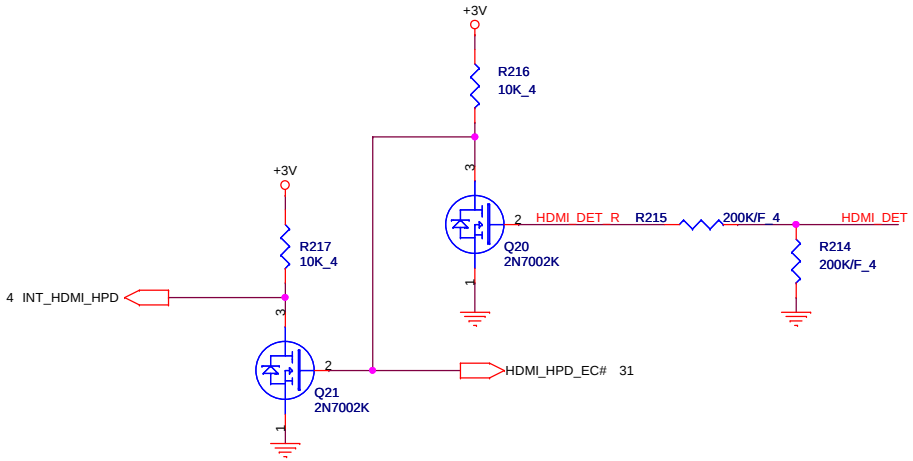
Date: Monday, November 01, 2010 Sheet 20 of 41

HDMI SDVO I2C Control

4 HDMI_DDCDATA
4 HDMI_DDCCLK
HDMI_DDCDATA
HDMI_DDCCLK

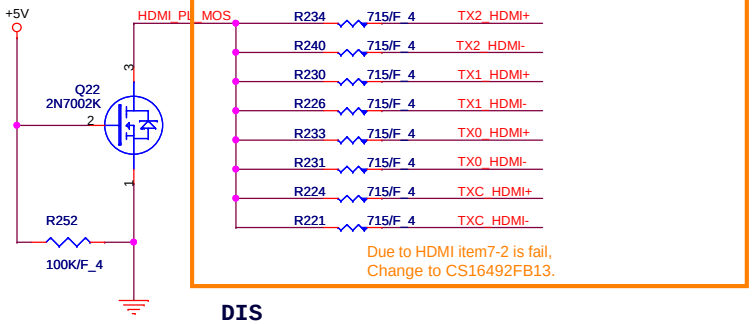
HDMI HPD SENSE (HDM)

UMA use +3V for the detect pin
Dis use +3V_DELAY for the detect pin



HDMI (HDM)

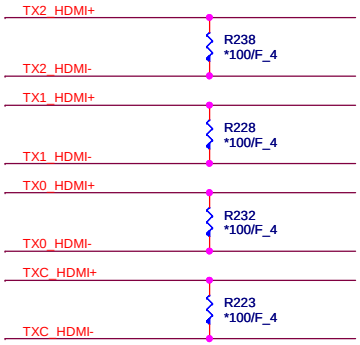
Close to HDMI Connector



DIS
Stuff 499 ohm CS14992FB24

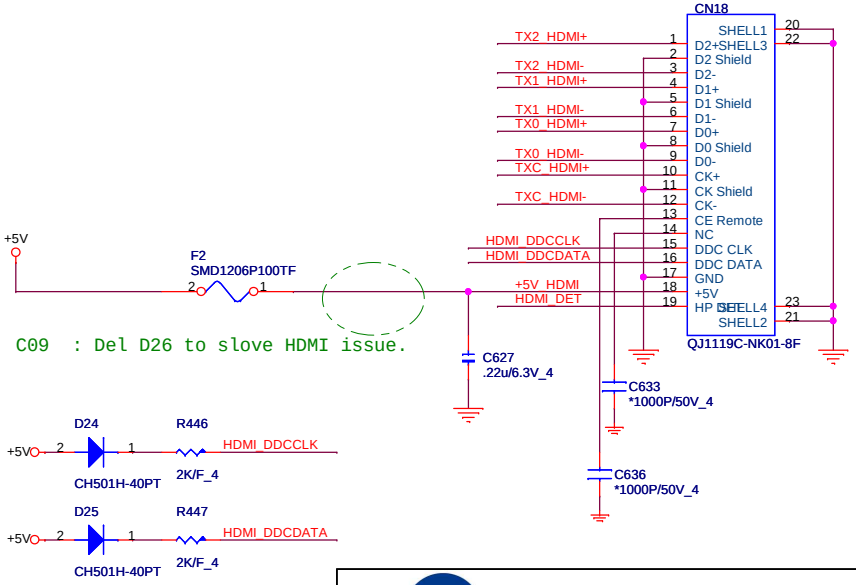
EMI reserve for HDMI(EMC)

Close connector



4 TX2_HDMI+
4 TX2_HDMI-
4 TX1_HDMI+
4 TX1_HDMI-
4 TX0_HDMI+
4 TX0_HDMI-
4 TXC_HDMI+
4 TXC_HDMI-
TX2_HDMI+
TX2_HDMI-
TX1_HDMI+
TX1_HDMI-
TX0_HDMI+
TX0_HDMI-
TXC_HDMI+
TXC_HDMI-

HDMI PORT (HDM)



C09 : Del D26 to slove HDMI issue.

Quanta Computer Inc.
PROJECT : ZQG

Size	Document Number	Rev
	HDMI	1A
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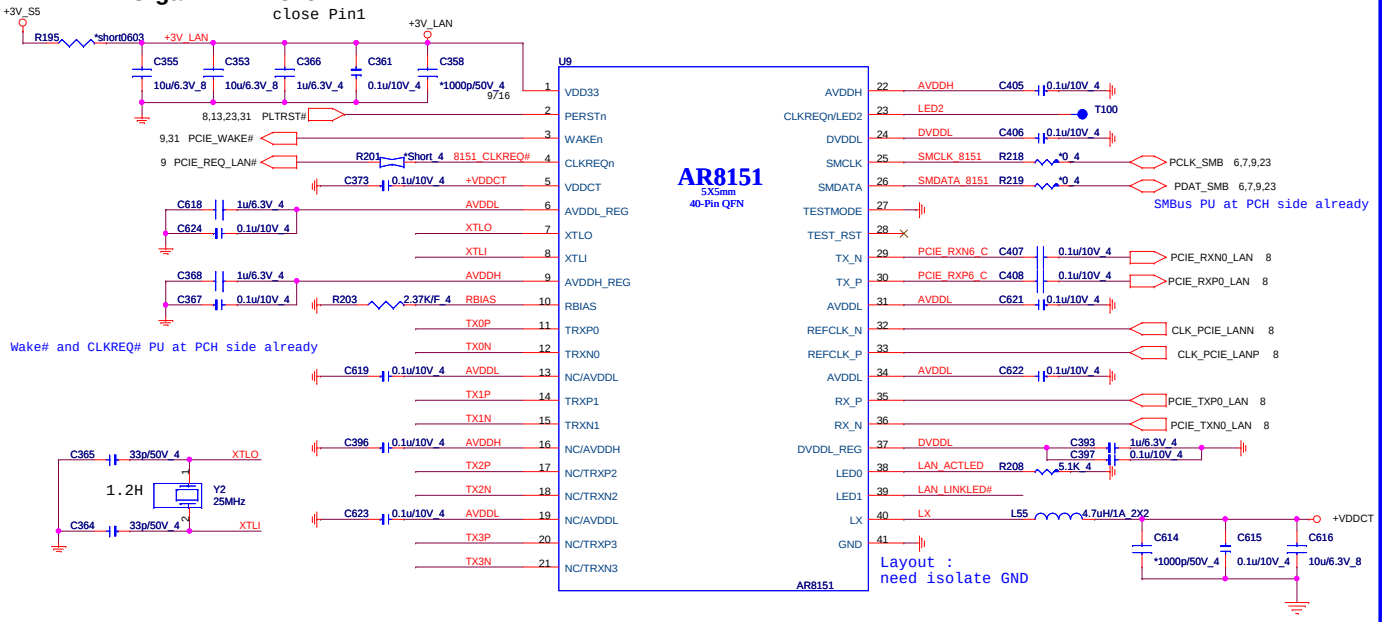
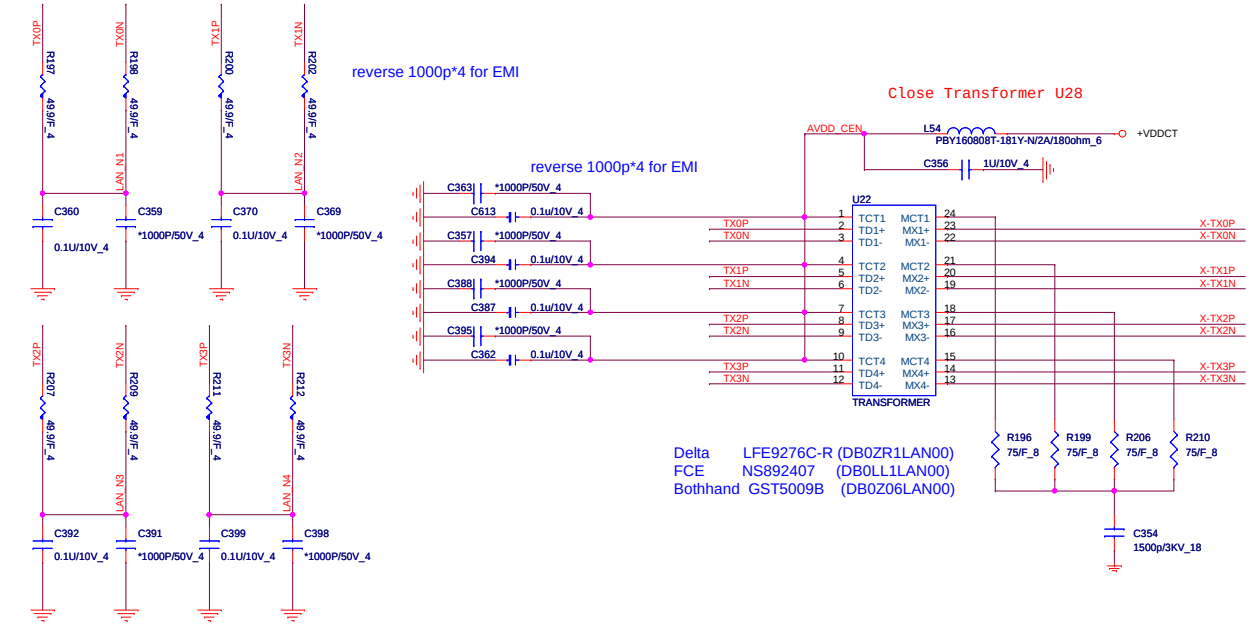
Giga-LAN AR8151

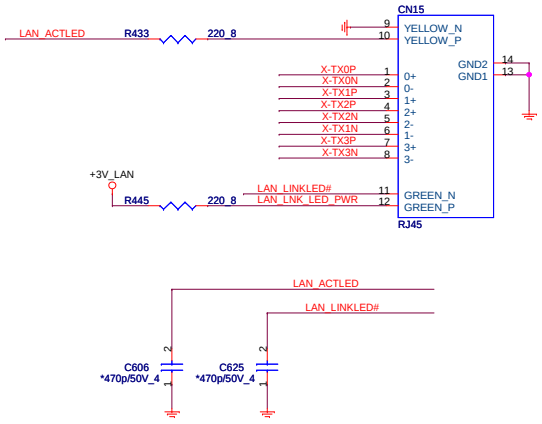
close Pin1



TRANSFORMER(LAN)



RJ45(LAN)

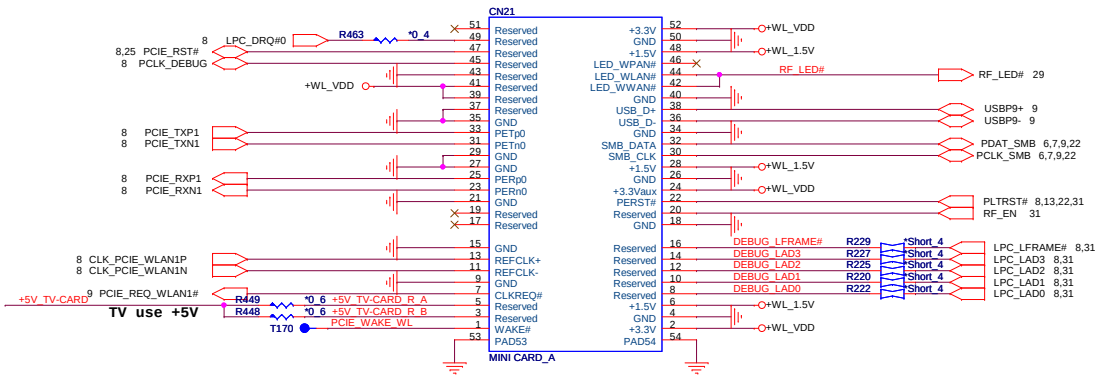


Quanta Computer Inc.		
PROJECT : ZQG		
Size	Document Number: LAN (AR8151)	Rev: 1A
Date: Monday, November 01, 2010	Sheet 22 of 41	

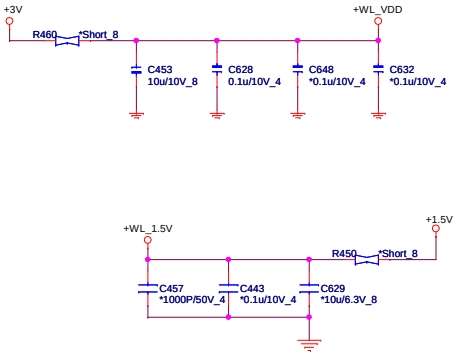
MINI-CARD WLAN(MPC)

+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

Check LED signal. (active high or low)



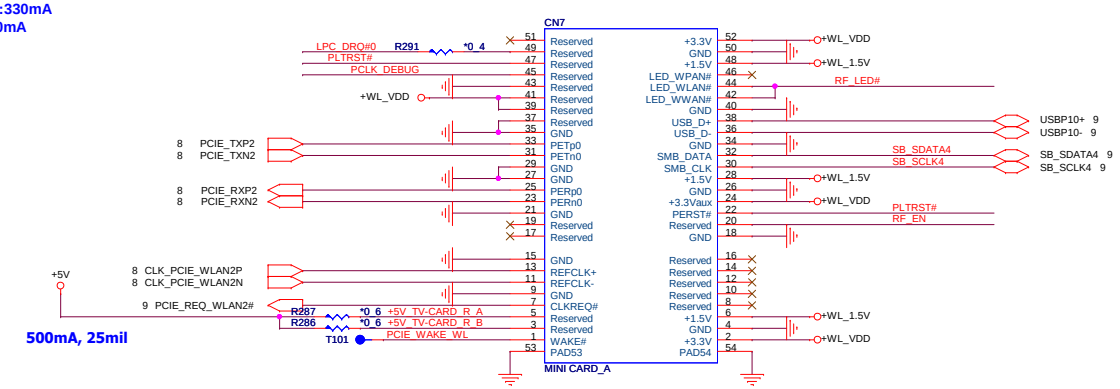
Debug

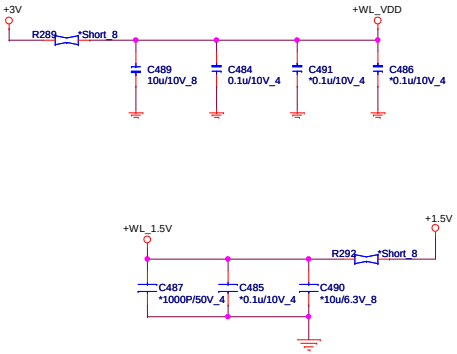


MINI-CARD WLAN(MPC)

+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

Check LED signal. (active high or low)

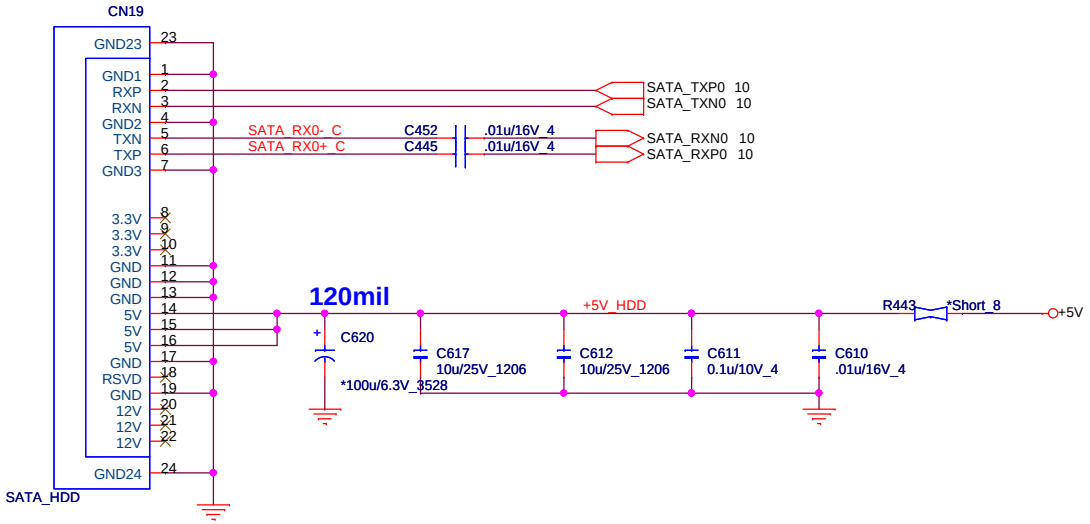




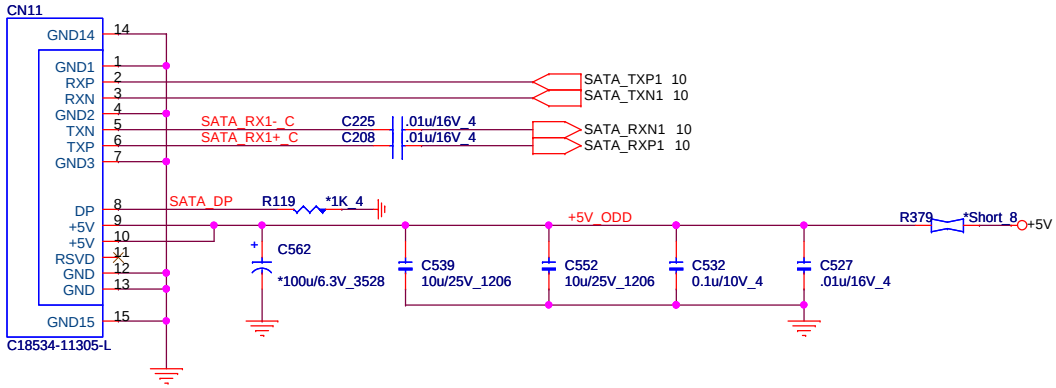
Quanta Computer Inc.
PROJECT : ZQG

Size	Document Number	Rev
	MINI PCI-E card	1A
Date: Monday, November 01, 2010	Sheet 23 of 41	

SATA HDD



SATA ODD



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PROJECT : ZQG

Size	Document Number	Rev
	SATA-HDD/ODD/HOLE	1A

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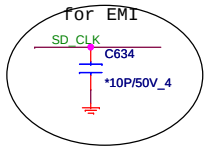
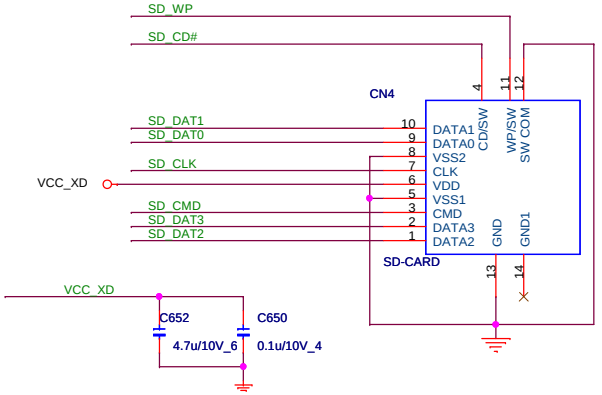
2 IN 1 CARD READER (MMC)

CARD READER Controller

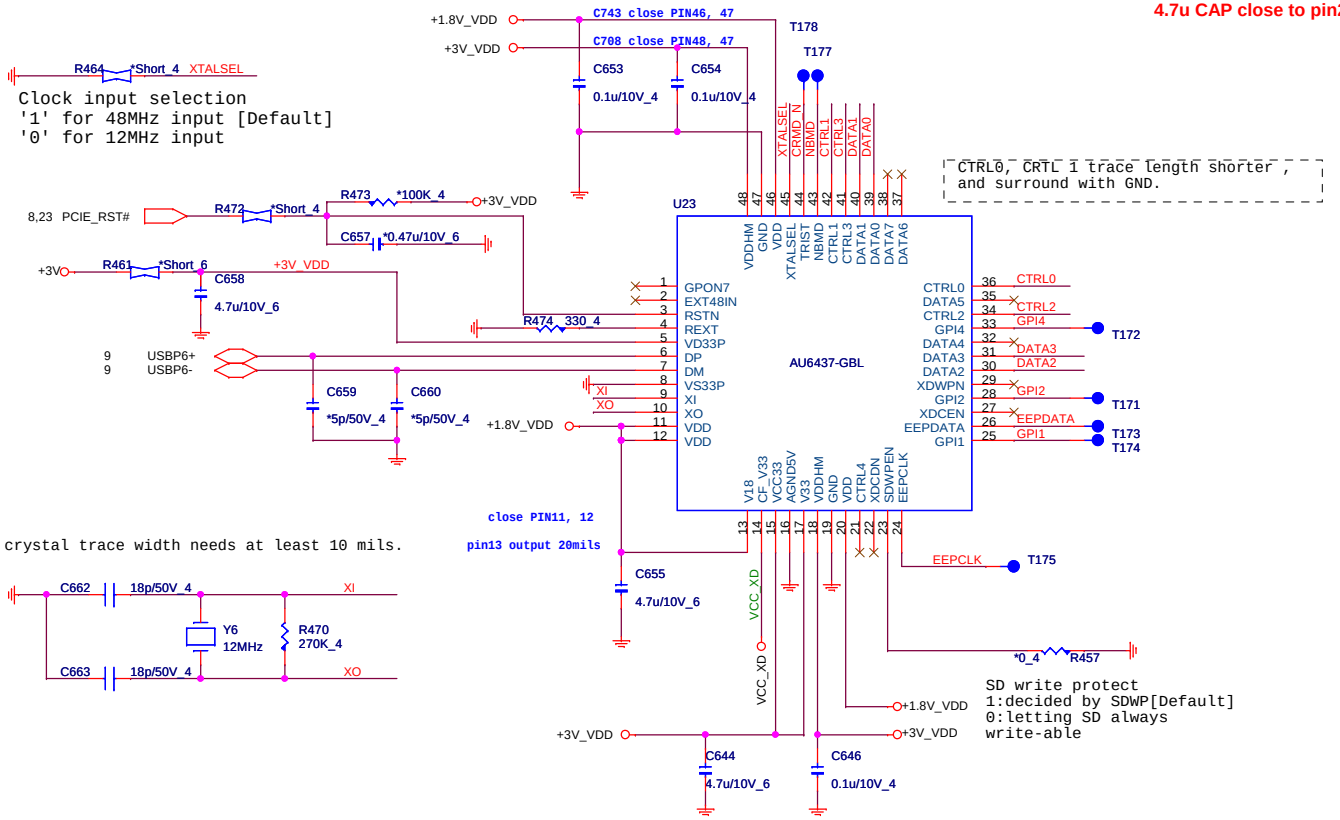


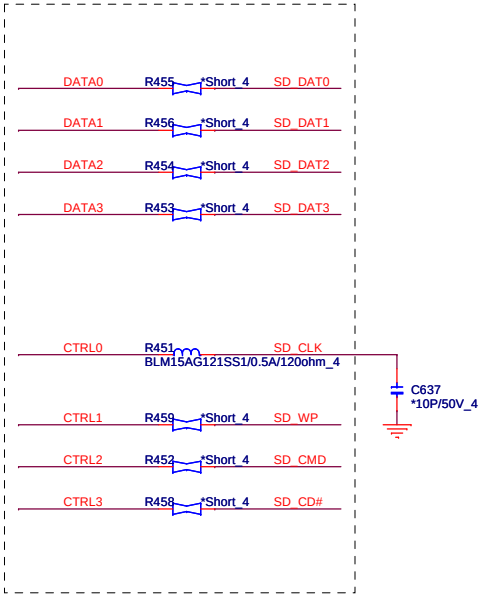
Main	DFHS11FR011
Second	DFHS11FR033



Close to CNxx pin 14 & pin23
4.7u CAP close to pin23

5/10 change Card Redaer conn
footpirnt sdcard-sdsn09-08-xa-11p-smt





Quanta Computer Inc.
PROJECT : ZQG

Size	Document Number	Rev
	AU6433 CardReader	1A
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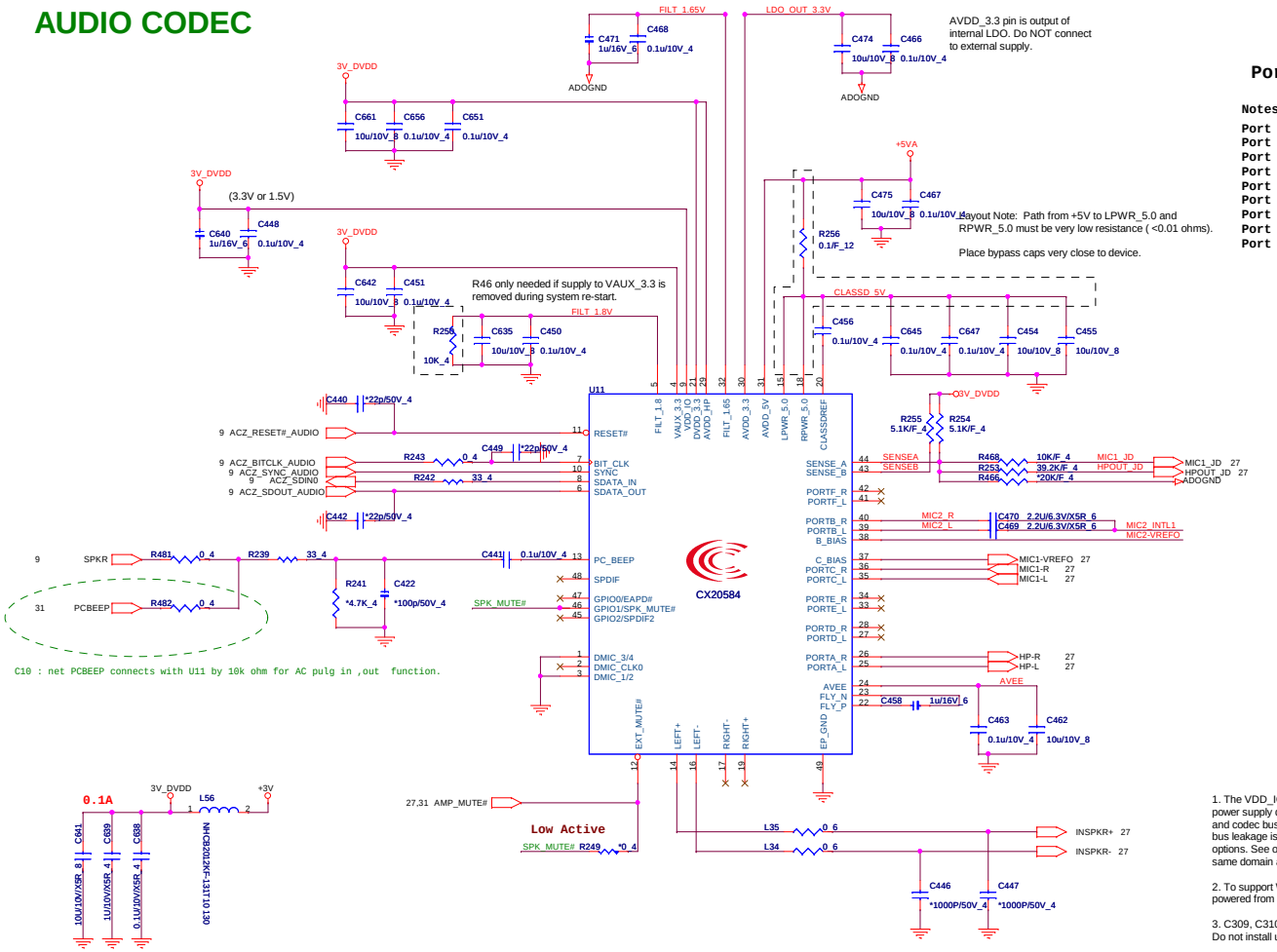
AUDIO CODEC



AVDD_3.3 pin is output of internal LDO. Do NOT connect to external supply.

Port Configuration

Notes:

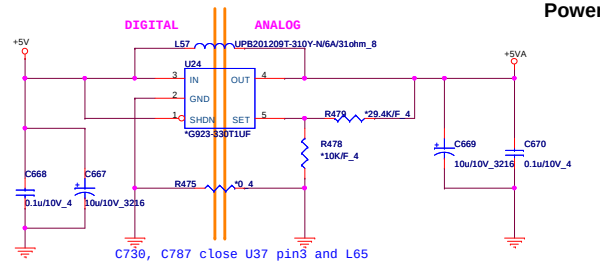
Port A: Headphone jack (jack shared with S/PDIF)
Port B: Internal MIC (mono or stereo)
Port C: Microphone/LI/LO jack
Port D: Line Out jack (Optional)
Port E: Line In jack (Optional)
Port F: Not used.
Port G: Internal stereo speakers
Port J: Internal stereo digital mic (Optional)
Port H: S/PDIF (jack shared with headphone)

1. The VDD_IO and VAUX_3.3 pins should be connected to same power supply domain as HDA bus controller so that the HDA controller and codec bus interface will power-up at the same time. This will avoid bus leakage issues if using HDA controller with bus pull-up strap options. See other FET option on this page if these supplies are not on same domain as HDA controler.

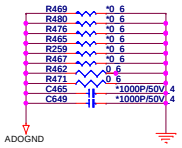
2. To support Wake-on-Jack, the codec VAUX_3.3 pin must be powered from a Standby supply.

3. C309, C310, C311 are optional.
Do not install unless needed for EMI/SI.

Power (ADO)



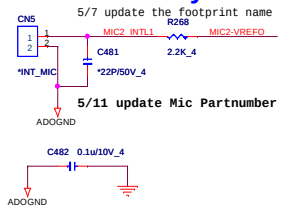
C730, C787 close U37 pin3 and L65



Tied at one point only under the codec or near the codec

INT MIC array

5/7 update the footprint name



5/11 update Mic Partnumber

cap place close to MIC-connector

Quanta Computer Inc.
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	CONEXANT 20584	1A

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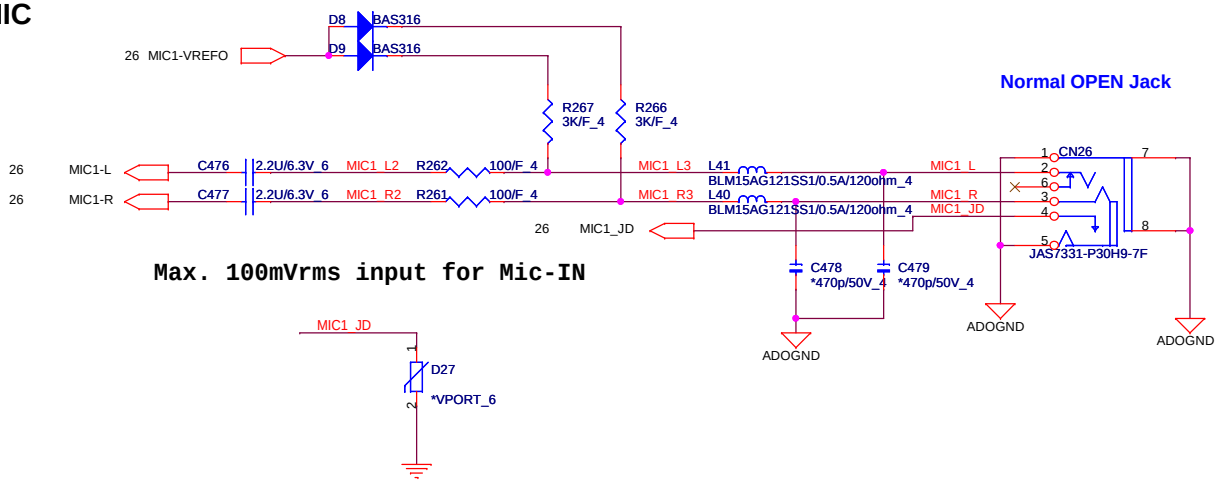
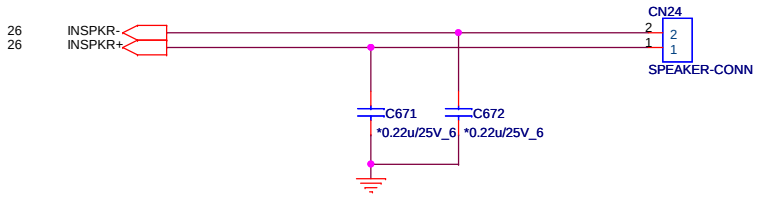
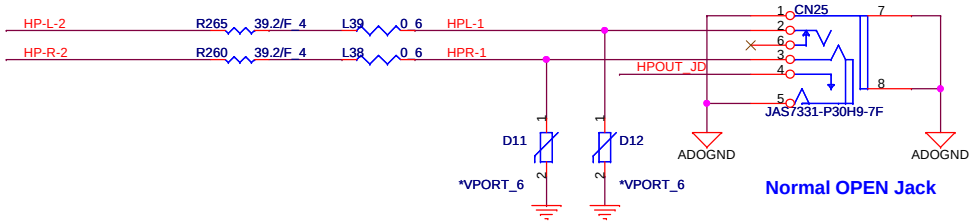
MIC

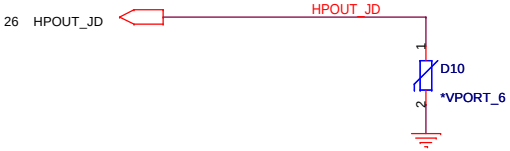


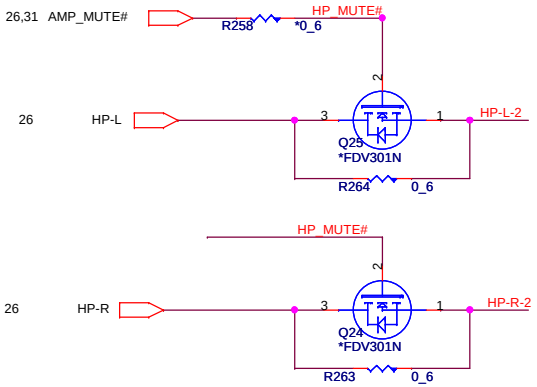
Internal Speaker



HP







Quanta Computer Inc.

PROJECT : ZQG

Size	Document Number	Rev
	AUDIO JACK CONN	1A
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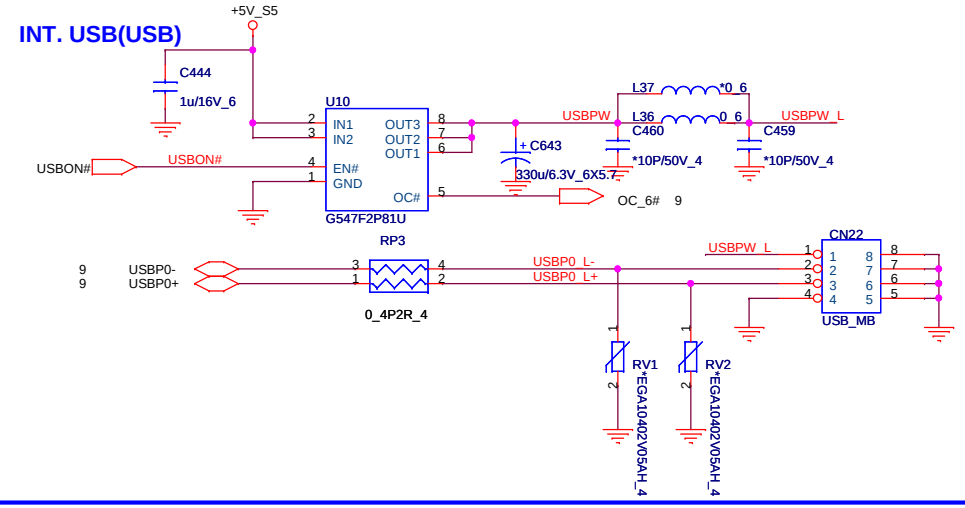
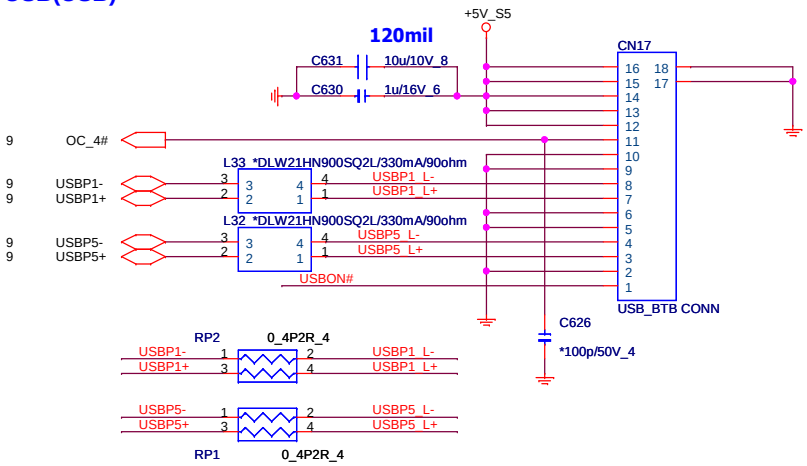
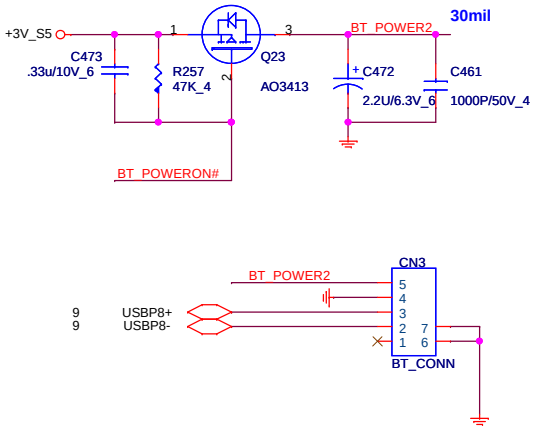
INT. USB(USB)



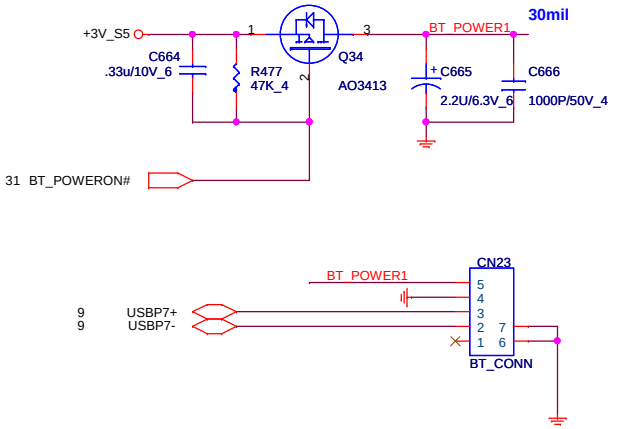
EXT. USB(USB)



BLUETOOTH V2.1 CONN(BTM)



BLUETOOTH V3.0 CONN(BTM)



Quanta Computer Inc.

PROJECT : ZQG

Size	Document Number	Rev
	USB/BT	1A

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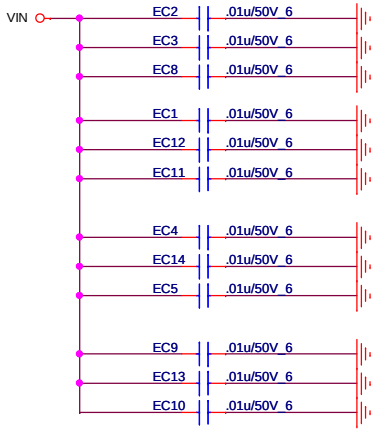
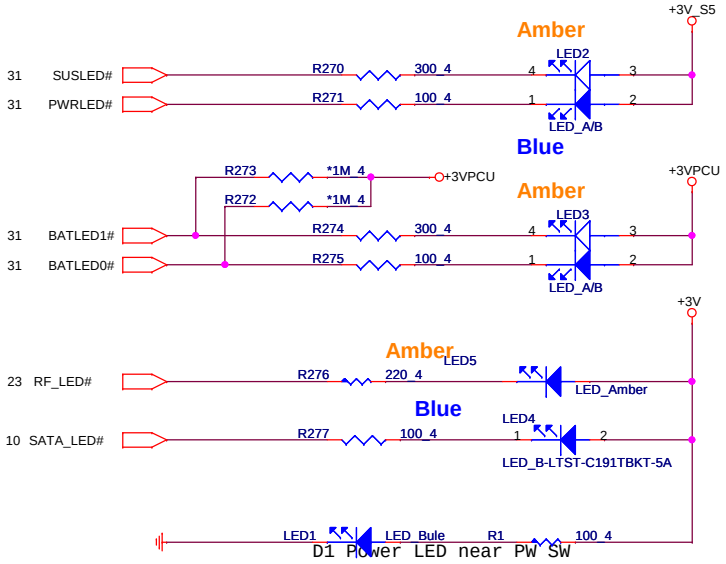
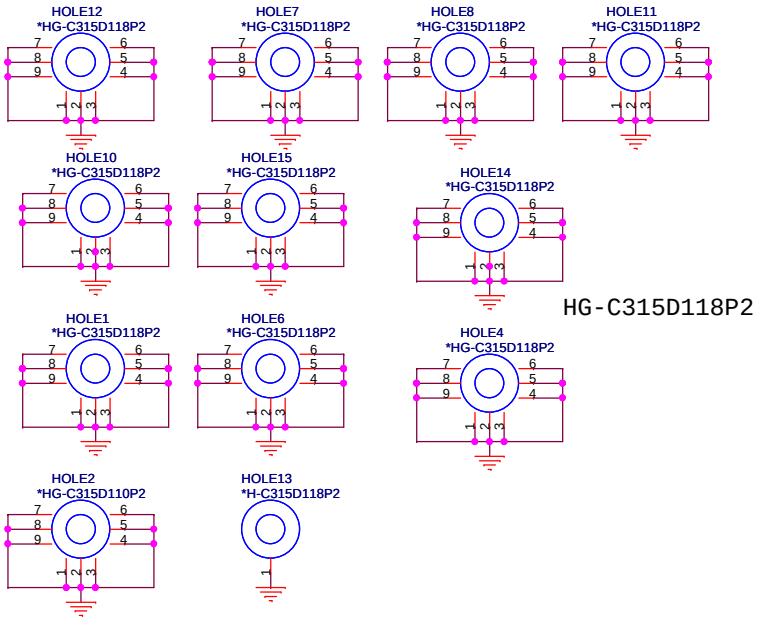
EE RETURN-PATH CAPACITORS(EMC)



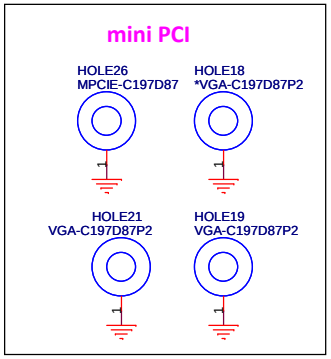
LED(UIF)

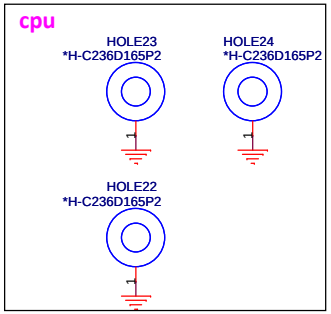


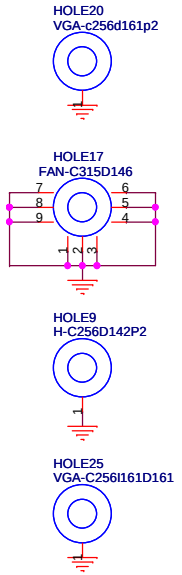
HOLE(OTH)

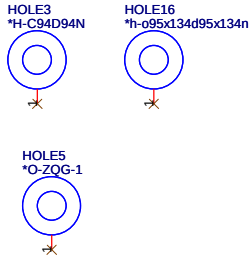


HG-C315D118P2









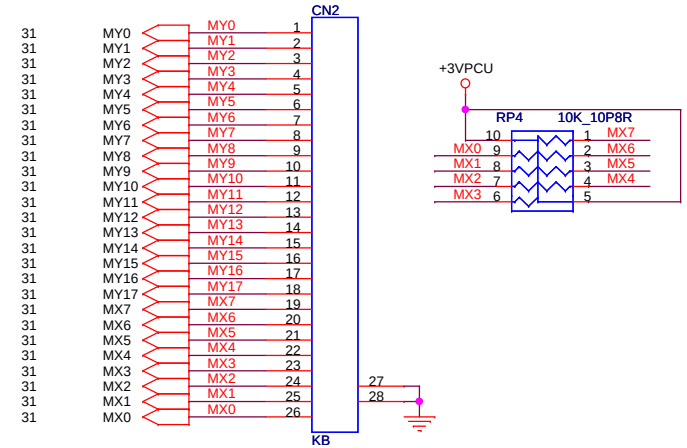
CPU nut PN : FBBU1001010 x 3 @ SHOLE1~3

Quanta Computer Inc.

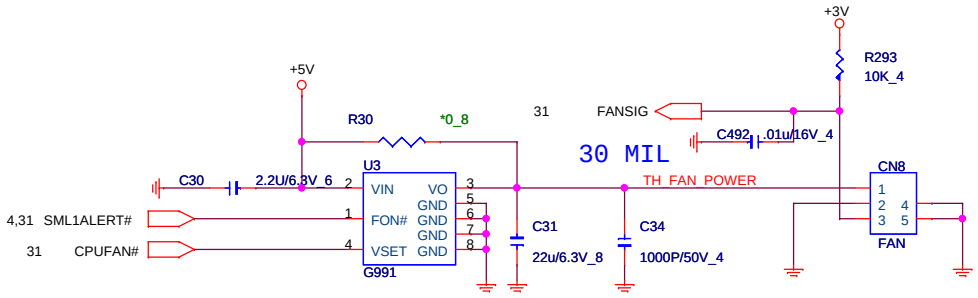
PROJECT : ZQG

Size	Document Number	Rev
	29 -- LED/ EMI/ Screw Hole& Nut	1A
Date: Monday, November 01, 2010	Sheet 29 of 41	

K/B(KBC)

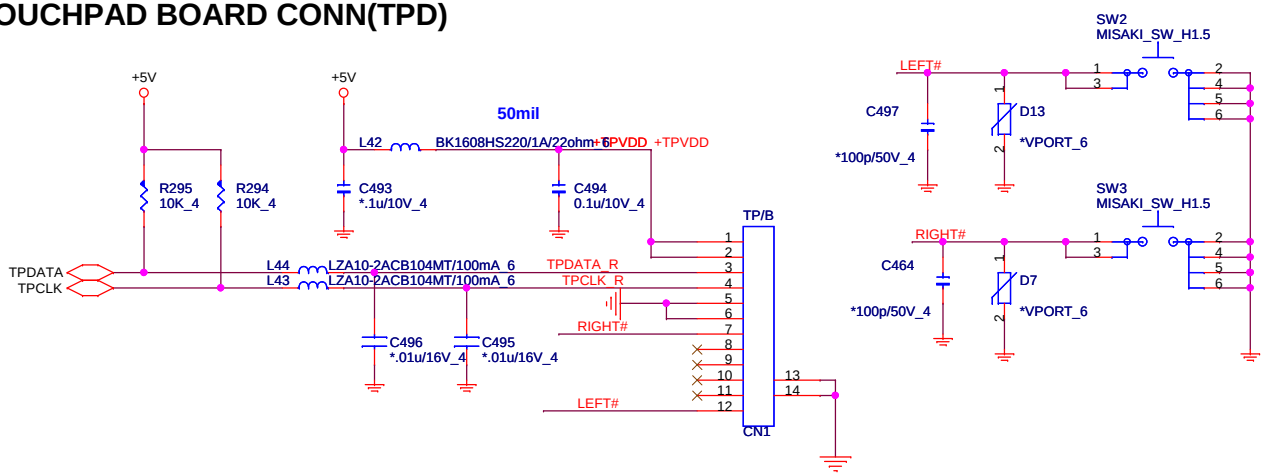


CPU FAN(THM)



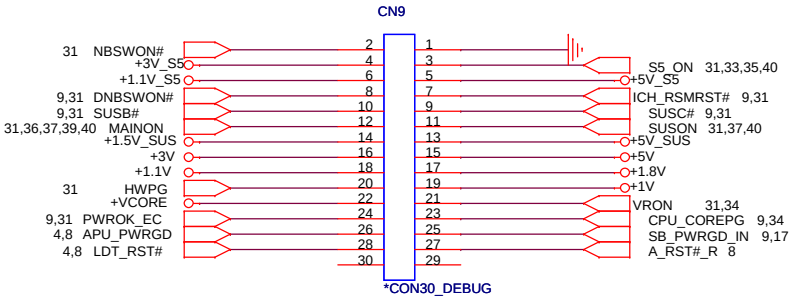
change footpirnt as SA6
4/23

TOUCHPAD BOARD CONN(TPD)



Power Sequence

0903--Add Connecotr



Quanta Computer Inc.		
PROJECT : ZQG		
Size	Document Number: 30 -- KB/TP/FAN	Rev: 1A
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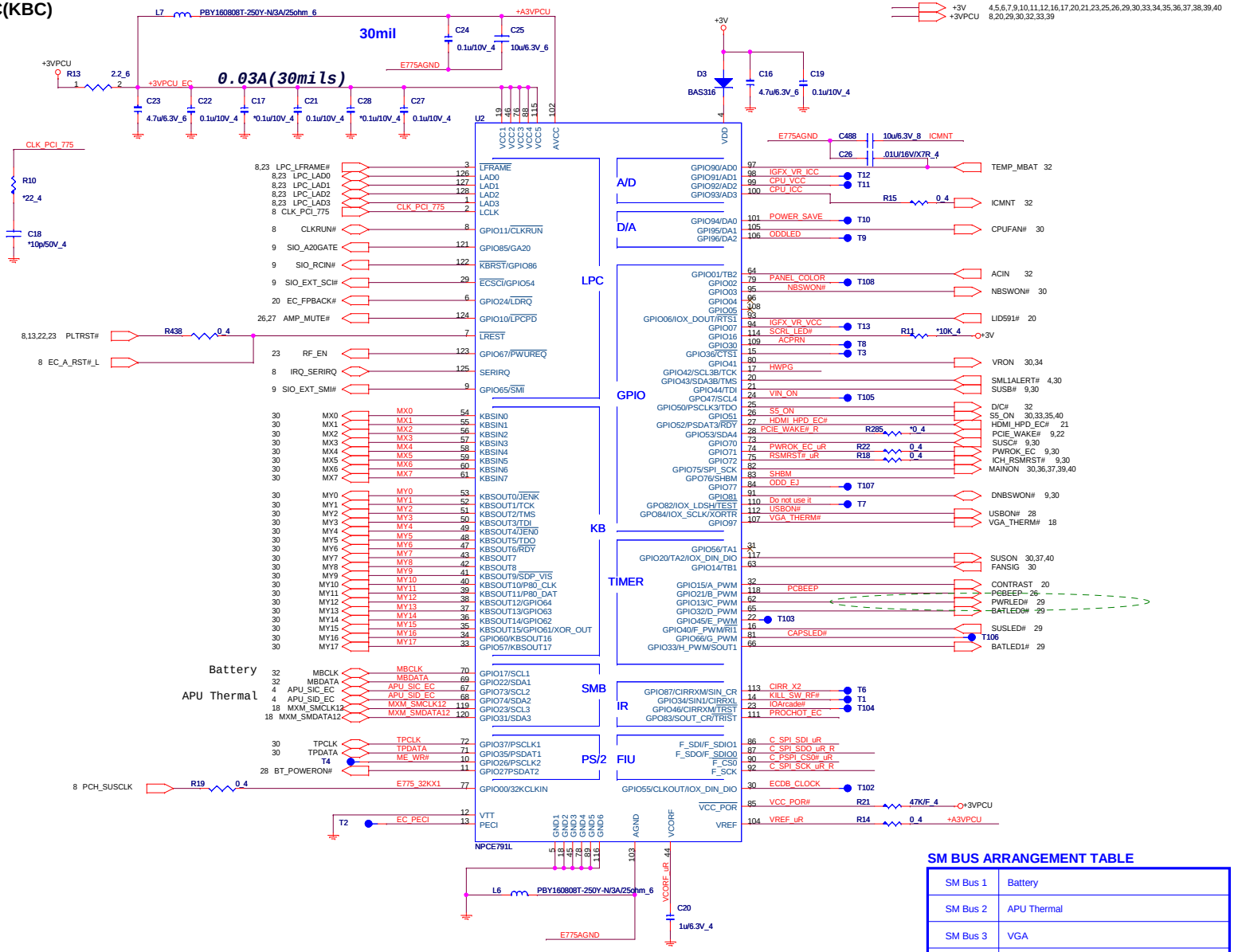
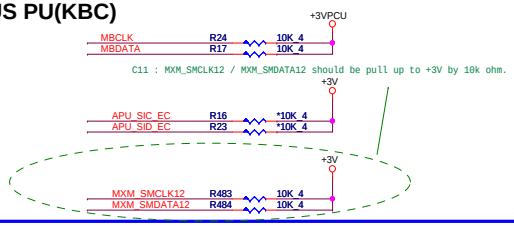
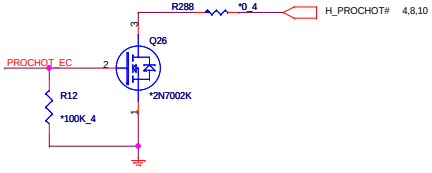
EC(KBC)



I/O ADDRESS SETTING(KBC)

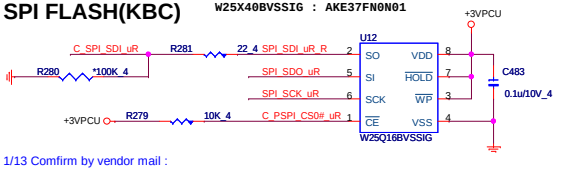
SM BUS PU(KBC)





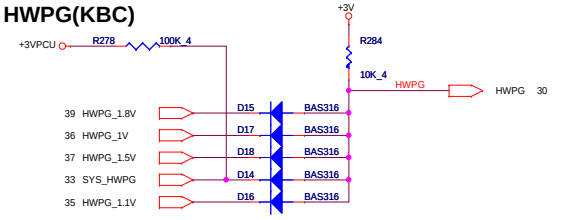
SPI FLASH(KBC)

socket : DG008000031
W25X40BVSSIG : AKE37FN0N01

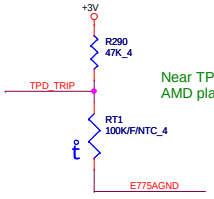


1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by
default, the flash device should be 50MHz (or faster)

HWPG(KBC)



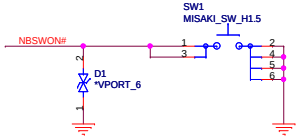
PALM REST THERMAL SENSOR (THM)

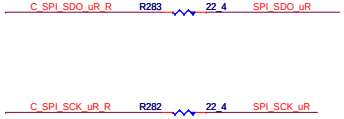


Near TP on TOP side and only for
AMD platform Palm Rest use.

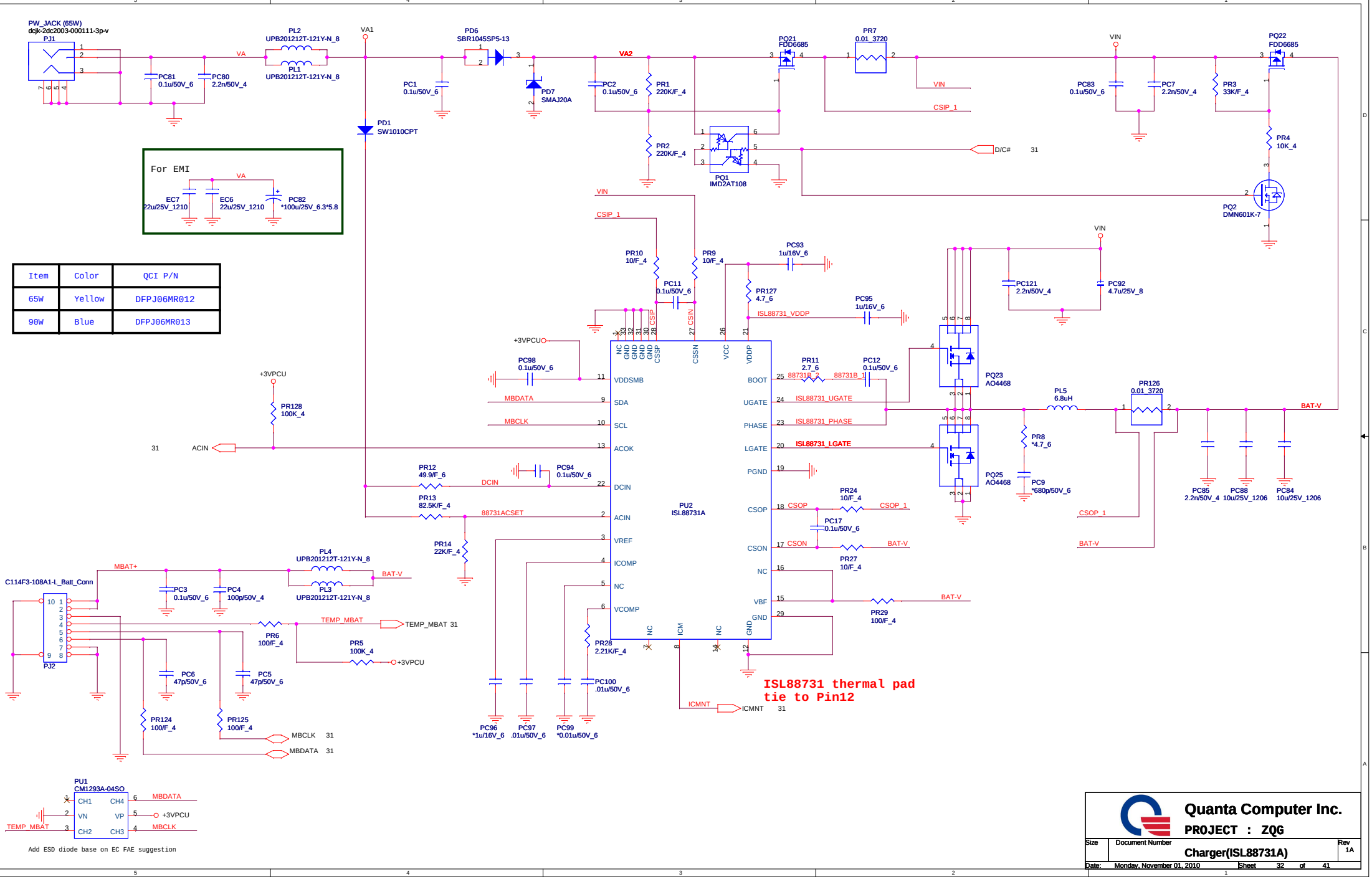
(02/25)
Per QSMC SMT request, change to
Mitsubishi.
Main: CU4100B0000
Second: CU410000Z07 (MIT)

POWER-ON SWITCH (KBC)





Quanta Computer Inc.	
PROJECT : ZQ6	
Size	Document Number: WPCE791 & FLASH — Rev: 1A
Date: Monday, November 01, 2010	Sheet 31 of 41


PW_JACK (65W)
dcjk-2dc2003-000111-3p-v
PJ1
PL2
UPB201212T-121Y-N_8
PL1
UPB201212T-121Y-N_8
VA1
PD6
SBR1045SP5-13
PD7
SMAJ20A
PD1
SW1010CPT
VA2
PQ21
FDD6685
PR7
0.01_3720
VIN
CSIP_1
PQ22
FDD6685
PR3
33K/F_4
PR4
10K_4
PQ2
DMN601K-7
PC81
0.1u/50V_6
PC80
2.2n/50V_4
PC1
0.1u/50V_6
PC2
0.1u/50V_6
PR1
220K/F_4
PR2
220K/F_4
PQ1
IMD2AT108
D/C#
31
PC83
0.1u/50V_6
PC7
2.2n/50V_4
For EMI
EC7
22u/25V_1210
EC6
22u/25V_1210
PC82
*100u/25V_6.3*5.8
Item
Color
QCI P/N
65W
Yellow
DFPJ06MR012
90W
Blue
DFPJ06MR013
PR10
10/F_4
PR9
10/F_4
PC11
0.1u/50V_6
PR127
4.7_6
PC93
1u/16V_6
PC95
1u/16V_6
ISL88731_VDDP
PC121
2.2n/50V_4
PC92
4.7u/25V_8
+3VPCU
PC98
0.1u/50V_6
PR128
100K_4
31
ACIN
MBDATA
MBCLK
PR12
49.9/F_6
PR13
82.5K/F_4
DCIN
PC94
0.1u/50V_6
88731ACSET
PR14
22K/F_4
PU2
ISL88731A
NC
GND
GND
GND
GND
CSSP
CSSN
VCC
VDDP
VDDSMB
SDA
SCL
ACOK
DCIN
ACIN
VREF
ICOMP
NC
VCOMP
BOOT
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC
VBF
GND
NC
ICM
NC
GND
PR11
2.7_6
PC12
0.1u/50V_6
88731B_2
88731B_1
ISL88731_UGATE
ISL88731_PHASE
ISL88731_LGATE
PR24
10/F_4
PC17
0.1u/50V_6
PR27
10/F_4
PR29
100/F_4
PR28
2.21K/F_4
PC100
.01u/50V_6
PC96
*1u/16V_6
PC97
.01u/50V_6
PC99
*0.01u/50V_6
ICMNT
ISL88731 thermal pad
tie to Pin12
PQ23
AO4468
PQ25
AO4468
PL5
6.8uH
PR126
0.01_3720
PR8
*4.7_6
PC9
*680p/50V_6
BAT-V
CSOP_1
PC85
2.2n/50V_4
PC88
10u/25V_1206
PC84
10u/25V_1206
C114F3-108A1-L_Batt_Conn
PJ2
MBAT+
PC3
0.1u/50V_6
PC4
100p/50V_4
PL4
UPB201212T-121Y-N_8
PL3
UPB201212T-121Y-N_8
TEMP_MBAT
PR6
100/F_4
PR5
100K_4
TEMP_MBAT
31
PC6
47p/50V_6
PC5
47p/50V_6
PR124
100/F_4
PR125
100/F_4
MBCLK
31
MBDATA
31
PU1
CM1293A-04SO
CH1
CH4
VN
VP
CH2
CH3
MBDATA
+3VPCU
MBCLK
TEMP_MBAT
Add ESD diode base on EC FAE suggestion
Quanta Computer Inc.
PROJECT : ZQG
Size
Document Number
Charger(ISL88731A)
Rev
1A
Date:
Monday, November 01, 2010
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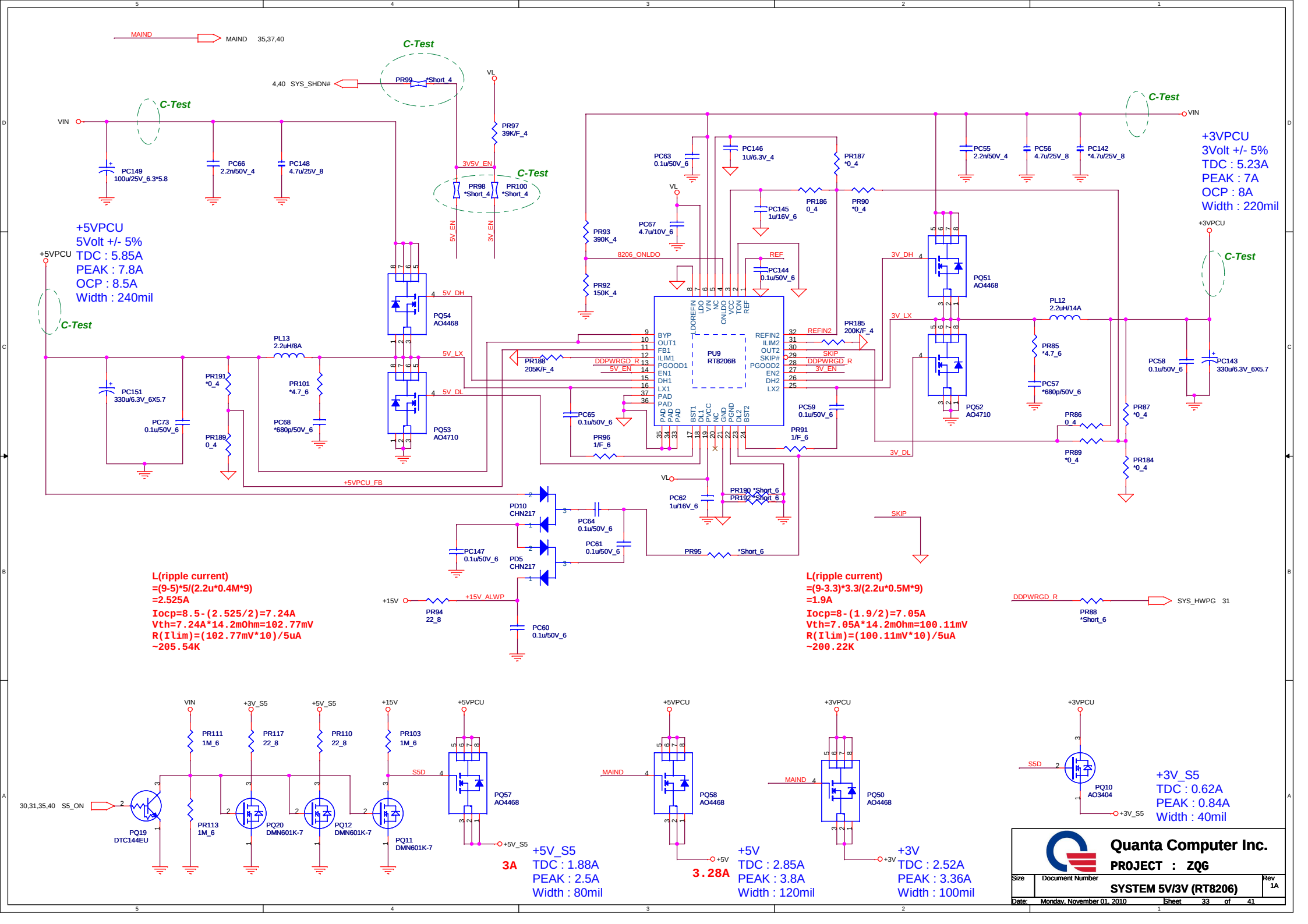
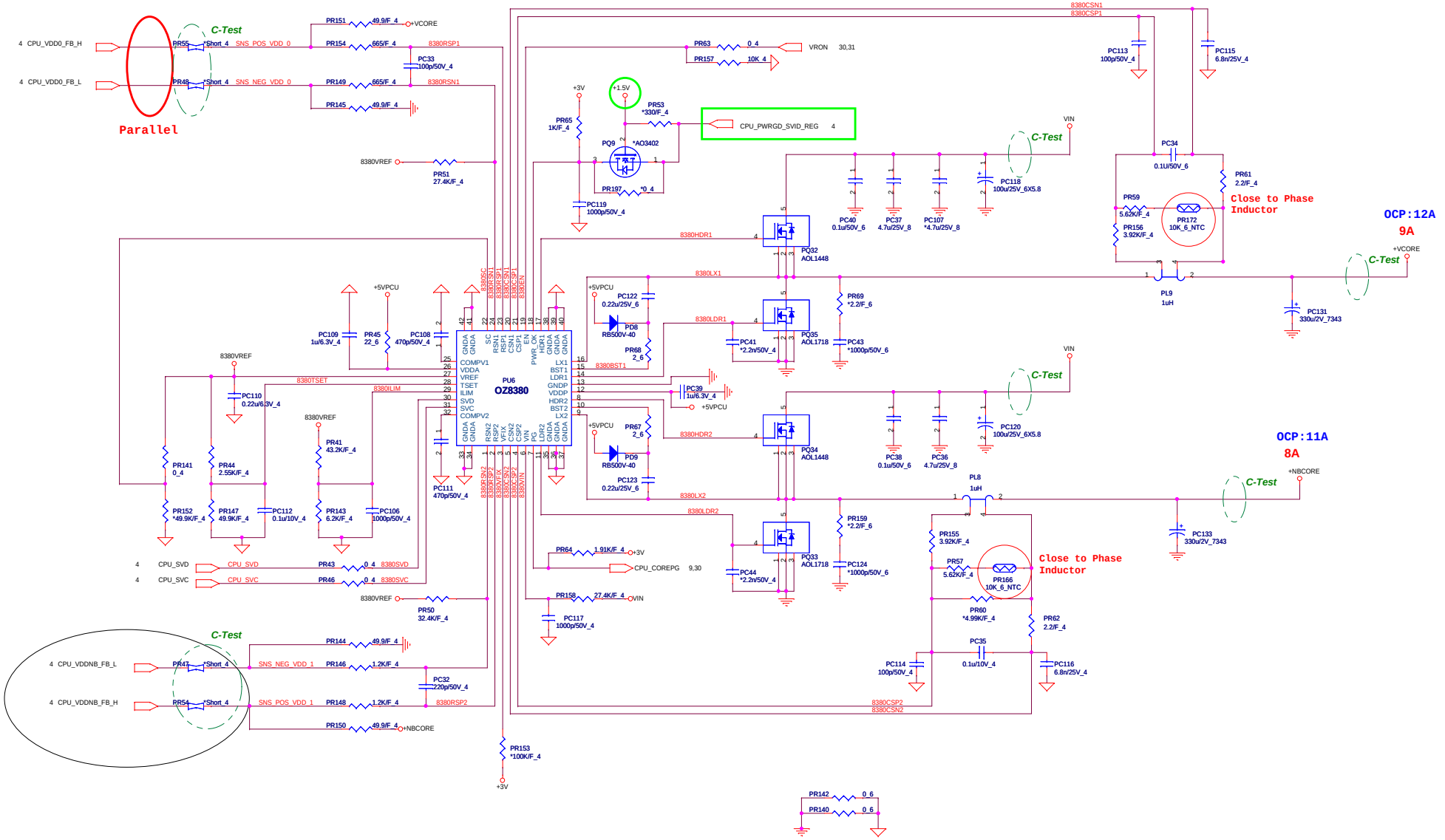
32
of
41


MAIND
MAIND 35,37,40
C-Test
4,40 SYS_SHDN#
PR99 *Short_4
VL
PR97 39K/F_4
3V5V_EN
PR98 *Short_4
PR100 *Short_4
5V_EN
3V_EN
VIN
PC149 100u/25V_6.3*5.8
PC66 2.2n/50V_4
PC148 4.7u/25V_8
+5VPCU
5Volt +/- 5%
TDC : 5.85A
PEAK : 7.8A
OCP : 8.5A
Width : 240mil
PC63 0.1u/50V_6
PC146 1U/6.3V_4
PR187 *0_4
PC55 2.2n/50V_4
PC56 4.7u/25V_8
PC142 *4.7u/25V_8
+3VPCU
3Volt +/- 5%
TDC : 5.23A
PEAK : 7A
OCP : 8A
Width : 220mil
PR186 0_4
PR90 *0_4
PC145 1u/16V_6
PC67 4.7u/10V_6
PR93 390K_4
8206_ONLDO
REF
PC144 0.1u/50V_6
PR92 150K_4
3V_DH
PQ51 AO4468
PL12 2.2uH/14A
3V_LX
PR85 *4.7_6
PC57 *680p/50V_6
PQ52 AO4710
PC58 0.1u/50V_6
PC143 330u/6.3V_6X5.7
PR86 0_4
PR87 *0_4
PR89 *0_4
PR184 *0_4
PR185 200K/F_4
REFIN2
SKIP
DDPWRGD_R
3V_EN
PR188 205K/F_4
5V_EN
PU9 RT8206B
LDOREFIN LDO VIN NC ONLDO VCC TON REF
BYP OUT1 FB1 ILIM1 PGOOD1 EN1 DH1 LX1 PAD PAD
REFIN2 ILIM2 OUT2 SKIP# PGOOD2 EN2 DH2 LX2
PAD PAD PAD BST1 PVCC NC GND PGND DL2 BST2
PC65 0.1u/50V_6
PC59 0.1u/50V_6
PR96 1/F_6
PR91 1/F_6
PR190 *Short_6
PR192 *Short_6
PC62 1u/16V_6
PD10 CHN217
PC64 0.1u/50V_6
PC61 0.1u/50V_6
PC147 0.1u/50V_6
PD5 CHN217
PR95 *Short_6
PC60 0.1u/50V_6
PR94 22_8
+15V
+15V_ALWP
PL13 2.2uH/8A
PC151 330u/6.3V_6X5.7
PR191 *0_4
PR189 0_4
PC73 0.1u/50V_6
PR101 *4.7_6
PC68 *680p/50V_6
5V_DH
5V_LX
5V_DL
PQ54 AO4468
PQ53 AO4710
+5VPCU_FB
L(ripple current)
=(9-5)*5/(2.2u*0.4M*9)
=2.525A
Iocp=8.5-(2.525/2)=7.24A
Vth=7.24A*14.2mOhm=102.77mV
R(Ilim)=(102.77mV*10)/5uA
~205.54K
L(ripple current)
=(9-3.3)*3.3/(2.2u*0.5M*9)
=1.9A
Iocp=8-(1.9/2)=7.05A
Vth=7.05A*14.2mOhm=100.11mV
R(Ilim)=(100.11mV*10)/5uA
~200.22K
DDPWRGD_R
PR88 *Short_6
SYS_HWPG 31
VIN
+3V_S5
+5V_S5
+15V
+5VPCU
PR111 1M_6
PR117 22_8
PR110 22_8
PR103 1M_6
S5D
30,31,35,40 S5_ON
PQ19 DTC144EU
PR113 1M_6
PQ20 DMN601K-7
PQ12 DMN601K-7
PQ11 DMN601K-7
PQ57 AO4468
+5V_S5
3A
+5V_S5
TDC : 1.88A
PEAK : 2.5A
Width : 80mil
MAIND
PQ58 AO4468
+5V
3.28A
+5V
TDC : 2.85A
PEAK : 3.8A
Width : 120mil
PQ50 AO4468
+3V
+3V
TDC : 2.52A
PEAK : 3.36A
Width : 100mil
PQ10 AO3404
+3V_S5
+3V_S5
TDC : 0.62A
PEAK : 0.84A
Width : 40mil
Quanta Computer Inc.
PROJECT : ZQG
Size
Document Number
SYSTEM 5V/3V (RT8206)
Rev 1A
Date: Monday, November 01, 2010
Sheet 33 of 41


Parallel
C-Test
OCP:12A
9A
OCP:11A
8A
Close to Phase Inductor
Close to Phase Inductor
OZ8380
PU6
CPU_VDD0_FB_H
CPU_VDD0_FB_L
CPU_VDDNB_FB_L
CPU_VDDNB_FB_H
CPU_SVD
CPU_SVC
CPU_PWRGD_SVID_REG
CPU_COREPG
VRON
+VCORE
+NBCORE
+5VPCU
+3V
+1.5V
VIN
8380VREF
8380TSET
8380ILIM
8380LX1
8380LX2
8380LDR1
8380LDR2
8380HDR1
8380HDR2
8380BST1
8380CSN1
8380CSP1
8380CSN2
8380CSP2
8380RSP1
8380RSN1
8380RSP2
8380RSN2
PR55 *Short_4
PR48 *Short_4
PR54 *Short_4
PR47 *Short_4
SNS_POS_VDD_0
SNS_NEG_VDD_0
SNS_POS_VDD_1
SNS_NEG_VDD_1
PR151 49.9/F_4
PR154 665/F_4
PR149 665/F_4
PR145 49.9/F_4
PR144 49.9/F_4
PR146 1.2K/F_4
PR148 1.2K/F_4
PR150 49.9/F_4
PC33 100p/50V_4
PC32 220p/50V_4
PR51 27.4K/F_4
PR50 32.4K/F_4
PR63 0_4
PR157 10K_4
PR53 *330/F_4
PR65 1K/F_4
PQ9 *AO3402
PR197 *0_4
PC119 1000p/50V_4
PR64 1.91K/F_4
PR158 27.4K/F_4
PC117 1000p/50V_4
PR153 *100K/F_4
PR142 0_6
PR140 0_6
PC109 1u/6.3V_4
PR45 22_6
PC108 470p/50V_4
PC110 0.22u/6.3V_4
PC111 470p/50V_4
PR141 0_4
PR44 2.55K/F_4
PR152 *49.9K/F_4
PR147 49.9K/F_4
PC112 0.1u/10V_4
PR41 43.2K/F_4
PR143 6.2K/F_4
PC106 1000p/50V_4
PR43 0_4
PR46 0_4
PC122 0.22u/25V_6
PD8 RB500V-40
PR68 2_6
PC39 1u/6.3V_4
PR67 2_6
PD9 RB500V-40
PC123 0.22u/25V_6
PC41 *2.2n/50V_4
PC44 *2.2n/50V_4
PQ32 AOL1448
PQ35 AOL1718
PQ34 AOL1448
PQ33 AOL1718
PR69 *2.2/F_6
PC43 *1000p/50V_6
PR159 *2.2/F_6
PC124 *1000p/50V_6
PC40 0.1u/50V_6
PC37 4.7u/25V_8
PC107 *4.7u/25V_8
PC118 100u/25V_6X5.8
PC38 0.1u/50V_6
PC36 4.7u/25V_8
PC120 100u/25V_6X5.8
PC113 100p/50V_4
PC115 6.8n/25V_4
PC34 0.1U/50V_6
PR61 2.2/F_4
PR59 5.62K/F_4
PR156 3.92K/F_4
PR172 10K_6_NTC
PL9 1uH
PC131 330u/2V_7343
PL8 1uH
PR155 3.92K/F_4
PR57 5.62K/F_4
PR166 10K_6_NTC
PR60 *4.99K/F_4
PR62 2.2/F_4
PC35 0.1u/10V_4
PC114 100p/50V_4
PC116 6.8n/25V_4
PC133 330u/2V_7343
Quanta Computer Inc.
PROJECT : ZQG
CPU Core (OZ8380)
Size
Document Number
Rev 1A
Date: Monday, November 01, 2010
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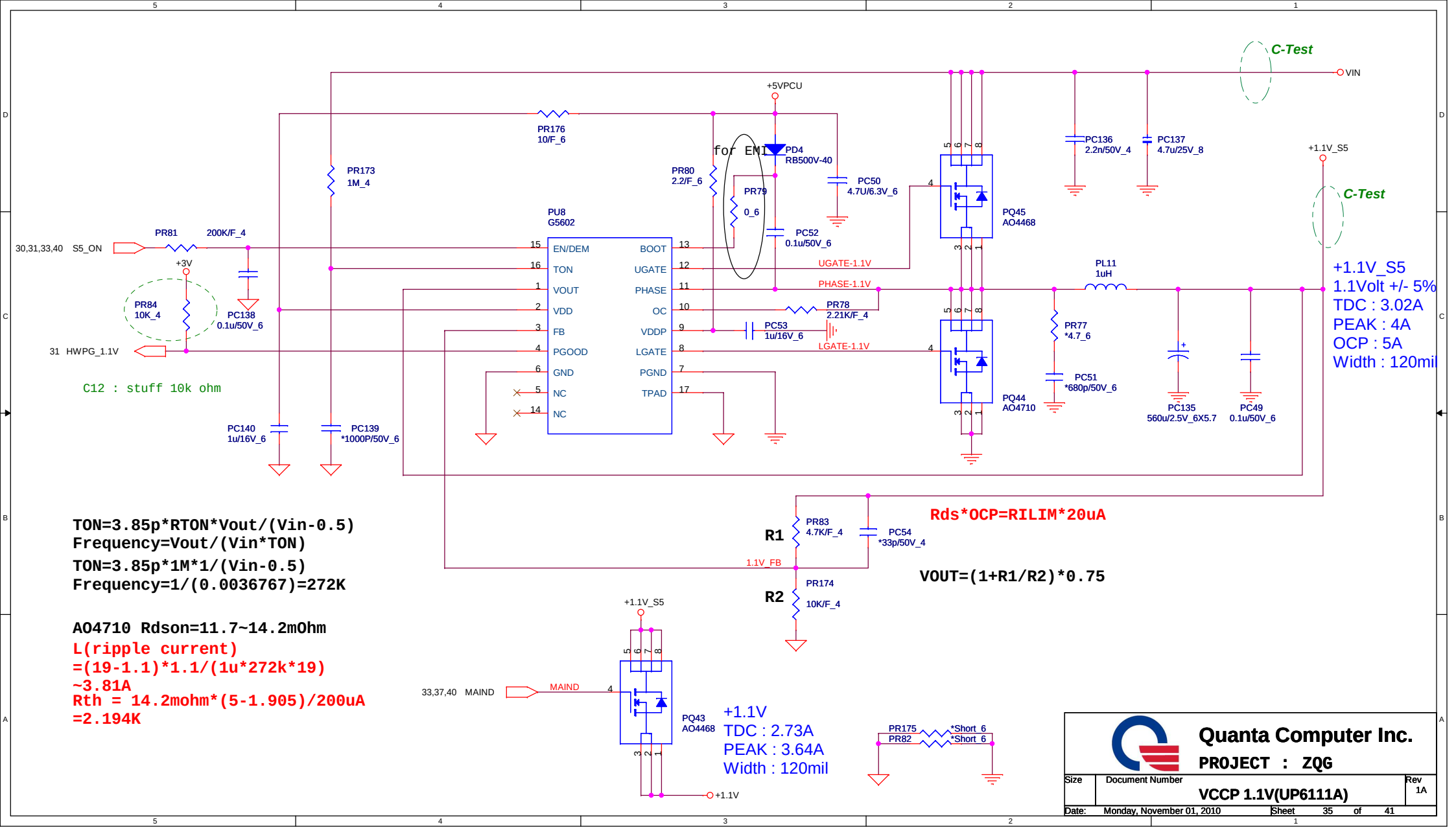
C-Test
VIN
+5VPCU
PR176
10/F_6
for EMI
PD4
RB500V-40
PR173
1M_4
PR80
2.2/F_6
PR79
0_6
PC50
4.7U/6.3V_6
PC52
0.1u/50V_6
PU8
G5602
EN/DEM
TON
VOUT
VDD
FB
PGOOD
GND
NC
NC
BOOT
UGATE
PHASE
OC
VDDP
LGATE
PGND
TPAD
UGATE-1.1V
PHASE-1.1V
LGATE-1.1V
PR78
2.21K/F_4
PC53
1u/16V_6
PQ45
AO4468
PQ44
AO4710
PC136
2.2n/50V_4
PC137
4.7u/25V_8
+1.1V_S5
C-Test
PL11
1uH
PR77
*4.7_6
PC51
*680p/50V_6
PC135
560u/2.5V_6X5.7
PC49
0.1u/50V_6
+1.1V_S5
1.1Volt +/- 5%
TDC : 3.02A
PEAK : 4A
OCP : 5A
Width : 120mil
PR81
200K/F_4
30,31,33,40 S5_ON
+3V
PR84
10K_4
PC138
0.1u/50V_6
31 HWPG_1.1V
C12 : stuff 10k ohm
PC140
1u/16V_6
PC139
*1000P/50V_6
TON=3.85p*RTON*Vout/(Vin-0.5)
Frequency=Vout/(Vin*TON)
TON=3.85p*1M*1/(Vin-0.5)
Frequency=1/(0.0036767)=272K
AO4710 Rdson=11.7~14.2mOhm
L(ripple current)
=(19-1.1)*1.1/(1u*272k*19)
~3.81A
Rth = 14.2mohm*(5-1.905)/200uA
=2.194K
R1
PR83
4.7K/F_4
PC54
*33p/50V_4
1.1V_FB
R2
PR174
10K/F_4
Rds*OCP=RILIM*20uA
VOUT=(1+R1/R2)*0.75
+1.1V_S5
33,37,40 MAIND
MAIND
PQ43
AO4468
+1.1V
TDC : 2.73A
PEAK : 3.64A
Width : 120mil
PR175
PR82
*Short_6
*Short_6
+1.1V
Quanta Computer Inc.
PROJECT : ZQG
Size
Document Number
VCCP 1.1V(UP6111A)
Rev
1A
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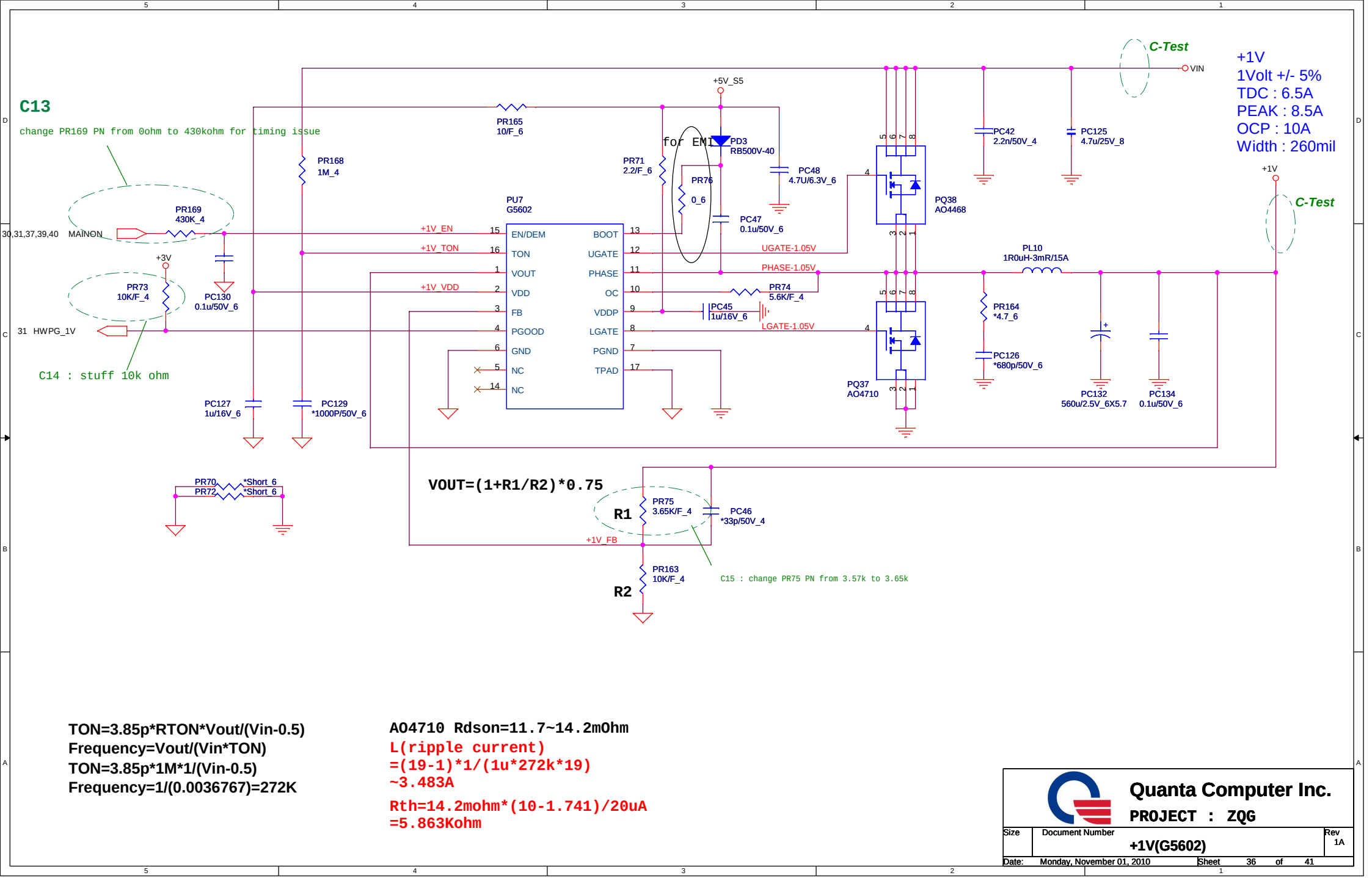

TON=3.85p*RTON*Vout/(Vin-0.5)
Frequency=Vout/(Vin*TON)
TON=3.85p*1M*1/(Vin-0.5)
Frequency=1/(0.0036767)=272K

AO4710 Rdson=11.7~14.2mOhm
L(ripple current)
=(19-1)*1/(1u*272k*19)
~3.483A

Rth=14.2mohm*(10-1.741)/20uA
=5.863Kohm

Quanta Computer Inc.
PROJECT : ZQG

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	+1V(G5602)	1A
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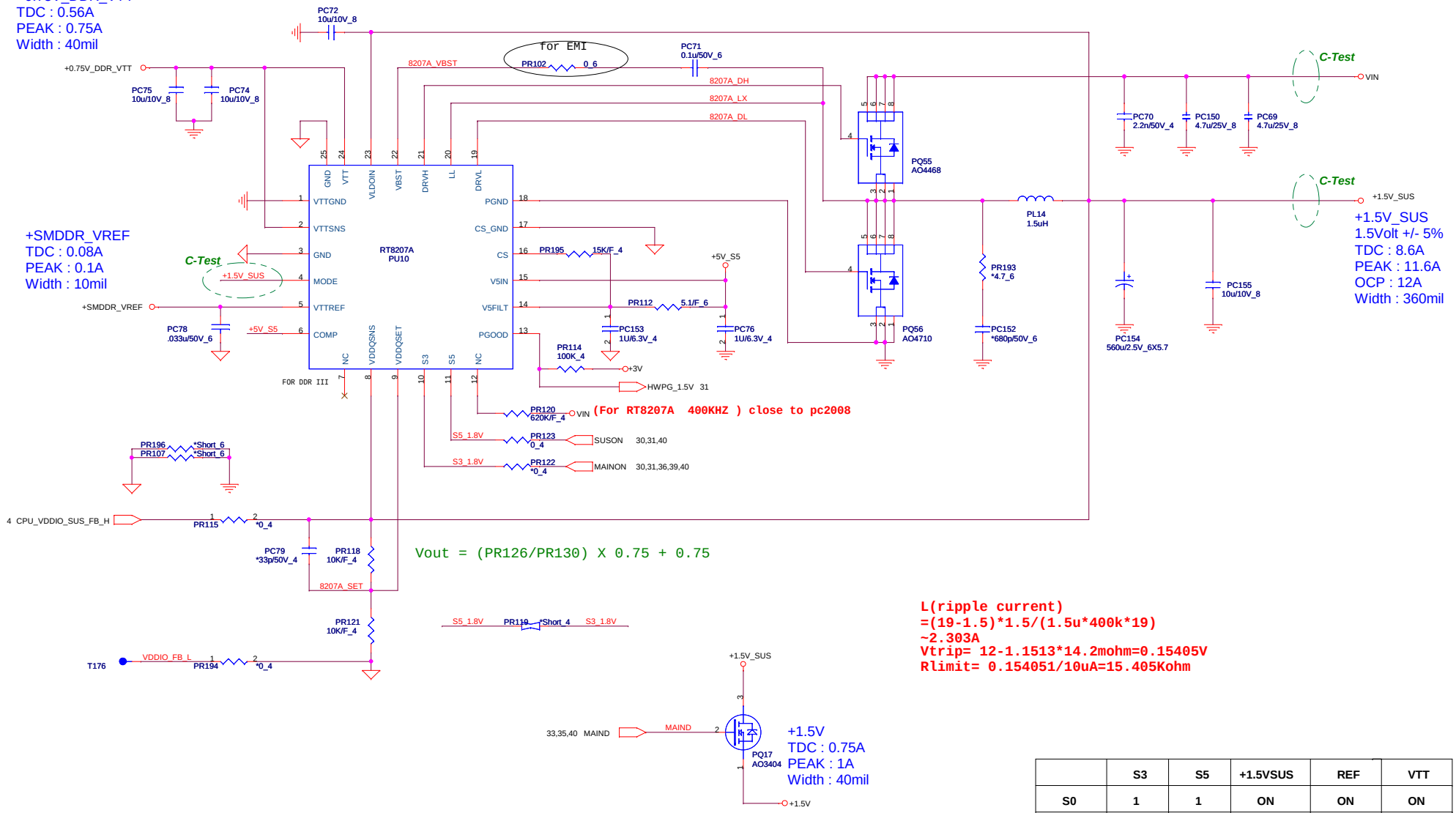
+0.75V_DDR_VTT
TDC : 0.56A
PEAK : 0.75A
Width : 40mil

+SMDDR_VREF
TDC : 0.08A
PEAK : 0.1A
Width : 10mil



Vout = (PR126/PR130) X 0.75 + 0.75

L(ripple current)
=(19-1.5)*1.5/(1.5u*400k*19)
~2.303A
Vtrip= 12-1.1513*14.2mohm=0.15405V
Rlimit= 0.154051/10uA=15.405Kohm

+1.5V_SUS
1.5Volt +/- 5%
TDC : 8.6A
PEAK : 11.6A
OCP : 12A
Width : 360mil

+1.5V
TDC : 0.75A
PEAK : 1A
Width : 40mil

	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

Quanta Computer Inc.
PROJECT : ZQ6
Size | Document Number: DDR 1.5V(TPS51116) | Rev 1A
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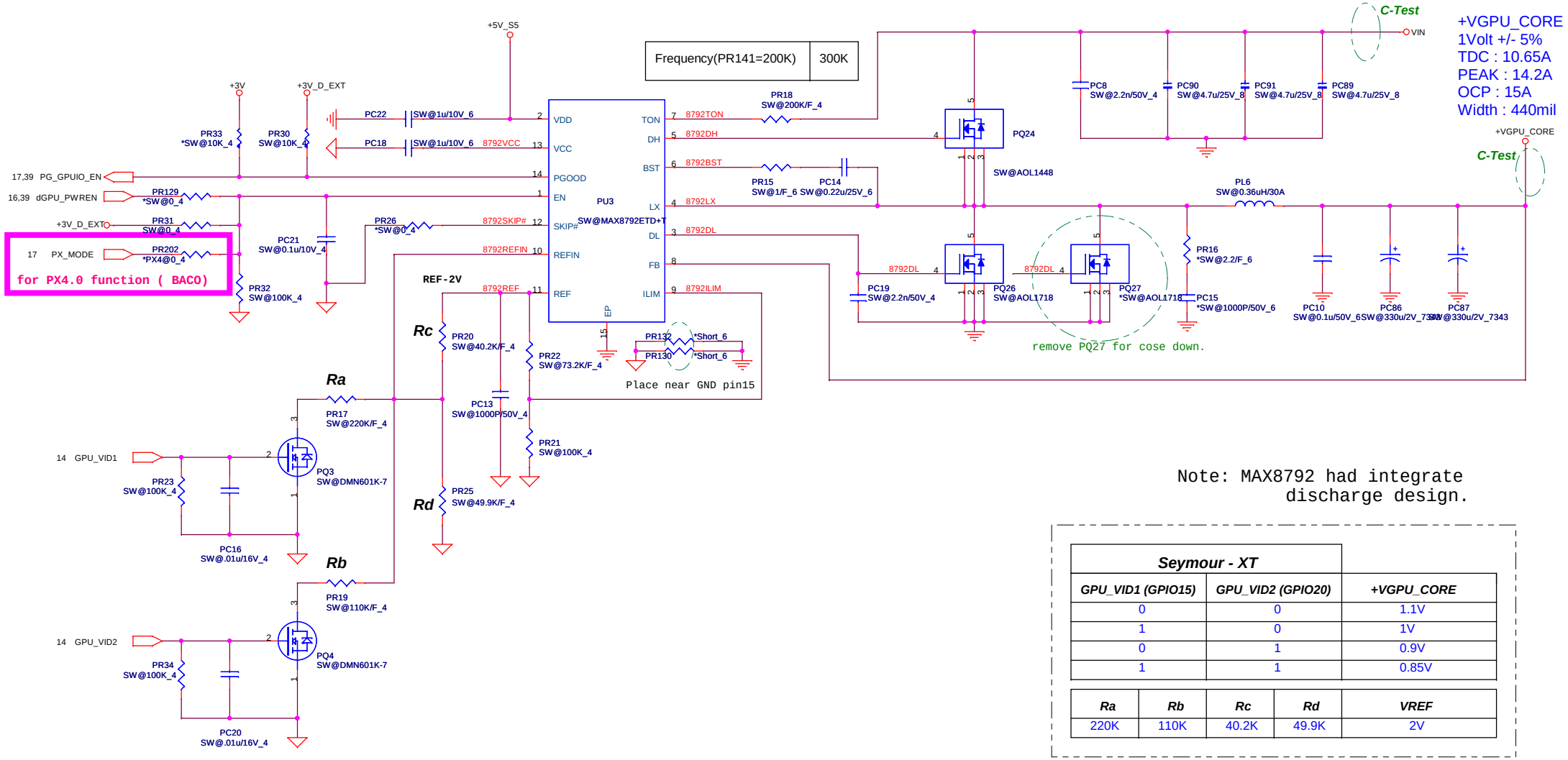

Note: MAX8792 had integrate discharge design.

Seymour - XT		
GPU_VID1 (GPIO15)	GPU_VID2 (GPIO20)	+VGPU_CORE
0	0	1.1V
1	0	1V
0	1	0.9V
1	1	0.85V

Ra	Rb	Rc	Rd	VREF
220K	110K	40.2K	49.9K	2V

Ra --> 220K/F_4 (CS42202FB01) *Rb --> 110K/F_4 (CS41102FB13)*
Rc --> 40.2K/F_4 (CS34022FB15) *Rd --> 49.9K/F_4 (CS34992FB10)*

Quanta Computer Inc.
PROJECT : ZQG

Size	Document Number	Rev
	GPU CORE(MAX8792)	1A
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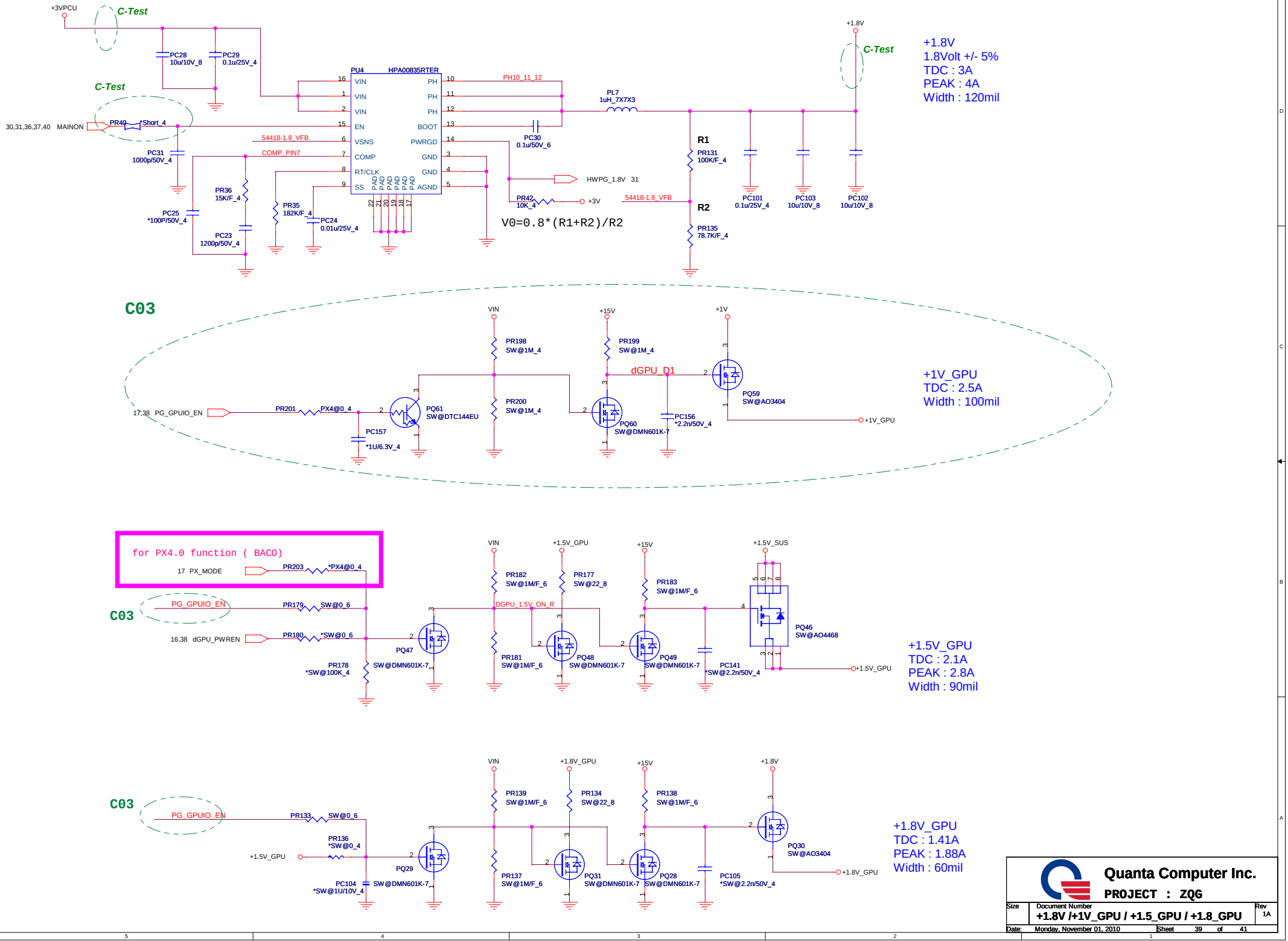
+3VPCU
C-Test
PC28 10u/10V_8
PC29 0.1u/25V_4
C-Test
30,31,36,37,40 MAINON
PR40 *Short_4
PC31 1000p/50V_4
PC25 *100P/50V_4
PR36 15K/F_4
PC23 1200p/50V_4
PR35 182K/F_4
PC24 0.01u/25V_4
54418-1.8_VFB
COMP_PIN7
PU4 HPA00835RTER
VIN
VSNS
COMP
RT/CLK
SS
EN
PH
BOOT
PWRGD
GND
AGND
PAD
PH10_11_12
PC30 0.1u/50V_6
PL7 1uH_7X7X3
HWPG_1.8V 31
PR42 10K_4
+3V
54418-1.8_VFB
V0=0.8*(R1+R2)/R2
R1
PR131 100K/F_4
R2
PR135 78.7K/F_4
+1.8V
C-Test
PC101 0.1u/25V_4
PC103 10u/10V_8
PC102 10u/10V_8
+1.8V
1.8Volt +/- 5%
TDC : 3A
PEAK : 4A
Width : 120mil
C03
VIN
+15V
+1V
PR198 SW@1M_4
PR199 SW@1M_4
dGPU_D1
PR200 SW@1M_4
17,38 PG_GPUIO_EN
PR201 PX4@0_4
PC157 *1U/6.3V_4
PQ61 SW@DTC144EU
PQ60 SW@DMN601K-7
PC156 *2.2n/50V_4
PQ59 SW@AO3404
+1V_GPU
+1V_GPU
TDC : 2.5A
Width : 100mil
for PX4.0 function (BACO)
17 PX_MODE
PR203 *PX4@0_4
C03
PG_GPUIO_EN
PR179 SW@0_6
16,38 dGPU_PWREN
PR180 *SW@0_6
PR178 *SW@100K_4
PQ47 SW@DMN601K-7
VIN
+1.5V_GPU
+15V
+1.5V_SUS
PR182 SW@1M/F_6
PR177 SW@22_8
DGPU_1.5V_ON_R
PR181 SW@1M/F_6
PQ48 SW@DMN601K-7
PR183 SW@1M/F_6
PQ49 SW@DMN601K-7
PC141 *SW@2.2n/50V_4
PQ46 SW@AO4468
+1.5V_GPU
+1.5V_GPU
TDC : 2.1A
PEAK : 2.8A
Width : 90mil
C03
PG_GPUIO_EN
PR133 SW@0_6
+1.5V_GPU
PR136 *SW@0_4
PC104 *SW@1U/10V_4
PQ29 SW@DMN601K-7
VIN
+1.8V_GPU
+15V
+1.8V
PR139 SW@1M/F_6
PR134 SW@22_8
PR137 SW@1M/F_6
PQ31 SW@DMN601K-7
PR138 SW@1M/F_6
PQ28 SW@DMN601K-7
PC105 *SW@2.2n/50V_4
PQ30 SW@AO3404
+1.8V_GPU
+1.8V_GPU
TDC : 1.41A
PEAK : 1.88A
Width : 60mil
Quanta Computer Inc.
PROJECT : ZQG
Size
Document Number
+1.8V /+1V_GPU / +1.5_GPU / +1.8_GPU
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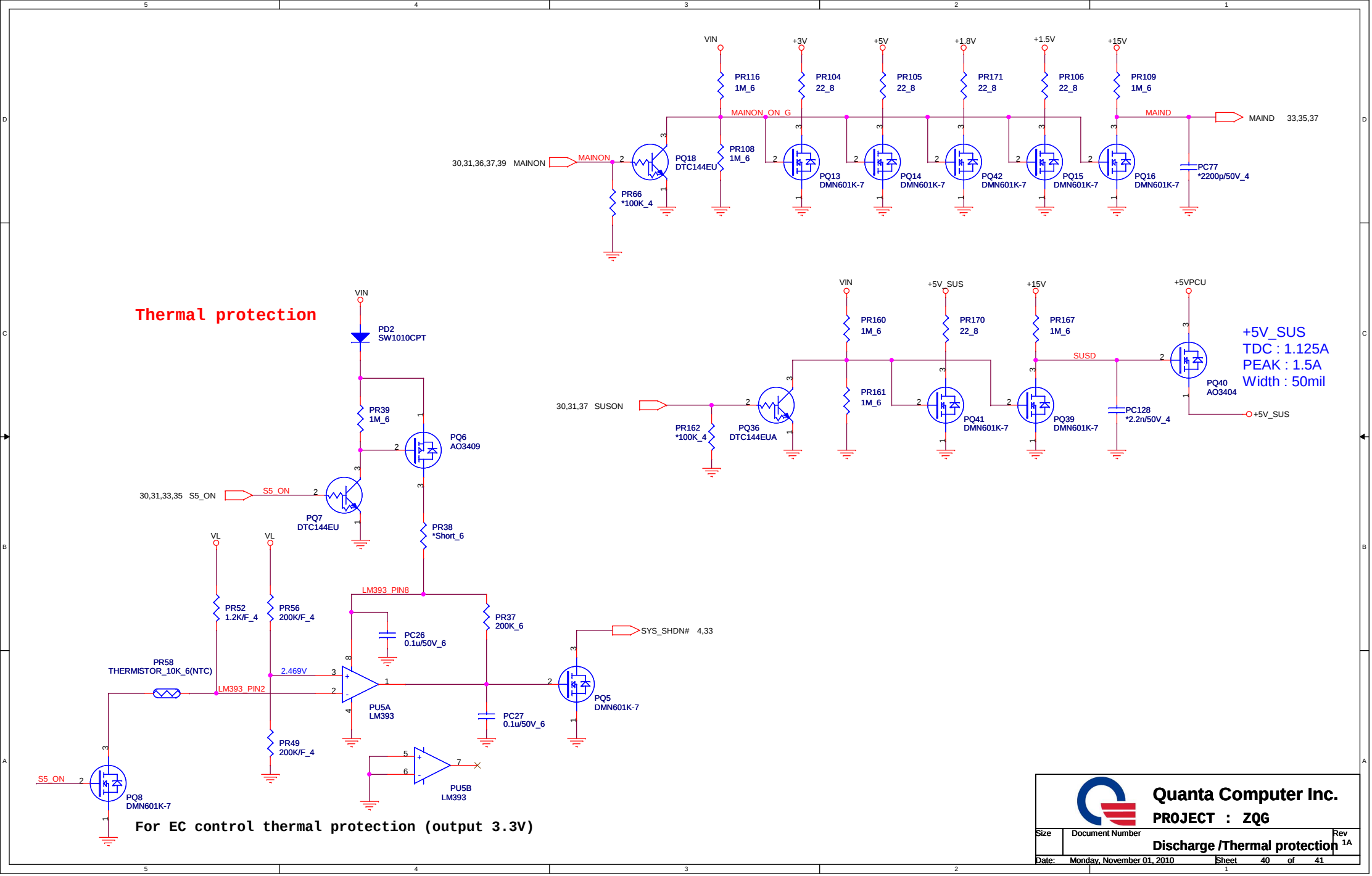
VIN
+3V
+5V
+1.8V
+1.5V
+15V
PR116 1M_6
PR104 22_8
PR105 22_8
PR171 22_8
PR106 22_8
PR109 1M_6
MAINON_ON_G
MAIND
MAIND 33,35,37
30,31,36,37,39 MAINON
MAINON
PQ18 DTC144EU
PR108 1M_6
PR66 *100K_4
PQ13 DMN601K-7
PQ14 DMN601K-7
PQ42 DMN601K-7
PQ15 DMN601K-7
PQ16 DMN601K-7
PC77 *2200p/50V_4
Thermal protection
VIN
PD2 SW1010CPT
PR39 1M_6
PQ6 AO3409
30,31,33,35 S5_ON
S5_ON
PQ7 DTC144EU
PR38 *Short_6
VL
VL
PR52 1.2K/F_4
PR56 200K/F_4
LM393_PIN8
PC26 0.1u/50V_6
PR37 200K_6
SYS_SHDN# 4,33
PR58 THERMISTOR_10K_6(NTC)
2.469V
LM393_PIN2
PU5A LM393
PC27 0.1u/50V_6
PQ5 DMN601K-7
PR49 200K/F_4
S5_ON
PQ8 DMN601K-7
PU5B LM393
For EC control thermal protection (output 3.3V)
VIN
+5V_SUS
+15V
+5VPCU
PR160 1M_6
PR170 22_8
PR167 1M_6
SUSD
PR161 1M_6
30,31,37 SUSON
PR162 *100K_4
PQ36 DTC144EUA
PQ41 DMN601K-7
PQ39 DMN601K-7
PC128 *2.2n/50V_4
PQ40 AO3404
+5V_SUS
+5V_SUS
TDC : 1.125A
PEAK : 1.5A
Width : 50mil
Quanta Computer Inc.
PROJECT : ZQG
Size
Document Number
Discharge /Thermal protection
Rev 1A
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MODEL	REV
ZQE/G M/B	3A

CHANGE LIST

C01

C02 PAGE18 : to slove the Power DVD issue , setting size to 256MB

C03 PAGE39 : add PR210,PC157,PQ61,PR198,PR200,PR199,PQ60,PC156,PQ69 for GPU +1V power source .
changed control net from HWPG_1V to PG_GPUIO_EN

C04 PAGE13 : change the power source from +1V to +1V_GPU

C05 PAGE14 : change the power source from +1V to +1V_GPU

C06 PAGE16 : change the power source from +1V to +1V_GPU

C07 PAGE17 : change the power source from +1V to +1V_GPU

C08 PAGE18 : to solve the HDMI issue , remove R112,R118 from BOMs

C09 PAGE21 : Del D26 to slove HDMI issue.

C10 PAGE26 : net PCBEEP connects with U11 by 10k ohm for AC pulg in /out function.

C11 PAGE31 : Both MXM_SMCLK12 / MXM_SMDATA12 should be pull up to +3V by 10k ohm.

C12 PAGE35 : stuff 10k ohm

C13 PAGE36 : change PR169 PN from 0 ohm to 430K ohm for timing issue.

C14 PAGE36 : stuff 10k ohm

C15 PAGE36 : change PR75 PN from 3.57k to 3.65k

C16 PAGE38 : remove PQ27 for cose down.

C17 PAGE38 : remove PQ27 for cose down.

C18 PAGE5 : Add C674 to reduce CRT noise.

C19 PAGE5 : del R100 , add L58 to reduce CRT noise.

Model	ZQE/G M/B BOARD	
Page	From	To
1	1A	3A
2	1A	3A
3	1A	3A
4	1A	3A
5	1A	3A
6	1A	3A
7	1A	3A
8	1A	3A
9	1A	3A
10	1A	3A
11	1A	3A
12	1A	3A
13	1A	3A
14	1A	3A
15	1A	3A
16	1A	3A
17	1A	3A
18	1A	3A
19	1A	3A
20	1A	3A
21	1A	3A
22	1A	3A
23	1A	3A
24	1A	3A
25	1A	3A
26	1A	3A
27	1A	3A
28	1A	3A
29	1A	3A
30	1A	3A
31	1A	3A
32	1A	3A
33	1A	3A
34	1A	3A
35	1A	3A
36	1A	3A
37	1A	3A
38	1A	3A
39	1A	3A
40	1A	3A
41	1A	3A

Note :
1. Remove Jumper : JP7,JP11,JP1,JP2,JP3,JP4,JP5,JP6,JP8,JP9,JP10,JP12,JP13,JP14,JP15,JP16,JP17,JP18

Quanta Computer Inc.
PROJECT : ZQG

Size	Document Number	Rev
	CHANGE LIST - 3A	1A

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Quanta Computer Inc. ZQE/G	PROJECT: ZQE/G	PCBA NO.	REV: 3A	DOC. NO :
	APPROVED BY : Johnny O	CHECK BY : Darren Liao	DRAWING BY : Kenneth Huang	DATE :10/18/2010 SHEET 1