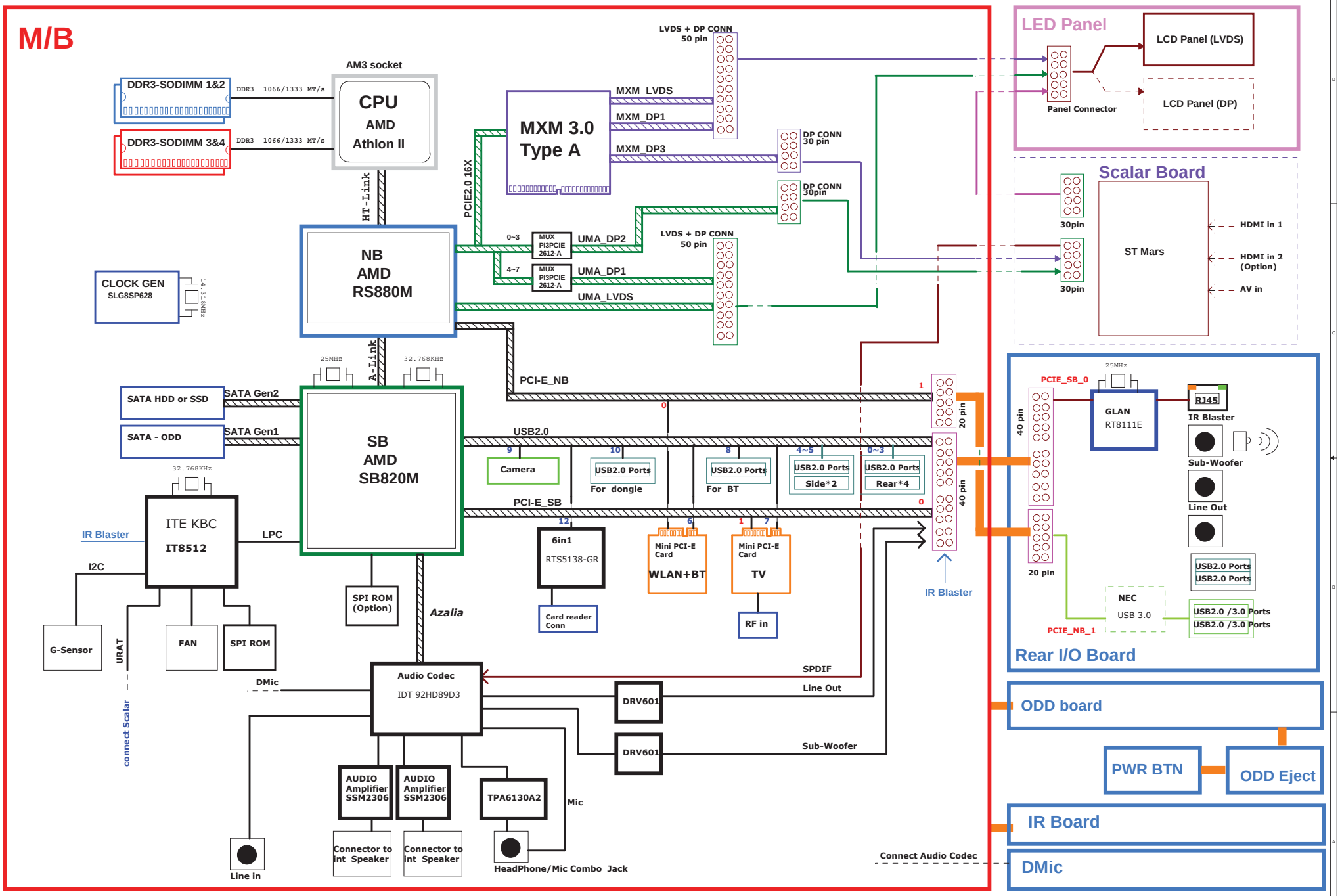
M3 System Block Diagram



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PROJECT : ZN8

Size	Document Number	Rev
	System Block Diagram	A

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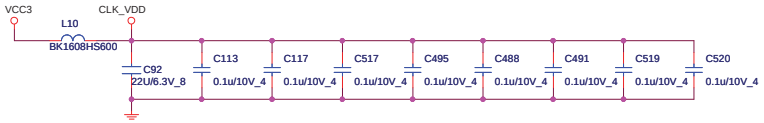
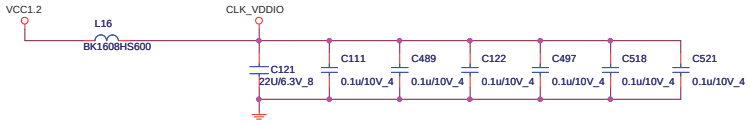
CLK_GEN_SLG8SP628





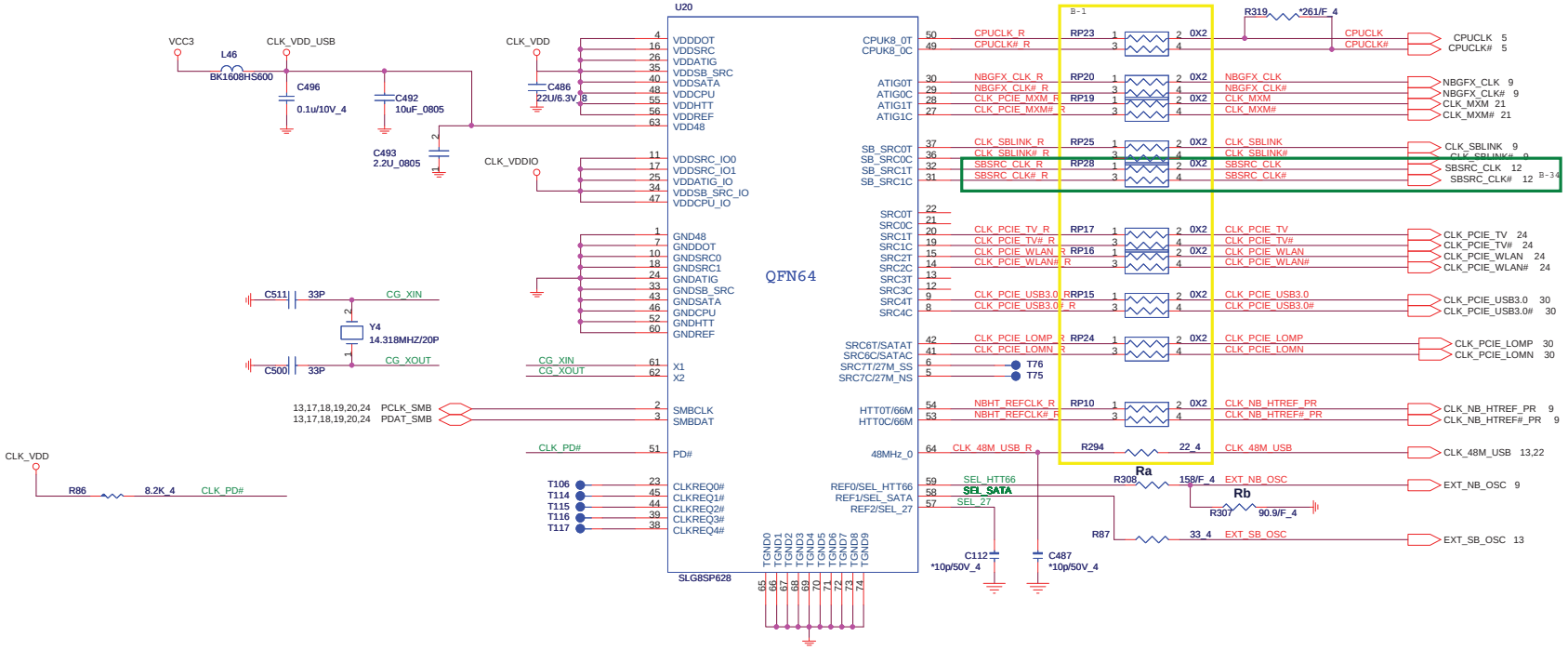
Clock chip has internal serial terminations for differencial pairs, external resistors are reserved for debug purpose.

Place within 0.5" of CLKGEN

ICS9LPRS480 P/N : ALPRS480000

SLG8SP628 P/N : AL8SP628000

RTM880N-796 P/N : AL000880000



To CPU	200 Mhz
To NB	RS880M for VGA
To NB	100 Mhz
To SB	
To LAN Controller	
To Mini PCIE Slot(TV)	
To Mini PCIE Slot(WLAN)	100 Mhz
To 6 in 1 Controller	
To USB 3.0	
To NB HT BUS	100 Mhz
To SB USB	48 Mhz
To NB	

SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1*	100 MHz non-spreading differential SRC clock
	0	100 MHz spreading differential SRC clock
SEL_27	1	27MHz and 27M SS outputs
	0*	100 MHz SRC clock

* default

CLOCK INPUT TABLE

CLOCKS	RS780
HT_REFCLKP	100M DIFF
HT_REFCLKN	100M DIFF
REFCLK_P	14M SE (1.1V)
REFCLK_N	vref
GFX_REFCLK	100M DIFF(IN/OUT)*
GPP_REFCLK	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF

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PROJECT : ZN8

Size	Document Number	Rev
	Clock Generator	1A

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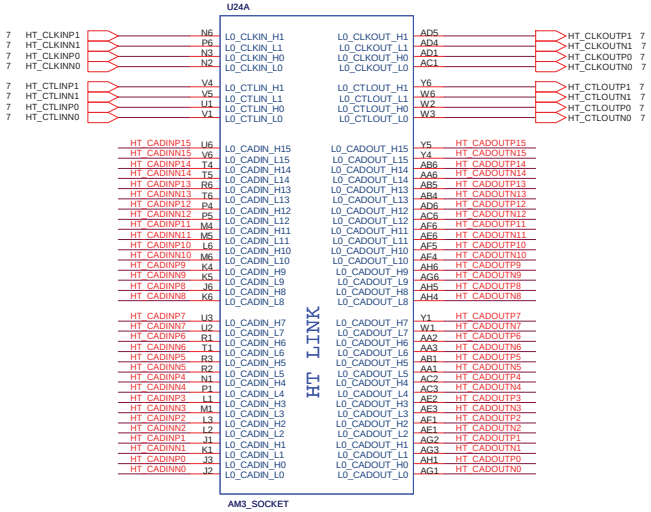
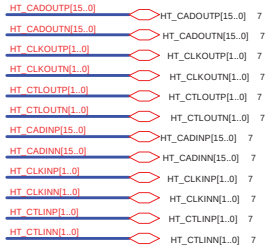
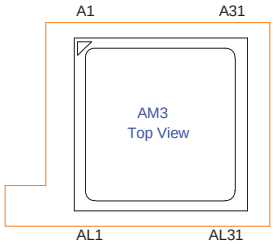
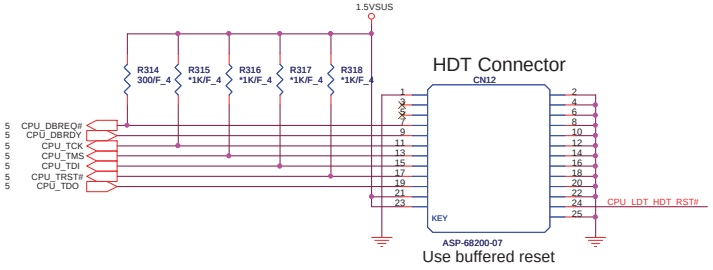
CPU HyperTransport and Debug



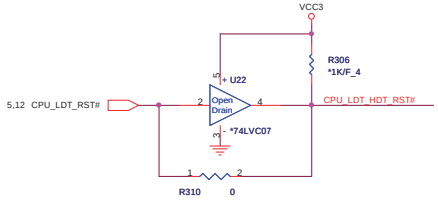






Use buffered reset

HDT Header



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PROJECT : ZN8		
Size	Document Number: CPU HyperTransport and Debug	Rev: 1A
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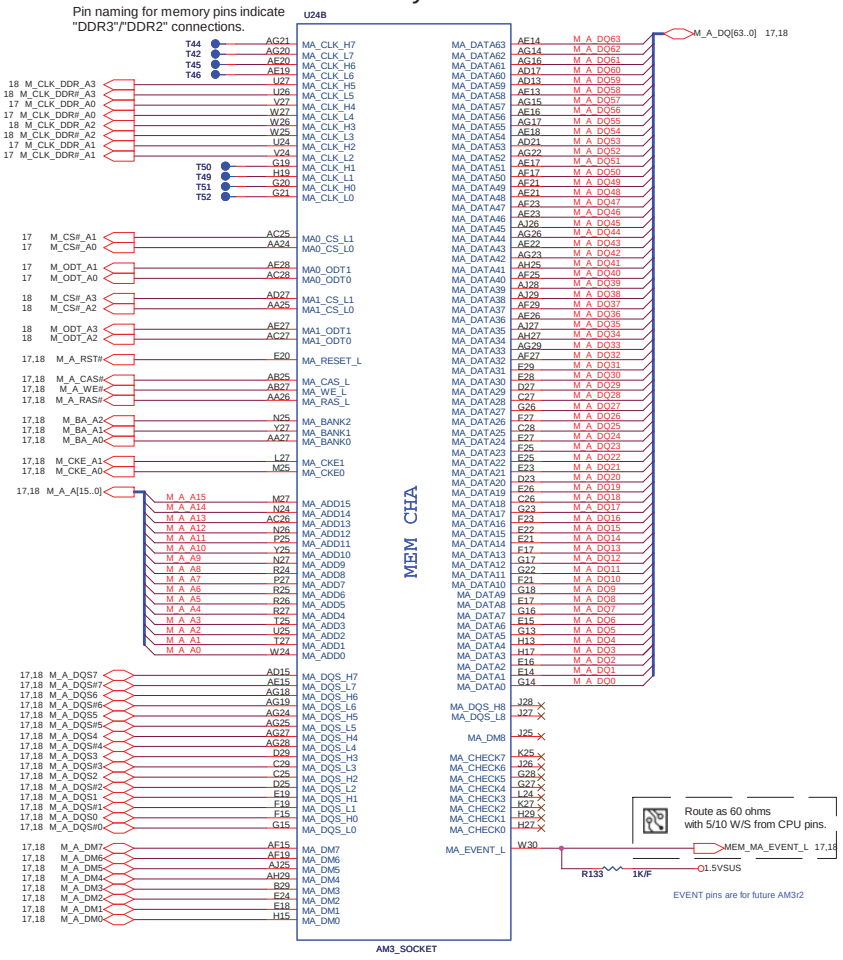
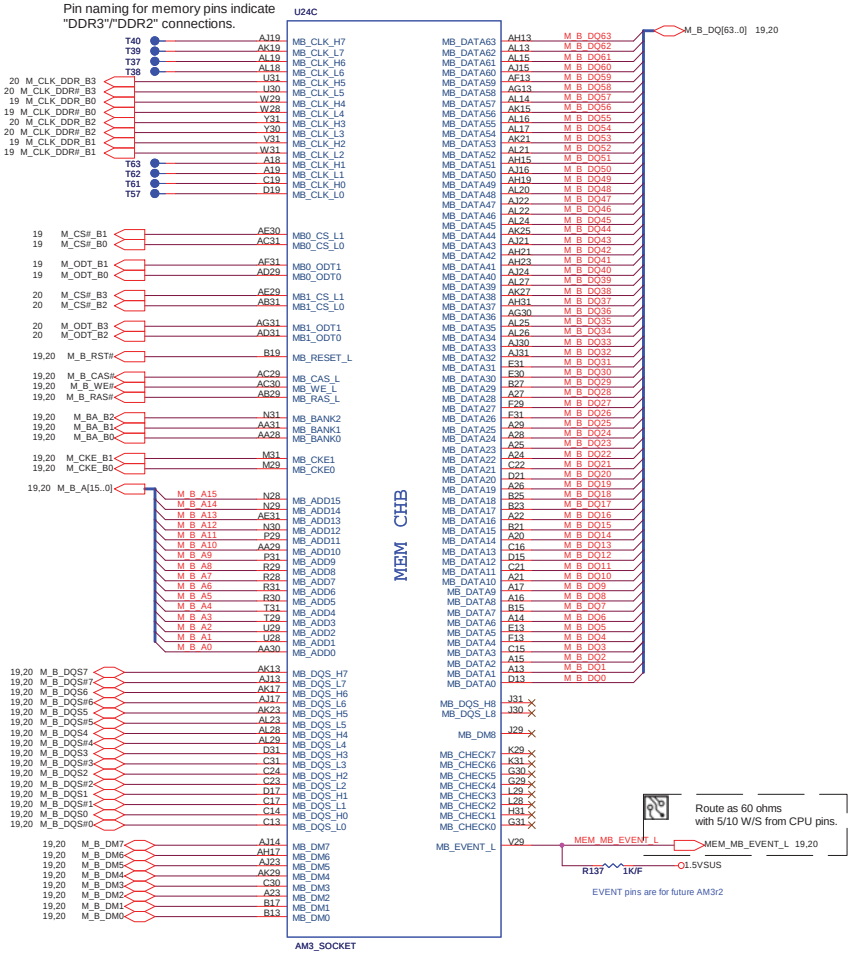
CPU Memory

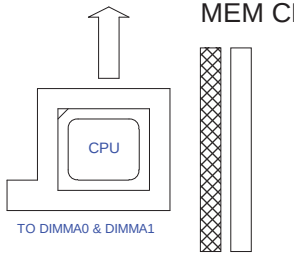
DDR3 Memory Interface A



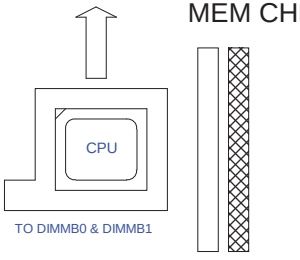
DDR3 Memory Interface B



MEM CHA



MEM CHB



Quanta Computer Inc.			
PROJECT : ZN8			
Size	Document Number: CPU Memory		Rev: 1A
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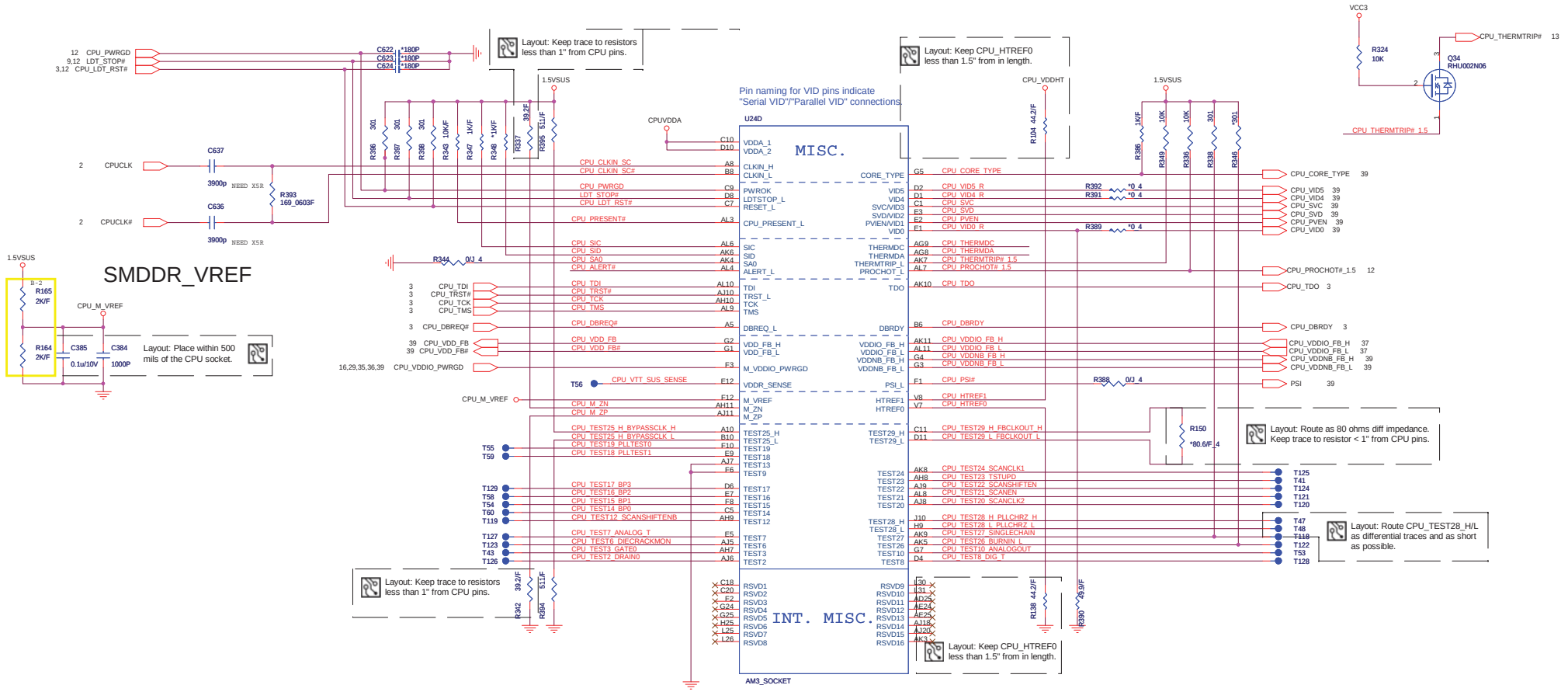
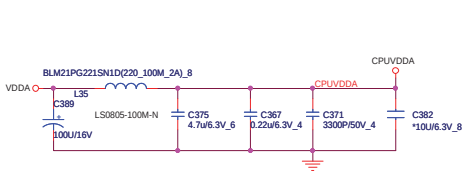
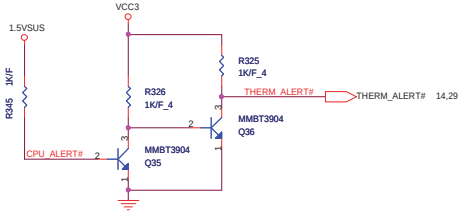
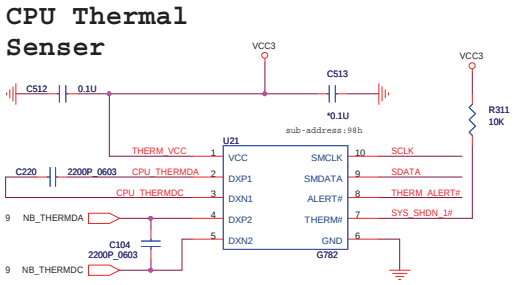
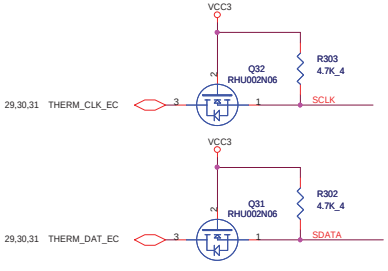
CPU Control and Miscellaneous

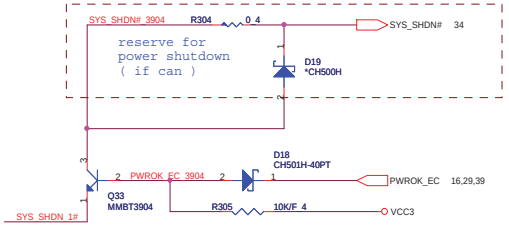












Quanta Computer Inc.			
PROJECT : ZN8			
Size	Document Number		Rev
	CPU Control & Misc		1A
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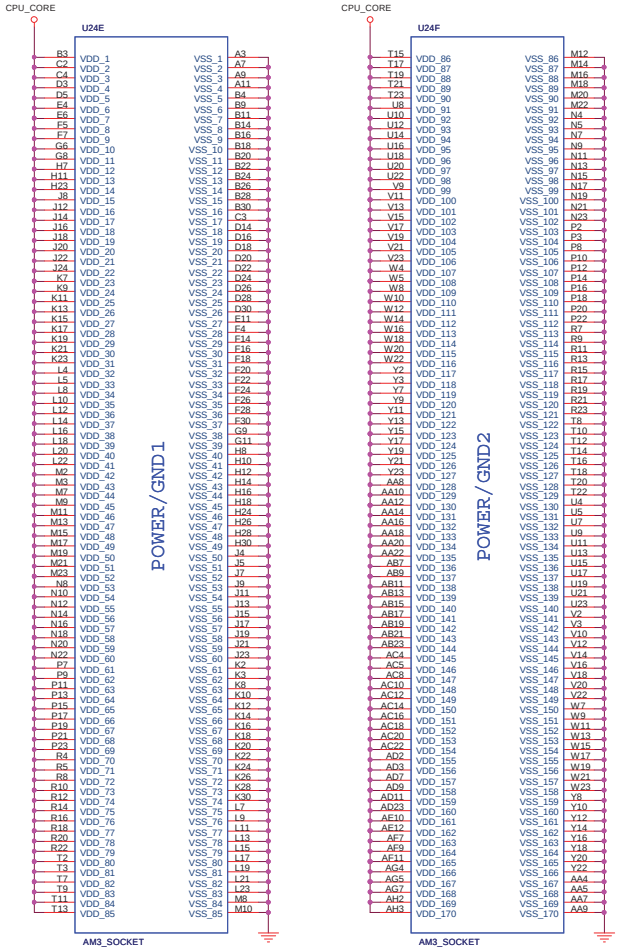
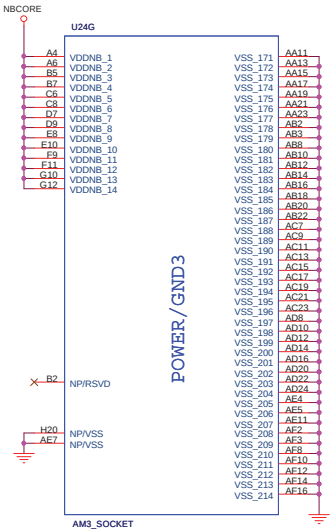
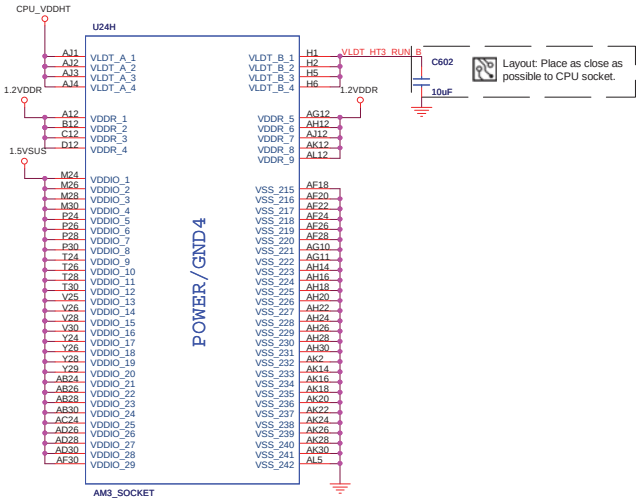
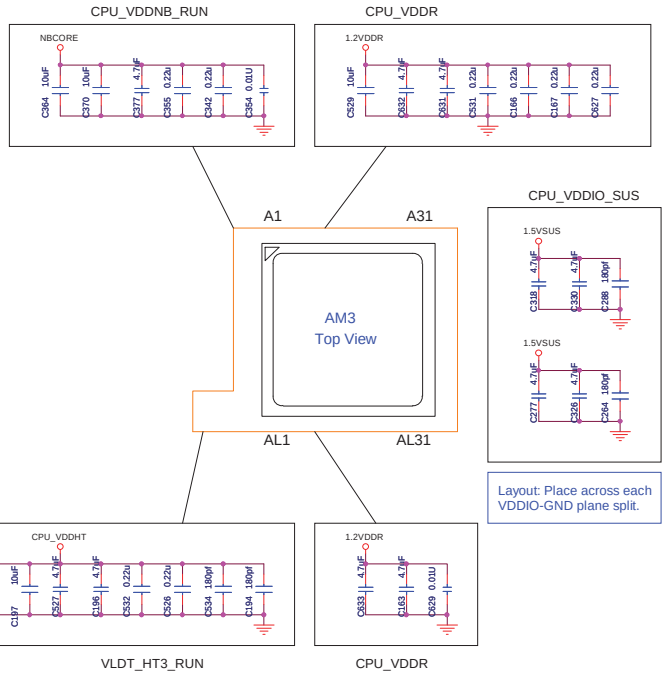
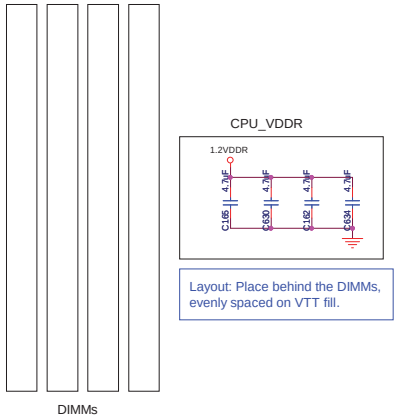
Processor Power and Ground



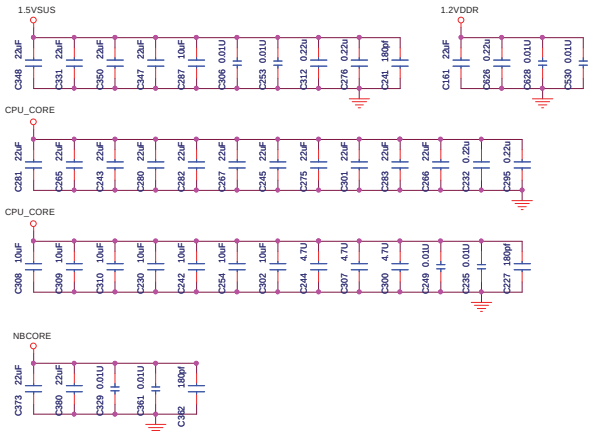








Bottom Side Decoupling



Quanta Computer Inc.			
PROJECT : ZN8			
Size	Document Number: CPU Power & GND		Rev: 1A
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signals	RS880M
HT_TXCALP	R430 301 ohm 1%
HT_TXCALN	
HT_RXCALP	R434 301 ohm 1%
HT_RXCALN	

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Size	Document Number	Rev
	RS880M-HT Link I/F	1A

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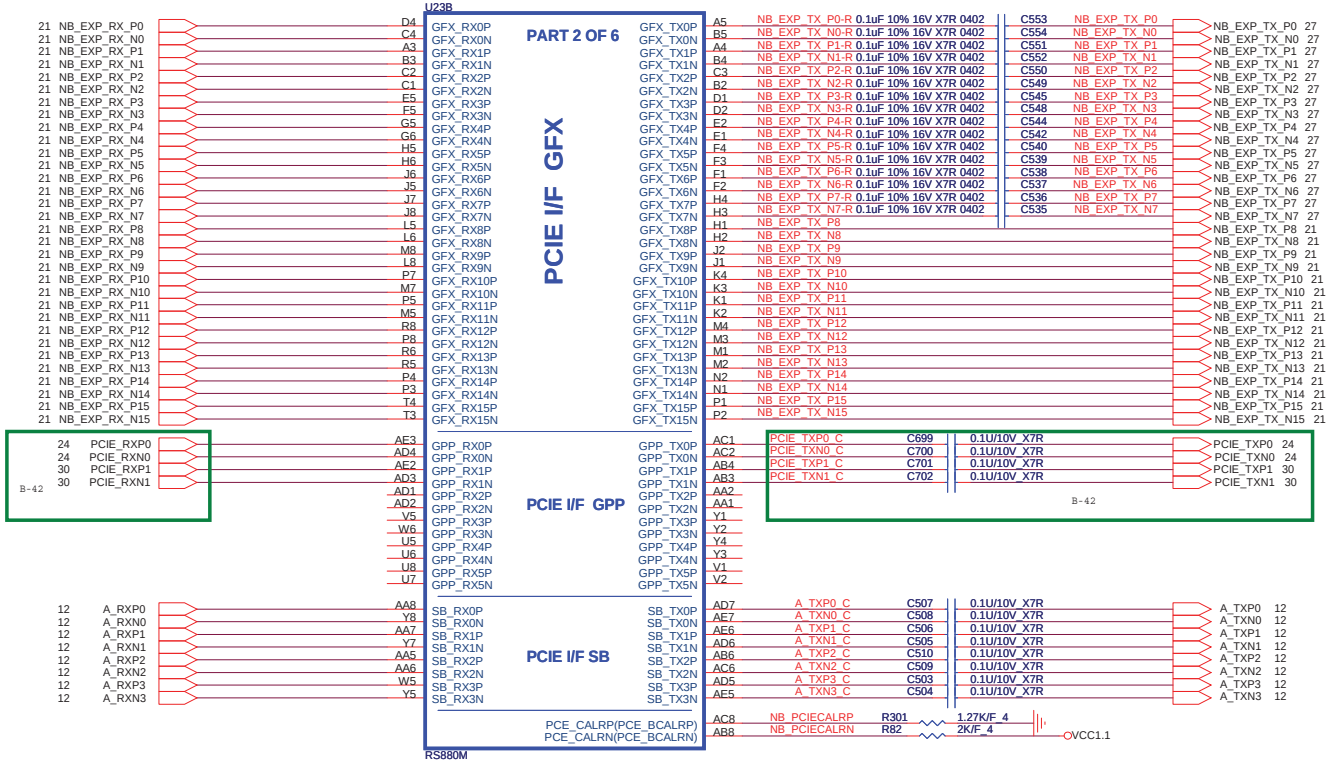

Quanta Computer Inc.	
PROJECT : ZN8	
Size	Document Number: RS880M-PCIE I/F
Rev	1A
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Enables Debug Bus acess
through memory I/O pads and GPIO.
0 : Enable RS880M , Default
1 : Disable RS880M
(RX881 use DAC_VSYNC)

INT_CRT_VSYNC_NB — R357 3K/J_4 — VCC3
R352 *3K/J_4

Indicates if memory Side port
is available or not
0: Reserved
1: Required setting. Select with a pull-up
resistor on the strap
(RX881 use DAC_HSYNC)

INT_CRT_HSYNC_NB — R356 3K/J_4 — VCC3

140ohm CS11402FB19

28 INT_CRT_RED — R364 *0/short_4 — INT_CRT_RED_R
28 INT_CRT_GREEN — R353 140/F_4 — R365 *0/short_4 — INT_CRT_GRE_R
28 INT_CRT_BLU — R354 150/F_4 — R366 *0/short_4 — INT_CRT_BLU_R
R355 150/F_4
10,28 INT_CRT_HSYNC — R361 *0/short_4 — INT_CRT_HSYNC_NB
10,28 INT_CRT_VSYNC — R362 *0/short_4 — INT_CRT_VSYNC_NB
28 INT_CRT_DDCDAT — R371 *0/short_4 — INT_CRT_DDCDAT_NB
28 INT_CRT_DDCCLK — R370 *0/short_4 — INT_CRT_DDCCLK_NB
R115 715/F_6 — DAC_RSET_NB

+3V_AVDD_NB
+1.8V_AVDDDI_NB
+1.8V_AVDDQ_NB
+1.1V_PLLVDD
+1.8V_PLLVDD18
+1.8V_VDDA18HTPLL
+1.8V_VDDA18PCIEPLL

20mA
120mA

B-66
12 A_RST#_SB
16 NB_PWRGD
R111 0_2
NB_RST#_IN
NB_PWRGD
NB_LDT_STOP#
NB_ALLOW_LDTSTOP

2 CLK_NB_HTREF_PR
2 CLK_NB_HTREF#_PR
2 EXT_NB_OSC — RP27 4 3 0_4P2R_4 2 1 B-3 — NB_REFCLK_N — R313 *4.7K
2 NBGFX_CLK — R309 *4.7K
2 NBGFX_CLK#
B-36

VCC1.1 — B-35 — R373 150/F_4 — R375 150/F_4
for EXT Gen.

For A11 version
R335 *49.9/F_4 — CLK_SBLINK
R333 *49.9/F_4 — CLK_SBLINK#

2 CLK_SBLINK
2 CLK_SBLINK#

B-4 21,26 LCD_CLK
21,26 LCD_DAT

26 DP_AUX0P
26 DP_AUX0N
26 DP_AUX1P
26 DP_AUX1N

VCC3 — R360 4.7K/J_4 — R359 4.7K/J_4 — EDID_CLK — EDID_DATA

R374 *2K/F — VCC3 — STRP_DATA
R372 *2K/F

STRP_DATA
T36
R358 150R — RS880_AUX_CAL

U23C

AVDD1(NC)	F12		
AVDD2(NC)	E12		
AVDDDI(NC)	F14		
AVSSDI(NC)	G15		
AVDDQ(NC)	H15		
AVSSQ(NC)	H14		
C_Pr(DFT_GPIO5)	E17		
Y(DFT_GPIO2)	F17		
COMP_Pb(DFT_GPIO4)	F15		
RED(DFT_GPIO0)	G18		
REDb(NC)	G17		
GREEN(DFT_GPIO1)	E18		
GREENb(NC)	F18		
BLUE(DFT_GPIO3)	E19		
BLUEb(NC)	F19		
DAC_HSYNC(PWM_GPIO4)	A11	CRT/TVOUT	
DAC_VSYNC(PWM_GPIO6)	B11		
DAC_SCL(PCE_RCALRN)	F8		
DAC_SDA(PCE_TCALRN)	E8		
DAC_RSET(PWM_GPIO1)	G14		
PLLVDD(NC)	A12		
PLLVDD18(NC)	D14	PLL PWR	
PLLVSS(NC)	B12		
VDDA18HTPLL	H17		
VDDA18PCIEPLL1	D7		
VDDA18PCIEPLL2	E7		
SYSRESETb	D8	PM	LVTM
POWERGOOD	A10		
LDTSTOPb	C10		
ALLOW_LDTSTOP	C12		
HT_REFCLKP	C25	CLOCKs	
HT_REFCLKN	C24		
REFCLK_P/OSCIN(OSCIN)	E11		
REFCLK_N(PWM_GPIO3)	F11		
GFX_REFCLKP	T2		
GFX_REFCLKN	T1		
GPP_REFCLKP	U1		
GPP_REFCLKN	U2		
GPPSB_REFCLKP(SB_REFCLKP)	V4		
GPPSB_REFCLKN(SB_REFCLKN)	V3		
I2C_CLK	B9	MIS.	
I2C_DATA	A9		
DDC_CLK0/AUX0P(NC)	A8		
DDC_DATA0/AUX0N(NC)	B8		
DDC_CLK1/AUX1P(NC)	B7		
DDC_DATA1/AUX1N(NC)	A7		
STRP_DATA	B10		
RSVD	G11		
AUX_CAL(NC)	C8		

PART 3 OF 6

TXOUT_L0P(NC)	A22	LVDS_TX_L0P	26
TXOUT_L0N(NC)	B22	LVDS_TX_L0N	26
TXOUT_L1P(NC)	A21	LVDS_TX_L1P	26
TXOUT_L1N(NC)	B21	LVDS_TX_L1N	26
TXOUT_L2P(NC)	B20	LVDS_TX_L2P	26
TXOUT_L2N(DBG_GPIO0)	A20	LVDS_TX_L2N	26
TXOUT_L3P(NC)	A19	LVDS_TX_L3P	26
TXOUT_L3N(DBG_GPIO2)	B19	LVDS_TX_L3N	26
TXOUT_U0P(NC)	B18	LVDS_TX_U0P	26
TXOUT_U0N(NC)	A18	LVDS_TX_U0N	26
TXOUT_U1P(PCIE_RESET_GPIO3)	A17	LVDS_TX_U1P	26
TXOUT_U1N(PCIE_RESET_GPIO2)	B17	LVDS_TX_U1N	26
TXOUT_U2P(NC)	D20	LVDS_TX_U2P	26
TXOUT_U2N(NC)	D21	LVDS_TX_U2N	26
TXOUT_U3P(PCIE_RESET_GPIO5)	D18	LVDS_TX_U3P	26
TXOUT_U3N(NC)	D19	LVDS_TX_U3N	26
TXCLK_LP(DBG_GPIO1)	B16	LVDS_TXCLK_LP	26
TXCLK_LN(DBG_GPIO3)	A16	LVDS_TXCLK_LN	26
TXCLK_UP(PCIE_RESET_GPIO4)	D16	LVDS_TXCLK_UP	26
TXCLK_UN(PCIE_RESET_GPIO1)	D17	LVDS_TXCLK_UN	26
VDDLTP18(NC)	A13	+1.8V_VDDLTP18_NB	
VSSLTP18(NC)	B13		
VDDLT18_1(NC)	A15	+1.8V_VDDLT_18_NB	
VDDLT18_2(NC)	B15		
VDDLT33_1(NC)	A14		
VDDLT33_2(NC)	B14		
VSSLT1(VSS)	C14		
VSSLT2(VSS)	D15		
VSSLT3(VSS)	C16		
VSSLT4(VSS)	C18		
VSSLT5(VSS)	C20		
VSSLT6(VSS)	E20		
VSSLT7(VSS)	C22		
LVDS_DIGON(PCE_TCALRP)	E9	R107 *0/short_4	INT_LVDS_PWREN 27
LVDS_BLON(PCE_RCALRP)	F7	R112 *0/short_4	INT_LVDS_BRIGHT 27
LVDS_ENA_BL(PWM_GPIO2)	G12	R113 *0/short_4	INT_LVDS_BLON 27
		R108 4.7K — R106 4.7K — R109 4.7K	
TMDS_HPD(NC)	D9	DP2_HPD	26
HPD(NC)	D10	DP_HPD	26
SUS_STAT#(PWM_GPIO5)	D12	R127 *0/short_4	SUS_STAT# 13
			SUS_STAT#_R 10
THERMALDIODE_P	AE8	NB_THERMDA	NB_THERMDA 5
THERMALDIODE_N	AD8	NB_THERMDC	NB_THERMDC 5
TESTMODE	D13	TEST_EN — R122 1.8K/F_4	

RS880M

VCC1.8 — VDDA18PCIEPLL -PCIE PLL
L27 BLM18PG221SN1D _6 — 20mils width — +1.8V_VDDA18PCIEPLL
C198 2.2U/6.3V_6

VDDA18HTPLL -HT LINK PLL
L17 BLM18PG221SN1D _6 — 20mils width — +1.8V_VDDA18HTPLL
C193 2.2U/6.3V_6

RS880M DEBUG PIN MAPPING

DEBUG_OUT0	LVDS_DIGON
DEBUG_OUT1	LVDS_ENA_BL
DEBUG_OUT2	LVDS_BLON
DEBUG_OUT3	TMDS_HPD
DEBUG_OUT4	AUX1N
DEBUG_OUT5	AUX1P
DEBUG_OUT6	HPD
DEBUG_OUT7	AUX_CAL

DDR3 based CPU : Level shifted to 1.8 V on the
Northbridge side using an open-drain buffer and
pulled up to 1.8V_S0 through a 2.2k Ohm 5% resistor
on the Northbridge side.

VCC1.8 — R119 1K/F_4 — NB_LDT_STOP#
VCC1.8 — U8 Open Drain — 74LVC07
5,12 LDT_STOP#

12 ALLOW_LDTSTOP — R120 *0/short_4 — NB_ALLOW_LDTSTOP
R121 1K/F_4 — VCC1.8

ALLOW_LDTSTOP	OC
LDT_STOP#	3.3V Input

* Although defined as 3.3V I/Os, a 1.8V signaling level is supported on LDT_STOP#/ALLOW_LDTSTOP given that Vih is 1.4V.
3.3V to 1.8V level translation is not required.

VCC3 — L33 BLM18PG181SN1D(180,1.5A)_6 — +3V_AVDD_NB
AVDD-DAC Analog
C238 2.2U/6.3V_6

VCC1.1 — BLM18PG181SN1D(180,1.5A)_6 — L28 — +1.1V_PLLVDD
PLLVDD - Graphics PLL
C222 2.2U/6.3V_6

VCC1.8 — BLM18PG181SN1D(180,1.5A)_6 — L32 — +1.8V_VDDLTP18_NB
VDDLTP18 - LVDS or DVI/HDMI PLL
C234 2.2U/6.3V_6

BLM21PG221SN1D(220,100M,2A)_8 — L31 — +1.8V_VDDLT_18_NB
C202 4.7U/6.3V_6 — C221 2.2U/6.3V_6 — C200 0.1U/10V_4
VDDLT18 - LVDS or DVI/HDMI digital

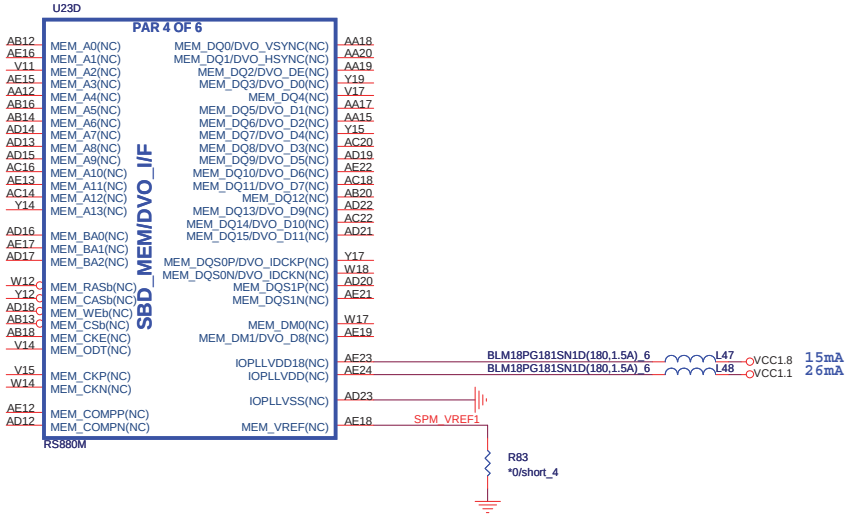
VCC1.8 — PLLVDD18 - Graphics PLL
L29 BLM18PG181SN1D(180,1.5A)_6 — +1.8V_PLLVDD18
C233 10U/6.3V_8 — C203 0.1U/10V_4

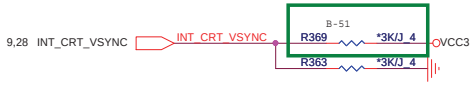
VCC1.8 — R117 0/J_6 — +1.8V_AVDDDI_NB
AVDDI-DAC Digital
C223 0.1U/10V_4

BLM18PG181SN1D(180,1.5A)_6 — L30 — +1.8V_AVDDQ_NB
AVDDQ-DAC Bandgap Reference
C224 0.1U/10V_4

Quanta Computer Inc.
PROJECT : ZN8

Size	Document Number	Rev
	RS880M-System I/F	1A
Date: Monday, March 22, 2010	Sheet 9 of 40	

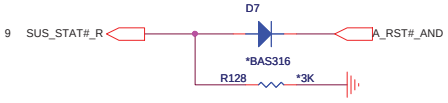




STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.

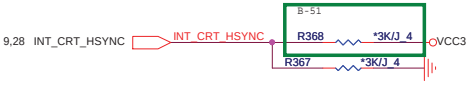
RS880M	
1 Disable	
0 Enable	



DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected



RS880M: Enables Side port memory

RS880M:HSYNC#

Selects if Memory SIDE PORT is available or not
1 = Memory Side port Not available
0 = Memory Side port available
Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]

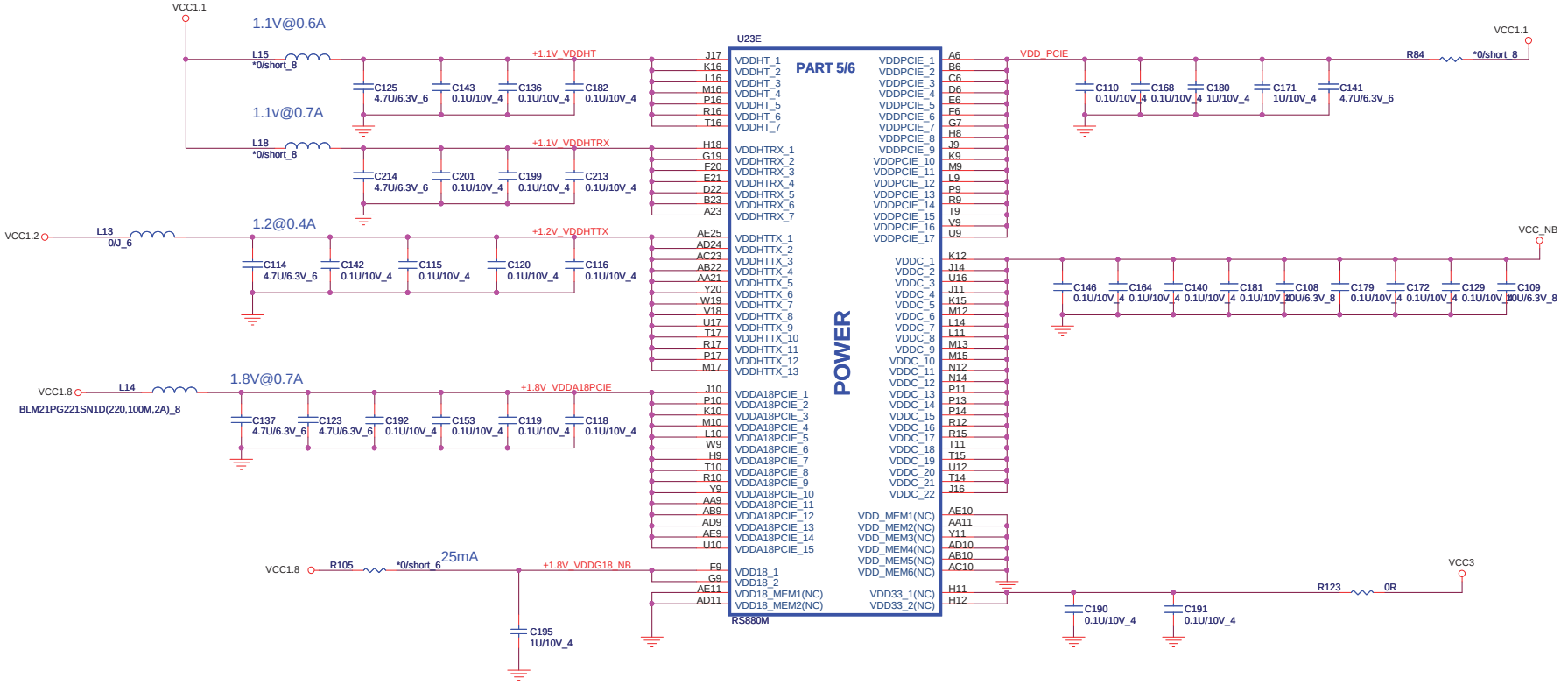
Quanta Computer Inc.
PROJECT : ZN8

Size	Document Number	Rev
	RS880M-Spmem/Straps	1A

Date: Monday, March 22, 2010 Sheet 10 of 40

RS880M POWER TABLE

PIN NAME	RS880M	PIN NAME	RS880M
VDDHT	+1.1V	IOPLLVDD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVDD	+1.1V
VDD18_MEM	+1.8V	PLLVDD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDLT18	+1.8V
IOPLLVDD18	+1.8V	VDDLT33	NC

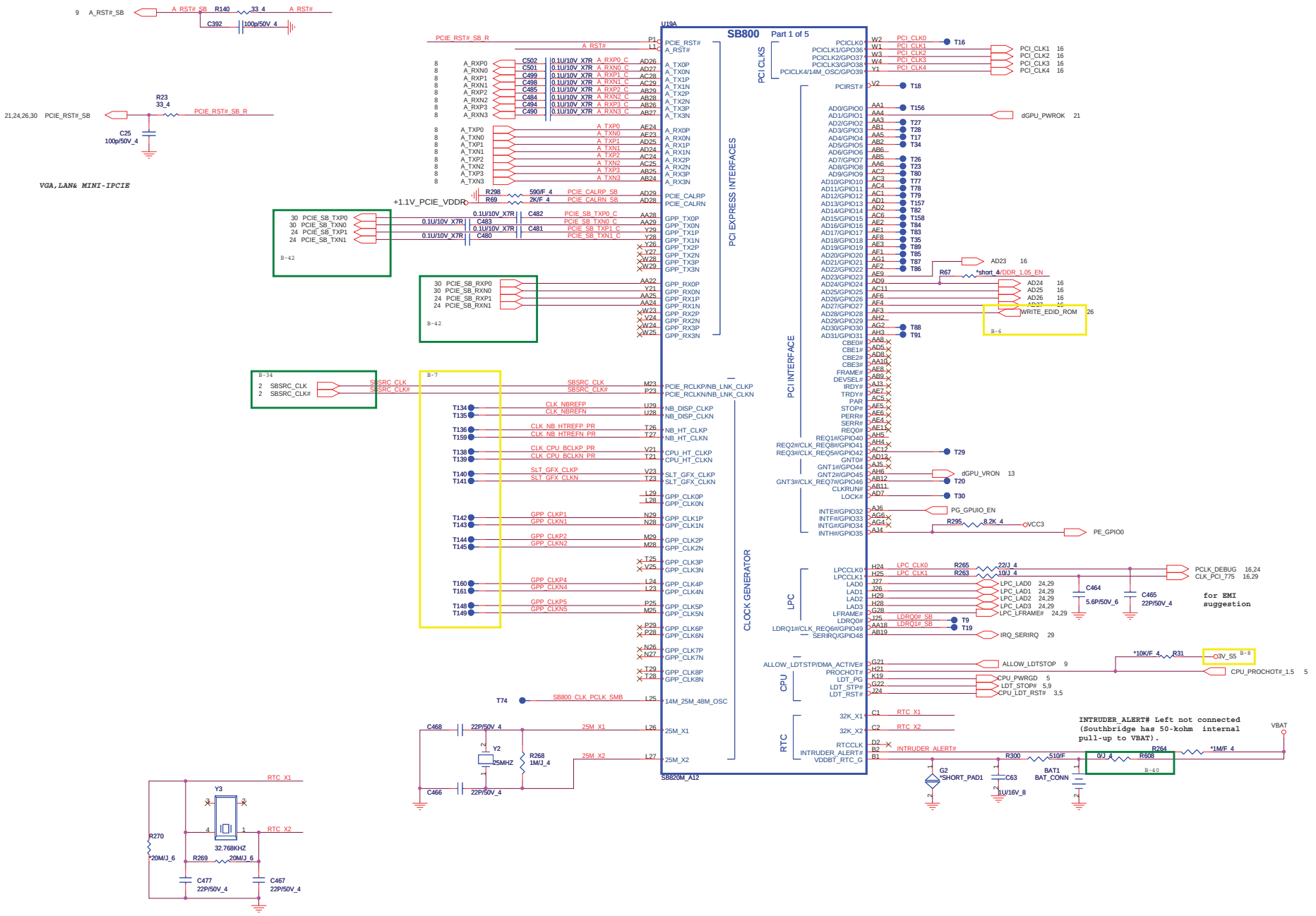


Quanta Computer Inc.

PROJECT : ZN8

Size	Document Number	Rev
	RS880M-Power	1A

Date: Monday, March 22, 2010 Sheet 11 of 40



Quanta Computer Inc.
PROJECT : ZN8

Size	Document Number	Rev
	SB820-PCIE/PCI/CPU/LPC 1/4	1A

Date: Monday, March 22, 2010 Sheet 12 of 40

NC only ,Can't be install

3V_S5 R41 *2.2K/J_4 SB_TEST0
R37 *2.2K/J_4 SB_TEST1
B-8 R51 *2.2K/J_4 SB_TEST2

3V_S5 B-48 R609 *2.2K/J_4 PCIE_WAKE#

VCC3 SCL0/SDATA0 is 3V tolerance AMD datasheet define it
R73 2.2K/J_4 PCLK_SMB
R74 2.2K/J_4 PDAT_SMB
Clock gen/Robson/TV tuner /DDR2/DDR2 thermal/Accelerometer

3V_S5 SCL1/SDATA1 is 3V/S5 tolerance AMD datasheet define it
B-8 R36 2.2K/J_4 SB_SMBCLK1
R47 2.2K/J_4 SB_SMBDATA1

3V_S5 SCL2/SDATA2 is 3V/S5 tolerance AMD datasheet define it
B-8 R33 2.2K/J_4 SB_SCLK2
R32 2.2K/J_4 SB_SDATA2
R186 *2.2K/J_4 DNBSWON#

VCC3 R52 *4.7K/J_4 SUS_STAT#

VCC3 B-9 R80 100K/F_6
dGPU_VRON 2ms MXM_PWR_EN
21 MXM_PWREN
29 MXMPWR_EN MXMPWR_EN
12 dGPU_VRON
D5 RB501V-40
D4 *SW@RB501V-40
C107 0.1u/10V_4
>1mS delay is required between all MXM power rail stable and MXM_PWREN(enables the module internal power)

CN1 C23 10P/50V_4
SB_JTAG_TCK SB_JTAG_TDO SB_JTAG_TDI SB_TEST1 SB_JTAG_RST#
*S/W JTAG DEBUG
SB JTAG

41 ACZ_SDOUT_AUDIO ACZ_SDOUT_AUDIO R273 33/J_4 ACZ_SDOUT
21 MXM_SDOUT_HDMI MXM_SDOUT_HDMI R249 33_4C478 *10P/50V_4
41 ACZ_SYNC_AUDIO ACZ_SYNC_AUDIO R277 33/J_4 ACZ_SYNC
21 MXM_SYNC_HDMI MXM_SYNC_HDMI R247 33_4C479 *10P/50V_4
41 ACZ_BITCLK_AUDIO ACZ_BITCLK_AUDIO R271 33/J_4 ACZ_BCLK
21 MXM_BIT_CLK_HDMI MXM_BIT_CLK_HDMI R248 33_4C75 10P/50V_4
41 ACZ_RST#_AUDIO ACZ_RST#_AUDIO R281 33/J_4 ACZ_RST#
21 MXM_RST#_R MXM_RST#_R R250 33_4
ACZ_SDIN0 ACZ_SDIN0 41
ACZ_SDIN1 ACZ_SDIN1 21

If the VDDIO_AZ_S power rail is configured for 1.5V_S5 then AZ_SDIN[3:0] can not be connected to 3.3-V devices.

2,3,5,9,10,11,12,14,15,16,17,18,19,20,21,22,23,24,25,26,27,29,30,31,33,34,38,39,41 VCC3 VCC3

USBCLK/41M_25M_48M_OSC pin is CLK input pin when EXT CLKGEN mode.
It is output CLK source when INT CLKGEN mode.

U19D
SB800 Part 4 of 5
SB820M_A12

	PCI_PME#/GEVENT4#		
	RI#/GEVENT22#		
	SPI_CS3#/GBE_STAT1/GEVENT21#		
29 SUSB#	SLP_S3#		
29 SUSC#	SLP_S5#		
29 DNBSWON#	PWR_BTN#		
16 SB_PWRGD_IN	PWR_GOOD		
9 SUS_STAT#	SUS_STAT#		
SB_TEST0	TEST0		
SB_TEST1	TEST1/TMS		
SB_TEST2	TEST2		
29 SIO_A20GATE	GA20IN/GEVENT0#		
29 SIO_RCIN#	KBRST#/GEVENT1#		
T70 LANLINK_STATE#	LPC_PME#/GEVENT3#		
29 SIO_EXT_SMI#	LPC_SMI#/GEVENT23#		
29 SIO_EXT_SCI#	GEVENT5#		
T71 SYS_RST#	SYS_RESET#/GEVENT19#		
PCIE_WAKE#	WAKE#/GEVENT8#		
T73 IR_RX1	IR_RX1/GEVENT20#		
5 CPU_THERMTRIP# R57 *0/short_4	THRMTRIP#/SMBALERT#/GEVENT2#		
16 NB_PWRGD_IN	NB_PWRGD		
29 ICH_RSMRST# R610 *0_4 R611 22K C703 4.7U/6.3V_6	RSMRST#		
SB_GPIO_PCIE_RST#	CLK_REQ4#/SATA_IS0#/GPIO64		
	CLK_REQ3#/SATA_IS1#/GPIO63		
	SMARTVOLT1/SATA_IS2#/GPIO50		
T31 MXM_PWR_EN	CLK_REQ0#/SATA_IS3#/GPIO60		
T33 SB_GPIO59	SATA_IS4#/FANOUT3/GPIO55		
41 SPKR	SATA_IS5#/FANIN3/GPIO59		
2,17,18,19,20,24 PCLK_SMB	SPKR/GPIO66		
2,17,18,19,20,24 PDAT_SMB	SCL0/GPIO43		
26 SB_SMBCLK1	SDA0/GPIO47		
26 SB_SMBDATA1	SCL1/GPIO227		
21,27,29 dGPU_PRSNT#	SDA1/GPIO228		
T25 CRD_CLKREQ#	CLK_REQ2#/FANIN4/GPIO62		
	CLK_REQ1#/FANOUT4/GPIO61		
T11	IR_LED#/LLB#/GPIO184		
	SMARTVOLT2/SHUTDOWN#/GPIO51		
	DDR3_RST#/GEVENT7#		
	GBE_LED0/GPIO183		
	GBE_LED1/GEVENT9#		
	GBE_LED2/GEVENT10#		
2 EXT_SB_OSC	GBE_STAT0/GEVENT11#		
	CLK_REQG#/GPIO65/OSCIN		
T72 OC7#	BLINK/USB_OC7#/GEVENT18#		
T3 OC6#	USB_OC6#/IR_TX1/GEVENT6#		
T5	USB_OC5#/IR_TX0/GEVENT17#		
T4 OC4#	USB_OC4#/IR_RX0/GEVENT16#		
SB_JTAG_TDO	USB_OC3#/AC_PRES/TDO/GEVENT15#		
SB_JTAG_TCK	USB_OC2#/TCK/GEVENT14#		
SB_JTAG_TDI	USB_OC1#/TDI/GEVENT13#		
SB_JTAG_RST#	USB_OC0#/TRST#/GEVENT12#		
	USBCLK/14M_25M_48M_OSC	A10	R257 22_4 CLK_48M_USB 2,22
	USB_RCOMP	G19	USB_RCOMP_SB R44 11.8K/F_6
	USB_FSD1P/GPIO186	J10	
	USB_FSD1N	H11	
	USB_FSD0P/GPIO185	H9	
	USB_FSD0N	J8	
	USB_HSD13P	B12	
	USB_HSD13N	A12	
	USB_HSD12P	F11	USB_CARDP 22
	USB_HSD12N	E11	USB_CARDN 22
	USB_HSD11P	E14	USB_FDS12P USB_FDS12P 25
	USB_HSD11N	E12	USB_FSD12N USB_FSD12N 25
	USB_HSD10P	J12	USBP10+ 25
	USB_HSD10N	J14	USBP10- 25
	USB_HSD9P	A13	USBP9+ 25
	USB_HSD9N	B13	USBP9- 25
	USB_HSD8P	D13	USBP8+ 25
	USB_HSD8N	C13	USBP8- 25
	USB_HSD7P	G12	USBP7+ 24
	USB_HSD7N	G14	USBP7- 24
	USB_HSD6P	G16	USBP6+ 24
	USB_HSD6N	G18	USBP6- 24
	USB_HSD5P	D16	USBP5+ 25
	USB_HSD5N	C16	USBP5- 25
	USB_HSD4P	B14	USBP4+ 25
	USB_HSD4N	A14	USBP4- 25
	USB_HSD3P	E18	USBP3+ 30
	USB_HSD3N	E16	USBP3- 30
	USB_HSD2P	J16	USBP2+ 30
	USB_HSD2N	J18	USBP2- 30
	USB_HSD1P	B17	USBP1+ 30
	USB_HSD1N	A17	USBP1- 30
	USB_HSD0P	A16	USBP0+ 30
	USB_HSD0N	B16	USBP0- 30
	SCL2/GPIO193	D25	SB_SCLK2
	SDA2/GPIO194	F23	SB_SDATA2
	SCL3_LV/GPIO195	B26	SB_GPIO195
	SDA3_LV/GPIO196	F26	SB_GPIO196
	EC_PWM0/EC_TIMER0/GPIO197	F25	
	EC_PWM1/EC_TIMER1/GPIO198	E22	
	EC_PWM2/EC_TIMER2/GPIO199	F22	GPIO199 16
	EC_PWM3/EC_TIMER3/GPIO200	F21	GPIO200 16
	KSI_0/GPIO201	G24	
	KSI_1/GPIO202	G25	
	KSI_2/GPIO203	E28	
	KSI_3/GPIO204	E29	
	KSI_4/GPIO205	D29	
	KSI_5/GPIO206	D28	
	KSI_6/GPIO207	C29	
	KSI_7/GPIO208	C28	
	KSO_0/GPIO209	B28	
	KSO_1/GPIO210	A27	
	KSO_2/GPIO211	B27	
	KSO_3/GPIO212	D26	
	KSO_4/GPIO213	A26	
	KSO_5/GPIO214	C26	
	KSO_6/GPIO215	A24	
	KSO_7/GPIO216	B25	
	KSO_8/GPIO217	A25	
	KSO_9/GPIO218	D24	
	KSO_10/GPIO219	B24	
	KSO_11/GPIO220	C24	
	KSO_12/GPIO221	B23	
	KSO_13/GPIO222	A23	
	KSO_14/GPIO223	D22	
	KSO_15/GPIO224	C22	
	KSO_16/GPIO225	A22	
	KSO_17/GPIO226	B22	

ACPI / WAKE UP EVENTS
USB 1.1 USB MISC
GPIO
USB 2.0
USB OC
HD AUDIO
GBE LAN
EMBEDDED CTRL
EMBEDDED CTRL

HD audio interface is +3VS5 voltage

16 ACZ_SDOUT
R56 *10K/F_4 ACZ_BCLK
ACZ_SDOUT
R422 *10K/F_4 ACZ_SDIN0
R144 *10K/F_4 ACZ_SDIN1
R272 *10K/F_4 ACZ_SDIN2
R59 *10K/F_4 ACZ_SDIN3
ACZ_SYNC
ACZ_RST#
AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO167
AZ_SDIN1/GPIO168
AZ_SDIN2/GPIO169
AZ_SDIN3/GPIO170
AZ_SYNC
AZ_RST#

3V_S5 B-8
R276 10K/F_4 GBE_COL
R63 10K/F_4 GBE_CRS
R58 10K/F_4 GBE_MDIO
R65 10K/F_4 GBE_RXERR
R64 10K/F_4 GBE_PHY_INTR
GBE_COL
GBE_CRS
GBE_MDCK
GBE_MDIO
GBE_RXCLK
GBE_RXD3
GBE_RXD2
GBE_RXD1
GBE_RXD0
GBE_RXCTL/RXDV
GBE_RXERR
GBE_TXCLK
GBE_TXD3
GBE_TXD2
GBE_TXD1
GBE_TXD0
GBE_TXCTL/TXEN
GBE_PHY_PD
GBE_PHY_RST#
GBE_PHY_INTR

T2 ADP_PRES0
T6
PS2_DAT/SDA4/GPIO187
PS2_CLK/SCL4/GPIO188
SPI_CS2#/GBE_STAT2/GPIO166
FC_RST#/GPO160
PS2KB_DAT/GPIO189
PS2KB_CLK/GPIO190
PS2M_DAT/GPIO191
PS2M_CLK/GPIO192

SB_GPIO195 R266 10K/F_4
SB_GPIO196 R267 10K/F_4

MULTI-TOUCH
Dongle
USB
CAMERA
BLUETOOTH
TV MINI
CARD
WLAN MINI
CARD
Side
USB
Side
USB
USB
board
USB
board
USB
board
USB
board

Quanta Computer Inc.
PROJECT : ZN8

Size	Document Number	Rev
	SB820-ACPI/GPIO/USB 2/4	1A
Date: Monday, March 22, 2010	Sheet 13 of 40	

SATA PORT 0,1,2,3
can support AHCI
mode

SATA1

SATA ODD

U19B

SB800
Part 2 of 5

SB820M_A12

Signal Name	Explanation
SATA_CALRP	SB800 A11: 800-? 1% resistor to GND. P/N:CS18062FB00(806 Ohm) SB800 A12: TBD-? 1% resistor to GND. (1K ohm)
SATA_CALRN	SB800 A11: 931-? 1% resistor to VDDAN_11_SATA. SB800 A12: TBD-? 1% resistor to VDDAN_11_SATA.

PLACE SATA_CAL
RES VERY CLOSE
TO BALL OF SB820

IF THERE IS NO IDE, TEST
POINTS FOR DEBUG BUS
IS MANDATORY

8Mbit , SPI

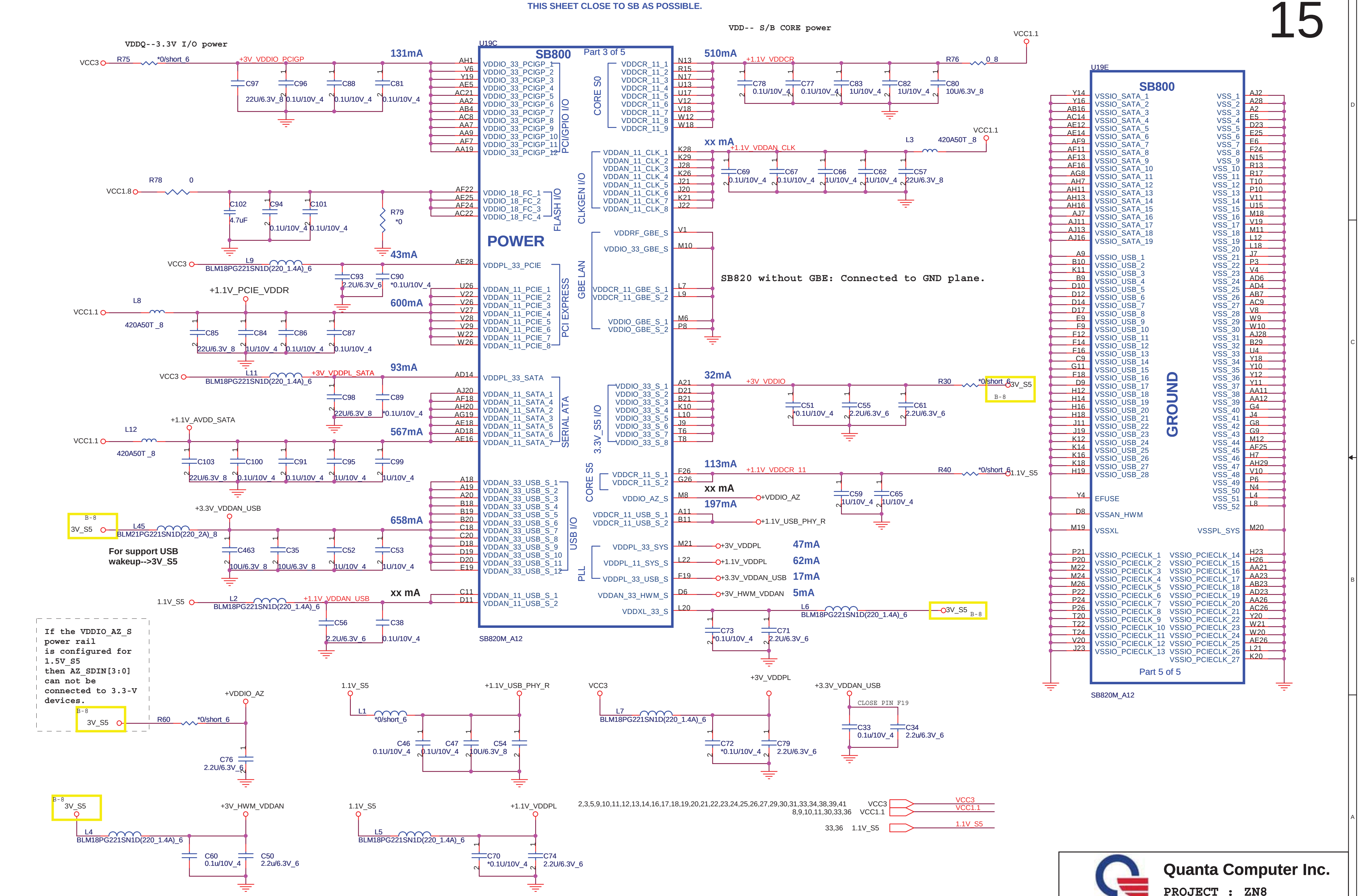
	ID4	ID3	ID2	ID1	ID0
0				UMA	14"
1				Discrete	15"

Quanta Computer Inc.
PROJECT : ZN8

Size	Document Number	Rev
	SB820-SATA/IDE/HWM/SPI 3/4	1A

Date: Monday, March 22, 2010 Sheet 14 of 40

PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.



Quanta Computer Inc.

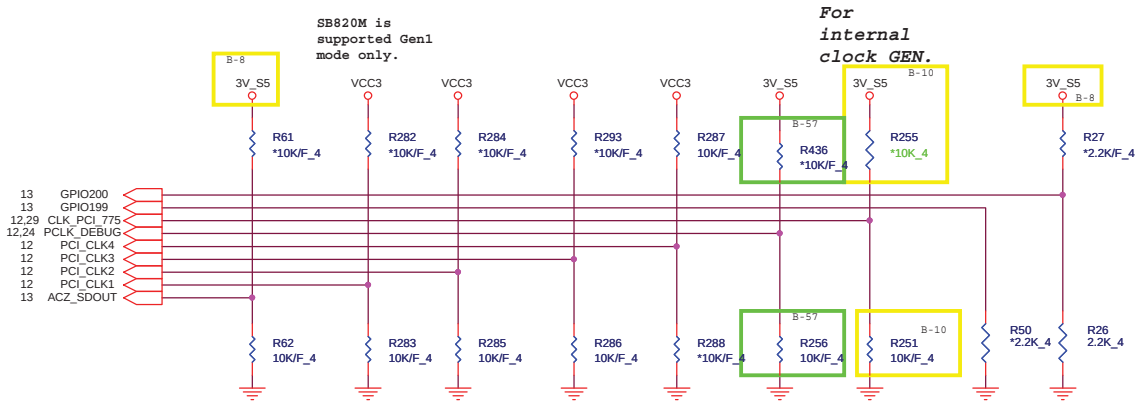
PROJECT : ZN8

Size	Document Number	Rev
	SB820-PWR/DECOUPLING 4/4	1A

Date: Monday, March 22, 2010 Sheet 15 of 40

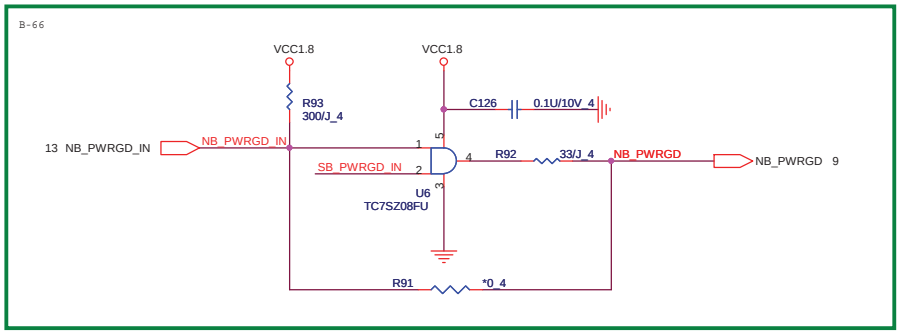
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

REQUIRED STRAPS



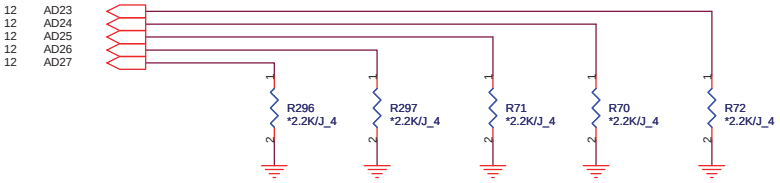
	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200 GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2	Watchdog Timer Enable	USE DEBUG STRAPS	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	INT. CLKGEN ENABLED DEFAULT	H, H=Reserved H, L=SPI ROM
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1 DEFAULT	Watchdog Timer Disable DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK MODE	EC DISABLED DEFAULT	EXT. CLKGEN ENABLE	L,H=LPC ROM DEFAULT L, L=FWH ROM

internal have pull Hi 10K



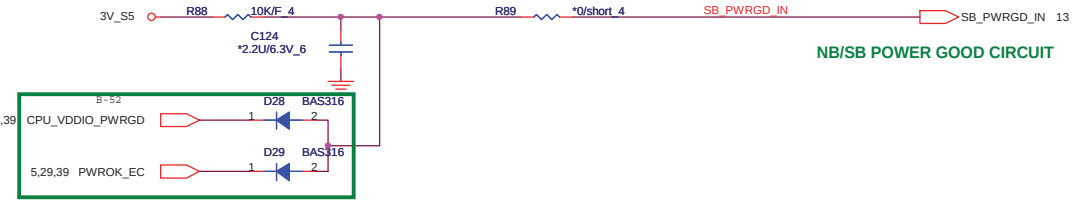
DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	DISABLE I2C ROM DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	ENABLE I2C ROM use REQ3# as SDA use GNT3# as SCL	ENABLE PCI MEM BOOT

NB_PWRGD_IN:
RS880/RX881 = 1.8V;
Do NOT share it with SB_PWRGD when use Internal Clk Gen (Need SB PLL initialize firstly)



NB/SB POWER GOOD CIRCUIT

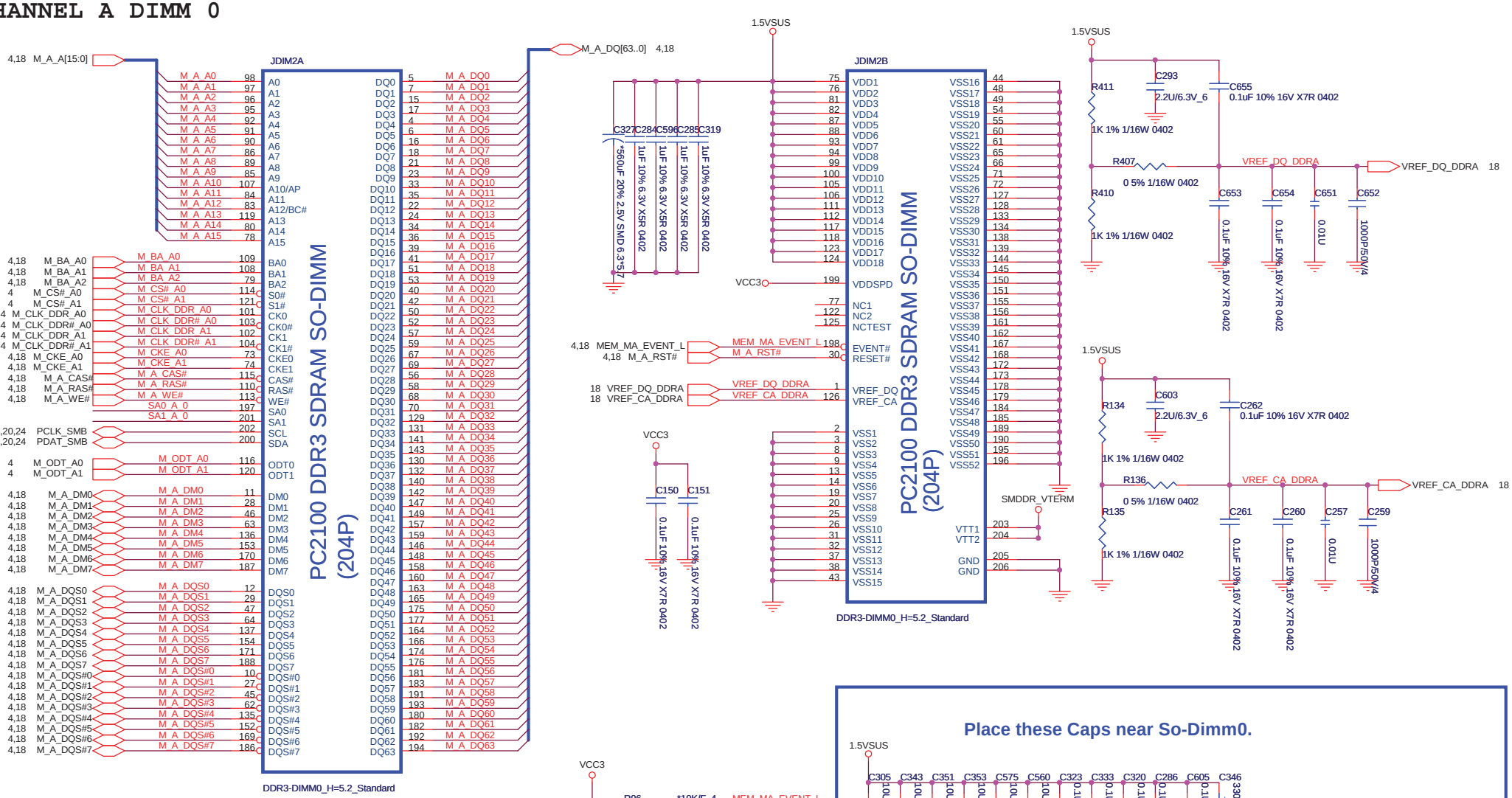
Quanta Computer Inc.

PROJECT : ZN8

Size	Document Number	Rev
	SB820-STRAPS/PWRGD	1A

Date: Monday, March 22, 2010 Sheet 16 of 40

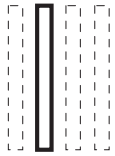
CHANNEL A DIMM 0



Place these Caps near So-Dimm0.

FOX H:9.2 white

PCB Placement



SPD SA0	0
SPD SA1	0

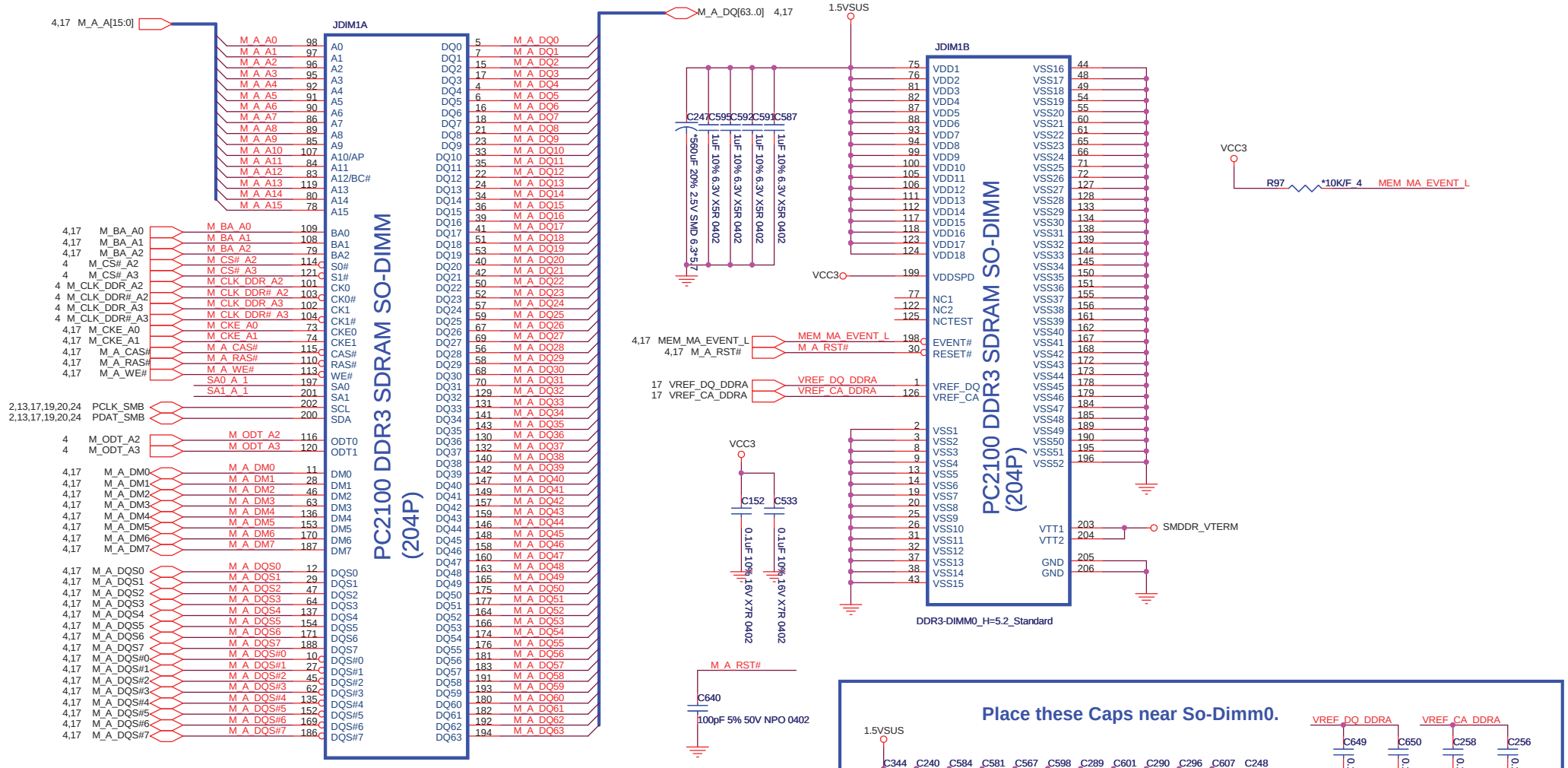
R98 0 5% 1/16W 0402 SA1_A_0

R99 0 5% 1/16W 0402 SA0_A_0

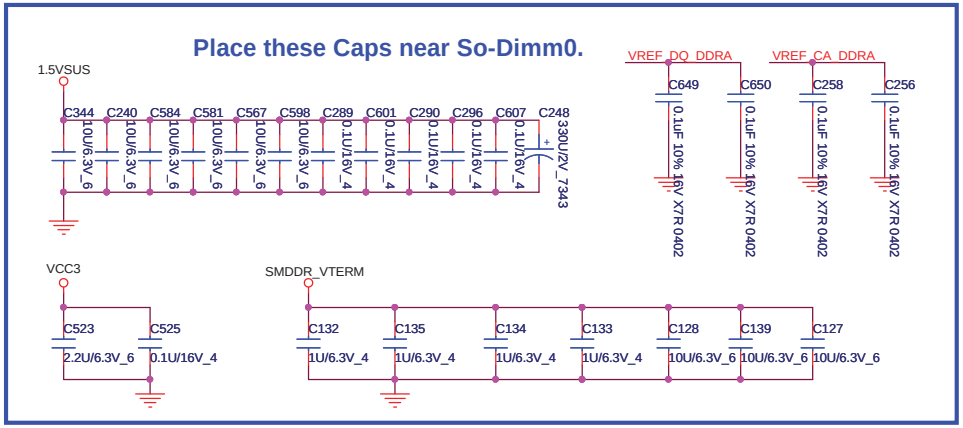
AM3

Quanta Computer Inc.			
PROJECT : ZN8			
Size	Document Number: DDR3 CHA DIMM 0		Rev 1A
Date: Monday, March 22, 2010		Sheet 17 of 40	

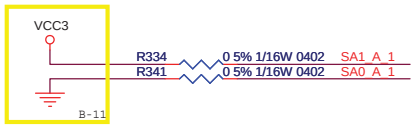
CHANNEL A DIMM 1



Place these Caps near So-Dimm0.



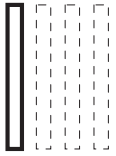
SPD SA0	1
SPD SA1	0



AM3

FOX H:5.2 white

PCB Placement

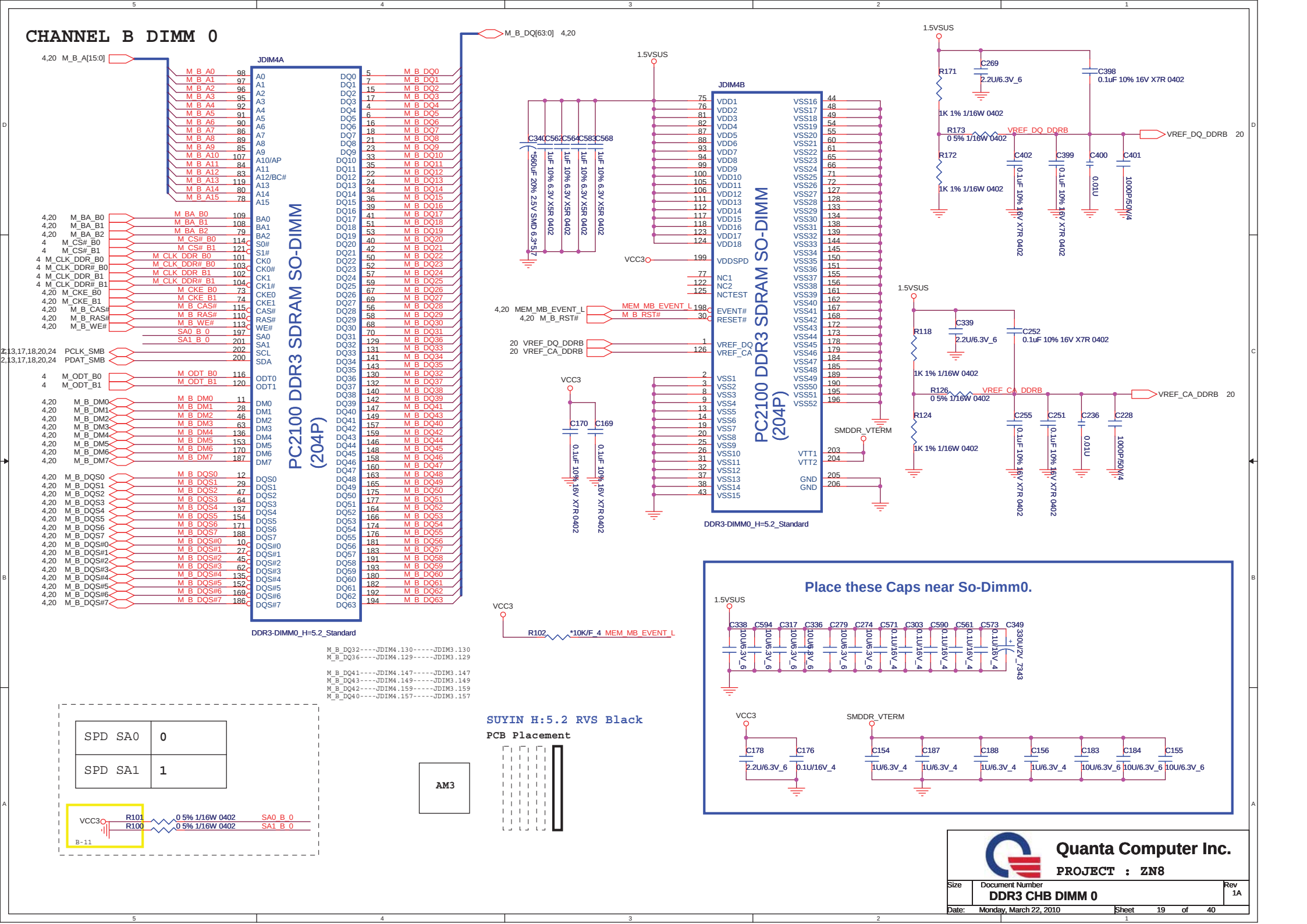


Quanta Computer Inc.

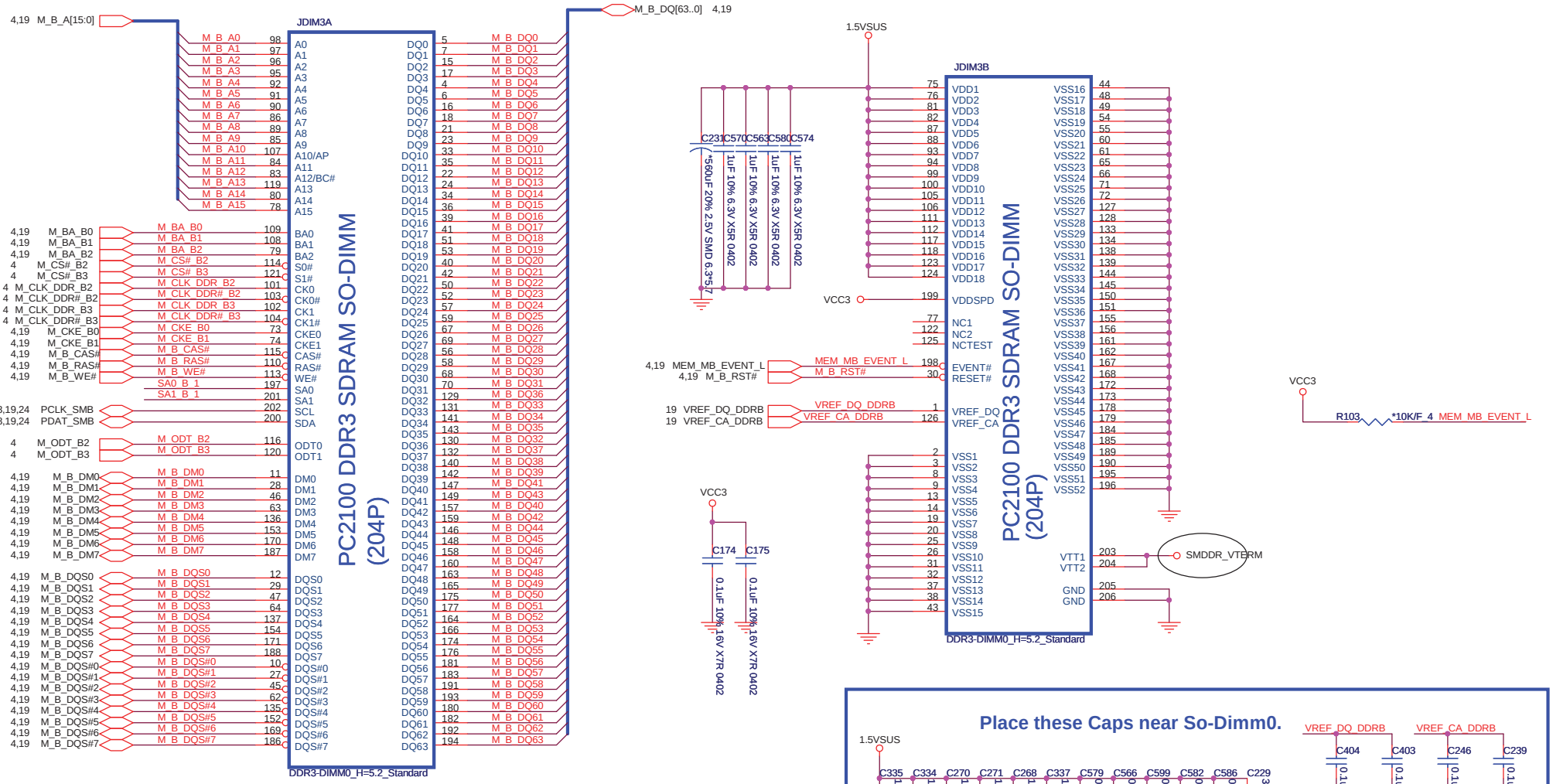
PROJECT : ZN8

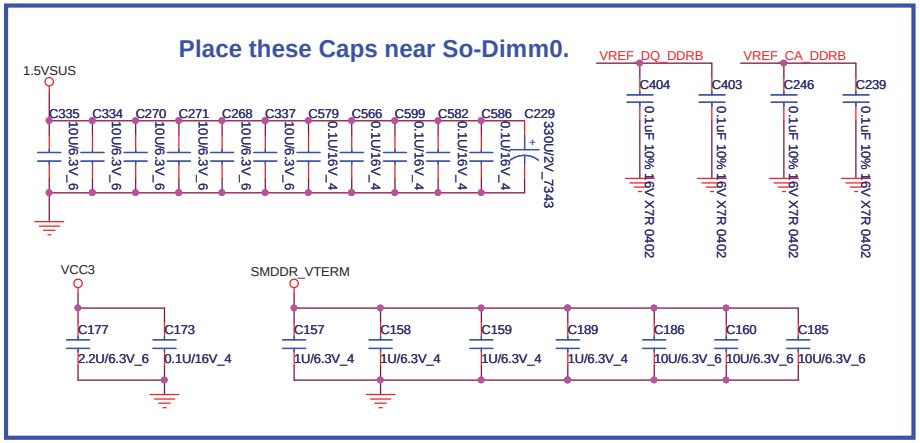
Size	Document Number	Rev
	DDR3 CHA DIMM1	1A
Date: Monday, March 22, 2010	Sheet 18 of 40	

CHANNEL B DIMM 0



CHANNEL B DIMM 1



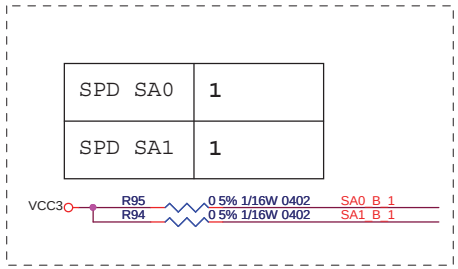


M_B_DQ32----JDIM4.130-----JDIM3.130
M_B_DQ36----JDIM4.129-----JDIM3.129

M_B_DQ41----JDIM4.147-----JDIM3.147
M_B_DQ43----JDIM4.149-----JDIM3.149
M_B_DQ42----JDIM4.159-----JDIM3.159
M_B_DQ40----JDIM4.157-----JDIM3.157

SUYIN H:9.2 RVS Black

PCB Placement



AM3

Quanta Computer Inc.

PROJECT : ZN8

Size	Document Number	Rev
	DDR3 CHB DIMM1	1A
Date: Monday, March 22, 2010	Sheet 20 of 40	

MXM Module

6/25 Change CN22 pin define and footprint at C test.

MXM3.0	n-Vidia	AMD
LVDS	LVDS	LVDS/Int. DP
DP_D	N/A	X
DP_A	HDMI	HDMI
DP_C	Ext. DP/DVI	Ext. DP/DVI
DP_B	N/A	N/A

dGPU_PRSNT#	Sku
Low	MXM
High	WO/ MXM

7/28: add decoupling capacitors for AMD recommendation

MXM DP CONN for Scalar Board

LVDS+DP CONN for MXM

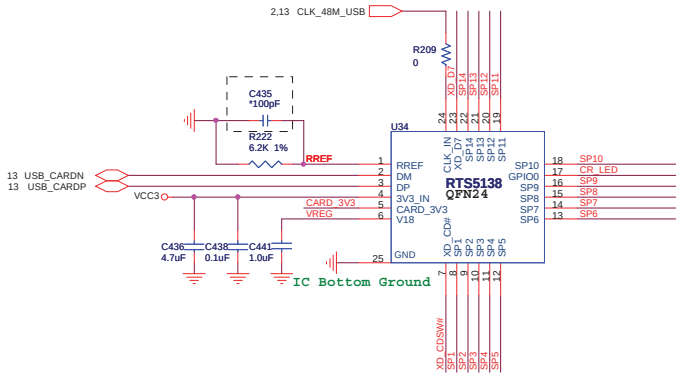
Thermo SMBus

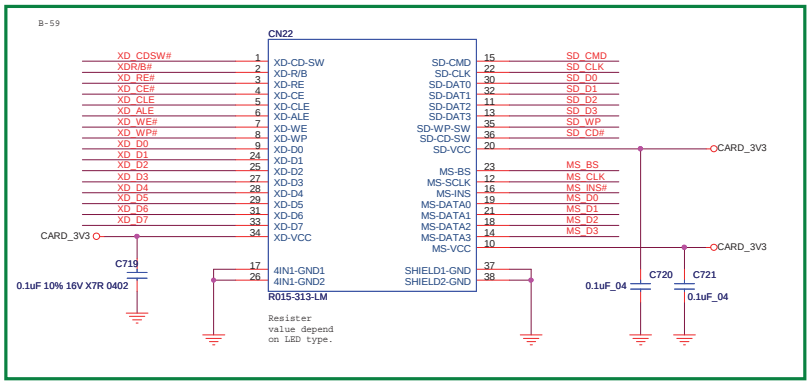
MXM VIN Power switch

MXM 3V/5V Power switch

To EC

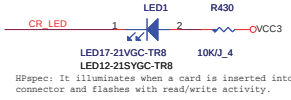
For CRT Debug

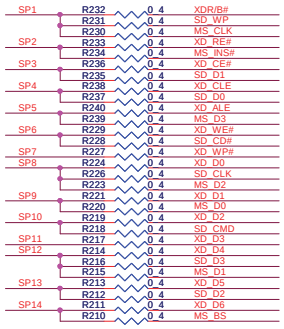


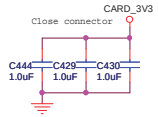


Share Pin

Share Pin	XD	MS	SD
SP1	XDR/B#	MS_CLK	SD_WP
SP2	XD_RE#	MS_INS#	
SP3	XD_CE#		SD_D1
SP4	XD_CLE	MS_D7	SD_D0
SP5	XD_ALE	MS_D3	SD_D7
SP6	XD_WE#		SD_CD#
SP7	XD_WP	MS_D6	SD_D6
SP8	XD_D0	MS_D2	SD_CLK
SP9	XD_D1	MS_D0	SD_D5
SP10	XD_D2		SD_CMD
SP11	XD_D3	MS_D4	SD_D4
SP12	XD_D4	MS_D1	SD_D3
SP13	XD_D5	MS_D5	SD_D2
SP14	XD_D6	MS_BS	







Quanta Computer Inc.

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Size	Document Number	Rev
	RTS5138	1A

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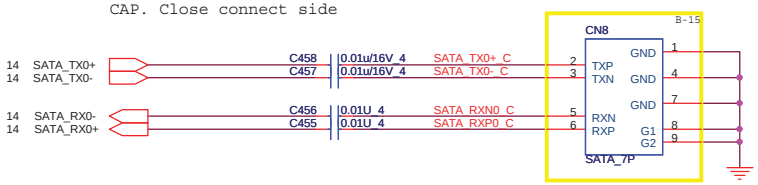
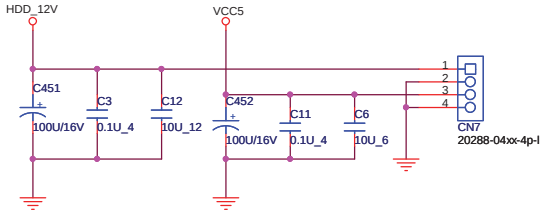
1st 2.5"/3/5" SATA HDD

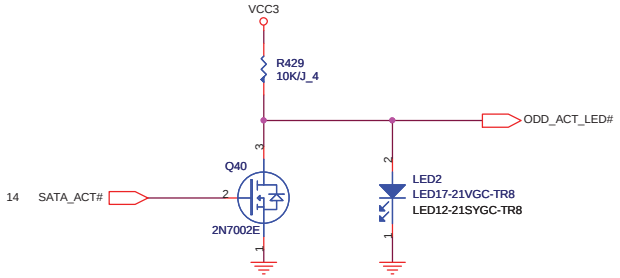
From PCH SATA

SATA HDD CONNECTOR

CAP. Close connect side





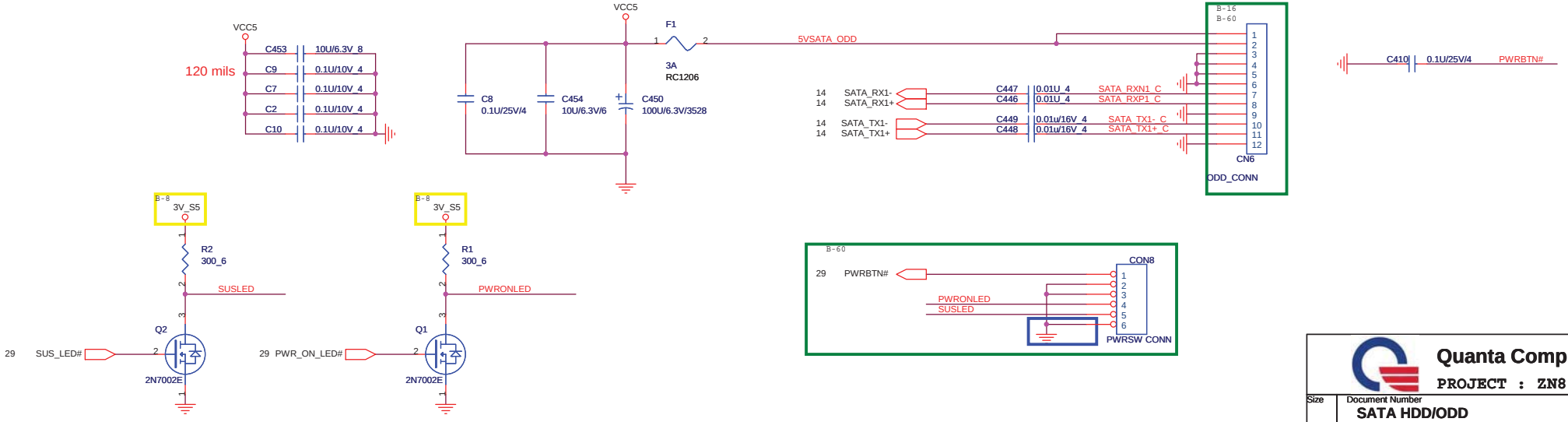


SATA CD-ROM

To SATA-HDD conn

SATA ODD CONNECTOR

USB connector same as ZN6



Quanta Computer Inc.

PROJECT : ZN8

Size	Document Number	Rev
	SATA HDD/ODD	1A

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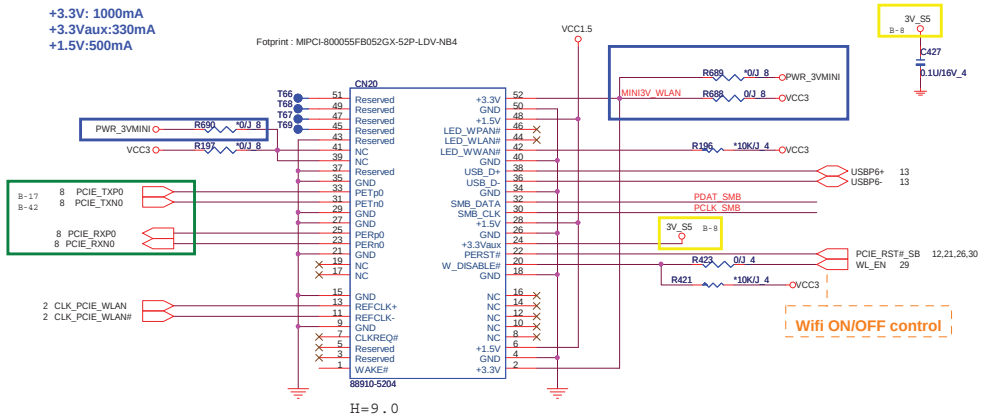
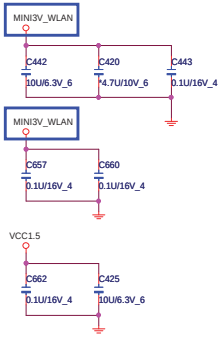
Wireless + BT

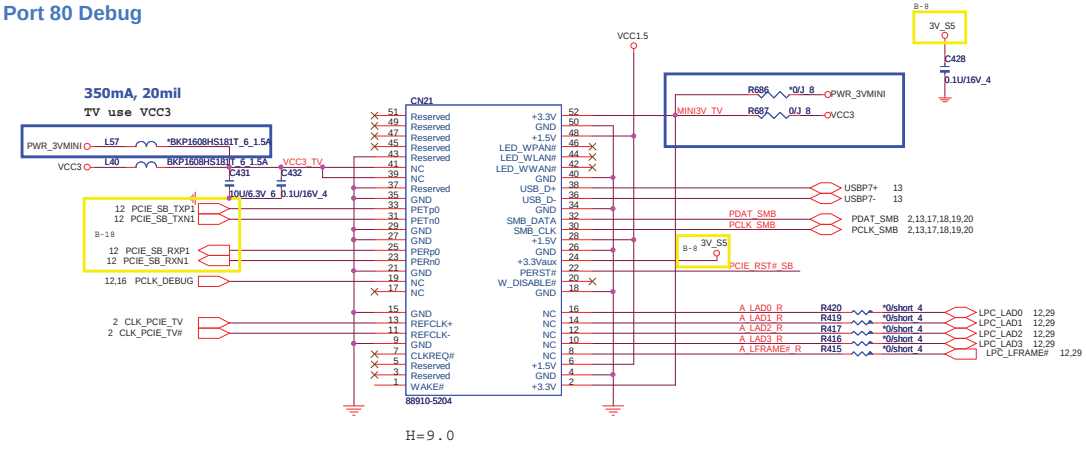
+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

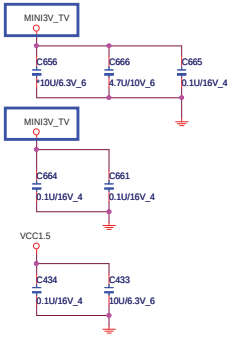


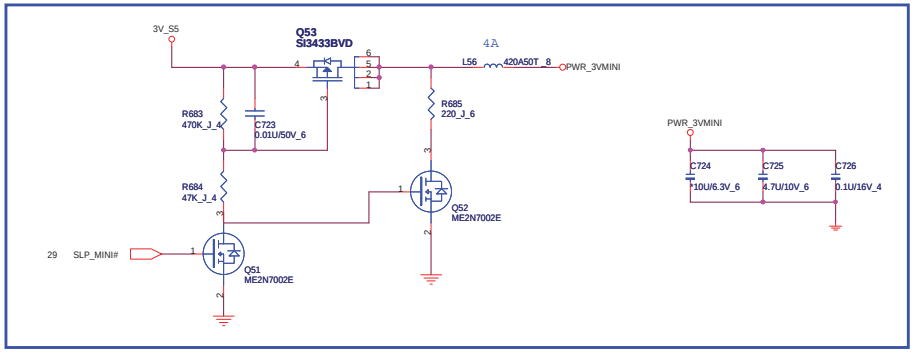


TV and Port 80 Debug

350mA, 20mil
TV use VCC3







Quanta Computer Inc.			
PROJECT : ZN8			
Size	Document Number		Rev
	MINI PCIE (WLAN/TV)		1A
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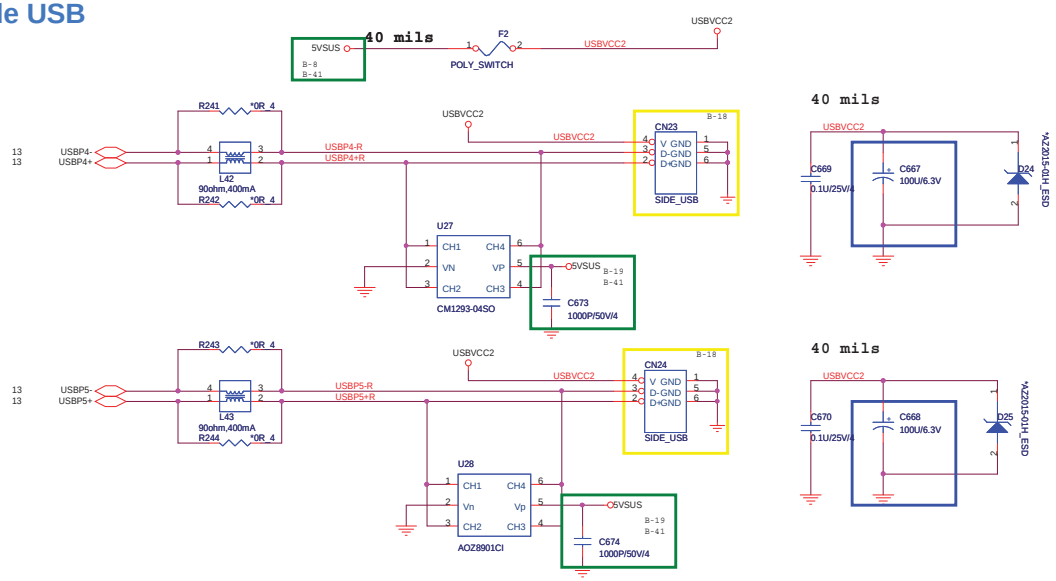
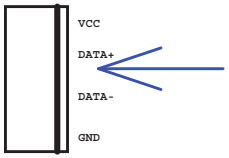
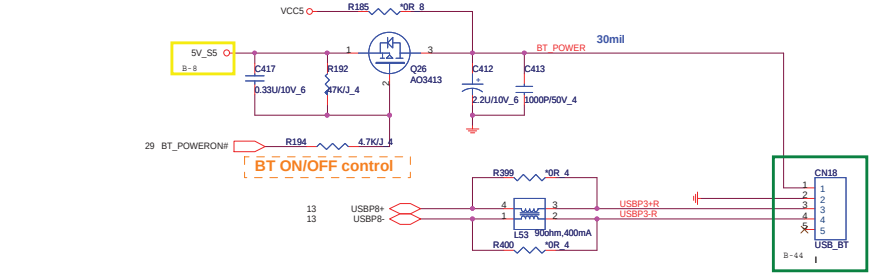
Side USB



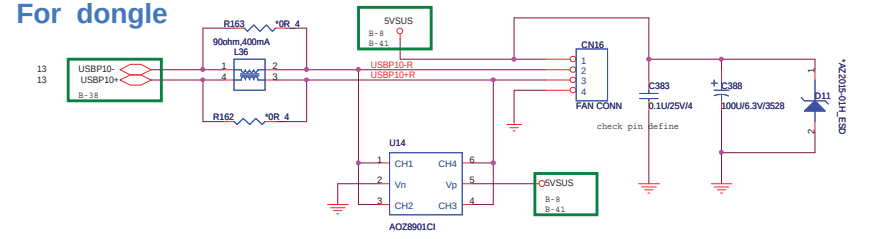


USB connector same as ZN6

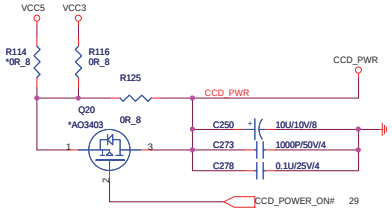
BLUETOOTH CONNECTOR



For dongle

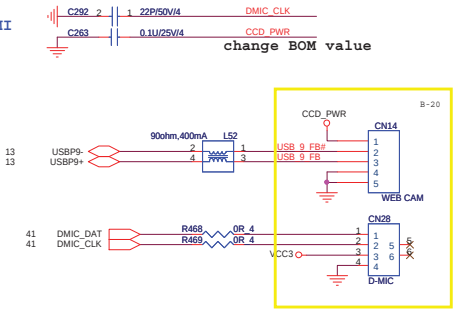


WEB CAM MODULE



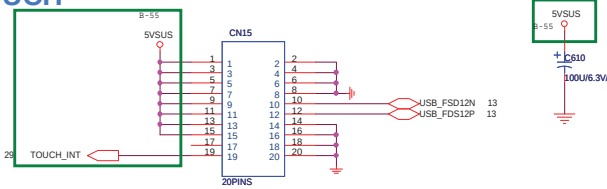
TO WEB CAM MODULE

FOR EMI



MULTI-TOUCH

HP spec:USB header for touch controller must be able to support 3.0 A.



Quanta Computer Inc.		
PROJECT : ZN8		
Size	Document Number: USB/CCD/BT/MT	Rev: 1A
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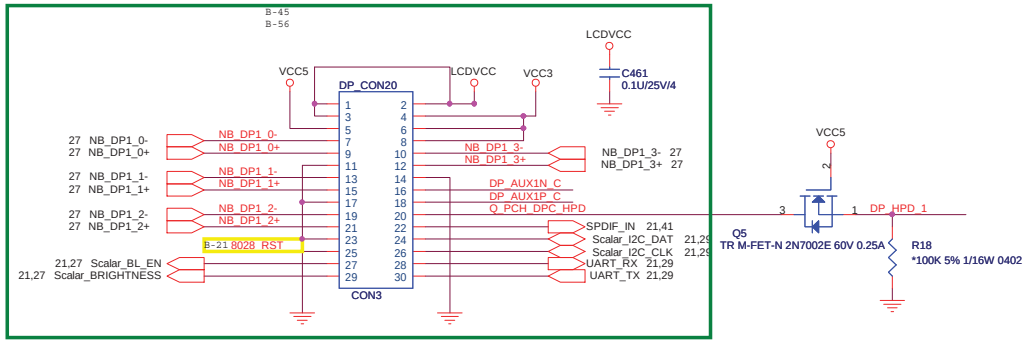
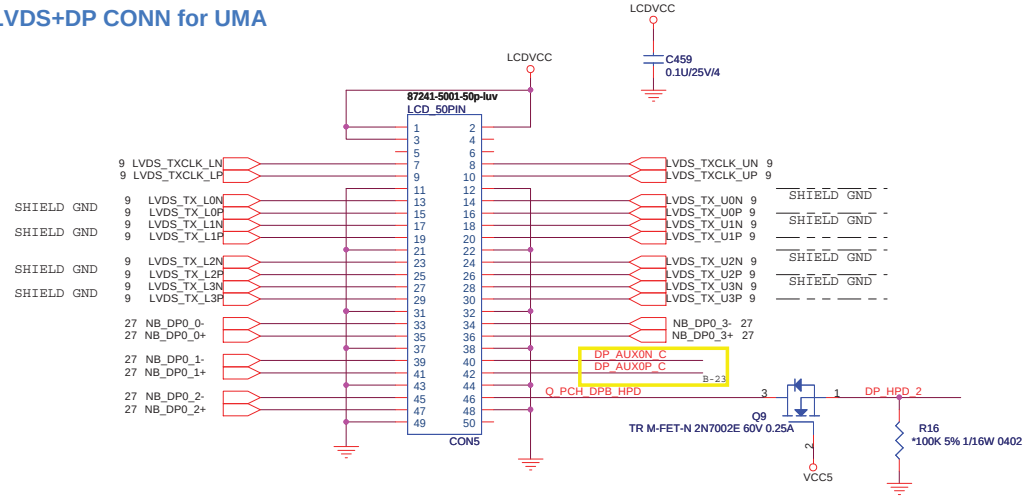
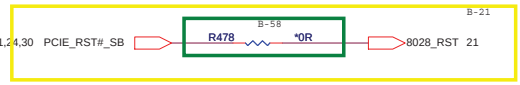
UMA DP CONN for scalar Board



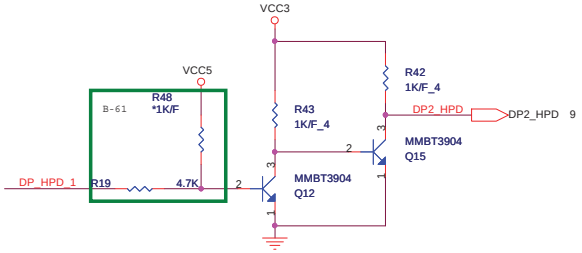
LVDS+DP CONN for UMA

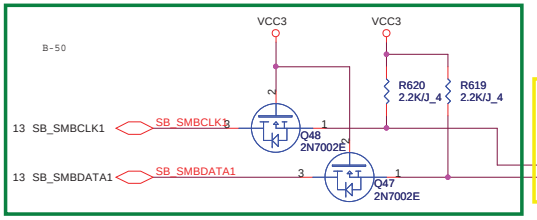


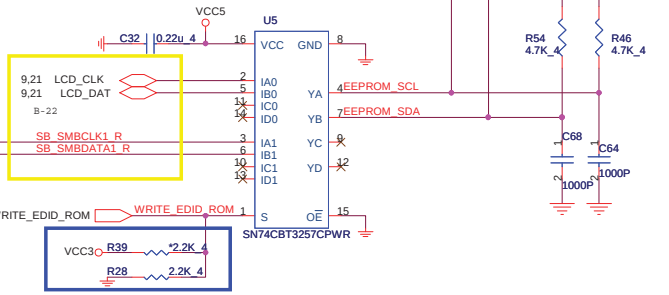


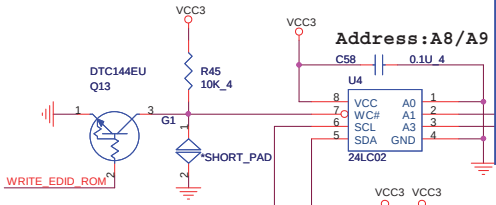
EEPROM IIC Selection

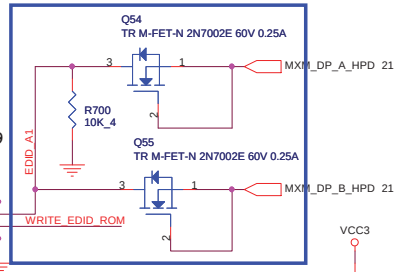
PANEL EDID DATA

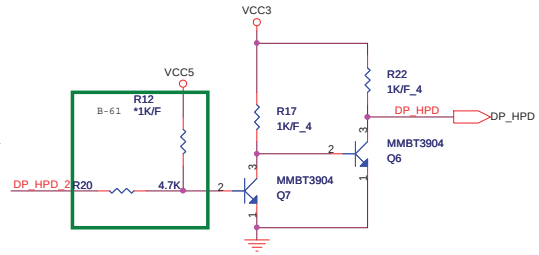


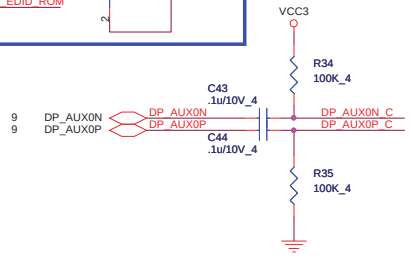


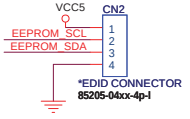


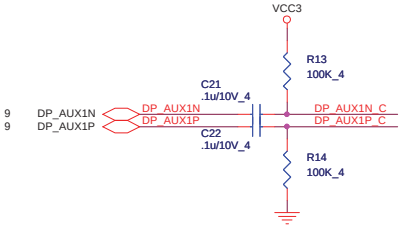












Quanta Computer Inc.

PROJECT : ZN8

Size	Document Number	Rev
	Panel (DP/LVDS)	1A

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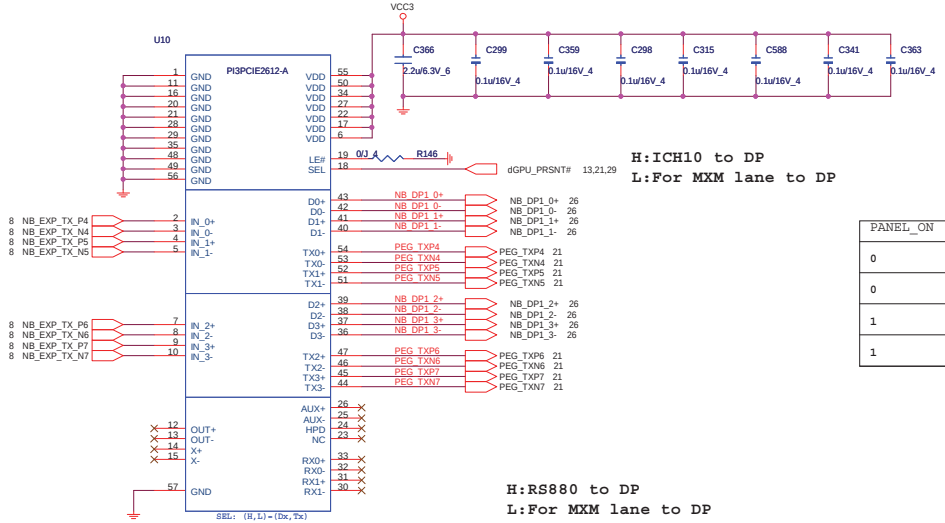
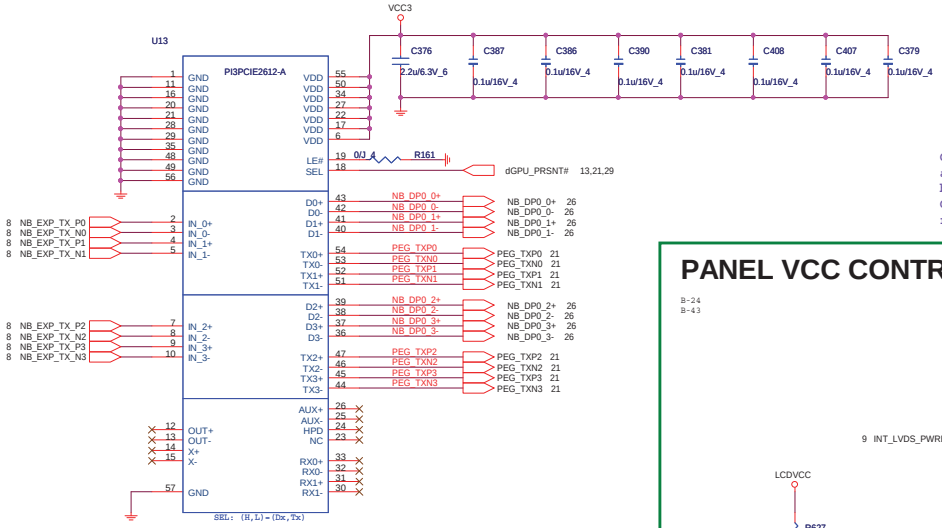
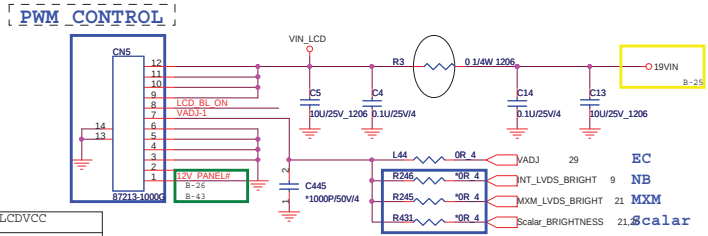
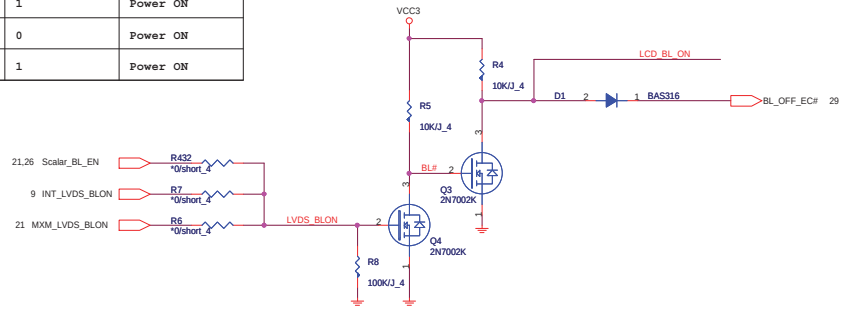
TO Converter Board

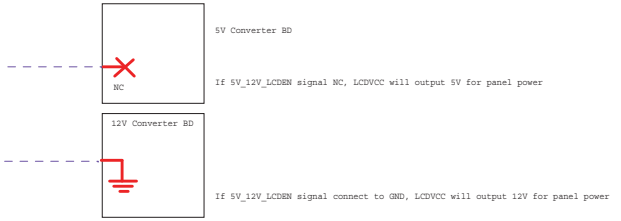






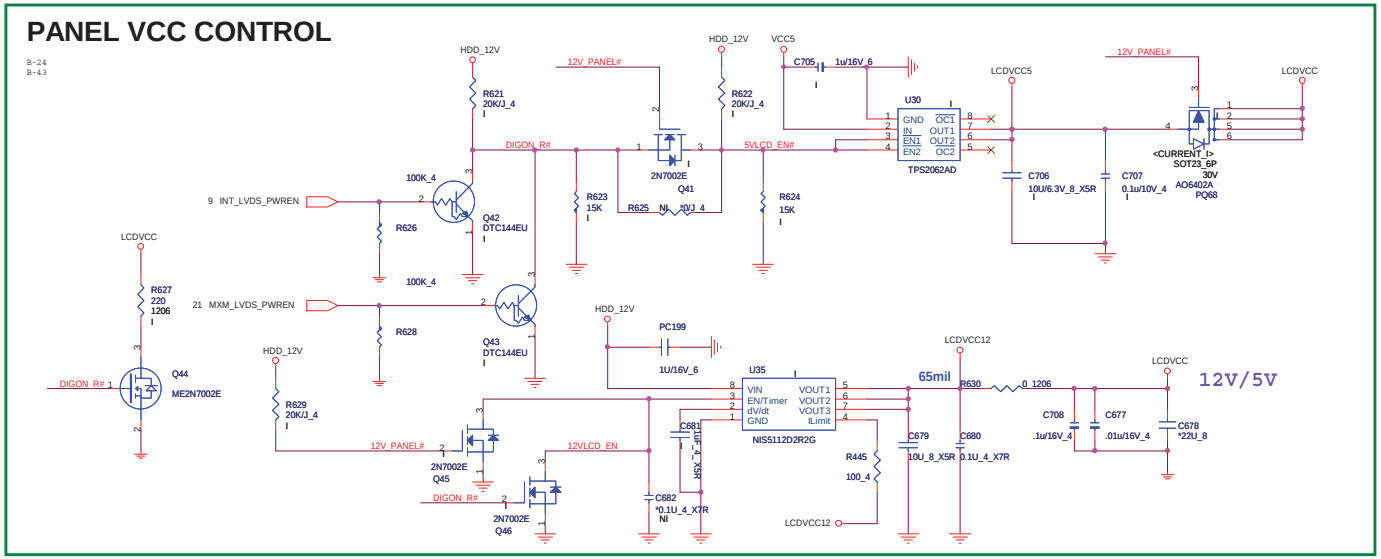
PANEL_ON	PANEL_ON_EC	LCDVCC
0	0	Power OFF
0	1	Power ON
1	0	Power ON
1	1	Power ON



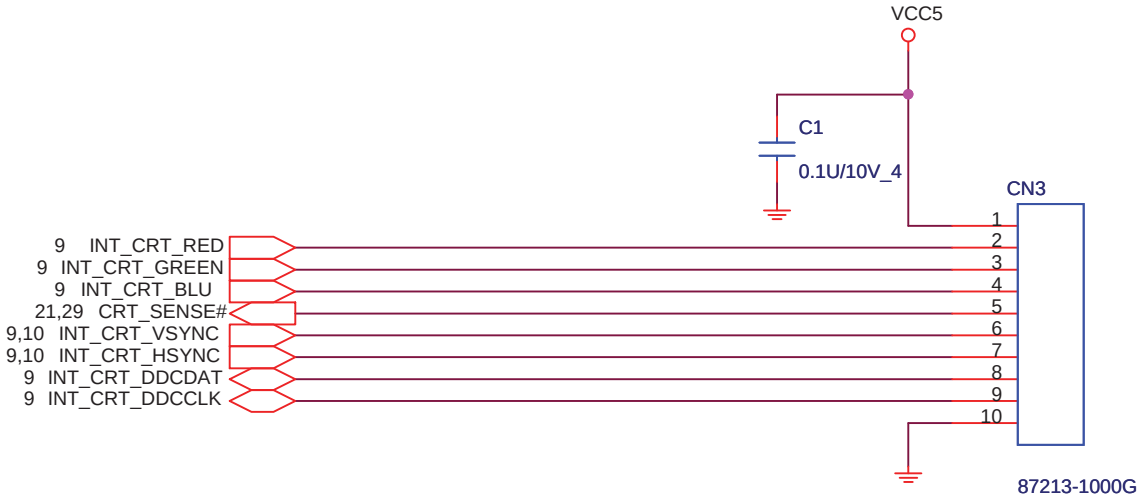


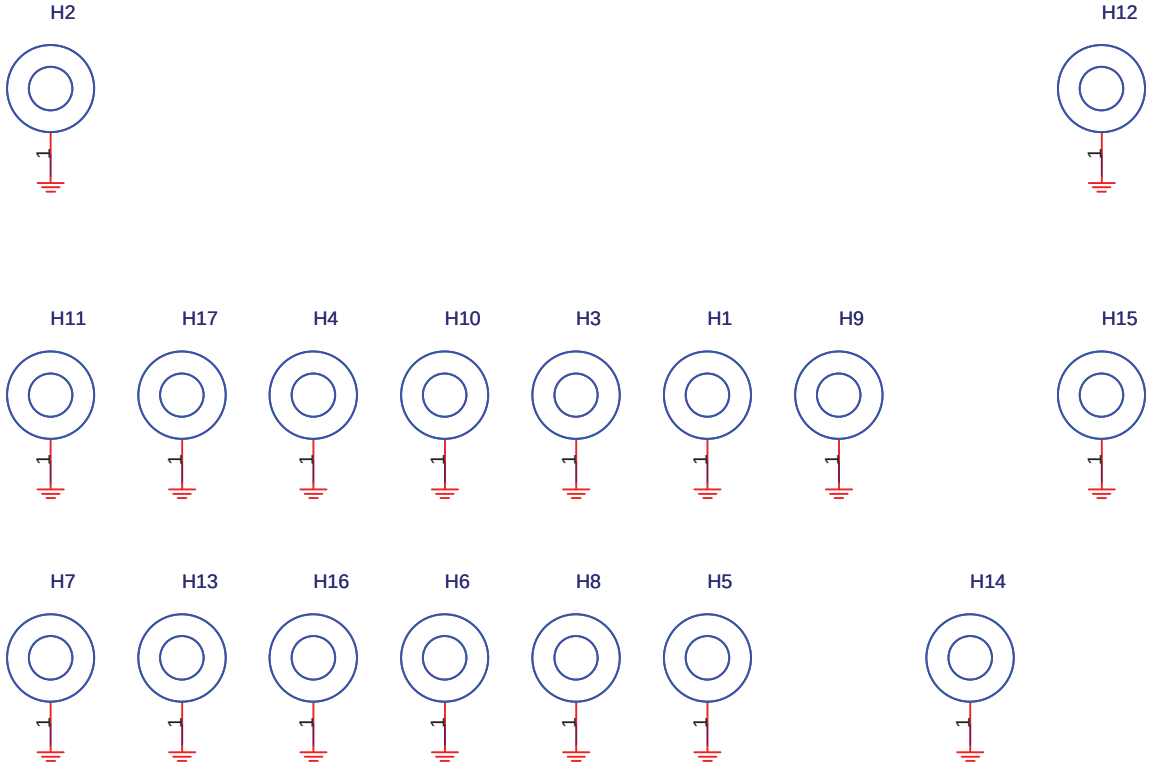
Option 2
a.5V panel --- remove Q41,C675,R438,R441,D26
b.12V panel --- remove Q41,R442,D26
Option 4
remove R441,R442

PANEL VCC CONTROL



CRT for Debug





Quanta Computer Inc.		
PROJECT : ZN8		
Size	Document Number: CRT	Rev: 1A
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EC

Layout Note:
Place all capacitors close to IT8512.

Layout Note:
net "3VPCU" and "RTC_VCC"
minimum trace width 12mils.

(For PLL Power)

IT8512NX

For PS2

For Debug use

8Mbit , SPI

HWPG

Input only

Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.

Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.

Layout Note:
Place R471,R498,R534 within 500 mils from SPI Flash.Place R567 within 500mils from R534; R520 within 500mils from R498 and R570 within 500mils from R471.

Layout Note:
32.768kHz clock lines:
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.

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Size	Document Number: EC ITE 8512N/FLASH		Rev: 1A
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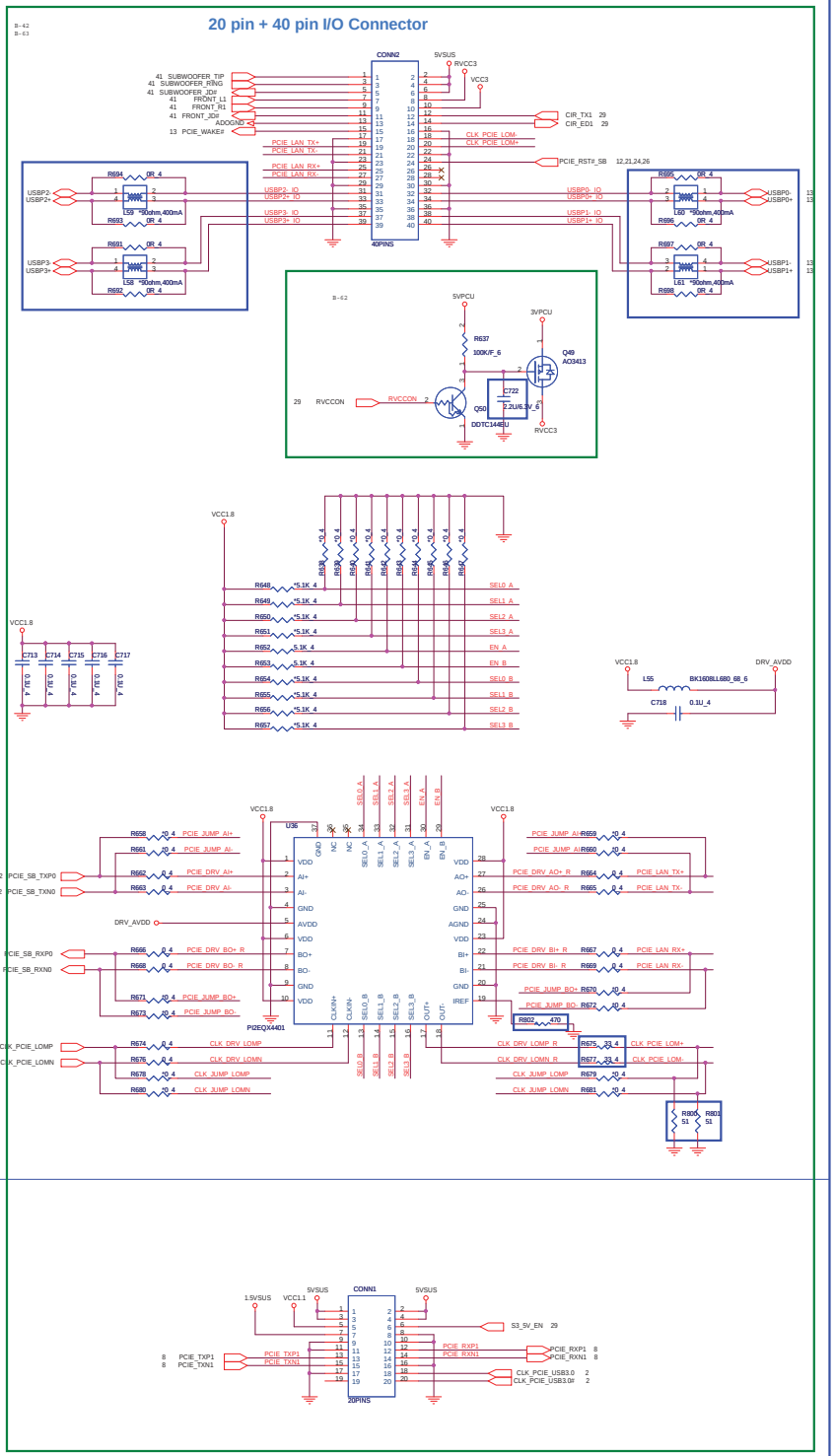
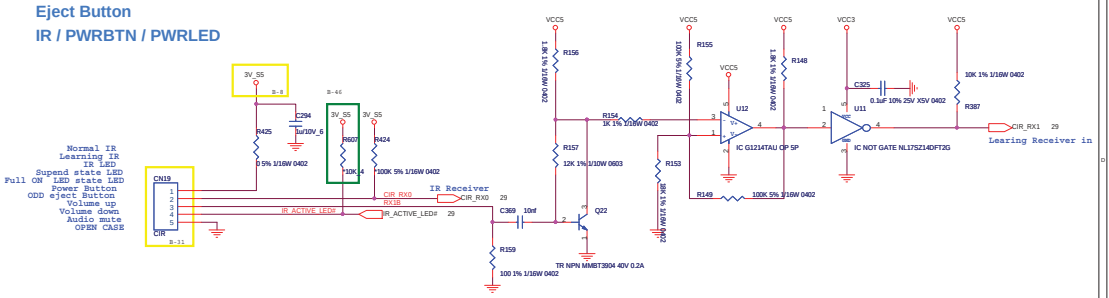
20 pin + 40 pin I/O Connector

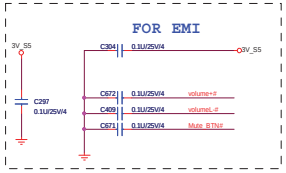


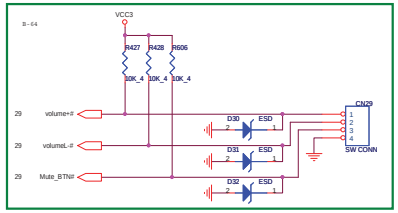
Eject Button
IR / PWRBTN / PWRLED

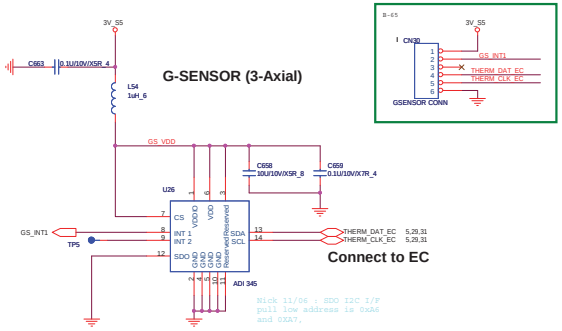


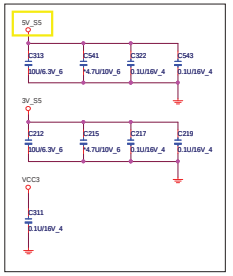
The aqua-white (470 +/- 5 nm) color is used to indicate the system is powered on and in the S0 state. The amber (590 +/- 5 nm) color is used to indicate the system is in one of the standby states (S3, S4, S5).

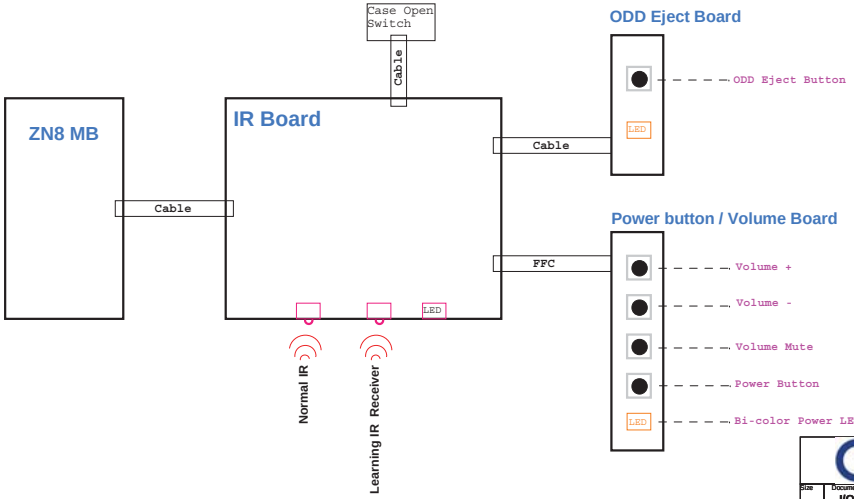
PWRBTN# must pull up to PCU power well











Quanta Computer Inc.			
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Size	Document Number		Rev
	I/O Board Connector		1A
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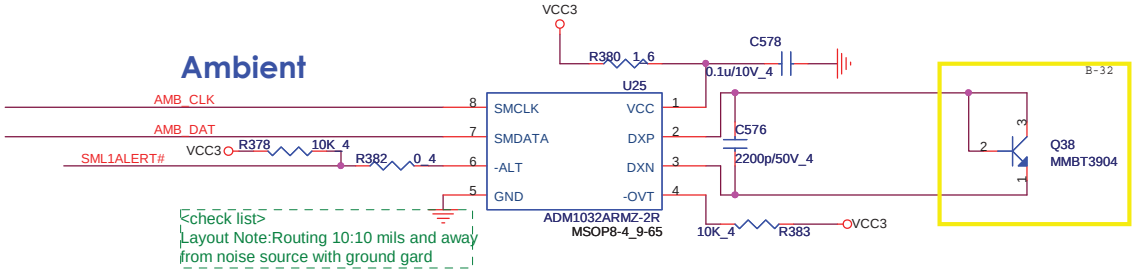

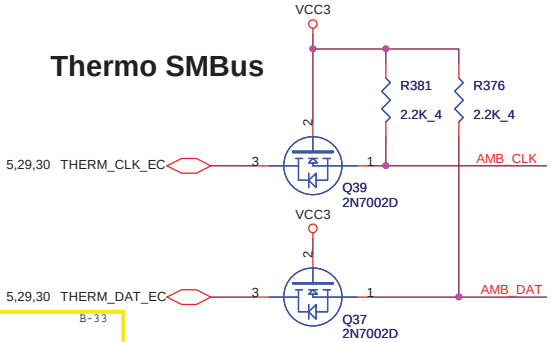

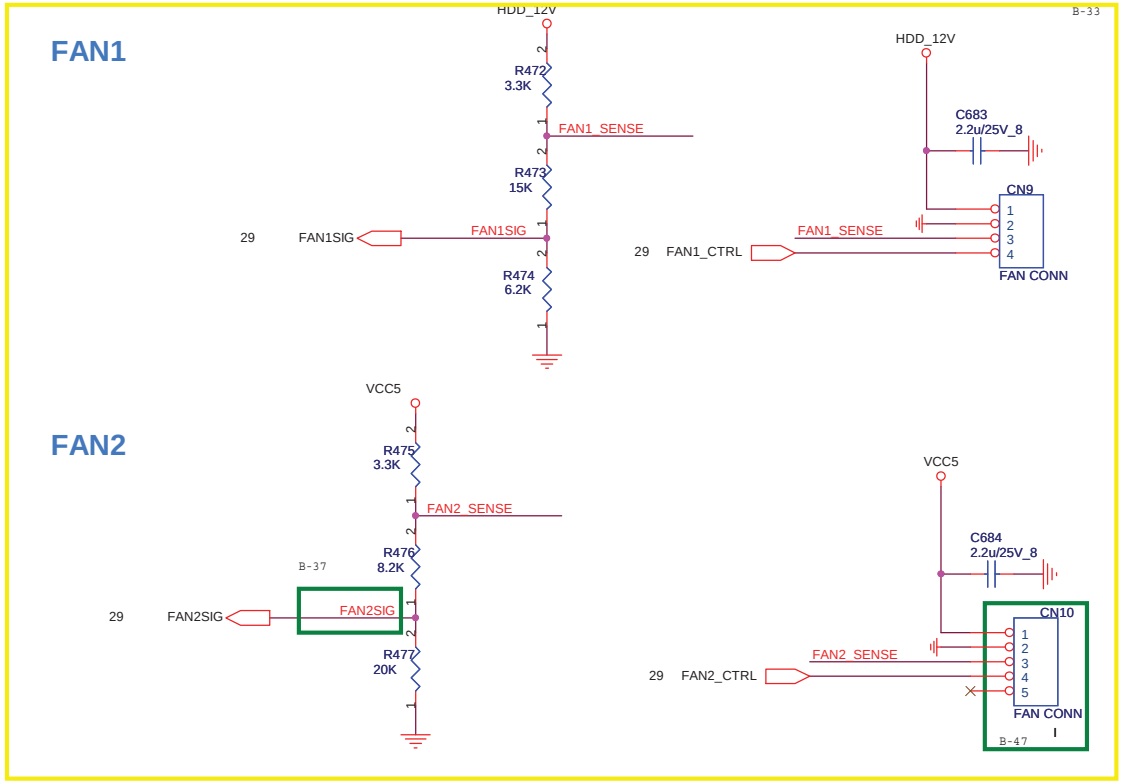

Quanta Computer Inc.

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Size	Document Number	Rev
	FAN/Thermal Protection	1A

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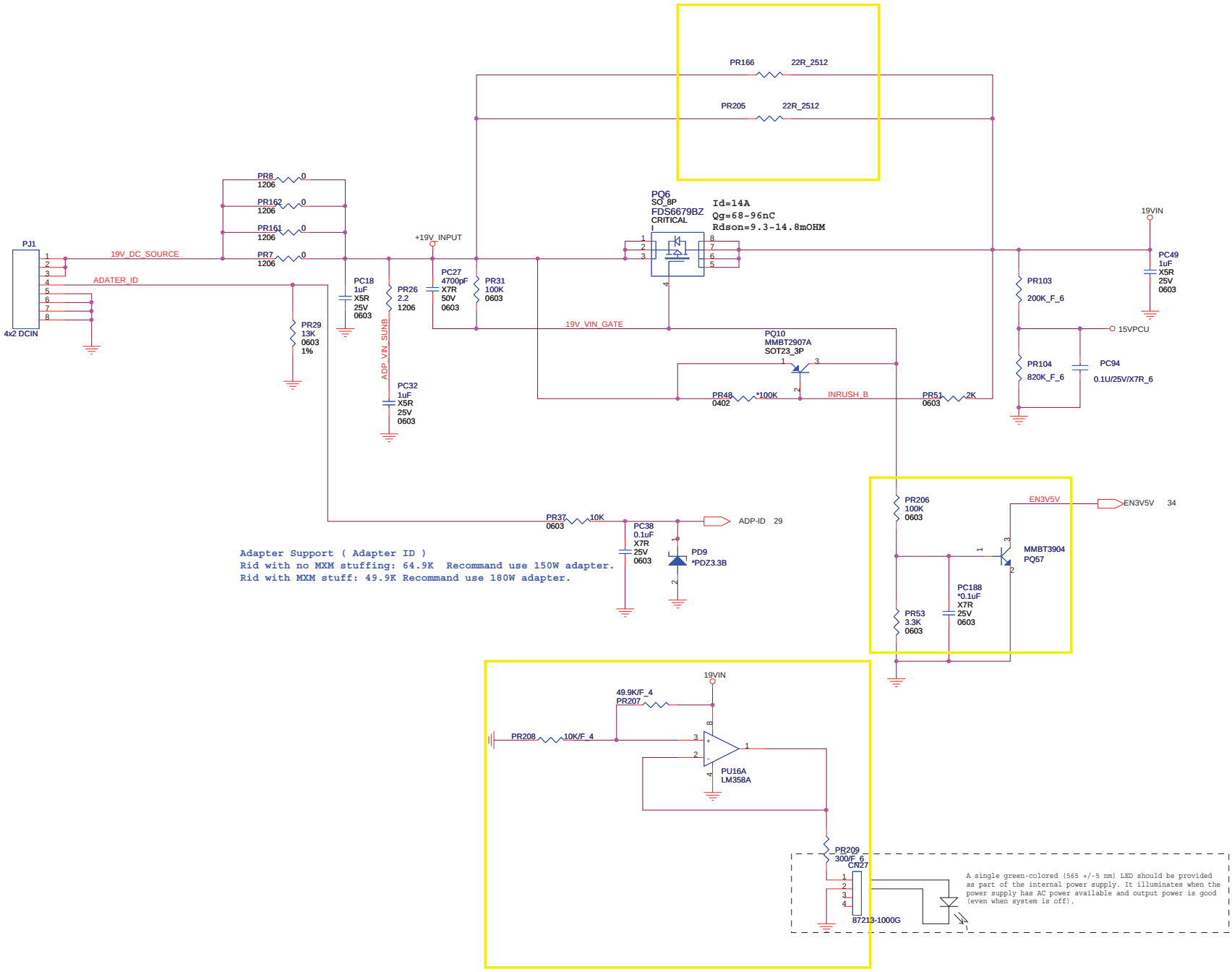

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Size	Document Number	Rev
	ACIN	1A

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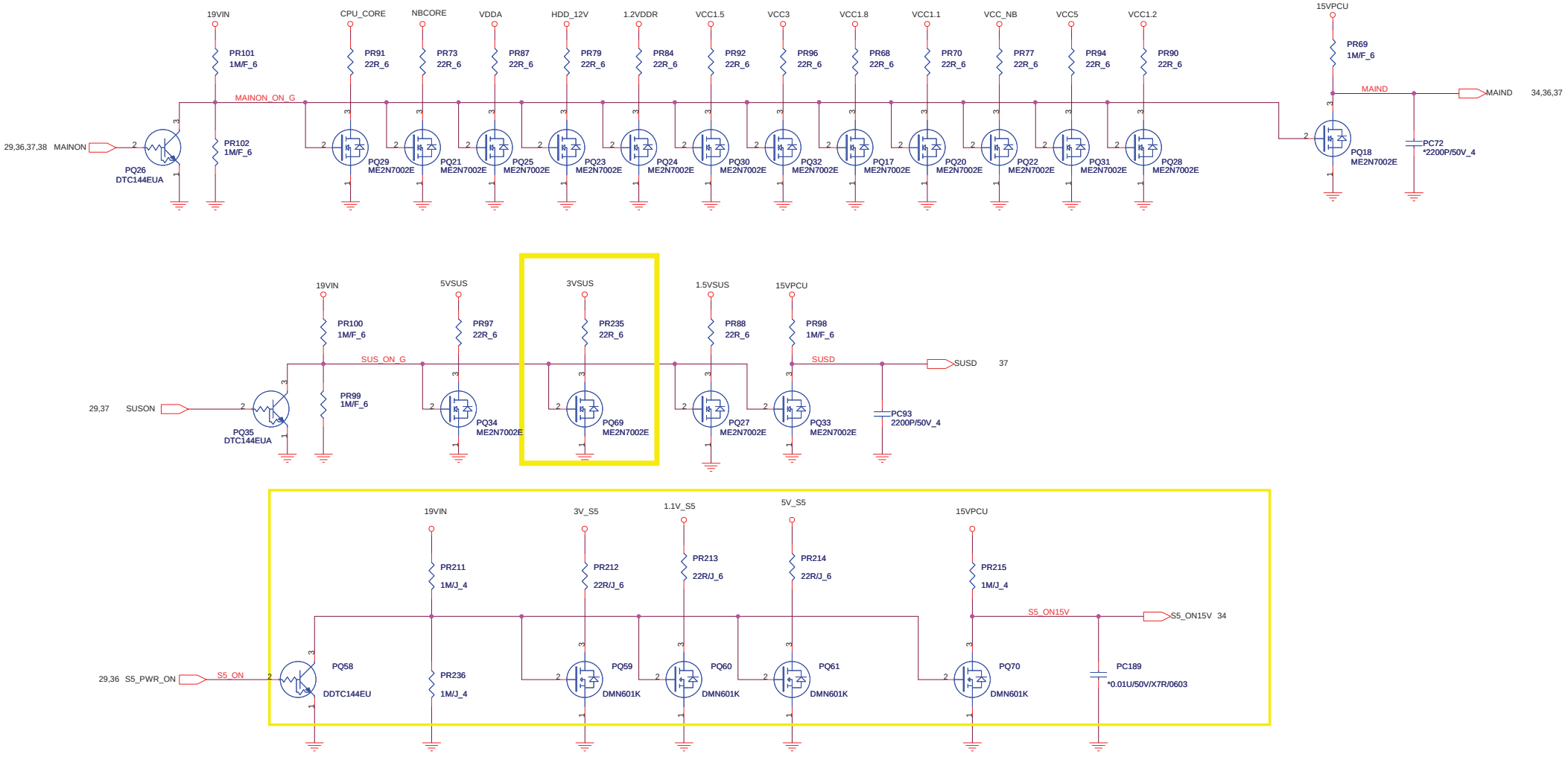

Quanta Computer Inc.

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	DISCHG & MOS SW	1A

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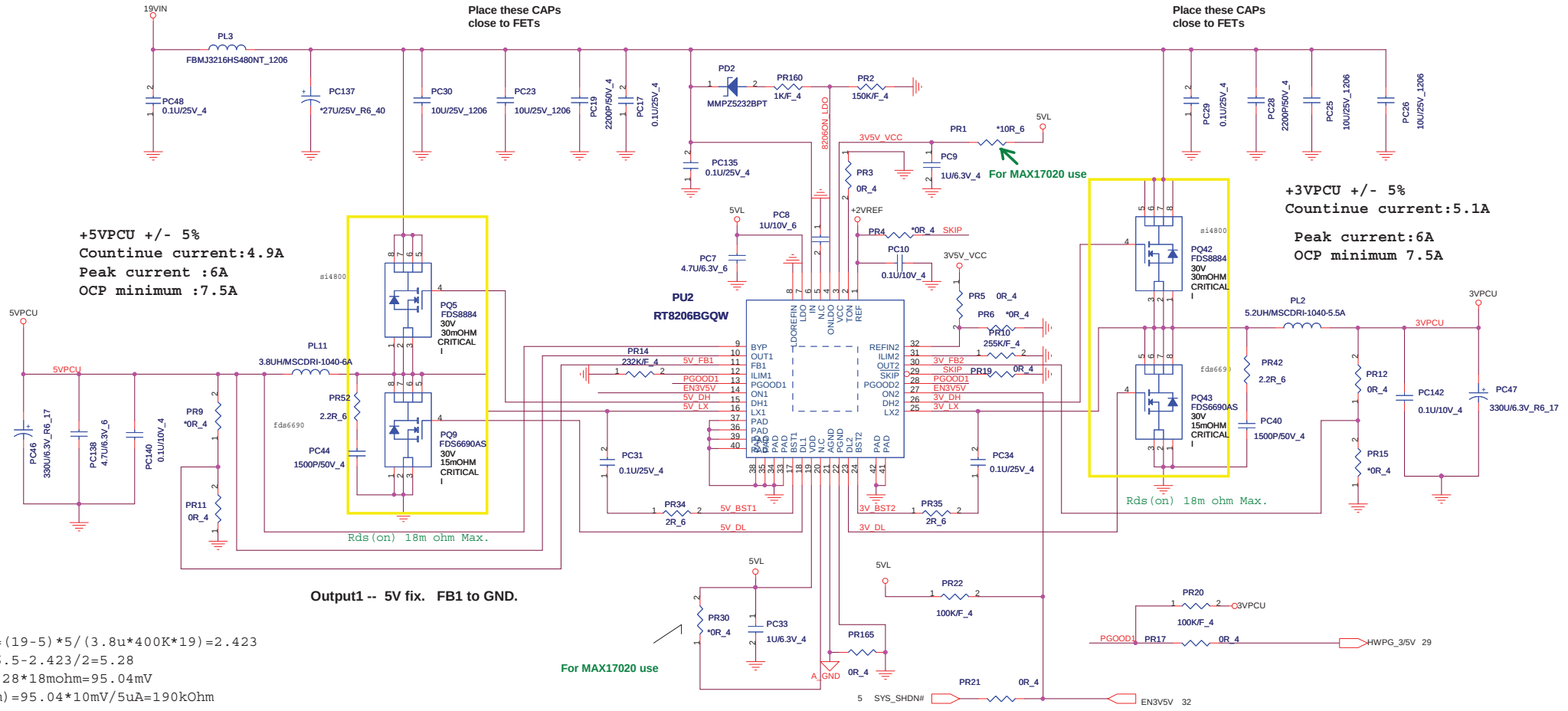
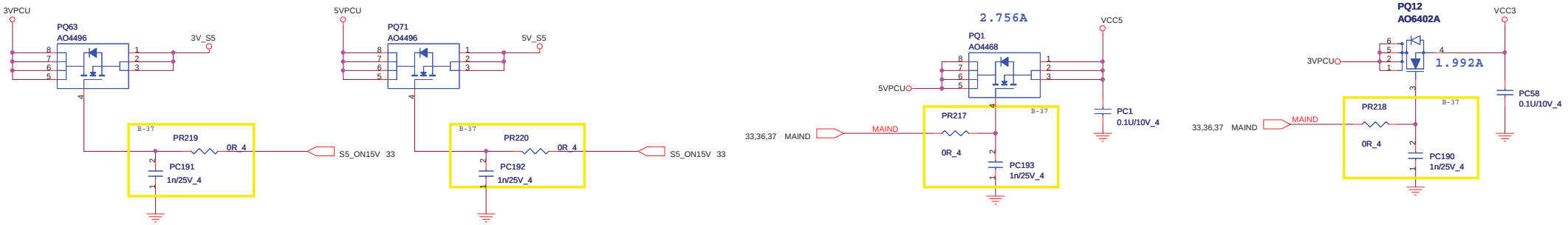
DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW



del I=(19-5)*5/(3.8u*400K*19)=2.423
Iocp=6.5-2.423/2=5.28
Vth=5.28*18mohm=95.04mV
R(Ilim)=95.04*10mV/5uA=190kOhm



ZN8_POWER-3V/5V

Design common circuit for ,
RT8206B or Max17020 or TPS51427

Quanta Computer Inc.
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	+5V/+3V (RT8206B)	1A
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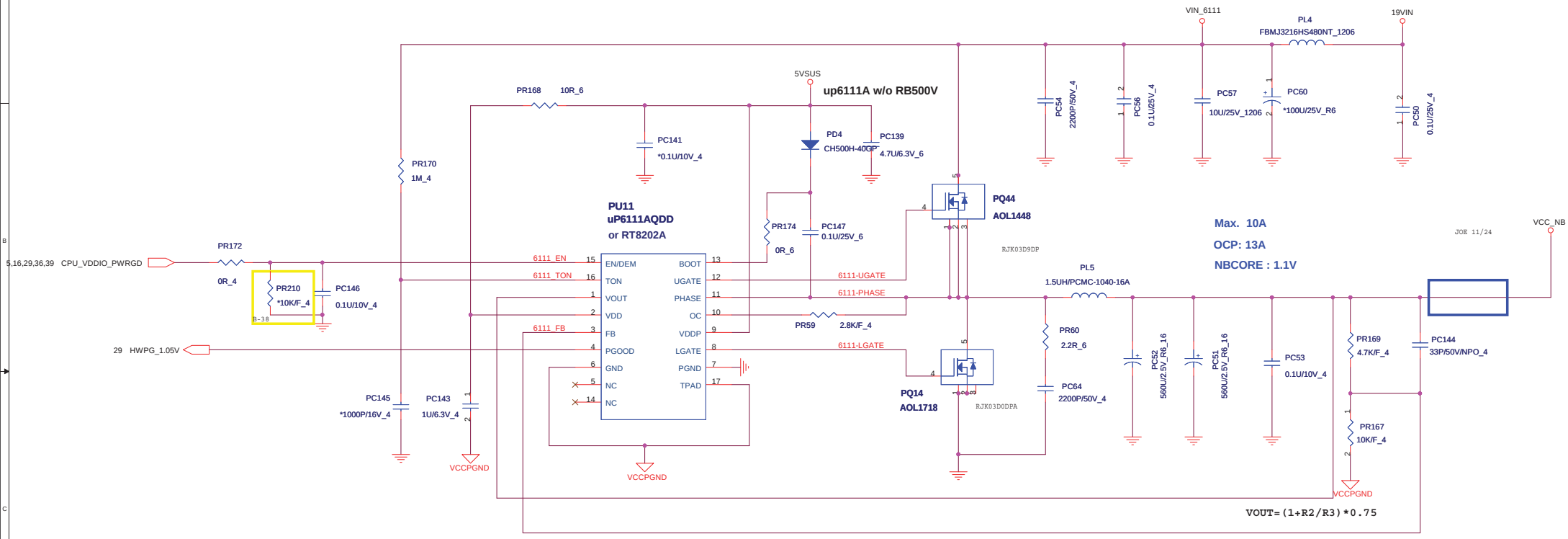
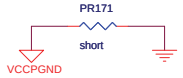


TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)



AO4712 Rds=4.3m Ohm Max./4.5V

Rds * OCP = RILIM * 20uA

13A OCP --- R_OC = 2.8K

Quanta Computer Inc.		
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Size	Document Number: NBCORE_1.1V(uP6111)	Rev: 1A
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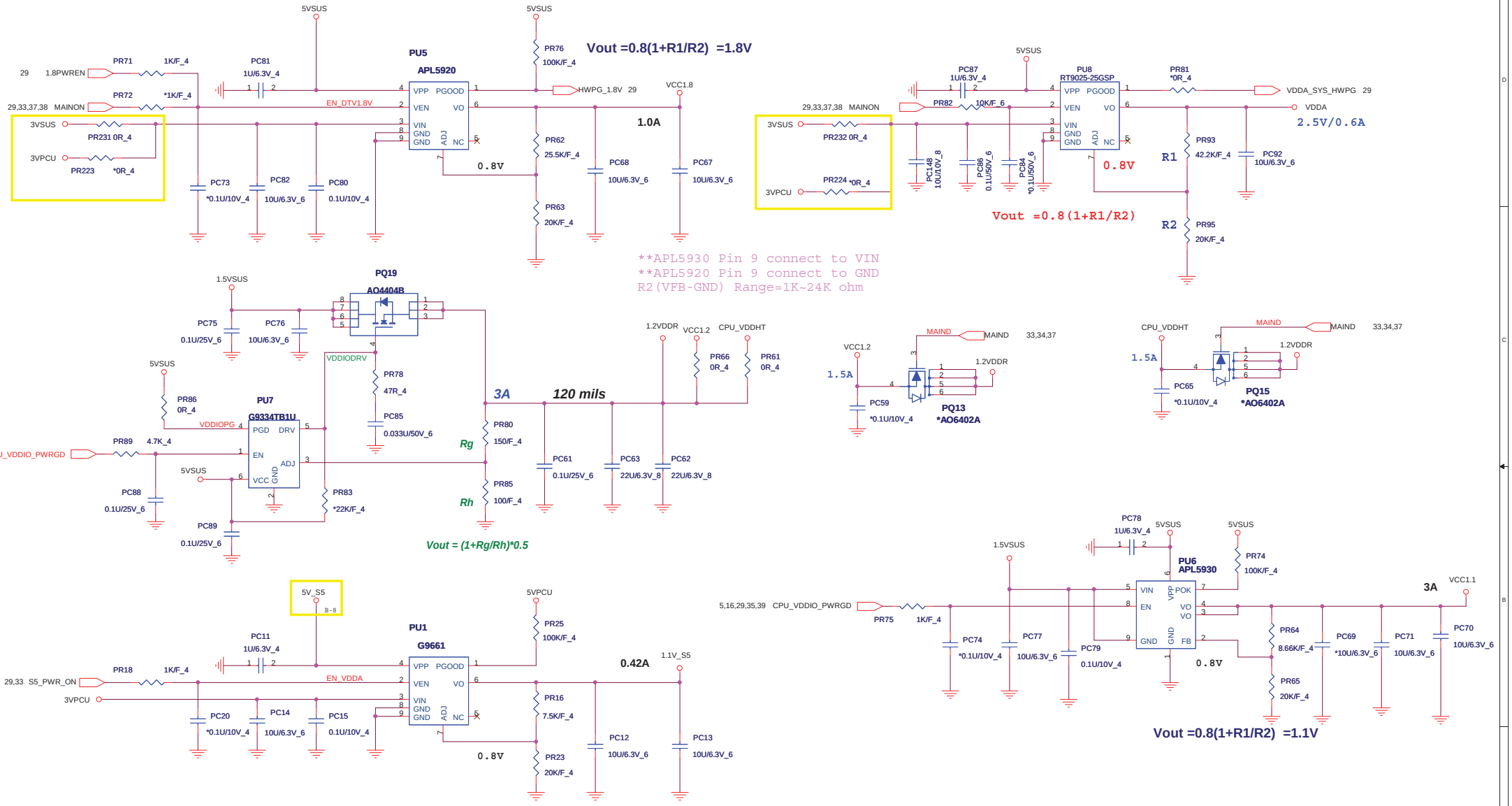
VCC1.1V, 1.2VDDR, VCC1.8V,VDDA,1.1V_S5



Quanta Computer Inc.		
PROJECT : ZN8		
Size	Document Number: VCC1.1,VDD1.8,2.5V(LDO)	Rev: 1A
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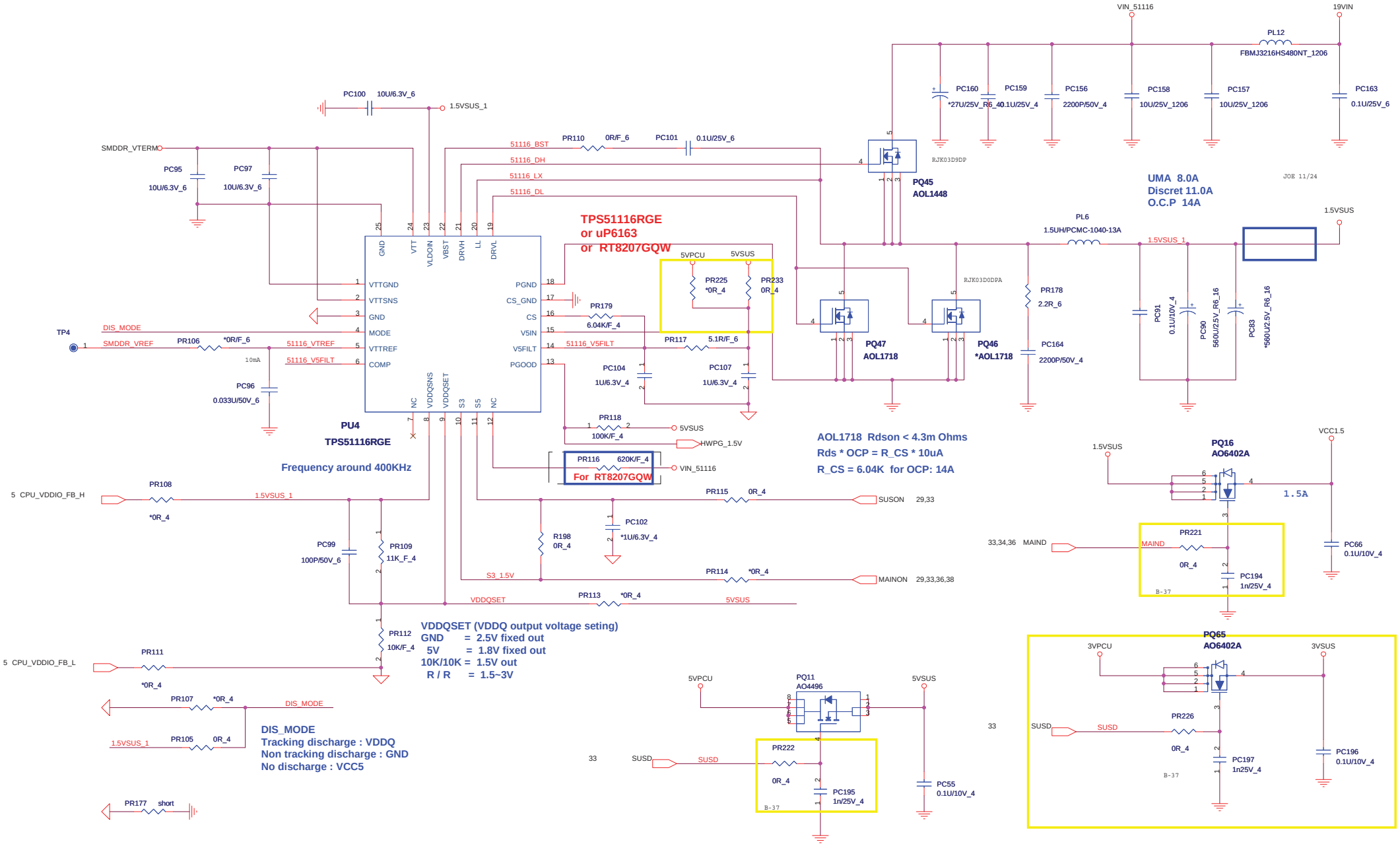
DDRIII-- 1.5VSUS



Quanta Computer Inc.		
PROJECT : ZN8		
Size	Document Number	Rev
	DDR(TPS51116)	1A
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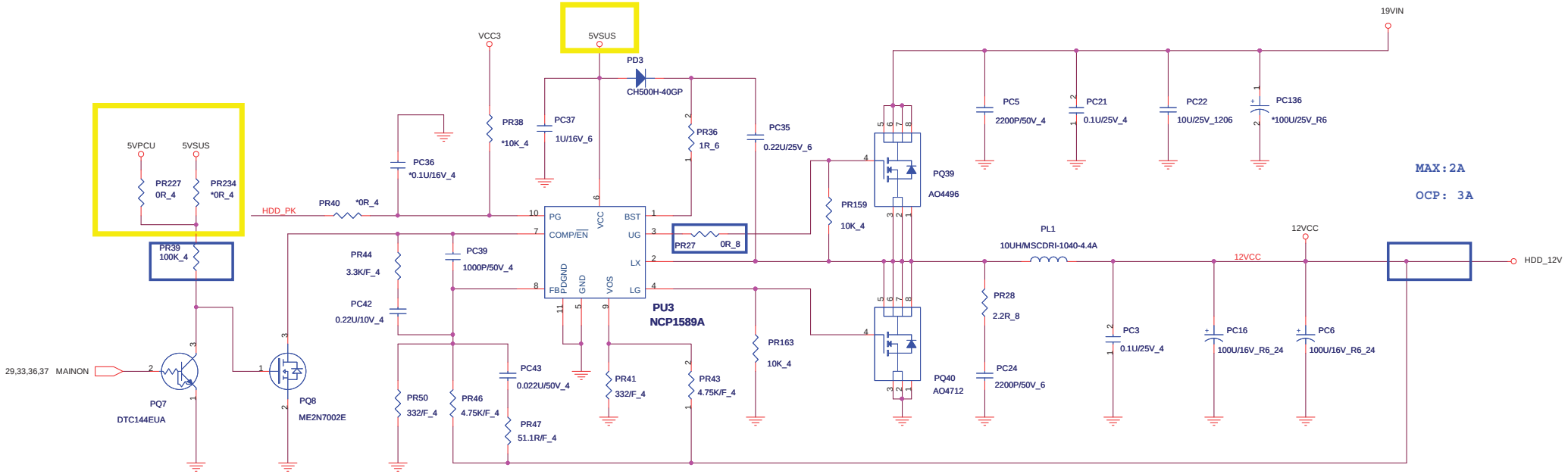

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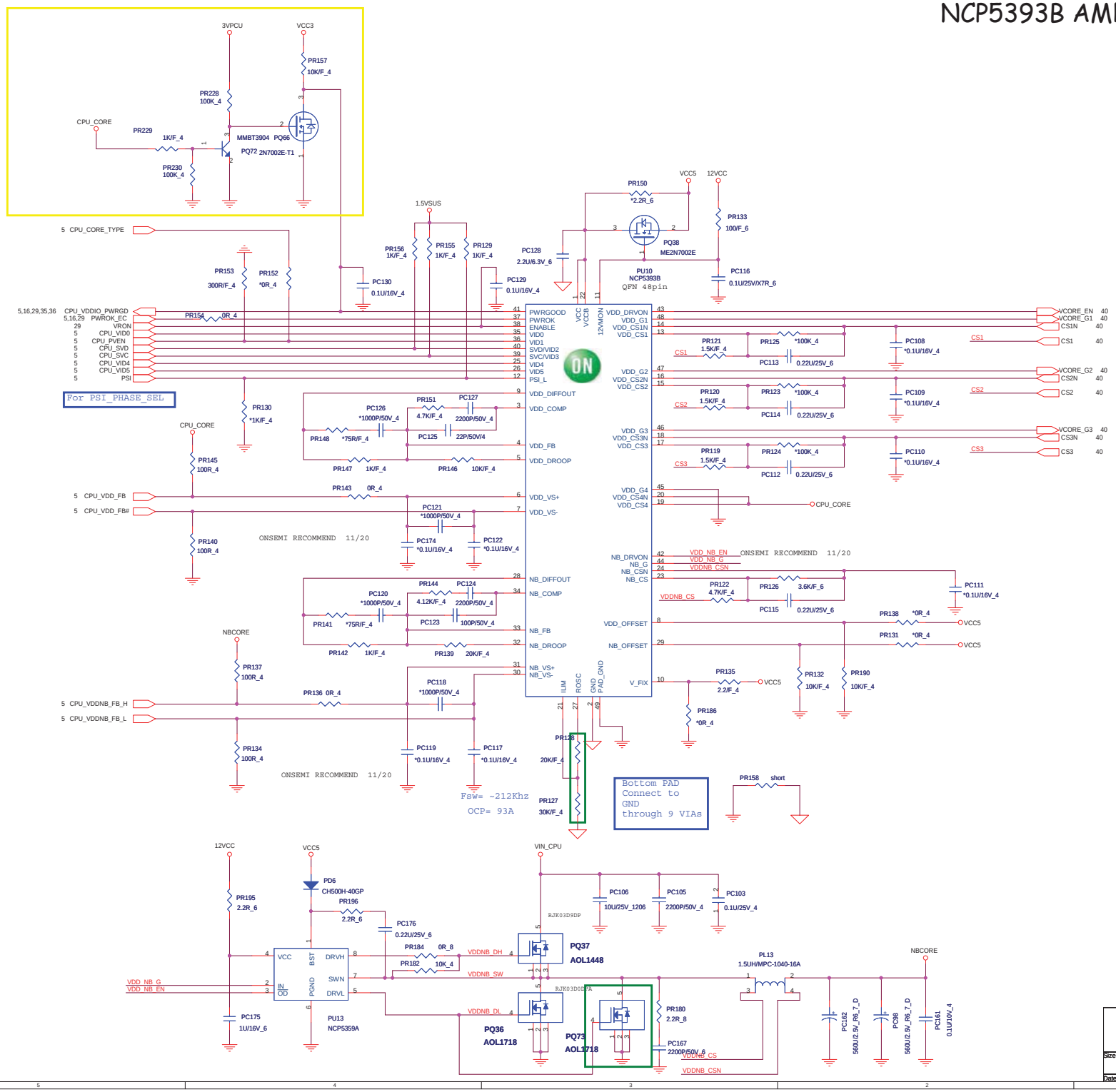
NCP5393B AMD AM3 POWER CKT



Quanta Computer Inc.

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Size	Document Number	Rev
	AMD AM3 CPUCORE(NCP5293)	1A
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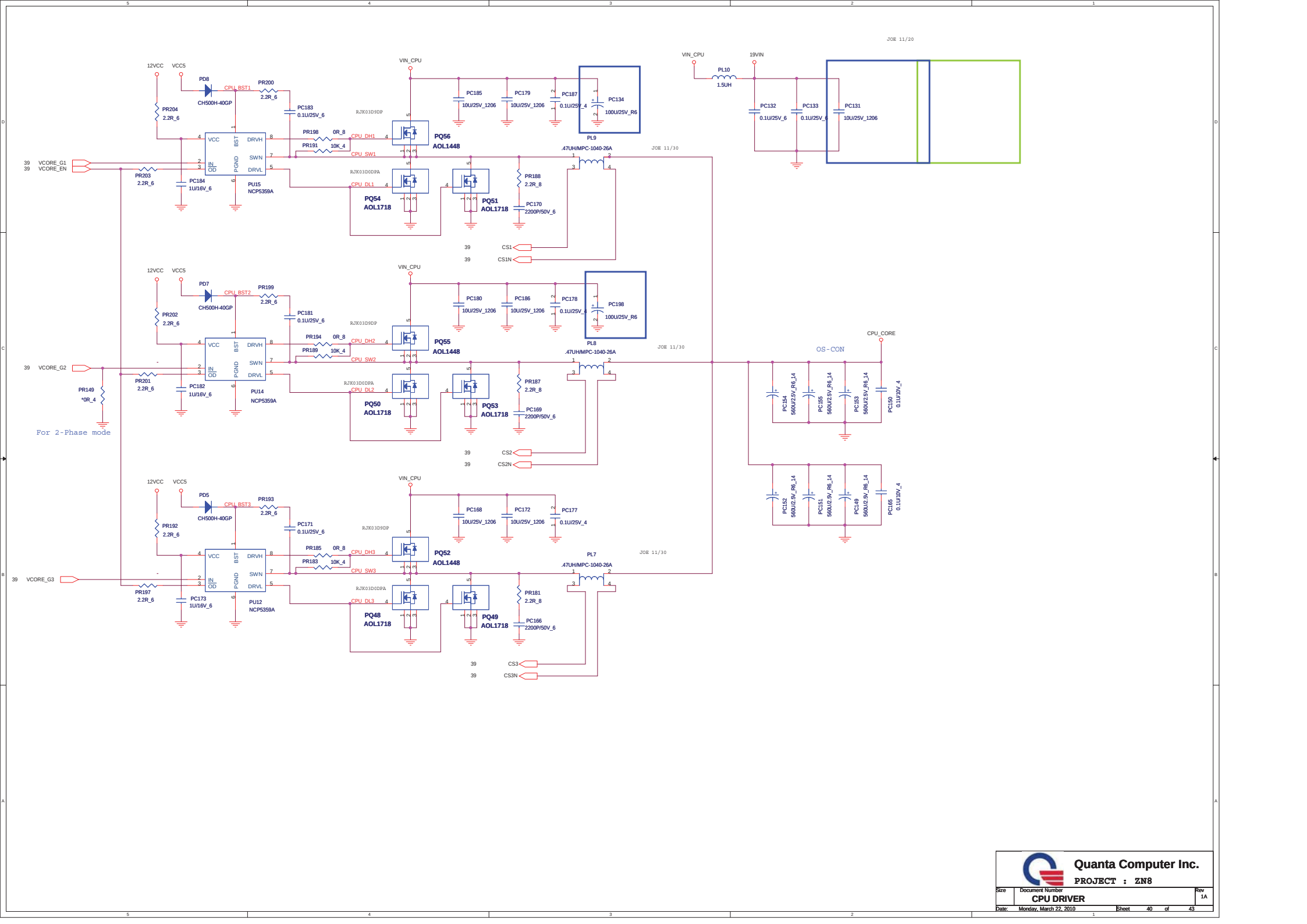

Quanta Computer Inc.

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Size	Document Number	Rev
	CPU DRIVER	1A

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CODEC

92HD89D3

IC AUDIO CODEC 92HD89D3

Analog / Digital

Near sense pin

12/8 AC90/AC93 change to 0ohms by IDT demanded

2/3 AC17/AC19 from 1u to 10u solved the THD issue.

2/3 AC20/AC21 from 1u to 100u solved the THD issue.

AC19/AC21 place near AU7 Pin9

2/3 AC14/AC16/AC18 from 1u to 10u solved the THD issue.

2/3 AC22/AC23 from 1u to 100u solved the THD issue.

AC92/AC23 place near AU7 Pin1,3

12/8. AR59 need move close to the MIC by IDT demanded

12/8 resistors change to null by IDT demanded

VOUT = 1.25 (1+R1/R2)

R1 R2

4.8375V 28.7K 10K

2nd source : G923-330T1U

AL000923003

12/8. AU3 current too small, when use we need to find other by IDT demanded

AC17 should near AU2

AC12 should near AU1

Place near AU4

11/30. change net name HPL and HPR to HPL1 and HPR1

BUZZER

BZ1 3.6V 90DB 8.5*8.5MM DNGJ4B20001

MMBT3904 40V 0.2A

LINE IN/Mic Reserved Jack

11/25 cancel BAT54C*2 by IDT demanded

Normal Close

SIE 2SJ-8960-001

HeadPhone/Mic Combo Jack

11/25 add filter by IDT demanded

2/3 change 22ohm to 16ohm for meet 2Vrms output.

11/25 value change from 100P to 0.01u by IDT demanded

MUTE Check

EC 29 EC_AMP_MUTE# AQ2 RB500V-40 AR15 47K_F4 AMP_MUTE# 42

PCH CODEC_RST PCH_AZ_CODEC_RST# AD1 RB500V-40

AC97 AUDIO SCHEMATIC (AFTER PLUG IN)

AC97 AUDIO SCHEMATIC (BEFORE PLUG IN)

Quanta Computer Inc.			
PROJECT : ZN8			
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	HD Audio Codec(92HD89D3)		A
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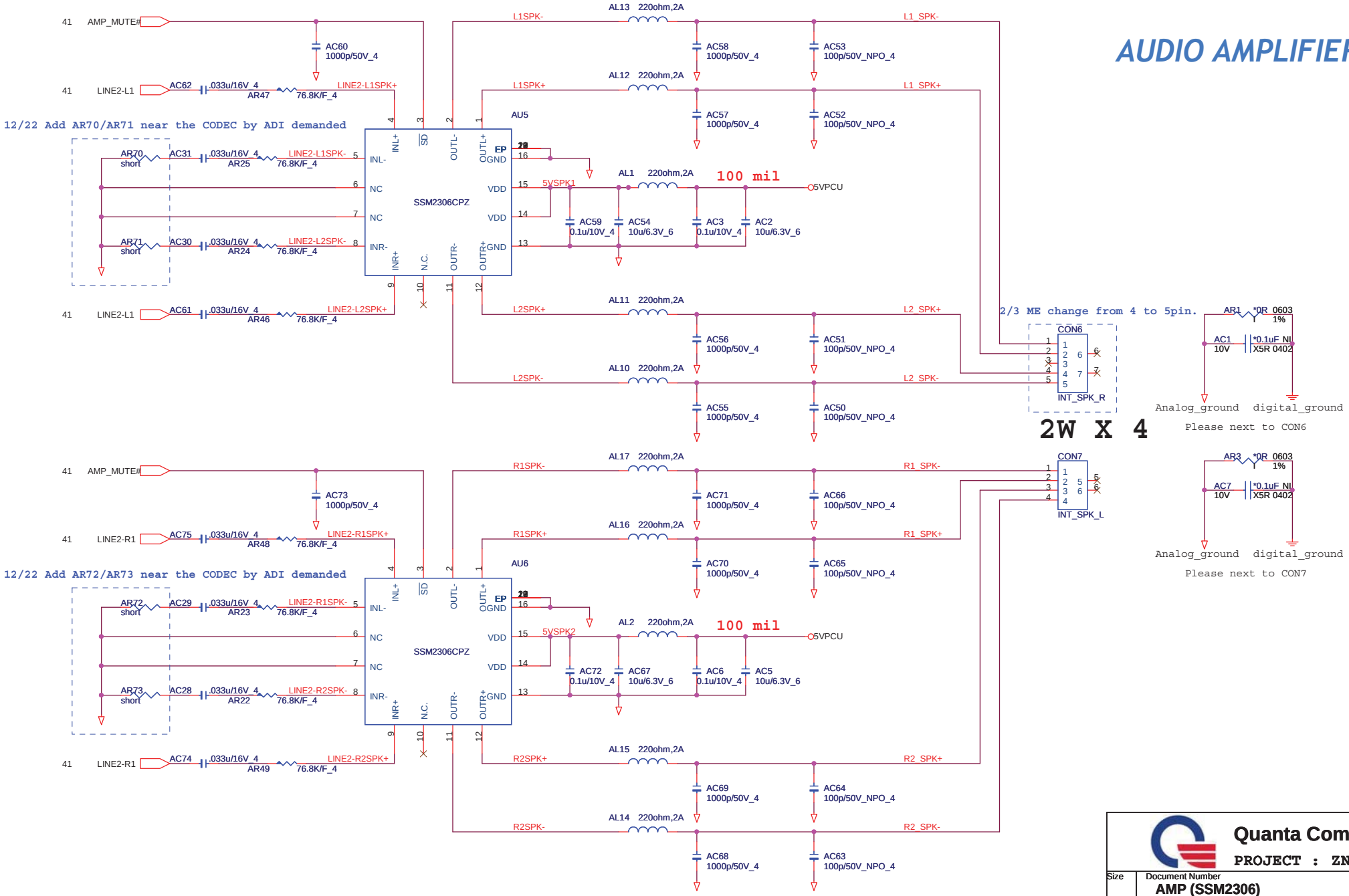
AUDIO AMPLIFIER



Quanta Computer Inc.		
PROJECT : ZN8		
Size	Document Number: AMP (SSM2306)	Rev: 1A
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0-1 : CLK source change to CLK GEN from SB
0-2 : Change resistor footprint type
0-3 : Remove resistor for CLK GEN source
0-4 : Linking for EDID read
0-5 : For LAN and USB3.0 PCIE signal
0-6 : For EDID writing control
0-7 : Change CLK source from SB to CLK GEN
0-8 : Separate system 5% power from 3VPCU
0-9 : Mount R80 and D5 for M2N control
0-10 : Change SB strap setting
0-11 : Correct DIMM setting
0-12 : Linking for EDID read
0-13 : Correct 19V power rail net name
0-14 : Correct PCIE_RST% SB connection
0-15 : Change CRT connector type
0-16 : Change VGA connector type
0-17 : Change mini PCIE controller form NB to SB
0-18 : Change mini PCIE controller form NB to SB
0-19 : Add capacitor for noise filtration
0-20 : Separate DMIC and camera connector
0-21 : Correct scalar board reset signal
0-22 : Modify panel EDID read / write function
0-23 : Modify display port AUX channel connection
0-24 : Add panel power 12V/5V switch function
0-25 : Correct 19V power rail net name
0-26 : Panel power 12V/5V power selection
0-27 : Link KP smp I2C to EC for GAIN control
0-28 : PWM driving for FAN control
0-29 : CPU_CORE PWRD assertion for EC
0-30 : Adjust I/O port pin define
0-31 : Change CIR connector type
0-32 : Correct DIMM thermal detect function
0-33 : Modify FAN circuit for 12V FAN
0-34: CLK_SRSRCP_PB / CLK_SRSRCN_PB link to CLK GEN SRSRC_CLK_R / SRSRC_CLK#_R
0-35: Change R173,R175 to 150 ohm from 4.7K
0-36: De-pop R111,R159
0-37: Fix FAN net name issue
0-38: Fix DDR dongle issue
0-39: Change MXM SB from prot B to port C
0-40: Add MXM 3.0
0-41:Change USB power to VSUS
0-42: Change PCIEx1 Lane to fix Lan issue
0-43: Modified Panel power circuit
0-44: Change CN19(MT) from 4pin to 5pin
0-45: Change CON2, CON3 pin definition
0-46: Reserve PU Res. for IR con pin4.
0-47: Change FAN2(CN13) from 4pin to 5pin
0-48: Connector PCIE_WAKE to IO_RD for WOL
0-49: Remove CN11 Logo light# circuit
0-50: Change DL SMBUS from main to resume
0-51: De-pop R144,R149
0-52: Change D4 to D28,D29
0-53: Add DDR SUSB3TS EC delay circuit
0-54: Reserve SB_SPI for debug
0-55: Change MT touch power to 5VSUS
0-56: Change scalar EC conn. power.
0-57: Disable SB EC strap
0-58: De-pop R479 to fix scalar RD reset issue
0-59: Change carder connector type(CN12)
0-60: isolate power btn from CN4 to CON8
0-61: Change R19,R20 to 4.7k and de-pop R12,R48 for RTD issue
0-62: Add EVCC1 power control circuit
0-63: Add re-driver IC for PCIE LAN and USB3.0
0-64: Add CN39 for vol+/vol-/mute function
0-65: Add CN38 for D-SENSOR
0-66: Add NB_PWRGD control circuit for spike issue

PAGE 32

1.del DCIN1 · PR176 · PR175 · PR173 · PR24 · PQ4 · PQ2 · PR32 · PR24 · PR49 · PD1 · PC41 · PR33 · PR164 · CR1 · PR13 · PQ41 · PQ3 · PR55 · PR56 · PC45 · PR54 · PR45 · PR57 · PC4 · PC2

2 - ADD PR206/100kohm · PC188/0.1uF · PQ57/MMBT3904 · PR207/49.9kohm · PR37/10kohm · PU16A/LM358 · PR166/22ohm · PD9/PDZ3.3B · PR209/300ohm

3 - change PR29 FROM 64.9k ohm TO 13kohm

PAGE 35

1 - change PR172 FROM 1k ohm TO 0 ohm

2 - ADD PR7/10kohm · PC51/560uF/2.5V

PAGE 36

1 - change PU8 VEN FROM CPU_VDDIO_PWRGD TO MAINON

PAGE 37

1 - change VCC1.5V TO VCC1.5

2 - add pq65, pr226,pc197,pc196 for 3vsus

PAGE 39

1 - change PU10 PWRGOOD FROM CPU_CORE TO VCC3

2 - add mosfet in VDDNB

3 - add pr229,pr230,pr228,pr157,pq67,p166 for pwrgood

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