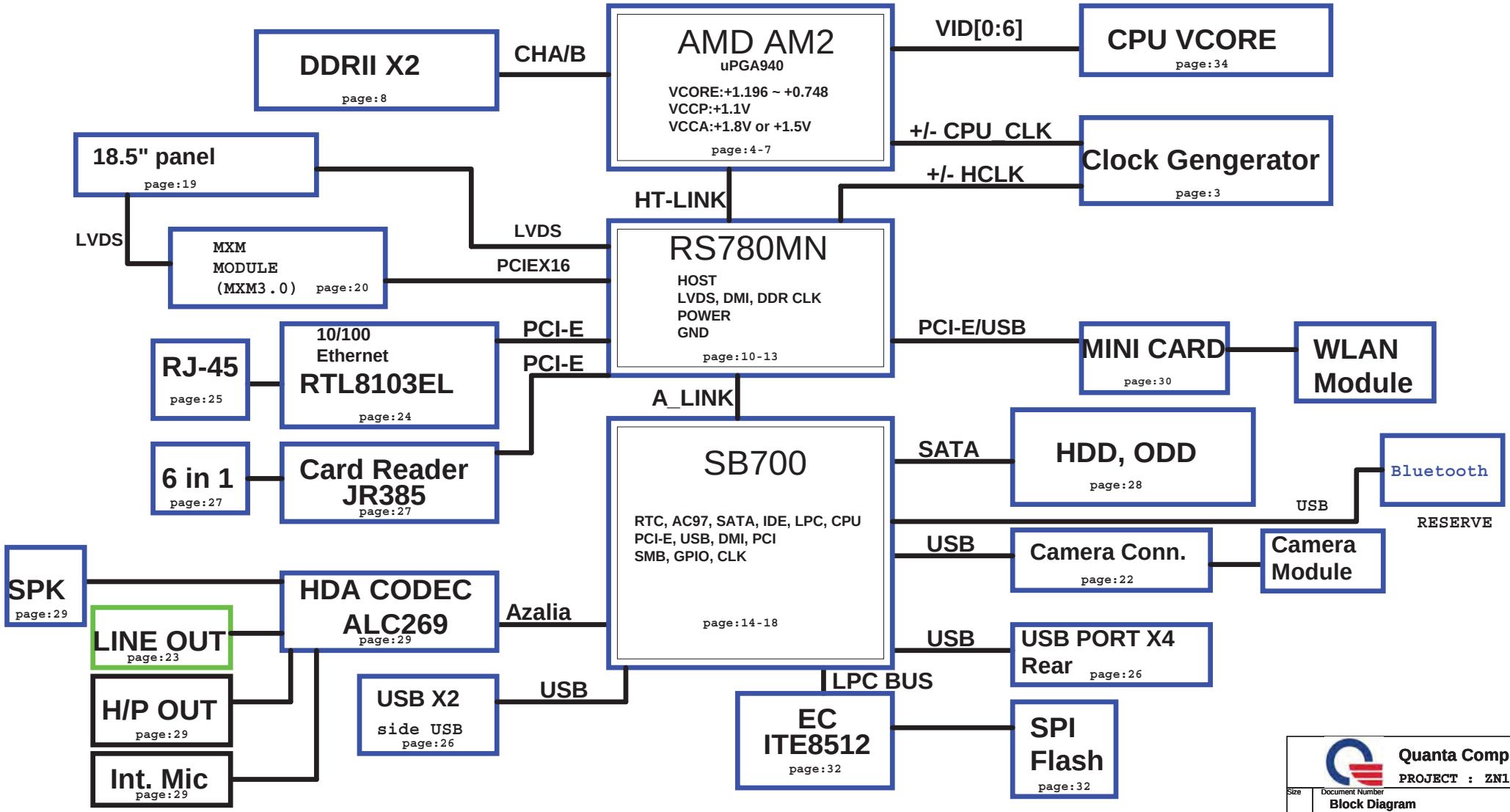
Amazon LCD PC Block Diagram

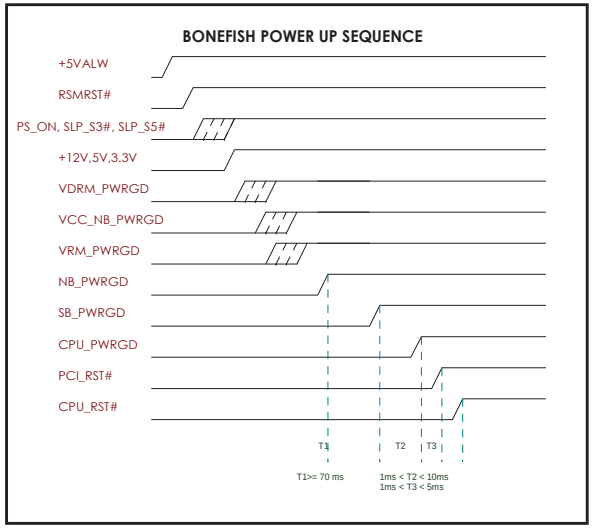


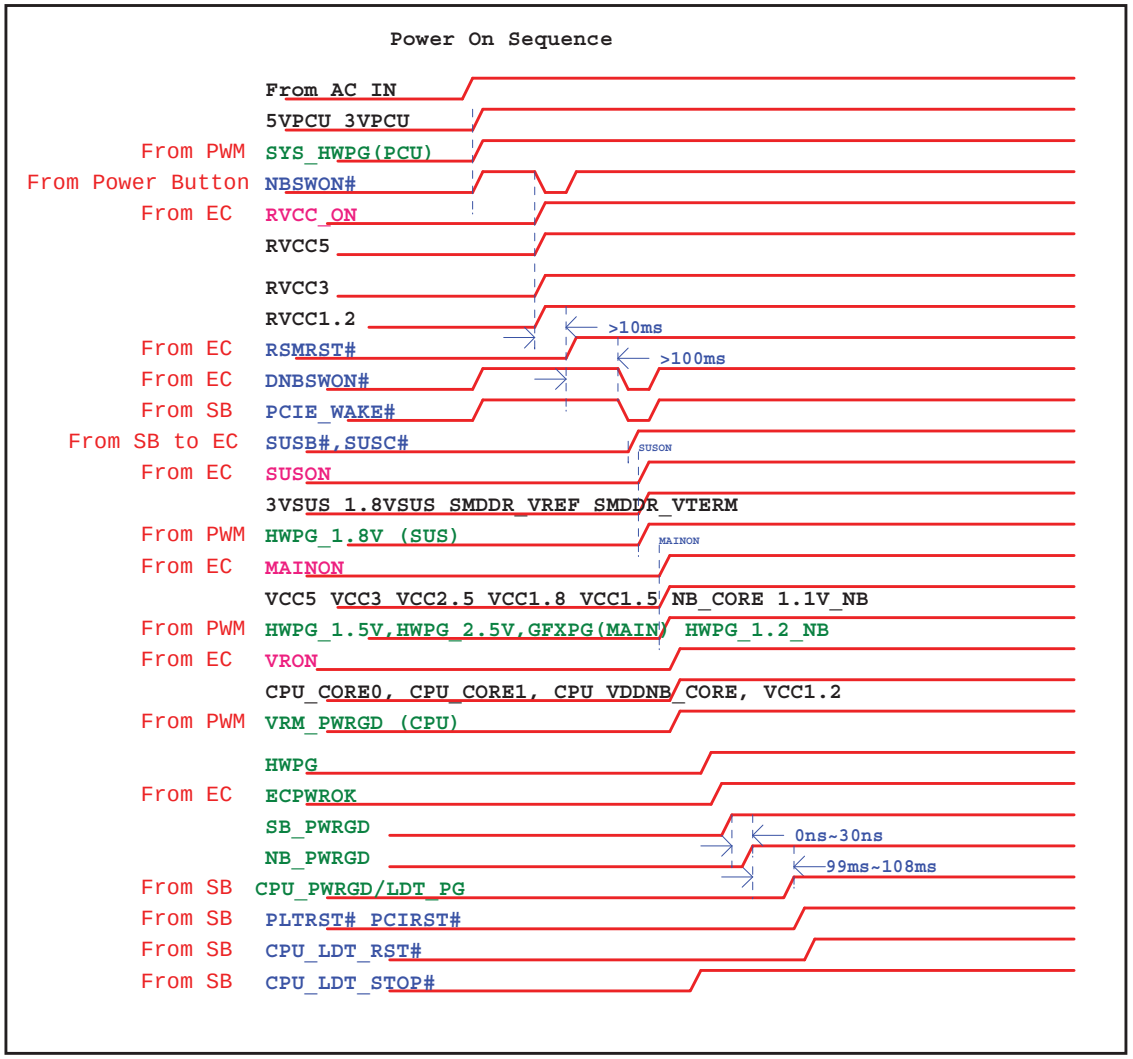
PCB STACK UP

LAYER 1 : TOP
LAYER 2 : VCC
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : GND
LAYER 6 : BOT

Voltage Rails

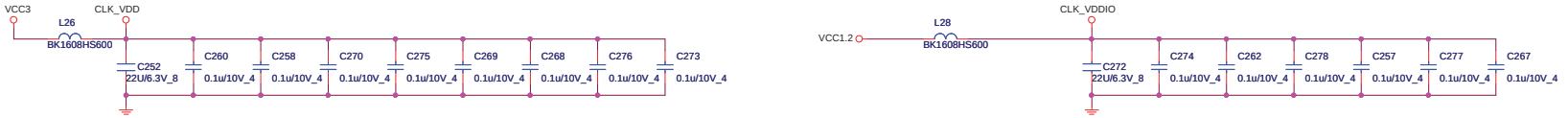
Power	Voltage	S0~S2	S3	S4	S5	Ctl Signal
15VPCU	15V	V	V	V	V	
5VPCU	5V	V	V	V	V	VIN
3VPCU	3V	V	V	V	V	VIN
RVCC3	3V	V	V	V	V	RVCC_ON
RVCC1.2	1.2V	V	V	V	V	RVCC_ON
5VSUS	5V	V	V			SUSD
1.8VSUS	1.8V	V	V			SUSON
VCC5	5V	V				MAIND
VCC3	3V	V				MAIND
VCC1.8	1.8V	V				MAIND
VCC1.5	1.5V	V				MAINON
VCC1.2	1.2V	V				MAINON
CPU_VDDA	2.5V	V				VCC3
NB_CORE	1.2V	V				VRON
SMDDR_VTERM	0.9V	V				SUSON
CPU_CORE	By CPU	V				VR_ON





Quanta Computer Inc.
PROJECT : ZN1
Size | Document Number: SYSTEM INFORMATION | Rev B
Date: Friday, May 08, 2009 | Sheet 2 of 41

CLK_GEN_SLG8SP628



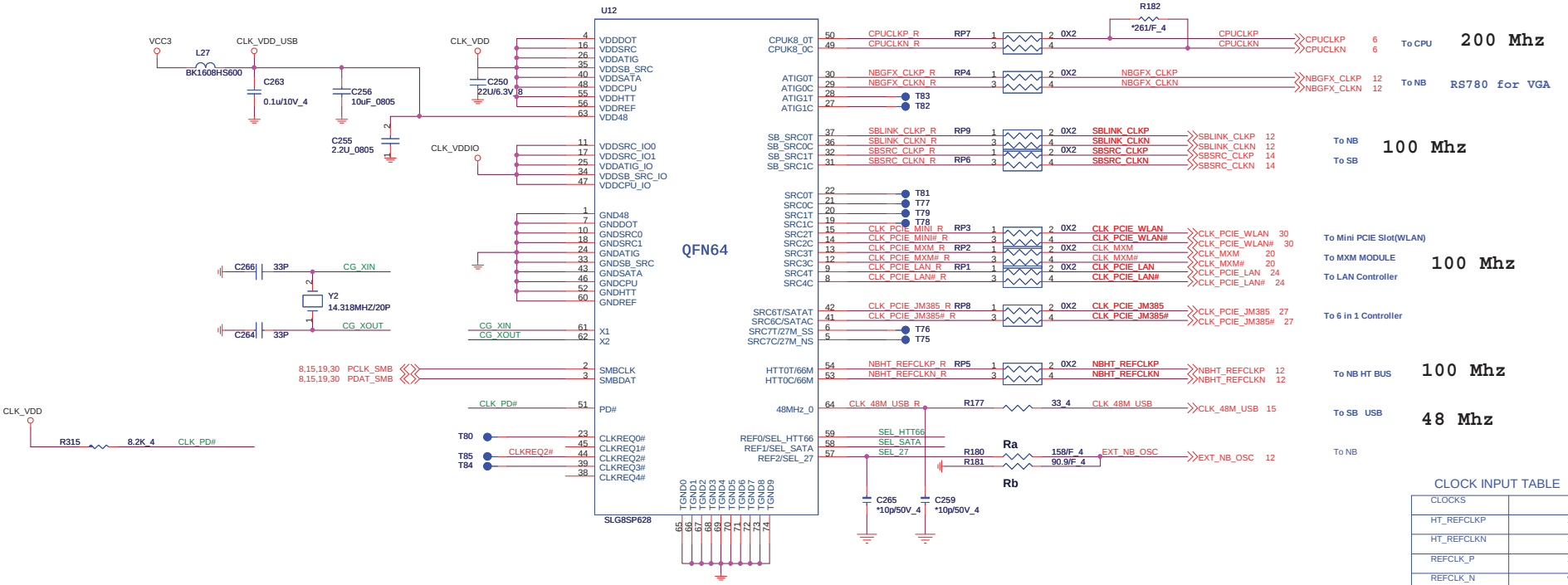
Clock chip has internal serial terminations for differencial pairs, external resistors are reserved for debug purpose.

Place within 0.5" of CLKGEN

ICS9LPRS480 P/N : ALPRS480000

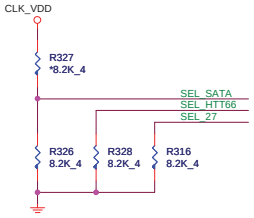
SLG8SP628 P/N : AL8SP628000

RTM880N-796 P/N : AL000880000



CLOCK INPUT TABLE

CLOCKS	RS780
HT_REFCLKP	100M DIFF
HT_REFCLKN	100M DIFF
REFCLK_P	14M SE (1.1V)
REFCLK_N	vref
GFX_REFCLK	100M DIFF(IN/OUT)*
GPP_REFCLK	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF



SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1*	100 MHz non-spreading differential SRC clock
	0	100 MHz spreading differential SRC clock
SEL_27	1	27MHz and 27M SS outputs
	0*	100 MHz SRC clock

* default

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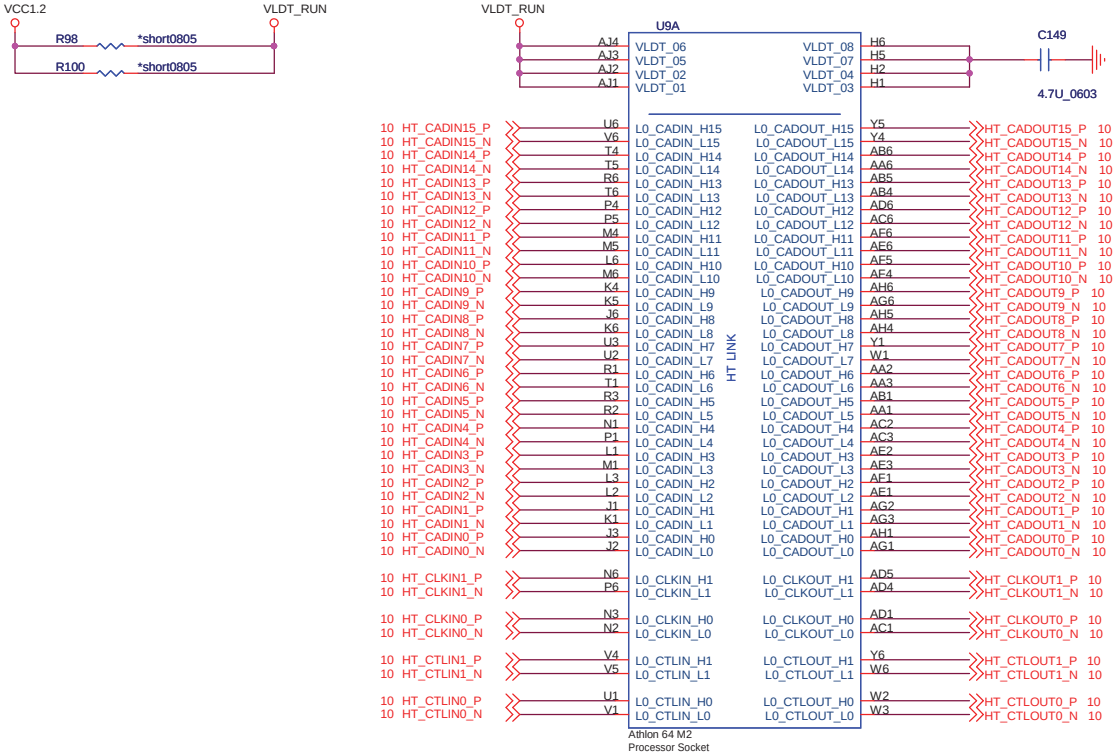
PROJECT : ZN1

Size	Document Number	Rev
	Clock Generator	1A

Date: Friday, May 08, 2009 Sheet 3 of 41

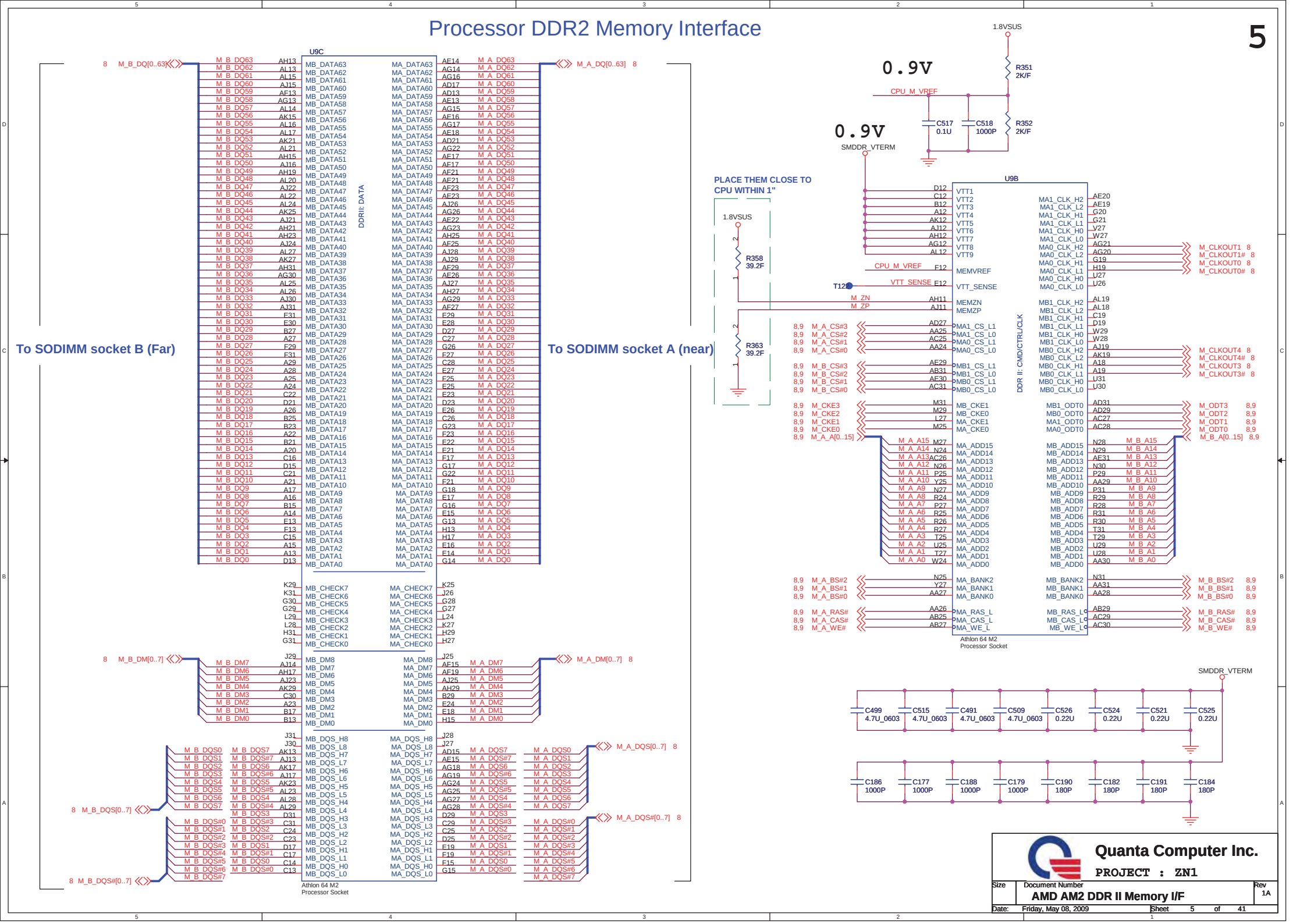
CPU HyperTransport Interface

VDDLDTRUNCPU is connected to the VDD_LDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.



Quanta Computer Inc.		
PROJECT : ZN1		
Size	Document Number: AMD AM2 HT I/F	Rev: 1A
Date: Friday, May 08, 2009	Sheet 4 of 41	

Processor DDR2 Memory Interface



Quanta Computer Inc.		
PROJECT : ZN1		
Size	Document Number: AMD AM2 DDR II Memory I/F	Rev: 1A
Date: Friday, May 08, 2009	Sheet 5 of 41	

Add component to BOM
Vender suggest

6

ATHLON Control and Debug

HDT Connector

CPU Thermal Senser

2.5V

Vout =1.25(1+R1/R2)
= 1.25 (1+20K/20K)
= 2.5V

If AMD SI is not used, the SID pin can be left unconnected and SIC should have a 300-Ω (±5%) pulldown to VSS.

close to CPU

place them to CPU within 1"

PLACE IT CLOSE TO CPU WITHIN 1"
ROUTE AS 80 Ohm DIFFERENTIAL PAIR

PSI_L is a Power Status Indicator signal. This signal is asserted when the processor is in a low powerstate. PSI_L should be connected to the power supply controller, if the controller supports "skipmode, or diode emulation mode". PSI_L is asserted by the processor during the C3 and S1 states.

AMD NPT M2 SOCKET
Processor Socket

*HDT CONN

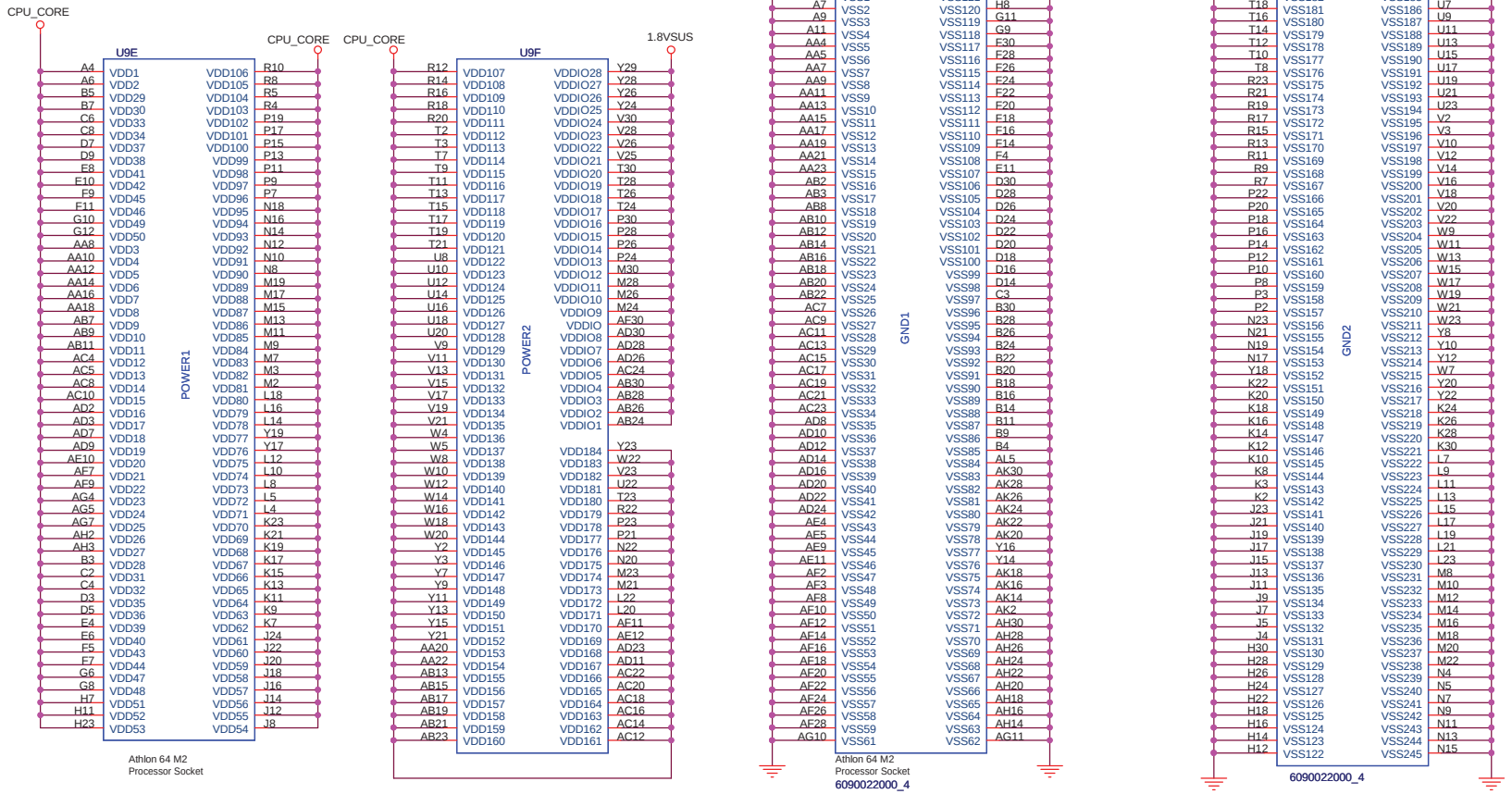
sub-address:9Ah

SMBUS SLAVE ADDRESS	
G781	98 (CPU)

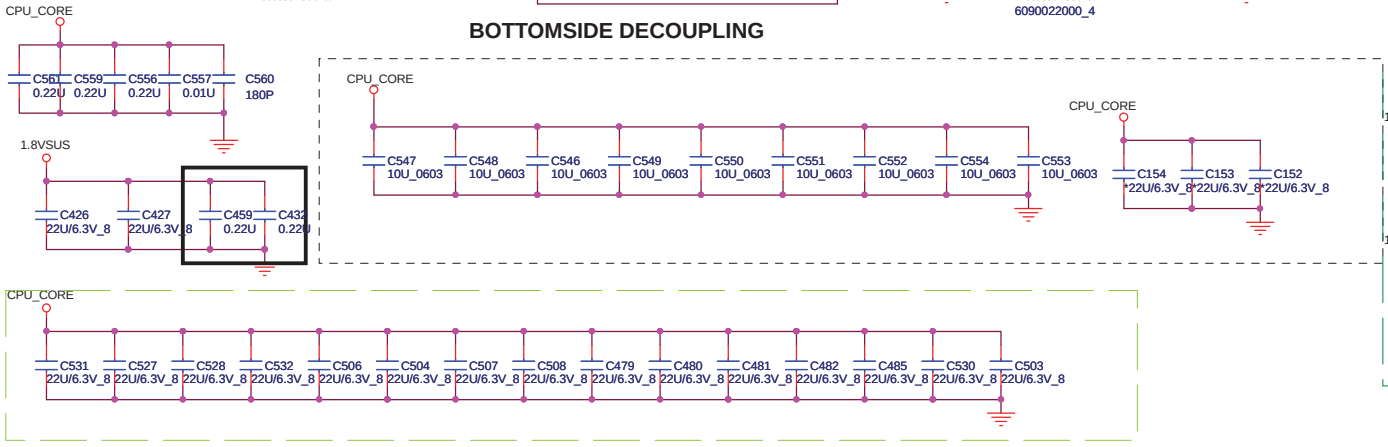
Quanta Computer Inc.
PROJECT : ZN1

Size	Document Number	Rev
	AMD AM2 CTRL & DEBUG	1A
Date: Friday, May 08, 2009	Sheet 6 of 41	

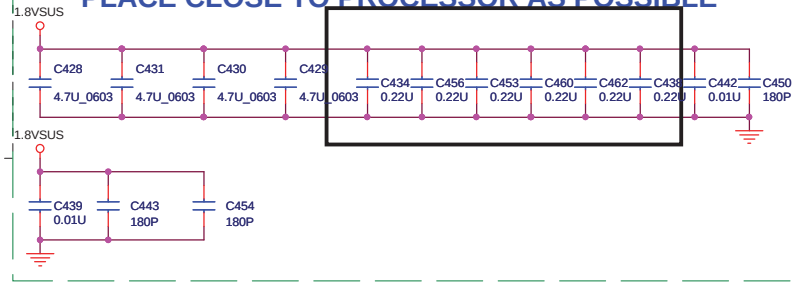
PROCESSOR POWER AND GROUND



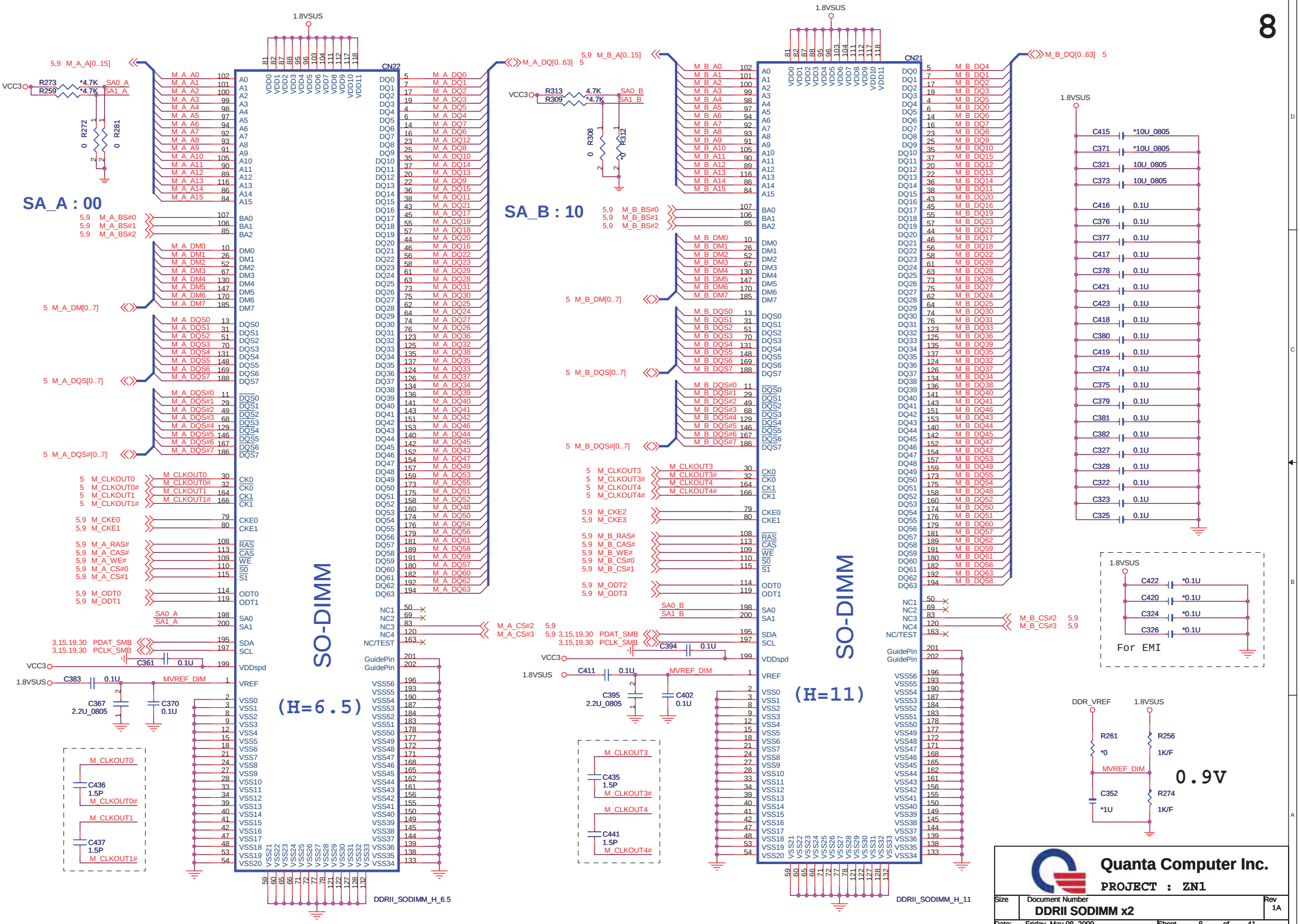
BOTTOMSIDE DECOUPLING



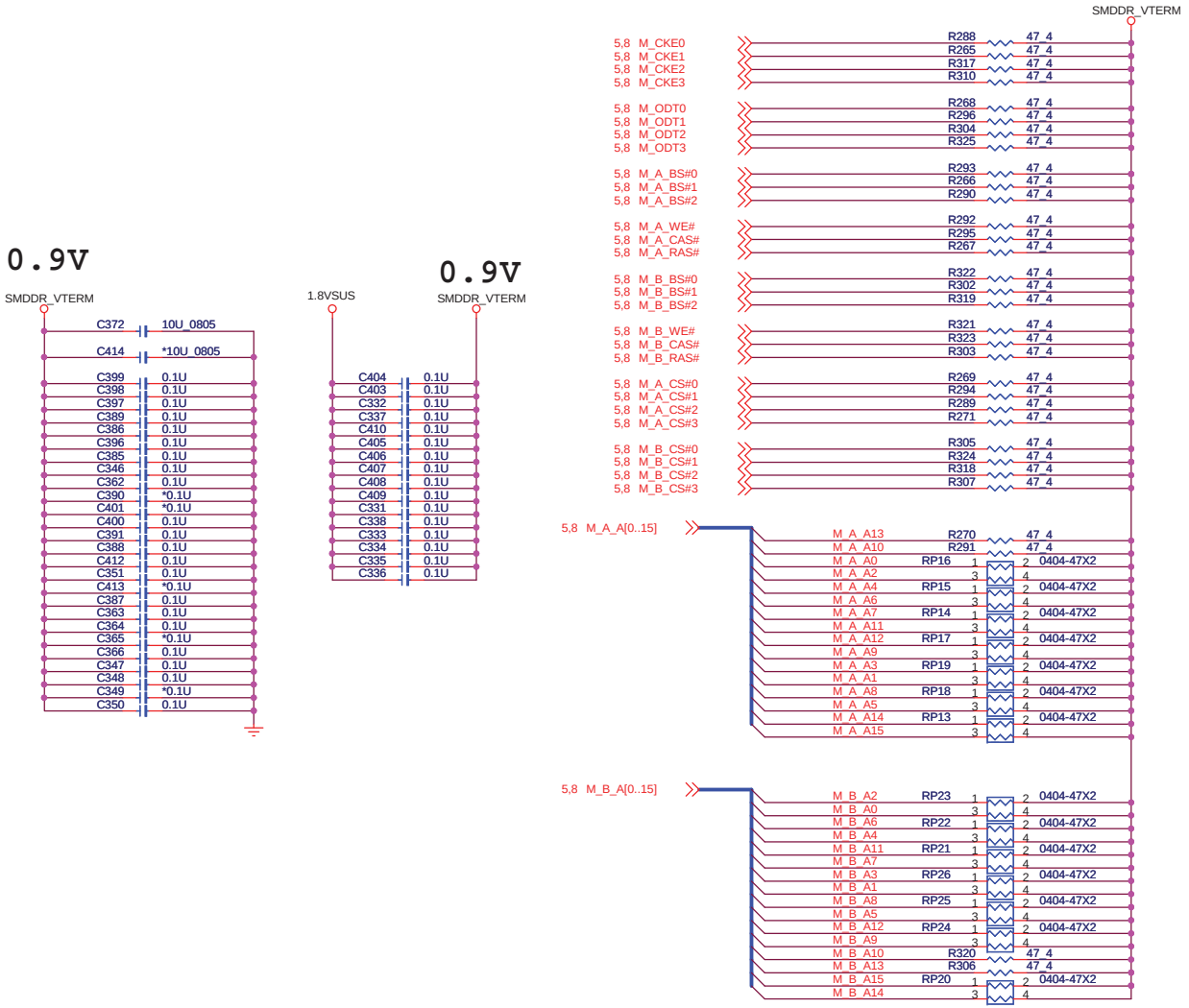
DECOUPLING BETWEEN PROCESSOR AND DIMMs
PLACE CLOSE TO PROCESSOR AS POSSIBLE



Quanta Computer Inc.		
PROJECT : ZN1		
Size	Document Number: AMD AM2 PWR & GND	Rev: 1A
Date: Friday, May 08, 2009	Sheet 7 of 41	



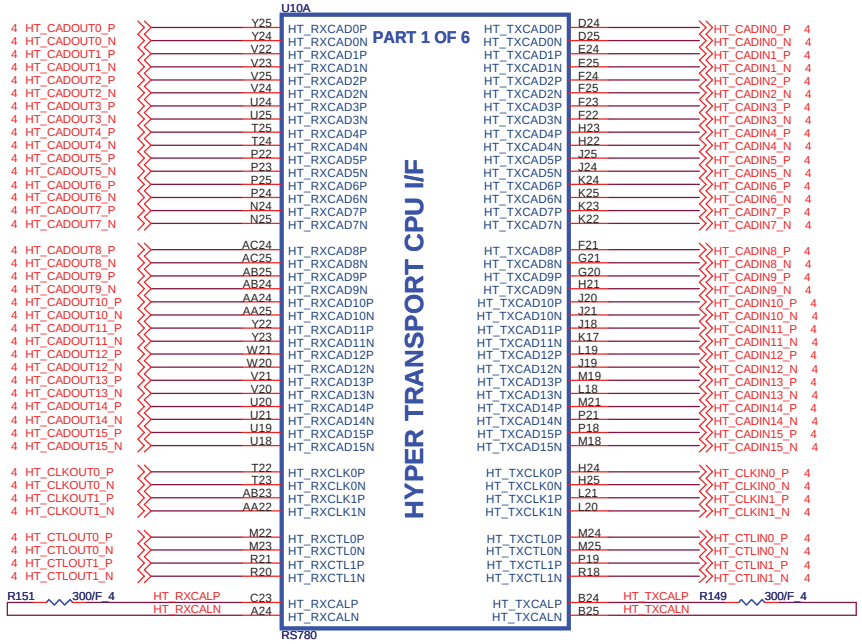
Quanta Computer Inc.		
PROJECT : ZN1		
Size	Document Number: DDRII SODIMM x2	Rev: 1A
Date: Friday, May 08, 2009	Sheet 8 of 41	



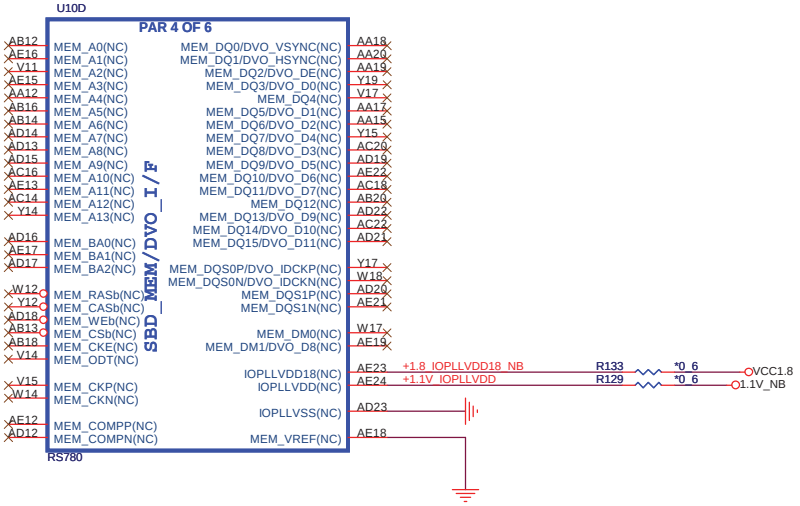
Quanta Computer Inc.

PROJECT : ZN1

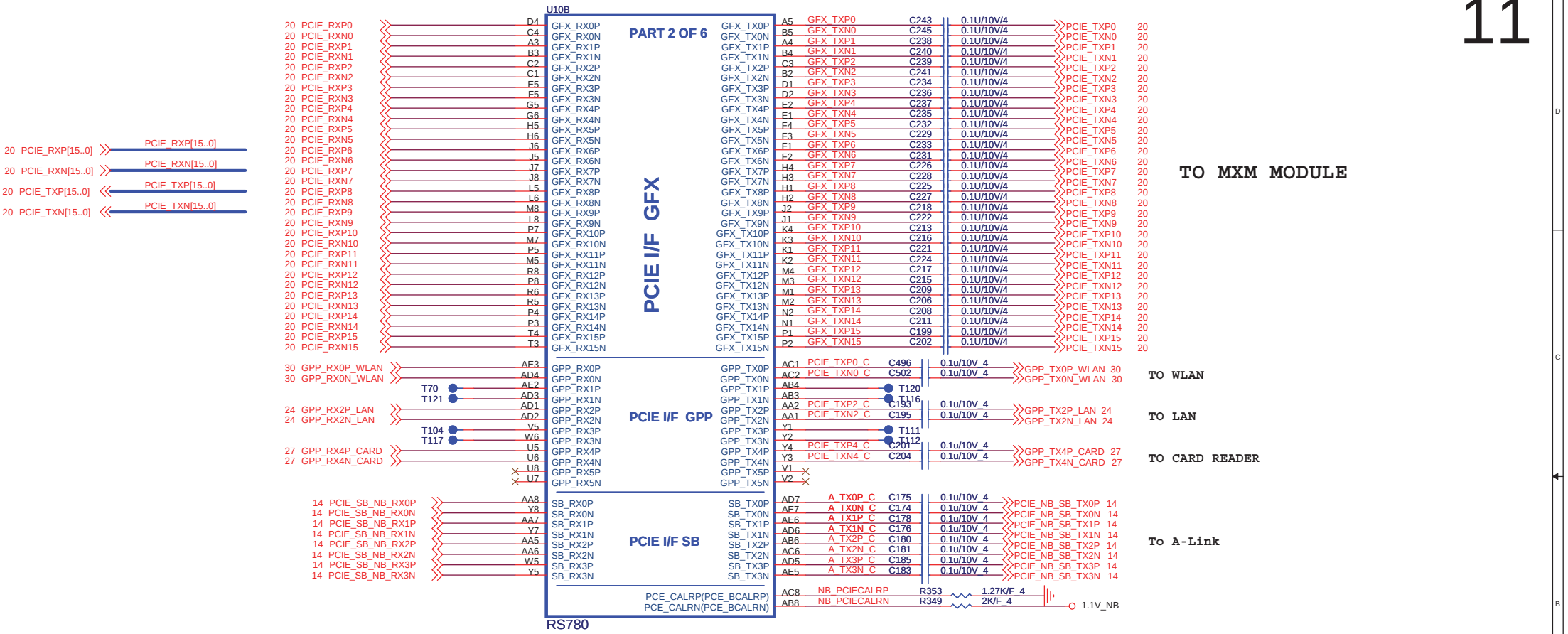
Size	Document Number	Rev
	DDRII TERMINATION	1A
Date: Friday, May 08, 2009	Sheet 9 of 41	



This block is for UMA RS780 only



Quanta Computer Inc.		
PROJECT : ZN1		
Size	Document Number: RS780M HT LINK I/F 1/4	Rev: 1A
Date: Friday, May 08, 2009	Sheet 10 of 41	


U10B
PART 2 OF 6
PCIE I/F GFX
PCIE I/F GPP
PCIE I/F SB
RS780
TO MXM MODULE
TO WLAN
TO LAN
TO CARD READER
To A-Link
PCE_CALRP(PCE_BCALRP)
PCE_CALRN(PCE_BCALRN)
1.1V_NB

Thermal Senser

SMBUS SLAVE ADDRESS	
G781	98 (NB)
G781-1	9A (CPU)

U7 G781 MSOP8-4_9-65 — SMBUS Add. : 98h

C165 0.1U_4 · C162 *0.1U · R128 0R_6 · C171 2200P_0603 · R_NB_THRMDA · R_NB_THRMDC · 6 NB_SHDN#1

MBCLK 6,32 · MBDATA 6,32 · NB_TALERT# 15

R449 1K/F_4

Change BOM value

RX780 / RS780 North Bridge RESET

6,14 CPU_LDT_RST# — R337 *0_4 — NB_RST#_IN

14 NB_PLTRST# — R336 0_4

18 NB_PWRGD_IN

14 ALLOW_LDTSTOP

3 NBHT_REFCLKP · 3 NBHT_REFCLKN

3 EXT_NB_OSC — R332 0_4 NB_REFCLK_P · R333 0_4 NB_REFCLK_N

1.1V_NB — R330 4.7K_4 RS780 R331 4.7K_4

3 NBGFX_CLKP · 3 NBGFX_CLKN

3 SBLINK_CLKP · 3 SBLINK_CLKN

19,20 LVDS_DAT · 19,20 LVDS_CLK

+NB_CORE_ON — R162 *10K/F_4 — VCC3 · R164 2.2K_4

CRT_RED · CRT_GRN · CRT_BLU — R205 150/F · R202 150/F · R197 140/F

RS780_AUX_CAL — R166 *3K_4

CRT_VSYNC — R160 3K_4 — VCC3 · R161 *3K_4

CRT_HSYNC — R159 3K_4 — VCC3 · R158 *3K_4

21 CRT_RED · 21 CRT_GRN · 21 CRT_BLU — R343 0_4 · R344 0_4 · R345 0_4

21 CRT_HSYNC · 21 CRT_VSYNC · 21 CRT_DDCDAT · 21 CRT_DDCCLK

R346 IV@715/F_6 — DAC_RSET_NB

T109 INT_TV_C/R · T118 · T114

T73 · T74 — RS740_DFT_GPIO1

+NB_CORE_ON

T72 — RS780_AUX_CAL

U10C — RS780 — PART 3 OF 6

CRT/TVOUT

AVDD1(NC) F12 · AVDD2(NC) F12 · AVDD3(NC) F14 · AVSSDI(NC) G15 · AVDDQ(NC) H15 · AVSSQ(NC) H14

C_Pr(DFT_GPIO5) F17 · Y(DFT_GPIO2) F17 · COMP_Pb(DFT_GPIO4) F15

RED(DFT_GPIO0) G18 · REDb(NC) G17 · GREEN(DFT_GPIO1) F18 · GREENb(NC) F18 · BLUE(DFT_GPIO3) E19 · BLUEb(NC) F19

DAC_HSYNC(PWM_GPIO4) A11 · DAC_VSYNC(PWM_GPIO6) B11 · DAC_SDA(PCE_TCALRN) E8 · DAC_SCL(PCE_RCALRN) F8

DAC_RSET(PWM_GPIO1) G14

TXOUT_L0P(NC) A22 · TXOUT_L0N(NC) B22 · TXOUT_L1P(NC) A21 · TXOUT_L1N(NC) B21 · TXOUT_L2P(NC) B20 · TXOUT_L2N(DBG_GPIO0) A20 · TXOUT_L3P(NC) A19 · TXOUT_L3N(DBG_GPIO2) B19

TXOUT_U0P(NC) B18 · TXOUT_U0N(NC) A18 · TXOUT_U1P(PCIE_RESET_GPIO3) A17 · TXOUT_U1N(PCIE_RESET_GPIO2) B17 · TXOUT_U2P(NC) D20 · TXOUT_U2N(NC) D21 · TXOUT_U3P(PCIE_RESET_GPIO5) D18 · TXOUT_U3N(NC) D19

TXCLK_LP(DBG_GPIO1) B16 · TXCLK_LN(DBG_GPIO3) A16 · TXCLK_UP(PCIE_RESET_GPIO4) D16 · TXCLK_UN(PCIE_RESET_GPIO1) D17

PLL PWR / LVTM

PLLVDD(NC) A12 · PLLVDD18(NC) D14 · PLLVSS(NC) B12

VDDA18HTPLL H17

VDDA18PCIEPLL1 D7 · VDDA18PCIEPLL2 E7

VDDLTP18(NC) A13 · VSSLTP18(NC) B13

VDDLT18_1(NC) A15 · VDDLT18_2(NC) B15 · VDDLT33_1(NC) A14 · VDDLT33_2(NC) B14

VSSLT1(VSS) C14 · VSSLT2(VSS) D15 · VSSLT3(VSS) C16 · VSSLT4(VSS) C18 · VSSLT5(VSS) C20 · VSSLT6(VSS) E20 · VSSLT7(VSS) C22

PM

SYSRESETb D8 · POWERGOOD A10 · LDTSTOPb C10 · ALLOW_LDTSTOP C12

CLOCKs

HT_REFCLKP C25 · HT_REFCLKN C24

REFCLK_P/OSCIN(OSCIN) E11 · REFCLK_N(PWM_GPIO3) F11

GFX_REFCLKP T2 · GFX_REFCLKN T1 — I/O

GPP_REFCLKP U1 · GPP_REFCLKN U2 — I/O

GPPSB_REFCLKP(SB_REFCLKP) V4 · GPPSB_REFCLKN(SB_REFCLKN) V3

MIS.

I2C_DATA A9 · I2C_CLK B9 · DDC_DATA/AUX0N(NC) B8 · DDC_CLK/AUX0P(NC) A8 · AUX1P(NC) B7 · AUX1N(NC) A7

STRP_DATA B10

RSVD G11

AUX_CAL(NC) C8

LVDS_DIGON(PCE_TCALRP) E9 · LVDS_BLON(PCE_RCALRP) F7 · LVDS_ENA_BL(PWM_GPIO2) G12 — DIGON 19 · T105 · BLON 19

TMDS_HPD(NC) D9 · HPD(NC) D10 — TMDS_HPD0 T102 · TMDS_HPD1 T106

TVCLKIN(PWM_GPIO5) D12 — SUS_STAT#_NB — R329 D48 *0_4 *1SS355 — SUS_STAT# 15 · PLTRST# 14,16,20,24,27,30

THERMALDIODE_P AE8 · THERMALDIODE_N AD8 — R_NB_THRMDA T68 · R_NB_THRMDC T69

TESTMODE D13 — TEST_EN — R334 1.82K/F_4

To LVDS panel

LVDS POWER

+1.8V_VDDLTP18_NB · +1.8V_VDDLT_18_NB · +3V_VDLT33_NB

Power rails

VCC3 — L48 BLM18PG201SN1D(200_1.4A)_6 — +3V_AVDD_NB — C461 2.2u/6.3V_6

1.1V_NB — BLM18PG201SN1D(200_1.4A)_6 L22 — +1.1V_PLLVDD — C219 2.2u/6.3V_6

VCC1.8 — L25 BLM18PG201SN1D(200_1.4A)_6 — +1.8V_PLLVDD18 — C230 10u/6.3V_8 · C474 2.2u/6.3V_6

VCC1.8 — R339 *short0603 — +1.8V_AVDDDI_NB — C466 0.1u/10V_4 — BLM18PG201SN1D(200_1.4A)_6 L43 — +1.8V_AVDDQ_NB — C433 2.2u/6.3V_6

VCC1.8 — L21 BLM18PG201SN1D(200_1.4A)_6 — +1.8V_VDDLTP18_NB — C455 2.2u/6.3V_6

L20 BLM21PG201SN1D(200_100M_2A)_8 — +1.8V_VDDLT_18_NB — C210 4.7u/6.3V_6 · C207 0.1u/10V_4

VCC1.8 — VDDA18PCIEPLL -PCIE PLL — L46 BLM18PG221SN1D(220_1.4A)_6 — 20mils width +1.8V_VDDA18PCIEPLL — C440 2.2u/6.3V_6

VDDA18HTPLL -HT LINK PLL — L24 BLM18PG201SN1D(200_1.4A)_6 — 20mils width +1.8V_VDDA18HTPLL — C223 2.2u/6.3V_6

VCC1.8 — R169 *300_4 — Q17 *BSS138_NL/SOT23 — VCC1.8 — +VDDG_NB — R165 *4.7K_4 — 6,14 CPU_LDT_STOP# — NB_LDT_STOP# — R167 0_4 — RS780

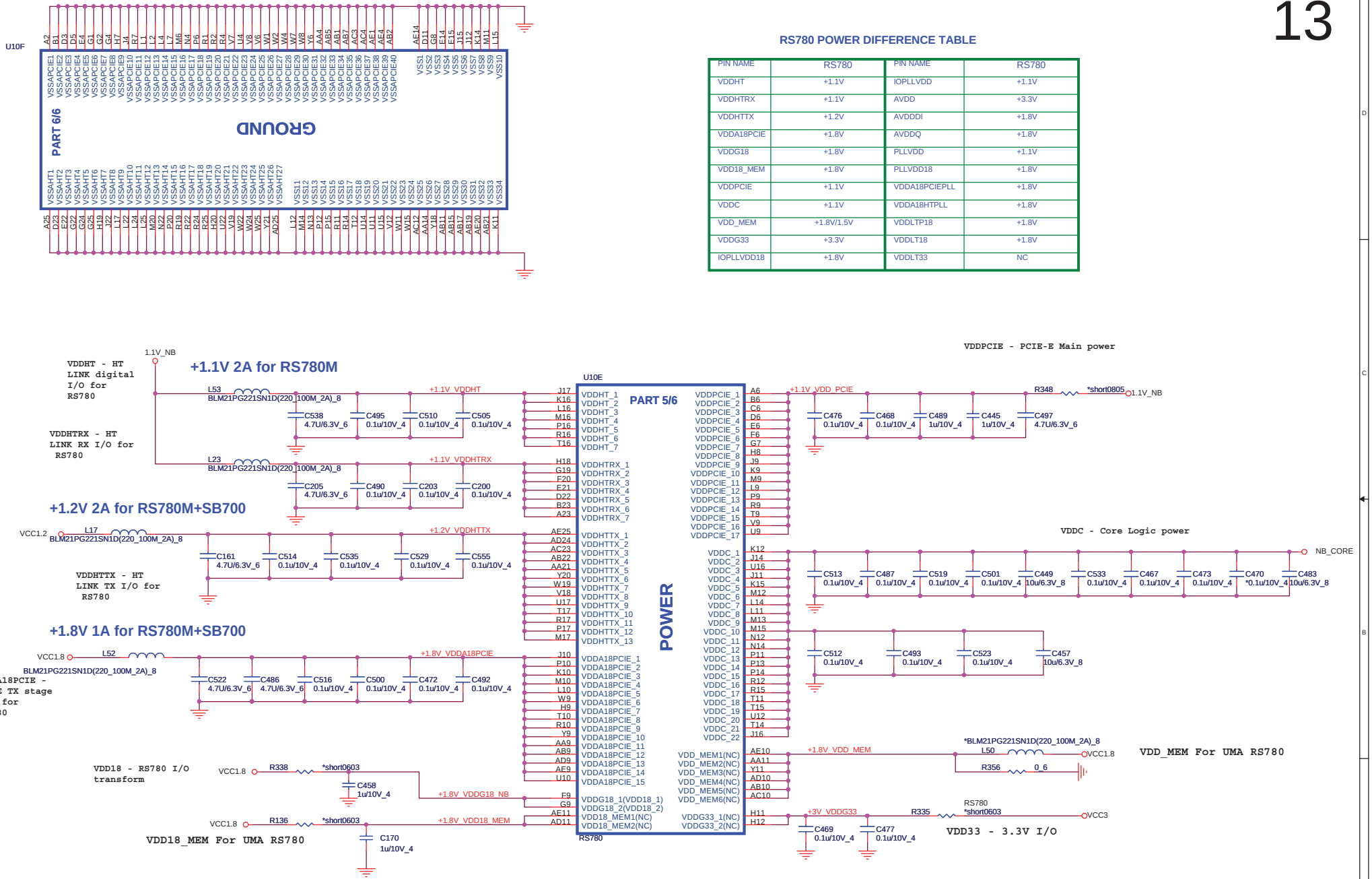
R163 0_6 — VCC3 — +VDDG_NB

VCC3 — L47 *BLM21PG221SN1D(220_100M_2A)_8 — +3V_VDLT33_NB — C444 *2.2u/6.3V_6

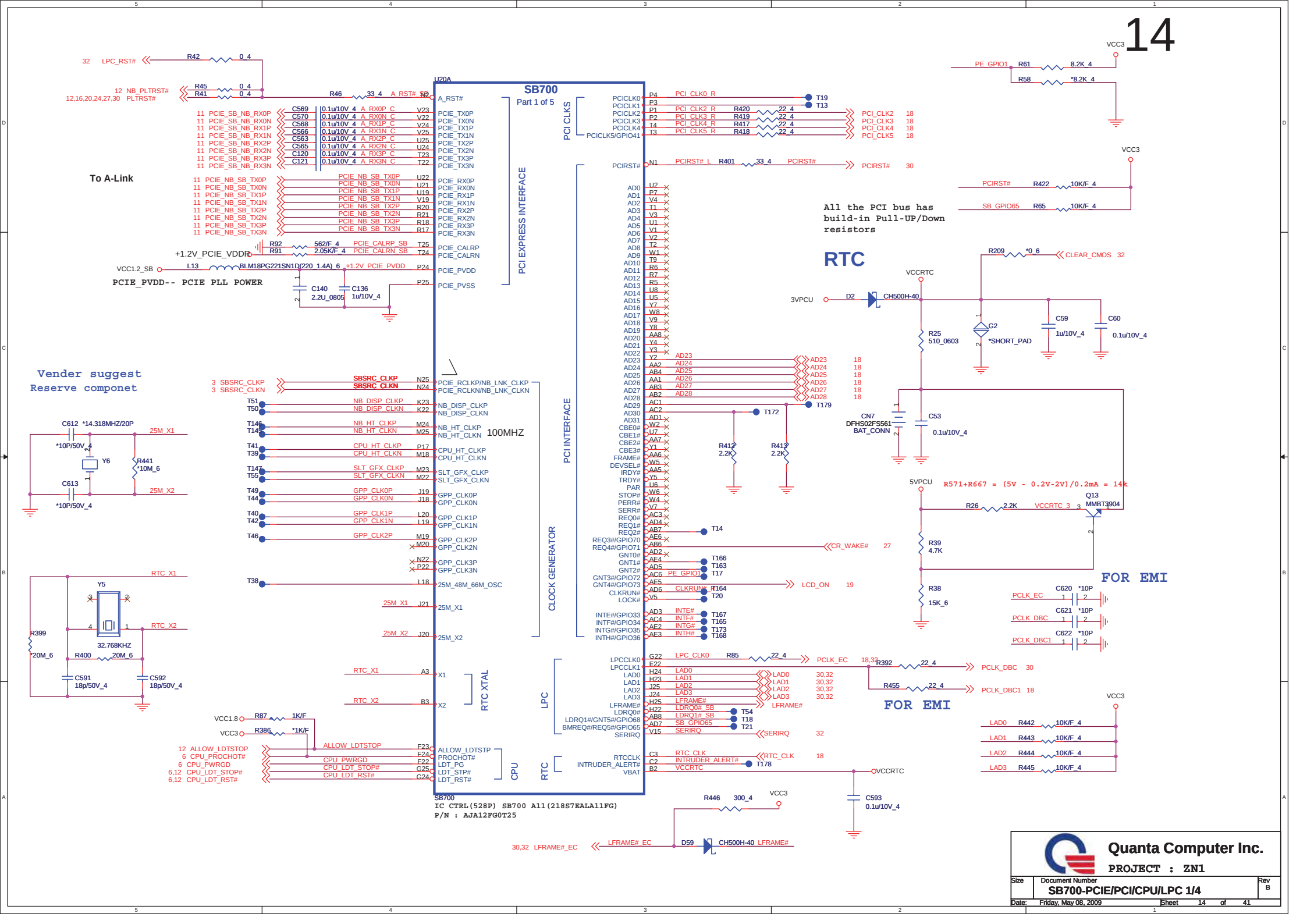
Quanta Computer Inc.		
PROJECT : ZN1		
Size	Document Number: RS780M-SYSTEM I/F 3/4	Rev: 1A
Date: Friday, May 08, 2009	Sheet 12 of 41	

RS780 POWER DIFFERENCE TABLE

PIN NAME	RS780	PIN NAME	RS780
VDDHT	+1.1V	IOPLLVDD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVDD	+1.1V
VDD18_MEM	+1.8V	PLLVDD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDLT18	+1.8V
IOPLLVDD18	+1.8V	VDDLT33	NC



Quanta Computer Inc.
PROJECT : ZN1
Size | Document Number: RS780M-POWER4/4 | Rev 1A
Date: Friday, May 08, 2009 | Sheet 13 of 41


SB700
Part 1 of 5
U20A
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
CLOCK GENERATOR
LPC
RTC XTAL
CPU
RTC
To A-Link
PCIE_PVDD-- PCIE PLL POWER
All the PCI bus has build-in Pull-UP/Down resistors
RTC
FOR EMI
FOR EMI
Vender suggest
Reserve componet
100MHZ
SB700
IC CTRL(528P) SB700 A11(218S7EALA11FG)
P/N : AJA12FG0T25
Quanta Computer Inc.
PROJECT : ZN1
SB700-PCIE/PCI/CPU/LPC 1/4
Size
Document Number
Rev B
Date: Friday, May 08, 2009
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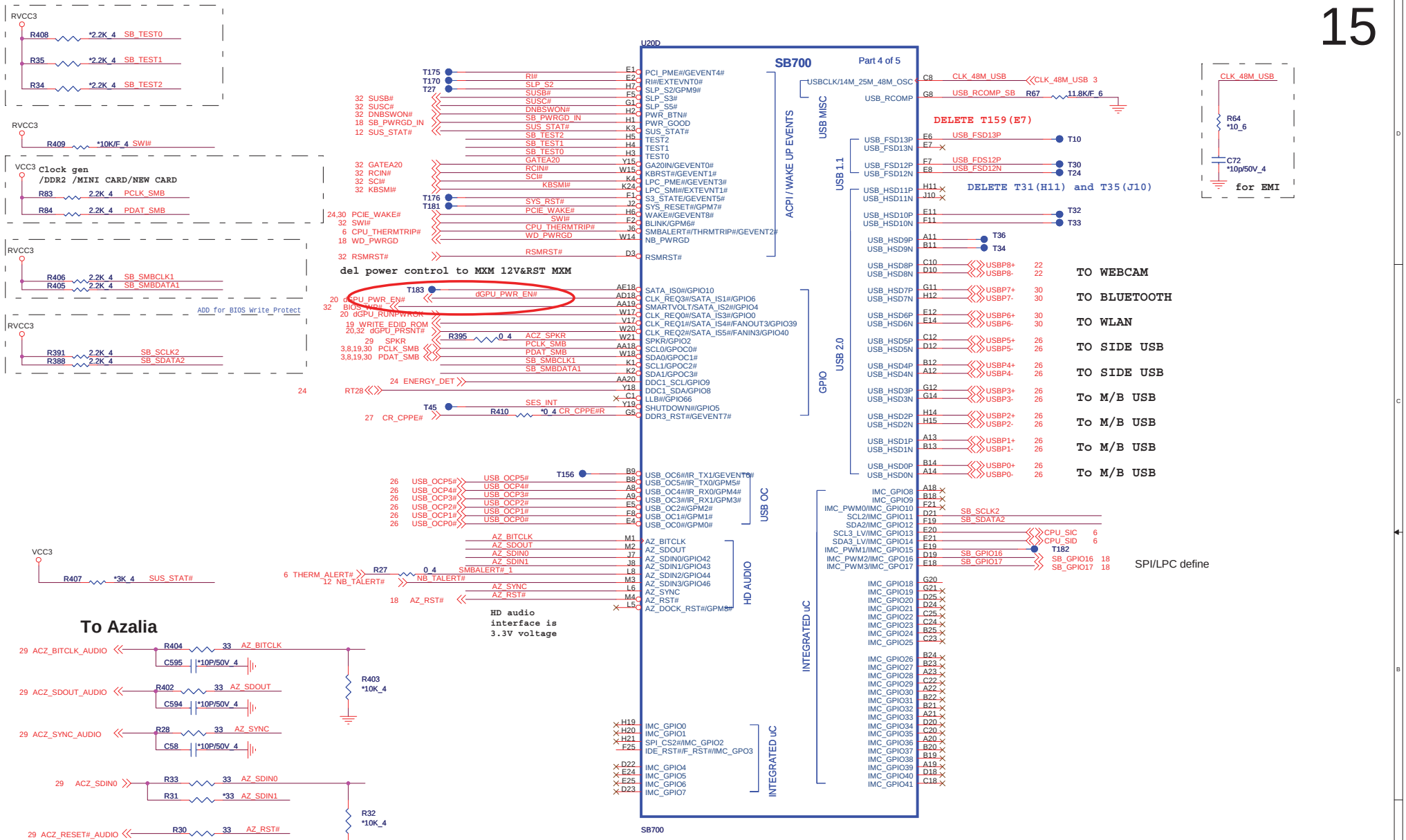
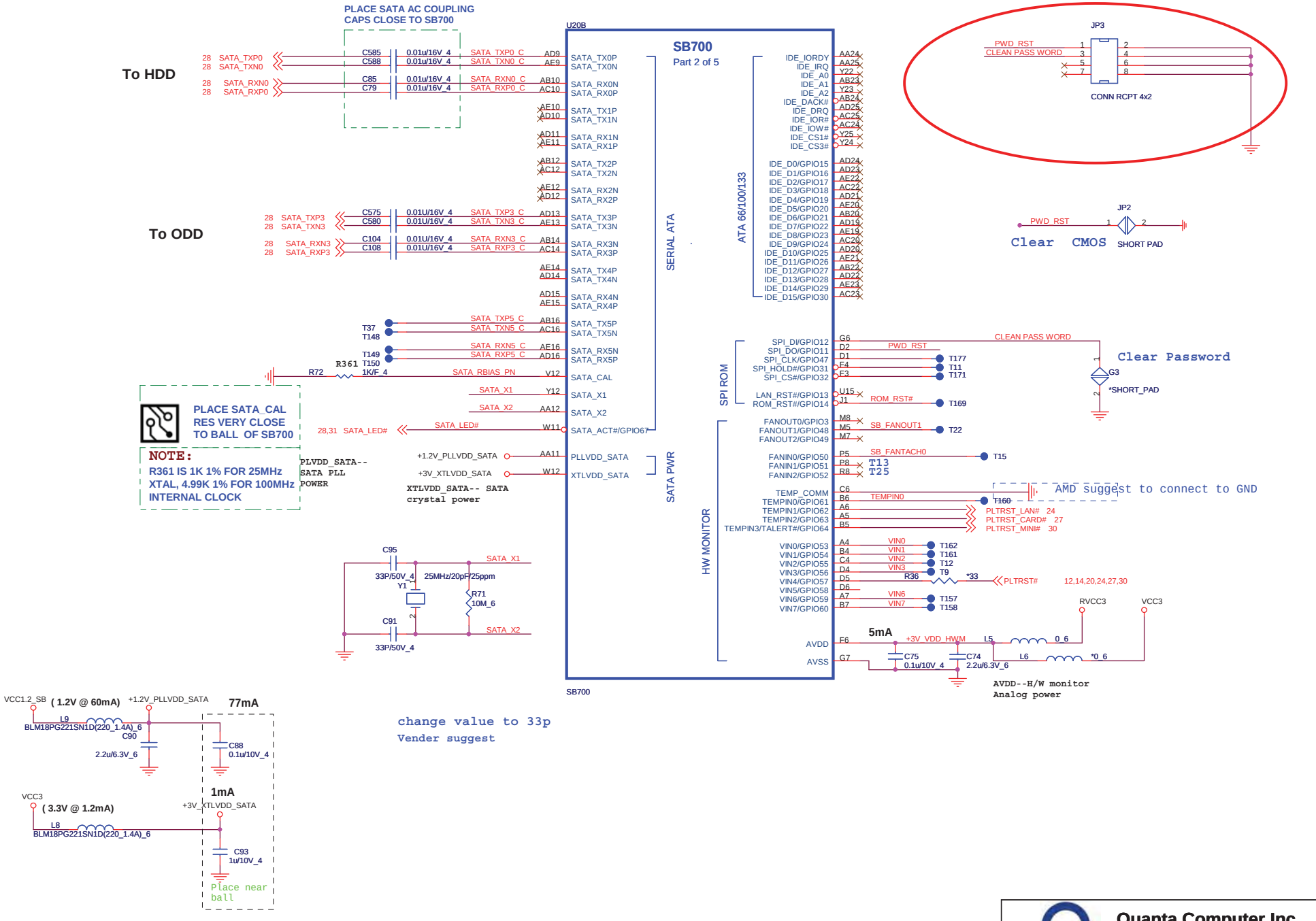


Quanta Computer Inc.
PROJECT : ZN1
Size | Document Number: SB700-ACPI/GPIO/USB 2/4 | Rev: 1A
Date: Friday, May 08, 2009 | Sheet 15 of 41


PLACE SATA AC COUPLING
CAPS CLOSE TO SB700
To HDD
To ODD
U20B
SB700
Part 2 of 5
SERIAL ATA
ATA 66/100/133
SATA PWR
SPI ROM
HW MONITOR
JP3
PWD_RST
CLEAN PASS WORD
CONN RCPT 4x2
JP2
Clear CMOS
SHORT PAD
Clear Password
*SHORT_PAD
PLACE SATA_CAL
RES VERY CLOSE
TO BALL OF SB700
NOTE:
R361 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK
PLLVDD_SATA--
SATA PLL
POWER
XTLVDD_SATA-- SATA
crystal power
AMD suggest to connect to GND
5mA
AVDD--H/W monitor
Analog power
77mA
1mA
Place near
ball
change value to 33p
Vender suggest
SB700

PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.

SB700 Part 3 of 5

POWER

VDDQ--3.3V I/O power

1.8V : FLASH MEMORY MODE(DEFAULT)
3.3V: IDE MODE

VDD33_18--3.3V IDE I/O power
1.8V flash memory I/O power

PCIE_VDDR--PCIE I/O power

AVDD_SATA--SATA phy power

For support USB wakeup-->3V_S5

AVDDTX--USB Phy
Analog I/O power

VDD-- S/B CORE power

CKVDD_1.2V-- Internal
clock Generator I/O
power

S5_3.3--3.3v standby power

S5_1.2V--1.2V standby power

V5_VREF--PCI 5V TOLERANCE

*:reserve

USB_PHY_1.2V--USB Phy
digital power

AVDDCK--USB Analog PLL power

AVDDCK_1.2--USB Phy
digital power

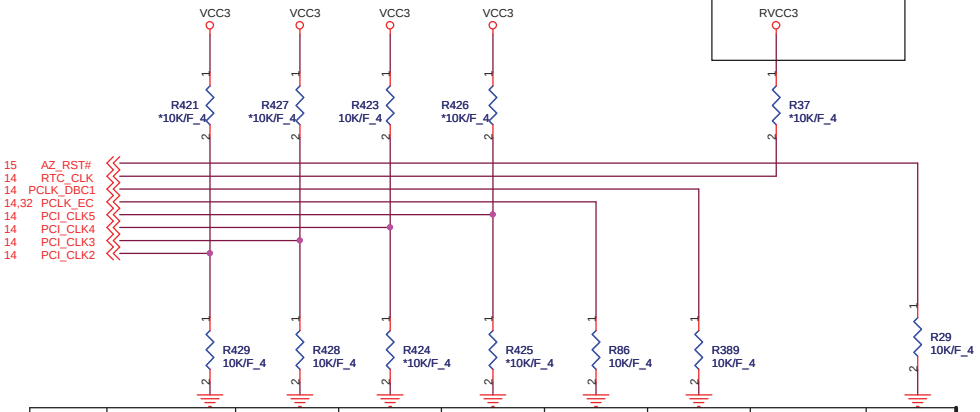
AVDDCK_3.3--Analog
system PLL power

Change to 0603

Quanta Computer Inc.	
PROJECT : ZN1	
Size	Document Number: SB700-PWR/DECOUPLING 4/4 — Rev: 1A
Date: Friday, May 08, 2009	Sheet 17 of 41

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

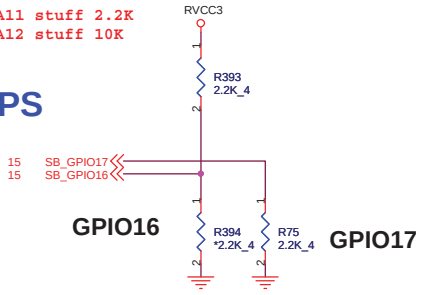
It must ready refore RSMRST#



	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT
					EC ENABLED			ENABLE PCI MEM BOOT

REQUIRED STRAPS

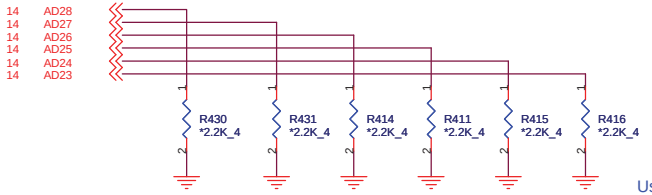
A11 stuff 2.2K
A12 stuff 10K



TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

DEBUG STRAPS

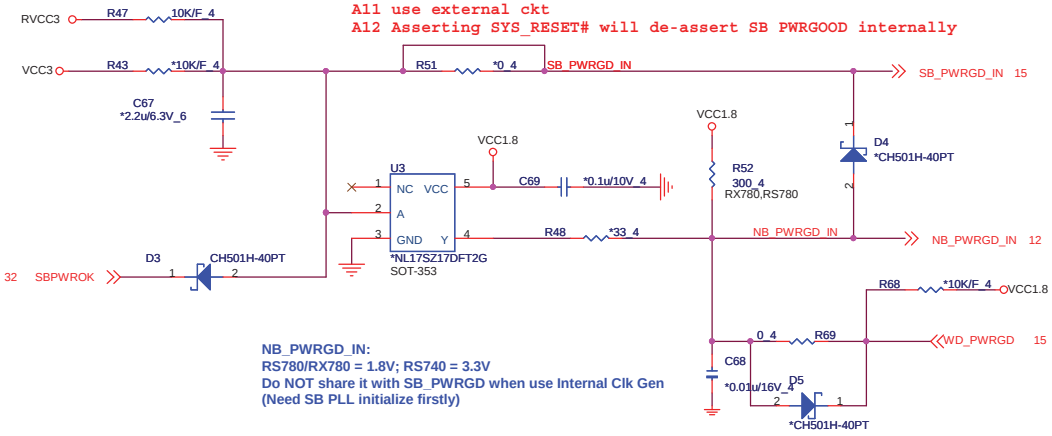
SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



Use 2.2K PD.

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

SB_PWRGD
A11 use external ckt
A12 Asserting SYS_RESET# will de-assert SB PWRGOOD internally

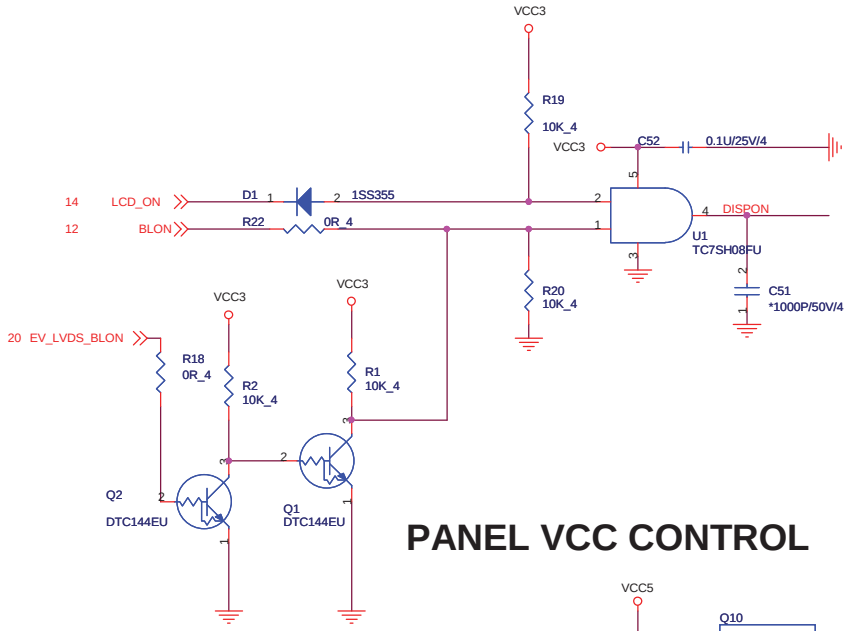


NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)

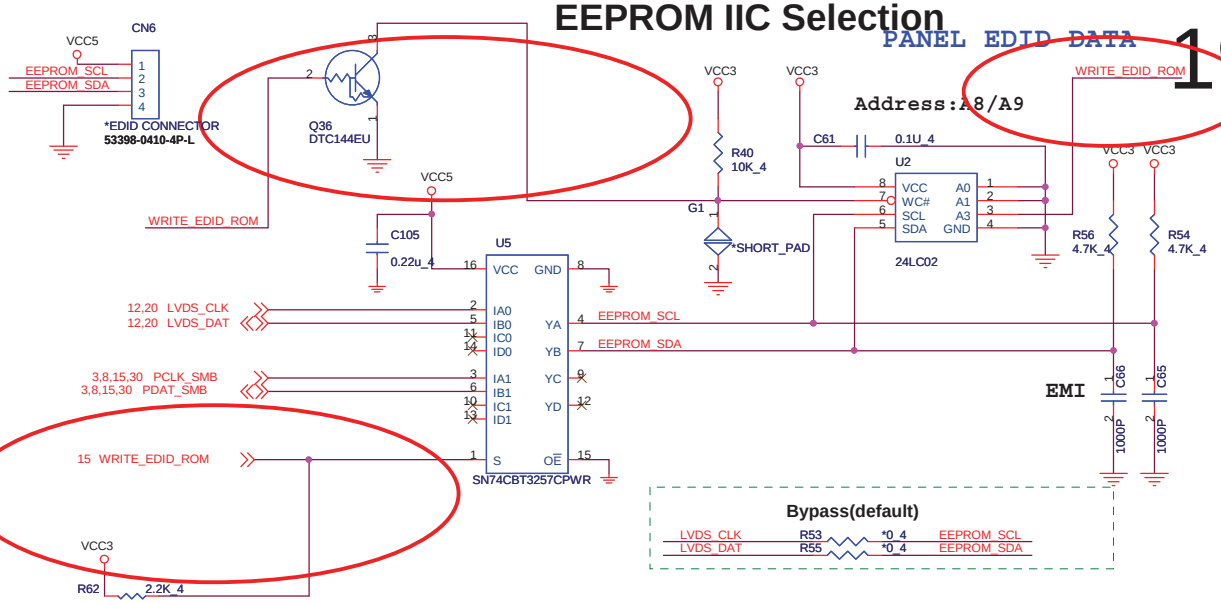
Quanta Computer Inc.
PROJECT : ZN1

Size	Document Number	Rev
	SB700-STRAPS	1A
Date: Friday, May 08, 2009	Sheet 18 of 41	

BACKLIGHT CONTROL



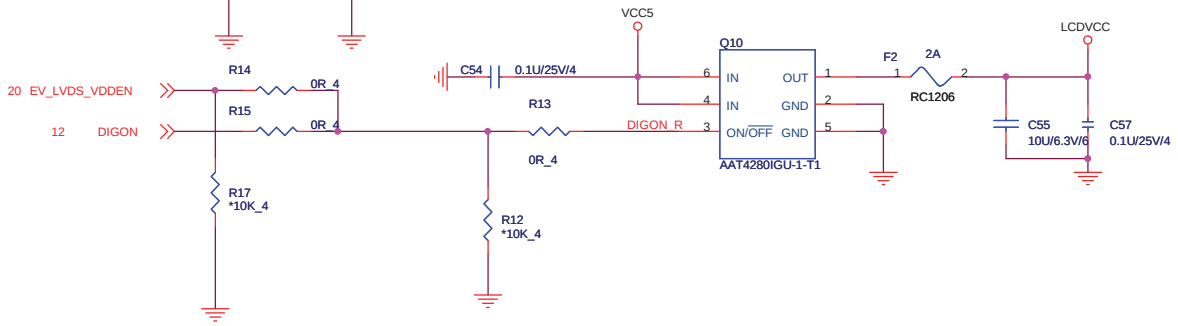
EEPROM IIC Selection



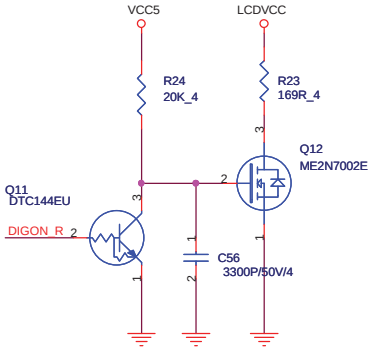
PANEL EDID DATA

Address:A8/A9

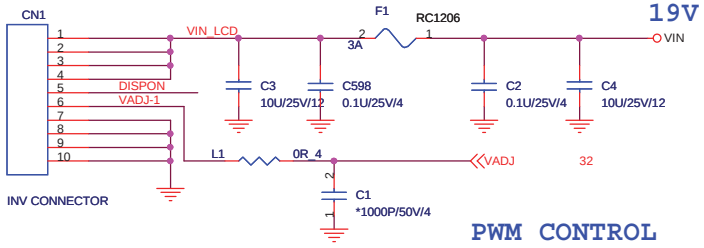
PANEL VCC CONTROL



Discharge panel power

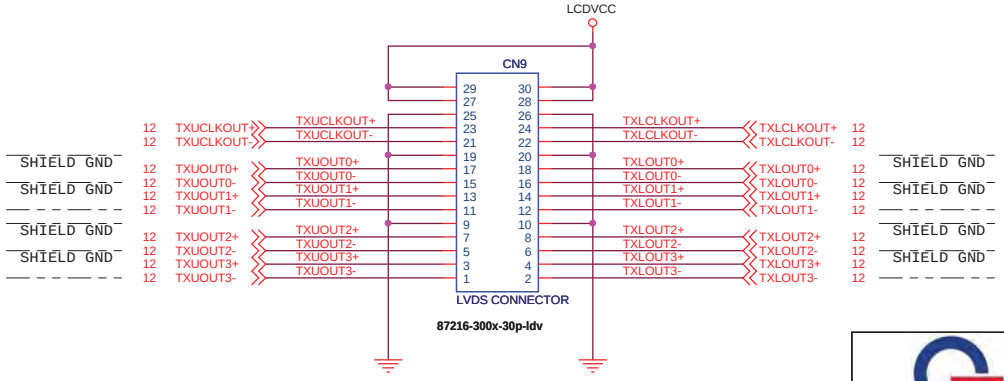


TO INVERTER POWER



PWM CONTROL

LCD PANEL CONNECTOR



Quanta Computer Inc.

PROJECT : ZN1

Size	Document Number	Rev
	LCD PANEL/WEBCAM	A
Date: Friday, May 08, 2009	Sheet 19 of 41	

MXM Module

dGPU_PRSNT#	Sku
Low	MXM
High	WO/ MXM

update MXM footprint to mxm-mm70-314-310b1-1-270p

MXM3.0	n-Vidia	AMD
LVDS	LVDS	LVDS/Int. DP
DP_D	Int. DP	X
DP_A	HDMI	HDMI
DP_C	Ext. DP/DVI	Ext. DP/DVI
DP_B	N/A	N/A

MXM Reset

SMBus

MXM VIN Power switch

MAINON	Behavior
Low	Enable dGPU PWR
High	Disable dGPU PWR

MXM 3V/5V Power switch

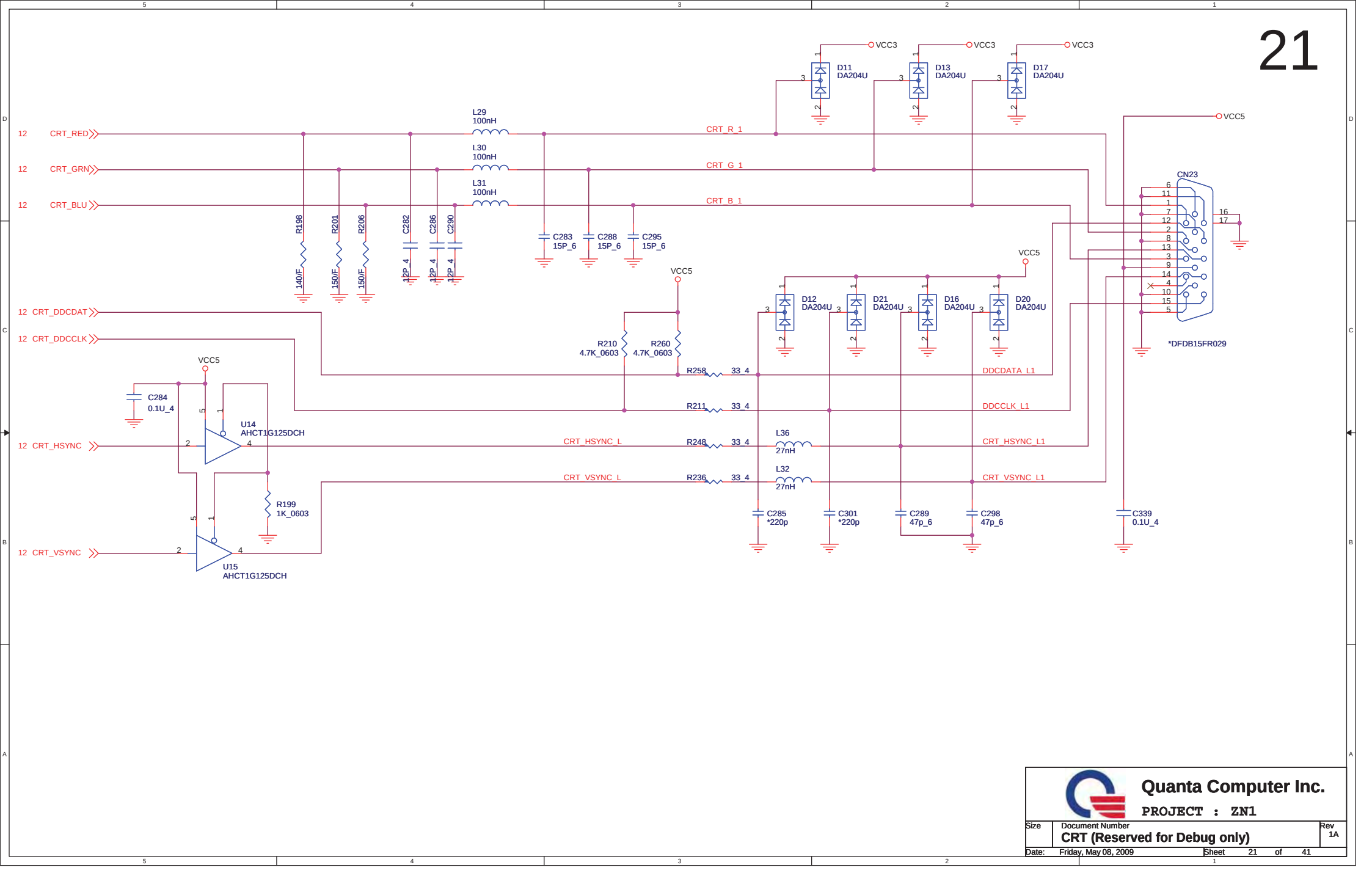
LCD PANEL CONNECTOR(WITH MXM)

Change BOM value

To low power status mode

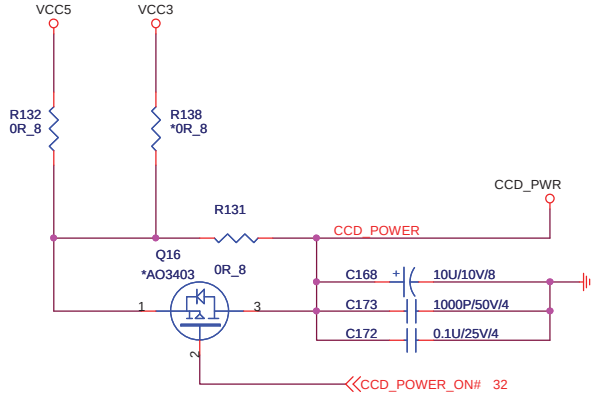
pin28 connect to LCDVCC

Quanta Computer Inc.
PROJECT : ZN1
Size | Document Number | Rev
MXM3.0 | 3B
Date: Friday, May 08, 2009 Sheet 20 of 41

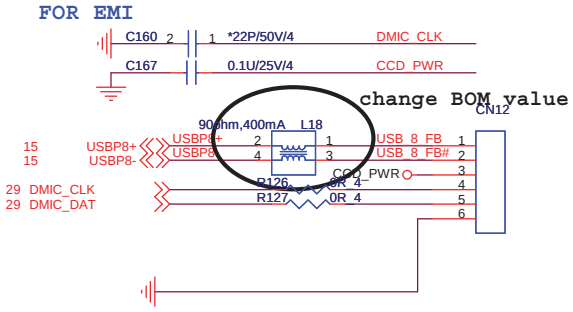


Quanta Computer Inc.		
PROJECT : ZN1		
Size	Document Number: CRT (Reserved for Debug only)	Rev: 1A
Date: Friday, May 08, 2009	Sheet 21 of 41	

CAMERA POWER CONTROL



TO WEB CAM MODULE

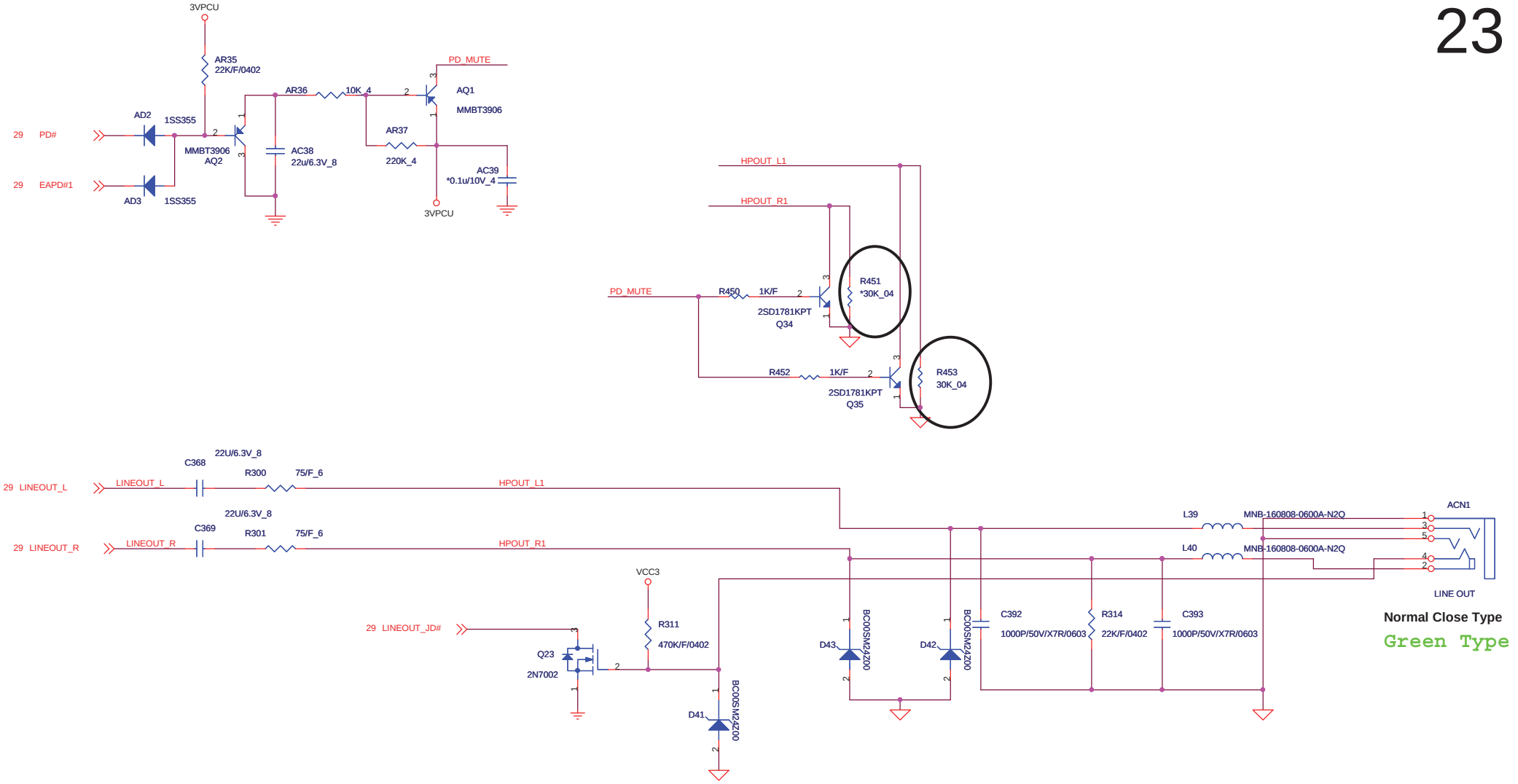


Quanta Computer Inc.

PROJECT : ZN1

Size	Document Number	Rev
	WEBCAM	1A

Date: Friday, May 08, 2009 Sheet 22 of 41



Quanta Computer Inc.		
PROJECT : ZN1		
Size	Document Number: Line Out	Rev: 1A
Date: Friday, May 08, 2009	Sheet 23 of 41	

LAN Power

Delete Q26,C475

WIDE TRACE

change L value to 0 in 8103EL

for 8103EL

Vender suggest

EC-A-01

RTL8103EL

U18

U19

*AT93C46A(3.3V)

25MHZ

VCC3

LANVCC

DVDD12

EVDD12

GND

CTRL12A

CTRL12/VDD

XTAL25

LAN_ACT# 25

LAN_LINK# 25

LAN_LINK1# 25

PCIE_WAKE# 15,30

PLTRST# 12,14,16,20,27,30

PLTRST_LAN# 16

ENERGY_DET 15

CLK_PCIE_LAN# 3

CLK_PCIE_LAN 3

GPP_RX2N_LAN 11

GPP_RX2P_LAN 11

11 GPP_TX2P_LAN

11 GPP_TX2N_LAN

LAN0_MDI0+ 25

LAN0_MDI0- 25

LAN0_MDI1+ 25

LAN0_MDI1- 25

LAN0_MDI2+ 25

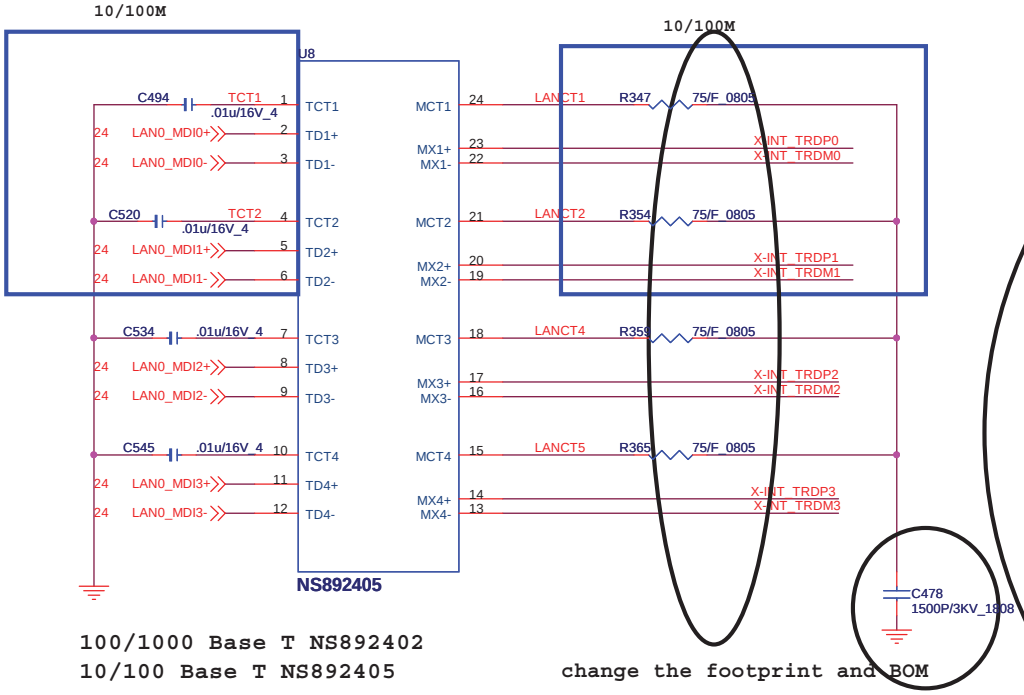
LAN0_MDI2- 25

LAN0_MDI3+ 25

LAN0_MDI3- 25

Quanta Computer Inc.		
PROJECT : ZN1		
Size	Document Number: LAN RTL8111DL/RTL8103EL	Rev 1A
Date: Friday, May 08, 2009	Sheet 24 of 41	

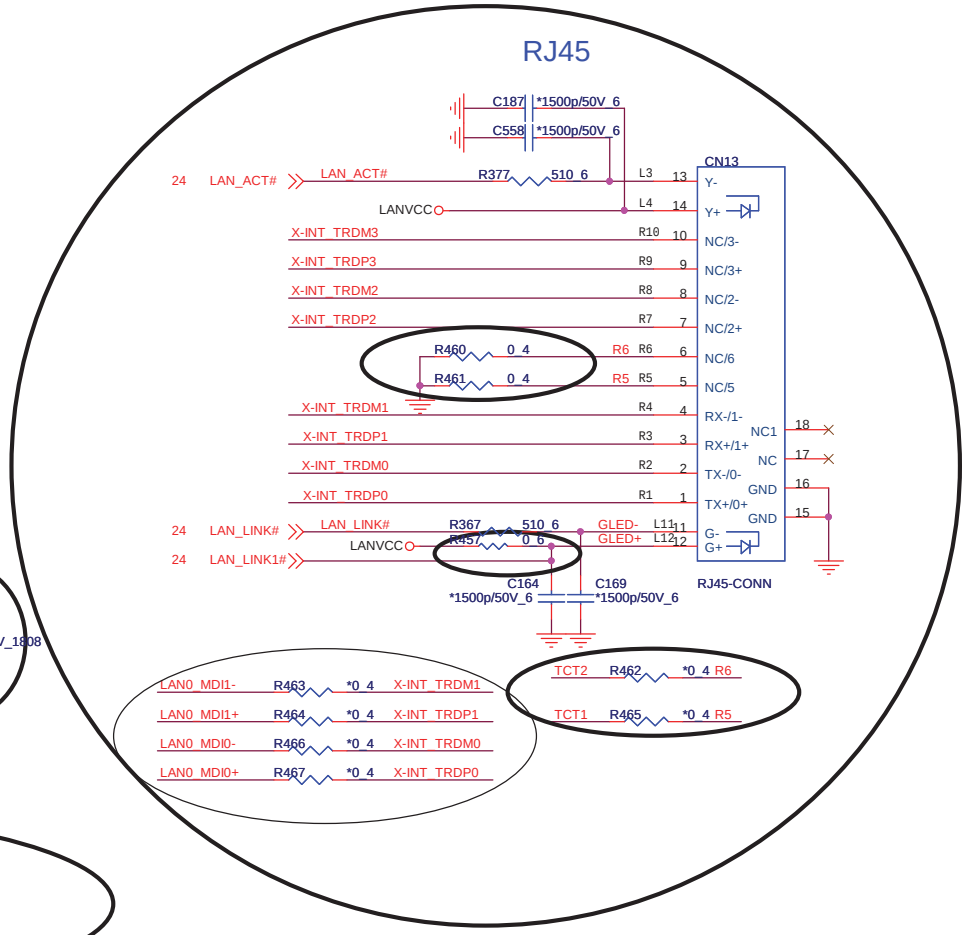
LAN Transformer & WIRE CONN to RJ45



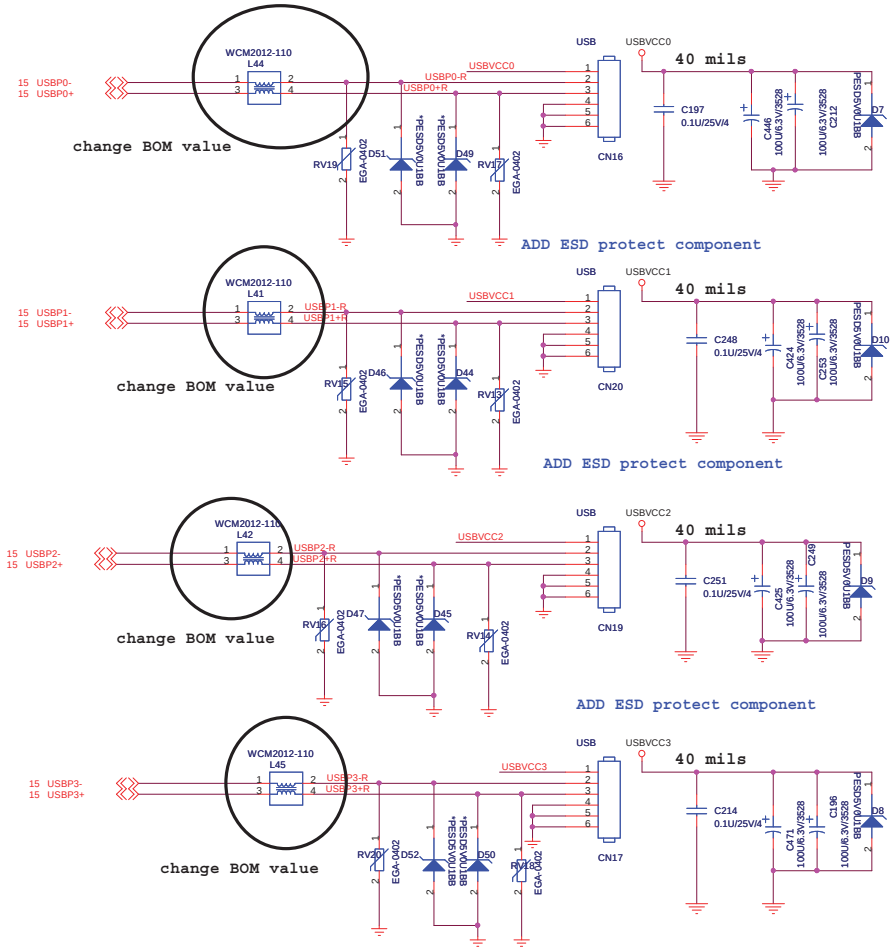
100/1000 Base T NS892402
10/100 Base T NS892405

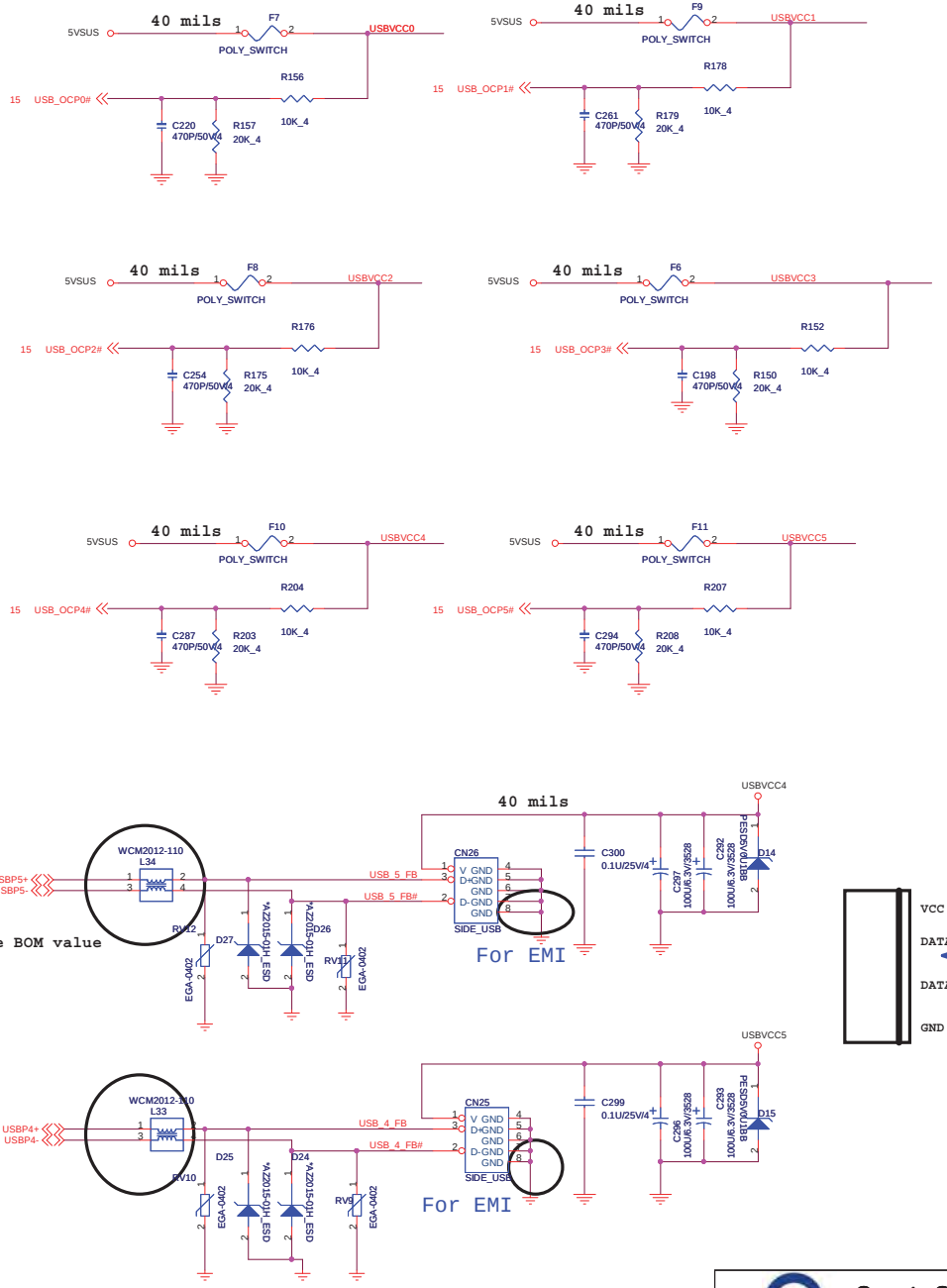
change the footprint and BOM

delete RV1-RV8



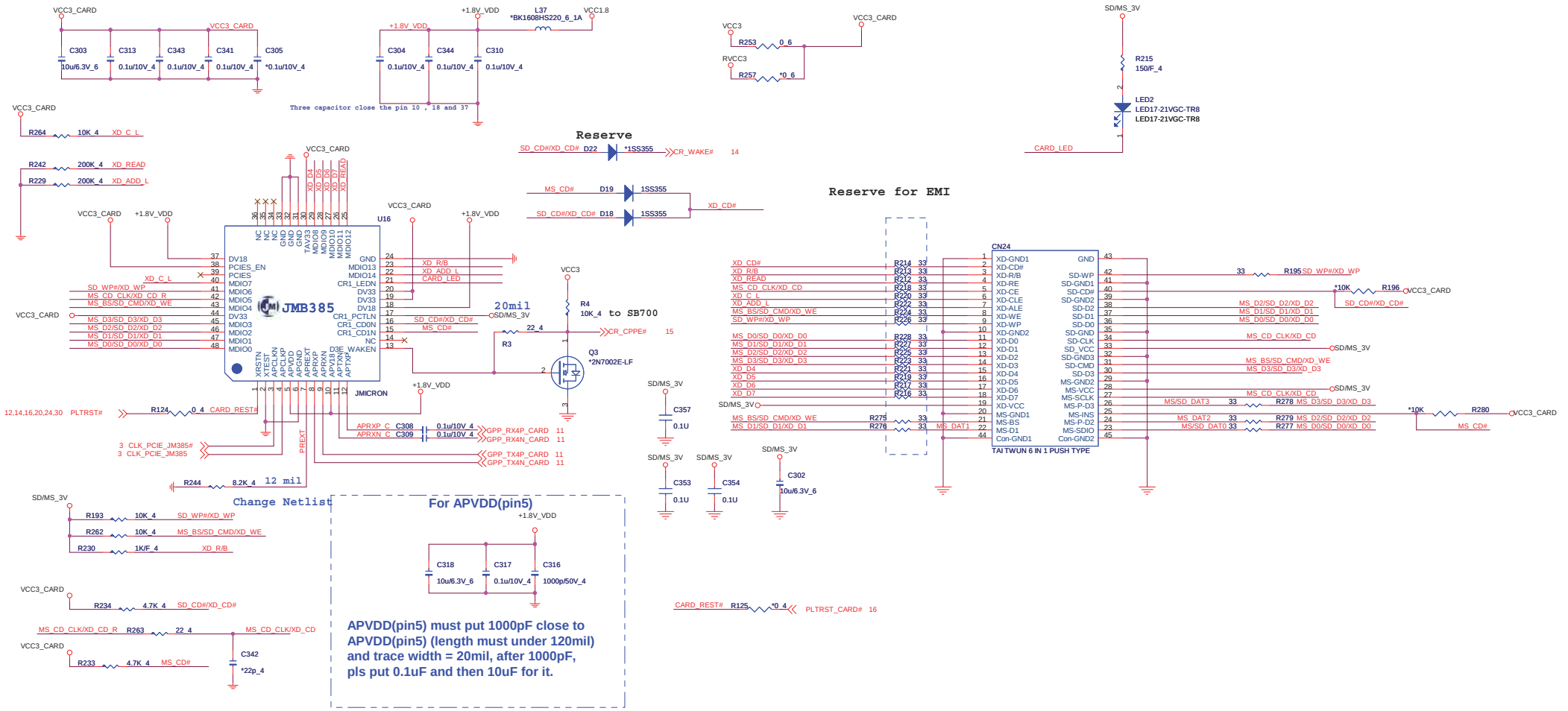
Quanta Computer Inc.		
PROJECT : ZN1		
Size	Document Number: LAN Transformer & RJ45	Rev 1A
Date: Friday, May 08, 2009	Sheet 25 of 41	





Quanta Computer Inc.		
PROJECT : ZN1		
Size	Document Number: USB Port X6	Rev: A
Date: Friday, May 08, 2009	Sheet 26 of 41	

Memory Card Power Supply



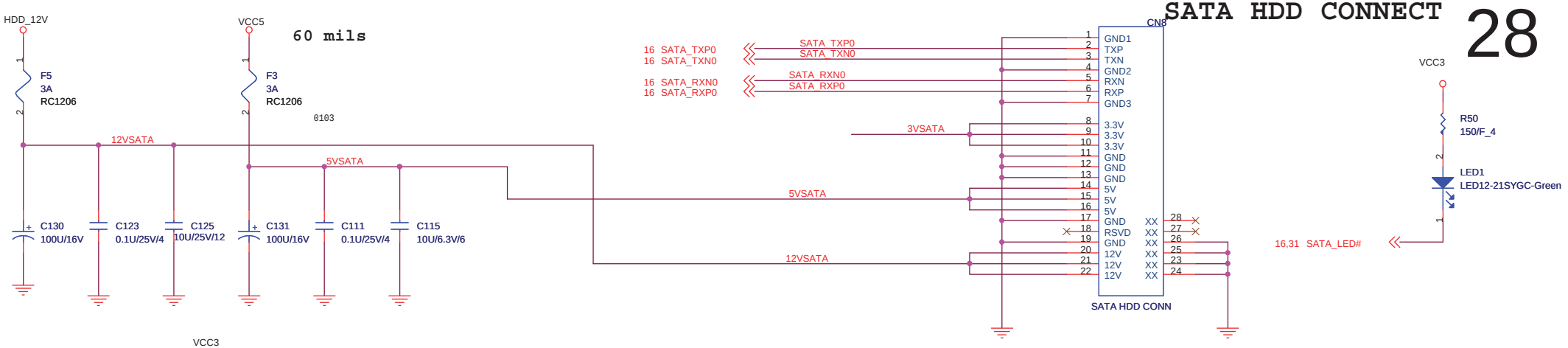
Quanta Computer Inc.
PROJECT : ZN1

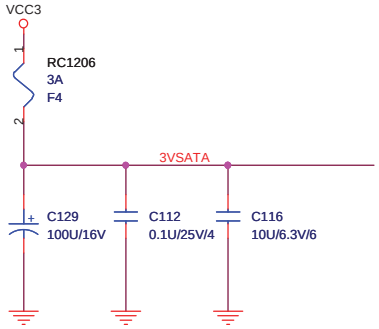
Size	Document Number	Rev
	Card Reader	1A

Date: Friday, May 08, 2009 Sheet 27 of 41

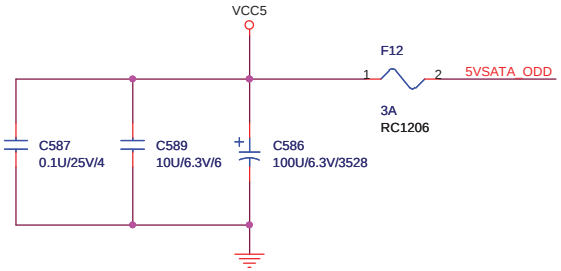
SATA HDD CONNECT

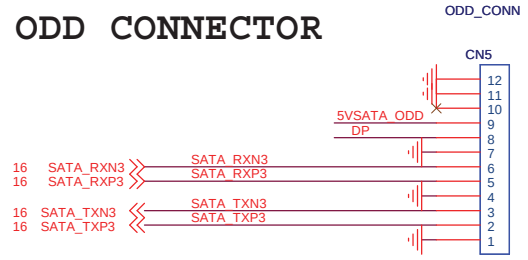
28





SATA ODD CONNECTOR



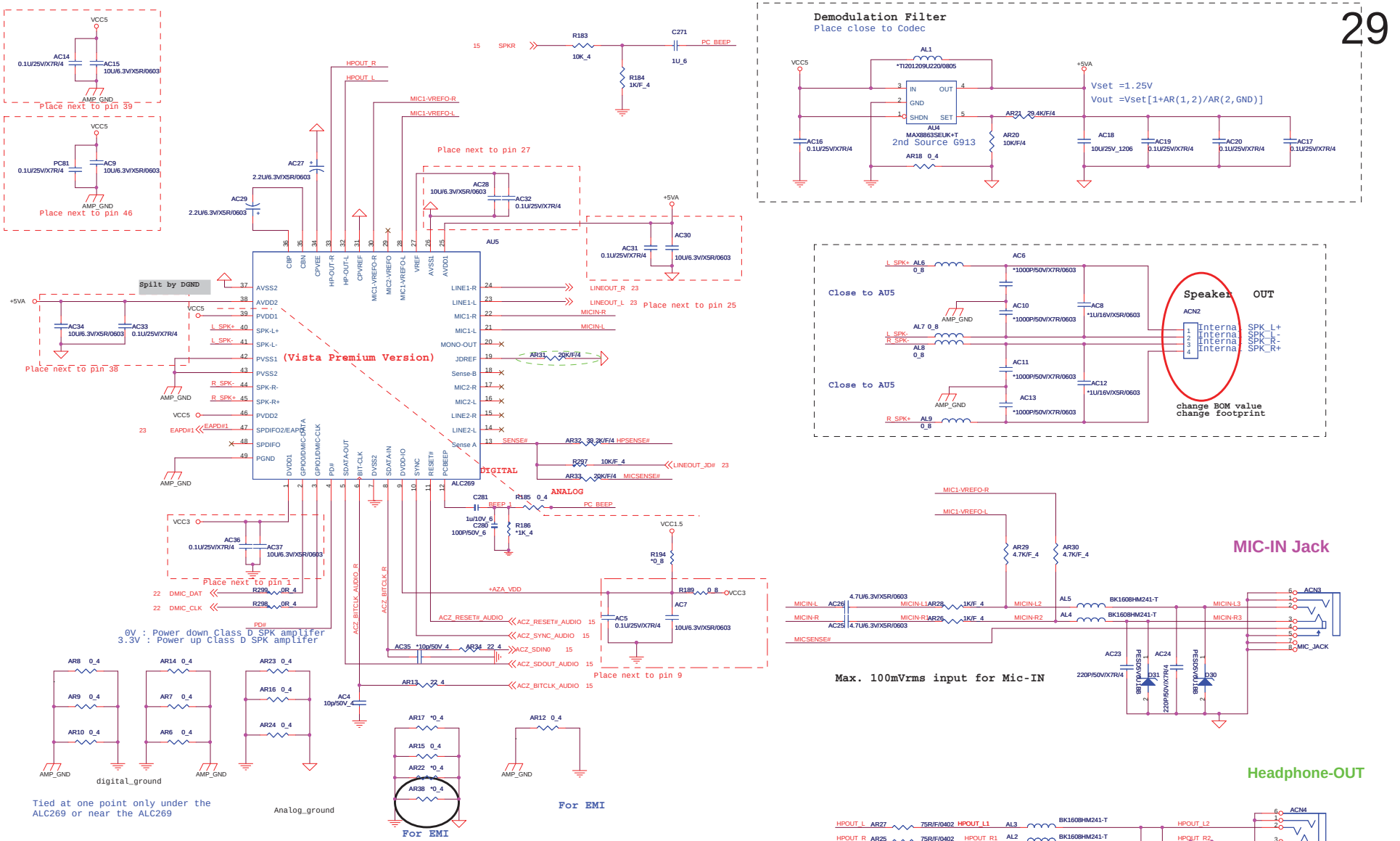


Quanta Computer Inc.

PROJECT : ZN1

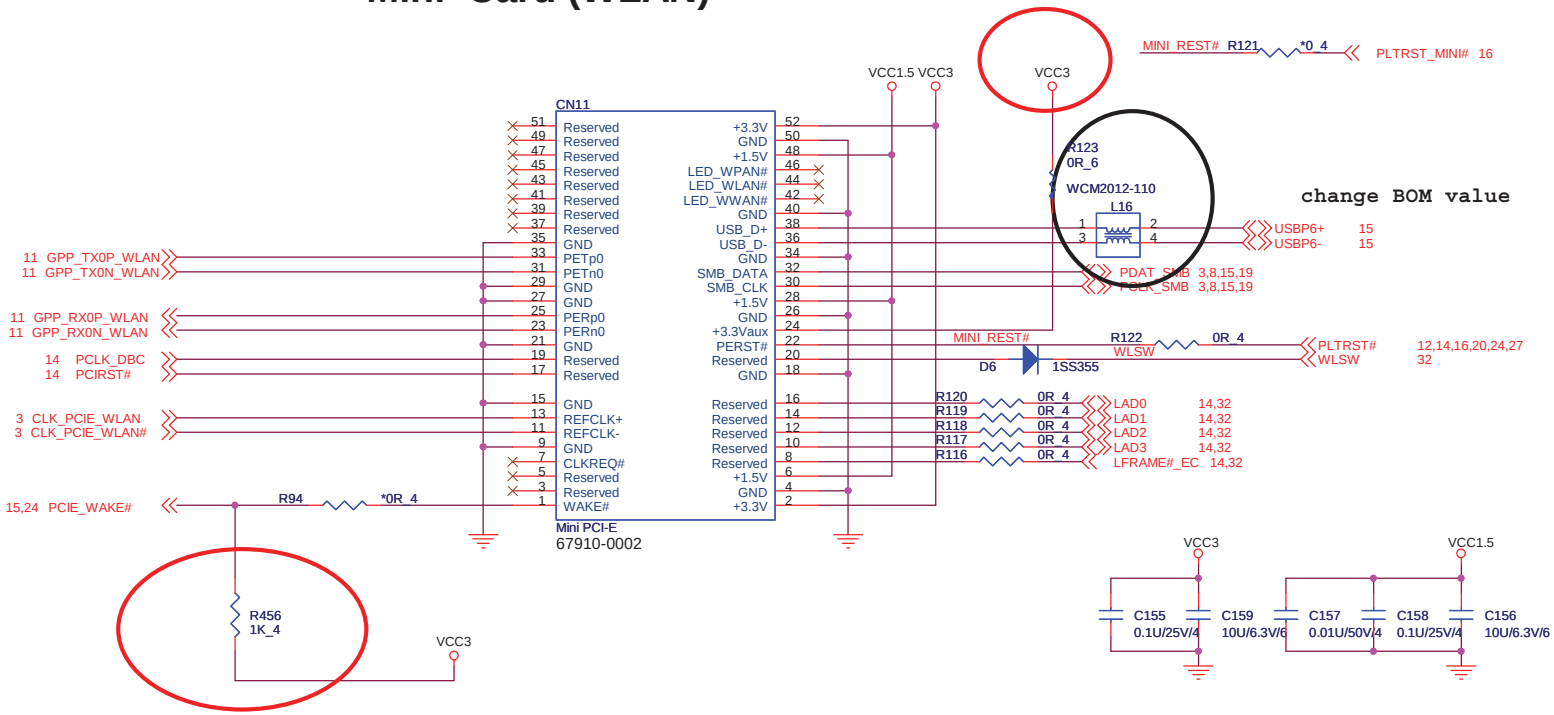
Size	Document Number	Rev
	SATA HDD/ODD	A

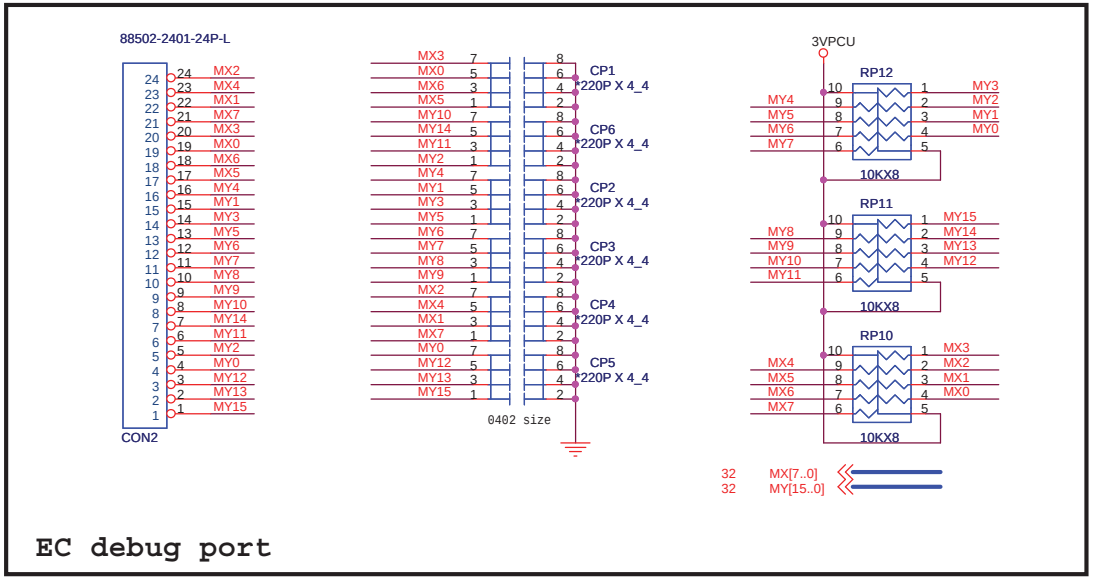
Date: Friday, May 08, 2009 Sheet 28 of 41



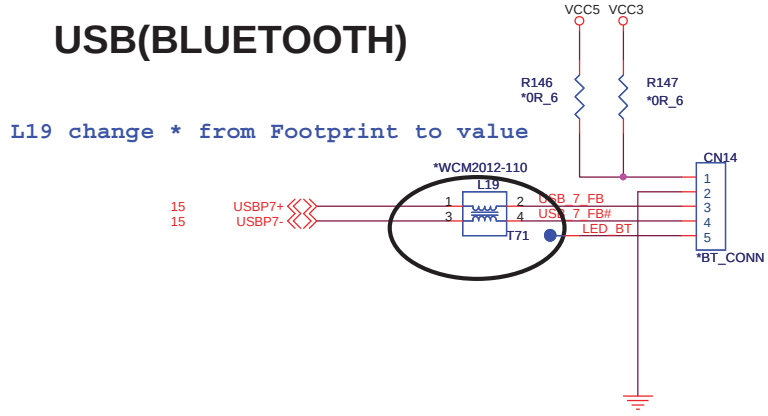
Quanta Computer Inc.			
PROJECT : ZN1			
Size	Document Number		Rev
	Realtek ALC269		1A
Date: Friday, May 08, 2009		Sheet 29 of 41	

Mini Card (WLAN)



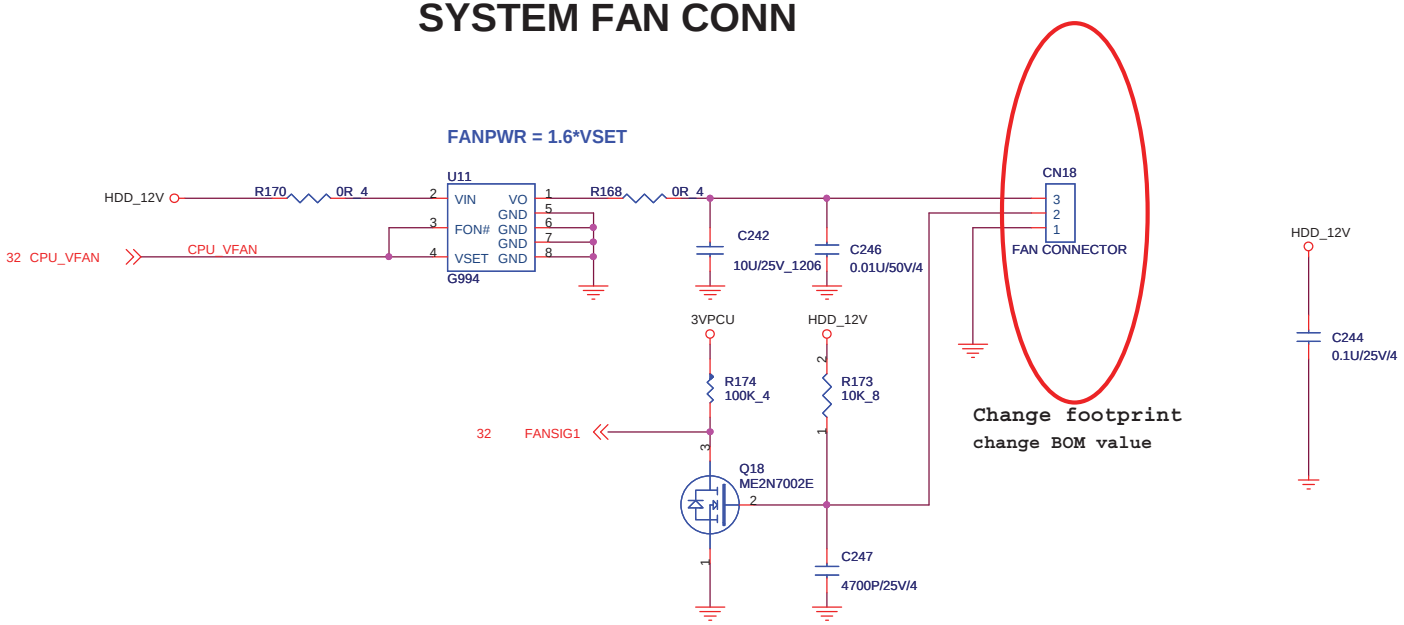


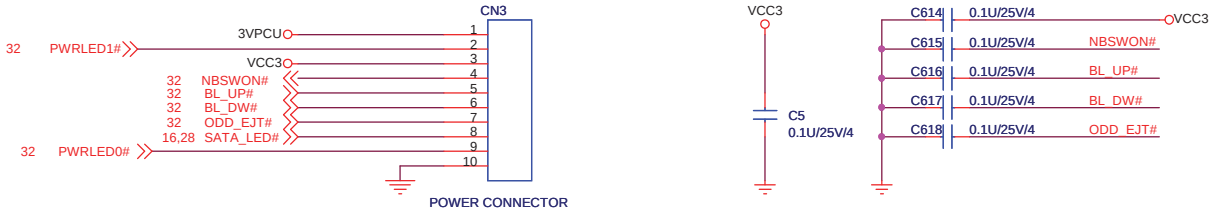
USB(BLUETOOTH)



Quanta Computer Inc.		
PROJECT : ZN1		
Size	Document Number: MINI CARD & BT	Rev: A
Date: Friday, May 08, 2009	Sheet 30 of 41	

SYSTEM FAN CONN





TO POWER BUTTON & LED LIGHT

Quanta Computer Inc.

PROJECT : ZN1

Size	Document Number	Rev
	FAN	A
Date: Friday, May 08, 2009	Sheet 31 of 41	

IT8512

Layout Note:
Place all capacitors close to IT8512.

Layout Note:
net "3VPCU" and "RTC_VCC"
minimum trace width 12mils.

(For PLL Power)

SMBUS
Pull Up for Low Active Pin

Layout Note:
Place R471,R498,R534 within 500 mils from SPI Flash.Place R567 within 500mils from R534; R520 within 500mils from R498 and R570 within 500mils from R471.

8Mbit , SPI

8M Winbond P/N:AKE3GZN0N00

SPI Socket P/N:DG008000031
A stage be use first

Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.

Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.

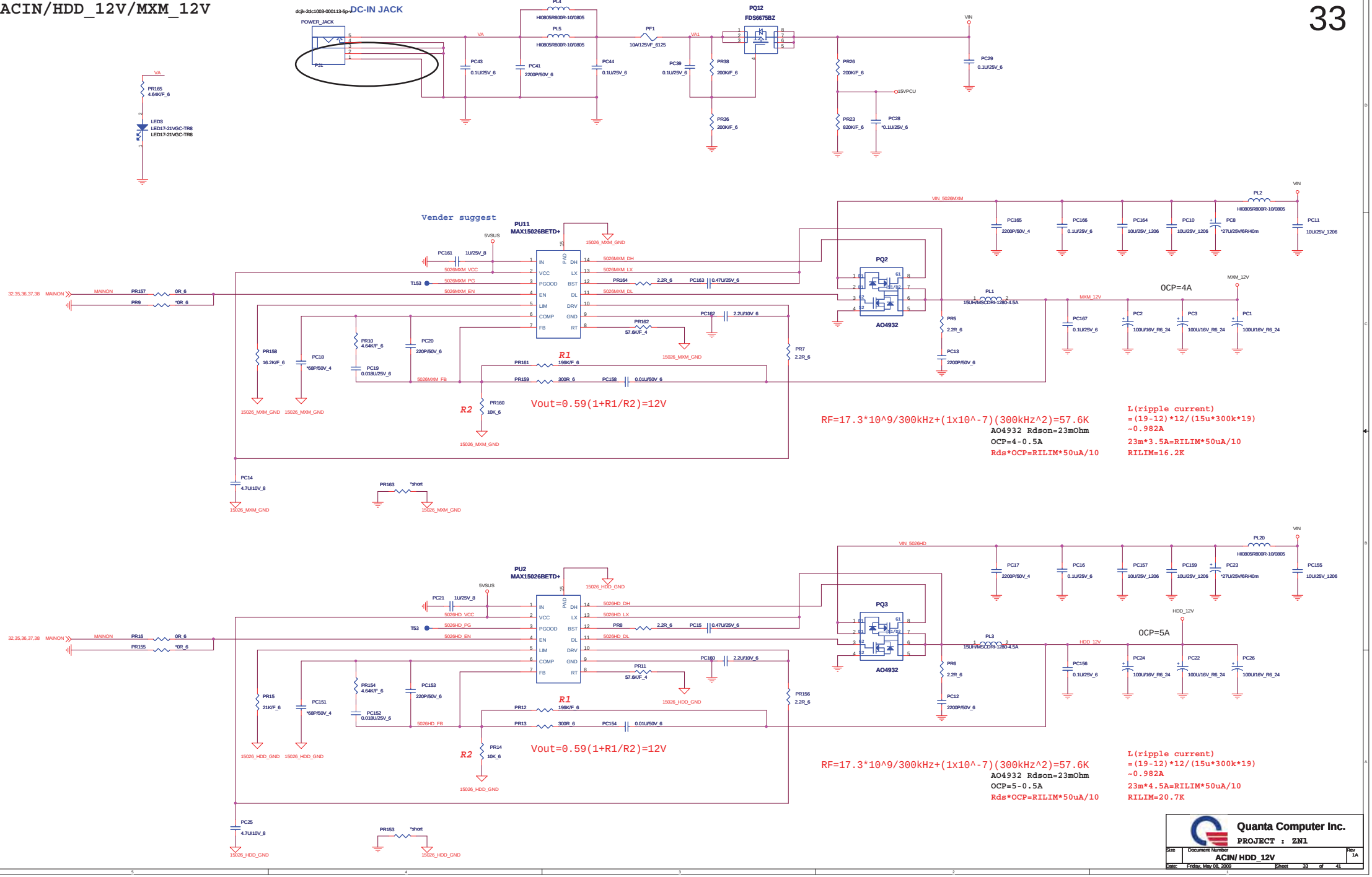
Layout Note:
32.768kHz clock lines:
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.

Please reserve this connector for serial debug port & KBS download usage.

IT8512 U17
AJ085120F03

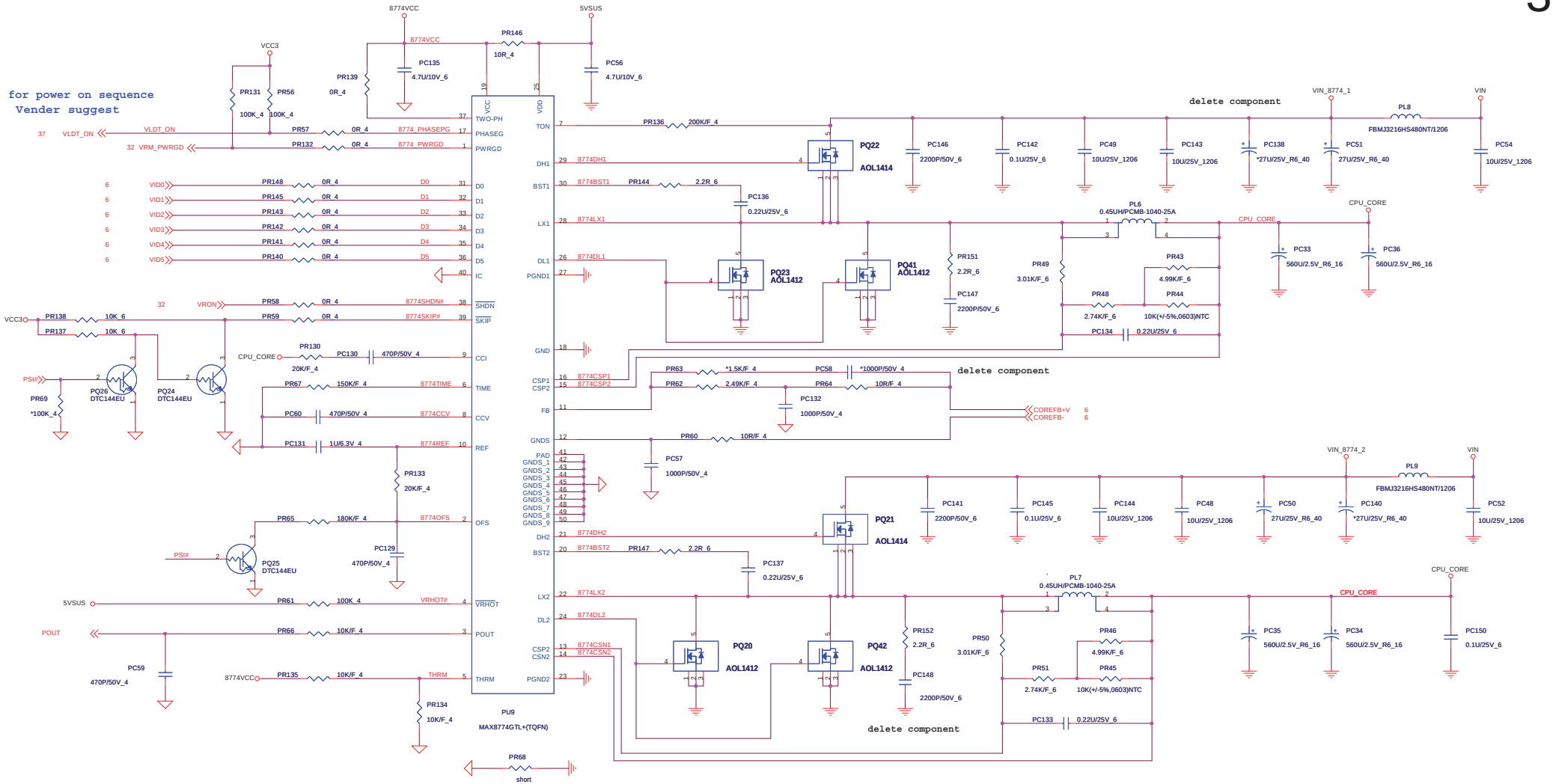
Quanta Computer Inc.
PROJECT : ZN1
Size | Document Number: EC ITE8512 | Rev 1A
Date: Friday, May 08, 2009 | Sheet 32 of 41

ACIN/HDD_12V/MXM_12V



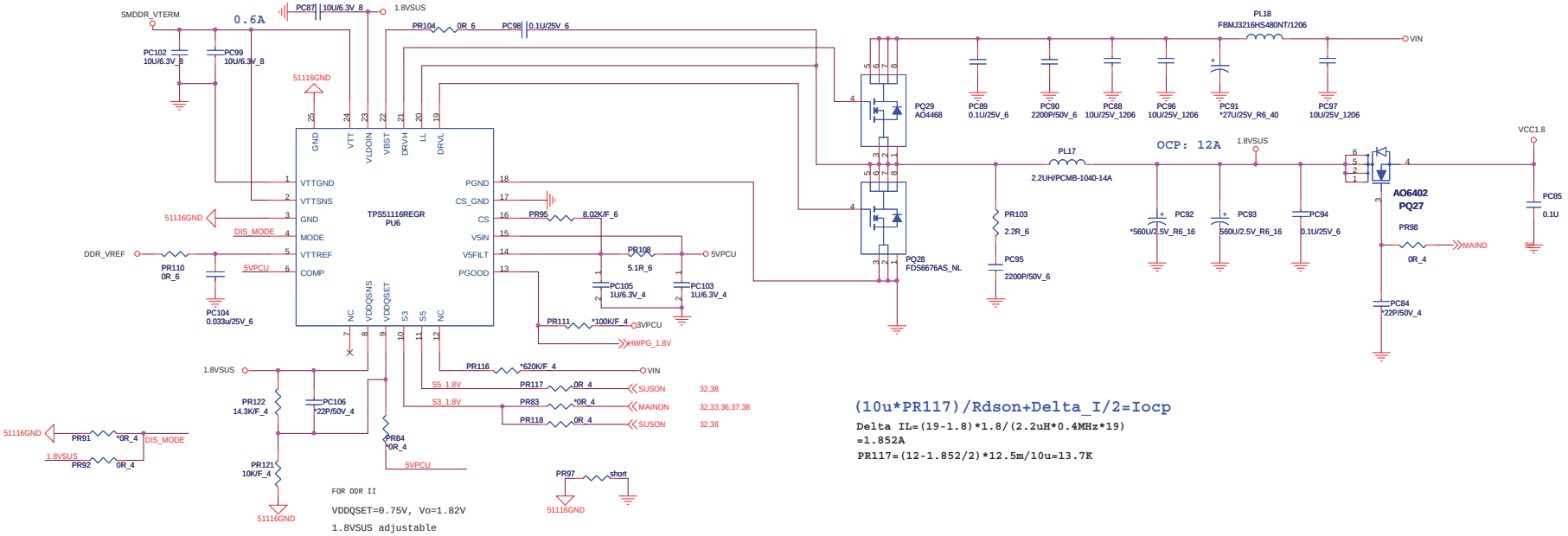
Quanta Computer Inc.			
PROJECT : ZN1			
Size	Document Number		Rev
	ACIN/ HDD_12V		1A
Date: Friday, May 08, 2009		Sheet 33 of 41	

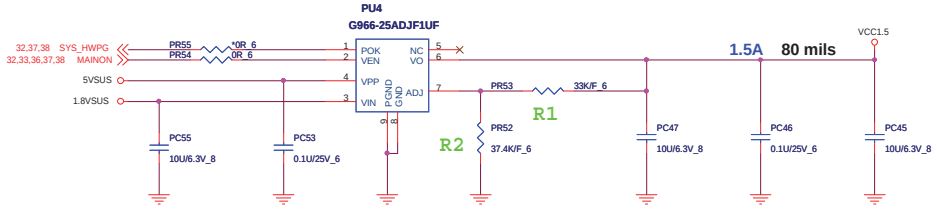
CPU_CORE and CPU_VDDNB_RUN



For AMD AM2 CORE

Quanta Computer Inc.		
PROJECT : ZN1		
Size	Document Number: CPU CORE(MAX8774)	Rev: 1A
Date: Friday, May 08, 2009	Sheet 34 of 41	

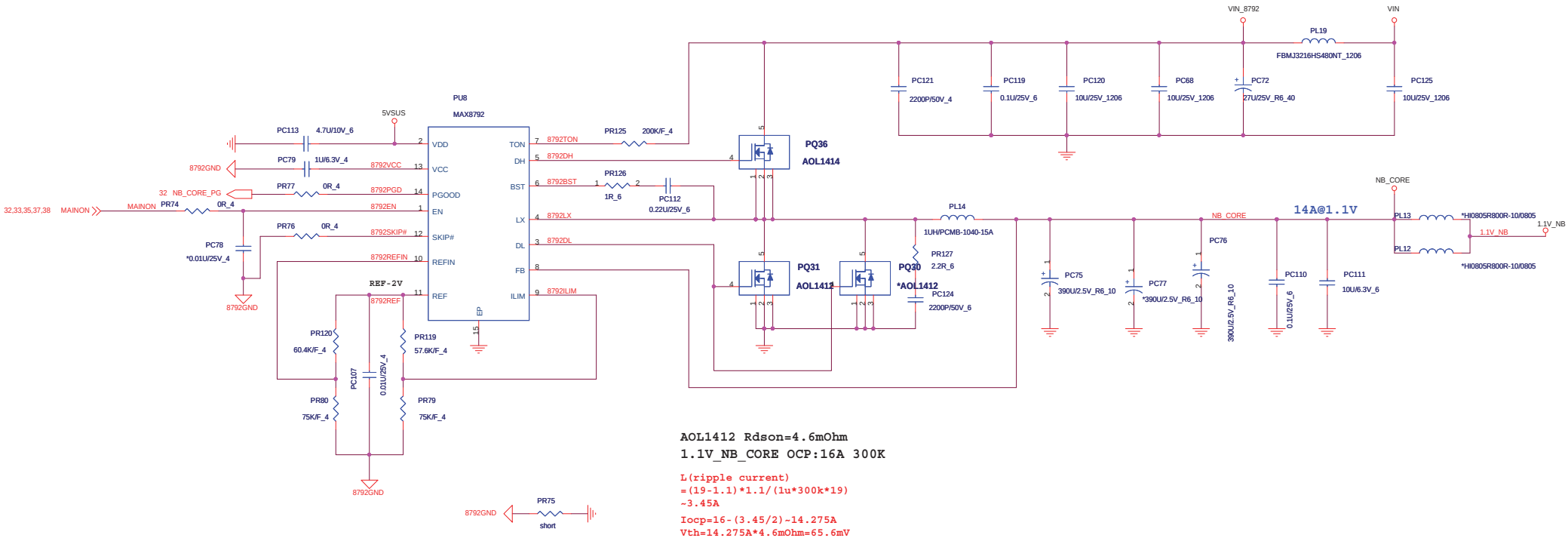




Quanta Computer Inc.

PROJECT : ZN1

Size	Document Number	Rev
	DDR 1.8V(TPS51116&VTERM)	2B
Date: Friday, May 08, 2009	Sheet 35 of 41	



AOL1412 Rdson=4.6mOhm

1.1V_NB_CORE OCP:16A 300K

L(ripple current)
=(19-1.1)*1.1/(1u*300k*19)
~3.45A

Iocp=16-(3.45/2)~14.275A
Vth=14.275A*4.6mOhm=65.6mV

Quanta Computer Inc.

PROJECT : ZN1

Size	Document Number	Rev
	POWER_VGA_CORE	A

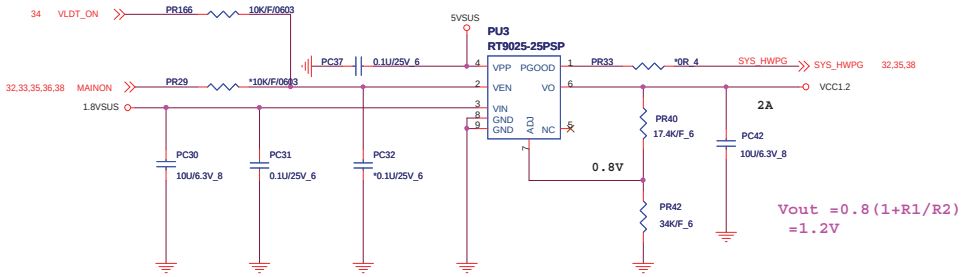
Date: Friday, May 08, 2009 Sheet 36 of 41

VCC1.2 & VCC1.2SB

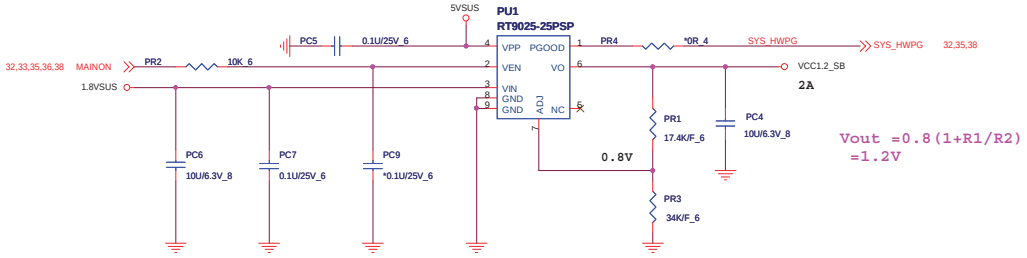
Change netlist for HT BUS power

Vender suggest

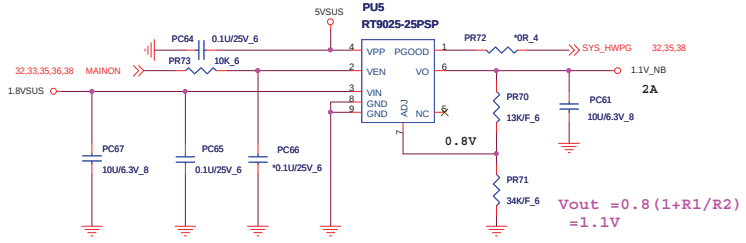
Colsed to CPU/NB



Colsed to SB



Colsed to NB



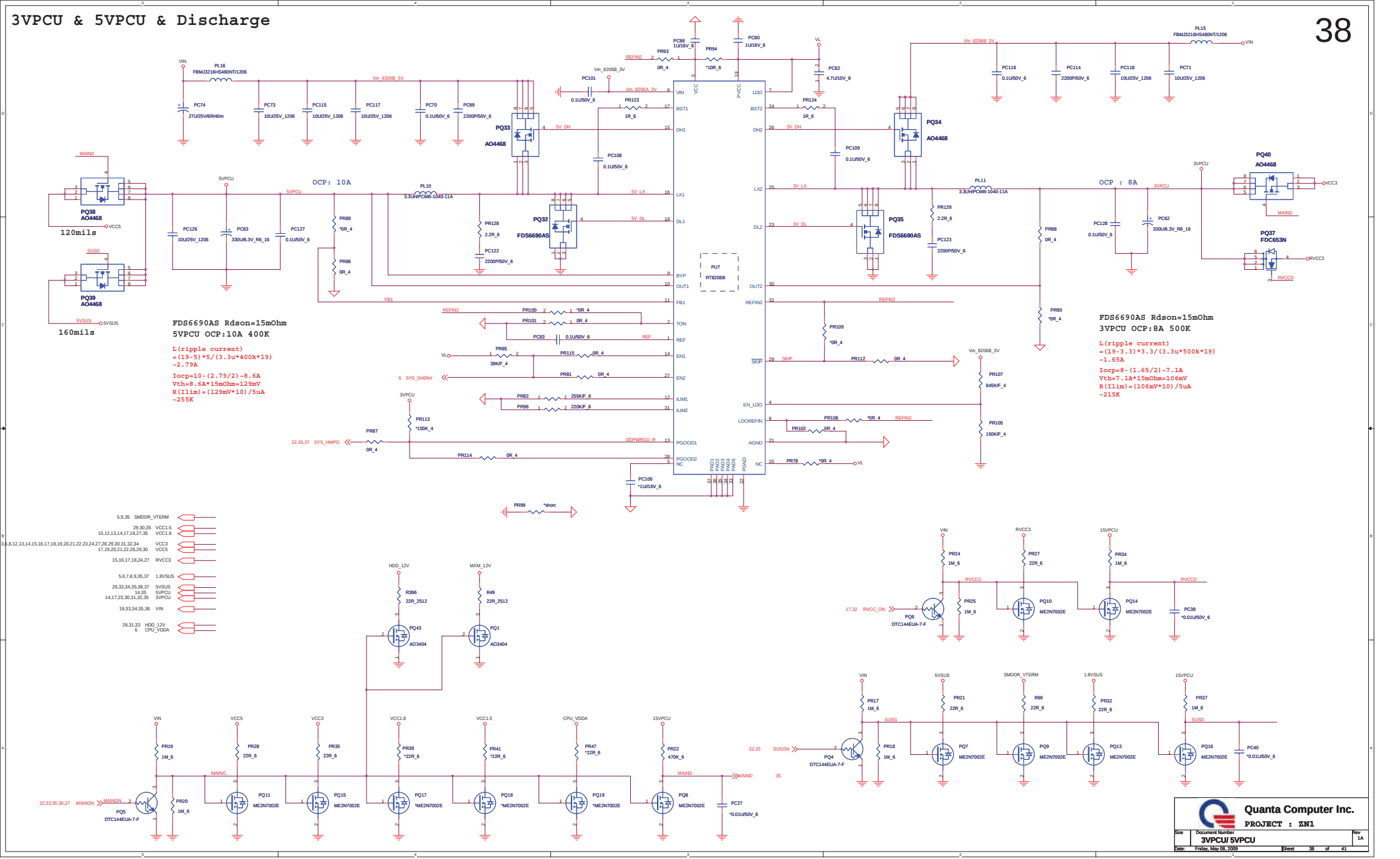
Quanta Computer Inc.

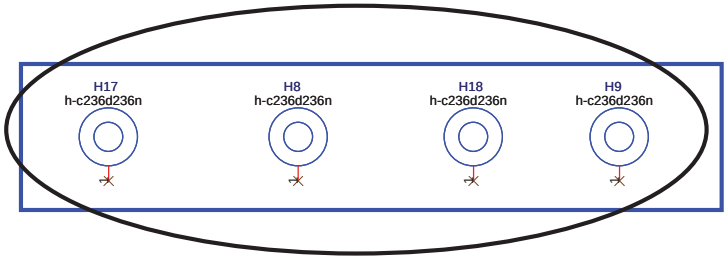
PROJECT : ZN1

Size	Document Number	Rev
	VCC1.2	1A

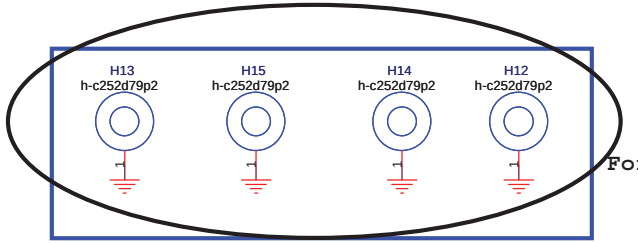
Date: Friday, May 08, 2009 Sheet 37 of 41

3VPCU & 5VPCU & Discharge

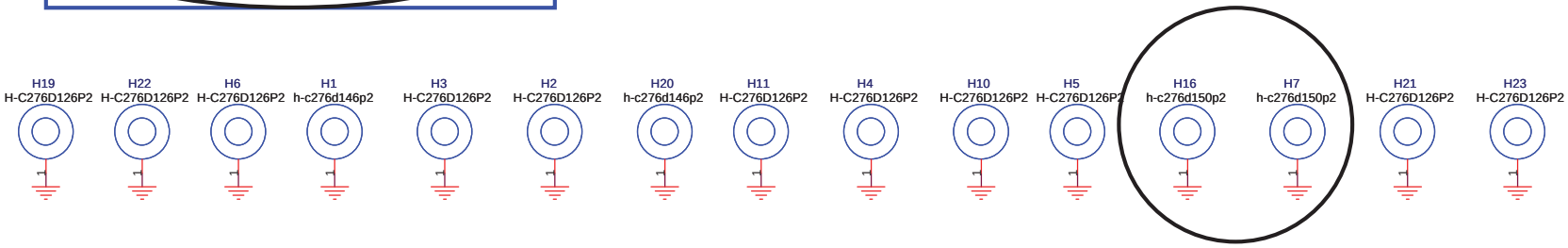




For cpu



For mini card



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	SCREW HOLE & EMI	A

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DATE	Description	Note	Page
2009 0320	1.change RP1-RP9 to 47 ohm (AMD suggestion)----PAGE 3 2.add R448 10k to VCC3---PAGE 6 3.add R101 300ohm to 1.8VSUS---PAGE 6 4.add R449 10K ohm to VCC3---PAGE12 5.Reserve C612,C613,R441,Y6 to schmatic---page14 6.add D59 and R446 10k to VCC3---page14 7.add R455,C621,C622 to schmatic for EMI---page14 8.add write EDID rom net to control ---page15 9.delete R403 and R32 --page 15 10.change C91,c95 value to 33p---page 16 11.Add 2 short pin for clear cmos and clear password --page16 12.add R86 10k--page 18 13.delete D4,D5 ,C68 component and add R69 0ohm---page18 14.change netlist to SB control (write_edid _rom)and add R62 2.2k ohm--- page19 15.change Q8 control pin to main pin---page 20 16.change MXM reset from pltrst.---page20 17.add ine out mute function---page23 add component ar35,ar36,ar37,ac38,aq1,aq2,ad2,ad3,q34,q35,r450,r452--page23 18.delete Q26,c475 and change LANVCC net to RVCC3 to control ---page24 19.change C447,C448 to 33p---page 24 20.change CN13 footprint for LED pin change---page 25 21.add ESD protect RV17,RV19,RV13,RV15,RV14,RV16, RV18,RV20,RV9,RV10,RV11,RV12---PAGE 26 22.Change CN25,CN26 footprint for ME---page26 23.add D18,D19 for XD detect and change net SD_WP#/XD_WP for SD write protect ---page27 24.change LED2 to Green type---page 27 25.change CN8 to rightangle and change odd connect to vertical type for ME---page 28 26.change au6 to OR-gate from AND-gate for pop sound---page 29 27.change fan control net from Vender suggestion.---page 31 28.add c614--618 0.1u for EMI--- page 31 29.add pr165 ,led3 for power line in ---page33 30.change VLDT_ON net for power on sequence--PAGE 34 31.change pr137,pr138 type to BOM---page 34	B2B	
	33.LED RT value need to change		

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DATE	ZN1 Board file	ZN1 Schematic
11th Mar. 2009	ZN1-0311-17-152.brd	AH1_A_FEB23_01.DSN
31th Mar. 2009	ZN1-0325-1830.brd	ZN1_B_HP_MAR31.DSN

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