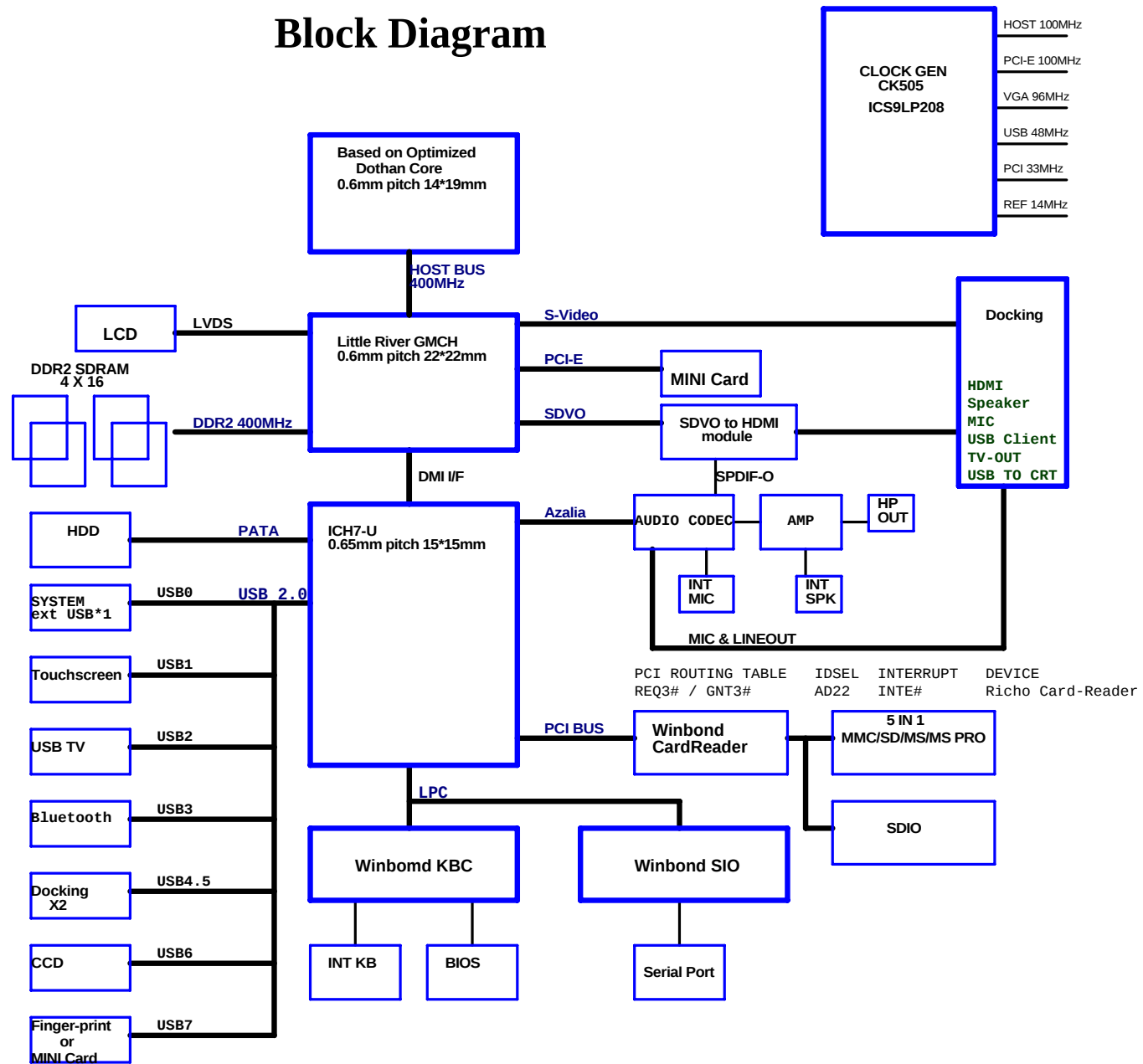
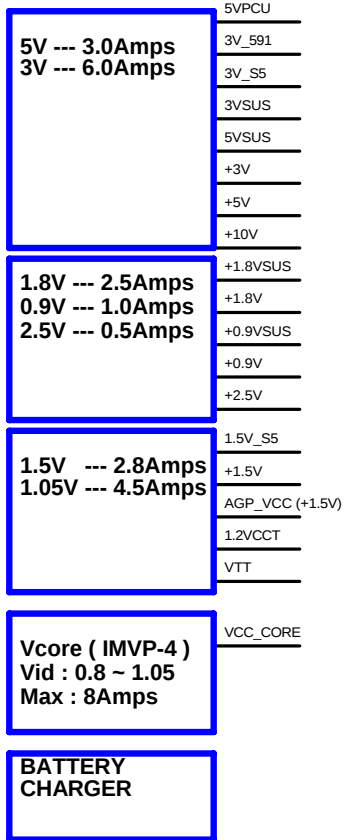
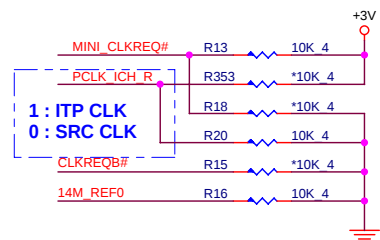
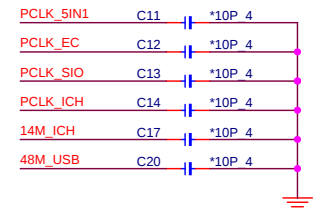
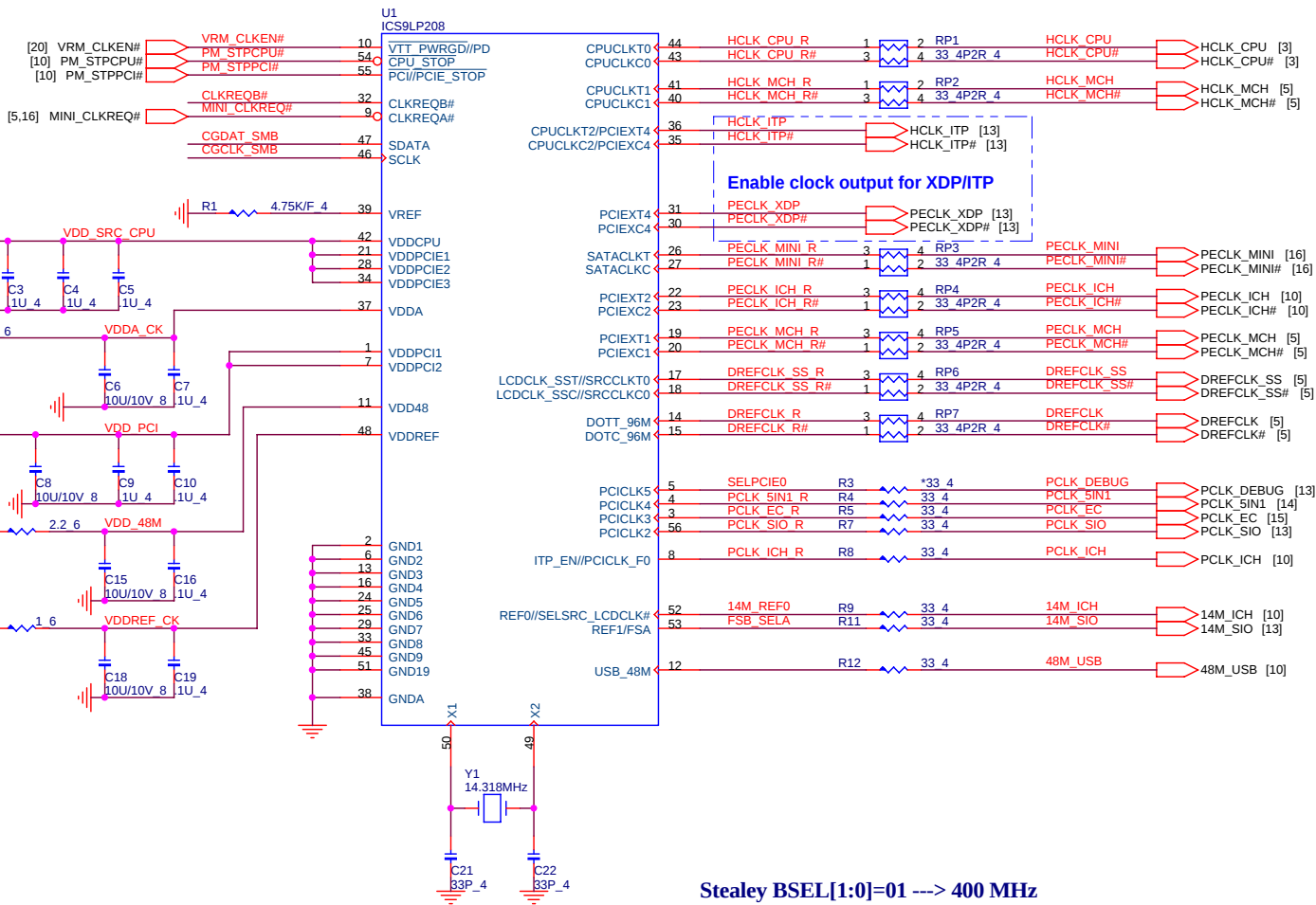
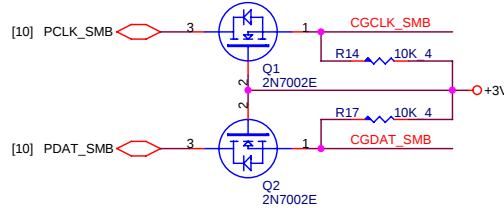
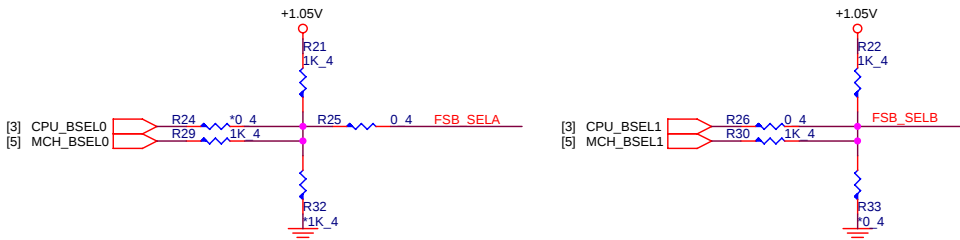


Block Diagram





Stealey BSEL[1:0]=01 ----> 400 MHz
CK505 BSEL[2:0]=101 ----> 400 MHz
ICS9LP208 FSA=1 ----> 400 MHz
FSA=0 ----> 533 MHz





QUANTA COMPUTER
HW Engineer :

Title

Clock Generator - ICS9LP208

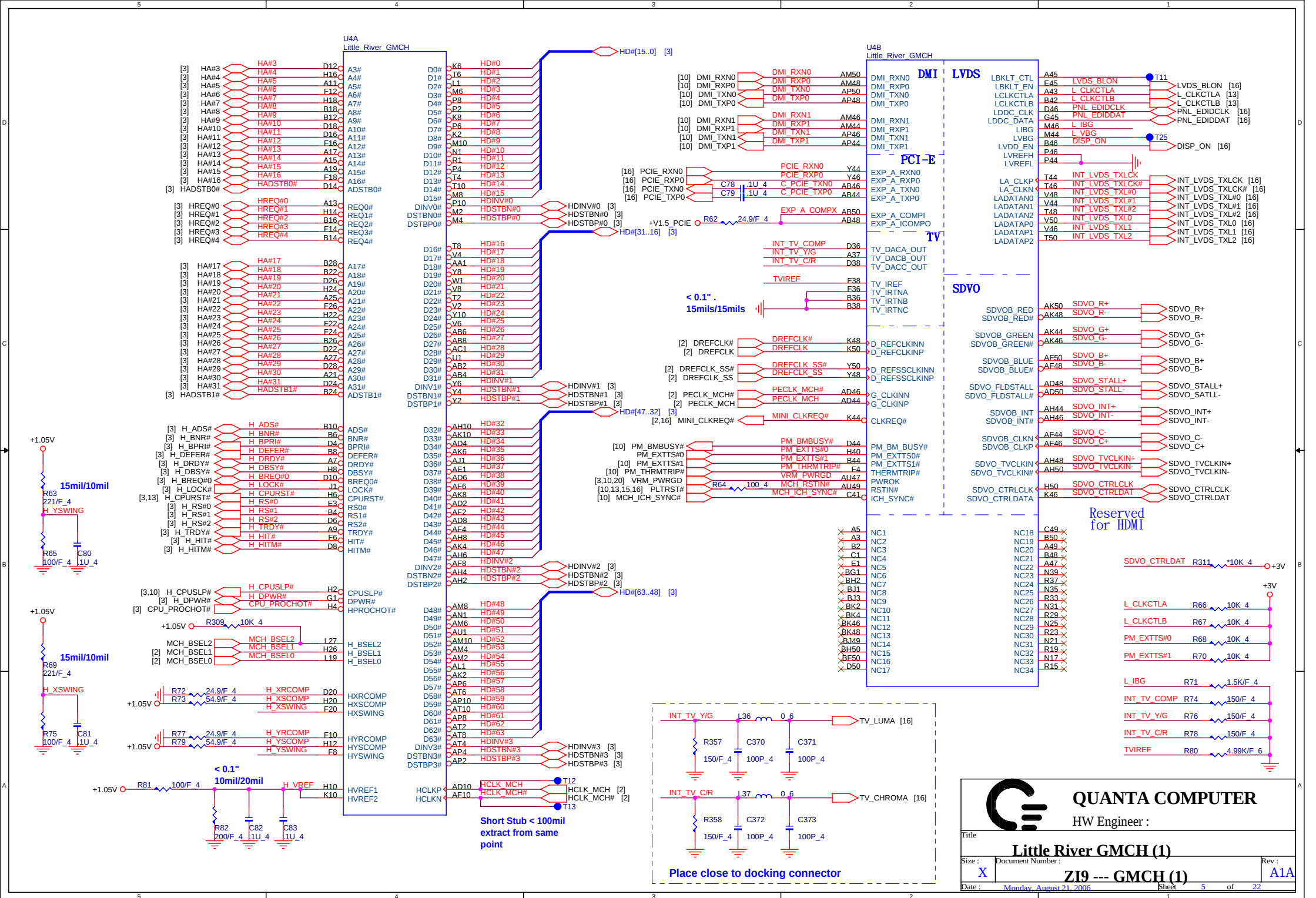
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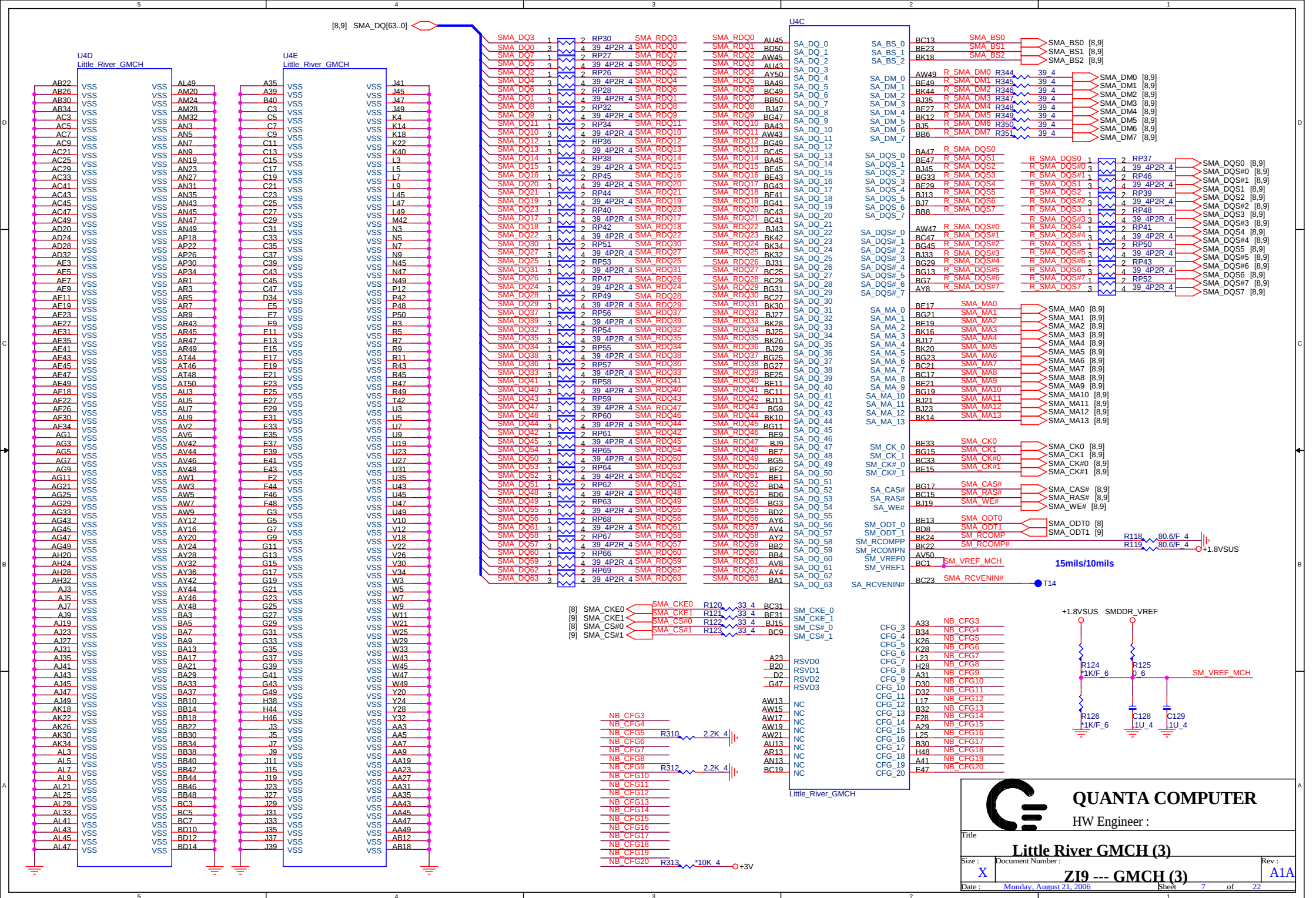
Document Number :

Rev : A1A

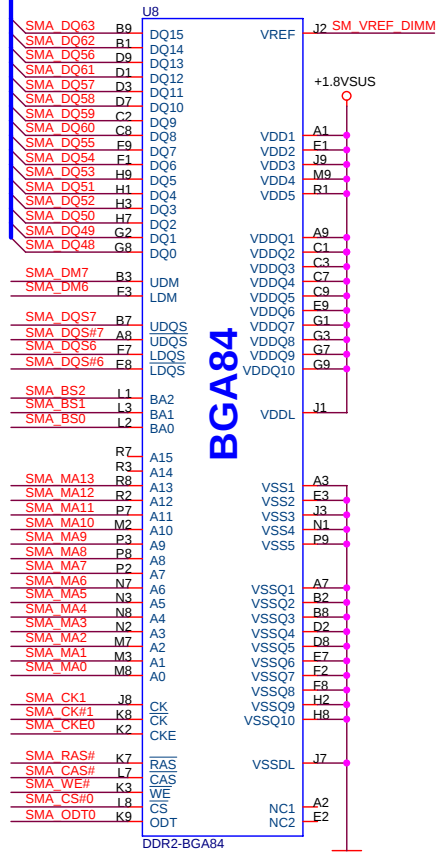
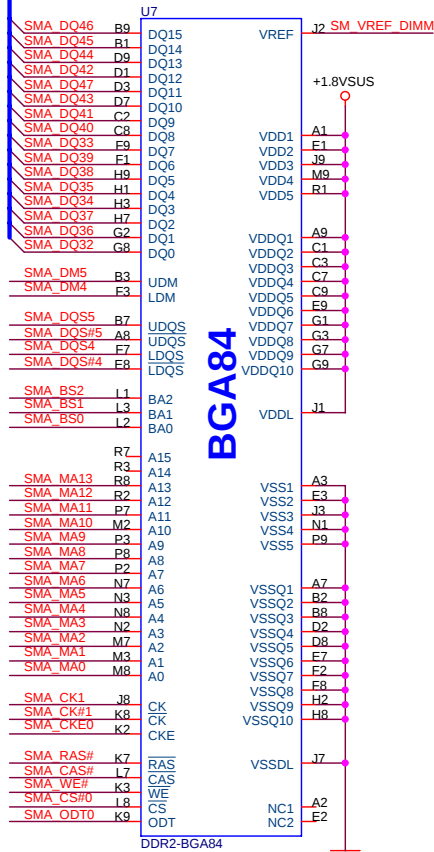
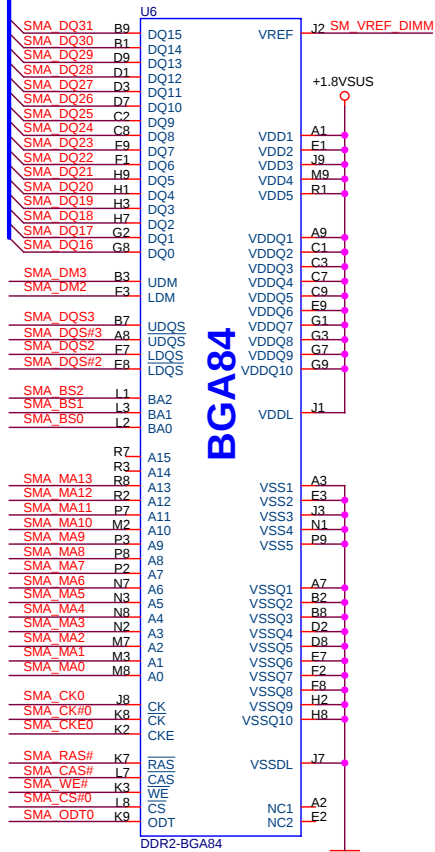
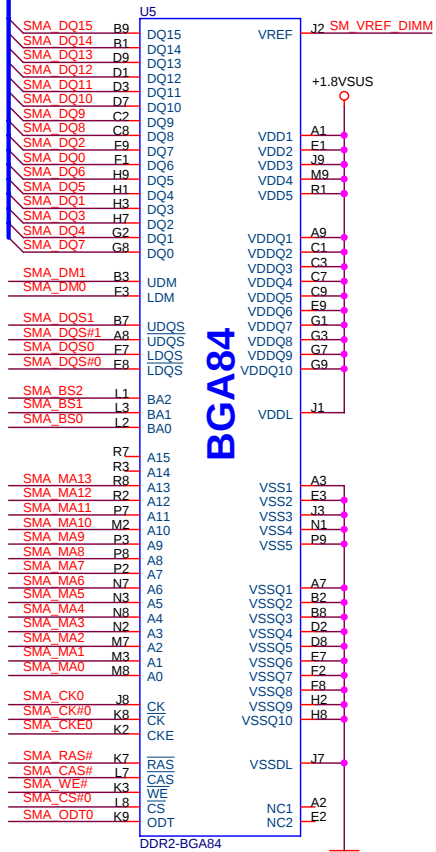
Date : Monday, August 21, 2006

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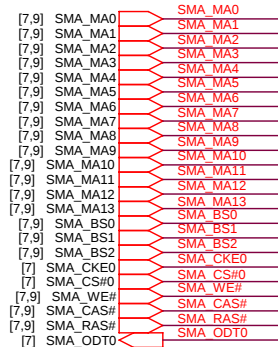
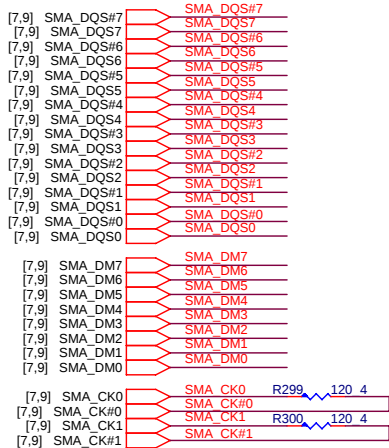




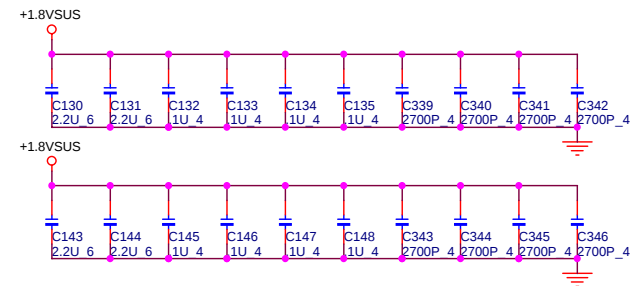
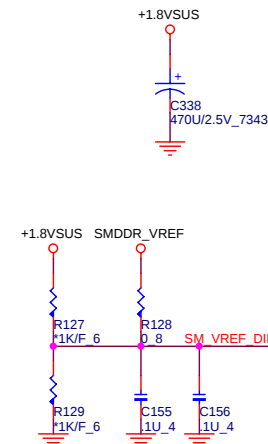
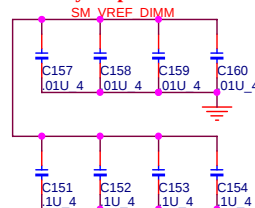
[7.9] SMA_DQ[63..0]



[9] SM_VREF_DIMM



one Cap close to each memory chip



QUANTA COMPUTER

HW Engineer :

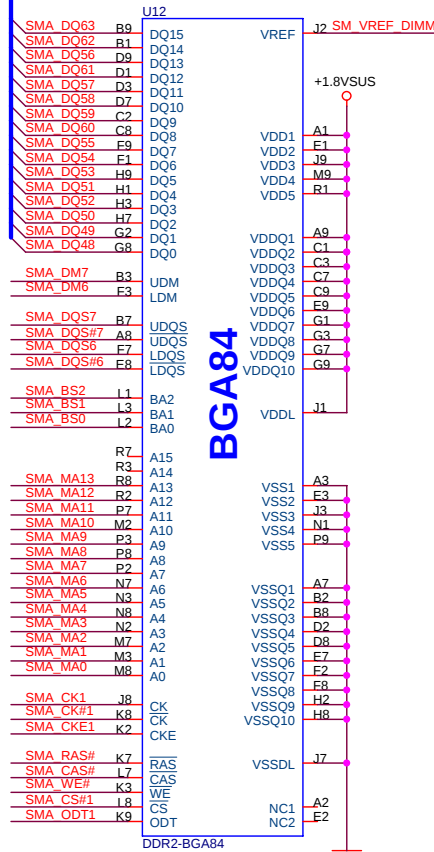
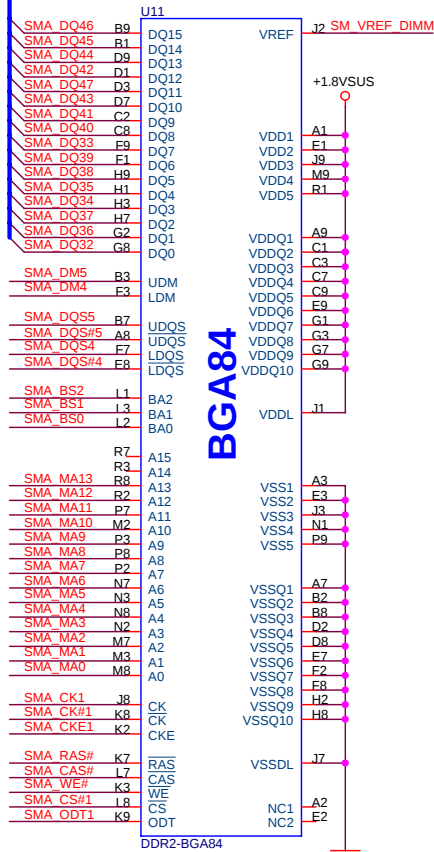
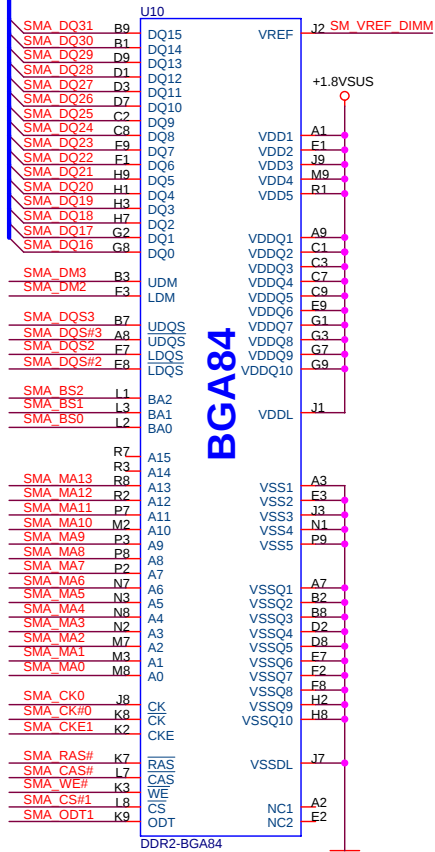
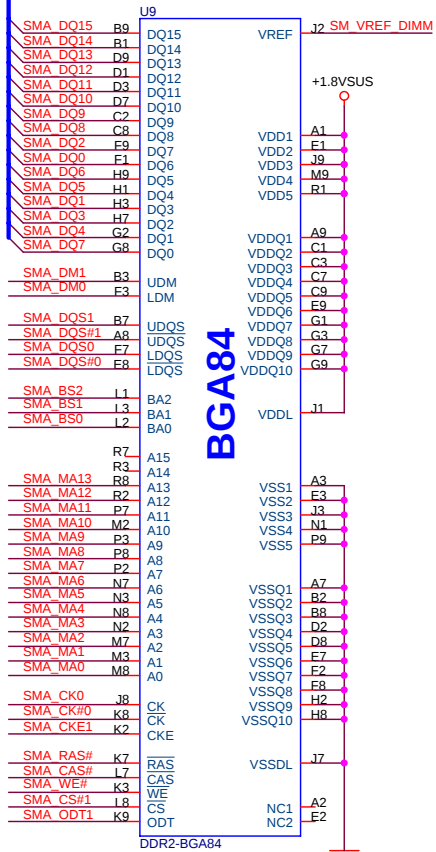
Title

DDRII Memory 4x16 --- (1)

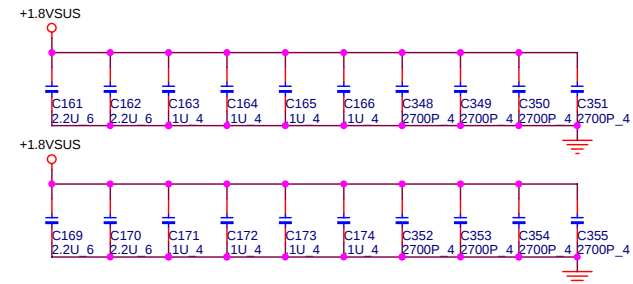
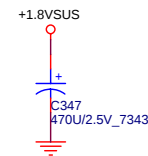
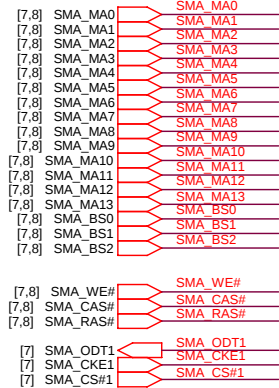
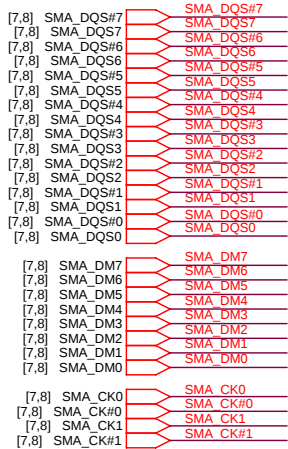
Size: X Document Number: **ZI9 --- DDRII Memory** Rev: **A1A**

Date: Monday, August 21, 2006 Sheet 8 of 22

[7,8] SMA_DQ[63..0]



[8] SM_VREF_DIMM



 **QUANTA COMPUTER**

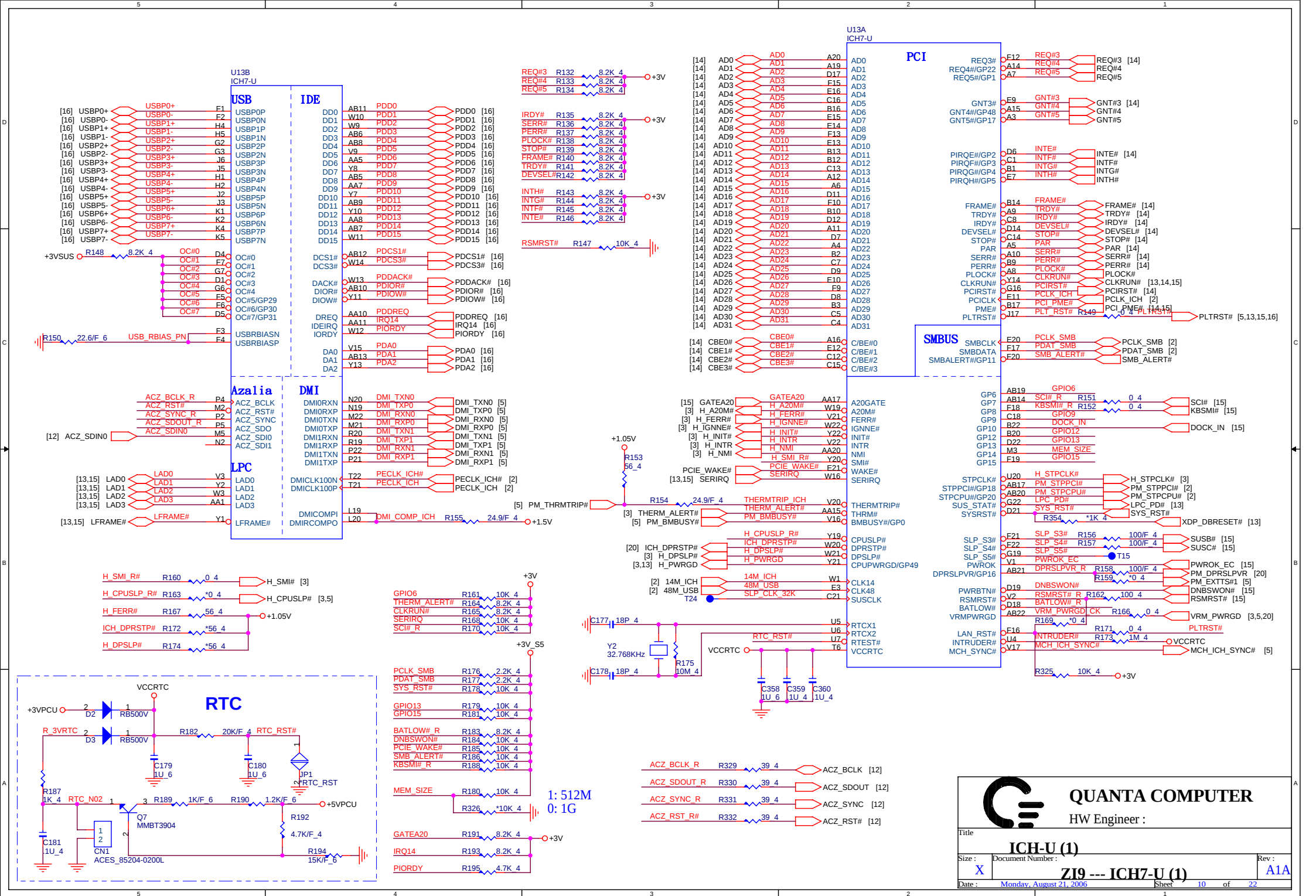
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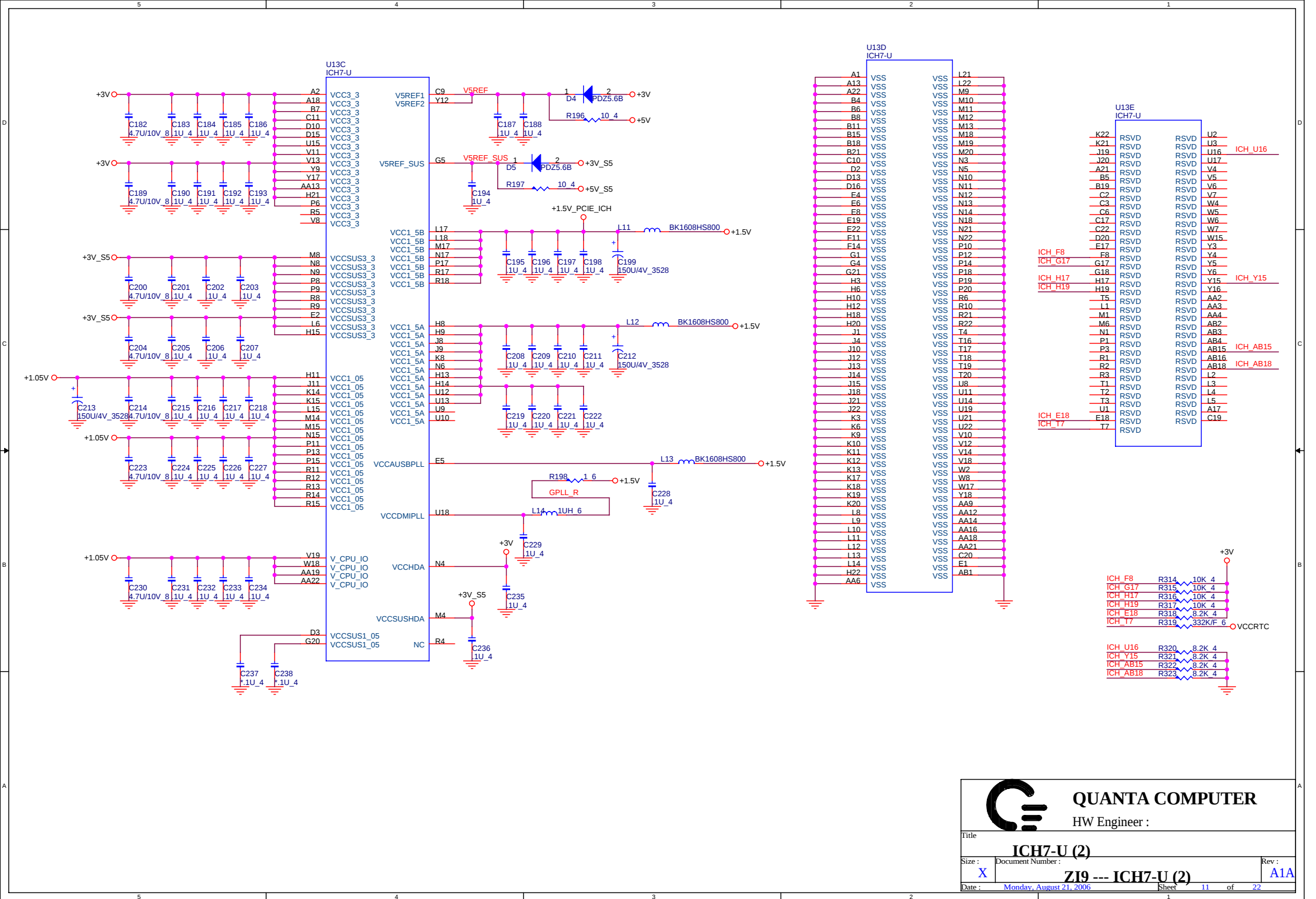
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DDR2 Memory 4x16 --- (2)

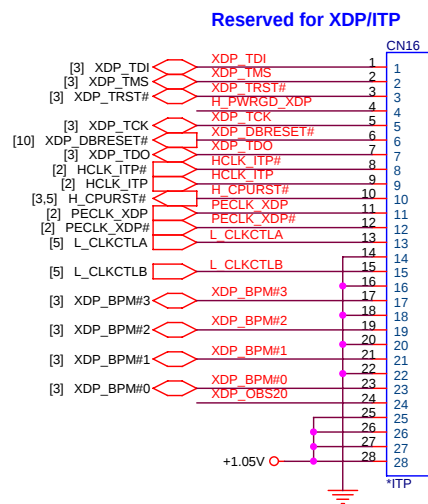
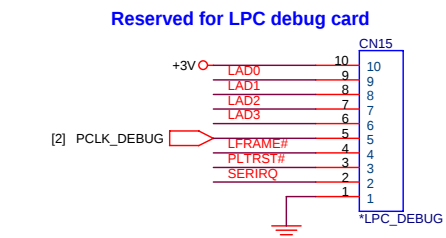
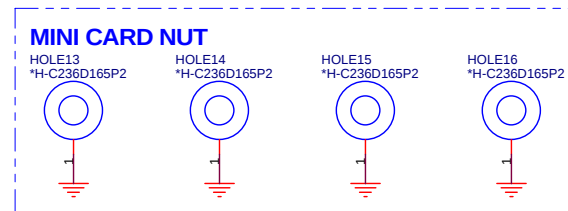
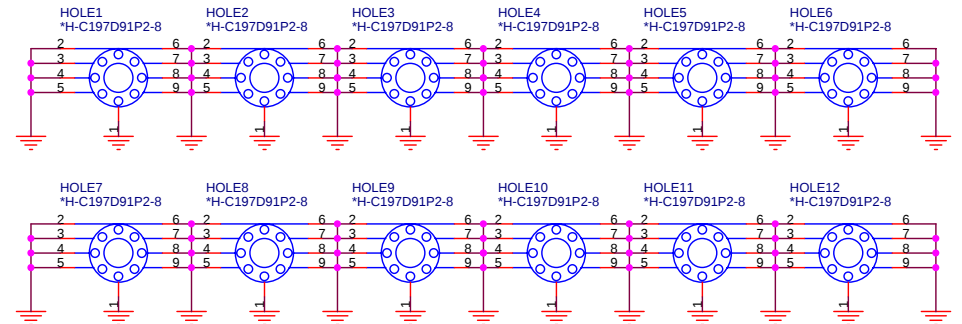
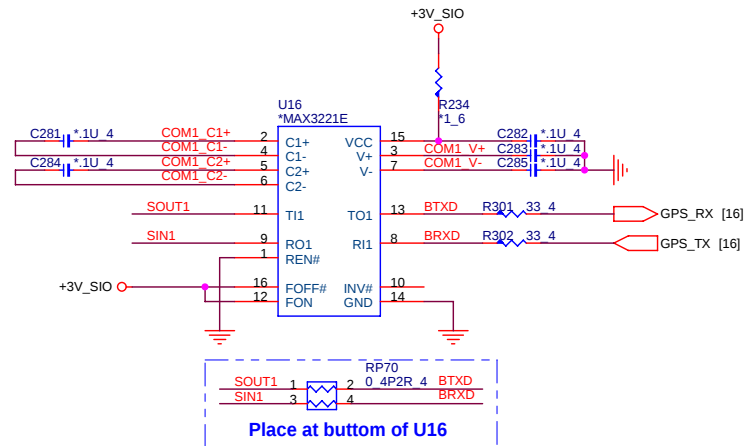
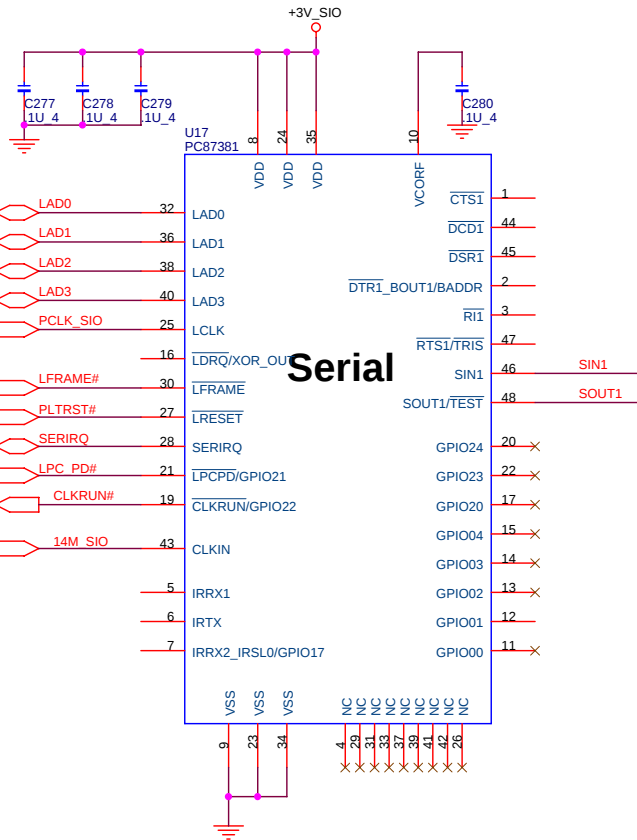
Size : X Document Number : ZI9 --- DDR2 Memory Rev : A1A

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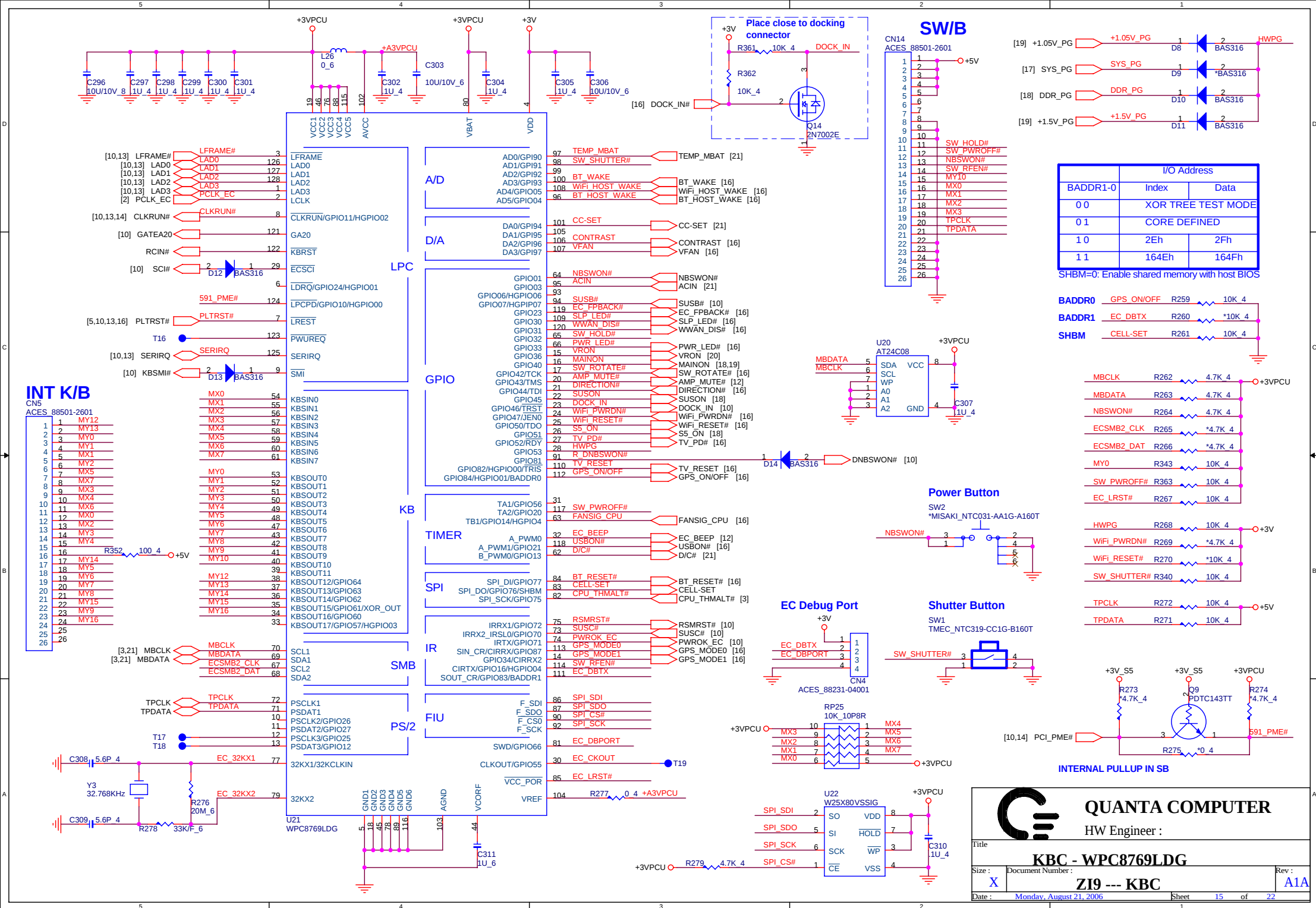




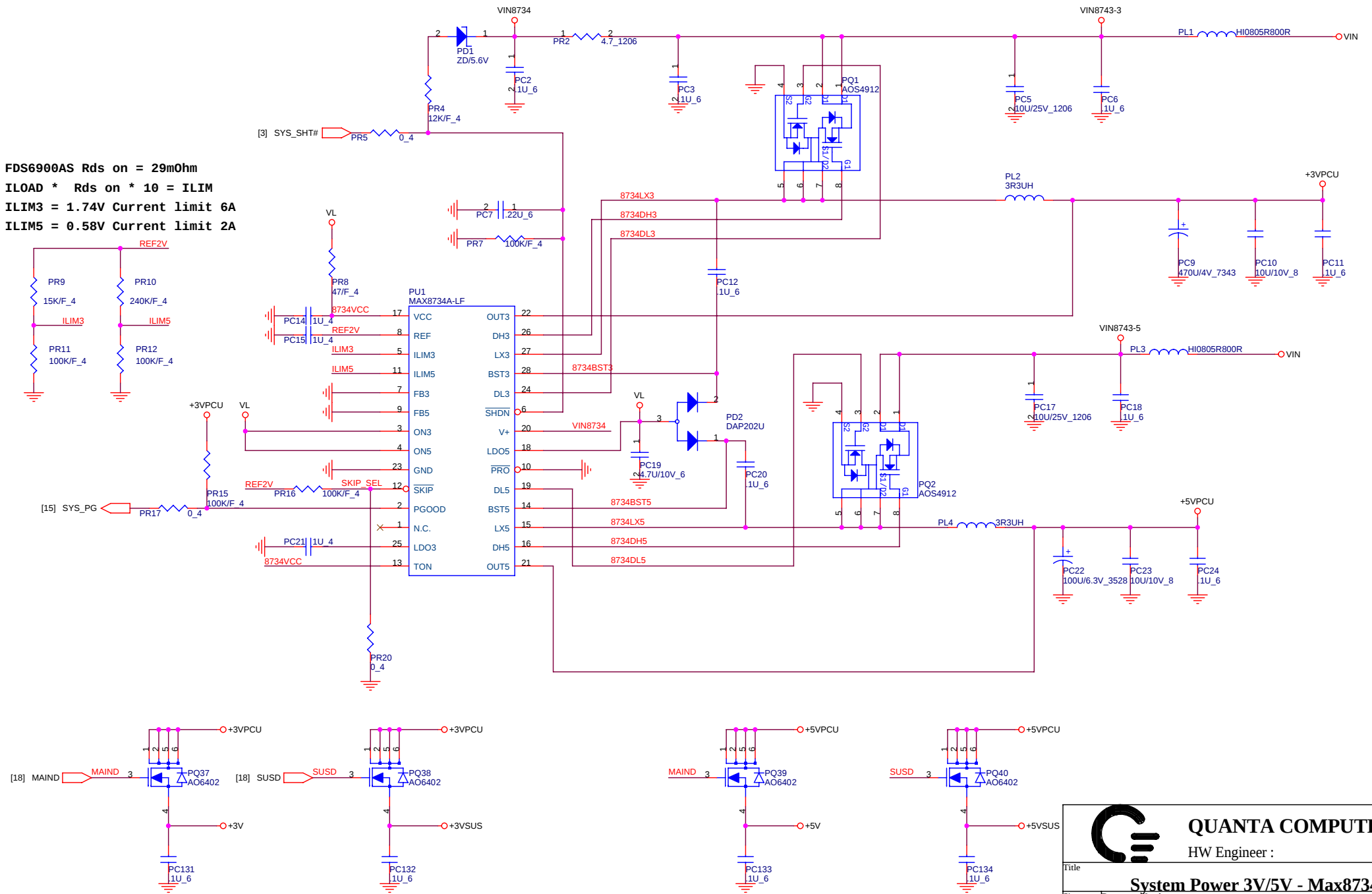
+3V L23 0 8 +3V_SIO



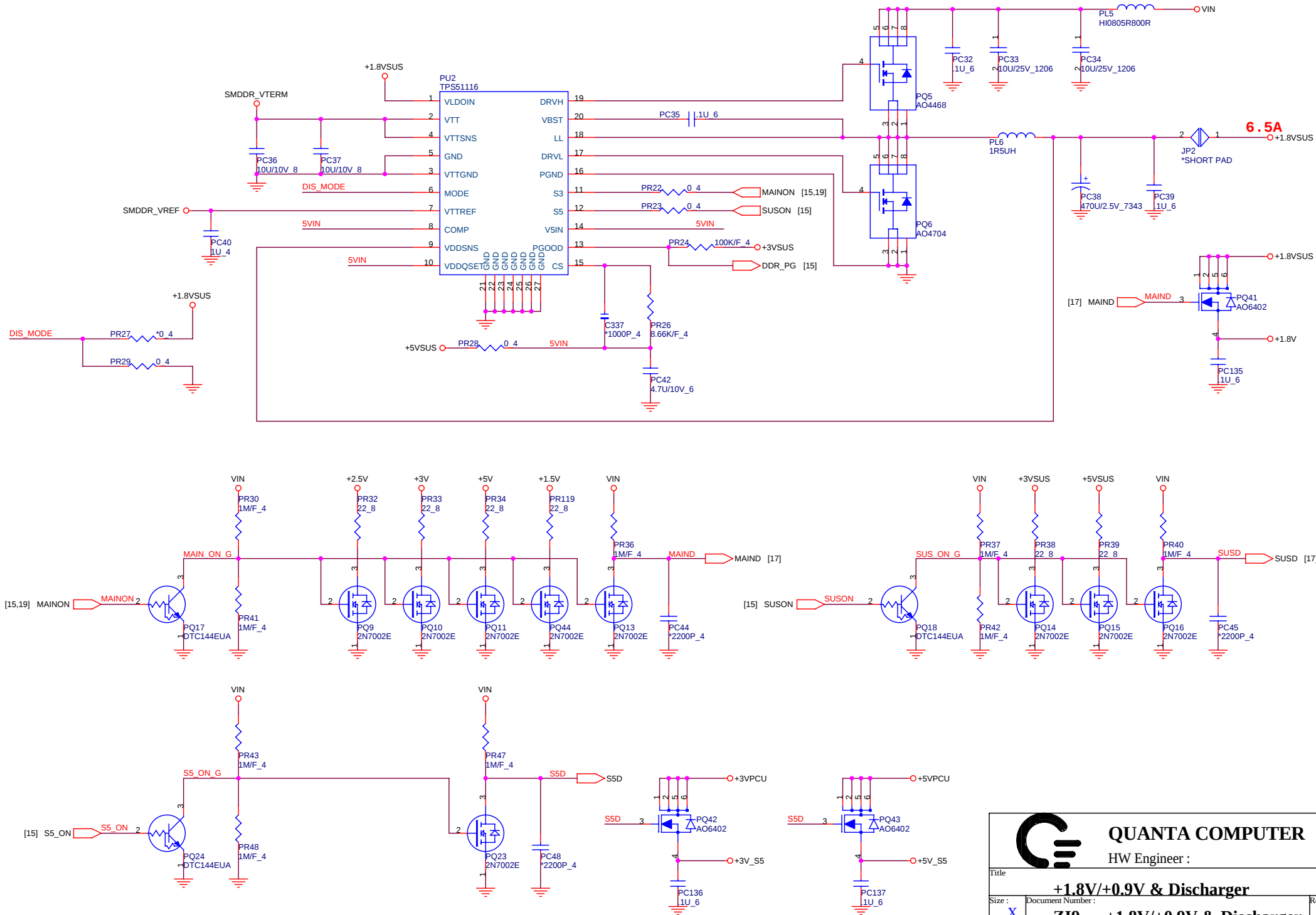
		QUANTA COMPUTER	
		HW Engineer :	
Title			
Serial Port - NS87381			
Size :	Document Number :	Rev :	
X	ZI9 --- Serial Port	A1A	
Date :	Monday, August 21, 2006	Sheet	13 of 22

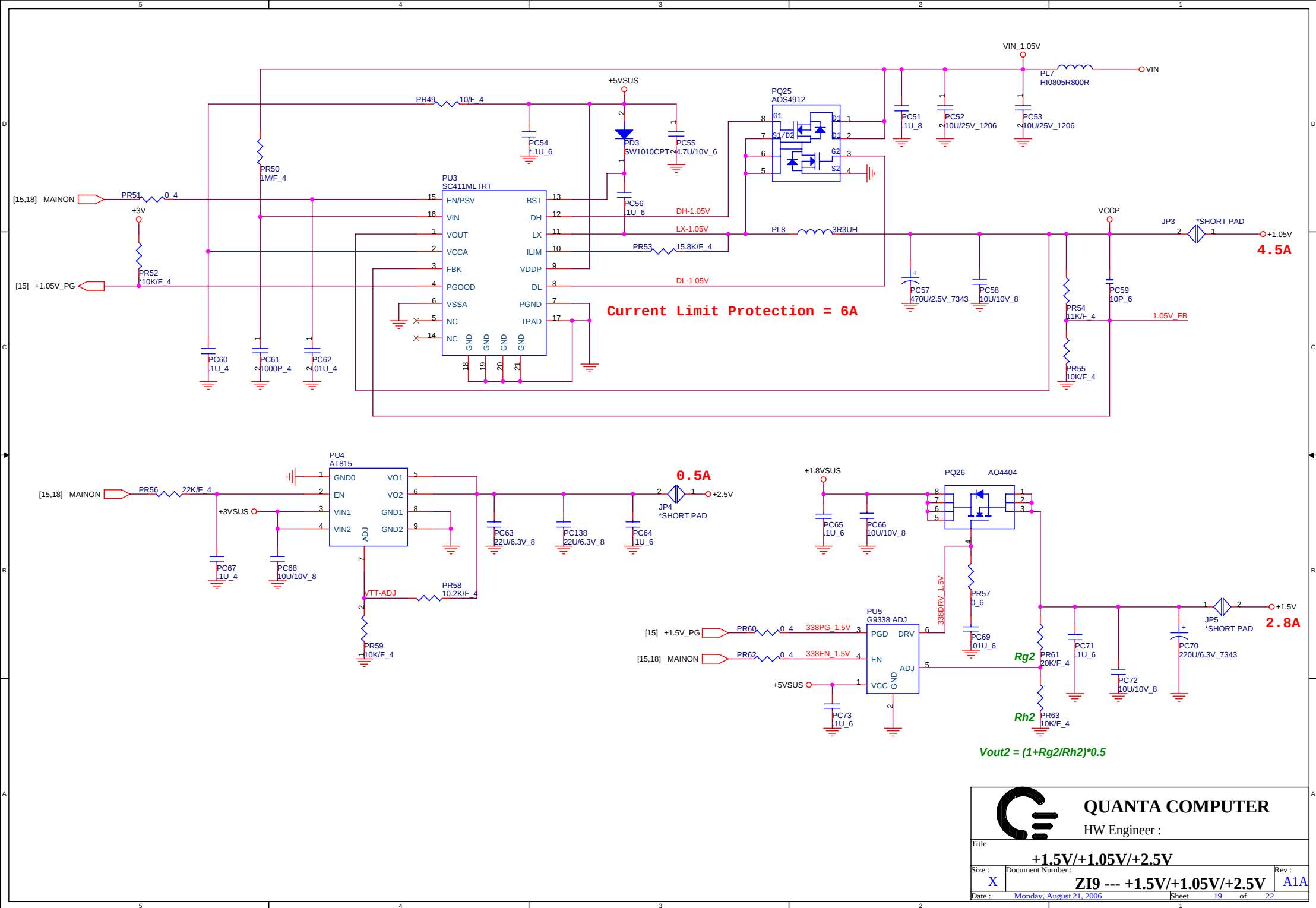


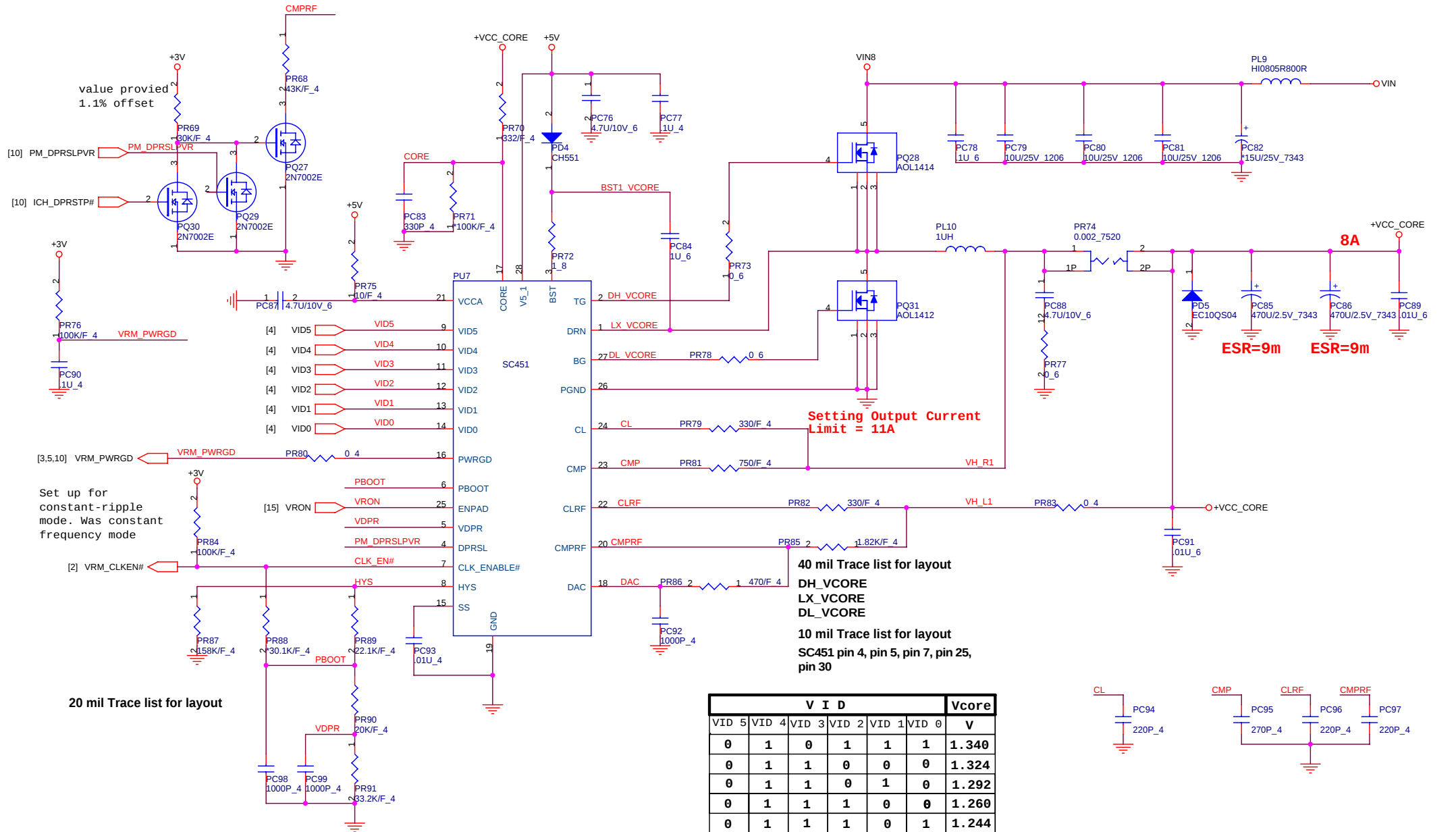
FDS6900AS Rds on = 29mOhm
 ILOAD * Rds on * 10 = ILIM
 ILIM3 = 1.74V Current limit 6A
 ILIM5 = 0.58V Current limit 2A



 QUANTA COMPUTER HW Engineer :		Title	
		System Power 3V/5V - Max8734A	
Size : X	Document Number :	Rev : A1A	
Date : Monday, August 21, 2006	Sheet 17	of 22	







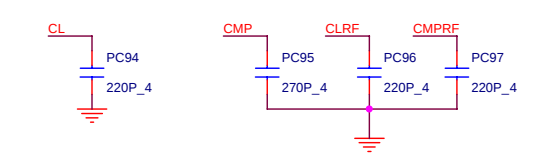
20 mil Trace list for layout

Setting Output Current Limit = 11A

40 mil Trace list for layout

10 mil Trace list for layout

V I D						Vcore
VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	V
0	1	0	1	1	1	1.340
0	1	1	0	0	0	1.324
0	1	1	0	1	0	1.292
0	1	1	1	0	0	1.260
0	1	1	1	0	1	1.244
0	1	1	1	1	1	1.212
1	0	0	0	0	1	1.180
1	0	0	0	1	1	1.148
1	0	1	0	0	1	1.052
1	0	1	0	1	1	1.020
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QUANTA COMPUTER

HW Engineer :

Title

CPU Vcore - SC451

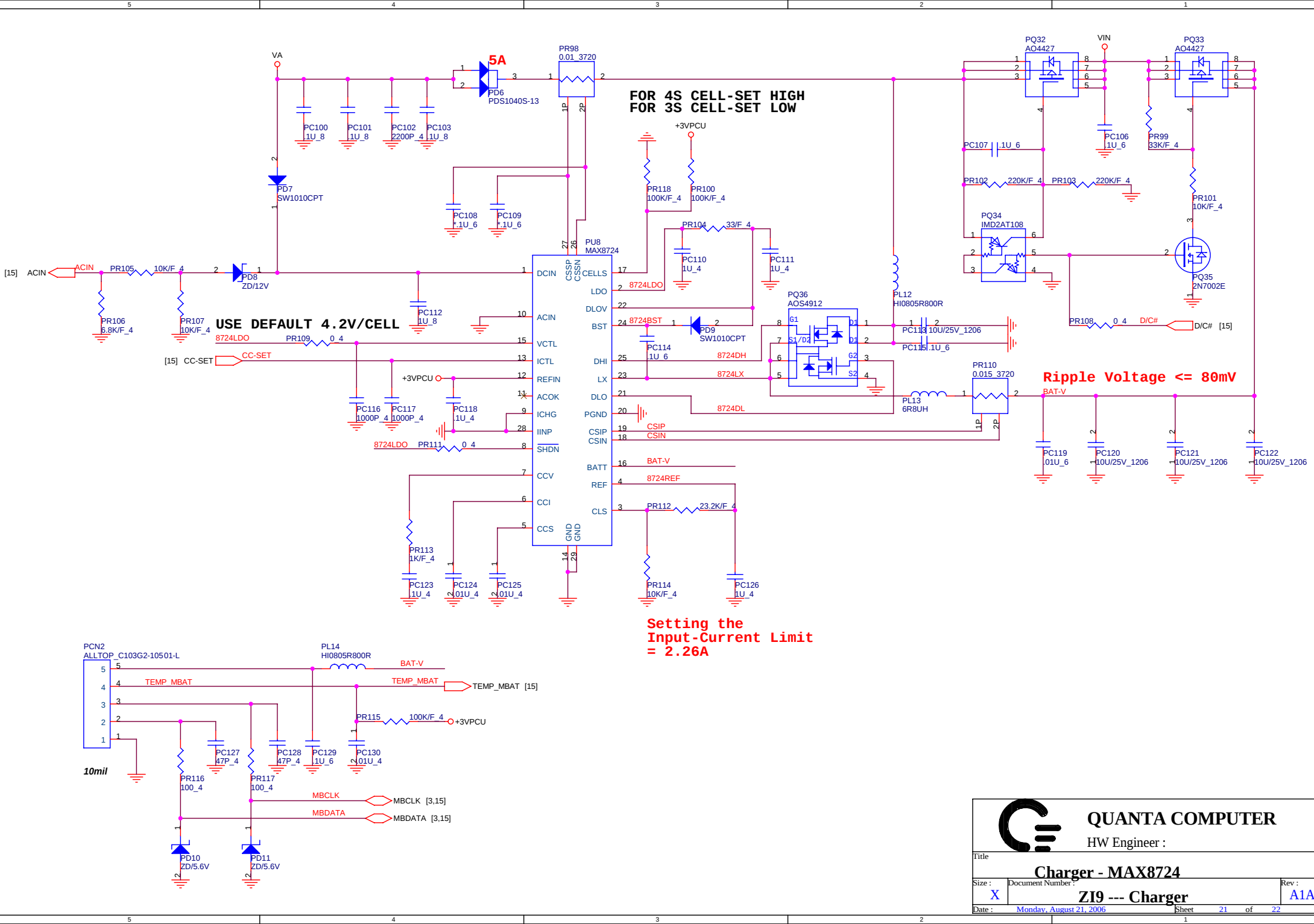
Size : X

Document Number : ZI9 --- CPU Vcore

Rev : A1A

Date : Monday, August 21, 2006

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ZI9 MotherBoard		A1A	FIRST RELEASE				PAGE	FROM	TO	
							1		A1A	
							2		A1A	
							3		A1A	
							4		A1A	
							5		A1A	
							6		A1A	
							7		A1A	
							8		A1A	
							9		A1A	
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							16		A1A	
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							18		A1A	
							19		A1A	
							20		A1A	
							21		A1A	
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Size	Document Number		Rev		MB ASSY'S P/N : 31ZI9MBXXX		PROJECT LEADER: SAINT LIN			
Change List		A1A				DOCUMENT NO:		DATE :2006/08/21		
Date: Monday, August 21, 2006			Sheet	22	of	22				