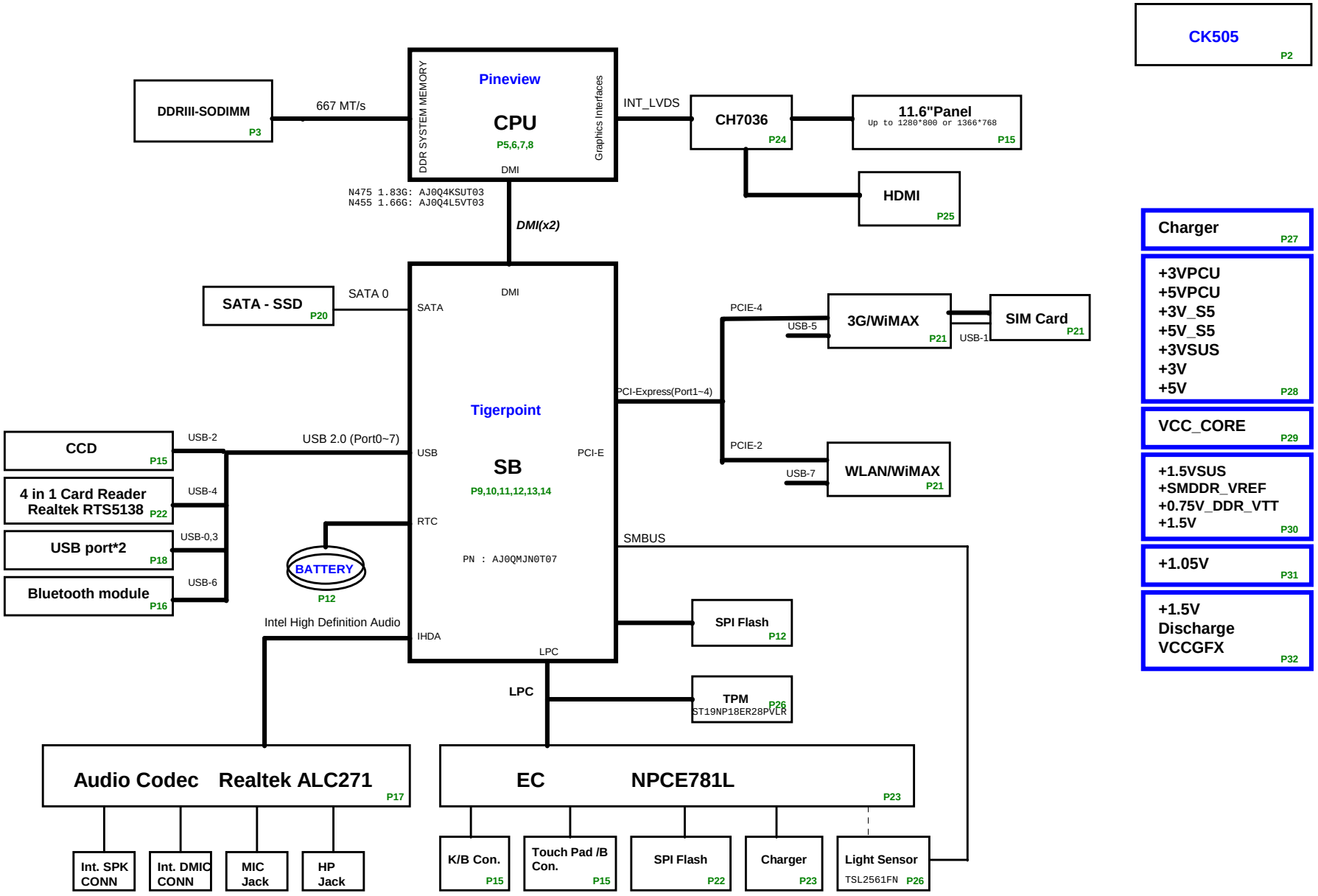
ZGA Block Diagram



Quanta Computer Inc.
PROJECT : ZGA

Size	Document Number	Rev
	Block Diagram	1B

Date: Wednesday, July 07, 2010 Sheet 1 of 38

Clock Generator(CLK)

02

The Beads for power 3.3V/1.05 are for EMI solution.
It is recommended to add it for better power/EMI performance.

0.08A

+1.05V_VDD

PBY160808T-301Y-N/2A/300ohm_6

L32 (+3V) — L31 PBY160808T-301Y-N/2A/300ohm_6 (+1.05V)

C346 *0.1u/10V_4
C356 *0.1u/10V_4
C350 *10u/10V_8
C364 0.1u/10V_4
C348 0.1u/10V_4
C377 0.1u/10V_4
C361 0.1u/10V_4
C380 10u/10V_8

C378 *10u/10V_8
C379 10u/10V_8
C360 0.1u/10V_4
C369 0.1u/10V_4
C375 0.1u/10V_4
C376 0.1u/10V_4
C371 0.1u/10V_4
C367 *0.1u/10V_4

VDD_CK_VDD_REF 0.25A

+1.05V_VDD

U25 CK505 SLG8SP513

9	VDD_PCI	NC	55
16	VDD_48	SCLK	7 SMBCK1
23	VDD_PLL3	SDA	6 SMBDT1
4	VDD_REF		
46	VDD_SRC	PCI_STOP#	45 PM_STPPCI# R420 *0_4 PM_STPPCI#
62	VDD_CPU	CPU_STOP#	44 PM_STPCPU#
19	VDD_96_IO	CPU0	61 CLK_CPU_BCLK (5)
27	VDD_PLL3_IO	CPU0#	60 CLK_CPU_BCLK# (5)
33	VDD_SRC_IO_1	CPU1	58 CLK_MCH_BCLK (5)
52	VDD_SRC_IO_3	CPU1#	57 CLK_MCH_BCLK# (5)
43	VDD_SRC_IO_2	SRC8/ITP	54 CLK_PCIE_DMIP (5)
56	VDD_CPU_IO	SRC8#/ITP#	53 CLK_PCIE_DMIN (5)
8	PCI0/CR#_A	SRC10	41 CLK_PCIE_Dec (26)
10	PCI1/CR#_B	SRC10#	42 CLK_PCIE_Dec# (26)
11	PCI2/TME	SRC11/CR#_H	40 CLKREQ_Dec# R416 475/F_4 CLKREQ_Dec# (26)
12	PCI3	SRC11#/CR#_G	39 T62
13	PCI4/27M_Select	SRC9	37 T63
14	PCI_F5/ITP_EN	SRC9#	38 T64
3	XTAL_IN	SRC7/CR#_F	51 CLK_PCIE_ICH (9)
2	XTAL_OUT	SRC7#/CR#_E	50 CLK_PCIE_ICH# (9)
17	USB_48/FSA	SRC6	48 CLK_PCIE_SATA (10)
64	FSB/TEST_MODE	SRC6#	47 CLK_PCIE_SATA# (10)
5	REF0/FSC/TESTSEL	SRC4	34 PE2CLK+ (21)
65	VSS_BODY	SRC4#	35 PE2CLK- (21)
15	VSS_PCI	SRC3/CR#_C	31 CLKREQ_3G# R404 475/F_4 CLKREQ_3G# (21)
18	VSS_48	SRC3#/CR#_D	32 CLKREQ_WLAN# R409 475/F_4 CLKREQ_WLAN# (21)
22	VSS_IO	SRC2/SATA	28 PE4CLK+ (21)
26	VSS_PLL3	SRC2#/SATA#	29 PE4CLK- (21)
59	VSS_CPU	27M_NosSS/SRC1(LCDCLK)	24 DREFSSCLK (5)
30	VSS_SRC1	27M_SS/SRC1#(LCDCLK#)	25 DREFSSCLK# (5)
36	VSS_SRC2	SRC0/DOT96	20 DREFCLK (5)
49	VSS_SRC3	SRC0#/DOT96#	21 DREFCLK# (5)
1	VSS_REF	CKPWRGD/PWRDWN#	63 VR_PWRGD_CK410

1/19 : 439549_439549_CorbettPark_Schm_Rev0.5: If this pin is used as PCI_STOP#, it is required to provide a 10-k pull-up to Vcc3_3. It is not recommended to connect this signal to the Tiger Point(NM10) as it may cause unexpected system behavior.

To SB
To CPU (Core CLK)
To CPU (Host CLK)
To CPU (DMI CLK)
To Decoder
To SB (DMI CLK)
To SB (SATA CLK)
To Mini Card 1 (WLAN)
To Mini Card 2 (3G/Wimax)
To CPU (SS CLK)
To CPU (PLL CLK)

T53

(21) PCLK_DEBUG — R367 33_4 — PCLK_DEBUG_R
PCLK_2
(26) PCLK_TPM — R374 33_4 — PCLK_TPM_R
(23) LCLK_EC — R371 33_4 — PCLK_EC_R
(11) PCLK_ICH — PCLK_ICH R379 33_4 — PCLK_ICH_R

CG_XIN
CG_XOUT

(22) CLK_Card48 — R385 22_4 — FSA
(9) CLKUSB_48 — R384 22_4
CLK_BSEL0 R393 2.2K_4 — FSB
FSC
CLK_BSEL1 R386 1K_4
CLK_BSEL2 R376 10K_4
(12) 14M_ICH — R375 33_4

C349 33p/50V_4 — CG_XIN
CL=20p — Y4 — 14.318MHZ
C354 33p/50V_4 — CG_XOUT

<Layout note>
Crystal place within 500mil of CK505

SLG8SP513VTR ,ICS9LPRS365BKLFT

<MAIN> : SLG8SP513VTR(AL8SP513000)
<SECOND> : ICS9LRS3165BKLFT(AL003165000)
<SECOND> : ICS9LPRS365BKLFT(ALPRS365000)

CLKREQA# CONTROL SRC0(default) or SRC2
CLKREQB# CONTROL SRC1(default) or SRC4
CLKREQC# CONTROL SRC2
CLKREQD# CONTROL SRC4
CLKREQE# CONTROL SRC6
CLKREQF# CONTROL SRC8
CLKREQG# CONTROL SRC9
CLKREQH# CONTROL SRC10

+3V — R365 10K_4 — PCLK_2
R366 *10K_4
+3V — R363 *10K_4 — PCLK_EC_R
R361 10K_4
+3V — R378 *10K_4 — PCLK_ICH_R
R377 10K_4

	SLG8SP513VTR (AL8SP513000)	ICS9LPRS365 (ALPRS365000)	PULL HIGH	PULL DOWN
Pin 11	PCI2	PCI2/TME	NO OVERCLOCKING (default)	NORMAL RUN
Pin 13	PCI4/ SEL_LCDCLK#	PCI4/ 27_Select	PIN 20/21 IS SRC0 PIN 24/25 IS 27MHz	PIN 20/21 IS DOT96 (default) PIN 24/25 IS LCDCLK
Pin 14	PCIF5/ITP_EN	PCIF5/ITP_EN	PIN 53/54 IS CPUITP	PIN 53/54 IS SRC8 (default)

+1.05V — R392 *1K_4 — (5) CPU_BSEL0 — R391 0_4 — CLK_BSEL0
R395 *0_4
+1.05V — R388 *1K_4 — (5) CPU_BSEL1 — R389 0_4 — CLK_BSEL1
R387 *0_4
+1.05V — R369 *1K_4 — (5) CPU_BSEL2 — R370 0_4 — CLK_BSEL2
R368 *0_4

FSC BSEL2	FSB BSEL1	FSA BSEL0	CPU	SRC	PCI	REF	USB	DOT
0	0	0	266.66	100	33.33	14.318	48	96
0	0	1	133.33	100	33.33	14.318	48	96
0	1	0	200.00	100	33.33	14.318	48	96
0	1	1	**166.66**	100	33.33	14.318	48	96
1	0	0	333.33	100	33.33	14.318	48	96
1	0	1	100.00	100	33.33	14.318	48	96
1	1	0	400.00	100	33.33	14.318	48	96
1	1	1	RESERVED					

<20090721(B2A)_Intel MOW WW28,2009>
Stuff R56,R60 to solve system maybe boot failure issue

+3V
PM_STPPCI# R R419 10K_4
PM_STPCPU# R418 10K_4
CLKREQ_WLAN# R R411 10K_4
CLKREQ_Dec# R R417 10K_4
CLKREQ_3G# R R406 10K_4

<20090527(A1A)_Silego suggestion>
The EMI capacitor should be placed between pin and series resistor for good EMI and SI

<EMI>
PCLK_DEBUG_R C343 *22p/50V_4
PCLK_EC_R C340 *33p/50V_4
PCLK_ICH_R C351 *33p/50V_4
FSA C362 *22p/50V_4
FSC C347 *33p/50V_4
PCLK_TPM_R C345 *33p/50V_4

VR PWRGD

(29) VR_PWRGD_CK410# — R400 *10K_4 — Q25 2N7002K — R394 10K_4 — +3V
VR_PWRGD_CK410 — VR_PWRGD_CK410 (12)

<20090721(B2A)>
Change Q3,Q5,Q6 from BAM700200F6 to BAM70020002 (with ESD protection function)

Clock Gen I2C

+3V — R359 2.2K_4
(12,21) PCLK_SMB — Q23 2N7002K — SMBCK1 — SMBCK1 (3,21,25,26)
+3V — R360 2.2K_4
(12,21) PDAT_SMB — Q24 2N7002K — SMBDT1 — SMBDT1 (3,21,25,26)

Quanta Computer Inc.
PROJECT : ZGA

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	CLOCK GENERATOR	1B
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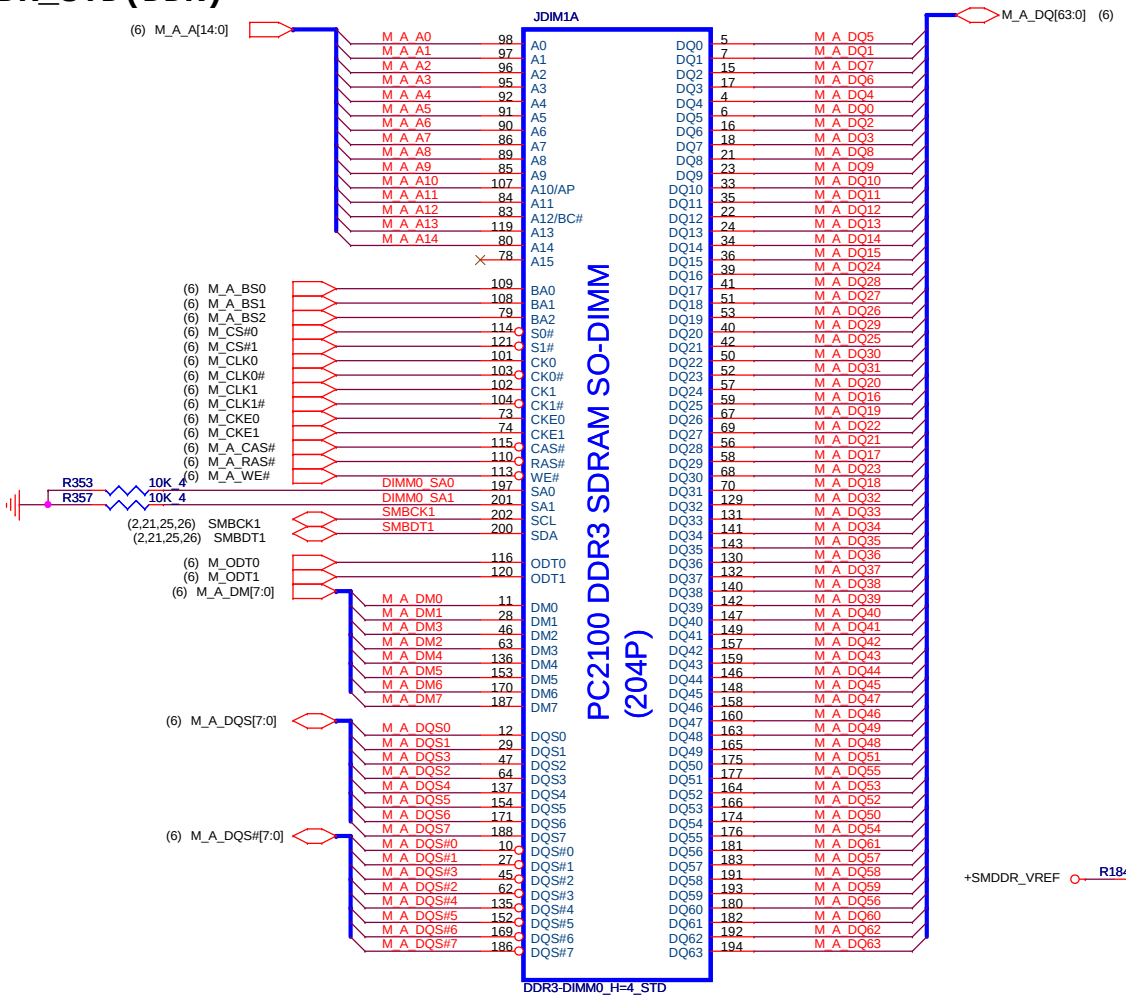
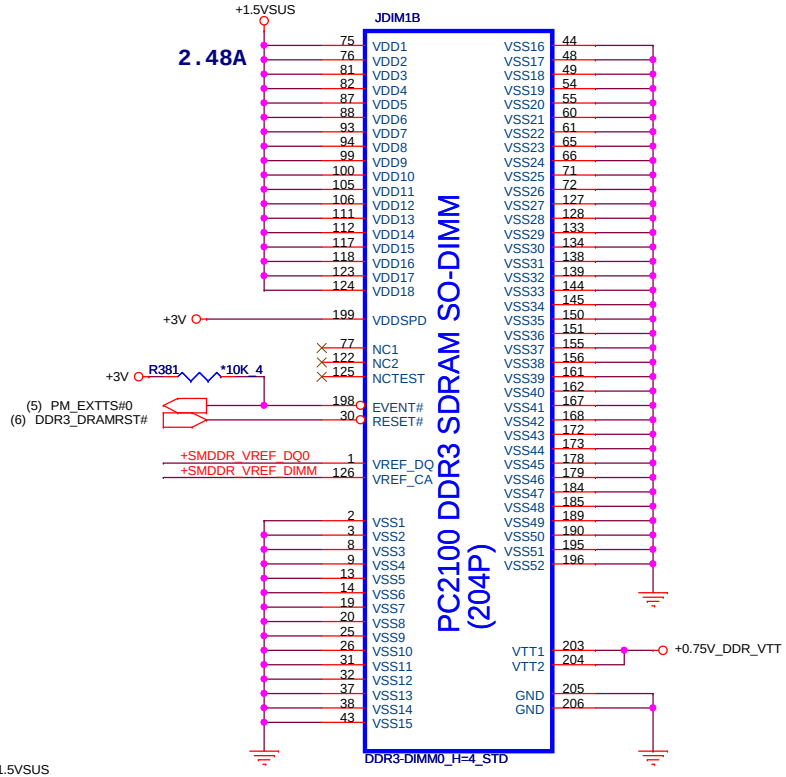
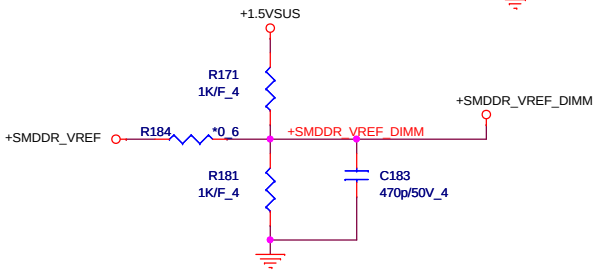
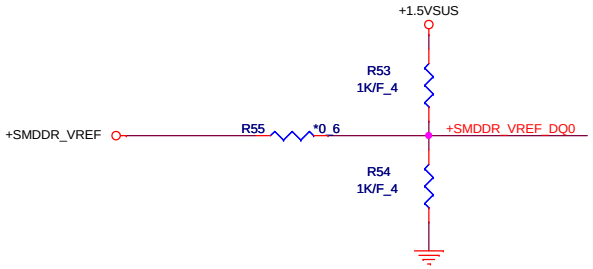
DDR_STD(DDR)

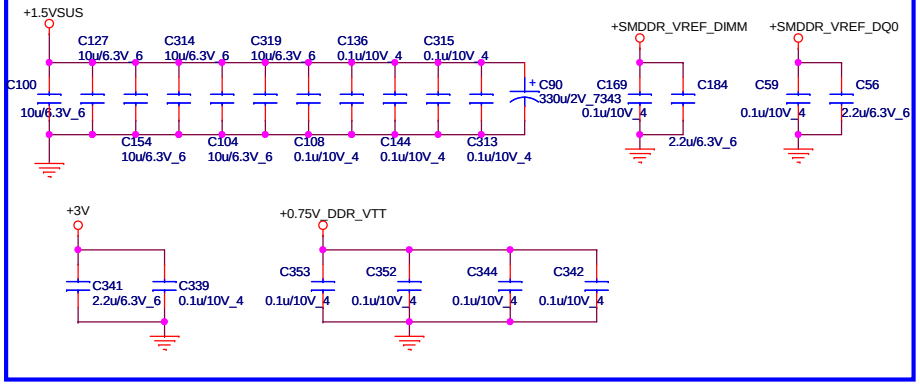








Place these Caps near So-Dimm0.



Quanta Computer Inc.		
PROJECT : ZGA		
Size	Document Number: DDRIII SO-DIMM-0	Rev: 1A
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Quanta Computer Inc.

PROJECT : ZGA

Size	Document Number	Rev
	BLANK	1A

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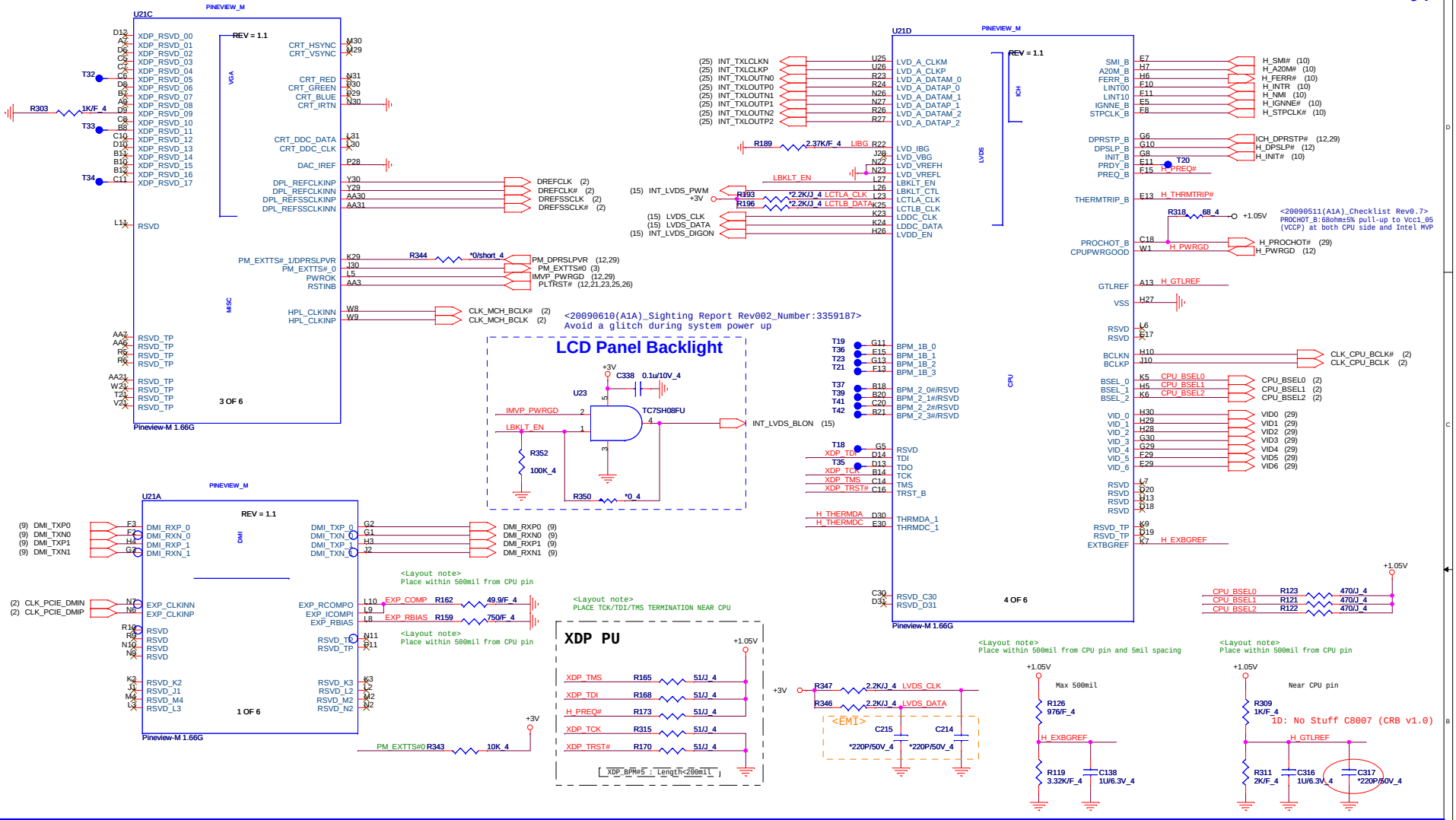
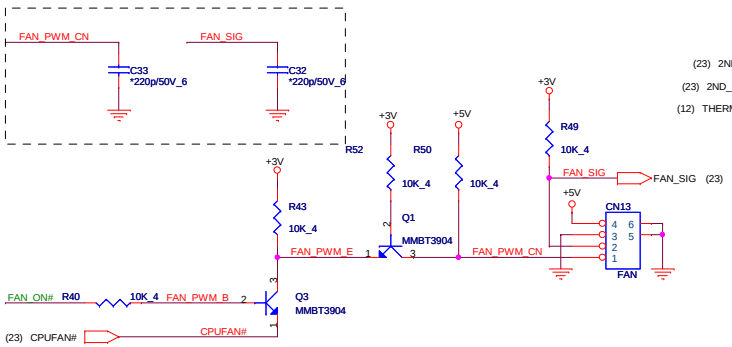
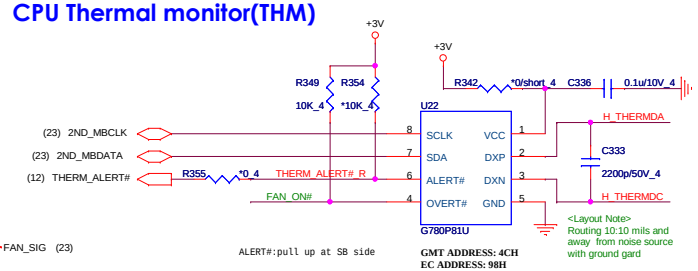


CPU FAN CTRL(THM)

8/11 B-test : for EMI

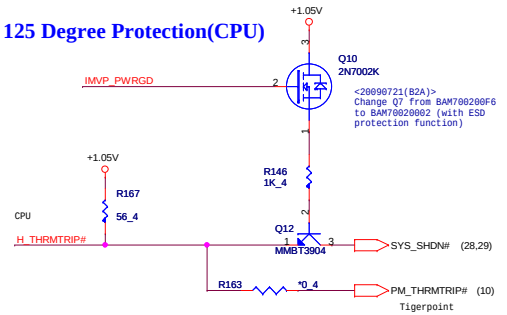


CPU Thermal monitor(THM)



GMT : AL000780000
WND : AL83L771K01

125 Degree Protection(CPU)



Quanta Computer Inc.		
PROJECT : ZGA		
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	Pineview DMI/Display	1B
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PINEVIEW_M

U21B

REV = 1.1

(3) M_A_A[14..0]

M_A_A0 AH19 DDR_A_MA_0
M_A_A1 AJ18 DDR_A_MA_1
M_A_A2 AK18 DDR_A_MA_2
M_A_A3 AK16 DDR_A_MA_3
M_A_A4 AJ14 DDR_A_MA_4
M_A_A5 AH14 DDR_A_MA_5
M_A_A6 AK14 DDR_A_MA_6
M_A_A7 AJ12 DDR_A_MA_7
M_A_A8 AH13 DDR_A_MA_8
M_A_A9 AK12 DDR_A_MA_9
M_A_A10 AK20 DDR_A_MA_10
M_A_A11 AH12 DDR_A_MA_11
M_A_A12 AJ11 DDR_A_MA_12
M_A_A13 AJ24 DDR_A_MA_13
M_A_A14 AJ10 DDR_A_MA_14

(3) M_A_WE#
(3) M_A_CAS#
(3) M_A_RAS#
M_A_WE# AK22 DDR_A_WEB
M_A_CAS# AJ22 DDR_A_CASB
M_A_RAS# AK21 DDR_A_RASB

(3) M_A_BS0
(3) M_A_BS1
(3) M_A_BS2
M_A_BS0 AJ20 DDR_A_BS_0
M_A_BS1 AH20 DDR_A_BS_1
M_A_BS2 AK11 DDR_A_BS_2

(3) M_CS#0
(3) M_CS#1
M_CS#0 AH22 DDR_A_CSB_0
M_CS#1 AK25 DDR_A_CSB_1
AJ21 DDR_A_CSB_2
AJ25 DDR_A_CSB_3

(3) M_CKE0
(3) M_CKE1
M_CKE0 AH10 DDR_A_CKE_0
M_CKE1 AH9 DDR_A_CKE_1
AK10 DDR_A_CKE_2
AJ8 DDR_A_CKE_3

(3) M_ODT0
(3) M_ODT1
M_ODT0 AK24 DDR_A_ODT_0
M_ODT1 AH26 DDR_A_ODT_1
AH24 DDR_A_ODT_2
AK27 DDR_A_ODT_3

(3) M_CLK0
(3) M_CLK0#
(3) M_CLK1
(3) M_CLK1#
M_CLK0 AG15 DDR_A_CK_0
M_CLK#0 AE15 DDR_A_CKB_0
M_CLK1 AD13 DDR_A_CK_1
M_CLK#1 AC13 DDR_A_CKB_1

AC15 DDR_A_CK_3
AD15 DDR_A_CKB_3
AF13 DDR_A_CK_4
AG13 DDR_A_CKB_4

AD17 RSVD_AD17
AC17 RSVD_AC17
AB15 RSVD_AB15
AB17 RSVD_AB17

DDRAM_PWROK AB4 VSS
AK8 RSVD

AB11 RSVD_TP
AB13 RSVD_TP

DDR_VREF AL28 DDR_VREF
SM_RCOMP AK28 DDR_RPD
SM_RCOMP# AJ26 DDR_RPU

AK29 RSVD

DDR_A

2 OF 6

Pineview-M 1.66G

DDR_A_DQS_0 AD3 M_A_DQS0
DDR_A_DQSB_0 AD2 M_A_DQS#0
DDR_A_DM_0 AD4 M_A_DM0

DDR_A_DQ_0 AC4 M_A_DQ0
DDR_A_DQ_1 AC1 M_A_DQ1
DDR_A_DQ_2 AF4 M_A_DQ2
DDR_A_DQ_3 AG2 M_A_DQ3
DDR_A_DQ_4 AB2 M_A_DQ4
DDR_A_DQ_5 AB3 M_A_DQ5
DDR_A_DQ_6 AE2 M_A_DQ6
DDR_A_DQ_7 AE3 M_A_DQ7

DDR_A_DQS_1 AB8 M_A_DQS1
DDR_A_DQSB_1 AD7 M_A_DQS#1
DDR_A_DM_1 AA9 M_A_DM1

DDR_A_DQ_8 AB6 M_A_DQ8
DDR_A_DQ_9 AB7 M_A_DQ9
DDR_A_DQ_10 AE5 M_A_DQ10
DDR_A_DQ_11 AG5 M_A_DQ11
DDR_A_DQ_12 AA5 M_A_DQ12
DDR_A_DQ_13 AB5 M_A_DQ13
DDR_A_DQ_14 AB9 M_A_DQ14
DDR_A_DQ_15 AD6 M_A_DQ15

DDR_A_DQS_2 AD8 M_A_DQS2
DDR_A_DQSB_2 AD10 M_A_DQS#2
DDR_A_DM_2 AE8 M_A_DM2

DDR_A_DQ_16 AG8 M_A_DQ16
DDR_A_DQ_17 AG7 M_A_DQ17
DDR_A_DQ_18 AE10 M_A_DQ18
DDR_A_DQ_19 AG11 M_A_DQ19
DDR_A_DQ_20 AF7 M_A_DQ20
DDR_A_DQ_21 AF8 M_A_DQ21
DDR_A_DQ_22 AD11 M_A_DQ22
DDR_A_DQ_23 AE10 M_A_DQ23

DDR_A_DQS_3 AK5 M_A_DQS3
DDR_A_DQSB_3 AK3 M_A_DQS#3
DDR_A_DM_3 AJ3 M_A_DM3

DDR_A_DQ_24 AH1 M_A_DQ24
DDR_A_DQ_25 AJ2 M_A_DQ25
DDR_A_DQ_26 AK6 M_A_DQ26
DDR_A_DQ_27 AJ7 M_A_DQ27
DDR_A_DQ_28 AF3 M_A_DQ28
DDR_A_DQ_29 AH2 M_A_DQ29
DDR_A_DQ_30 AL5 M_A_DQ30
DDR_A_DQ_31 AJ6 M_A_DQ31

DDR_A_DQS_4 AG22 M_A_DQS4
DDR_A_DQSB_4 AG21 M_A_DQS#4
DDR_A_DM_4 AD19 M_A_DM4

DDR_A_DQ_32 AE19 M_A_DQ32
DDR_A_DQ_33 AG19 M_A_DQ33
DDR_A_DQ_34 AF22 M_A_DQ34
DDR_A_DQ_35 AD22 M_A_DQ35
DDR_A_DQ_36 AG17 M_A_DQ36
DDR_A_DQ_37 AE19 M_A_DQ37
DDR_A_DQ_38 AF21 M_A_DQ38
DDR_A_DQ_39 AD21 M_A_DQ39

DDR_A_DQS_5 AE26 M_A_DQS5
DDR_A_DQSB_5 AG27 M_A_DQS#5
DDR_A_DM_5 AJ27 M_A_DM5

DDR_A_DQ_40 AE24 M_A_DQ40
DDR_A_DQ_41 AG25 M_A_DQ41
DDR_A_DQ_42 AD25 M_A_DQ42
DDR_A_DQ_43 AD24 M_A_DQ43
DDR_A_DQ_44 AC22 M_A_DQ44
DDR_A_DQ_45 AG24 M_A_DQ45
DDR_A_DQ_46 AD27 M_A_DQ46
DDR_A_DQ_47 AE27 M_A_DQ47

DDR_A_DQS_6 AE30 M_A_DQS6
DDR_A_DQSB_6 AE29 M_A_DQS#6
DDR_A_DM_6 AE30 M_A_DM6

DDR_A_DQ_48 AG31 M_A_DQ48
DDR_A_DQ_49 AG30 M_A_DQ49
DDR_A_DQ_50 AD30 M_A_DQ50
DDR_A_DQ_51 AD29 M_A_DQ51
DDR_A_DQ_52 AJ30 M_A_DQ52
DDR_A_DQ_53 AJ29 M_A_DQ53
DDR_A_DQ_54 AE29 M_A_DQ54
DDR_A_DQ_55 AD28 M_A_DQ55

DDR_A_DQS_7 AB27 M_A_DQS7
DDR_A_DQSB_7 AA27 M_A_DQS#7
DDR_A_DM_7 AB26 M_A_DM7

DDR_A_DQ_56 AA24 M_A_DQ56
DDR_A_DQ_57 AB25 M_A_DQ57
DDR_A_DQ_58 W24 M_A_DQ58
DDR_A_DQ_59 W22 M_A_DQ59
DDR_A_DQ_60 AB24 M_A_DQ60
DDR_A_DQ_61 AB23 M_A_DQ61
DDR_A_DQ_62 AA23 M_A_DQ62
DDR_A_DQ_63 W27 M_A_DQ63

M_A_DQ[63..0] (3)
M_A_DM[7..0] (3)
M_A_DQS[7..0] (3)
M_A_DQS#[7..0] (3)

DDR3 PWROK

+3V_S5

(23,30,32) SUSON
(23,30) HWPG_1.5V

U9
TC7SH08FU

R142 12.1K/F_4
R143 10K_4

DDRAM_PWROK

+1.5VSUS

R296 *10K_4

(3) DDR3_DRAMRST#

<Layout note>
Close to pin

C329 0.1U/10V_4
R339 80.6/F_4
R323 80.6/F_4
C322 0.01U/25V_4

+1.5VSUS

<Layout note>
Close to DDR_VREF pin

R325 1K/F_4
R330 *0_4
R335 1K/F_4
C330 0.1u/16V_6
C324 *1000p/50V_4

+SMDDR_VREF

DDG 2.1 : It is strongly recommended that the SODIMM VREF motherboard traces, going from their VREF resistor dividers to their specified SODIMM VREF pins, be ground referenced on the motherboard where ever possible to help minimize risks of any possible noise being coupled onto VREF. If they can't be referenced to ground we recommend placing a site for a 0603 capacitor near the VREF divider. These 0603 capacitor sites must be connected on one end to the non ground reference plane the VREF trace is referenced to and the other end must be connected to ground.

Quanta Computer Inc.
PROJECT : ZGA

Size	Document Number	Rev
	Pineview DDR	1B
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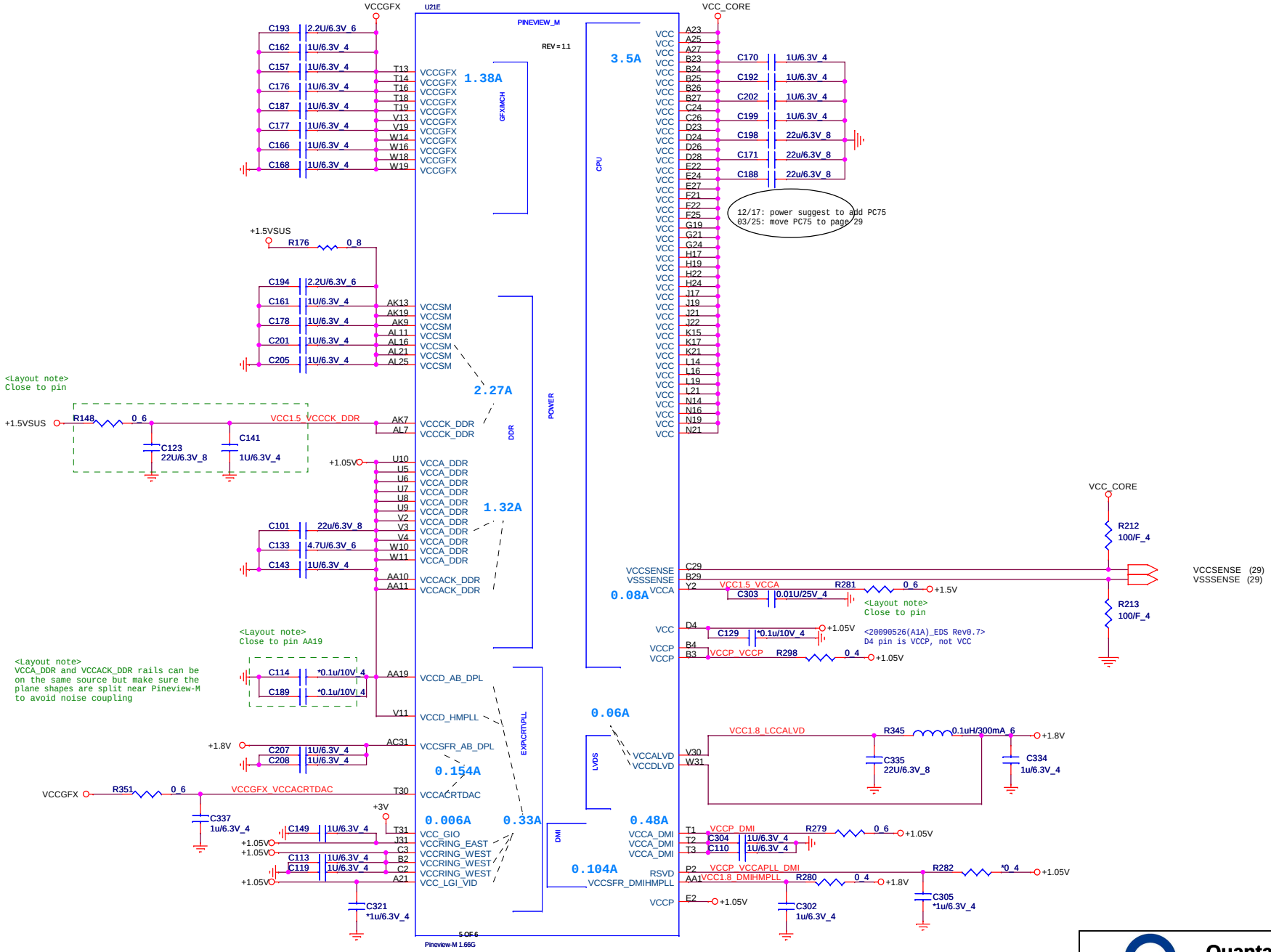
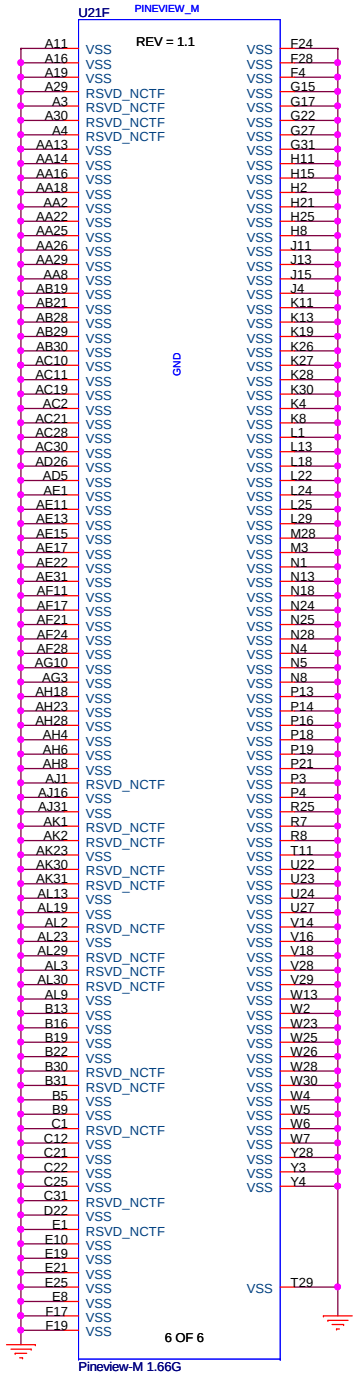
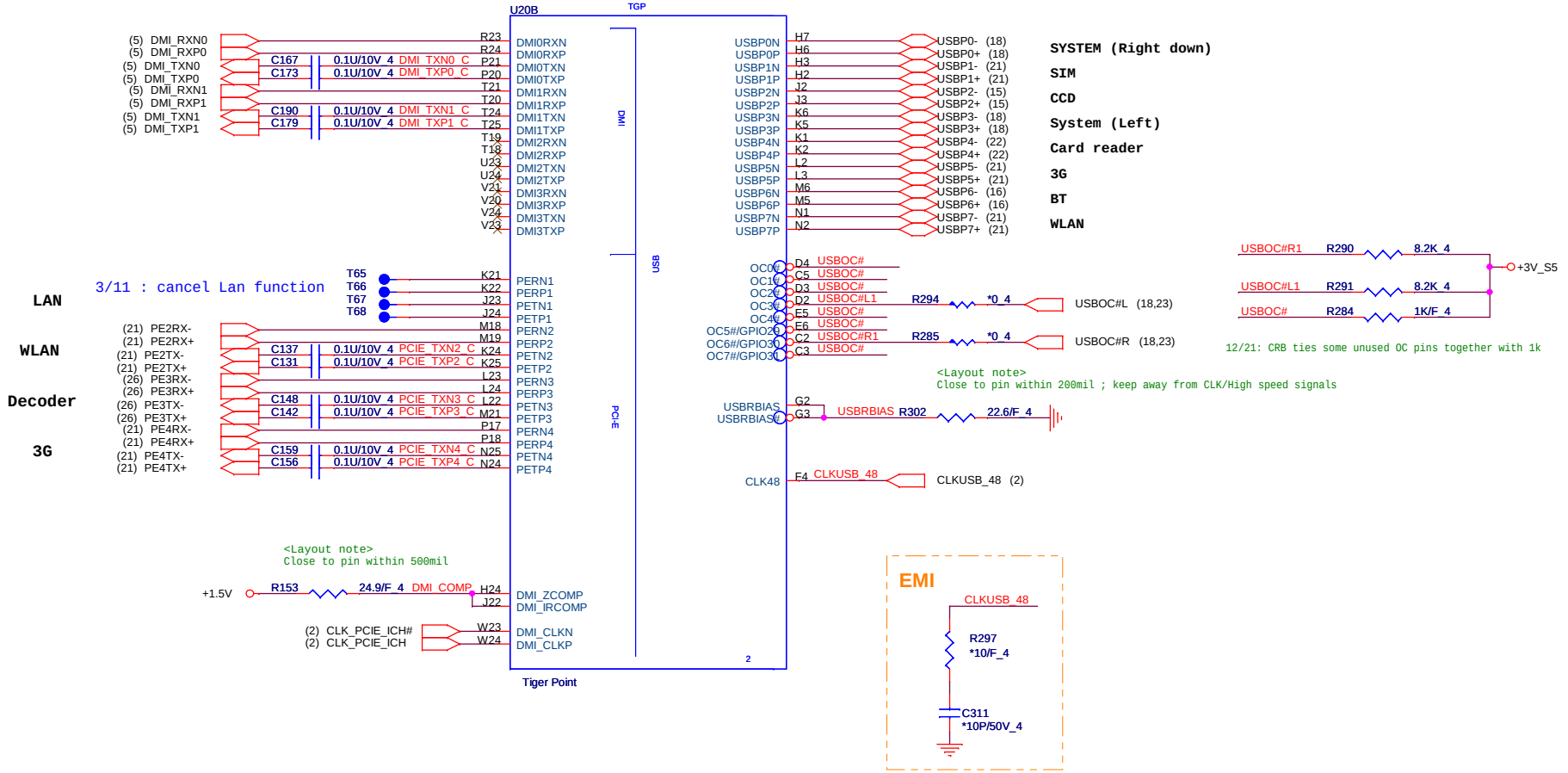
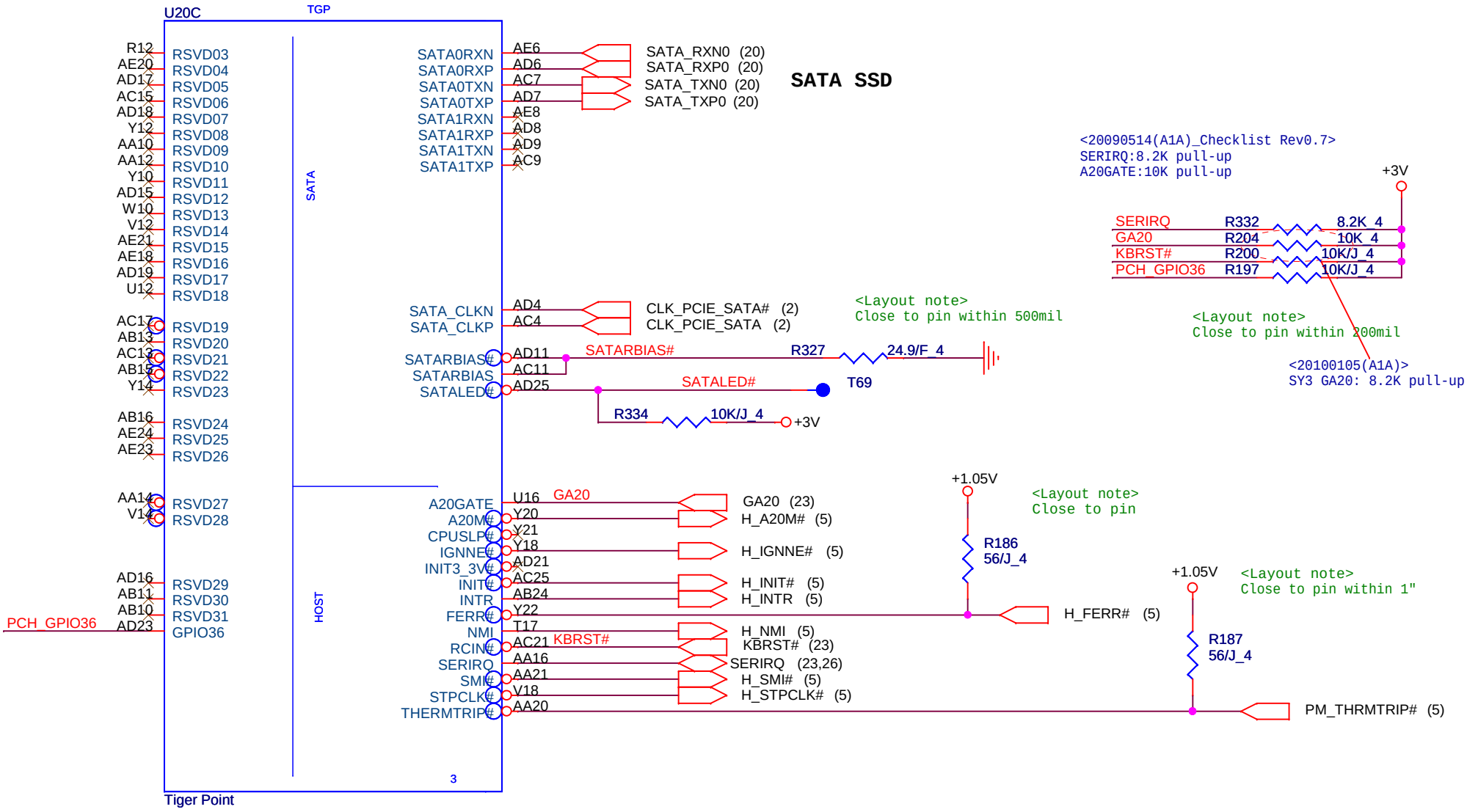

VCCGFX
U21E
PINEVIEW_M
REV = 1.1
VCC_CORE
3.5A
1.38A
GFX/MCH
CPU
POWER
DDR
2.27A
1.32A
0.08A
0.06A
0.154A
0.006A
0.33A
0.48A
0.104A
LVDS
DMI
EXPCRTPLL
+1.5VSUS
+1.05V
+1.8V
+3V
VCCGFX_VCCACRTDAC
VCC1.5_VCCCK_DDR
VCC1.5_VCCA
VCC1.8_LCCALVD
VCC1.8_DMIHMPLL
VCCP_VCCP
VCCP_DMI
VCCP_VCCAPLL_DMI
VCCSENSE
VSSSENSE
<Layout note>
Close to pin
<Layout note>
Close to pin AA19
<Layout note>
VCCA_DDR and VCCACK_DDR rails can be on the same source but make sure the plane shapes are split near Pineview-M to avoid noise coupling
12/17: power suggest to add PC75
03/25: move PC75 to page 29
<20090526(A1A)_EDS Rev0.7>
D4 pin is VCCP, not VCC
5 OF 6
Pineview-M 1.66G



Quanta Computer Inc.	
PROJECT : ZGA	
Size	Document Number: Pineview GND
Rev	1B
Date: Wednesday, July 07, 2010	Sheet 8 of 38

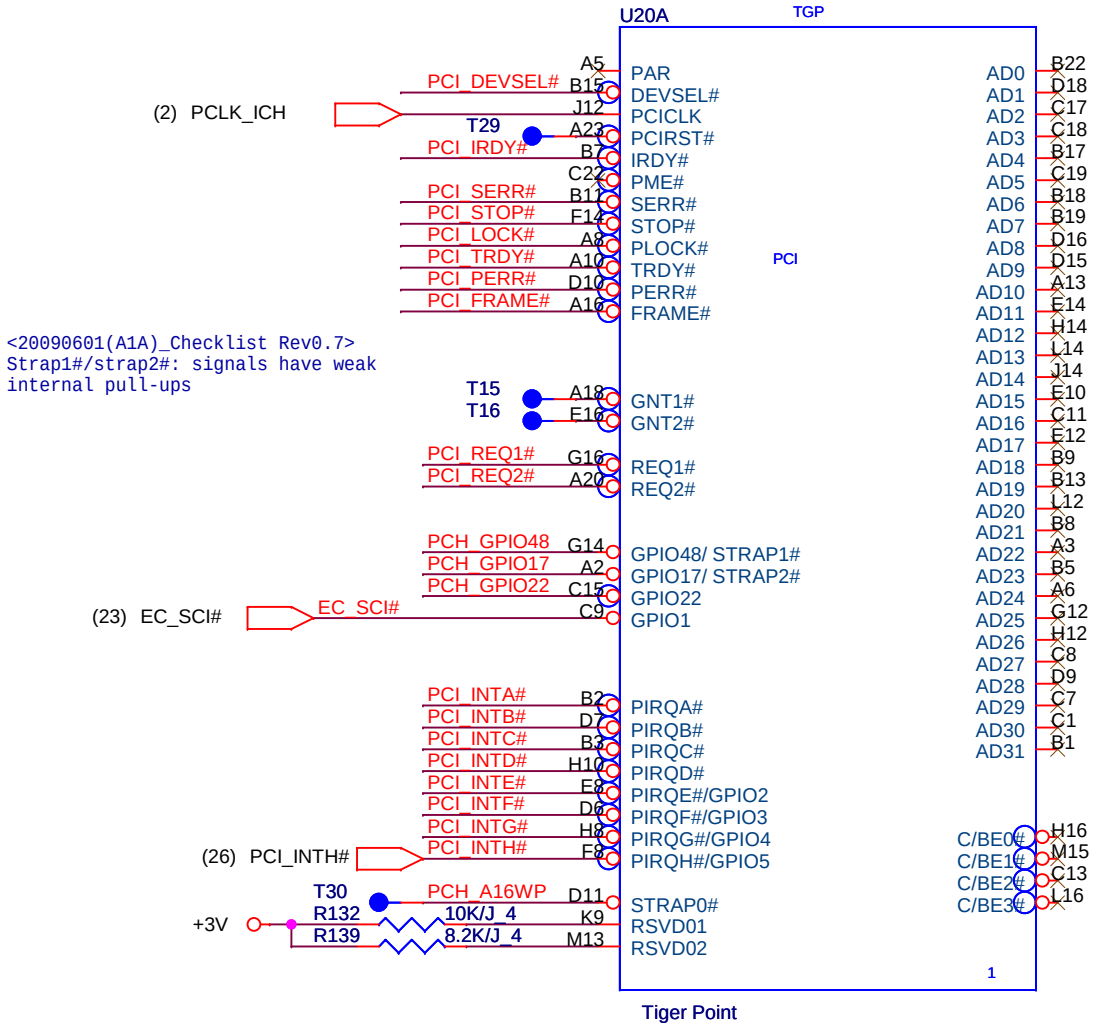


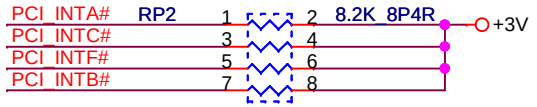
Quanta Computer Inc.		
PROJECT : ZGA		
Size	Document Number	Rev
	Tiger Point DMI/PCIE/USB	1B
Date: Wednesday, July 07, 2010	Sheet 9 of 38	

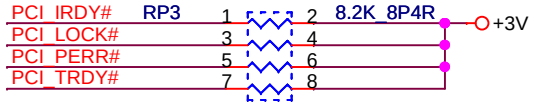


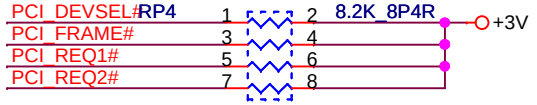
NOTE :
1. CPUSLP# is supported only on nettop platforms.

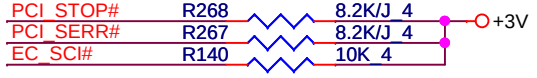
Quanta Computer Inc.		
PROJECT : ZGA		
Size	Document Number: Tiger Point Sata/Host	Rev: 1B
Date: Wednesday, July 07, 2010	Sheet 10 of 38	











IRQ	Description
PIRQA	USB UHCI Controller #1, #4
PIRQB	AC'97 Codec; option for SMBUS
PIRQC	USB UH Controller #3; SATA/IDE Native Mode
PIRQD	USB UHCI Controller #2
PIRQE	Internal LAN; Option for SCI, TCO, HPET#0,1,2
PIRQF	Option for SCI, TCO, HPET#0,1,2
PIRQG	Option for SCI, TCO, HPET#0,1,2
PIRQH	USB EHCI Controller; Option for SCI, TCO, HPET#0,1,2

PCI_GNT#2	Internal PU Should not be PD

ICH Boot BIOS select

PCH_GPIO17 (INT PU)	PCH_GPIO48 (INT PU)	Boot BIOS Location
0	1	SPI **(Default)**
1	0	PCI
1	1	LPC

A16 SWAP Override strap

PCH_A16WP (INT PU)	**Low = A16 swap override enabled** **High = Default**

Quanta Computer Inc.

PROJECT : ZGA

Size	Document Number	Rev
	TigerPoint PCI(3/6)	1B
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EMI

14M_ICH
R320 *33/J_4
C323 *10P/50V_4

debug port for google require

CN14
PCH_GPIO24
PCH_GPIO26
PCH_GPIO27
PCH_GPIO28
PCH_GPIO33
PCH_GPIO34
PCH_GPIO38
PCH_GPIO39
*88513-104N

place near to Tiger point.
R151 10K_4 SPI_CS#
R308 10K_4 SPI_MISO
R312 10K_4 SPI_MOSI_R

SPI FLASH(CLG)

U11 MX25L1605DM2I-12G
SPI_MISO R307 47/F_4 SPI_MISO_R
SPI_MOSI
SPI_CLK
SPI_CS# R152 10K_4
R120 3.3K_4 MANU_SW_R1
C96 .1u/10V_4
R438 100K/F_4
SPI_MOSI R310 47/F_4
SPI_CLK R305 47/F_4
MANU_SW_R1 D26 BAS316 MANU_SW_R (23)

1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

RTC(RTC)

At 11/24 add
Winbond W25X16AVSSIG AKE38ZP0N01
MXIC MX25L1605AM2C-15G AKE37FP0Z13
EON EN25F16-100HIP AKE38ZA0Q00
AMIC A25L016 AKE38ZN0800

VCCRTC
D30 CH500H-40 C332 1u/10V_6
D31 CH500H-40 R338 20K/F_6
RTCRST# G3 *SHORT_PAD
C331 1u/10V_6
R348 1K_4
20MIL 20MIL
VCCRTC_4 Q26 MMBT3904 VCCRTC_1 R415 2K/F_4 VCCRTC_2 R422 2K/F_4
R421 68.1K/F_4
R414 150K/F_4
CN22 RTC_CONN

Tiger Point

U20D TGP

LPC: LAD0/FWH0 LAD1/FWH1 LAD2/FWH2 LAD3/FWH3 LDRQ0# LFRAME#
AUDIO: HDA_BIT_CLK HDA_RST# HDA_SDI0 HDA_SDIN1 HDA_SDIN2 HDA_SDOUT HDA_SYNC CLK14
EEPROM: EE_CS EE_DIN EE_DOUT EE_SHCLK
LAN: LAN_CLK LANR_STSYNC LAN_RST# LAN_RXD0 LAN_RXD1 LAN_RXD2 LAN_TXD0 LAN_TXD1 LAN_TXD2
RTC: RTCX1 RTCX2 RTCRST#
SMB: SMBALERT#/GPIO11 SMBCLK SMBDATA SMLALERT# SMLINK0 SMLINK1
SPI: SPI_MISO SPI_MOSI SPI_CS# SPI_CLK SPI_ARB
MISC: BM_BUSY#/GPIO0 GPIO6 GPIO7 GPIO8 GPIO9 GPIO10 GPIO12 GPIO13 GPIO14 GPIO15 DPRSLPVR STP_PCI# STP_CPU# GPIO24 GPIO25 GPIO26 GPIO27 GPIO28 CLKRUN# GPIO33 GPIO34 GPIO38 GPIO39 CPUPWRGD/GPIO49 THRM# VRMPWRGD MCH_SYNC# PWRBTN# RI# SUS_STAT#/LPCPD# SUSCLK SYS_RESET# PLTRST# WAKE# INTRUDER# PWROK RSMRST# INTVRMEN SPKR SLP_S3# SLP_S4# SLP_S5# BATLOW# DPRSTP# DPSLP# RSVD31

Tiger Point

(21,23,26) LPCAD0 LPCAD1 LPCAD2 LPCAD3 LPCFRAME#
(17) ACZ_BITCLK_AUDIO R160 33/J_4 ACZ_BITCLK_R
(17) ACZ_RESET#_AUDIO R161 33/J_4 ACZ_RST#_R
(17) ACZ_SDIN0
(17) ACZ_SDOUT_AUDIO R185 33/J_4 ACZ_SDOUT_R
(17) ACZ_SYNC_AUDIO R175 33/J_4 ACZ_SYNC_R
(2) 14M_ICH
<20090529(A1A)_Checklist Rev0.7> If integrated LAN is not used LAN_RST# tie it to GND.
C318 15P/50V_4
Y3 32.768K/10PPM
R319 10M/J_4
C320 15P/50V_4
RTC_X1 RTC_X2 RTCRST#
(2,21) PCLK_SMB (2,21) PDAT_SMB
SMB_LINK_ALERT# SMLINK0 SMLINK1
SPI_MISO SPI_MOSI_R SPI_CS#_R SPI_CLK_R T22

D23,D24 are just for preventing EC/SB F/W error to cause to leakage current.If test OK, they can be connected directly.

BM_BUSY# RECOVER_KEY# R1 D24 BAS316 RECOVER_KEY#_R (23)
GPIO6 DEVELOPER# R1 D23 BAS316 DEVELOPER#_R (23)
GPIO8 EC_SMI# EC_SMI# (23)
GPIO9 LID# ICH D21 BAS316 LID# (15,23)
GPIO10 MANU_0_4 R118 MANU_SW_TPT (23)
HDMI_CON_HP_TP HDMI_CON_HP_TP (25)
DPRSLPVR PM_DPRSLPVR (5,29)
STP_PCI# PM_STPPCI# (2)
STP_CPU# PM_STPCPU# (2)
1C: Intel suggestion enable AC mode
PCH_GPIO24 DMI_AC_ENABLE
PCH_GPIO26 PCH_GPIO27 PCH_GPIO28
CLKRUN# CLKRUN# (23,26)
PCH_GPIO33 PCH_GPIO34 PCH_GPIO38 PCH_GPIO39
H_PWRGD (5)
THERM_ALERT# (5) VR_PWRGD_CK410 (2)
MCH_SYNC# ICH_RI# DNBSWON# (23)
T31
SUSCLK (23)
VCCRTC
PCIE_WAKE# (21) R164 1M/F_6
SM_INTRUDER# TPT_PWROK
EC_RSMRST# (23) R328 332K/F_4
SB_BEEP (17)
SUSB# (23) SUSC# (23)
T17
PM_BATLOW#
ICH_DPRSTP# (5,29) H_DPSLP# (5)

<20090515(A1A)_Checklist Rev0.7>
BATLOW#:8.2K pull-up to V3ALWAYS
WAKE#:10K pull-up to VccSus3_3
SYS_RST#:10K pull-up to VccSus3_3

+3V_S5
PCLK_SMB R130 2.2K_4
PDAT_SMB R127 2.2K_4
PM_BATLOW# R273 8.2K_4
THERM_ALERT# R188 10K/J_4
DNBSWON# R117 *10K_4
LID# ICH R150 8.2K_4
EC_SMI# R154 10K_4
SYS_RST# R115 10K_4
SMBALERT# R129 10K_4
SMB_LINK_ALERT# R128 10K_4
PCIE_WAKE# R274 10K_4
SMLINK1 R276 8.2K_4
SMLINK0 R277 8.2K_4
HDMI_CON_HP_TP R272 *8.2K_4
ICH_RI# R116 10K_4

+3V
RECOVER_KEY# R1 R182 1K/F_4
DEVELOPER# R1 R183 8.2K_4
MCH_SYNC# R331 1K/F_4
CLKRUN# R333 8.2K_4
BM_BUSY# R195 10K_4
DMI_AC_ENABLE R275 1K_4
TPT_PWROK R172 10K_4
EC_RSMRST# R190 10K_4

Platform Reset

U19 TC7SH08FU
C299 *0.1u/10V_4
PLT_RST# *TC7SH08FU PLTRST# (5,21,23,25,26)
R286 100K_4
R283 *0/short_4

TPT Power OK

<20090721(B2A)>
Stuff U19 and C275 and un-stuff R205 for power sequence

U14 TC7SH08FU
C209 0.1u/10V_4
(23) HWPG
(5,29) IMVP_PWRGD
TPT_PWROK
(23) ECPWROK R205 *0_4

+3V_S5
R261 10K_4 R271 10K_4 R304 10K_4
MBID2 MBID1 MBID0
R262 *10K_4 R270 *10K_4 R306 *10K_4

ACZ_SDOUT (INT PD)	ACZ_SYNC (INT PD)	Description
0	0	* 4 x 1s
1	0	Reserved
0	1	Reserved
1	1	1 x 4s(1 port/4 lanes)

INTVRMEN	
1	Enable internal VccSus1_5 VRM (default)
0	Disable

1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

Quanta Computer Inc.
PROJECT : ZGA

Size	Document Number	Rev
	TigerPoint GPIO	1A
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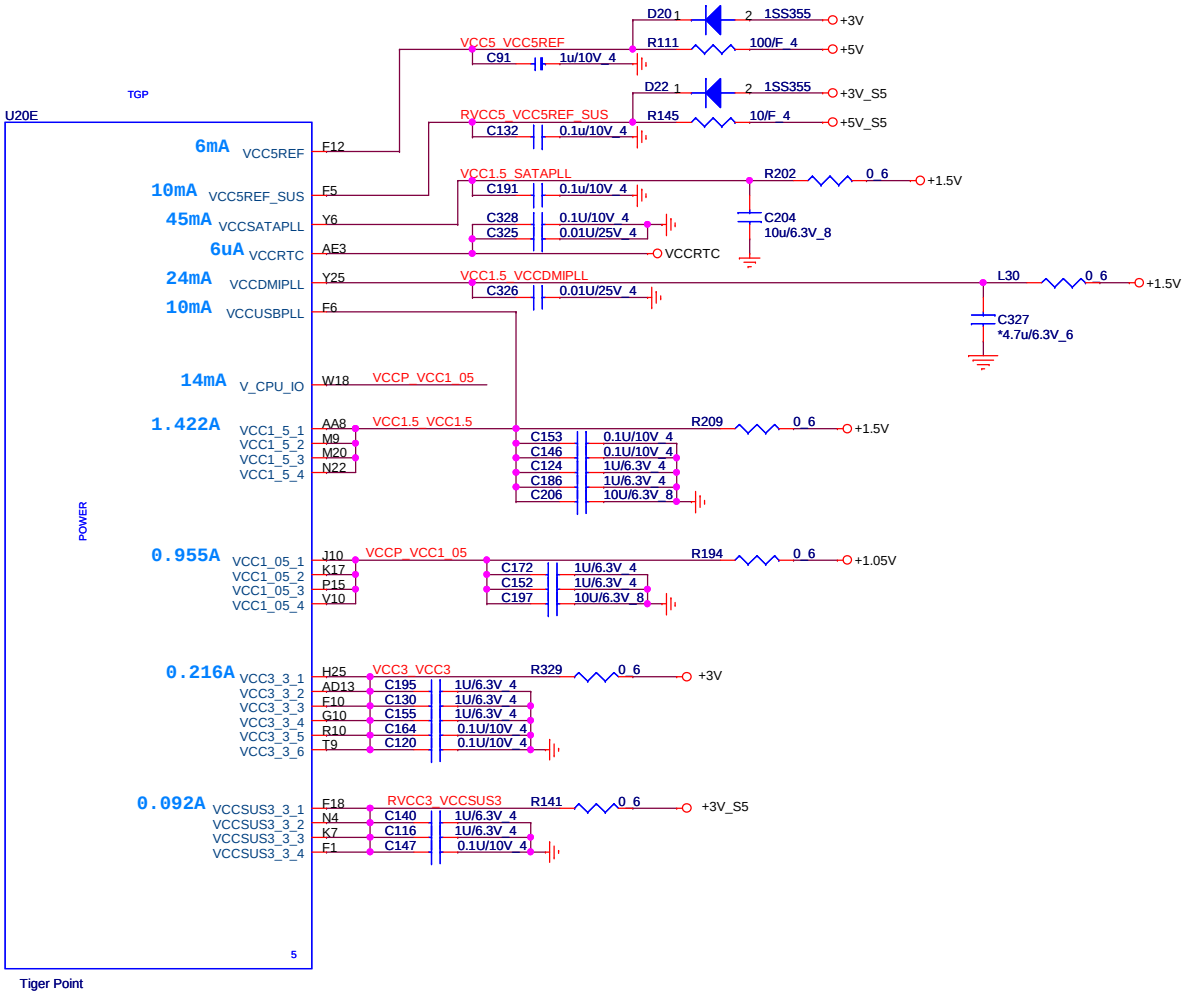
<Layout note>
Place 0402 caps close to ball
Place 0603/0805 caps close to ICH



1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

Quanta Computer Inc.
PROJECT : ZGA

Size	Document Number	Rev
	TigerPoint Power	1B
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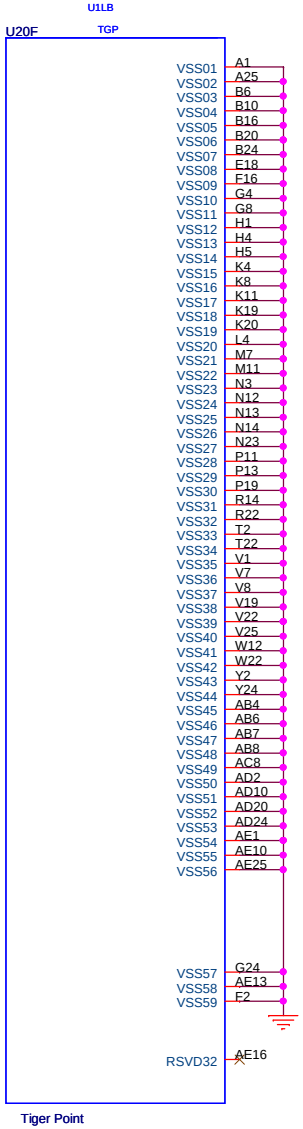

1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

Quanta Computer Inc.
PROJECT : ZGA

Size	Document Number	Rev
	TigerPoint GND	1B
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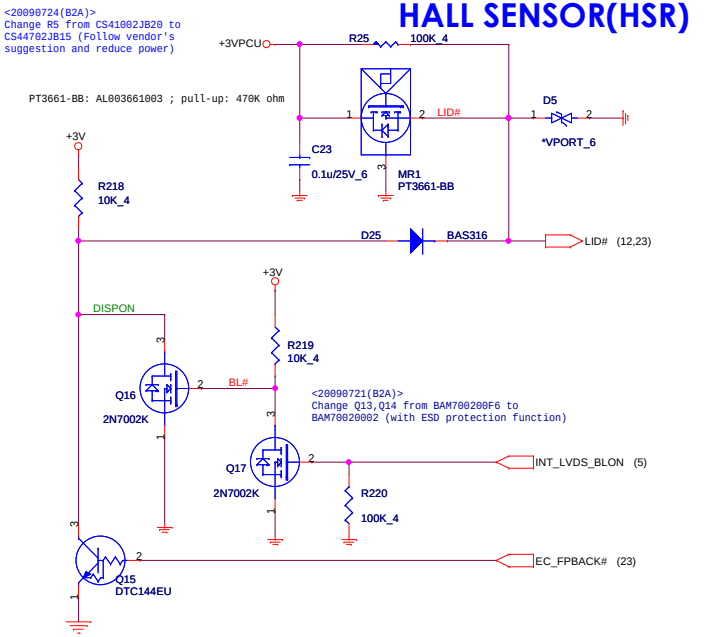
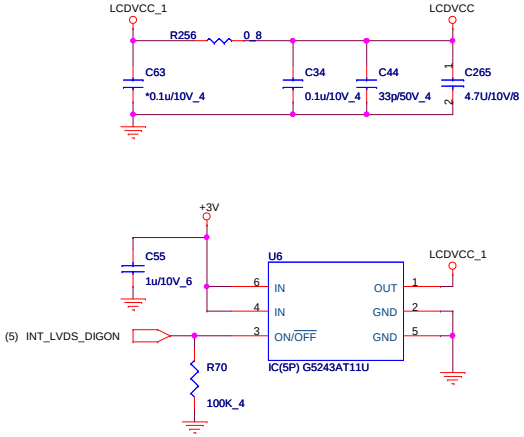
HALL SENSOR(HSR)



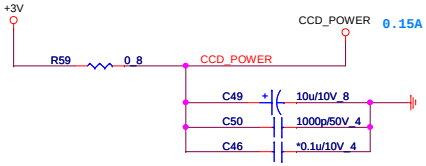
LED Panel POWER SWITCH(LDS)

Irush=1.5A

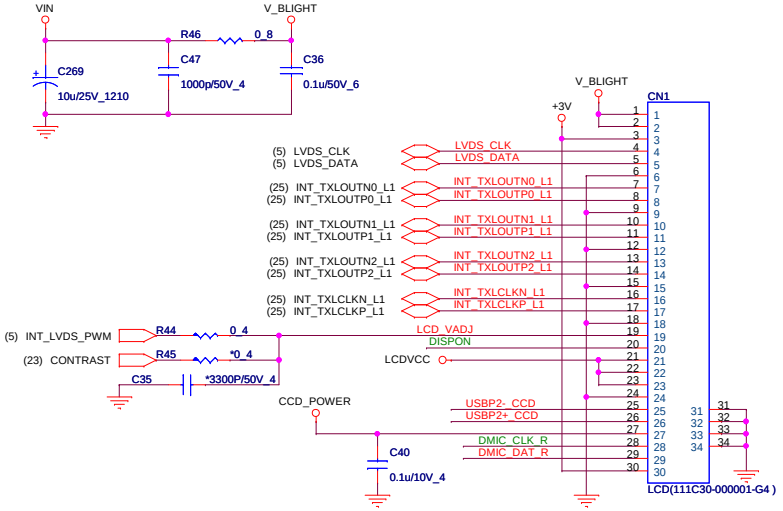


CAMERA POWER(CCD)

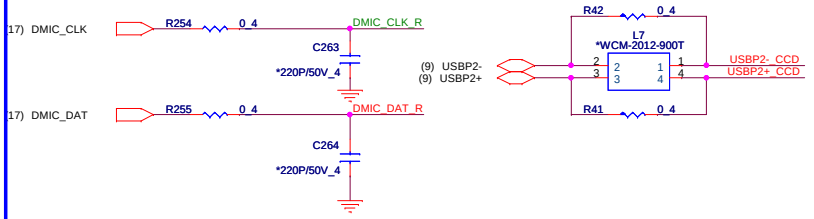
14



LED Panel(LDS)



B-test 8/11: for EMI



CRT(CRT)

3/11 : cancel CRT function

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PROJECT : ZGA

Size	Document Number	Rev
	CRT/LVDS	1B

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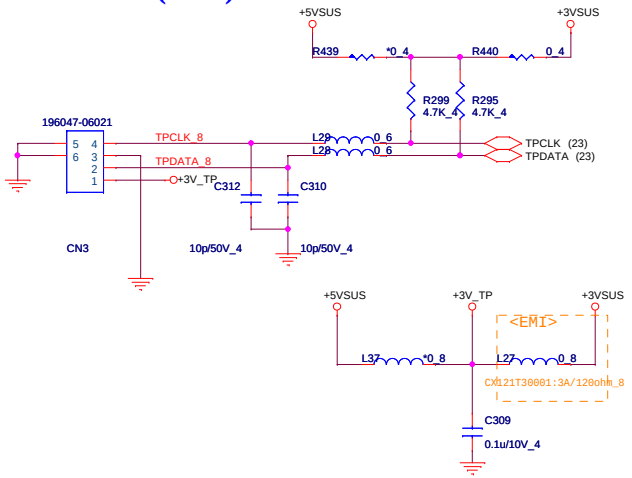
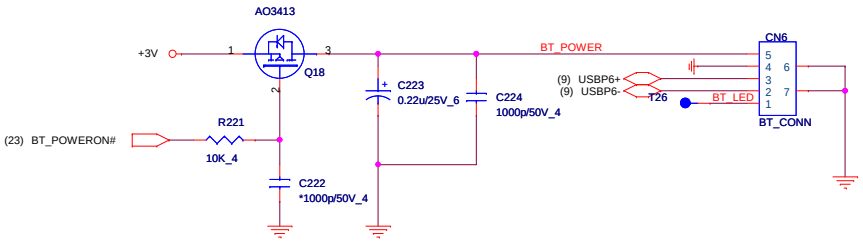
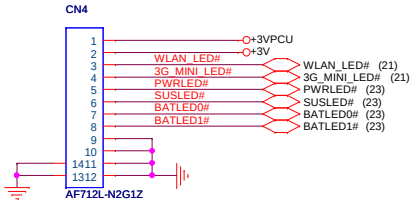
TOUCH PAD(TPD)



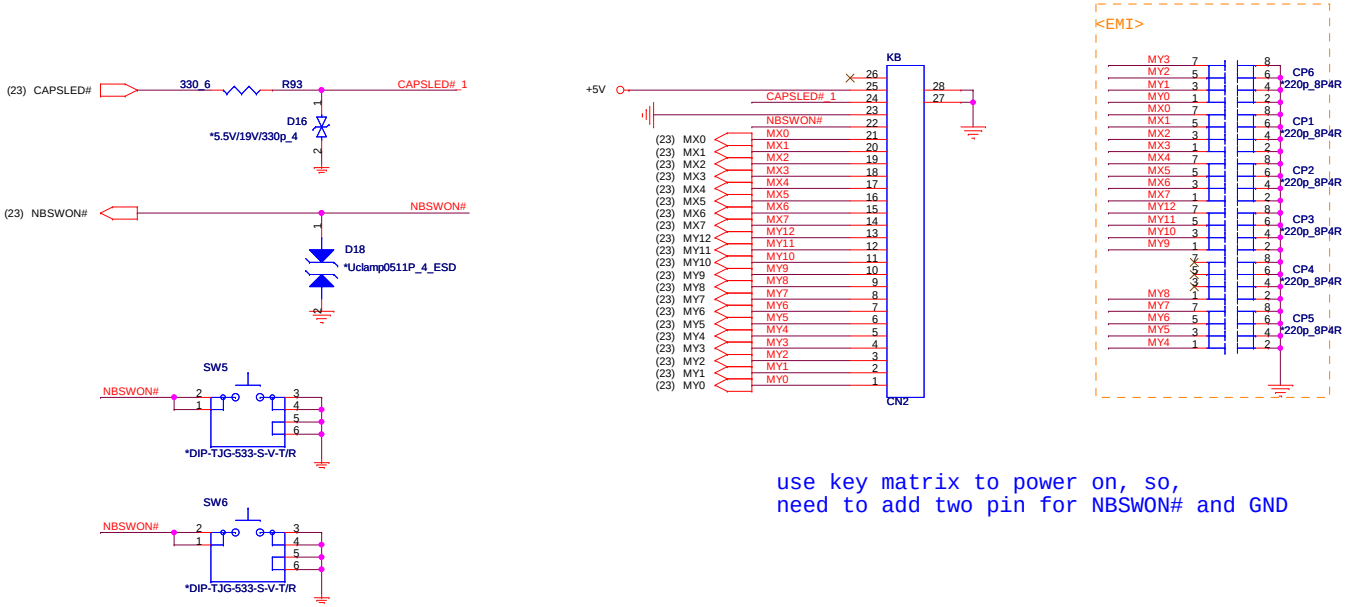
BLUETOOTH(BTM)



Connector (UIF)



KEYBOARD(KBC)



use key matrix to power on, so,
need to add two pin for NBSWON# and GND

place on top and botton for A2 test

RGB to HDMI(DB)

use LVDS to HDMI solution, so delete CN11

Quanta Computer Inc.

PROJECT : ZGA

Size	Document Number	Rev
	KB/BT/TP/LED/Power Connector	1B

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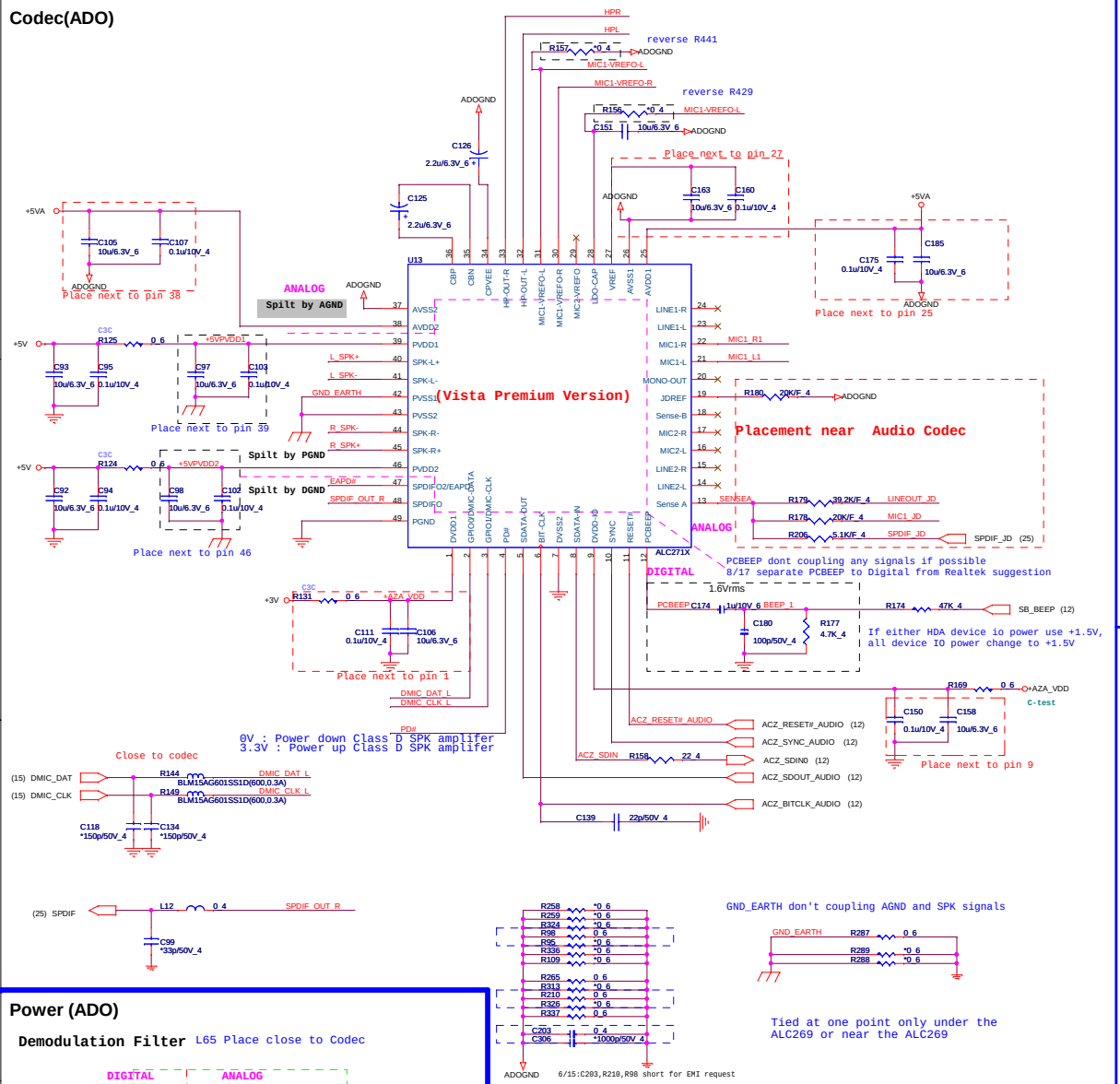
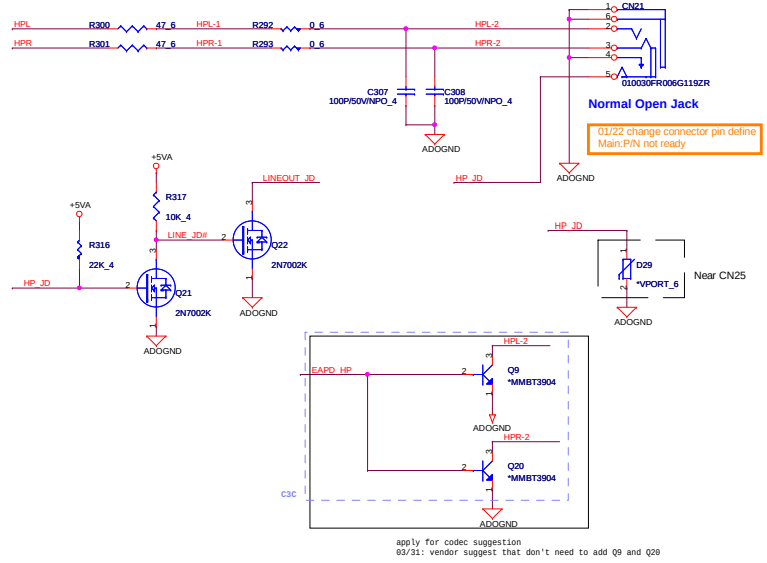
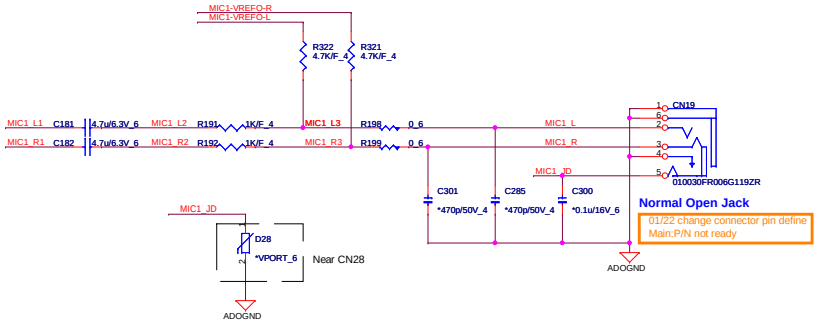
Codec(ADO)



HEADPHONE

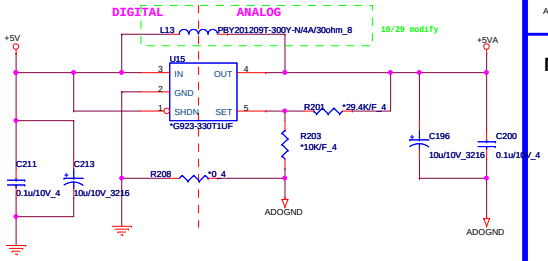


System MIC



Power (ADO)

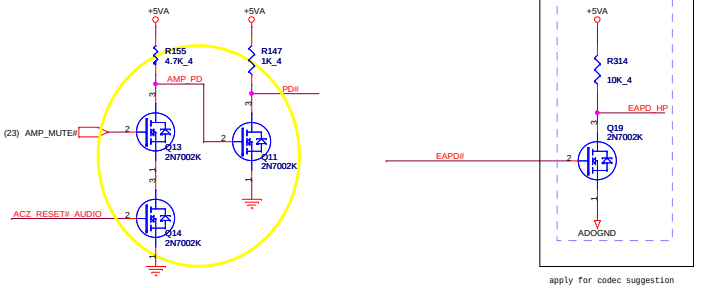
Demodulation Filter L65 Place close to Codec



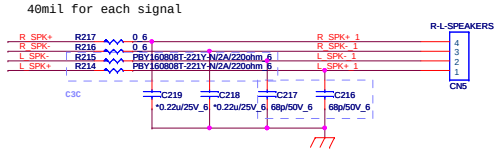
Vset =1.25V

Vout =Vset[1+AR(1,2)/AR(2,GND)]

Mute(ADO)



Internal Speaker



Quanta Computer Inc.		
PROJECT : ZGA		
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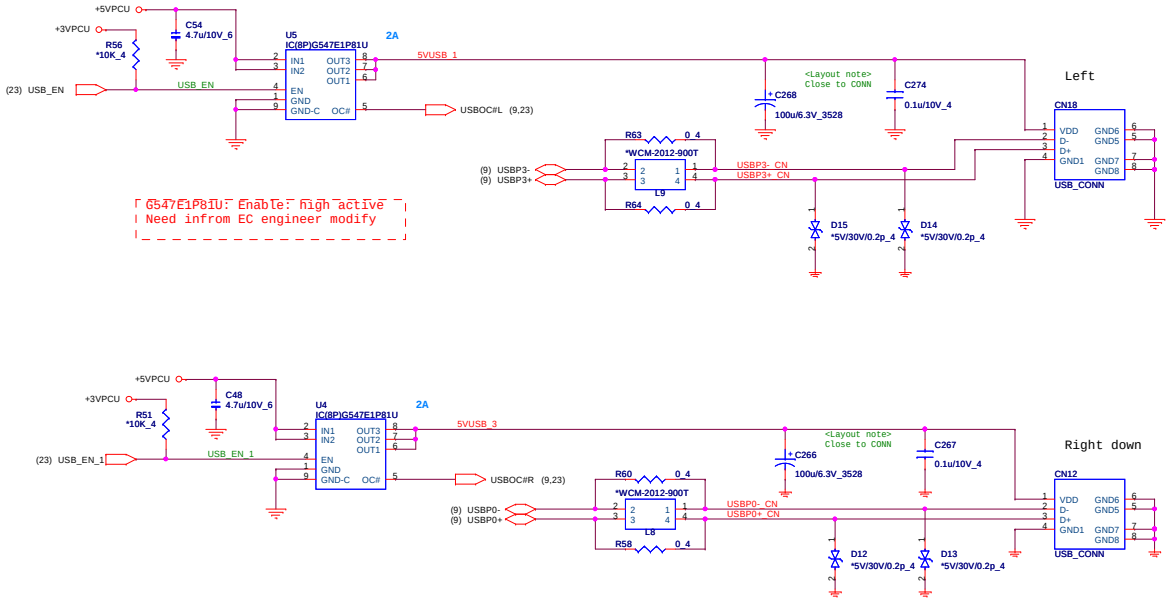
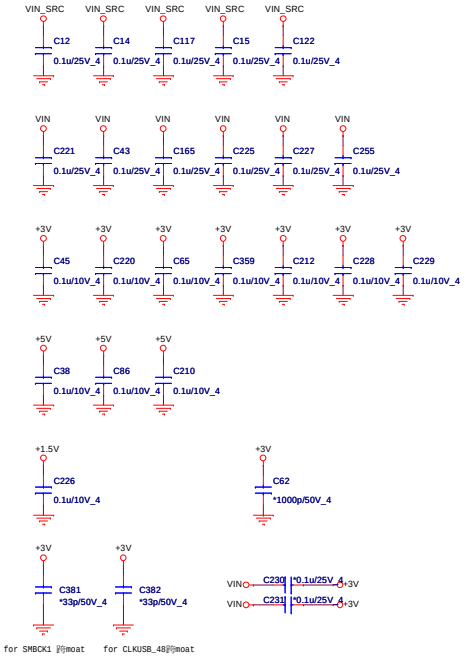
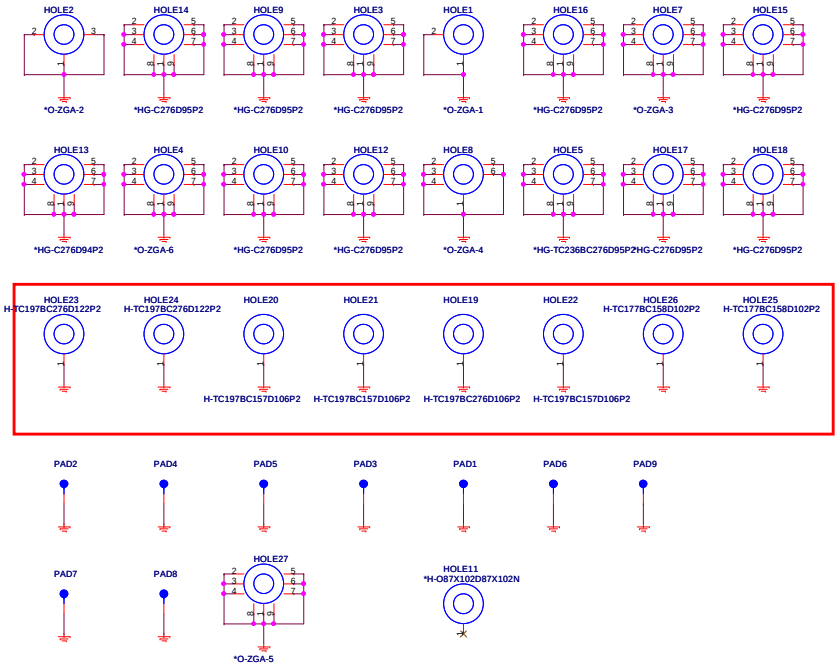
USB(USB)



EMI



Hole



Quanta Computer Inc.

PROJECT : ZGA

Size	Document Number	Rev
	USB on Board/LED/SW/HOLE	1B

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Giga-LAN AR8151(LAN)

RJ45(LAN)

TRANSFORMER(LAN)

Quanta Computer Inc.		
PROJECT : ZGA		
Size	Document Number: AR8151	Rev: 1A
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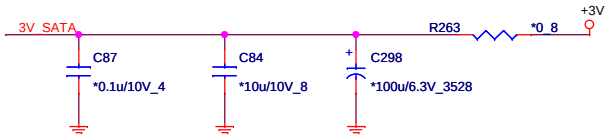

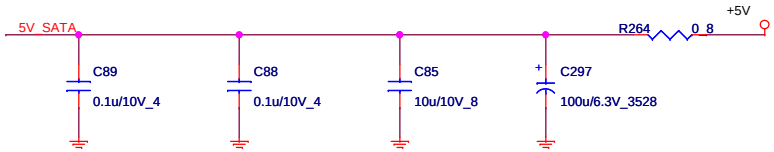

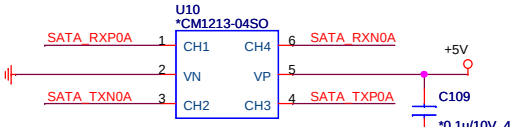

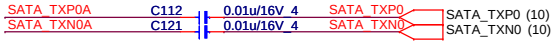

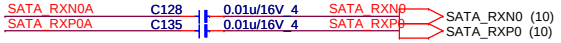

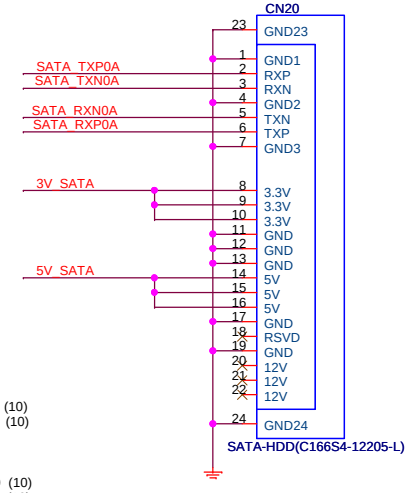

Quanta Computer Inc.		
PROJECT : ZGA		
Size	Document Number	Rev
	SATA-HDD/SSD	1B
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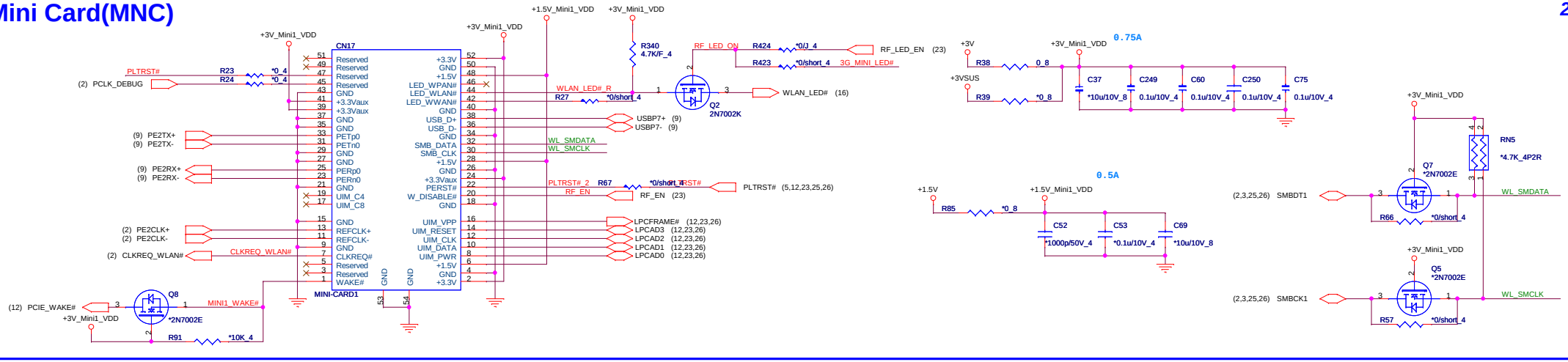
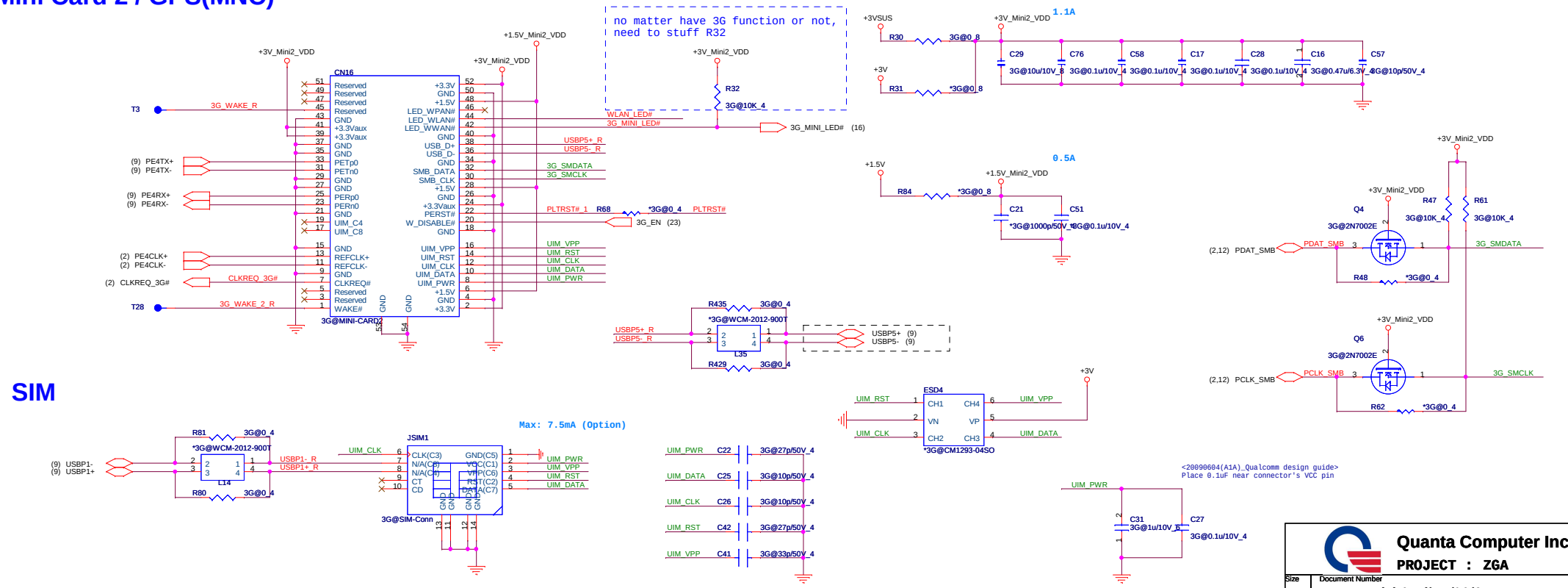
Mini Card(MNC)



Mini Card 2 / GPS(MNC)



SIM

Quanta Computer Inc.

PROJECT : ZGA

Size	Document Number	Rev
	Mini-Card/WL/3G/SIM	1B
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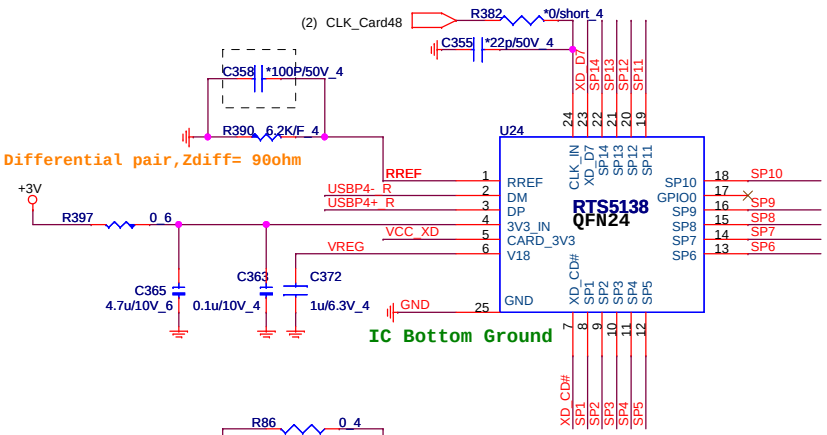
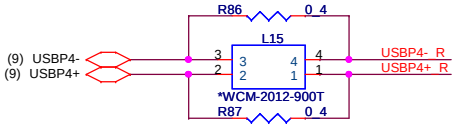
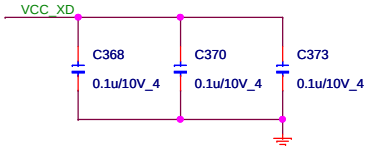
RTS5138

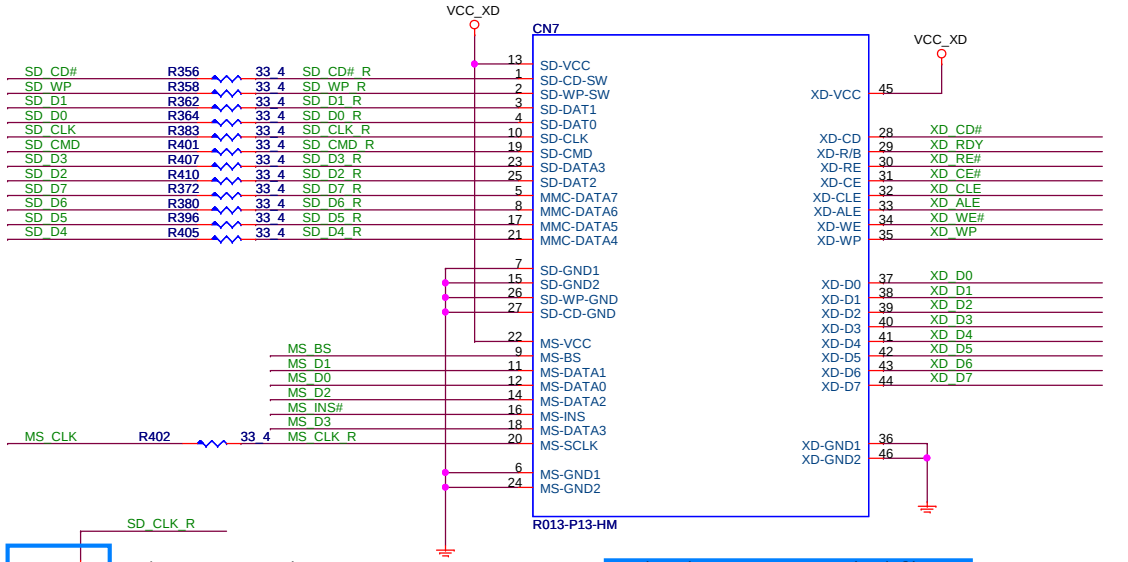


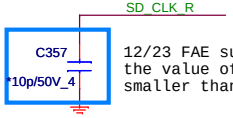




	XD_CD#		
SP1	XD_RDY	SD_WP	MS_CLK
SP2	XD_RE#		MS_INS#
SP3	XD_CE#	SD_D1	
SP4	XD_CLE	SD_D0	
SP5	XD_ALE	SD_D7	MS_D3
SP6	XD_WE#	SD_CD#	
SP7	XD_WP	SD_D6	
SP8	XD_D0	SD_CLK	MS_D2
SP9	XD_D1	SD_D5	MS_D0
SP10	XD_D2	SD_CMD	
SP11	XD_D3	SD_D4	
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	
SP14	XD_D6		MS_BS
	XD_D7		

Share Pin





12/23 FAE suggestion:
the value of C346 need
smaller than 10p

01/29 change connector pin define
Main:DFHS44FR012

03/11 change connector footprint for Dip type.

Quanta Computer Inc.
PROJECT : ZGA

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	RTS5138	1A
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EC(KBC)

30mil

0.03A(30mils)

NPCE781

12/21 : EC suggest to remove extrernal OSC

1'st SMBUS for Smart Battery / Charger

2nd SMBUS for CPU thermal sensor.

3rd SMBUS for Light sensor.

4th SMBUS for HDMI.

use keyboard matrix to power on, not bottom

<20090602(A1A)_Vendor suggest> Place 10nF-0.1uF capacitors for every AD input. And close to the AD input.

<20090721(B2A)_FAE suggestion> Stuff 100K and close to EC side for improving power consumption

10/27 Modify

SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	CPU thermal sensor
SM Bus 3	Light sensor

SW2 : connect pin2 and pin3, MANU_SW_R is high.
connect pin1 and pin3, MANU_SW_R is low.(default)

delete R373

default connect to EC

default connect pin2 and pin3

I/O ADDRESS SETTING(KBC)

SHBM=0: Enable shared memory with host BIOS

1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

SM BUS PU(KBC)

SPI FLASH(KBC)

1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

due to ZGA need to use block write protect function, so, only can use as the below parts

Winbond	W25X40BVSSIG	AKE37FN0N01	
EON	EN25F40-100HIP	AKE37ZN0Q00	

U17 colay with U12 for small size SPI FLASH

*EN25F40-100HIP

HWPG

INTERNAL KEYBOARD STRIP SET(KBC)

10/26 UnStuff

Quanta Computer Inc.
PROJECT : ZGA

Size	Document Number	Rev
	WPCE781 & FLASH	1A

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Quanta Computer Inc.

PROJECT : ZGA

Size	Document Number	Rev
	HDMI(1/2)	1A

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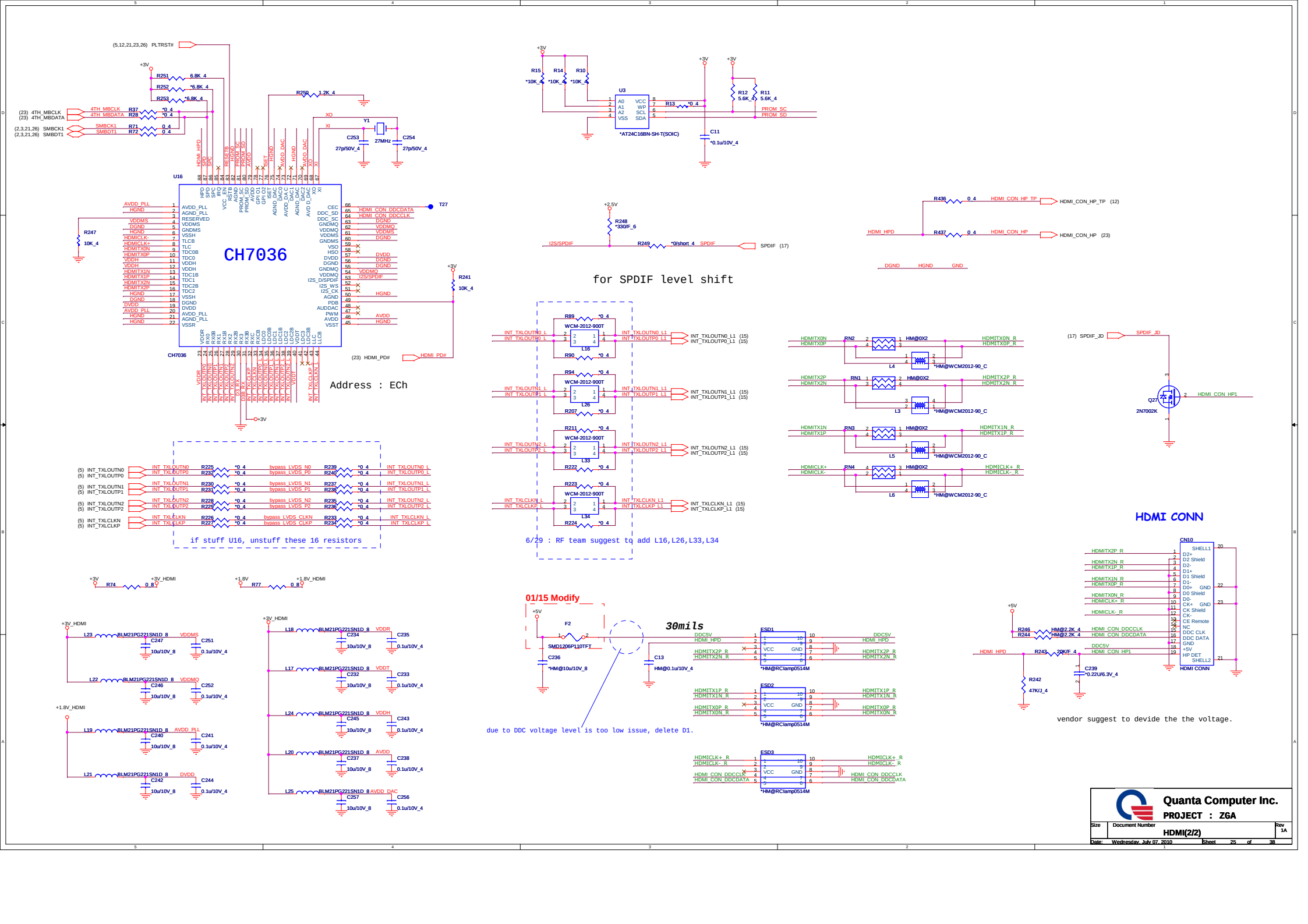
CH7036
U16
Address : ECh
if stuff U16, unstuff these 16 resistors
for SPDIF level shift
6/29 : RF team suggest to add L16,L26,L33,L34
01/15 Modify
30mils
due to DDC voltage level is too low issue, delete D1.
HDMI CONN
vendor suggest to devide the the voltage.
Quanta Computer Inc.
PROJECT : ZGA
HDMI(2/2)
Rev 1A
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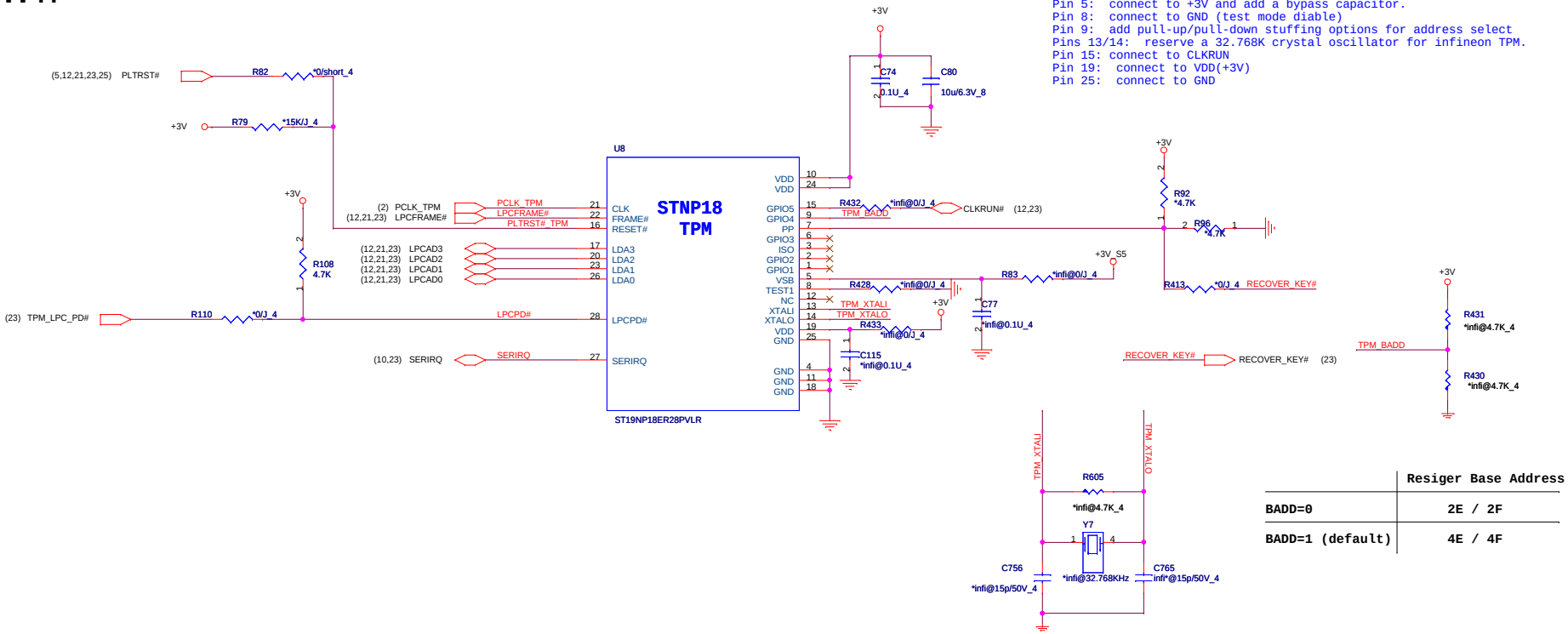
TPM

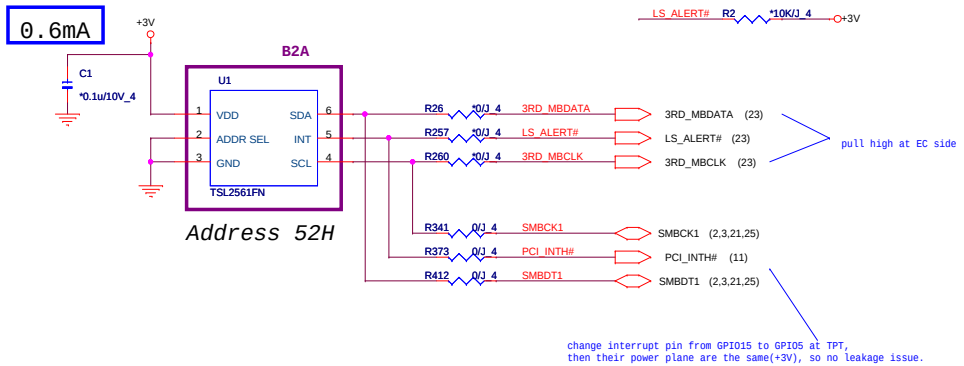
for google request to compliant with the full TPM pinout specification.(infineon TPM)
Pin 5: connect to +3V and add a bypass capacitor.
Pin 8: connect to GND (test mode diable)
Pin 9: add pull-up/pull-down stuffing options for address select
Pins 13/14: reserve a 32.768K crystal oscillator for infineon TPM.
Pin 15: connect to CLKRUN
Pin 19: connect to VDD(+3V)
Pin 25: connect to GND



	Resiger Base Address
BADD=0	2E / 2F
BADD=1 (default)	4E / 4F

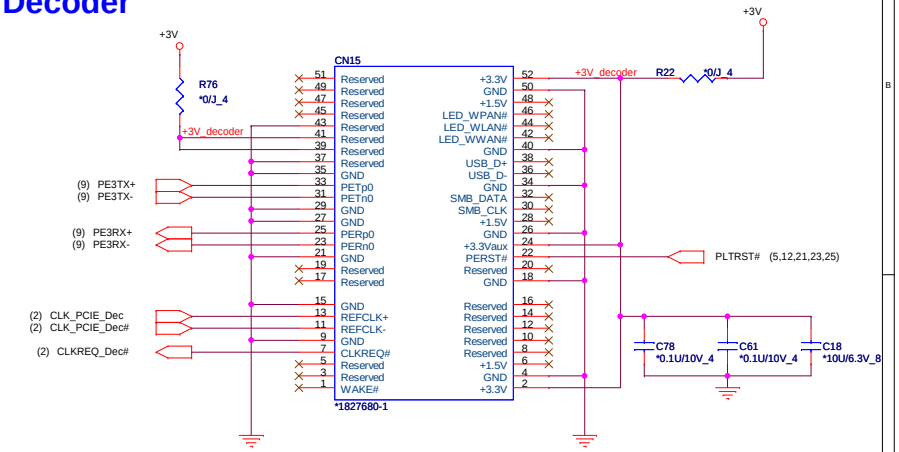
Light Sensor(LSR)

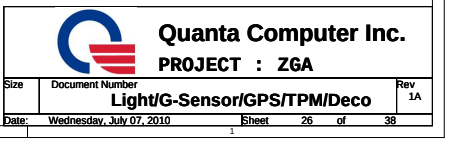
connector to EC, just stuff R2,R26,R257,R260
connector to TPT, just stuff R341,R373,R412

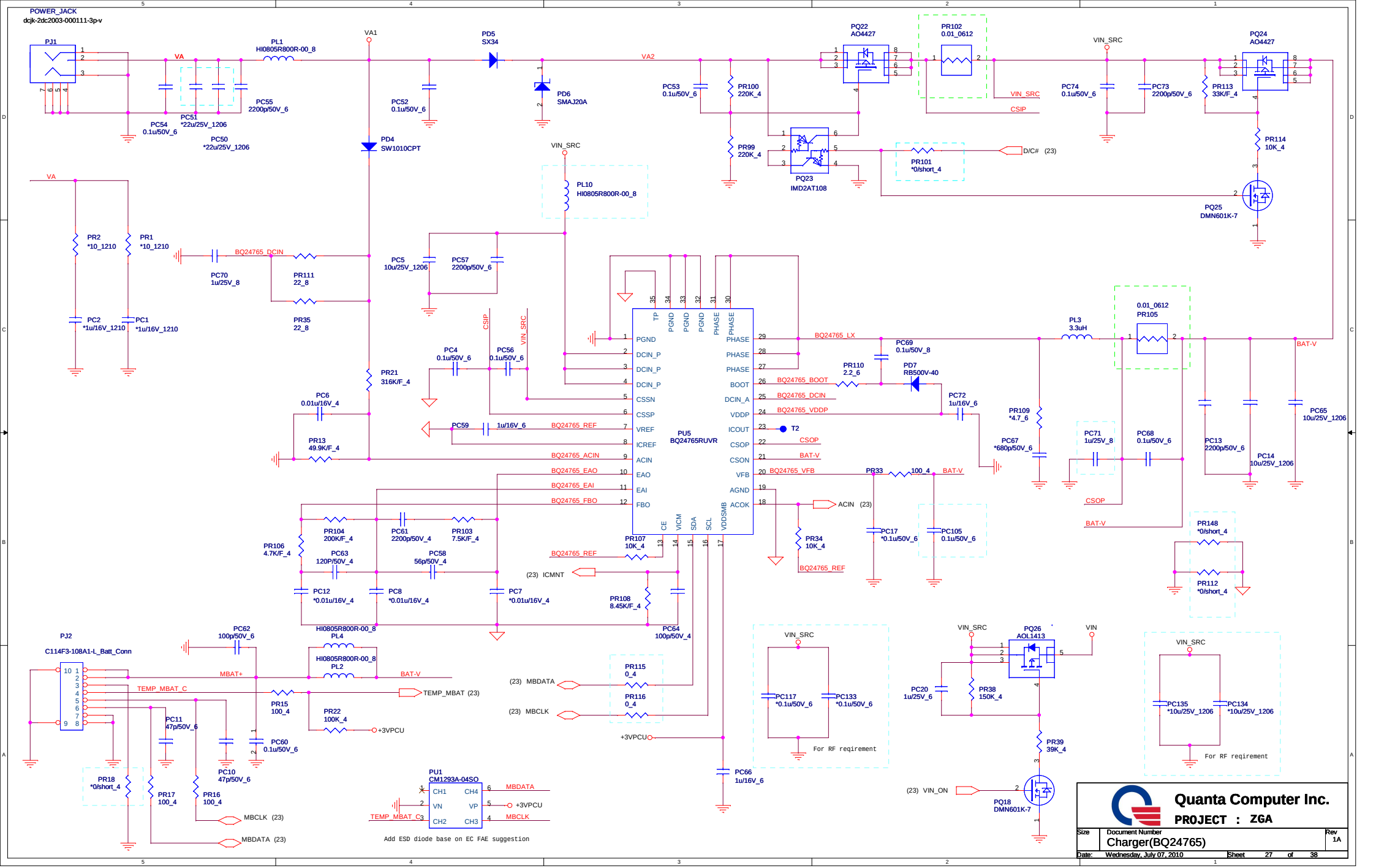


Video Decoder

dont need to stuff first, use innr document to add it.






POWER_JACK
dcjk-2dc2003-000111-3p-v
PJ1
VA
PL1
HI0805R800R-00_8
VA1
PD5
SX34
VA2
PD6
SMAJ20A
PC52
0.1u/50V_6
PC53
0.1u/50V_6
PR100
220K_4
PR99
220K_4
PQ22
AO4427
PR102
0.01_0612
VIN_SRC
CSIP
PQ23
IMD2AT108
PR101
*0/short_4
D/C# (23)
PQ24
AO4427
PR113
33K/F_4
PR114
10K_4
PQ25
DMN601K-7
PC74
0.1u/50V_6
PC73
2200p/50V_6
PC54
0.1u/50V_6
PC51
*22u/25V_1206
PC50
*22u/25V_1206
PC55
2200p/50V_6
PD4
SW1010CPT
PR2
*10_1210
PR1
*10_1210
PC2
*1u/16V_1210
PC1
*1u/16V_1210
BQ24765_DCIN
PC70
1u/25V_8
PR111
22_8
PR35
22_8
PL10
HI0805R800R-00_8
PC5
10u/25V_1206
PC57
2200p/50V_6
PR21
316K/F_4
PC6
0.01u/16V_4
PR13
49.9K/F_4
PC4
0.1u/50V_6
PC56
0.1u/50V_6
PC59
1u/16V_6
PU5
BQ24765RUVR
TP
PGND
DCIN_P
CSSN
CSSP
VREF
ICREF
ACIN
EAO
EAI
FBO
PHASE
BOOT
DCIN_A
VDDP
ICOUT
CSOP
CSON
VFB
AGND
ACOK
CE
VICM
SDA
SCL
VDDSMB
BQ24765_LX
BQ24765_BOOT
BQ24765_DCIN
BQ24765_VDDP
BQ24765_REF
BQ24765_ACIN
BQ24765_EAO
BQ24765_EAI
BQ24765_FBO
BQ24765_VFB
PR110
2.2_6
PD7
RB500V-40
PC72
1u/16V_6
PC69
0.1u/50V_8
PL3
3.3uH
0.01_0612
PR105
BAT-V
PR109
*4.7_6
PC67
*680p/50V_6
PC71
1u/25V_8
PC68
0.1u/50V_6
PC13
2200p/50V_6
PC14
10u/25V_1206
PC65
10u/25V_1206
PR33
100_4
PC17
*0.1u/50V_6
PC105
0.1u/50V_6
PR34
10K_4
ACIN (23)
CSOP
BAT-V
PR148
*0/short_4
PR112
*0/short_4
PR104
200K/F_4
PC61
2200p/50V_4
PR103
7.5K/F_4
PR106
4.7K/F_4
PC63
120P/50V_4
PC58
56p/50V_4
PC12
*0.01u/16V_4
PC8
*0.01u/16V_4
PC7
*0.01u/16V_4
PR107
10K_4
PR108
8.45K/F_4
PC64
100p/50V_4
(23) ICMNT
(23) MBDATA
(23) MBCLK
PR115
0_4
PR116
0_4
PJ2
C114F3-108A1-L_Batt_Conn
PC62
100p/50V_6
HI0805R800R-00_8
PL4
HI0805R800R-00_8
PL2
MBAT+
BAT-V
TEMP_MBAT_C
TEMP_MBAT (23)
PR15
100_4
PR22
100K_4
+3VPCU
PC11
47p/50V_6
PC10
47p/50V_6
PC60
0.1u/50V_6
PR18
*0/short_4
PR17
100_4
PR16
100_4
MBCLK (23)
MBDATA (23)
PU1
CM1293A-04SO
CH1
CH4
VN
VP
CH2
CH3
MBDATA
+3VPCU
MBCLK
TEMP_MBAT_C
Add ESD diode base on EC FAE suggestion
PC66
1u/16V_6
PC117
*0.1u/50V_6
PC133
*0.1u/50V_6
For RF reqirement
PQ26
AOL1413
VIN
PC20
1u/25V_6
PR38
150K_4
PR39
39K_4
(23) VIN_ON
PQ18
DMN601K-7
PC135
*10u/25V_1206
PC134
*10u/25V_1206
For RF reqirement
Quanta Computer Inc.
PROJECT : ZGA
Size
Document Number
Charger(BQ24765)
Rev
1A
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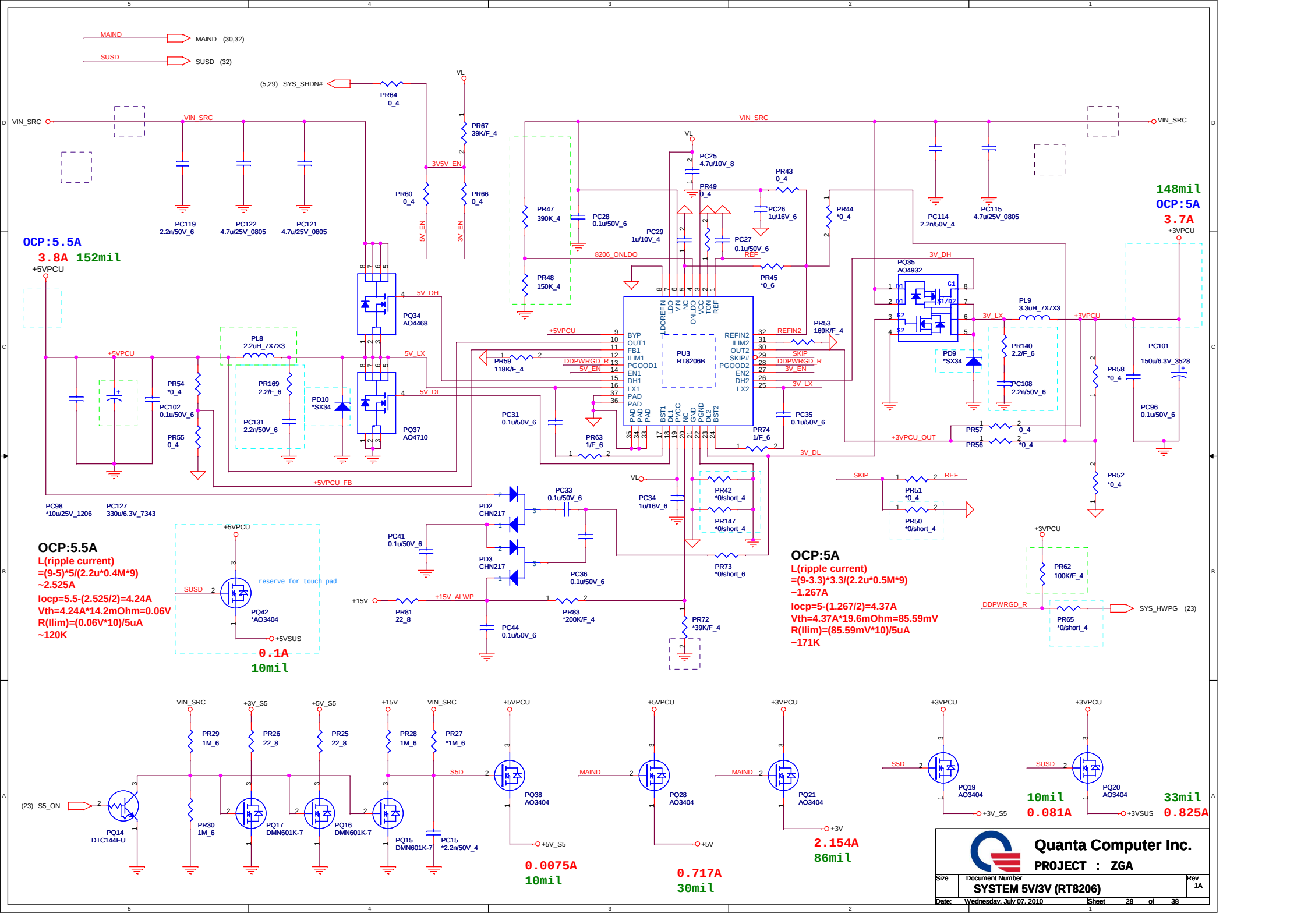
MAIND
MAIND (30,32)
SUSD
SUSD (32)
(5,29) SYS_SHDN#
VIN_SRC
VL
3V5V_EN
5V_EN
3V_EN
8206_ONLDO
REF
5V_DH
5V_LX
5V_DL
3V_DH
3V_LX
3V_DL
+5VPCU
+3VPCU
+5VPCU_FB
+3VPCU_OUT
DDPWRGD_R
REFIN2
SKIP
+15V
+15V_ALWP
SUSD
S5D
(23) S5_ON
SYS_HWPG (23)
PU3 RT8206B
PQ34 AO4468
PQ37 AO4710
PQ35 AO4932
PD2 CHN217
PD3 CHN217
PD9 *SX34
PD10 *SX34
PQ42 *AO3404
PQ14 DTC144EU
PQ15 DMN601K-7
PQ16 DMN601K-7
PQ17 DMN601K-7
PQ19 AO3404
PQ20 AO3404
PQ21 AO3404
PQ28 AO3404
PQ38 AO3404
PL8 2.2uH_7X7X3
PL9 3.3uH_7X7X3
PR64 0_4
PR67 39K/F_4
PR66 0_4
PR60 0_4
PR47 390K_4
PR48 150K_4
PR59 118K/F_4
PR63 1/F_6
PR74 1/F_6
PR53 169K/F_4
PR45 *0_6
PR44 *0_4
PR43 0_4
PR49 0_4
PR54 *0_4
PR55 0_4
PR169 2.2/F_6
PR140 2.2/F_6
PR58 *0_4
PR57 0_4
PR56 *0_4
PR52 *0_4
PR51 *0_4
PR50 *0/short_4
PR42 *0/short_4
PR147 *0/short_4
PR73 *0/short_6
PR72 *39K/F_4
PR81 22_8
PR83 *200K/F_4
PR62 100K/F_4
PR65 *0/short_4
PR29 1M_6
PR26 22_8
PR25 22_8
PR28 1M_6
PR27 *1M_6
PR30 1M_6
PC119 2.2n/50V_6
PC122 4.7u/25V_0805
PC121 4.7u/25V_0805
PC114 2.2n/50V_4
PC115 4.7u/25V_0805
PC25 4.7u/10V_8
PC26 1u/16V_6
PC27 0.1u/50V_6
PC28 0.1u/50V_6
PC29 1u/10V_4
PC31 0.1u/50V_6
PC33 0.1u/50V_6
PC34 1u/16V_6
PC35 0.1u/50V_6
PC36 0.1u/50V_6
PC41 0.1u/50V_6
PC44 0.1u/50V_6
PC98 *10u/25V_1206
PC127 330u/6.3V_7343
PC131 2.2n/50V_6
PC102 0.1u/50V_6
PC108 2.2n/50V_6
PC96 0.1u/50V_6
PC101 150u/6.3V_3528
PC15 *2.2n/50V_4
OCP:5.5A
3.8A 152mil
OCP:5.5A
L(ripple current)
=(9-5)*5/(2.2u*0.4M*9)
~2.525A
Iocp=5.5-(2.525/2)=4.24A
Vth=4.24A*14.2mOhm=0.06V
R(Ilim)=(0.06V*10)/5uA
~120K
reserve for touch pad
0.1A
10mil
148mil
OCP:5A
3.7A
OCP:5A
L(ripple current)
=(9-3.3)*3.3/(2.2u*0.5M*9)
~1.267A
Iocp=5-(1.267/2)=4.37A
Vth=4.37A*19.6mOhm=85.59mV
R(Ilim)=(85.59mV*10)/5uA
~171K
0.0075A
10mil
0.717A
30mil
2.154A
86mil
10mil
0.081A
33mil
0.825A
Quanta Computer Inc.
PROJECT : ZGA
Size
Document Number
SYSTEM 5V/3V (RT8206)
Rev
1A
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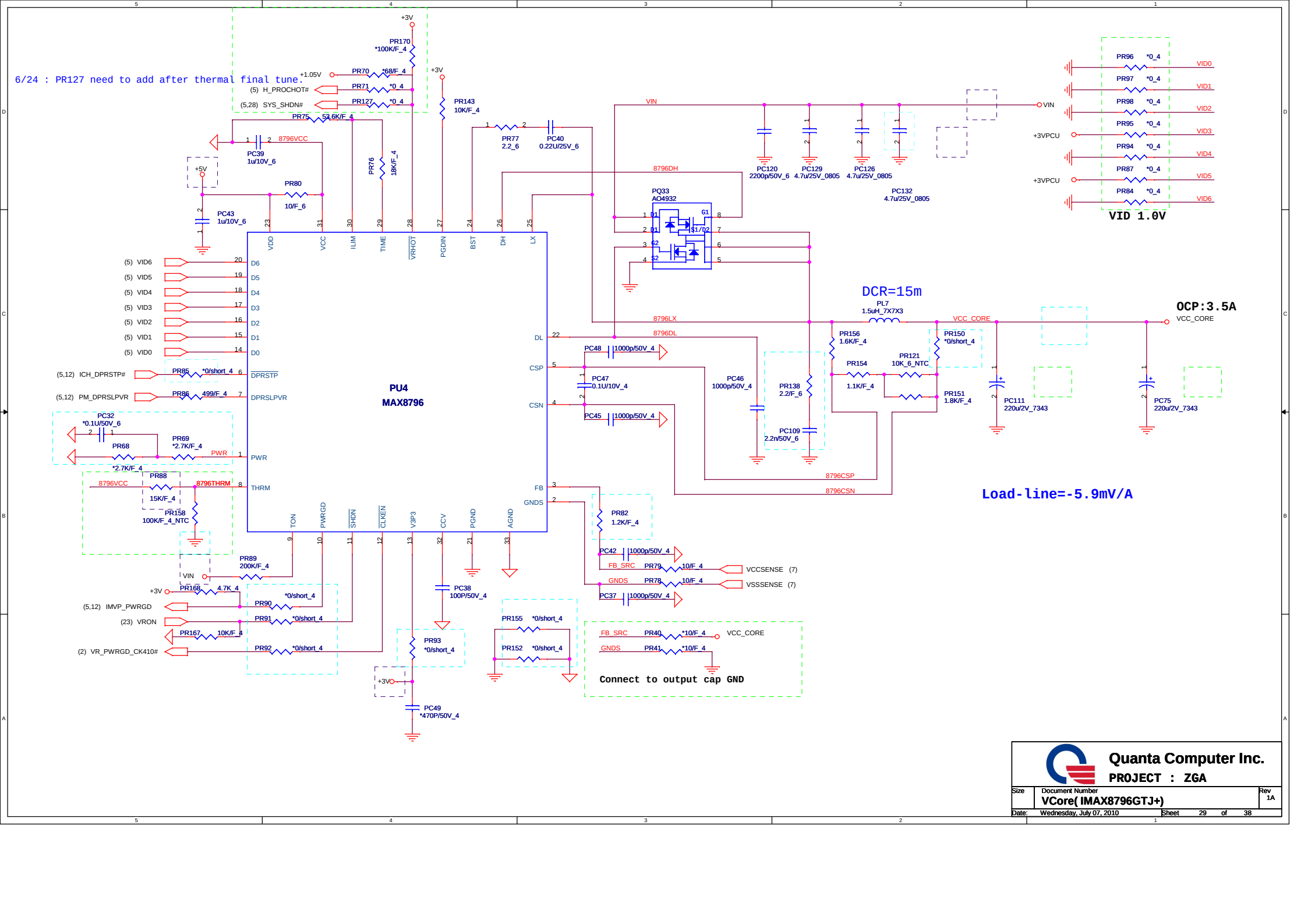
6/24 : PR127 need to add after thermal final tune
PU4
MAX8796
DCR=15m
OCP:3.5A
Load-line=-5.9mV/A
VID 1.0V
Connect to output cap GND
Quanta Computer Inc.
PROJECT : ZGA
VCore(IMAX8796GTJ+)
Wednesday, July 07, 2010
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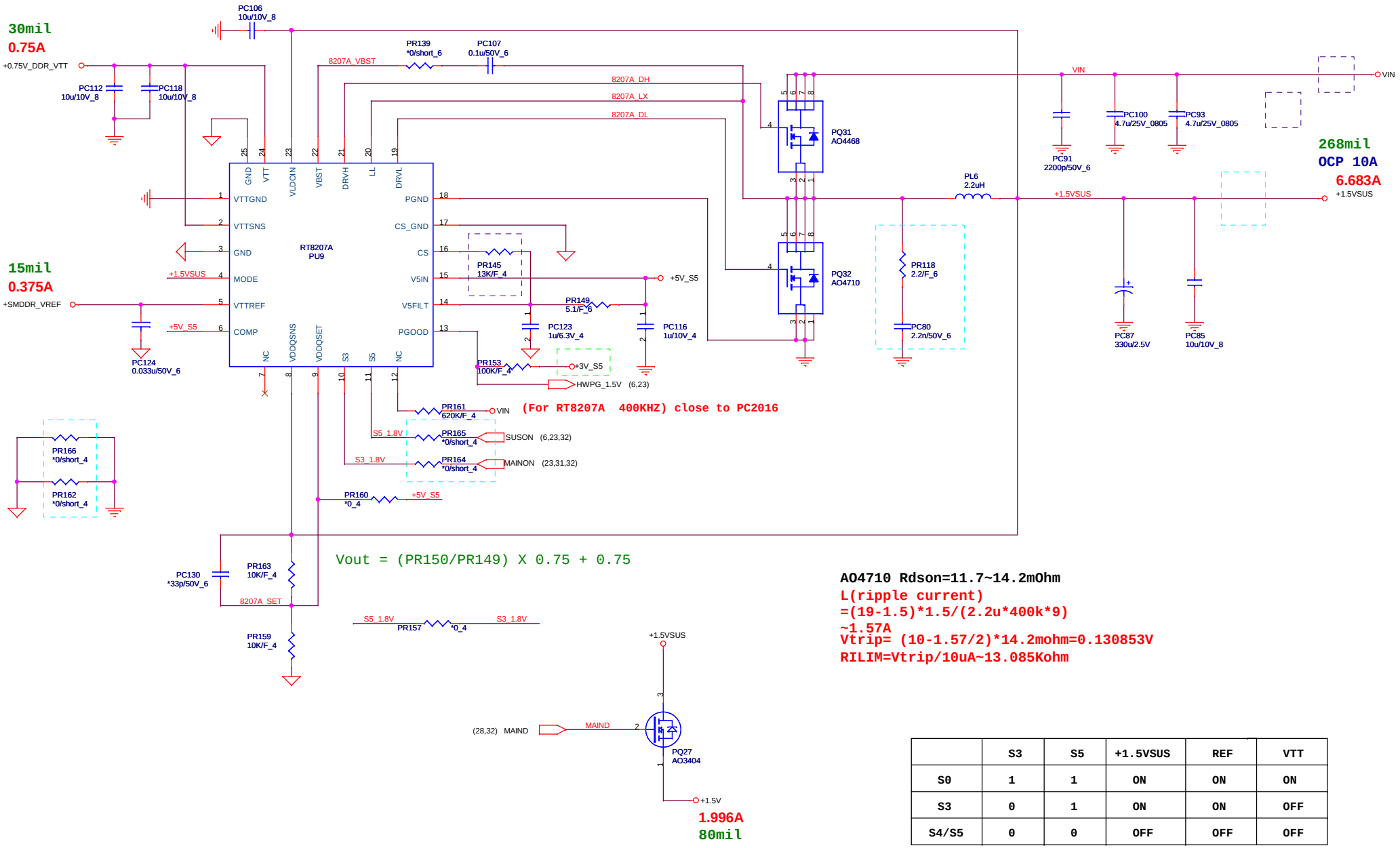
[PWM]



Vout = (PR150/PR149) X 0.75 + 0.75

AO4710 Rdson=11.7~14.2mOhm
L(ripple current)
=(19-1.5)*1.5/(2.2u*400k*9)
~1.57A
Vtrip= (10-1.57/2)*14.2mohm=0.130853V
RILIM=Vtrip/10uA~13.085Kohm

	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

Quanta Computer Inc.
PROJECT : ZGA

Size	Document Number	Rev
	DDR 1.5V(TPS51116)	1A

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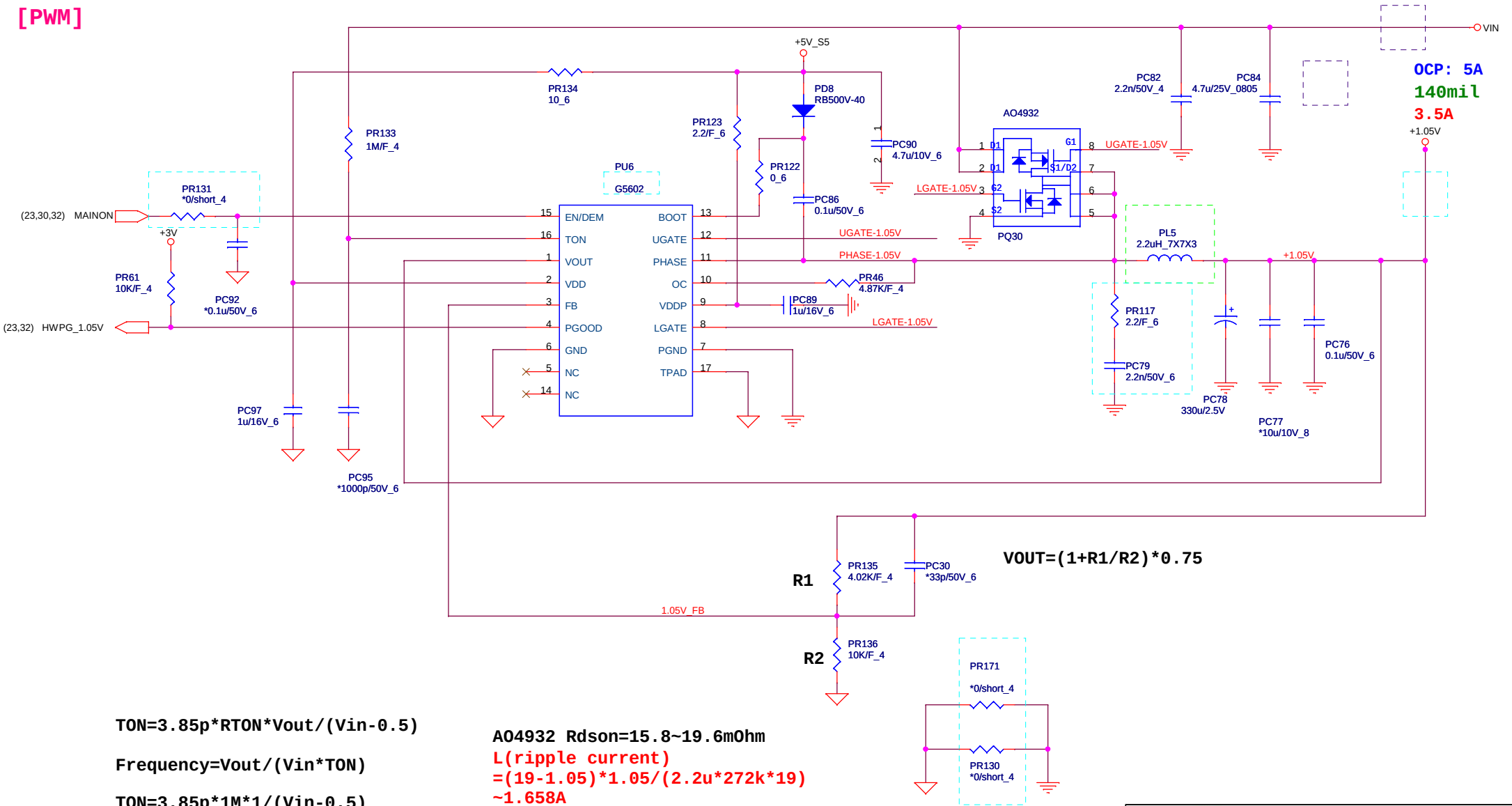

Quanta Computer Inc.

PROJECT : ZGA

Size	Document Number	Rev
	+1.05V(UP6111AQDD)	1A

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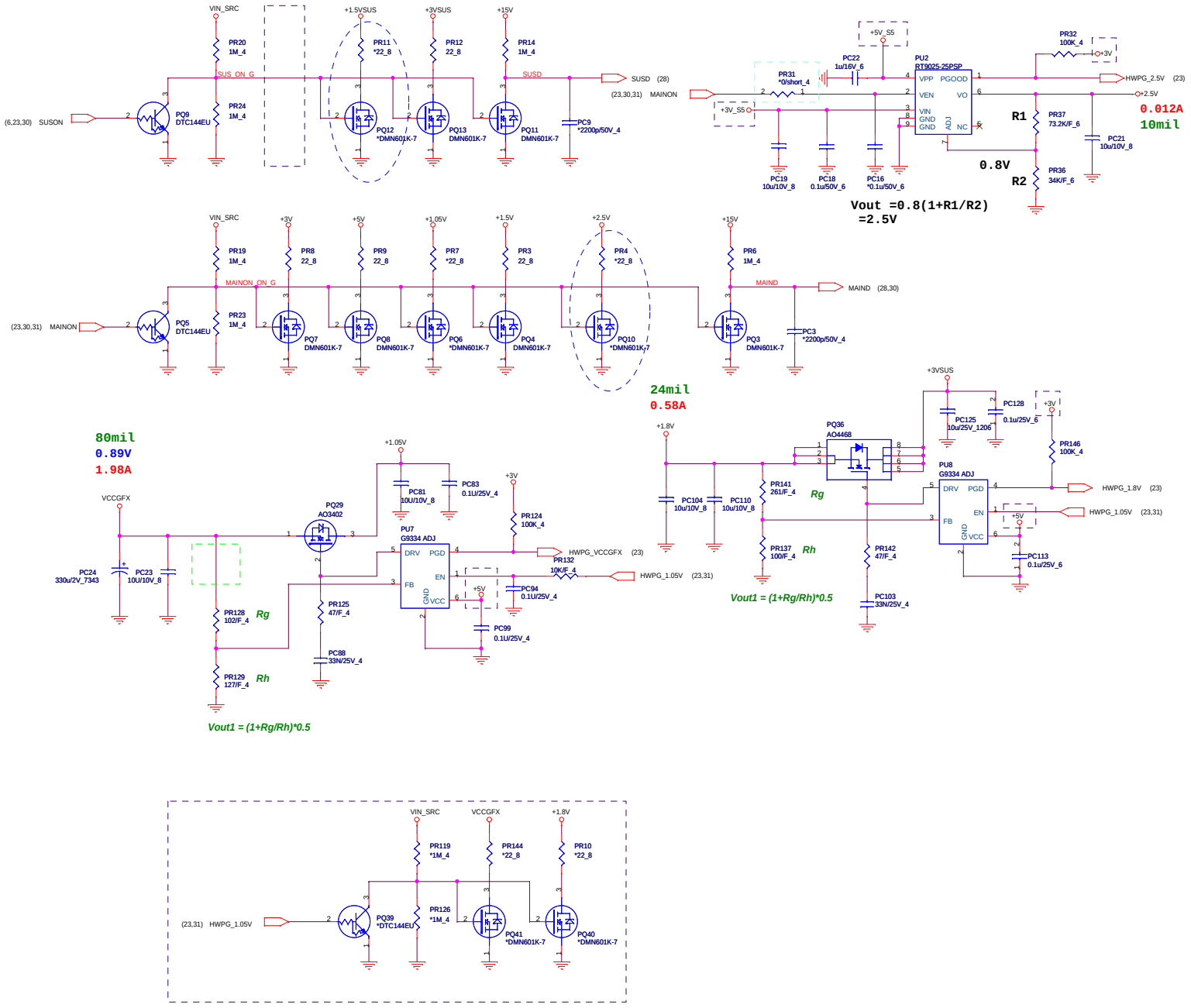

Quanta Computer Inc.		
PROJECT : ZGA		
Size	Document Number: Discharge/1.8V)	Rev: 1A
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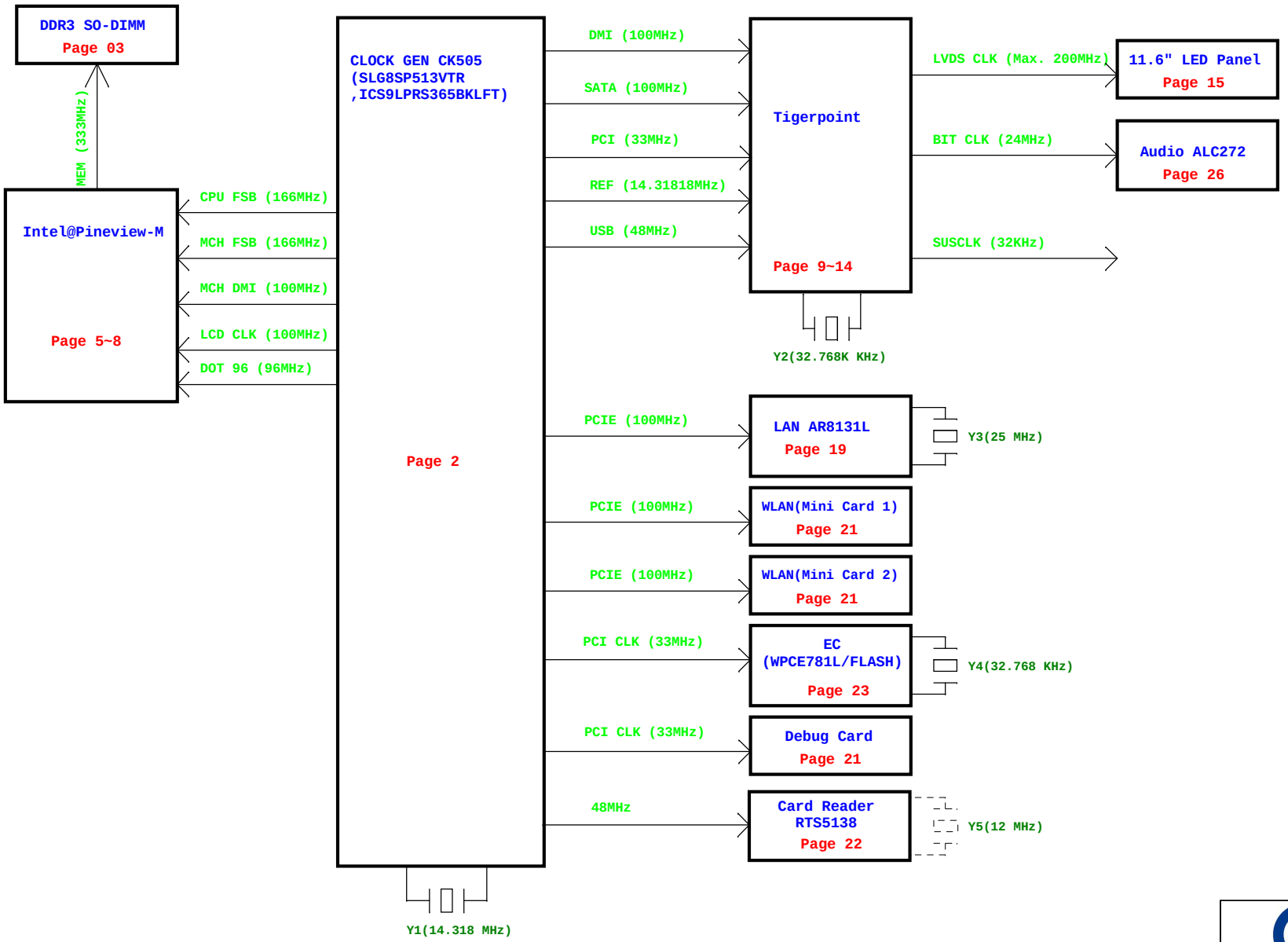
Quanta Computer Inc.	
PROJECT : ZGA	
Size	Document Number: Blank
Rev	1A
Date: Wednesday, July 07, 2010	Sheet 33 of 38



Quanta Computer Inc.

PROJECT : ZGA

Size	Document Number	Rev
	Clock Distribution Diagram	1B

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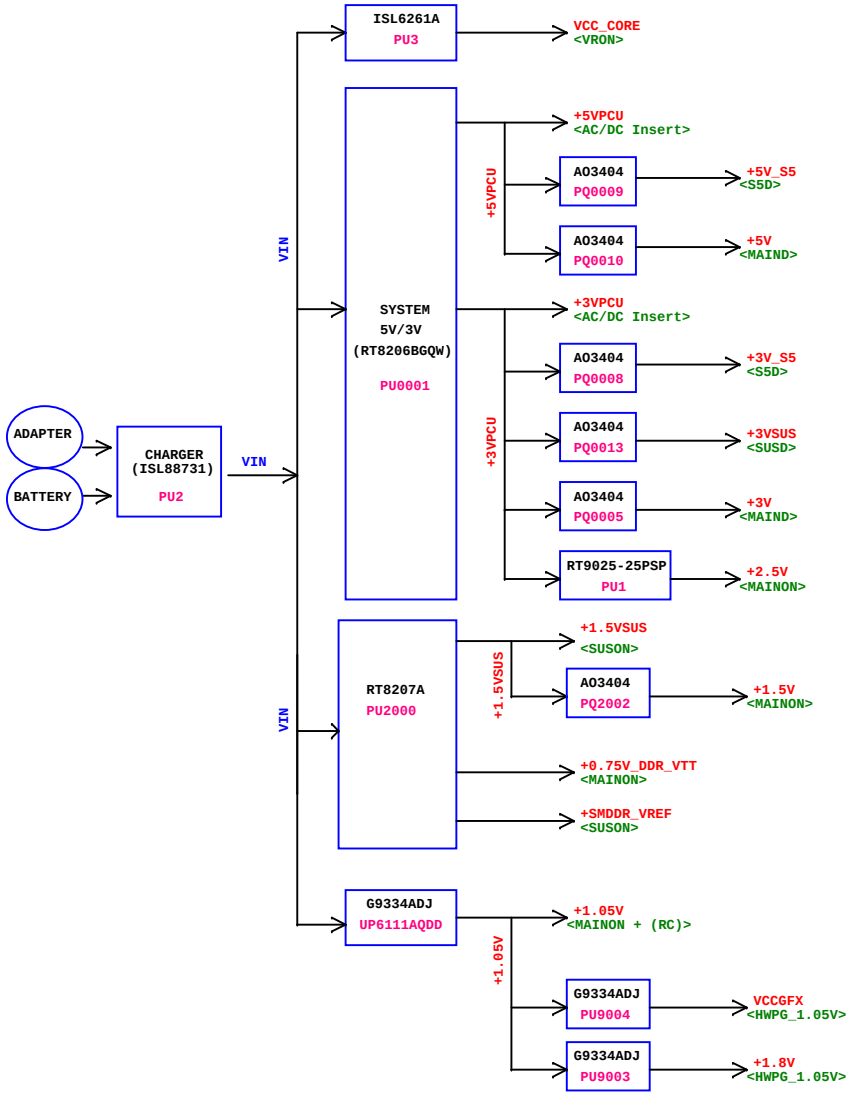
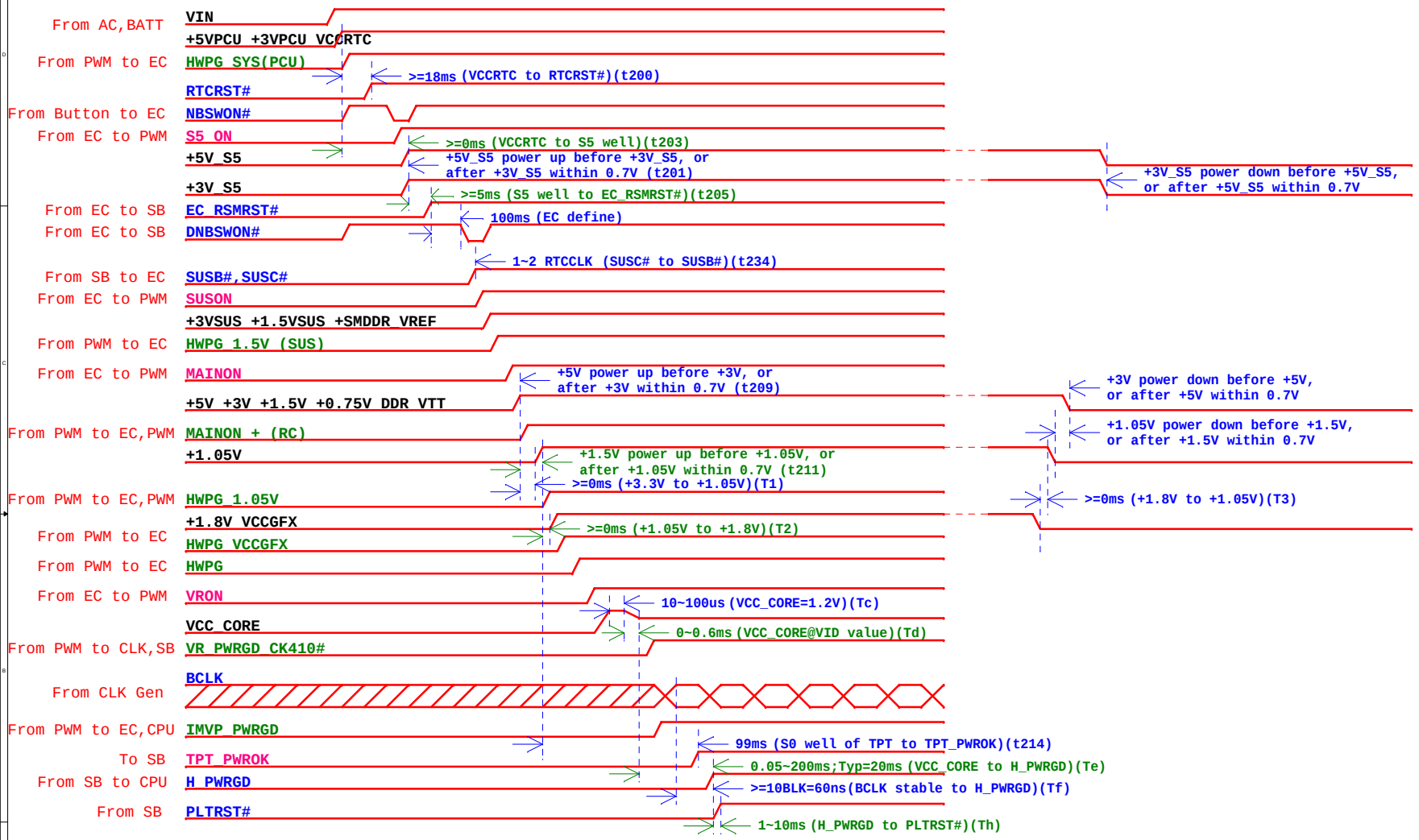


POWER	Distribution
VIN	LCD Backlight
VCC_CORE	CPU
+5VPCU	USB Connecter
+5V_S5	RTC, TPT
+5V	TPT , CRT , TouchPad , Codec , SATA , FAN , HDMI
+3VPCU	RTC, Hall Sensor, Light Sensor, EC, BIOS
+3V_S5	TPT , LAN , LAN EEPROM , RJ45 LED
+3VSUS	3G
+3V	CLK_GEN, CPU, TPT , LCD , CCD, DMIC, BT, Codec, WLAN/Wimax, Card reader, EC, DDR, HDMI
+1.5VSUS	DDR
+1.8V	CPU, HDMI
+1.5V	CPU, TPT
+0.75V_DDR_VTT	DDR
+SMDDR_VREF	CPU, DDR
+1.05V	CLK_GEN , CPU, TPT
VCCGFX	CPU
+2.5V	HDMI

ZGA Power On Sequence



*Note: EC will sampling SUSB# & SUSC# every 5ms.

ICH SMBUS Table

	CLK GEN	RAM	Mini Card (WLAN)	Mini Card (3G)
(SMB_DATA)/(SMB_CLK) (+3V_S5)	V	V	V	V
Power Plane	+3V	+3V	+3V	+3V_SUS
MOS CKT (Level shift)	Stuff	Stuff	*Reserve	Stuff

*Reserve: There is not SMBUS function in AVL

EC SMBUS Table

	Battery	CPU thermal Sensor	Light Sensor
EC781 SDA1 / SCL1 (+3VPCU)	V		
EC781 SDA2 / SCL2 (+3V)		V	
EC781 SDA3 / SCL3 (+3VPCU)			V
Power Plane	+3VPCU	+3V	+3VPCU
MOS CKT (Level shift)	X	X	X

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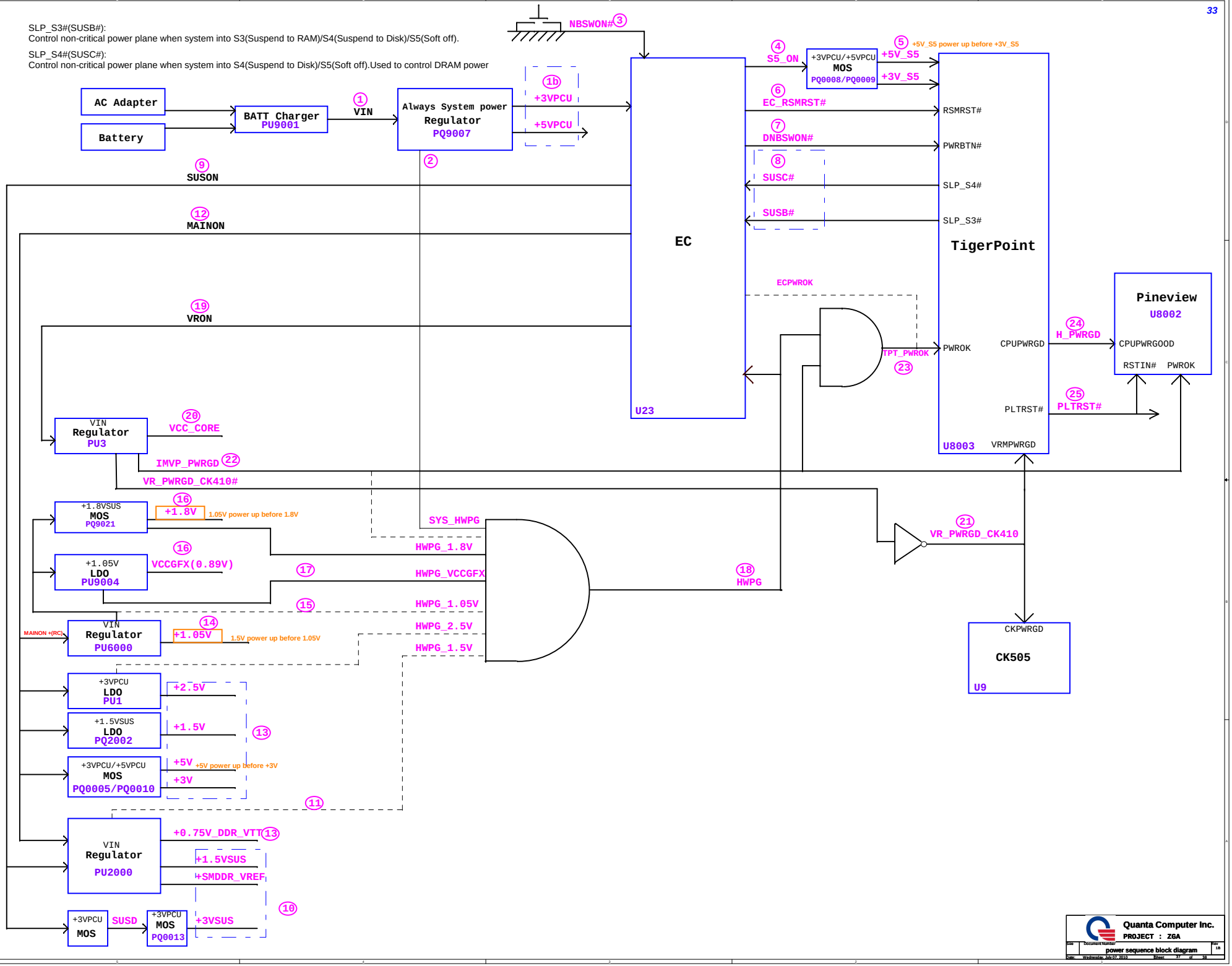
SLP_S3#(SUSB#):
Control non-critical power plane when system into S3(Suspend to RAM)/S4(Suspend to Disk)/S5(Soft off).

SLP_S4#(SUSC#):
Control non-critical power plane when system into S4(Suspend to Disk)/S5(Soft off).Used to control DRAM power



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power sequence block diagram
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Model	REV	CHANGE LIST	MODEL	ZGA FROM	ZGA To
ZGA MB	A1	FIRST RELEASED: (PCB:A)		X	1A
	A2 (V1.3)	delete CRT function			
		delete on board LAN function			
		page 16 : change CN2 follow KB pin define			
		page 16 : change CN4 pin define for deleting sata and caps LED			
		page 16 : add SW5 and SW6 for power on the system easily.			
		page 17 : follow the vendor's suggetsion to change R300 and R301 from 75 ohm to 47 ohm.			
		page 17 : add R206 for HDMI spdif function.			
		page 25 : add R74 and R77 for measuring the power consumption of HDMI function.			
	A2 (V1.4)	page 21 : stuff R32 and add R340,R423,R424 for 3G LED purple light issue.			
		page 18 : add C15 and C122 for EMI.			
		page 16 : use LVDS to HDMI solution, so delete CN11(RGB to HDMI solution)			
		page 21 : add R80,R81,R429,R435,L35 and L14 for RF request for EMI.			
		page 22 : add R86,R87 and L15 for RF request for EMI.			
		page 26 :(issue 86) connect pin 5 of U8 to +3V_S5 plane by R83 to meet standard TPM pincount.			
		page 25 : add R89,R90,R94,R207,R211~R224, L16,L26,L33 and L34 for RF request for EMI.			
		page 26 : (issue 102) reserve R341,R412 and D26 to connect Light sensor to TPT.			
		page 23 : (issue 109) delete R373 to ensure that the MANU_SW net can be read, but not written to by both the EC and Tigerpoint.			
	A2 (V1.5)	page 11,26 : (issue 102) change interrupt pin from GPIO15 to GPIO5 at TPT, then their power plane are the same(+3V), so no leakage issue and can del D26, only connected by R373.			
		page 26 : (issue 86) to compliant with the full TPM pin out specification(infineon TPM). Change the circuit as below. pin 5 : connect pin5 of U8 to +3V_S5 plane by R83 and add a bypass capacitor C77. pin 8 : connect to GND (test mode diable) pin 9 : reserve pull-up/pull-down resistors R430,R431 stuffing options for address select pins 13/14 : reserve a 32.768K crystal(Y7),R605,C756,C765 to compliant with the full TPM pinout specification(infineon TPM) pin 15 : reserve R432 to connect CLKRUN of TPT,EC and TPM. pin 19 : connect to VDD(+3V) by R433 and add a bypass capacitor pin 25 : connect to GND			
	A2 (V1.6)	page 26 : (issue 86) connect U8.8 to GND by reserve R428 to prevent trouble with ST part. move C77 close to U8.5.			
		page 23 : (issue 109) move D32, C386 to the MANU_SW_R net. add R434,Q29,R429 to prevent EC(+3VPCU) leakage current to TPT(+3V_S5).			
		page 26 : (issue 102) control light sensor by TPT, so, stuff R341,R373,R412 and unstuff R2,R26,R257,R260.			
		page 25 : (issue 126) connect U16.49 to GPIO22 (+3V power plane)of TPT by R435(0 ohm).			
	A2 (V1.7)	page 25 : (issue 126) According to currently architecture, most HDMI algorithm is controller by EC, not tigerpoint. So, change the circuit to connect U16.49 to GPIO10 (+3VPCU power plane)of EC and add D11 to prevent leakage issue.			
	A2 (V1.8)	page 23 : (issue 109) change Q28 from P-mos to N-mos. Tie Q29 gate to MANU_SW_R, Tie Q29 source to GND, Tie Q29 drain through R434 to +3V_S5 and to MANU_SW_TPT, Delete R429.			
	A2 (V1.9)	page 15 : unstuff R45 and stuff R44 for TPT to control LVDS_PWM.			
		page 25 : unstuff R28,R37 and stuff R71,R72 for TPT to control HDMI function.			
	B (V2.0)	page 12, 25 : (issue 124)connect HDMI_CON_HP_TP to GPIO pin15 of Tigerpoint for support interrupt function.			
	1D				

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