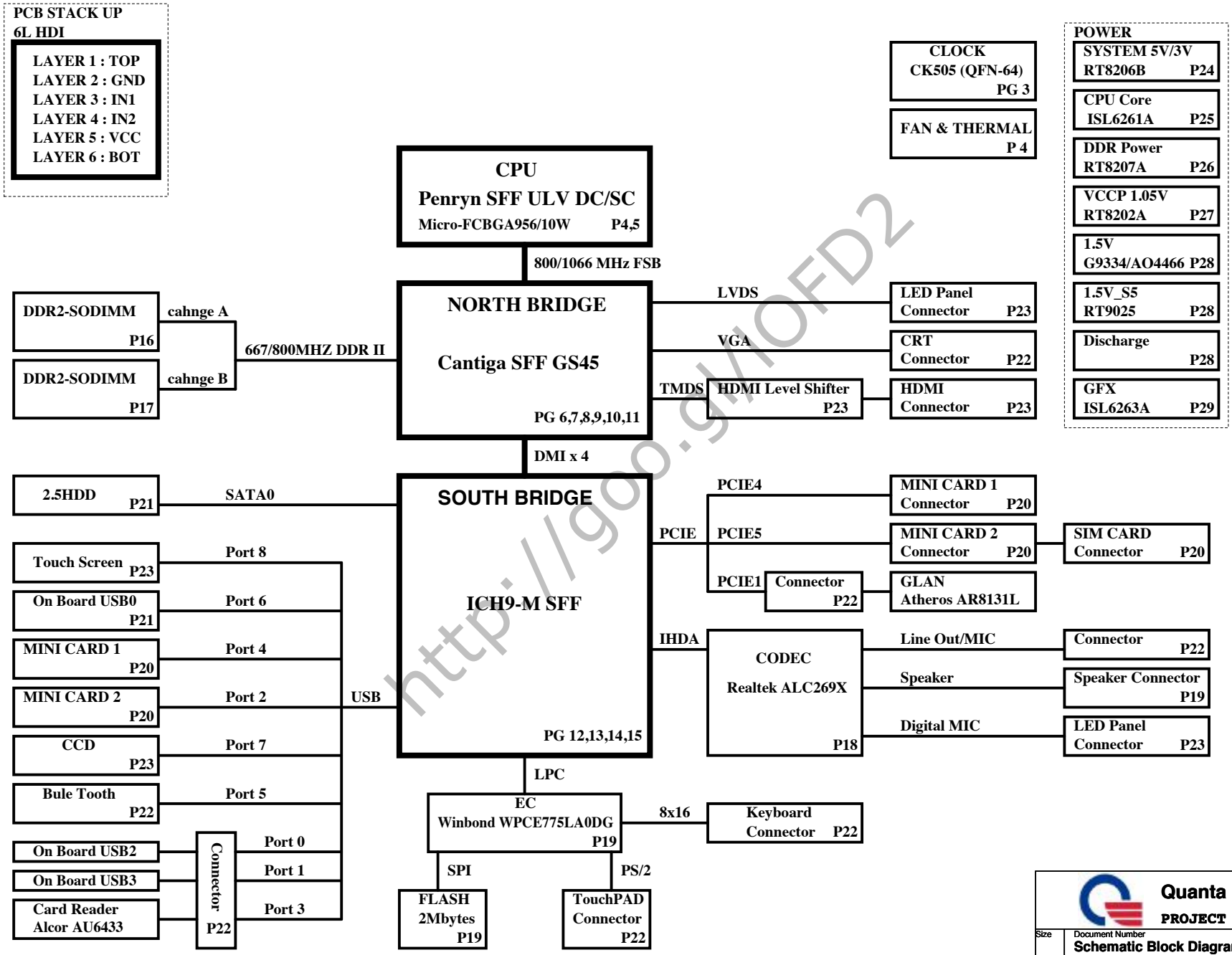
ZE8 BLOCK DIAGRAM



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PROJECT : ZE8

Size	Document Number	Rev
	Schematic Block Diagram	1A

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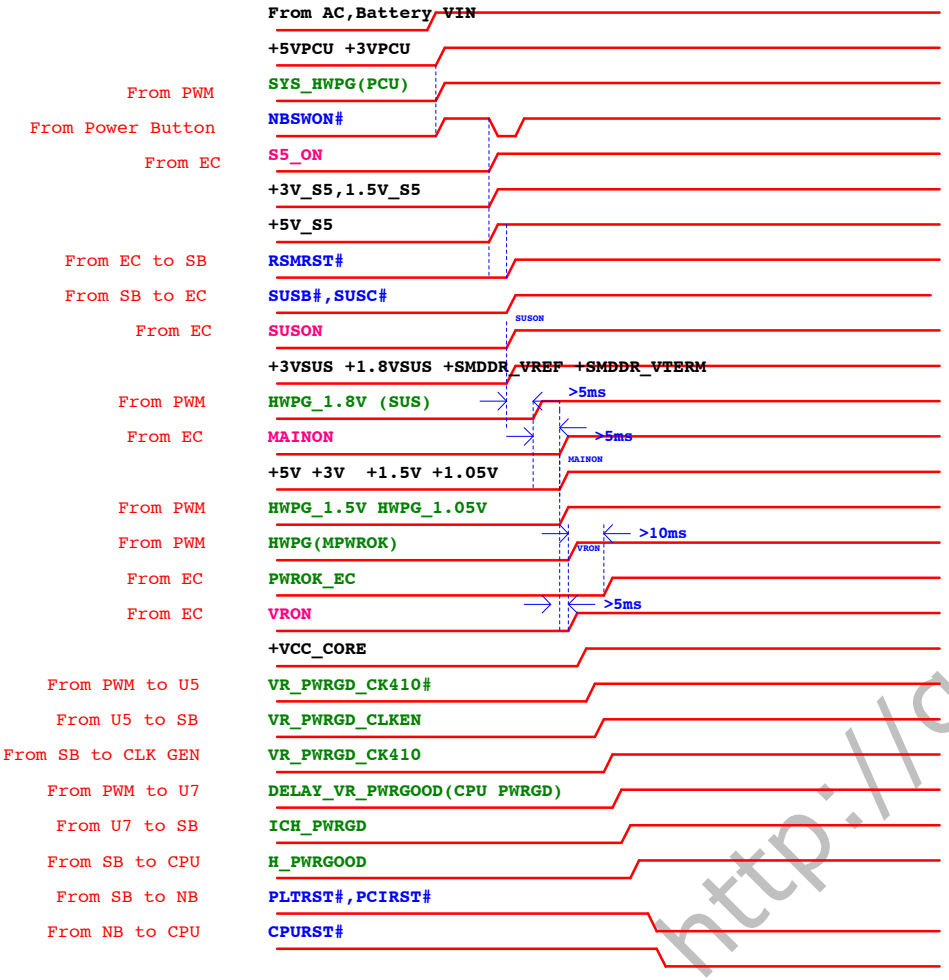
ZE8 Power On Sequence



BOM naming rule

Items	Function	Name	Description
1	With HDMI	HD@	
2	Without HDMI	NHD@	
3	3G Module	3G@	
4			
5			
6			

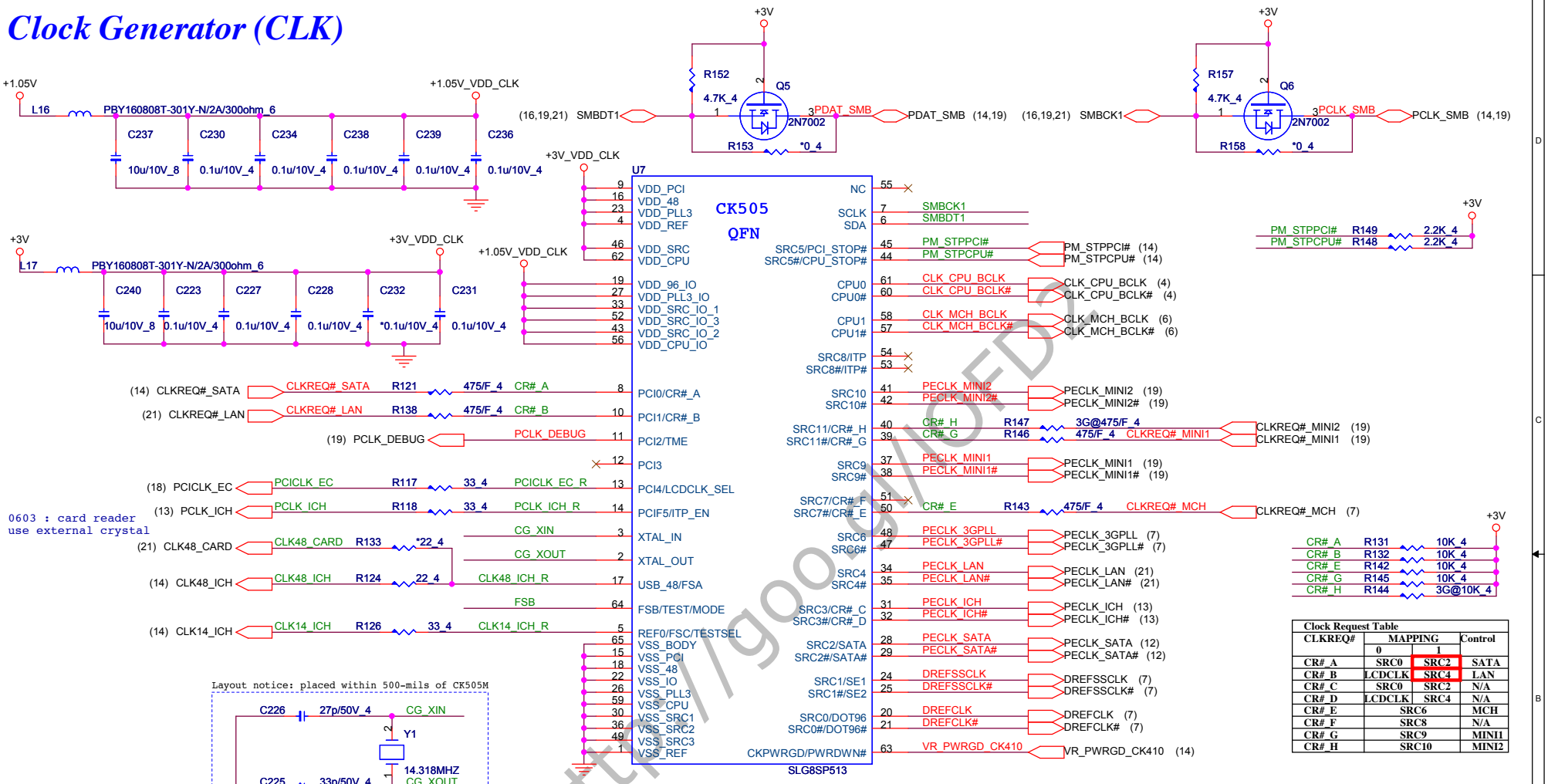
ICH9M SFF SMBUS Table

	CLK GEN	RAM	Mini Card (WLAN/WMAX)	Mini Card (3G)	G sensor
(SMB_DATA) / (SMB_CLK) (+3V_S5)	V	V	V	V	V
Power Plane	+3V	+3V	+3V	+3VSUS	+3V
MOS CKT	Stuff	Stuff	Stuff	Stuff	Stuff

EC SMBUS Table

	Battery	CPU thermal Sensor	EC EEPROM
EC775 SDATA1/SCLK1(+3VPCU)	V		
EC775 SDATA2/SCLK2(+3V)		V	
EC775 SDATA3/SCLK3(+3VPCU)			V
Power Plane	+3VPCU	+3V	+3VPCU
MOS CKT	X	X	X

Clock Generator (CLK)



SLG8SP513VTR ,ICS9LPRS365BKLFT

SMbus address D2

Clock Request Table			
CLKREQ#	MAPPING 0	MAPPING 1	Control
CR# A	SRC0	SRC2	SATA
CR# B	LCDCLK	SRC4	LAN
CR# C	SRC0	SRC2	N/A
CR# D	LCDCLK	SRC4	N/A
CR# E	SRC6		MCH
CR# F	SRC8		N/A
CR# G	SRC9		MINI1
CR# H	SRC10		MINI2

	SLG8SP513VTR (AL8SP513000)	ICS9LPRS365 (ALPRS365000)	PULL HIGH	PULL DOWN
Pin 11	PCI2/TME	PCI2/TME	NO OVERCLOCKING (default)	NORMAL RUN
Pin 13	PCI4/ 27_Select	PCI_4/ SEL_LCDCLK#	PIN 24/25 IS 27MHz	PIN 24/25 IS SRC/DOT (default)
Pin 14	PCIF-5/ITP_EN	PCIF-5/ITP_EN	PIN 53/54 IS CPUITP	PIN 53/54 IS SRC8 (default)

<MAIN> : SLG8SP513VTR(AL8SP513000)
<SECOND> : ICS9LPRS365BKLFT(ALPRS365000)

FSC	FSB	FSA	CPU (MHz)	SRC (MHz)	PCI (MHz)	REF (MHz)	DOT96 (MHz)	USB (MHz)
0	0	0	266.6	100.0	33.3	14.318	96.0	48.0
0	0	1	133.3	100.0	33.3	14.318	96.0	48.0
0	1	0	200.0	100.0	33.3	14.318	96.0	48.0
0	1	1	166.6	100.0	33.3	14.318	96.0	48.0
1	0	0	333.3	100.0	33.3	14.318	96.0	48.0
1	0	1	100.0	100.0	33.3	14.318	96.0	48.0
1	1	0	400.0	100.0	33.3	14.318	96.0	48.0
1	1	1	Reserved					

ITP_EN	Pin 53/54
0	SRC_8/SRC_8#
1	ITP/ITP#

LCDCLK_SEL	Pin 20/21	Pin 24/25
0	DOT_96/DOT96#	LCDCLK/LCDCLK#
1	SRC_0/SRC_0#	27M/27M_SS

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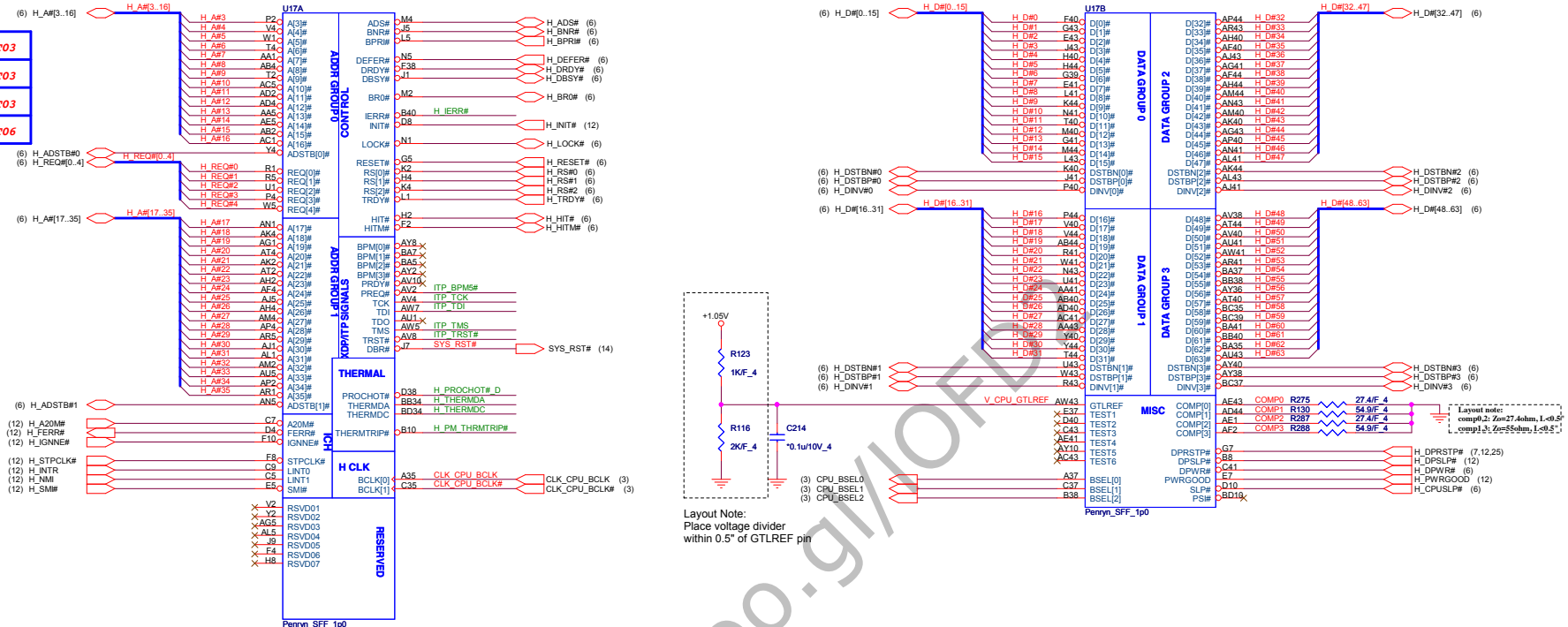
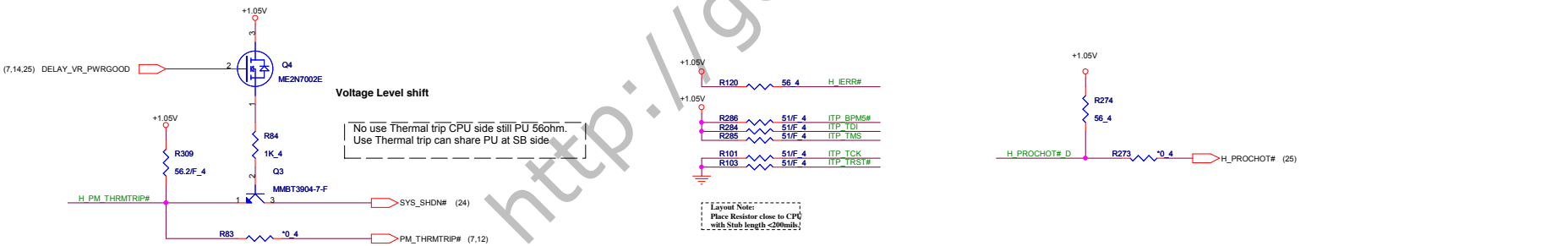
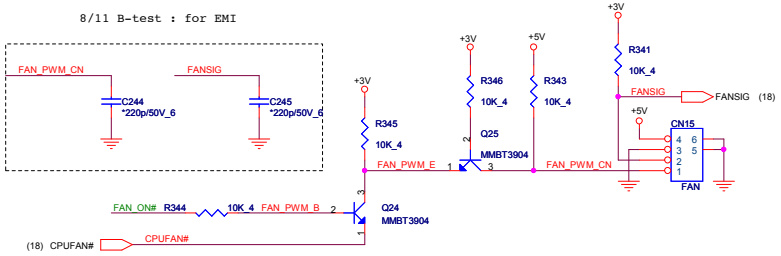
Penryn SFF - Host Bus (CPU)

Celeron 743	AJSLGEVVT03
SU2300	AJSLGYWVT03
SU4100	AJSLGS4VT03
SU7300	AJSLGYVVT06

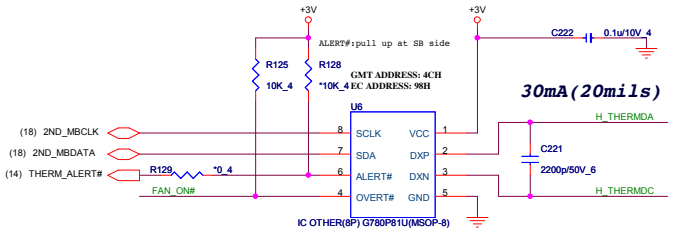




CPU FAN CTRL(THM)



CPU Thermal Monitor(THM)



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	Penryn SFF (Host Bus)/FAN/Thermal	1A
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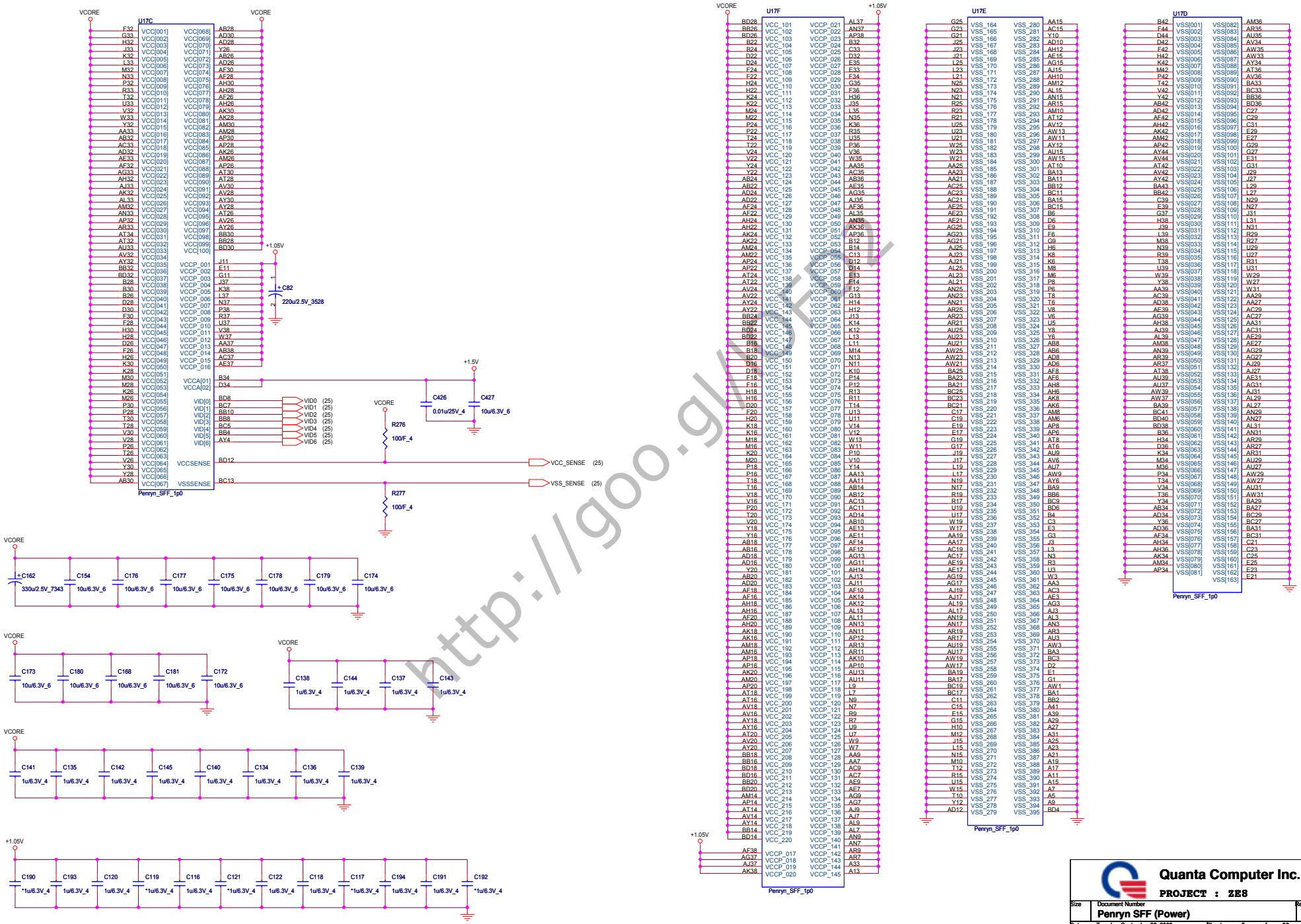
Penryn SFF - Power (CPU)



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Size	Document Number: Penryn SFF (Power)	Rev: 1A
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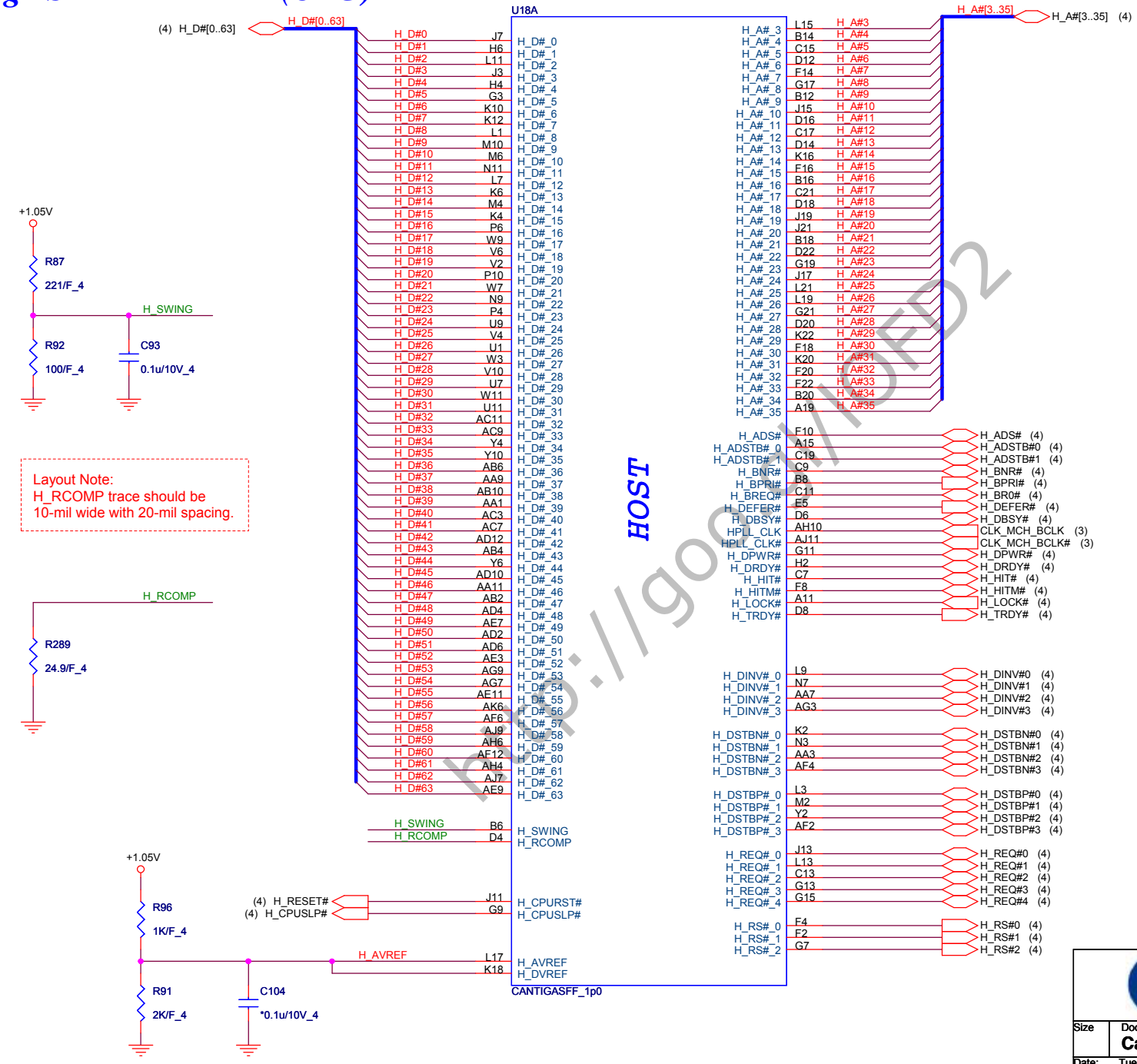
Cantiga SFF - Host Bus (CLG)



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Size	Document Number	Rev
	Cantiga SFF (Host Bus)	1A
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Cantiga SFF - DMI/VGA (CLG)

Intel GS40/GS45 Strapping Signals and Configuration		
Pin Name	Strap Description	Configuration
CFG2:0	FSB Frequency	000 = FSB1066 010 = FSB800 011 = FSB667 Other = Reserved
CFG4:3	Reserved	
CFG5	DMI x2 Select	1 = DMI x 4 0 = DMI x2
CFG6	ITPM Host Interface	1 = ITPM disabled 0 = ITPM enabled
CFG7	Intel Management Engine Crypto Strap	1 = Intel Management Engine Crypto TLS cipher suite with confidentiality 0 = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality
CFG8	Reserved	
CFG9	PCIE Graphics Lane	1 = Normal operation : Lane Numbered in Order 0 = Reverse Lanes
CFG10	PCIE Loopback enable	1 = Disabled 0 = Enabled
CFG11	Reserved	
CFG12	ALLZ	1 = Disabled 0 = ALLZ mode enabled
CFG13	XOR	1 = Disabled 0 = XOR mode enabled
CFG14	Reserved	
CFG15	Reserved	
CFG16	FSB Dynamic ODT	1 = Dynamic ODT enabled 0 = Dynamic ODT disabled
CFG17	Reserved	
CFG18	Reserved	
CFG19	DMI Lane Reversal	1 = Reverse Lanes 0 = Normal operation : Lane Numbered in Order
CFG20	Digital DisplayPort (SDVO/DP/iHDMI) Concurrent with PCIE	1 = Digital DisplayPort (SDVO/DP/iHDMI) and PCIE are operating simultaneously via the PEG port 0 = Digital DisplayPort (SDVO/DP/iHDMI) or PCIE are operational
SDVO_CTRLDATA	SDVO Present	1 = SDVO/IHDMI/DP interface enabled 0 = No SDVO/IHDMI/DP interface disabled
L_DDC_DATA	Local Flat Panel (LFP) Present	1 = LFP Card Present; PCIE disabled 0 = LFP Disable
DDPC_CTRLDATA	Digital Display Present	1 = Digital display (iHDMI/DP) device present 0 = Digital display (iHDMI/DP) interface absent

- The recommended pull-up resistor value is 4.02 k Ω ±1%
- The recommended pull-down resistor value is 2.21 k Ω ±1%.

U18B

RSVD / CONTROL/COMPENSATION

J43 RSVD1
L43 RSVD2
J41 RSVD3
L41 RSVD4
AN11 RSVD5
AM10 RSVD6
AK10 RSVD7
AL11 RSVD8
F12 RSVD9
C27 RSVD14
D30 RSVD15
J9 RSVD17
AW42 RSVD20
BB20 RSVD22
BE19 RSVD23
BF20 RSVD24
BF18 RSVD25

DDR CLK / CONTROL / COMPENSATION

SA_CK_0 BB32 → M_CLK_DDR0 (16)
SA_CK_1 BB25 → M_CLK_DDR1 (16)
SB_CK_0 BA33 → M_CLK_DDR2 (16)
SB_CK_1 BA23 → M_CLK_DDR3 (16)
SA_CK#_0 BA31 → M_CLK_DDR#0 (16)
SA_CK#_1 BC25 → M_CLK_DDR#1 (16)
SB_CK#_0 BC33 → M_CLK_DDR#2 (16)
SB_CK#_1 BB24 → M_CLK_DDR#3 (16)
SA_CKE_0 BC35 → M_CKE0 (16)
SA_CKE_1 BB33 → M_CKE1 (16)
SB_CKE_0 BE37 → M_CKE2 (16)
SB_CKE_1 BC37 → M_CKE3 (16)
SA_CS#_0 BK18 → M_CS#0 (16)
SA_CS#_1 BK16 → M_CS#1 (16)
SB_CS#_0 BE23 → M_CS#2 (16)
SB_CS#_1 BC19 → M_CS#3 (16)
SA_ODT_0 BJ17 → M_ODT0 (16)
SA_ODT_1 BJ19 → M_ODT1 (16)
SB_ODT_0 BC17 → M_ODT2 (16)
SB_ODT_1 BE17 → M_ODT3 (16)

SM_VREF=0.5*VCC_SM
SM_PWROK only for DDR3.(DDR2 PD only)
SM_DRAMRST# only for DDR3.(DDR2:NC)

SM_RCOMP BL25 SMRCOMPP
SM_RCOMP# BK26 SMRCOMPN
SM_RCOMP_VOH BK32 SM_RCOMP_VOH
SM_RCOMP_VOL BL31 SM_RCOMP_VOL
SM_VREF BC51 +SMDDR_VREF_NB
SM_PWROK AY37 SM_PWROK
SM_REXT BH20 SM_REXT
SM_DRAMRST# BA37 → DDR3_RST# (16)

DDR CLK

DPLL_REF_CLK B42 DREFCLK → DREFCLK (3)
DPLL_REF_CLK# D42 DREFCLK# → DREFCLK# (3)
DPLL_REF_SSCLK B50 DREFSSCLK → DREFSSCLK (3)
DPLL_REF_SSCLK# D50 DREFSSCLK# → DREFSSCLK# (3)
PEG_CLK R49 PECLK_3GPLL → PECLK_3GPLL (3)
PEG_CLK# P50 PECLK_3GPLL# → PECLK_3GPLL# (3)

DMI / CFG

DMI_RXN_0 AG55 → DMI_MRX_ITX_N0 (13)
DMI_RXN_1 AL49 → DMI_MRX_ITX_N1 (13)
DMI_RXN_2 AH54 → DMI_MRX_ITX_N2 (13)
DMI_RXN_3 AL47 → DMI_MRX_ITX_N3 (13)
DMI_RXP_0 AG53 → DMI_MRX_ITX_P0 (13)
DMI_RXP_1 AK50 → DMI_MRX_ITX_P1 (13)
DMI_RXP_2 AH52 → DMI_MRX_ITX_P2 (13)
DMI_RXP_3 AL45 → DMI_MRX_ITX_P3 (13)
DMI_TXN_0 AG49 → DMI_MTX_IRX_N0 (13)
DMI_TXN_1 AJ49 → DMI_MTX_IRX_N1 (13)
DMI_TXN_2 AJ47 → DMI_MTX_IRX_N2 (13)
DMI_TXN_3 AG47 → DMI_MTX_IRX_N3 (13)
DMI_TXP_0 AF50 → DMI_MTX_IRX_P0 (13)
DMI_TXP_1 AH50 → DMI_MTX_IRX_P1 (13)
DMI_TXP_2 AJ45 → DMI_MTX_IRX_P2 (13)
DMI_TXP_3 AG45 → DMI_MTX_IRX_P3 (13)

(3) MCH_BSEL0 → K26 CFG_0
(3) MCH_BSEL1 → G23 CFG_1
(3) MCH_BSEL2 → G25 CFG_2
J25 CFG_3
L25 CFG_4
T10 MCH_CFG5 → L27 CFG_5
T17 MCH_CFG7 → F24 CFG_6
D24 CFG_7
D26 CFG_8
J23 CFG_9
B26 CFG_10
A23 CFG_11
T16 MCH_CFG12 → C23 CFG_12
T15 MCH_CFG13 → B24 CFG_13
B22 CFG_14
T14 MCH_CFG16 → K24 CFG_15
C25 CFG_16
L23 CFG_17
L33 CFG_18
T8 MCH_CFG19 → K32 CFG_19
T9 MCH_CFG20 → K34 CFG_20

GRAPHICS VID

GFX_VID_0 G33 → GPU_VID0 (29)
GFX_VID_1 G37 → GPU_VID1 (29)
GFX_VID_2 F38 → GPU_VID2 (29)
GFX_VID_3 F36 → GPU_VID3 (29)
GFX_VID_4 G35 → GPU_VID4 (29)
GFX_VR_EN G39 → GFX_VR_EN (29)

PM

(14) PM_SYNC# → J35 PM_SYNC#
(4,12,25) H_DPRSTP# → F6 PM_DPRSTP#
(16) PM_EXTTS#0 → PM_EXTTS#0 J39 PM_EXT_TS#_0
(16) PM_EXTTS#1 → PM_EXTTS#1 L39 PM_EXT_TS#_1
(4,14,25) DELAY_VR_PWRGOOD → AY39 PWROK
(13,18,19,21) PLTRST# → R136 100_4 RSTIN#_MCH BB18 RSTIN#
(4,12) PM_THRMTRIP# → R98 0_4 K28 THERMTRIP#
(14,25) DPRSLPVR → K36 DPRSLPVR

MISC

CL_CLK AK52 → CL_CLK0 (14)
CL_DATA AK54 → CL_DATA0 (14)
CL_PWROK AW40 → MPWROK (14,18)
CL_RST# AL53 → ICH_CL_RST0# (14)
CL_VREF AL55 MCH_CLVREF

DDPC_CTRLCLK F34 DDPC_CTRLCLK
DDPC_CTRLDATA F32 DDPC_CTRLDATA
SDVO_CTRLCLK B38 SDVO_CTRLCLK → SDVO_CTRLCLK (22)
SDVO_CTRLDATA A37 SDVO_CTRLDATA → SDVO_CTRLDATA (22)
CLKREQ# C31 CLKREQ#_MCH → CLKREQ#_MCH (3)
ICH_SYNC# K42 → MCH_ICH_SYNC# (14)
TSATN# D10 TSATN#

HDA

HDA_BCLK C29 HDA_BIT_CLK_HDMI → HDA_BIT_CLK_HDMI (12)
HDA_RST# B30 HDA_RST#_HDMI → HDA_RST#_HDMI (12)
HDA_SDI D28 HDA_SDIN_HDMI → HDA_SDIN_HDMI (12)
HDA_SDO A27 HDA_SDOUT_HDMI → HDA_SDOUT_HDMI (12)
HDA_SYNC B28 HDA_SYNC_HDMI → HDA_SYNC_HDMI (12)

NC

A7 NC_1
A49 NC_2
A52 NC_3
A54 NC_4
B54 NC_5
D55 NC_6
G55 NC_7
BE55 NC_8
BH55 NC_9
BK55 NC_10
BK54 NC_11
BL54 NC_12
BL52 NC_13
BL49 NC_14
BL7 NC_15
BL4 NC_16
BL2 NC_17
BK2 NC_18
BK1 NC_19
BH1 NC_20
BE1 NC_21
G1 NC_22

CANTIGASFF_1p0

U18C

(22) INT_LVDS_PWM → L_BKLT_CTRL D38
(22) INT_LVDS_BLON → L_BKLT_EN C37
L_CTRL_CLK K38
L_CTRL_DATA L37
(22) PHL_CLK → PHL_CLK J37
(22) PHL_DATA → PHL_DATA L35
L_DDC_CLK
L_DDC_DATA
(22) INT_LVDS_DIGON → LVDS_IBG B36
L_VDD_EN F50
LVDS_IBG K46
LVDS_VBG P44
LVDS_VREFH K46
LVDS_VREFL D46
(22) TXLCLKOUT- → TXLCLKOUT- LVDSA_CLK# B46
(22) TXLCLKOUT+ → TXLCLKOUT+ LVDSA_CLK D44
LVDSB_CLK# B44
LVDSB_CLK
(22) TXLOUT0- → TXLOUT0- LVDSA_DATA#_0 G45
(22) TXLOUT1- → TXLOUT1- LVDSA_DATA#_1 F46
(22) TXLOUT2- → TXLOUT2- LVDSA_DATA#_2 G41
LVDSA_DATA#_3 C45
(22) TXLOUT0+ → TXLOUT0+ LVDSA_DATA_0 F44
(22) TXLOUT1+ → TXLOUT1+ LVDSA_DATA_1 G47
(22) TXLOUT2+ → TXLOUT2+ LVDSA_DATA_2 F40
LVDSA_DATA_3 A45
LVDSB_DATA#_0 B40
LVDSB_DATA#_1 A41
LVDSB_DATA#_2 F42
LVDSB_DATA#_3 D48
LVDSB_DATA_0 D40
LVDSB_DATA_1 C41
LVDSB_DATA_2 G43
LVDSB_DATA_3 B48

INT_TV_COMP → J27 TVA_DAC
INT_TV_Y/G → E27 TVB_DAC
INT_TV_C/R → G27 TVC_DAC
F26 TVA_RTN
B34 TV_DCONSEL_0
D34 TV_DCONSEL_1

(21) CRT_B → CRT_BLUE J29
(21) CRT_G → CRT_GREEN G29
(21) CRT_R → CRT_RED F30
CRT_IRTN E29
(21) DDCCLK → CRT_DDC_CLK D36
(21) DDCDATA → CRT_DDC_DATA C35
(21) VGAHSYNC → R81 30.1/F_4 HSYNC → CRT_HSYNC J33
CRT_IREF → CRT_TVO_IREF D32
(21) VGAVSYNC → R80 30.1/F_4 VSYNC → CRT_VSYNC G31

CANTIGASFF_1p0

PCI-EXPRESS GRAPHICS

PEG_COMPI U45
PEG_COMPO T44
PEG_COMP1 → R104 49.9/F_4 → +1.05V

PEG_RX#_0 D52
PEG_RX#_1 G49
PEG_RX#_2 K54
PEG_RX#_3 H50
PEG_RX#_4 M52
PEG_RX#_5 N49
PEG_RX#_6 P54
PEG_RX#_7 V46
PEG_RX#_8 Y50
PEG_RX#_9 V52
PEG_RX#_10 W49
PEG_RX#_11 AB54
PEG_RX#_12 AD46
PEG_RX#_13 AC55
PEG_RX#_14 AE49
PEG_RX#_15 AF54
PEG_RX_0 E51
PEG_RX_1 F48
PEG_RX_2 J55
PEG_RX_3 J49 → HDMI_HP_IV# (22)
PEG_RX_4 M54
PEG_RX_5 M50
PEG_RX_6 P52
PEG_RX_7 U47
PEG_RX_8 AA49
PEG_RX_9 V54
PEG_RX_10 V50
PEG_RX_11 AB52
PEG_RX_12 AC47
PEG_RX_13 AC53
PEG_RX_14 AD50
PEG_RX_15 AF52

HDMI Port B

PEG_TX#_0 L47 PEG_TXN0 C73 0.1u/10V_4 HDMITX2N (22)
PEG_TX#_1 F52 PEG_TXN1 C74 0.1u/10V_4 HDMITX1N (22)
PEG_TX#_2 P46 PEG_TXN2 C71 0.1u/10V_4 HDMITX0N (22)
PEG_TX#_3 H54 PEG_TXN3 C92 0.1u/10V_4 HDMICLKN (22)
PEG_TX#_4 L55
PEG_TX#_5 T46
PEG_TX#_6 R53
PEG_TX#_7 U49
PEG_TX#_8 T54
PEG_TX#_9 Y46
PEG_TX#_10 AB46
PEG_TX#_11 W55
PEG_TX#_12 Y54
PEG_TX#_13 AC49
PEG_TX#_14 AF46
PEG_TX#_15 AD54

PEG_TX_0 J47 PEG_TXP0 C72 0.1u/10V_4 HDMITX2P (22)
PEG_TX_1 F54 PEG_TXP1 C75 0.1u/10V_4 HDMITX1P (22)
PEG_TX_2 N47 PEG_TXP2 C70 0.1u/10V_4 HDMITX0P (22)
PEG_TX_3 H52 PEG_TXP3 C99 0.1u/10V_4 HDMICLKP (22)
PEG_TX_4 L53
PEG_TX_5 R47
PEG_TX_6 R55
PEG_TX_7 T50
PEG_TX_8 T52
PEG_TX_9 W47
PEG_TX_10 AA47
PEG_TX_11 W55
PEG_TX_12 Y52
PEG_TX_13 AB50
PEG_TX_14 AE47
PEG_TX_15 AD52

Layout notice: Place the resistor within 500 mils (1.27 mm) of the (G)MCH.

CRT setting

R84:
~~if the total motherboard route length is less than 12",~~
the recommended reference resistor value is 1 K Ω ±1%
For longer route lengths between 12" - 15.3",
the recommended reference resistor value is 976 Ω ±1%

R93 1.02K/F_4 CRT_IREF

R82 150/F_4 CRT_B
R78 150/F_4 CRT_G
R79 150/F_4 CRT_R

R102 75/F_4 INT_TV_COMP
R291 75/F_4 INT_TV_Y/G
R292 75/F_4 INT_TV_C/R

LVDS setting

+3V
R95 10K_4 L_CTRL_CLK
R94 10K_4 L_CTRL_DATA
R300 2.2K_4 PHL_DATA
R301 2.2K_4 PHL_CLK
R290 2.4K_4 LVDS_IBG

DDR3 PWROK

+3V_S5
(18,26,28) SUSON
(18,26) HWPG_+1.5V_SUS
U21 TC7SH08FU
R347 12.1K/F_4
SM_PWROK
R348 10K_4
At 11/19 change U21 power supply from +3VSUS to +3V_S5

DDR3 VREF

(20mils)
+SMDDR_VREF_NB
R113 BLM18BA750SN1D_6
+SMDDR_VREF
+1.5V_SUS
R350 *10K/F_4
R349 *10K/F_4
+SMDDR_VREF_NB:Default use voltage divider for poor layout cause +SMDDR_VREF not meet spec.And Intel circuit PU/PD is 1K,But Check list PU/PD is 10K.

Check list note : CL_REF=0.35V
+1.05V
(15mils)
MCH_CLVREF
R112 1K/F_4
C170 0.1u/10V_4
R111 511/F_6

<Checklist ver0.8>
If TSATN# is not used, then it must be terminated with a 56-Ω pull-up resistor to VCCP.
+1.05V
TSATN# R296 56_4
+3V
PM_EXTTS#0 R100 10K_4
PM_EXTTS#1 R97 10K_4
SM_REXT R271 499/F_4

DDR3 RCOMP

+1.5V_SUS
SMRCOMPP R270 80.6/F_4
SMRCOMPN R272 80.6/F_4

DDR3 RCOMP_VOH/VOL

+1.5V_SUS
R264 1K/F_4
SM_RCOMP_VOH
R269 3.01K/F_4
C423 0.01u/25V_4
C421 2.2u/6.3V_6
SM_RCOMP_VOL
R266 1K/F_4
C422 0.01u/25V_4
C418 2.2u/6.3V_6

+3V
DDPC_CTRLCLK R294 2.2K_4
DDPC_CTRLDATA R295 2.2K_4
SDVO_CTRLCLK R297 4.7K_4
SDVO_CTRLDATA R299 4.7K_4
CLKREQ#_MCH R293 10K_4
(7/7) intel check list 360543 rev 2.0 CLKREQ# need to 10K pull high to 3.3V

Quanta Computer Inc.
PROJECT : ZE8

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	Cantiga SFF (DMI/VGA)	1A
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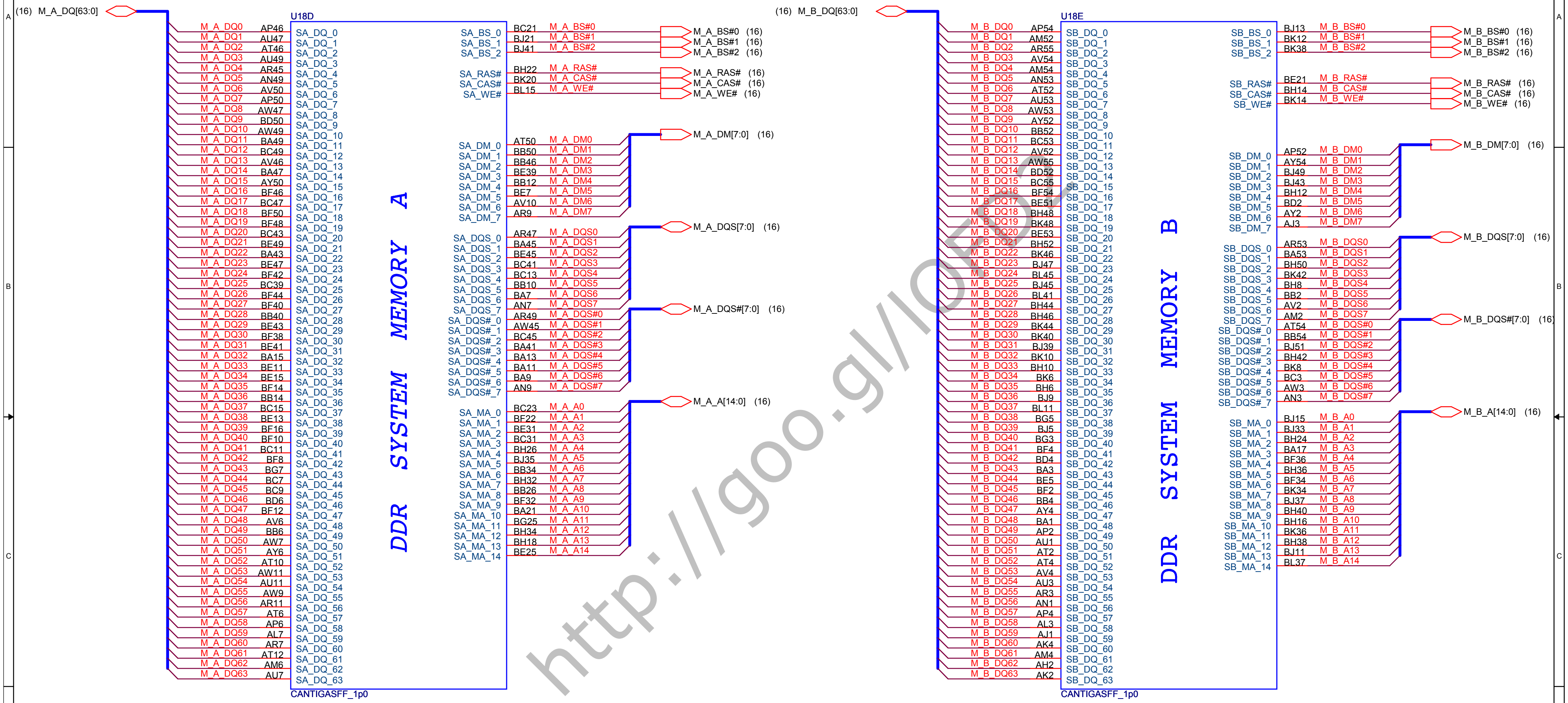
Cantiga SFF - DDRII (CLG)



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M_A_DQ6 AV50 SA_DQ_6
M_A_DQ7 AP50 SA_DQ_7
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M_A_DQ55 AW9 SA_DQ_55
M_A_DQ56 AR11 SA_DQ_56
M_A_DQ57 AT6 SA_DQ_57
M_A_DQ58 AP6 SA_DQ_58
M_A_DQ59 AL7 SA_DQ_59
M_A_DQ60 AR7 SA_DQ_60
M_A_DQ61 AT12 SA_DQ_61
M_A_DQ62 AM6 SA_DQ_62
M_A_DQ63 AU7 SA_DQ_63
DDR SYSTEM MEMORY A
SA_BS_0 BC21 M_A_BS#0
SA_BS_1 BJ21 M_A_BS#1
SA_BS_2 BJ41 M_A_BS#2
SA_RAS# BH22 M_A_RAS#
SA_CAS# BK20 M_A_CAS#
SA_WE# BL15 M_A_WE#
M_A_BS#0 (16)
M_A_BS#1 (16)
M_A_BS#2 (16)
M_A_RAS# (16)
M_A_CAS# (16)
M_A_WE# (16)
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SA_DM_1 BB50 M_A_DM1
SA_DM_2 BB46 M_A_DM2
SA_DM_3 BE39 M_A_DM3
SA_DM_4 BB12 M_A_DM4
SA_DM_5 BE7 M_A_DM5
SA_DM_6 AV10 M_A_DM6
SA_DM_7 AR9 M_A_DM7
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SA_DQS_0 AR47 M_A_DQS0
SA_DQS_1 BA45 M_A_DQS1
SA_DQS_2 BE45 M_A_DQS2
SA_DQS_3 BC41 M_A_DQS3
SA_DQS_4 BC13 M_A_DQS4
SA_DQS_5 BB10 M_A_DQS5
SA_DQS_6 BA7 M_A_DQS6
SA_DQS_7 AN7 M_A_DQS7
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SA_DQS#_3 BA41 M_A_DQS#3
SA_DQS#_4 BA13 M_A_DQS#4
SA_DQS#_5 BA11 M_A_DQS#5
SA_DQS#_6 BA9 M_A_DQS#6
SA_DQS#_7 AN9 M_A_DQS#7
M_A_DQS#[7:0] (16)
SA_MA_0 BC23 M_A_A0
SA_MA_1 BF22 M_A_A1
SA_MA_2 BE31 M_A_A2
SA_MA_3 BC31 M_A_A3
SA_MA_4 BH26 M_A_A4
SA_MA_5 BJ35 M_A_A5
SA_MA_6 BB34 M_A_A6
SA_MA_7 BH32 M_A_A7
SA_MA_8 BB26 M_A_A8
SA_MA_9 BF32 M_A_A9
SA_MA_10 BA21 M_A_A10
SA_MA_11 BG25 M_A_A11
SA_MA_12 BH34 M_A_A12
SA_MA_13 BH18 M_A_A13
SA_MA_14 BE25 M_A_A14
M_A_A[14:0] (16)
CANTIGASFF_1p0
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M_B_DQ60 AK4 SB_DQ_60
M_B_DQ61 AM4 SB_DQ_61
M_B_DQ62 AH2 SB_DQ_62
M_B_DQ63 AK2 SB_DQ_63
DDR SYSTEM MEMORY B
SB_BS_0 BJ13 M_B_BS#0
SB_BS_1 BK12 M_B_BS#1
SB_BS_2 BK38 M_B_BS#2
SB_RAS# BE21 M_B_RAS#
SB_CAS# BH14 M_B_CAS#
SB_WE# BK14 M_B_WE#
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M_B_BS#1 (16)
M_B_BS#2 (16)
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SB_DM_6 AY2 M_B_DM6
SB_DM_7 AJ3 M_B_DM7
M_B_DM[7:0] (16)
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SB_DQS_2 BH50 M_B_DQS2
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SB_DQS_4 BH8 M_B_DQS4
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SB_DQS#_2 BJ51 M_B_DQS#2
SB_DQS#_3 BH42 M_B_DQS#3
SB_DQS#_4 BK8 M_B_DQS#4
SB_DQS#_5 BC3 M_B_DQS#5
SB_DQS#_6 AW3 M_B_DQS#6
SB_DQS#_7 AN3 M_B_DQS#7
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SB_MA_1 BJ33 M_B_A1
SB_MA_2 BH24 M_B_A2
SB_MA_3 BA17 M_B_A3
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SB_MA_5 BH36 M_B_A5
SB_MA_6 BF34 M_B_A6
SB_MA_7 BK34 M_B_A7
SB_MA_8 BJ37 M_B_A8
SB_MA_9 BH40 M_B_A9
SB_MA_10 BH16 M_B_A10
SB_MA_11 BK36 M_B_A11
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SB_MA_13 BJ11 M_B_A13
SB_MA_14 BL37 M_B_A14
M_B_A[14:0] (16)
CANTIGASFF_1p0

Quanta Computer Inc.

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Cantiga SFF - VCC/NCTF (CLG)

Ivcc internal VGA 2.4A
(Shape or 140mils)

VCC_SM(+1.5V_SUS)
DDR3(800M) : 3162.5mA
DDR3(1067M) : 4140mA

UMA 9.6A(GM45)
(Plane or shape)

VCC 2200mA

VCC_SM :3000mA

VCC_AXG 7700mA

U18F

U18G

CANTIGASFF_1p0

Celeron 723,743 not support graphics render standby mode,
so add R64 , R65, del GFX power (Page 29)
SU type cpu support it, so del R64, R65 and add GFX power (Page 29)

9/28: add R183 for voltage low issue

Layout Note:
Inside GMCH cavity.

Close to GMCH
Layout Note:
370 mils from edge.

Differential routing
(29) GFX_VCCSENSE
(29) GFX_VSSSENSE

1. Route VCC_AXG_SENSE and VSS_AXG_SENSE differentially
2. VCC_AXG_SENSE PU to +VGFX_CORE_INT with 10ohm
and VSS_AXG_SENSE PD with 10ohm for Intel suggest

Quanta Computer Inc.		
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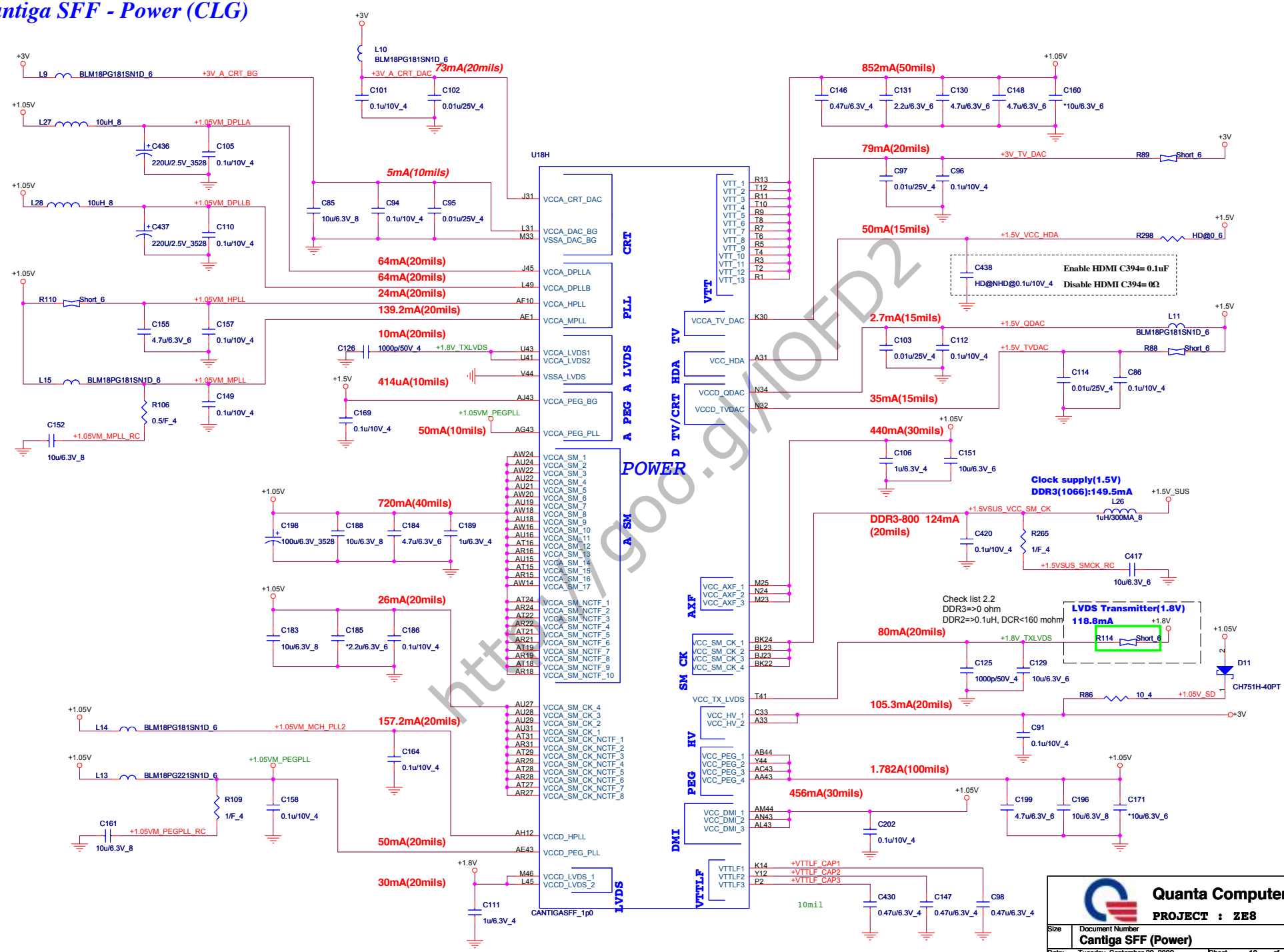
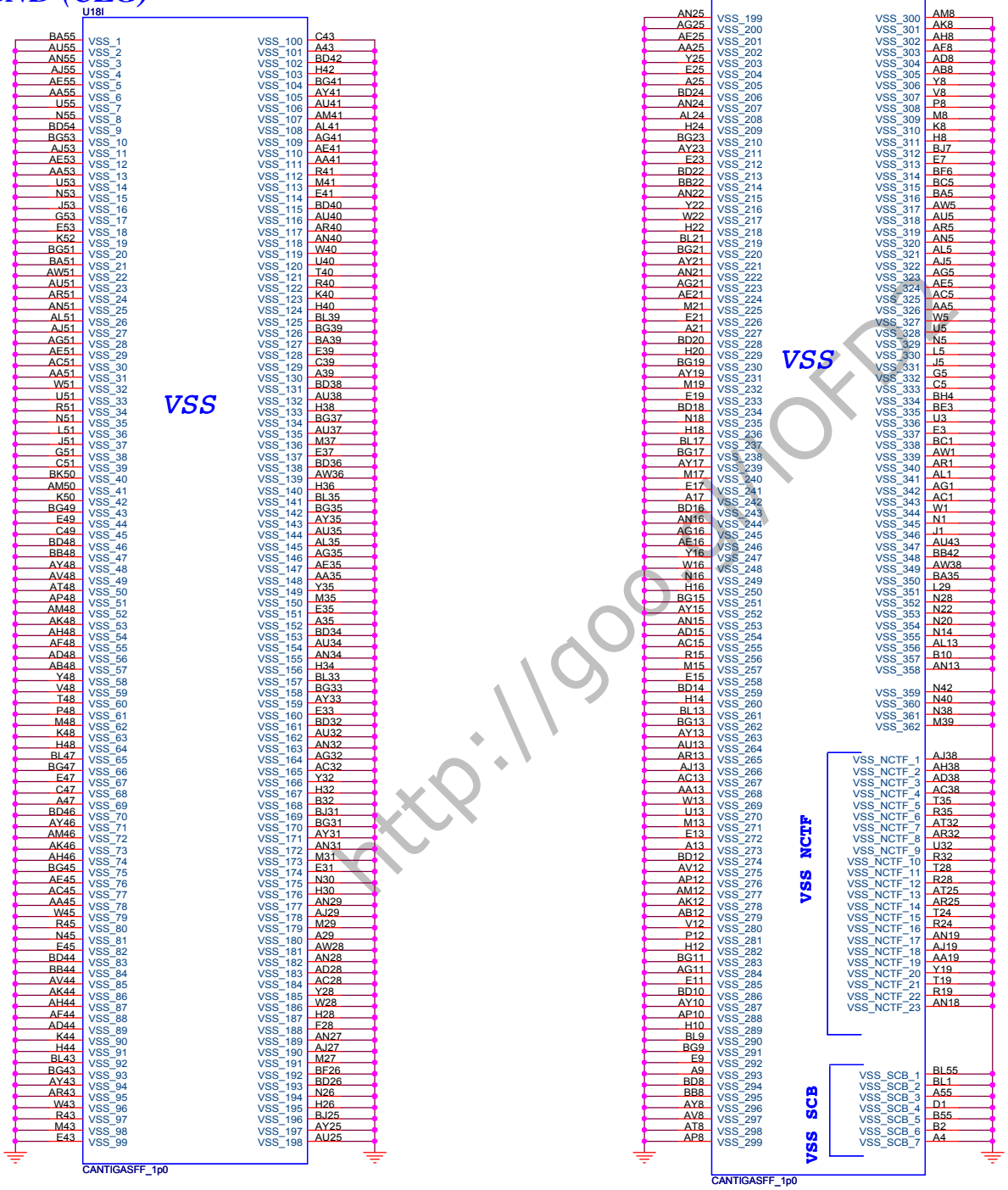
Cantiga SFF - Power (CLG)



Cantiga SFF - GND (CLG)



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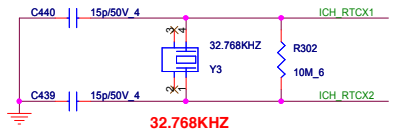
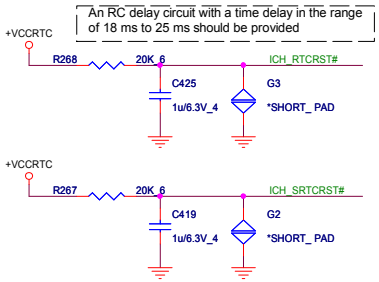
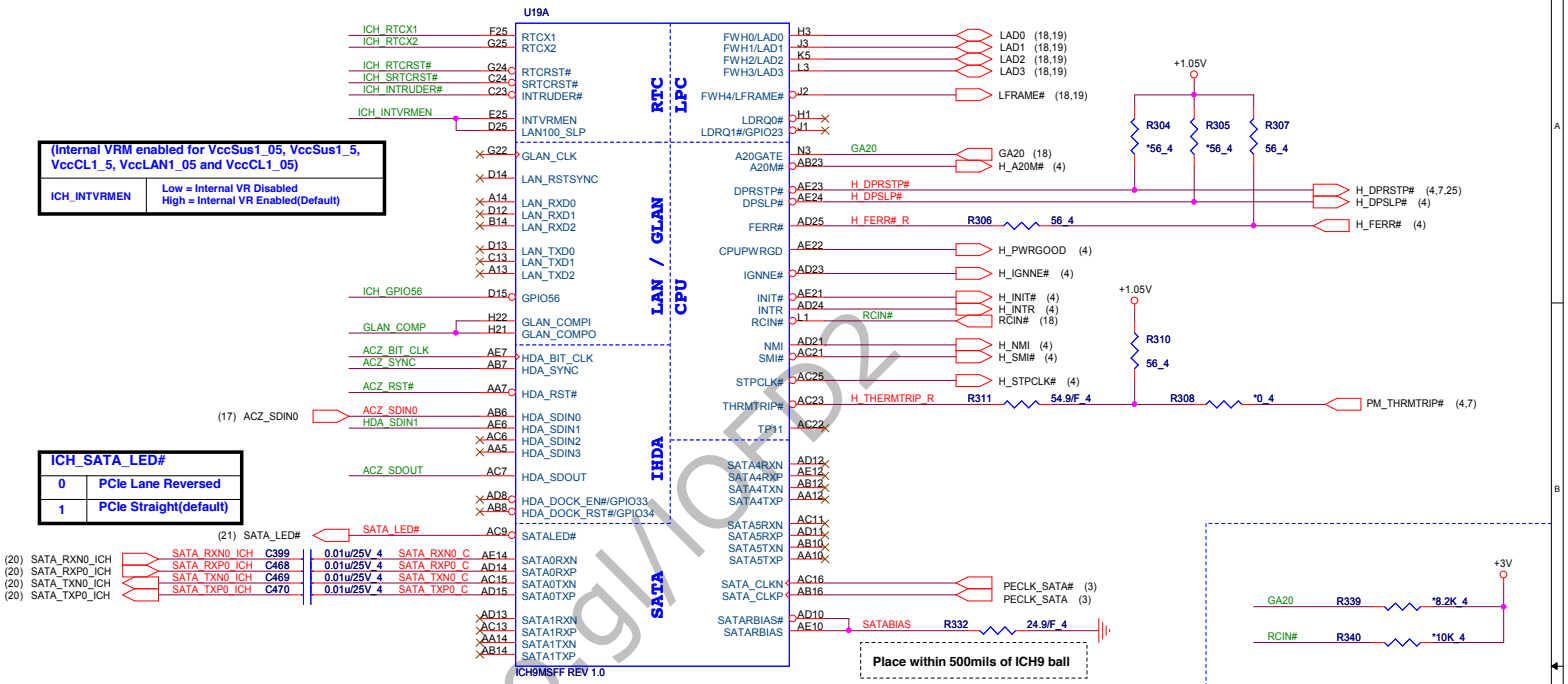
RTC CRYSTAL



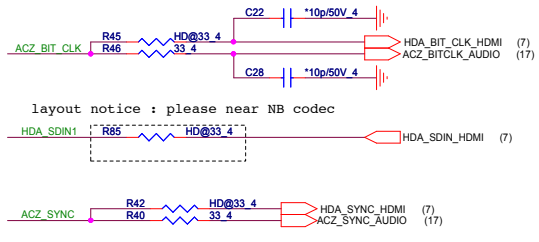
RESET JUMP

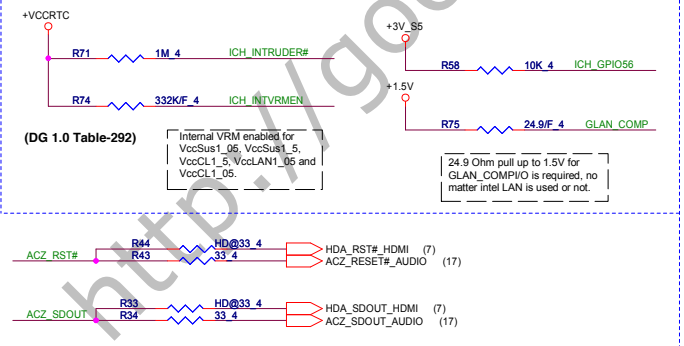


ICH9M SFF - Host,SATA,HDA (CLG)

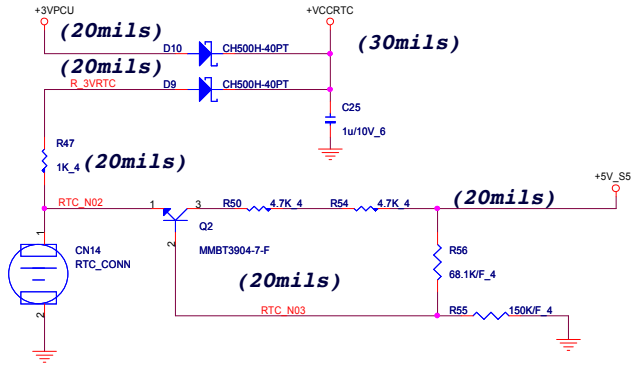


HD Audio Interface





RTC BATTERY (RTC)



South Bridge Strap Pin (1/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect	This strap should only be enabled in manufacturing environments using an external pull-up resistor.
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU	
	XOR Chain Entrance	PWROK	ICH_TP3 / HDA_SDOUT: 0/0 RSVD; 0/1 Enter XOR Chain; 1/0 Normal opration(Default); 1/1 Set PCIE port config bit 1	(14) ICH_TP3 — ICH_TP3 — R316 — *1K_4
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK		HDA_IO_ICH — R37 *1K_4 ACZ_SDOUT; R36 *1K_4 ACZ_SYNC; intel design guide: pull high 3.3k

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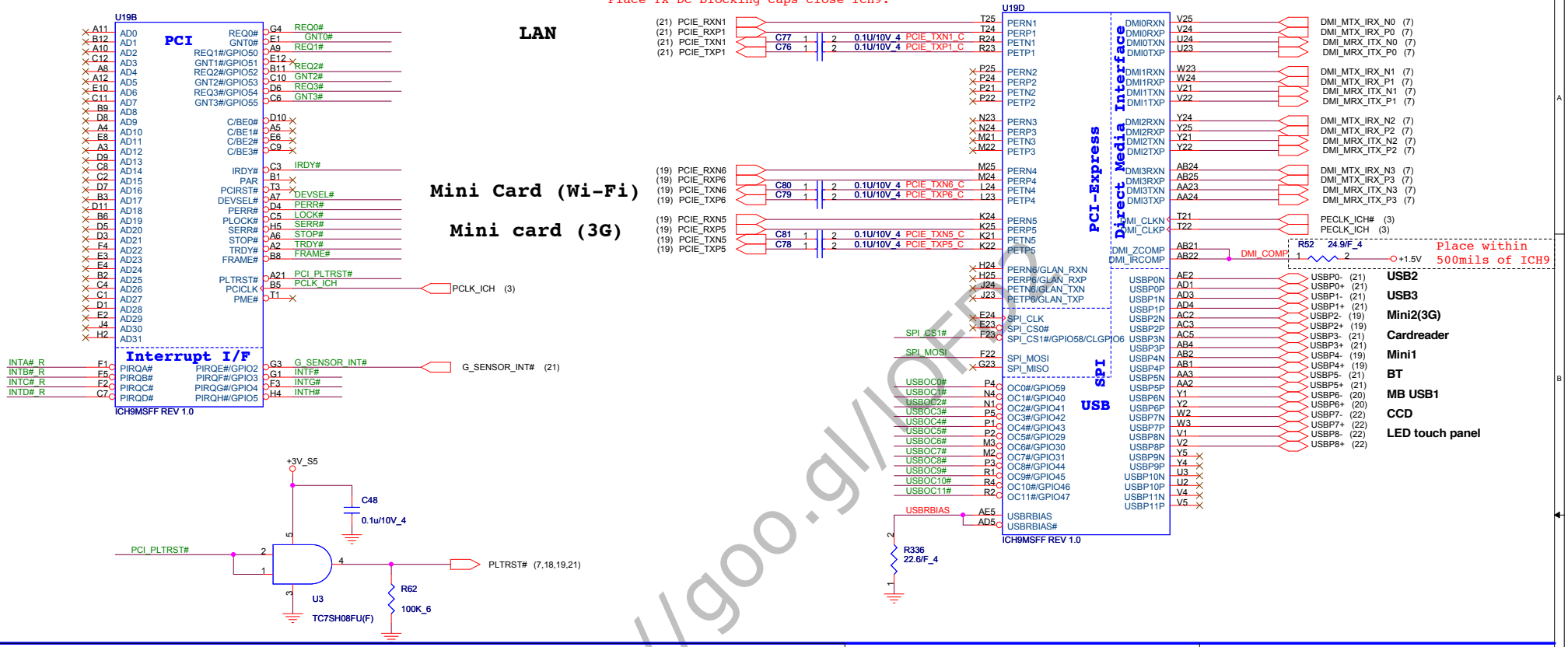
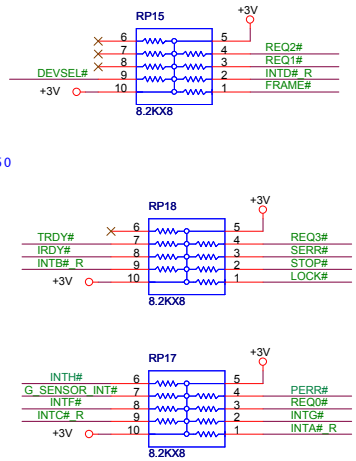
ICH9M SFF - USB/PCIE/DMI (CLG)



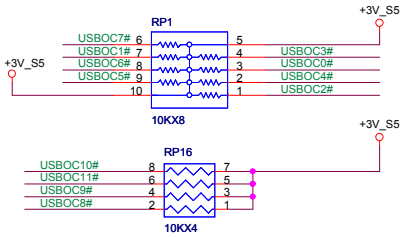
South Bridge Strap Pin (2/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0	
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default	GNT2# — T20
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default	8/28 : add pull high resister R160 in GNT3# pin for no video issue.
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default	T3 — GNT3# — R160 10K_4 — +3V
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable	SPI_MOSI — T18
GNT0#	Boot BIOS Selection 0	PWROK	PCI_GNT#0 / SPI_CS#1 / Boot Location 0 / 1 / SPI(Default) 1 / 0 / PCI	GNT0# — T21
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK		SPI_CS1# — T19

PCI PULL-UP



USBOC# PULL-UP



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	ICH9M SFF (USB/PCIE/DMI)	1A

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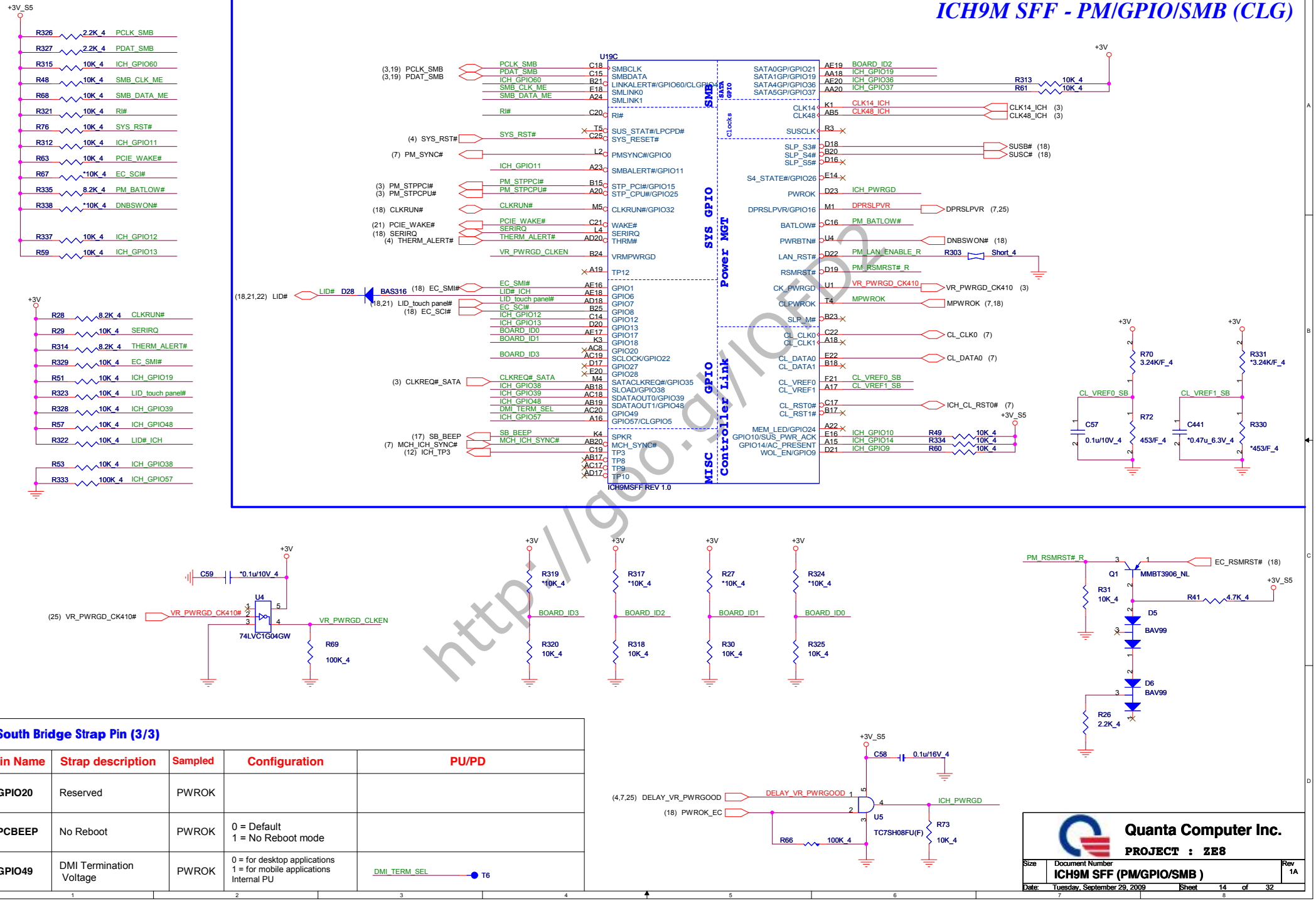
ICH9M SFF - PM/GPIO/SMB (CLG)



South Bridge Strap Pin (3/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
PCBEEP	No Reboot	PWROK	0 = Default 1 = No Reboot mode	
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	DMI_TERM_SEL — T6

Quanta Computer Inc.

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	ICH9M SFF (PM/GPIO/SMB)	1A

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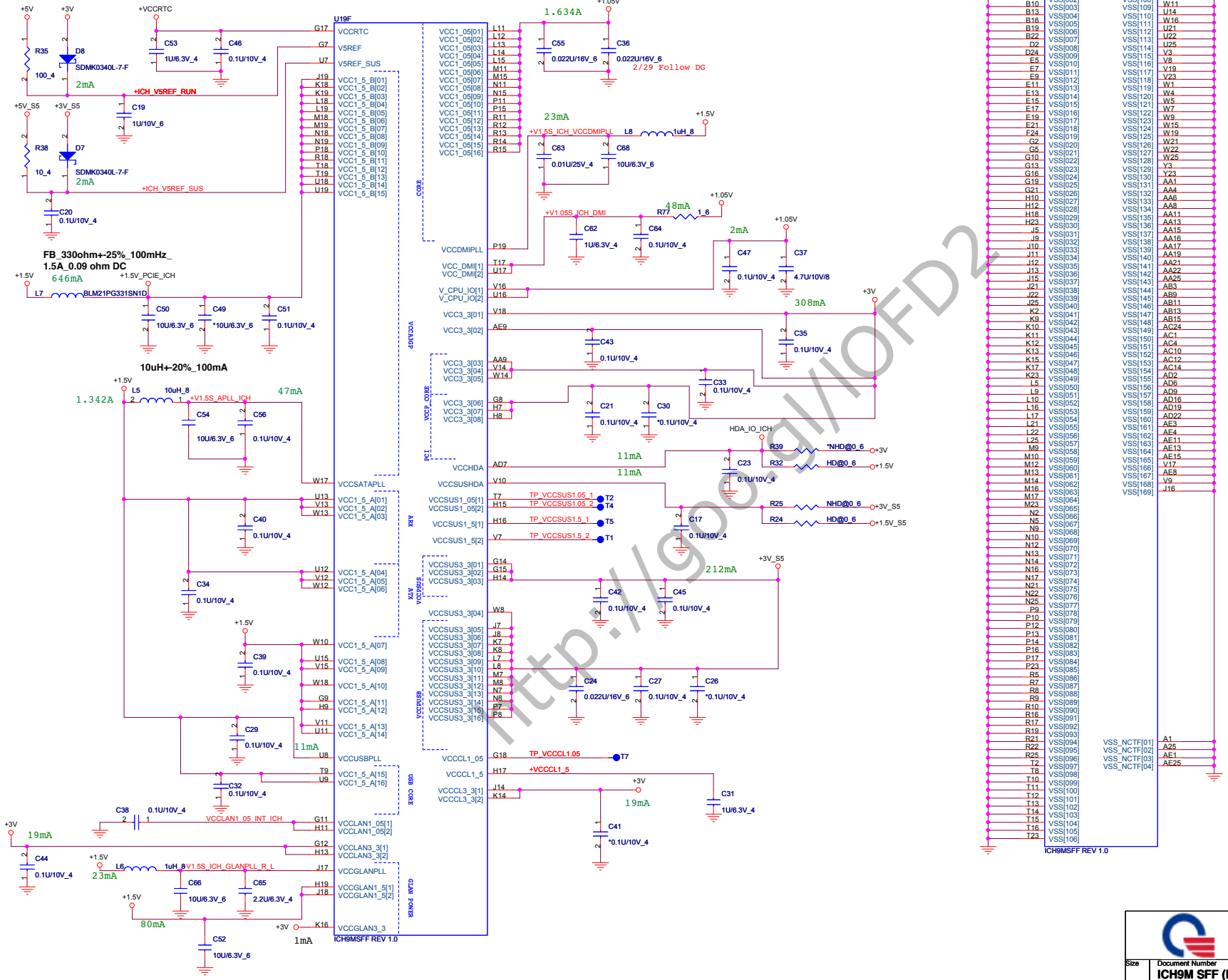
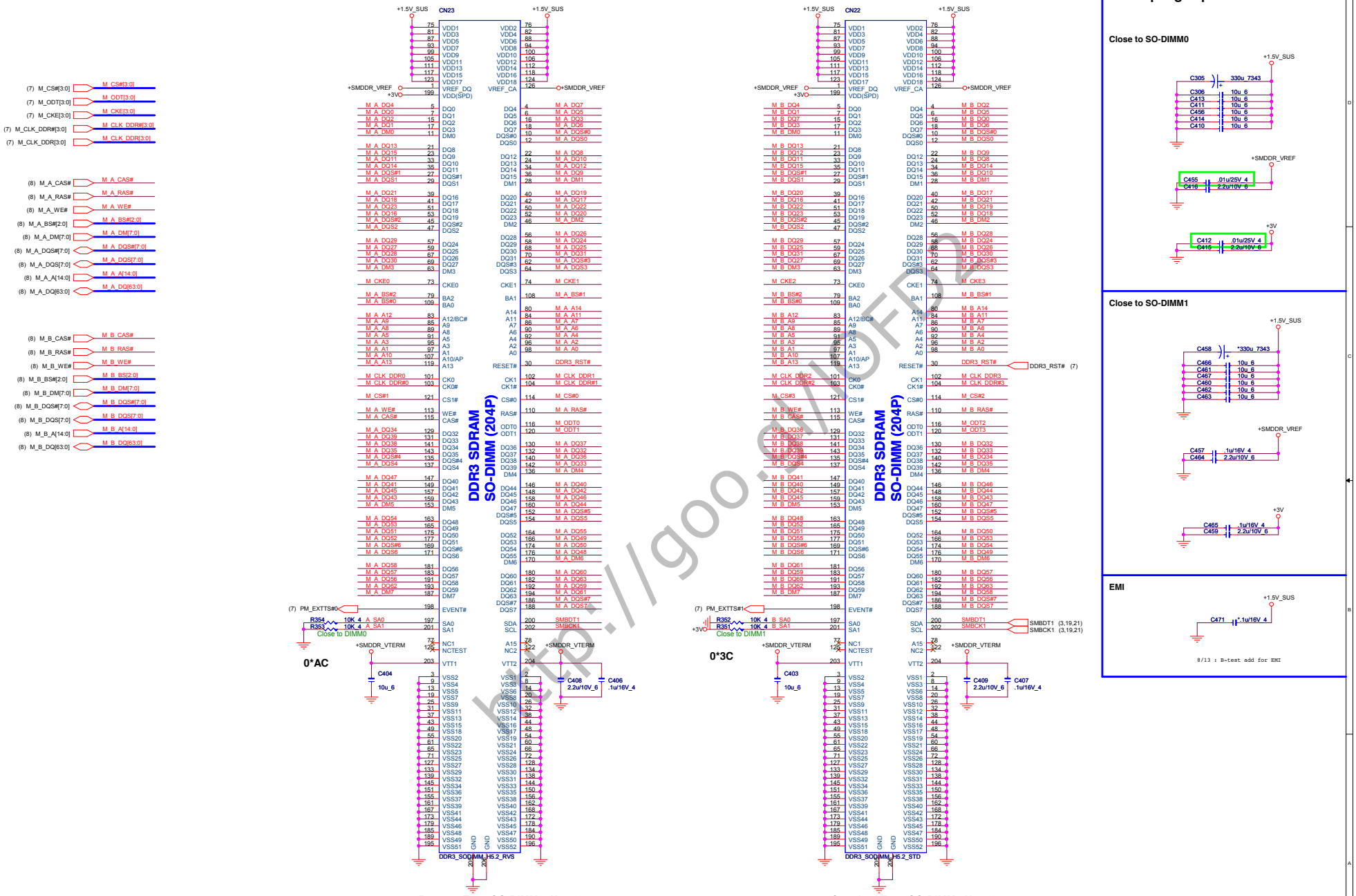
ICH9M SFF - Power/GND (CLG)





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	DDRIII SO-DIMM	1A

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Codec ALC269X (ADO)

B-test 8/11: for EMI

SPDIF_OUT — C243 *680p/50V_6; +5VA — C363 0.1U/10V_4

HPOUT-R → HPOUT-R (21)
HPOUT-L → HPOUT-L (21)
MIC1-VREFO-R
MIC1-VREFO-L
Place next to pin 27

ADOGND
C358 2.2U/6.3V_6
C352 2.2U/6.3V_6
C359 *10U/6.3V/6
C353 0.1U/10V/4
C348 0.1U/10V_4
C347 *10U/6.3V_6
Place next to pin 25

U11 (ALC269)

Spilt by DGND

+5VA
C350 10U/6.3V_6
C349 0.1U/10V_4
Place next to pin 38

(Vista Premium Version)

Placement near Audio Codec

DIGITAL
ANALOG
1.6Vrms

MIC1_R1
MIC1_L1
R226 20K/F_4 → ADOGND

SENSEA
R209 39.2K/F/4 → LINEOUT_JD# (21)
R221 20K/F/4 → MIC1_JD# (21)

(21) SPDIF_OUT → SPDIF_OUT

C342 0.1U/10V_4
C334 10U/6.3V_6
Place next to pin 39

C325 0.1U/10V_4
C327 10U/6.3V_6
Place next to pin 1

(22) DMIC_DAT
(22) DMIC_CLK

C332 0.1U/10V_4
C335 *10U/6.3V_6
Place next to pin 46

PCBEEP C324 1u/10V_6 BEEP_1 R198 47K_4 → SB_BEEP (14)
C316 100p/50V_6
R203 2K_4

SDIN3 ADZ

BOM notice: just can stuff one in BOM
R192 *NHD@0_6 → +3V
R189 HD@0_6 → +1.5V

+AZA_VDD
C315 0.1U/10V/4
C323 10U/6.3V/_6
Place next to pin 9

ACZ_RESET#_AUDIO → ACZ_RESET#_AUDIO (12)
ACZ_SYNC_AUDIO (12)
ACZ_SDIN0 (12)
ACZ_SDOUT_AUDIO (12)
ACZ_BITCLK_AUDIO (12)

R196 22_4
C322 10P/50V_4
R195 Short_4
C321 *10P/50V_4

PD#
0V : Power down Class D SPK amplifer
3.3V : Power up Class D SPK amplifer

Speaker (AMP)

R_SPK+ R242 Short_6 R_SPK+_1
C357 *0.22U/25V/6
C365 *1u/6.3V_4
C356 *0.22U/25V/6
R_SPK- R241 Short_6 R_SPK-_1
L_SPK- R240 Short_6 L_SPK-_1
CN8 Speak CNN
C355 *0.22U/25V/6
C364 *1u/6.3V_4
C354 *0.22U/25V/6
L_SPK+ R239 Short_6 L_SPK+_1

MIC1-VREFO-R
MIC1-VREFO-L
R238 4.7K/F_4
R237 4.7K/F_4
MIC1_L1 C338 4.7U/6.3V/6 R234 1K/F_4 → MIC1_L2 (21)
MIC1_R1 C341 4.7U/6.3V/6 R233 1K/F_4 → MIC1_R2 (21)

stitching caps for Audio signals
C345 +3VPCU → +3V 0.1U/10V_4
C385 +3VPCU → +3V 0.1U/10V_4

R259 Short_6
R248 *0_6
R250 *0_6
R243 *0_6
R254 Short_6
C377 *1000p/50V_4
C387 *1000p/50V_4
R247 *0_6
ADOGND

R202 *HD@100K_4
R188 *HD@100K_4
Q15 *HD@2N7002E
Q14 *HD@DTC144EU
ACZ_RESET#_AUDIO
PD#
*NHD@BAS316 D24 ACZ_RESET#_AUDIO
*BAS316 D25 EAPD#
*BAS316 D23 AMP_MUTE#
AMP_MUTE# (18)
R199 Short_4

Power (ADO)

Demodulation Filter

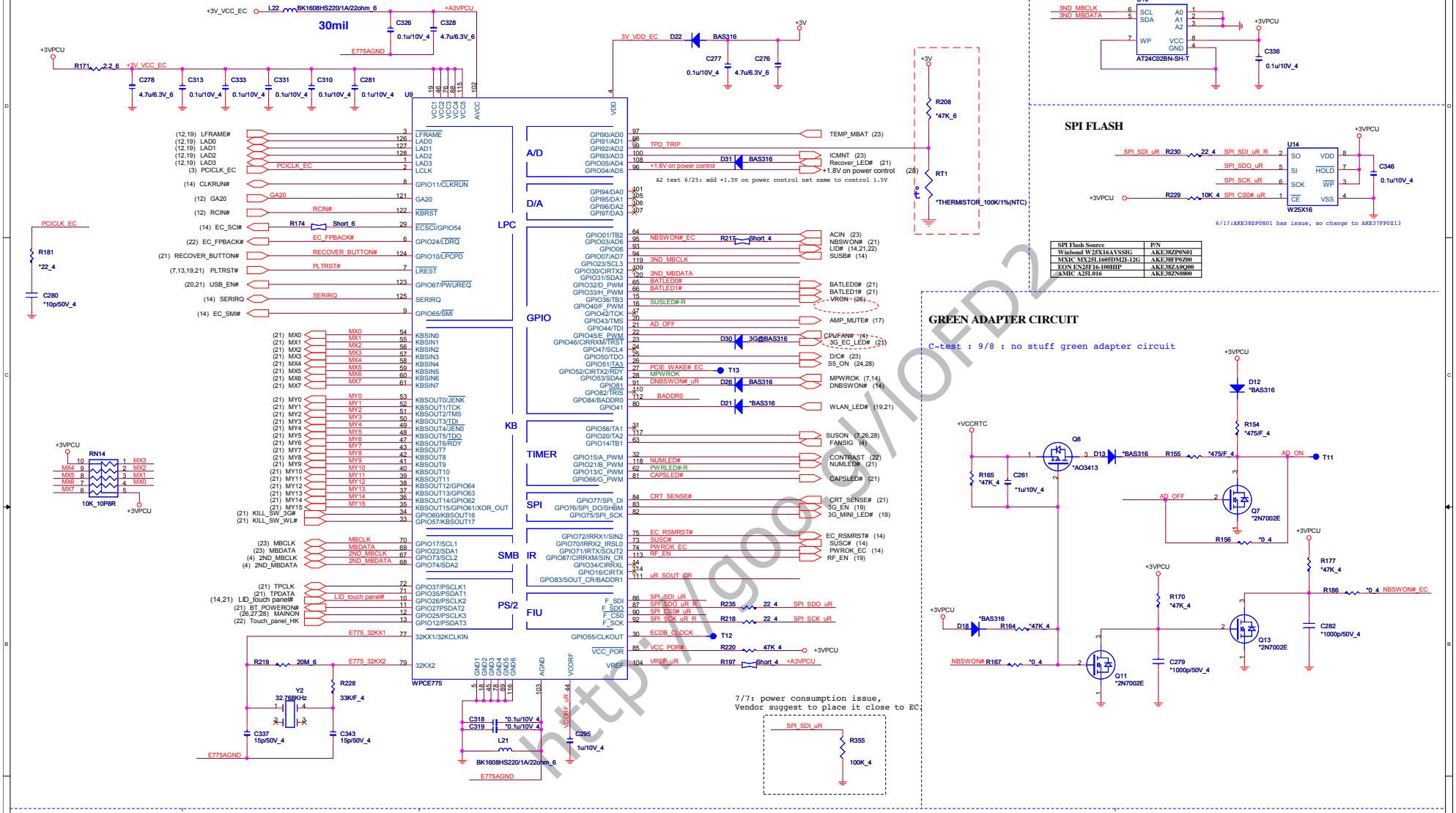
Place close to Codec

L25 TI201209U220/8
U15 *MAX8863SEUK+T (IN, GND, SHDN, OUT, SET)
C373 *0.1U/10V/4
R245 *29.4K/F/4
R246 *10K/F/4
C366 *10U/10V/3216

Quanta Computer Inc.
PROJECT : ZE8

Size	Document Number	Rev
	Codec ALC269X	1A
Date: Tuesday, September 29, 2009	Sheet 17 of 32	

EC WPCE775LA0DG (KBC)



ACER ID

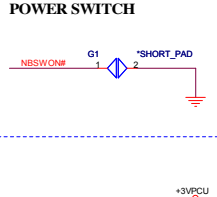
SPI FLASH

SPI Flash Source	P/N
Winbond W25X16AVSSIG	AKE38ZP0N01
MXIC MX25L1605DM2I-12G	AKE38FP0Z00
EON EN25F16-100HIP	AKE38ZA0Q00
AMIC A25L016	AKE38ZN0B00

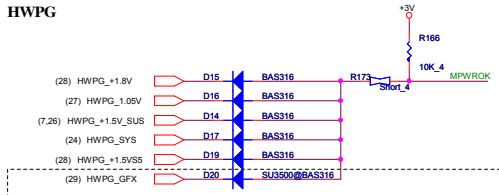
GREEN ADAPTER CIRCUIT

C-test : 9/8 : no stuff green adapter circuit

POWER SWITCH



HWPG

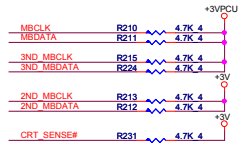


I/O ADDRESS SETTING

	I/O Address	
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

SM BUS PU



INTERNAL KEYBOARD STRIP SET

Quanta Computer Inc.
PROJECT : ZE8

Size	Document Number	Rev
	EC WPCE775LA0DG	1A

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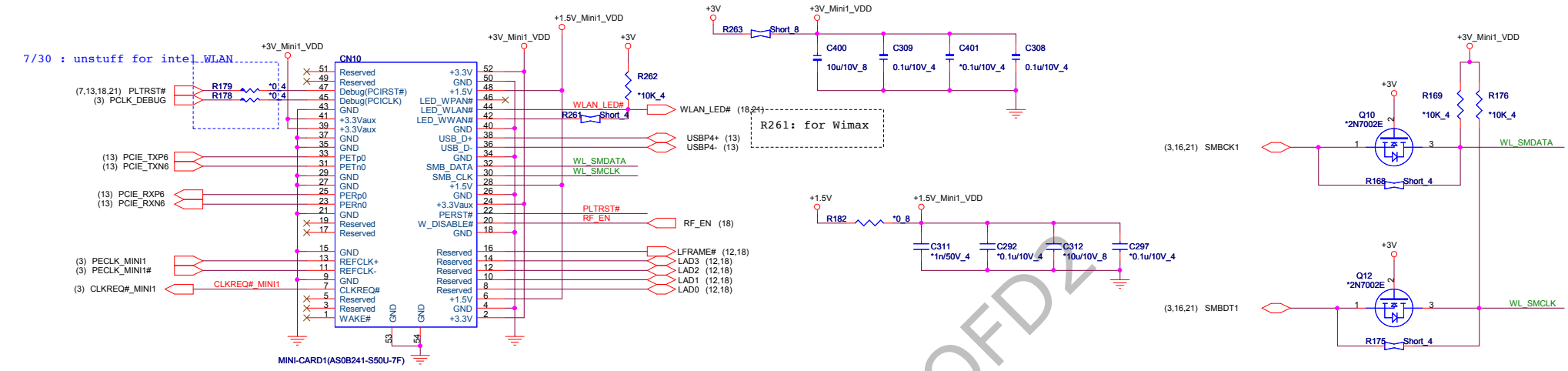
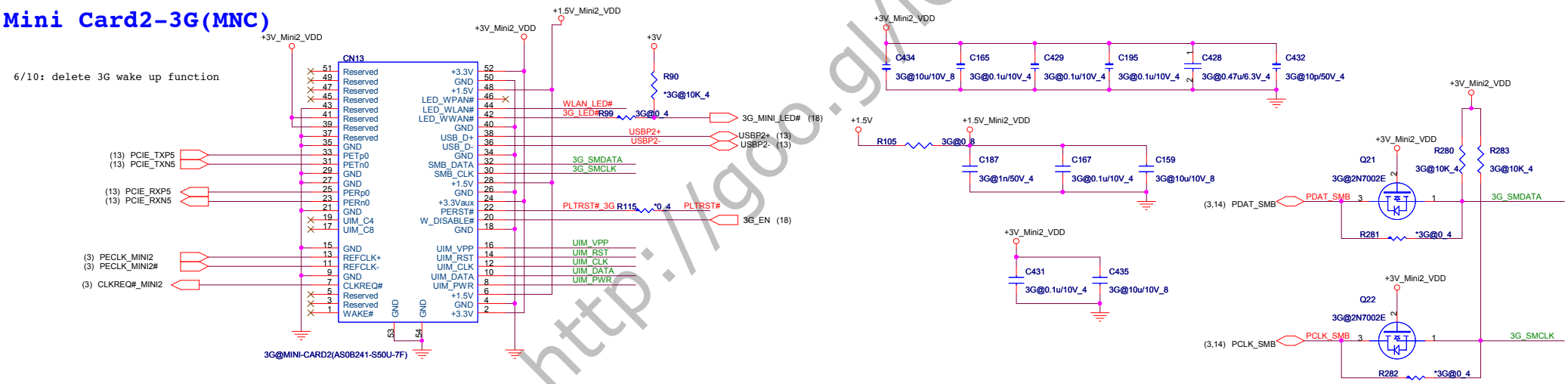
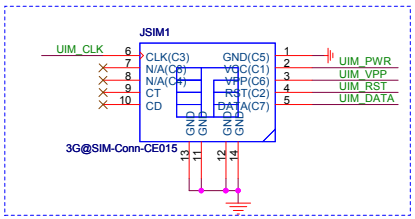
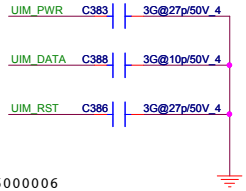
Mini Card1-WLAN/WMAX(MNC)

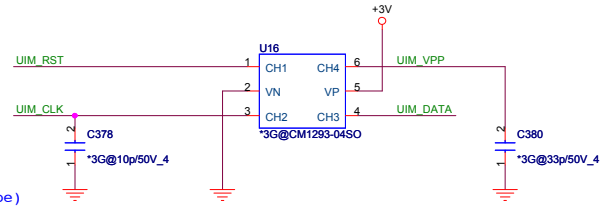


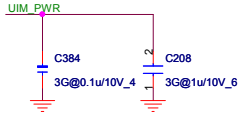
Mini Card2-3G(MNC)

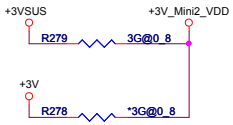












6/23 A2 test : change PN to DG006000005 or DG006000006

9/2 C test : change PN and footprint to DFHS10FR381(change back to A1 type)

Layout : C431 and C252 place near JSIM2

Quanta Computer Inc.		
PROJECT : ZE8		
Size	Document Number: MINI PCIE (WLAN/WMAX/3G)	Rev: 1A
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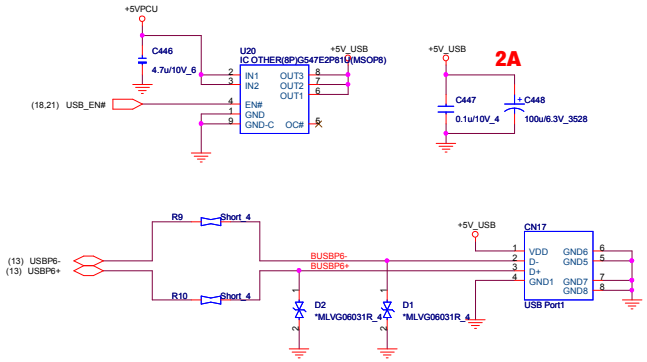
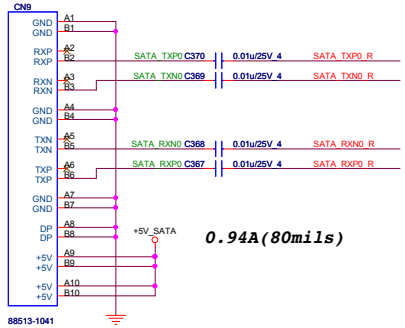
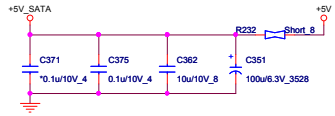
MB USB (USB)



2.5" SATA HDD(HDD)



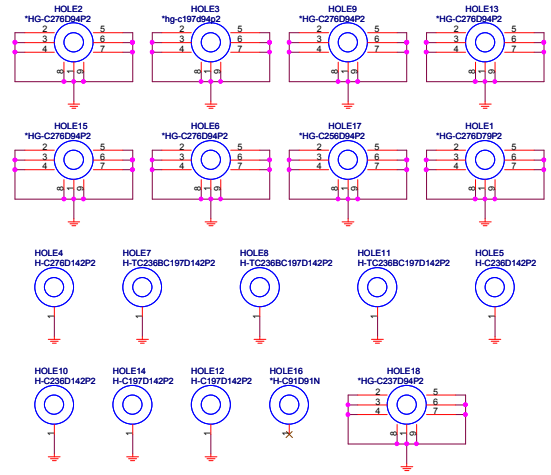
0.94A(80mils)



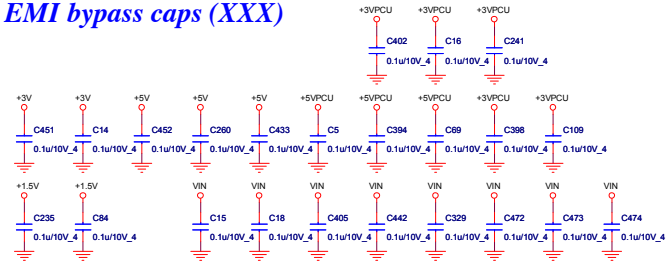
SATA ESD(EMC)

8/5 : because of the space is not enough, so, del SATA ESD U12 and C363.

HOLE (EXC)

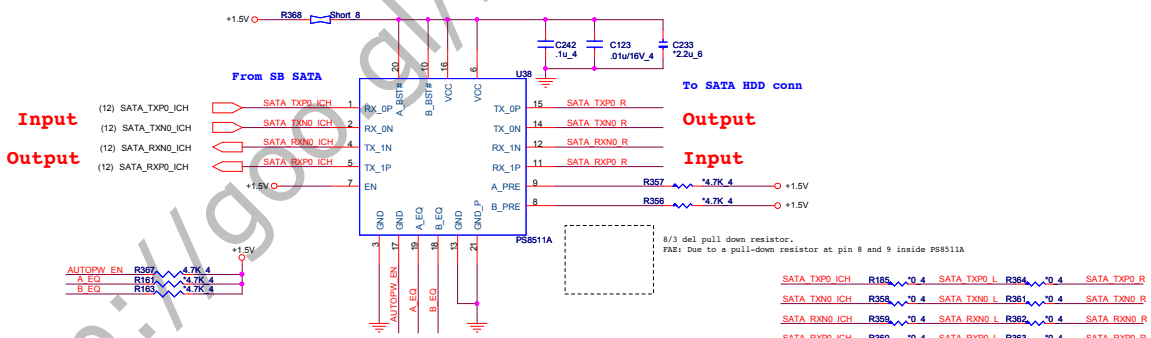


EMI bypass caps (XXX)



PAD

SATA RE-DRIVER IC(XXX)



8/3 del pull down resistor.
FAE: Due to a pull-down resistor at pin 8 and 9 inside PS8511A

SATA_TXP0_ICH	R185	*0_4	SATA_TXP0_L	R364 *0_4 SATA_TXP0_R
SATA_TXN0_ICH	R358	*0_4	SATA_TXN0_L	R361 *0_4 SATA_TXN0_R
SATA_RXN0_ICH	R359	*0_4	SATA_RXN0_L	R362 *0_4 SATA_RXN0_R
SATA_RXP0_ICH	R360	*0_4	SATA_RXP0_L	R363 *0_4 SATA_RXP0_R

PARADE : PS8511A

PIN 18,19	Input Equalization setting: Internal pull down ~150Kohm A_EQ/B_EQ = LOW: For short and medium length PCB traces (default) A_EQ/B_EQ = HIGH: For long length PCB traces
PIN 8,9	Output Pre-emphasis Setting: Internal pull down ~150Kohm A_PRE/B_PRE = LOW, Pre-emphasis disabled (default) A_PRE/B_PRE = HIGH, Pre-emphasis enabled
PIN 10,20	Output Level Boost setting: Internal pull up~150Kohm A_BST#/B_BST# = HIGH, SATAi/m output level 400~700mVpp A_BST#/B_BST# = LOW, SATAx output level 800~1200mVpp (default--SATA internal)
PIN 17	Automatic Power Saving Enable: Internal pull down~150Kohm AUTOPW_EN = HIGH, automatic power saving enable (default) AUTOPW_EN = LOW, automatic power saving disable

PARADE : PS8511A

EN	A_PRE	B_PRE	CH-0	CH-1
0	X	X	Standby	Standby
1	0	0	0dB	0dB
1	1	0	Pre-emphasis (3.5dB)	0dB
1	0	1	0dB	Pre-emphasis (3.5dB)
1	1	1	Pre-emphasis (3.5dB)	Pre-emphasis (3.5dB)

Quanta Computer Inc.
PROJECT : ZE8
Size | Document Number: USB/HDD/HOLE | Rev: 1A
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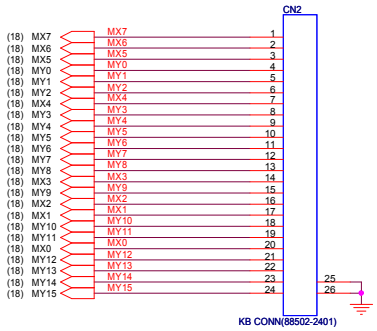
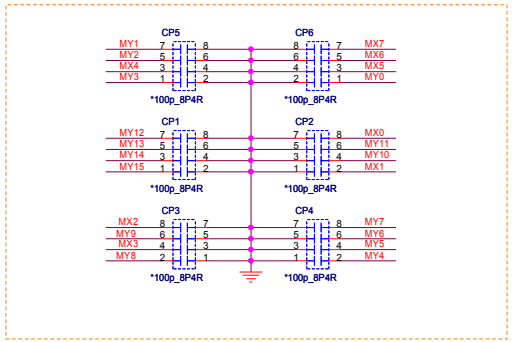
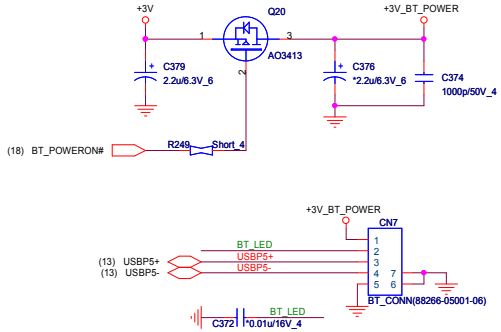
Keyboard(KBC)



For EMI Reserve Caps for debug

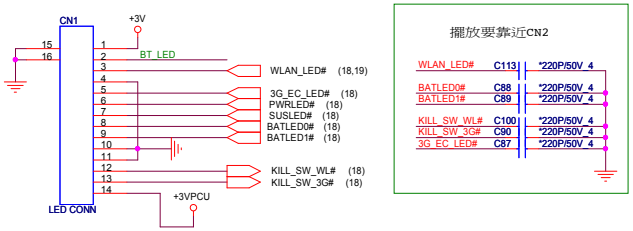


BuleTooth (BTM)

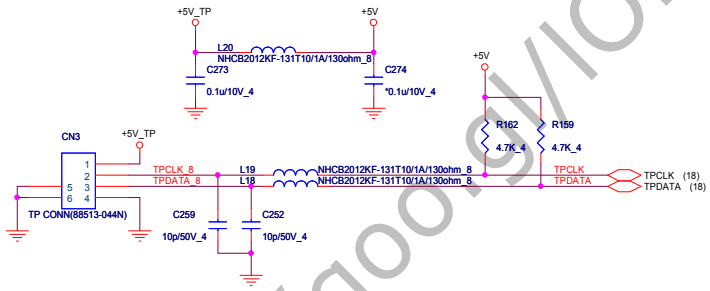


Be careful that bluetooth module PIN 2 is GND and PIN 5 is BT_LED.

LED D/B (UIF)



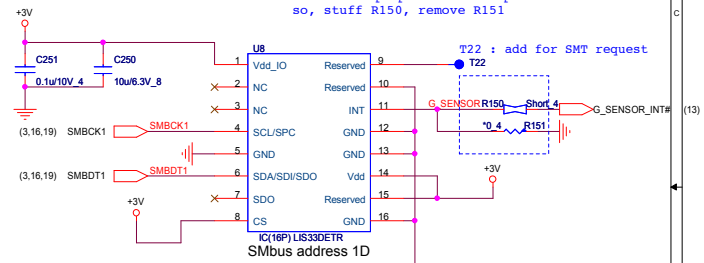
Touch Pad D/B (TPD)



G SENSOR(GSR)

A0 test : have free fall function, stuff R329, if not, stuff R327 just can stuff one of them

6/23 A2 test : per Acer request, use interrupt pin to detect panel status so, stuff R150, remove R151

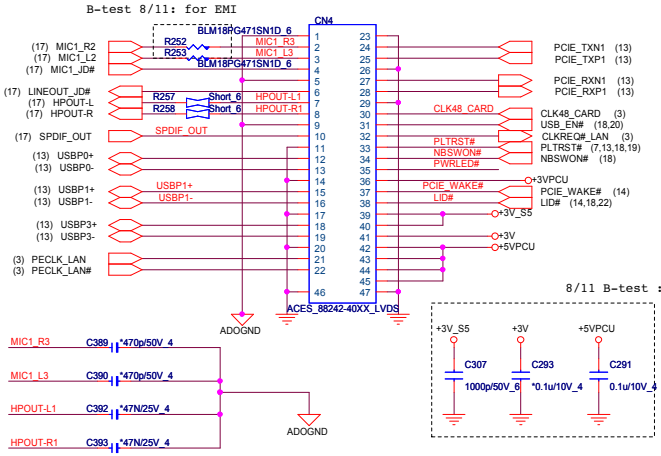


9/2 C-test : change footprint to sensor-3x3-5-16p-smt

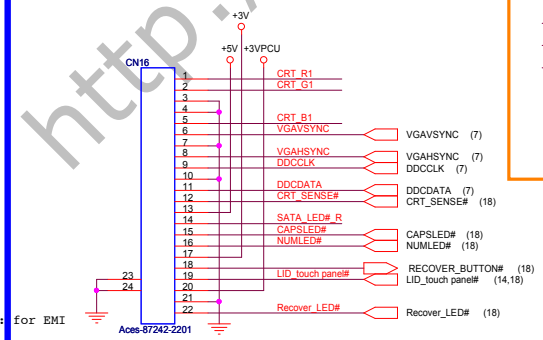
9/24 Ramp-test : change footprint to sensor-3x3-5-16p-smt.(part two)

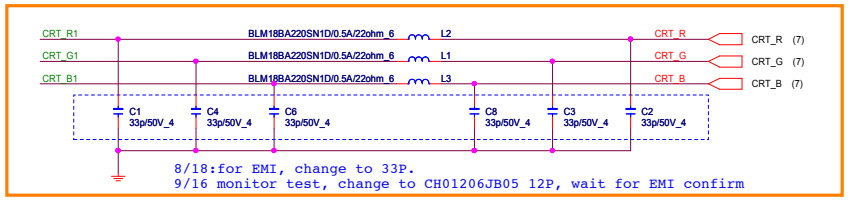
FAE : Because of internal pull-high in SDO, I2C address for SDO floated is the same as that for SDO high

Card Reader/USB DB CONNECTER(MMC)/Power Connector

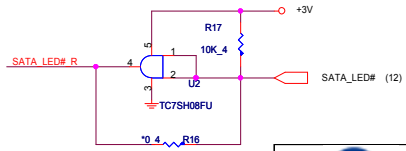


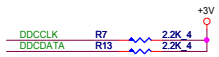
CRT D/B (CRT)





For EMI





Quanta Computer Inc.

PROJECT : ZE8

Size	Document Number	Rev
	KB/BT/PR/TP/LAN/LED/CR Connects	1A

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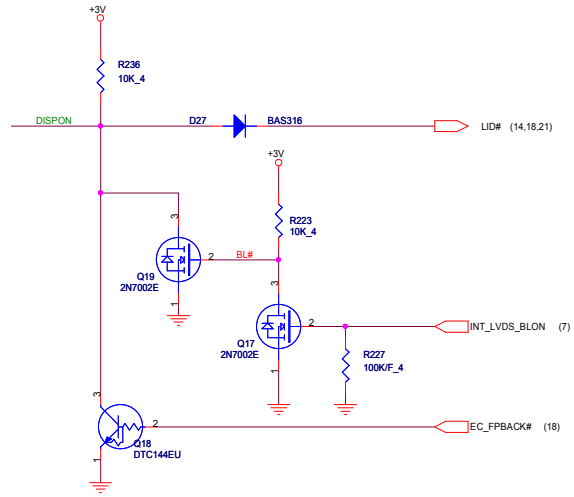
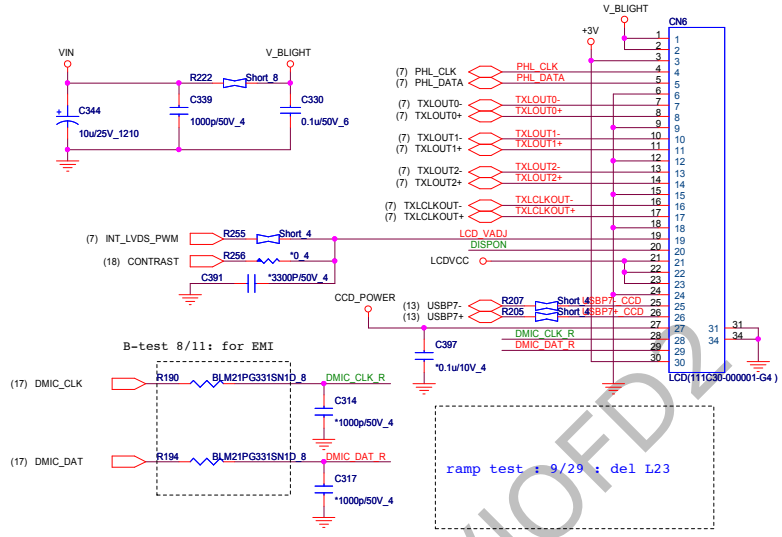
Backlight Control(LDS)

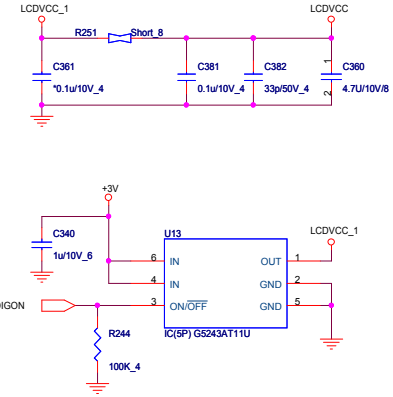


LED Panel(LDS)

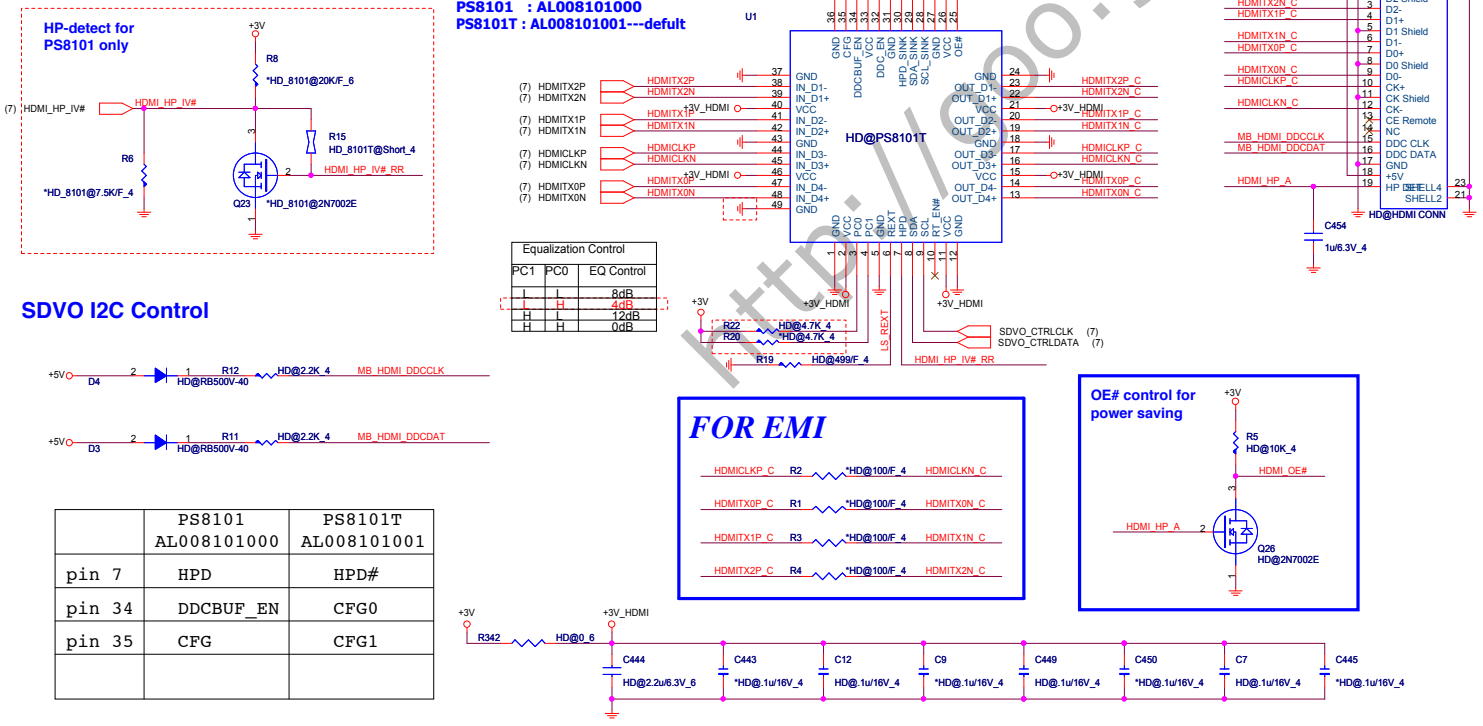
C test: 8/31: exchange V_BLIGHT and LCDVCC pin define



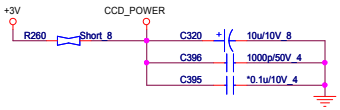
LED Panel POWER SWITCH(LDS)



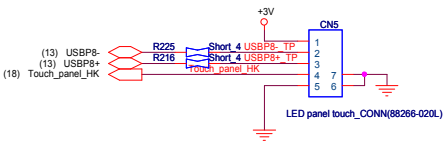
HDMI(HDM)



Camera(CCD)



LED touch Panel connector (LDS)



ramp test : 9/29 : del L24

Quanta Computer Inc.
PROJECT : ZE8

Size	Document Number	Rev
	LED Panel/CCD/HDMI	1A

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Charger(DCD)

DC-IN JACK

PJ2 — POWER_JACK dcjk-2dc3003-001211-5p

PA1 — PL10 HI0805R800R-10/5A/80ohm_8 — VA

PC148 2200p/50V_6 — PC150 0.1u/50V_6 — PC4 *0.1u/50V_6

PD1 1N4148WS

PD10 SX34 — PD9 CYSMAJ20

PC6 0.1u/50V_6 — PC145 0.1u/50V_6

R1 — PR5 0.01_3720

PC12 0.1u/50V_6 — PR6 220K/F_6 — PR10 220K/F_6

PQ1 IMD2AT108

C-STAGE change source

PQ36 AO4427 — PC147 *0.1u/50V_6 — PC146 2200p/50V_6

C-STAGE change source

PQ4 AO4427 — PR57 33K_6 — PC162 1000p/50V_4

PR59 10K_6

PQ5 2N7002K — (18) D/C#

PR168 100K/F_6 — +3VPCU

(18) ACIN — ACIN

PR45 10/F_6 — PR43 10/F_6 — PC47 0.1u/50V_6 — PR20 4.7_6 — PC43 1u/16V_6

CSIP_1 — CSIP — CSIN — VA2

PC25 1u/16V_6 — 88731_VDDP — PD8 RB500V-40

PC58 2200p/50V_6 — PC57 *0.1u/50V_6 — PC56 10u/25V_1206 — VIN

PC30 0.1u/50V_6

(18) MBDATA — (18) MBCLK

PU5 CM1293A-04SO — CH1 CH4 VN VP CH2 CH3 — MBCLK +3VPCU MBDATA — TEMP_MBAT

Add ESD diode base on EC FAE suggestion

PU2 ISL88731A

NC GND GND GND GND CSSP CSSN VCC VDDP

VDDSMB SDA SCL ACOK DCIN ACIN VREF ICOMP NC VCOMP

BOOT UGATE PHASE LGATE PGND CSOP CSON NC VBF GND

NC ICM NC GND

PR40 2.7_6 — PC34 0.1u/50V_8

88731_DH — 88731_LX — 88731_DL

PQ3 AO4932

PR58 0.01_3720 — PL6 6.8uH/4.5A_7X7X3 — BAT-V

PR56 2.2/F_6 — PC55 2200p/50V_6

PC130 2200p/50V_6 — PC62 10u/25V_1206 — PC80 10u/25V_1206 — PC131 0.01u/50V_6 — PC163 1000p/50V_4

CSOP_1 — BAT-V

PC31 0.1u/50V_6 — DCIN

PR23 49.9/F_6 — PR164 82.5K/F_6 — PR48 22K/F_6

PR180 10/F_6 — PC27 0.1u/50V_6 — PR179 10/F_6 — PR172 *Short_4 — PR16 100_4

PR47 2.21K/F_6 — PC49 0.01u/50V_6 — PC52 *1u/16V_6 — PC51 0.01u/50V_6 — PC50 *0.01u/50V_6

ICMNT (18) — PC44 3300p/50V_4

C114F3-108A1-L_Batt_Conn — PJ1 — MBAT+

PR65 *Short_6 — PC67 100p/50V_6

PR63 *0_6 — PD5 RB500V-40

PL1 HI0805R800R-10/5A/80ohm_8 — PL4 HI0805R800R-10/5A/80ohm_8 — BAT-V

TEMP_MBAT (18)

PR147 100K/F_6 — +3VPCU

PC121 0.1u/50V_6 — PC127 47p/50V_6 — PC63 47p/50V_6

PR152 100_4 — PR150 100_4 — MBCLK — MBDATA

PR148 *100K/F_6 — PC122 0.01u/16V_4

Quanta Computer Inc.

PROJECT : ZE8

Size	Document Number	Rev
	CHARGER (ISL88731)	1A

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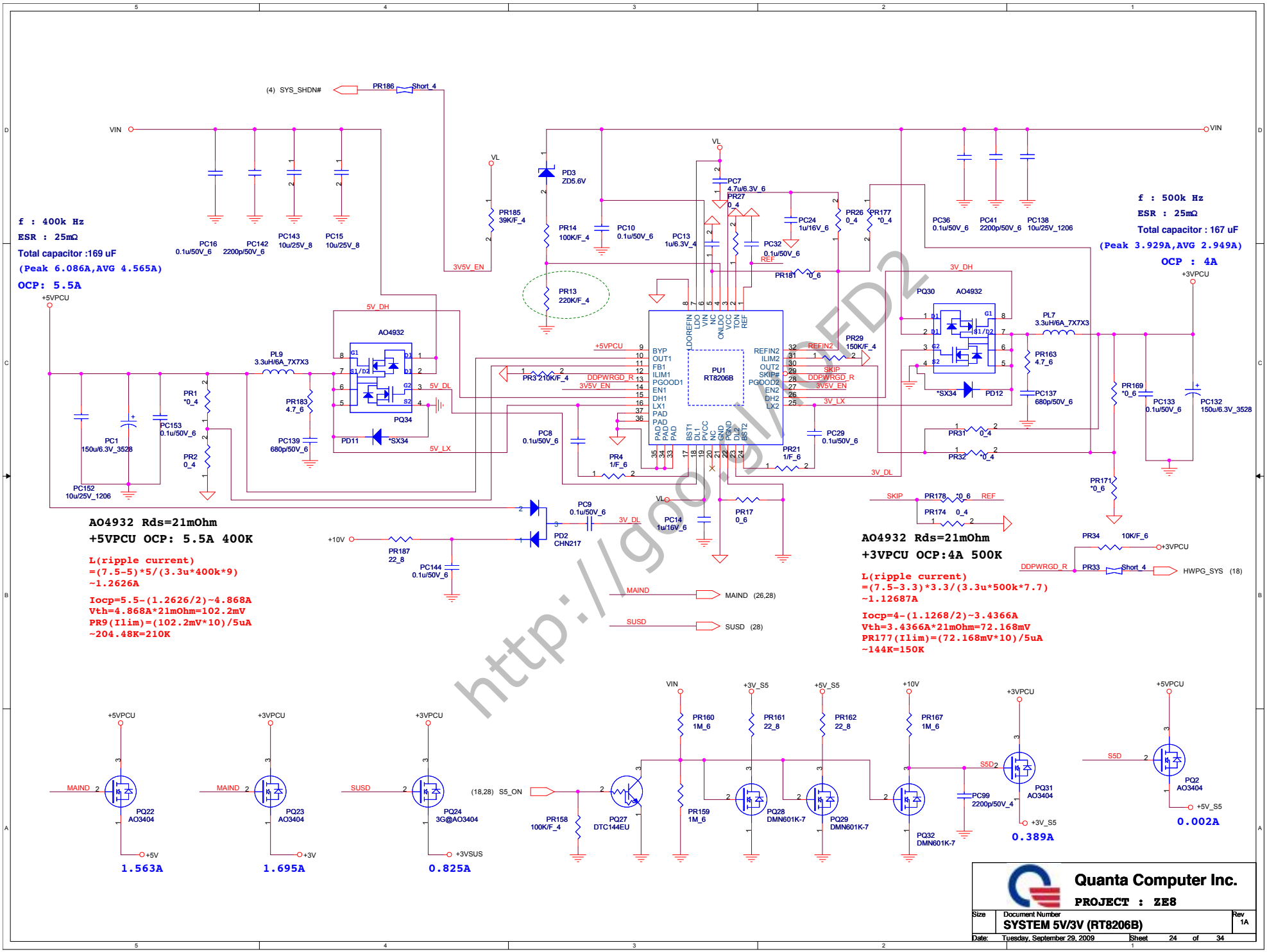

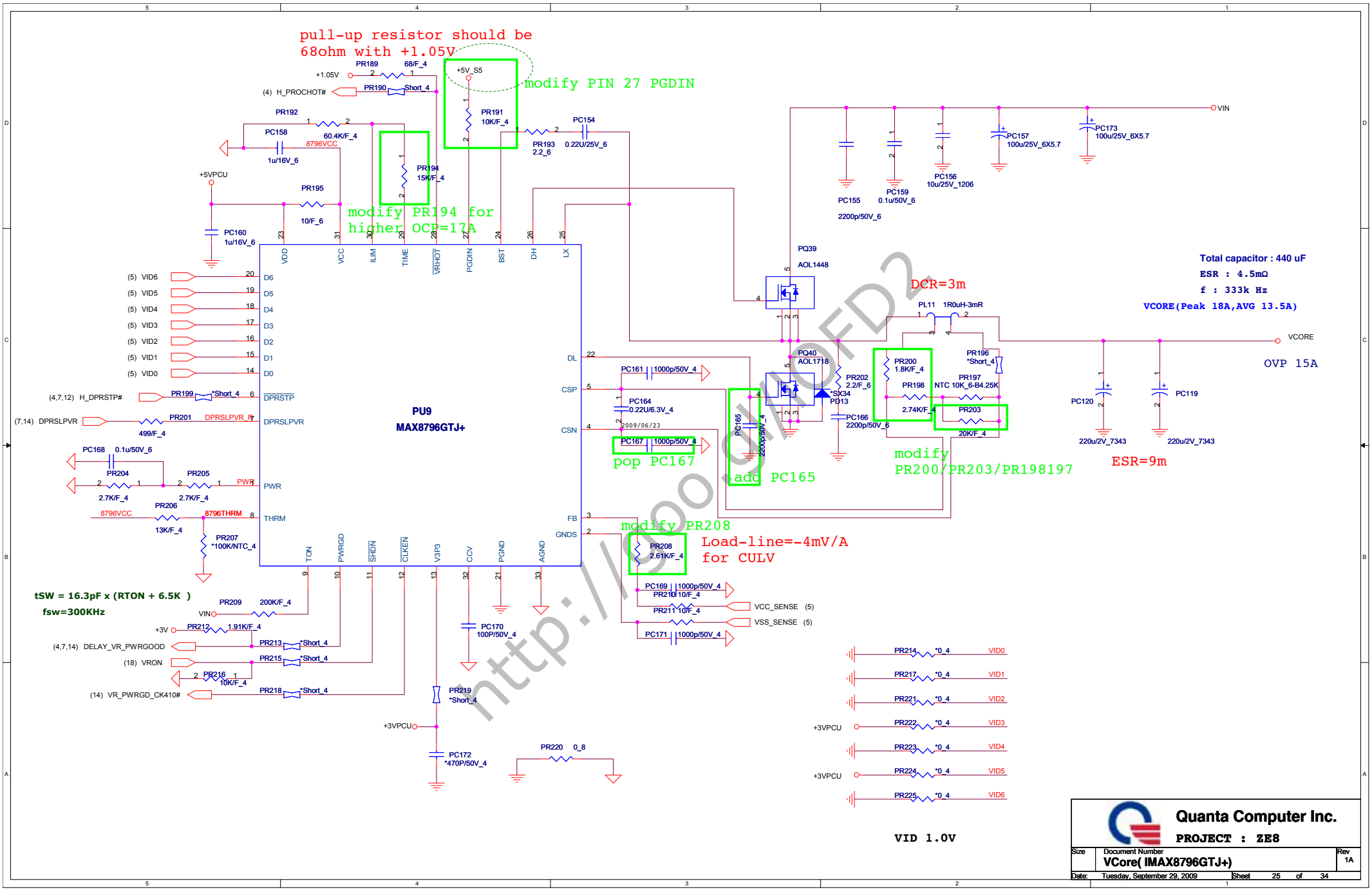
pull-up resistor should be
68ohm with +1.05V
modify PIN 27 PGDIN
modify PR194 for
higher OCP=17A
PU9
MAX8796GTJ+
PQ39
AOL1448
PQ40
AOL1718
DCR=3m
Total capacitor : 440 uF
ESR : 4.5mΩ
f : 333k Hz
VCORE(Peak 18A,AVG 13.5A)
OVP 15A
ESR=9m
pop PC167
add PC165
modify
PR200/PR203/PR198197
modify PR208
Load-line=-4mV/A
for CULV
tSW = 16.3pF x (RTON + 6.5K)
fsw=300KHz
VID 1.0V
VIN
VCORE
+5V_S5
+1.05V
+5VPCU
+3V
+3VPCU
8796VCC
8796THRM
VCC_SENSE (5)
VSS_SENSE (5)
(4) H_PROCHOT#
(4,7,12) H_DPRSTP#
(7,14) DPRSLPVR
(4,7,14) DELAY_VR_PWRGOOD
(18) VRON
(14) VR_PWRGD_CK410#
(5) VID6
(5) VID5
(5) VID4
(5) VID3
(5) VID2
(5) VID1
(5) VID0
PR189 68/F_4
PR190 Short_4
PR191 10K/F_4
PR192 60.4K/F_4
PR193 2.2_6
PR194 15K/F_4
PR195 10/F_6
PR196 *Short_4
PR197 NTC 10K_6-B4.25K
PR198 2.74K/F_4
PR199 *Short_4
PR200 1.8K/F_4
PR201 499/F_4
PR202 2.2/F_6
PR203 20K/F_4
PR204 2.7K/F_4
PR205 2.7K/F_4
PR206 13K/F_4
PR207 *100K/NTC_4
PR208 2.61K/F_4
PR209 200K/F_4
PR210 10/F_4
PR211 10/F_4
PR212 1.91K/F_4
PR213 *Short_4
PR214 *0_4
PR215 *Short_4
PR216 10K/F_4
PR217 *0_4
PR218 *Short_4
PR219 *Short_4
PR220 0_8
PR221 *0_4
PR222 *0_4
PR223 *0_4
PR224 *0_4
PR225 *0_4
PC154 0.22U/25V_6
PC155 2200p/50V_6
PC156 10u/25V_1206
PC157 100u/25V_6X5.7
PC158 1u/16V_6
PC159 0.1u/50V_6
PC160 1u/16V_6
PC161 1000p/50V_4
PC164 0.22U/6.3V_4
PC165 2200p/50V_4
PC166 2200p/50V_6
PC167 1000p/50V_4
PC168 0.1u/50V_6
PC169 1000p/50V_4
PC170 100P/50V_4
PC171 1000p/50V_4
PC172 *470P/50V_4
PC173 100u/25V_6X5.7
PC119 220u/2V_7343
PC120 220u/2V_7343
PL11 1R0uH-3mR
*SX34 PD13
2009/06/23
VDD
VCC
ILIM
TIME
VRHOT
PGDIN
BST
DH
LX
DL
CSP
CSN
FB
GNDS
D6
D5
D4
D3
D2
D1
D0
DPRSTP
DPRSLPVR
PWR
THRM
TON
PWRGD
SHDN
CLKEN
V3P3
CCV
PGND
AGND
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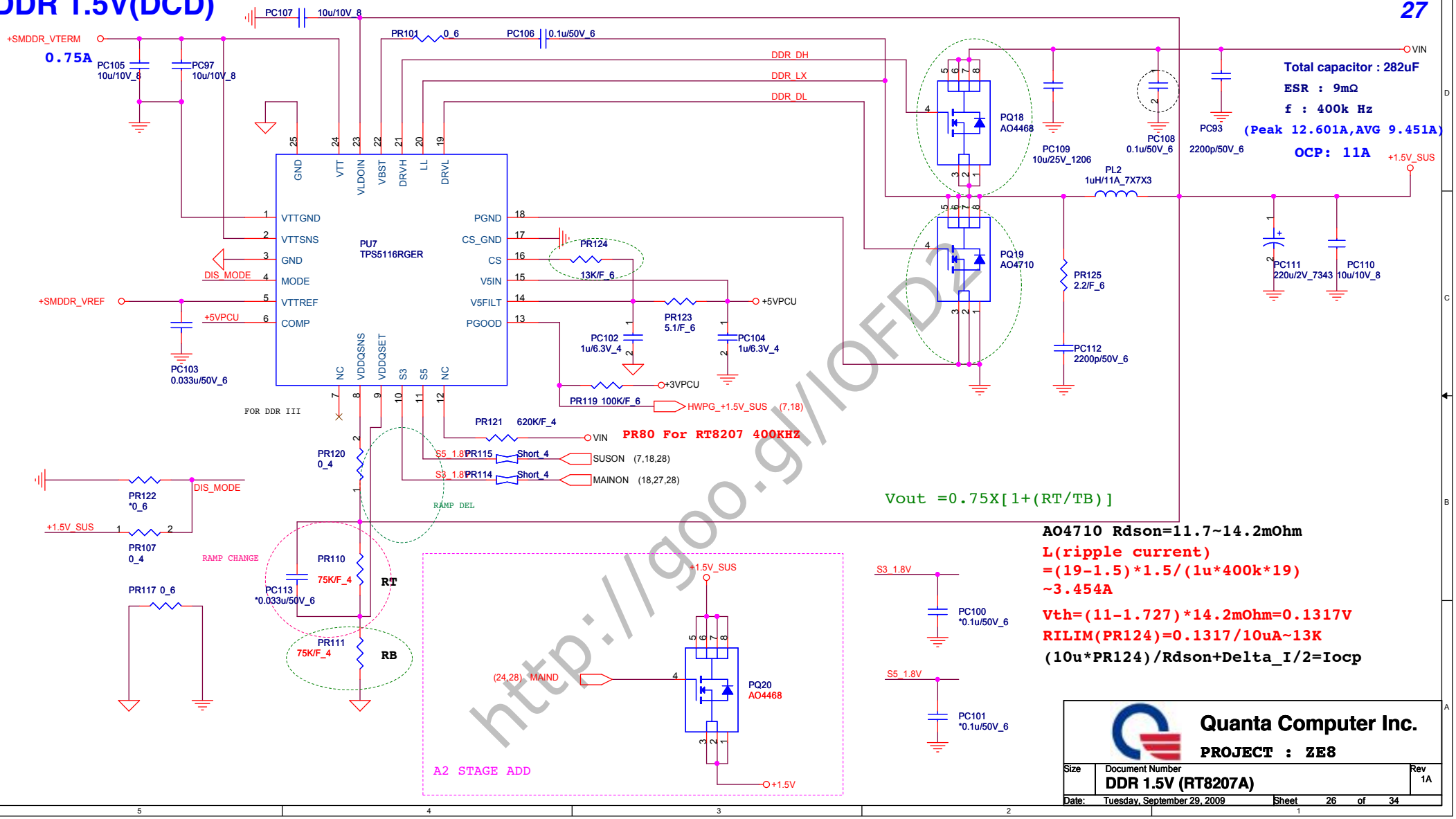
DDR 1.5V(DCD)



AO4710 Rdson=11.7~14.2mOhm

L(ripple current)
=(19-1.5)*1.5/(1u*400k*19)
~3.454A

Vth=(11-1.727)*14.2mOhm=0.1317V

RILIM(PR124)=0.1317/10uA~13K

(10u*PR124)/Rdson+Delta_I/2=Iocp

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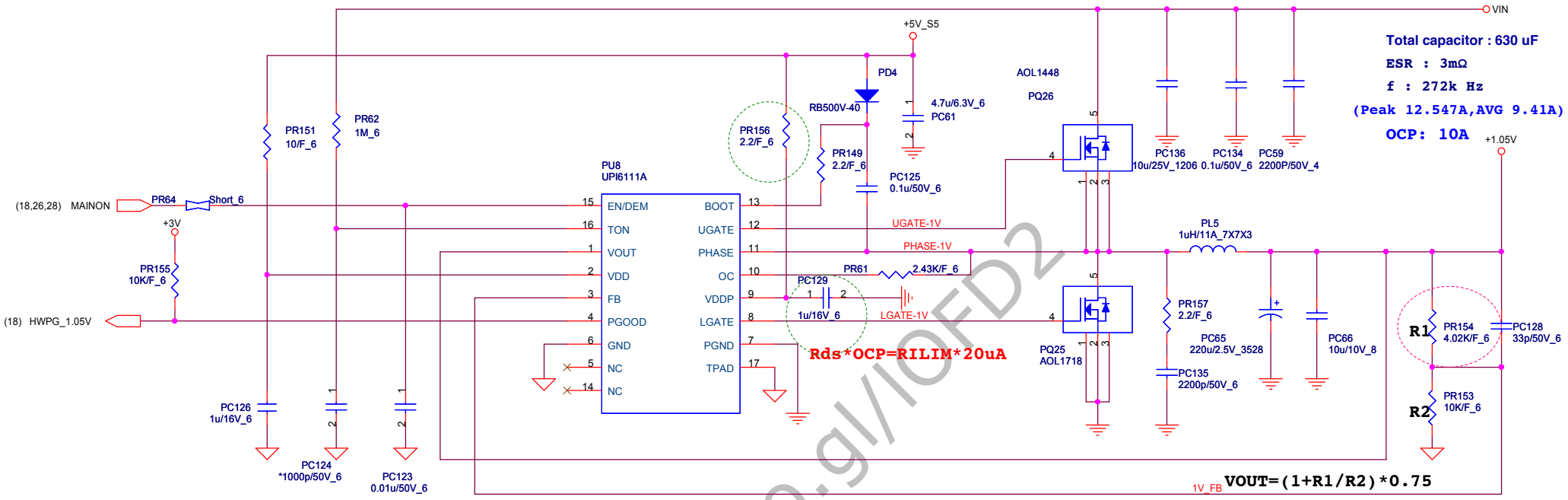


TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

AOL1718 Rdson=4.6mOhm

OCP=10-0.8A

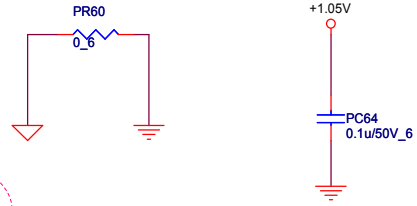
L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.646A

4.6m*10=RILIM*20uA

RILIM(PR61)=2.3K--- 2.43K

RAMP CHANGE

	743 CPU	Other CPU
PR154	4.22K (CS24223F917)	4.02K (CS24023F928)



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	VCCP 1.05V (RT8202A)	1A

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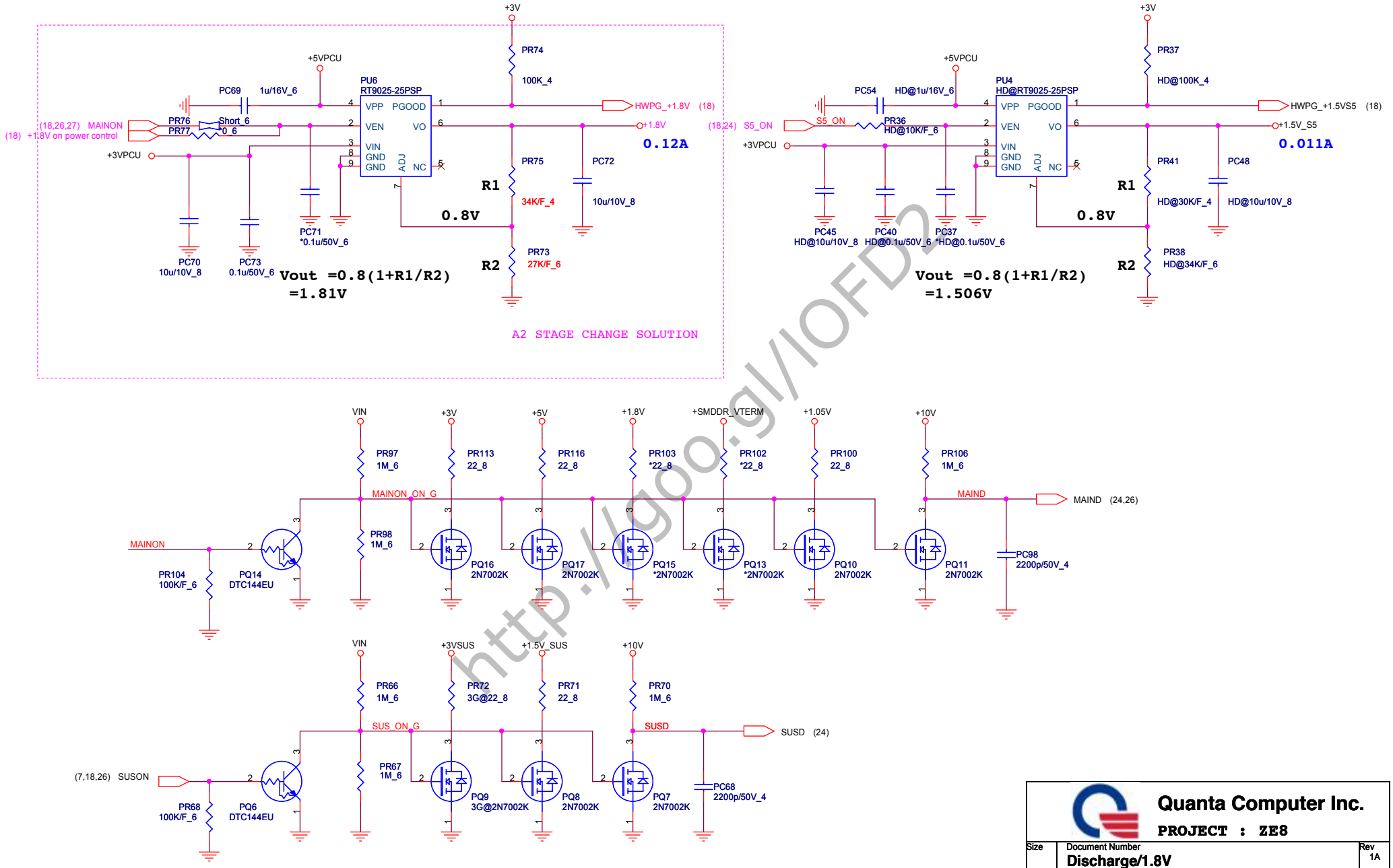
Discharger/1.8V(DCD)



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	Discharge/1.8V	1A

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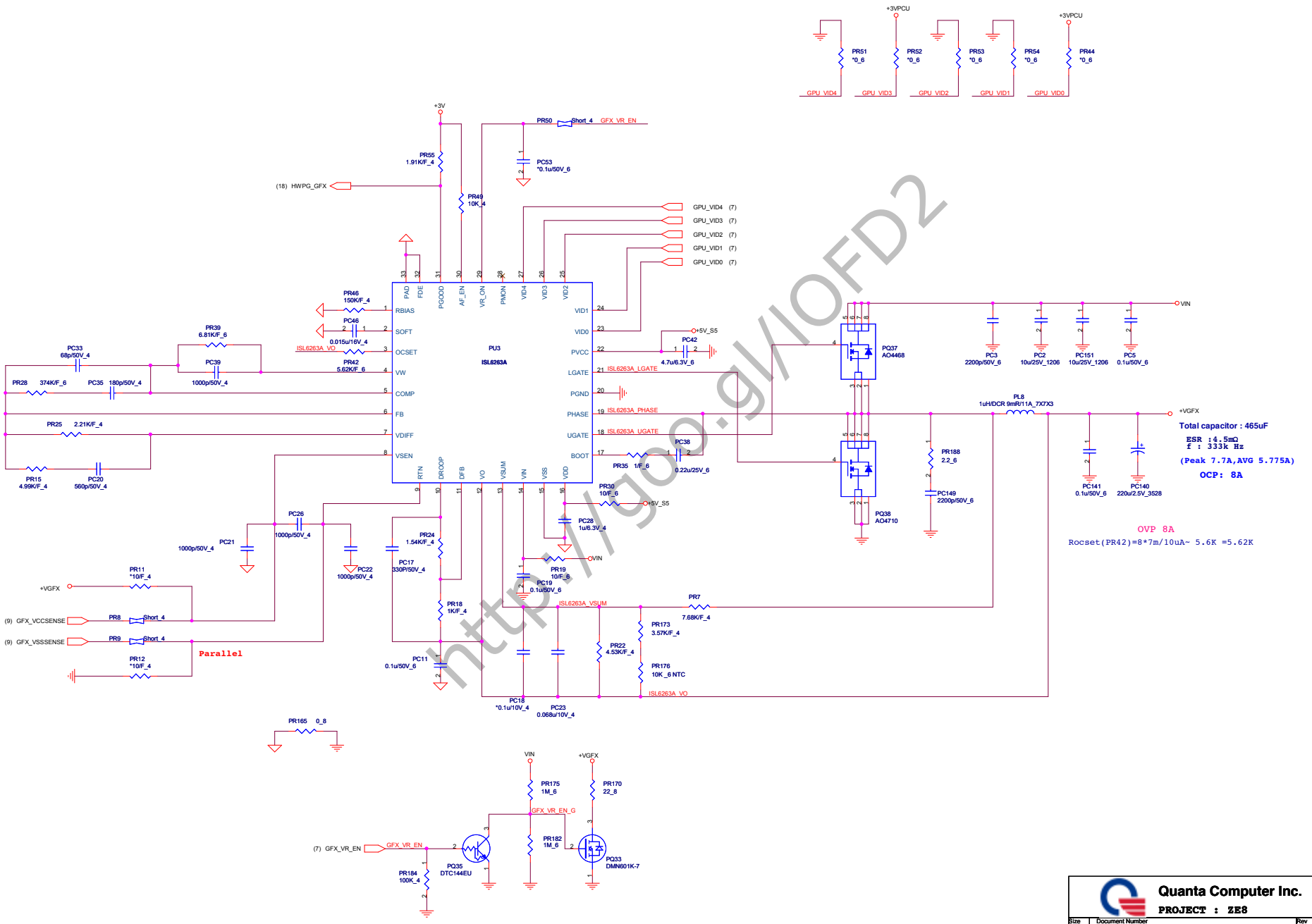

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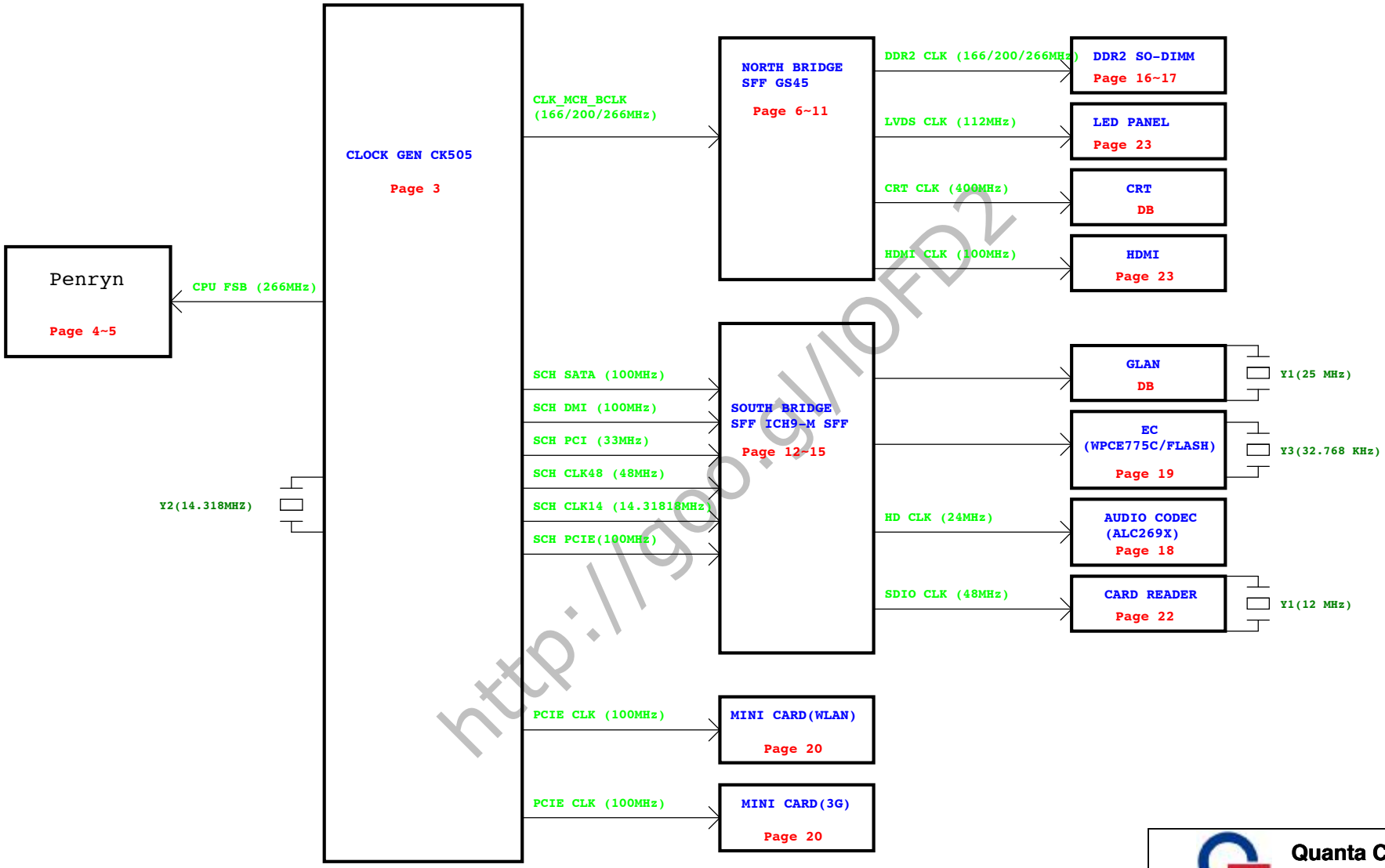

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Size	Document Number	Rev
	Clock Distribution Diagram	1A

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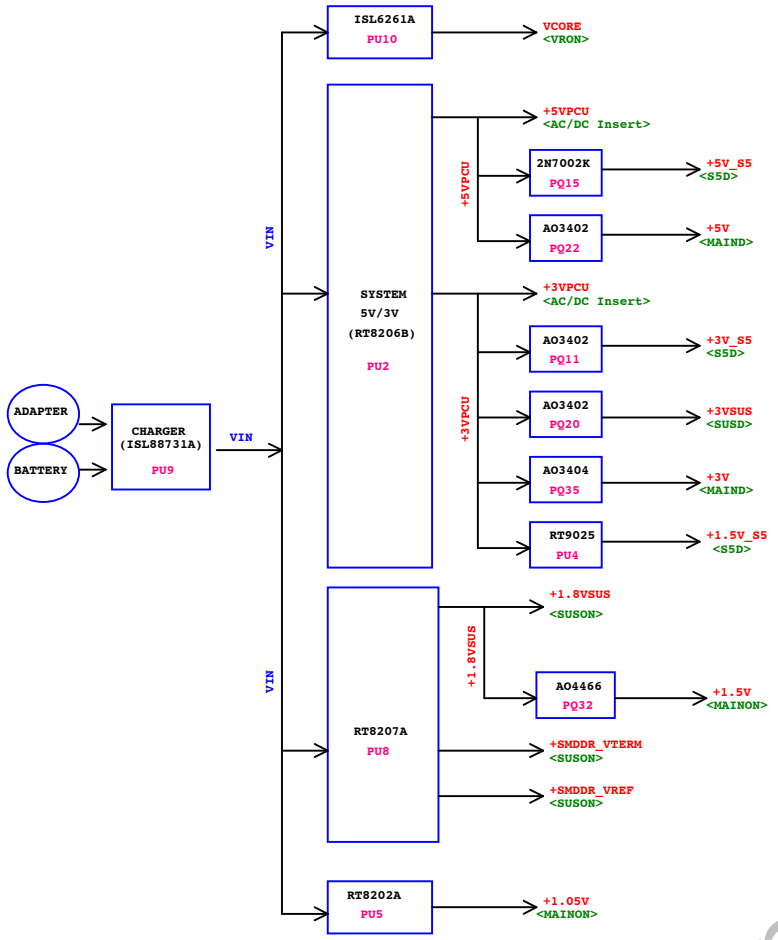

POWER	Distribution
VCORE	CPU
+5VPCU	RTC, USB Connecter
+5V_S5	ICH9M Power
+5V	ICH9M Power, CRT, Audio Codec, SATA HDD, Touch Pad ,HDMI
+3VPCU	RTC, LED Power, CRT, EC, ID , SPI Flash , Green Adapter
+3V_S5	ICH9M Power, CR
+3VSUS	3G
+3V	CLK_GEN Power, Thermal Sensor Power, NB Power, SB, DDRII Power, Audio Codec, LCD Power, WLAN/WMAX, 3G, Card Reader, BT, EC, LED, CRT, CAMERA
+1.5V_S5	ICH9M Power
+1.8VSUS	NB Power, DDRII SO-DIMM
+1.5V	CPU, NB, SB, AUDIO Codec, WLAN/WMAX, 3G
+SMDDR_VTERM	DDRII SO-DIMM
+SMDDR_VREF	DDRII SO-DIMM
+1.05V	CLK_GEN, CPU, NB, SB

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CK505 Clock Setting Table

Differential CPU Clock

Pin Name	Pin	Net Name	Description
CPU_0	61	CLK_CPU_BCLK	
CPU_0#	60	CLK_CPU_BCLK#	Differential CPU clock
CPU_1	58	CLK_MCH_BCLK	
CPU_1#	57	CLK_MCH_BCLK#	Differential NB GS45 clock

PCI Express Clock

Pin Name	Pin	Net Name	Description
SRC0/DOT96	20	DREFCLK	
SRC0#/DOT96#	21	DREFCLK#	96MHz DOT clock for NB GS45
LCDCLK/27M	24	DREFSSCLK	
LCDCLK#/27M_SS	25	DREFSSCLK#	Clock output for NB GS45 graphic contoller
SRC2	28	PECLK_SATA	
SRC2#	29	PECLK_SATA#	Differential Serial Reference Clock for SB ICH9M SATA
SRC3/CR#_C	31	PECLK_ICH	
SRC3#/CR#_D	32	PECLK_ICH#	Differential Serial Reference Clock for SB ICH9M
SRC4	34	PECLK_LAN	
SRC4#	35	PECLK_LAN#	Differential Serial Reference Clock for on board LAN
SRC6	48	PECLK_MINI2	
SRC6#	47	PECLK_MINI2#	Differential Serial Reference Clock for Mini Card 2
SRC7/CR#_F	51		No use
SRC7#/CR#_E	50	CLKREQ#_MINI2	Clock Request for Mini Card 2 (SRC6)
SRC8/CPU_ITP	54		
SRC8#/CPU_ITP#	53		No use
SRC9	37	PECLK_MINI1	
SRC9#	38	PECLK_MINI1#	Differential Serial Reference Clock for MINI CARD 1
SRC10	41	PECLK_3GPLL	
SRC10#	42	PECLK_3GPLL#	Differential Serial Reference Clock for NB GS45
SRC11/CR#_H	40	CLKREQ#_MCH	Clock Request for NB GS45 (SRC10)
SRC11#/CR#_G	39	CLKREQ#_MINI1	Clock Request for Mini Card 1 (SRC9)

PCI Clock

Pin Name	Pin	Net Name	Description
PCI0/CR#_A	8	CLKREQ#_SATA	Clock Request for SATA (SRC2)
PCI1/CR#_B	10	CLKREQ#_LAN	Clock Request for on board LAN (SRC4)
PCI2	11	PCLK_DEBUG	PCI clock for debug card
PCI3	12		No use
PCI4	13	PCLK_EC	PCI clock for EC
PCI5	14	PCLK_ICH	PCI clock for SB ICH9M

Other Clock

Pin Name	Pin	Net Name	Description
USB_48	17	CLK48_ICH	48MHz for SB ICH9M
		CLK48_CARD	48MHz for USB Card Reader
REF	5	CLK14_ICH	14.318MHz for SB ICH9M

Clock Request Table

CLKREQ#	MAPPING		Control
	0	1	
CR#_A	SRC0	SRC2	SATA
CR#_B	LCDCLK	SRC4	LAN
CR#_C	SRC0	SRC2	N/A
CR#_D	LCDCLK	SRC4	N/A
CR#_E	SRC6		MINI2
CR#_F	SRC8		N/A
CR#_G	SRC9		MINI1
CR#_H	SRC10		MCH

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	Schematic Setting	1A

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Model	REV	DATE	CHANGE LIST	NOTE
ZE8	A1A		PAGE23 :move LED touch Panel hall sensor to LAN DB	ECN Release
			PAGE20 : reserve R179 , R183 for 3G wake up function	
			PAGE5 : Del C128,C173,C149,C171,C130,C131,C133,C169,C181,C177,C132,C175,C140,C138,C185,C154,C135,C92,C184,C106,C117,C156,C186,C153 for placeing C386 in CPU BGA TOP side	
			PAGE18 :change U14 footprint to qfn48-7x7-5-58p-0_9h	
			PAGE23 :change CN18 PN to DFHD19MR053	
			PAGE23 :Add L28 and L29 for CCD and Touch screen USB signals	
			PAGE23 :change CN18 footprint to hdmi-100042mr019m21hzr-19p-v	
			PAGE23 :change CN19 footprint to 85204-0500x-5p-l	
			PAGE23 :add 5V power trace to CN19 for touch screen IC	
			PAGE19 :FAE suggest that add R352 for VCC latch up	
			PAGE19 : FAE suggest that change C347 and C350 value from 15p to 6.8p	
			PAGE10 : add stitching caps C149,C153 and C154 for DMI signals	
			PAGE14 : add stitching caps C156,C169 and C171 for DMI signals	
			PAGE20 : add C431 for SIM Card to filter power noise.	
			PAGE20 : change U10 PN from AL001293003 to AL001293000	
			PAGE21 : reserve ESD protection U11 for SATA signals.	
			PAGE23 : del +5V signal of CN19	
			PAGE18 : add stitching caps C432,C438 for Audio signals	
			PAGE21 : del hole 19	
			PAGE22 : reserve C439, C440,C445,C446,C447,C448 for EMI	
			PAGE23 : reserve C106 for EMI	
			PAGE 19, 20 : del R179, R183 and 3G wake up signals of 3G wake up function	
			PAGE19 : add D30 for WLAN_LED# connect from WALN connector to EC	
			PAGE19 : add 3G_EC_LED# signal from EC to LED connector CN2	
			PAGE19 : change R233 to D31 for leakage issue.	
			PAGE22 : del C426 due to don't need 3G_MINI_LED# singal from 3G connector to LED connector CN2	
			PAGE21 : add EMI bypass caps	
			PAGE23 : HDMICLKP swap to HDMITX0P,HDMICLKN swap to HDMITX0N,HDMICLKP_C swap to HDMITX0P_C,HDMICLKN_C swap to HDMITX0N_C	
			6/13 : PAGE10 : change C63 and C208 value from 220u to 10u.	
			6/15 : PAGE18 : due to layout, add 9 GND pin for U14	
			6/15 : PAGE19 and 23 : add Touch_panel_HK signal for hot key on touch panel	
			6/16 : PAGE 23 : change R14 to C454 of CN18 for HDMI detect issue	
			6/18 : PAGE 23 : change CN5 PN to DFHD05MRD98	
			6/18 : PAGE 19 : change U14 PN to AKE38ZA0Q00	
	B1A		6/22 : PAGE 21 : change CN17_PN to DFHS04FR269	
			6/22 : PAGE 24 : change PJ1_PN to DFHD08MR085	
			6/23 : PAGE 22 : Per Acer request, use interrupt pin of G-sensor to detect panel status ,so , stuff R150, remove R151	
			6/25 : PAGE 19 : EC add +1.5V on power control net name to control 1.5V	
			6/25 : PAGE 22 : connect G-sensor interrupt signal to SB PIRQE#	
			6/26 : PAGE 26 : change V-core solution to Maxim IC	
			6/26 : PAGE 24 : add PD20 in TEMP_MBAT signal	
			6/29 : PAGE 9 : change C212 from 330U to 10U for placement issue	
			6/30 : PAGE 16 : change DDR2 to DDR3	
			7/2 : PAGE 14 : LID_touch panel# change from GPIO19 to GPIO7 (SCI)	
			7/2 : PAGE 16 : change DDR3 connector footprint to H=5.2mm	
			7/6 : PAGE 18,21 : add RECOVER_BUTTON# signal in EC and CRT DB	
			7/7 : PAGE 18,21 : add RECOVER_LED# signal in EC and CRT DB	
			7/7 : PAGE 24 : add PD11 and PD12	
			7/7 : PAGE 25 : add PD13	
			7/7 : PAGE 20 : add nut on Hole 7, Hole 8 and Hole 11	
			7/7 : PAGE 18 : add R355 for power consumption issue,Vendor suggest to place it close to EC.	
			7/8 : PAGE 18 : add D30 for current leakage issue of 3G_EC_LED# signal.	
			7/9 : PAGE 18 : add D31 to prevent current leakage of Recover_LED# signal.	
			7/10 : PAGE 19 : change the direction of Q21 and Q22 to prevent the current leakage	
			7/10 : PAGE 3 : follow vendor suggestion to change C226 from 33p to 27p.	
			7/13 : PAGE 18 : follow vendor suggestion to change C337 and C343 from 6.8p to 15p.	

Model	REV	DATE	CHANGE LIST	NOTE
ZE8	C1A		7/23 : PAGE 20 : change CN17 footprint to usb-04wl4b-4p-r-v	ECN Release
			7/23 : PAGE 20 : add U38 re-driver IC for SATA connector	
			7/29 : PAGE 19 : change JSIM1 pin define to solve SIM card not detect issue	
			7/31 : PAGE 20 : add parade solution of SATA re-driver IC	
			8/4 : PAGE 20 : change footprint of U38 to qfn20-4x4-5-21p-ps8511b	
			8/6 : because of DMI reference to GND, so, del C60 C67 C61 C150 C166 C153 CAPS	
			8/6 : PAGE 20 : change Hole 18 footprint HG-C237D94P2, Hole 16 to H-C91D91N	
			8/10 : PAGE 19 : change JSIM1 PN to DFHS06FS017 and change footprint to simcard-sim-06lj3g-10p	
			8/11 : add C244 C245=220pF, add C243 =680pF,change C11= 1000pF,add C60=1000pF,change C307= 1000pF,add C363=0.1uF,change C10= 0.1uF, R113 change to BLM18BA750SN1 ferrite bead,R252, R253 = ferrite bead (BLM18PG471SN1),R190, R194 = BLM21PG331SN1 for EMI	
			8/12 : change JSIM1 back to A2-test P/N and footprint.	
			8/13 : add C246,C247=220pF, add C471=0.1uF for EMI	
			8/28 : page13 : add pull high resister R160 in GNT3# pin for no video issue.	
			8/31 : page 22 : exchange V_BLIGHT and LCDVCC pin define	
			9/2 : page 19 : change PN and footprint of JSIM1 back to A1 type.	
			9/2 : page 21 : change G-Sensor footprint to sensor-3x3-5-16p-smt for SMT solder issue.	
			9/8 : page 23 : change battery connector footprint to bat-btj-08fg0b-8p-l-v for SMT issue.	
			9/8 : change R141,R303,R199,R259,R254,R174,R201,R172,R173,R217,R261,R168,R175,R249,R150,R15 to short pad	
	C3A		9/28 : change PU2 footprint from QFN28-5X5-5-33P to qfn28-5x5-5-33p-nb4	

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	Change List01	1A

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