Z06 SYSTEM BLOCK DIAGRAM

BOM MARK
IV@: INT VGA
EV@: STUFF FOR EXT VGA
SP@: STUFF FOR UMA or VGA

DDR PWR TPS5116 P34	CHARGER ISL6251 P30
THERMAL PROTECTION P37	3/5V SYS PWR ISL6237 P31
1.5V PWR DISCHARGER P36	CPU CORE PWR OZ8116LN P33
VGA CORE OZ8118 P35	+1.05V RT8202 P32

X'TAL 14.318MHz
CLOCK GENERATOR
ICS:
SELGO: SLG8SP512TTR
P2

Penryn 479
uFCPGA
P3, P4

Thermal Sensor
(G780P81U) P3

Fan Driver
(G991) P24

FSB
667/800/1067 Mhz

NVIDIA N10M-GE1
VRAM 512MB
P17-P22

PCIE 16X

EXT_LVDS
EXT_CRT
EXT_HDMI

SWITCH CIRCUIT
P23

CRT P23
LVDS P23
HDMI P23

HDMI switch (PS8122)
P23

DDRII
SO-DIMM 0
SO-DIMM 1
P16

Dual Channel DDR2
667/800 MHz

NB Cantiga
(GM45/ PM45/ GL40)
P5, P6, P7, P8, P9, P10, P11

LVDS
RGB
INT_LVDS
INT_CRT
INT_HDMI

X4 DMI interface

HDD (SATA) *1
P24

ODD (SATA)
P24

SATA0
SATA1

SB ICH9M
P12,P13,P14,P15

X'TAL 32.768KHz

PCI-Express
PCIE-1

Mini Card WLAN
USB2 P25
USB2

Ext USB Port x 2
USB 0,1 P25

Int USB Port x 1
USB 7 P25

Bluetooth
USB5 P25

CCD
USB11 P23

USB 2.0
Azalia

USB8

PCIE-6

X'TAL 25MHz

Media Cardreader
(RTS5158E)
USB2 P28

Broadcom Giga-LAN
(BCM5764)
P27

LPC

EC (WPC775LDG)
P29

X'TAL 32.768KHz

Audio CODEC (CX20561) P26

MDC 1.5 P26

RJ11 WIRE CONN.

SPI ROM P29

Card Reader Connector P28

Transformer

RJ45 P27

Audio Amplifier G1441 P26

Touch Pad P24

MMB P24

Int. Speaker P26

S/PDIF P26

MIC Jack P26

Int. MIC P23

K/B COON. P29

Quanta Computer Inc.
PROJECT : Z06

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	Block Diagram	1A
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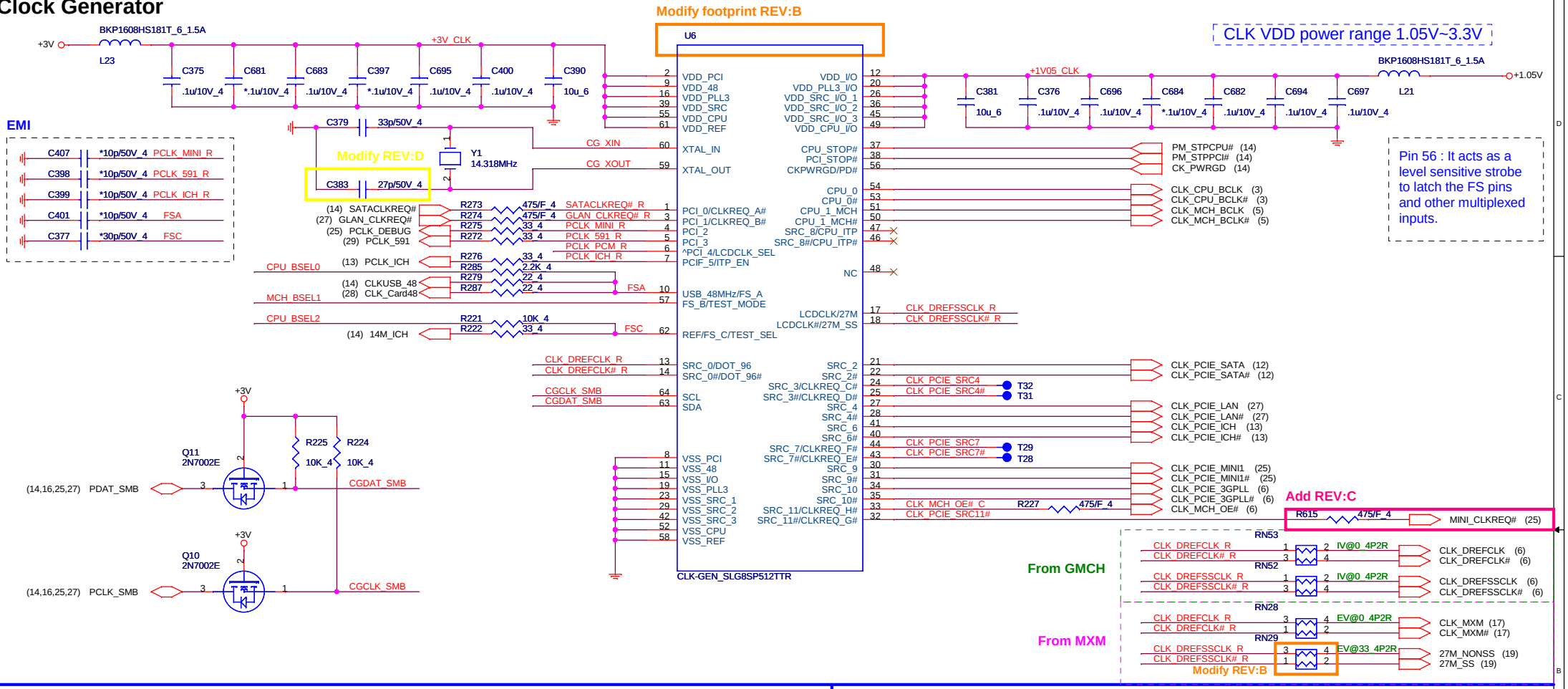
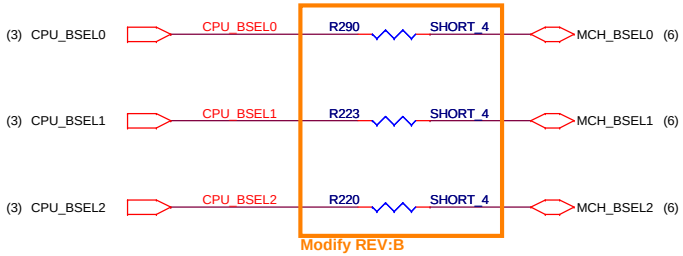
Clock Generator



CPU Clock select

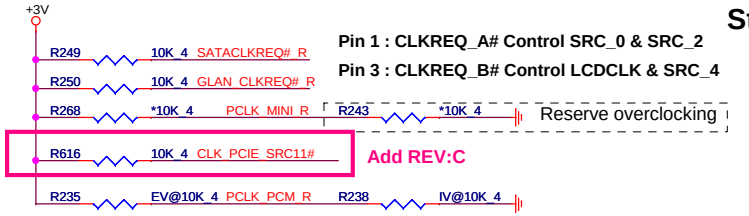
Pin 10/57/62 : For Pin CPU frequency selection



BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz

Strap table



Pin 1 : CLKREQ_A# Control SRC_0 & SRC_2

Pin 3 : CLKREQ_B# Control LCDCLK & SRC_4

Pin 6 : For Pin 13/14 and 17/18 selection
0 = LCDCLK & DOT96 for internal graphic controller support
1 = 27M & 27M_SS &SRC_0 for external graphic controller support

PCLK_ICH_R R269 10K_4

Pin 7 : For Pin 46/47 selection
1 = CPU_ITP
0 = SRC_8

CLOCK GENERATOR

Quanta Computer Inc.
PROJECT : Z06

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	CLOCK GENERATOR	2A
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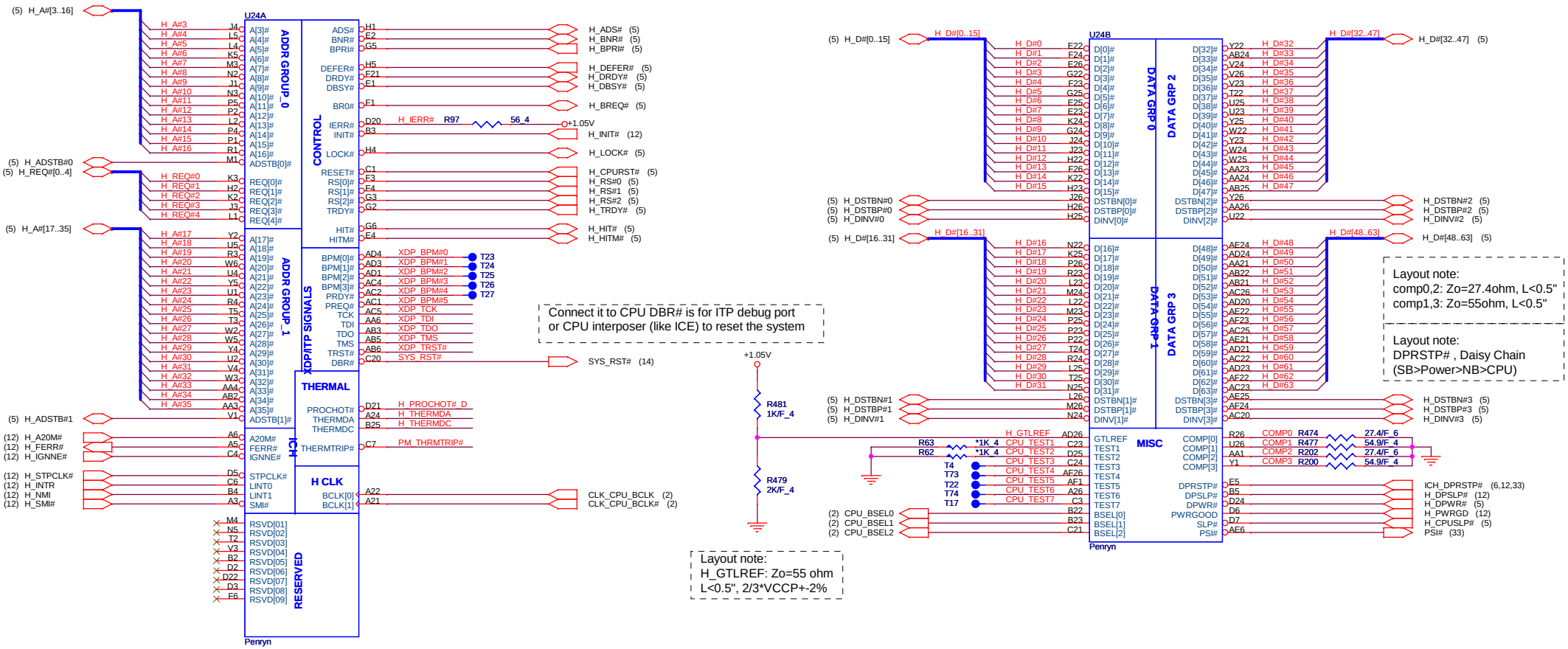
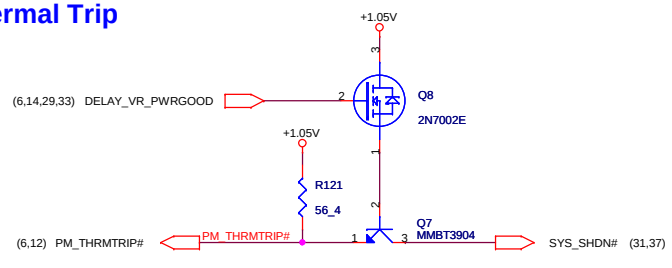
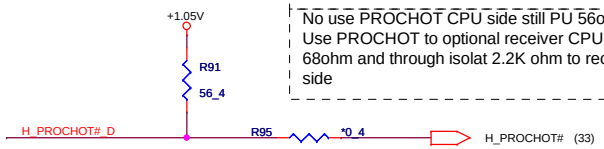


Thermal Trip



Processor hot

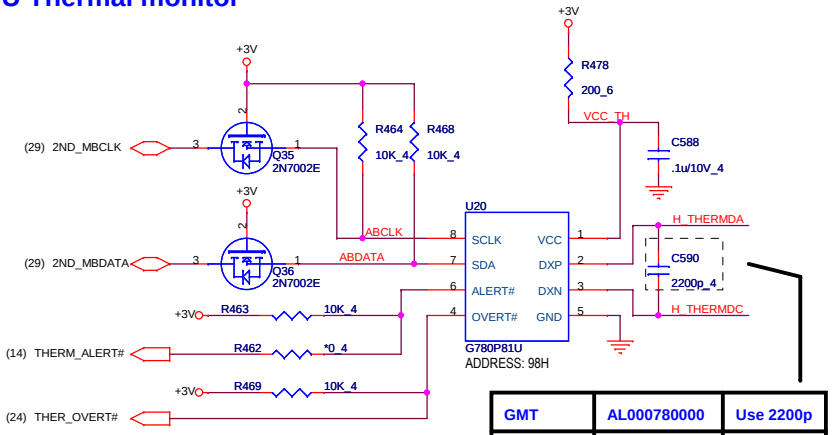


No use Thermal trip CPU side still PU 56ohm.
Use Thermal trip can share PU at SB side

No use PROCHOT CPU side still PU 56ohm.
Use PROCHOT to optional receiver CPU side PU 68ohm and through isolat 2.2K ohm to receiver side

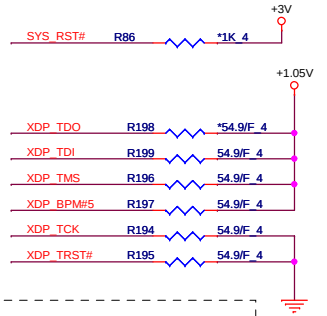
CPU 1/2

CPU Thermal monitor



GMT	AL000780000	Use 2200p
NS	AL095245000	Use 2200p
WINDBOND	AL83L771K01	Use 2200p

XDP PU/PD



XDP_DBRESET# and XDP_TDO reserve for XDP

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	CPU Host Bus	1A
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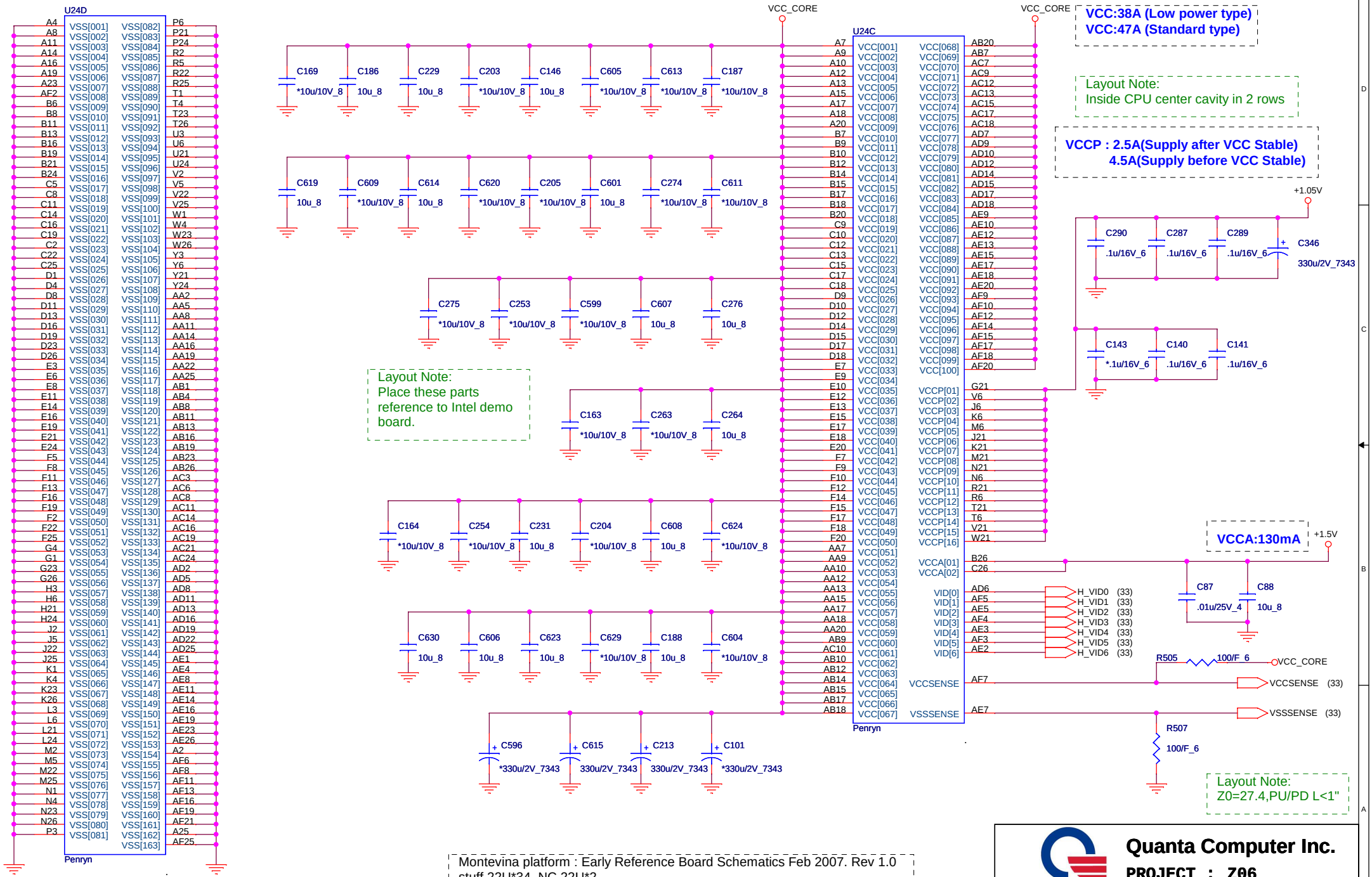

Montevina platform : Early Reference Board Schematics Feb 2007. Rev 1.0
stuff 22U*34, NC 22U*2
stuff 330U*2, NC330U*2

CPU 2/2

Quanta Computer Inc.			
PROJECT : Z06			
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	CPU Power		1A
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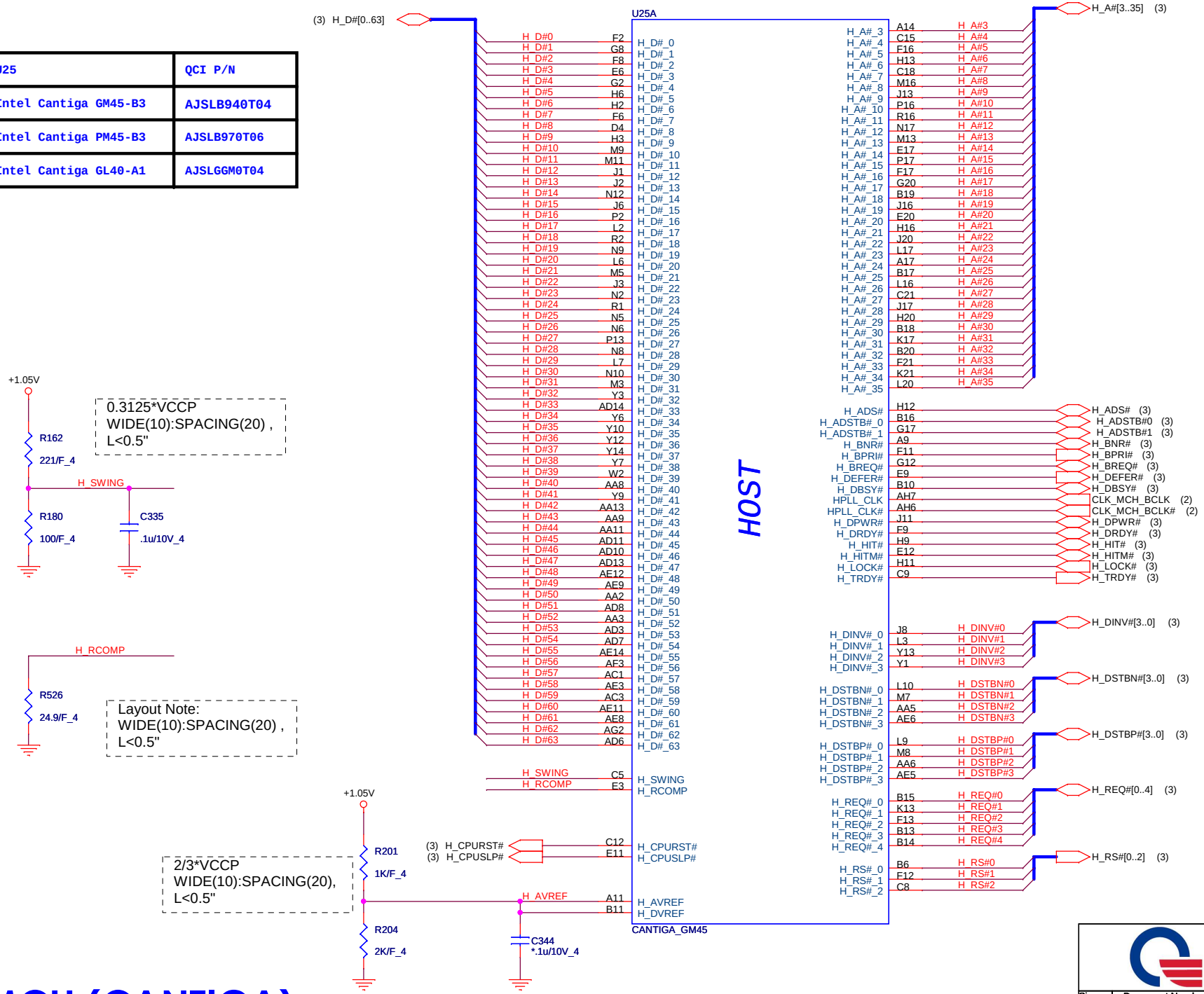
U25	QCI P/N
Intel Cantiga GM45-B3	AJSLB940T04
Intel Cantiga PM45-B3	AJSLB970T06
Intel Cantiga GL40-A1	AJSLGGM0T04



GMCH (CANTIGA)

Quanta Computer Inc.

PROJECT : Z06

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	GMCH HOST	1A
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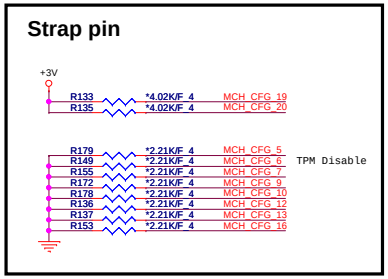
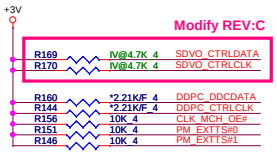
IV@
EV@

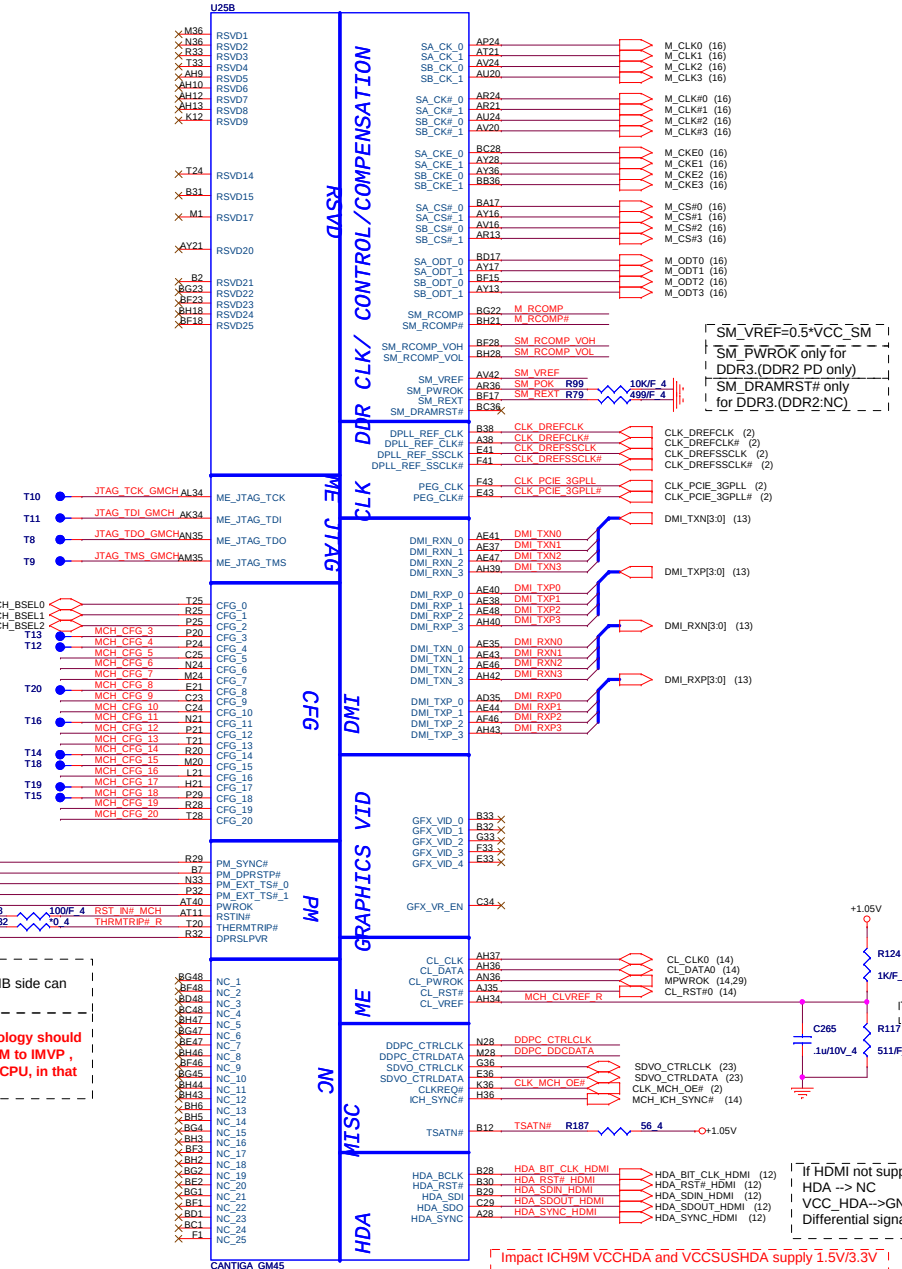
Strap table

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	000= FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)
CFG7	ME TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)
CFG8	Reserved	
CFG9	PCIE Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG10	PCIE Loopback enable	0 = Enabled 1 = Disabled (Default)
CFG11	Reserved	
CFG12	ALLZ	0 = ALLZ mode enable 1 = disable(Default)
CFG13	XOR	0 = XOR mode enable 1 = disable(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display port (SDVO/DP/iHDMI) or PCIE is operational (Default) 1 = Digital Display port (SDVO/DP/iHDMI) and PCIE are operating simultaneously via PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/HDMI Device Present(Default) 1 = SDVO/HDMI Device present
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent(Default) 1 = Digital display(HDMI/DP) device present

Strap pin



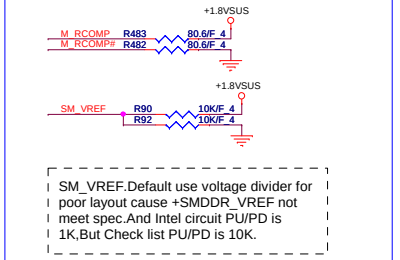




SM_VREF=0.5*VCC_SM

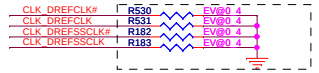
SM_PWROK only for DDR3.(DDR2 PD only)

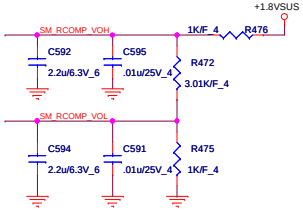
SM_DRAMRST# only for DDR3.(DDR2:NC)



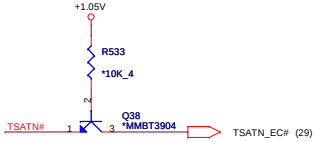
SM_VREF.Default use voltage divider for poor layout cause +SMDDR_VREF not meet spec.And Intel circuit PU/PD is 1K,But Check list PU/PD is 10K.

INTEL FAE Suggest PD for Ext graphics





NB Thermaltrip



NB Thermal trip pin
No use Thermal trip NB side can NC.(NB has ODT)

PM_DPRSTP#
The Daisy chain topology should be routed from ICH9M to IMVP , then to (G)MCH and CPU, in that order.

Check list note : CL_VREF=0.35V

If HDMI not support
HDA --> NC
VCC_HDA-->GND
Differential signal-->NC

DDPC_CTRL for HDMI port C
SDVO_CTRL for HDMI port B

<Checklist ver0.8>
If TSATN# is not used, then it must be terminated with a 56- pull-up resistor to VCCP.

<Pin out check issue>
Cantiga EDS 0.7 change Ball B12 to TSATN# from TSATN

Impact ICH9M VCCHDA and VCCSUSHDA supply 1.5V/3.3V

NOTE:
If (G)MCH's HD Audio signals are connected to ICH9M for iHDMI, VCCHDA and VCCSUSHDA on ICH9M should be only on 1.5V. These power pins on ICH9M can be supplied with 3.3V if and only if (G)MCH's HDA is not connected to ICH9M. Consequently, only 1.5V audio/modem codecs can be used on the platform.

GMCH (CANTIGA)

Quanta Computer Inc.
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	GMCH DMI	1A

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IV@

EV@

SP@

IV&EV Dis/Enable setting

If LVDS no use,all signal can NC

U25C

(23) L_BKLT_CTRL
(23) INT_LVDS_BLON
R154 IV@10K_4 L_CTRL_CLK
+3V
R148 IV@10K_4 L_CTRL_DATA
(23) INT_LVDS_EDIDCLK
(23) INT_LVDS_EDIDDATA
(23) INT_LVDS_DIGON
R190 IV@2.4K/F_4 LVDS_IBG
R166 IV@0_4 LVDS_VREF
(23) INT_TXLCLKOUT-
(23) INT_TXLCLKOUT+
(23) INT_TXLOUT0-
(23) INT_TXLOUT1-
(23) INT_TXLOUT2-
(23) INT_TXLOUT0+
(23) INT_TXLOUT1+
(23) INT_TXLOUT2+

L32 L_BKLT_CTRL
G32 L_BKLT_EN
M32 L_CTRL_CLK
M33 L_CTRL_DATA
K33 L_DDC_CLK
J33 L_DDC_DATA
M29 L_VDD_EN
C44 LVDS_IBG
B43 LVDS_VBG
E37 LVDS_VREFH
E38 LVDS_VREFL
C41 LVDSA_CLK#
C40 LVDSA_CLK
B37 LVDSB_CLK#
A37 LVDSB_CLK
H47 LVDSA_DATA#_0
E46 LVDSA_DATA#_1
G40 LVDSA_DATA#_2
A40 LVDSA_DATA#_3
H48 LVDSA_DATA_0
D45 LVDSA_DATA_1
F40 LVDSA_DATA_2
B40 LVDSA_DATA_3
A41 LVDSB_DATA#_0
H38 LVDSB_DATA#_1
G37 LVDSB_DATA#_2
J37 LVDSB_DATA#_3
B42 LVDSB_DATA_0
G38 LVDSB_DATA_1
F37 LVDSB_DATA_2
K37 LVDSB_DATA_3

LVDS

SP@ TV_A/B/C
For IV: 75ohm
For EV:0ohm

R174 SP@75_4 INT_TV_COMP F25
R161 SP@75_4 INT_TV_Y/G H25
R158 SP@75_4 INT_TV_C/R K25
H24 TV_RTN
C31 TV_DCONSEL_0
E32 TV_DCONSEL_1

TVA_DAC
TVB_DAC
TVC_DAC

(23) INT_CRT_BLU INT_CRT_BLU E28
(23) INT_CRT_GRN INT_CRT_GRN G28
(23) INT_CRT_RED INT_CRT_RED J28
G29 CRT_IRTN
H32 CRT_DDC_CLK
J32 CRT_DDC_DATA
J29 CRT_HSYNC
E29 CRT_TVO_IREF
L29 CRT_VSYNC

(23) INT_CRT_DDCCLK
(23) INT_CRT_DDCDAT
(23) INT_HSYNC
R192 IV@30.1_4 HSYNC_G
CRTIREF
(23) INT_VSYNC
R193 IV@30.1_4 VSYNC_G

VGA

HSYNC/VSYNC serial R place close to NB

MXM STUFFED. (CRT)

HSYNC_G
VSYNC_G
R188 EV@0_4
R189 EV@0_4

CRTIREF pull down
for IV cantiga 1.02k ohm/F

CANTIGA_GM45

L<0.5" , If PCIE not support
still connect to +VCC_PEG

+1.05V
T37 EXP_A_COMPX R125 49.9/F_4
T36

PEG_COMPI
PEG_COMPO

PEG_RX#_0 H44 PEG_RXN0
PEG_RX#_1 J46 PEG_RXN1
PEG_RX#_2 L44 PEG_RXN2
PEG_RX#_3 L40 PEG_RXN3
PEG_RX#_4 N41 PEG_RXN4
PEG_RX#_5 P48 PEG_RXN5
PEG_RX#_6 N44 PEG_RXN6
PEG_RX#_7 T43 PEG_RXN7
PEG_RX#_8 U43 PEG_RXN8
PEG_RX#_9 Y43 PEG_RXN9
PEG_RX#_10 Y48 PEG_RXN10
PEG_RX#_11 Y36 PEG_RXN11
PEG_RX#_12 AA43 PEG_RXN12
PEG_RX#_13 AD37 PEG_RXN13
PEG_RX#_14 AC47 PEG_RXN14
PEG_RX#_15 AD39 PEG_RXN15

PEG_RXN[15:0] (17)

PEG_RX_0 H43 PEG_RXP0
PEG_RX_1 J44 PEG_RXP1
PEG_RX_2 L43 PEG_RXP2
PEG_RX_3 L41 PEG_RXP3
PEG_RX_4 N40 PEG_RXP4
PEG_RX_5 P47 PEG_RXP5
PEG_RX_6 N43 PEG_RXP6
PEG_RX_7 T42 PEG_RXP7
PEG_RX_8 U42 PEG_RXP8
PEG_RX_9 Y42 PEG_RXP9
PEG_RX_10 W47 PEG_RXP10
PEG_RX_11 Y37 PEG_RXP11
PEG_RX_12 AA42 PEG_RXP12
PEG_RX_13 AD36 PEG_RXP13
PEG_RX_14 AC48 PEG_RXP14
PEG_RX_15 AD40 PEG_RXP15

PEG_RXP[15:0] (17)

Can support reversal routing.If CFG9=1, PCI Express is normal operation. If CFG9=0, then PEG_TXP0 becomes PEG_TXP15, PEG_TXP1 becomes PEG_TXP14, PEG_TXP2 becomes PEG_TXP13, etc. similarly for PEG_RXP[15:0] and PEG_RXN[15:0]

PCI-EXPRESS GRAPHICS

PEG_TX#_0	J41	C_PEG_TXN0	C347	.1u/10V_4	PEG_TXN0
PEG_TX#_1	M46	C_PEG_TXN1	C670	.1u/10V_4	PEG_TXN1
PEG_TX#_2	M47	C_PEG_TXN2	C674	.1u/10V_4	PEG_TXN2
PEG_TX#_3	M40	C_PEG_TXN3	C350	.1u/10V_4	PEG_TXN3
PEG_TX#_4	M42	C_PEG_TXN4	C334	EV@.1U/10V_4	PEG_TXN4
PEG_TX#_5	R48	C_PEG_TXN5	C646	EV@.1U/10V_4	PEG_TXN5
PEG_TX#_6	N38	C_PEG_TXN6	C353	EV@.1U/10V_4	PEG_TXN6
PEG_TX#_7	T40	C_PEG_TXN7	C650	EV@.1U/10V_4	PEG_TXN7
PEG_TX#_8	U37	C_PEG_TXN8	C636	EV@.1U/10V_4	PEG_TXN8
PEG_TX#_9	U40	C_PEG_TXN9	C309	EV@.1U/10V_4	PEG_TXN9
PEG_TX#_10	Y40	C_PEG_TXN10	C280	EV@.1U/10V_4	PEG_TXN10
PEG_TX#_11	AA46	C_PEG_TXN11	C625	EV@.1U/10V_4	PEG_TXN11
PEG_TX#_12	AA37	C_PEG_TXN12	C250	EV@.1U/10V_4	PEG_TXN12
PEG_TX#_13	AA40	C_PEG_TXN13	C234	EV@.1U/10V_4	PEG_TXN13
PEG_TX#_14	AD43	C_PEG_TXN14	C212	EV@.1U/10V_4	PEG_TXN14
PEG_TX#_15	AC46	C_PEG_TXN15	C618	EV@.1U/10V_4	PEG_TXN15

PEG_TXN[15:0] (17,23)

PEG_TX_0	J42	C_PEG_TXP0	C348	.1u/10V_4	PEG_TXP0
PEG_TX_1	L46	C_PEG_TXP1	C669	.1u/10V_4	PEG_TXP1
PEG_TX_2	M48	C_PEG_TXP2	C673	.1u/10V_4	PEG_TXP2
PEG_TX_3	M39	C_PEG_TXP3	C349	.1u/10V_4	PEG_TXP3
PEG_TX_4	M43	C_PEG_TXP4	C333	EV@.1U/10V_4	PEG_TXP4
PEG_TX_5	R47	C_PEG_TXP5	C645	EV@.1U/10V_4	PEG_TXP5
PEG_TX_6	N37	C_PEG_TXP6	C352	EV@.1U/10V_4	PEG_TXP6
PEG_TX_7	T39	C_PEG_TXP7	C651	EV@.1U/10V_4	PEG_TXP7
PEG_TX_8	U36	C_PEG_TXP8	C637	EV@.1U/10V_4	PEG_TXP8
PEG_TX_9	U39	C_PEG_TXP9	C311	EV@.1U/10V_4	PEG_TXP9
PEG_TX_10	Y39	C_PEG_TXP10	C270	EV@.1U/10V_4	PEG_TXP10
PEG_TX_11	Y46	C_PEG_TXP11	C628	EV@.1U/10V_4	PEG_TXP11
PEG_TX_12	AA36	C_PEG_TXP12	C257	EV@.1U/10V_4	PEG_TXP12
PEG_TX_13	AA39	C_PEG_TXP13	C249	EV@.1U/10V_4	PEG_TXP13
PEG_TX_14	AD42	C_PEG_TXP14	C199	EV@.1U/10V_4	PEG_TXP14
PEG_TX_15	AD46	C_PEG_TXP15	C617	EV@.1U/10V_4	PEG_TXP15

PEG_TXP[15:0] (17,23)

IV&EV Dis/Enable setting

<5/31>Montevina_Schematics_Checklist_Rev0_8
a)For TVOUT Disabled, TV_DCONSEL[1:0] Connect to GND. But design guide Rev0.7 show NC.What is correct.
b)For CRT DAC Disable, CRT_DDC_CLK, CRT_DDC_DATA . CRT_HSYNC, CRT_VSYNCThese signals should be connected to GND. But design guide Rev0.7 show NC, Intel suggest follow Design guide.

<check list>	<check list>
For EV@	For IV@
CRT R/G/B 0ohm to GND	CRT R/G/B 150ohm to GND
CRTIREF 0ohm to GND	CRTIREF 1.02Kohm to GND

CRTIREF
For IV: 1.02Kohm
For EV:0ohm
R186 SP@1.02K/F_4 CRTIREF

SP@

CRT_R/G/B
For IV: 150ohm
For EV:0ohm
R185 SP@150/F_4 INT_CRT_BLU
R173 SP@150/F_4 INT_CRT_GRN
R164 SP@150/F_4 INT_CRT_RED

Quanta Computer Inc.
PROJECT : Z06

Size	Document Number	Rev
	GMCH VGA	1A
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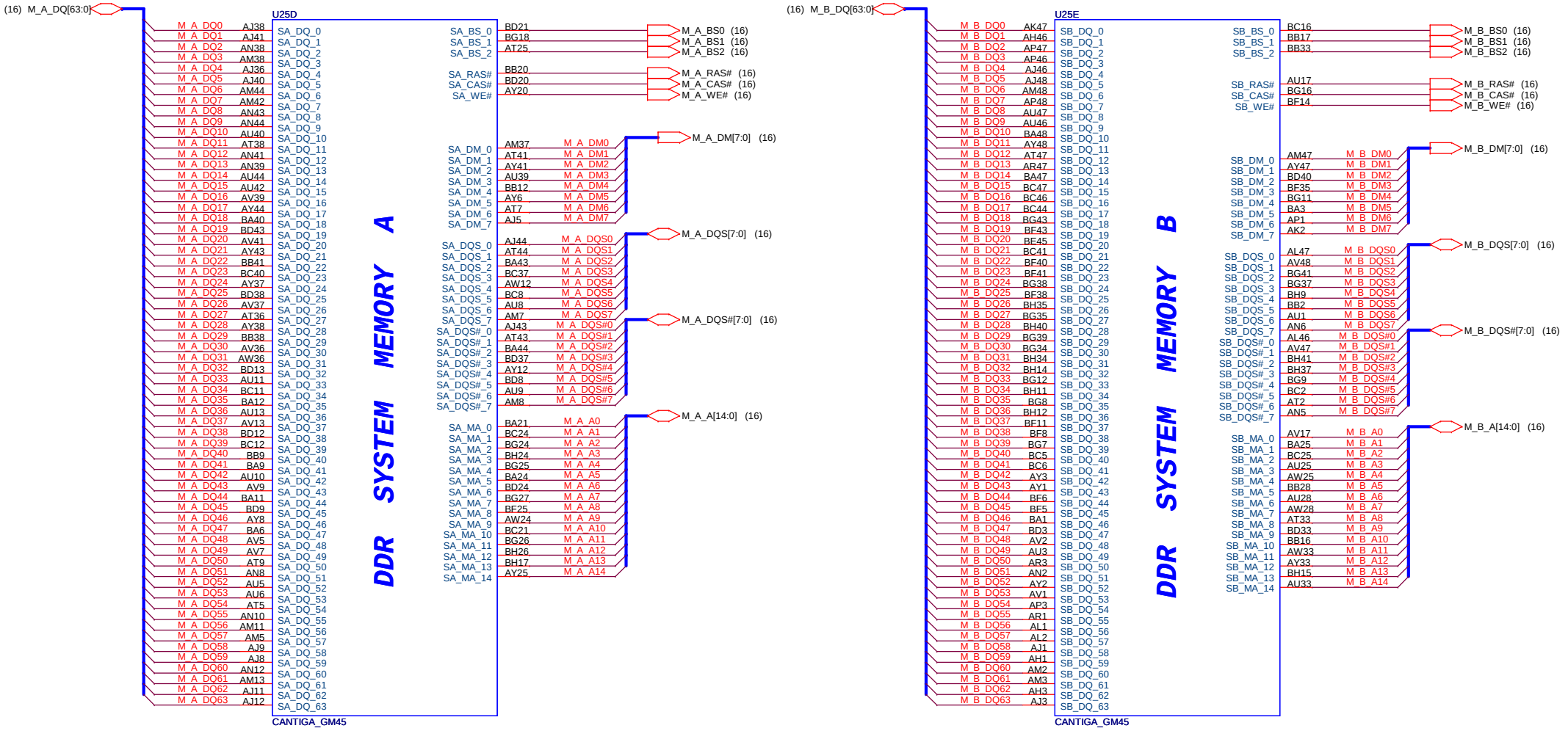

GMCH (CANTIGA)

Quanta Computer Inc.

PROJECT : Z06

Size	Document Number	Rev
	GMCH DDRII	1A

Date: Thursday, March 12, 2009 Sheet 8 of 39

IV@

SP@

Power consumption reference to Intel
644135 Cantiga chipset EDS Volume1.
Section 10

GM_TDP 10.5~12W
GS_TDP 7~8W
PM_TDP 7W

Intel check list(Rev 0.8)
No description for VCC_SM bulk CAP
Intel CRB(Rev 0.7)
330U*1 Reserve near to power
330U*1 near to NB

Intel check list(Rev 0.8)
270U*1 near to power(+V1.05M).
270U*2 near to NB
Intel CRB(Rev 0.7)
270U*3 near to power(+V1.05M).
270U*1 near to NB
ESR=12m ohm

+1.8VSUS

C81 22u_8 | C82 22u_8 | C158 .1u/10V_4 | C86 330u/2V_7343

U25G

VCC_SM(1.8V)
DDR2(800M)
3000mA_S0 , 1mA_S3
DDR2(667M) : 2600mA_S0
DDR3(1067M) : 4140mA_S0

VCC_SM_1 … VCC_SM_42 / VCC_SM_36/NC … VCC_SM_42/NC — **VCC SM POWER**

+1.05V_AXG

VCC_AXG_NCTF_1 … VCC_AXG_NCTF_60 — **VCC GFX NCTF**

1.05V
Graphics core
VCC_AXG
VCC_AXG_NCTF
6326.84mA

Voltage regulator is shared between
the Graphics Core Rail,
VCCA_HPLL,VCCA_MPLL,VCCA_PEG_PLL,VCCD_PEG_PLL,
VCCA_SM_CK, VCCA_DPLLA, VCCA_DPLLB, VCCD_HPLL,
VCCA_SM, VCC_AXF

VCC_AXG_1 … VCC_AXG_42 — **VCC GFX**

VCC_AXG_SENSE / VSS_AXG_SENSE

+1.05V_AXG — IV@ — R103 IV@10/F_4 | R111 IV@10/F_4

1. Route VCC_AXG_SENSE and VSS_AXG_SENSE differentially
2. VCC_AXG_SENSE PU to +VGFX_CORE_INT with 10ohm
and VSS_AXG_SENSE PD with 10ohm for Intel suggest

CANTIGA_GM45

+1.05V — IV@ — R128 IV@0_8 | R130 IV@0_8 | R129 IV@0_8

IV&EV Dis/Enable setting
Design guide(Table 72)
For INT VGA diasble.VCC_AXG power can connect to GND

+1.05V_AXG — C622 IV@330u/2V_7343 | C621 IV@330u/2V_7343 | C228 IV@.47u/6.3V_4 | SP@ C159 SP@1u_6 | C223 IV@10u_8 | C272 IV@22u_8 | C267 IV@.1u_4 | C261 IV@.1u_4 | C273 IV@.1u_4

Place close to the GMCH

SP@:IV Sutff 1uf
EVstuff 0 ohm

Cavity Capacitors

Intel check list(Rev 0.8)
220U*2 near to NB(ESR=15m ohm)
Intel CRB(Rev 0.7)
270U*4 near to power(+V1.05S).
330U*2 near to NB

1.8V
Internal connect to power

VCC_SM_LF1 … VCC_SM_LF7 — **VCC SM LF**

C118 .1u/10V_4 | C176 .1u/10V_4 | C121 .22u/6.3V_4 | C127 .22u/6.3V_4 | C178 .47u/6.3V_4 | C113 1u_4 | C128 1u_4

+1.05V — C192 .1u/10V_4 | C218 .22u/6.3V_4 | C181 .22u/6.3V_4 | C260 22u_8 | C616 330u/2V_7343

Place close to the GMCH

U25F

VCC_1 … VCC_35 — **VCC CORE POWER**

+1.05V

VCC_NCTF_1 … VCC_NCTF_44 — **VCC NCTF**

CANTIGA_GM45

VCC
VCC_NCTF
1210.34mA_EV
1930.4mA_IV
ME Engine
508.12mA
Total Max=2438.52mA

NB Power Status and max current table(1/3)

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCC(EXT_VGA)	O	X	X	+1.05V	2178mA	
VCC(INT_VGA)	O	X	X	+1.05V	2899mA	
VCC_AXG	O	X	X	+1.05V	8700mA	Graphics Core
VCC_SM(800)	O	O	X	+1.8VSUS	3A	(DDRII-667) 2.6A
VCC_SM(Standby)	O	O	X	+1.8VSUS	1mA	Self Refresh during S3

(See NB EDS Rev:1.0 Section 10.1 for max current)
(See NB EDS Rev:1.0 Section 12.2 for DC voltage)

GMCH (CANTIGA)

Quanta Computer Inc.
PROJECT : Z06

Size	Document Number	Rev
	GMCH VCC,NCTF	1A

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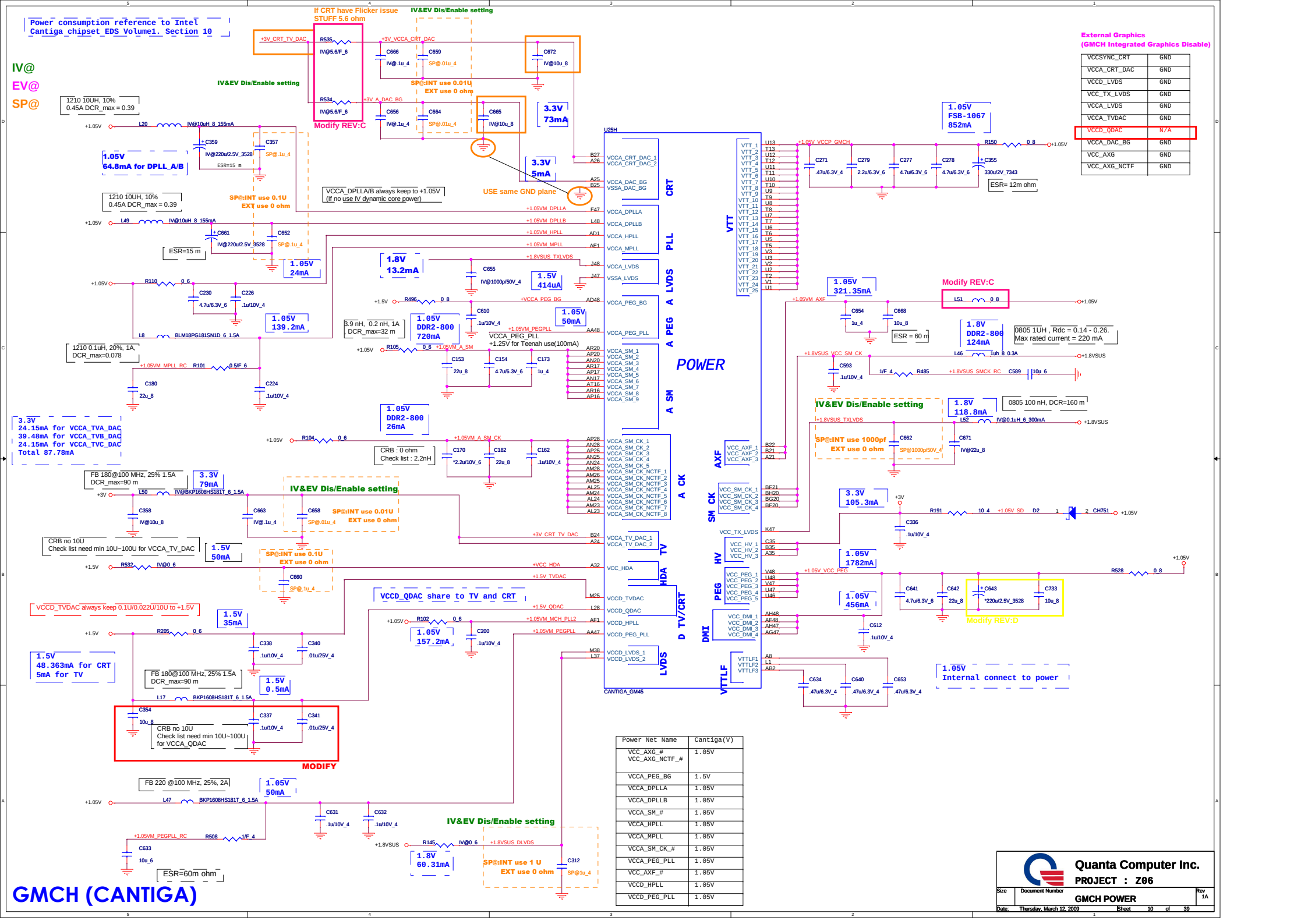
Power consumption reference to Intel Cantiga chipset EDS Volume1. Section 10
IV@
EV@
SP@
If CRT have Flicker issue
STUFF 5.6 ohm
IV&EV Dis/Enable setting
Modify REV:C
SP@:INT use 0.01U
EXT use 0 ohm
3.3V
73mA
3.3V
5mA
USE same GND plane
VCCA_DPLLA/B always keep to +1.05V
(If no use IV dynamic core power)
SP@:INT use 0.1U
EXT use 0 ohm
1.05V
64.8mA for DPLL_A/B
1.05V
24mA
1.8V
13.2mA
1.5V
414uA
1.05V
DDR2-800
720mA
1.05V
50mA
1.05V
139.2mA
1.05V
DDR2-800
26mA
3.3V
24.15mA for VCCA_TVA_DAC
39.48mA for VCCA_TVB_DAC
24.15mA for VCCA_TVC_DAC
Total 87.78mA
CRB : 0 ohm
Check list : 2.2nH
3.3V
79mA
CRB no 10U
Check list need min 10U~100U for VCCA_TV_DAC
1.5V
50mA
VCCD_TVDAC always keep 0.1U/0.022U/10U to +1.5V
1.5V
35mA
VCCD_QDAC share to TV and CRT
1.05V
157.2mA
1.5V
48.363mA for CRT
5mA for TV
1.5V
0.5mA
CRB no 10U
Check list need min 10U~100U
for VCCA_QDAC
MODIFY
FB 220 @100 MHz, 25%, 2A
1.05V
50mA
ESR=60m ohm
1.8V
60.31mA
SP@:INT use 1 U
EXT use 0 ohm
POWER
CRT
PLL
A LVDS
A PEG
A SM
A CK
TV
HDA
D TV/CRT
LVDS
VTT
AXF
SM CK
HV
PEG
DMI
VTTLF
CANTIGA_GM45
1.05V
FSB-1067
852mA
ESR= 12m ohm
1.05V
321.35mA
Modify REV:C
ESR = 60 m
1.8V
DDR2-800
124mA
0805 1UH , Rdc = 0.14 - 0.26.
Max rated current = 220 mA
0805 100 nH, DCR=160 m
1.8V
118.8mA
SP@:INT use 1000pf
EXT use 0 ohm
3.3V
105.3mA
1.05V
1782mA
1.05V
456mA
Modify REV:D
1.05V
Internal connect to power
External Graphics
(GMCH Integrated Graphics Disable)
VCCSYNC_CRT GND
VCCA_CRT_DAC GND
VCCD_LVDS GND
VCC_TX_LVDS GND
VCCA_LVDS GND
VCCA_TVDAC GND
VCCD_QDAC N/A
VCCA_DAC_BG GND
VCC_AXG GND
VCC_AXG_NCTF GND
Power Net Name | Cantiga(V)
VCC_AXG_# VCC_AXG_NCTF_# | 1.05V
VCCA_PEG_BG | 1.5V
VCCA_DPLLA | 1.05V
VCCA_DPLLB | 1.05V
VCCA_SM_# | 1.05V
VCCA_HPLL | 1.05V
VCCA_MPLL | 1.05V
VCCA_SM_CK_# | 1.05V
VCCA_PEG_PLL | 1.05V
VCC_AXF_# | 1.05V
VCCD_HPLL | 1.05V
VCCD_PEG_PLL | 1.05V
GMCH (CANTIGA)
Quanta Computer Inc.
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Size
Document Number
GMCH POWER
Rev 1A
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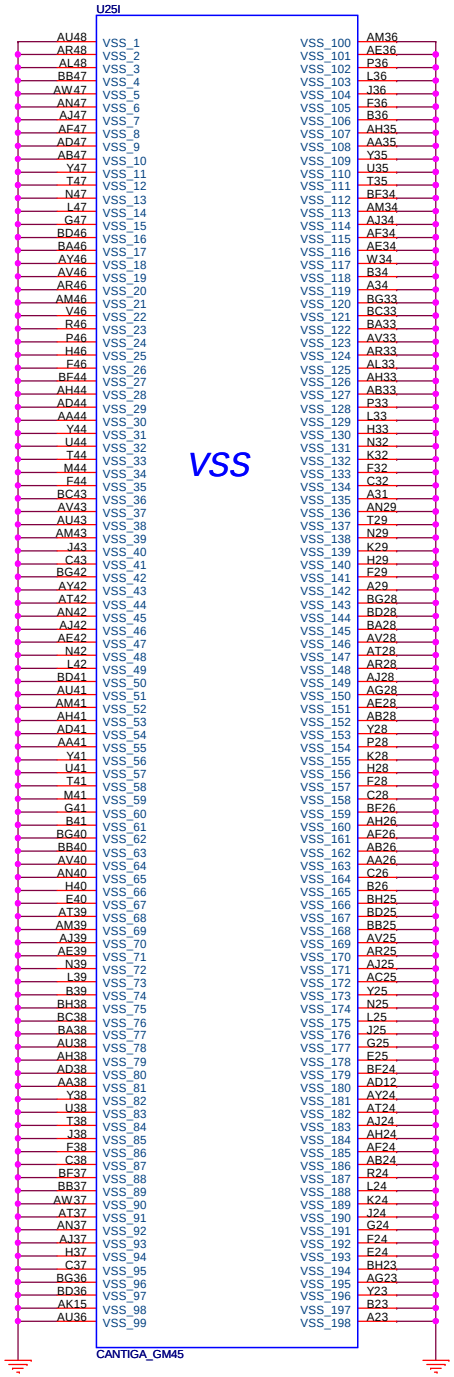

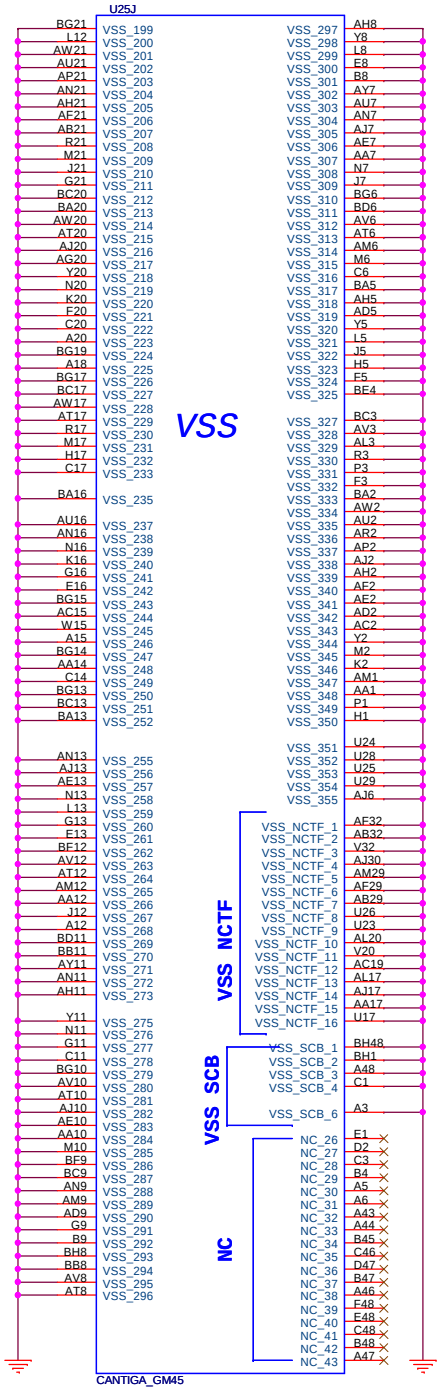

GMCH (CANTIGA)

Quanta Computer Inc.

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	GMCH VSS	1A
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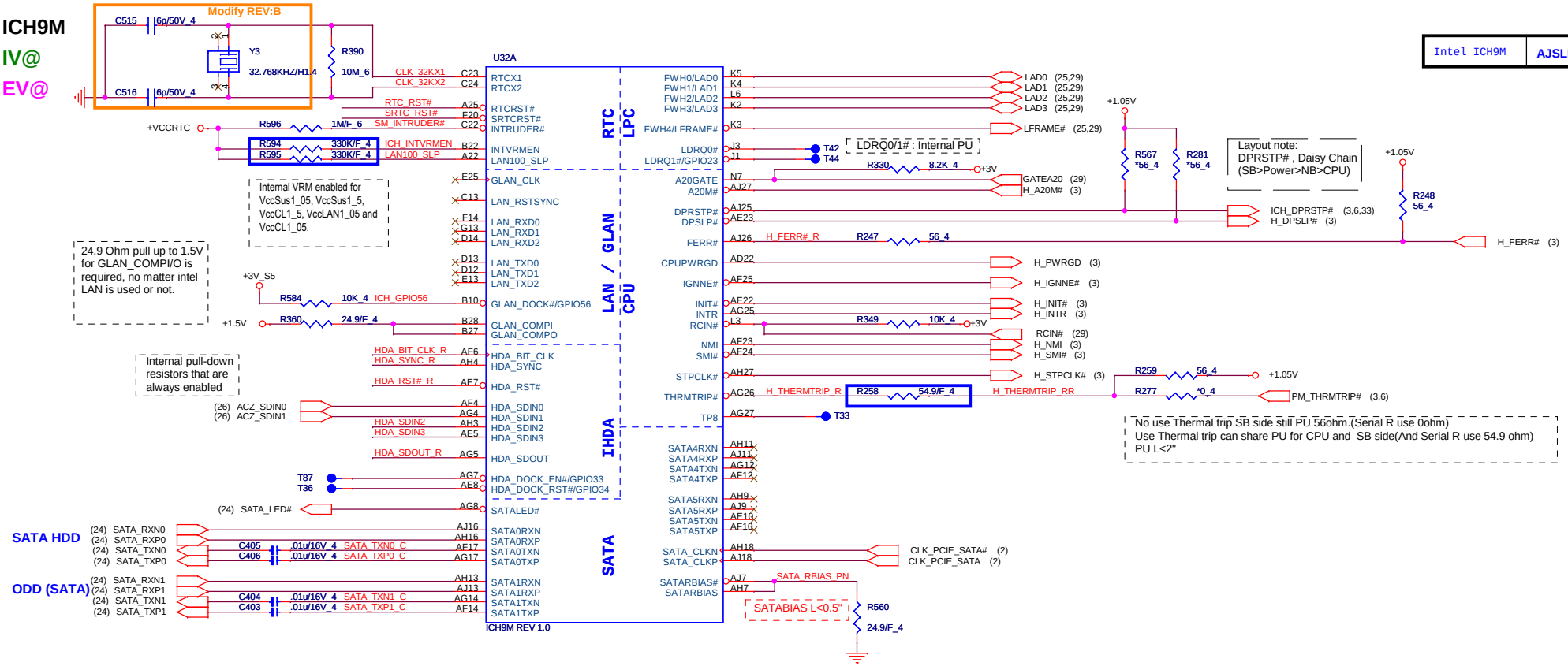
ICH9M

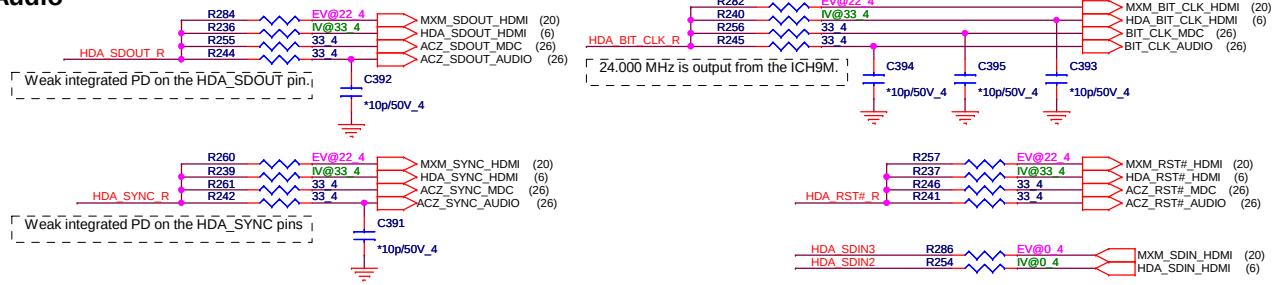
IV@

EV@

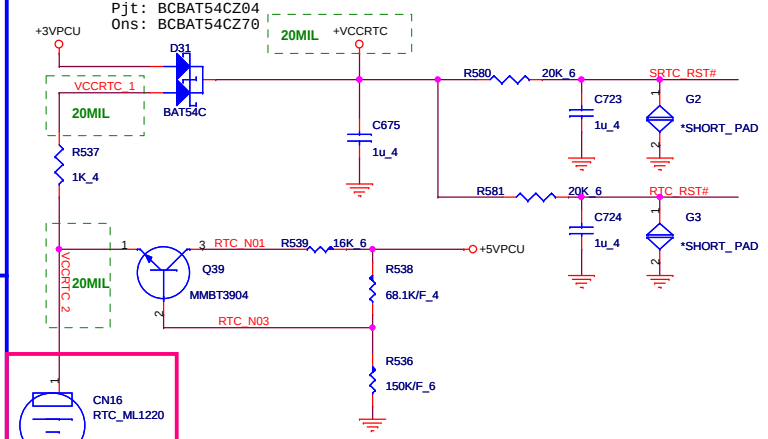
Intel ICH9M | AJSLB8Q0T03



HD Audio



RTC



South Bridge Strap Pin (1/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect	This strap should only be enabled in manufacturing environments using an external pull-up resistor.
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU	
TP3	XOR Chain Entrance	PWROK	(14) ICH_TP3 — ICH_TP3 R592 *1K_4	
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK	HDA_SDOUT_R R271 *1K_4 +3V	

ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1

Quanta Computer Inc.

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	ICH9M HOST	2A
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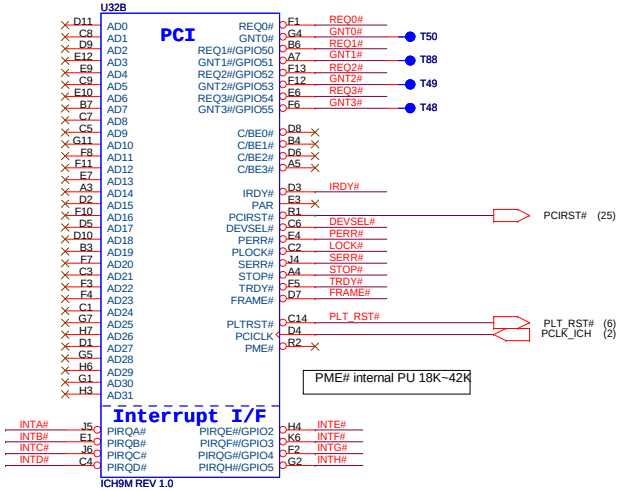
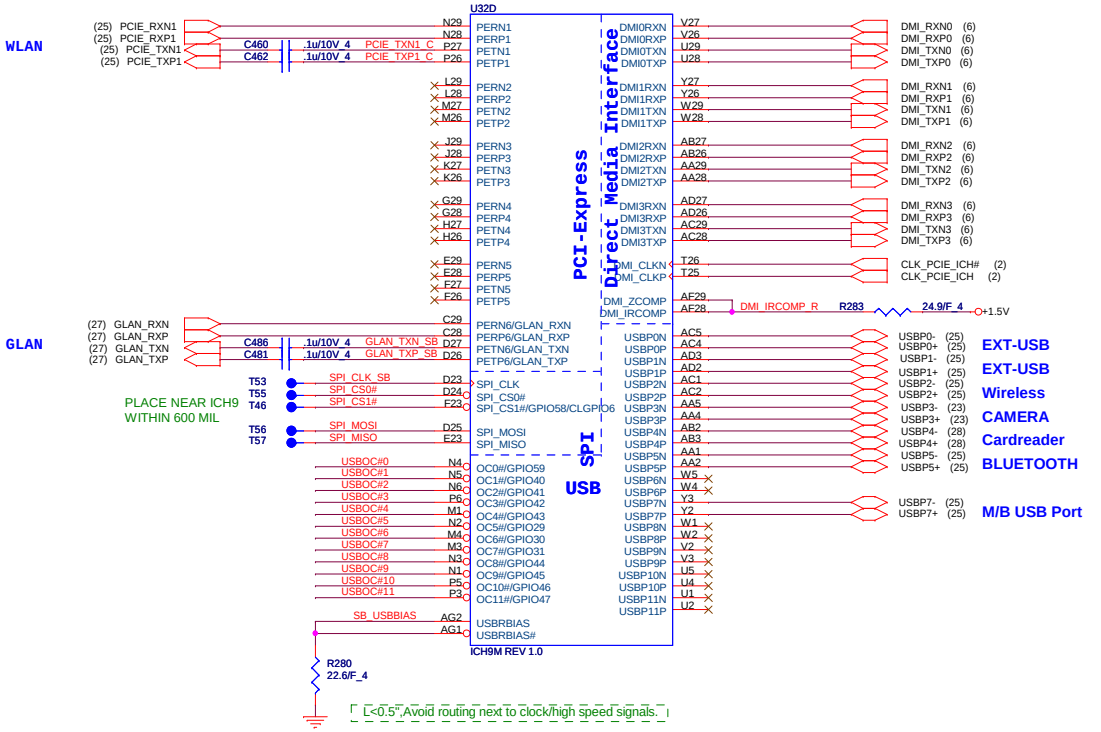
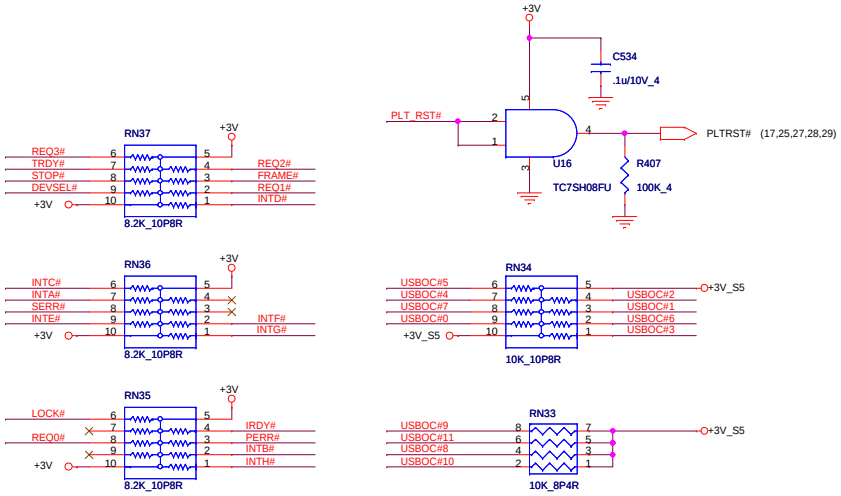
ICH9M

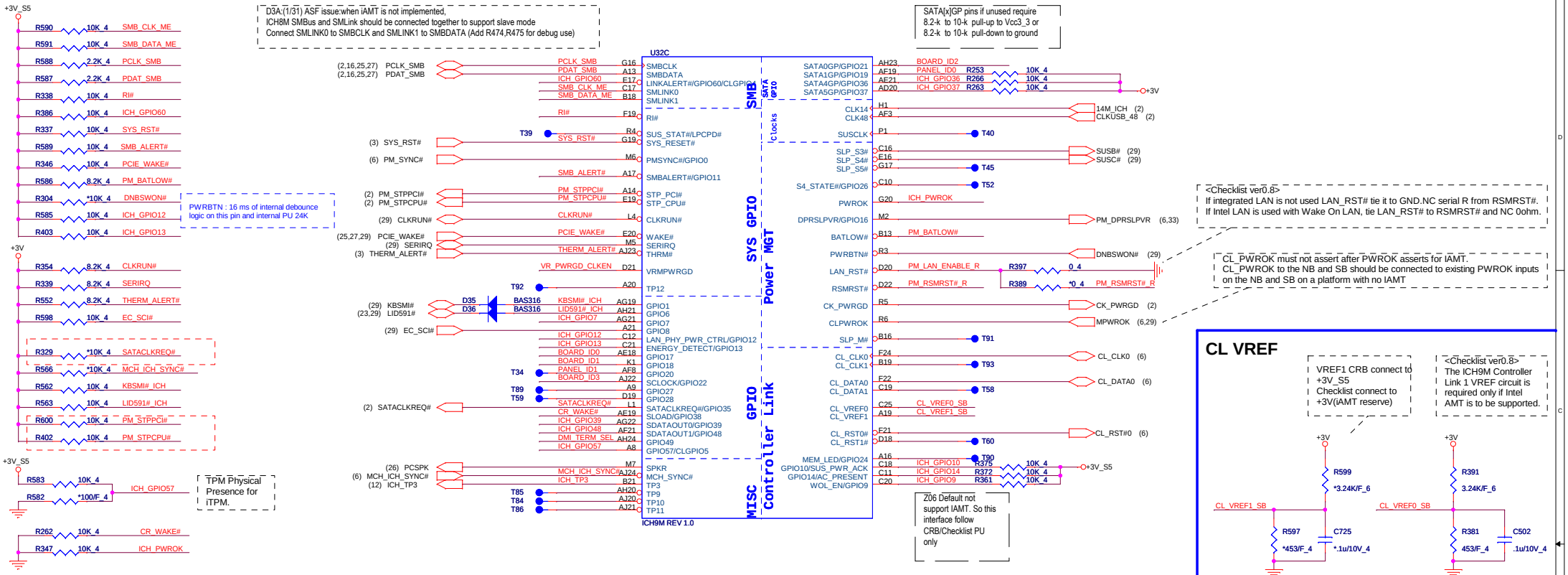






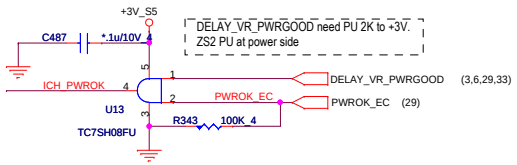
South Bridge Strap Pin (2/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0	
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default	
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default	GNT3# R369 *1K_4
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable	
GNT0#	Boot BIOS Selection 0	PWROK	PCI_GNT#0 / SPI_CS#1 / Boot Location 0 / 1 / SPI 1 / 0 / PCI 1 / 1 / **LPC(Default)**	GNT0# R353 *1K_4
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK		

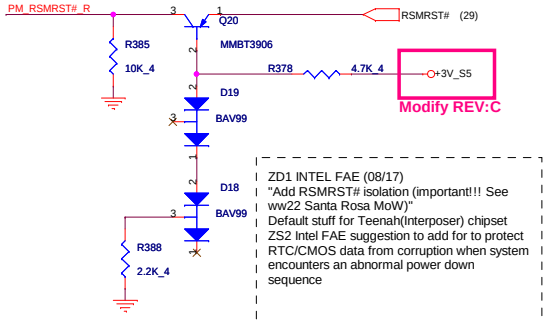


Follow CHECK LIST V1.5

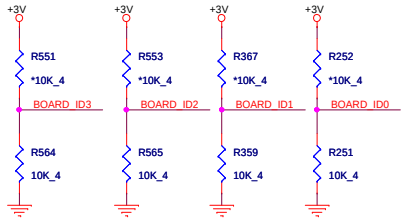
ICH PWROK



Resume RST



M/B ID

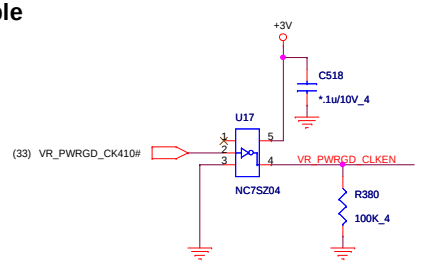


Board ID	ID3	ID2	ID1	ID0
default	0	0	0	0
	0	0	0	1
	0	0	1	0
	0	0	1	1
	0	1	0	0

South Bridge Strap Pin (3/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
SPKR	No Reboot	PWROK	0 = Default 1 = No Reboot mode	PCSPK R316 *1K_4 +3V
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	DMI_TERM_SEL R554 *1K_4

CLK Enable



Quanta Computer Inc.	
PROJECT : Z06	
Size	Document Number: ICH9M GPIO
Rev	1A
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ICH9M

IV@

EV@

Power consumption reference to Intel ICH9 Family EDS Rev 1.6

2~3.456v 3.6uA_G3

PER INTEL SUGGESTION: CHANGE TO 100OHM & 1UF

330 Ohms@ 100 MHz , 0805

5V 2mA

5V S0:2mA S3/4/5:1mA

1.5V 646mA

1.5V 47mA

1.5V 11mA

1.05V , Powered by VCC1_05 in S0

VCC1_5_A 1.5V 1342mA

3.3V S0:19mA S3/4/5:78mA

1.5V 23mA

1.5V 80mA

3.3V 1mA

1.05V 1634mA

1.5V 23mA

1.05V 48mA

1.05V 2mA

3.3V 308mA

3.3V S0:212mA S3/4/5:53mA

3.3V S0:19mA S3/4/5:73mA

1.5V / 3.3V 11mA

1.5V / 3.3V S0:11mA S3/4/5:1mA

500 mA, 20%

5 Ohms @ 100 MHz , 0.7A

VCCUS1_05 power by VCC1_05 in S0 / VCCSUS3_3 in S3/S4/S5

VCCUS1_5 power by VCC1_5_A in S0 / VCCSUS3_3 in S3/S4/S5

VCCCL1_05 power by VCC1_05_A in S0

VCCCL1_5 power by VCC1_5_A in S0

Impact ICH9M VCCHDA and VCCSUSHDA supply 1.5V/3.3V

Support INT HDMI HDA interface. These power only support 1.5V.Device must to meet.

NOTE:
If (G)MCH's HD Audio signals are connected to ICH9M for iHDMI, VCCHDA and VCCSUSHDA on ICH9M should be only on 1.5V. These power pins on ICH9M can be supplied with 3.3V if and only if (G)MCH's HDA is not connected to ICH9M. Consequently, only 1.5V audio/modem codecs can be used on the platform.

If use SB MAC for LAN function. And support wake up need connect to relation power.

If use SB MAC for LAN function. And support wake up need connect to relation power.

Modify REV:D

MODIFY

ICH9M REV 1.0

Quanta Computer Inc. PROJECT : Z06			
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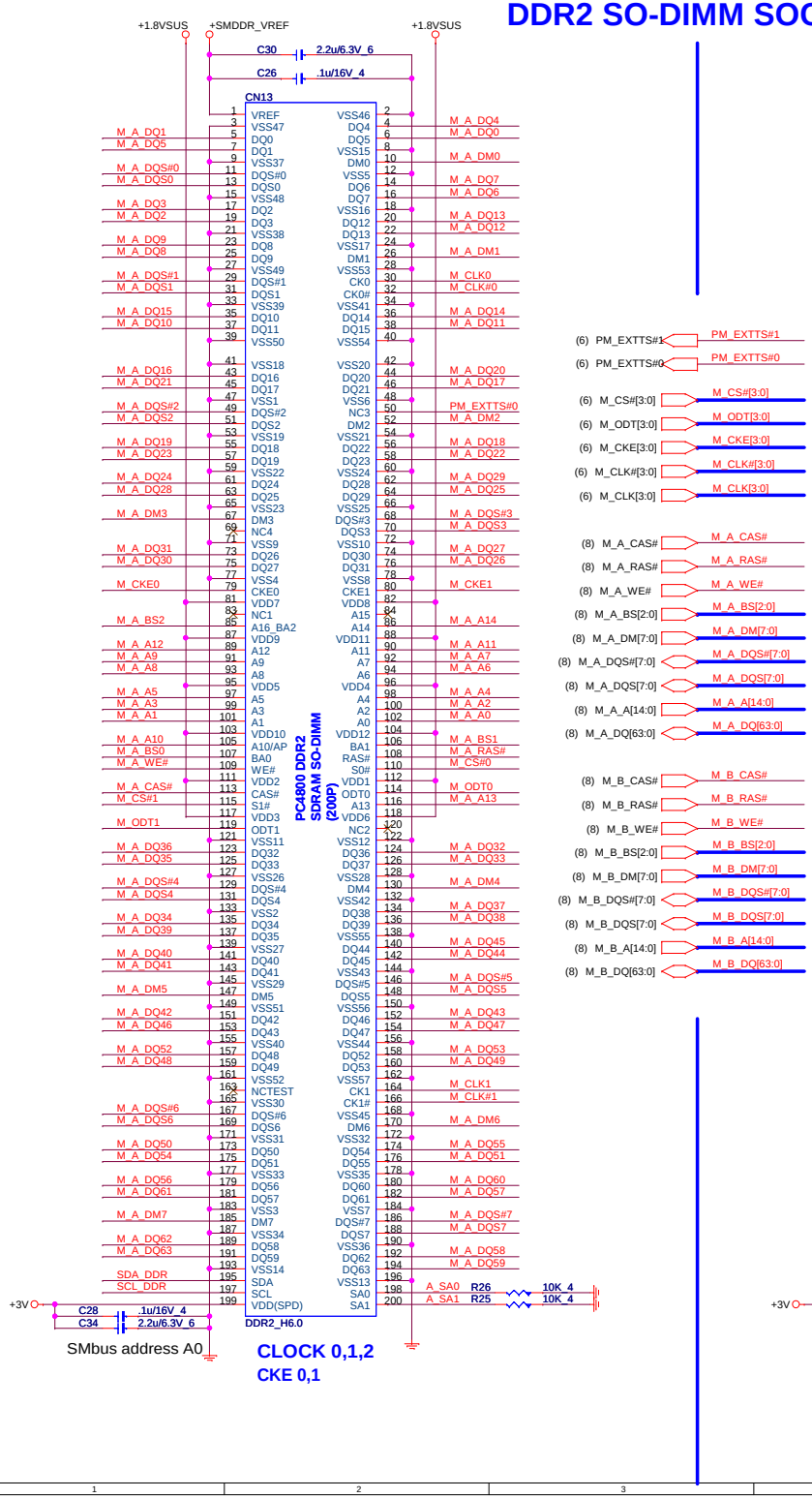
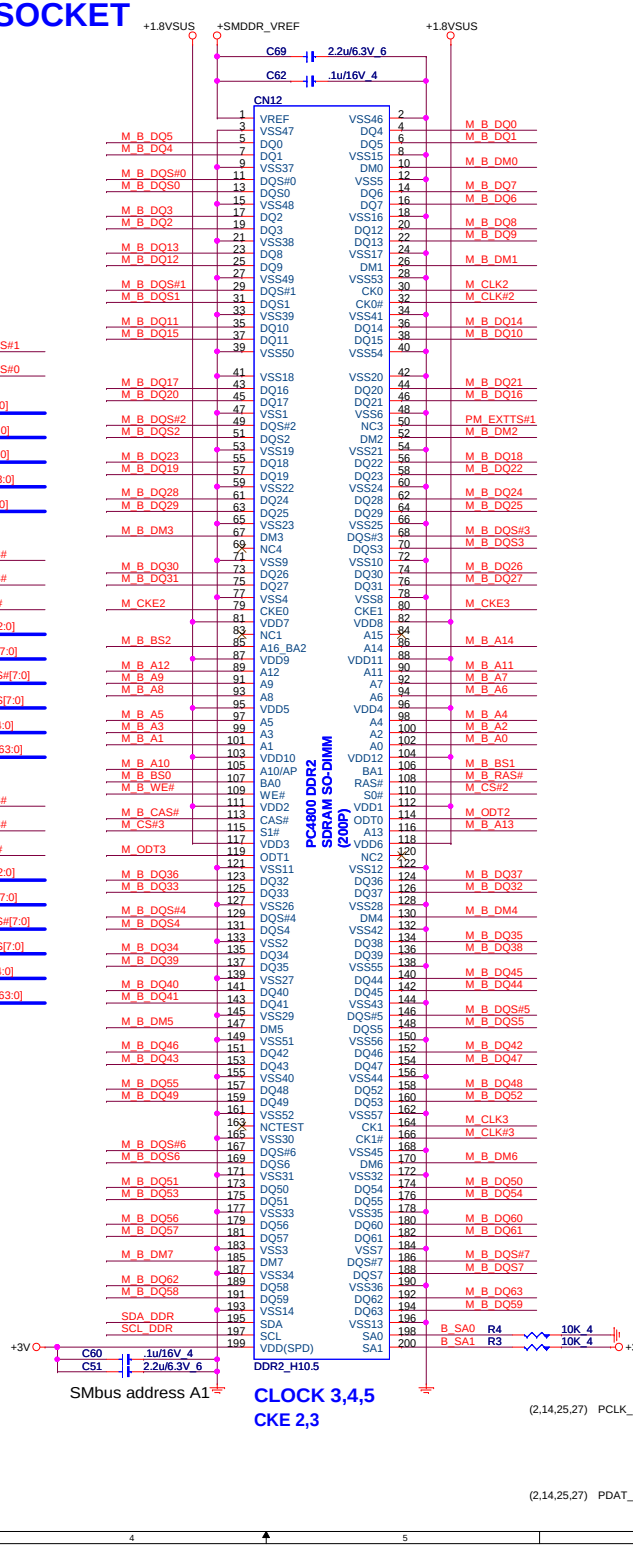
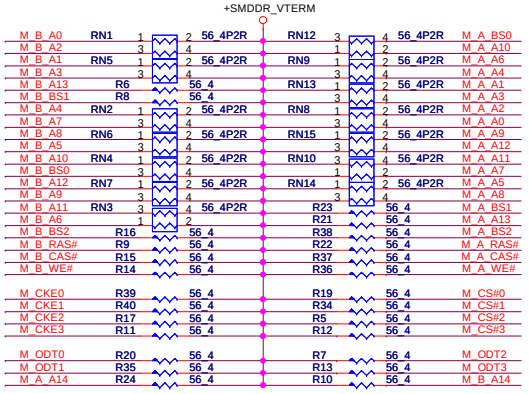
DDR2 SO-DIMM SOCKET

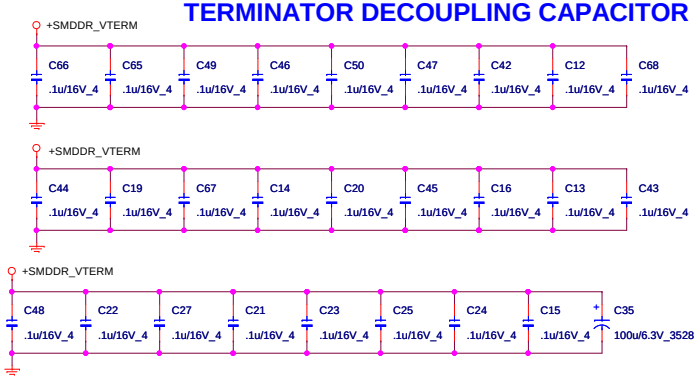




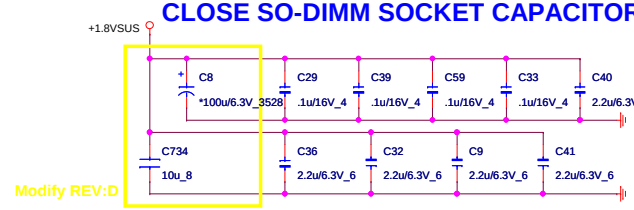
DDR2 TERMINATOR



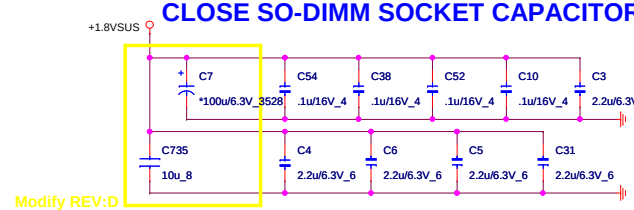
TERMINATOR DECOUPLING CAPACITOR

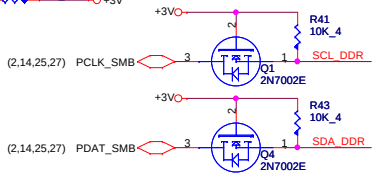


CLOSE SO-DIMM SOCKET CAPACITORS



CLOSE SO-DIMM SOCKET CAPACITORS





Quanta Computer Inc.

PROJECT : Z06

Size	Document Number	Rev
	DDRII SO-DIMM	1A

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(2,3,6,7,10,12,13,14,15,16,19,20,23,24,25,26,27,29,31,33,35,36) +3V
(18,19,35) +VGA1.1V

U23A
EV@N10M-GE1-B-U2/H

+VGA1.1V
~ 500mA
C238 EV@22U_8
C236 EV@4.7U/6.3V_6
C211 EV@1U/6.3V_4
C191 EV@1U/6.3V_4
C246 EV@.1U/10V_4
C210 EV@.1U/10V_4
C209 EV@.47U/6.3V_4

+VGA1.1V
1600mA
C667 EV@22U_8
C657 EV@4.7U/6.3V_6
C237 EV@1U/6.3V_4
C259 EV@.47U/6.3V_4
C232 EV@.47U/6.3V_4
C227 EV@.1U/10V_4

Near BGA

+3V
R70 EV@0_6
+PEX_VDD3
C100 EV@1U/6.3V_4
C104 EV@.1U/10V_4
C107 EV@.1U/10V_4

(35) VGA_SENSE
SI-2 4/10 For Nvidia recommend.
100mA
12~16 mils width

+VGA1.1V
L48 EV@MLG1608B10NJ_6
+PEX_PLLVDD
C255 EV@4.7U/6.3V_6
C649 EV@4.7U/6.3V_6
C215 EV@1U/6.3V_4
C216 EV@.1U/10V_4
C648 EV@.01U/16V/X7R_4

AK16 PEX_IOVDD_1
AK17 PEX_IOVDD_2
AK21 PEX_IOVDD_3
AK24 PEX_IOVDD_4
AK27 PEX_IOVDD_5

AG11 PEX_IOVDDQ_1
AG12 PEX_IOVDDQ_2
AG13 PEX_IOVDDQ_3
AG15 PEX_IOVDDQ_4
AG16 PEX_IOVDDQ_5
AG17 PEX_IOVDDQ_6
AG18 PEX_IOVDDQ_7
AG22 PEX_IOVDDQ_8
AG23 PEX_IOVDDQ_9
AG24 PEX_IOVDDQ_10
AG25 PEX_IOVDDQ_11
AG26 PEX_IOVDDQ_12
AJ14 PEX_IOVDDQ_13
AJ15 PEX_IOVDDQ_14
AJ19 PEX_IOVDDQ_15
AJ21 PEX_IOVDDQ_16
AJ22 PEX_IOVDDQ_17
AJ24 PEX_IOVDDQ_18
AJ25 PEX_IOVDDQ_19
AJ27 PEX_IOVDDQ_20
AK18 PEX_IOVDDQ_21
AK20 PEX_IOVDDQ_22
AK23 PEX_IOVDDQ_23
AK26 PEX_IOVDDQ_24
AL16 PEX_IOVDDQ_25

J10 VDD33_1
J11 VDD33_2
J12 VDD33_3
J13 VDD33_4
J9 VDD33_5

AD20 VDD_SENSE
AD19 GND_SENSE
AG14 PEX_PLLVDD
AG19 PEX_CAL_PD_VDDQ
AG20 PEX_CAL_PU_GND

A2 NC_1
AB7 NC_2
AD6 NC_3
AE6 NC_4
AG6 NC_5
AJ5 NC_6
AK15 NC_7
AL7 NC_8
D35 NC_9
E35 NC_10
E7 NC_11
F7 NC_12
H32 NC_13
M7 NC_14
P6 NC_15
P7 NC_16
R7 NC_17
U7 NC_18
V6 NC_19

PCI EXPRESS

PEX_RX0 AP17 PEG_TXP0_R RN42 3 4 EV@0_4P2R PEG_TXP0 (7,23)
PEX_RX0* AN17 PEG_TXN0_R 1 2 PEG_TXN0 (7,23)
PEX_RX1 AN19 PEG_TXP1_R RN41 3 4 EV@0_4P2R PEG_TXP1 (7,23)
PEX_RX1* AP19 PEG_TXN1_R 1 2 PEG_TXN1 (7,23)
PEX_RX2 AR19 PEG_TXP2_R RN40 3 4 EV@0_4P2R PEG_TXP2 (7,23)
PEX_RX2* AR20 PEG_TXN2_R 1 2 PEG_TXN2 (7,23)
PEX_RX3 AP20 PEG_TXP3_R RN39 3 4 EV@0_4P2R PEG_TXP3 (7,23)
PEX_RX3* AN20 PEG_TXN3_R 1 2 PEG_TXN3 (7,23)
PEX_RX4 AN22 PEG_TXP4 PEG_TXP4 (7)
PEX_RX4* AP22 PEG_TXN4 PEG_TXN4 (7)
PEX_RX5 AR22 PEG_TXP5 PEG_TXP5 (7)
PEX_RX5* AR23 PEG_TXN5 PEG_TXN5 (7)
PEX_RX6 AP23 PEG_TXP6 PEG_TXP6 (7)
PEX_RX6* AN23 PEG_TXN6 PEG_TXN6 (7)
PEX_RX7 AN25 PEG_TXP7 PEG_TXP7 (7)
PEX_RX7* AP25 PEG_TXN7 PEG_TXN7 (7)
PEX_RX8 AR25 PEG_TXP8 PEG_TXP8 (7)
PEX_RX8* AR26 PEG_TXN8 PEG_TXN8 (7)
PEX_RX9 AN26 PEG_TXP9 PEG_TXP9 (7)
PEX_RX9* AN28 PEG_TXN9 PEG_TXN9 (7)
PEX_RX10 AP28 PEG_TXP10 PEG_TXP10 (7)
PEX_RX10* AR28 PEG_TXN10 PEG_TXN10 (7)
PEX_RX11 AR29 PEG_TXP11 PEG_TXP11 (7)
PEX_RX11* AP29 PEG_TXN11 PEG_TXN11 (7)
PEX_RX12 AN29 PEG_TXP12 PEG_TXP12 (7)
PEX_RX12* AN31 PEG_TXN12 PEG_TXN12 (7)
PEX_RX13 AP31 PEG_TXP13 PEG_TXP13 (7)
PEX_RX13* AR31 PEG_TXN13 PEG_TXN13 (7)
PEX_RX14 AR32 PEG_TXP14 PEG_TXP14 (7)
PEX_RX14* AR34 PEG_TXN14 PEG_TXN14 (7)
PEX_RX15 AP34 PEG_TXP15 PEG_TXP15 (7)
PEX_RX15* PEG_TXN15 PEG_TXN15 (7)

PEX_TX0 AL17 C_PEG_RXP0 C307 EV@.1U/10V_4 PEG_RXP0 (7)
PEX_TX0* AM17 C_PEG_RXN0 C306 EV@.1U/10V_4 PEG_RXN0 (7)
PEX_TX1 AM18 C_PEG_RXP1 C320 EV@.1U/10V_4 PEG_RXP1 (7)
PEX_TX1* AM19 C_PEG_RXN1 C319 EV@.1U/10V_4 PEG_RXN1 (7)
PEX_TX2 AL19 C_PEG_RXP2 C330 EV@.1U/10V_4 PEG_RXP2 (7)
PEX_TX2* AK19 C_PEG_RXN2 C327 EV@.1U/10V_4 PEG_RXN2 (7)
PEX_TX3 AL20 C_PEG_RXP3 C305 EV@.1U/10V_4 PEG_RXP3 (7)
PEX_TX3* AM20 C_PEG_RXN3 C304 EV@.1U/10V_4 PEG_RXN3 (7)
PEX_TX4 AM21 C_PEG_RXP4 C318 EV@.1U/10V_4 PEG_RXP4 (7)
PEX_TX4* AM22 C_PEG_RXN4 C317 EV@.1U/10V_4 PEG_RXN4 (7)
PEX_TX5 AL22 C_PEG_RXP5 C332 EV@.1U/10V_4 PEG_RXP5 (7)
PEX_TX5* AK22 C_PEG_RXN5 C331 EV@.1U/10V_4 PEG_RXN5 (7)
PEX_TX6 AL23 C_PEG_RXP6 C302 EV@.1U/10V_4 PEG_RXP6 (7)
PEX_TX6* AM23 C_PEG_RXN6 C303 EV@.1U/10V_4 PEG_RXN6 (7)
PEX_TX7 AM24 C_PEG_RXP7 C315 EV@.1U/10V_4 PEG_RXP7 (7)
PEX_TX7* AM25 C_PEG_RXN7 C316 EV@.1U/10V_4 PEG_RXN7 (7)
PEX_TX8 AL25 C_PEG_RXP8 C301 EV@.1U/10V_4 PEG_RXP8 (7)
PEX_TX8* AK25 C_PEG_RXN8 C300 EV@.1U/10V_4 PEG_RXN8 (7)
PEX_TX9 AL26 C_PEG_RXP9 C329 EV@.1U/10V_4 PEG_RXP9 (7)
PEX_TX9* AM26 C_PEG_RXN9 C328 EV@.1U/10V_4 PEG_RXN9 (7)
PEX_TX10 AM27 C_PEG_RXP10 C314 EV@.1U/10V_4 PEG_RXP10 (7)
PEX_TX10* AM28 C_PEG_RXN10 C313 EV@.1U/10V_4 PEG_RXN10 (7)
PEX_TX11 AL28 C_PEG_RXP11 C299 EV@.1U/10V_4 PEG_RXP11 (7)
PEX_TX11* AK28 C_PEG_RXN11 C298 EV@.1U/10V_4 PEG_RXN11 (7)
PEX_TX12 AK29 C_PEG_RXP12 C326 EV@.1U/10V_4 PEG_RXP12 (7)
PEX_TX12* AL29 C_PEG_RXN12 C325 EV@.1U/10V_4 PEG_RXN12 (7)
PEX_TX13 AM29 C_PEG_RXP13 C297 EV@.1U/10V_4 PEG_RXP13 (7)
PEX_TX13* AM30 C_PEG_RXN13 C296 EV@.1U/10V_4 PEG_RXN13 (7)
PEX_TX14 AM31 C_PEG_RXP14 C293 EV@.1U/10V_4 PEG_RXP14 (7)
PEX_TX14* AM32 C_PEG_RXN14 C292 EV@.1U/10V_4 PEG_RXN14 (7)
PEX_TX15 AN32 C_PEG_RXP15 C295 EV@.1U/10V_4 PEG_RXP15 (7)
PEX_TX15* AP32 C_PEG_RXN15 C294 EV@.1U/10V_4 PEG_RXN15 (7)

PEX_REFCLK AR16 CLK_MXM CLK_MXM (2)
PEX_REFCLK* AR17 CLK_MXM# CLK_MXM# (2)

PEX_TSTCLK_OUT AJ17 R114 *200_4
PEX_TSTCLK_OUT* AJ18

PEX_RST* AM16 VGA_RST#
PEX_CLKREQ* AR13 PEX_CLKREQ# T82
PEX_TERMP AG21 PEX_TERMP R109 EV@2.49K/F_4
TESTMODE AP35 TESTMODE R168 EV@10K/F_4

D30
1 2 PLTRST# PLTRST# (13,25,27,28,29)
*BAS316
R519 *100K/F_4
R525 EV@0_4

FOR UMA iHDMI HPD
PEG_RXP3 R175 IV@0_4 HDMI_HP_IV# (23)

Quanta Computer Inc.
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U23B
EV@N10M-GE1-B-U2/H

MEMORY I/F A

(22) VMA_MA3 (22) VMA_MA0 (22) VMA_MA2 (22) VMA_MA1 (22) VMA_MA3H (22) VMA_MA4H (22) VMA_MA5H
(22) VMA_CS0# (22) VMA_WE# (22) VMA_BA0 (22) VMA_CKE (22) VMA_ODT (22) VMA_MA2H (22) VMA_MA12 (22) VMA_RAS# (22) VMA_MA11 (22) VMA_MA10 (22) VMA_BA1 (22) VMA_MA8 (22) VMA_MA9 (22) VMA_MA6 (22) VMA_MA5 (22) VMA_MA7 (22) VMA_MA4 (22) VMA_CAS#
(22) VMA_BA2
Si-II Add

VMA_DM0 VMA_DM1 VMA_DM2 VMA_DM3 VMA_DM4 VMA_DM5 VMA_DM6 VMA_DM7

VMA_WDQS0 VMA_WDQS1 VMA_WDQS2 VMA_WDQS3 VMA_WDQS4 VMA_WDQS5 VMA_WDQS6 VMA_WDQS7

VMA_RDQS0 VMA_RDQS1 VMA_RDQS2 VMA_RDQS3 VMA_RDQS4 VMA_RDQS5 VMA_RDQS6 VMA_RDQS7

+1.8V

(19,22,34) +1.8V
(17,19,35) +VGA1.1V

(22) VMA_DQ[63..0]
(22) VMA_DM[7..0]
(22) VMA_WDQS[7..0]
(22) VMA_RDQS[7..0]

R502 EV@10K/F_4 VMA_ODT
R498 EV@10K/F_4 VMA_CKE

for DDR2 need use CMD11(CKE) and CMD12(ODT)

T32 VMA_CLK0 — VMA_CLK0 (22)
T31 VMA_CLK0# — VMA_CLK0# (22)
AC31 VMA_CLK1 — VMA_CLK1 (22)
AC30 VMA_CLK1# — VMA_CLK1# (22)

FB_VREF J27 +FB_VREF1
15mils width
C93 EV@.1U/10V_4
R78 *1K/F_4
R75 *1K/F_4
use internal Vref, ext divider no stuff

For Debug only
FBA_DEBUG T30 FBA_DEBUG *60.4/F_4 R100 +1.8V

FB_DLLAVDD0 AG27 +FB_PLLAVDD
FB_PLLAVDD0 AF27
15mils width
L11 EV@BKP1608HS181T_6_1.5A +VGA1.1V
C94 EV@.1U/10V_4
C90 EV@.1U/10V_4
C214 EV@1U/6.3V_4
C235 EV@4.7U/6.3V_6

For Nvidia request

C157 EV@4.7U/6.3V_6 C74 EV@.47U/6.3V_4 C110 EV@.47U/6.3V_4 C129 EV@.1U/10V_4 C77 EV@4.7U/6.3V_6 C172 EV@.47U/6.3V_4 C108 EV@.47U/6.3V_4 C103 EV@.1U/10V_4 C193 EV@.1U/10V_4 C133 EV@.1U/10V_4 C179 EV@.1U/10V_4 C102 EV@.1U/10V_4 C638 EV@.1U/10V_4 C112 EV@.1U/10V_4

C97 EV@4.7U/6.3V_6 C109 EV@.47U/6.3V_4 C98 EV@.47U/6.3V_4 C91 EV@.1U/10V_4 C89 EV@4.7U/6.3V_6 C120 EV@.47U/6.3V_4 C96 EV@.47U/6.3V_4 C92 EV@.1U/10V_4 C111 EV@.1U/10V_4 C134 EV@.1U/10V_4 C85 EV@.1U/10V_4 C201 EV@.1U/10V_4 C155 EV@.1U/10V_4 C95 EV@.1U/10V_4

U23C
EV@N10M-GE1-B-U2/H

MEMORY I/F B

FBC_CMD0 FBC_CMD1 FBC_CMD2 FBC_CMD3 FBC_CMD4 FBC_CMD5 FBC_CMD6 FBC_CMD7 FBC_CMD8 FBC_CMD9 FBC_CMD10 FBC_CMD11 FBC_CMD12 FBC_CMD13 FBC_CMD14 FBC_CMD15 FBC_CMD16 FBC_CMD17 FBC_CMD18 FBC_CMD19 FBC_CMD20 FBC_CMD21 FBC_CMD22 FBC_CMD23 FBC_CMD24 FBC_CMD25 FBC_CMD26 FBC_CMD27 FBC_CMD28 FBC_CMD29 FBC_CMD30

FBC_DQM0 FBC_DQM1 FBC_DQM2 FBC_DQM3 FBC_DQM4 FBC_DQM5 FBC_DQM6 FBC_DQM7

FBC_DQS_WP0 FBC_DQS_WP1 FBC_DQS_WP2 FBC_DQS_WP3 FBC_DQS_WP4 FBC_DQS_WP5 FBC_DQS_WP6 FBC_DQS_WP7

FBC_DQS_RN0 FBC_DQS_RN1 FBC_DQS_RN2 FBC_DQS_RN3 FBC_DQS_RN4 FBC_DQS_RN5 FBC_DQS_RN6 FBC_DQS_RN7

FBC_WDS0 FBC_WDS0* FBC_WDS1 FBC_WDS1* FBC_WDS2 FBC_WDS2* FBC_WDS3 FBC_WDS3*

FBC_CLK0 FBC_CLK0* FBC_CLK1 FBC_CLK1*

+1.8V
FBVDDQ_28 FBVDDQ_29 FBVDDQ_30 FBVDDQ_31 FBVDDQ_32 FBVDDQ_33 FBVDDQ_34 FBVDDQ_35 FBVDDQ_36 FBVDDQ_37 FBVDDQ_38

FB_CAL_PD_VDDQ K27 FB_CAL_PD_VDDQ R83 EV@30.1/F_4 +1.8V
FB_CAL_PU_GND L27 FB_CAL_PU_GND R84 EV@30.1/F_4
FB_CAL_TERM_GND M27 FB_CAL_TERM_GND R88 *30.1/F_4
R184 Install for DDR3
FBC_DEBUG G19 FBC_DEBUG R77 *60.4/F_4 +1.8V
R196 no stuff

G96 only
FB_DLLAVDD1 J19 +FB_PLLAVDD
FB_PLLAVDD1 J18
C99 EV@.1U/10V_4
C217 EV@.1U/10V_4

For NB9P-GS only

NB10M_GE1:FB_CAL_PD_VDDQ=30.1ohm;FB_CAL_PU_GND=30.1ohm
NB10M_GS1:FB_CAL_PD_VDDQ=30.1ohm;FB_CAL_PU_GND=36.5ohm

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U23D
EV@N10M-GE1-B-U2/H

IFPAB(LVDS)
IFPCD
IFPC
IFPD
IFPEF
DACA(CRT)
DACC(CRT2)
DACB(TV)
XTAL_PLL

TMDS channel two
Display port output
Modify REV:C
NV: R,G,B +- 250ps length-matched
Close to GPU
PLACE CLOSE TO GPU
STUFF PDs on XTALSSIN and XTALOUTBUFF WHEN EXT_SS IS NOT USED
SI_modified
Nvidia request

SPREAD SPECTRUM

U1 *ICS91730AMLF-T
I2C ADDRESS: 0xD4H

NVidia suggest:
10 k pull-down only if no spread chip used.

05/12 (PV) FOR EMI Solution

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U23E
EV@N10M-GE1-B-U2/H

MIOA
MIOA_VDDQ_1 P9
MIOA_VDDQ_2 R9
MIOA_VDDQ_3 T9
MIOA_VDDQ_4 U9
MIOA_CAL_PD_VDDQ U5
MIOA_CAL_PU_GND T5
MIOA_VREF N5
MIOA_D0 N1
MIOA_D1 P4
MIOA_D2 P1
MIOA_D3 P2
MIOA_D4 P3
MIOA_D5 T3
MIOA_D6 T2
MIOA_D7 T1
MIOA_D8 U4
MIOA_D9 U1
MIOA_D10 U2
MIOA_D11 U3
MIOA_D12 R6
MIOA_D13 T6
MIOA_D14 N6
MIOA_CTL3 P5
MIOA_HSYNC N3
MIOA_VSYNC L3
MIOA_DE N2
MIOA_CLKOUT R4
MIOA_CLKOUT* T4
MIOA_CLKIN N4
MIOA_CLKIN R488 EV@10K/F_4

MIOB
MIOB_VDDQ_1 AA9
MIOB_VDDQ_2 AB9
MIOB_VDDQ_3 W9
MIOB_VDDQ_4 Y9
MIOB_CAL_PD_VDDQ AA7
MIOB_CAL_PU_GND AA6
MIOB_VREF AF1
MIOB_D0 Y1
MIOB_D1 Y2
MIOB_D2 Y3
MIOB_D3 AB3
MIOB_D4 AB2
MIOB_D5 AB1
MIOB_D6 AC4
MIOB_D7 AC1
MIOB_D8 AC2
MIOB_D9 AC3
MIOB_D10 AE3
MIOB_D11 AE2
MIOB_D12 U6
MIOB_D13 W6
MIOB_D14 Y5
MIOB_D15 W5 STRAP0
MIOB_D16 W7 STRAP1
MIOB_D17 V7 STRAP2
MIOB_CTL3 W3
MIOB_HSYNC W1
MIOB_VSYNC W2
MIOB_DE Y5
MIOB_CLKOUT V4
MIOB_CLKOUT* W4
MIOB_CLKIN AE1
MIOB_CLKIN R497 EV@10K/F_4

MISC1 (GPIOS,JTAG,THERM,I2C)
THERMDN T72 GFX_THMD-
THERMDP T71 GFX_THMD+
JTAG_TCK AP14
JTAG_TMS AR14
JTAG_TDI AN14
JTAG_TDO AN16
JTAG_TRST# AP16
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_TRST*
T83
MXMCLK E2
MXMDATA E1
I2CS_SCL E3
I2CS_SDA F4
I2CC_SCL
I2CC_SDA
I2CD_SCL G5
I2CD_SDA D5
I2CE_SCL E5
I2CE_SDA
(19,23) EV_LVDS_DDCCLK R66 EV@33_4 I2CC_SCL_G
(19,23) EV_LVDS_DDCDAT R65 EV@33_4 I2CC_SDA_G
(23) HDMI_DDCCLK
(23) HDMI_DDCDATA
I2CE_SCL_G
I2CE_SDA_G
GPIO0 K1 T6
GPIO1 K2
GPIO2 K3 EV_LVDS_BL_BRGHT HDMI_HP_EV (23)
GPIO3 H3 EV_LVDS_BL_BRGHT (23)
GPIO4 H2 EV_LVDS_VDDEN (23)
GPIO5 H1 EV_LVDS_BLON (23)
GPIO6 H4 GPU_VID0 (35)
GPIO7 H5 T5 VGA_THERM# GPU_VID1 (35)
GPIO8 ALERT# VGA_THERM# (29)
GPIO9 J7
GPIO10 K4 T7
GPIO11 K5 T75
GPIO12 H7 MXM_ACIN
GPIO13 J4
GPIO14 J6
GPIO15 L1
GPIO16 L2
GPIO17 L4
GPIO18 M4
GPIO19 L7
GPIO20 L5
GPIO21 K6
GPIO22 L6
GPIO23 M6

HD Audio Level :3V
MISC2(ROM)
BBIASN_NC J26
BBIASP_NC J25
(12) MXM_BIT_CLK_HDMI MXM_BIT_CLK_HDMI D7
(12) MXM_RST#_HDMI MXM_RST#_HDMI D6
(12) MXM_SDIN_HDMI R55 EV@10_4 MXM_SDIN_HDMI_G C7
(12) MXM_SDOUT_HDMI MXM_SDOUT_HDMI B7
(12) MXM_SYNC_HDMI MXM_SYNC_HDMI A7
HDA_BCLK
HDA_RST*
HDA_SDI
HDA_SDO
HDA_SYNC
R89 EV@40.2K/F_4 STRAP_REF_3V3 N9
R87 EV@40.2K/F_4 STRAP_REF_MIOB M9
STRAP_REF_3V3
STRAP_REF_MIOB
ROM_CS* C3
ROM_SI D3 ROM_SI
ROM_SO C4 ROM_SO
ROM_SCLK D4 ROM_SCLK
I2CH_SCL F6 HDCP_SCL
I2CH_SDA G6 HDCP_SDA
SPDIF A5 SPDIF_VGA
BUFRST* A4
PGOOD_OUT* C5
RFU AK14
RFU_GND K9
R470 *EV@24.3K/F_4
C585 *EV@0.01u/16V_4
MXM_SPDIF_OUT (26)
R467 EV@35.7K/F_4

Nvidia suggest:
Removed T14, T18, T19, T20, T29, T30, T32, T33 that reduce via counts

(2,3,6,7,10,12,13,14,15,16,17,19,23,24,25,26,27,29,31,33,35,36) +3V

R473 STUFF
20K ohm For Samsung , 64M*16
4.99K ohm For Hynix , 64M*16

NB9P-GS (G96) Straps
NB9M-GE (G98) Straps
GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	PRIMARY DVI HOTPLUG
1	IN	N/A	SECONDARY DVI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	FBVDD VID0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	AC DETECT
13	OUT	LOW	PS CONTROL OR HDMI_CEC
14	OUT	HIGH	PS CONTROL

PCI_DEVID[4]/SUBVENDOR
R471 *4.99K/F_4
R58 EV@45.3K/F_4
R56 *4.99K/F_4
ROM_SI
ROM_SO
ROM_SCLK
R473 EV@4.99K/F_4
R59 *4.99K/F_4
R57 EV@15K/F_4

SEE Datasheet for details on G9x Straps!
R494 EV@45.3K/F_4
R491 *4.99K/F_4
R489 EV@24.9K/F_4
STRAP0
STRAP1
STRAP2
R493 *4.99K/F_4
R492 EV@10K/F_4
R490 *15K/F_4

09/09 (UT7G DB)
Change for N10P.

JTAG_TMS R522 EV@10K/F_4
JTAG_TDI R523 EV@10K/F_4
VGA_THERM# R76 EV@10K/F_4
ALERT# R85 EV@10K/F_4
I2CE_SCL_G R54 EV@2.2K_4
I2CE_SDA_G R53 EV@2.2K_4
JTAG_TCK R521 EV@10K/F_4
JTAG_TRST# R520 EV@10K/F_4
EV_LVDS_BL_BRGHT R487 EV@10K/F_4
MXM_RST#_HDMI R88 EV@10K/F_4
MXM_ACIN R80 EV@10K/F_4
NVidia suggest:
Pull low 10KR for R95, R7 & R525

Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
40K	1111	0111

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	XCLK_277	TVMODE2]	TVMODE[1]	TVMODE[0]	1111
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM100	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	XXXX
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0001
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

Delete VGA thermal circuit

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor		N10M (500MHz)	QCI P/N
0111	DDR2 32Mx16x8, 128bit, 512MB	Hynix			
0110	DDR2 32Mx16x8, 128bit, 512MB	Qimonda			
0101	DDR2 32Mx16x8, 128bit, 512MB	Samsung			
0100	DDR2 32Mx16x8, 128bit, 512MB	Nanya/Elpida			
0000	DDR2 64Mx16x8, 128bit, 1GB	Hynix		H5PS1G63EFR-20L	AKD5LG-TW02
0001	DDR2 64Mx16x8, 128bit, 1GB	Samsung		K4N1G164QE-HC20	AKD5LG-T510
0010	DDR2 64Mx16x8, 128bit, 1GB	Qimonda			

PCI_DEVID: STRAP2 R489

NB9M-GE	0x06E	8	1000
NB9M-GS	0x06E	9	1001
NB9P-GE2	0x064	8	1000
NB9P-GS	0x064	9	1001
N10P-GE1	0x065	2	0010
N10M-GE1	0x06E	C	1100 default

CS33572FB13 RES CHIP 35.7K 1/16W +-1%(0402)

HDCP ROM

DHCP ROM	
HDCP_SCL	Low: Crypto ROM Hi: I2C ROM

Change P/N
U2
A0 A1 A2 GND VCC WP SCL SDA
HDCP_SCL HDCP_SDA
EV@AT24C16B
C71 EV@.1U/10V_4
Waiting Confirm from Nvidia
R52 EV@2.2K_4
R45 EV@2.2K_4
R44 *2.2K_4
SI modified
Nvidia suggest:

R49 4.7K_4
R50 4.7K_4
(29) MXM_SMCLK
(29) MXM_SMDATA
Q2 2N7002E
Q3 2N7002E
MXMCLK
MXMDATA
MXMCLK (24)
MXMDATA (24)

RB1 *10K_4
MXM_ACIN
Q6 *EV@DTA114YUA
R74 *EV@10K_4
Q5 *EV@2N7002E
ACIN (29,30)
R82 *0_4

Quanta Computer Inc.
PROJECT : Z06
Size | Document Number: N10P (GPIO & STRAPS) 4/5 | Rev 1A
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NVVDD Decoupling

(35,36) +VGACORE

+VGACORE

+VGACORE

U23F

EV@N10M-GE1-B-U2/H

NVVDD

AB11	VDD_001	VDD_057	P21
AB13	VDD_002	VDD_058	P23
AB15	VDD_003	VDD_059	P25
AB17	VDD_004	VDD_060	R11
AB19	VDD_005	VDD_061	R12
AB21	VDD_006	VDD_062	R13
AB23	VDD_007	VDD_063	R14
AB25	VDD_008	VDD_064	R15
AC11	VDD_009	VDD_065	R16
AC12	VDD_010	VDD_066	R17
AC13	VDD_011	VDD_067	R18
AC14	VDD_012	VDD_068	R19
AC15	VDD_013	VDD_069	R20
AC16	VDD_014	VDD_070	R21
AC17	VDD_015	VDD_071	R22
AC18	VDD_016	VDD_072	R23
AC19	VDD_017	VDD_073	R24
AC20	VDD_018	VDD_074	R25
AC21	VDD_019	VDD_075	T12
AC22	VDD_020	VDD_076	T14
AC23	VDD_021	VDD_077	T16
AC24	VDD_022	VDD_078	T18
AC25	VDD_023	VDD_079	T20
AD12	VDD_024	VDD_080	T22
AD14	VDD_025	VDD_081	T24
AD16	VDD_026	VDD_082	V11
AD18	VDD_027	VDD_083	V13
AD22	VDD_028	VDD_084	V15
AD24	VDD_029	VDD_085	V17
L11	VDD_030	VDD_086	V19
L12	VDD_031	VDD_087	V21
L13	VDD_032	VDD_088	V23
L14	VDD_033	VDD_089	V25
L15	VDD_034	VDD_090	W11
L16	VDD_035	VDD_091	W12
L17	VDD_036	VDD_092	W13
L18	VDD_037	VDD_093	W14
L19	VDD_038	VDD_094	W15
L20	VDD_039	VDD_095	W16
L21	VDD_040	VDD_096	W17
L22	VDD_041	VDD_097	W18
L23	VDD_042	VDD_098	W19
L24	VDD_043	VDD_099	W20
L25	VDD_044	VDD_100	W21
M12	VDD_045	VDD_101	W22
M14	VDD_046	VDD_102	W23
M16	VDD_047	VDD_103	W24
M18	VDD_048	VDD_104	W25
M20	VDD_049	VDD_105	Y12
M22	VDD_050	VDD_106	Y14
M24	VDD_051	VDD_107	Y16
P11	VDD_052	VDD_108	Y18
P13	VDD_053	VDD_109	Y20
P15	VDD_054	VDD_110	Y22
P17	VDD_055	VDD_111	Y24
P19	VDD_056		

PLACE NEAR BALLS

NEAR BGA

+VGACORE

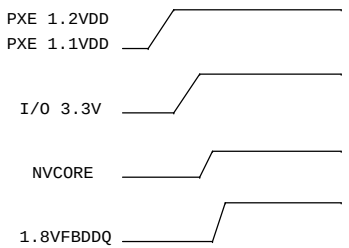
C123 EV@.022u/16V_4	C124 EV@.022u/16V_4	C114 EV@.022u/16V_4	C116 EV@.022u/16V_4	C148 EV@.022u/16V_4	C183 EV@4.7U/6.3V_6	C144 EV@330u/2V_7343
C165 EV@.022u/16V_4	C138 EV@.022u/16V_4	C166 EV@.022u/16V_4	C122 EV@.022u/16V_4	C125 EV@.022u/16V_4	C185 EV@4.7U/6.3V_6	
C136 EV@.1U/10V_4	C147 EV@.1U/10V_4	C117 EV@.1U/10V_4	C167 EV@.1U/10V_4	C139 EV@.1U/10V_4	C184 EV@4.7U/6.3V_6	
C168 EV@.1U/10V_4	C150 EV@.1U/10V_4	C115 EV@.1U/10V_4	C149 EV@.1U/10V_4	C137 EV@.1U/10V_4		

SI modified

Follow Design Guide DG-04131-001 4.7uFx3 and 0.022x10 uF and 0.1uF x10

NB9M: VGACORE +0.90V (Normal) , +1.09V

power up sequence



U23G

EV@N10M-GE1-B-U2/H

GROUND

AA11	GND_1	GND_096	E15
AA12	GND_2	GND_097	E18
AA13	GND_3	GND_098	E24
AA14	GND_4	GND_099	E27
AA15	GND_5	GND_100	E30
AA16	GND_6	GND_101	E6
AA17	GND_7	GND_102	E9
AA18	GND_8	GND_103	F2
AA19	GND_9	GND_104	F31
AA2	GND_10	GND_105	F34
AA20	GND_11	GND_106	F5
AA21	GND_12	GND_107	J2
AA22	GND_13	GND_108	J31
AA23	GND_14	GND_109	J34
AA24	GND_15	GND_110	J5
AA25	GND_16	GND_111	L9
AA34	GND_17	GND_112	M11
AA5	GND_18	GND_113	M13
AB12	GND_19	GND_114	M15
AB14	GND_20	GND_115	M17
AB16	GND_21	GND_116	M19
AB18	GND_22	GND_117	M2
AB20	GND_23	GND_118	M21
AB22	GND_24	GND_119	M23
AB24	GND_25	GND_120	M25
AC9	GND_26	GND_121	M31
AD11	GND_27	GND_122	M34
AD13	GND_28	GND_123	M5
AD15	GND_29	GND_124	N11
AD17	GND_30	GND_125	N12
AD2	GND_31	GND_126	N13
AD21	GND_32	GND_127	N14
AD23	GND_33	GND_128	N15
AD25	GND_34	GND_129	N16
AD31	GND_35	GND_130	N17
AD34	GND_36	GND_131	N18
AD5	GND_37	GND_132	N19
AE11	GND_38	GND_133	N20
AE12	GND_39	GND_134	N21
AE13	GND_40	GND_135	N22
AE14	GND_41	GND_136	N23
AE15	GND_42	GND_137	N24
AE16	GND_43	GND_138	N25
AE17	GND_44	GND_139	P12
AE18	GND_45	GND_140	P14
AE19	GND_46	GND_141	P16
AE20	GND_47	GND_142	P18
AE21	GND_48	GND_143	P20
AE22	GND_49	GND_144	P22
AE23	GND_50	GND_145	P24
AE24	GND_51	GND_146	P2
AE25	GND_52	GND_147	R31
AG2	GND_53	GND_148	R34
AG31	GND_54	GND_149	R5
AG34	GND_55	GND_150	T11
AG5	GND_56	GND_151	T13
AK2	GND_57	GND_152	T15
AK31	GND_58	GND_153	T17
AK34	GND_59	GND_154	T19
AK5	GND_60	GND_155	T21
AL12	GND_61	GND_156	T23
AL15	GND_62	GND_157	T25
AL18	GND_63	GND_158	U11
AL21	GND_64	GND_159	U12
AL24	GND_65	GND_160	U13
AL27	GND_66	GND_161	U14
AL30	GND_67	GND_162	U15
AL6	GND_68	GND_163	U16
AL9	GND_69	GND_164	U17
AN2	GND_70	GND_165	U18
AN34	GND_71	GND_166	U19
AP12	GND_72	GND_167	U20
AP15	GND_73	GND_168	U21
AP18	GND_74	GND_169	U22
AP21	GND_75	GND_170	U23
AP24	GND_76	GND_171	U24
AP27	GND_77	GND_172	U25
AP3	GND_78	GND_173	V12
AP30	GND_79	GND_174	V14
AP33	GND_80	GND_175	V16
AP6	GND_081	GND_176	V18
AP9	GND_082	GND_177	V2
B12	GND_083	GND_178	V20
B15	GND_084	GND_179	V22
B21	GND_085	GND_180	V24
B24	GND_086	GND_181	V31
B27	GND_087	GND_182	V5
B3	GND_088	GND_183	V9
B30	GND_089	GND_184	Y11
B33	GND_090	GND_185	Y13
B6	GND_091	GND_186	Y15
B9	GND_092	GND_187	Y17
C2	GND_093	GND_188	Y19
C34	GND_094	GND_189	Y21
E12	GND_095	GND_190	Y23
		GND_191	Y25

Quanta Computer Inc.

PROJECT : Z06

Size	Document Number	Rev
	N10P (POWER & GND) 5/5	1A

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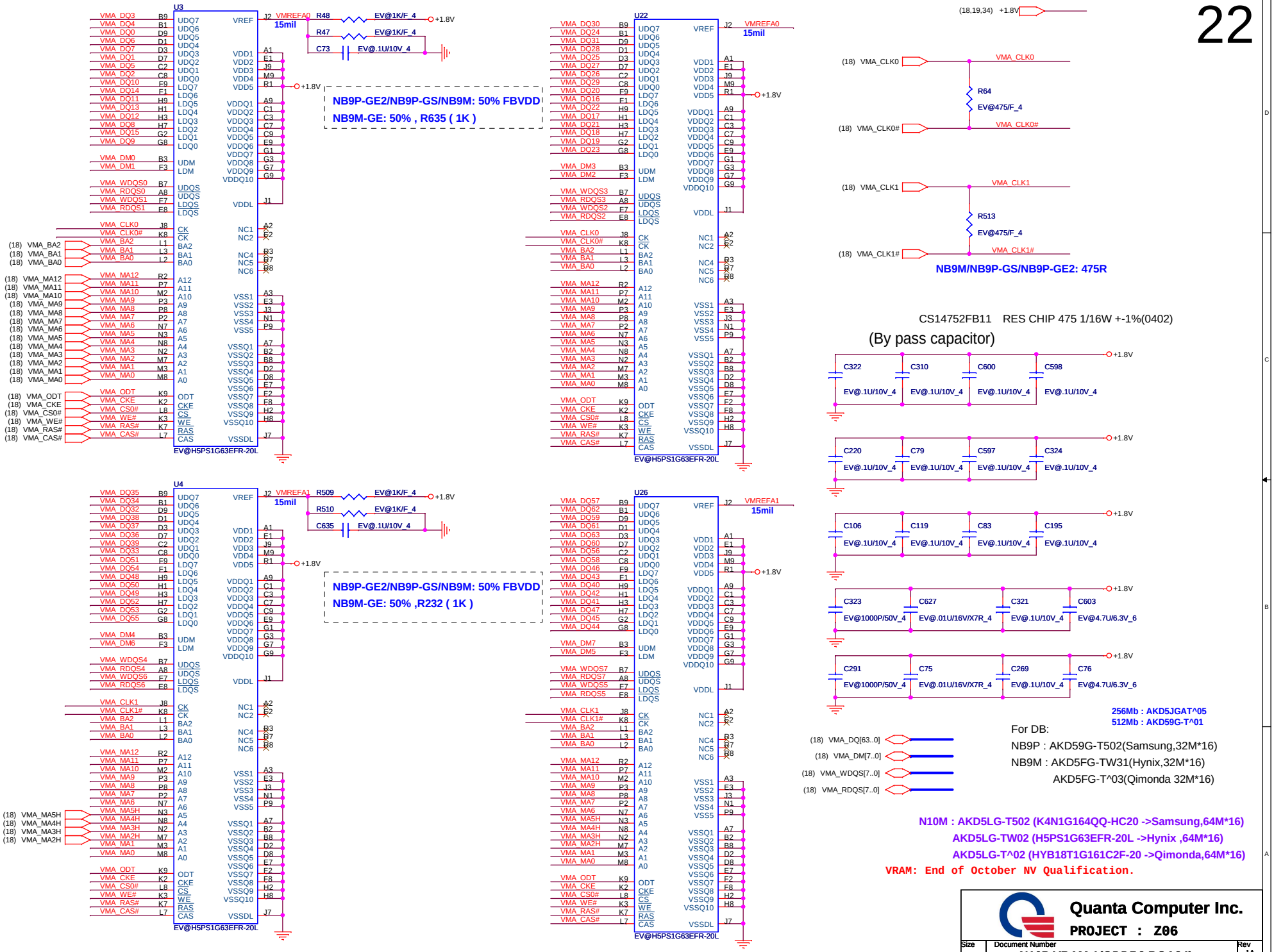
U3
U4
U22
U26
EV@H5PS1G63EFR-20L
NB9P-GE2/NB9P-GS/NB9M: 50% FBVDD
NB9M-GE: 50% , R635 (1K)
NB9P-GE2/NB9P-GS/NB9M: 50% FBVDD
NB9M-GE: 50% ,R232 (1K)
15mil
+1.8V
(18,19,34) +1.8V
(18) VMA_CLK0
VMA_CLK0
R64
EV@475/F_4
(18) VMA_CLK0#
VMA_CLK0#
(18) VMA_CLK1
VMA_CLK1
R513
EV@475/F_4
(18) VMA_CLK1#
VMA_CLK1#
NB9M/NB9P-GS/NB9P-GE2: 475R
CS14752FB11 RES CHIP 475 1/16W +-1%(0402)
(By pass capacitor)
C322 C310 C600 C598
C220 C79 C597 C324
C106 C119 C83 C195
C323 C627 C321 C603
C291 C75 C269 C76
EV@.1U/10V_4
EV@1000P/50V_4
EV@.01U/16V/X7R_4
EV@4.7U/6.3V_6
(18) VMA_DQ[63..0]
(18) VMA_DM[7..0]
(18) VMA_WDQS[7..0]
(18) VMA_RDQS[7..0]
256Mb : AKD5JGAT^05
512Mb : AKD59G-T^01
For DB:
NB9P : AKD59G-T502(Samsung,32M*16)
NB9M : AKD5FG-TW31(Hynix,32M*16)
AKD5FG-T^03(Qimonda 32M*16)
N10M : AKD5LG-T502 (K4N1G164QQ-HC20 ->Samsung,64M*16)
AKD5LG-TW02 (H5PS1G63EFR-20L ->Hynix ,64M*16)
AKD5LG-T^02 (HYB18T1G161C2F-20 ->Qimonda,64M*16)
VRAM: End of October NV Qualification.
Quanta Computer Inc.
PROJECT : Z06
Size
Document Number
N10P VRAM-1(GDDR2 BGA84)
Rev 1A
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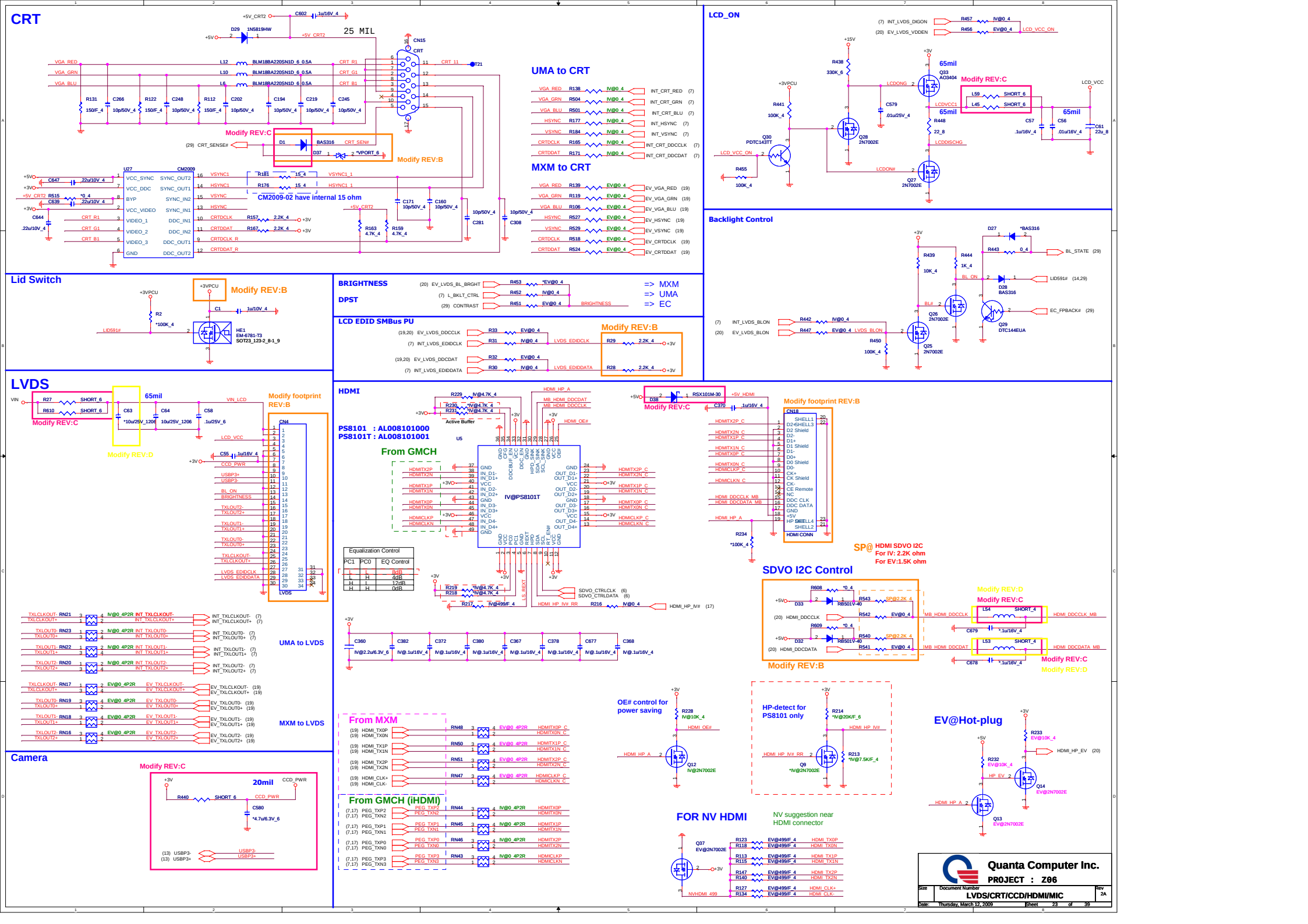
CRT
Modify REV:C
Modify REV:B
CM2009-02 have internal 15 ohm
UMA to CRT
MXM to CRT
LCD_ON
Modify REV:C
65mil
Backlight Control
Lid Switch
Modify REV:B
BRIGHTNESS
DPST
=> MXM
=> UMA
=> EC
LCD EDID SMBus PU
Modify REV:B
LVDS
Modify footprint REV:B
65mil
Modify REV:C
Modify REV:D
HDMI
PS8101 : AL008101000
PS8101T : AL008101001
From GMCH
IV@PS8101T
Equalization Control
SP@ HDMI SDVO I2C
For IV: 2.2K ohm
For EV:1.5K ohm
SDVO I2C Control
Modify REV:B
Modify REV:C
Modify REV:D
UMA to LVDS
MXM to LVDS
OE# control for power saving
HP-detect for PS8101 only
EV@Hot-plug
From MXM
From GMCH (iHDMI)
FOR NV HDMI
NV suggestion near HDMI connector
Camera
Modify REV:C
20mil
Quanta Computer Inc.
PROJECT : Z06
LVDS/CRT/CCD/HDMI/MIC
Rev 2A
Thursday, March 12, 2009
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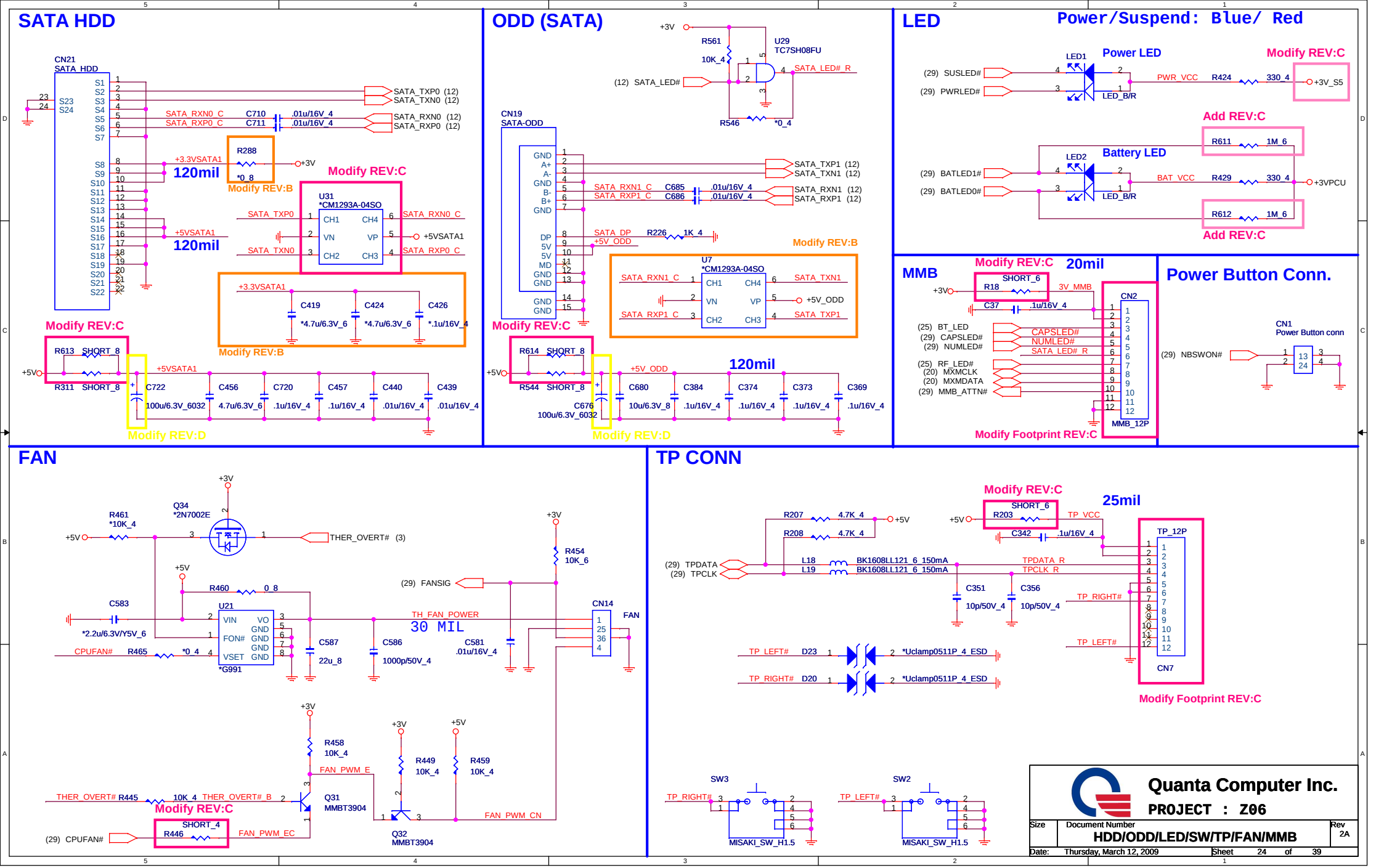
SATA HDD
CN21
SATA_HDD
SATA_TXP0 (12)
SATA_TXN0 (12)
SATA_RXN0 (12)
SATA_RXP0 (12)
SATA_RXN0_C
SATA_RXP0_C
C710
C711
.01u/16V_4
+3.3VSATA1
120mil
R288
*0_8
+3V
Modify REV:C
Modify REV:B
U31
*CM1293A-04SO
SATA_TXP0
SATA_TXN0
SATA_RXN0_C
SATA_RXP0_C
+5VSATA1
+5VSATA1
120mil
C419
C424
C426
*4.7u/6.3V_6
*.1u/16V_4
R613 SHORT_8
R311 SHORT_8
C722
100u/6.3V_6032
C456
4.7u/6.3V_6
C720
C457
C440
C439
.1u/16V_4
.01u/16V_4
Modify REV:D
ODD (SATA)
+3V
R561
10K_4
U29
TC7SH08FU
SATA_LED#
SATA_LED# R
R546
*0_4
CN19
SATA-ODD
SATA_TXP1 (12)
SATA_TXN1 (12)
SATA_RXN1 (12)
SATA_RXP1 (12)
SATA_RXN1_C
SATA_RXP1_C
C685
C686
SATA_DP
+5V_ODD
R226
1K_4
U7
*CM1293A-04SO
SATA_TXN1
SATA_TXP1
+5V_ODD
R614 SHORT_8
R544 SHORT_8
C676
100u/6.3V_6032
C680
10u/6.3V_8
C384
C374
C373
C369
120mil
LED
Power/Suspend: Blue/ Red
LED1
Power LED
(29) SUSLED#
(29) PWRLED#
LED_B/R
PWR_VCC
R424
330_4
+3V_S5
Add REV:C
R611
1M_6
LED2
Battery LED
(29) BATLED1#
(29) BATLED0#
BAT_VCC
R429
330_4
+3VPCU
R612
1M_6
MMB
Modify REV:C
20mil
SHORT_6
R18
3V_MMB
+3V
C37
.1u/16V_4
CN2
(25) BT_LED
(29) CAPSLED#
(29) NUMLED#
CAPSLED#
NUMLED#
SATA_LED# R
(25) RF_LED#
(20) MXMCLK
(20) MXMDATA
(29) MMB_ATTN#
MMB_12P
Modify Footprint REV:C
Power Button Conn.
CN1
Power Button conn
(29) NBSWON#
FAN
Q34
*2N7002E
R461
*10K_4
THER_OVERT# (3)
R454
10K_6
(29) FANSIG
R460
0_8
C583
*2.2u/6.3V/Y5V_6
U21
VIN
VO
FON#
VSET
GND
*G991
CPUFAN#
R465
*0_4
C587
22u_8
C586
1000p/50V_4
C581
.01u/16V_4
TH_FAN_POWER
30 MIL
CN14
FAN
R458
10K_4
FAN_PWM_E
R449
10K_4
R459
10K_4
THER_OVERT#
R445
10K_4
THER_OVERT# B
Q31
MMBT3904
Modify REV:C
SHORT_4
R446
(29) CPUFAN#
FAN_PWM_EC
Q32
MMBT3904
FAN_PWM_CN
TP CONN
Modify REV:C
25mil
R207
4.7K_4
R208
4.7K_4
+5V
SHORT_6
R203
TP_VCC
C342
.1u/16V_4
TP_12P
(29) TPDATA
(29) TPCLK
L18
L19
BK1608LL121_6_150mA
TPDATA_R
TPCLK_R
C351
C356
10p/50V_4
TP_RIGHT#
TP_LEFT#
D23
D20
*Uclamp0511P_4_ESD
CN7
Modify Footprint REV:C
SW3
SW2
MISAKI_SW_H1.5
Quanta Computer Inc.
PROJECT : Z06
Size
Document Number
HDD/ODD/LED/SW/TP/FAN/MMB
Rev
2A
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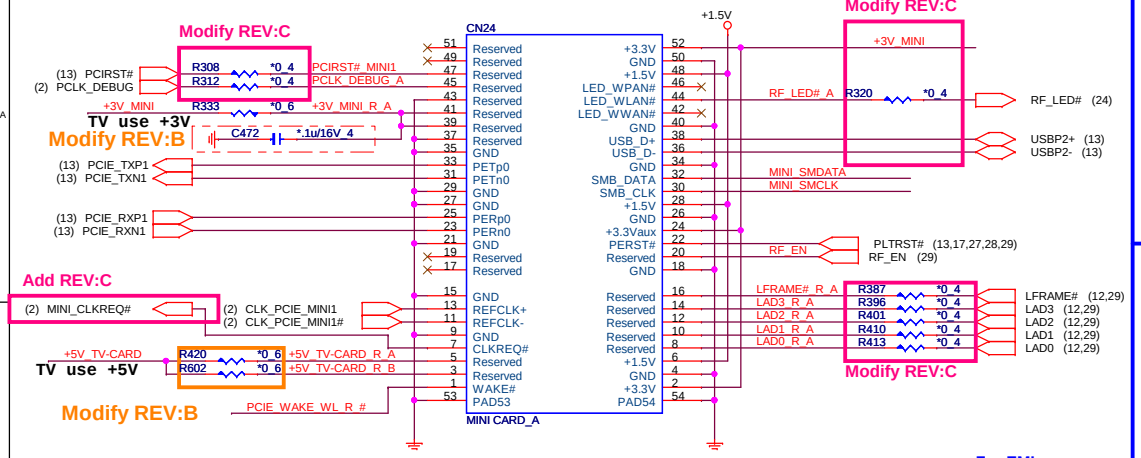
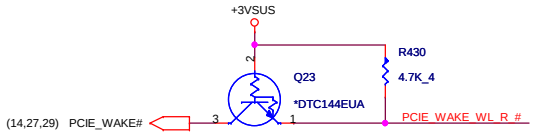
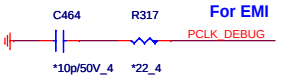
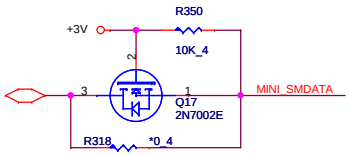
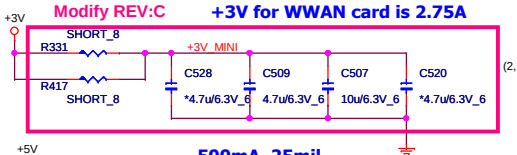
MINI-CARD

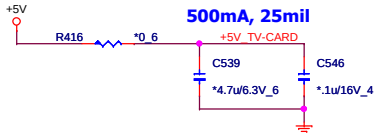


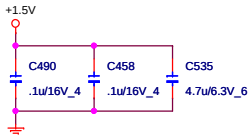


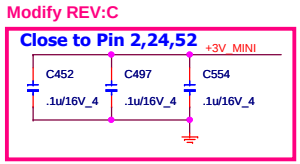




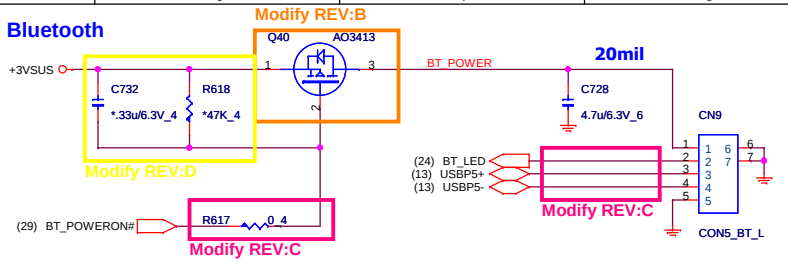






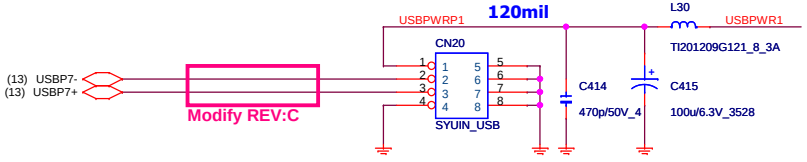


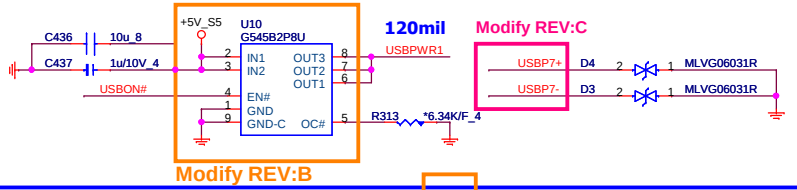
Bluetooth



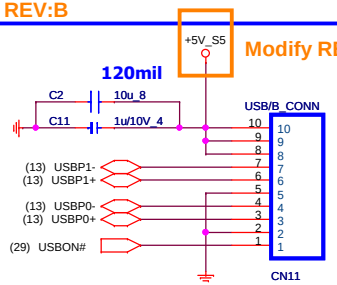
If stuff C732 & R618 , Pls will
R617 change to 4.7K ohm
(P/N : CS24702JB38)

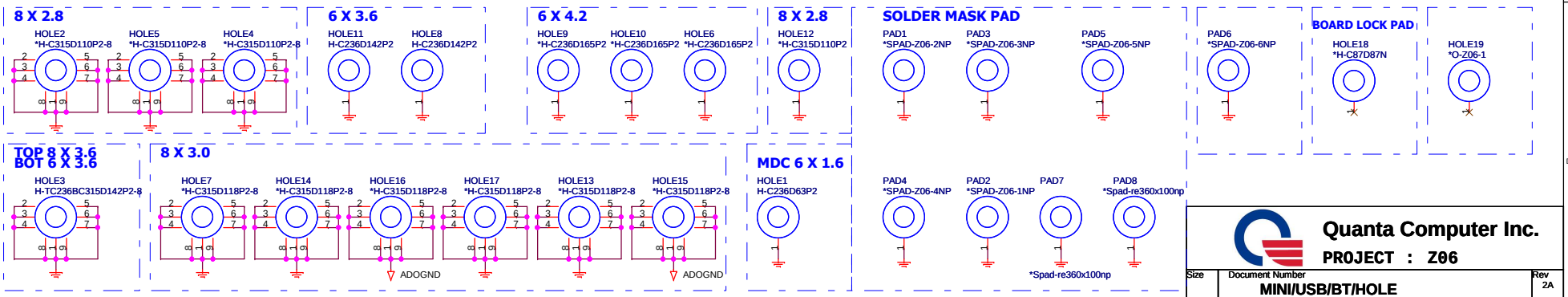
INT. USB





EXT. USB





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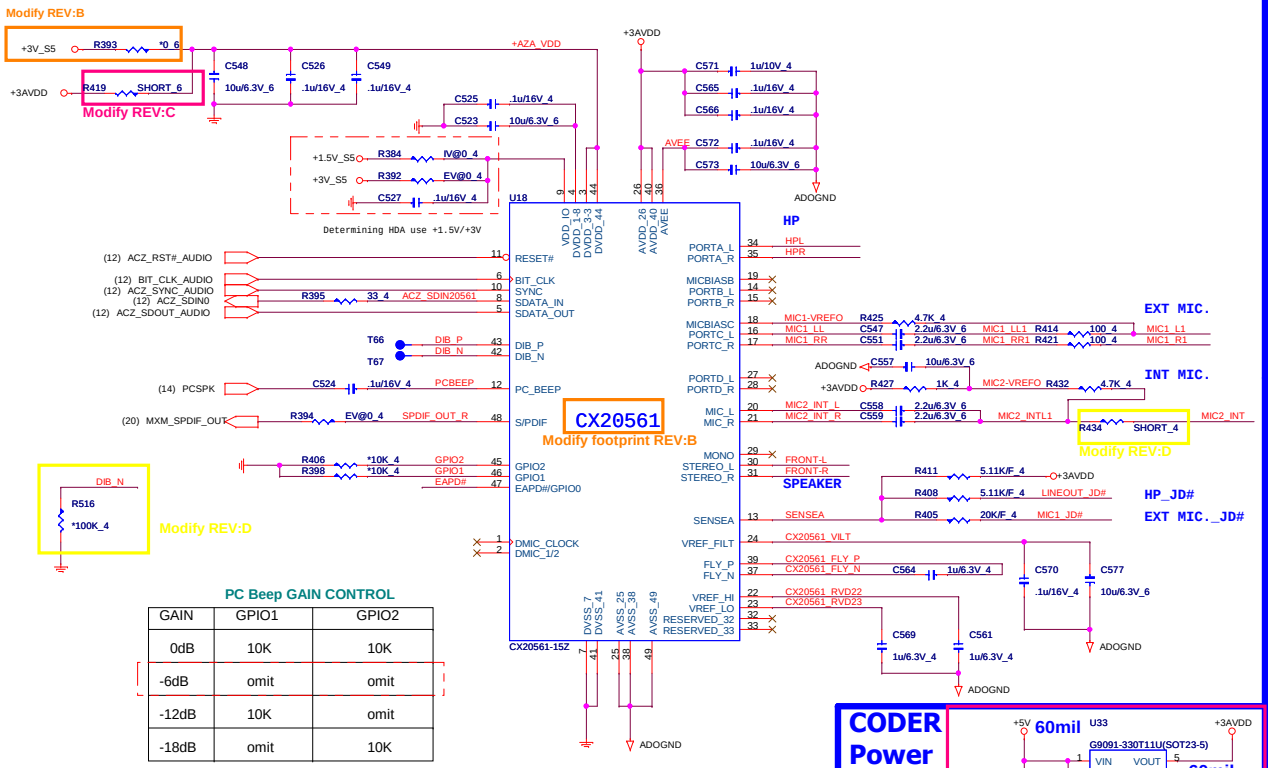
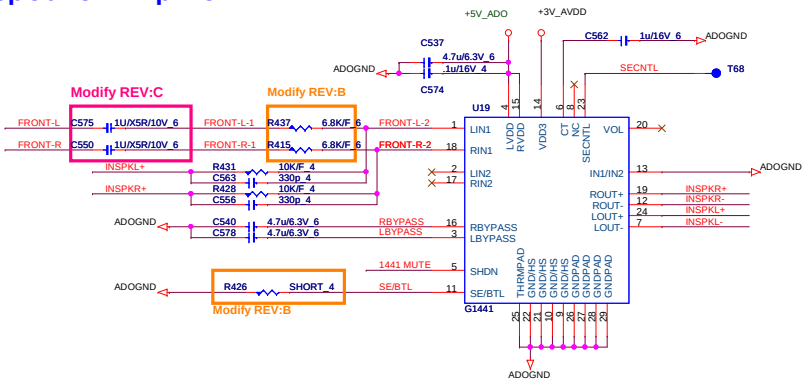
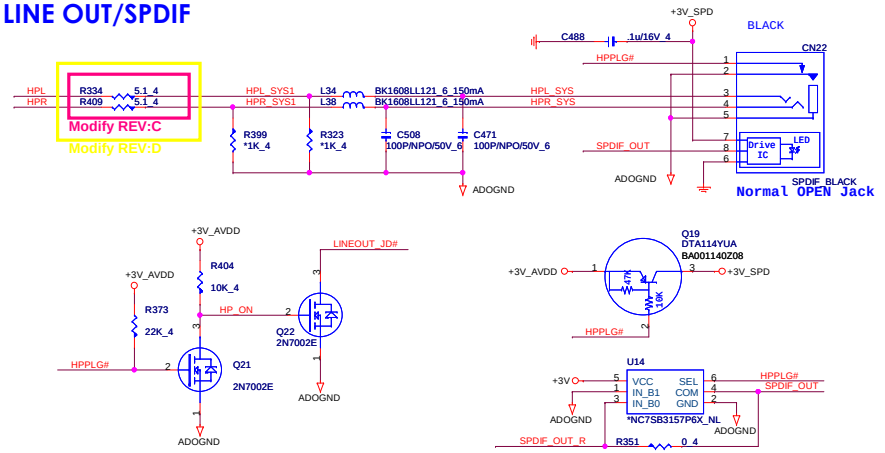
Codec CX20561-15Z (QFN)



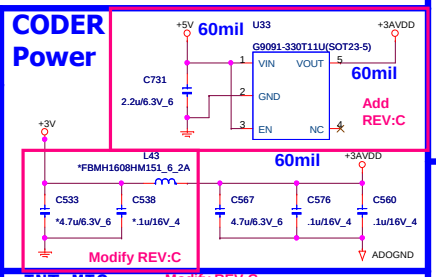
Speaker Amplifier



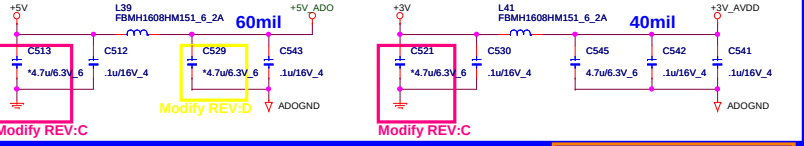
LINE OUT/SPDIF



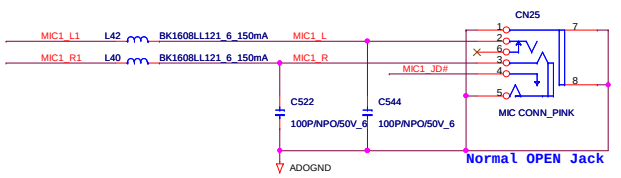
CODER Power



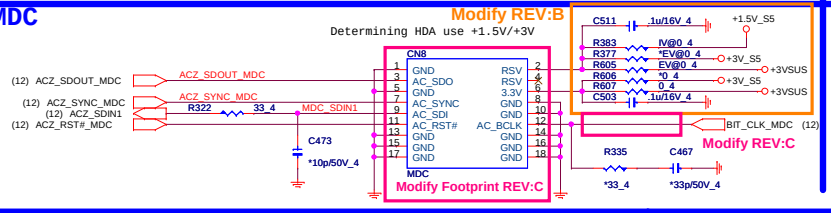
AMP Power



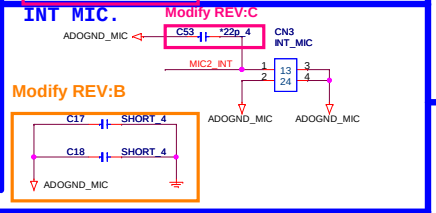
MIC



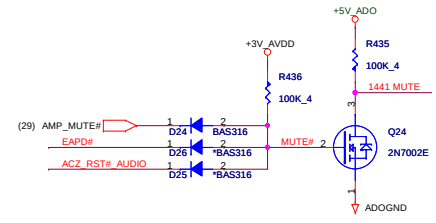
MDC



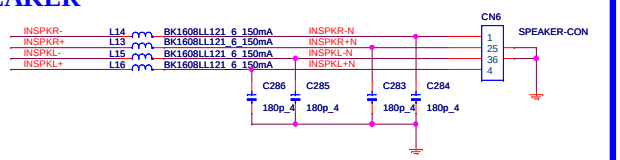
INT MIC.



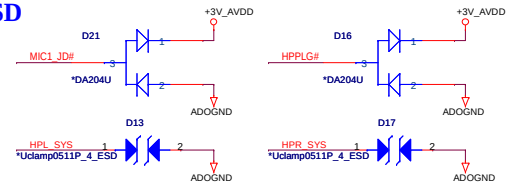
MUTE

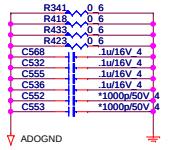


SPEAKER



ESD





Quanta Computer Inc.

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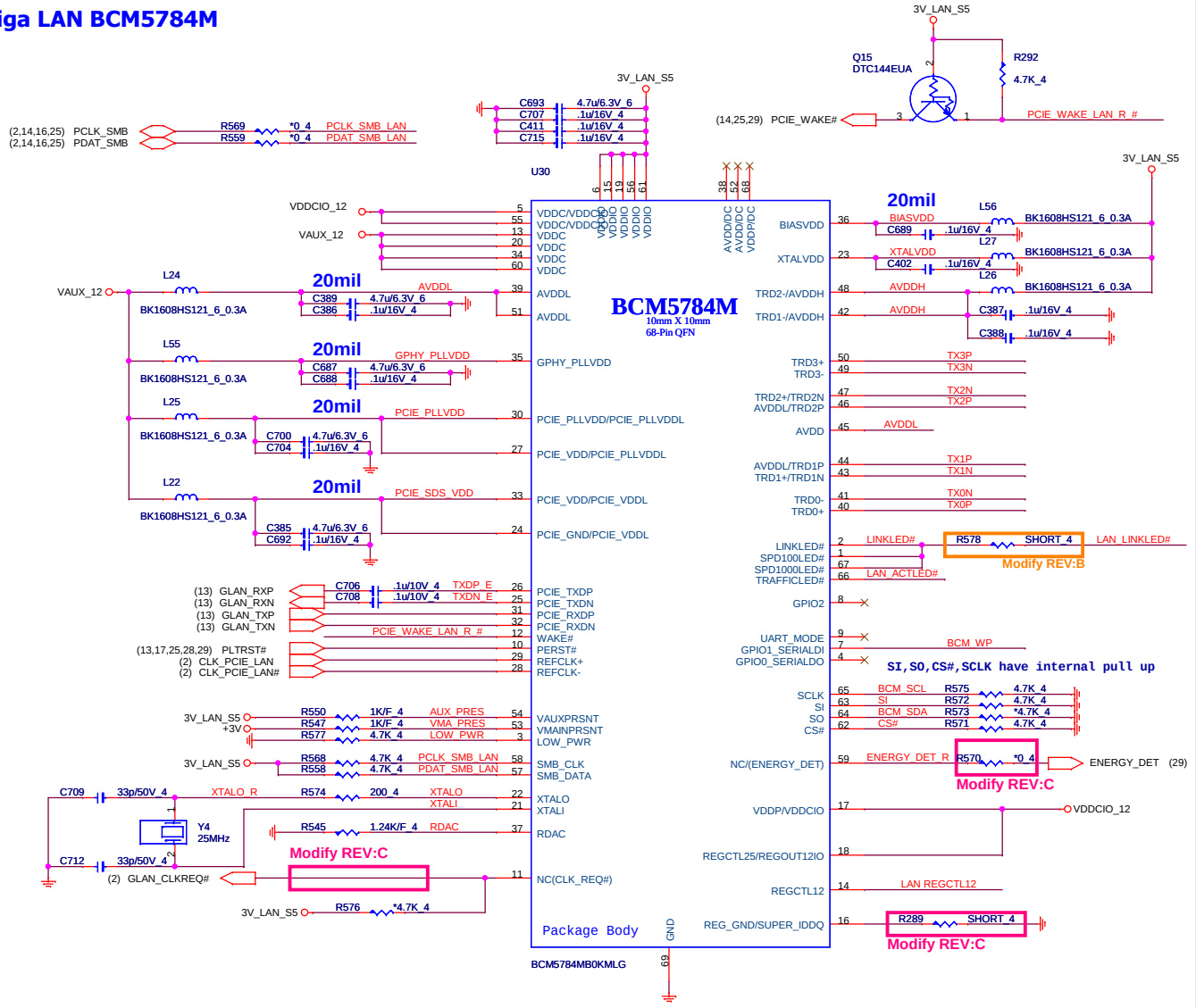
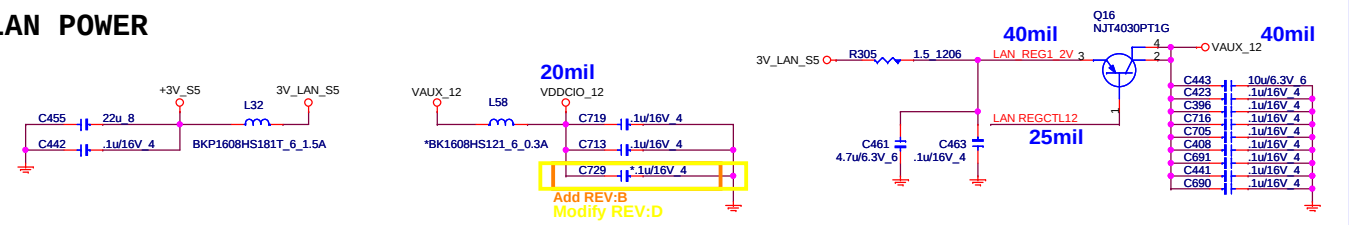
Giga LAN BCM5784M

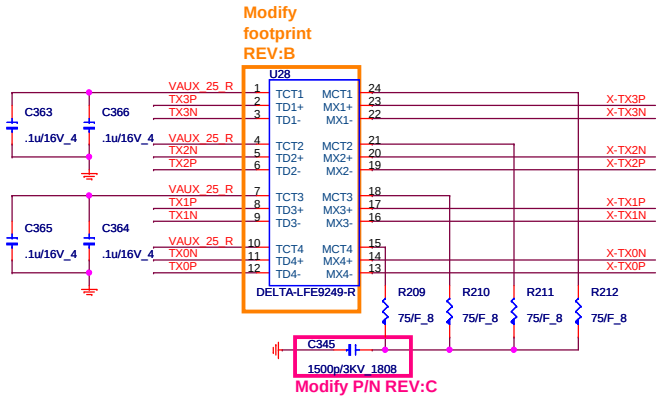


LAN POWER

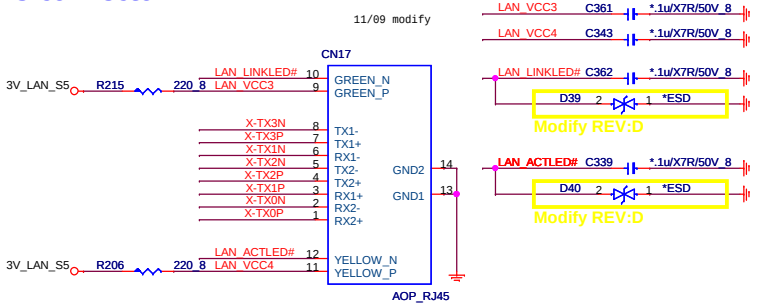


Transfomer

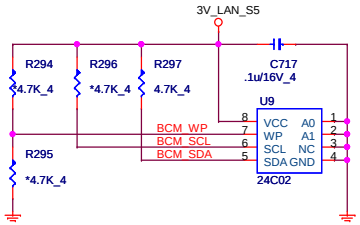
Source 1: DELTA LFE9249-R DB0ZR1LAN11
Source 2: BOT GST5009B DB0Z06LAN00



RJ45 connector



EEPROM



EEPROM Strapping

	SO	SI	CS#	SCLK
24LC02	1	0	0	0

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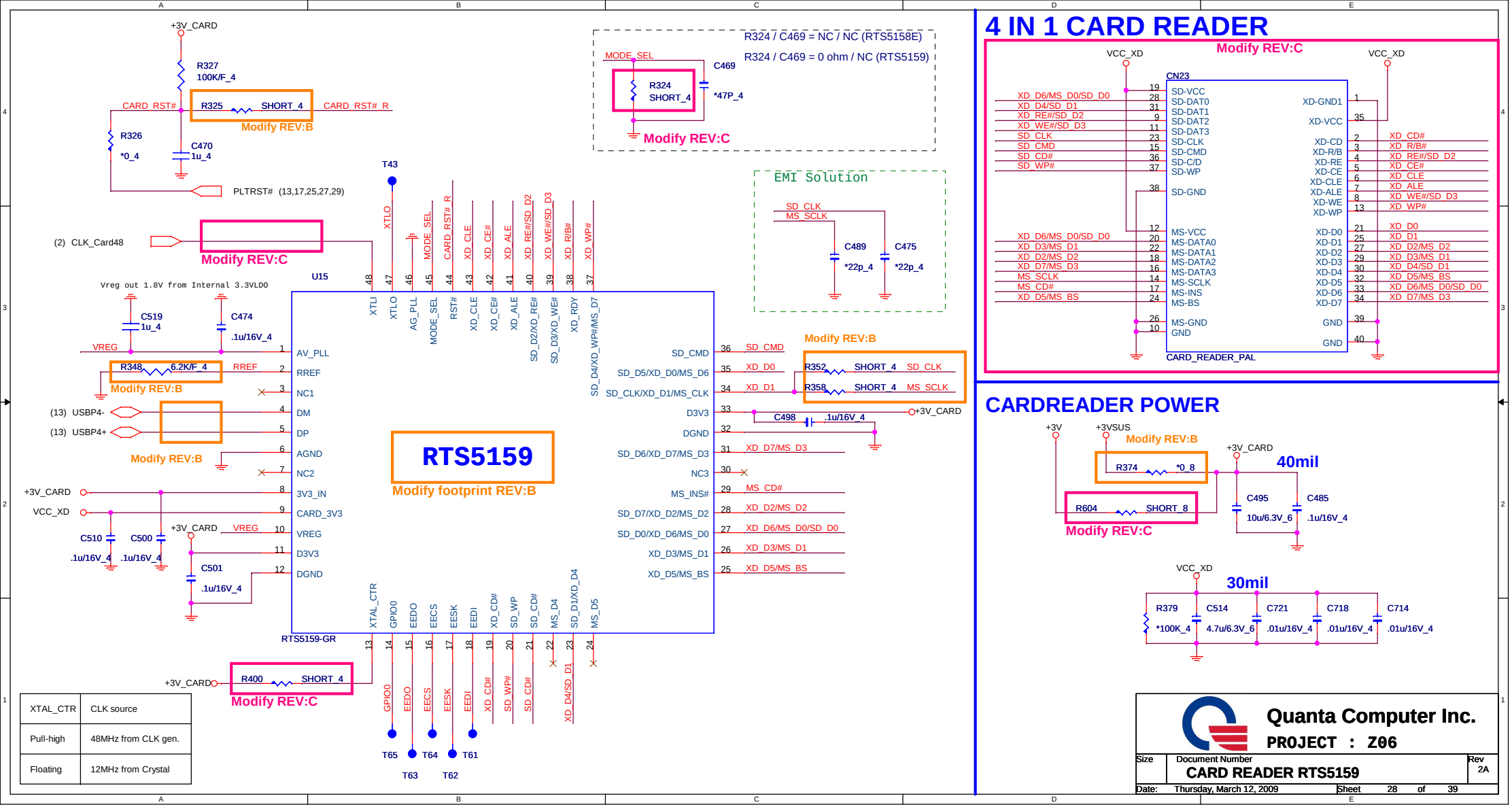
4 IN 1 CARD READER



XTAL_CTR	CLK source
Pull-high	48MHz from CLK gen.
Floating	12MHz from Crystal

CARDREADER POWER

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EC

I/O ADDRESS SETTING

BADDR1-0	I/O Address	
	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

BADDR0 — BADDR0 — R363 10K_4
BADDR1 — uR_SOUT_CR — R362 *10K_4
SHBM — SHBM — R310 10K_4

1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

SM BUS PU

+3VPCU
MBCLK — R300 4.7K_4
MBDATA — R299 4.7K_4
2ND_MBCLK — R291 4.7K_4
2ND_MBDATA — R298 4.7K_4
MXM_SMCLK — R365 4.7K_4
MXM_SMDATA — R366 4.7K_4
+3V
CRT_SENSE# — R309 4.7K_4

ACER ID

MXM_SMCLK
MXM_SMDATA
U8 24C02 (SCL, SDA, A0, A1, A2, WP, VCC, GND)
+3VPCU — R270 *0_4
+3V_S5 — R278 0_4
C409 *.1u/16V_4_X7R

SPI FLASH

SPI_SDI_uR R314 22_4 SPI_SDI_uR_R
SPI_SDO_uR
SPI_SCK_uR
SPI_CS0#_uR
+3VPCU R321 10K_4
U12 W25X16AVSSIG (SO, SI, SCK, CE, VDD, HOLD, WP, VSS)
C448 .1u/16V_4_X7R

1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

HWPG

+3V — R356 10K_4
(34,35) 1V8_ON — D9 EV@BAS316
(36) HWPG_1.5V — D10 BAS316
(32) HWPG_1.05V — D12 BAS316
(34) HWPG_1.8V — D5 BAS316
(31) SYS_HWPG — D8 BAS316
(3,6,14,33) DELAY_VR_PWRGOOD — D11 *BAS316
(35) HWPG_1.1V — D7 EV@BAS316
HWPG — R303 SHORT_4 — Modify REV:B
MPWROK (6,14)

POWER-ON PAD

G1 — NBSWON# — *SHORT_ PAD

Thermal Sensor

+3V — R371 *47K/F_4
R370 *100K/F _4 NTC
TPD_TRIP

INTERNAL KEYBOARD STRIP SET

+3VPCU — MY0 — R579 10K_4

+3VPCU — L35 BK1608HS220_6_1A — 30mil — +A3VPCU
C491 .1u/16V_4_X7R — C496 10u_6 — E775AGND
C492 4.7u/6.3V_6 — C446 .1u/16V_4_X7R — C416 *.1u/16V_4_X7R — C438 .1u/16V_4_X7R — C454 *.1u/16V_4_X7R — C465 .1u/16V_4_X7R

Modify footprint REV:B
D15 RB520S30 — 3V_VDD_EC — +3V — C484 4.7u/6.3V_6 — C478 .1u/16V_4_X7R

U11 WPCE775LA0DG

LPC: LFRAME, LAD0–LAD3, LCLK, GPIO11/CLKRUN, GA20, KBRST, ECSCI/GPIO54, GPIO24/LDRQ, GPIO10/LPCPD, LREST, GPIO67/PWUREQ, SERIRQ, GPIO65/SMI
A/D: GPI90/AD0 TEMP_MBAT (30); GPI91/AD1 TSATN_EC# (6); GPI92/AD2 TPD_TRIP; GPI93/AD3 ICMNT (30); GPIO05/AD4; GPIO04/AD5
D/A: GPI94/DA0 CC-SET (30); GPI95/DA1 ENERGY_DET (27); GPI96/DA2 BL_STATE (23); GPI97/DA3
GPIO: GPIO01/TB2 ACIN (20,30); GPIO03/AD6 NBSWON# (24); GPIO06 LID591# (14,23); GPIO07/AD7 SUSB# (14); GPIO23/SCL3 MXM_SMCLK (20); GPIO30/CIRTX2; GPIO31/SDA3 MXM_SMDATA (20); GPIO32/D_PWM BATLED0# (24); GPIO33/H_PWM BATLED1# (24); GPIO36/TB3 VRON (33); GPIO40/F_PWM; GPIO42/TCK; GPIO43/TMS AMP_MUTE# (26); GPIO44/TDI; GPIO45/E_PWM CPUFAN# (24); GPIO46/CIRRXM/TRST MMB_ATTN# (24); GPO47/SCL4; GPIO50/TDO D/C# (30); GPIO51/TA3 S5_ON (31,36,37); GPIO52/CIRTX2/RDY PCIE_WAKE# (14,25,27); GPIO53/SDA4 HWPG; GPIO81 DNBSWON# uR — D14 BAS316 — DNBSWON# (14); GPO82/TRIS BADDR0; GPO84/BADDR0; GPIO41
KB: KBSIN0–KBSIN7; KBSOUT0/JENK … KBSOUT17; KBSOUT12/GPIO64 … KBSOUT15/GPIO61/XOR_OUT; GPIO60/KBSOUT16
TIMER: GPIO56/TA1 SUSON (34,36); GPIO20/TA2 FANSIG (24); GPIO14/TB1; GPIO15/A_PWM CONTRAST (23); GPIO21/B_PWM NUMLED# (24); GPIO13/C_PWM PWRLED# (24); GPIO66/G_PWM CAPSLED# (24)
SPI: GPIO77/SPI_DI CRT_SENSE# (23); GPO76/SPI_DO/SHBM SHBM; GPIO75/SPI_SCK CELL-SET — T41
SMB: GPIO17/SCL1; GPIO22/SDA1; GPIO73/SCL2; GPIO74/SDA2
IR: GPIO72/IRRX1/SIN2 RSMRST#_uR — R302 SHORT_4 — RSMRST# (14); GPIO70/IRRX2_IRSL0 SUSC# (14) — R301 SHORT_4 — PWROK_EC (14); GPIO71/IRTX/SOUT2 PWROK_EC_uR; GPIO87/CIRRXM/SIN_CR RF_EN; GPIO34/CIRRXL RF_EN (25); GPIO16/CIRTX TP_LED# — T54; GPO83/SOUT_CR/BADDR1 uR_SOUT_CR
PS/2: GPIO37/PSCLK1; GPIO35/PSDAT1; GPIO26/PSCLK2; GPIO27PSDAT2; GPIO25/PSCLK3; GPIO12/PSDAT3
FIU: F_SDI SPI_SDI_uR; F_SDO SPI_SDO_uR_R — R319 22_4 — SPI_SDO_uR; F_CS0 SPI_CS0#_uR; F_SCK SPI_SCK_uR_R — R342 22_4 — SPI_SCK_uR
32KX1/32KCLKIN; GPIO55/CLKOUT ECDB_CLOCK — T37 — Output 25MHz (T37)
VCC_POR VCC_POR# — R315 47K_4 — +3VPCU
VREF VREF_uR — R368 SHORT_4 — +A3VPCU — Modify REV:B
32KX2

Modify REV:B: SUSLED# (24)

For PCICLK: PCLK_591 — R345 *22_4 — C483 *10p/50V_4
PU +3V for SCI: LFRAME#, LAD0–LAD3, PCLK_591, CLKRUN#, GATEA20, RCIN#, EC_SCI# — D6 BAS316 — SCI# uR; EC_FPBACK#
PU +3V for SMI: T51 E_KEY; PLTRST#; USBON#; SERIRQ; KBSMI#

CN5 FFC_26P_KB: MY0–MY17, MX0–MX7

(30) MBCLK, (30) MBDATA, (3) 2ND_MBCLK, (3) 2ND_MBDATA
(24) TPCLK, (24) TPDATA, (30) CHG_EN, (25) BT_POWERON#, (32,34,35,36) MAINON, (20) VGA_THERM#

RP1 10K_10P8R: MX3, MX2, MX4, MX1, MX5, MX0, MX6, MX7

R307 20M_6 — Y2 32.768KHZ/H1.4 — R306 33K/F_4 — C445 6p/50V_4 — C444 6p/50V_4 — E775AGND — Modify REV:B
E775_32KX1, E775_32KX2

C493 .1u/16V_4_X7R — C494 .1u/16V_4_X7R — L36 BK1608HS220_6_1A — E775AGND
AGND, VCORF — VCORF_uR — C417 1u_4

1'st AKE38ZP0N01 : Winbond W25X16AVSSIG
2'nd AKE37FP0Z13 : MXIC MX25L1605AM2C-15G
3'rd AKE38ZA0Q00 : EON EN25F16-100HIP
4'rd AKE38ZN0800 : AMIC A25L016

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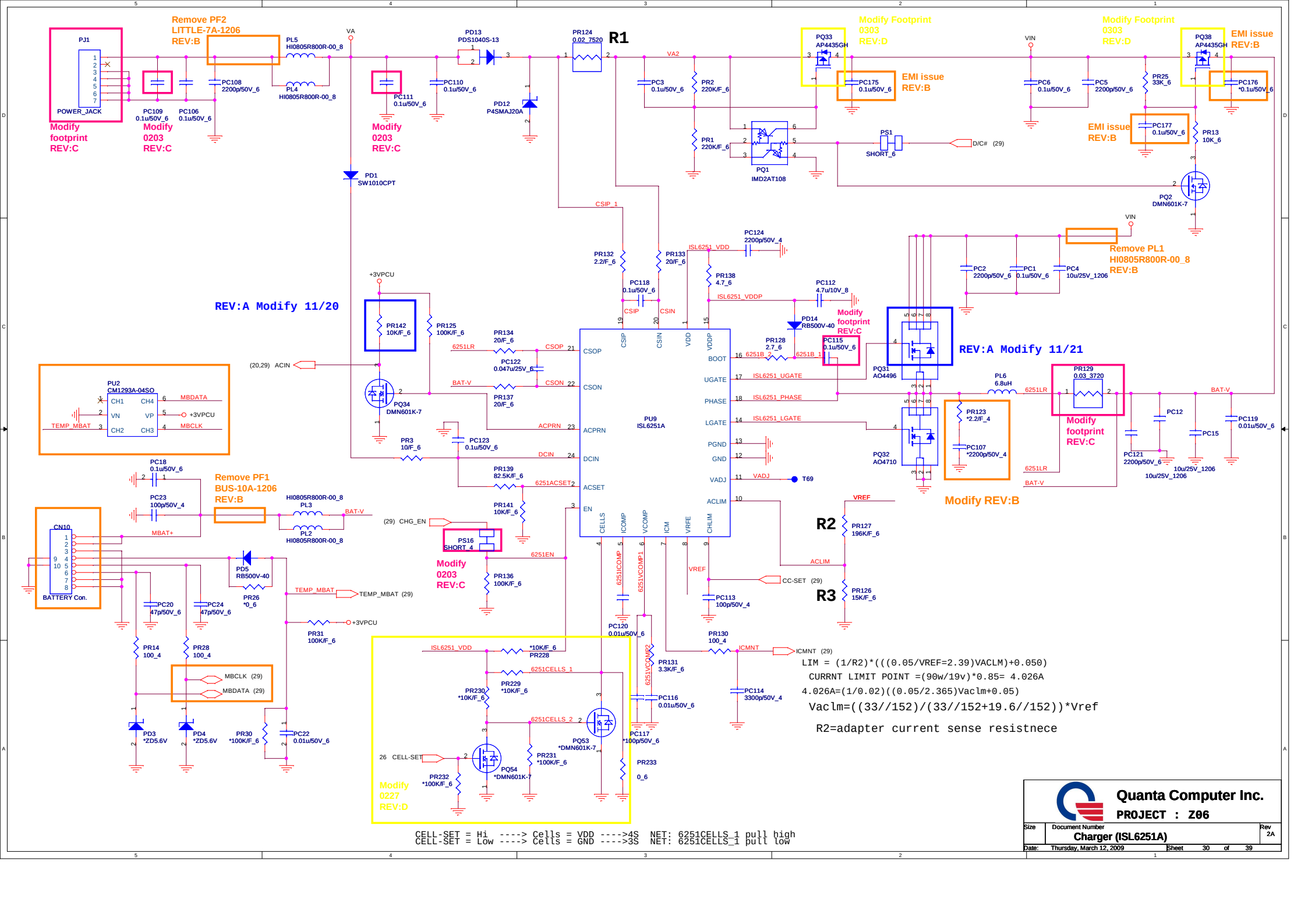
Remove PF2
LITTLE-7A-1206
REV:B
PJ1
POWER_JACK
Modify
footprint
REV:C
PC109
0.1u/50V_6
Modify
0203
REV:C
PC106
0.1u/50V_6
PC108
2200p/50V_6
PL5
HI0805R800R-00_8
PL4
HI0805R800R-00_8
VA
PC111
0.1u/50V_6
Modify
0203
REV:C
PD13
PDS1040S-13
PC110
0.1u/50V_6
PD12
P4SMAJ20A
PD1
SW1010CPT
PR124
0.02_7520
R1
VA2
PC3
0.1u/50V_6
PR2
220K/F_6
PR1
220K/F_6
PQ1
IMD2AT108
PS1
SHORT_6
D/C# (29)
Modify Footprint
0303
REV:D
PQ33
AP4435GH
PC175
0.1u/50V_6
EMI issue
REV:B
VIN
PC6
0.1u/50V_6
PC5
2200p/50V_6
PR25
33K_6
Modify Footprint
0303
REV:D
PQ38
AP4435GH
EMI issue
REV:B
PC176
*0.1u/50V_6
EMI issue
REV:B
PC177
0.1u/50V_6
PR13
10K_6
PQ2
DMN601K-7
CSIP_1
PR132
2.2/F_6
PR133
20/F_6
PC118
0.1u/50V_6
CSIP
CSIN
ISL6251_VDD
PC124
2200p/50V_4
PR138
4.7_6
ISL6251_VDDP
PC112
4.7u/10V_8
PD14
RB500V-40
PC115
0.1u/50V_6
Modify
footprint
REV:C
REV:A Modify 11/20
REV:A Modify 11/21
PQ31
AO4496
PQ32
AO4710
PL6
6.8uH
PR123
*2.2/F_4
PC107
*2200p/50V_4
Modify REV:B
PR129
0.03_3720
Modify
footprint
REV:C
PC12
PC121
2200p/50V_6
PC15
10u/25V_1206
10u/25V_1206
PC119
0.01u/50V_6
BAT-V
6251LR
Remove PL1
HI0805R800R-00_8
REV:B
PC2
2200p/50V_6
PC1
0.1u/50V_6
PC4
10u/25V_1206
+3VPCU
PR142
10K/F_6
PR125
100K/F_6
PR134
20/F_6
6251LR
CSOP
PC122
0.047u/25V_6
BAT-V
CSON
PR137
20/F_6
(20,29) ACIN
PQ34
DMN601K-7
ACPRN
PR3
10/F_6
PC123
0.1u/50V_6
DCIN
PR139
82.5K/F_6
6251ACSET
PR141
10K/F_6
PU9
ISL6251A
CSOP
CSON
ACPRN
DCIN
ACSET
EN
CSIP
CSIN
VDD
VDDP
BOOT
UGATE
PHASE
LGATE
PGND
GND
VADJ
ACLIM
CELLS
ICOMP
VCOMP
ICM
VFRE
CHLIM
ISL6251_UGATE
ISL6251_PHASE
ISL6251_LGATE
VADJ
T69
PU2
CM1293A-04SO
CH1
CH4
MBDATA
VN
VP
+3VPCU
CH2
CH3
MBCLK
TEMP_MBAT
PC18
0.1u/50V_6
PC23
100p/50V_4
Remove PF1
BUS-10A-1206
REV:B
HI0805R800R-00_8
PL3
HI0805R800R-00_8
PL2
BAT-V
MBAT+
CN10
BATTERY Con.
(29) CHG_EN
PS16
SHORT_4
Modify
0203
REV:C
6251EN
PR136
100K/F_6
PD5
RB500V-40
PR26
*0_6
TEMP_MBAT
TEMP_MBAT (29)
+3VPCU
PR31
100K/F_6
PC20
47p/50V_6
PC24
47p/50V_6
PR14
100_4
PR28
100_4
MBCLK (29)
MBDATA (29)
PD3
*ZD5.6V
PD4
*ZD5.6V
PR30
*100K/F_6
PC22
0.01u/50V_6
R2
VREF
PR127
196K/F_6
ACLIM
CC-SET (29)
R3
PR126
15K/F_6
PC113
100p/50V_4
6251ICOMP
6251VCOMP1
6251VCOMP2
PC120
0.01u/50V_6
PR130
100_4
ICMNT
ICMNT (29)
PR131
3.3K/F_6
PC116
0.01u/50V_6
PC114
3300p/50V_4
PC117
*100p/50V_6
PR233
0_6
ISL6251_VDD
*10K/F_6
PR228
6251CELLS_1
PR229
*10K/F_6
PR230
*10K/F_6
6251CELLS_2
PQ53
*DMN601K-7
26 CELL-SET
PR231
*100K/F_6
PQ54
*DMN601K-7
PR232
*100K/F_6
Modify
0227
REV:D
LIM = (1/R2)*(((0.05/VREF=2.39)VACLM)+0.050)
CURRNT LIMIT POINT =(90w/19v)*0.85= 4.026A
4.026A=(1/0.02)((0.05/2.365)Vaclm+0.05)
Vaclm=((33//152)/(33//152+19.6//152))*Vref
R2=adapter current sense resistnece
CELL-SET = Hi ----> Cells = VDD ----->4S NET: 6251CELLS_1 pull high
CELL-SET = Low ----> Cells = GND ----->3S NET: 6251CELLS_1 pull low
Quanta Computer Inc.
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Charger (ISL6251A)
Rev
2A
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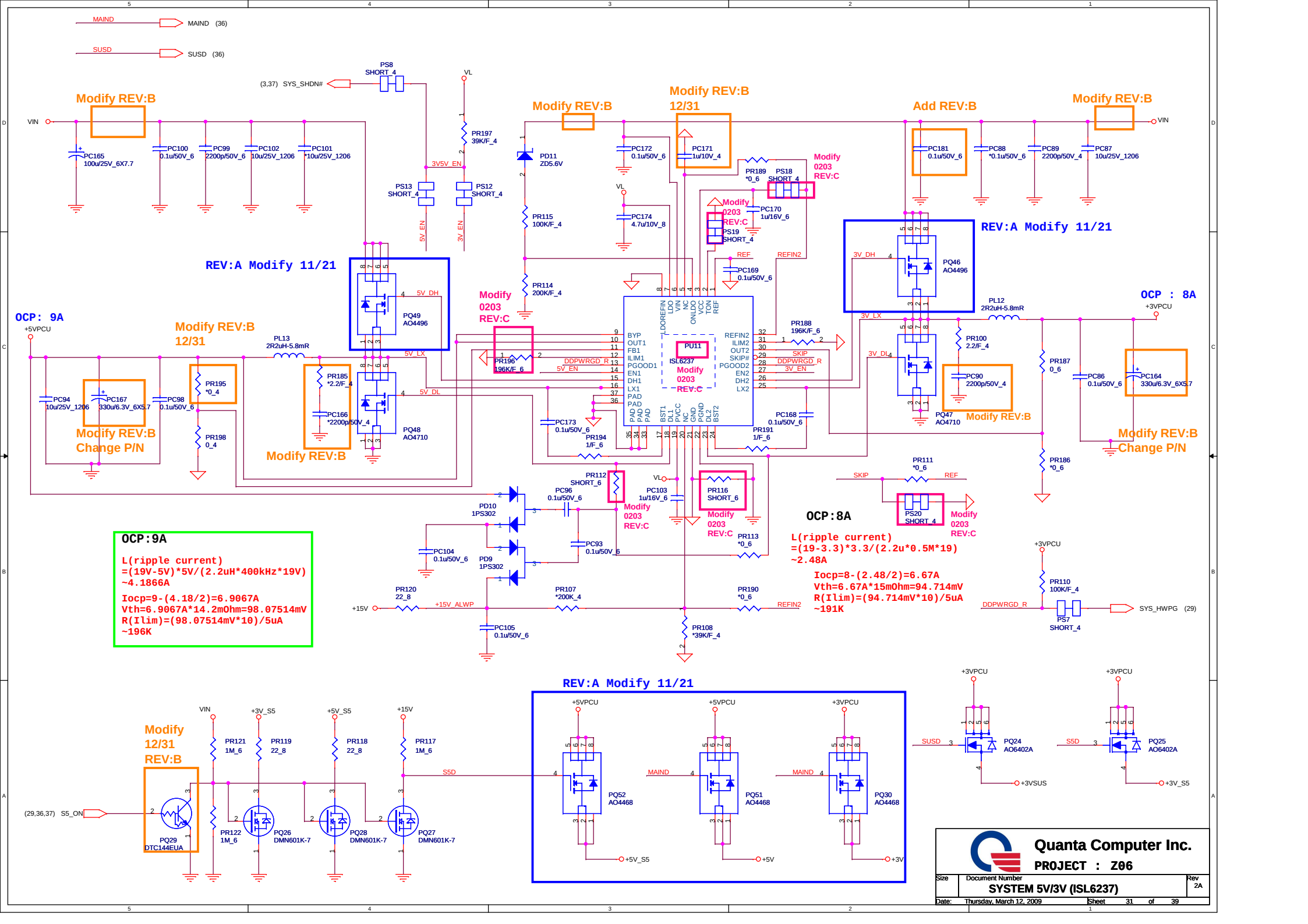
MAIND
MAIND (36)
SUSD
SUSD (36)
(3,37) SYS_SHDN#
PS8 SHORT_4
VL
VIN
Modify REV:B
PC165 100u/25V_6X7.7
PC100 0.1u/50V_6
PC99 2200p/50V_6
PC102 10u/25V_1206
PC101 *10u/25V_1206
PR197 39K/F_4
3V5V_EN
PS13 SHORT_4
PS12 SHORT_4
5V_EN
3V_EN
PD11 ZD5.6V
PR115 100K/F_4
PR114 200K/F_4
Modify REV:B
Modify REV:B 12/31
PC172 0.1u/50V_6
PC171 1u/10V_4
PC174 4.7u/10V_8
PR189 *0_6
PS18 SHORT_4
Modify 0203 REV:C
PC170 1u/16V_6
PS19 SHORT_4
Add REV:B
PC181 0.1u/50V_6
PC88 *0.1u/50V_6
PC89 2200p/50V_4
PC87 10u/25V_1206
Modify REV:B
REV:A Modify 11/21
PQ46 AO4496
3V_DH
3V_LX
3V_DL
PL12 2R2uH-5.8mR
OCP : 8A
+3VPCU
PR100 2.2/F_4
PC90 2200p/50V_4
PR187 0_6
PC86 0.1u/50V_6
PC164 330u/6.3V_6X5.7
PQ47 AO4710
Modify REV:B
Modify REV:B Change P/N
REF
REFIN2
PC169 0.1u/50V_6
PR188 196K/F_6
SKIP
DDPWRGD_R
3V_EN
PU11 ISL6237
Modify 0203 REV:C
LDOREFIN LDO VIN NC ONLDO VCC TON REF
BYP OUT1 FB1 ILIM1 PGOOD1 EN1 DH1 LX1 PAD PAD PAD PAD
REFIN2 ILIM2 OUT2 SKIP# PGOOD2 EN2 DH2 LX2
BST1 DL1 PVCC NC GND PGND DL2 BST2
OCP: 9A
+5VPCU
PL13 2R2uH-5.8mR
Modify REV:B 12/31
PC94 10u/25V_1206
PC167 330u/6.3V_6X5.7
PC98 0.1u/50V_6
PR195 *0_4
PR198 0_4
Modify REV:B Change P/N
PR185 *2.2/F_4
PC166 *2200p/50V_4
Modify REV:B
PQ49 AO4496
PQ48 AO4710
5V_DH
5V_LX
5V_DL
PC173 0.1u/50V_6
PR194 1/F_6
PC168 0.1u/50V_6
PR191 1/F_6
PR186 *0_6
PR111 *0_6
PS20 SHORT_4
Modify 0203 REV:C
PR112 SHORT_6
PR116 SHORT_6
PC96 0.1u/50V_6
PC103 1u/16V_6
PD10 1PS302
PD9 1PS302
PC104 0.1u/50V_6
PC93 0.1u/50V_6
PR113 *0_6
PR120 22_8
+15V
+15V_ALWP
PR107 *200K_4
PR190 *0_6
PC105 0.1u/50V_6
PR108 *39K/F_4
PR110 100K/F_4
PS7 SHORT_4
SYS_HWPG (29)
OCP:9A
L(ripple current) =(19V-5V)*5V/(2.2uH*400kHz*19V) ~4.1866A
Iocp=9-(4.18/2)=6.9067A
Vth=6.9067A*14.2mOhm=98.07514mV
R(Ilim)=(98.07514mV*10)/5uA
~196K
OCP:8A
L(ripple current) =(19-3.3)*3.3/(2.2u*0.5M*19) ~2.48A
Iocp=8-(2.48/2)=6.67A
Vth=6.67A*15mOhm=94.714mV
R(Ilim)=(94.714mV*10)/5uA
~191K
REV:A Modify 11/21
Modify 12/31 REV:B
VIN
+3V_S5
+5V_S5
+15V
PR121 1M_6
PR119 22_8
PR118 22_8
PR117 1M_6
S5D
(29,36,37) S5_ON
PQ29 DTC144EUA
PR122 1M_6
PQ26 DMN601K-7
PQ28 DMN601K-7
PQ27 DMN601K-7
+5VPCU
+5V
+3V
MAIND
PQ52 AO4468
PQ51 AO4468
PQ30 AO4468
+5V_S5
SUSD
S5D
PQ24 AO6402A
PQ25 AO6402A
+3VSUS
+3V_S5
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SYSTEM 5V/3V (ISL6237)
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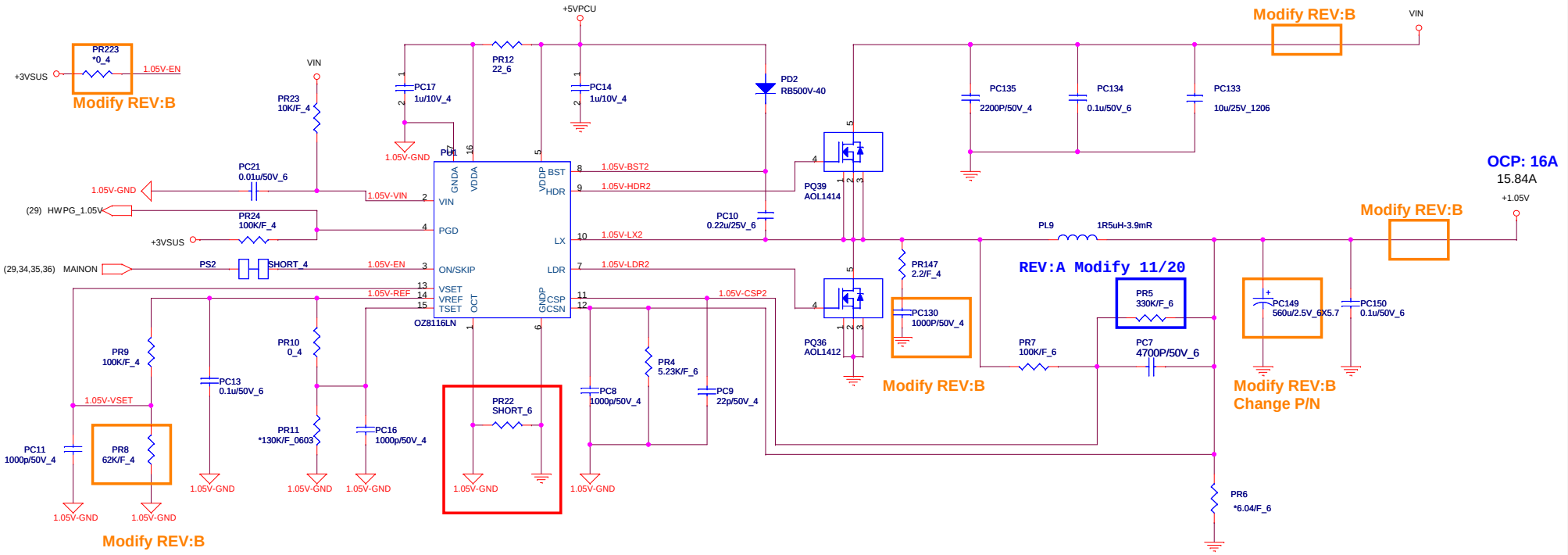
VTT 1.05V



Quanta Computer Inc.		
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Size	Document Number: +1.05V (OZ8116LN)	Rev: 2A
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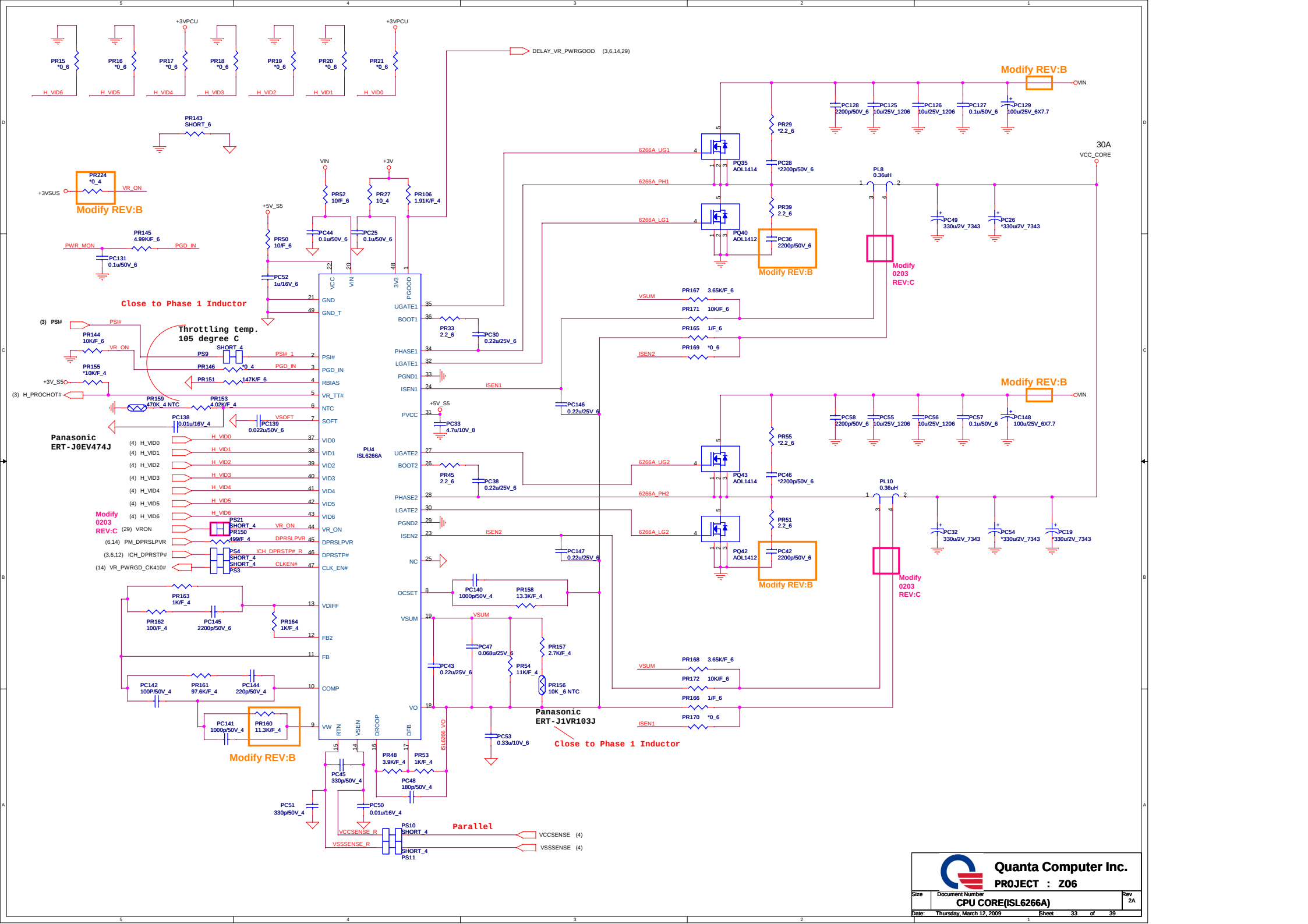
PU4
ISL6266A
Panasonic
ERT-J0EV474J
Panasonic
ERT-J1VR103J
Close to Phase 1 Inductor
Throttling temp.
105 degree C
Modify REV:B
Modify 0203 REV:C
Parallel
DELAY_VR_PWRGOOD (3,6,14,29)
VCC_CORE
30A
+3VPCU
+3VSUS
+5V_S5
+3V
VIN
PWR_MON
PGD_IN
VR_ON
PSI#
H_PROCHOT#
VSUM
ISEN1
ISEN2
6266A_UG1
6266A_PH1
6266A_LG1
6266A_UG2
6266A_PH2
6266A_LG2
VCCSENSE_R
VSSSENSE_R
VCCSENSE (4)
VSSSENSE (4)
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CPU CORE(ISL6266A)
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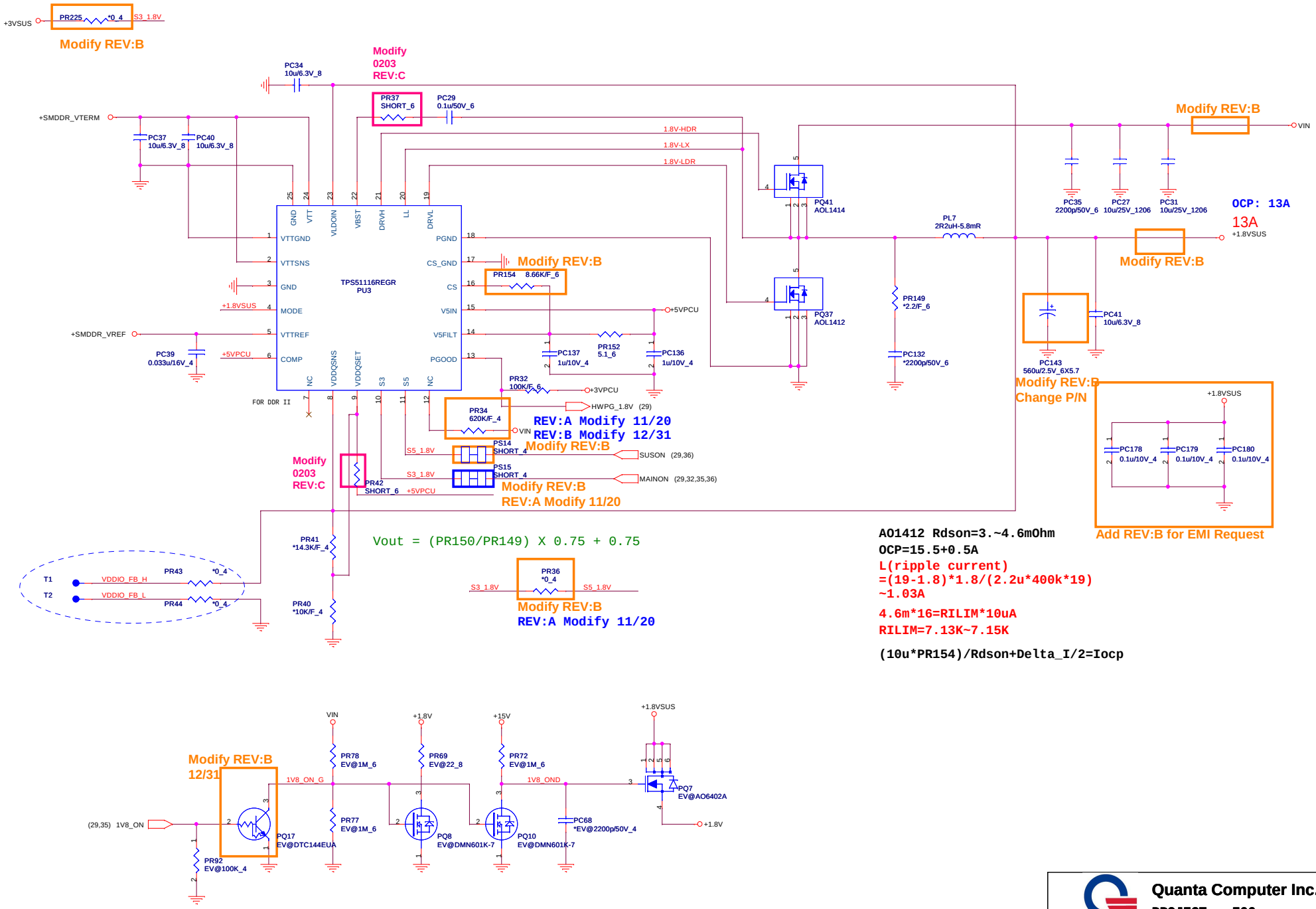

Quanta Computer Inc.			
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Size	Document Number: DDR 1.8V(TPS51116)		Rev 2A
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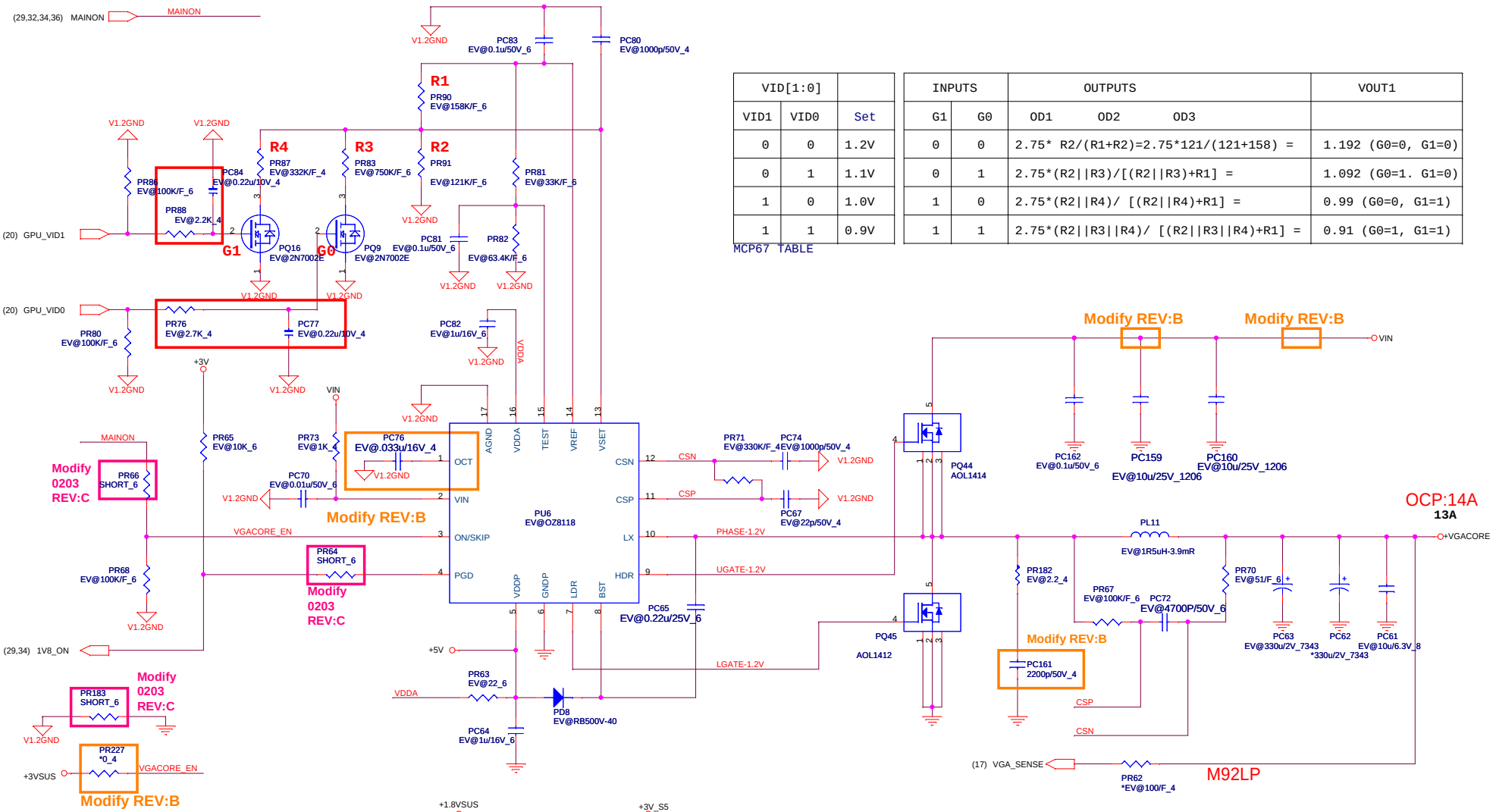

VID[1:0]		
VID1	VID0	Set
0	0	1.2V
0	1	1.1V
1	0	1.0V
1	1	0.9V

MCP67 TABLE

INPUTS		OUTPUTS	VOUT1
G1	G0	OD1 OD2 OD3	
0	0	2.75* R2/(R1+R2)=2.75*121/(121+158) =	1.192 (G0=0, G1=0)
0	1	2.75*(R2||R3)/[(R2||R3)+R1] =	1.092 (G0=1. G1=0)
1	0	2.75*(R2||R4)/ [(R2||R4)+R1] =	0.99 (G0=0, G1=1)
1	1	2.75*(R2||R3||R4)/ [(R2||R3||R4)+R1] =	0.91 (G0=1, G1=1)

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Size	Document Number	Rev
	VGA M92LP (OZ8118)	2A
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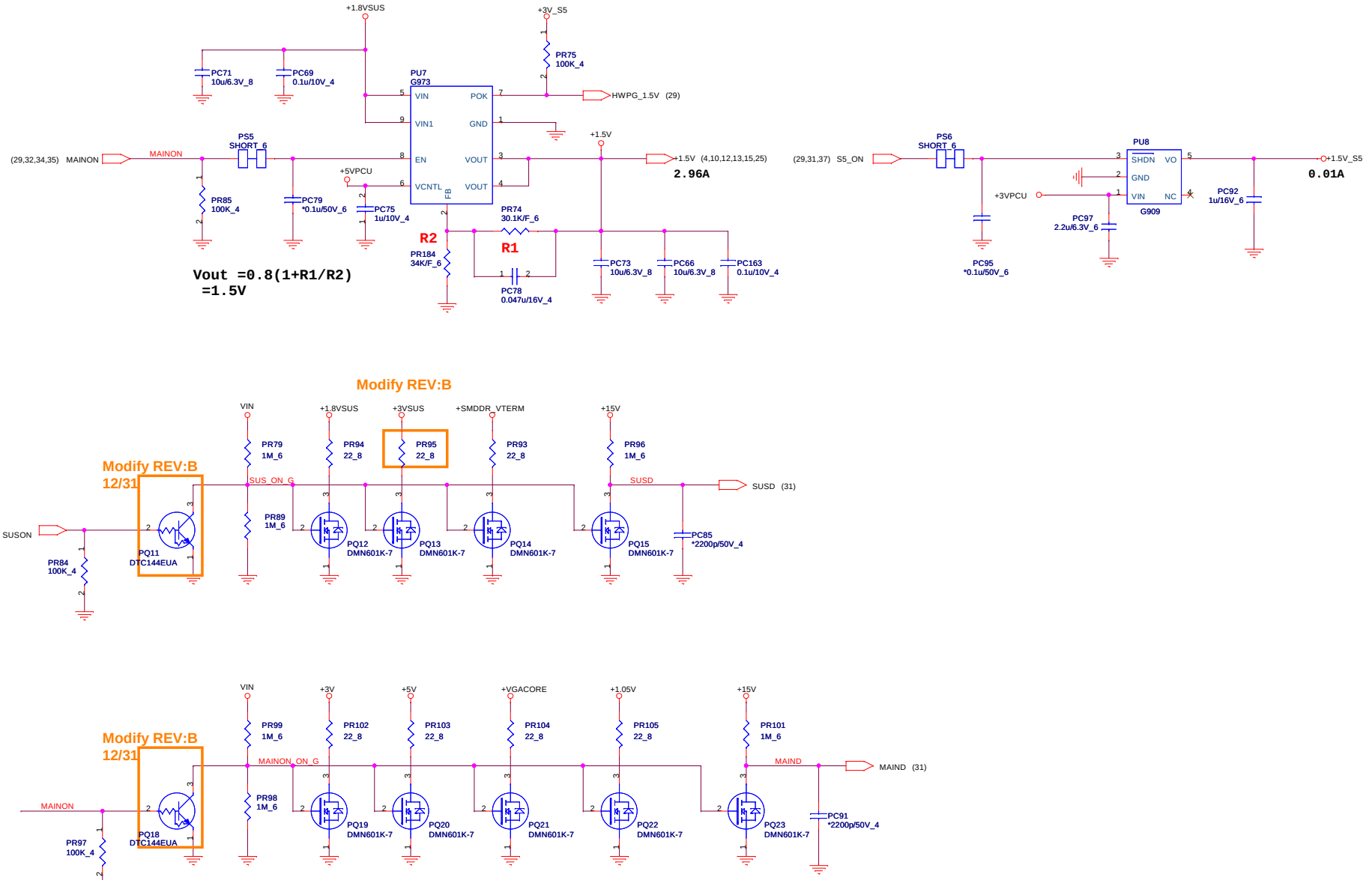

Quanta Computer Inc.		
PROJECT : Z06		
Size	Document Number: Discharge/1.5V	Rev: 2A
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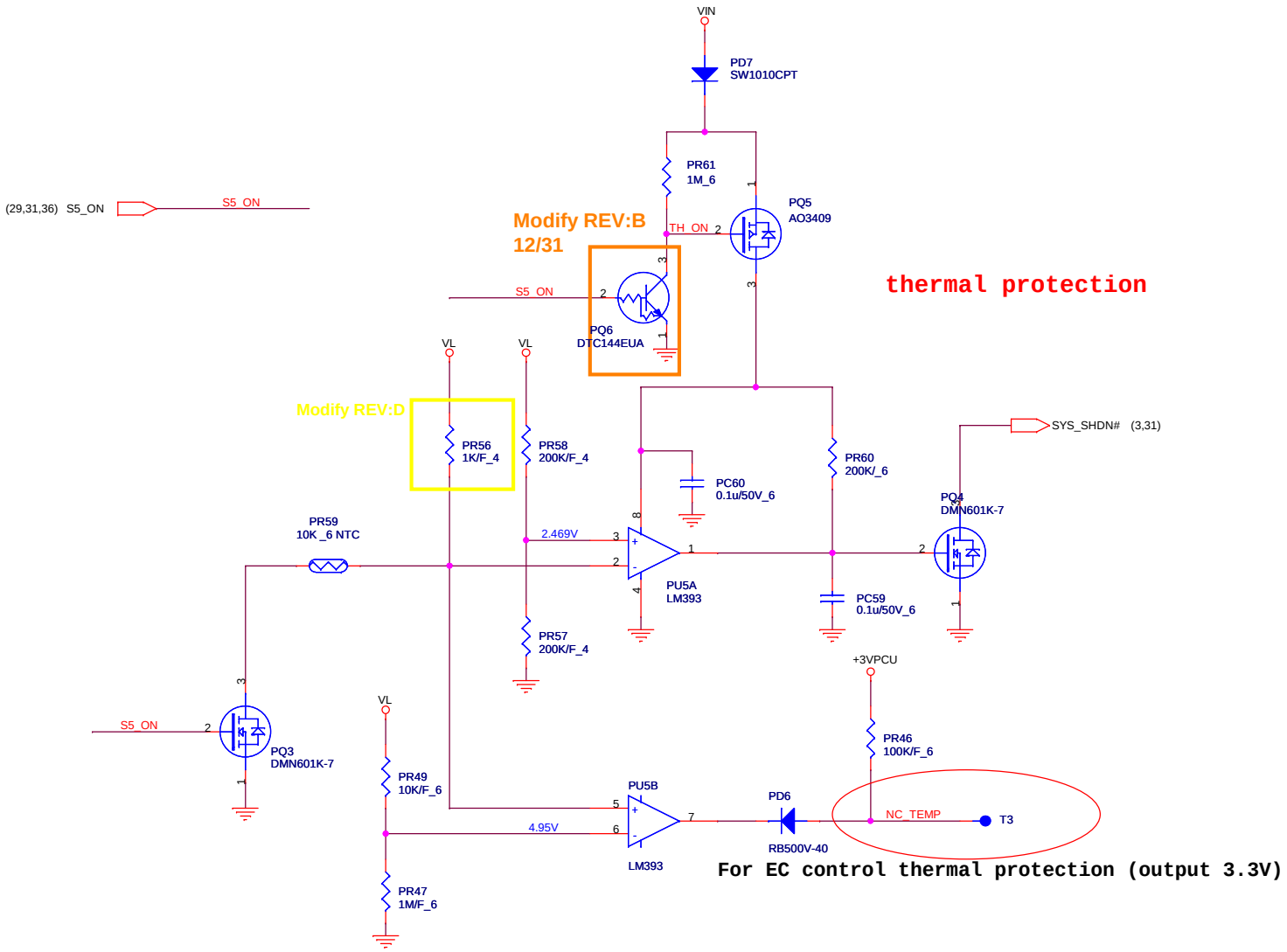

Quanta Computer Inc.		
PROJECT : Z06		
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