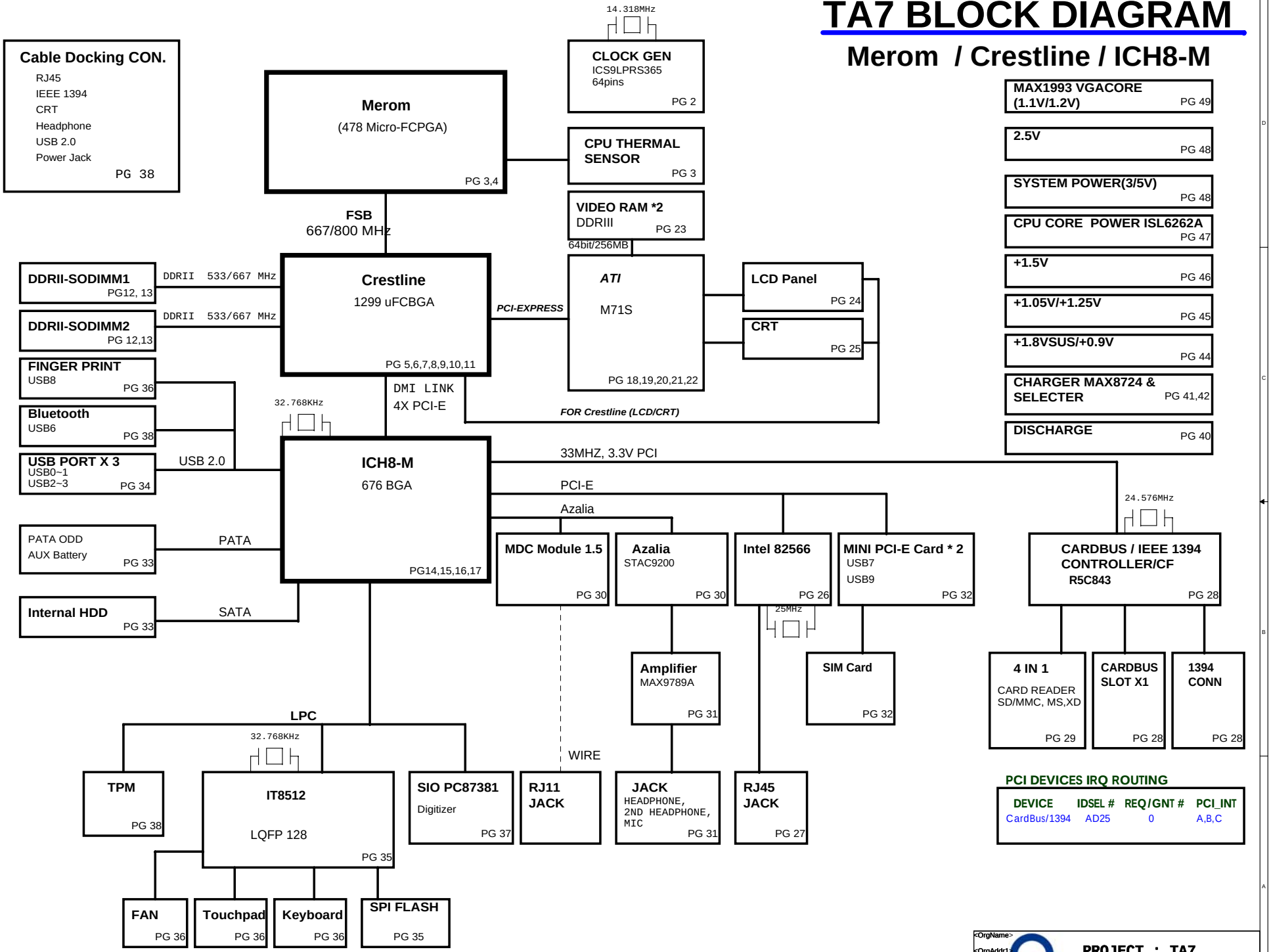
TA7 BLOCK DIAGRAM

Merom / Crestline / ICH8-M



PCI DEVICES IRQ ROUTING

DEVICE	IDSEL #	REQ/GNT #	PCI_INT
CardBus/1394	AD25	0	A,B,C

<OrgName>
<OrgAddr1>
<OrgAddr2>
<OrgAddr3>
<OrgAddr4>

PROJECT : TA7
Quanta Computer Inc.

Size	Document Number	Rev
	Block Diagram	1A

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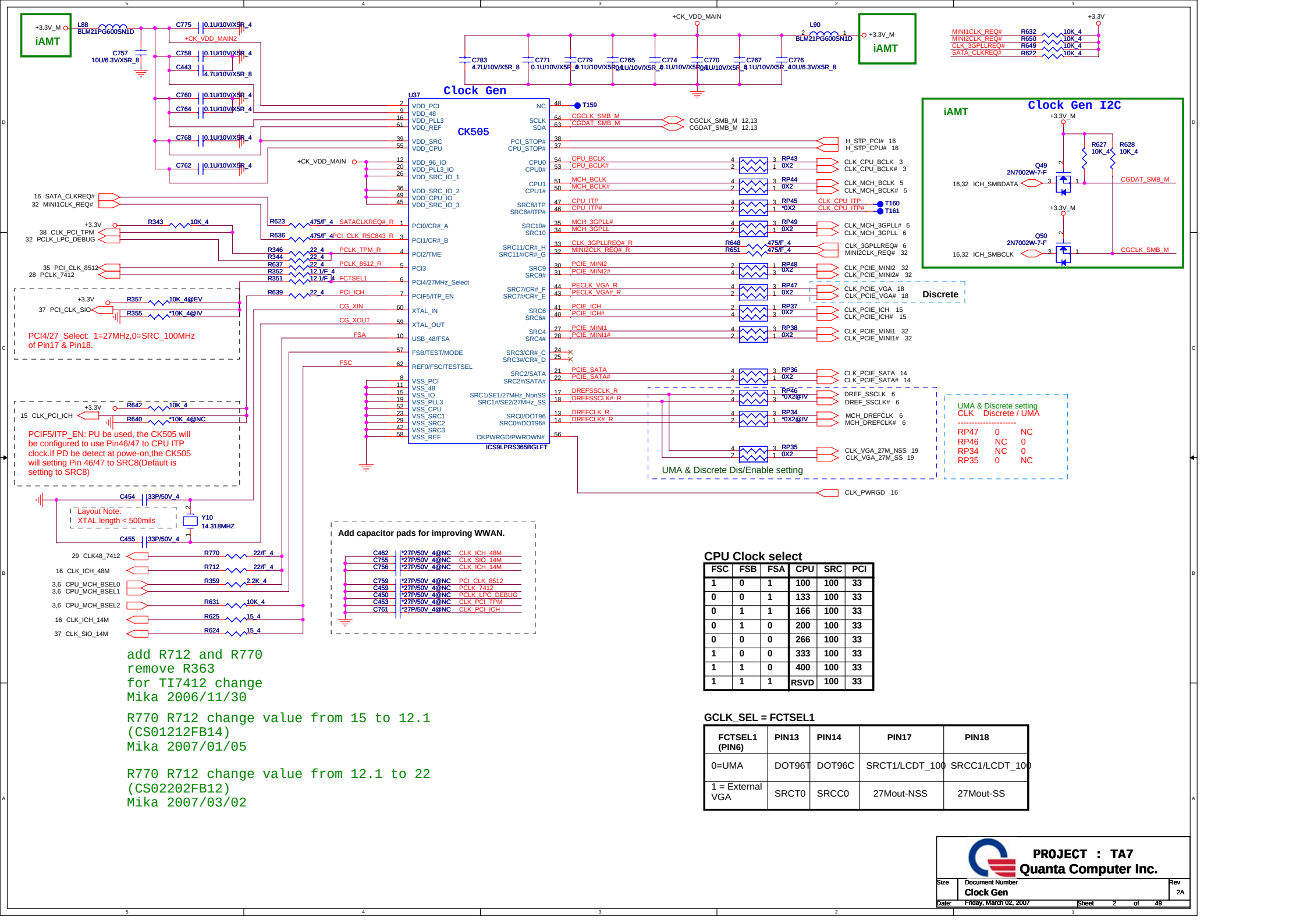

CPU Clock select

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

GCLK_SEL = FCTSEL1

FCTSEL1 (PIN6)	PIN13	PIN14	PIN17	PIN18
0=UMA	DOT96T	DOT96C	SRCT1/LCDT_100	SRCC1/LCDT_100
1 = External VGA	SRCT0	SRCC0	27Mout-NSS	27Mout-SS

PROJECT : TA7
Quanta Computer Inc.

Size	Document Number	Rev
	Clock Gen	2A
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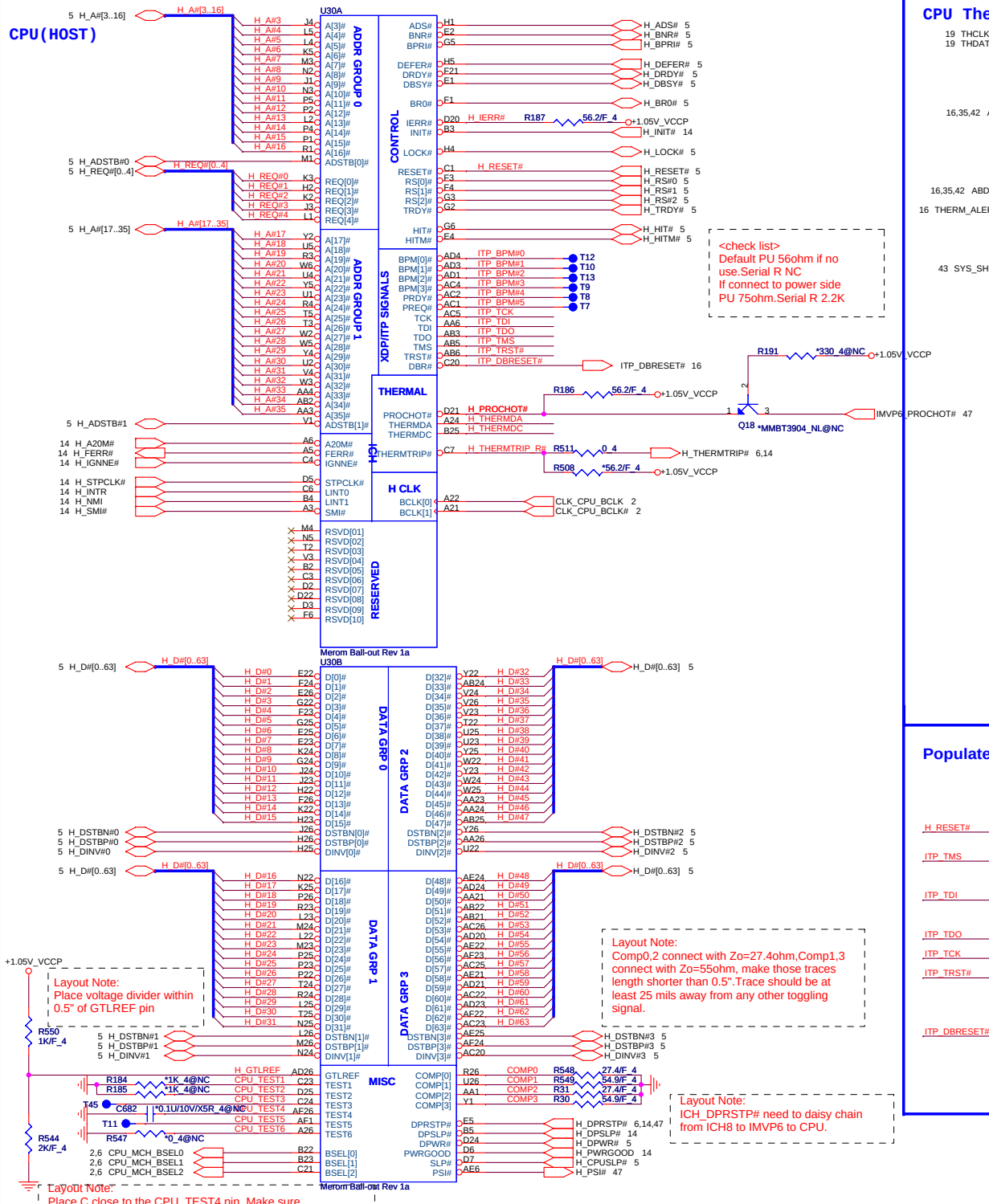
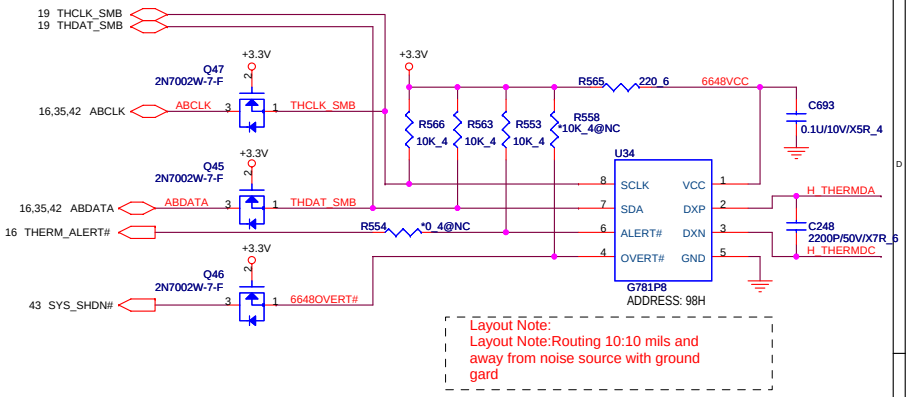
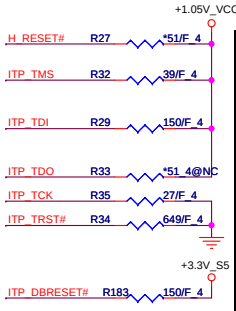
CPU(HOST)



CPU Thermal monitor



Populate ITP700Flex for bringup



ITP700 layout guidelines

Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm ± 5%	VCCP	Place the pull-up near CPU
TMS	39 ohm ± 1%	VCCP	Within 200ps of ITP connector
TRST#	500 to 680 ohm ± 5%	GND	Place the pull-up near CPU
TCK	27 ohm ± 1%	GND	Connect to TCK pin of CPU and then connect it to FBO pin of ITP connector in daisy chain. Place the pull-down near TCK0 pin of ITP connector
TDO	51 ohm ± 5%	VCCP	Place the pull-up near CPU
RESET#	22.6 ohm ± 1% series resistor and pullup 51 ohm ± 1%.	VCCP	Connect to CPURST# pin of GMCH through the series resistor placed within 200ps of ITP connector. Place the pull-up after the series resistor from ITP connector.

PROJECT : TA7
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Size	Document Number	Rev
	CPU(1 of 2)/FAN/Thermal	1A

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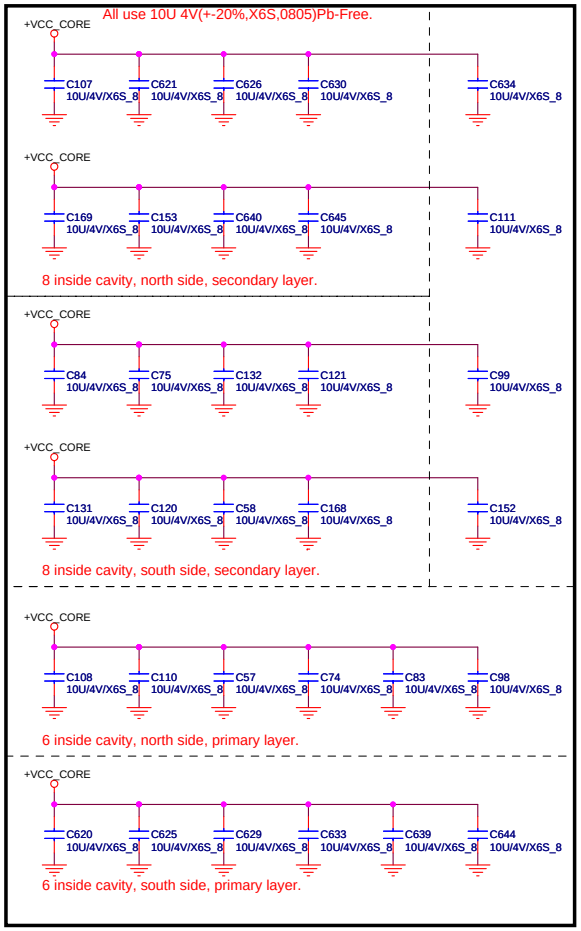
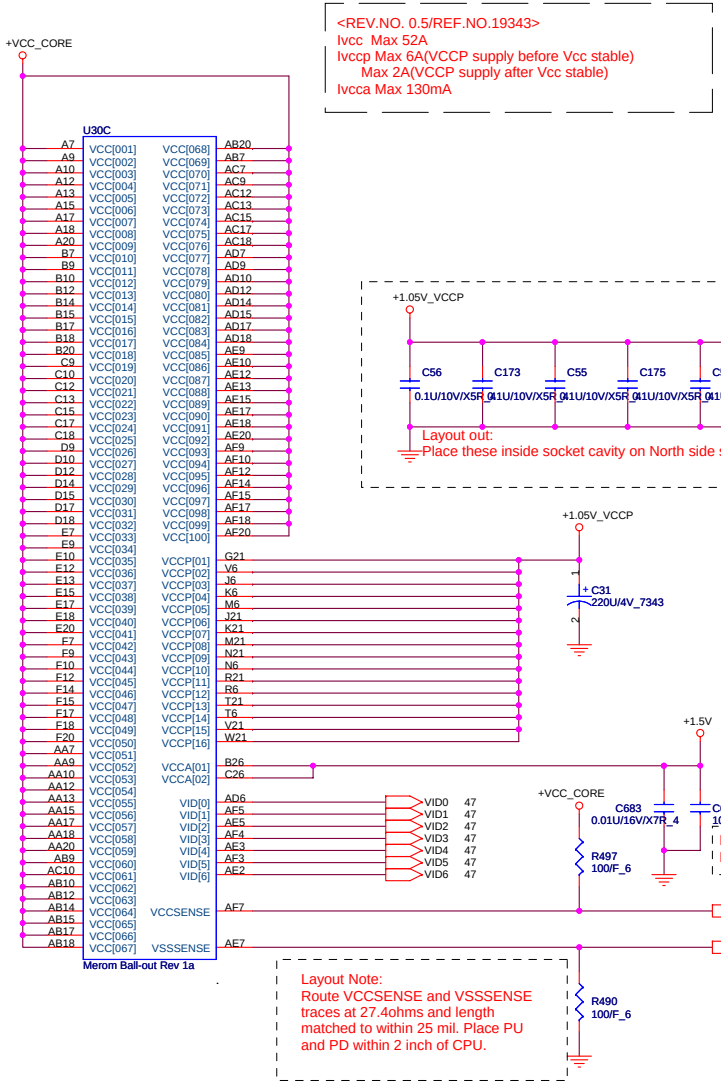
CPU(Power)





PROJECT : TA7			
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Size	Document Number		Rev
	CPU(2 of 2)		1A
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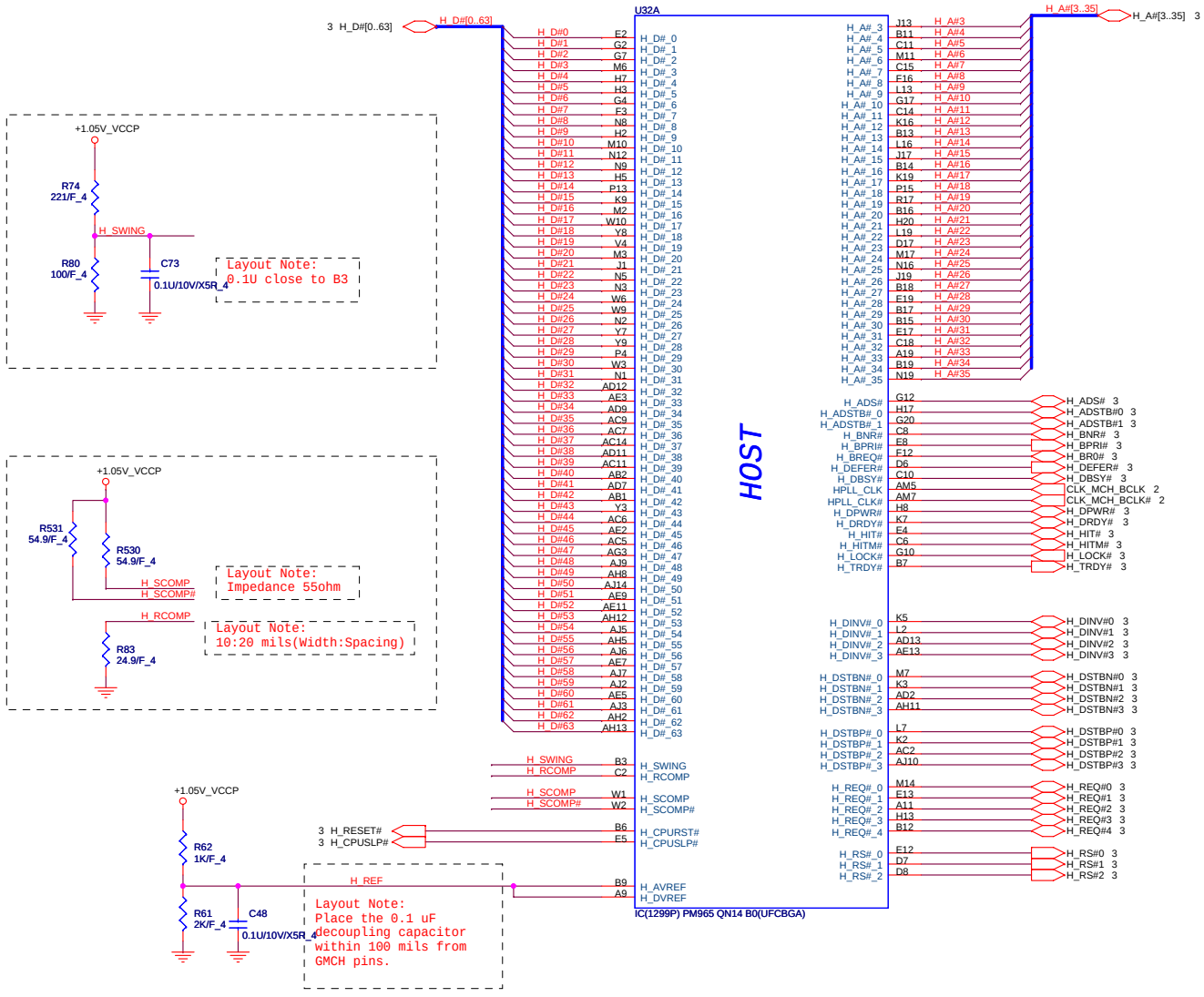
NB(HOST)



PROJECT : TA7			
Quanta Computer Inc.			
Size	Document Number		Rev
	GMCH HOST(1 of 6)		1A
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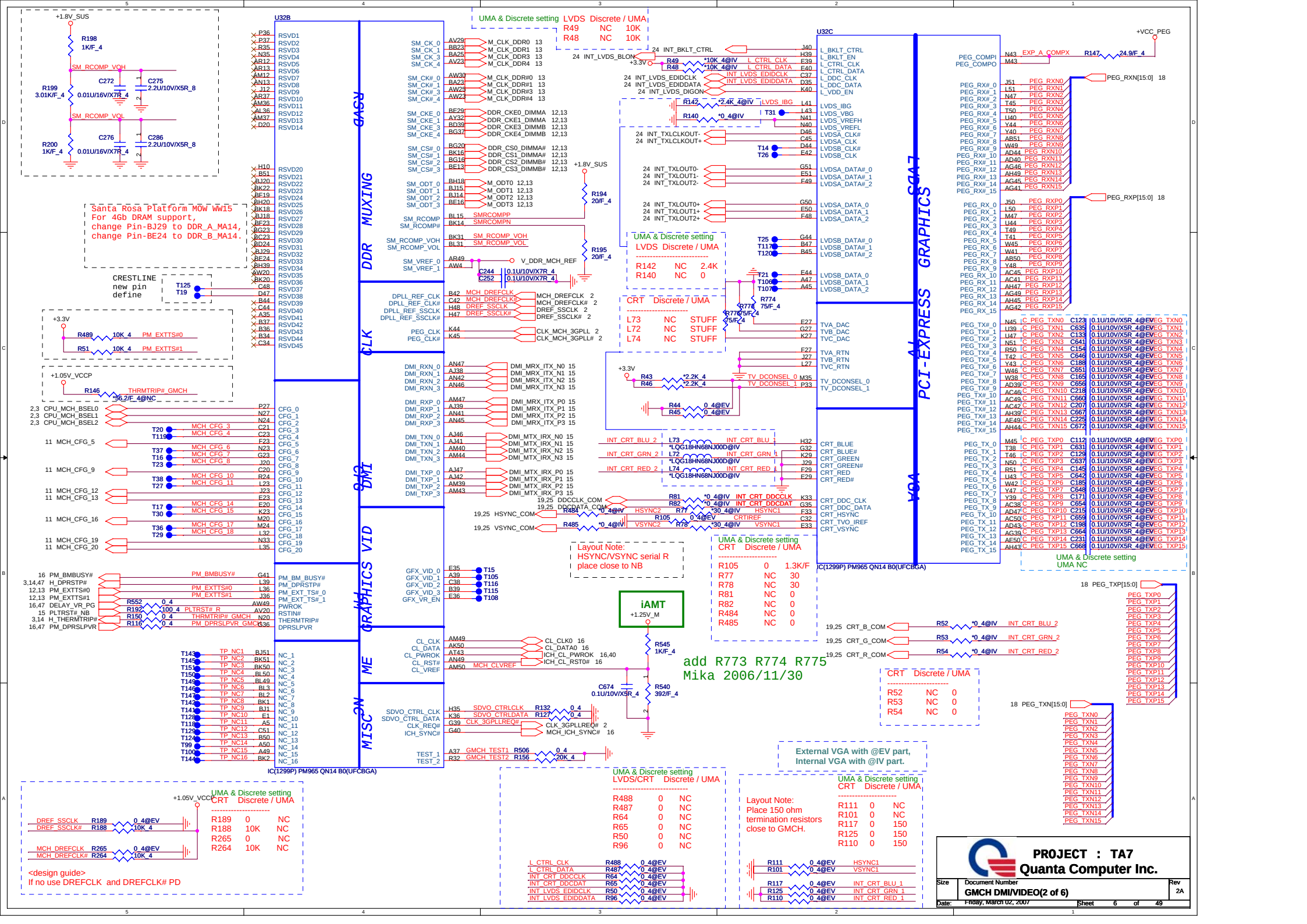
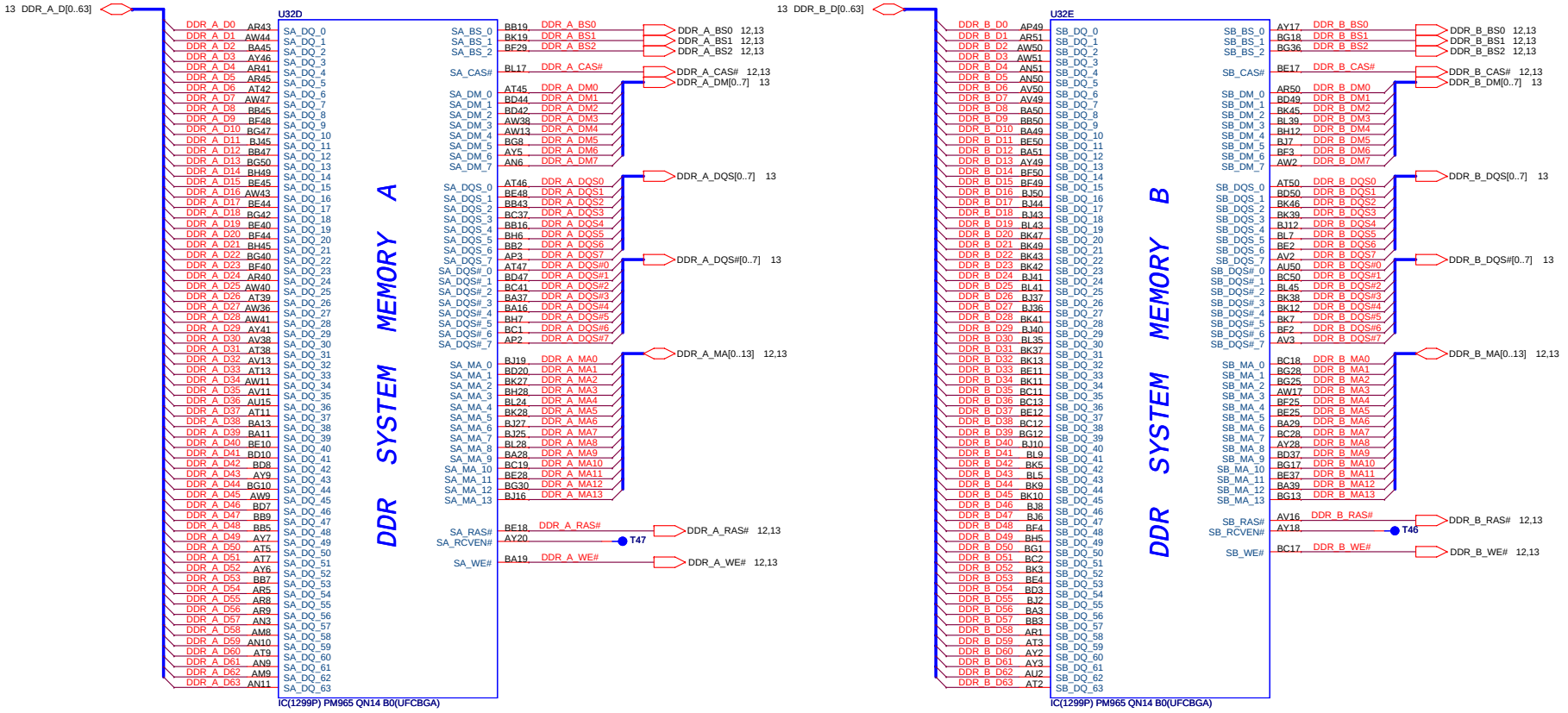

U32B
U32C
DMI
CLK
DDR MUXING
GRAPHICS VID
MISC
SM
PCI-EXPRESS GRAPHICS
VGA
Santa Rosa Platform MOW WW15
For 4Gb DRAM support,
change Pin-BJ29 to DDR_A_MA14,
change Pin-BE24 to DDR_B_MA14.
CRESTLINE
new pin
define
UMA & Discrete setting
LVDS Discrete / UMA
R49 NC 10K
R48 NC 10K
CRT Discrete / UMA
L73 NC STUFF
L72 NC STUFF
L74 NC STUFF
R142 NC 2.4K
R140 NC 0
Layout Note:
HSYNC/VSYNC serial R
place close to NB
iAMT
+1.25V_M
add R773 R774 R775
Mika 2006/11/30
External VGA with @EV part,
Internal VGA with @IV part.
Layout Note:
Place 150 ohm
termination resistors
close to GMCH.
<design guide>
If no use DREFCLK and DREFCLK# PD
IC(1299P) PM965 QN14 B0(UFCBGA)
PROJECT : TA7
Quanta Computer Inc.
GMCH DMI/VIDEO(2 of 6)
Rev 2A
Friday, March 02, 2007
Sheet 6 of 49

NB(Memory controller)



<OrgName>
<OrgAddr1>
<OrgAddr2>
<OrgAddr3>
<OrgAddr4>

PROJECT : TA7

Quanta Computer Inc.

Size	Document Number	Rev
	GMCH DDR/Strap(3 of 6)	1A

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GMCH 1.05V	current(A)	Remark
VCC Core	1.573	(1.3A for external GFX)
VCC_AXG	7.7	for integrated Gfx
VCC_AXD	0.2	
VTT	0.85	FSB VCCP
VCC_PEG	1.2	for PCIEG
VCC_AXM	0.54	for IAMT function
VCCR_RX_DMI	0.25	DMI
SUM	**12.313**	

POWER

+1.05V_VCCP

U32G

VCC CORE

VCC SM

VCC GFX NCTF

VCC GFX

VCC SM LF

+VCC_AXG

+1.8V_SUS

IVCCSM supply current 1 channel 1.615A 2 channel 3.138A

C246 0.1U/10V/X5R_4

C309 220U/4V_7343

C266

C258 22U/4V/X6S_8

22U/4V/X6S_8

Layout Note: Place C125 where LVDS and DDR2 taps.

change C309 value from 330U/2V to 220U/4V
Mika 2006/12/26

IC(1299P) PM965 QN14 B0(UFCBGA)

+3.3V

R496 10_4

+VCC_GMCH_L

D26 CH751H-40PT

Ivcc (External GFX 1.310 A, integrate 1.572 A)

Layout Note: 370 mils from edge.

C604 220U/2.5V_7343

C650 22U/4V/X6S_8

C653 0.22U/6.3V/X5R_4

C172 0.22U/6.3V/X5R_4

C164 0.1U/10V/X5R_4

Layout Note: Inside GMCH cavity.

Ivcc_AXG Graphics core supply current 7.7A

Layout Note: 370 mils from edge.

R84 *HI0805R800R-5A

R85 *HI0805R800R-5A

C139 *330U/2V_7343@NC

C181 *330U/2V_7343@NC

C249 *330U/2V_7343@NC

C104 *330U/2V_7343@NC

UMA & Discrete setting

C196 *0.1U/10V/X5R_4@IV

C187 0.1U/10V/X5R_4@IV

C228 *0.47U/10V/X7R_6@IV

C163 *1U/6.3V/X5R_6@IV

C156 *22U/4V/X6S_8@IV

C223 0_8@EV

UMA & Discrete setting

Layout Note: Inside GMCH cavity for VCC_AXG.

UMA & Discrete setting

VCC_AXG Discrete / UMA

R84	NC	STUFF
R85	NC	STUFF
C104	NC	NC
C249	NC	NC
C181	NC	330U
C139	NC	330U
C196	NC	0.1U
C187	NC	0.1U
C228	NC	0.47U
C163	NC	1U
C156	NC	22U
C223	0	10U

External VGA with @EV part, Internal VGA with @IV part.

Ivcc_AXM Controller supply current 540mA

iAMT +1.05V_M

Layout Note: Inside GMCH cavity for VCC_AXG.

C222 0.1U/10V/X5R_4

C234 0.1U/10V/X5R_4

C210 0.1U/10V/X5R_4

C235 22U/4V/X6S_8

C240 0.22U/10V/X7R_6

C220 0.22U/10V/X7R_6

Layout Note: Place close to GMCH edge.

U32F

VCC NCTF

VSS NCTF

VSS SCB

VCC AXM

VCC AXM NCTF

iAMT +1.05V_M

IC(1299P) PM965 QN14 B0(UFCBGA)

C241 0.1U/10V/X5R_4

C254 1U/10V/X5R_4

C261 22U/10V/X7R_6

C262 0.22U/6.3V/X5R_4

C269 0.47U/10V/X7R_6

C251 1U/6.3V/X5R_6

C256 1U/6.3V/X5R_6

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	GMCH Power-1(4 of 6)	1A
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UMA & Discrete setting

PLL	Discrete / UMA	
L13	NC	10uH
C38	NC	470U
C72	0	0.1U
L77	NC	10uH
C600	NC	470U
C102	0	0.1U

UMA & Discrete setting

CRT	Discrete / UMA	
R55	NC	0
C42	NC	0.1U
R59	NC	0
R124	0	22nF
C610	NC	10U
L66	NC	STUFF
C609	NC	0.1U
R504	NC	0
R87	0	22nF

External VGA with @EV part,
Internal VGA with @IV part.

IVCC_SYNC current 0.01A

IVCCA_DPLLA~B current 0.08A

IVCCA_HPLL current 0.05A

IVCCA_MPLL current 0.15A

IVCCA_LVDS current 0.01A

UMA & Discrete setting

LVDS	Discrete / UMA	
R95	0	1000P

IVCCA_PEG_BG current 0.04A

change C306 value
from 100U/10V to 220U/4V
Mika 2006/12/26

IVCCD_CRT current 0.06A

IVCCD_TVDAC current 0.06A

IVCC_QDAC current 0.005A

IVCCD_HPLL current 0.25A

IVCCA/D_PEG_PLL current 0.1A

UMA & Discrete setting

CRT	Discrete / UMA	
L18	NC	100ohm
C60	NC	0.1U
R72	NC	0
R148	0	1UF
R133	0	NC
R141	NC	0

IVCCD_LVDS current 0.15A

UMA & Discrete setting

LVDS	Discrete / UMA	
R58	NC	0
C71	0	1U
C50	NC	NC
C80	NC	1000P

If:SDVO Disabled,VCCD_LDVS to GND.
If:SDVO Enabled,VCCD_LDVS to +1.8V.

U32H
IC(1299P) PM965 QN14 B0(UFCBGA)

CRT: VCCSYNC, VCCA_CRT_DAC_1, VCCA_CRT_DAC_2, VCCA_DAC_BG, VSSA_DAC_BG
PLL: VCCA_DPLLA, VCCA_DPLLB, VCCA_HPLL, VCCA_MPLL
LVDS: VCCA_LVDS, VSSA_LVDS
PEG: VCCA_PEG_BG, VSSA_PEG_BG, VCCA_PEG_PLL
SM: VCCA_SM_1..5, VCCA_SM_7..11, VCCA_SM_NCTF_1, VCCA_SM_NCTF_2
CK: VCCA_SM_CK_1, VCCA_SM_CK_2
TV: VCCA_TVA_DAC_1, VCCA_TVA_DAC_2, VCCA_TVB_DAC_1, VCCA_TVB_DAC_2, VCCA_TVC_DAC_1, VCCA_TVC_DAC_2
TV/CRT: VCCD_CRT, VCCD_TVDAC, VCCD_QDAC, VCCD_HPLL, VCCD_PEG_PLL
LVDS: VCCD_LVDS_1, VCCD_LVDS_2

POWER
VTT: VTT_1..22
AXD: VCC_AXD_1..6, VCC_AXD_NCTF
AXF: VCC_AXF_1..3, VCC_DMI
SM CK: VCC_SM_CK_1..4
HV: VCC_HV_1, VCC_HV_2
PEG: VCC_PEG_1..5
DMI: VCC_RXR_DMI_1, VCC_RXR_DMI_2
VTTLF: VTTLF1, VTTLF2, VTTLF3

+3V_VCC_HV

Ivtt_FSB core supply current 0.85A

Ivcc_AXD current 0.25A

Ivcc_AXF current 0.35A

Ivcc_DMI current 0.1A

Ivcc_SM_CK current 0.2A

IVCC_TX_LVDS current 0.1A

IVCC_HV current 0.1A

UMA & Discrete setting

LVDS	Discrete / UMA	
L65	NC	1UH
C34	NC	220U
R97	0	1000P

Ivcc_PEG PCI-E current 1.2A

Ivcc_RX_DMI current 0.25A

40 mil wide

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Quanta Computer Inc.	
Size	Document Number: GMCH Power-2(5 of 6)
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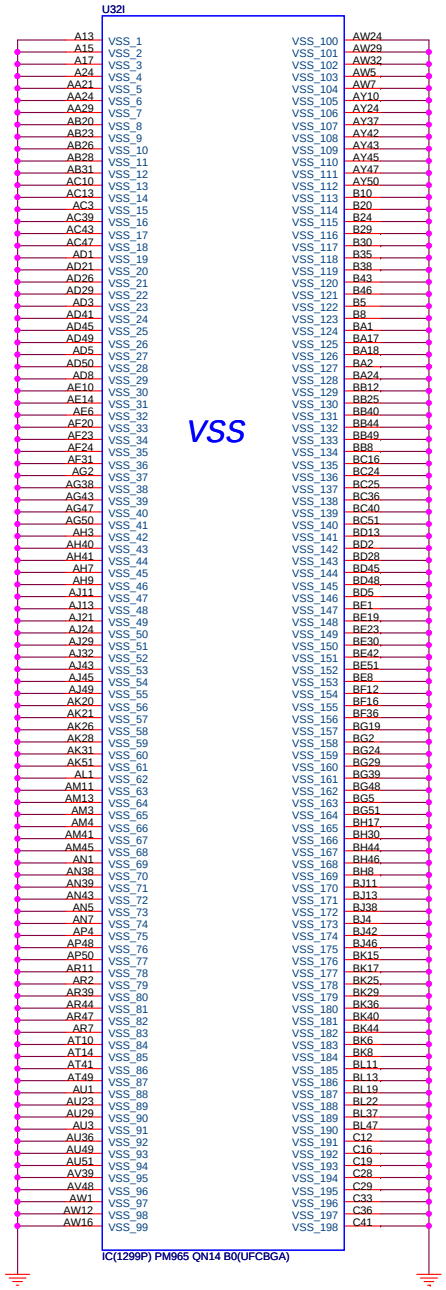
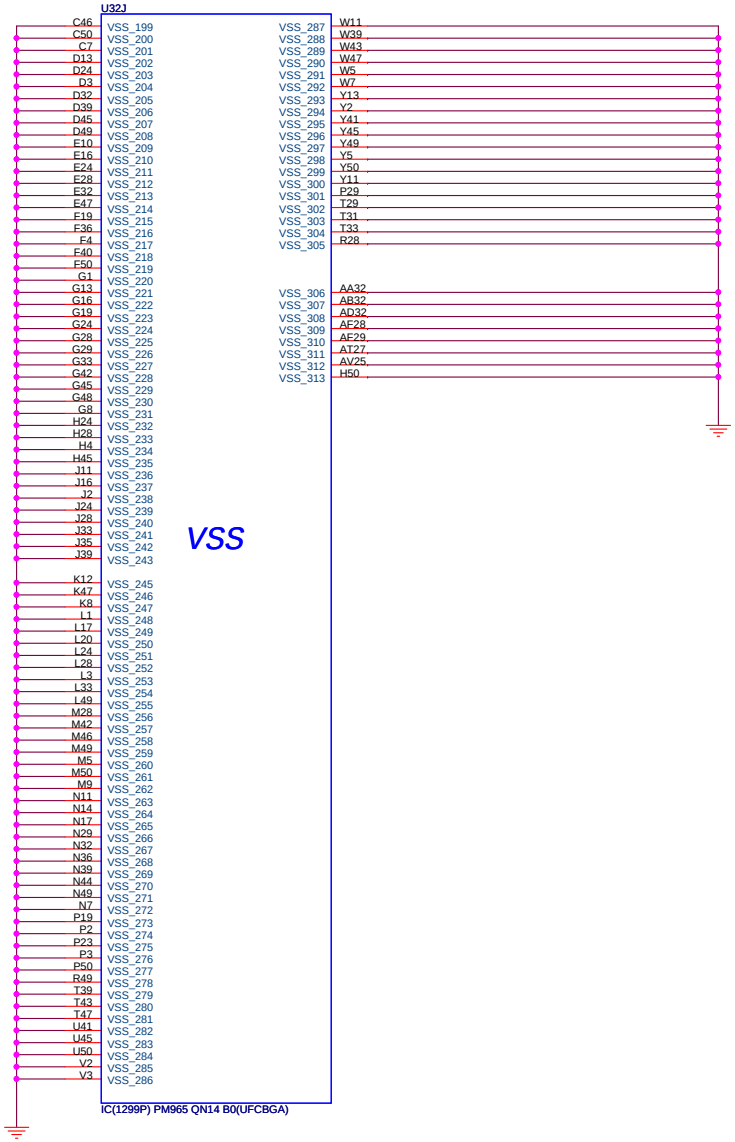
NB(Power-3)





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Strap table

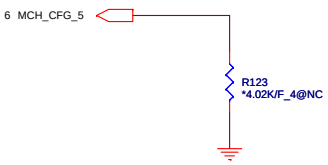
All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal

CFG[17:3] Have internal Pull-up
CFG[18:19] Have internal Pull-down
Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Low power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIe concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

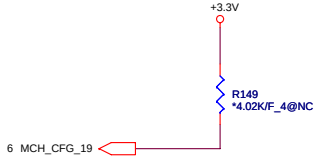
DMI X2 Select

MCH_CFG_5	Low = DMIX2 High = IDMIX4(Default)



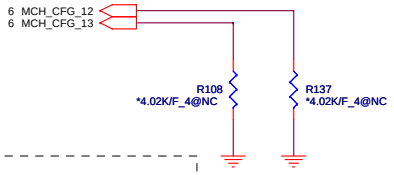
DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane



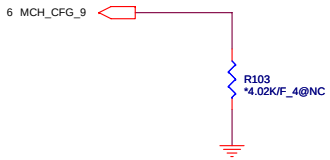
XOR /ALLz /Clock Un-gating

MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)



PCI Express Graphics

MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)

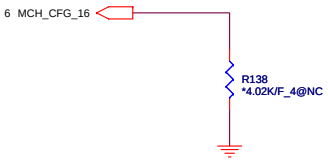


SDVO Present

Strap define at External DVI control page

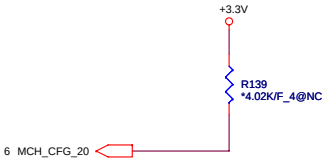
FSB Dynamic ODT

MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)



SDVO/PCIE Concurrent operation

MCH_CFG_20	Low = Only SDVO or PCIE X1 is operational(Default) High = SDVO andPCIE X1 are operating simultaneously via the PEG port



Layout Note:
Location of all MCH_CFG strap resistors needs to be close to minmize stub.

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Quanta Computer Inc.

Size	Document Number	Rev
	GMCH Strap Table	1A
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DDR2 Dual channel A/B PU

DDRII A CHANNEL

+0.9V_DDR_VTT

Layout note: Place 1 cap close to every 1 R-pack terminated to SMDDR_VTERM.

C353 C406 C408 C389 C363 C409 C362 C405 C404 C426 C388 C350 C386

0.1U/10V/X5R_4 0.1U/10V/X5R_4 0.1U/10V/X5R_4 0.1U/10V/X5R_4 0.1U/10V/X5R_4 0.1U/10V/X5R_4 0.1U/10V/X5R_4 0.1U/10V/X5R_4 0.1U/10V/X5R_4 0.1U/10V/X5R_4 0.1U/10V/X5R_4 0.1U/10V/X5R_4

DDRII B CHANNEL

+0.9V_DDR_VTT

C390 C428 C427 C403 C351 C352 C354 C349 C425 C387 C407 C402 C429

0.1U/10V/X5R_4 0.1U/10V/X5R_4 0.1U/10V/X5R_4 0.1U/10V/X5R_4 0.1U/10V/X5R_4 0.1U/10V/X5R_4 0.1U/10V/X5R_4 0.1U/10V/X5R_4 0.1U/10V/X5R_4 0.1U/10V/X5R_4 0.1U/10V/X5R_4 0.1U/10V/X5R_4

+0.9V_DDR_VTT

7,13 DDR_A_MA[0..13]

6,13 M_ODT0

6,13 DDR_CKE1_DIMMA

7,13 DDR_A_BS0

7,13 DDR_A_RAS#
7,13 DDR_A_BS1

7,13 DDR_A_WE#
7,13 DDR_A_CAS#

6,13 DDR_CS0_DIMMA#

6,13 DDR_CS1_DIMMA#
6,13 M_ODT1

6,13 DDR_CKE0_DIMMA
7,13 DDR_A_BS2

M_ODT0 DDR_A_MA13	RP32	56X2	RP17	56X2	DDR_B_BS1 DDR_B_MA0	DDR_B_BS1 7,13	
DDR_A_MA8 DDR_A_MA5	RP22	56X2	RP10	56X2	DDR_B_MA5 DDR_B_MA3		
DDR_A_MA3 DDR_A_MA1	RP23	56X2	RP9	56X2	DDR_B_MA1 DDR_B_MA8		
DDR_A_MA11	RP27	56X2	RP16	56X2	DDR_B_MA4 DDR_B_MA2		
DDR_A_MA10 DDR_A_BS0	RP24	56X2	RP8	56X2	DDR_B_MA12 DDR_B_MA9		
DDR_A_MA7 DDR_A_MA6	RP28	56X2	RP15	56X2	DDR_B_MA7 DDR_B_MA6		
DDR_A_MA2 DDR_A_MA4	RP29	56X2	RP7	56X2		DDR_B_BS2 7,13 DDR_CKE3_DIMMB 6,13	
DDR_A_RAS# DDR_A_BS1	RP31	56X2	RP18	56X2	DDR_B_RAS# DDR_B_MA13	DDR_B_RAS# 7,13	
DDR_A_MA9 DDR_A_MA12	RP21	56X2	RP12	56X2	DDR_B_WE# DDR_B_CAS#	DDR_B_WE# 7,13 DDR_B_CAS# 7,13	
DDR_A_WE# DDR_A_CAS#	RP25	56X2	RP11	56X2	DDR_B_MA10 DDR_B_BS0	DDR_B_BS0 7,13	
DDR_A_MA0	RP30	56X2	RP19	56X2	M_ODT2	M_ODT2 6,13 DDR_CS2_DIMMB# 6,13	
	RP26	56X2	RP13	56X2		M_ODT3 6,13 DDR_CS3_DIMMB# 6,13	
	RP20	56X2	RP14	56X2	DDR_B_MA11	DDR_CKE4_DIMMB 6,13	

Please these resistor closely DIMMA,all trace length<750 mil.

Please these resistor closely DIMMB,all trace length<750 mil.

DDR2 Thermal Sensor SO-DIMM 0 & 1

Uninstall

+3.3V_M

R293 *220_6@NC

C431 *0.1U/10V/X5R_4@NC

U19

2,13 CGCLK_SMB_M
2,13 CGDAT_SMB_M
6,13 PM_EXTTS#0
6,13 PM_EXTTS#1

SCLK VCC
SDA DXP
ALERT# DXN
OVERT# GND

LM86_3V
DDR_THERMDA
DDR_THERMDC

C417 *1000P/16V/X7R_4

Q24 *MMBT3904_NL@NC

R279 *0_4@NC

*LM86CIMM@NC

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A is required to route to Top SoDIMM for AMT to function.This will need to change for M08

DDR2 Dual channel A/B CONN

CN33

DDR2_SODIMM
H 9.2

PC4800 DDR2 SDRAM SO-DIMM (200P)

CKE 0,1
CLOCK 0,1

SMbus address A0

CN31

2-1734073-2
H 5.2

PC4800 DDR2 SDRAM SO-DIMM (200P)

CKE 3,4
CLOCK 3,4

SMbus address A4

Place these Caps near So-Dimm1.

Place these Caps near So-Dimm2.

iAMT

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RTC

SB Strap

+RTC_CELL — R338 332K/F_4 — ICH_INTVRMEN — R339 *0_4@NC

ICH8M Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)

ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)

+RTC_CELL — R353 332K/F_4 — LAN100_SLP — R345 *0_4@NC

ICH8M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)

ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)

+RTC_CELL, +3.3V_ALW — D24 CH501H-40PT — C440 1U/10V/X5R_6

VCCRTC_4 — D23 CH501H-40PT — R331 20K_4 — G7 *SHORT_PAD — C438 1U/10V/X5R_6

R310 1K_4 — R358 1M/F_4 — CN25 ML1220-SOCKET

VCCRTC_3

+5V_ALW — R562 1.2K_4 — VCCRTC_1 — R556 1K_4 — VCCRTC_2 — Q44 MMBT3904_NL — R560 4.7K_4 — R559 15K_4

+3.3V_S5 — R614 *10K_4@NC — ENERGY_DET

C444 18P/50V_4 — Y9 32.768KHZ — R341 10M_6 — C447 18P/50V_4

ICH_RTCX1 AG25 — ICH_RTCX2 AF24 — RTCRST# AF23 — SM_INTRUDER# AD22 — ICH_INTVRMEN AF25 — LAN100_SLP AD21

26 GLAN_CLK — B24 GLAN_CLK

26 LAN_RSTSYNC — D22 LAN_RSTSYNC

26 LAN_RXD0 — C21 LAN_RXD0
26 LAN_RXD1 — B21 LAN_RXD1
26 LAN_RXD2 — C22 LAN_RXD2

26 LAN_TXD0 — D21 LAN_TXD0
26 LAN_TXD1 — E20 LAN_TXD1
26 LAN_TXD2 — C20 LAN_TXD2

27 ENERGY_DET — ENERGY_DET — AH21 GLAN_DOCK#/GPIO13

+1.5V_PCIE_ICH — R383 24.9/F_4 — GLAN_COMP_SB — D25 GLAN_COMPI — C25 GLAN_COMPO

ACZ_BIT_CLK — AJ16 HDA_BIT_CLK
ACZ_SYNC — AJ15 HDA_SYNC
ACZ_RST# — AE14 HDA_RST#

30 ICH_AZ_CODEC_SDIN0 — AJ17 HDA_SDIN0
30 ICH_AZ_MDC_SDIN1 — AH17 HDA_SDIN1
T157 — ACZ_SDIN2 — AH15 HDA_SDIN2
T68 — ACZ_SDIN3 — AD13 HDA_SDIN3

R324 *10K_4 — ACZ_SDOUT — AE13 HDA_SDOUT

+3.3V — R325 10K_4 — GPIO33 — AE10 HDA_DOCK_EN#/GPIO33
R330 10K_4 — GPIO34 — AG14 HDA_DOCK_RST#/GPIO34

33 SATA_LED# — SATA_LED# — AE10 SATALED#

33 SATA_RX0- — AF6 SATA0RXN
33 SATA_RX0+ — AF5 SATA0RXP
SATA_TX0- C — AH5 SATA0TXN
SATA_TX0+ C — AH6 SATA0TXP

R630 10K_4 — R638 10K_4 — AG3 SATA1RXN — AG4 SATA1RXP — AJ4 SATA1TXN — AJ3 SATA1TXP

33 SATA_RX2- — AF2 SATA2RXN
33 SATA_RX2+ — AF1 SATA2RXP
SATA_TX2- C — AE4 SATA2TXN
SATA_TX2+ C — AE3 SATA2TXP

2 CLK_PCIE_SATA# — AB7 SATA_CLKN
2 CLK_PCIE_SATA — AC6 SATA_CLKP

R635 24.9/F_4 — SATA_BIAS — AG1 SATARBIAS# — AG2 SATARBIAS

Layout Note: L<500mils

ICH8M REV 1.0

U39A

RTC: RTCX1, RTCX2, RTCRST#, INTRUDER#, INTVRMEN, LAN100_SLP

LPC: FWH0/LAD0 E5 — LPC_LAD0 32,35,37,38
FWH1/LAD1 F5 — LPC_LAD1 32,35,37,38
FWH2/LAD2 G8 — LPC_LAD2 32,35,37,38
FWH3/LAD3 F6 — LPC_LAD3 32,35,37,38
FWH4/LFRAME# C4 — LPC_LFRAME# 32,35,37,38
LDRQ0# G9 — LPC_LDRQ0# 32,37
LDRQ1#/GPIO23 E6 — LDRQ#1 — T167

LAN / GLAN: A20GATE AF13 — GATEA20 — GATEA20 35
A20M# AG26 — H_A20M# 3
DPRSTP# AF26 — H_DPRSTP# — H_DPRSTP# 3,6,47
DPSLP# AE26 — H_DPSLP# — H_DPSLP# 3
FERR# AD24 — H_FERR# — H_FERR# 3
CPUPWRGD/GPIO49 AG29 — H_PWRGOOD 3
IGNNE# AF27 — H_IGNNE# 3
INIT# AE24 — H_INIT# 3
INTR AC20 — H_INTR 3
RCIN# AH14 — RCIN# — RCIN# 35
NMI AD23 — H_NMI 3
SMI# AG28 — H_SMI# — H_SMI# 3
STPCLK# AA24 — H_STPCLK# 3
THRMTRIP# AF27 — H_THERMTRIP_R — R356 24/F_6 — H_THERMTRIP# 3,6

CPU: TP8 AA23 — ICH_TP8 — T72 — IDE_DD[0..15] — IDE_DD[0..15] 33

IHDA: DD0 V1 — IDE_DD0
DD1 U2 — IDE_DD1
DD2 V3 — IDE_DD2
DD3 T1 — IDE_DD3
DD4 V4 — IDE_DD4
DD5 T5 — IDE_DD5
DD6 AB2 — IDE_DD6
DD7 T6 — IDE_DD7
DD8 T3 — IDE_DD8
DD9 R2 — IDE_DD9
DD10 T4 — IDE_DD10
DD11 V6 — IDE_DD11
DD12 V5 — IDE_DD12
DD13 U1 — IDE_DD13
DD14 V2 — IDE_DD14
DD15 U6 — IDE_DD15

SATA / IDE: DA0 AA4 — IDE_DA0 — IDE_DA0 33
DA1 AA1 — IDE_DA1 — IDE_DA1 33
DA2 AB3 — IDE_DA2 — IDE_DA2 33
DCS1# Y6 — IDE_DCS1# — IDE_DCS1# 33
DCS3# Y5 — IDE_DCS3# — IDE_DCS3# 33
DIOR# W4 — IDE_DIOR# 33
DIOW# W3 — IDE_DIOW# 33
DDACK# Y2 — IDE_DDACK# 33
IDEIRQ Y3 — IDE_IRQ 33
IORDY Y1 — IDE_IORDY 33
DDREQ W5 — IDE_DDREQ 33

+1.05V_VCCP — R350 *56.2/F_4@NC — R347 *56.2/F_4@NC — R349 56.2/F_4
H_DPSLP# — H_DPRSTP# — H_FERR#

+3.3V — +3.3V — R607 10K_4 — R370 10K_4
RCIN# — GATEA20

+1.05V_VCCP — R348 56.2/F_4

Layout Note: Placement close SB L<2"

30 ICH_AZ_MDC_BITCLK — R612 33_4 — R319 33_4 — ACZ_BIT_CLK
30 ICH_AZ_CODEC_BITCLK
C754 *10P/50V_4@NC — C437 *10P/50V_4@NC

30 ICH_AZ_MDC_SYNC — R610 33_4 — ACZ_SYNC
30 ICH_AZ_CODEC_SYNC — R317 33_4
30 ICH_AZ_MDC_RST# — R611 33_4 — ACZ_RST#
30 ICH_AZ_CODEC_RST# — R318 33_4
30 ICH_AZ_MDC_SDOUT — R609 33_4 — ACZ_SDOUT
30 ICH_AZ_CODEC_SDOUT — R316 33_4

Place all series terms close to ICH8 except for SDIN input lines,which should be close to source.Placement of R292, R286, R283 & R289 should equal distance to the T split trace point as R291, R285, R284 & R290 respective. Basically,keep the same distance from T for all series termination resistors.

33 SATA_TX0- — C323 3900P/25V/X7R_4 — SATA_TX0- C
33 SATA_TX0+ — C322 3900P/25V/X7R_4 — SATA_TX0+ C

Distance between the ICH-8 M and cap on the "P" signal should be identical distance between the ICH-6 M and cap on the "N" signal for same pair.

33 SATA_TX2- — C787 3900P/25V/X7R_4 — SATA_TX2- C
33 SATA_TX2+ — C784 3900P/25V/X7R_4 — SATA_TX2+ C

XOR Chain Entrance Strap

ICH_RSV0	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1

+3.3V — R321 *1K_4@NC — ACZ_SDOUT — ICH_RSVD 16 — R615 *1K_4@NC

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Place TX DC blocking caps close ICH8.

32 PCIE_TX1-
32 PCIE_TX1+
C778 0.1U/10V/X5R_4 PCIE_TXN1_C
C782 0.1U/10V/X5R_4 PCIE_TXP1_C

32 PCIE_TX2-
32 PCIE_TX2+
C786 0.1U/10V/X5R_4 PCIE_TXN2_C
C788 0.1U/10V/X5R_4 PCIE_TXP2_C

26 PCIE_TX6-/GLAN_TX-
26 PCIE_TX6+/GLAN_TX+
C811 0.1U/10V/X5R_4 GLAN_TXN_C
C807 0.1U/10V/X5R_4 GLAN_TXP_C

32 PCIE_RX1-
32 PCIE_RX1+
MiniWLAN
PCIE_TXN1_C
PCIE_TXP1_C

32 PCIE_RX2-
32 PCIE_RX2+
MiniWWAN
PCIE_TXN2_C
PCIE_TXP2_C

26 PCIE_RX6-/GLAN_RX-
26 PCIE_RX6+/GLAN_RX+
GLAN_TXN_C
GLAN_TXP_C

U39D

PCI-Express Direct Media Interface

PERN1 P27
PERP1 P26
PETN1 N29
PETP1 N28

PERN2 M27
PERP2 M26
PETN2 L29
PETP2 L28

PERN3 K27
PERP3 K26
PETN3 J29
PETP3 J28

PERN4 H27
PERP4 H26
PETN4 G29
PETP4 G28

PERN5 F27
PERP5 F26
PETN5 E29
PETP5 E28

PERN6/GLAN_RXN D27
PERP6/GLAN_RXP D26
PETN6/GLAN_TXN C29
PETP6/GLAN_TXP C28

DMI0RXN V27
DMI0RXP V26
DMI0TXN U29
DMI0TXP U28
DMI_MTX_IRX_N0 6
DMI_MTX_IRX_P0 6
DMI_MRX_ITX_N0 6
DMI_MRX_ITX_P0 6

DMI1RXN Y27
DMI1RXP Y26
DMI1TXN W29
DMI1TXP W28
DMI_MTX_IRX_N1 6
DMI_MTX_IRX_P1 6
DMI_MRX_ITX_N1 6
DMI_MRX_ITX_P1 6

DMI2RXN AB26
DMI2RXP AB25
DMI2TXN AA29
DMI2TXP AA28
DMI_MTX_IRX_N2 6
DMI_MTX_IRX_P2 6
DMI_MRX_ITX_N2 6
DMI_MRX_ITX_P2 6

DMI3RXN AD27
DMI3RXP AD26
DMI3TXN AC29
DMI3TXP AC28
DMI_MTX_IRX_N3 6
DMI_MTX_IRX_P3 6
DMI_MRX_ITX_N3 6
DMI_MRX_ITX_P3 6

DMI_CLKN T26
DMI_CLKP T25
CLK_PCIE_ICH# 2
CLK_PCIE_ICH 2

DMI_ZCOMP Y23
DMI_IRCOMP Y24
+1.5V_PCIE_ICH
R376 24.9/F_4
DMI_IRCOMP_R
Layout Note: DMI_IRCOMP_R<500mils

SPI

SPI_CLK C23
SPI_CS0# B23
SPI_CS1# F22
SPI_MOSI D23
SPI_MISO F21

27 ICH_SPI_CLK
27 ICH_SPI_CS0#
27 ICH_SPI_CS1#
R395 15_4
R399 15_4
R391 15_4
SPI_CS1#_R

27 ICH_SPI_DIN
27 ICH_SPI_DO
R396 0_4

USB

OC0# AJ19
OC1#/GPIO40 AG16
OC2#/GPIO41 AG15
OC3#/GPIO42 AE15
OC4#/GPIO43 AE15
OC5#/GPIO29 AG17
OC6#/GPIO30 AD12
OC7#/GPIO31 AJ18
OC8# AD14
OC9# AH18

34 USB_OC0#
34 USB_OC1#
34 USB_OC2#
USB_OC0#
USB_OC1#
USB_OC2#
USB_OC3#
USB_OC4#
USB_OC5#
USB_OC8#
USB_OC9#

32 WLAN_RF_OFF#
33,35 BAYINS#
WLAN_RF_OFF#

USBP0N G3
USBP0P G2
USBP1N H5
USBP1P H4
USBP2N H2
USBP2P H1
USBP3N J3
USBP3P J2
USBP4N K5
USBP4P K4
USBP5N K2
USBP5P K1
USBP6N L3
USBP6P L2
USBP7N M5
USBP7P M4
USBP8N M2
USBP8P M1
USBP9N N3
USBP9P N2

USBP0- 34
USBP0+ 34
USBP1- 34
USBP1+ 34
USBP2- 34
USBP2+ 34
T73
T74
USBP4- 38
USBP4+ 38
T164
T163
USBP6- 38
USBP6+ 38
USBP7- 32
USBP7+ 32
USBP8- 36
USBP8+ 36
USBP9- 32
USBP9+ 32

System
System
System
Docking 1
BLUETOOTH
MiniCard 2 WWAN
FINGER PRINT
MiniCard 1 WWAN

USBRBIAS# F2
USBRBIAS F3
USB_RBIAS_PN
R660 22.6/F_6
Short F2 and F3 at the package and keep length to less than 500mils. Trace Impedance should be 60ohms +/- 15%.

ICH8M REV 1.0

iAMT

+3.3V_S5
RP33
USB_OC2# 6
WLAN_RF_OFF# 7
USB_OC4# 8
USB_OC3# 9
10
5 USB_OC1#
4 BAYINS#
3 USB_OC0#
2 USB_OC5#
1
10K-10P8R

+3.3V_S5 R332 10K_4 USB_OC8#
+3.3V_S5 R617 10K_4 USB_OC9#

ICH8 Boot BIOS select

Boot BIOS Strap

		GNT0#	SPI_CS1#
LPC	11	No stuff	No stuff
PCI	10	No stuff	Stuff
SPI	01	Stuff	No stuff

SPI_CS1#_R R392 *1K_4@NC
PCI_GNT0# R386 *1K_4@NC

A16 SWAP Override strap

SB_NB_PCIE_RST#	Low = A16 swap override enabled High = Default

SB_NB_PCIE_RST# R394 *1K_4@NC

SB-PCI

U39B

28 PCI_AD[0..31]

PCI

PCI_AD0 D20
PCI_AD1 E19
PCI_AD2 D19
PCI_AD3 A20
PCI_AD4 D17
PCI_AD5 A21
PCI_AD6 A19
PCI_AD7 C19
PCI_AD8 A18
PCI_AD9 B16
PCI_AD10 A12
PCI_AD11 E16
PCI_AD12 A14
PCI_AD13 G16
PCI_AD14 A15
PCI_AD15 B6
PCI_AD16 C11
PCI_AD17 A9
PCI_AD18 D11
PCI_AD19 B12
PCI_AD20 C12
PCI_AD21 D10
PCI_AD22 C7
PCI_AD23 F13
PCI_AD24 E11
PCI_AD25 E13
PCI_AD26 F12
PCI_AD27 D8
PCI_AD28 A6
PCI_AD29 F8
PCI_AD30 D6
PCI_AD31 A3

REQ0# A4 PCI_REQ0# PCI_REQ0# 28
GNT0# D7 PCI_GNT0# PCI_GNT0# 28
REQ1#/GPIO50 E18 BOARD_ID1 BOARD_ID1 16
GNT1#/GPIO51 C18 BOARD_ID2 BOARD_ID2 16
REQ2#/GPIO52 B19 PCI_REQ2#
GNT2#/GPIO53 F18 PCI_GNT2# T81
REQ3#/GPIO54 A11 PCI_REQ3#
GNT3#/GPIO55 C10 SB_NB_PCIE_RST#

C/BE0# C17 PCI_C_BE0# 28
C/BE1# E15 PCI_C_BE1# 28
C/BE2# F16 PCI_C_BE2# 28
C/BE3# E17 PCI_C_BE3# 28

IRDY# C8 PCI_IRDY# PCI_IRDY# 28
PAR D9 PCI_PAR 28
PCIRST# G6 PCIRST# 28,37
DEVSEL# D16 PCI_DEVSEL# PCI_DEVSEL# 28
PERR# A7 PCI_PERR# PCI_PERR# 28
PLOCK# B7 PCI_PLOCK#
SERR# E10 PCI_SERR# PCI_SERR# 28
STOP# C16 PCI_STOP# PCI_STOP# 28
TRDY# C9 PCI_TRDY# PCI_TRDY# 28
FRAME# A17 PCI_FRAME# PCI_FRAME# 28

PLTRST# AG24 PLTRST#_NB PLTRST#_NB 6
PCICLK B10 CLK_PCI_ICH CLK_PCI_ICH 2
PME# G7 ICH_PME# 28

+3.3V
C436 0.1U/10V/X5R_4
U21 TC7SH08FU(F)
PLTRST# 16,18,32,37,38
R308 100K_4

Interrupt I/F

28 PCI_PIRQA#
28 PCI_PIRQB#
28 PCI_PIRQC#
28 PCI_PIRQD#
R393 *0_4
PCI_PIRQD#_R

PIRQA# F9
PIRQB# B5
PIRQC# C5
PIRQD# A10

PIRQE#/GPIO2 F8 BAYID0 BAYID0 33
PIRQF#/GPIO3 G11 BAYID1 BAYID1 33
PIRQG#/GPIO4 E12 ICH_GPIO4_PIRQG#
PIRQH#/GPIO5 B3 ICH_GPIO5_PIRQH#

ICH8M REV 1.0

Cardbus/ CardReader/1394	REQ0	GNT0	PIRQA PIRQB PIRQC

Reserved for EMI. Place resister and cap close to ICH.
CLK_PCI_ICH
R685 *10_4@NC
C834 *10P/50V_4@NC

PCI Pullups

RP51
+3.3V
PCI_STOP# 6
PCI_REQ2# 7
PCI_FRAME# 8
9
10
5 PCI_REQ3#
4 PCI_PIRQD#
3 PCI_TRDY#
2 PCI_DEVSEL#
1
8.2K-10P8R

RP39
PCI_SERR# 6
PCI_IRDY# 7
PCI_PERR# 8
PCI_PLOCK# 9
10
5
4 PCI_REQ0#
3 ICH_GPIO4_PIRQG#
2 BAYID1
1
8.2K-10P8R

RP50
6
7
8
PCI_PIRQA# 9
10
5 BAYID0
4 PCI_PIRQC#
3 PCI_PIRQB#
2 ICH_GPIO5_PIRQH#
1
8.2K-10P8R

<OrgName>
<OrgAddr1>
<OrgAddr2>
<OrgAddr3>
<OrgAddr4>

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remove R241 for S3 leakage current
Mika 2007/02/26

iAMT

+3.3V_S5
R336 10K_4 ICH_CL_RST1#
R334 10K_4 ICH_RI#
R322 10K_4 SCI#
R333 1K_4 ICH_PCIE_WAKE#

R336 NON-IAMT 10K
IAMT NC

iAMT

+3.3V_S5
R629 2.2K_4 ICH_SMBCLK
R335 2.2K_4 ICH_SMBDATA
R366 10K_4 AMT_SMBCLK
R368 10K_4 AMT_SMBDATA

iAMT

+3.3V_S5
Q28 *2N7002W-7-F
AMT_SMBCLK 1
3 ABCLK
ABCLK 3,35,42
+3.3V_S5
Q29 *2N7002W-7-F
AMT_SMBDATA 1
3 ABDATA
ABDATA 3,35,42

+3.3V_M
R711 *10K_4@AMT H_STP_PCI#
R710 *10K_4@AMT H_STP_CPU#

+3.3V
R595 8.2K_4
CLKRUN#
R620 *10K_4@NC
Option to " Disable " clkrun. Pulling it down will keep the clks running.

U39C

2,32 ICH_SMBCLK
2,32 ICH_SMBDATA
32 ICH_CL_RST1#
ICH_SMBCLK AJ26 SMBCLK
ICH_SMBDATA AD19 SMBDATA
ICH_CL_RST1# AG21 LINKALERT#
AMT_SMBCLK AC17 SMLINK0
AMT_SMBDATA AE19 SMLINK1
SMB
ICH_RI# AF17 RI#
32,37,38 LPC_PD#
3 ITP_DBRESET#
LPC_PD# F4 SUS_STAT#/LPCPD#
AD15 SYS_RESET#
6 PM_BMBUSY# AG12 BMBUSY#/GPIO0
35 SCI# SCI# AG22 SMBALERT#/GPIO11
2 H_STP_PCI#
2 H_STP_CPU#
H_STP_PCI# AE20 STP_PCI#/GPIO15
H_STP_CPU# AG18 STP_CPU#/GPIO25
28,32,37,38 CLKRUN#
CLKRUN# AH11 CLKRUN#/GPIO32
32 ICH_PCIE_WAKE#
28,32,35,37,38 IRQ_SERIRQ
3 THERM_ALERT#
ICH_PCIE_WAKE# AE17 WAKE#
IRQ_SERIRQ AE12 SERIRQ
THERM_ALERT# AC13 THRM#
SYS GPIO
VR_PWRGD_CLKEN AJ20 VRMPWRGD
T158 AJ22 TP7
T154 RSVD_GPIO1 AJ8 TACH1/GPIO1
24 FPBACK# FPBACK# AJ9 TACH2/GPIO6
PEN_SW AH9 TACH3/GPIO7
35 KBSMI# KBSMI# AE16 GPIO8
46 LAN_POWER_SB AC19 GPIO12
BOARD_ID0 AG8 TACH0/GPIO17
T66 BOARD_ID3 AH12 GPIO18
RSVD_GPIO22 AE11 GPIO20
T155 38 BT_ON# BT_ON# AG10 SCLOCK/GPIO22
RST_BAY_R# AH25 QRT_STATE0/GPIO27
2 SATA_CLKREQ# SATA_CLKREQ# AD16 QRT_STATE1/GPIO28
T69 RSVD_GPIO38 AG13 SATACLKREQ#/GPIO35
T156 RSVD_GPIO39 AF9 SLOAD/GPIO38
38 TPM_SENSE# AJ11 SDATAOUT0/GPIO39
AD10 SDATAOUT1/GPIO48
30 ACZ_SPKR ACZ_SPKR AD9 SPKR
6 MCH_ICH_SYNC# R315 0_4 MCH_ICH_SYNC#_R AJ13 MCH_SYNC#
14 ICH_RSVD AJ21 TP3
GPIO Controller Link
MISC
ICH8M REV 1.0

SATA GPIO
SATA0GP/GPIO21 AJ12 R605 8.2K_4
SATA1GP/GPIO19 AJ10 R602 8.2K_4
SATA2GP/GPIO36 AE11 R328 8.2K_4
SATA3GP/GPIO37 AG11 R327 8.2K_4
+3.3V
Clocks
CLK14 AG9 CLK_ICH_14M
CLK48 G5 CLK_ICH_48M
SUSCLK D3 ICH_SUSCLK T82
SLP_S3# AG23 SLP_S3# R616 100/F_4 SUSB# 35
SLP_S4# AE21 SLP_S4# R313 100/F_4 SUSC# 35
SLP_S5# AD18 SLP_S5# T70
S4_STATE#/GPIO26 AH27 S4_STAT# 35
PWROK AE23 ICH_PWROK
DPRSLPVR/GPIO16 AJ14 PM_DPRSLPVR_R R608 100/F_4 PM_DPRSLPVR
BATLOW# AE21 PM_BATLOW#_R
PWRBTN# C2 DNBSWON#
LAN_RST# AH20 PM_LAN_ENABLE_R R619 0_4 R618 *0_4@NC R594 *0_4@NC
RSMRST# AG27 PM_RSMRST#_R R340 100/F_4 RSMRST#
CK_PWRGD E1
CLPWROK E3 ICH_CL_PWROK
SLP_M# AJ25
Power MGT
CL_CLK0 F23
CL_CLK1 AE18
CL_DATA0 F22
CL_DATA1 AF19
CL_VREF0 D24 CL_VREF0_SB
CL_VREF1 AH23 CL_VREF1_SB
CL_RST# AJ23
MEM_LED/GPIO24 AJ27 BAYON#
ME_EC_ALERT/GPIO10 AJ24
EC_ME_ALERT/GPIO14 AE22 EC_ME_ALERT
WOL_EN/GPIO9 AG19 LAN_WOL_EN

PM_DPRSLPVR 6,47
DNBSWON# 35
PM_LAN_RST# 35
PLTRST# 15,18,32,37,38
RSMRST# 35
CLK_PWRGD 2
ICH_CL_PWROK 6,40
SUSM# 35
CL_CLK0 6
ICH_CL_CLK1 32
CL_DATA0 6
ICH_CL_DATA1 32
ICH_CL_RST0# 6
BAYON# 33
ME_EC_ALERT 35
EC_ME_ALERT 35
LAN_WOL_EN 35

+3.3V_S5
R241 *10K_4
PM_LAN_RST#

Place these close to ICH8.
CLK_ICH_48M R380 *10_4@NC C480 *10P/50V_4@NC
CLK_ICH_14M R342 *33_4@NC C445 *10P/50V_4@NC

If no use internal LAN MAC connect LAN_RST# to PLTRST#
Use internal LAN MAC connect LAN_RST# to RSMRST# should go high no sooner than 10 ms after both VccLAN3_3 and VccLAN1_5 have reached their nominal voltages.

+3.3V
0.1U/10V/X5R_4 C435
33 RST_BAY#
R304 100K_4
U20 TC7SH08FU(F)
R305 *0_4@NC
38 BT_ON#
2 SATA_CLKREQ#

iAMT
+3.3V_S5
+3.3V_M
R593 3.24K/F_4
R398 3.24K/F_4
R591 453/F_4
C449 0.1U/10V/X5R_4
R397 453/F_4
C510 0.1U/10V/X5R_4
Controller Link 1 VREF for IAMT support only

+3.3V_S5
R337 10K_4 PM_BATLOW#_R
R371 10K_4 KBSMI#
R306 10K_4 RST_BAY_R#
R626 10K_4 BT_ON#
R667 10K_4 DNBSWON#
R633 10K_4 BAYON#
R320 *10K_4@NC EC_ME_ALERT
R367 10K_4 LAN_POWER_SB

+3.3V
R369 8.2K_4 THERM_ALERT#
R606 *10K_4@NC MCH_ICH_SYNC#_R
R329 10K_4 IRQ_SERIRQ
R613 *2.2K_4@NC VR_PWRGD_CLKEN
R600 10K_4 PEN_SW
R599 10K_4 RSVD_GPIO1
R603 10K_4 RSVD_GPIO22
R323 10K_4 RSVD_GPIO38
R604 10K_4 RSVD_GPIO39
R326 1M_4 TPM_SENSE#
R601 10K_4 FPBACK#

No Reboot strap
HDA_SPKR | Low = Default High = No Reboot
+3.3V
*10K_4@NC R360 ACZ_SPKR

PM_DPRSLPVR R314 *100K_4@NC
RSMRST# R596 10K_4
PM_LAN_ENABLE_R R592 *1M_4@NC
ICH_CL_PWROK R385 1M_4
LAN_WOL_EN R354 100K_4

U36
+3.3V
47 VR_PWRGD_CLKEN#
C753 0.1U/10V/X5R_4
VR_PWRGD_CLKEN
NL17SZ14DFT2G
R590 100K_4

+3.3V
+3.3V_SUS
R378 2K_4
C478 0.1U/10V/X5R_4
6,47 DELAY_VR_PG
35,40 PWROK
ICH_PWROK
U23 TC7SH08FU(F)
R375 100K_4
R374 10K_4

GPIO[20]--(PCIE_MCARD2_DET#)
Integrated Pull-Down 20K.

Board ID	ID3	ID2	ID1	ID0
Default	1	1	1	1
RSV	0	0	0	1
RSV	0	0	1	0
RSV	0	0	1	1
RSV	0	1	0	0

+3.3V
R361 1K_4
R362 *10K_4@NC
R390 10K_4
R389 *10K_4@NC
R387 10K_4
R388 *10K_4@NC
R598 10K_4
R597 *10K_4@NC
BOARD_ID0
BOARD_ID1
BOARD_ID2
BOARD_ID3
BOARD_ID1 15
BOARD_ID2 15

SW12
R301 1K_4
SWAP_SWITCH
PEN_SW
C433 1000P/16V/X7R_4
PEN DETECT SWITCH

PROJECT : TA7
Quanta Computer Inc.
Size
Document Number ICH8M GPIO(3 of 4)
Rev 1A
Date: Friday, March 02, 2007
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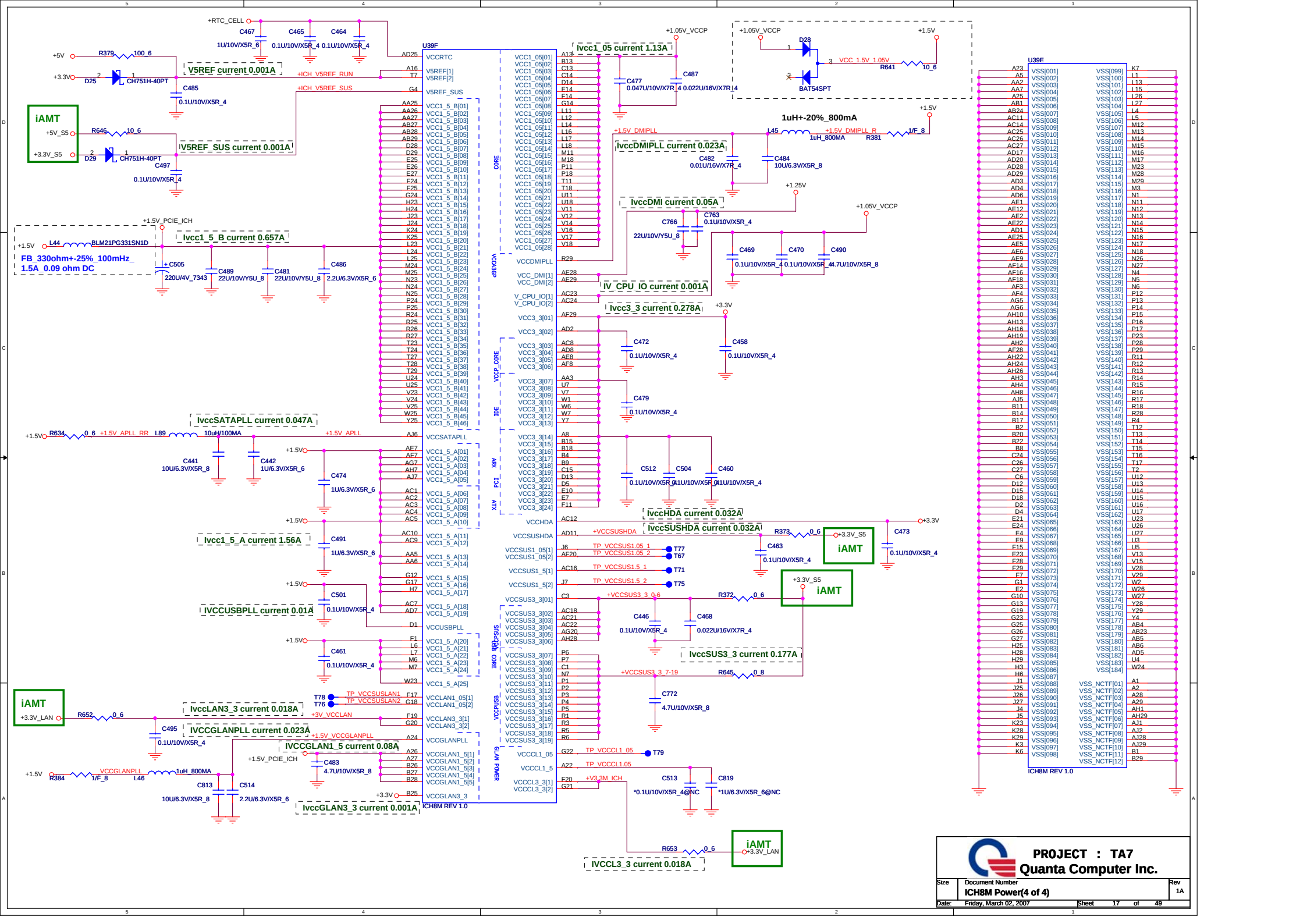
U39F
U39E
+RTC_CELL
C467
C465
C464
1U/10V/X5R_6
0.1U/10V/X5R_4
0.1U/10V/X5R_4
+5V
R379
100_6
+3.3V
D25
CH751H-40PT
V5REF current 0.001A
+ICH_V5REF_RUN
C485
0.1U/10V/X5R_4
+ICH_V5REF_SUS
iAMT
+5V_S5
R646
10_6
+3.3V_S5
D29
CH751H-40PT
V5REF_SUS current 0.001A
C497
0.1U/10V/X5R_4
+1.5V_PCIE_ICH
Ivcc1_5_B current 0.657A
+1.5V
L44
BLM21PG331SN1D
FB_330ohm+-25%_100mHz_
1.5A_0.09 ohm DC
C505
220U/4V_7343
C489
22U/10V/Y5U_8
C481
22U/10V/Y5U_8
C486
2.2U/6.3V/X5R_6
IvccSATAPLL current 0.047A
+1.5V
R634
0_6
+1.5V_APLL_RR
L89
10uH/100MA
+1.5V_APLL
C441
10U/6.3V/X5R_8
C442
1U/6.3V/X5R_6
C474
1U/6.3V/X5R_6
Ivcc1_5_A current 1.56A
C491
1U/6.3V/X5R_6
C501
0.1U/10V/X5R_4
IVCCUSBPLL current 0.01A
C461
0.1U/10V/X5R_4
iAMT
+3.3V_LAN
R652
0_6
IvccLAN3_3 current 0.018A
+3V_VCCLAN
C495
0.1U/10V/X5R_4
IVCCGLANPLL current 0.023A
+1.5V_VCCGLANPLL
IVCCGLAN1_5 current 0.08A
+1.5V_PCIE_ICH
C483
4.7U/10V/X5R_8
+1.5V
R384
1/F_8
VCCGLANPLL
L46
1uH_800MA
C813
10U/6.3V/X5R_8
C514
2.2U/6.3V/X5R_6
+3.3V
IvccGLAN3_3 current 0.001A
ICH8M REV 1.0
Ivcc1_05 current 1.13A
+1.05V_VCCP
C477
0.047U/10V/X7R_4
C487
0.022U/16V/X7R_4
+1.05V_VCCP
D28
BAT54SPT
VCC_1.5V_1.05V
R641
10_6
+1.5V
1uH+-20%_800mA
+1.5V_DMIPLL
IvccDMIPLL current 0.023A
C482
0.01U/16V/X7R_4
C484
10U/6.3V/X5R_8
L45
1uH_800MA
+1.5V_DMIPLL_R
R381
1/F_8
+1.25V
IvccDMI current 0.05A
C766
22U/10V/Y5U_8
C763
0.1U/10V/X5R_4
+1.05V_VCCP
C469
0.1U/10V/X5R_4
C470
0.1U/10V/X5R_4
C490
4.7U/10V/X5R_8
IV_CPU_IO current 0.001A
Ivcc3_3 current 0.278A
+3.3V
C472
0.1U/10V/X5R_4
C458
0.1U/10V/X5R_4
C479
0.1U/10V/X5R_4
C512
0.1U/10V/X5R_4
C504
0.1U/10V/X5R_4
C460
0.1U/10V/X5R_4
IvccHDA current 0.032A
IvccSUSHDA current 0.032A
+VCCSUSHDA
R373
0_6
+3.3V_S5
iAMT
C463
0.1U/10V/X5R_4
C473
0.1U/10V/X5R_4
+3.3V
TP_VCCSUS1.05_1
TP_VCCSUS1.05_2
TP_VCCSUS1.5_1
TP_VCCSUS1.5_2
+3.3V_S5
iAMT
+VCCSUS3_3_0-6
R372
0_6
C446
0.1U/10V/X5R_4
C468
0.022U/16V/X7R_4
IvccSUS3_3 current 0.177A
+VCCSUS3_3_7-19
R645
0_8
C772
4.7U/10V/X5R_8
TP_VCCCL1_05
TP_VCCCL1.05
+V3.3M_ICH
C513
*0.1U/10V/X5R_4@NC
C819
*1U/6.3V/X5R_6@NC
R653
0_6
+3.3V_LAN
iAMT
IVCCL3_3 current 0.018A
ICH8M REV 1.0
PROJECT : TA7
Quanta Computer Inc.
Size
Document Number
ICH8M Power(4 of 4)
Rev
1A
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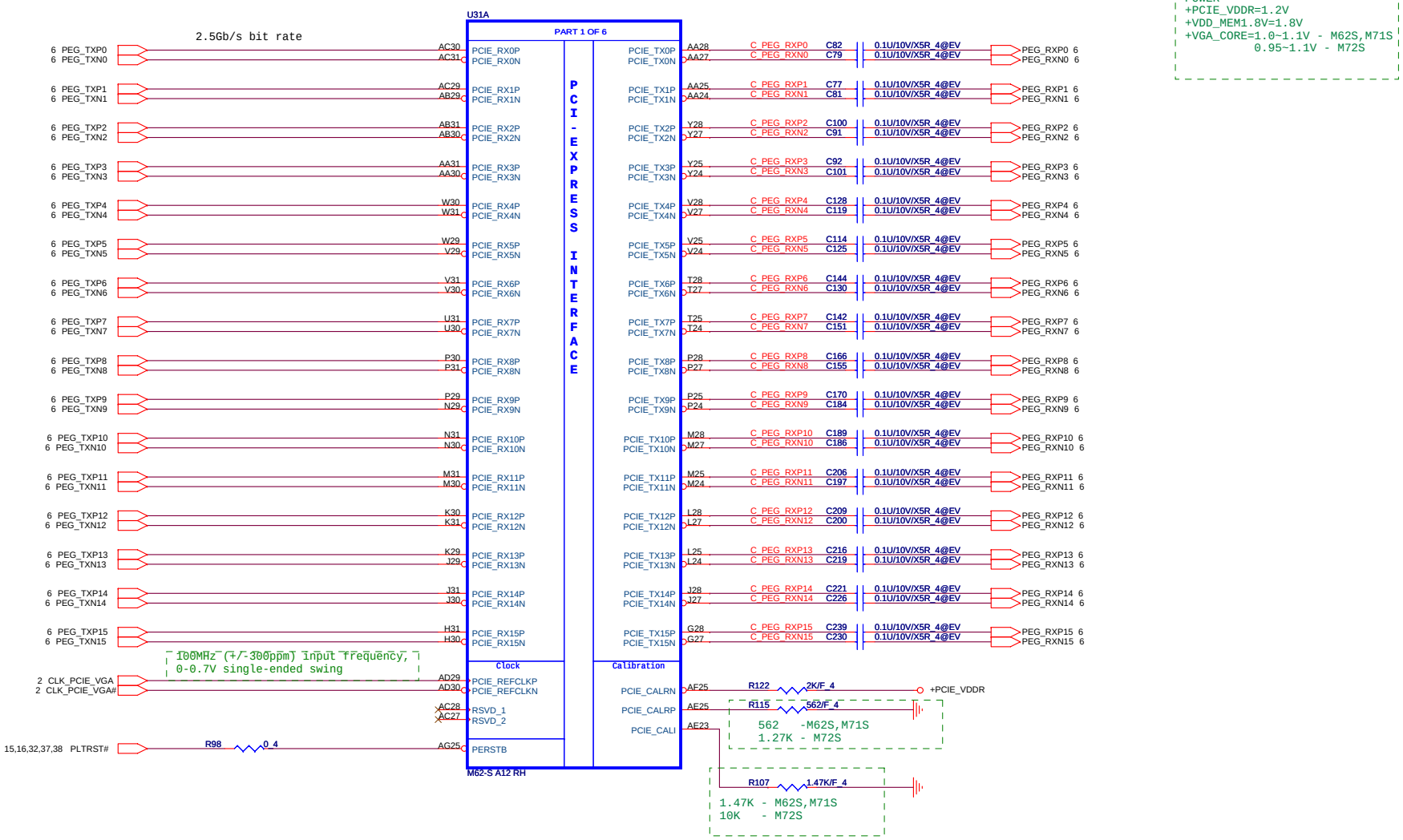

PROJECT : TA7		
Quanta Computer Inc.		
Size	Document Number: M7X/66-M_PCIE_Interface	Rev: 1A
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R162 *1K_4@M72S GPIO_24_JMODE
NA- M62S,M71S
PD 1K- M72S

R161 *10K_4@NC PWRCNTL_1 +3.3V
8/16 change to "Not Stuffed"

R166 10K_4
R165 *10K_4@NC ROMCS# +3.3V
GPIO22(ROMCS#)
PU with external ROM
PD without external ROM

R151 *10K_4@NC BBEN
NA - M64/M62, M71
BBEN- M66
BBEN(10K PD)- M76

R154 *10K_4@NC GPIO_19_CTF +3.3V
NA- M62S,M71S
PU to 3.3V- M72S

R143 *10K_4@NC GPIO_23_CLKREQb
Reserved- M62S,M71S
PCIE CLKREQ# 10K- M72S

DVPDATA_[3:0]	Vendor	Type	Vendor P/N
0000	Qimonda (Infineon)	16*16	HYB18T256161BF-25
0001	Qimonda (Infineon)	32*16	HYB18T512161BF-25
0010	Hynix	16*16	HY5PS561621AFP-25
0011	Hynix	32*16	HY5PS121621BFP-25
0100	Samsung	16*16	K4N561630G-ZC25
0101	Samsung	32*16	K4N511630C-ZC25
0110			Reserved
0111			Reserved
1000			Reserved
1001			Reserved
1010			Reserved
1011			Reserved
1100	Samsung	64M (GDDR3)	
1101	Samsung	128M (GDDR3)	
1110	Hynix	64M (GDDR3)	
1111	Hynix	128M (GDDR3)	

U31B
PART 2 OF 6
M62-S A12 RH

1.M66M TMDS SUPPORTS ONE SINGLE LINK USING TXCA,TX0:2 OR ONE DUAL LINK USING TXCA,TX0:5
2.M71M,M72M TMDS SUPPORTS ONE SINGLE LINK ONLY USING TXCA,TX0:2
3.M76M TMDS SUPPORTS TWO SINGLE LINKS USING TXCA,TX0:2 AND TXCB,TX3:5 OR ONE DUAL LINK USING TXCA,TX0:5

Memory ID
+3.3V
R524 10K_4 MEM_ID0
R523 10K_4 MEM_ID1
R521 10K_4 MEM_ID2
R522 10K_4 MEM_ID3

add R779 10K pull down
Mika 2007/02/14

R160 10K_4 24 EXT_LVDS_BLON T136 GPIO10
R779 10K_4 T39
To control power VDDC 49 GFX_CORE_CNTRL

2.5V(170mA)- M62S,M71S
1.8V(40mA)- M72S
+1.8V L16 *BLM11A05S@NC
+2.5V L12 BLM11A05S

1.2V(90mA)- M62S,M71S
1.8V(40mA)- M72S
+PCIE_VDDR L64 BLM11A05S
+1.8V L71 *BLM11A05S@NC
sensitive

must be very clean
+VGA_CORE L83 BLM18PG181SN1D
VDDC(230mA)- M62S,M71S
VDDC(345mA)- M72S

+PCIE_VDDR L14 BLM11A05S
1.2/1.25V(65mA)- M62S,M71S
1.1V(100mA)- M72S

NC- M62S,M71S T40
M71S /M72S
R118 NC 499
R128 499 NC
R121 499 249
+1.8V +3.3V R118 *499_4@NC R128 499/F_4 R121 499/F_4
3.3V+R316(499R)=3.3V/2=1.65V- M62S,M71S
1.8V+R316(249R)=1.8V/3=0.6V- M72S

Integrated TMDS
External TMDS
DAC / CRT
DAC2 (TV/CRT2)
General Purpose I/O
Monitor Interface
Thermal
PLL & XTAL
VIP / I2C

EXT_CRT_R RB_DAC1 R73 0_4 L69 LQG18HN68NJ00D@EV CRT_R_COM 6,25
EXT_CRT_G GB_DAC1 R69 0_4 L68 LQG18HN68NJ00D@EV CRT_G_COM 6,25
EXT_CRT_B BB_DAC1 R68 0_4 L67 LQG18HN68NJ00D@EV CRT_B_COM 6,25
EXT_HSYNC R492 0_4@EV HSYNC_COM 6,25
EXT_VSYNC R495 0_4@EV VSYNC_COM 6,25
RB_DAC2 R501 0_4
GB_DAC2 R500 0_4
BB_DAC2 R499 0_4
EXT_CRT_DDCDATA R76 0_4@EV DDCDATA_COM 6,25
EXT_CRT_DDCCLK R75 0_4@EV DDCCLK_COM 6,25
DDC2DATA R126 4.7K_4 R113 4.7K_4
DDC2CLK R134 4.7K_4 R114 4.7K_4 +3.3V
VTHM_DAT
VTHM_CLK
TMDS_HPD R135 100K_4
VGAFAN_PWM T24
R104 1K_4

TPVDD_LPVDD L63 *BLM11A05S@NC +1.8V
L61 BLM11A05S +2.5V
2.5V(20mA)- M62S,M71S
1.8V(20mA)- M72S
L62 BLM18PG181SN1D +2.5V
L59 *BLM18PG181SN1D@NC +1.8V
2.5V(S100,D155mA)- M62S,M71S
1.8V(S100,D200mA)- M72S

C611 0.1U/10V/X5R_4 C605 1000P/16V/X7R_4 C599 10U/6.3V/X5R_6
C612 0.1U/10V/X5R_4 C602 1000P/16V/X7R_4 C597 10U/6.3V/X5R_6
C64 0.1U/10V/X5R_4
C78 0.1U/10V/X5R_4
C105 0.1U/10V/X5R_4
C86 0.1U/10V/X5R_4
C87 *1U/6.3V/X5R_4@NC

L24 *BLM11A05S@NC +3.3V_DELAY
R92 0_6 A2VDD_Q
2.5V(120mA)- M62S,M71S
3.3V(135mA)- M72S
L25 *BLM11A05S@NC A2VDD_Q
NC- M62S,M71S
1.8V(2mA)- M72S

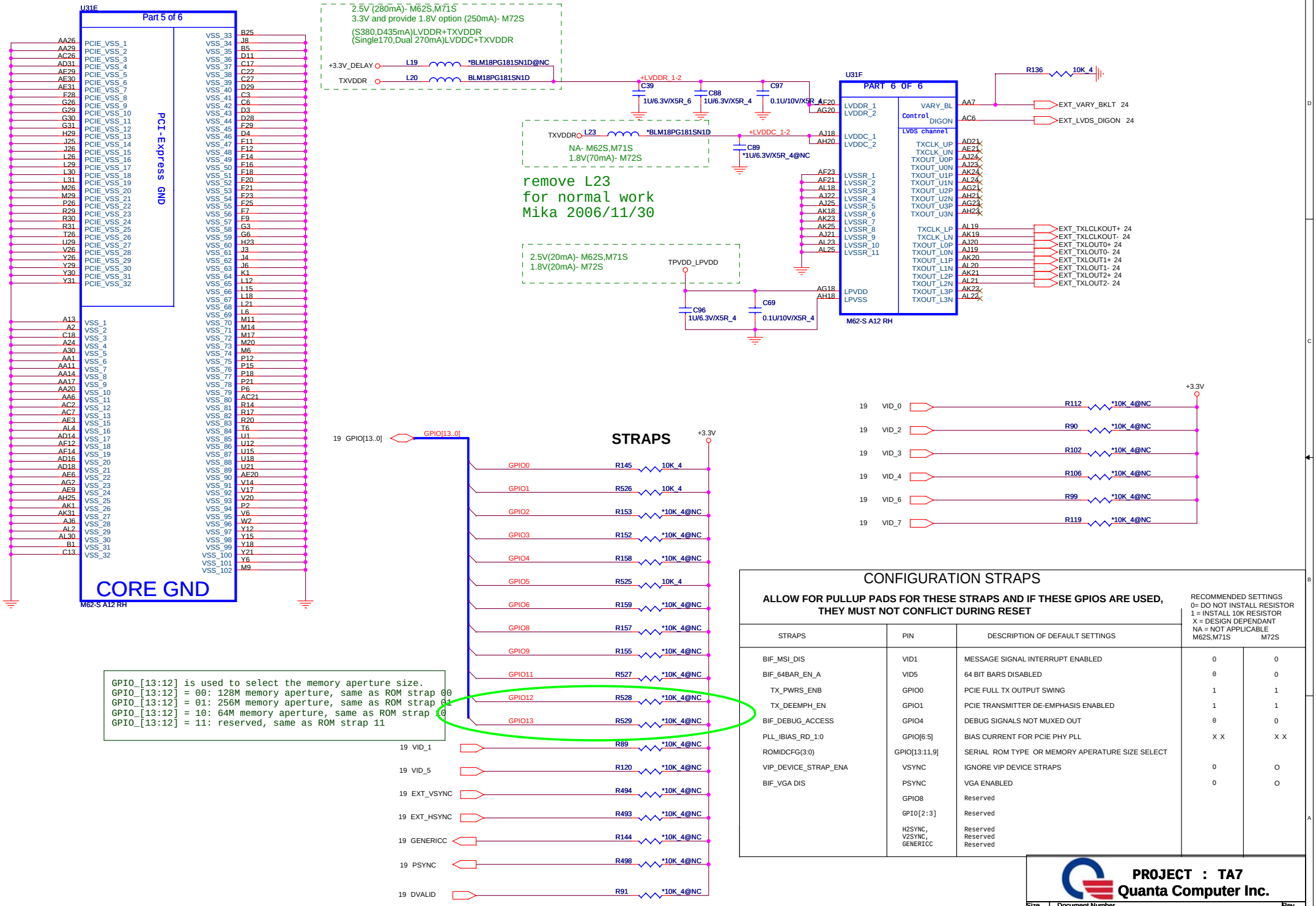
8/17 add R6621(0R) isolated from the major noisy ground

L15 BLM18PG181SN1D +2.5V
L17 *BLM18PG181SN1D@NC +1.8V
C63 0.1U/10V/X5R_4 C62 10U/6.3V/X5R_6 C49 10U/6.3V/X5R_6
2.5V(330mA)- M62S,M71S
1.8V(202mA)- M72S
(202mA)AVDD+A2VDDQ+VDD1DI+VDD2DI
(330mA)AVDD+A2VDD+VDD1DI+VDD2DI

2 CLK_VGA_27M_SS
2 CLK_VGA_27M_NSS
SSFOUT R63 *22_4@NC OSC_SPREAD
R71 80.6/F_4 XTALIN_1 R70 0_4
R67 61.9/F_4 R66 0_4
Ref Clock Swing level on XTALIN
VDDC- M62S,M71S
1.8V- M72S
C37 *22P/50V_4@NC XT_IN R56 *22_4@NC XTALIN
R39 *22_4@NC XTALOUT
*27MHZ Y7
C35 *22P/50V_4@NC XT_OUT
+3.3V
R37 *10K_4@NC R38 *10K_4@NC
U8
XT_IN XIN/CLKIN XOUT XT_OUT
VSS VDD +3.3V_PG1819
SO PD#
SSCLK REFCLK
*PG1819G-08SR@NC
R41 *0_4@NC SSFOUT
XTALIN R40 *22_4@NC
C33 *1U/6.3V/X5R_4 L58 *BLM11A05S C32 *0.1U/10V/X5R_4
MEMORY CLOCK SPREAD SPECTRUM

Thermal Sensor
3 THDAT_SMB R215 0_4
3 THCLK_SMB R209 0_4
VTHM_CLK R210 *0_4@NC 781-1_SMCLK
VTHM_DAT R214 *0_4@NC 781-1_SMDAT
+3.3V R219 10K_4 VGA_ALERT
U13
SMCLK VCC
SMDATA DXP
-ALT DXN
GND -OVT
G781-1P8
781-1_3V R211 100_6 +3.3V
C302 0.1U/10V/X5R_4
VGATHRM+
C304 2200P/50V/X7R_6
VGATHRM-
-VGATHRM R220 10K_4 +3.3V
10 mil trace / 10 mil space
ADDRESS: 9AH

PROJECT : TA7
Quanta Computer Inc.
Size | Document Number: M7X/66-M_Main | Rev: 1A
Date: Friday, March 02, 2007 | Sheet 19 of 49



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	M62S,M71S	M72S
BIF_MSI_DIS	VID1	MESSAGE SIGNAL INTERRUPT ENABLED	0	0
BIF_64BAR_EN_A	VID5	64 BIT BARS DISABLED	0	0
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	1	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	1	1
BIF_DEBUG_ACCESS	GPIO4	DEBUG SIGNALS NOT MUXED OUT	0	0
PLL_IBIAS_RD_1:0	GPIO[6:5]	BIAS CURRENT FOR PCIE PHY PLL	X X	X X
ROMIDCFG(3:0)	GPIO[13:11,9]	SERIAL ROM TYPE OR MEMORY APERATURE SIZE SELECT		
VIP_DEVICE_STRAP_ENA	VSYNC	IGNORE VIP DEVICE STRAPS	0	O
BIF_VGA DIS	PSYNC	VGA ENABLED	0	O
	GPIO8	Reserved		
	GPIO[2:3]	Reserved		
	H2SYNC, V2SYNC, GENERICC	Reserved Reserved Reserved		

PROJECT : TA7
Quanta Computer Inc.

Size	Document Number	Rev
	M7X/66-M_GND / LVDS/ Straps	2A
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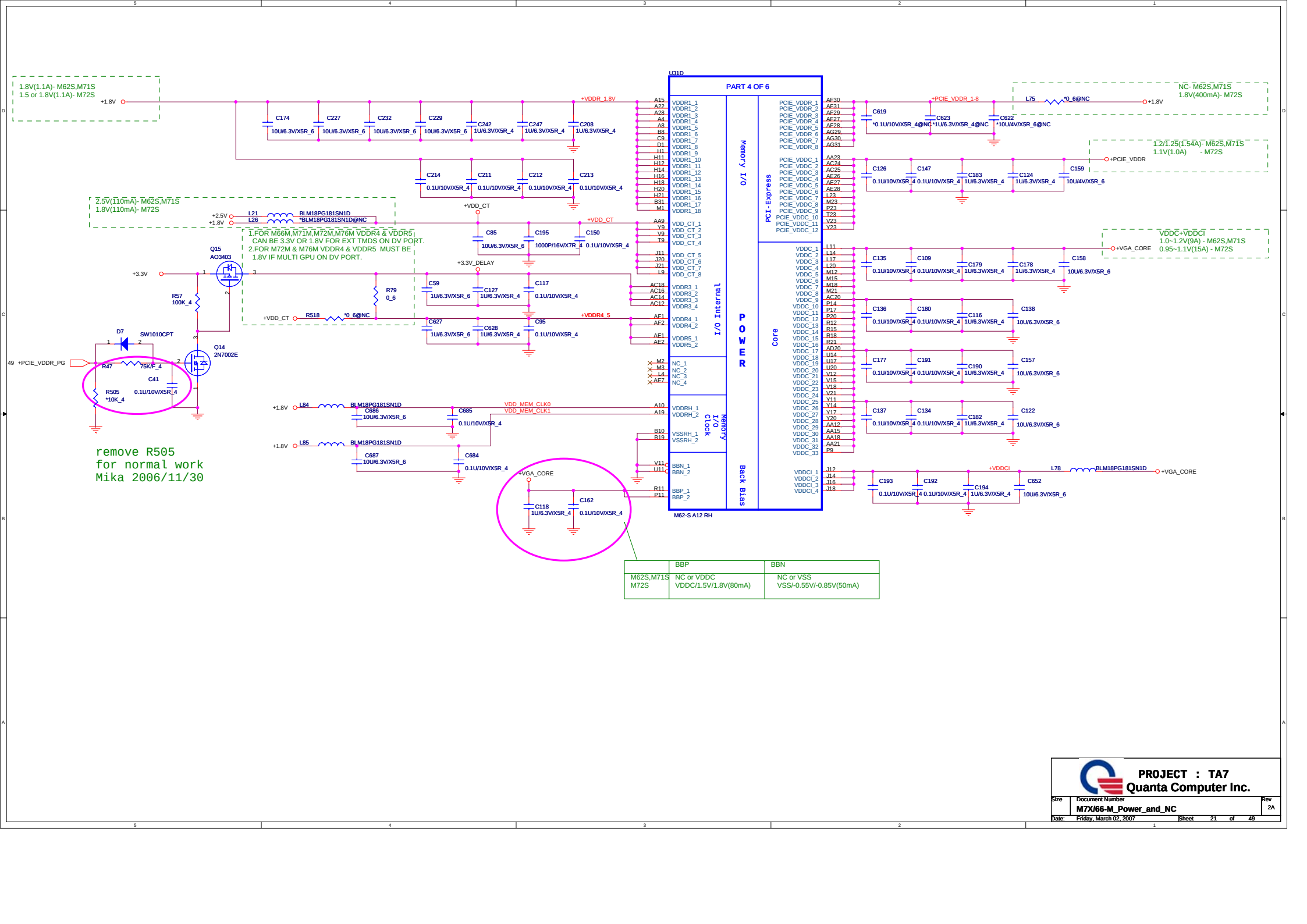
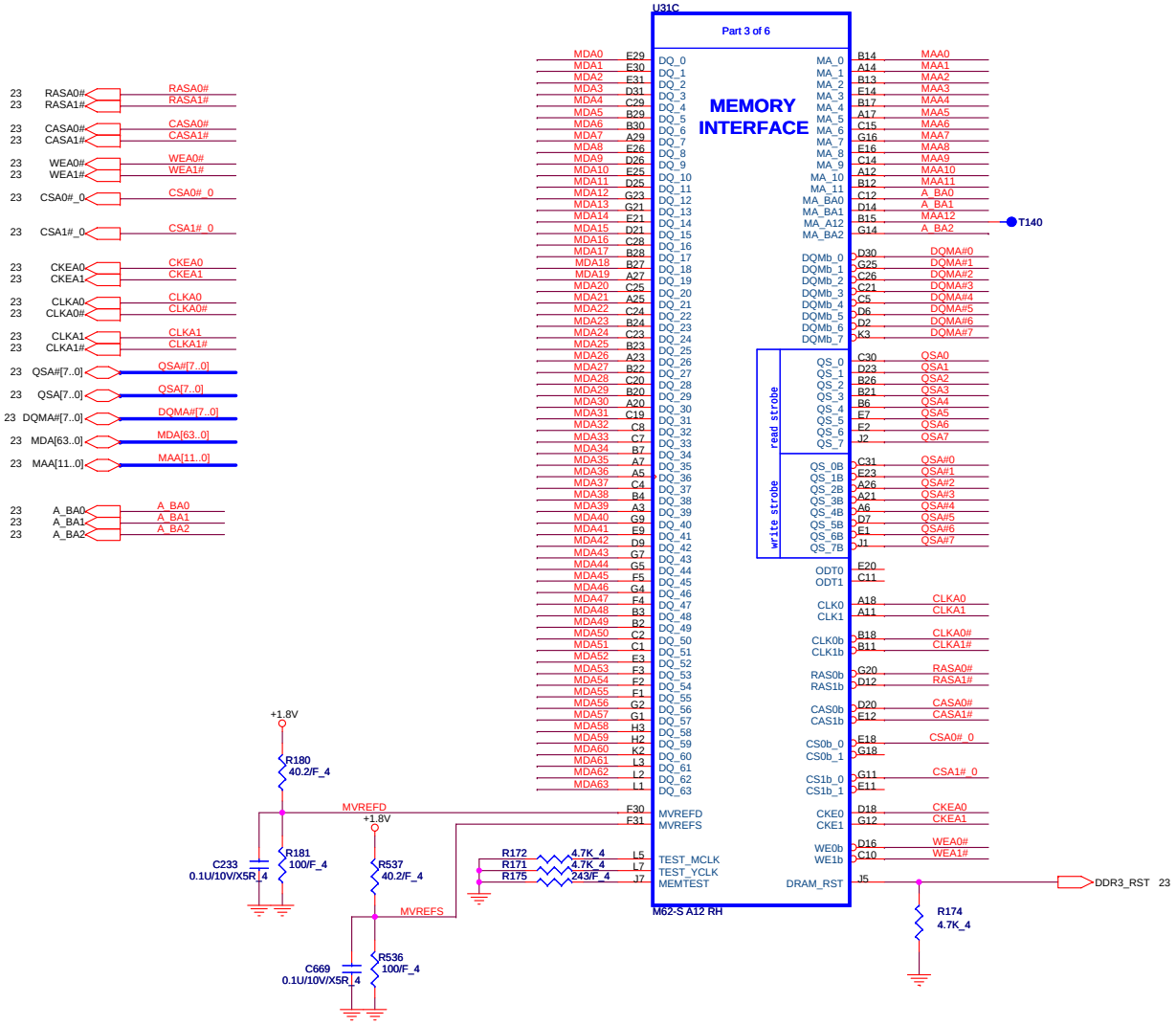


PROJECT : TA7
Quanta Computer Inc.

Size	Document Number	Rev
	M7X/66-M_Power_and_NC	2A

Date: Friday, March 02, 2007 Sheet 21 of 49



PROJECT : TA7

Quanta Computer Inc.

Size	Document Number	Rev
	M7X/66-M MEM_Interface	1A

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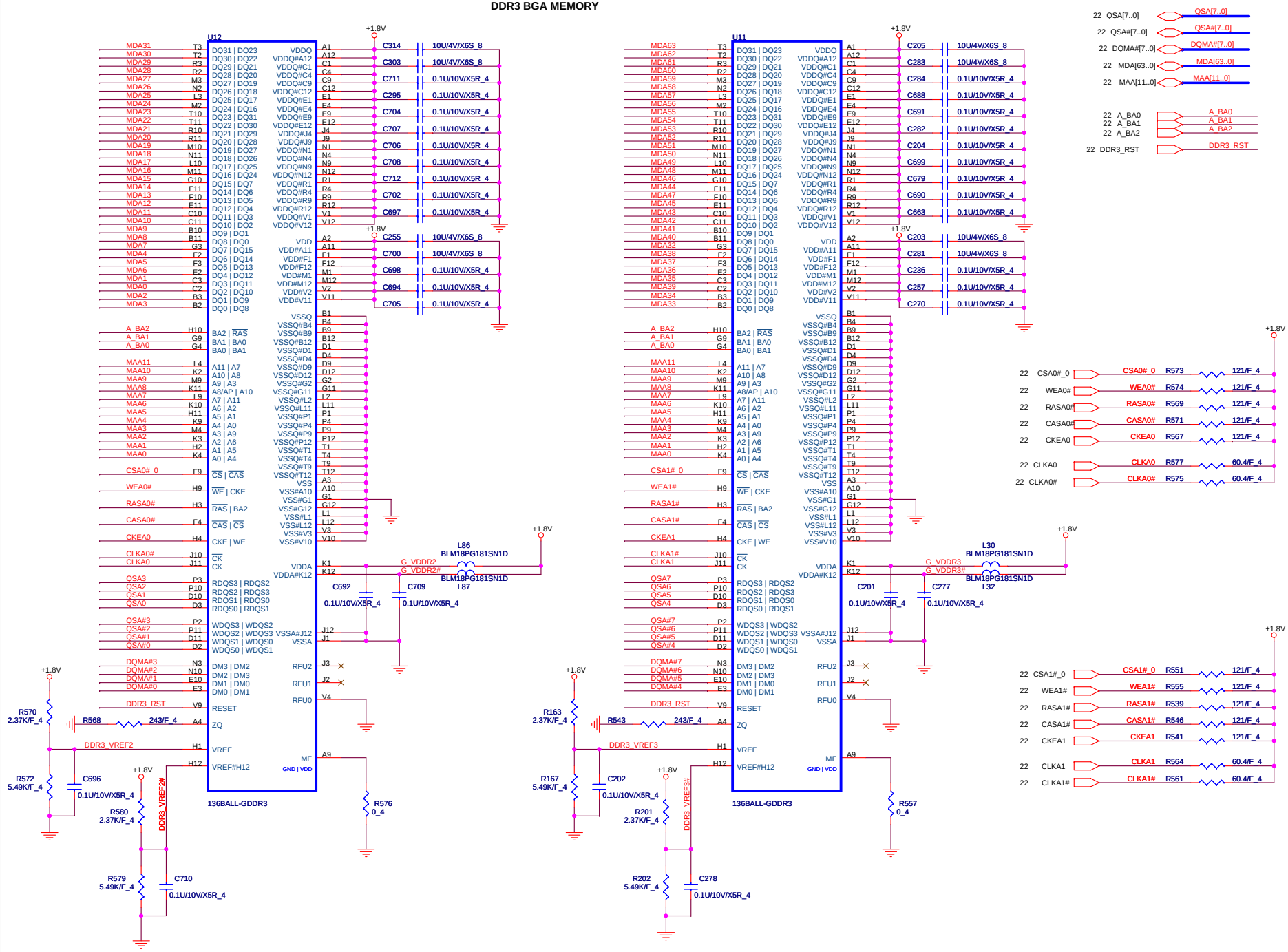
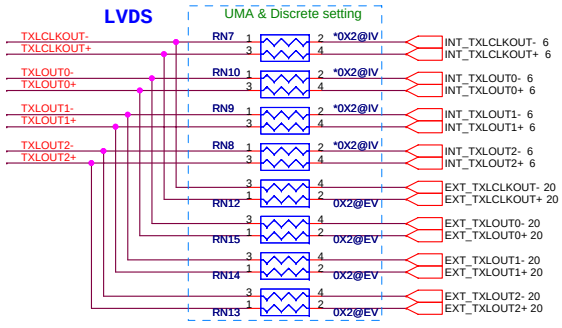
DDR3 BGA MEMORY



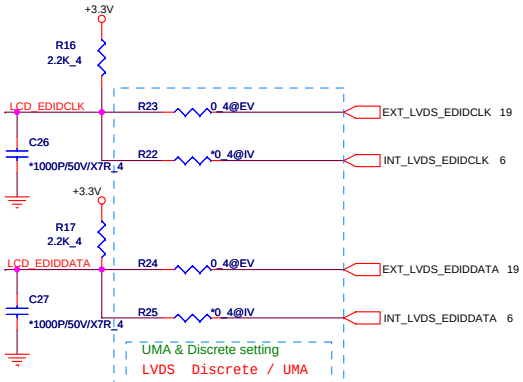


External VGA with @EV part,
Internal VGA with @IV part.

UMA & Discrete setting

LVDS Discrete / UMA

RN7	NC	0
RN10	NC	0
RN9	NC	0
RN8	NC	0
RN12	0	NC
RN15	0	NC
RN14	0	NC
RN13	0	NC

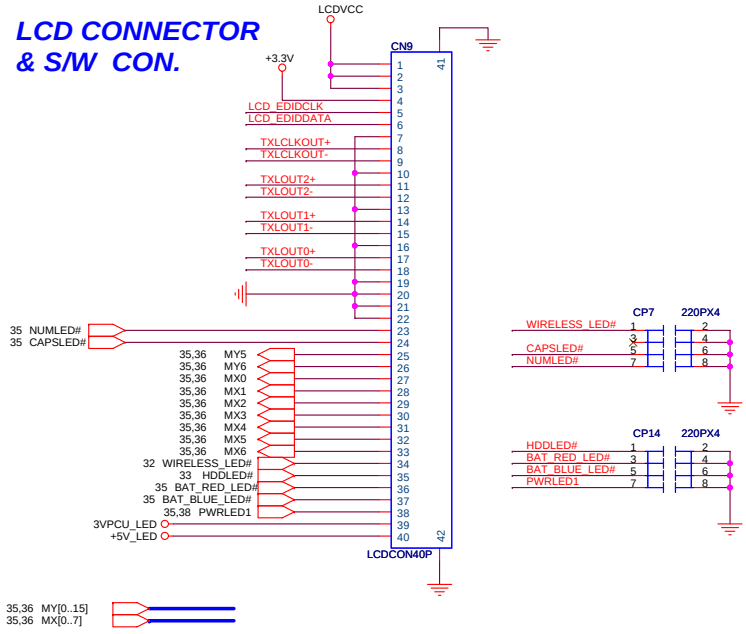


UMA & Discrete setting

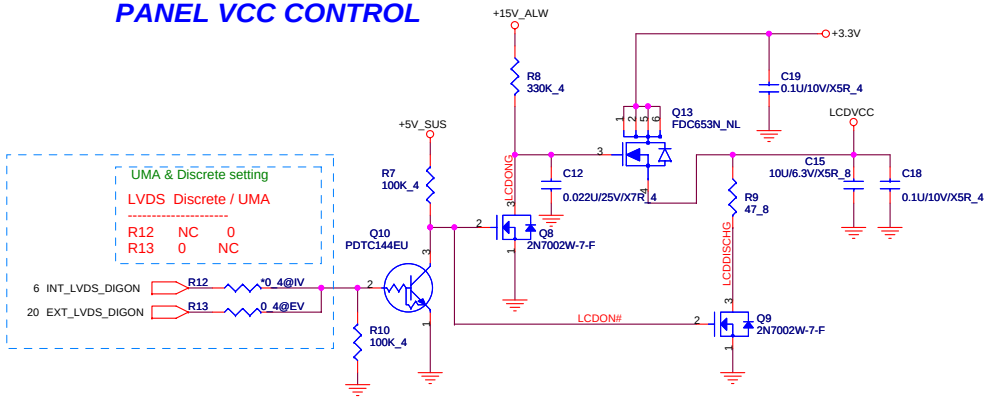
LVDS Discrete / UMA

R23	0	NC
R22	NC	0
R24	0	NC
R25	NC	0

LCD CONNECTOR & S/W CON.



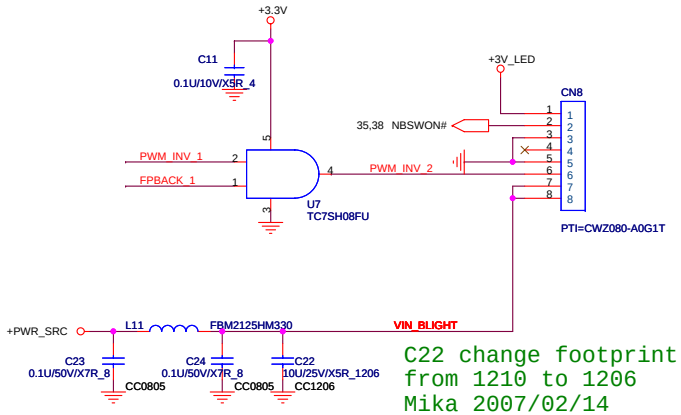
PANEL VCC CONTROL



UMA & Discrete setting

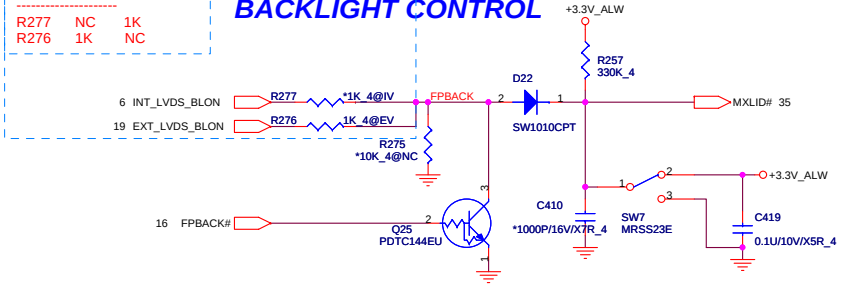
LVDS Discrete / UMA

R12	NC	0
R13	0	NC



C22 change footprint
from 1210 to 1206
Mika 2007/02/14

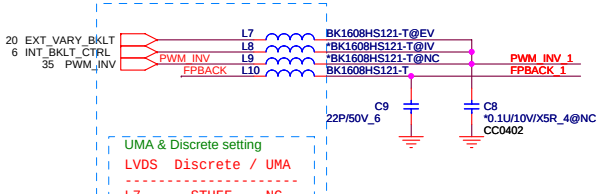
BACKLIGHT CONTROL



UMA & Discrete setting

LVDS Discrete / UMA

R277	NC	1K
R276	1K	NC



UMA & Discrete setting

LVDS Discrete / UMA

L7	STUFF	NC
L8	NC	STUFF

<OrgName>
<OrgAddr1>
<OrgAddr2>
<OrgAddr3>
<OrgAddr4>

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Quanta Computer Inc.

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	LVDS/HDMI	1A

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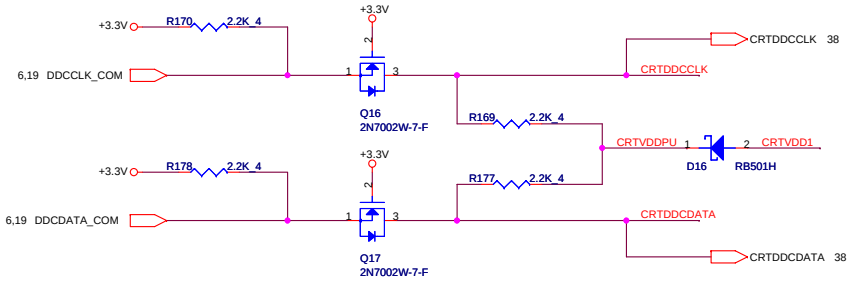
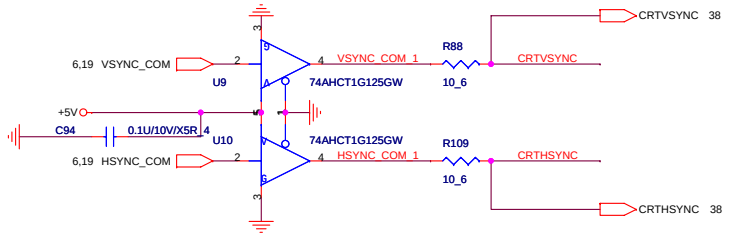
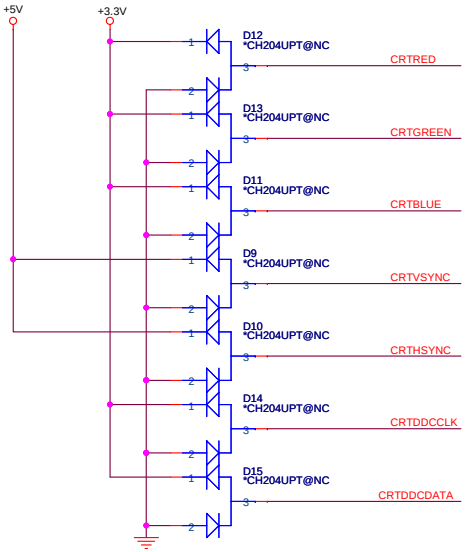
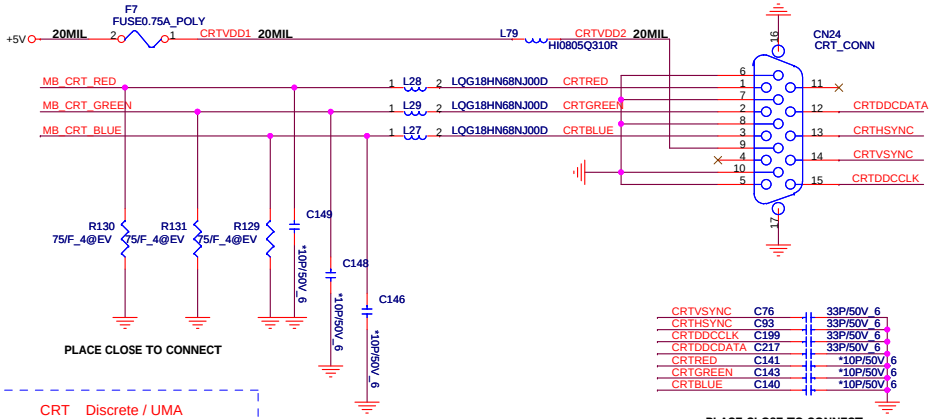




PLACE CLOSE TO CONNECT

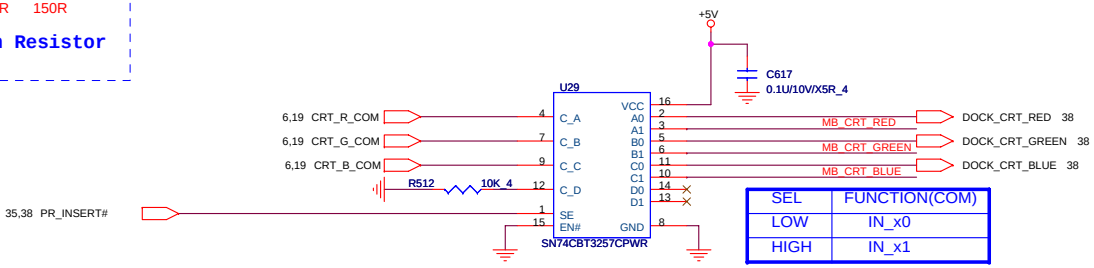


CRT PORT



CRT	Discrete / UMA
R130	75R 150R
R131	75R 150R
R129	75R 150R

Termination Resistor



SEL	FUNCTION(COM)
LOW	IN_x0
HIGH	IN_x1

<OrgName>
<OrgAddr1>
<OrgAddr2>
<OrgAddr3>
<OrgAddr4>

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Quanta Computer Inc.

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	CRT	1A

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LAN

JKCLK Pin	
Power down	0MHz
10Mbps	5MHz
100Mbps	50MHz
1000Mbps	62.5MHz

Layout Note:
Place series resistor close to LAN controller.

Link Speed	LCI	GLCI
1000Mbps	Runing	Runing
100Mbps	Runing	Idle
10Mbps	Runing	Idle
No Link	Runing or power down	Idle
Power down	Power down	Power down

add R781 30 ohm
for Intel suggestion
Mika 2007/02/14

Layout Note:
Place the resistors less than 1" from LAN controller.

Layout Note:
Connect the resistor
to GND near ball E6

Test Mode Enable
Strap low for normal operation
82566 100~200 pull down for normal operation
82562 200 pull down for normal operaiton

82562V and 82566MM
R245,R254 NC

82566MM
1. R232~R235 , R237~R240 --- 49.9/F (CS04992FB31).
2. C330~C333 --- 0.1U.

need FAE support
82562 question
(mode select)

Place termination resistors and caps as close to LAN controller as possible

NINEVEH-EKRON_N (REV 1p0)

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Quanta Computer Inc.

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	LAN-NINEVEH-EKRON_N	1A

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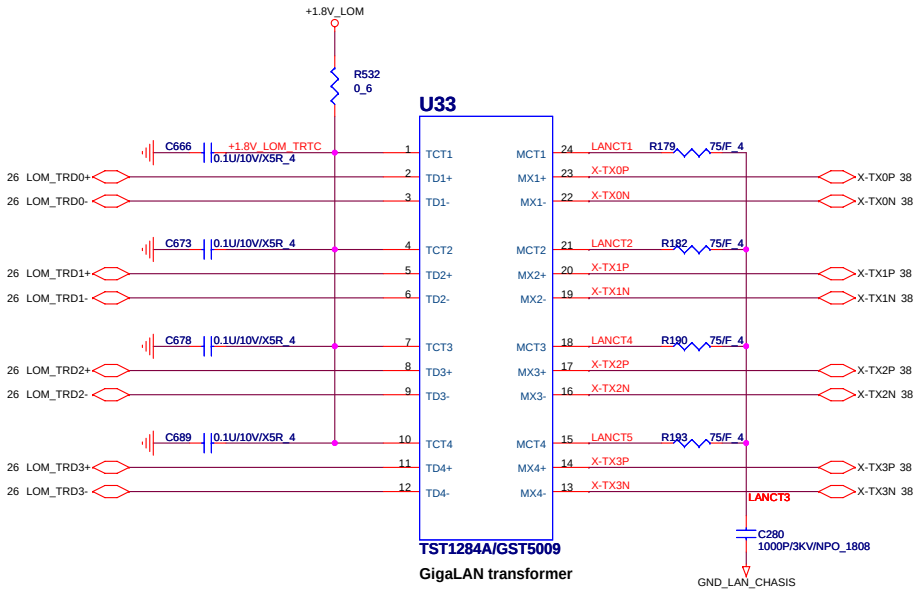

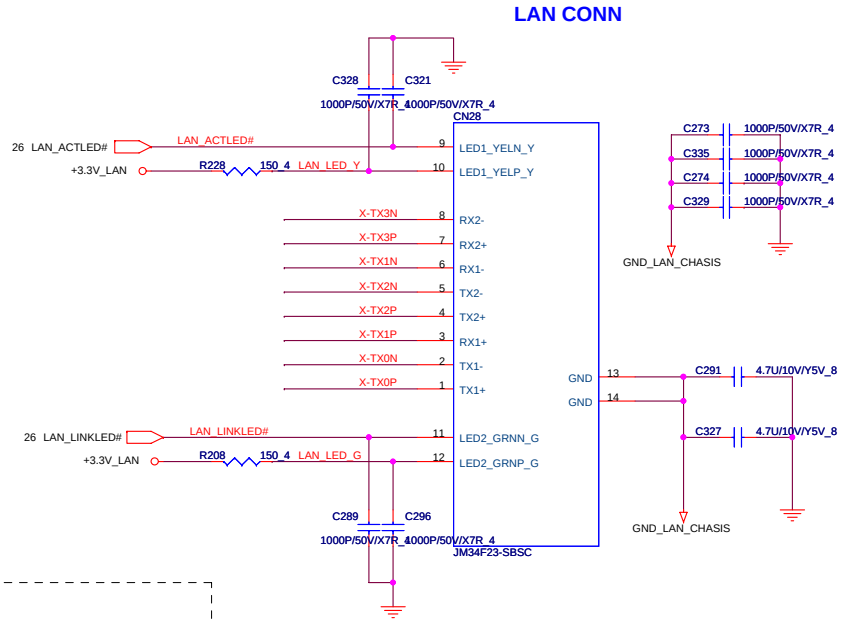

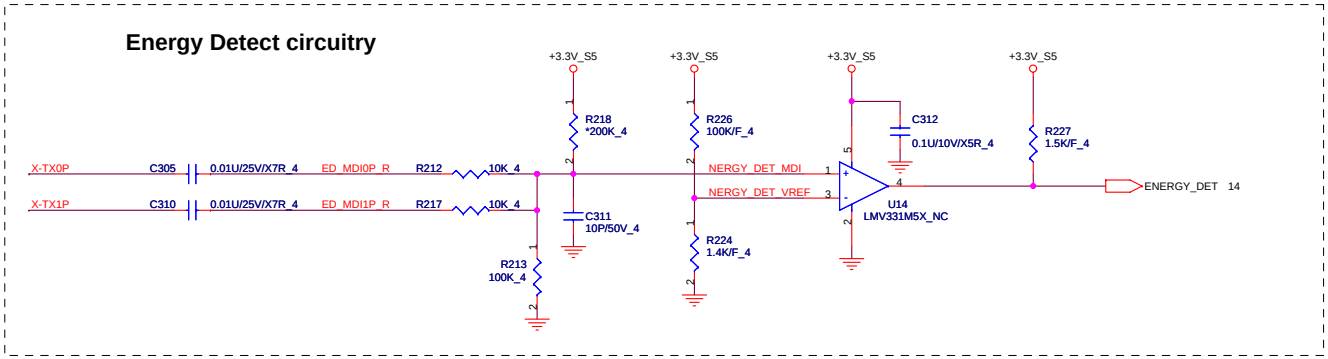

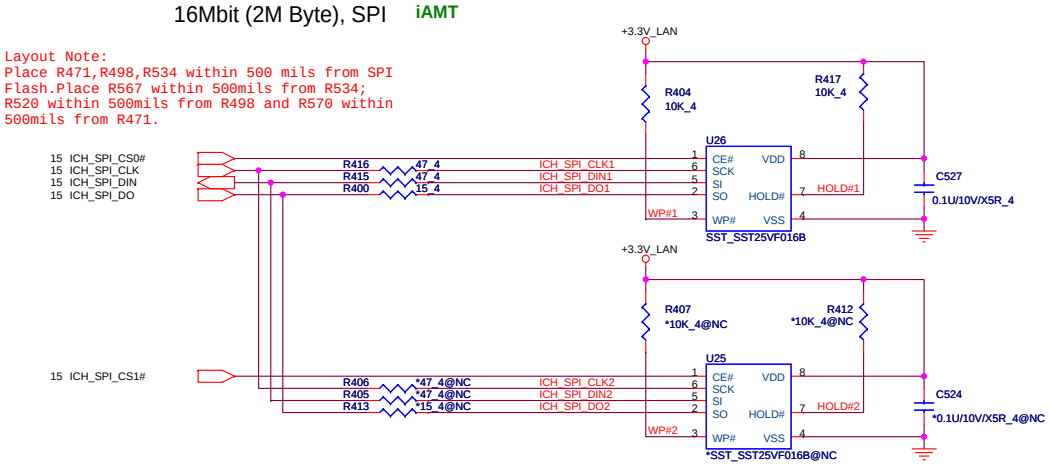

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Quanta Computer Inc.

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	TRANSFORMER/RJ45	1A
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change RICO R5C843 to TI 7412 for customer request
Mika 2006/11/30

IEEE 1394

del R311 R312 L43
del R309 R307 L42
from C.S suggestion
Mika 2007/02/26

U24A
PCI Interface
1394 Interface
Miscellaneous
PCI7412ZHK
Closed Phy IC
Closed Phy IC
CN34
1394 CONNECTOR
U42
NM24C02-WMN6T
U24B
CardBus Interface
CN15
CARDBUS-SANTA
CARDBUS POWER SWITCH
U22
TPS2220B(PWR)
U24D
Power/GND
PCI7412ZHK
PCI7412ZHK
40mil
40mil
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Quanta Computer Inc.
PCI7412 CARDBUS,1394
Size
Document Number
Rev 2A
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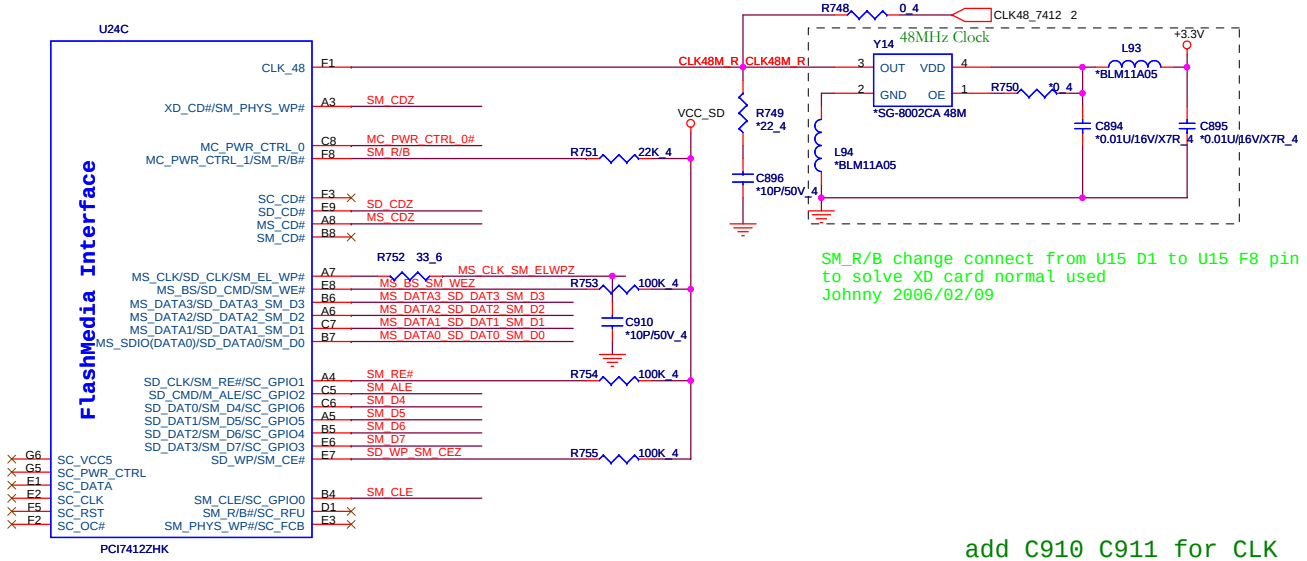
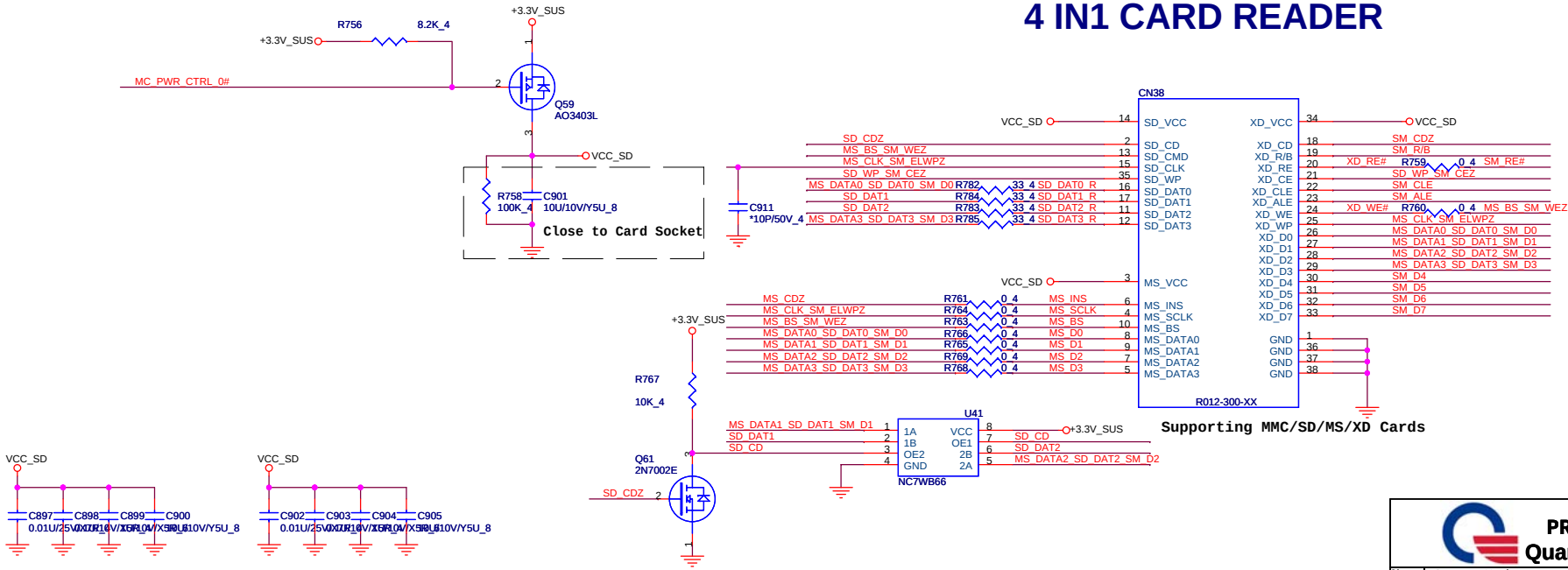
change RICO R5C843 to TI 7412 for customer request
Mika 2006/11/30



SM_R/B change connect from U15 D1 to U15 F8 pin
to solve XD card normal used
Johnny 2006/02/09

add C910 C911 for CLK
add R782 R783 R784 R785 for DATA
that suggestion is from EMI
Mika 2007/02/14

4 IN1 CARD READER



PROJECT : TA7
Quanta Computer Inc.

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	PCI7412_CARD READER	2A
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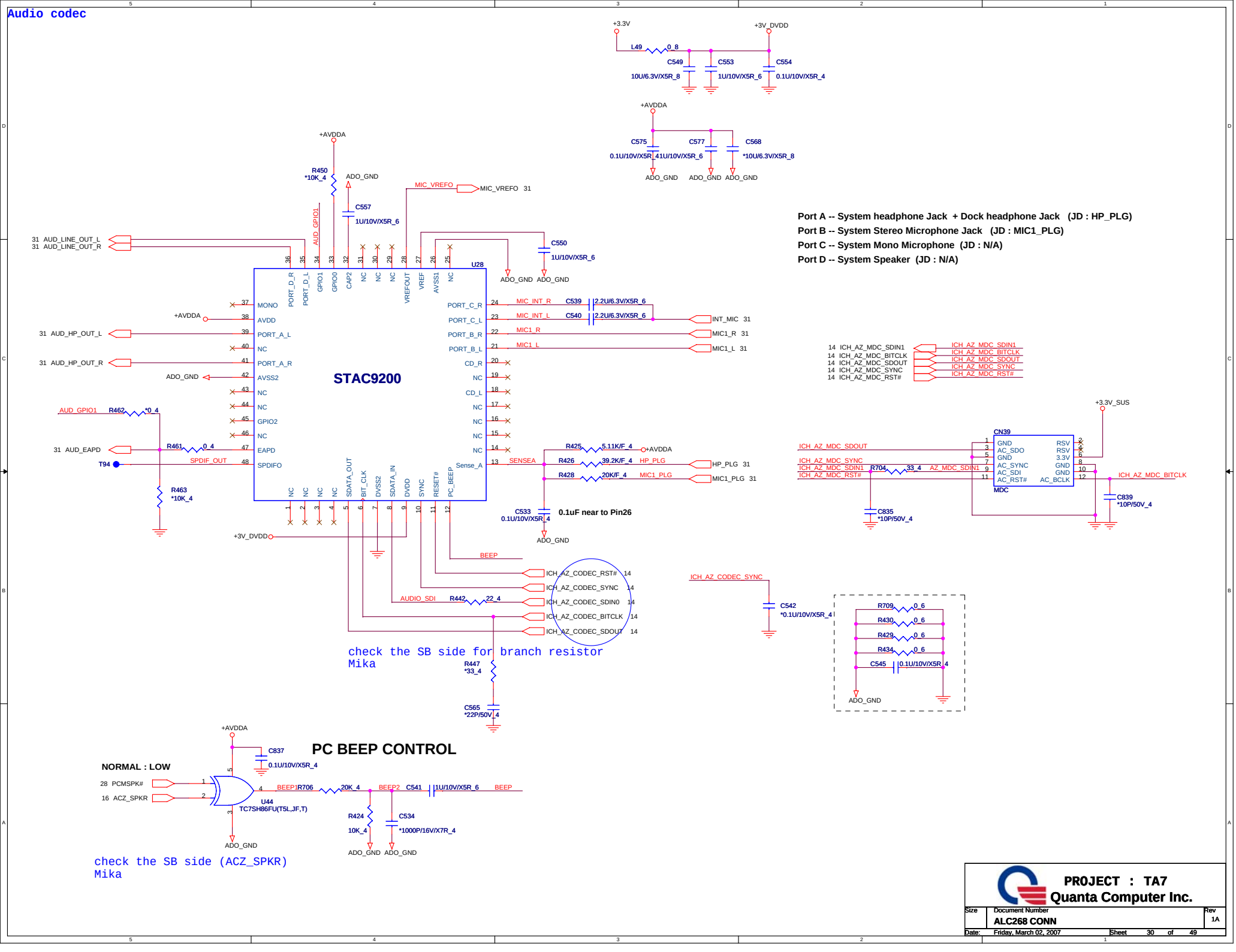
Audio codec


+3.3V
+3V_DVDD
L49 0_8
C549 10U/6.3V/X5R_8
C553 1U/10V/X5R_6
C554 0.1U/10V/X5R_4
+AVDDA
C575 0.1U/10V/X5R_4
C577 1U/10V/X5R_6
C568 *10U/6.3V/X5R_8
ADO_GND
R450 *10K_4
C557 1U/10V/X5R_6
MIC_VREFO
MIC_VREFO 31
AUD_GPIO1
C550 1U/10V/X5R_6
31 AUD_LINE_OUT_L
31 AUD_LINE_OUT_R
U28
STAC9200
MONO
AVDD
PORT_A_L
PORT_A_R
AVSS2
GPIO2
EAPD
SPDIFO
PORT_C_R
PORT_C_L
PORT_B_R
PORT_B_L
CD_R
CD_L
Sense_A
MIC_INT_R
MIC_INT_L
C539 2.2U/6.3V/X5R_6
C540 2.2U/6.3V/X5R_6
INT_MIC 31
MIC1_R
MIC1_L
MIC1_R 31
MIC1_L 31
31 AUD_HP_OUT_L
31 AUD_HP_OUT_R
AUD_GPIO1 R462 *0_4
31 AUD_EAPD
R461 0_4
T94
SPDIF_OUT
R463 *10K_4
R425 5.11K/F_4
R426 39.2K/F_4 HP_PLG
R428 20K/F_4 MIC1_PLG
HP_PLG 31
MIC1_PLG 31
C533 0.1U/10V/X5R_4
0.1uF near to Pin26
SDATA_OUT
BIT_CLK
SDATA_IN
DVDD
SYNC
RESET#
PC_BEEP
BEEP
ICH_AZ_CODEC_RST# 14
ICH_AZ_CODEC_SYNC 14
ICH_AZ_CODEC_SDIN0 14
ICH_AZ_CODEC_BITCLK 14
ICH_AZ_CODEC_SDOUT 14
AUDIO_SDI R442 22_4
R447 *33_4
C565 *22P/50V_4
check the SB side for branch resistor
Mika
Port A -- System headphone Jack + Dock headphone Jack (JD : HP_PLG)
Port B -- System Stereo Microphone Jack (JD : MIC1_PLG)
Port C -- System Mono Microphone (JD : N/A)
Port D -- System Speaker (JD : N/A)
14 ICH_AZ_MDC_SDIN1
14 ICH_AZ_MDC_BITCLK
14 ICH_AZ_MDC_SDOUT
14 ICH_AZ_MDC_SYNC
14 ICH_AZ_MDC_RST#
+3.3V_SUS
CN39
MDC
GND
AC_SDO
GND
AC_SYNC
AC_SDI
AC_RST#
RSV
RSV
3.3V
GND
GND
AC_BCLK
R704 33_4
C835 *10P/50V_4
C839 *10P/50V_4
ICH_AZ_CODEC_SYNC
C542 *0.1U/10V/X5R_4
R709 0_6
R430 0_6
R429 0_6
R434 0_6
C545 0.1U/10V/X5R_4
PC BEEP CONTROL
NORMAL : LOW
28 PCMSPK#
16 ACZ_SPKR
U44
TC7SH86FU(T5L,JF,T)
C837 0.1U/10V/X5R_4
BEEP1 R706 20K_4
BEEP2 C541 1U/10V/X5R_6
BEEP
R424 10K_4
C534 *1000P/16V/X7R_4
check the SB side (ACZ_SPKR)
Mika
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Quanta Computer Inc.
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1A
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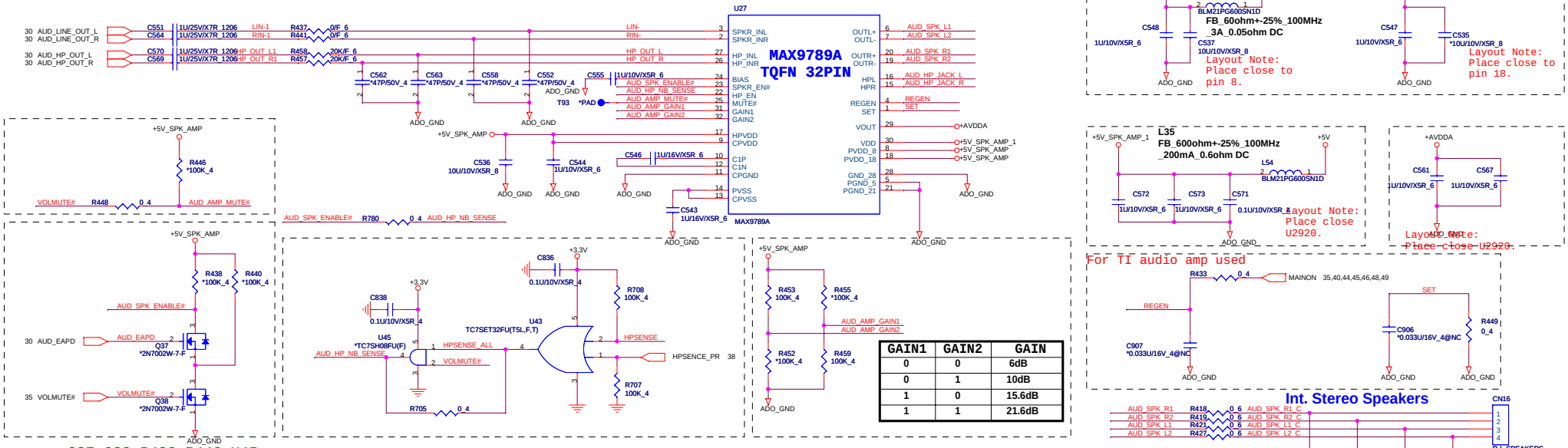
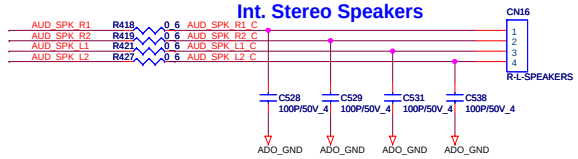
AUDIO AMPLIFIER

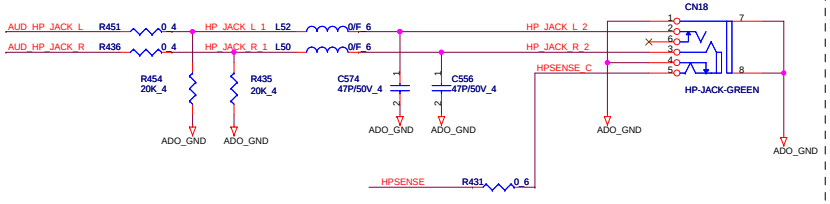


GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

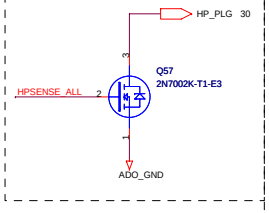


remove Q37 Q38 R438 R446 U45
add R448 R705 R780
change R437 R441 to 0ohm
change C551 C564 C569 C570 to 1U
solve audio bo sound Mika 2007/02/14

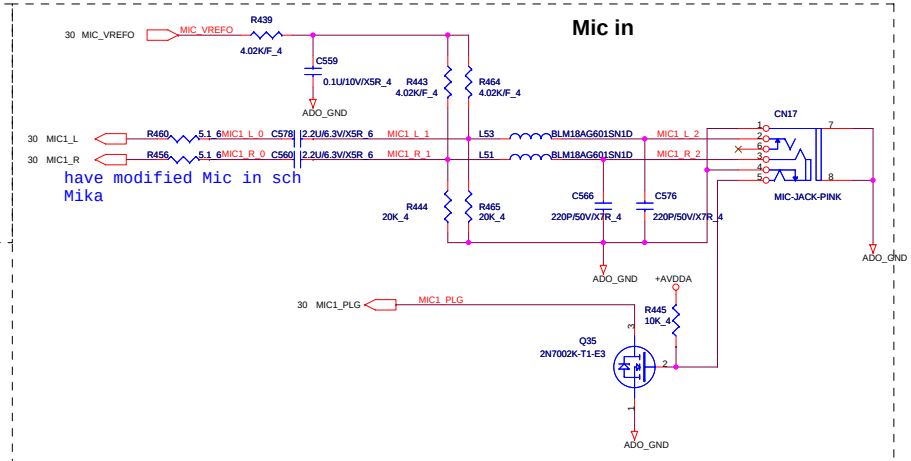
Headphone out

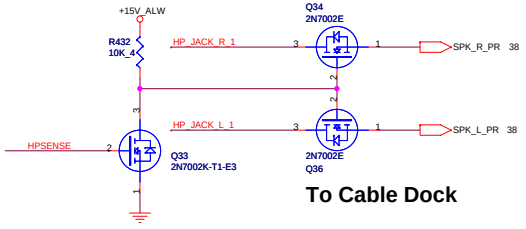


L50 L52 P/N change to 0_0603(CS00003F916)
MIKA 2007/01/04

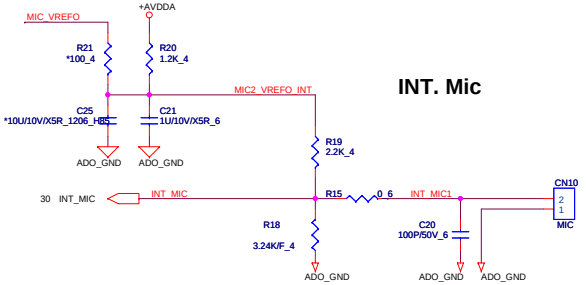


Mic in





To Cable Dock



INT. Mic

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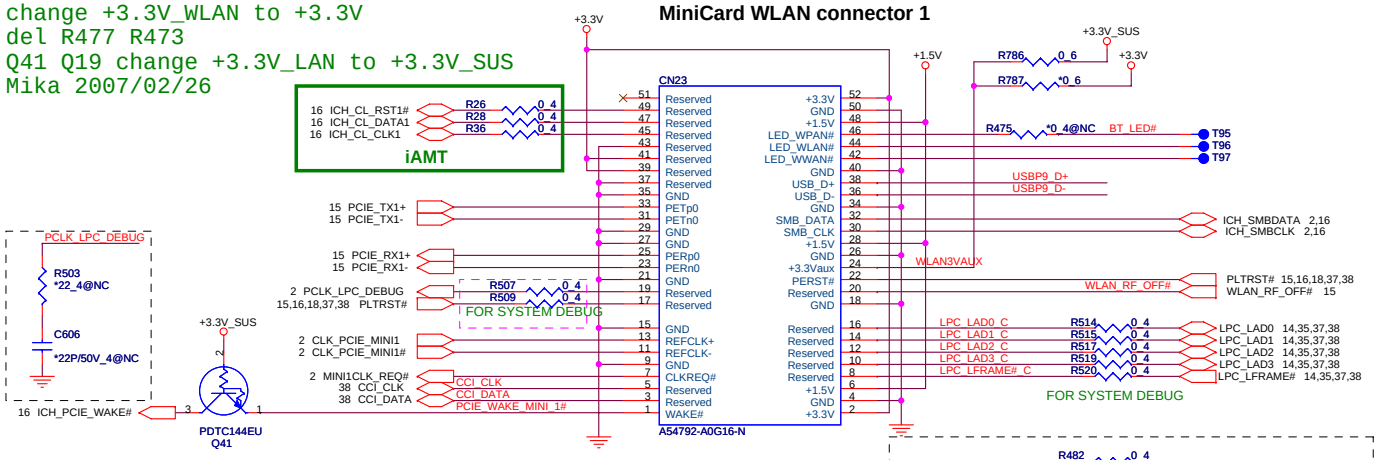
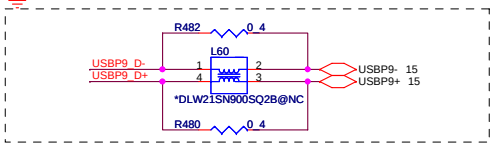
Quanta Computer Inc.

change +3.3V_WLAN to +3.3V
del R477 R473
Q41 Q19 change +3.3V_LAN to +3.3V_SUS
Mika 2007/02/26

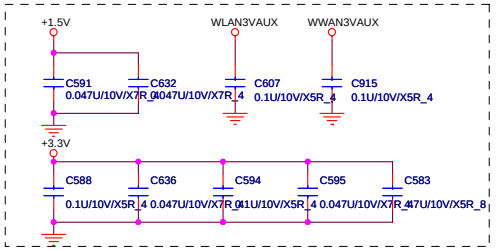
MiniCard WLAN connector 1

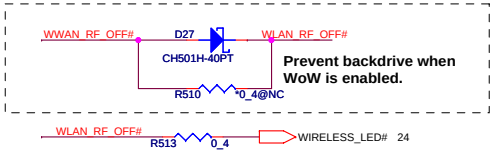




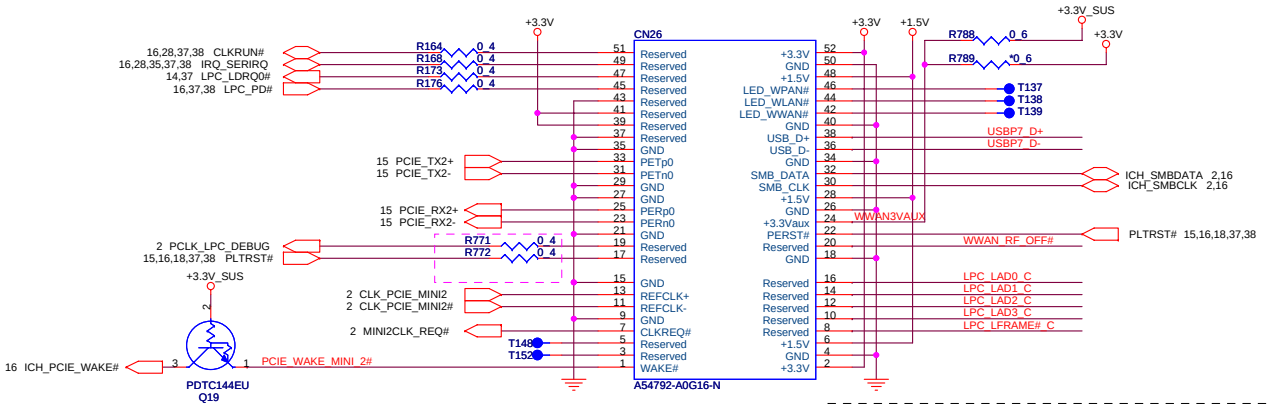
del R491 R486 Q39 Q40
and directly connect both signal
Mika 2007/02/26

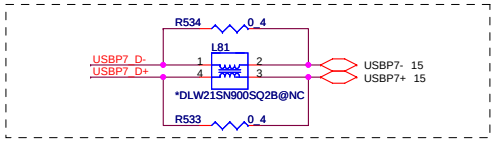
add R786 R787 for select power
Mika 2007/02/26





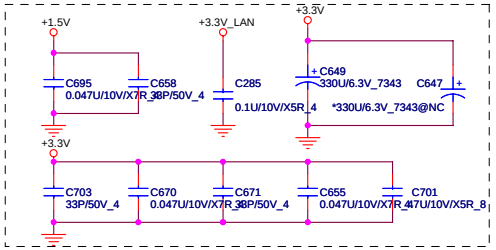
MiniCard WWAN connector 2





del R542 R538 Q42 Q43
and directly connect both signal
Mika 2007/02/26

add R788 R789 for select power
add C915 for WWAN3VAUX
Mika 2007/02/26



add R771 R772
for Debug card used
Mika 2006/11/30

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Quanta Computer Inc.		
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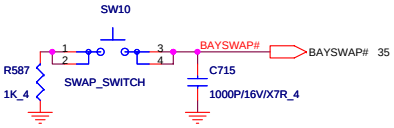
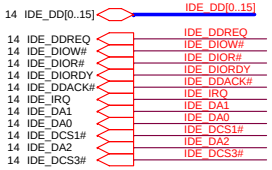
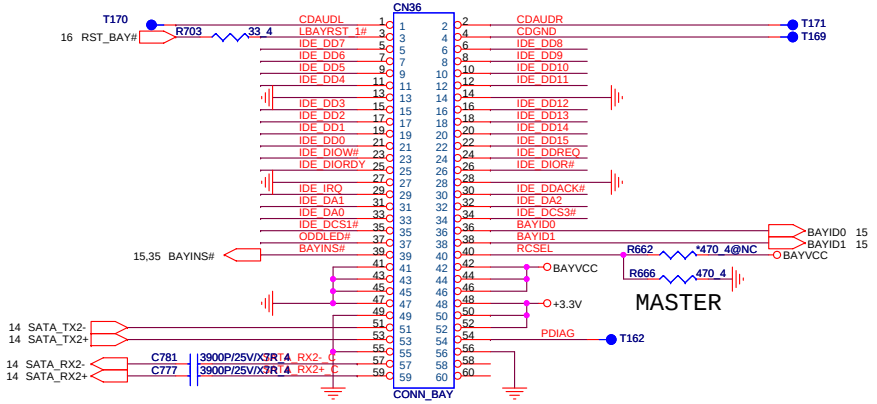
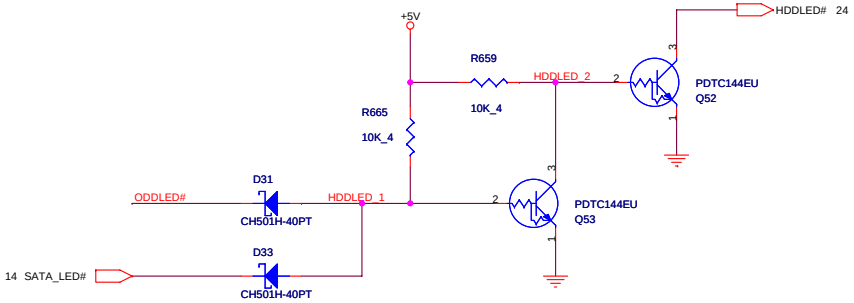


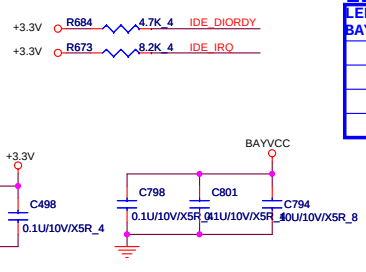




LBAY_ID_STATUS

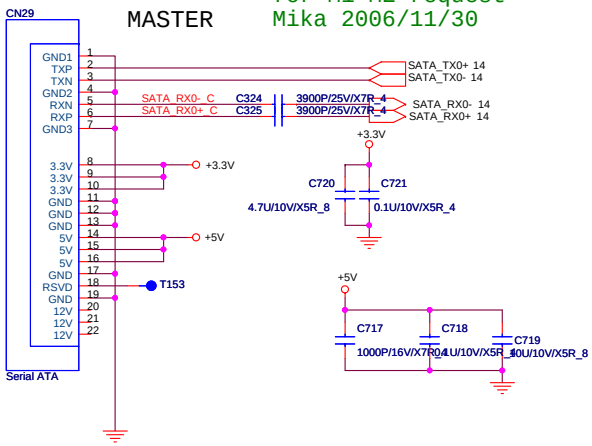
LEFT BAYID1	LEFT BAYID0	STATUS
0	0	Reserve
0	1	ODD
1	0	Reserve
1	1	Reserve



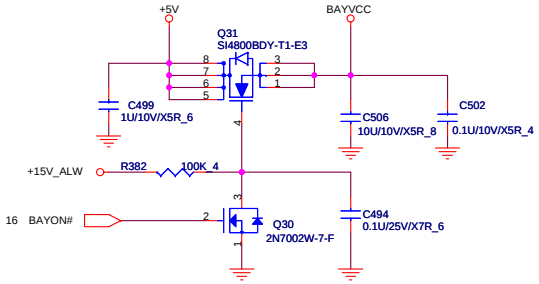


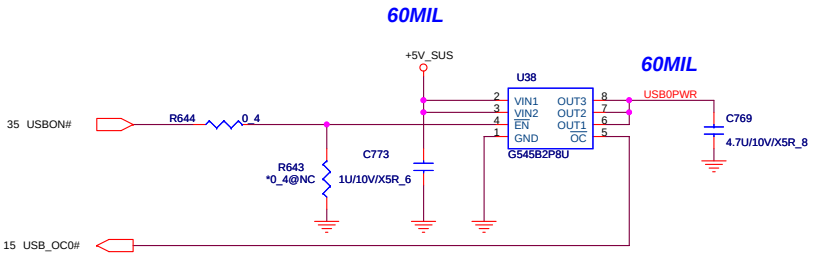
SATA CONNECTOR

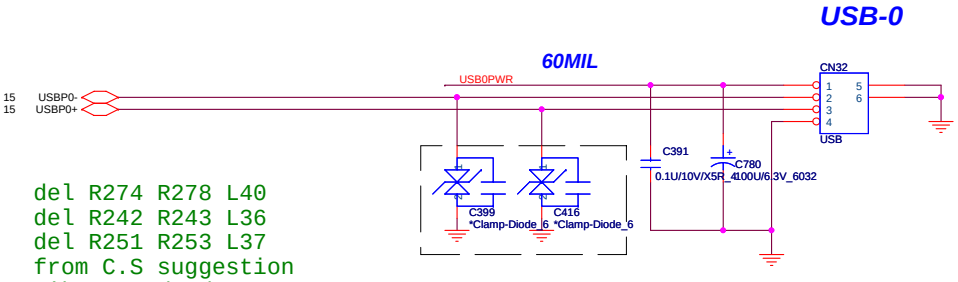
change SATA connector
for M1 ME request
Mika 2006/11/30



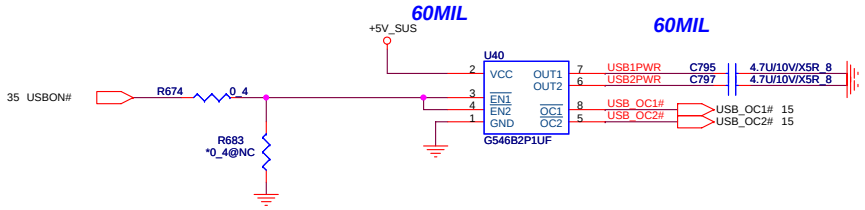
BAY POWER CONTROL

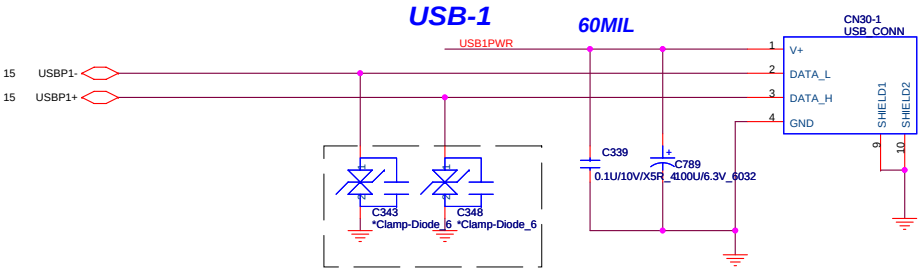


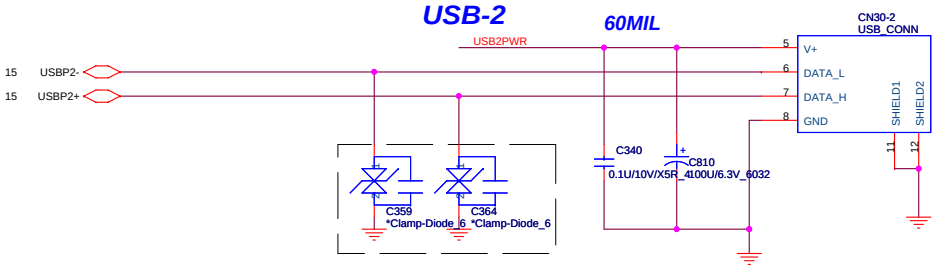




del R274 R278 L40
del R242 R243 L36
del R251 R253 L37
from C.S suggestion
Mika 2007/02/26

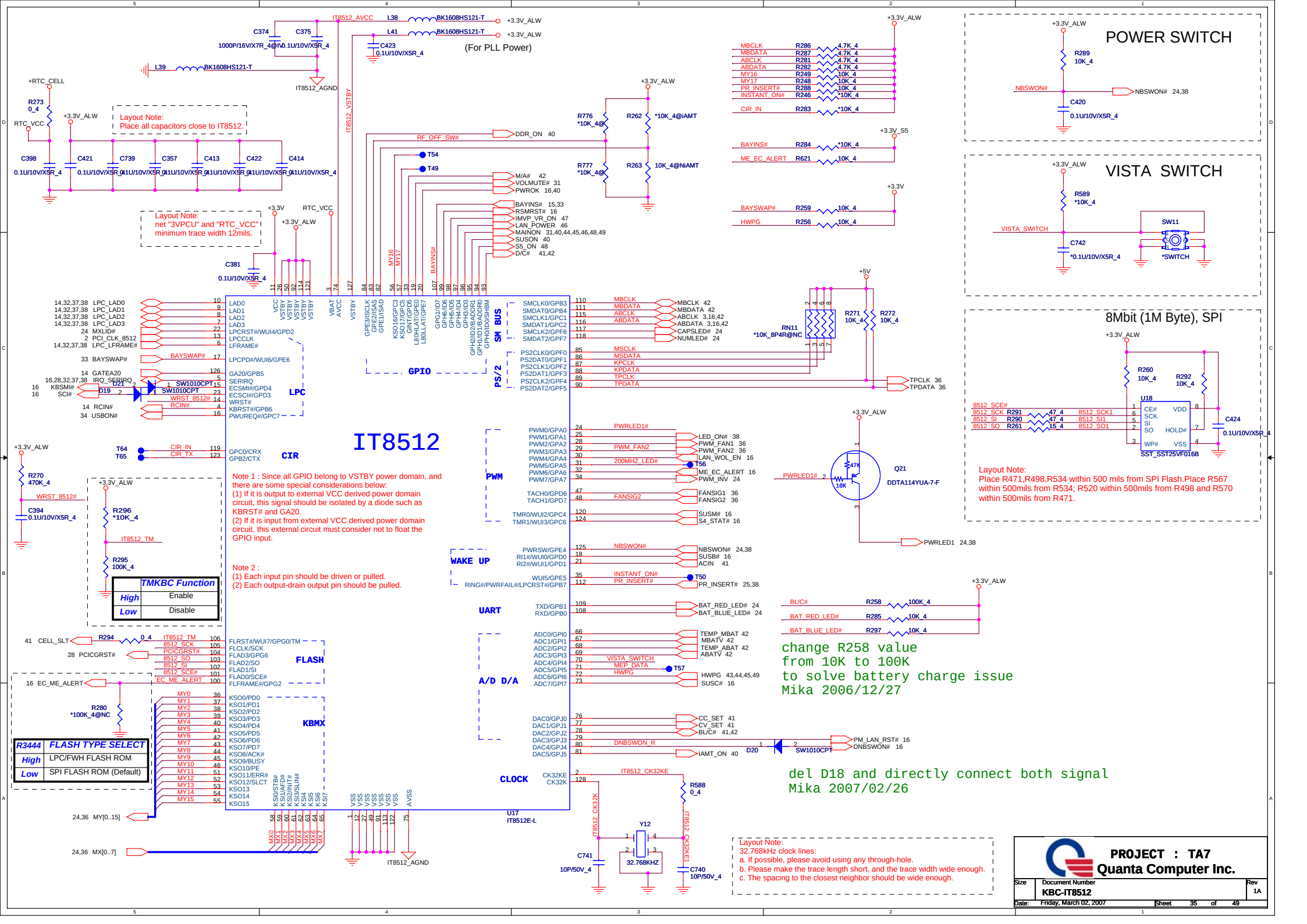






PROJECT : TA7
Quanta Computer Inc.

Size	Document Number	Rev
	USB CONN	1A
Date: Friday, March 02, 2007	Sheet 34 of 49	


IT8512
(For PLL Power)
Layout Note:
Place all capacitors close to IT8512.
Layout Note:
net "3VPCU" and "RTC_VCC"
minimum trace width 12mils.
POWER SWITCH
VISTA SWITCH
8Mbit (1M Byte), SPI
SST_SST25VF016B
Layout Note:
Place R471,R498,R534 within 500 mils from SPI Flash.Place R567 within 500mils from R534; R520 within 500mils from R498 and R570 within 500mils from R471.
GPIO
SM BUS
PS/2
LPC
CIR
PWM
WAKE UP
UART
FLASH
KBMX
A/D D/A
CLOCK
U17
IT8512E-L
Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.
Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.
TMKBC Function
High Enable
Low Disable
R3444 FLASH TYPE SELECT
High LPC/FWH FLASH ROM
Low SPI FLASH ROM (Default)
change R258 value
from 10K to 100K
to solve battery charge issue
Mika 2006/12/27
del D18 and directly connect both signal
Mika 2007/02/26
Layout Note:
32.768kHz clock lines:
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.
PROJECT : TA7
Quanta Computer Inc.
Size
Document Number
KBC-IT8512
Rev
1A
Date: Friday, March 02, 2007
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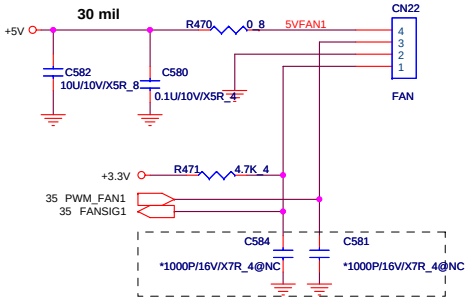
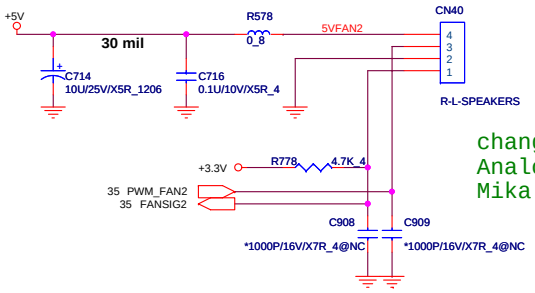
CPU FAN

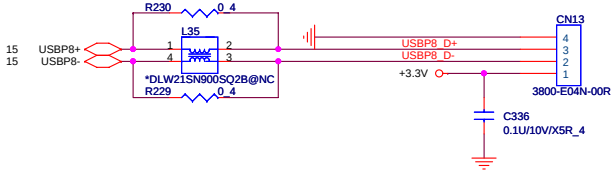


Second FAN for Discrete VGA

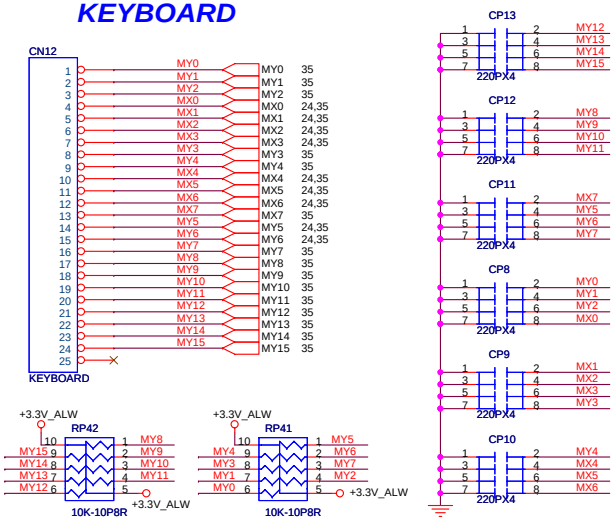


change FAN type from
Analog to PWM
Mika 2006/12/26

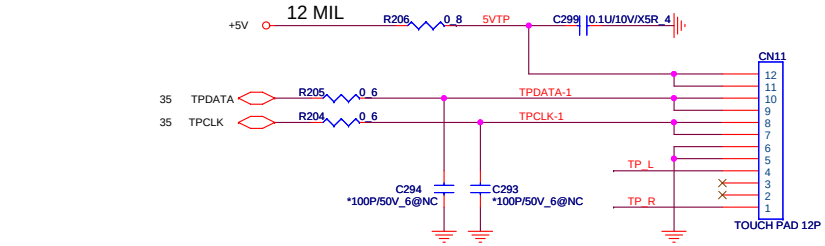
FINGER PRINT CONN

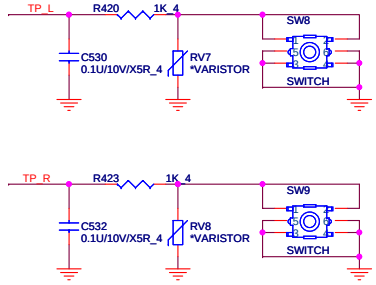


KEYBOARD



TOUCHPAD CONN





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Quanta Computer Inc.

Size	Document Number	Rev
	TPM/TP/KEY/IR/BTB	1A
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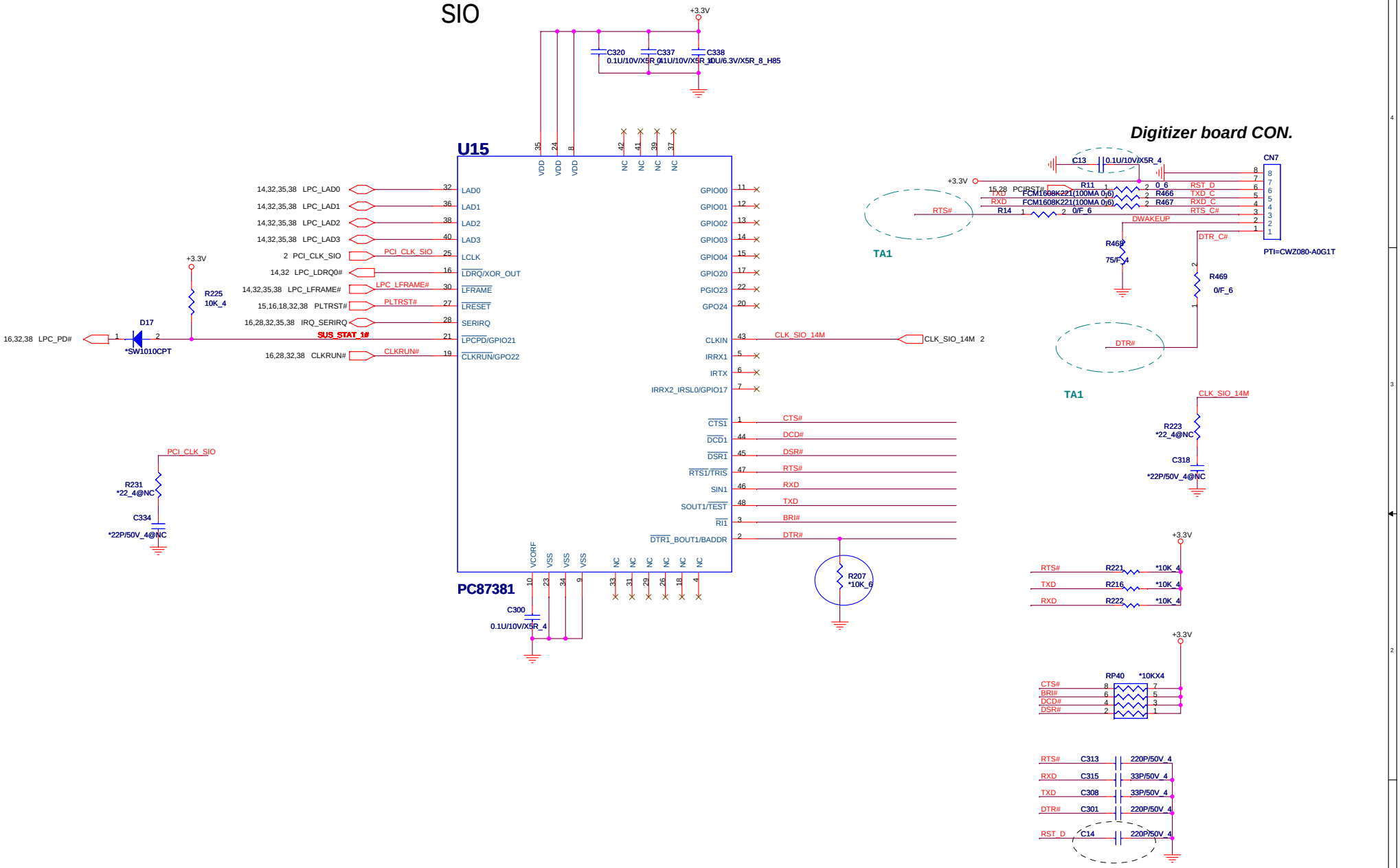
SIO



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Quanta Computer Inc.		
Size	Document Number	Rev
	SUPER I/O - PC87383	1A
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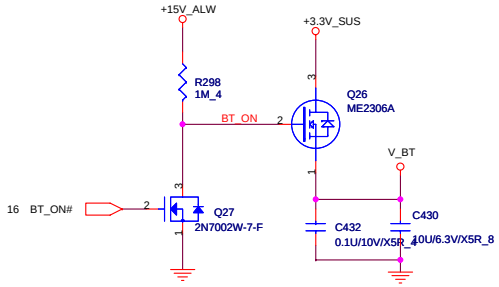
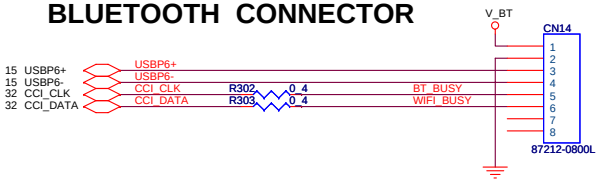
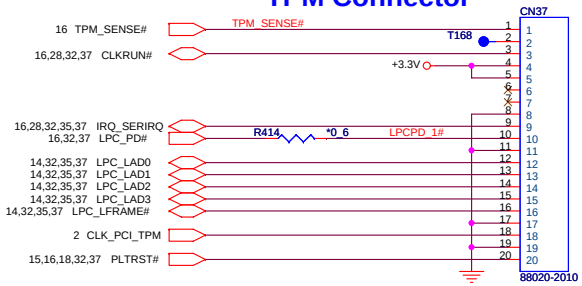


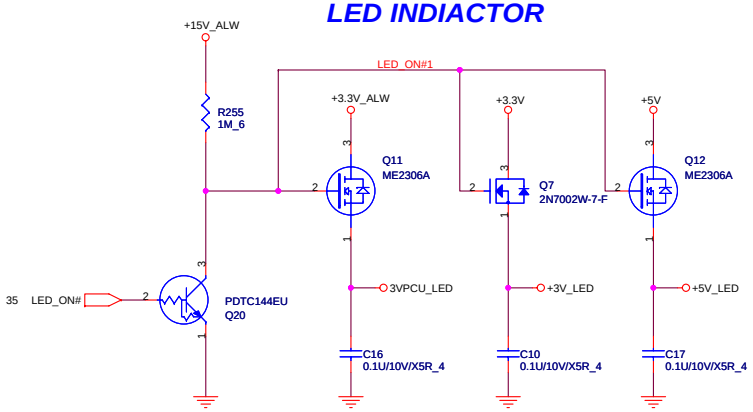
BLUETOOTH CONNECTOR



TPM Connector

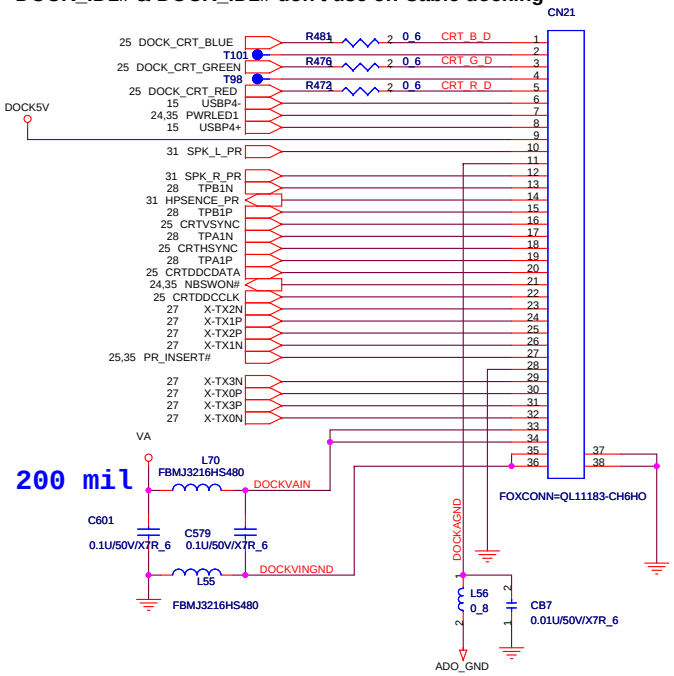


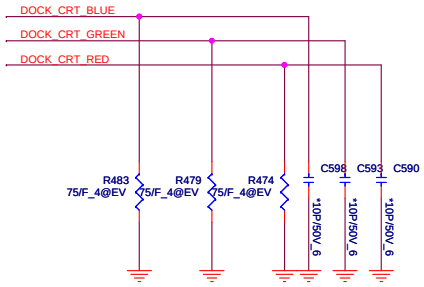
LED INDIACTOR



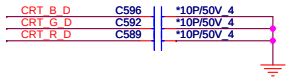
CABLE DOCK

DOCK_ID1# & DOCK_ID2# don't use on Cable docking





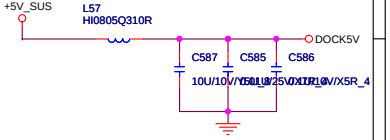
PLACE CLOSE TO CONNECT



PLACE CLOSE TO CONNECT

CRT	Discrete / UMA
R483	75R 150R
R479	75R 150R
R474	75R 150R

Termination Resistor



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Quanta Computer Inc.

Size	Document Number	Rev
	PORT REPLICATOR(152P)	1A

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PAD7 FDTM1012019
PAD8 FDTM1012019

HOLE7 *H-C315D106P2
HOLE8 *H-TC315BC236D106P2
HOLE17 *H-C315D106P2
HOLE21 *H-C315D106P2
HOLE20 *H-C315D118P2
HOLE11 *H-C315D118P2
HOLE10 *H-C315D102P2
HOLE26 *H-C315D118P2
HOLE24 *H-C315D118P2
HOLE18 *H-C315D118P2
HOLE15 *H-C315D118P2
HOLE13 *H-C315D118P2
HOLE14 *H-C315D118P2
HOLE25 *H-C315D118P2
HOLE16 *H-C315D118P2
HOLE35 H-C315D118P2
HOLE30 H-C315D118P2
HOLE9 *H-C315D102P2
HOLE23 *H-T315B217D118P2
HOLE22 *H-T315B217D118P2
HOLE12 *H-C236D236N
HOLE29 H-T276B217I158D118P2
HOLE33 H-T276B217I158D118P2
HOLE34 H-T276B217I158D118P2
HOLE28 H-T276B217I158D118P2
HOLE19 *H-C315D118I158P2

HOLE36 H-C217D142P2
HOLE39 H-C217D142P2
HOLE31 H-C217D142P2
HOLE27 H-C217D142P2
Mini PCI-E Card Screw

HOLE32 H-C217D142P2
HOLE38 H-C217D142P2
TPM module Screw

HOLE37 H-C217D146P2
HOLE40 H-C217D146P2

+PWR_SRC
C263 0.1U/50V/X7R_6
C28 0.1U/50V/X7R_6
C29 0.1U/50V/X7R_6
C385 0.1U/50V/X7R_6
C30 0.1U/50V/X7R_6

+5V_SUS
C7 0.1U/50V/X7R_6
C51 0.1U/50V/X7R_6
C113 0.1U/50V/X7R_6
C451 0.1U/50V/X7R_6
C448 0.1U/50V/X7R_6
C511 0.1U/50V/X7R_6

+1.8V_SUS
C319 0.1U/10V/X5R_4
C396 0.1U/10V/X5R_4
C434 0.1U/10V/X5R_4

+5V_ALW
C316 0.1U/10V/X5R_4
C439 0.1U/10V/X5R_4
C317 0.1U/10V/X5R_4
C912 0.1U/10V/X5R_4
C913 0.1U/10V/X5R_4

+1.05V_VCCP
C279 0.1U/10V/X5R_4
C326 0.1U/10V/X5R_4
C268 0.1U/10V/X5R_4

+1.25V_M
C288 0.1U/50V/X7R_6
C722 0.1U/50V/X7R_6
C452 0.1U/50V/X7R_6
C526 0.1U/50V/X7R_6

+3.3V
C914 0.1U/10V/X5R_4

add C912 C913 C914
from C.S suggestion
Mika 2007/02/26

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Quanta Computer Inc.

Size	Document Number	Rev
	PAD & SCREW	1A
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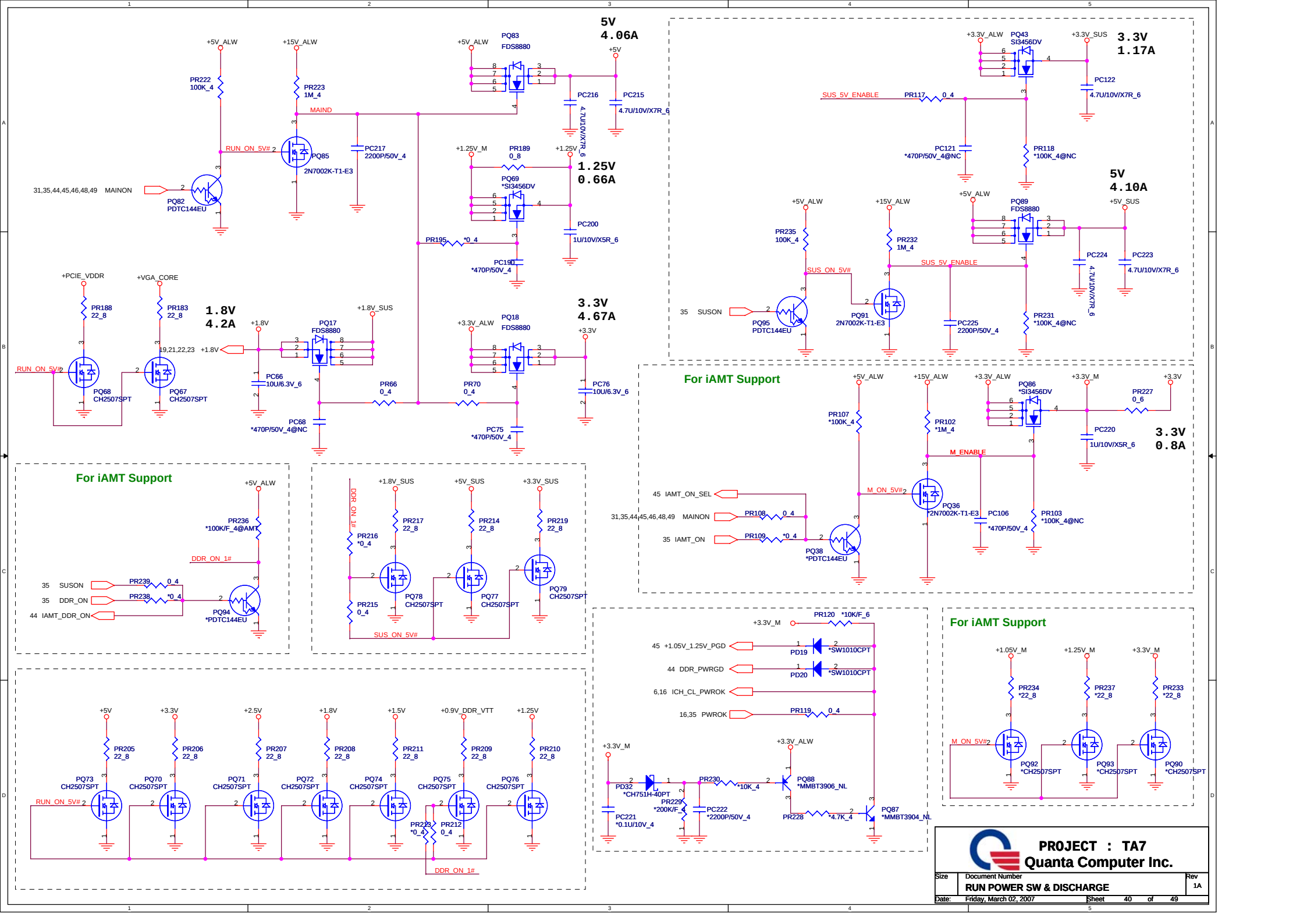
5V
4.06A
1.25V
0.66A
1.8V
4.2A
3.3V
4.67A
3.3V
1.17A
5V
4.10A
3.3V
0.8A
For iAMT Support
For iAMT Support
For iAMT Support
PROJECT : TA7
Quanta Computer Inc.
RUN POWER SW & DISCHARGE
Size
Document Number
Rev
1A
Date: Friday, March 02, 2007
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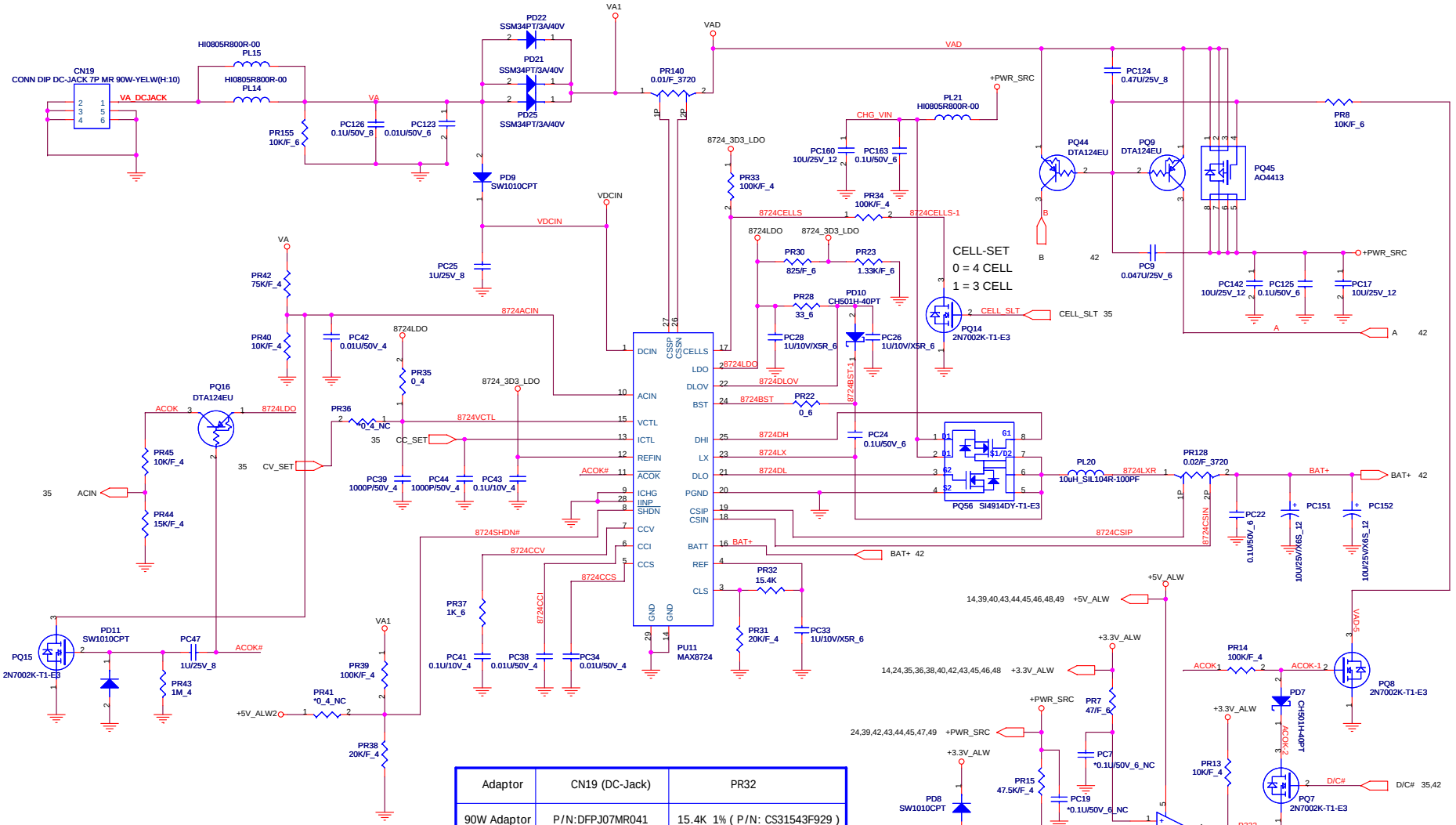
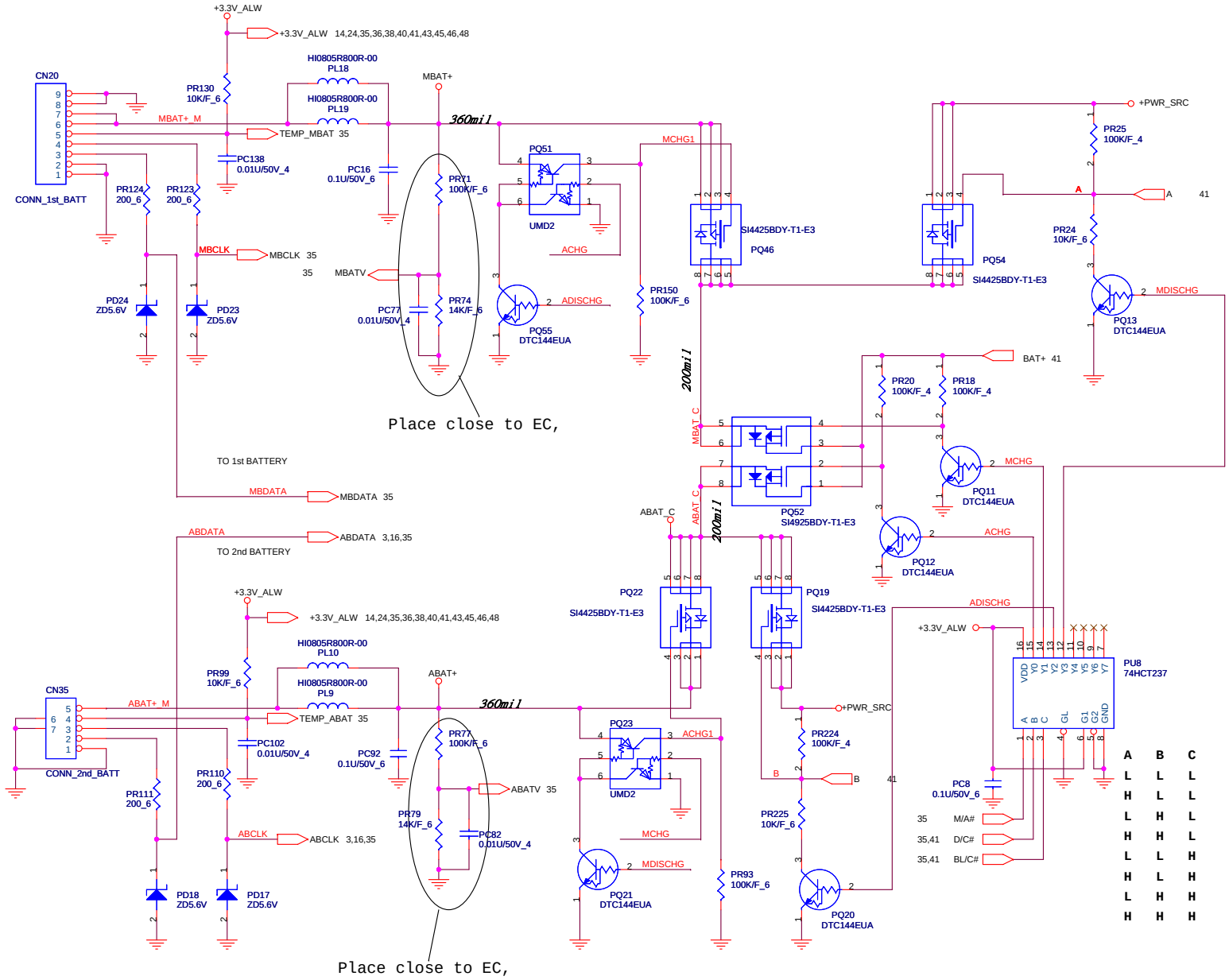


Adaptor	CN19 (DC-Jack)	PR32
90W Adaptor	P/N:DFPJ07MR041	15.4K_1% (P/N: CS31543F929)
65W Adaptor	P/N:DFPJ06MR097	30.9K_1% (P/N: CS33092FB06)

<OrgName>
<OrgAddr1>
<OrgAddr2>
<OrgAddr3>
<OrgAddr4>

PROJECT : TA7
Quanta Computer Inc.

Size	Document Number	Rev
	CHARGER	1A
Date: Friday, March 02, 2007	Sheet 41 of 49	



A	B	C	Y0	Y1	Y2	Y3
L	L	L	H	L	L	L
H	L	L	L	H	L	L
L	H	L	L	L	H	L
H	H	L	L	L	L	H
L	L	H	L	L	L	L
H	L	H	L	L	L	L
L	H	H	L	L	L	L
H	H	H	L	L	L	L

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Quanta Computer Inc.

Size	Document Number	Rev
	BATT SELECTOR	1A

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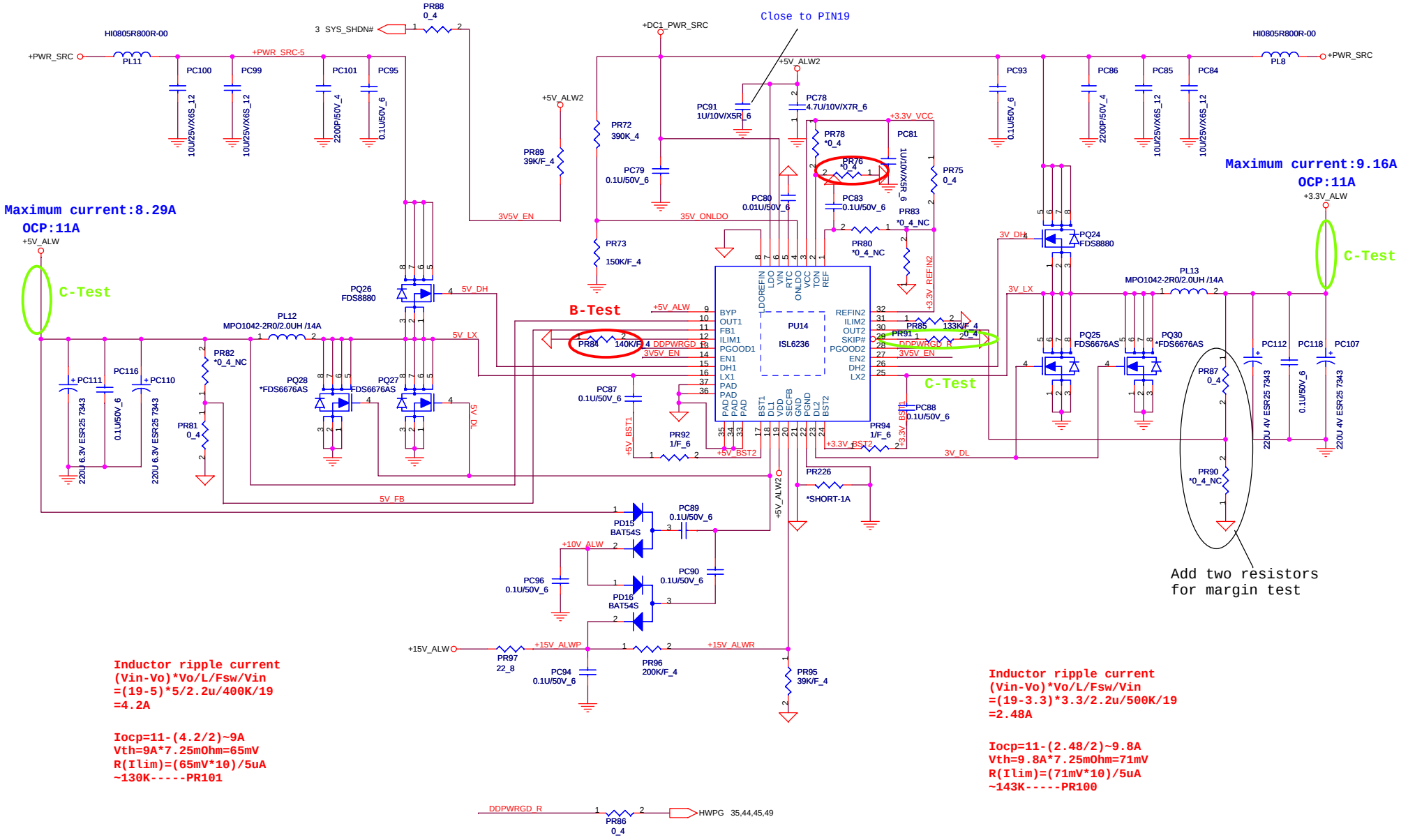

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Quanta Computer Inc.

Size	Document Number	Rev
	+3.3V & +5V	2A
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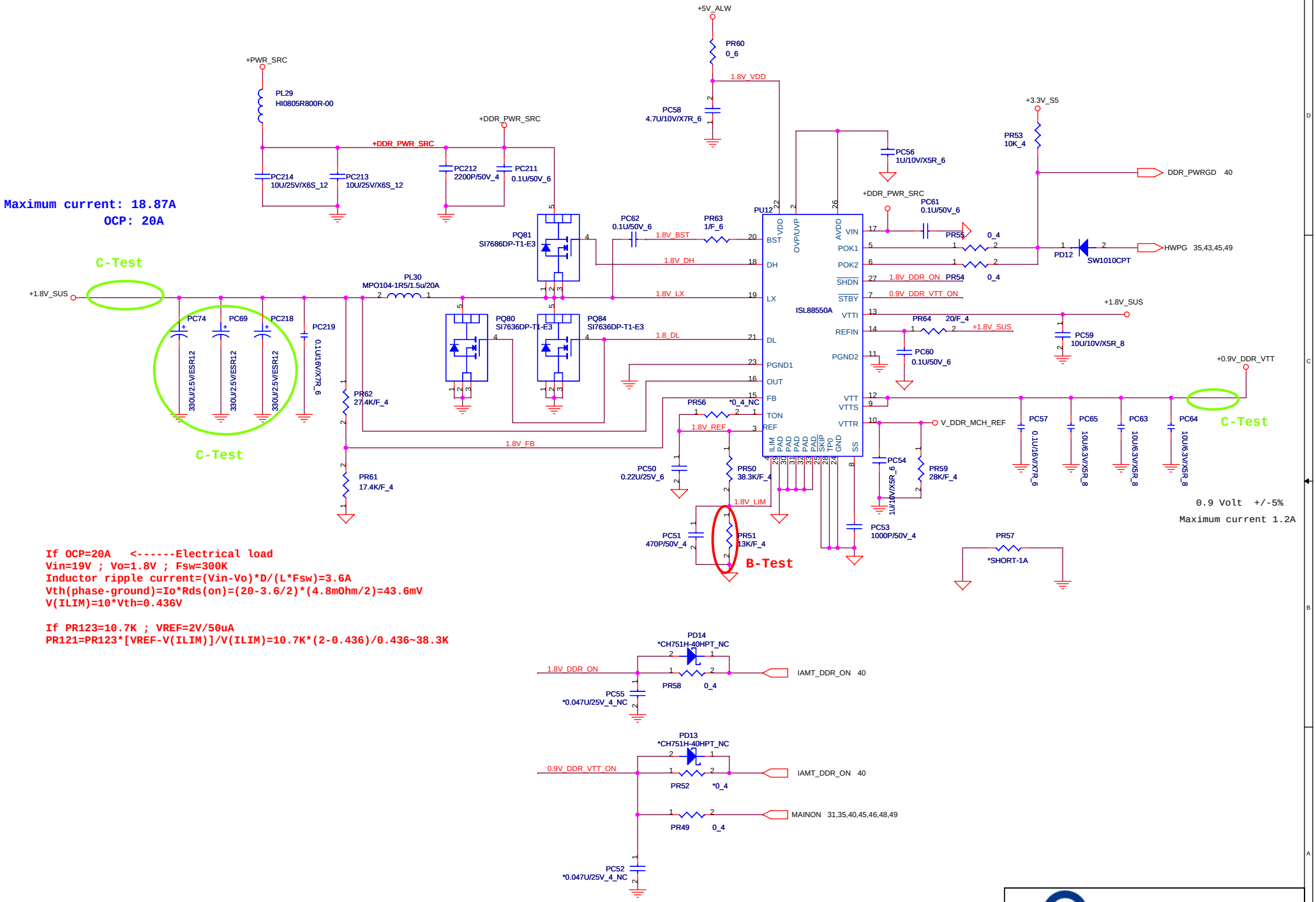

Size	Document Number		Rev
	1.8V_SUS & 0.9V_VTT		2A
Date:	Friday, March 02, 2007	Sheet 44 of 49	

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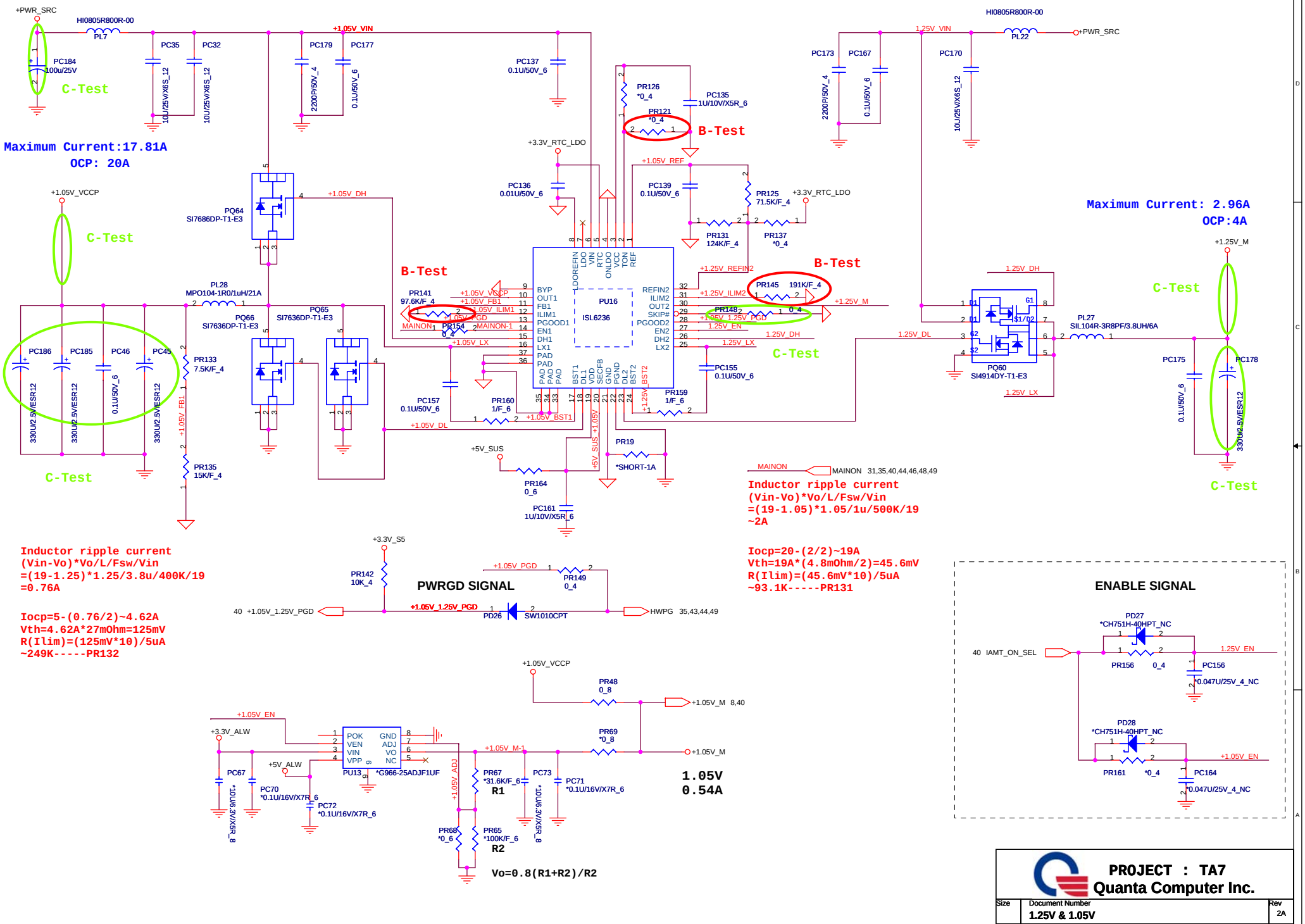
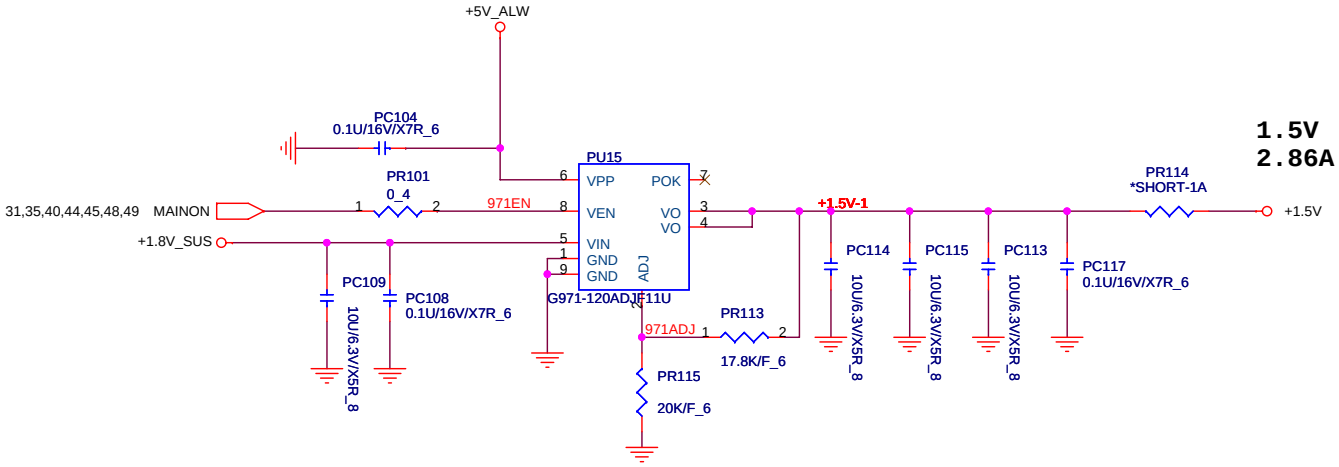
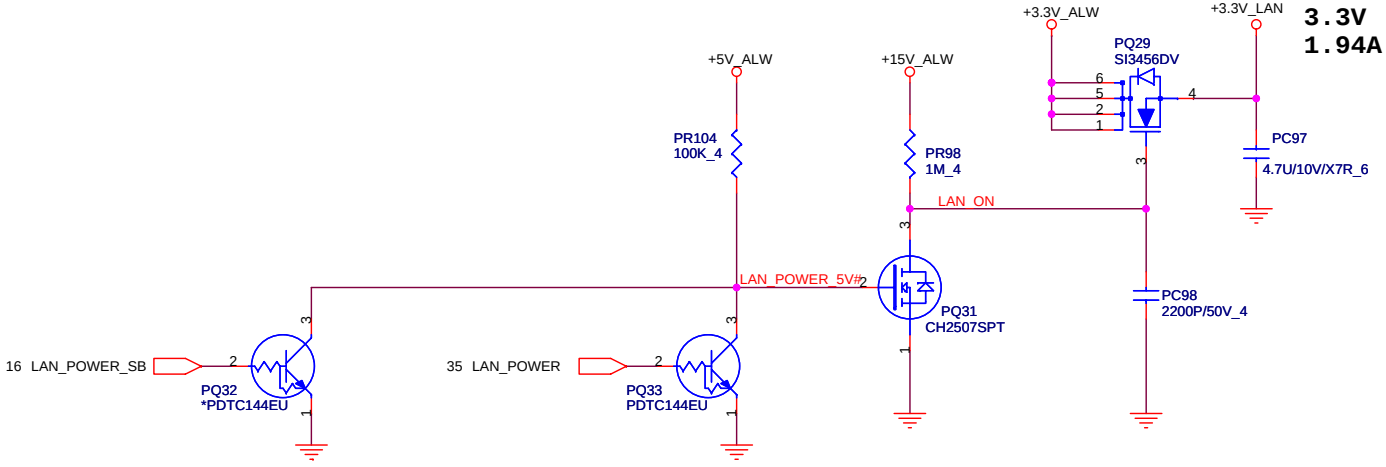
Quanta Computer Inc.



PROJECT : TA7		
Quanta Computer Inc.		
Size	Document Number	Rev
	1.25V & 1.05V	2A
Date: Friday, March 02, 2007	Sheet 45 of 49	



Vout =0.8(1+R1/R2) =
0.8(1+17.8K/20K) =
1.512V



<OrgName>
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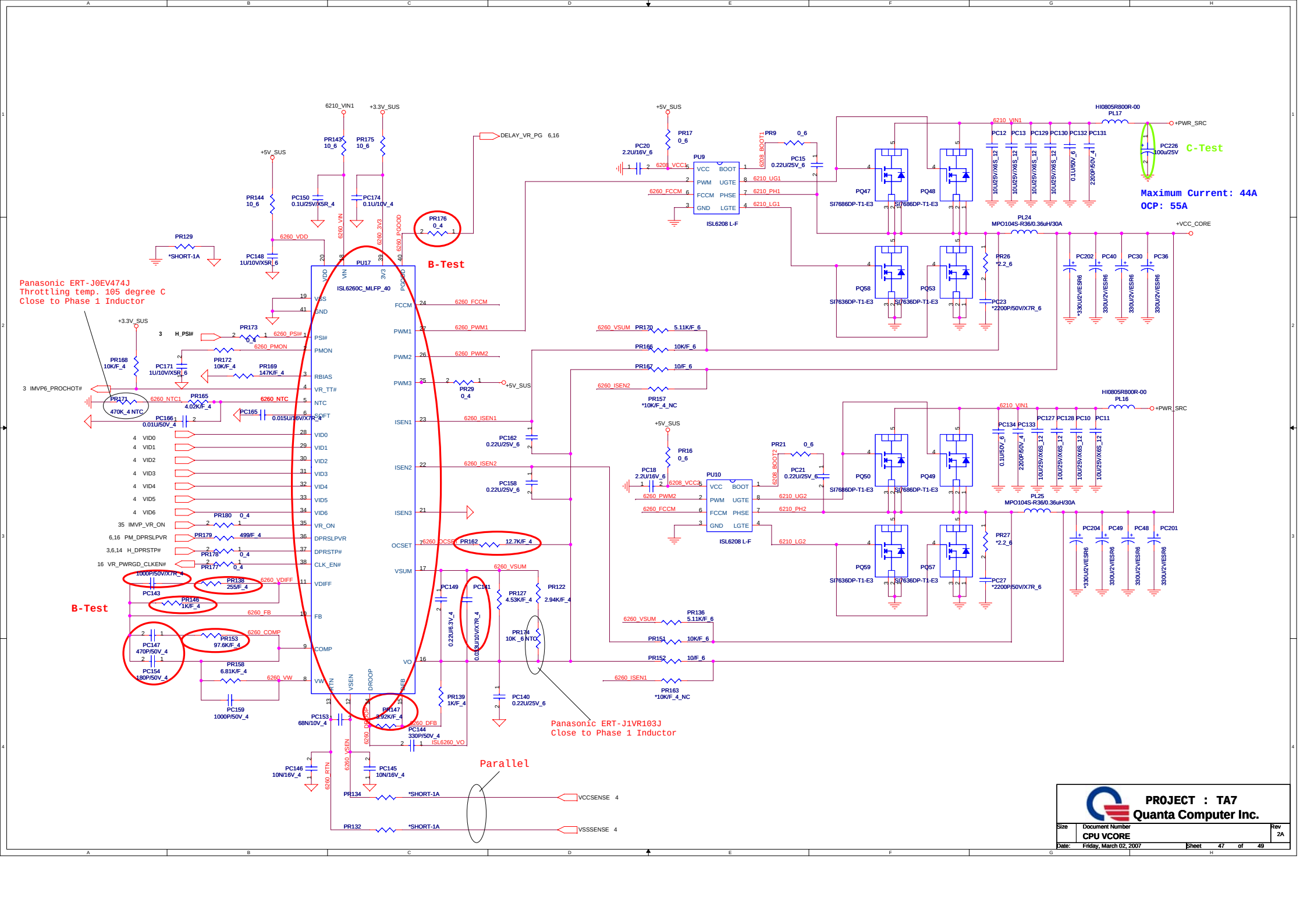
PROJECT : TA7
Quanta Computer Inc.

Size	Document Number	Rev
	1.5V, +3.3V_LAN	1A
Date: Friday, March 02, 2007	Sheet 46 of 49	


Panasonic ERT-J0EV474J
Throttling temp. 105 degree C
Close to Phase 1 Inductor
B-Test
B-Test
Panasonic ERT-J1VR103J
Close to Phase 1 Inductor
Parallel
C-Test
Maximum Current: 44A
OCP: 55A
ISL6260C_MLFP_40
ISL6208 L-F
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Quanta Computer Inc.
CPU VCORE
Size
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2A
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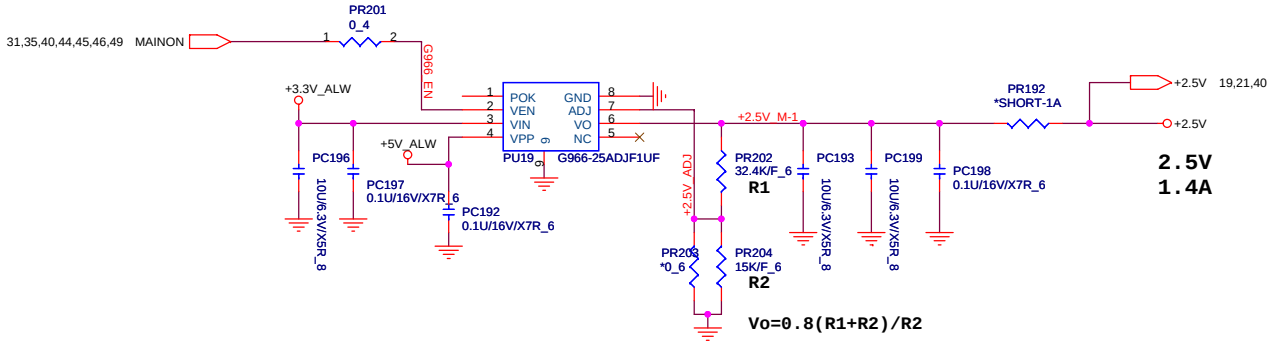
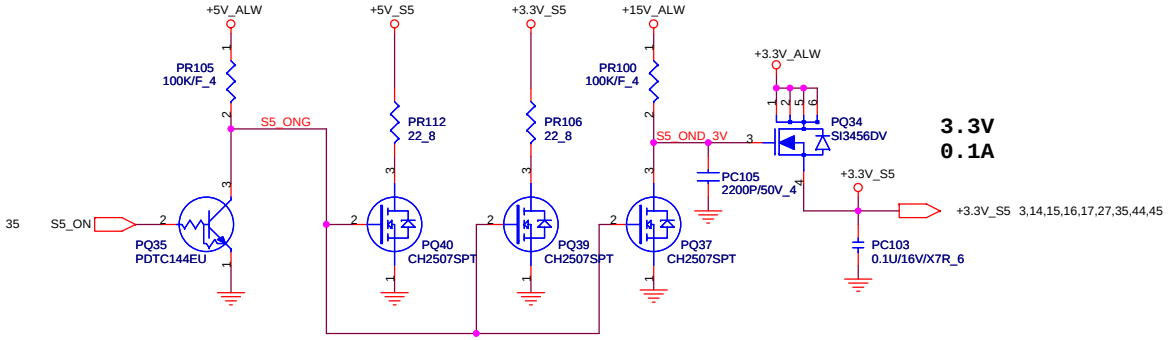
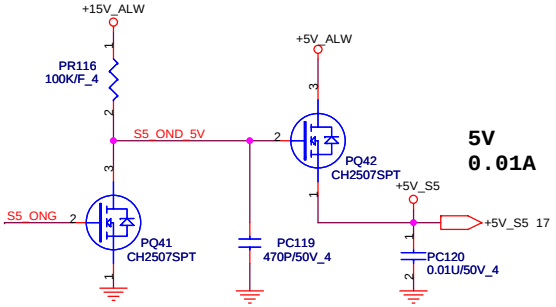
For Discrete M71S Model Only







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Quanta Computer Inc.		
Size	Document Number	Rev
	+2.5V/3VS5/5VS5	1A
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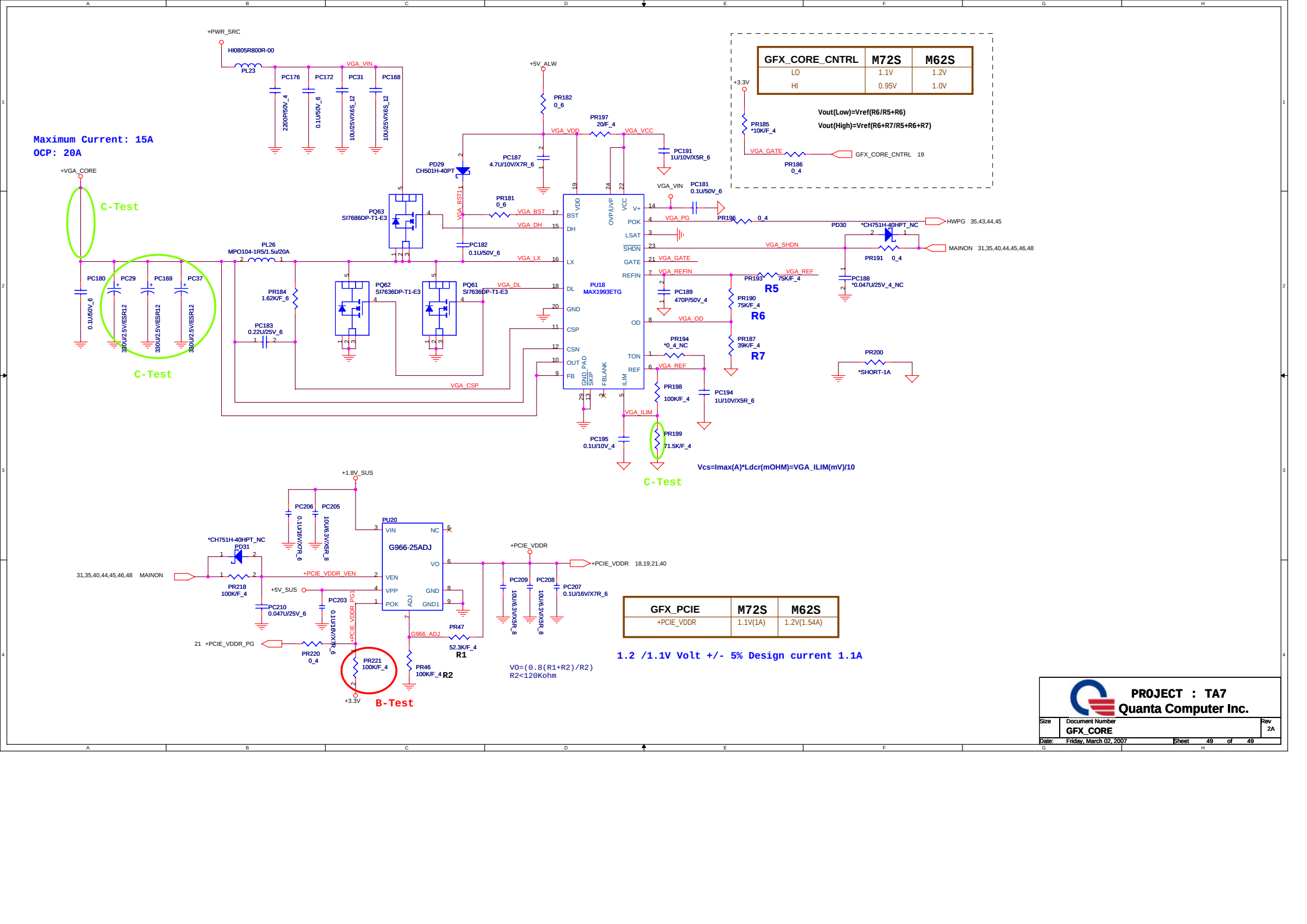
Maximum Current: 15A
OCP: 20A
+PWR_SRC
HI0805R800R-00
PL23
VGA_VIN
PC176
PC172
PC31
PC168
2200P/50V_4
0.1U/50V_6
10U/25V/X6S_12
10U/25V/X6S_12
+5V_ALW
PR182
0_6
PR197
20/F_4
VGA_VDD
VGA_VCC
PC191
1U/10V/X5R_6
PD29
CH501H-40PT
PC187
4.7U/10V/X7R_6
VGA_BST1
PR181
0_6
VGA_BST
VGA_DH
VGA_LX
PC182
0.1U/50V_6
PQ63
SI7686DP-T1-E3
PU18
MAX1993ETG
VDD
BST
DH
LX
DL
GND
CSP
CSN
OUT
FB
OV/PUVP
VCC
V+
POK
LSAT
SHDN
GATE
REFIN
OD
TON
REF
GND_PAD
SKIP
FBLANK
ILIM
VGA_VIN
PC181
0.1U/50V_6
PR196
0_4
VGA_PG
VGA_SHDN
PD30
*CH751H-40HPT_NC
HWPG 35,43,44,45
MAINON 31,35,40,44,45,46,48
PR191
0_4
VGA_GATE
VGA_REFIN
PR193
75K/F_4
VGA_REF
PC189
470P/50V_4
PR190
75K/F_4
R5
R6
VGA_OD
PR194
*0_4_NC
PR187
39K/F_4
R7
PC188
*0.047U/25V_4_NC
PR200
*SHORT-1A
VGA_REF
PR198
100K/F_4
PC194
1U/10V/X5R_6
VGA_ILIM
PC195
0.1U/10V_4
PR199
71.5K/F_4
Vcs=Imax(A)*Ldcr(mOHM)=VGA_ILIM(mV)/10
C-Test
+VGA_CORE
C-Test
PC180
PC29
PC169
PC37
0.1U/50V_6
330U/2.5V/ESR12
330U/2.5V/ESR12
330U/2.5V/ESR12
C-Test
PL26
MPO104-1R5/1.5u/20A
PR184
1.62K/F_6
PC183
0.22U/25V_6
PQ62
SI7636DP-T1-E3
PQ61
SI7636DP-T1-E3
VGA_CSP
GFX_CORE_CNTRL
M72S
M62S
LO
1.1V
1.2V
HI
0.95V
1.0V
+3.3V
Vout(Low)=Vref(R6/R5+R6)
Vout(High)=Vref(R6+R7/R5+R6+R7)
PR185
*10K/F_4
VGA_GATE
GFX_CORE_CNTRL 19
PR186
0_4
+1.8V_SUS
PC206
PC205
0.1U/16V/X7R_6
10U/6.3V/X5R_8
PU20
G966-25ADJ
VIN
NC
VO
VEN
VPP
GND
POK
ADJ
GND1
*CH751H-40HPT_NC
PD31
31,35,40,44,45,46,48 MAINON
PR218
100K/F_4
+PCIE_VDDR_VEN
+5V_SUS
PC203
0.1U/16V/X7R_6
PC210
0.047U/25V_6
+PCIE_VDDR_PG1
G966_ADJ
PR47
52.3K/F_4
R1
21 +PCIE_VDDR_PG
PR220
0_4
PR221
100K/F_4
PR46
100K/F_4
R2
+3.3V
B-Test
+PCIE_VDDR
PC209
PC208
PC207
0.1U/16V/X7R_6
10U/6.3V/X5R_8
10U/6.3V/X5R_8
+PCIE_VDDR 18,19,21,40
GFX_PCIE
M72S
M62S
+PCIE_VDDR
1.1V(1A)
1.2V(1.54A)
1.2 /1.1V Volt +/- 5% Design current 1.1A
VO=(0.8(R1+R2)/R2)
R2<120Kohm
PROJECT : TA7
Quanta Computer Inc.
Size
Document Number
GFX_CORE
Rev
2A
Date: Friday, March 02, 2007
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