SA8 SYSTEM DIAGRAM

AMD Smarter Choice

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND1
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : IN3
- LAYER 7 : SGND2
- LAYER 8 : BOT

DDRII-SODIMM1 PAGE 6,7 — DDRII 667/800 MHz
DDRII-SODIMM2 PAGE 6,7 — DDRII 667/800 MHz

AMD Griffin Lion Sabie
S1G2 Processor
638P (uPGA)/35W
PAGE 3,4,5

CPU THERMAL SENSOR PAGE 5

14.31818MHz

CLOCK GEN
ICS9LPRS476AKLFT-->HP
SLG8SP626VTR-->HP
RTM880N-795 -->HP
PAGE 2

CPU_CLK
NBGFX_CLK
NBGPP_CLK
SBLINK_CLK

HT3

PCI-E

PCI-Express 16X

NORTH BRIDGE
RS780MN
29mm X 29mm, 528pin BGA
PAGE 8,9,10,11,

HDMI PAGE 23
CRT PAGE 25
LVDS PAGE 24

ATI Hybrid CrossFire
128 Bit GDDR3*4
M82M/M86LP
PAGE 17,18,19 20,21,22

LAN
PCIE-LAN
MARVELL_88E8040
(10/100/GagaLAN)
PAGE 26

Express Card X1
(NEW CARD)
PAGE 35

Mini PCI-E Card X2
(Wireless LAN)
PAGE 30

RJ45 PAGE 26

Side port
Reserved
256mb RAM for UMA only PAGE 8

PCIE X4

SBSRC_CLK

USB2.0

SOUTH BRIDGE
SB700
21mm X 21mm, 528pin BGA
4.5W(Ext)
4.3W(Int)
PAGE 12,13.14.15.16

0,8,2	1	6	4,5	11	7
USB2.0 Ports X3 PAGE 31,32	Bluetooth PAGE 31	Fingerprint PAGE 31	Mini PCI-E X2 PAGE 30	Express Card X1 (NEW CARD) PAGE 35	Camera PAGE 24

SATA - HDD PAGE 29 — SATA0
SATA - ODD PAGE 29 — SATA4

PCI BUS / 33MHz

CARD reader
OZ126T
PAGE 27

Azalia

CX20561
AUDIO CODEC
PAGE 28

MDC CONN PAGE 31

RJ11
to Daughter board

AUDIO Amplifier
TPA6017A2
PAGE 28

AUDIO CONN
(Phone/ MIC)
PAGE 28

Speaker Conn.
PAGE 28

LPC

Keyboard PAGE 34
Touch Pad PAGE 34

KBC
ITE
IT8502
PAGE 33

FAN PAGE 32

SPI FLASH PAGE 33

SYSTEM CHARGER PAGE 36

SYSTEM POWER PAGE 37

DDR II SMDDR_VTERM 1.8V/1.8VSUS PAGE 39

VCCP +1.2V & +1.1V PAGE 38

VGACORE(1.1V~1.2V) PAGE 42

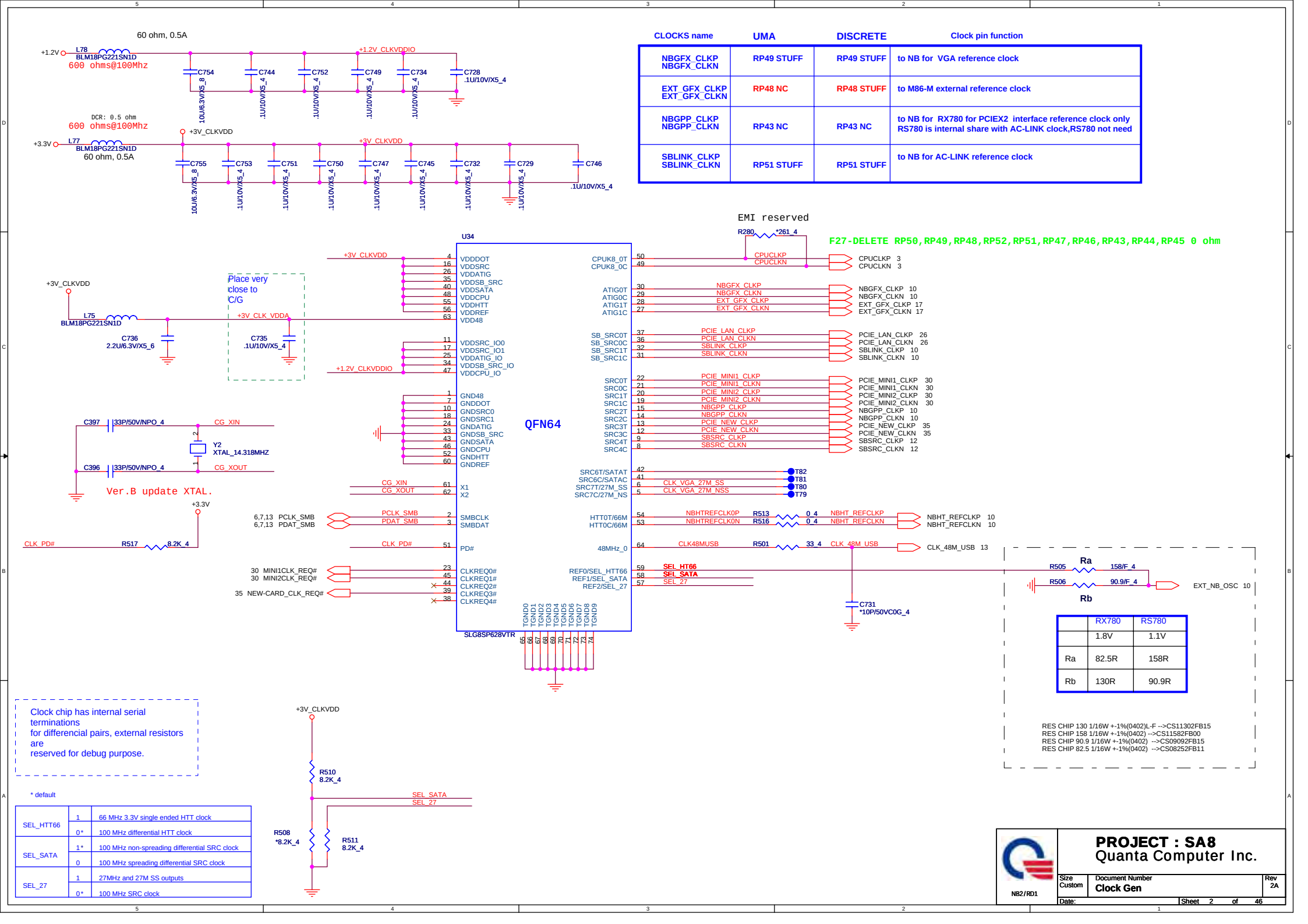
CPU CORE +VCORE0 +VCORE1 PAGE 40

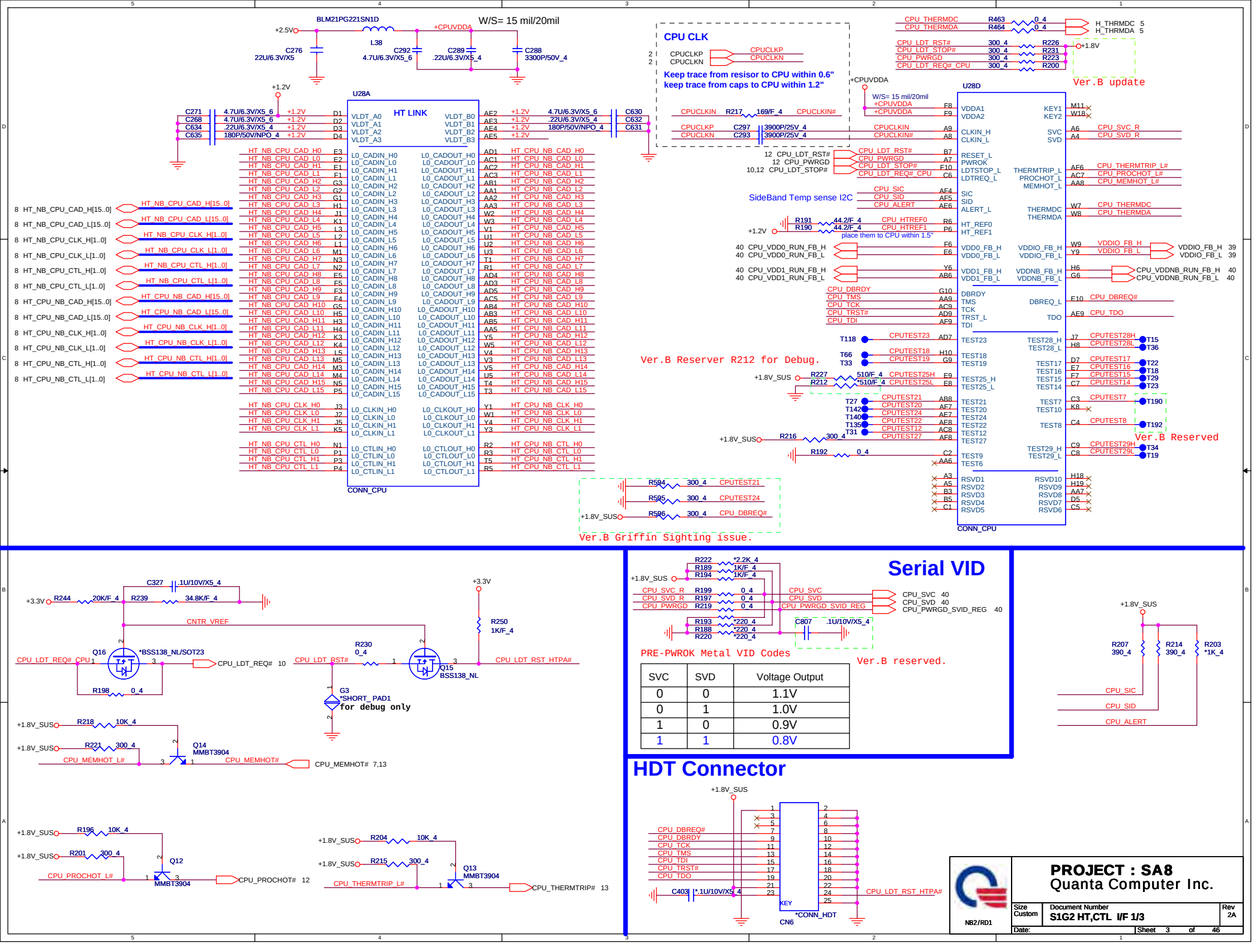
SMBUS TABLE		
SB--SCL0/SD0	Clock gen /DDR2/DDR2 thermal/Accelerometer	+3V
SB--SCL1/SD1	Wlan Card	+3V/S5
SB--SCL2/SD2	epress card	+3v/S5
EC --SCL/SD	Battery charge/discharge	+3VPCU
EC--SCL2/SD2	VGA thermal/system thermal	+3V

NB2/RD1

PROJECT : SA8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	1A
Date:	Sheet 1 of 46	


60 ohm, 0.5A
+1.2V
L78
BLM18PG221SN1D
600 ohms@100Mhz
C754
C744
C752
C749
C734
C728
.1U/10V/X5_4
+1.2V_CLKVDDIO
DCR: 0.5 ohm
600 ohms@100Mhz
+3.3V
L77
BLM18PG221SN1D
60 ohm, 0.5A
+3V_CLKVDD
C755
C753
C751
C750
C747
C745
C732
C729
C746
10U/6.3V/X5_8
.1U/10V/X5_4
CLOCKS name
UMA
DISCRETE
Clock pin function
NBGFX_CLKP
NBGFX_CLKN
RP49 STUFF
RP49 STUFF
to NB for VGA reference clock
EXT_GFX_CLKP
EXT_GFX_CLKN
RP48 NC
RP48 STUFF
to M86-M external reference clock
NBGPP_CLKP
NBGPP_CLKN
RP43 NC
RP43 NC
to NB for RX780 for PCIEX2 interface reference clock only
RS780 is internal share with AC-LINK clock,RS780 not need
SBLINK_CLKP
SBLINK_CLKN
RP51 STUFF
RP51 STUFF
to NB for AC-LINK reference clock
EMI reserved
R280
*261_4
F27-DELETE RP50,RP49,RP48,RP52,RP51,RP47,RP46,RP43,RP44,RP45 0 ohm
U34
QFN64
SLG8SP628VTR
VDDDOT
VDDSRC
VDDATIG
VDDSB_SRC
VDDSATA
VDDCPU
VDDHTT
VDDREF
VDD48
VDDSRC_IO0
VDDSRC_IO1
VDDATIG_IO
VDDSB_SRC_IO
VDDCPU_IO
GND48
GNDDOT
GNDSRC0
GNDSRC1
GNDATIG
GNDSB_SRC
GNDSATA
GNDCPU
GNDHTT
GNDREF
X1
X2
SMBCLK
SMBDAT
PD#
CLKREQ0#
CLKREQ1#
CLKREQ2#
CLKREQ3#
CLKREQ4#
TGND0
TGND1
TGND2
TGND3
TGND4
TGND5
TGND6
TGND7
TGND8
TGND9
CPUK8_0T
CPUK8_0C
CPUCLKP
CPUCLKN
ATIG0T
ATIG0C
ATIG1T
ATIG1C
NBGFX_CLKP
NBGFX_CLKN
EXT_GFX_CLKP
EXT_GFX_CLKN
SB_SRC0T
SB_SRC0C
SB_SRC1T
SB_SRC1C
PCIE_LAN_CLKP
PCIE_LAN_CLKN
SBLINK_CLKP
SBLINK_CLKN
SRC0T
SRC0C
SRC1T
SRC1C
SRC2T
SRC2C
SRC3T
SRC3C
SRC4T
SRC4C
PCIE_MINI1_CLKP
PCIE_MINI1_CLKN
PCIE_MINI2_CLKP
PCIE_MINI2_CLKN
NBGPP_CLKP
NBGPP_CLKN
PCIE_NEW_CLKP
PCIE_NEW_CLKN
SBSRC_CLKP
SBSRC_CLKN
SRC6T/SATAT
SRC6C/SATAC
SRC7T/27M_SS
SRC7C/27M_NS
CLK_VGA_27M_SS
CLK_VGA_27M_NSS
T82
T81
T80
T79
HTT0T/66M
HTT0C/66M
NBHTREFCLK0P
NBHTREFCLK0N
NBHT_REFCLKP
NBHT_REFCLKN
48MHz_0
CLK48MUSB
CLK_48M_USB
REF0/SEL_HTT66
REF1/SEL_SATA
REF2/SEL_27
SEL_HT66
SEL_SATA
SEL_27
+3V_CLK_VDDA
Place very close to C/G
C736
2.2U/6.3V/X5_6
C735
.1U/10V/X5_4
C731
*10P/50VC0G_4
C397
33P/50V/NPO_4
C396
33P/50V/NPO_4
CG_XIN
CG_XOUT
Y2
XTAL_14.318MHZ
Ver.B update XTAL.
PCLK_SMB
PDAT_SMB
CLK_PD#
R517
8.2K_4
R513
R516
R501
33_4
Ra
Rb
R505
158/F_4
R506
90.9/F_4
EXT_NB_OSC
RX780
RS780
1.8V
1.1V
Ra
82.5R
158R
Rb
130R
90.9R
RES CHIP 130 1/16W +-1%(0402)L-F -->CS11302FB15
RES CHIP 158 1/16W +-1%(0402) -->CS11582FB00
RES CHIP 90.9 1/16W +-1%(0402) -->CS09092FB15
RES CHIP 82.5 1/16W +-1%(0402) -->CS08252FB11
Clock chip has internal serial terminations
for differencial pairs, external resistors are
reserved for debug purpose.
R510
8.2K_4
R508
*8.2K_4
R511
8.2K_4
SEL_SATA
SEL_27
* default
SEL_HTT66
1 66 MHz 3.3V single ended HTT clock
0* 100 MHz differential HTT clock
SEL_SATA
1* 100 MHz non-spreading differential SRC clock
0 100 MHz spreading differential SRC clock
SEL_27
1 27MHz and 27M SS outputs
0* 100 MHz SRC clock
PROJECT : SA8
Quanta Computer Inc.
NB2/RD1
Size
Custom
Document Number
Clock Gen
Rev
2A
Date:
Sheet 2 of 46



SVC	SVD	Voltage Output
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

PROJECT : SA8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	S1G2 HT,CTL I/F 1/3	2A
Date:	Sheet 3 of 46	

NB2/RD1

Processor Memory Interface

PLACE CLOSE TO CPU WITHIN 1"

U28B — MEM:CMD/CTRL/CLK — CONN_CPU

+0.9VSMVTT

750 mA

R236 39.2/F_4 M_ZP
R229 39.2/F_4 M_ZN
+1.8V_SUS

T71 MEM_MA_RESET#

6,7 MEM_MA0_ODT0
6,7 MEM_MA0_ODT1
6,7 MEM_MA0_CS#0
6,7 MEM_MA0_CS#1
6,7 MEM_MA_CKE0
6,7 MEM_MA_CKE1
6 MEM_MA_CLK1_P
6 MEM_MA_CLK1_N
6 MEM_MA_CLK7_P
6 MEM_MA_CLK7_N

6,7 MEM_MA_ADD[0..15]
MEM_MA_ADD0 N21
MEM_MA_ADD1 M20
MEM_MA_ADD2 N22
MEM_MA_ADD3 M19
MEM_MA_ADD4 M22
MEM_MA_ADD5 L20
MEM_MA_ADD6 M24
MEM_MA_ADD7 L21
MEM_MA_ADD8 L19
MEM_MA_ADD9 K22
MEM_MA_ADD10 R21
MEM_MA_ADD11 L22
MEM_MA_ADD12 K20
MEM_MA_ADD13 V24
MEM_MA_ADD14 K24
MEM_MA_ADD15 K19

6,7 MEM_MA_BANK0
6,7 MEM_MA_BANK1
6,7 MEM_MA_BANK2
6,7 MEM_MA_RAS#
6,7 MEM_MA_CAS#
6,7 MEM_MA_WE#

CPU_VTT_SENSE 39

MEMVREF_CPU

MEM_MB_RESET# T72

MEM_MB0_ODT0 6,7
MEM_MB0_ODT1 6,7
MEM_MB0_CS#0 6,7
MEM_MB0_CS#1 6,7
MEM_MB_CKE0 6,7
MEM_MB_CKE1 6,7
MEM_MB_CLK1_P 6
MEM_MB_CLK1_N 6
MEM_MB_CLK7_P 6
MEM_MB_CLK7_N 6

MEM_MB_ADD[0..15] 6,7
MEM_MB_BANK0 6,7
MEM_MB_BANK1 6,7
MEM_MB_BANK2 6,7
MEM_MB_RAS# 6,7
MEM_MB_CAS# 6,7
MEM_MB_WE# 6,7

+1.8V_SUS
R272 2K/F_4
R273 *0_4 Reserved
R271 2K/F_4
C400 .1U/10V/X5_4
C401 1000P/50V_4
+0.9VSMVREF 6,39

6 MEM_MB_DATA[0..63]
6 MEM_MB_DM[0..7]
6 MEM_MB_DQS0_P
6 MEM_MB_DQS0_N
6 MEM_MB_DQS1_P
6 MEM_MB_DQS1_N
6 MEM_MB_DQS2_P
6 MEM_MB_DQS2_N
6 MEM_MB_DQS3_P
6 MEM_MB_DQS3_N
6 MEM_MB_DQS4_P
6 MEM_MB_DQS4_N
6 MEM_MB_DQS5_P
6 MEM_MB_DQS5_N
6 MEM_MB_DQS6_P
6 MEM_MB_DQS6_N
6 MEM_MB_DQS7_P
6 MEM_MB_DQS7_N

U28C — MEM:DATA — CONN_CPU

MEM_MA_DATA[0..63] 6
MEM_MA_DM[0..7] 6
MEM_MA_DQS0_P 6
MEM_MA_DQS0_N 6
MEM_MA_DQS1_P 6
MEM_MA_DQS1_N 6
MEM_MA_DQS2_P 6
MEM_MA_DQS2_N 6
MEM_MA_DQS3_P 6
MEM_MA_DQS3_N 6
MEM_MA_DQS4_P 6
MEM_MA_DQS4_N 6
MEM_MA_DQS5_P 6
MEM_MA_DQS5_N 6
MEM_MA_DQS6_P 6
MEM_MA_DQS6_N 6
MEM_MA_DQS7_P 6
MEM_MA_DQS7_N 6

Place close to socket

+0.9VSMVTT
C319 4.7U/6.3V/X5_6
C352 4.7U/6.3V/X5_6
C336 4.7U/6.3V/X5_6
C322 4.7U/6.3V/X5_6
C321 .22U/6.3V/X5_4
C323 .22U/6.3V/X5_4
C335 .22U/6.3V/X5_4
C351 .22U/6.3V/X5_4

+0.9VSMVTT
C347 1000P/50V_4
C329 1000P/50V_4
C340 1000P/50V_4
C328 1000P/50V_4
C313 180P/50V/NPO_4
C320 180P/50V/NPO_4
C324 180P/50V/NPO_4
C325 180P/50V/NPO_4

MEM_MB_CLK7_P
C373 1.5P/50V/NPO_4
MEM_MB_CLK7_N
MEM_MB_CLK1_P
C388 1.5P/50V/NPO_4
MEM_MB_CLK1_N

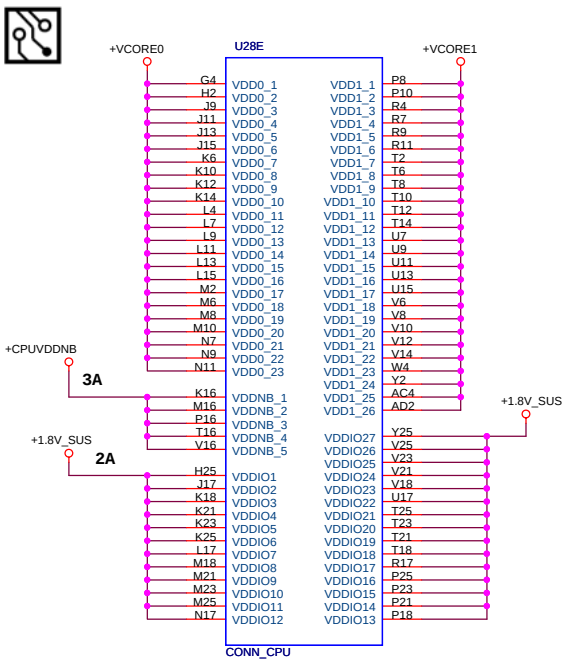
Close to CPU within 1500 mils

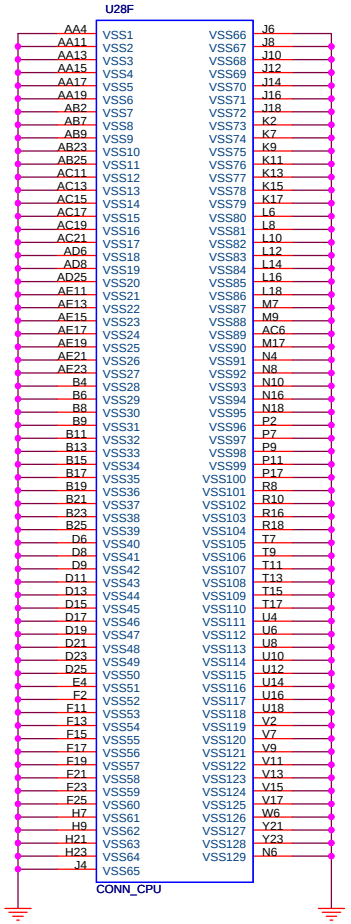
MEM_MA_CLK7_P
C362 1.5P/50V/NPO_4
MEM_MA_CLK7_N
MEM_MA_CLK1_P
C374 1.5P/50V/NPO_4
MEM_MA_CLK1_N

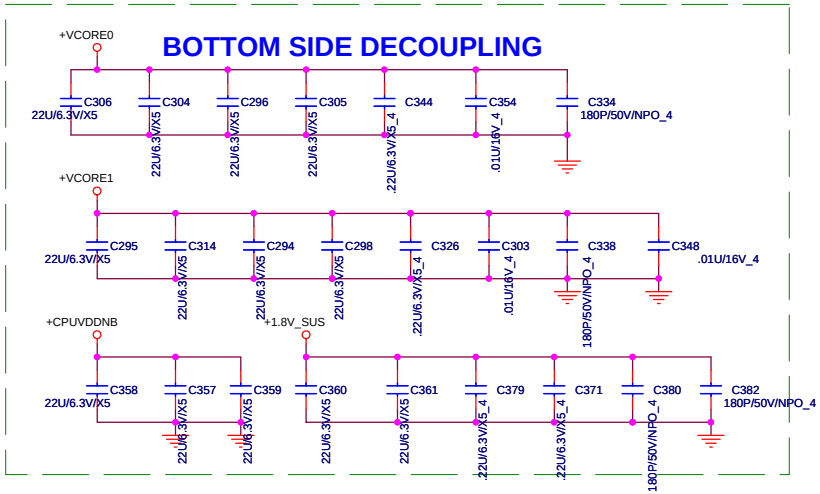
NB2/RD1

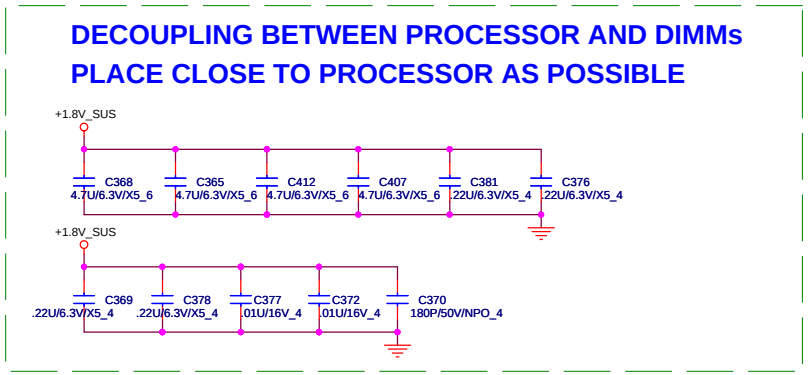
PROJECT : SA8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	S1G2 DDRII MEMORY I/F 2/3	1A
Date:	Sheet 4 of 46	

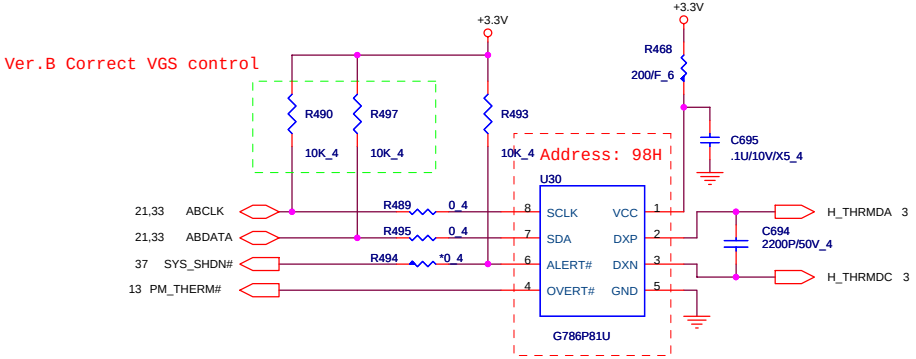


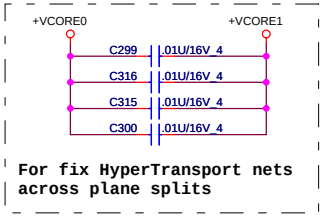






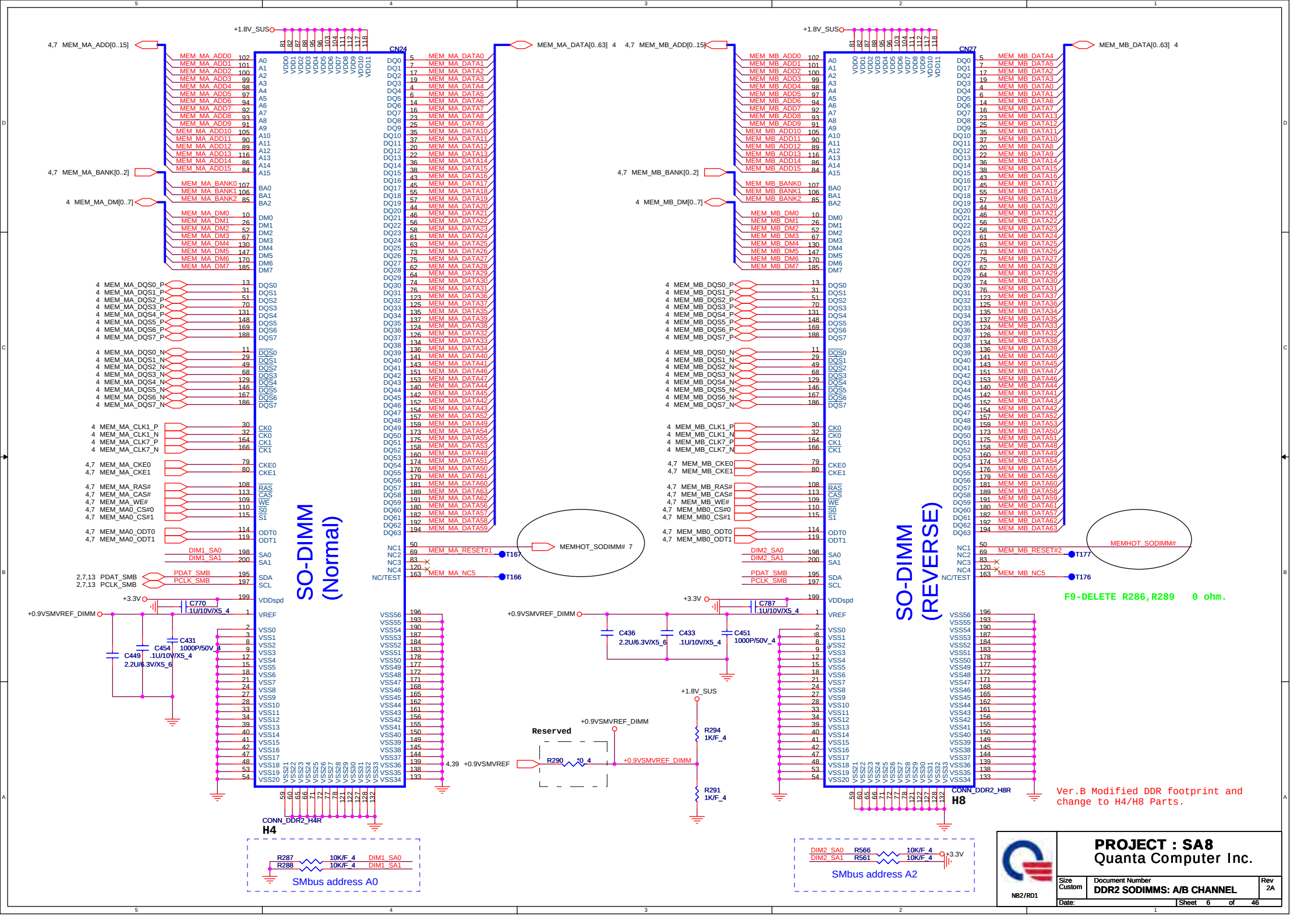
PROCESSOR POWER AND GROUND





EC C-11 2/20 Change CPU thermal IC to 781-1P8.

NB2/RD1	**PROJECT : SA8** Quanta Computer Inc.	
Size: Custom	Document Number: **S1G2 PWR & GND 3/3**	Rev: 2A
Date:	Sheet 5 of 46	


SO-DIMM (Normal)
CN24
H4
CONN_DDR2_H4R
SO-DIMM (REVERSE)
CN27
H8
CONN_DDR2_H8R
Reserved
R290 0_4
R294 1K/F_4
R291 1K/F_4
R287 10K/F_4 DIM1_SA0
R288 10K/F_4 DIM1_SA1
SMbus address A0
R566 10K/F_4 DIM2_SA0
R561 10K/F_4 DIM2_SA1
SMbus address A2
F9-DELETE R286,R289 0 ohm.
Ver.B Modified DDR footprint and change to H4/H8 Parts.
PROJECT : SA8
Quanta Computer Inc.
NB2/RD1
DDR2 SODIMMS: A/B CHANNEL
Size Custom
Rev 2A
Sheet 6 of 46

4,6 MEM_MA_ADD[0..15] → MEM_MA_ADD[0..15]
4,6 MEM_MA_BANK[0..2] → MEM_MA_BANK[0..2]

+0.9VSMVTT

4,6 MEM_MA_CKE0	MEM_MA_CKE0	RP9	4	3	47_4P2R	C461 .1U/10V/X5_4 +1.8V_SUS
	MEM_MA_BANK2		2	1		
	MEM_MA_ADD12	RP8	4	3	47_4P2R	C452 .1U/10V/X5_4
	MEM_MA_ADD9		2	1		
	MEM_MA_ADD8	RP5	2	1	47_4P2R	C447 .1U/10V/X5_4 +1.8V_SUS
	MEM_MA_ADD5		4	3		
	MEM_MA_ADD3	RP4	2	1	47_4P2R	C434 .1U/10V/X5_4
	MEM_MA_ADD1		4	3		
	MEM_MA_ADD10	RP7	4	3	47_4P2R	C446 .1U/10V/X5_4 +1.8V_SUS
	MEM_MA_BANK0		2	1		
4,6 MEM_MA_WE#	MEM_MA_WE#	RP6	4	3	47_4P2R	C453 .1U/10V/X5_4
4,6 MEM_MA_CAS#	MEM_MA_CAS#		2	1		
4,6 MEM_MA0_ODT1	MEM_MA0_ODT1	RP10	4	3	47_4P2R	C422 .1U/10V/X5_4 +1.8V_SUS
4,6 MEM_MA0_CS#1	MEM_MA0_CS#1		2	1		
	MEM_MA_ADD15	RP17	4	3	47_4P2R	C429 .1U/10V/X5_4
4,6 MEM_MA_CKE1	MEM_MA_CKE1		2	1		
	MEM_MA_ADD7	RP16	4	3	47_4P2R	C443 .1U/10V/X5_4 +1.8V_SUS
	MEM_MA_ADD14		2	1		
	MEM_MA_ADD6	RP15	4	3	47_4P2R	C428 .1U/10V/X5_4
	MEM_MA_ADD11		2	1		
	MEM_MA_ADD2	RP12	4	3	47_4P2R	C421 .1U/10V/X5_4 +1.8V_SUS
	MEM_MA_ADD4		2	1		
	MEM_MA_BANK1	RP11	2	1	47_4P2R	C448 .1U/10V/X5_4
	MEM_MA_ADD0		4	3		
4,6 MEM_MA0_CS#0	MEM_MA0_CS#0	RP14	4	3	47_4P2R	C460 .1U/10V/X5_4 +1.8V_SUS
4,6 MEM_MA_RAS#	MEM_MA_RAS#		2	1		
	MEM_MA_ADD13	RP13	4	3	47_4P2R	C426 .1U/10V/X5_4
4,6 MEM_MA0_ODT0	MEM_MA0_ODT0		2	1		C459 .1U/10V/X5_4 +1.8V_SUS
						C458 .1U/10V/X5_4

4,6 MEM_MB_ADD[0..15] → MEM_MB_ADD[0..15]
4,6 MEM_MB_BANK[0..2] → MEM_MB_BANK[0..2]

+0.9VSMVTT

4,6 MEM_MB_CKE0	MEM_MB_CKE0	RP23	4	3	47_4P2R	C445 .1U/10V/X5_4 +1.8V_SUS
	MEM_MB_BANK2		2	1		
	MEM_MB_ADD12	RP22	2	1	47_4P2R	C462 .1U/10V/X5_4
	MEM_MB_ADD9		4	3		
	MEM_MB_ADD8	RP21	4	3	47_4P2R	C442 .1U/10V/X5_4 +1.8V_SUS
	MEM_MB_ADD5		2	1		
	MEM_MB_ADD3	RP20	4	3	47_4P2R	C427 .1U/10V/X5_4
	MEM_MB_ADD1		2	1		
	MEM_MB_ADD10	RP19	4	3	47_4P2R	C441 .1U/10V/X5_4 +1.8V_SUS
	MEM_MB_BANK0		2	1		
4,6 MEM_MB_WE#	MEM_MB_WE#	RP18	4	3	47_4P2R	C463 .1U/10V/X5_4
4,6 MEM_MB_CAS#	MEM_MB_CAS#		2	1		
4,6 MEM_MB0_ODT1	MEM_MB0_ODT1	RP24	4	3	47_4P2R	C420 .1U/10V/X5_4 +1.8V_SUS
4,6 MEM_MB0_CS#1	MEM_MB0_CS#1		2	1		
4,6 MEM_MB_CKE1	MEM_MB_CKE1	RP33	2	1	47_4P2R	C457 .1U/10V/X5_4
	MEM_MB_ADD15		4	3		
	MEM_MB_ADD7	RP32	4	3	47_4P2R	C423 .1U/10V/X5_4 +1.8V_SUS
	MEM_MB_ADD14		2	1		
	MEM_MB_ADD6	RP31	4	3	47_4P2R	C438 .1U/10V/X5_4
	MEM_MB_ADD11		2	1		
	MEM_MB_ADD2	RP30	4	3	47_4P2R	C419 .1U/10V/X5_4 +1.8V_SUS
	MEM_MB_ADD4		2	1		
	MEM_MB_BANK1	RP29	4	3	47_4P2R	C450 .1U/10V/X5_4
	MEM_MB_ADD0		2	1		
4,6 MEM_MB0_CS#0	MEM_MB0_CS#0	RP28	4	3	47_4P2R	C440 .1U/10V/X5_4 +1.8V_SUS
4,6 MEM_MB_RAS#	MEM_MB_RAS#		2	1		
	MEM_MB0_ODT0	RP27	2	1	47_4P2R	C435 .1U/10V/X5_4
4,6 MEM_MB0_ODT0	MEM_MB_ADD13		4	3		C444 .1U/10V/X5_4 +1.8V_SUS
						C437 .1U/10V/X5_4

PLACE CLOSE TO PROCESSOR WITHIN 1.5 INCH

+1.8V_SUS

C416 .1U/10V/X5_4 C417 .1U/10V/X5_4 C418 .1U/10V/X5_4 C425 .1U/10V/X5_4 C406 .1U/10V/X5_4 C414 .1U/10V/X5_4

PLACE CLOSE TO SOCKET(FOR EMI/EMC)

PLACE CLOSE TO PROCESSOR WITHIN 1.5 INCH

+1.8V_SUS

C424 .1U/10V/X5_4 C409 .1U/10V/X5_4 C411 .1U/10V/X5_4 C415 .1U/10V/X5_4 C405 .1U/10V/X5_4 C791 .1U/10V/X5_4

PLACE CLOSE TO SOCKET(FOR EMI/EMC)

Close DDR2 socket

U37 *DS75U+T&R

+3.3V

A0 A1 A2 SDA SCL +VS O.S GND

C792 .1U/10V/X5_4

MEMHOT_SODIMM#

2,6,13 PDAT_SMB
2,6,13 PCLK_SMB

Address:92h

R519 *10K/F_4 → CPU_MEMHOT# 3,13

R520 *10K/F_4

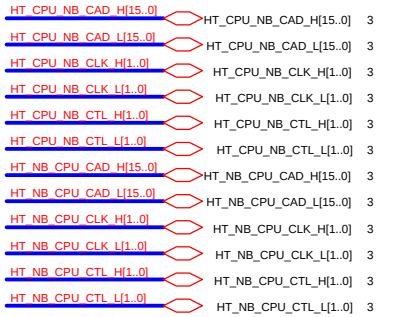
R521 *33_4

Q36 *2N7002E-G

Q37 *2N7002E-G

+3.3V R526 10K/F_4 MEMHOT_SODIMM# → MEMHOT_SODIMM# 6

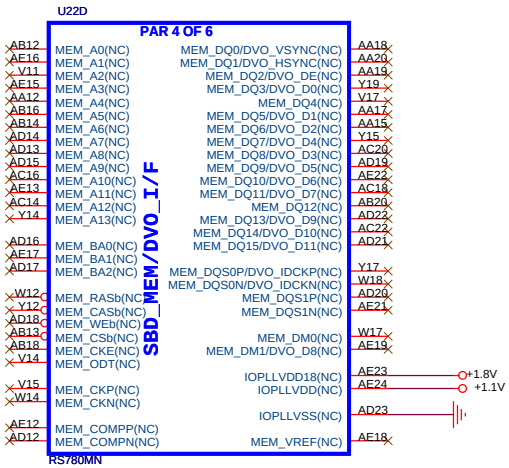
NB2/RD1	**PROJECT : SA8** Quanta Computer Inc.
Size: Custom	Document Number: DDR2 SODIMMS TERMINATIONS
Rev: 1A	
Date:	Sheet 7 of 46



signals	RS780	RX780
HT_TXCALP	R401 300 ohm 1%	R401 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	R400 300 ohm 1%	R400 1.21k ohm 1%
HT_RXCALN		

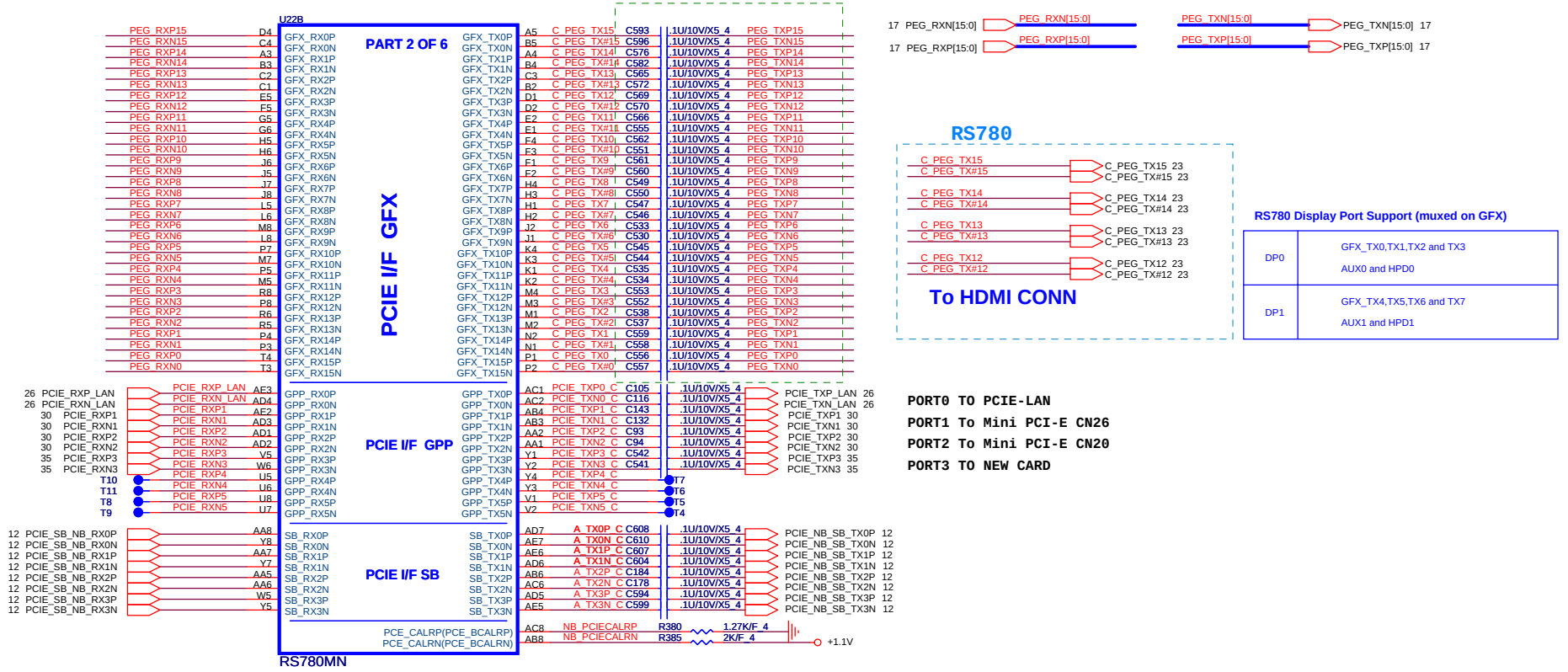
SIDE-PORT Reserved

This block is for UMA RS780 only , RX780 NC



Discrete M8x

Close to North Bridge



17 PEG_RXN[15:0] PEG_RXN[15:0] PEG_TXN[15:0] PEG_TXN[15:0] 17

17 PEG_RXP[15:0] PEG_RXP[15:0] PEG_TXP[15:0] PEG_TXP[15:0] 17

RS780 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

PORT0 TO PCIE-LAN
PORT1 To Mini PCI-E CN26
PORT2 To Mini PCI-E CN20
PORT3 TO NEW CARD

RX780/RS740/RS780 difference table (PCIE LINK)

	RX780/RS780
NB_PCIECALRP	1.27K (GND)
GPP4	GPP4
GPP5	GPP5

NB2/RD1

PROJECT : SA8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RS780MN-PCIE I/F 2/4	1A
Date:	Sheet 9 of 46	

RX780: Powered from the 1.8-V rail
and driven by SB600 LDT_RST#, or
SB700 LDT_RST# or A_RST#.
RS780: Powered from the 3.3-V rail
and driven by SB600 LDT_RST#, or
SB700 LDT_RST# or A_RST#.

12 NB_PLTRST# R129 0_4 NB_RST#_IN
RS780
North Bridge RESET
C200 *1000P/16V_4

ESD Reserved
NB_PWRGD_IN
C612 *1000P/16V_4

F10-DELETE R158,R160,
R165,R383,R382,R117,R121
,R374,R377,R601,R602,R104,R112 0 ohm

Ver.B Check PowerXpress switch
24,25 PX_LVDS_SWITCH R149 *0_4
25 INT_CRT_RED R152 150/F_4
25 INT_CRT_GRN R156 150/F_4
25 INT_CRT_BLU R159 150/F_4
25 INT_HSYNC
25 INT_VSYNC
25 INT_CRT_DDCDAT
25 INT_CRT_DDCCLK
R142 715/F_6 DAC_RSET_NB

Ver.B Update

	UMA	Hybrid
R383,R382,R117,R121	V	V
R158,R152,R160 R156,R165,R159	V	V

16,24 NB_PWRGD_IN
2 NBHT_REFCLKP
2 NBHT_REFCLKN
2 EXT_NB_OSC R126 0_4 R123 0_4 NB_REFCLK_P NB_REFCLK_N
+1.1V R134 4.7K_4 R124 4.7K_4
2 NBGFX_CLKP
2 NBGFX_CLKN
2 NBGPP_CLKP
2 NBGPP_CLKN
2 SBLINK_CLKP
2 SBLINK_CLKN
24 INT_LVDS_PNDAT
24 INT_LVDS_PNLCLK
T193
23 HDMI_DDC_CLK
23 HDMI_DDC_DATA
38 DYN_PWR_EN R379 0_4 STRP_DATA
T97 RS780_AUX_CAL

U22C
PART 3 OF 6

CRT/TVOUT
AVDD1(NC) F12
AVDD2(NC) F12
AVDD3(NC) F14
AVSSDI(NC) G15
AVDDQ(NC) H15
AVSSQ(NC) H14
C_Pr(DFT_GPIO5) E17
Y(DFT_GPIO2) E17
COMP_Pb(DFT_GPIO4) F15
RED(DFT_GPIO0) G18
REDn(NC) G17
GREEN(DFT_GPIO1) E18
GREENb(NC) F18
BLUE(DFT_GPIO3) E19
BLUEb(NC) F19
DAC_HSYNC(PWM_GPIO4) A11
DAC_VSYNC(PWM_GPIO6) B11
DAC_SDA(PCE_TCALRN) E8
DAC_SCL(PCE_RCALRN) F8
DAC_RSET(PWM_GPIO1) G14

PLL PWR
PLLVDD(NC) A12
PLLVDD18(NC) D14
PLLVSS(NC) B12
VDDA18HTPLL H17
VDDA18PCIEPLL1 D7
VDDA18PCIEPLL2 E7

PM
SYSRESETb D8
POWERGOOD A10
LDTSTOPb C10
ALLOW_LDTSTOP C12

CLOCKs
HT_REFCLKP C25
HT_REFCLKN C24
REFCLK_P/OSCIN(OSCIN) E11
REFCLK_N(PWM_GPIO3) F11
GFX_REFCLKP T2
GFX_REFCLKN T1
GPP_REFCLKP U1
GPP_REFCLKN U2
GPPSB_REFCLKP(SB_REFCLKP) V4
GPPSB_REFCLKN(SB_REFCLKN) V3

MIS.
I2C_DATA A9
I2C_CLK B9
DDC_DATA/AUX0N(NC) B8
DDC_CLK/AUX0P(NC) A8
AUX1P(NC) B7
AUX1N(NC) A7
STRP_DATA B10
RSVD G11
AUX_CAL(NC) C8

LVTM
TXOUT_L0P(NC) A22 LA_DATAP0
TXOUT_L0N(NC) B22 LA_DATAN0
TXOUT_L1P(NC) A21 LA_DATAP1
TXOUT_L1N(NC) B21 LA_DATAN1
TXOUT_L2P(NC) B20 LA_DATAP2
TXOUT_L2N(DBG_GPIO0) A20 LA_DATAN2
TXOUT_L3P(NC) A19 LA_DATAP3 T104
TXOUT_L3N(DBG_GPIO2) B19 LA_DATAN3 T103
TXOUT_U0P(NC) B18 LB_DATAP0
TXOUT_U0N(NC) A18 LB_DATAN0
TXOUT_U1P(PCIE_RESET_GPIO3) A17 LB_DATAP1
TXOUT_U1N(PCIE_RESET_GPIO2) B17 LB_DATAN1
TXOUT_U2P(NC) D20 LB_DATAP2
TXOUT_U2N(NC) D21 LB_DATAN2
TXOUT_U3P(PCIE_RESET_GPIO5) D18 LB_DATAP3 T105
TXOUT_U3N(NC) D19 LB_DATAN3 T106
TXCLK_LP(DBG_GPIO1) B16 LA_CLK
TXCLK_LN(DBG_GPIO3) A16 LA_CLK#
TXCLK_UP(PCIE_RESET_GPIO4) D16 LB_CLK
TXCLK_UN(PCIE_RESET_GPIO1) D17 LB_CLK#
VDDLTP18(NC) A13 +1.8V_VDDLTP18_NB
VSSLTP18(NC) B13
VDDLT18_1(NC) A15 +1.8V_VDDLT_18_NB
VDDLT18_2(NC) B15
VDDLT33_1(NC) A14
VDDLT33_2(NC) B14
VSSLT1(VSS) C14
VSSLT2(VSS) D15
VSSLT3(VSS) C16
VSSLT4(VSS) C18
VSSLT5(VSS) C20
VSSLT6(VSS) E20
VSSLT7(VSS) C22
LVDS_DIGON(PCE_TCALRP) E9 DISP_ON_NB
LVDS_BLON(PCE_RCALRP) E7 LVDS_BLON_NB
LVDS_ENA_BL(PWM_GPIO2) G12 R140 *0_4 DPST_PWM
TMDS_HPD(NC) D9 TMDS_HPD0
HPD(NC) D10 TMDS_HPD1 T100
TVCLKIN(PWM_GPIO5) D12 SUS_STAT#_NB R127 0_4 SUS_STAT# 13
THERMALDIODE_P AE8 R_NB_THRMDA T102
THERMALDIODE_N AD8 R_NB_THRMDC T101
TESTMODE D13 TEST_EN R394 1.82K/F_4

RS780MN

Ver.B Update

	UMA	Hybrid
R112/R104/R371	V	V

Ver.B Modified for PX_EN control

+3.3V R600 0_4 +3.3V
R580 4.7K_4 Q56 *2N7002E R581 *10K_4
HDTV_DET D31 CH501H-40PT
PX_LVDS_SWITCH 24,25
PX_EN 12
CH501H-40PT D32
R586 *10K_4

POWER XPRESS	PX_LVDS_SWITCH	PX_EN
VGA only	0	1
VGA+IGP	1	1

RS780
+3.3V R369 *4.7K_4 HDTV_DET
R378 4.7K_4 INT_CRT_DDCDAT
R376 4.7K_4 INT_CRT_DDCCLK

Ver.B Update

	UMA	Hybrid
R372/R368	V	X
R378/R376 R377/R374	V	V
D31/D32/R580 R581/Q56	X	V
R586	V	X

SA8 didn't support Hybrid for HDMI.

RX780 -->NC / RS780 --- ADD

+3.3V L30 BLM18PG221SN1D +3V_AVDD_NB
AVDD-DAC Analog not applicable to RX780
C228 2.2U/6.3V/X5_6

+1.1V BLM18PG221SN1D L62 +1.1V_PLLVDD
C615 2.2U/6.3V/X5_6
PLLVDD - Graphics PLL not applicable to RX780

+1.8V L29 BLM18PG221SN1D +1.8V_PLLVDD18
C626 10U/6.3V/X5_8
C227 2.2U/6.3V/X5_6
PLLVDD18 - Graphics PLL not applicable to RX780

+1.8V R135 0_6 +1.8V_AVDDDI_NB
C211 2.2U/6.3V/X5_6
AVDDI-DAC Digital not applicable to RX780

BLM18PG221SN1D L31 +1.8V_AVDDQ_NB
C226 2.2U/6.3V/X5_6
AVDDQ-DAC Bandgap Reference not applicable to RX780

+1.8V BLM18PG221SN1D L63 +1.8V_VDDLTP18_NB
C617 2.2U/6.3V/X5_6
VDDLTP18 - LVDS or DVI/HDMI PLL not applicable to RX780

BLM21PG221SN1D L66 +1.8V_VDDLT_18_NB
C624 4.7U/6.3V/X5_6
C619 .1U/10V/X5_4
VDDLT18 - LVDS or DVI/HDMI digital not applicable to RX780

Enables Debug Bus acess
through memory T/O pads and GPIO.
0 : Enable RS780 , Default
1 : Disable RS780
(RS780 use VSYNC#)
RS780
INT_VSYNC R386 3K_4 +3.3V

Indicates if memory Side port
is available or not
0: available RS780 , Default
1: Not available RS780
(RS780 use HSYNC#)
RS780
INT_HSYNC R387 3K_4 +3.3V
R384 *3K_4

For extrnal EEPROM Debug only
RS780/RX780
STRP_DATA R390 10K/F_4 +VDDG_NB
R381 *10K/F_4

+1.8V
VDDA18PCIEPLL -PCIE PLL
L24 BLM18PG221SN1D 20mils width +1.8V_VDDA18PCIEPLL
C179 2.2U/6.3V/X5_6
VDDA18HTPLL -HT LINK PLL
L33 BLM18PG221SN1D 20mils width +1.8V_VDDA18HTPLL
C240 2.2U/6.3V/X5_6

+1.8V +VDDG_NB
RS780
Q34 *BSS138_NL R395 *4.7K_4 RS780
3,12 CPU_LDT_STOP# NB_LDT_STOP#
R614 0_4
+VDDG_NB
RS780 Q33 *BSS138_NL RS780 R389 *4.7K_4
3 CPU_LDT_REQ# R396 0_4 NB_ALLOW_LDTSTOP
12 ALLOW_LDTSTOP R615 0_4

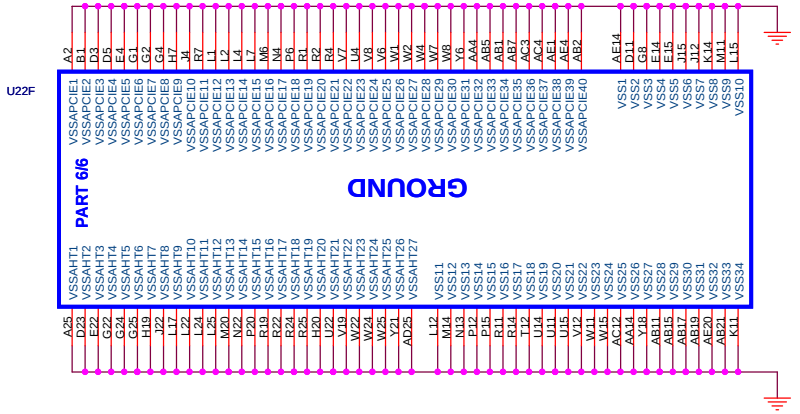
D11-Signal by pass directly for AMD request.

RS780 +3.3V R393 0_6 +VDDG_NB

NB2/RD1

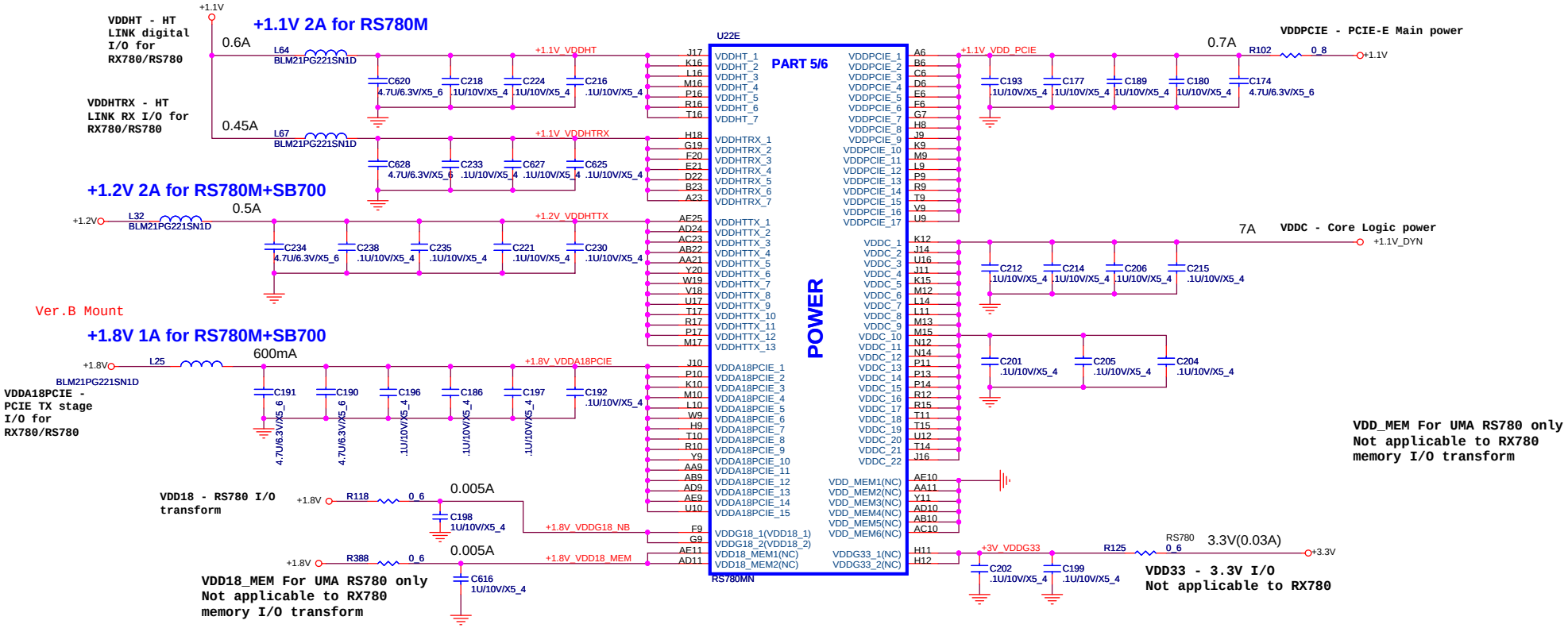
PROJECT : SA8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RS780MN-SYSTEM I/F 3/4	2A
Date:	Sheet 10 of 46	



RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RX780	RS780	PIN NAME	RX780	RS780
VDDHT	+1.1V	+1.1V	IOPLLVDD	NC	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	NC	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	NC	+1.8V
VDDG18	+1.8V	+1.8V	PLLVDD	NC	+1.1V
VDD18_MEM	NC	+1.8V	PLLVDD18	NC	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	NC	+1.8V/1.5V	VDDLTP18	NC	+1.8V
VDDG33	NC	+3.3V	VDDLT18	NC	+1.8V
IOPLLVDD18	NC	+1.8V	VDDLT33	NC	NC

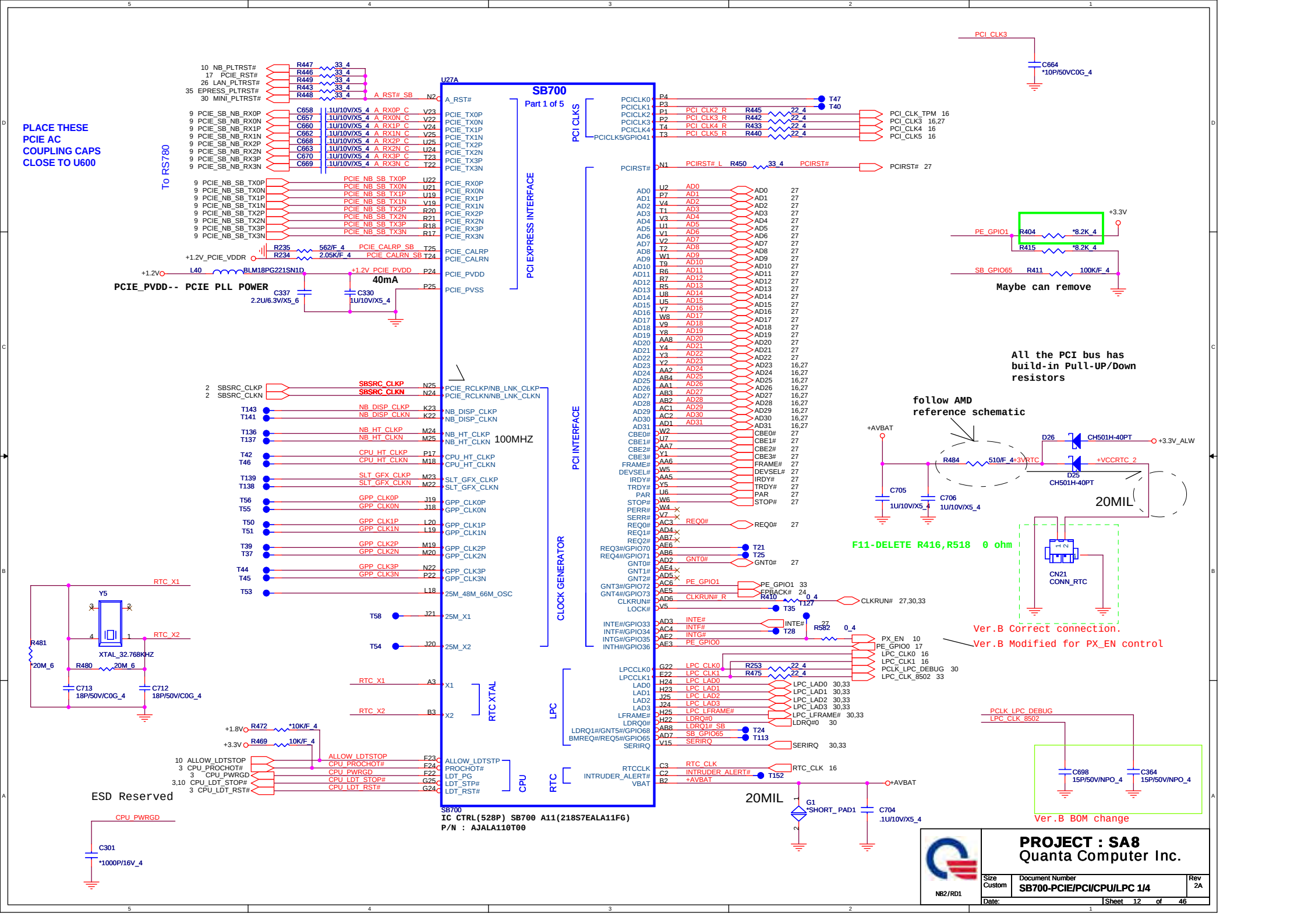


PROJECT : SA8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RS780MN-POWER 4/4	2A

NB2/RD1

Date: | Sheet 11 of 46


PLACE THESE
PCIE AC
COUPLING CAPS
CLOSE TO U600
To RS780
SB700
Part 1 of 5
U27A
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
CLOCK GENERATOR
LPC
RTC XTAL
CPU
RTC
PCIE_PVDD-- PCIE PLL POWER
40mA
100MHZ
20MIL
ESD Reserved
All the PCI bus has build-in Pull-UP/Down resistors
follow AMD reference schematic
F11-DELETE R416,R518 0 ohm
Maybe can remove
Ver.B Correct connection.
Ver.B Modified for PX_EN control
Ver.B BOM change
SB700
IC CTRL(528P) SB700 A11(218S7EALA11FG)
P/N : AJALA110T00
PROJECT : SA8
Quanta Computer Inc.
NB2/RD1
SB700-PCIE/PCI/CPU/LPC 1/4
Size Custom
Rev 2A
Date:
Sheet 12 of 46

NC only ,Can't be install

R460 *2.2K_4 SB_TEST0
R275 *2.2K_4 SB_TEST1
R246 *2.2K_4 SB_TEST2

F12-DELETE R255,R254,R242,R258,R474 0 ohm

R262 *10K/F_4 SWI#

SCL0/SDATA0 is 3V tolerance
AMD datasheet define it
Clock gen/Robson
/DDR2/DDR2
thermal/Accelerometer

R185 2.2K_4 PCLK_SMB
R186 2.2K_4 PDAT_SMB

SCL1/SDATA1 is 3V/S5 tolerance
AMD datasheet define it

R458 2.2K_4 SB_SMBCLK1
R457 2.2K_4 SB_SMBDATA1

SCL2/SDATA2 is 3V/S5 tolerance
AMD datasheet define it

R172 2.2K_4 SB_SCLK2
R173 2.2K_4 SB_SDATA2
R245 1K_4 DNBSWON#
PCI_PME#
R583 10K_4

Ver.B Correct GPIO6,39 netname
Ver.B correct R180 BOM error
Ver.B add R583

E3 Change R241 to ASM.
D1-R241 Delete for AMD request.

R406 10K_4 GPIO10
R241 4.7K_4 SUS_STAT#
R211 10K_4 GPIO0
R210 10K_4 GPIO39
R208 10K_4 GPIO40
R209 10K_4 GPIO4
R405 10K_4 GPIO6

G2 *SHORT_PAD1

To Azalia

ACZ_SDOUT R451 33_4 C671 *10P/50VC0G_4 ACZ_SDOUT_AUDIO 28
ACZ_SYNC R225 33_4 C302 *10P/50VC0G_4 ACZ_SYNC_AUDIO 28
ACZ_BCLK R454 33_4 C676 *10P/50VC0G_4 BIT_CLK_AUDIO 28
ACZ_RST# R233 33_4 ACZ_RST#_AUDIO 28
ACZ_SDIN0_R R238 0_4 ACZ_SDIN0 28

To Modem Board

ACZ_SDOUT R453 33_4 C674 *10P/50VC0G_4 ACZ_SDOUT_AUDIO_MDC 31
ACZ_SYNC R228 33_4 C317 *10P/50VC0G_4 ACZ_SYNC_AUDIO_MDC 31
ACZ_BCLK R455 33_4 L86 27NH_5%_200MA C681 10P/50V/C0G_4 BIT_CLK_AUDIO_MDC 31
ACZ_RST# R232 33_4 ACZ_RST#_AUDIO_MDC 31
ACZ_SDIN1_R R243 33_4 ACZ_SDIN1 31

Ver.B Add for EMI

D20 CH501H-40PT
3,7 CPU_MEMHOT# R491 *0_4 CPU_MEMHOT# IN
5 PM_THERM# R492 *10K/F_4 SMBALERT# 1
+3.3V

T153 T26 T60 PM_BATLOW# SES_INT GEVENT7#

R180 0_4 ACZ_SPKR_R

T49 T52

R466 22K_4 HDD_AUX_RST#

U27D

SB700

Part 4 of 5

27 PCI_PME#	PCI_PME#	E1	PCI_PME#/GEVENT4#
T149	RI#	E2	RI#/EXTEVNT0#
T57	SLP_S2	H7	SLP_S2/GPM9#
33 SUSB#	SUSB#	F5	SLP_S3#
33 SUSC#	SUSC#	G1	SLP_S5#
33 DNBSWON#	DNBSWON#	H2	PWR_BTN#
16 SB_PWRGD_IN	SB_PWRGD_IN	H1	PWR_GOOD
10 SUS_STAT#	SUS_STAT#	K3	SUS_STAT#
	SB_TEST2	H5	TEST2
	SB_TEST1	H4	TEST1
	SB_TEST0	H3	TEST0
33 GATEA20	GATEA20	Y15	GA20IN/GEVENT0#
33 RCIN#	RCIN#	W15	KBRST#/GEVENT1#
33 SCI#	SCI#	K4	LPC_PME#/GEVENT3#
33 KBSMI#	KBSMI#	K24	LPC_SMI#/EXTEVNT1#
T145		F1	S3_STATE/GEVENT5#
	SYS_RST#	J2	SYS_RESET#/GPM7#
26,30,35 PCIE_WAKE#	PCIE_WAKE#	H6	WAKE#/GEVENT8#
33 SWI#	SWI#	F2	BLINK/GPM6#
3 CPU_THERMTRIP#	CPU_THERMTRIP#	J6	SMBALERT#/THRMTRIP#/GEVENT2#
16 WD_PWRGD	WD_PWRGD	W14	NB_PWRGD
33 RSMRST#		D3	RSMRST#
	GPIO10	AE18	SATA_IS0#/GPIO10
	GPIO6	AD18	CLK_REQ3#/SATA_IS1#/GPIO6
	GPIO4	AA19	SMARTVOLT/SATA_IS2#/GPIO4
	GPIO0	W17	CLK_REQ0#/SATA_IS3#/GPIO0
	GPIO39	V17	CLK_REQ1#/SATA_IS4#/FANOUT3/GPIO39
	GPIO40	W20	CLK_REQ2#/SATA_IS5#/FANIN3/GPIO40
28 ACZ_SPKR	ACZ_SPKR_R	W21	SPKR/GPIO2
2,6,7 PCLK_SMB	PCLK_SMB	AA18	SCL0/GPOC0#
2,6,7 PDAT_SMB	PDAT_SMB	W18	SDA0/GPOC1#
30 SB_SMBCLK1	SB_SMBCLK1	K1	SCL1/GPOC2#
30 SB_SMBDATA1	SB_SMBDATA1	K2	SDA1/GPOC3#
		AA20	DDC1_SCL/GPIO9
		Y18	DDC1_SDA/GPIO8
T153		C1	LLB#/GPIO66
T26	SES_INT	Y19	SHUTDOWN#/GPIO5
T60	GEVENT7#	G5	DDR3_RST#/GEVENT7#
		B9	USB_OC6#/IR_TX1/GEVENT6#
		B8	USB_OC5#/IR_TX0/GPM5#
		A8	USB_OC4#/IR_RX0/GPM4#
		A9	USB_OC3#/IR_RX1/GPM3#
35 NEWCARD_DETECT	SB_JTAG_TDO	E5	USB_OC2#/GPM2#
31 USB_OC2#	SB_JTAG_TCK	F8	USB_OC1#/GPM1#
32 USB_OC1#	SB_JTAG_TDI	E4	USB_OC0#/GPM0#
32 USB_OC0#	SB_JTAG_RST#		
	ACZ_BCLK	M1	AZ_BITCLK
	ACZ_SDOUT	M2	AZ_SDOUT
	ACZ_SDIN0_R	J7	AZ_SDIN0/GPIO42
	ACZ_SDIN1_R	J8	AZ_SDIN1/GPIO43
		L8	AZ_SDIN2/GPIO44
		M3	AZ_SDIN3/GPIO46
	ACZ_SYNC	L6	AZ_SYNC
16 ACZ_RST#	ACZ_RST#	M4	AZ_RST#
		L5	AZ_DOCK_RST#/GPM8#
		H19	IMC_GPIO0
		H20	IMC_GPIO1
		H21	SPI_CS2#/IMC_GPIO2
		F25	IDE_RST#/F_RST#/IMC_GPO3
		D22	IMC_GPIO4
		E24	IMC_GPIO5
		E25	IMC_GPIO6
		D23	IMC_GPIO7

HD audio interface is 3.3V voltage

USB MISC: USBCLK/14M_25M_48M_OSC, USB_RCOMP
ACPI / WAKE UP EVENTS
USB 1.1
USB 2.0
GPIO
USB OC
HD AUDIO
INTEGRATED uC

C8	CLK_48M_USB	CLK_48M_USB 2	
G8	USB_RCOMP_SB	R247 11.8K/F_6	
USB_FSD13P	E6	USB_FSD13P	T78
USB_FSD13N	E7	USB_FSD13N	T155
USB_FSD12P	F7	USB_FSD12P	T68
USB_FSD12N	E8	USB_FSD12N	T73
USB_HSD11P	H11	USBP11+ 35	NEW CARD
USB_HSD11N	J10	USBP11- 35	
USB_HSD10P	E11	T74	
USB_HSD10N	F11	T69	
USB_HSD9P	A11	T189	
USB_HSD9N	B11	T188	
USB_HSD8P	C10	USBP8+ 32	USB Connector
USB_HSD8N	D10	USBP8- 32	
USB_HSD7P	G11	USBP7+ 24	Carama USB
USB_HSD7N	H12	USBP7- 24	
USB_HSD6P	E12	USBP6+ 31	FINGERPRINT
USB_HSD6N	E14	USBP6- 31	
USB_HSD5P	C12	USBP5+ 30	Min-Card
USB_HSD5N	D12	USBP5- 30	
USB_HSD4P	B12	USBP4+ 30	WLAN Min-Card
USB_HSD4N	A12	USBP4- 30	
USB_HSD3P	G12	T59	Ver.B Change Port9 to Port2
USB_HSD3N	G14	T64	
USB_HSD2P	H14	USBP9+ 32	USB Connector
USB_HSD2N	H15	USBP9- 32	
USB_HSD1P	A13	USBP1+ 31	BLUETOOTH
USB_HSD1N	B13	USBP1- 31	
USB_HSD0P	B14	USBP0+ 31	USB Connector
USB_HSD0N	A14	USBP0- 31	

IMC_GPIO8	A18		
IMC_GPIO9	B18		
IMC_PWM0/IMC_GPIO10	F21		
SCL2/IMC_GPIO11	D21	SB_SCLK2	SB_SCLK2 35
SDA2/IMC_GPIO12	F19	SB_SDATA2	SB_SDATA2 35
SCL3_LV/IMC_GPIO13	F20	SB_SCLK3	T67
SDA3_LV/IMC_GPIO14	F21	SB_SDATA3	T61
IMC_PWM1/IMC_GPIO15	E19		
IMC_PWM2/IMC_GPO16	D19	SB_GPIO16	SB_GPIO16 16
IMC_PWM3/IMC_GPO17	E18	SB_GPIO17	SB_GPIO17 16
IMC_GPIO18	G20		SPI/LPC define
IMC_GPIO19	G21		
IMC_GPIO20	D25		
IMC_GPIO21	D24		
IMC_GPIO22	C25		
IMC_GPIO23	C24		
IMC_GPIO24	B25		
IMC_GPIO25	C23		
IMC_GPIO26	B24		
IMC_GPIO27	B23		
IMC_GPIO28	A23		
IMC_GPIO29	C22		
IMC_GPIO30	A22		
IMC_GPIO31	B22		
IMC_GPIO32	B21		
IMC_GPIO33	A21		
IMC_GPIO34	D20		
IMC_GPIO35	C20		
IMC_GPIO36	A20		
IMC_GPIO37	B20		
IMC_GPIO38	B19		
IMC_GPIO39	A19		
IMC_GPIO40	D18		
IMC_GPIO41	C18		

SB JTAG

CN4: 1 SB_JTAG_TCK, 2 SB_JTAG_TDO, 3 SB_JTAG_TDI, 4 SB_TEST1, 5 SB_JTAG_RST#, 6 7 8
+3.3V_SUS
*S/W_JTAG_DEBUG

NB2/RD1

PROJECT : SA8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB700-ACPI/GPIO/USB 2/4	2A
Date:	Sheet 13 of 46	

SATA PORT 0,1,2,3 can support AHCI mode

SATA HDD

PLACE SATA AC COUPLING CAPS CLOSE TO SB600

SATA PORT 4,5 are only support IDE mode

SATA ODD

U27B

SB700
Part 2 of 5

SERIAL ATA

ATA 66/100/133

SPI ROM

HW MONITOR

SATA PWR

IF THERE IS NO IDE, TEST POINTS FOR DEBUG BUS IS MANDATORY

F13-DELETE R184,R422 0 ohm

	UMA	M82	M86
ID0	0	0	1
ID1	0	1	1
ID2	0	1	1
ID3	0	1	1
ID4	0	1	0

PLACE SATA_CAL RES VERY CLOSE TO BALL OF SB700

NOTE:
R361 IS 1K 1% FOR 25MHz XTAL, 4.99K 1% FOR 100MHz INTERNAL CLOCK

PLVDD_SATA-- SATA PLL POWER

XTLVDD_SATA-- SATA crystal power

AVDD--H/W monitor Analog power

Ver.B update XTAL. Cload.

Ver.B Correct Pin error

Place near ball

Project	SA8
Company	Quanta Computer Inc.
Size	Custom
Document Number	SB700-ACPI/GPIO/USB 2/4
Rev	2A
Date:	
Sheet	14 of 46

NB2/RD1

EC C-07 2/20 Del R465 and Add R237 for SB source.

PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.

VDD-- S/B CORE power

A1-2 chip using +1.2V

SB700
Part 3 of 5

POWER

VDDQ--3.3V I/O power

+3.3V_SB_R

0.8A

+3.3V

R409 0_8

C642 100U/6.3V/TAN_3528

C277 22U/6.3V/X5

C331 C275 C307 C291 C346 C281 1U/10V/X5_4

C285 1U/10V/X5_4

+3.3V_SB_R

C287 .1U/10V/X5_4

C290 .1U/10V/X5_4

U27C

VDDQ_1 VDDQ_2 VDDQ_3 VDDQ_4 VDDQ_5 VDDQ_6 VDDQ_7 VDDQ_8 VDDQ_9 VDDQ_10 VDDQ_11 VDDQ_12

L9 M9 T15 U9 U16 U17 V8 W7 Y6 AA4 AB5 AB21

PCI/GPIO I/O

+VDD33_18

0.45A

+3.3V R213 0_8

VDD33_18--3.3V IDE I/O power
1.8V flash memory I/O power

VDD33_18_1 VDD33_18_2 VDD33_18_3 VDD33_18_4

Y20 AA21 AA22 AE25

IDE/FLSH I/O

CKVDD_1.2V_1 CKVDD_1.2V_2 CKVDD_1.2V_3 CKVDD_1.2V_4

L21 L22 L24 L25

CLKGEN I/O

CORE S0

VDD_1 VDD_2 VDD_3 VDD_4 VDD_5 VDD_6 VDD_7 VDD_8 VDD_9

L15 M12 M14 N13 P12 P14 R11 R15 T16

+1.2V_VCC_SB_R

604mA

C333 C342 C350 C355 1U/10V/X5_4

C356 22U/6.3V/X5

C341 .1U/10V/X5_4

C332 .1U/10V/X5_4

R237 0_8 +1.2V

CKVDD_1.2V-- Internal
clock Generator I/O
power

+1.2V_CKVDD

286mA

C345 2.2U/6.3V/X5_6

C343 .1U/50V_6

C349 .1U/50V_6

L41 BLM18PG221SN1D +1.2V

C353 2.2U/6.3V/X5_6

+1.2V_PCIE_VDDR

844mA

PCIE_VDDR--PCIE I/O power

+1.2V L39 BLM18PG221SN1D

C308 22U/6.3V/X5

C312 C310 C311 C309 1U/10V/X5_4

PCIE_VDDR_1 PCIE_VDDR_2 PCIE_VDDR_3 PCIE_VDDR_4 PCIE_VDDR_5 PCIE_VDDR_6 PCIE_VDDR_7

P18 P19 P20 P21 R22 R24 R25

A-LINK I/O

S5_3.3V_1 S5_3.3V_2 S5_3.3V_3 S5_3.3V_4 S5_3.3V_5 S5_3.3V_6 S5_3.3V_7

3.3V_S5 I/O

S5_3.3--3.3v standby power

+3VALW_R

0.01A

A17 A24 B17 J4 J5 L1 L2

C702 C339 .1U/10V/X5_4

C714 10U/6.3V/X5_8

R498 0_6 +3.3V_S5

Ver.B

S5_1.2V--1.2V standby power

+1.2V_AVDD_SATA

0.2A

AVDD_SATA--SATA phy power

+1.2V L68 BLM18PG221SN1D

C633 10U/6.3V/X5_8

C640 C645 C641 C644 .1U/10V/X5_4

AVDD_SATA_1 AVDD_SATA_4 AVDD_SATA_2 AVDD_SATA_3 AVDD_SATA_5 AVDD_SATA_6 AVDD_SATA_7

AA14 AB18 AA15 AA17 AC18 AD17 AE17

SATA I/O

S5_1.2V_1 S5_1.2V_2

CORE S5

0.22A

+1.2VALW_R

G2 G4

R467 0_6 +1.2V_S5

C693 1U/10V/X5_4

C692 1U/10V/X5_4

USB_PHY_1.2V_1 USB_PHY_1.2V_2

0.2A

A10 B10 +1.2V_USB_PHY_R

For support USB wakeup-->3V_S5

+3V_AVDD_USB

AVDDTX--USB Phy
Analog I/O power

0.2A

+3.3V_S5 L74 BLM18PG221SN1D

C725 10U/6.3V/X5_8

C724 10U/6.3V/X5_8

C699 C709 .1U/10V/X5_4

C394 C375 C700 C395 C393 C708 C366 1U/10V/X5_4

AVDDTX_0 AVDDTX_1 AVDDTX_2 AVDDTX_3 AVDDTX_4 AVDDTX_5 AVDDRX_0 AVDDRX_1 AVDDRX_2 AVDDRX_3 AVDDRX_4 AVDDRX_5

A16 B16 C16 D16 D17 E17 F15 F17 F18 G15 G17 G18

USB I/O

PLL

V5_VREF AVDDCK_3.3V AVDDCK_1.2V AVDDC

AE7 J16 K17 E9

+5V_VREF +3V_AVDDCK +1.2V_AVDDCK +3V_AVDDC

V5_VREF--PCI 5V TOLERANCE

4mA

7mA

44mA

16mA

R412 1K/F_4 +5V

D19 CH501H-40PT +3.3V

C643 1U/10V/X5_4

+1.2V_S5

R485 0_6

+1.2V_USB_PHY_R

USB_PHY_1.2V--USB Phy
digital power

C701 C710 .1U/10V/X5_4

C711 10U/6.3V/X5_8

+3.3V_S5

+3V_AVDDC

AVDDC--USB Analog PLL power

L48 BLM18PG221SN1D

C383 .1U/10V/X5_4

C390 22U/6.3V/X5

+1.2V

+1.2V_AVDDCK

AVDDCK_1.2--USB Phy
digital power

L44 BLM18PG221SN1D

C385 2.2U/6.3V/X5_6

+3.3V

+3V_AVDDCK

AVDDCK_3.3--Analog
system PLL power

L45 BLM18PG221SN1D

C386 2.2U/6.3V/X5_6

U27E

SB700

AVSS_SATA_1 AVSS_SATA_2 AVSS_SATA_3 AVSS_SATA_4 AVSS_SATA_5 AVSS_SATA_6 AVSS_SATA_7 AVSS_SATA_8 AVSS_SATA_9 AVSS_SATA_10 AVSS_SATA_11 AVSS_SATA_12 AVSS_SATA_13 AVSS_SATA_14 AVSS_SATA_15 AVSS_SATA_16 AVSS_SATA_17 AVSS_SATA_18 AVSS_SATA_19 AVSS_SATA_20

T10 U10 U11 U12 V11 V14 W9 Y9 Y11 Y14 Y17 AA9 AB9 AB11 AB13 AB15 AB17 AC8 AD8 AE8

AVSS_USB_1 AVSS_USB_2 AVSS_USB_3 AVSS_USB_4 AVSS_USB_5 AVSS_USB_6 AVSS_USB_7 AVSS_USB_8 AVSS_USB_9 AVSS_USB_10 AVSS_USB_11 AVSS_USB_12 AVSS_USB_13 AVSS_USB_14 AVSS_USB_15 AVSS_USB_16 AVSS_USB_17 AVSS_USB_18 AVSS_USB_19 AVSS_USB_20 AVSS_USB_21 AVSS_USB_22 AVSS_USB_23 AVSS_USB_24

A15 B15 C14 D8 D9 D11 D13 D14 D15 E15 F12 F14 G9 H9 H17 J9 J11 J12 J14 J15 K10 K12 K14 K15

PCIE_CK_VSS_1 PCIE_CK_VSS_2 PCIE_CK_VSS_3 PCIE_CK_VSS_4 PCIE_CK_VSS_5 PCIE_CK_VSS_6 PCIE_CK_VSS_7 PCIE_CK_VSS_8

H18 J17 J22 K25 M16 M17 M21 P16

AVSSC F9

VSS_1 VSS_2 VSS_3 VSS_4 VSS_5 VSS_6 VSS_7 VSS_8 VSS_9 VSS_10 VSS_11 VSS_12 VSS_13 VSS_14 VSS_15 VSS_16 VSS_17 VSS_18 VSS_19 VSS_20 VSS_21 VSS_22 VSS_23 VSS_24 VSS_25 VSS_26 VSS_27 VSS_28 VSS_29 VSS_30 VSS_31 VSS_32 VSS_33 VSS_34 VSS_35 VSS_36 VSS_37 VSS_38 VSS_39 VSS_40 VSS_41 VSS_42 VSS_43 VSS_44 VSS_45 VSS_46 VSS_47 VSS_48 VSS_49 VSS_50

A2 A25 B1 D7 F20 G19 H8 K9 K11 K16 L4 L7 L10 L11 L12 L14 L16 M6 M10 M11 M13 M15 N4 N12 N14 P6 P9 P10 P11 P13 P15 R1 R2 R4 R9 R10 R12 R14 T11 T12 T14 U4 U14 V6 Y21 AB1 AB19 AB25 AE1 AE24

PCIE_CK_VSS_9 PCIE_CK_VSS_10 PCIE_CK_VSS_11 PCIE_CK_VSS_12 PCIE_CK_VSS_13 PCIE_CK_VSS_14 PCIE_CK_VSS_15 PCIE_CK_VSS_16 PCIE_CK_VSS_17 PCIE_CK_VSS_18 PCIE_CK_VSS_19 PCIE_CK_VSS_20 PCIE_CK_VSS_21

P23 R16 R19 T17 U18 U20 V18 V20 V21 W19 W22 W24 W25

AVSSCK L17

GROUND

Part 5 of 5

SB700

NB2/RD1

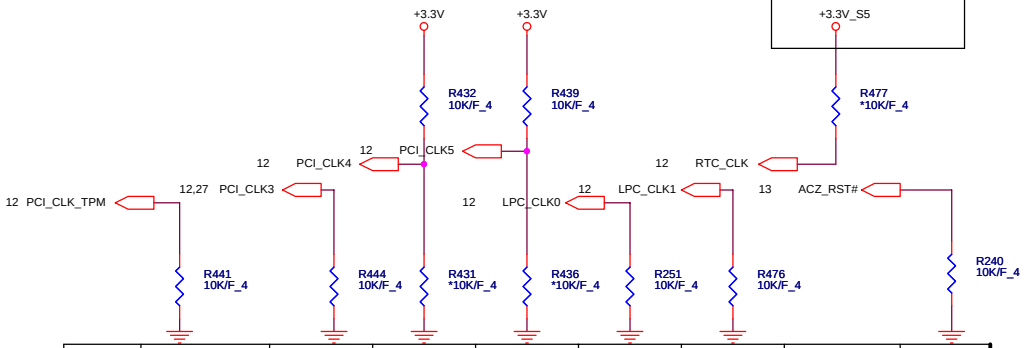
PROJECT : SA8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB700-PWR/DECOUPLING 4/4	2A
Date:	Sheet 15 of 46	

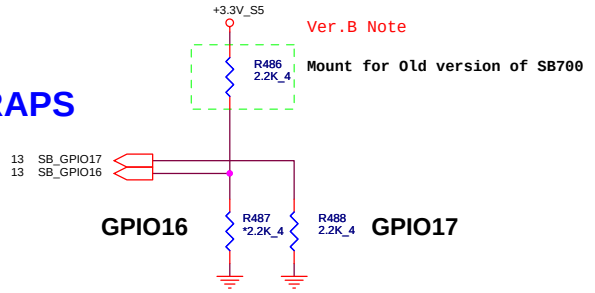
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

It must ready refore RSMRST#

REQUIRED STRAPS



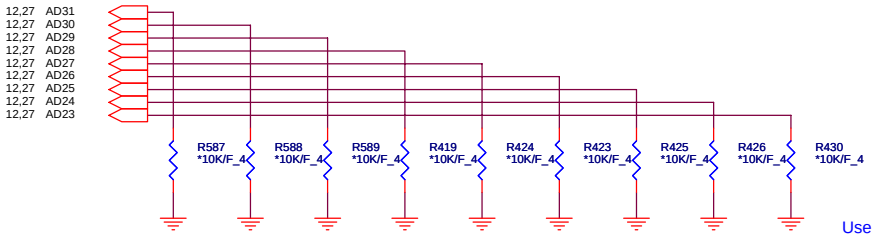
	PCI_CLK_TPM	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT



TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

DEBUG STRAPS

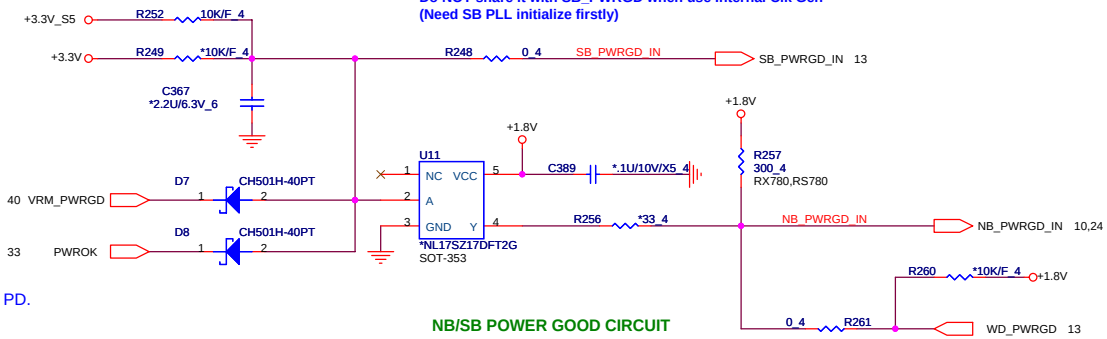
SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



Use 2.2K PD.

Ver.B Add AD[30..31] Reserved PD.

NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)



NB/SB POWER GOOD CIRCUIT

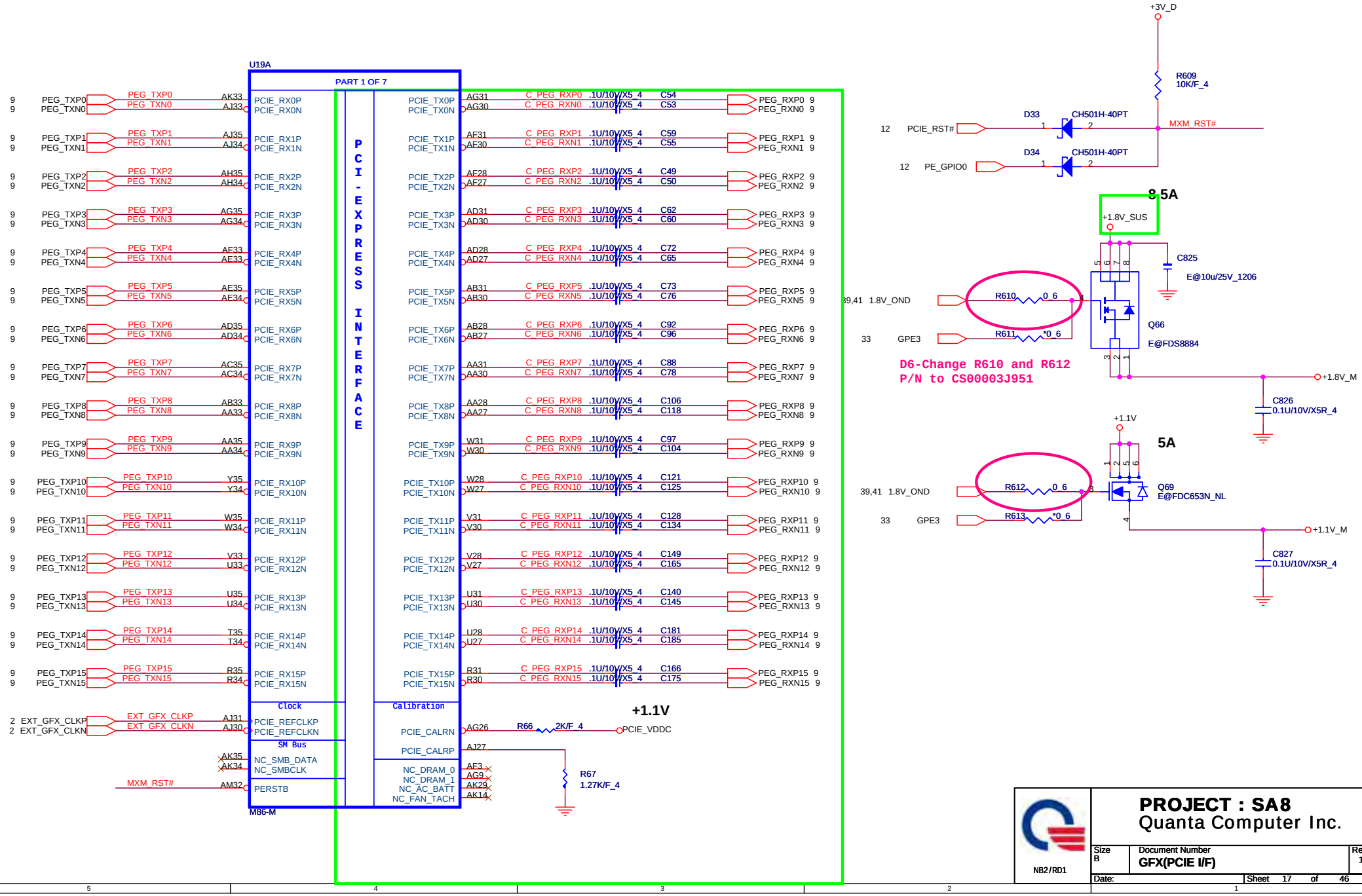
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

AL17SZ17000	IC(5P) NL17SZ17DFT2G(SOT-353)	SOT-353
ALUC1G17000	IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5)	SOT23-5

NB2/RD1

PROJECT : SA8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB700-STRAPS	2A
Date:	Sheet 16 of 46	


U19A
PART 1 OF 7
PCI-EXPRESS INTERFACE
M86-M
PEG_TXP0
PEG_TXN0
PEG_TXP1
PEG_TXN1
PEG_TXP2
PEG_TXN2
PEG_TXP3
PEG_TXN3
PEG_TXP4
PEG_TXN4
PEG_TXP5
PEG_TXN5
PEG_TXP6
PEG_TXN6
PEG_TXP7
PEG_TXN7
PEG_TXP8
PEG_TXN8
PEG_TXP9
PEG_TXN9
PEG_TXP10
PEG_TXN10
PEG_TXP11
PEG_TXN11
PEG_TXP12
PEG_TXN12
PEG_TXP13
PEG_TXN13
PEG_TXP14
PEG_TXN14
PEG_TXP15
PEG_TXN15
PCIE_RX0P
PCIE_RX0N
PCIE_RX1P
PCIE_RX1N
PCIE_RX2P
PCIE_RX2N
PCIE_RX3P
PCIE_RX3N
PCIE_RX4P
PCIE_RX4N
PCIE_RX5P
PCIE_RX5N
PCIE_RX6P
PCIE_RX6N
PCIE_RX7P
PCIE_RX7N
PCIE_RX8P
PCIE_RX8N
PCIE_RX9P
PCIE_RX9N
PCIE_RX10P
PCIE_RX10N
PCIE_RX11P
PCIE_RX11N
PCIE_RX12P
PCIE_RX12N
PCIE_RX13P
PCIE_RX13N
PCIE_RX14P
PCIE_RX14N
PCIE_RX15P
PCIE_RX15N
Clock
EXT_GFX_CLKP
EXT_GFX_CLKN
PCIE_REFCLKP
PCIE_REFCLKN
SM Bus
NC_SMB_DATA
NC_SMBCLK
MXM_RST#
PERSTB
PCIE_TX0P
PCIE_TX0N
PCIE_TX1P
PCIE_TX1N
PCIE_TX2P
PCIE_TX2N
PCIE_TX3P
PCIE_TX3N
PCIE_TX4P
PCIE_TX4N
PCIE_TX5P
PCIE_TX5N
PCIE_TX6P
PCIE_TX6N
PCIE_TX7P
PCIE_TX7N
PCIE_TX8P
PCIE_TX8N
PCIE_TX9P
PCIE_TX9N
PCIE_TX10P
PCIE_TX10N
PCIE_TX11P
PCIE_TX11N
PCIE_TX12P
PCIE_TX12N
PCIE_TX13P
PCIE_TX13N
PCIE_TX14P
PCIE_TX14N
PCIE_TX15P
PCIE_TX15N
Calibration
PCIE_CALRN
PCIE_CALRP
NC_DRAM_0
NC_DRAM_1
NC_AC_BATT
NC_FAN_TACH
C_PEG_RXP0 .1U/10V/X5_4 C54
C_PEG_RXN0 .1U/10V/X5_4 C53
C_PEG_RXP1 .1U/10V/X5_4 C59
C_PEG_RXN1 .1U/10V/X5_4 C55
C_PEG_RXP2 .1U/10V/X5_4 C49
C_PEG_RXN2 .1U/10V/X5_4 C50
C_PEG_RXP3 .1U/10V/X5_4 C62
C_PEG_RXN3 .1U/10V/X5_4 C60
C_PEG_RXP4 .1U/10V/X5_4 C72
C_PEG_RXN4 .1U/10V/X5_4 C65
C_PEG_RXP5 .1U/10V/X5_4 C73
C_PEG_RXN5 .1U/10V/X5_4 C76
C_PEG_RXP6 .1U/10V/X5_4 C92
C_PEG_RXN6 .1U/10V/X5_4 C96
C_PEG_RXP7 .1U/10V/X5_4 C88
C_PEG_RXN7 .1U/10V/X5_4 C78
C_PEG_RXP8 .1U/10V/X5_4 C106
C_PEG_RXN8 .1U/10V/X5_4 C118
C_PEG_RXP9 .1U/10V/X5_4 C97
C_PEG_RXN9 .1U/10V/X5_4 C104
C_PEG_RXP10 .1U/10V/X5_4 C121
C_PEG_RXN10 .1U/10V/X5_4 C125
C_PEG_RXP11 .1U/10V/X5_4 C128
C_PEG_RXN11 .1U/10V/X5_4 C134
C_PEG_RXP12 .1U/10V/X5_4 C149
C_PEG_RXN12 .1U/10V/X5_4 C165
C_PEG_RXP13 .1U/10V/X5_4 C140
C_PEG_RXN13 .1U/10V/X5_4 C145
C_PEG_RXP14 .1U/10V/X5_4 C181
C_PEG_RXN14 .1U/10V/X5_4 C185
C_PEG_RXP15 .1U/10V/X5_4 C166
C_PEG_RXN15 .1U/10V/X5_4 C175
PEG_RXP0 PEG_RXN0
PEG_RXP1 PEG_RXN1
PEG_RXP2 PEG_RXN2
PEG_RXP3 PEG_RXN3
PEG_RXP4 PEG_RXN4
PEG_RXP5 PEG_RXN5
PEG_RXP6 PEG_RXN6
PEG_RXP7 PEG_RXN7
PEG_RXP8 PEG_RXN8
PEG_RXP9 PEG_RXN9
PEG_RXP10 PEG_RXN10
PEG_RXP11 PEG_RXN11
PEG_RXP12 PEG_RXN12
PEG_RXP13 PEG_RXN13
PEG_RXP14 PEG_RXN14
PEG_RXP15 PEG_RXN15
+1.1V
R66 2K/F_4
PCIE_VDDC
R67 1.27K/F_4
+3V_D
R609 10K/F_4
D33 CH501H-40PT
D34 CH501H-40PT
PCIE_RST#
PE_GPIO0
MXM_RST#
3.5A
+1.8V_SUS
C825 E@10u/25V_1206
R610 0_6
R611 *0_6
Q66 E@FDS8884
1.8V_OND
GPE3
D6-Change R610 and R612
P/N to CS00003J951
+1.8V_M
C826 0.1U/10V/X5R_4
+1.1V
5A
R612 0_6
R613 *0_6
Q69 E@FDC653N_NL
+1.1V_M
C827 0.1U/10V/X5R_4
NB2/RD1
PROJECT : SA8
Quanta Computer Inc.
Size B
Document Number
GFX(PCIE I/F)
Rev 1A
Date:
Sheet 17 of 46

F14-DELETE R41 0 ohm

M86-M=> LVDDR+LVDDC(400mA)

+1.8V(400mA)

FOR M8x
INSTALL LVDDR AND LVDDC TO +1.8V(400mA)
WITH THE ONE LVDDC FILTER
DO NOT INSTALL LVDDR FILTER
INSTALL STRAP RESISTOR

+1.8V(20mA)

MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Hynix	16*32 700	HY5RS123235BFP-14
0001	Qimonda	16*32 700	HYB18H512321BF-14
0010	Samsung	16*32 700	K4J52324QE-BC14
0011	Hynix	32X32	NA
0100	Qimonda	32X32 700	HYB18H1G321AF-14
0101	Samsung	32X32	NA
0110	Hynix	16*32 900	HY5RS123235BFP-11
0111			Reserved
1000			Reserved
1001			Reserved
1010			Reserved
1011			Reserved
1100			Reserved
1101			Reserved
1110			Reserved
1111			Reserved

D13

+1.8V(120mA)

+1.8V(40mA)

+VGA_CORE(414mA)

+1.1V(300mA)

Ver.B update XTAL.

Ver.B Correct HDMI P/N connection.

120 ohm/300mA

+1.8V(40mA)

+1.1V(200mA)

+1.1V(200mA)

F15-DELETE R40,R42,R43 0 ohm

+1.8V(121mA)

+1.8V(85mA)

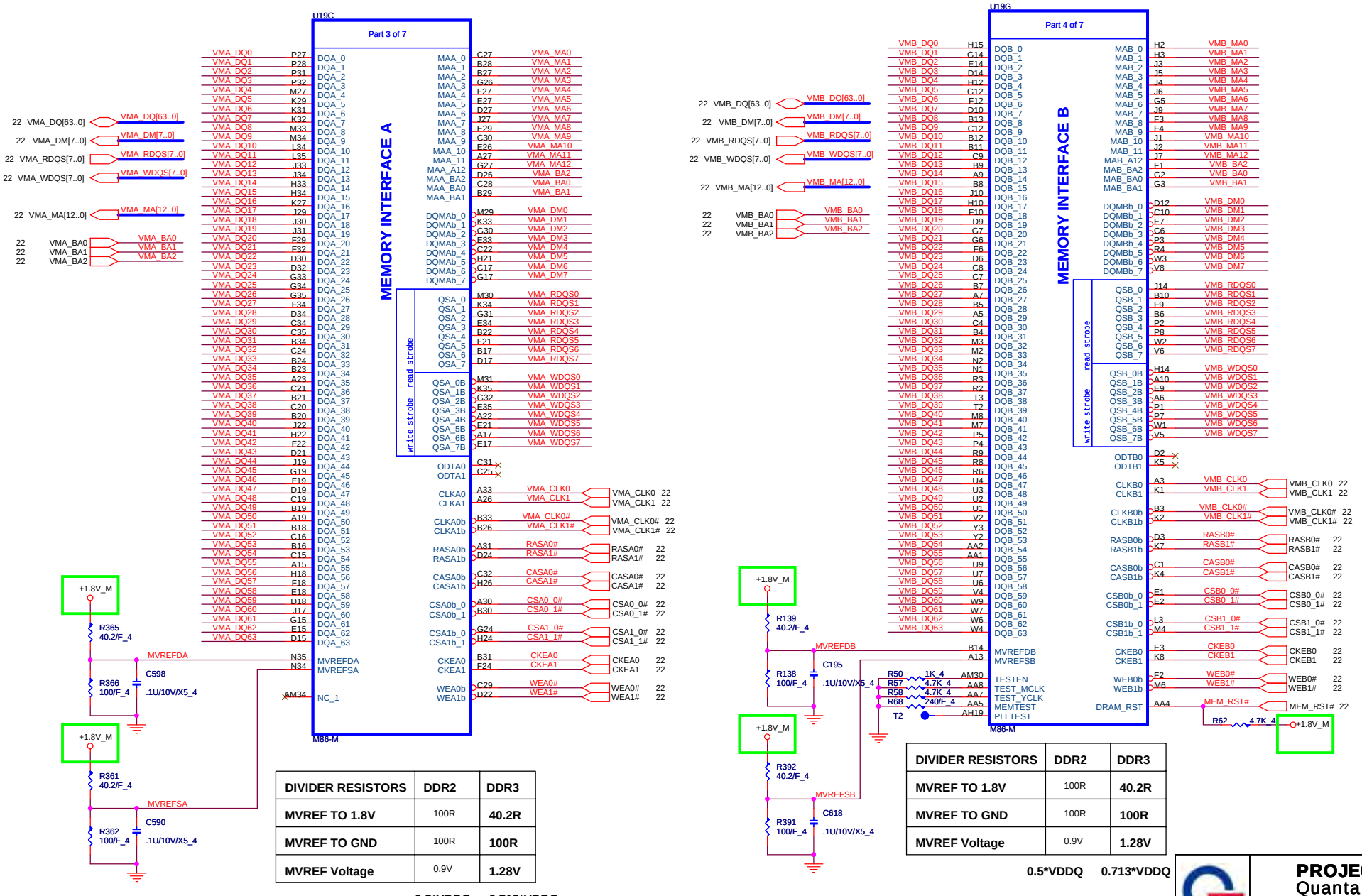
+1.8V(48mA)

+3.3V(135mA)

DDC3,DDC4 ARE 5V TOLERANT ON M8x

PROJECT : SA8
Quanta Computer Inc.

Size	Document Number	Rev
C	GFX(LVDS, DVI, CRT, TV)	2A
NB2/RD1	Date:	Sheet 18 of 46



DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R
MVREF Voltage	0.9V	1.28V

0.5*VDDQ 0.713*VDDQ

DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R
MVREF Voltage	0.9V	1.28V

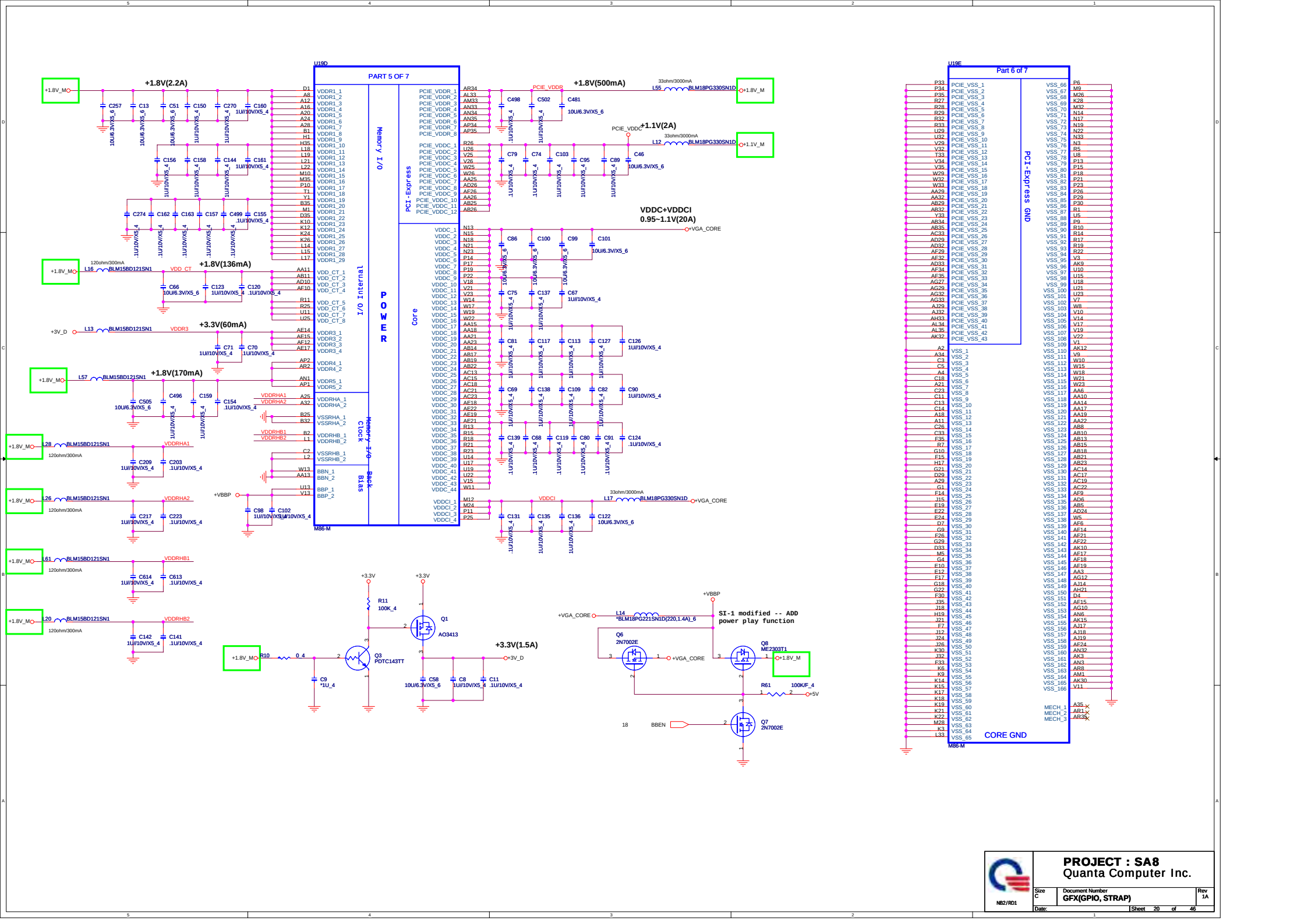
0.5*VDDQ 0.713*VDDQ

PROJECT : SA8
Quanta Computer Inc.

NB2/RD1

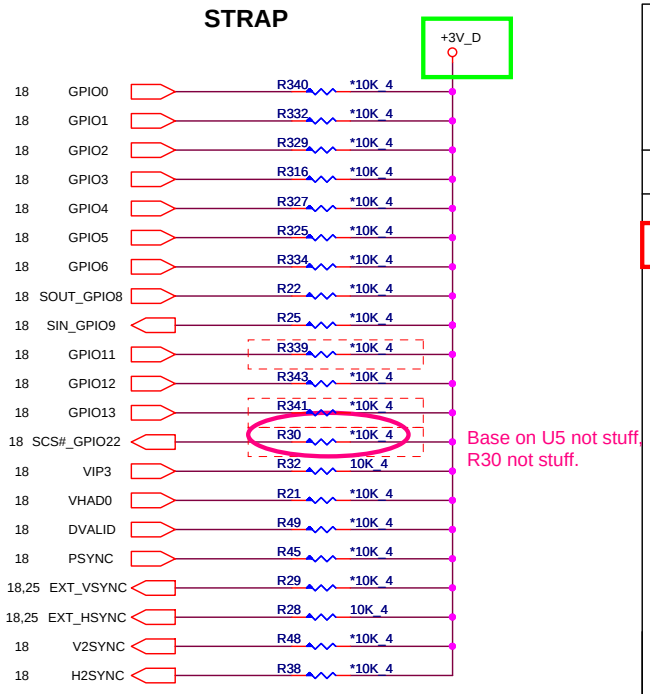
Size	Document Number	Rev
Custom	GFX(MEM I/F 1/2)	1A

Date: Sheet 19 of 46



PROJECT : SA8			
Quanta Computer Inc.			
NB2/RD1	Size C	Document Number GFX(GPIO, STRAP)	Rev 1A
	Date:	Sheet 20 of 46	

STRAP



Base on U5 not stuff, R30 not stuff.

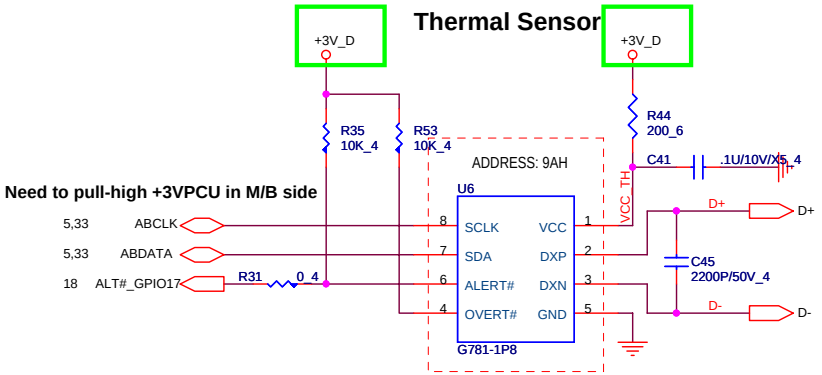
EC C-12 2/20 For M86 HDMI audio issue.

CONFIGURATION STRAPS

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE
RSVD = ATI RESERVED (DO NOT INSTALL)

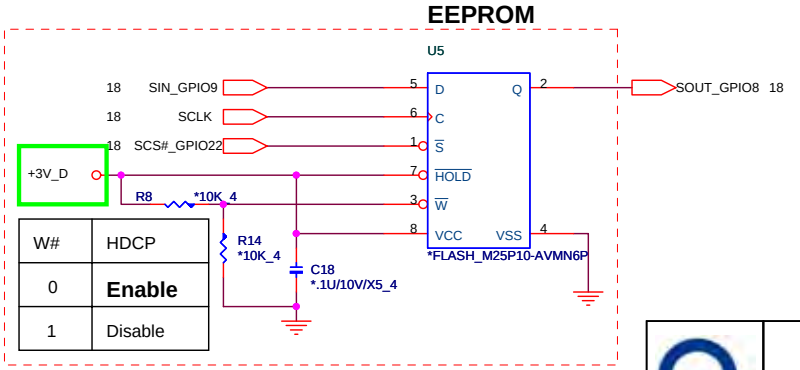
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	M8x	M7x
BIF_MSI_DIS	VIP1	MESSAGE SIGNAL INTERRUPT ENABLED	NA	0
BIF_AUDIO_EN	VIP3	ENABLE HD AUDIO (M8x-M)	NA	X
BIF_64BAR_EN_A	VIP5	64 BIT BARS DISABLED	NA	0
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X	X
BIF_DEBUG_ACCESS	GPIO4	DEBUG SIGNALS MUXED OUT	0	0
BIF_AUDIO_EN	GPIO8	ENABLE HD AUDIO (M82-S)	X	RSVD
BIF_GEN2_EN_A	GPIO5	Allows either PCIe 2.5GT/s or 5.0GT/s operation	X	0
BIOS_ROM_EN	GPIO_22_ROMCSB	DISABLE EXTERNAL BIOS ROM	NA	X
ROMIDCFG(3:0)	GPIO[13:11,9]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XX X X	X X X X
VIP_DEVICE_STRAP_ENA	VSYNC	IGNORE VIP DEVICE STRAPS	O	O
BIF_VGA DIS	PSYNC	VGA ENABLED	0	O
BIF_HDMI_EN	HSYNC	HDMI ENABLE (SEE NOTE 2)	X	X
DEBUG_ I2C_ENABLE	GPIO6	Internal use only	0	0
MEM_TYPE	ANY UNUSED GPIO OR DVP THAT ARE NOT CONFIG STRAPS FOR EXAMPLE DVPDATA20:23 IN THIS DESIGN	MEMORY TYPE,MAKE AND SIZE INFO	X X X X	X X X X

Thermal Sensor



EC C-10 2/20 Change VGA thermal IC to 781-1P8.

EEPROM

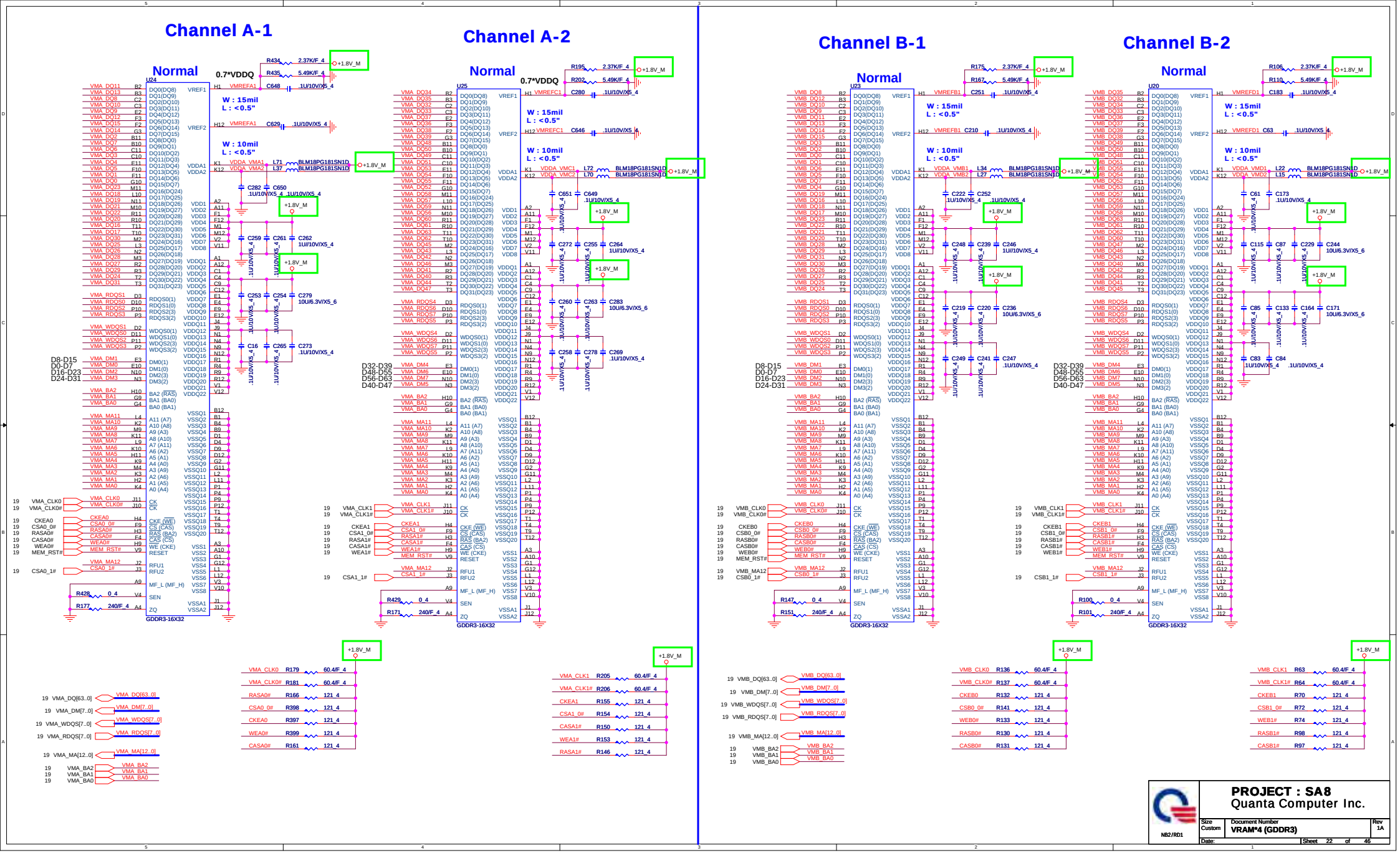


W#	HDCP
0	**Enable**
1	Disable

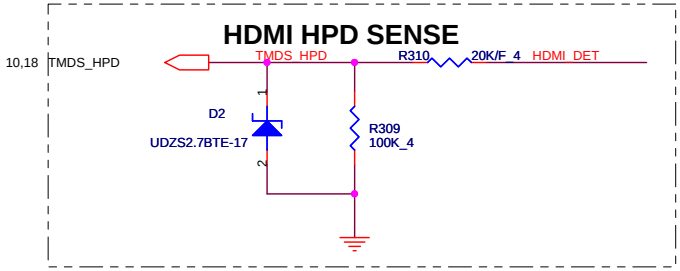
NB2/RD1

PROJECT : SA8
Quanta Computer Inc.

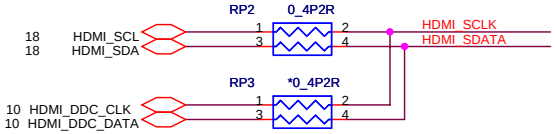
Size	Document Number	Rev
B	STRAP & Others	1A
Date:	Sheet 21 of 46	


Channel A-1
Channel A-2
Channel B-1
Channel B-2
Normal
0.7*VDDQ
W : 15mil
L : <0.5"
W : 10mil
L : <0.5"
GDDR3-16X32
D8-D15
D0-D7
D16-D23
D24-D31
D32-D39
D48-D55
D56-D63
D40-D47
PROJECT : SA8
Quanta Computer Inc.
N82/RD1
Size
Custom
Document Number
VRAM*4 (GDDR3)
Rev
1A
Date:
Sheet 22 of 46

HDMI HPD SENSE



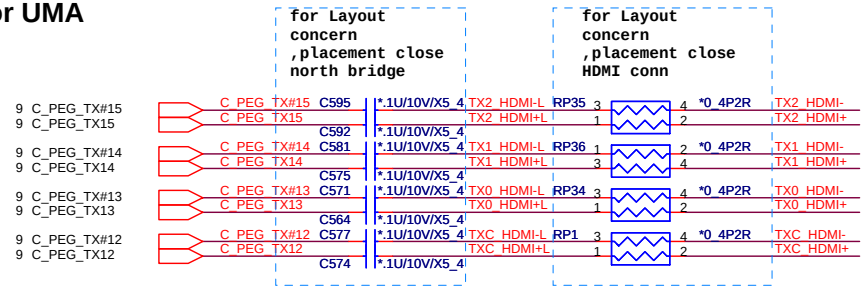
UMA AND DISCRETE SELECT



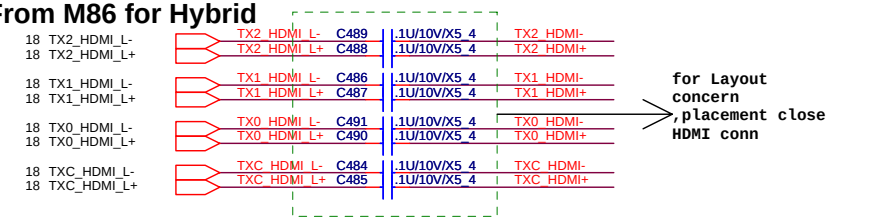
SA8 not support HDMI hybrid

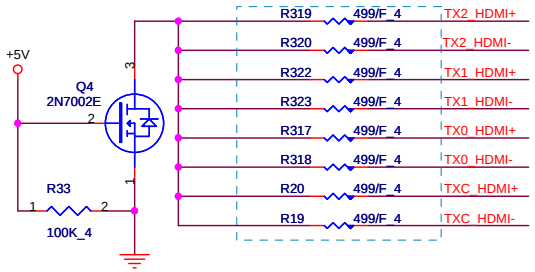
	UMA	Hybrid
PR2	X	V
PR3	V	X

From RS780M For UMA



From M86 for Hybrid



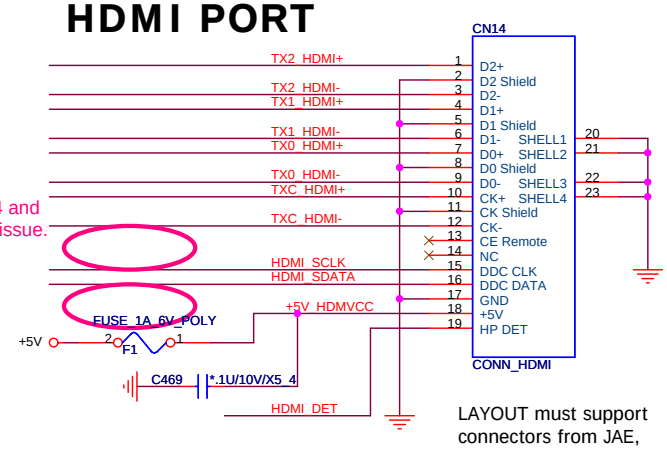


RS780M put 750 ohm CS17502FB19

DIS M86M put 499 ohm CS14992FB24

Close to HDMI Connector

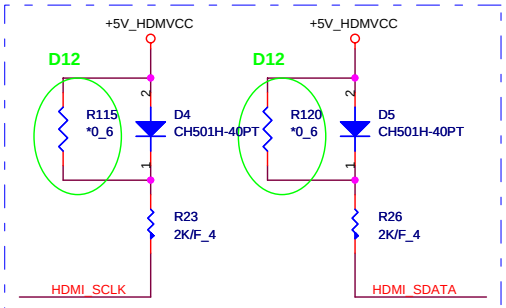
HDMI PORT



D8-Delete C4 and C5 for HDMI issue.

LAYOUT must support connectors from JAE, Molex, and Acon

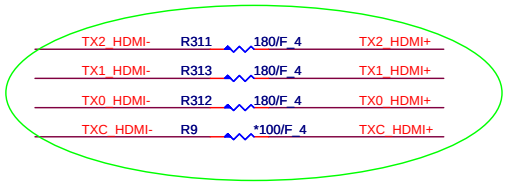
F16-DELETE L2,L3 0 ohm



Close to HDMI Connector

DDC4 is 5V tolerance , the MOSFET level shifter no need

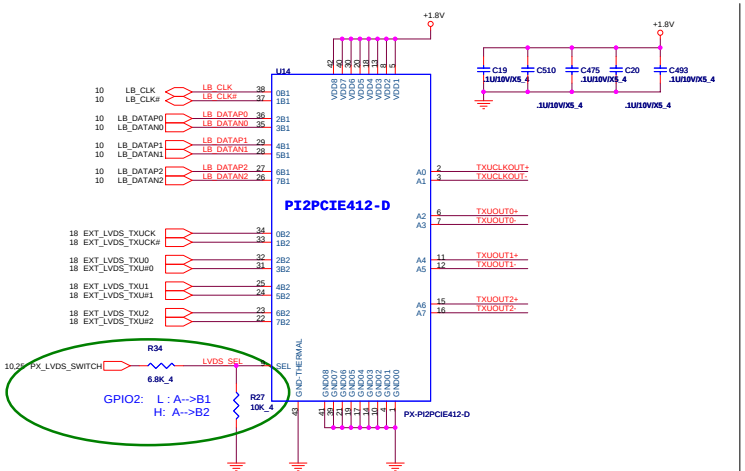
F29



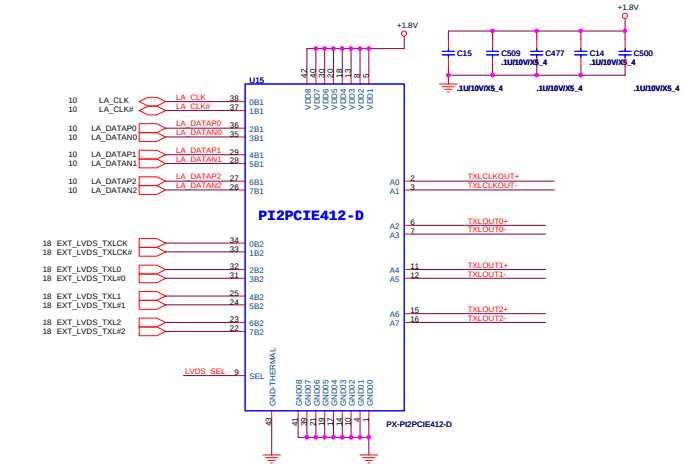
NB2/RD1

PROJECT : SA8
Quanta Computer Inc.

Size	Document Number	Rev
B	HDMI CONN	2A
Date:	Sheet 23 of 46	



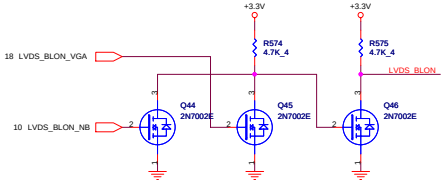
Rev.C : Modify resistor divider R34/R27 value from 0/100kohm to 6.8k/10k to allow LVDS_SEL is 1.8V swing



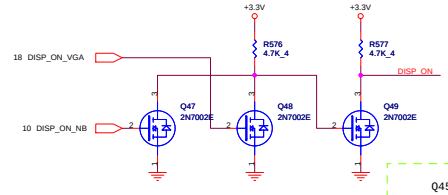
between NB & VGA

UMA NC

Ver.B Update



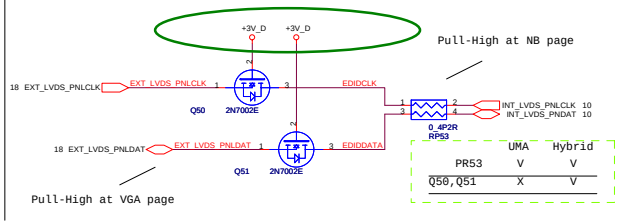
Inverter Wired OR



LCDVcc Wired OR

	UMA	Hybrid
Q45,Q48	X	V

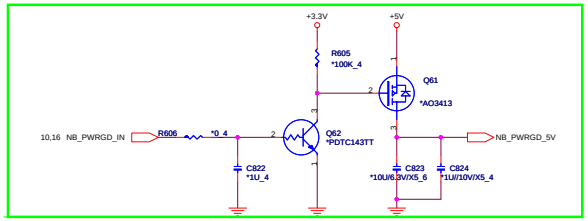
Rev.C: Gate terminal on both Q50 and Q51 must be changed from +3.3V to +3V_D

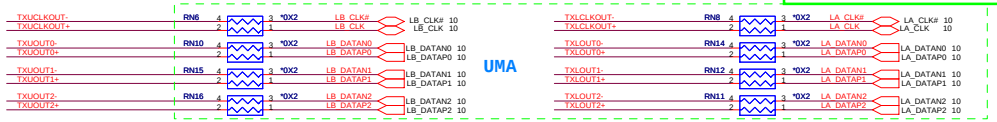


	UMA	Hybrid
PR53	V	V
Q50,Q51	X	V

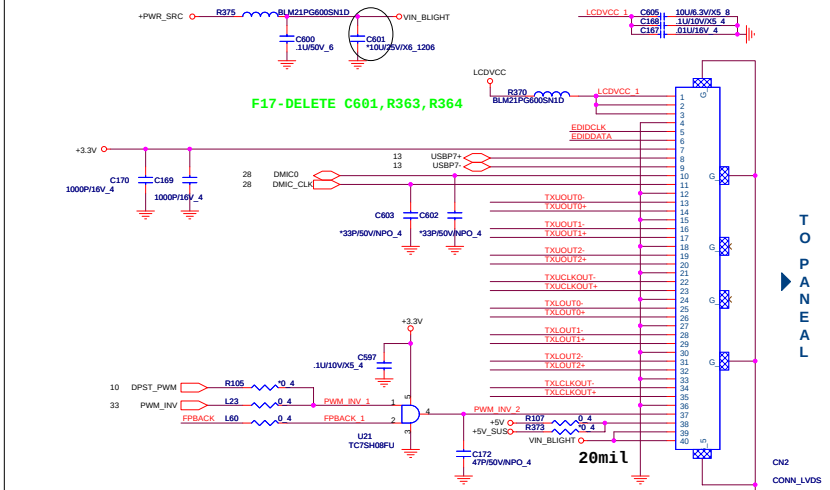
between NB & VGA

UMA only

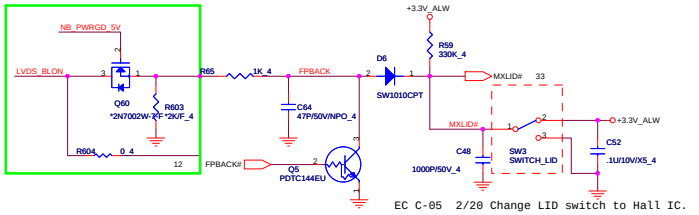




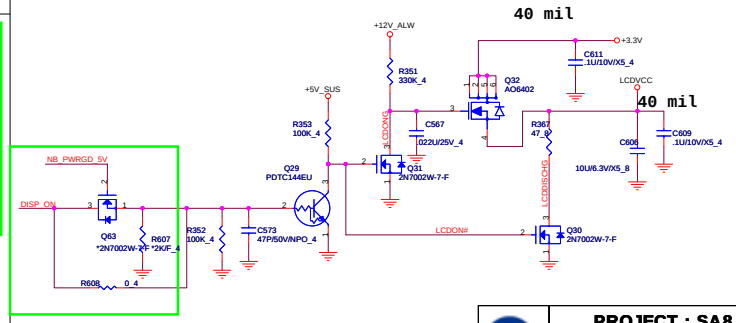
Ver.B delete discrete only selection.



LCD CONNECTOR(Include WEB CAM function)

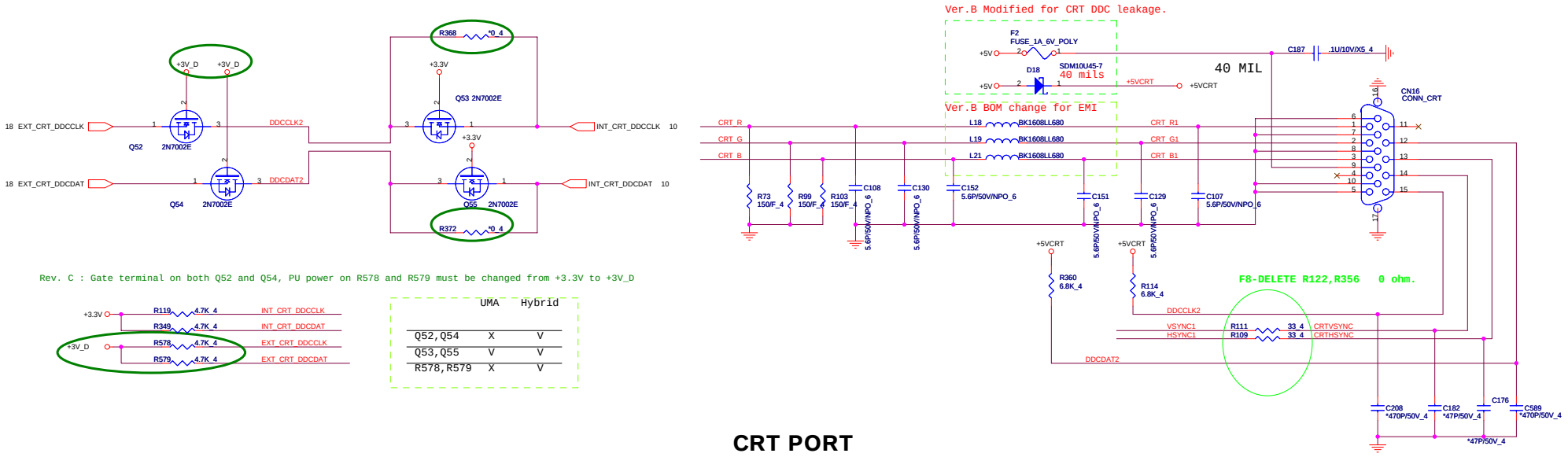


BACKLIGHT CONTROL

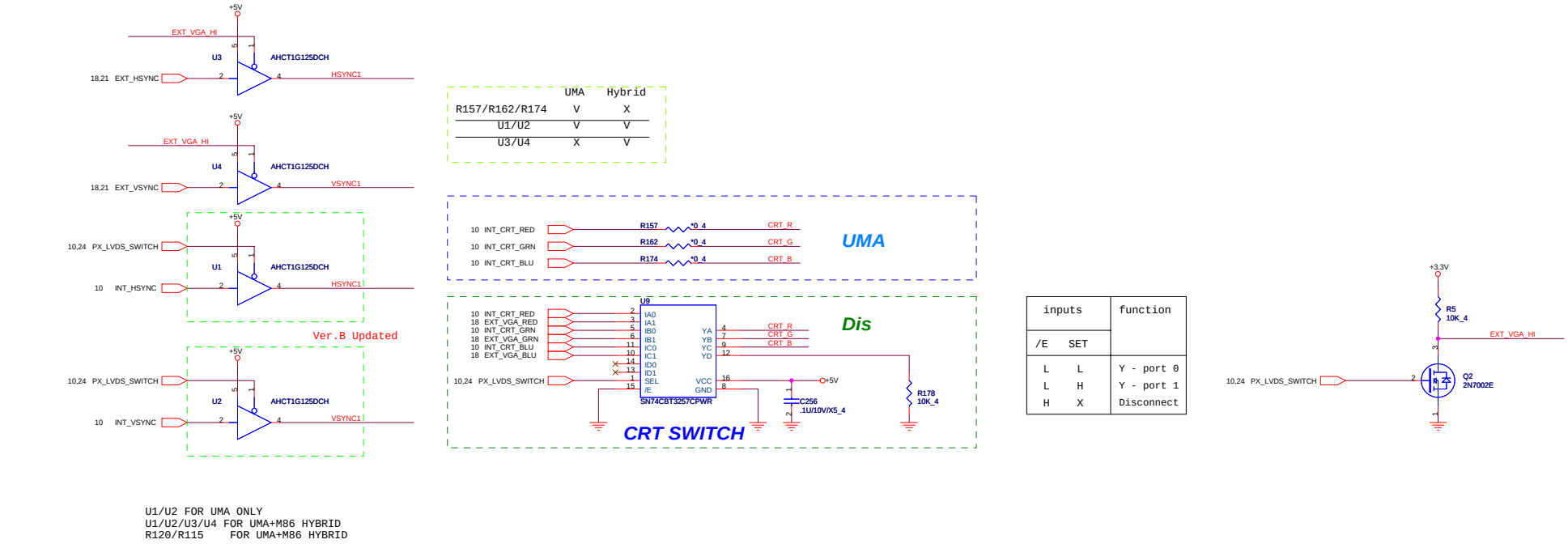


PANEL VCC CONTROL

PROJECT : SA8	
Quanta Computer Inc.	
Size: Custom	Document Number: LCD CONN & MUX
Rev: 2A	
Date:	Sheet 24 of 46
NB2/RD1	



CRT PORT



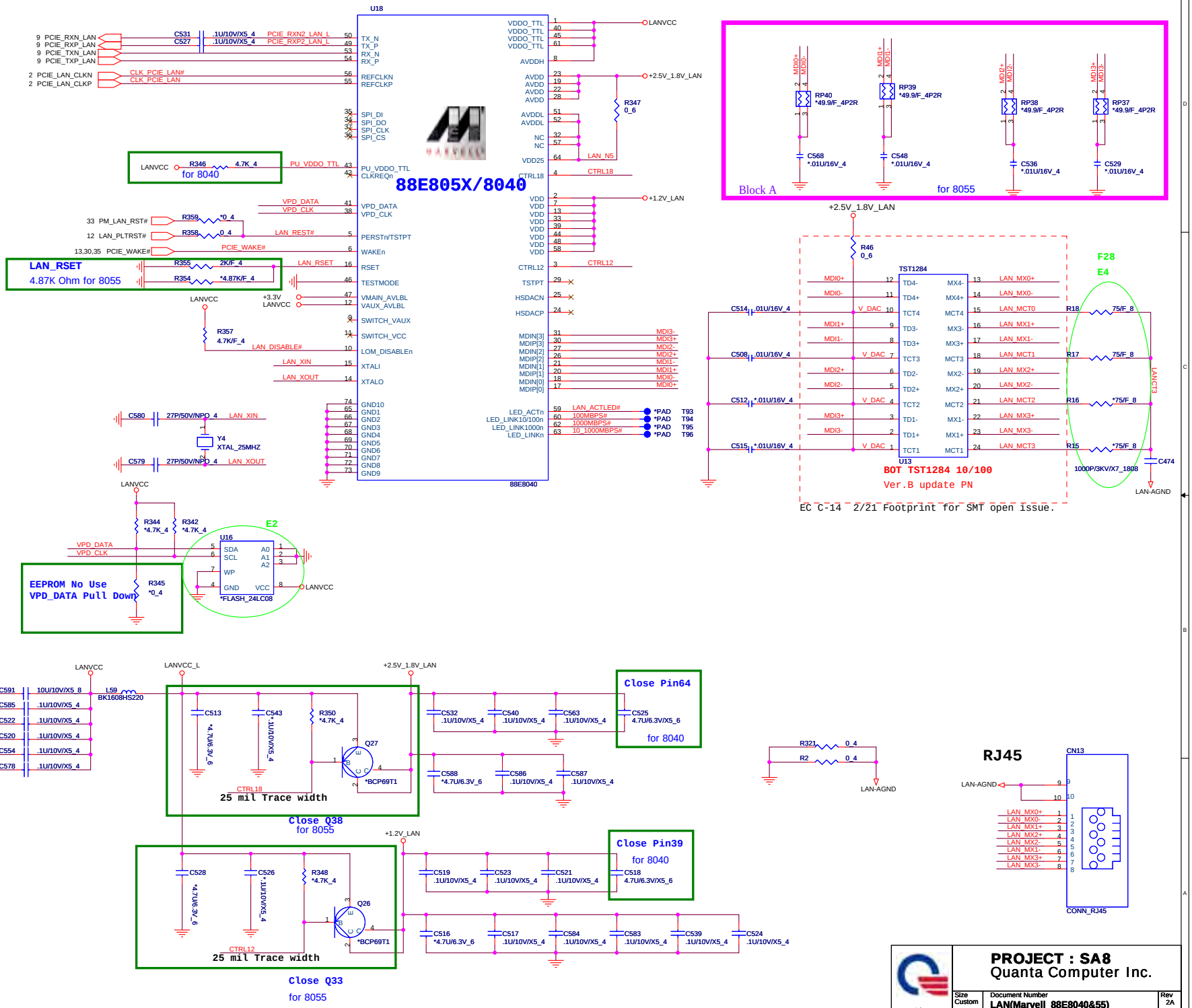
	UMA	Hybrid
R157/R162/R174	V	X
U1/U2	V	V
U3/U4	X	V

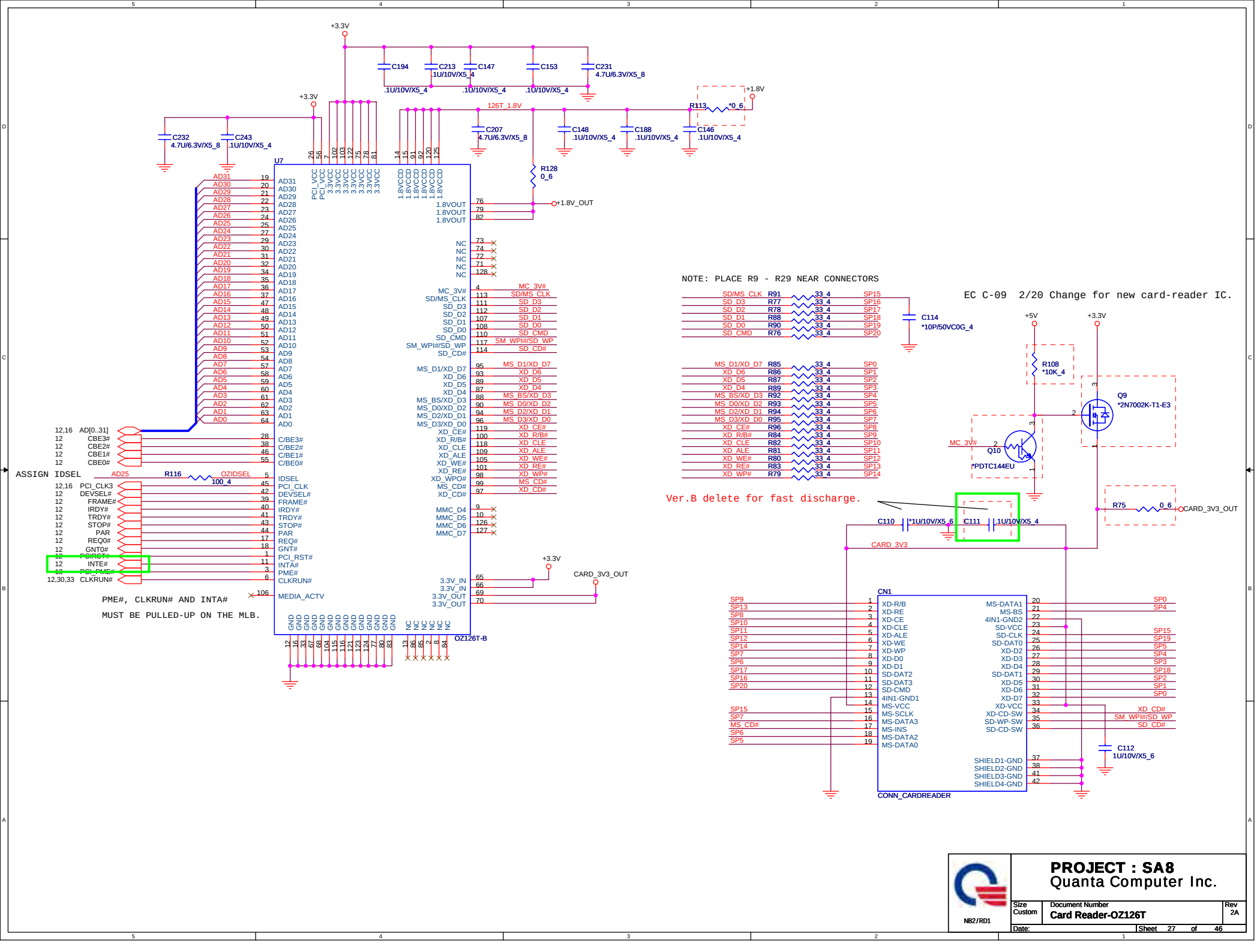
inputs		function
/E	SET	
L	L	Y - port 0
L	H	Y - port 1
H	X	Disconnect

PROJECT : SA8
Quanta Computer Inc.

Size	Document Number	Rev
C	CRT CONN & MUX	2A

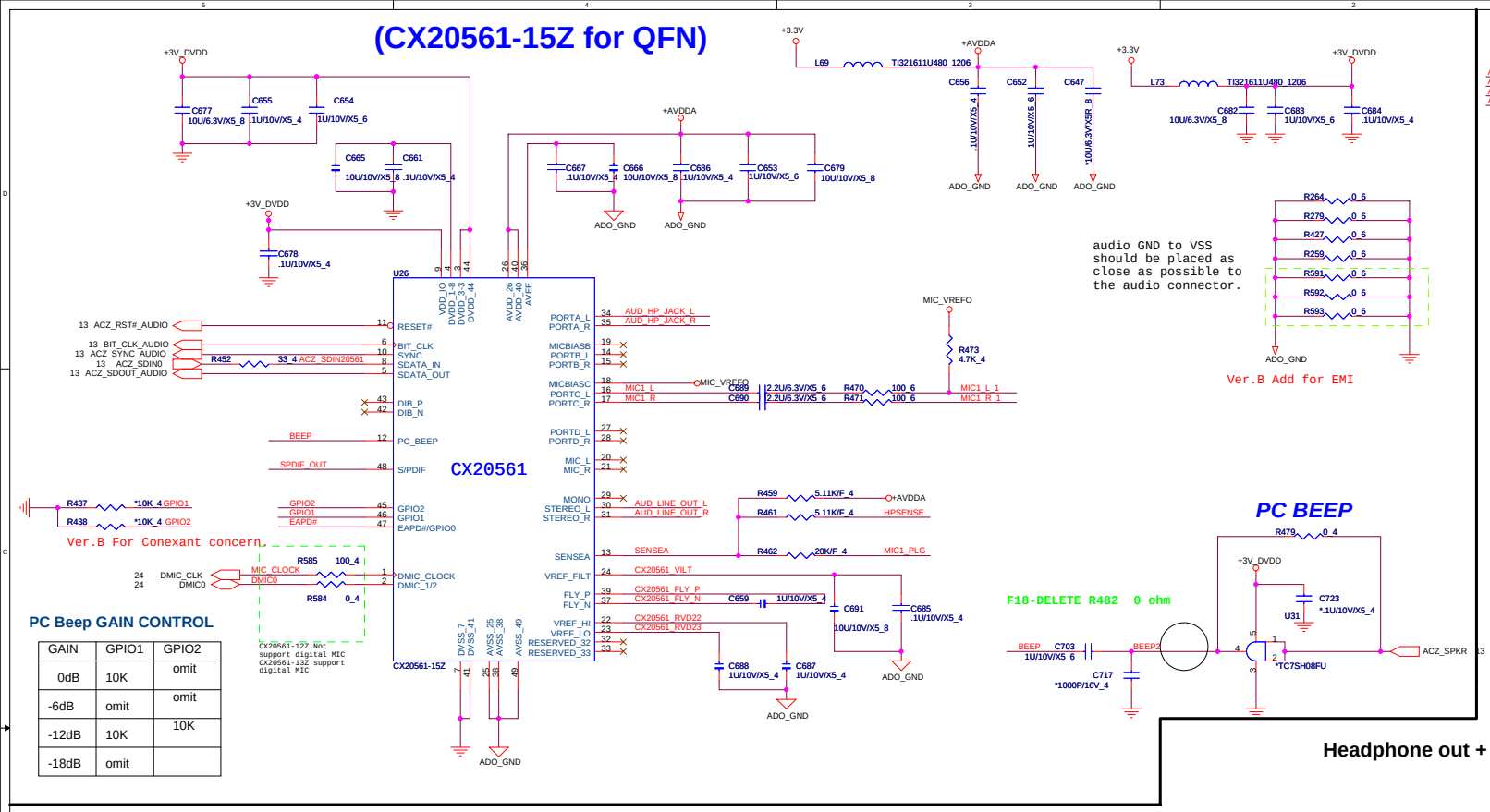
NB2/RD1 Date: Sheet 25 of 46


U18
88E805X/8040
88E8040
LANVCC
+2.5V_1.8V_LAN
+1.2V_LAN
LAN_RSET
4.87K Ohm for 8055
for 8040
for 8055
Block A
EEPROM No Use
VPD_DATA Pull Down
*FLASH_24LC08
Y4
XTAL_25MHZ
U13
TST1284
BOT TST1284 10/100
Ver.B update PN
EC C-14 2/21 Footprint for SMT open issue.
Close Pin64
Close Q38
Close Pin39
Close Q33
25 mil Trace width
RJ45
CONN_RJ45
LAN-AGND
PROJECT : SA8
Quanta Computer Inc.
LAN(Marvell 88E8040&55)
NB2/RD1



NB2/RD1	**PROJECT : SA8** Quanta Computer Inc.	
Size: Custom	Document Number: **Card Reader-OZ126T**	Rev: 2A
Date:	Sheet 27 of 46	

(CX20561-15Z for QFN)



audio GND to VSS should be placed as close as possible to the audio connector.

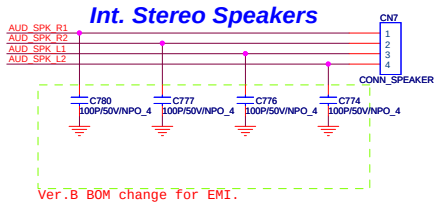
Ver.B Add for EMI

Ver.B For Conexant concern.

PC Beep GAIN CONTROL

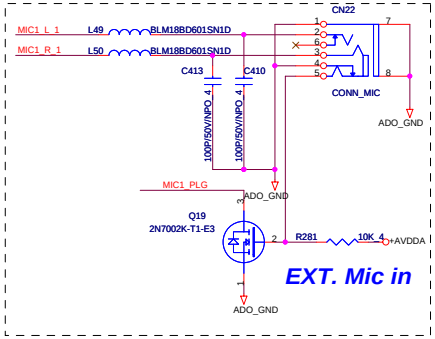
GAIN	GPIO1	GPIO2
0dB	10K	omit
-6dB	omit	omit
-12dB	10K	10K
-18dB	omit	

Int. Stereo Speakers



Ver.B BOM change for EMI.

EXT. Mic in

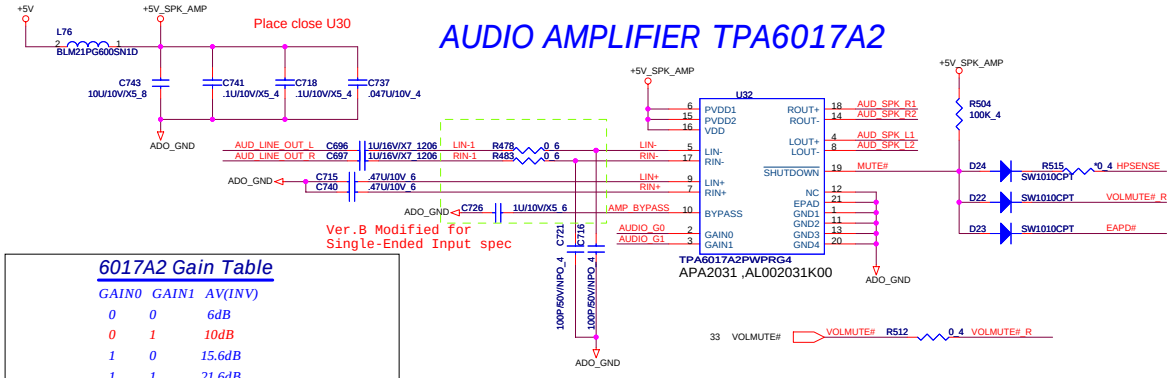


PC BEEP

F18-DELETE R482 0 ohm

Headphone out + Spdif Out (normal open)

AUDIO AMPLIFIER TPA6017A2



6017A2 Gain Table

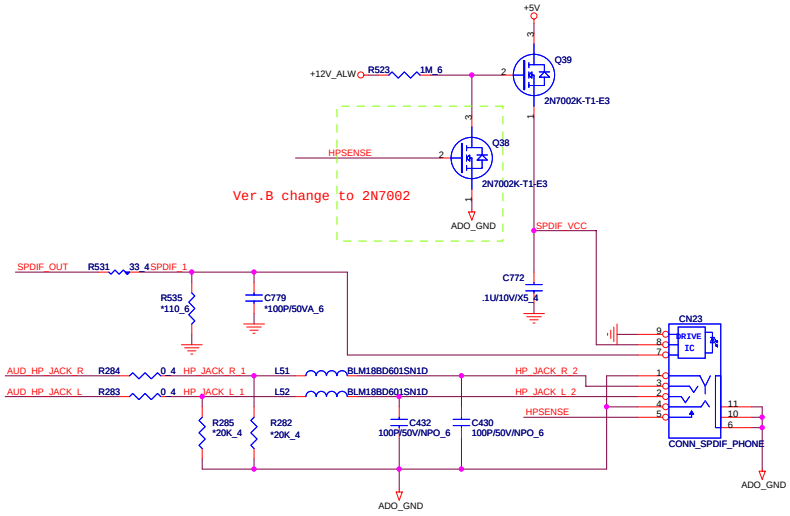
GAIN0	GAIN1	AV(INV)
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

D3- Seting Gain value for TGA request.

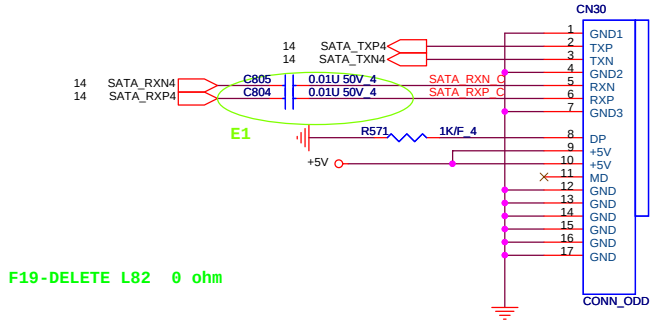
Ver.B reserver for ESD

D8-Add C808 varistor for ESD issue.

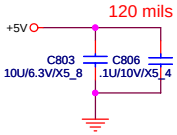
Ver.B change to 2N7002



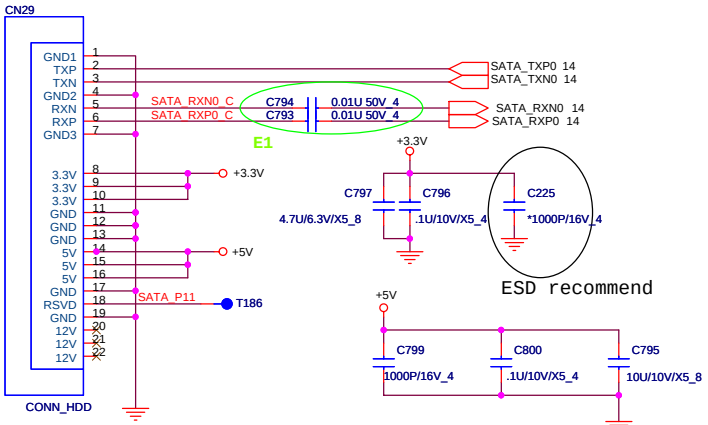
SATA ODD CONNECTOR Ver.B Change footpring for SMT issue.



F19-DELETE L82 0 ohm

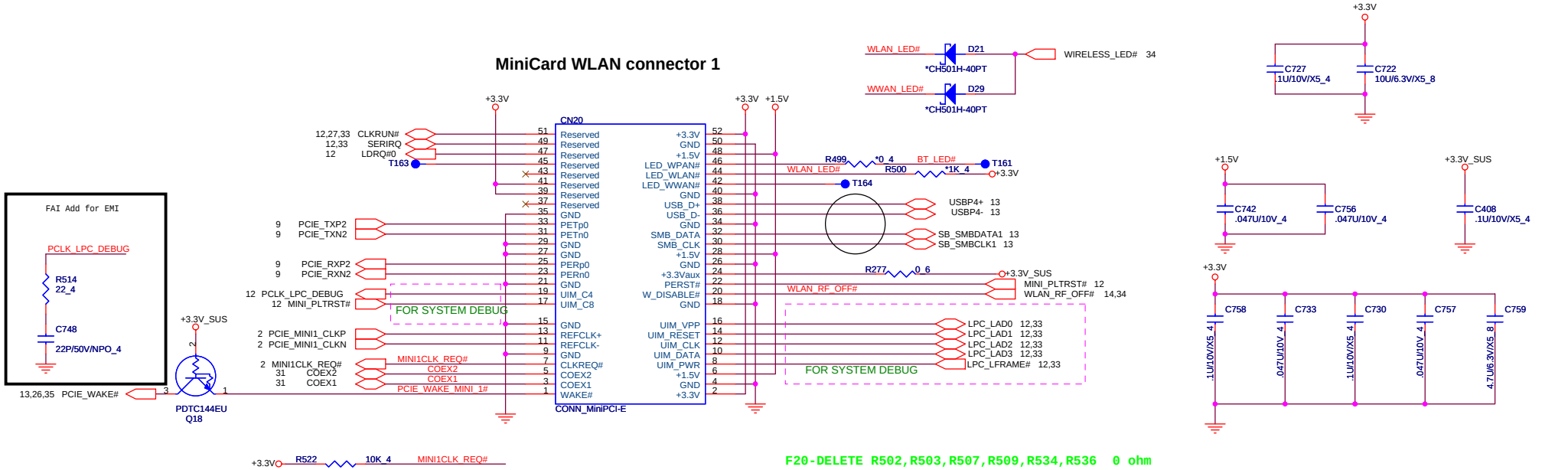


SATA HDD CONNECTOR



NB2/RD1	PROJECT : SA8 Quanta Computer Inc.	
Size: Custom	Document Number: SATA HDD ODD	Rev: 2A
Date:	Sheet 29 of 46	

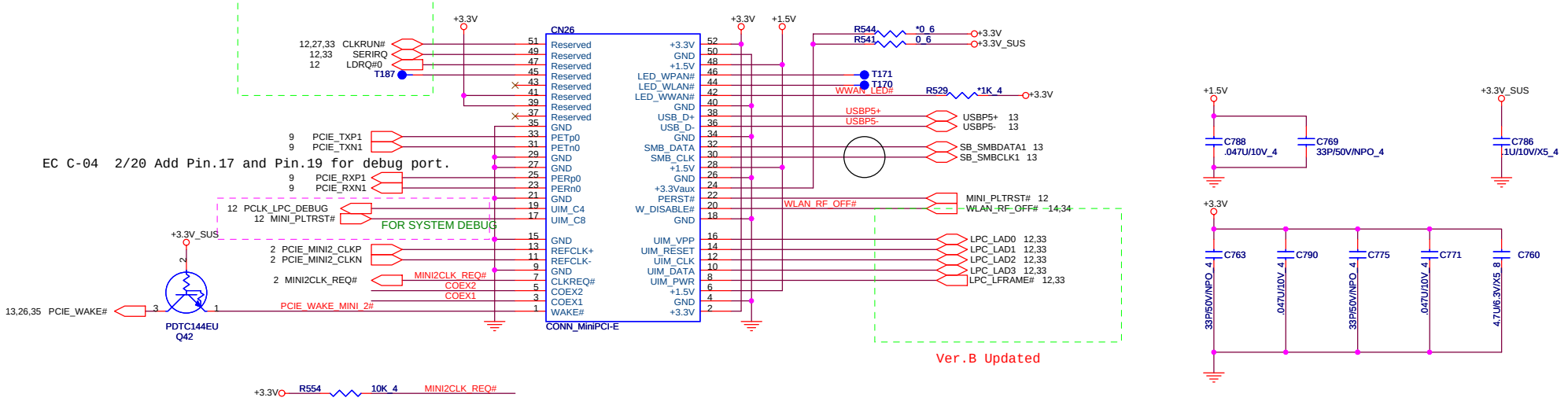
MiniCard WLAN connector 1



F20-DELETE R502,R503,R507,R509,R534,R536 0 ohm

Ver.B Updated

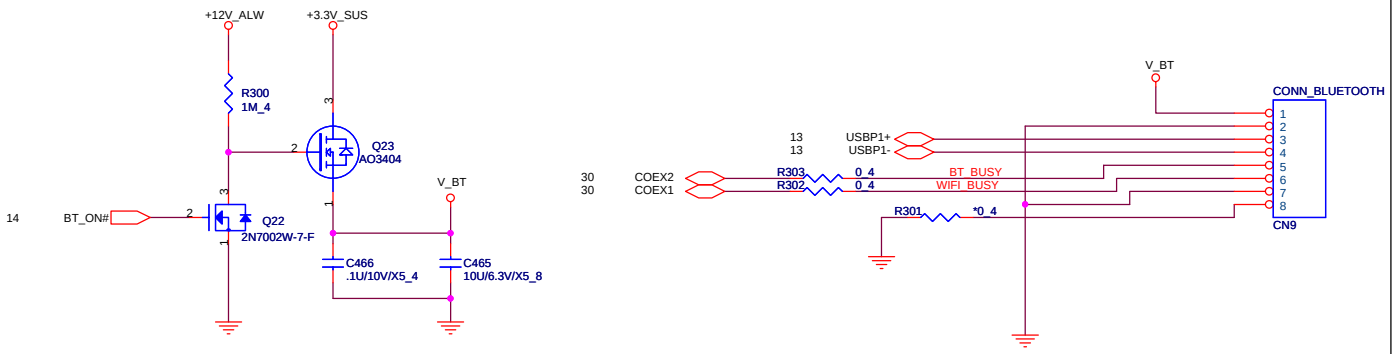
MiniCard connector 2



EC C-04 2/20 Add Pin.17 and Pin.19 for debug port.

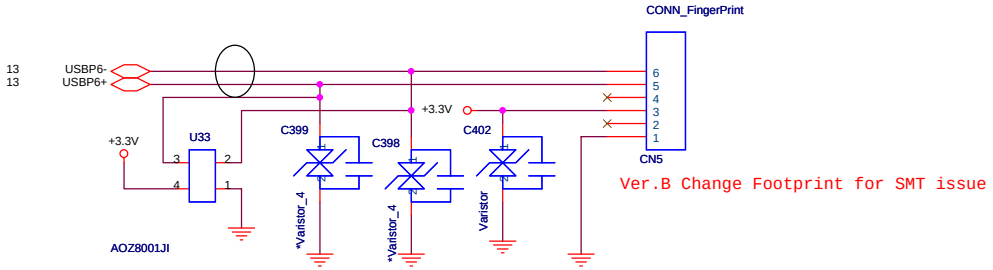
NB2/RD1	PROJECT : SA8 Quanta Computer Inc.		
	Size: Custom	Document Number: MINI PCI-E Card X2	Rev: 2A
	Date:	Sheet 30 of 46	

BLUETOOTH CONNECTOR



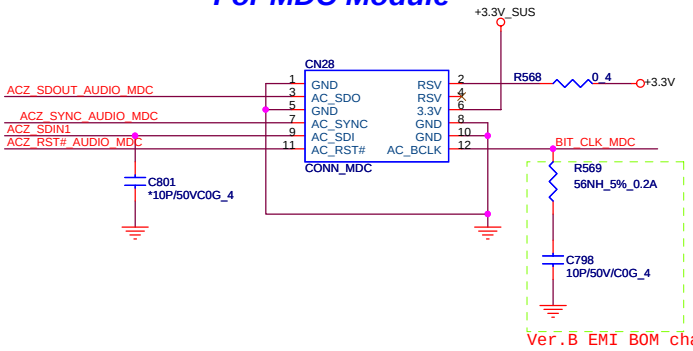
FINGERPRINT CONNECTOR

F21-DELETE R267,R268 0 ohm

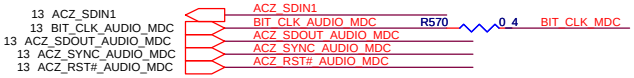


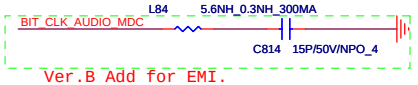
Ver.B Change Footprint for SMT issue

For MDC Module



Ver.B EMI BOM change

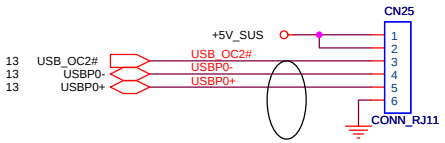


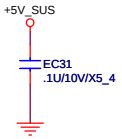


Ver.B Add for EMI.

TO RJ11/USB PORT

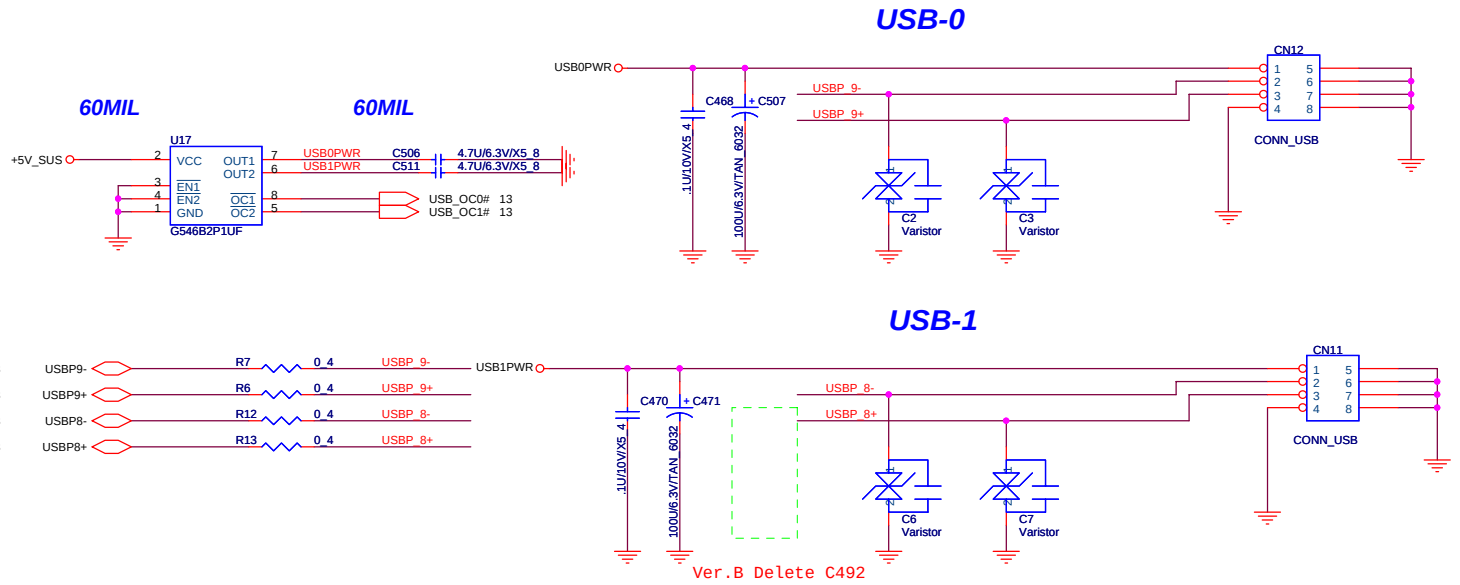
F22-DELETE R538,R540 0 ohm

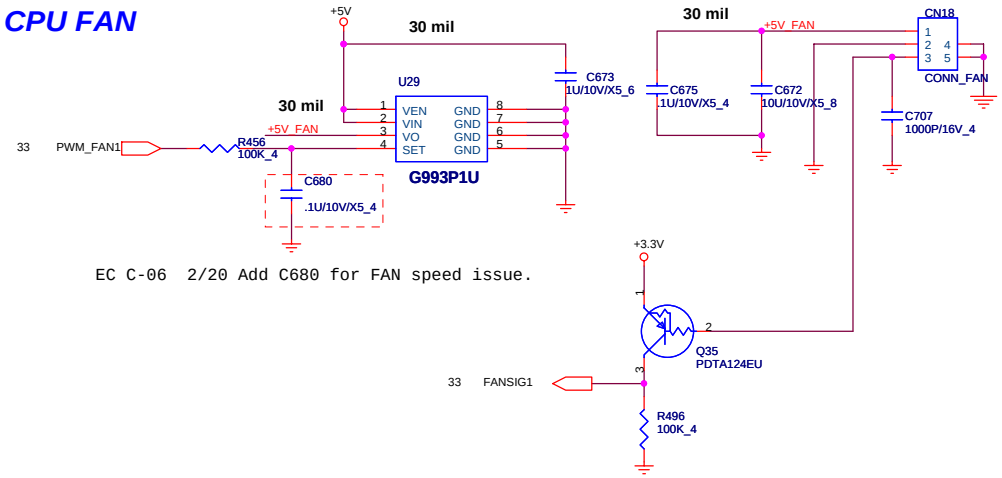




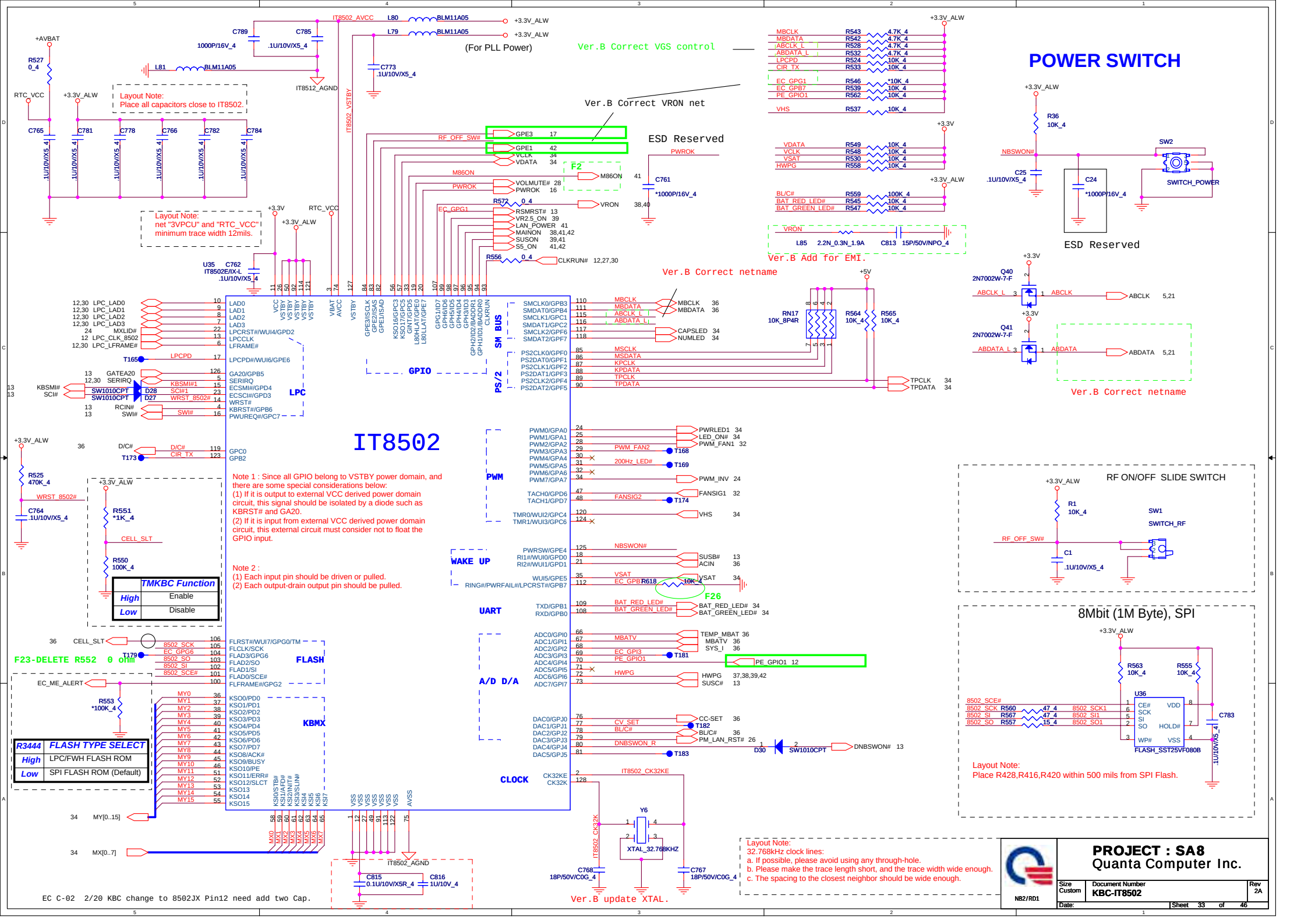
Ver.B Close to CN25.1

NB2/RD1	PROJECT : SA8 Quanta Computer Inc.	
	Size: Custom Document Number: Bluetooth,FingerPrint,USBX1	Rev: 2A
	Date:	Sheet 31 of 46

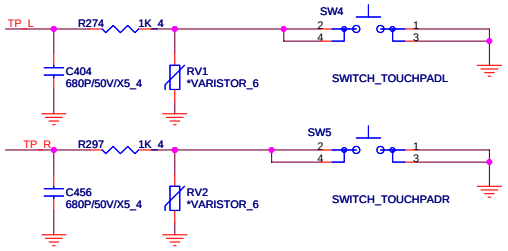




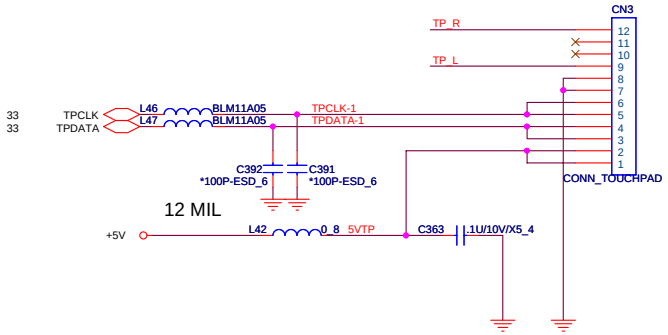
NB2/RD1	**PROJECT : SA8** Quanta Computer Inc.	
Size: Custom	Document Number: **USB CONN X2ports**	Rev: 2A
Date:	Sheet 32 of 46	


IT8502
POWER SWITCH
(For PLL Power)
Ver.B Correct VGS control
Ver.B Correct VRON net
ESD Reserved
Ver.B Add for EMI.
Ver.B Correct netname
RF ON/OFF SLIDE SWITCH
8Mbit (1M Byte), SPI
Layout Note:
Place all capacitors close to IT8502.
Layout Note:
net "3VPCU" and "RTC_VCC"
minimum trace width 12mils.
Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.
Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.
F23-DELETE R552 0 ohm
F2
F26
Layout Note:
Place R428,R416,R420 within 500 mils from SPI Flash.
Layout Note:
32.768kHz clock lines:
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.
Ver.B update XTAL.
EC C-02 2/20 KBC change to 8502JX Pin12 need add two Cap.
PROJECT : SA8
Quanta Computer Inc.
KBC-IT8502
NB2/RD1
Sheet 33 of 46

TOUCHPAD SWITCH CONN

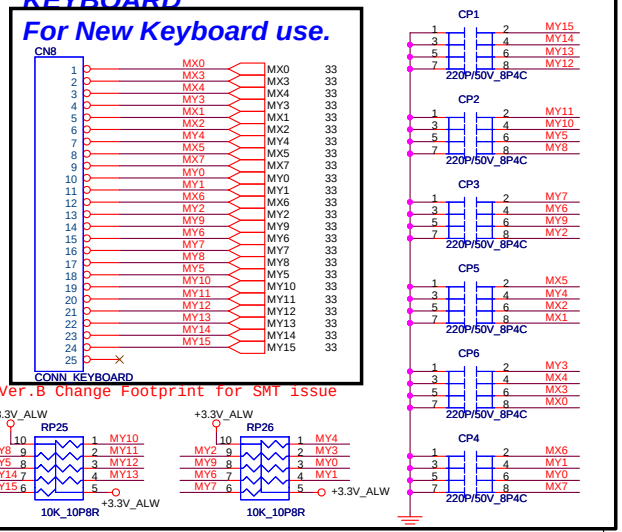


Ver.B Change Footprint for SMT issue

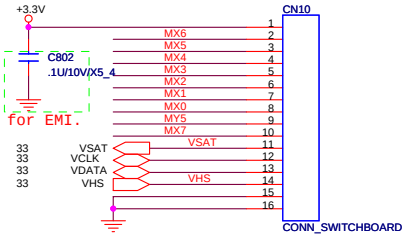


KEYBOARD

For New Keyboard use.



Ver.B Change Footprint for SMT issue

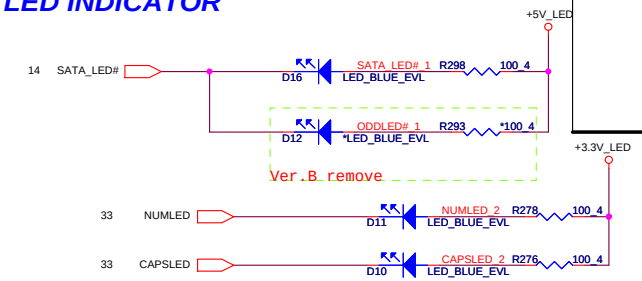


Ver.B BOM change for EMI.

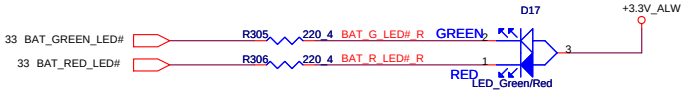
Ver.B Change Footprint for SMT issue

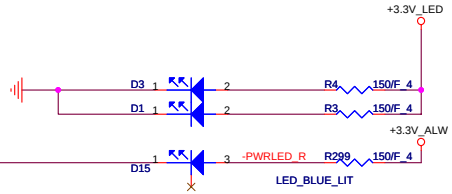
F24-DELETE R307,R308 0 ohm

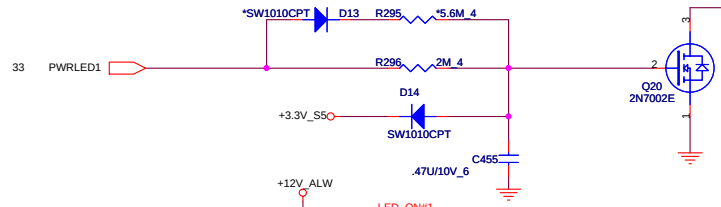
LED INDICATOR



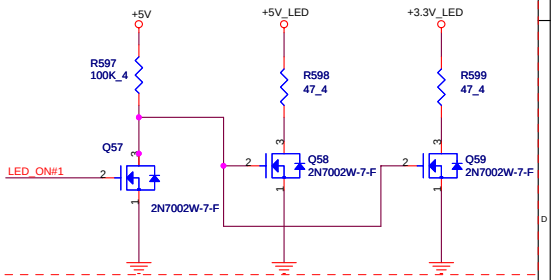
Ver.B remove

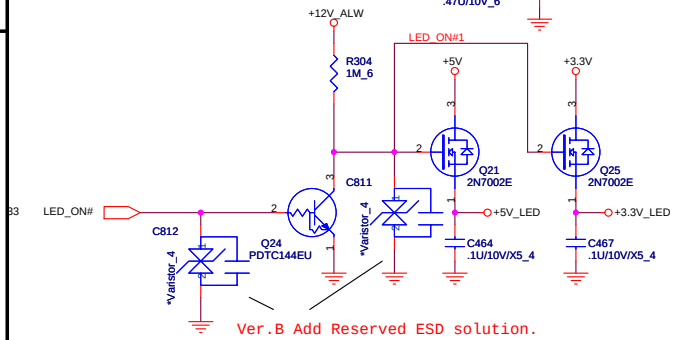






EC C-01 2/20 for LED +3.3V_LED and +5V_LED leak electricity.



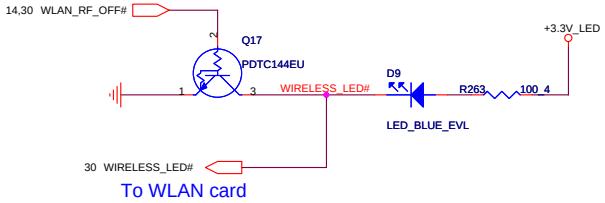


Ver.B Add Reserved ESD solution.

SWITCH/Volume cintral BOARD

WIRELESS LED

From ICH8-M

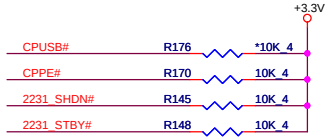


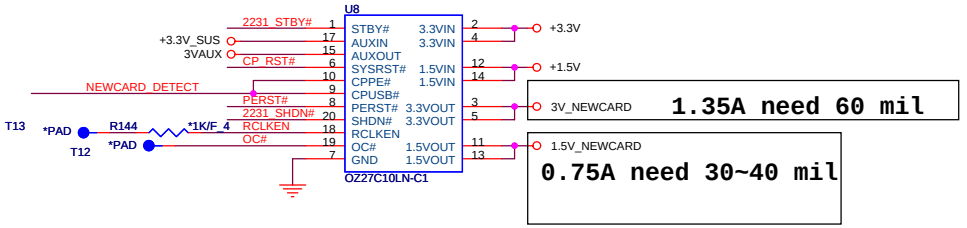
To WLAN card

LED POWER DISCHARGE

N82/RD1	PROJECT : SA8 Quanta Computer Inc.	
Size: Custom	Document Number: TP/KB/LED/SW CONN.	Rev: 2A
Date:	Sheet 34 of 46	

NEWCARD





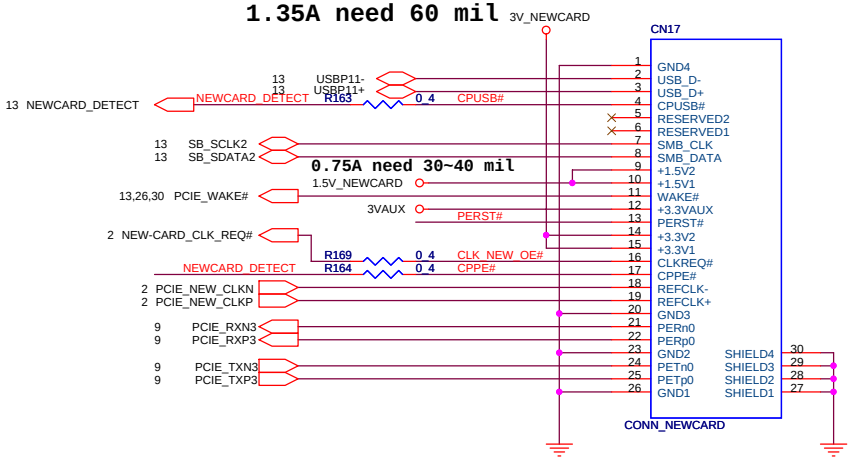
1.35A need 60 mil

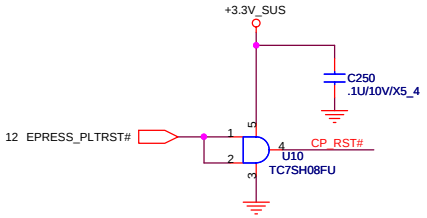
3V_NEWCARD

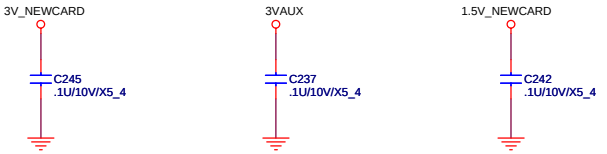
1.5V_NEWCARD

0.75A need 30~40 mil

F25-DELETE R402,R403 0 ohm







NB2/RD1

PROJECT : SA8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NEW CARD	1A
Date:	Sheet 35 of 46	

BATTERY CHARGER

Ver.B Change Footprint

90W for Discrete
65W for UMA

C-Test Modify

Place close to EC,

Place these CAPs close to FETs

Ver.B BOM change

Ver.B Change BOM for EMI

Setting the Vin min to 12V
For ACSET 1.26V

Setting the Vin min to 17V
For EN = 1.06V

CELL_SLT = 1 -- 3 S (Cells = GND 3S) Ver.B Modified.
CELL_SLT = 0 -- 4 S (Cells = VDD 4S)

Charging Curret setting =>
I chg = 165mV / R2 * (Vchlim / 3.3V)

Input Current monitor
V icm = 19.9 * (Vcsip - Vcsin)

Battery Low 7.5V

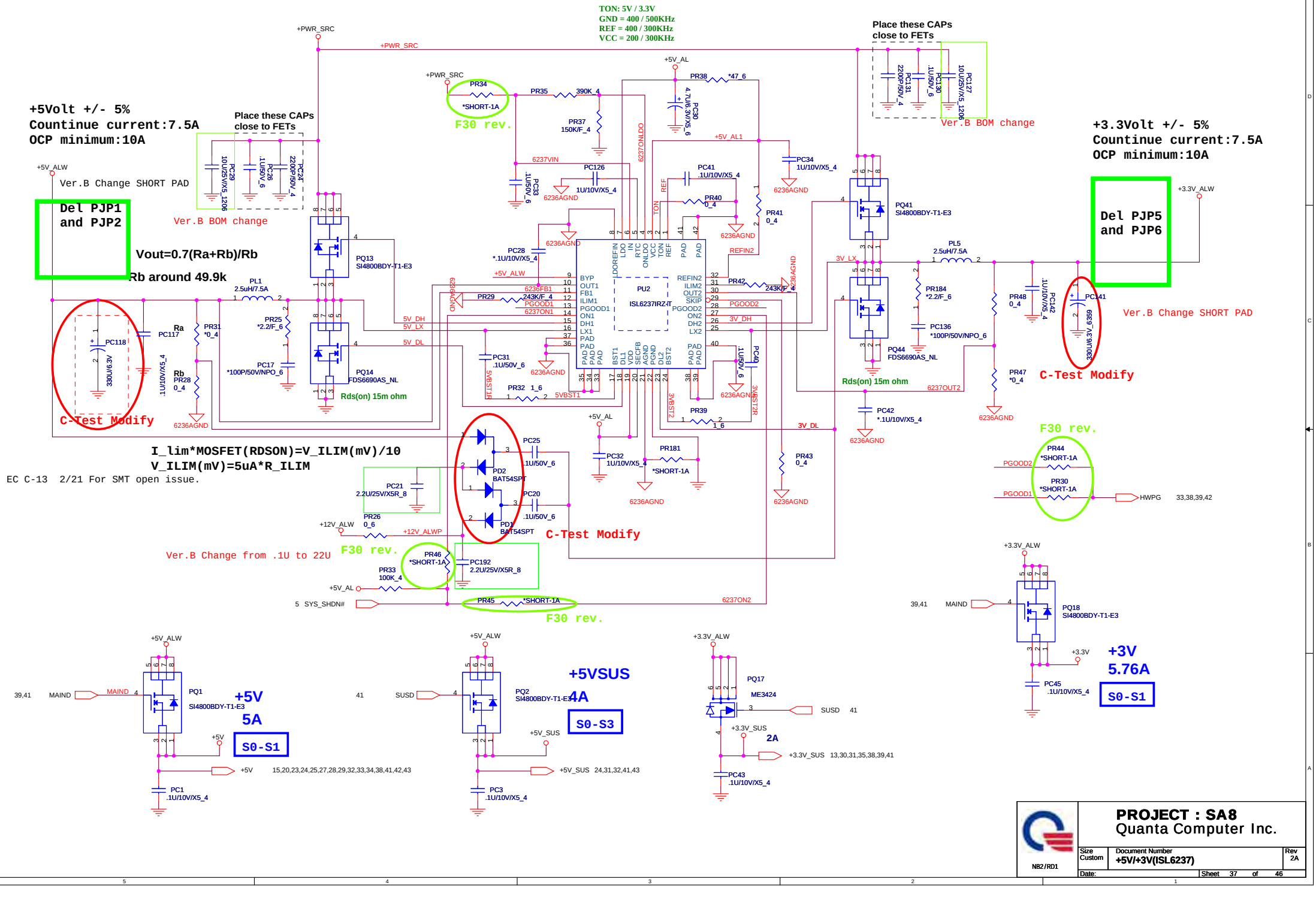
ADP TYPE	Rhigh	P/N
65W	178K/F_4	CS41782FB11
90W	11K/F_4	CS31102FB11

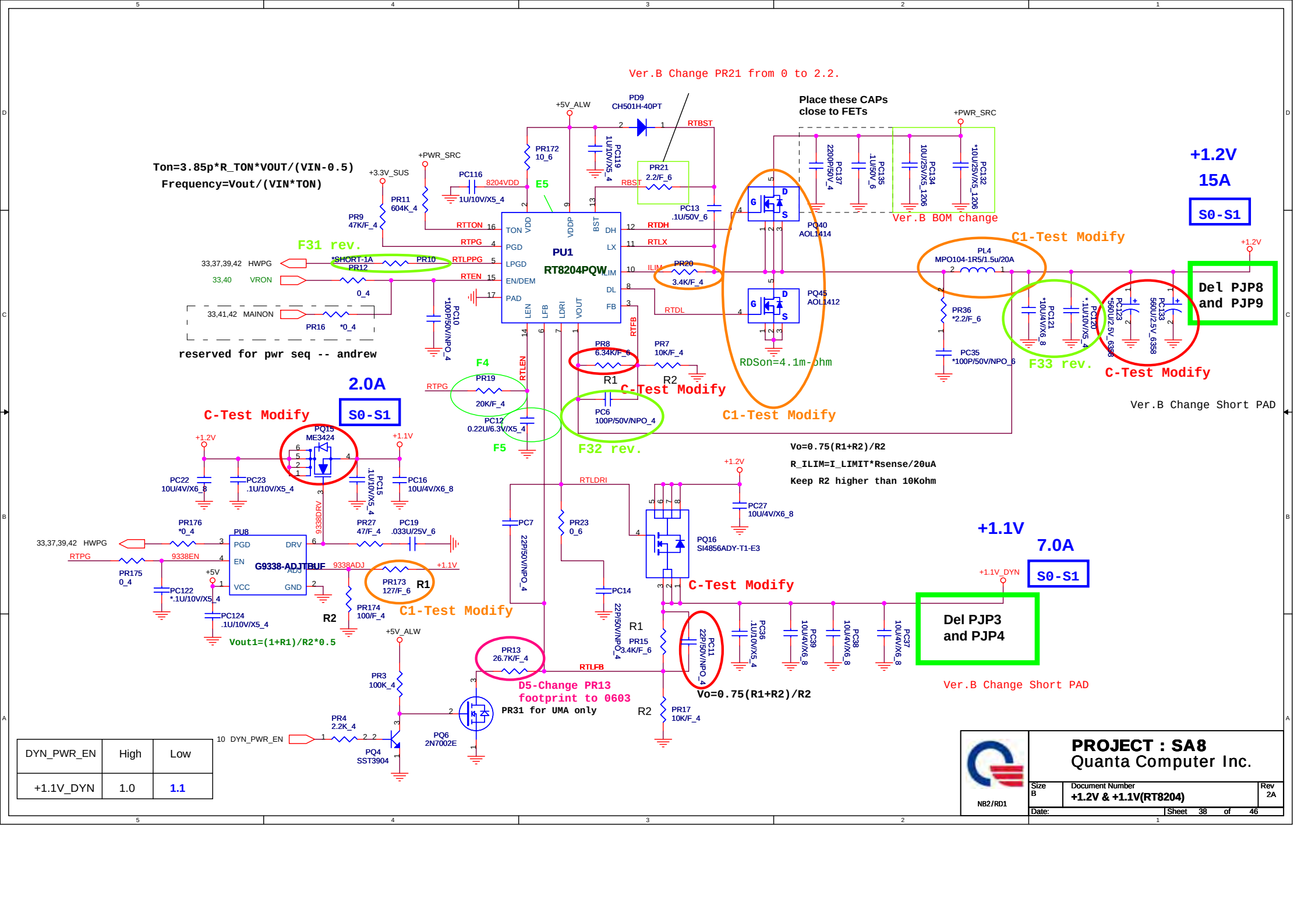
Ver.B change PR214/PR216 from 100K to 10K
Ver.B PC185 NC
Ver.B PC184 NC

PROJECT : SA8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CHARGER (ISL6251)	2A
Date:	Sheet 36 of 46	

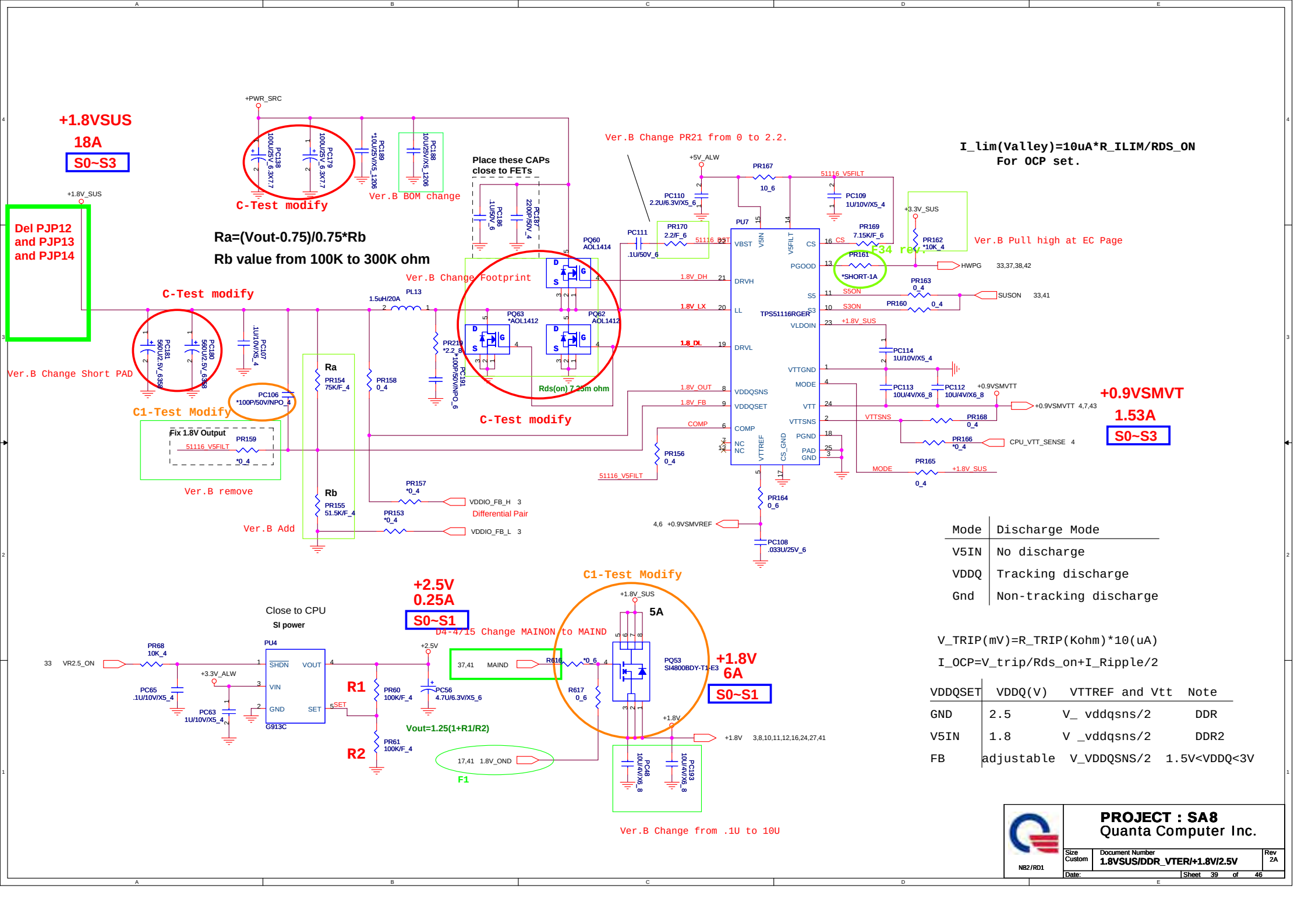
NB2/RD1


TON: 5V / 3.3V
GND = 400 / 500KHz
REF = 400 / 300KHz
VCC = 200 / 300KHz
+5Volt +/- 5%
Countinue current:7.5A
OCP minimum:10A
Ver.B Change SHORT PAD
Del PJP1 and PJP2
Vout=0.7(Ra+Rb)/Rb
Rb around 49.9k
Place these CAPs close to FETs
Ver.B BOM change
C-Test Modify
Rds(on) 15m ohm
I_lim*MOSFET(RDSON)=V_ILIM(mV)/10
V_ILIM(mV)=5uA*R_ILIM
EC C-13 2/21 For SMT open issue.
F30 rev.
Ver.B Change from .1U to 22U
+3.3Volt +/- 5%
Countinue current:7.5A
OCP minimum:10A
Del PJP5 and PJP6
+5V 5A S0-S1
+5VSUS 4A S0-S3
+3V 5.76A S0-S1
PROJECT : SA8
Quanta Computer Inc.
NB2/RD1
Document Number +5V/+3V(ISL6237)
Size Custom
Rev 2A
Sheet 37 of 46



DYN_PWR_EN	High	Low
+1.1V_DYN	1.0	1.1

NB2/RD1	PROJECT : SA8 Quanta Computer Inc.	
	Size: B Document Number: +1.2V & +1.1V(RT8204)	Rev: 2A
	Date:	Sheet 38 of 46



Mode	Discharge Mode
V5IN	No discharge
VDDQ	Tracking discharge
Gnd	Non-tracking discharge

VDDQSET	VDDQ(V)	VTTREF and Vtt	Note
GND	2.5	V_ vddqsns/2	DDR
V5IN	1.8	V _vddqsns/2	DDR2
FB	adjustable	V_VDDQSNS/2	1.5V<VDDQ<3V

PROJECT : SA8
Quanta Computer Inc.

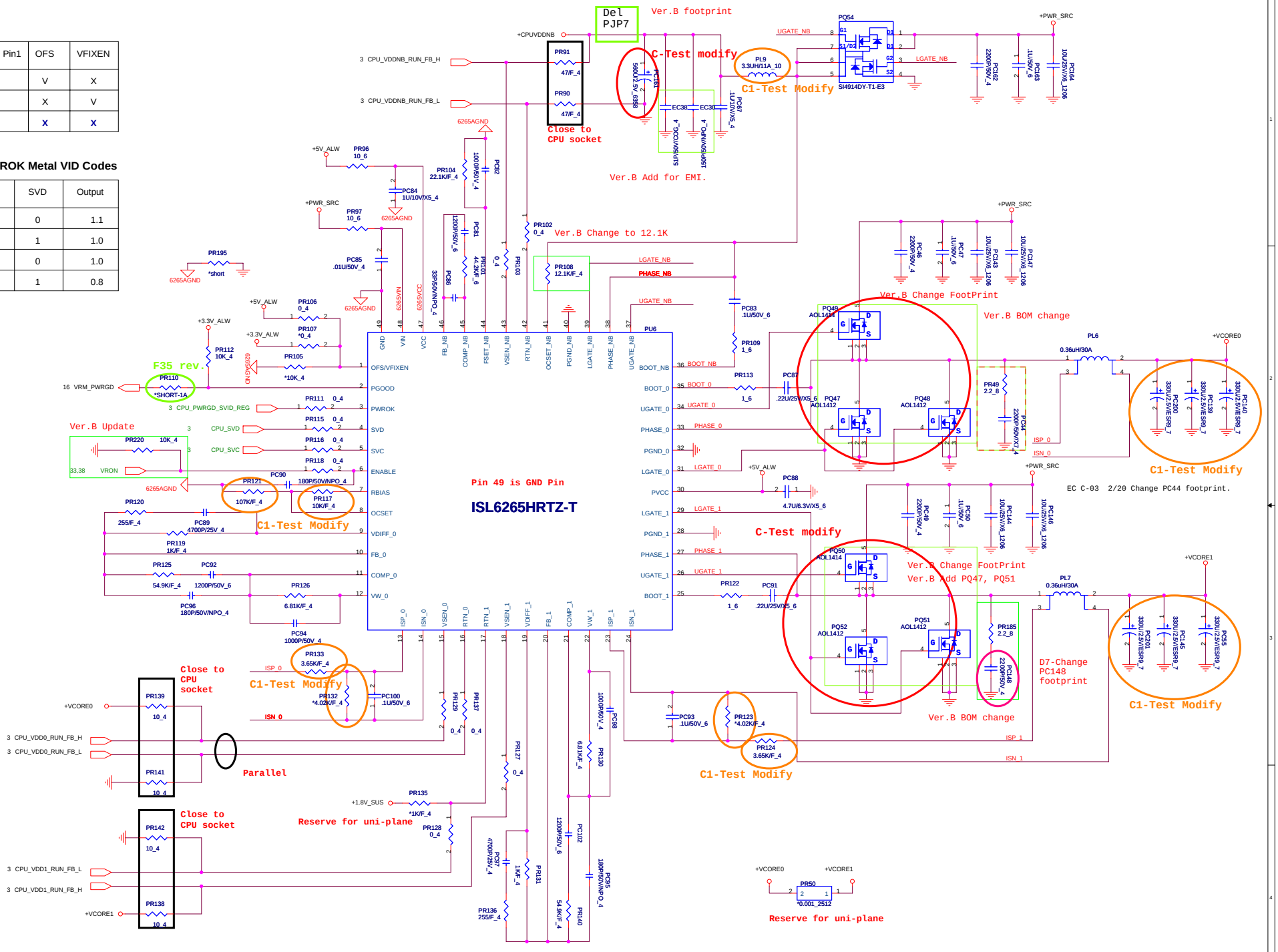
NB2/RD1

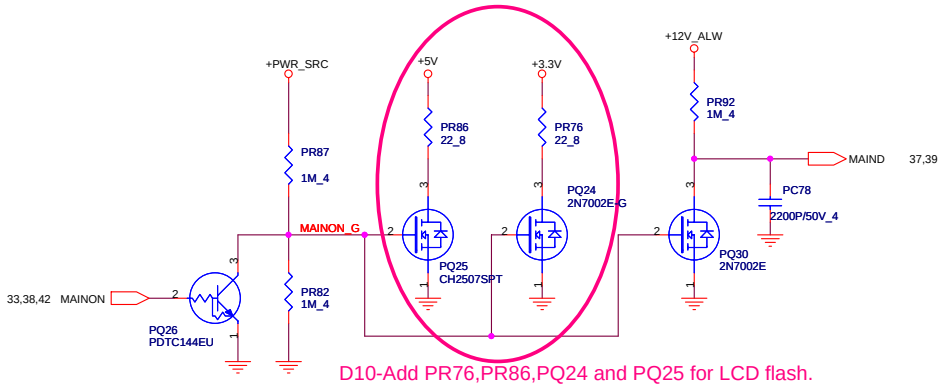
Size	Document Number	Rev
Custom	1.8VSUS/DDR_VTER/+1.8V/2.5V	2A
Date:	Sheet 39 of 46	

ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

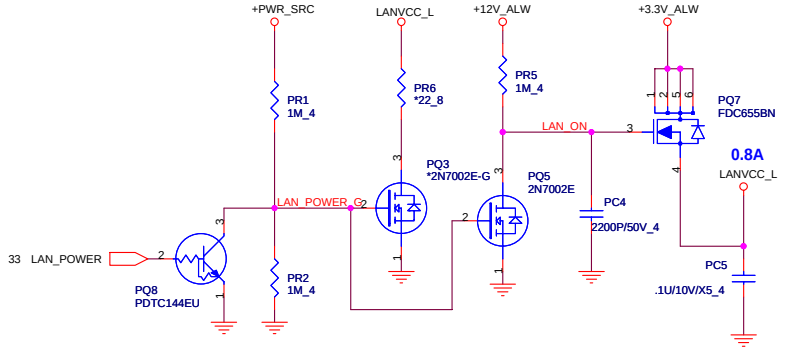
Pre-PWROK Metal VID Codes

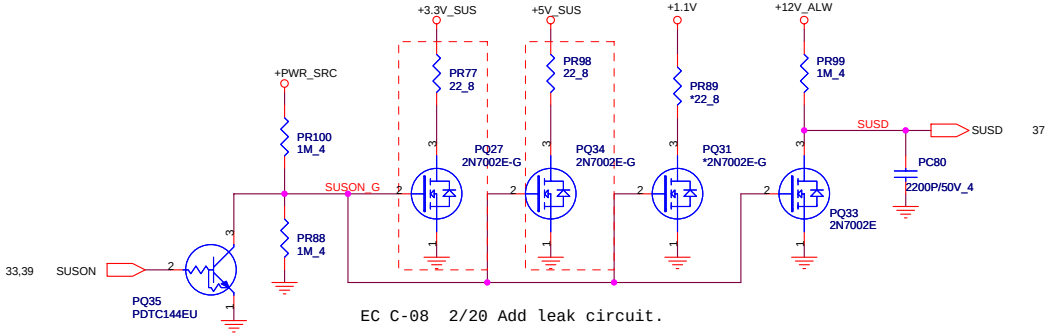
SVC	SVD	Output
0	0	1.1
0	1	1.0
1	0	1.0
1	1	0.8



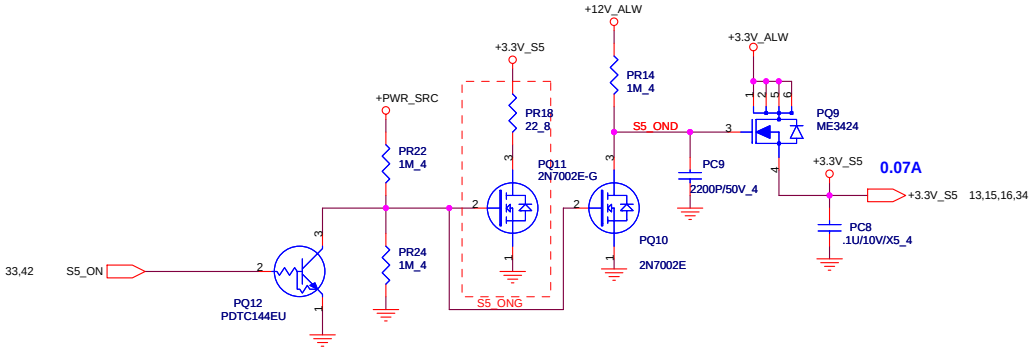


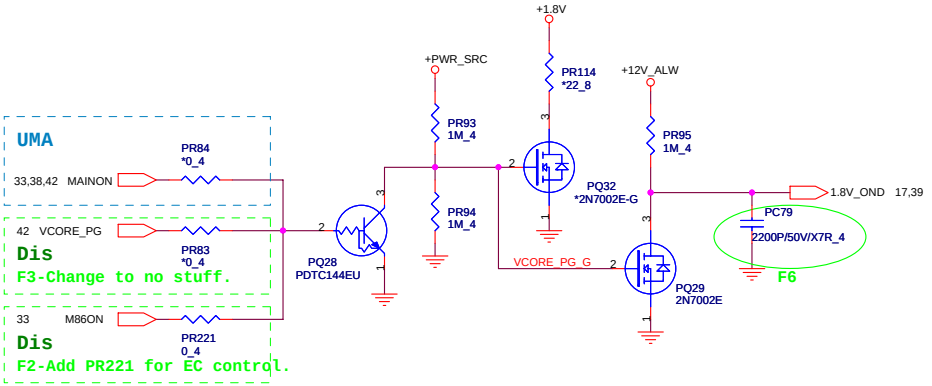
D10-Add PR76,PR86,PQ24 and PQ25 for LCD flash.





EC C-08 2/20 Add leak circuit.

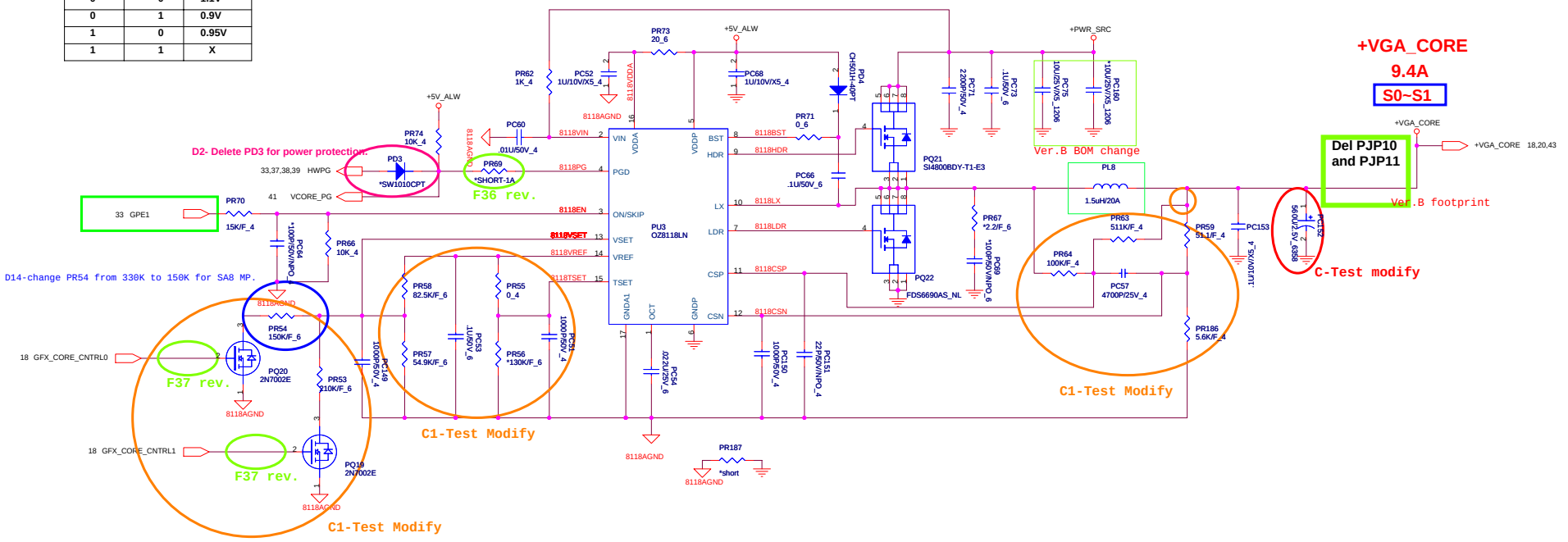


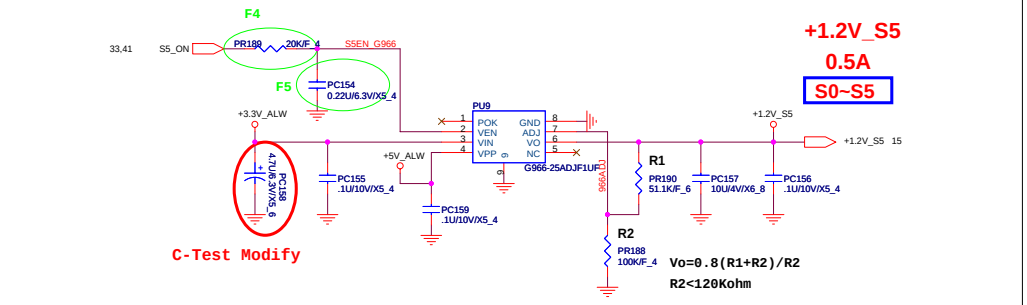


	PROJECT : SA8 Quanta Computer Inc.	
N82/RD1	Size: Custom Document Number: **DISCHARGE**	Rev: 1A
	Date:	Sheet 41 of 46

ATI M86

PWRCTL1	PWRCTL0	VDD_CORE
0	0	1.1V
0	1	0.9V
1	0	0.95V
1	1	X



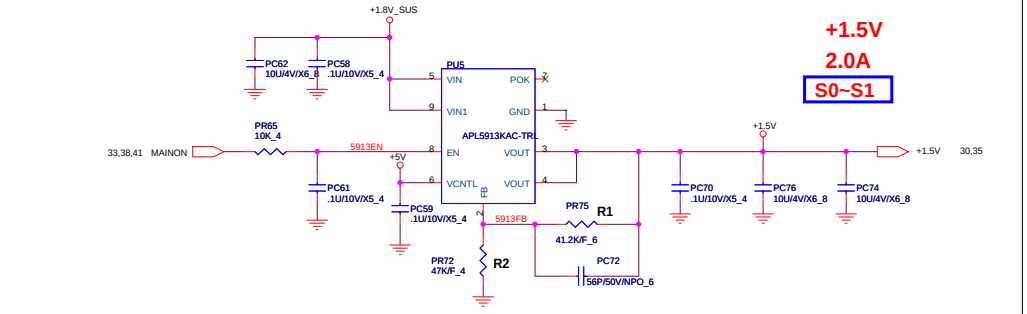


Ver.B Add +1.35V power supply for A11 version of RS780.

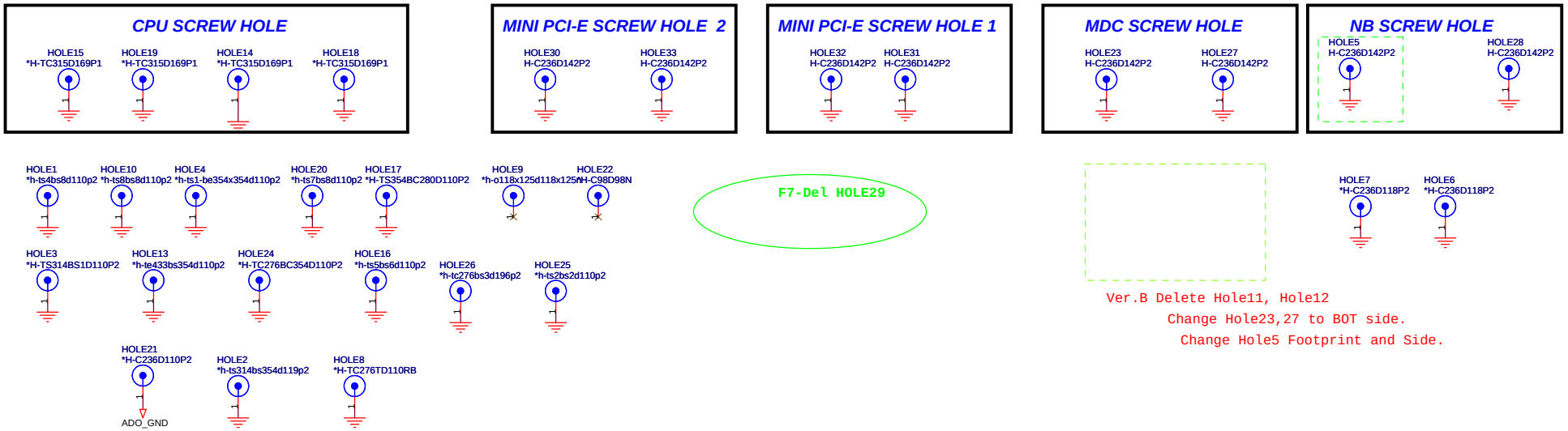
Ver.D Del +1.35V power supply for A11 version of RS780.

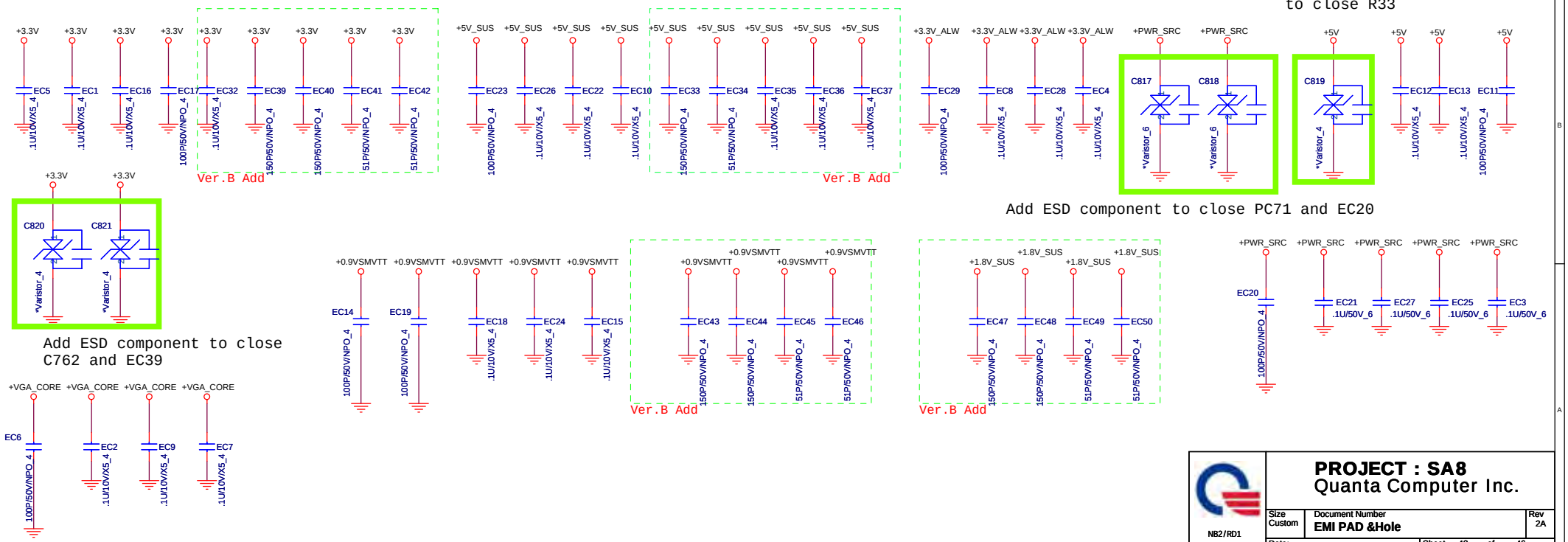
0.5A

S0-S1



PROJECT : SA8 Quanta Computer Inc.		
NB2/RD1	Size: C Document Number: VGA PWR 1.2V_S5/+1.5/+1.35V	Rev: 2A
	Date:	Sheet 42 of 46





PROJECT : SA8 Quanta Computer Inc.			
Size: Custom	Document Number: EMI PAD &Hole		Rev: 2A
NB2/RD1	Date:	Sheet 43 of 46	

Ver.A to Ver.B

PAGE 2

(1) Update Xtal Y2 Cload to 33P...12/25

PAGE 3

(1) Add C807 for Old CPU Boot-up issue.
(2) NC R212 for Debug reserved.
(3) Correct REST_L,PWROK,LDTSTOP_L,LDTREQ_L to +1.8V...12/14
(4) Add R594,R595,R596 for Griffin Sighting issue...12/18
(5) Add test PAD for TEST7,TEST8...12/18

PAGE 5

(1) Correct SM Bus Level Shift VGS control.

PAGE 6

(1) Modify DDR Socket footprint, and change Part to Heigh 4/8.

PAGE 10

(1) Add CRT Sync and DDC connection for Hybrid.
(2) Add Hot Plug TMDS connection. for M86.
(3) Modify PX_EN control logic.
(4) Update PX_EN control logic, add R586 for UMA reserved..12/14

PAGE 11

(1) Mount L32 for NB 1.2V source.

PAGE 12

(1) Correct CMOS Battery connector connection.
(2) Connect GPIO35 for PX_EN control.
(3) C698,C364 change BOM for EMI...12/17

PAGE 13

(1) Correct GPIO6, GPIO39 netname.
(2) Change USB Port9 to Port2 due to Phoenix BIOS can't program in DOS mode.
(3) Correct R180 BOM error.
(4) Add R583 to pull high PCI_PME# to solve CardController S3 floating issue...12/12
(5) Add L86 for EMI...12/17

PAGE 14

(1) Correct U12 Power and GND Pin define.
(2) Update 25MHz Xtal Cload to 27P...12/25

PAGE 15

(1) Correct U27.F12 connection.

PAGE 16

(1) Reserve R486 for old version of SB700.
(2) Add AD[30..31] Reserved PD...12/17

PAGE 18

(1) Correct HDMI_P/N connection for Discrete HDMI issue... 12/14
(2) Update XTAL Y3 to 6.8P...12/25

PAGE 23

(1) Add Isolation Logic for HPD signal...Cancel change on 12/18

PAGE 24

(1) Remove VGA to LVDS Jump connection.RN1,2,3,4,5,7,9,13.
(2) Add Isolation and Wired Or Logic for LVDS control signal.

PAGE 25

(1) Add U1/U2 Synce connection from VGA for Hybrid.
(2) Change +5VCRT source for DDC leakage issue.
(3) Add F2 for CRT Pin9 5V current limit.
(4) Add Isolataion Logic for Sync control.
(5) Change L18,L19,L21 BOM for EMI...12/17

PAGE 26

(1) Change 10/100 transformer PN for material issue...12/31

PAGE 27

(1) Remove C110,C111 for VCC fast discharge...12/20

PAGE 28

(1) Swap AMp Pin9/7 connection to Pin5/17 for Singal
End input Spec, Also change 726 to 1U for pop issue.
(2) Change Q38 to 2N7002E...12/12
(3) Add ESD solution(Reserved) for Audio...12/14
(4) Add 100Ohm in series with DMIC_CLK...12/14
(5) EMI BOM change for Speaker out...12/17
(6) Add R591,R592,R593 for ADO/GND EMI...12/17

PAGE 29

(1) Change SATA ODD connector for SMT issue.

PAGE 30

(1) Add LPC connection for CN26, Futher Wirelss support.

PAGE 31

(1) Change CN5 Footprint for SMT issue...12/12
(2) Add EC31 close to CN25.1 for EMI...12/17
(3) Add L84,C814 for BICLK EMI...12/17
(4) Change R569,C798 BOM for EMI...12/17

PAGE 32

(1) Delete C492, Already have USB Bulk in design.

PAGE 33

(1) Correct ABDATA netname.
(2) Correct EC output ABCLK,ABDATA netname.
(3) Correct VRON net and remove R546 due to VRON
pull-low at power page.
(4) Correct SM Bus level shift VGS control.
(5) Add R572 to connect VRON.
(6) Add ESD(Reserved) solution for Led_On#1 and LED_ON#...12/14
(7) Add L85,C813 for VRON EMI...12/17
(8) Update Xtal Y6 CLoad to 18P...12/25

PAGE 34
(1) Remove ODD LED indicator.
(2) Change CN10 Footprint for SMT issue...12/12
(3) Change CN8 Footprint for SMT issue...12/12
(3) Change CN3 Footprint for SMT issue...12/12
(4) C802 BOM change for EMI...12/17

POWER CHANGES

PAGE 36

(1) Change PR214/PR216 from 100K to 10K.
(2) Change CN15 DC Jack Footprint for SMT issue.
(3) Delete PC185, PC184.
(4) PR134,PC103 BOM change for EMI...12/17
(5) PC101,PC168,PC165,PC166 change BOM...12/17
(6) NC PQ38, PR205, Mount PR151...12/19

PAGE 37

(1) Change PJP1,2,5,6 Open PAD to SHORT PAD
(2) Change PC21,PC18 from .1U to 22U
(3) PC127,PC29 change BOM...12/17

PAGE 38

(1) Change PJP8,9,3,4 Open PAD to SHORT PAD
(2) Change PR21/PR36 from 0 to 2.2.
(3) PQ46 remove...12/17
(4) Change PL4 PN...12/17
(5) PC134 change BOM...12/17

PAGE 39

(1) Change PJP12,13,14 Open PAD to SHORT PAD
(2) Remove PR162 due to HWPG Pull-High at EC Page.
(3) Change PQ60,62,63 footprint and material.
(4) Add +1.8V Bulk, PC48, PC193.
(5) Change PR170 from 0 to 2.2Ohm
(6) Change PL4 PN...12/17
(7) PC188 change PN...12/17
(8) Remove PR159...12/22
(9) Add PR154,PR155 to fine tune +1.8V...12/22

PAGE 40

(1) Change PQ49,PQ48,PQ47,PQ50,PQ51,PQ52 footprint and material.
(2) Change PR108 to 12.1K.
(3) Add VRON Pulllow PR220= 10K.
(4) Change PR121 to 22K.
(5) Update PL9 Footprint.
(6) Add PD47,PD51.
(7) Add EC30/EC38 for EMI...12/17
(8) PR185,PR49,PC148,PC44 BOM change for EMI...12/17
(9) Change PJP7 footprint.
(10) Change PC145,PC55 to ESR9 material for 3DMark ripple issue...12/31

PAGE 42

(1) Add VGA core vary control for M86/M82 Config.
(2) Change PR54 from 665K to 604K; PR53 from 665K to 240K...12/21
(3) Change PR58 from 165K to 147K...12/19
(4) Change PR57 from 110K to 100K.
(5) Add +1.35V support.
(6) PC75 change PN...12/17
(7) Change PJP10,PJP11 footprint...12/17
(8) Change PL8 to 1.5uH/20A...12/19

PAGE 43

(1) Delete Hole11, Hole12.
(2) Change HOLE23,HOLE27 to Bottom side.
(3) Change Hole5 Footprint and Side.
(4) Add EMI decoupling...12/17

NB2/RD1	**PROJECT : SA8** Quanta Computer Inc.	
Size: C	Document Number: **Change List Ver.A to Ver.B**	Rev: 1A
Date:	Sheet 44 of 46	

PAGE 34
(1) EC C-01 2/20 for LED +3.3V_LED and +5V_LED leak electricity.
PAGE 33
(2) EC C-02 2/20 KBC change to 8502JX Pin12 need add two Cap.
PAGE 40
(3) EC C-03 2/20 Change PC44 footprint.
PAGE 30
(4) EC C-04 2/20 Add Pin.17 and Pin.19 for debug port.
PAGE 24
(5) EC C-05 2/20 Change LID switch to Hall IC.
PAGE 32
(6) EC C-06 2/20 Add C680 for FAN speed issue.
PAGE 15
(7) EC C-07 2/20 Del R465 and Add R237 for SB source.
PAGE 41
(8) EC C-08 2/20 Add leak circuit.
PAGE 27
(9) EC C-09 2/20 Change for new card-reader IC.
PAGE 21
(10) EC C-10 2/20 Change VGA thermal IC to 781-1P8.
PAGE 5
(11) EC C-11 2/20 Change CPU thermal IC to 781-1P8.
PAGE 21
(12) EC C-12 2/20 For M86 HDMI audio issue.
PAGE 37
(13) EC C-13 2/21 For SMT open issue.
PAGE 26
(14) EC C-14 2/21 Footprint for SMT open issue.

NB2/RD1

PROJECT : SA8
Quanta Computer Inc.

Size	Document Number	Rev
B	**Change List Ver.B to Ver.C**	1A
Date:	Sheet 45 of 46	

(01) D1-R241 Delete for AMD request.
PAGE 13
(02) D2-Delete PD3 for power protection.
PAGE 42
(03) D3-Seting Gain value for TGA request.
PAGE 28
(04) D4-4/15 Change driver from MAINON to MAIND; PQ53 P/N from BAM653N0Z03 to BAM48000040
PAGE 39
(05) D5-Change PR13 footprint to 0603
PAGE 38
(06) D6-Change R610 and R612 P/N to CS00003J951
PAGE 17
(07) D7-Change PC148 footprint
PAGE 40
(08) D8-Delete C4 and C5 for HDMI issue.
PAGE 23
(09) D8-Add C808 varistor for ESD issue.
PAGE 28
(10) D10-Add PR76,PR86,PQ24 and PQ25 for LCD flash.
PAGE 41
(11) D11-Signal by pass directly for AMD request.
PAGE 10

Change PR20 value from CS31072FB10 to CS23402FB08.
Change PQ40 value and footprint from BAM48000040 to BAM14140001.
Change PQ45 value and footprint from BAM66900022 to BAM14120000.
Delete PQ46.
Change PL4 PN from DC-15A00010 to CV-15K0MZ05.
Change PR173 value from CS12213F915 to CS11273F928.
PAGE 38 (Power)

Delete PC106 (Don't put it in BOM).
Change PQ53 value and footprint from BAM653N0Z03 to BAM48000040 (Drive net must be "maind").
PAGE 39 (Power)

Change PL9 value from CV-2575TZ51 to DC-33B0M003.
Add a capacitor (CH733RY8802) at Vcore0 output.
Add a capacitor (CH733RY8802) at Vcore1 output.
PC55 and PC145 must use CH733RY8802, don't change them.
Change PR121 value from CS32202FB18 to CS41072FB11.
Change PR117 value from CS41002FB28 to CS31002FB26.
Change PR133 and PR124 value from CS31622FB27 to CS23652FB08.
Delete PR132 and PR123 (Don't put it in BOM).
PAGE 40 (Power)

Change PR51 and PR52 value from CS00002JB38 to CS21002JB34.
Add a capacitor (CH14706KB18) at PQ20 pin2.
Add a capacitor (CH14706KB18) at PQ19 pin2.
Change PQ20 and PQ19 pin1 from GND to 8118agnd.
Change PR54 value from CS46043F901 to CS43303F912.
Change PR53 value from CS43323F911 to CS42103F900.
Change PR58 value from CS41473F912 to CS38253F913.
Change PR57 value from CS41003F932 to CS35493F911.
Change PR55 value from CS36342FB11 to CS00002JB38.
Delete PR56 (Don't put it in BOM)
Change PR64 value from CS31102FB11 to CS41002FB28.
Change PR63 value from CS41912FB17 to CS45112FB19.
Change PC57 value from CH33302KB12 to CH24704KB19.
Change PR186 value from CS34992FB10 to CS25602FB19 (This component must put in BOM).
Change PR59 to connect to PR63.
PAGE 42 (Power)

(12) D12-Add R115,R120 Reserve for AMD requement.
PAGE 23
(13) D13-Add C828,C829,C830,C831,C832 Reserve for +VGA_CORE Power.
PAGE 18
(14) D14-Change PR54 value from CS43303F912 to CS41503F914 for SA8 MP.
PAGE 42 (Power)
(15) E1-Change C804,C805,C793,C794 value from CH23904KB13 to CH31006KB18
for blue screen 0xEA issue.
PAGE 29
(16) E2-Change U16,R344,R342 to no stuff.
PAGE 26
(17) E3-Change R241 to ASM.
PAGE 13
(18) E4-Change R15,R16,R17,R18 Footprint from 0402 to 0603.
PAGE 26
(19) E5-Change PU1 P/N from AL008204000 to AL008204001.
PAGE 26
(20) F1-PQ53 pin4 change to PQ29 pin 3 for power sequence issue.
PAGE 39
(21) F2-PQ28 pin 2 connect to U35 pin 33(T172) for power sequence issue.
PAGE 33,41
(22) F3-Delete PR83 for power sequence issue.
PAGE 41
(23) F4-Change PR19 from 0 ohm to 20K ohm and PR189 From 10K to 20K ohm.
PAGE 38,42
(24) F5-Change PC12,PC154 from no stuff to 0.22U.
PAGE 38,42
(25) F6-Add PC79 for power sequence issue.
PAGE 41
(26) F7-DELETE HOLE29.
PAGE 43
(27) F8-DELETE R122,R356 0 ohm.
PAGE 25
(28) F9-DELETE R286,R289 0 ohm.
PAGE 6
(29) F10-DELETE R158,R160,R165,R383,R382,R117,R121,R374,R377,R601,R602,R104,R112 0 ohm
PAGE 10
(30) F11-DELETE R416,R518 0 ohm
PAGE 12
(31) F12-DELETE R255,R254,R242,R258,R474 0 ohm
PAGE 13
(32) F13-DELETE R184,R422 0 ohm
PAGE 14
(33) F14-DELETE R41 0 ohm
PAGE 18
(34) F15-DELETE R40,R42,R43 0 ohm
PAGE 18
(35) F16-DELETE L2,L3 0 ohm
PAGE 23
(36) F17-DELETE C601,R363,R364
PAGE 24
(37) F18-DELETE R482 0 ohm
PAGE 28
(38) F19-DELETE L82 0 ohm
PAGE 29
(39) F20-DELETE R502,R503,R507,R509,R534,R536 0 ohm
PAGE 30
(40) F21-DELETE R267,R268 0 ohm
PAGE 31
(41) F22-DELETE R538,R540 0 ohm
PAGE 31
(42) F23-DELETE R552 0 ohm
PAGE 33
(43) F24-DELETE R307,R308 0 ohm
PAGE 34
(44) F25-DELETE R402,R403 0 ohm
PAGE 35
(45) F26-Add R618 pull low for PCB Rev: F
PAGE 33
(46) F27-DELETE RP50,RP49,RP48,RP52,RP51,RP47,RP46,RP43,RP44,RP45 0 ohm
PAGE 02
(47) F28-Change R15,R16,R17,R18 Footprint from 0603 to 0805.
PAGE 26

(48) F29-Change R311,R313,R312 from no stuff to 180ohm for EMI.
PAGE 23
(50) F30-PR30,PR34,PR44,PR45,PR46 change from 0Ω to short pad.
PAGE 37
(51) F31-PR10 change from 0Ω to short pad.
PAGE 38
(52) F32-Add PC6 (100P/50V/NPO_4)
PAGE 38
(53) F33-Delete PC120, PC121
PAGE 38
(54) F34-PR161 change from 0Ω to short pad.
PAGE 39
(55) F35-PR110 change from 0Ω to short pad.
PAGE 40
(56) F36-PR69 change from 0Ω to short pad.
PAGE 42
(57) F37-Delete PR51, PR52, PC202, PC203
PAGE 42
(58) F38-
PAGE
(59) F39-
PAGE
(60) F40-
PAGE
(61) F41-
PAGE

NB2/RD1

PROJECT : SA8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Change List Ver.C to MP	1A
Date:	Sheet 46 of 45	