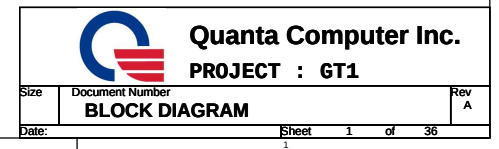


1



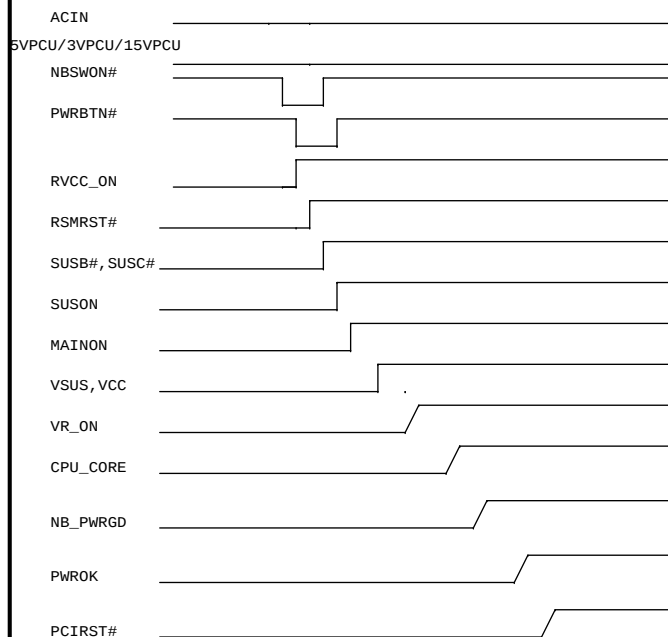
Voltage Rails

Power	Voltage	S0~S2	S3	S4	S5	Ctl Signal
15VPCU	15V	V	V	V	V	
5VPCU	5V	V	V	V	V	
3VPCU	3V	V	V	V	V	
VCCRTC	3V	V	V	V	V	
+3.3VALW	3V	V	V	V	V	STB_ON_D
+1.2VALW	1.2V	V	V	V	V	STB_ON
5VSUS	5V	V	V			SUSON
3VSUS	3V	V	V			SUSON
1.8VSUS	1.8V	V	V			SUSON
SMDDR_VTERM	0.9V	V				SUSON
VCC5	5V	V				MAINON
VCC3	3V	V				MAINON
VCC1.8	1.8V	V				MAINON
VCC1.5	1.5V	V				MAINON
VCC1.2	1.2V	V				MAINON
VLDT_RUN	1.2V	V				VLDT_ON_D
CPU_VCCA	2.5V	V				MAINON
CPU_CORE	0.9V	V				VRON

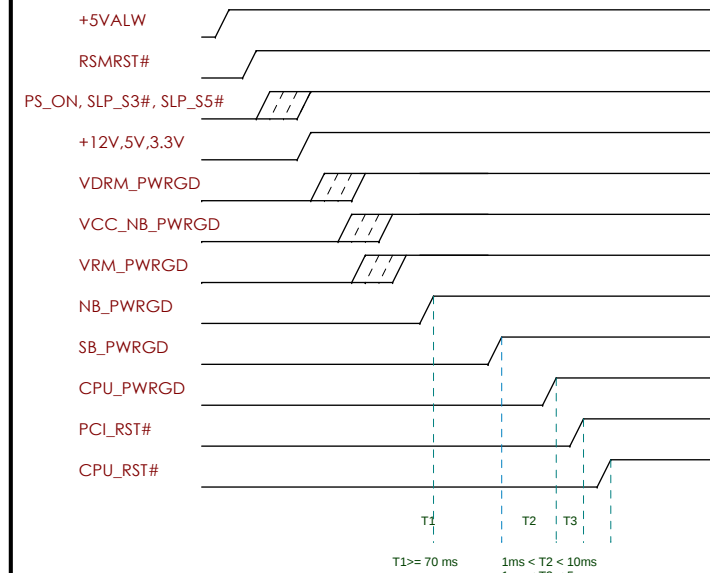
PCI DEVICES IRQ ROUTING

PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts	CLK
NB(RS690)	NA	NA	NA	NA
SB(SB600)	DEVSEL#	REQ0#/GNT0#	INTE#	PCICLK0
R5C833	IDSEL	REQ#/GNT#	INTA#/INTB#	PCICLK

Power On Sequence



BONEFISH POWER UP SEQUENCE

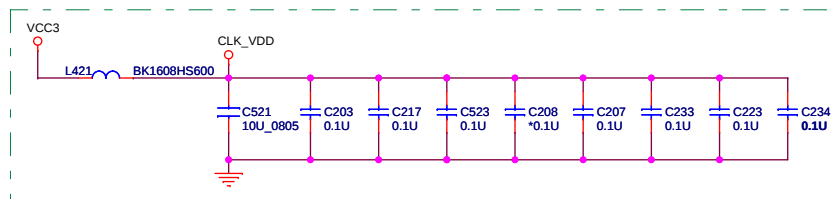


PCB STACK UP

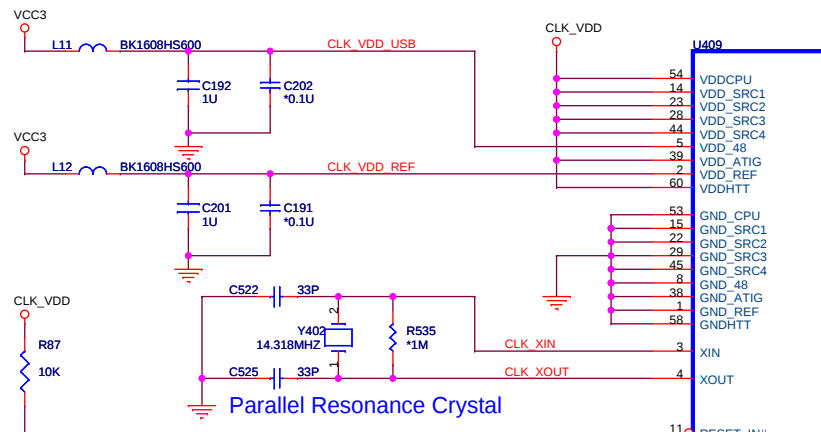
LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT



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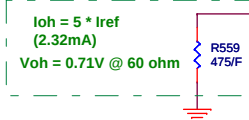


Put Decoupling Caps close to Clock Fen. power pin



Parallel Resonance Crystal

(8.15) SCLK0
(8.15) SDATA0

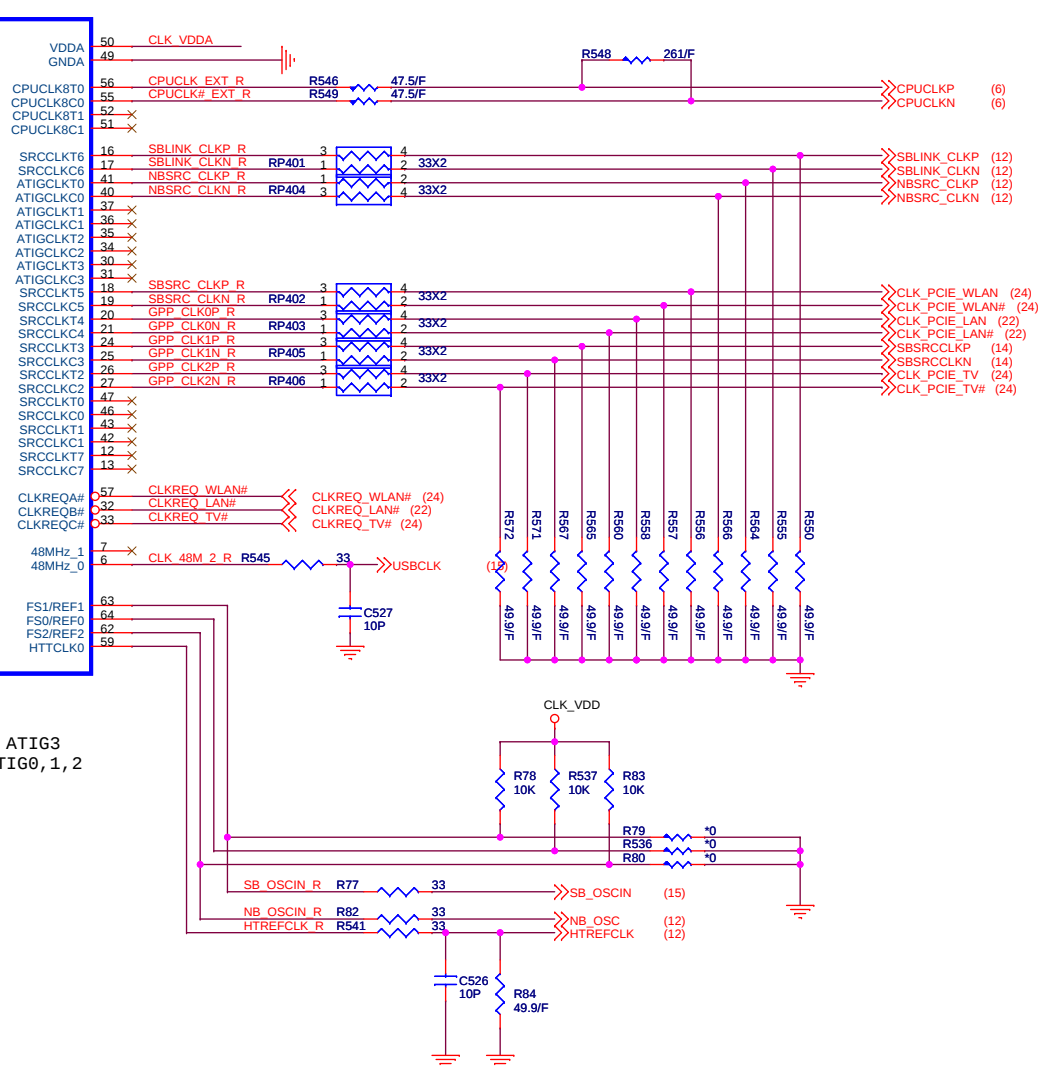
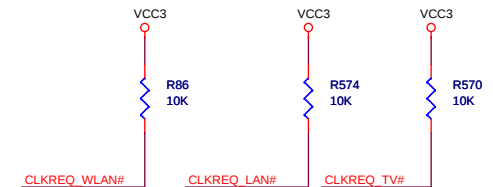
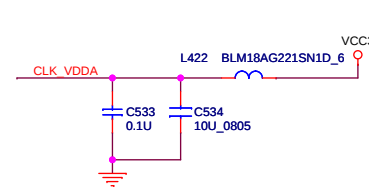


CLKREQA# CONTROL SRC5,6,7
CLKREQB# CONTROL SRC2,3,4 ATIG3
CLKREQC# CONTROL SRC0,1 ATIG0,1,2

EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

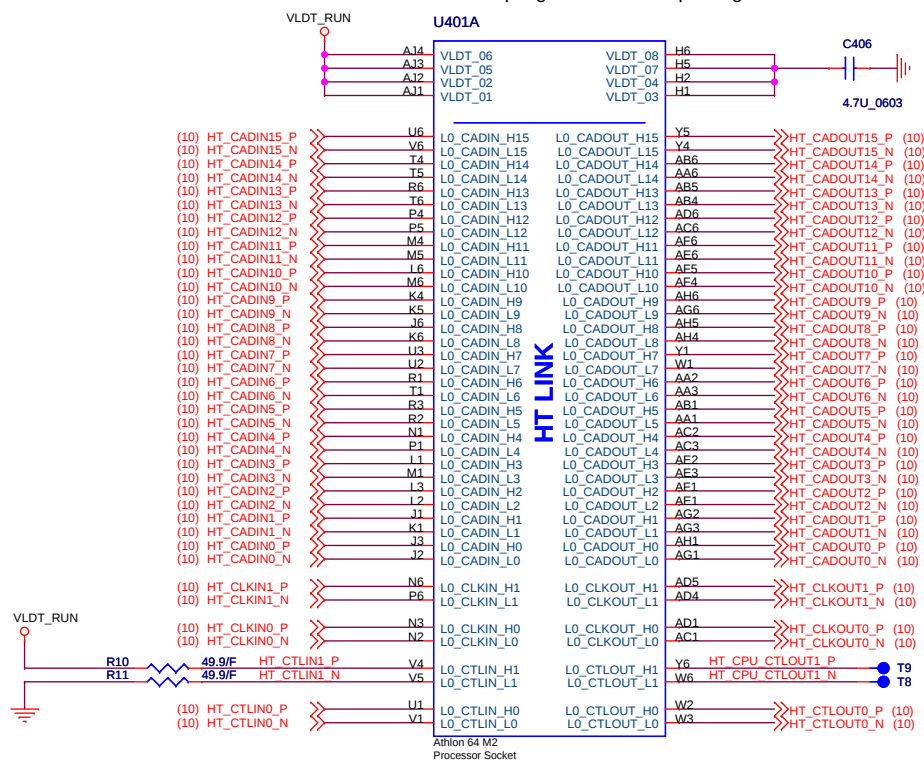
Check AMD clock



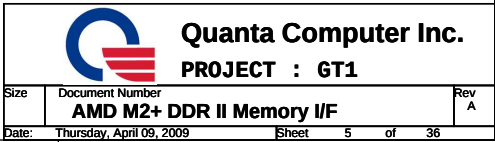
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CPU HyperTransport Interface

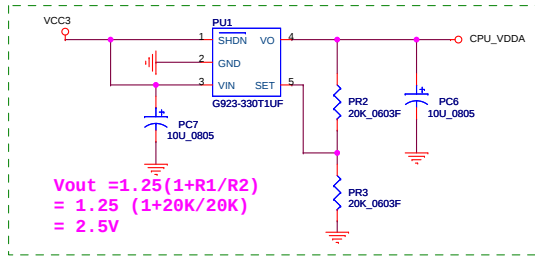
VDDLDTRUNCPU is connected to the VDD_LDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.



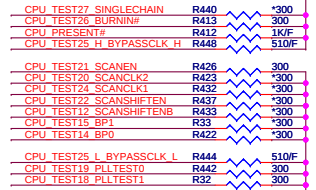
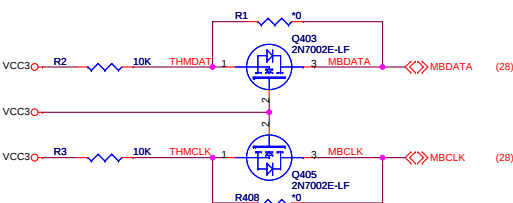
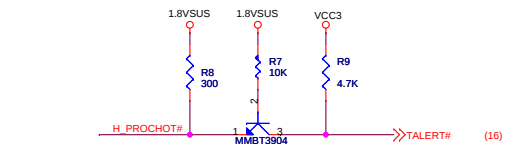
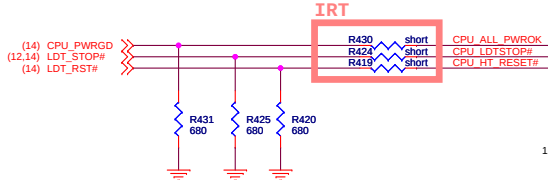
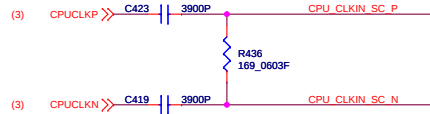
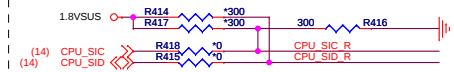
5



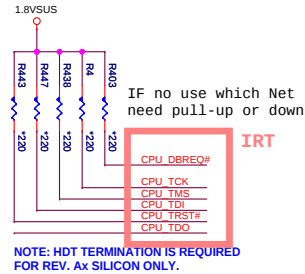
ATHLON Control and Debug



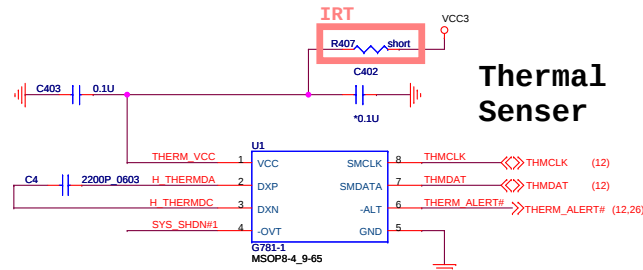
If AMD SI is not used, the SID pin can be left unconnected and SIC should have a 300Ω (±5%) pull-down to VSS.



HDT Test Point

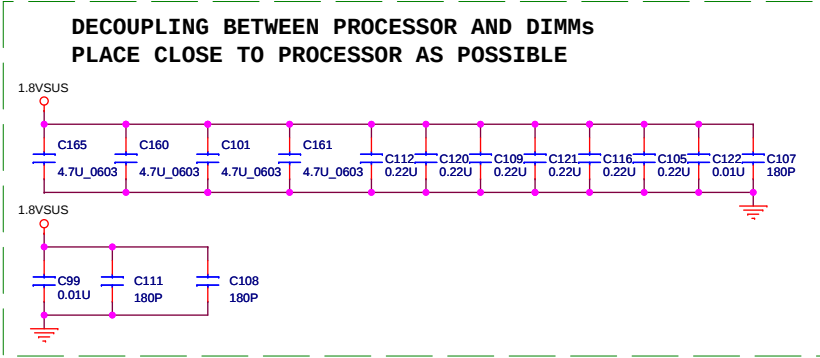
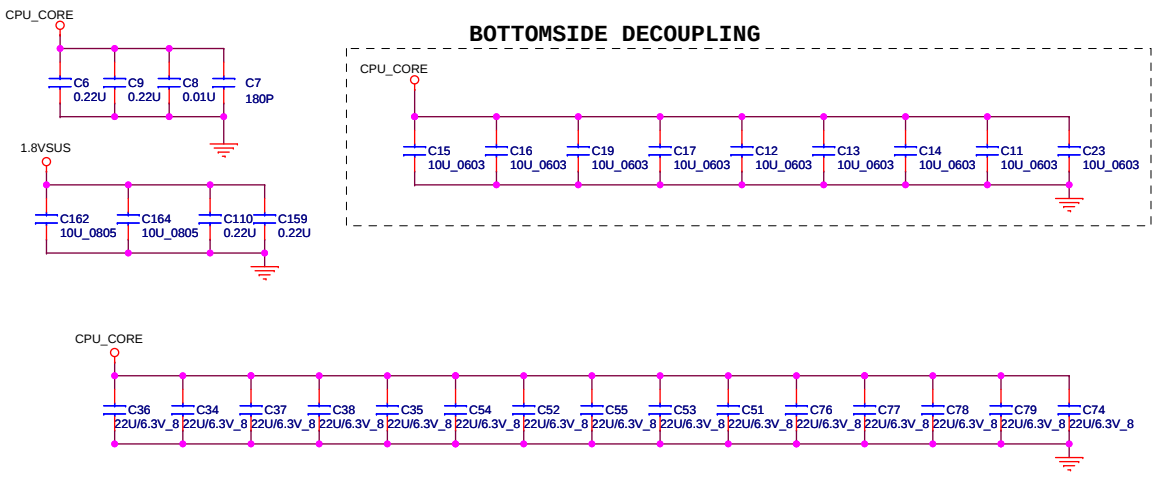
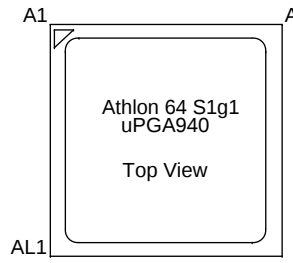
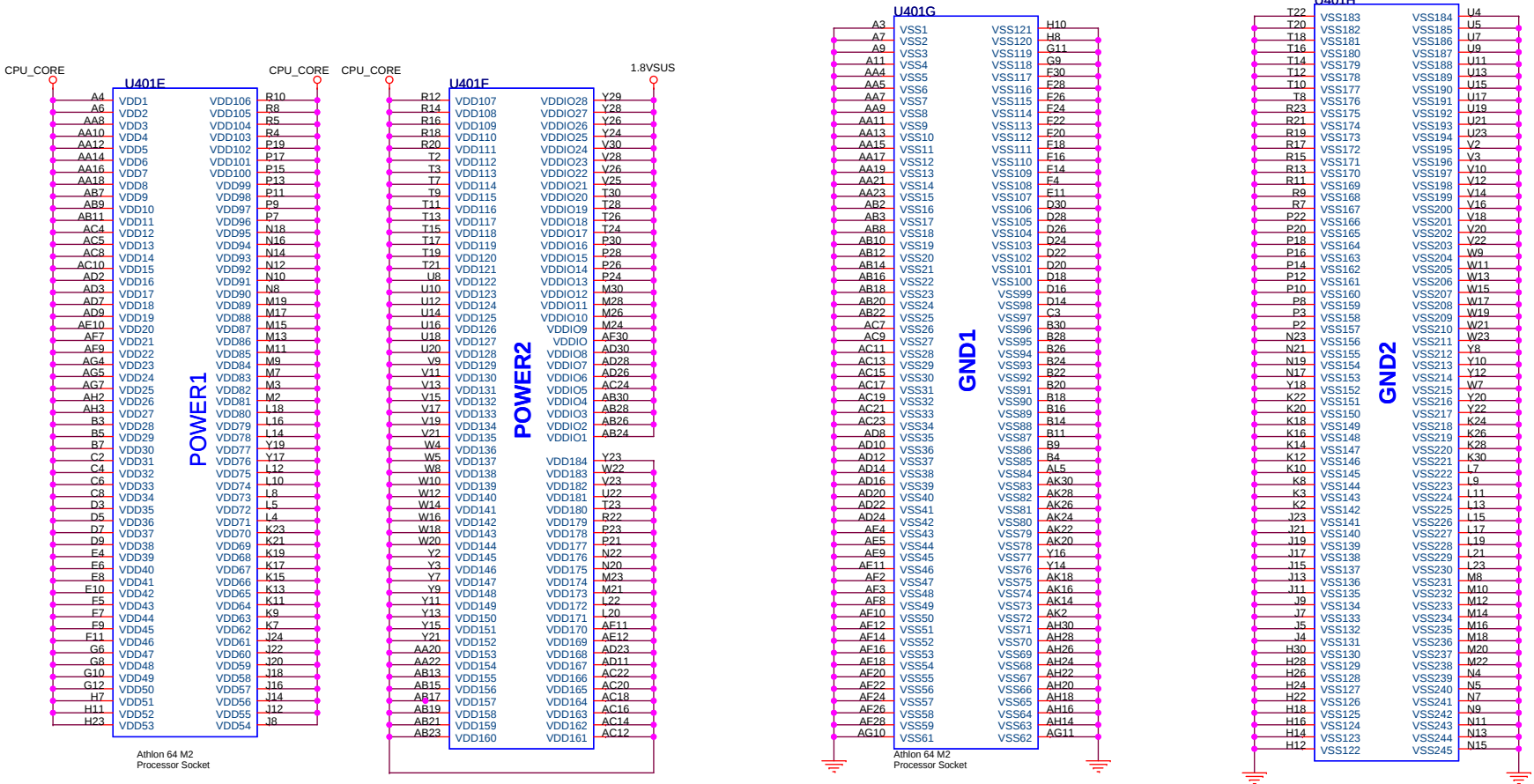


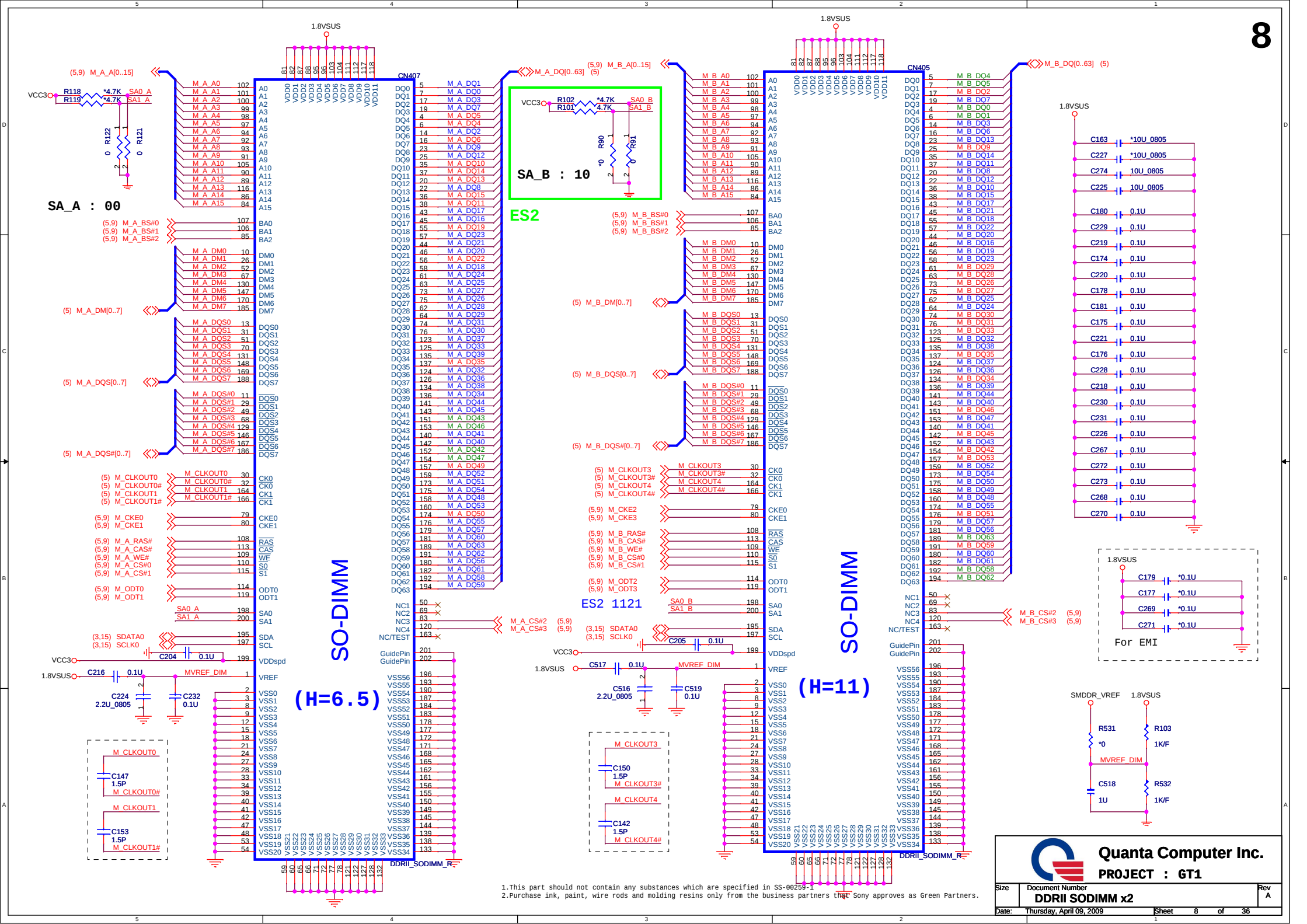
Thermal Sensor

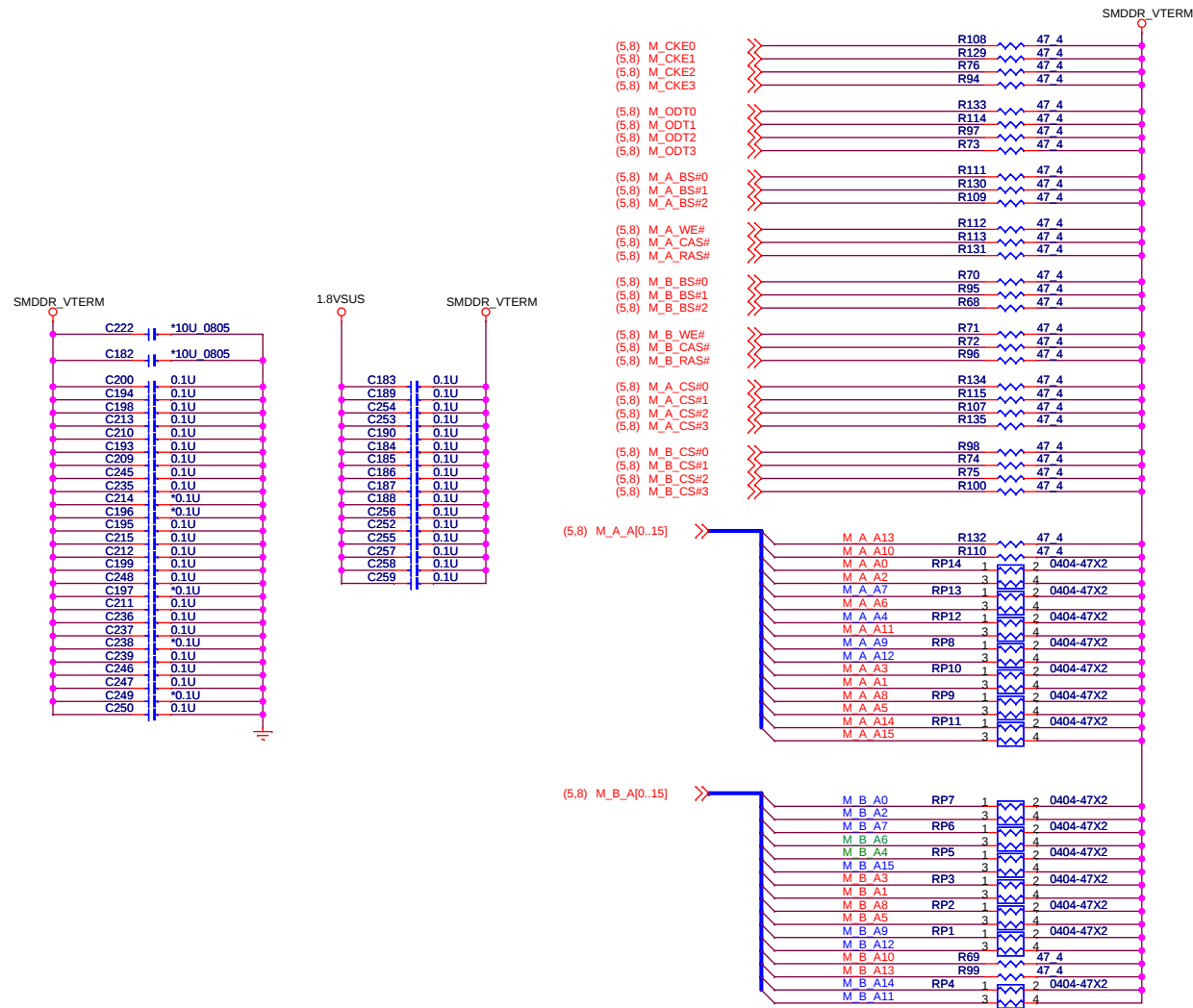


SMBUS SLAVE ADDRESS	
G781	98 (NB)
G781-1	9A (CPU)

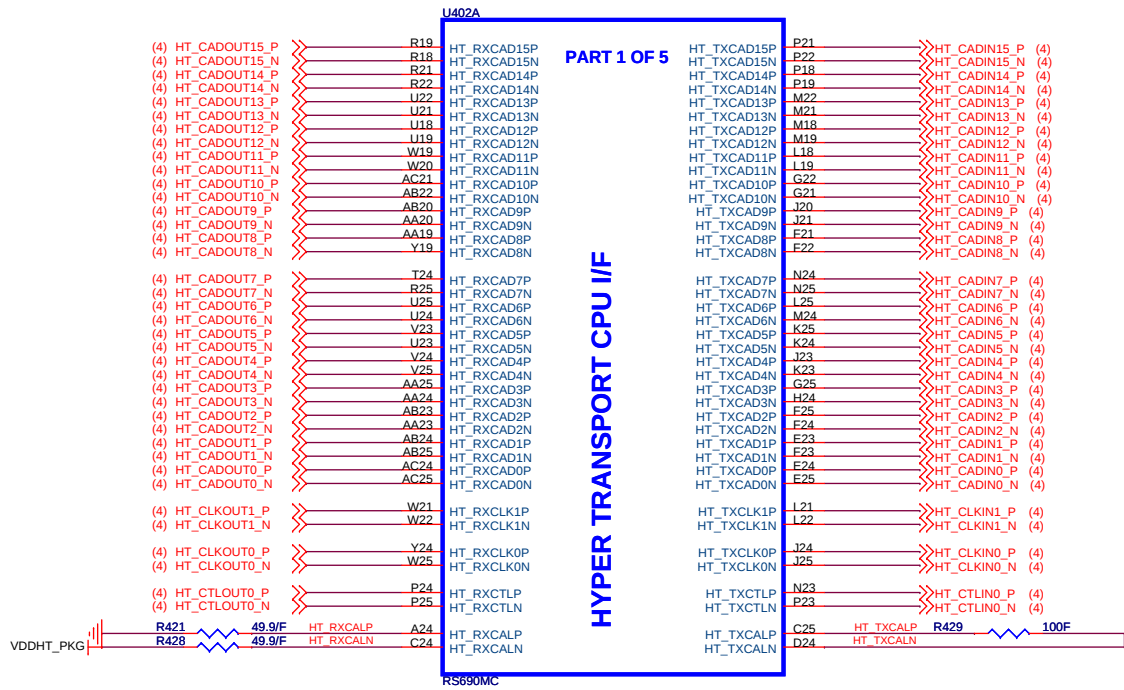
PROCESSOR POWER AND GROUND

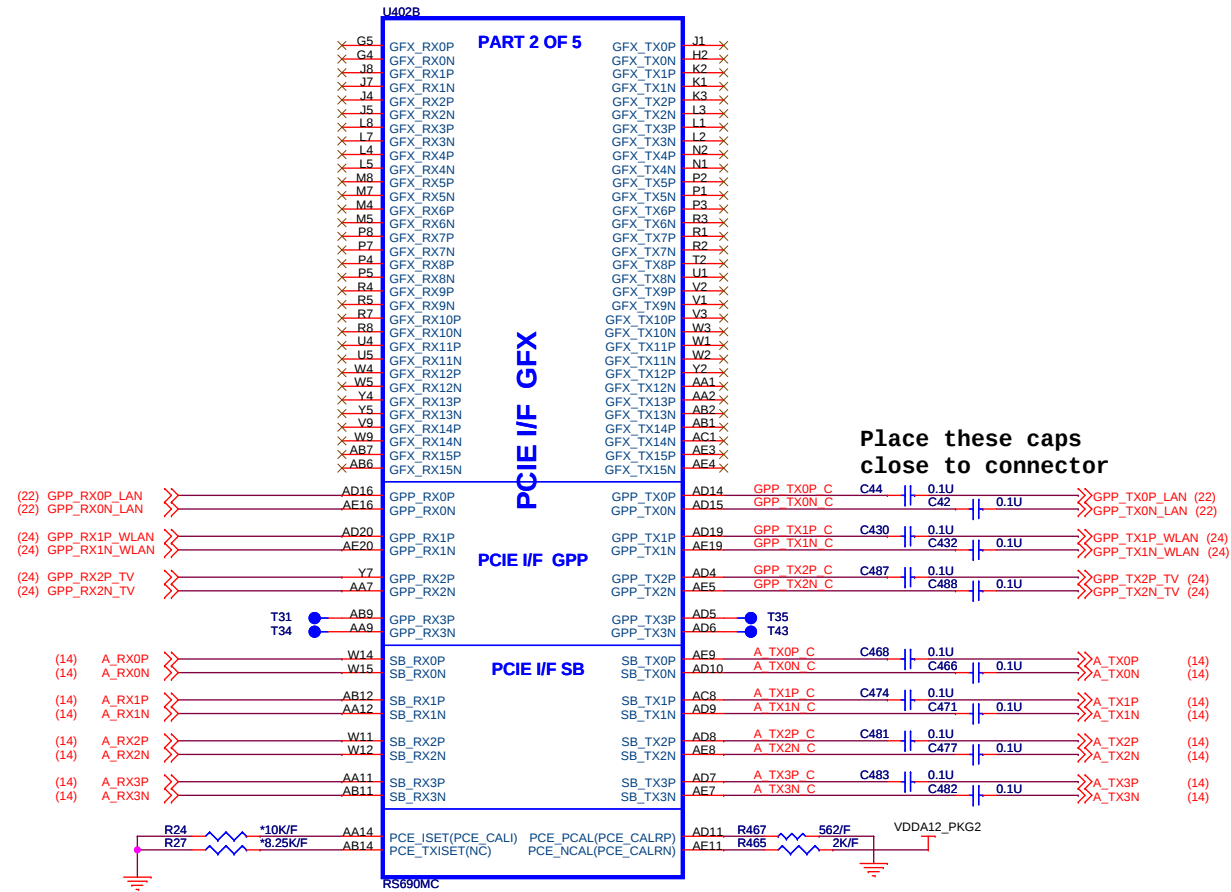


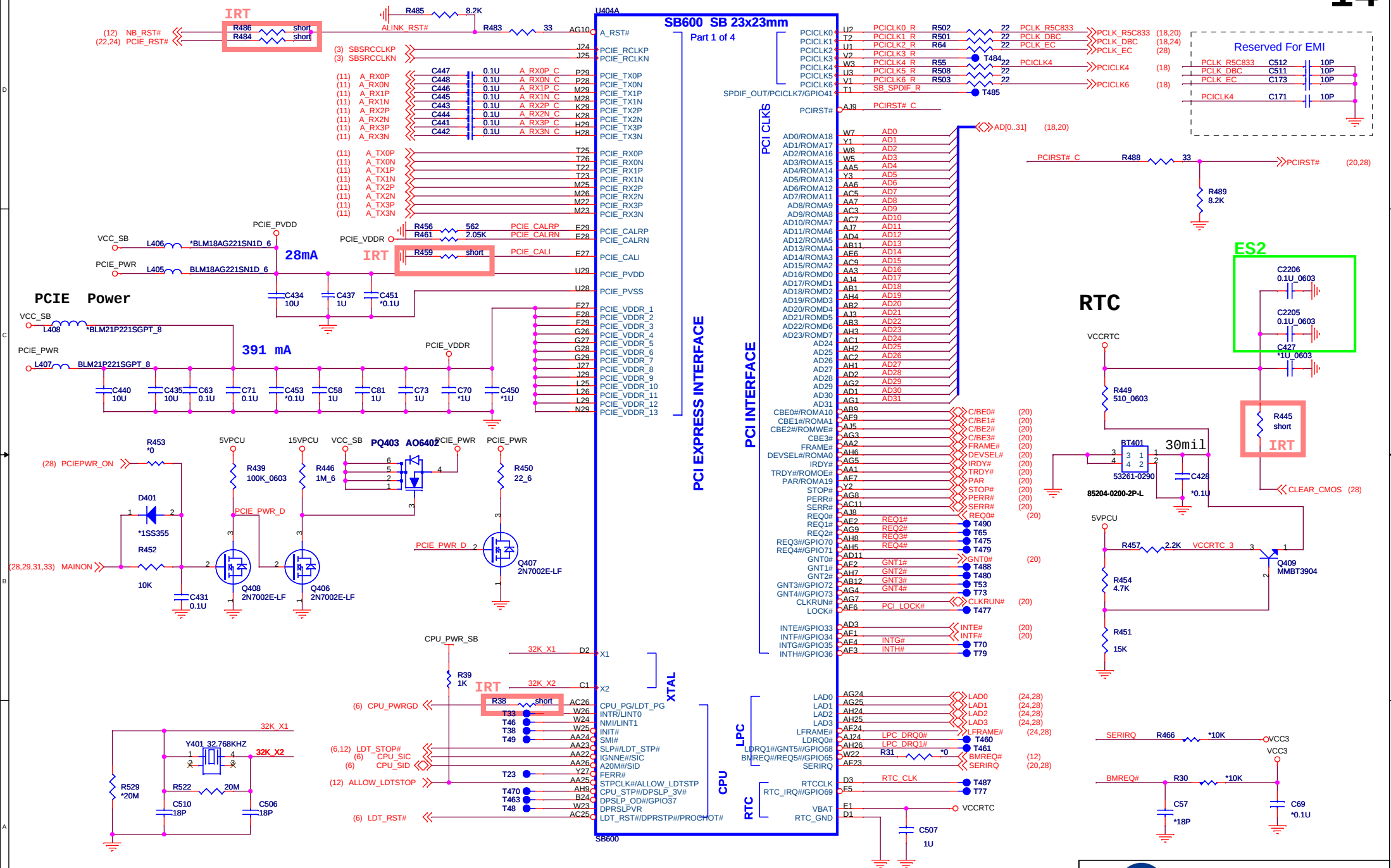


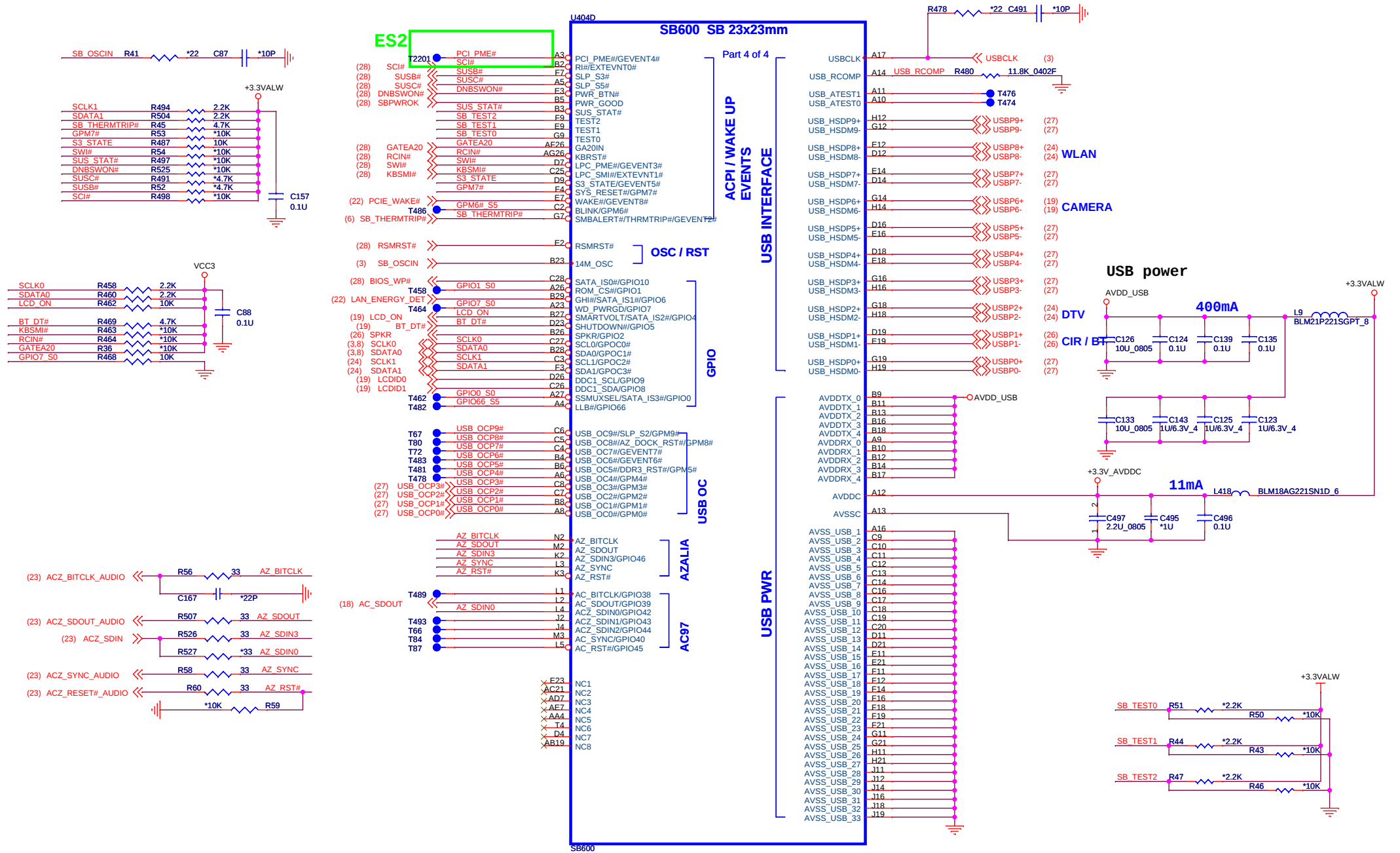


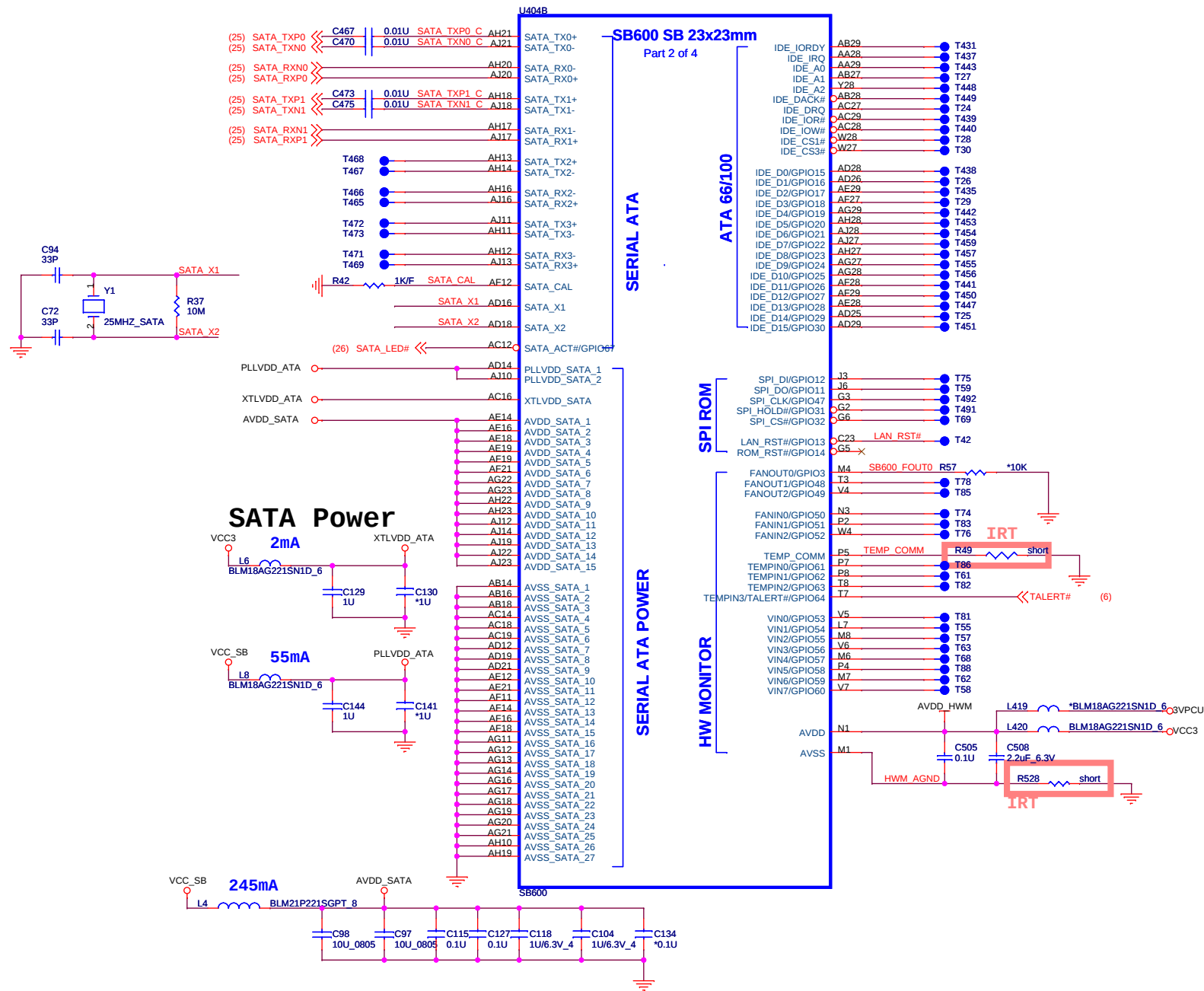
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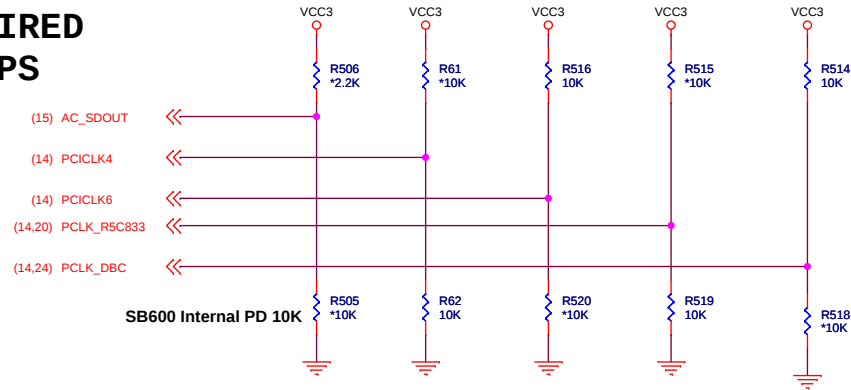






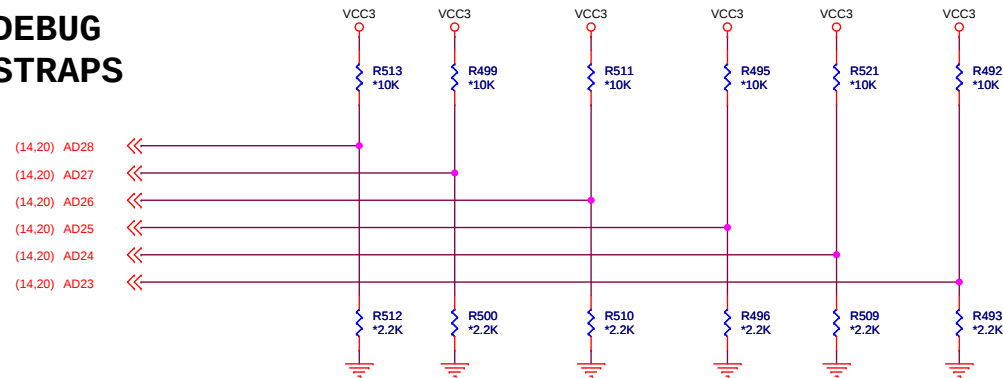
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REQUIRED STRAPS



				PCLK_R5C833	PCLK_DBC
	AC_SDOUT	PCICLK4	PCICLK6	PCI_CLK0	PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM	DEFAULT
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	USE EXT. 48MHZ DEFAULT	CPU IF=P4		

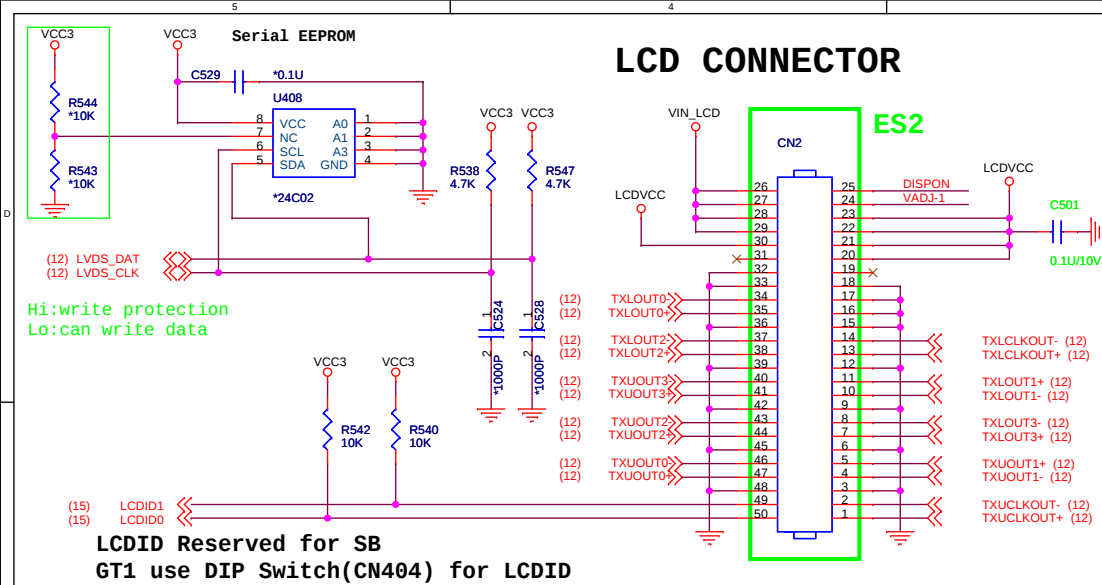
DEBUG STRAPS



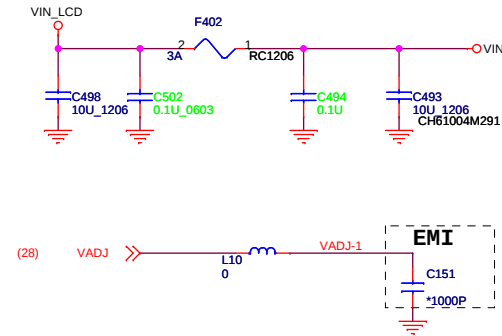
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOTFAILTIMER DISABLED DEFAULT
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED



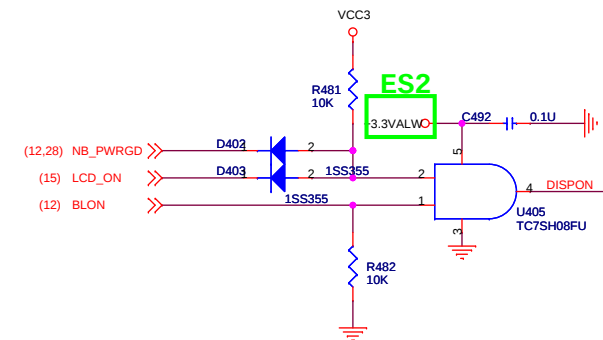
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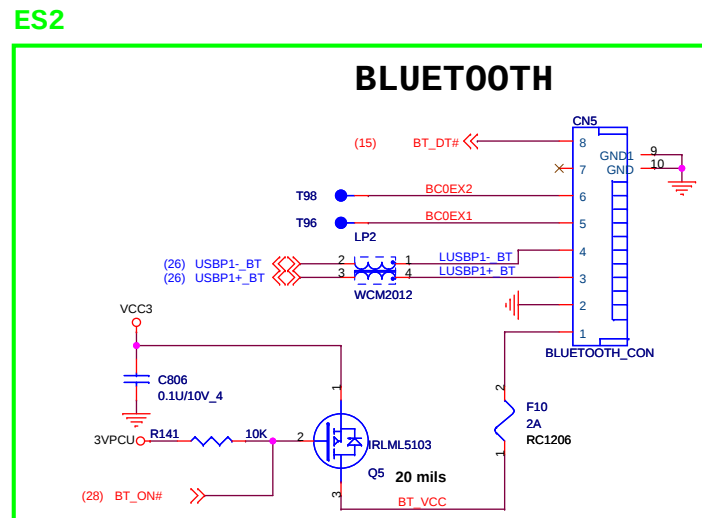
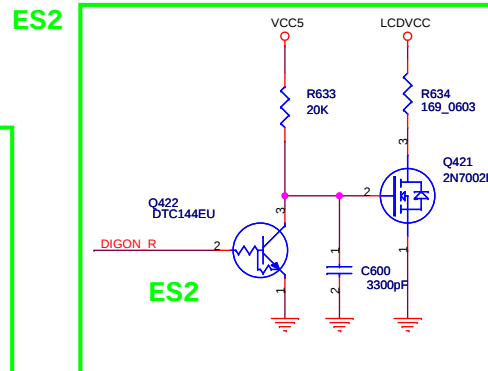
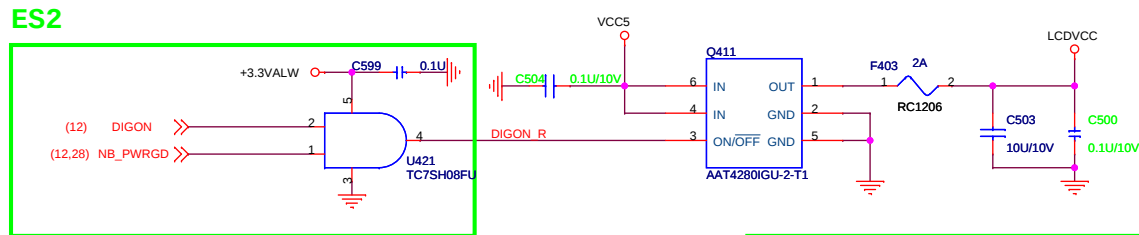
INVERTER POWER



BACKLIGHT CONTROL

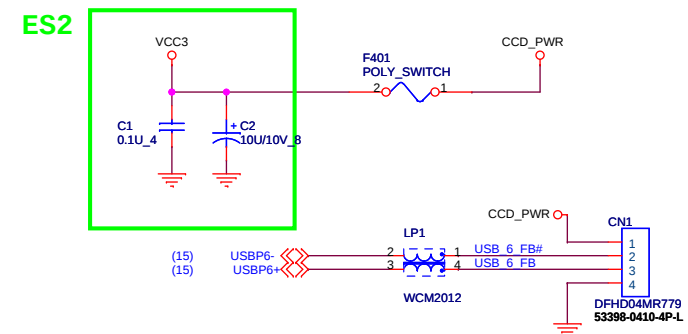


PANEL VCC CONTROL



BT_ON#	High	low
	No device	Bluetooth IN

CAMERA



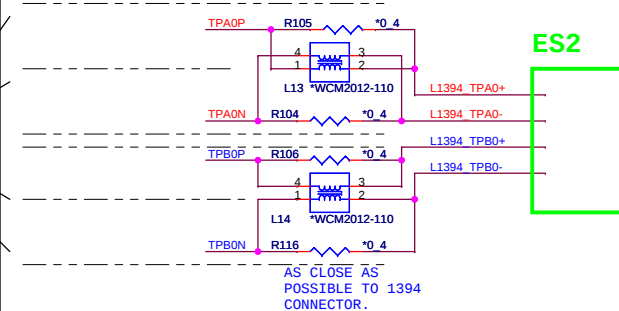
PCI Routing

AD24

INTE# , INTF#

REQ0#,GNT0#

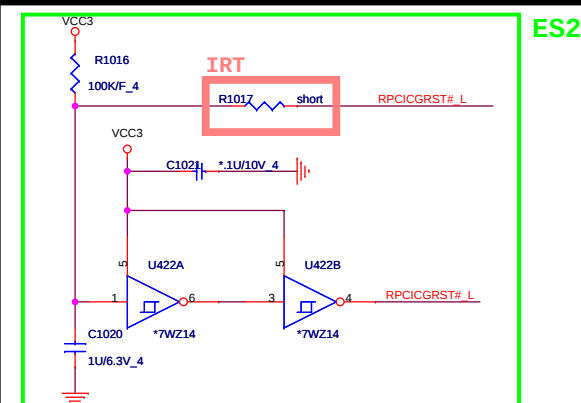
1394 Reserved for Debug only



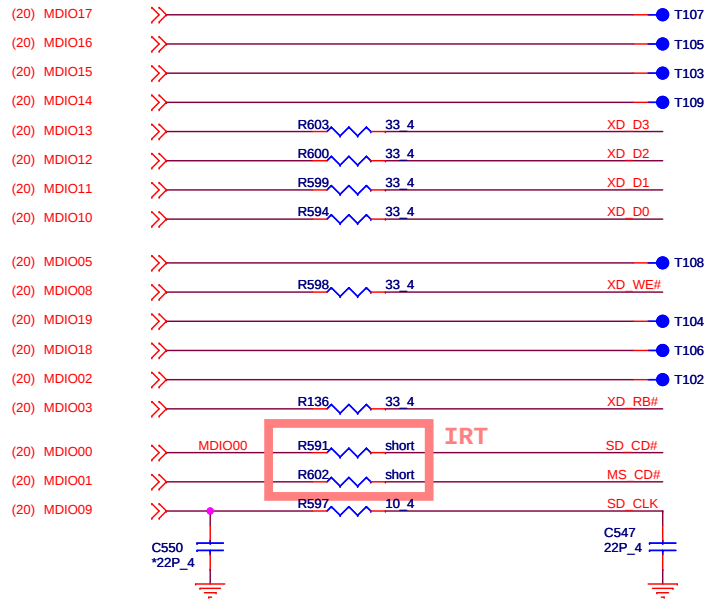
*TPA/TPA#,TPB/TPB# pair trace : As close as possible.

*TPA/TPA#,TPB/TPB# pair trace : Same length electrically.And layot with shields.

*Termination resistor for TPA+/- TPB+/- : As close as possible to its cable driver (device pin out).

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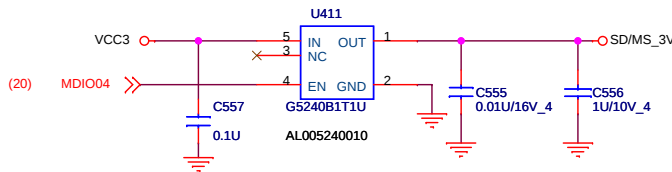
PROJECT : GT1



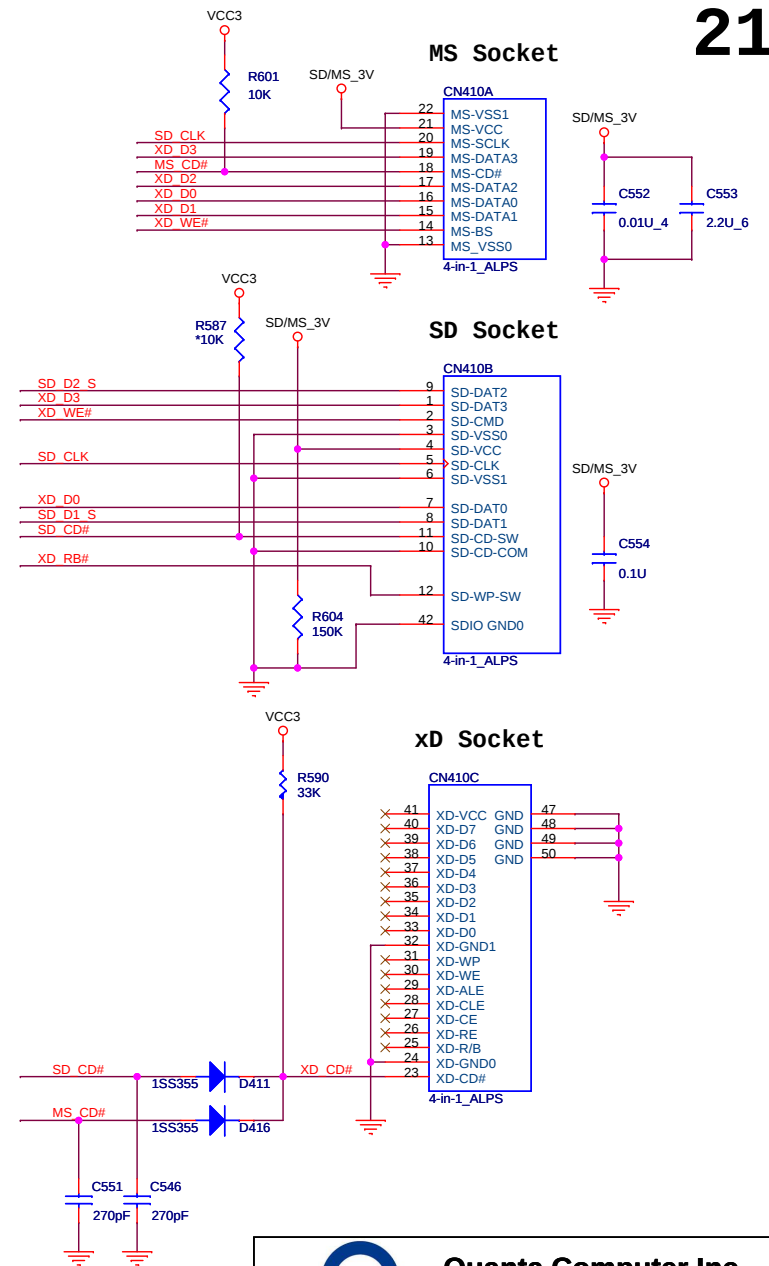
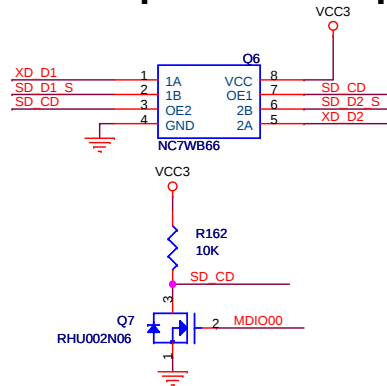
Card Detect

	MDIO00	MDIO01
SD/MMC	L	H
MS	H	L

Flash Card Power SW

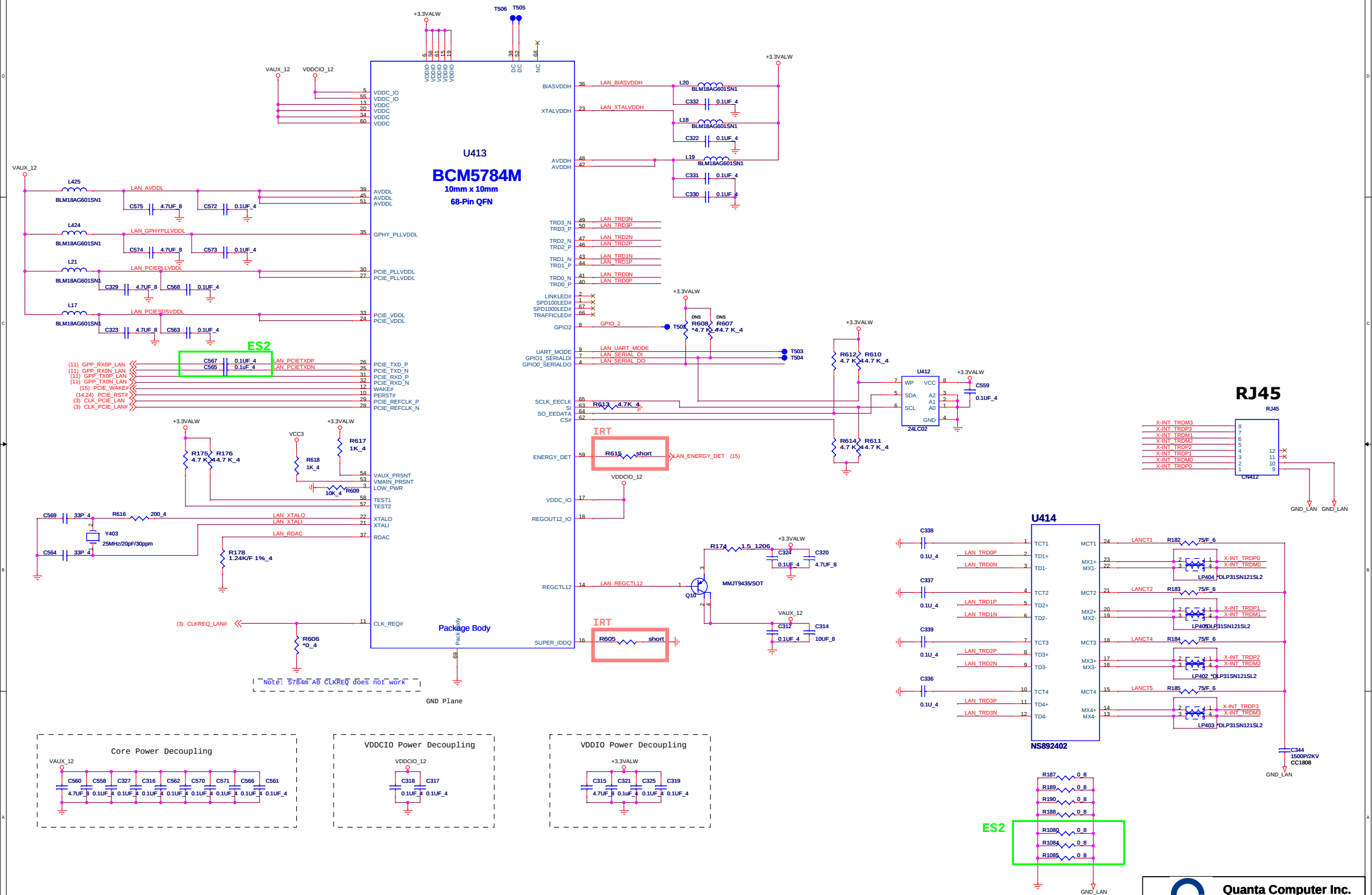


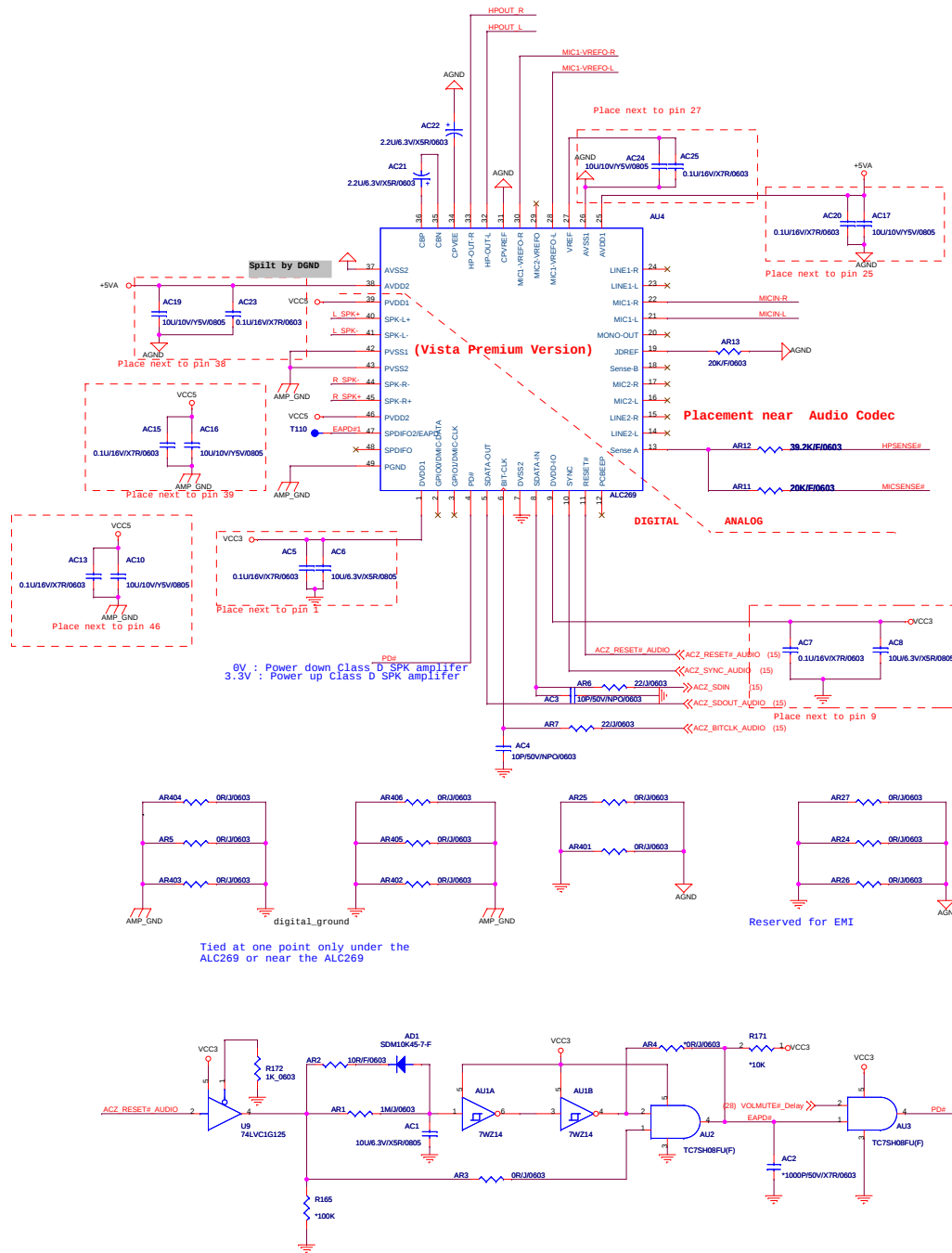
MSDuo pin short protect



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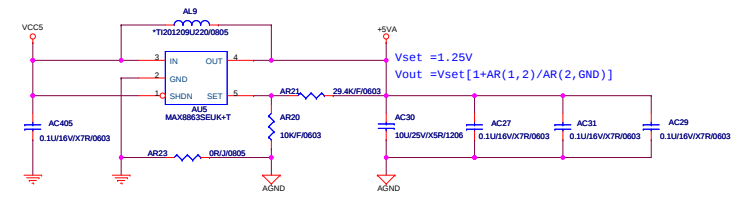
Size	Document Number	Rev
	Card Reader CONN	A
Date:	Thursday, April 09, 2009	Sheet 21 of 36



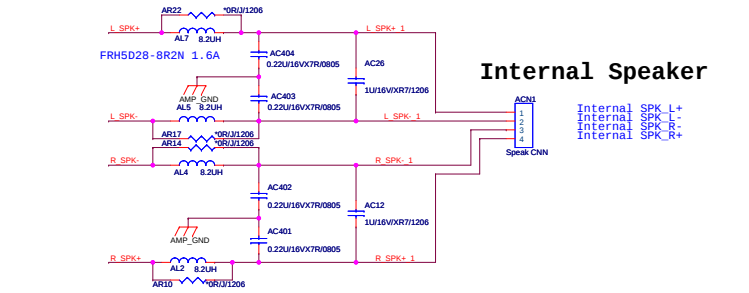


Demodulation Filter

Place close to Codec

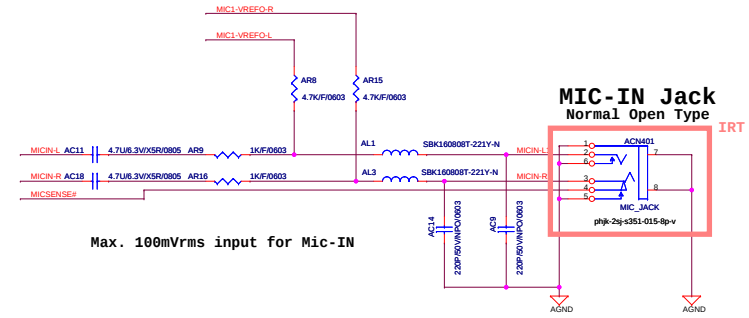


Internal Speaker



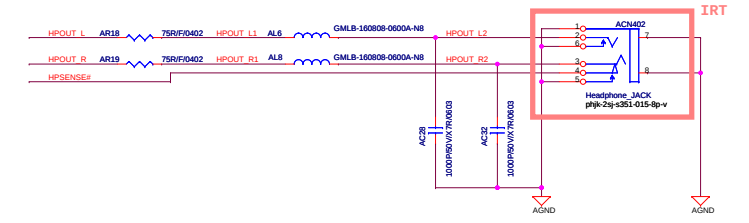
MIC-IN Jack

Normal Open Type



Headphone-OUT

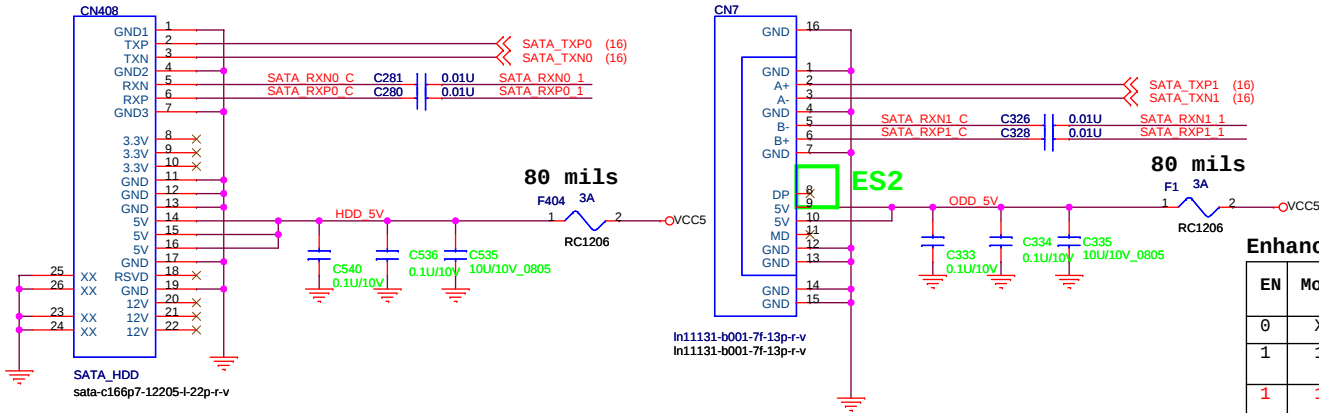
Normal Open Type



SATA HDD

SATA ODD

25



Standard mode

EN	Mode	B_EM	A_EM	Output B	Output A	Input B	Input A
0	X	X	X	Disable	Disable	Disable	Disable
1	0	0	0	0dB	0dB	2.5dB	2.5dB
1	0	0	1	0dB	3dB	2.5dB	2.5dB
1	0	1	0	3dB	0dB	2.5dB	2.5dB
1	0	1	1	3dB	3dB	2.5dB	2.5dB

Enhanced mode

EN	Mode	x_EN#	x_EQ	Input X Equalization	x_EM	Output X Emphasis	Function
0	X	X	X	n/a	X	n/a	chip power down
1	1	1	X	n/a	X	n/a	chip enabled Channel x disabled
1	1	0	0	2.5dB	1.5K-20K resistor	resistor controlled (table A)	chip and channel enabled, low input equalization
1	1	0	1	6.5dB	1.5K-20K resistor	resistor controlled (table A)	chip and channel enabled, low input equalization

SATA Re-driver IC

(Default---PI3EQX4951B Enhanced mode, Emphasis is +3dB)

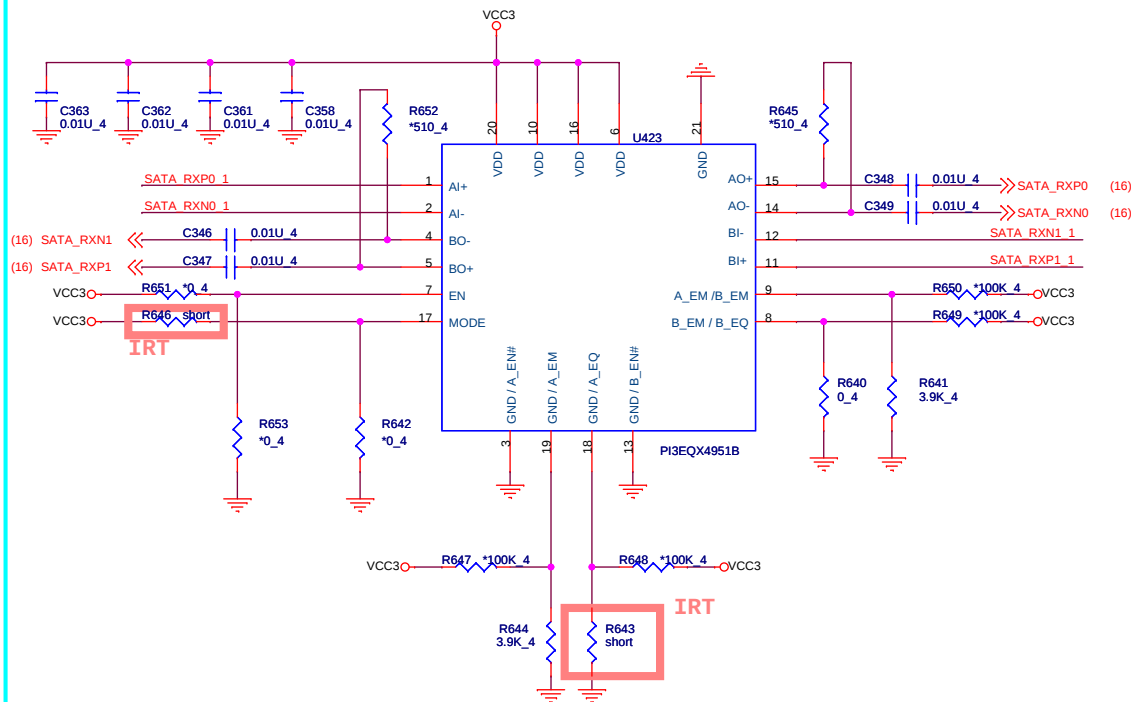


table A

Pre-emphasis	R_EX(K-Ohm)
0dB	Do Not Connect
+1.5dB	6.98
+2.0dB	5.76
+2.5dB	4.7
+3.0dB	3.9
+3.5dB	3.4
+4.0dB	2.94
+4.5dB	2.49
+5.0dB	2.21
+5.5dB	1.91
+6.0dB	1.69

table B

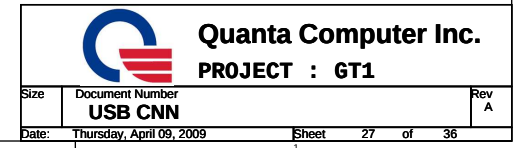
	Standard mode	Enhanced mode	MAX4951(Boost)
R640	NC	0 ohm	NC
R641	NC	3.9K	NC
R642	0 ohm	NC	0 ohm
R643	0 ohm	0 ohm	0 ohm
R644	0 ohm	3.9K	0 ohm
R645	NC	NC	NC
R646	NC	0 ohm	NC
R647	NC	NC	NC
R648	NC	NC	NC
R649	100K ohm	NC	100K ohm
R650	100K ohm	NC	100K ohm
R651	NC	NC	100K ohm
R652	NC	NC	NC
R653	NC	NC	NC

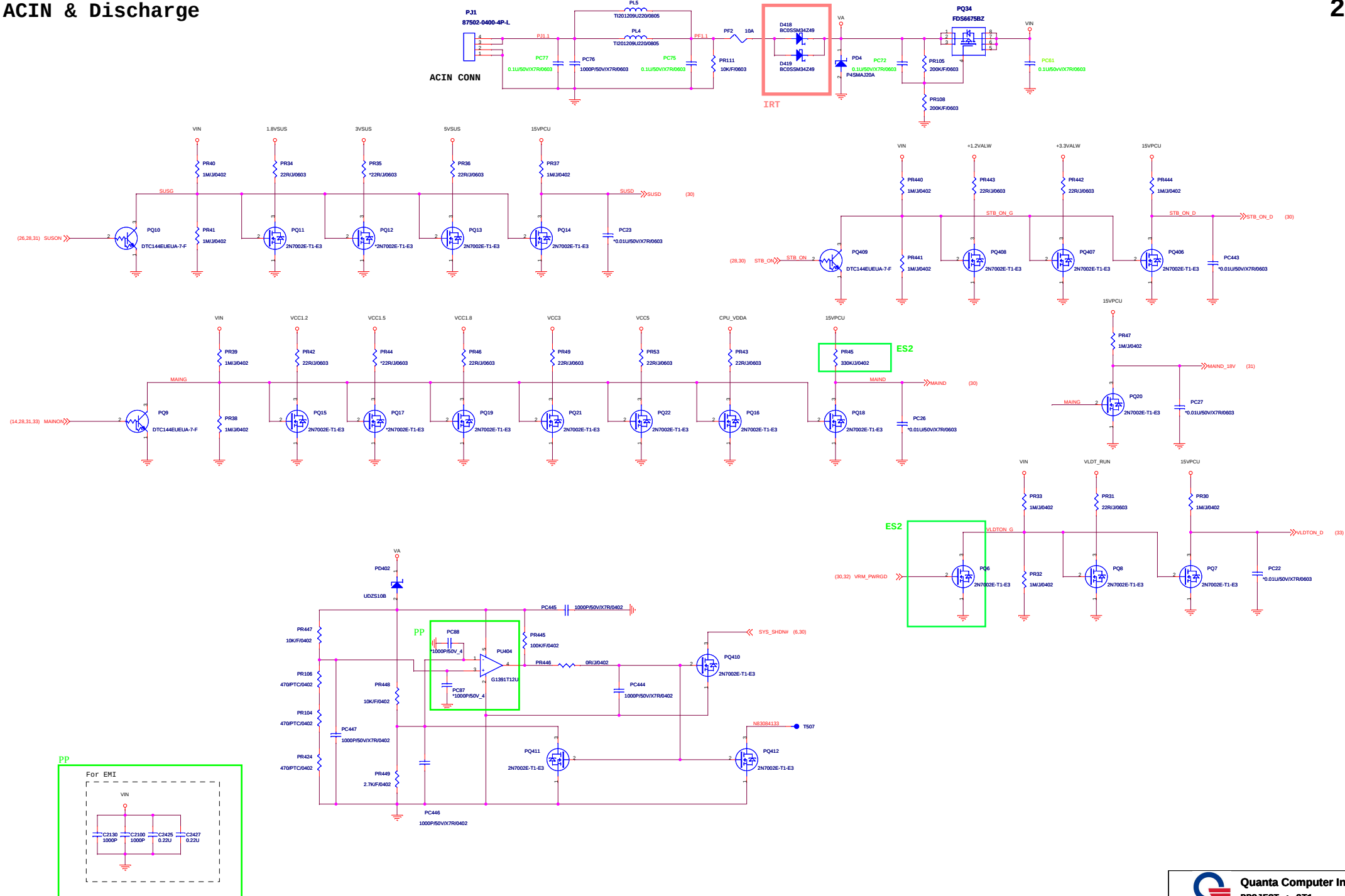
MAX4951

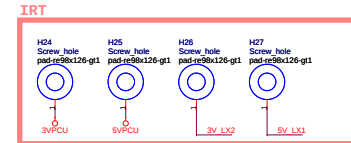
EN	A_EM	B_EM	Output A	Output B
0	X	X	Standby	Standby
1	0	0	Standard SATA	Standard SATA
1	1	0	Boost	Standard SATA
1	0	1	Standard SATA	Boost
1	1	1	Boost	Boost

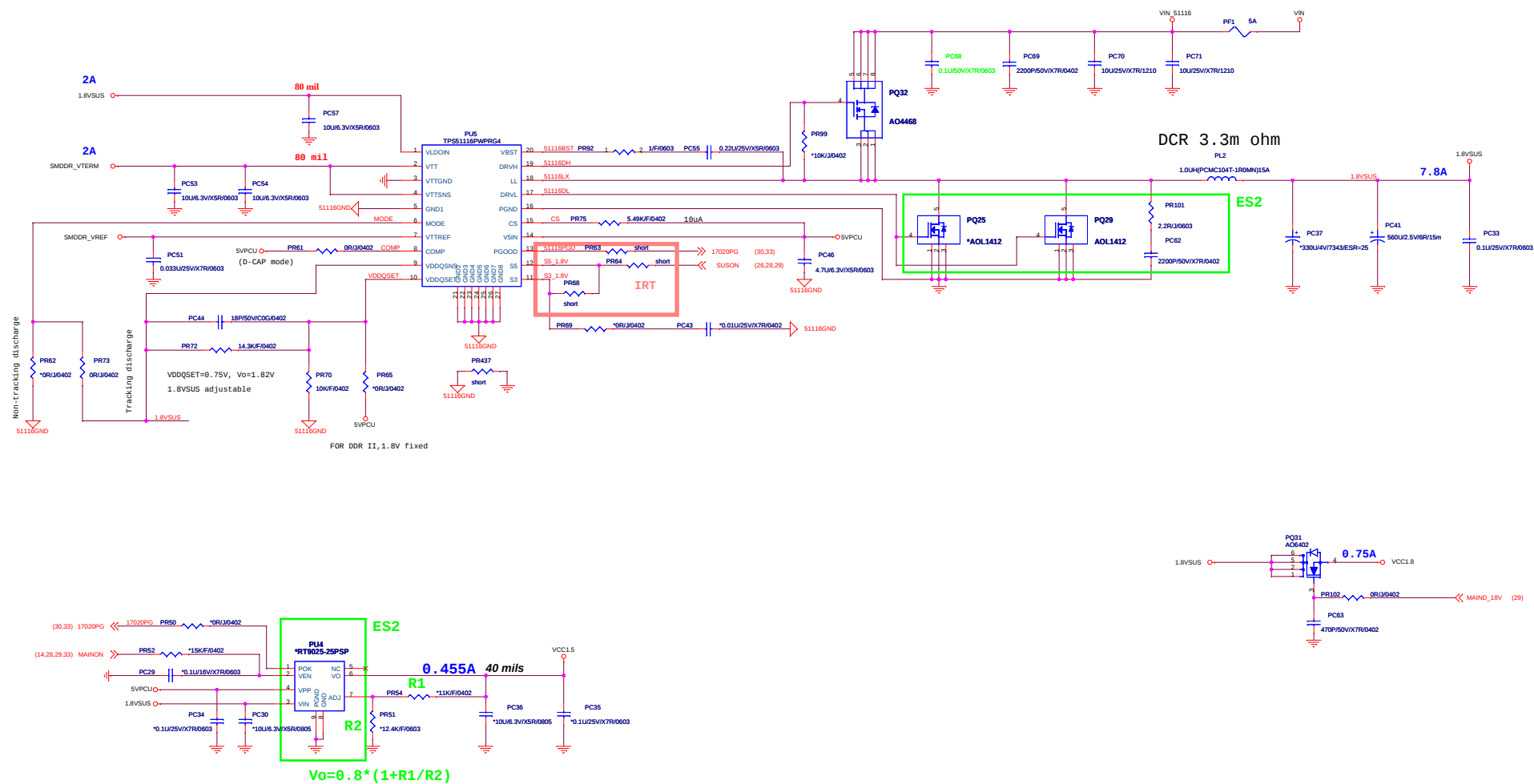


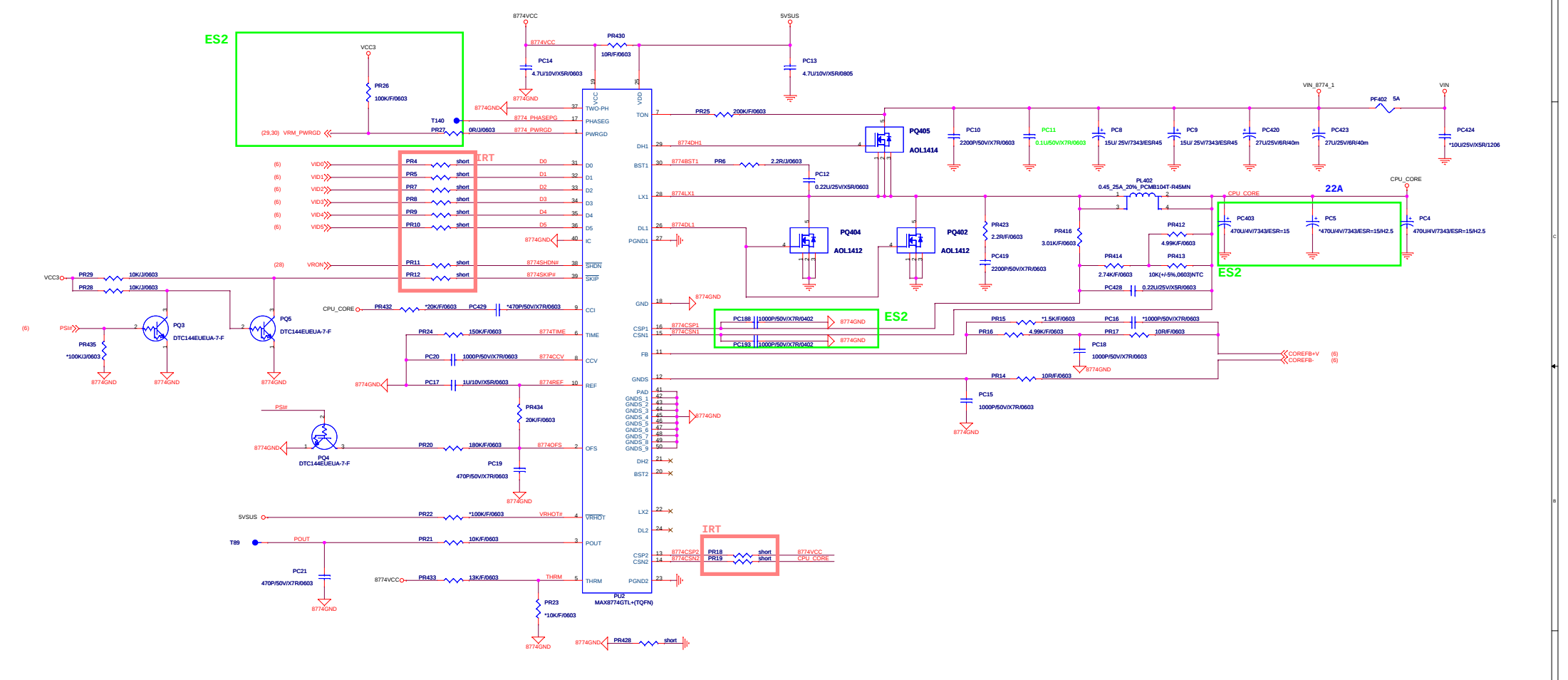
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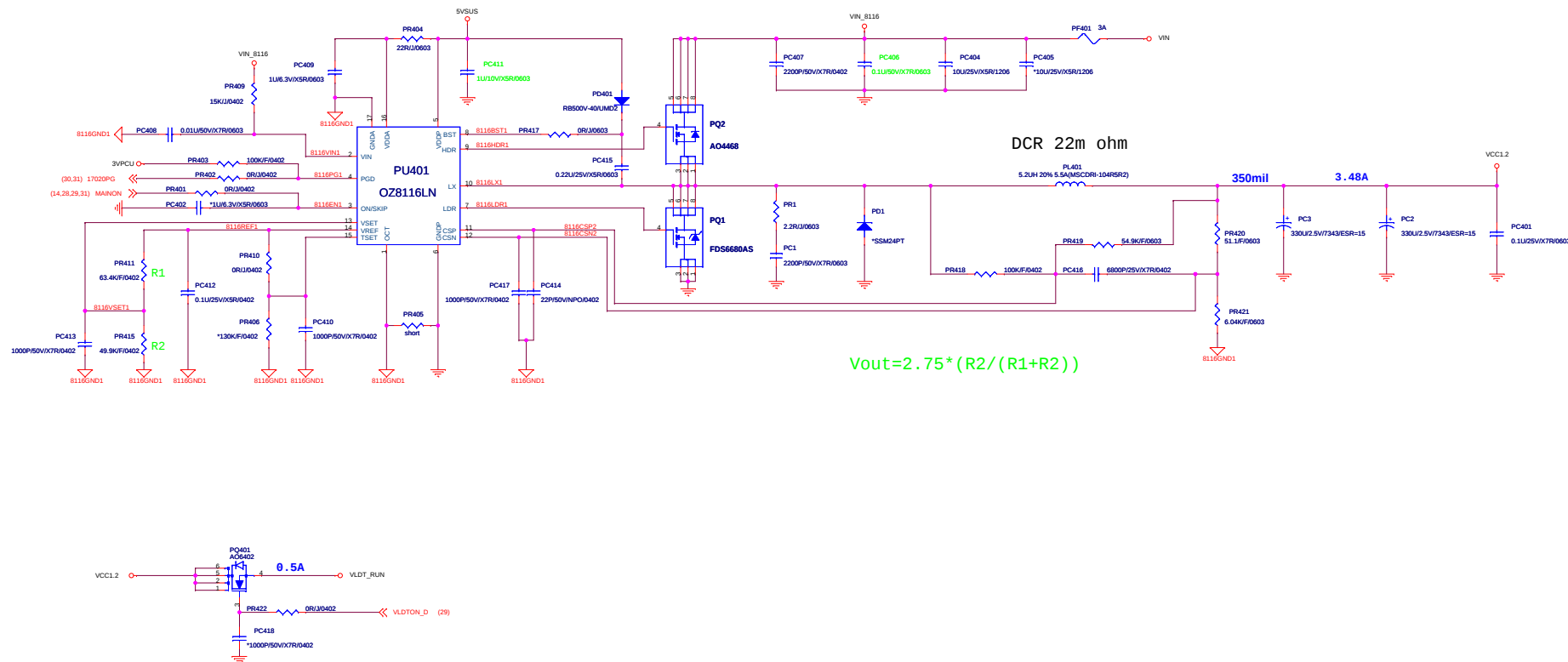








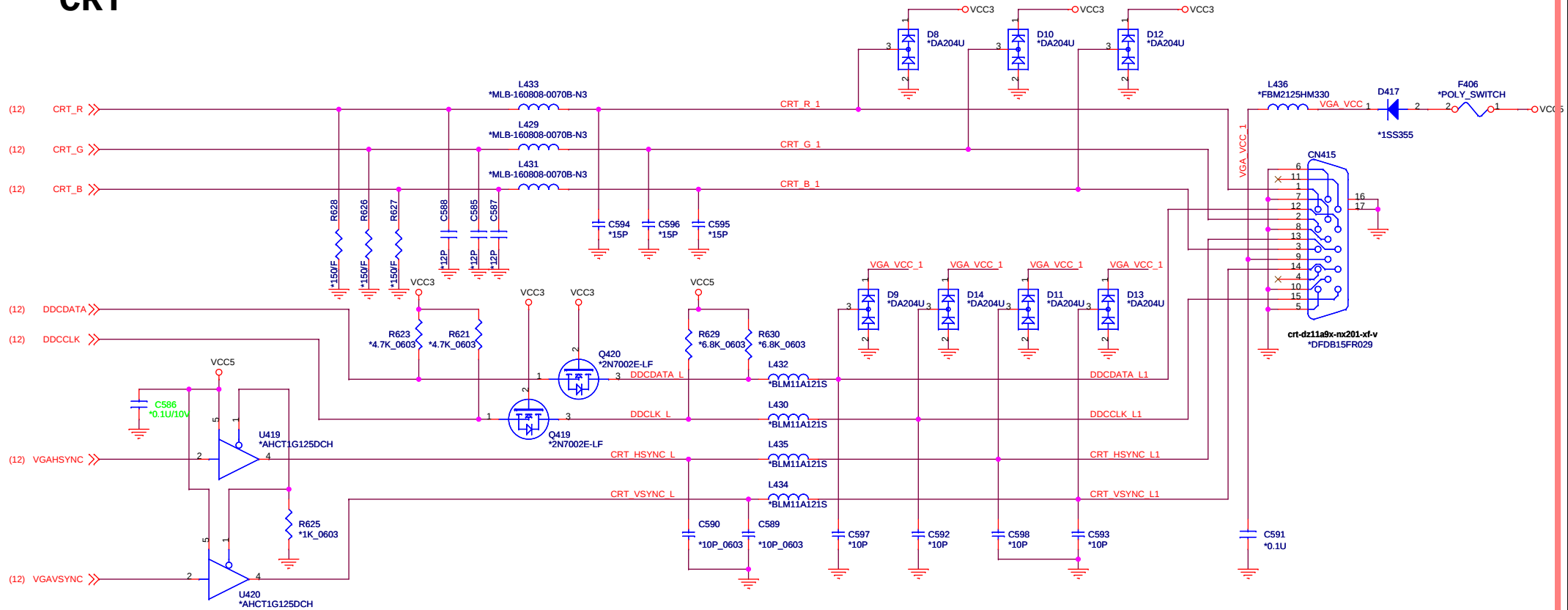




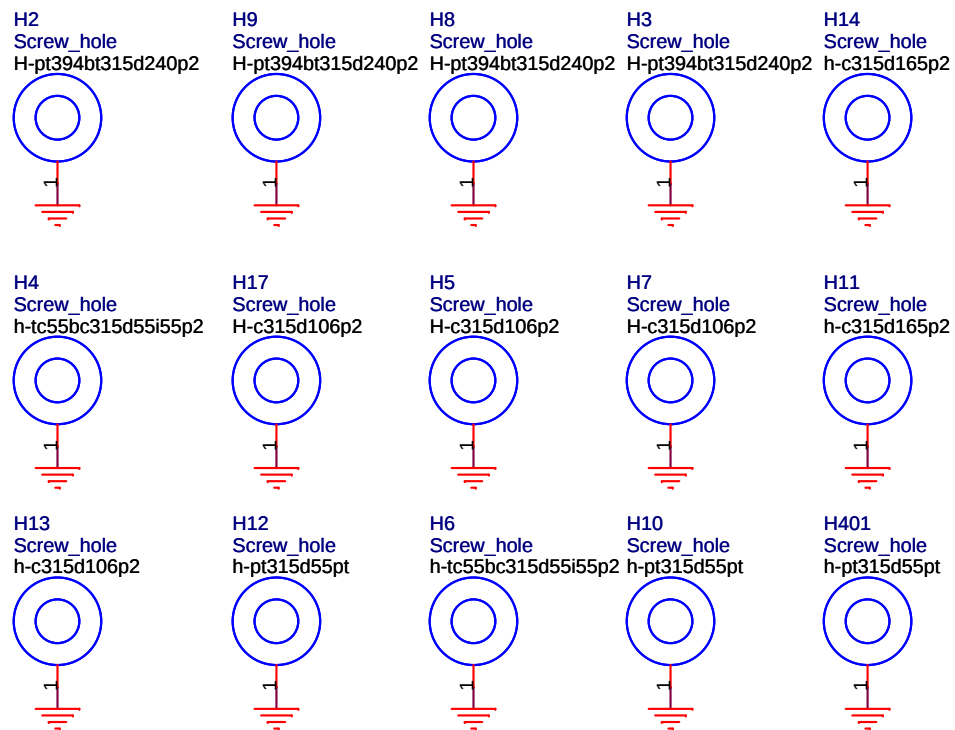
All Component in This Page is Reserved for Debug Only

CRT

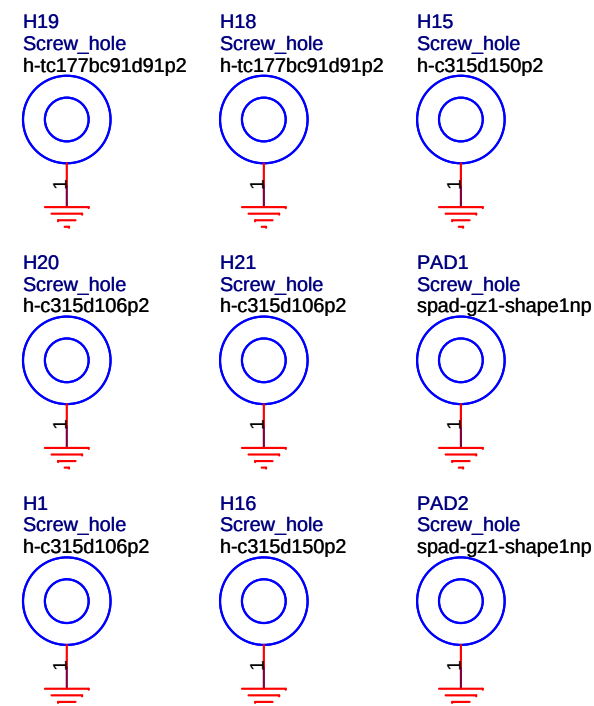
IRT



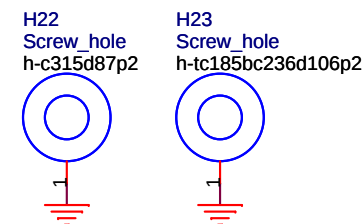
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PROJECT : GT1



ES2



IRT



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PROJECT : GT1

Size	Document Number	Rev
	History	A
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GT1 Mother Board Schematics Revision History

PCB Rev	Sch Rev	BOM Rev	DATE	Change List & Description
A	1A	A1A	Jan/06/09'	* 1st Release
B	2A	B1A	Feb/06/09'	Page 08 Mount R91 and R101 , demount R90 and R102 for memory can't be recognized Page 14 Add C2205 C2206 for EMI Page 15 Remove PCIE_PME# for S3 auto boot issue by Ricoh suggest Page 19 Change panel VCC control by DIGON and NB_PWRGD Page 19 Change CN2 footprint.Add F10 Page 20 Remove 1394 connector then add test point Page 20 Reserve 2 inverter for GBRST# timing of R5C833 Page 20 Add U422,C1021,Delete 1394 connector location Page 22 Change C567,C565 to X5R type Page 22 Add R1080 R1084 R1085 for GND_LAN Page 24 Change PCIRST# to pin22 of CN3, Add T2200 to pin17 on CN3 Page 24 Add CN10 for debug card Page 24 Change CLKREQ_WLAN# to PIN7 from PIN1,Add T2199 on PIN1 on CN3 Page 24 Delete PCIERST# and R89 on PIN22, Add T2200 on PIN22 of CN3 Page 25 Delete R177,change pin7 of CN7 to NC Page 26 Correct R581 to 330 ohm from 220 ohm Page 27 Add LP1013 on CN403 for EMI Page 28 Modify PS/2 function Page 29 Change PR45 to 330k ohm, make VCC3 assertion before VCC1.8 assertion Page 29 Change PQ6 to 2N7002,because former design make power on shut down Page 30 Add PR95 PR89 PC59 PC56 for power signal Page 30 Change PU402 to RT9025,because there is internal PU resistor in G966 which make leakage from 5VPCU to 3VPCU Page 31 Mount PQ29 for 1.8VSUS signal quality Page 32 VLDT_RUN no power issue Page 32 Add PC188 PC193 for CPU_CORE quality
C	3A	C2A	Mar/05/09'	Page 25 Add SATA Re-dricer circuit to fixed RX singal Page 26 Add Q423 and Q424 to meet some short-cut key power on function . Page 29 Chage PU404 form G1331T11U to G1391T12U for fitting SPEC Page 29 Add PC87 and PC88 for EMI interference Page 29 Add C2425 C2427 C2100 C2130 for EMI request
D	4A	D3A	Apr/04/09'	Page 06 R430,R424,R419,R407 change to default short pad Save one set HDT test points Page 12 R16,R20,R23 change to default short pad Page 13 L5,L7, L411 change to default short pad Add L2013 for NB VCC1.2V plane Page 14 R459,R445,R484,R486,R38 change to default short pad Page 16 R49,R528 change to default short pad Page 17 R434,R435 change to default short pad Page 20 R144,R143,R1017 change to default short pad Page 21 R591,R602 change to default short pad Page 23 ACN401,ACN402 change footprint for SMT solder hole issue Page 22 R605,R615 change to default short pad Page 23 ACN401 ACN402 change footprint to fit SMT request Page 24 R89,R138,R573,R582 change to default short pad Page 25 R643,R646 change to default short pad Page 26 LP3 change footprint to meet SMT parts lost issue Add Pad H30,H31 to increas pad size for SMT more easy to check if choke is cold solder or not Page 27 LP4,LP5,LP6,LP7,LP401,LP1013 change footprint to meet SMT parts lost issue Page 28 R575 change to default short pad Page 29 Add D418 D419 prevent DC-in inverse Page 30 PR48,PR56,PR66,PR77 change to default short pad Add Pad H24,H25,H26,H27 to increas pad size of PL1,PL3 for SMT more easy to check if choke is cold solder or not Page 31 PR63,PR64,PR68 change to default short pad Page 32 PR4,PR5,PR7-PR12,PR18,PR19 change to default short pad Page 34 All CRT compoenets do not staff Page 35 Add 2 screw hole : H22,H23 for ME request