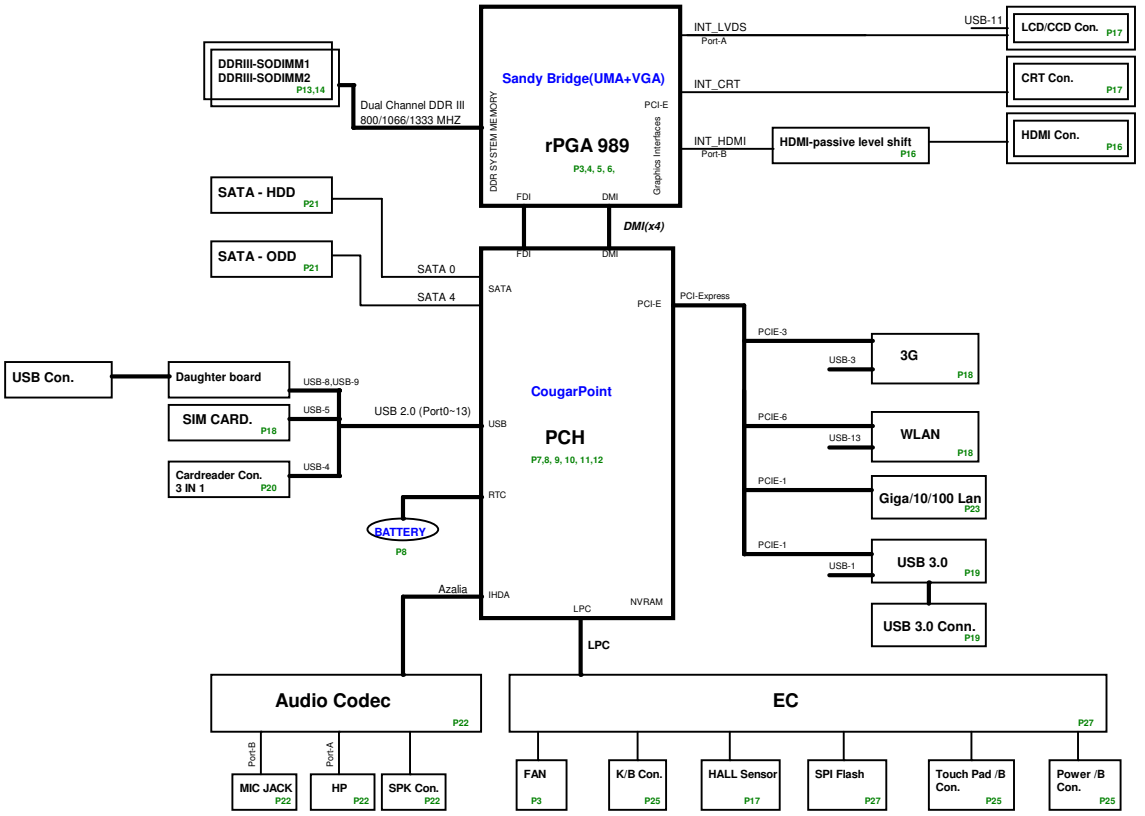
BU5 Block Diagram

01

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : SVCC
- LAYER 5 : IN2
- LAYER 6 : IN3
- LAYER 7 : GND
- LAYER 8 : BOT



POWER SYSTEM

ISL88731C	P28
PM6686	P29
UP6163	P30
RT8240	P31
TPS51461	P32
ISL95835HRTZ	P33
G966A	P34

+VCC_CORE

+1.5V
+1.5VSUS

+VTT
+1.05V

+1.8V

+1.5V_S5
+3VPCU
+3V_S5
+3V
+5VPCU
+5V_S5
+5V
+SMDDR_VTERM
+SMDDR_VREF

+VCCSA

Quanta Computer Inc.
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Block Diagram
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Table of Contents

POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0~S5
+VCCRTC	+3.0V~+3.3V		S0~S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0~S5
+3V_HDP	+3.3V	MAIN_ON	S0
+3VPCU	+3.3V	AC/DC Insert enable	S0
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0~S5
+5VPCU	+5V	AC/DC Insert enable	S0~S5
+5V_TMA	+5V	MAIN_ON	S0
WIMAX_P	+3.3V	WMAX_P for EC	
+1.8V	+1.8V	MAIN_ON	S0
+1.5V	+1.5V	MAIN_ON	S0
+1.5V_S5	+1.5V	S5_ON	S0~S5
+1.5V_SUS	+1.5V	SUSON	S0~S3
+VCC_CORE		VRON	S0
+VTT	+1.05V~+1.1V	MAIN_ON	S0
+1.05V	+1.05V	MAIN_ON	S0
+VAXG		GFXVR_EN	S0

GND PLANE	PAGE
GND_SIGNAL	32
CARD_GND	21
AGND_DC/DC	31
GND	ALL

ITEM	Value Code	FUNCTIONS
1	EV@	DISCRETE
2	IV@	UMA
3	U3@	USB 3.0
4	U2@	USB 2.0 (colay W USB 3.0)
5	HM@	HDMI
6	IHM@	Internal HDMI
7	EHM@	External HDMI
8	3G@	3G
9	C@	Cost issue
10	MDC@	Modem
11	S3@	S3 Power Reduction
12	NS3@	No S3 Power Reduction
13	E@	EMI
14	51@	1G LAN
15	52@	10/100 LAN
16	GS@	G-SENSOR
17	NGS@	No G-SENSOR

Quanta Computer Inc.

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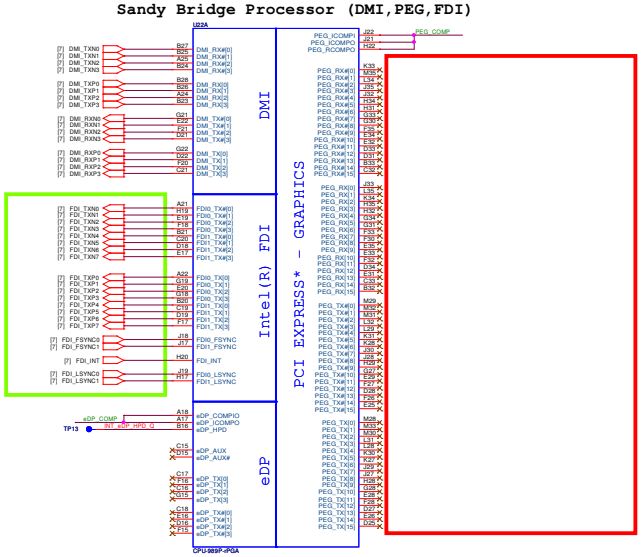
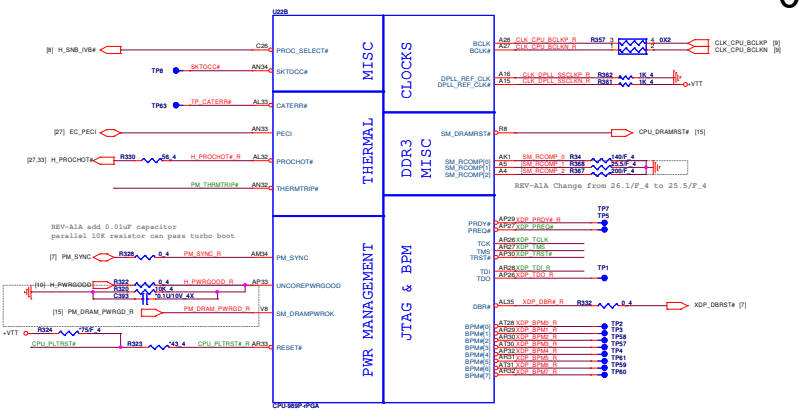
<CPU>

Sandy Bridge Processor (DMI,PEG,FDI)



Sandy Bridge Processor (CLK,MISC,JTAG)

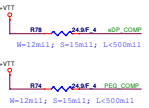


REV-A1A Change from 26.1/F_4 to 25.5/F_4

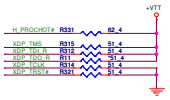
REV-A1A add 0.01uF capacitor parallel 10K resistor can pass turbo boot

FDI Disabling (Discrete Only) <CPU>

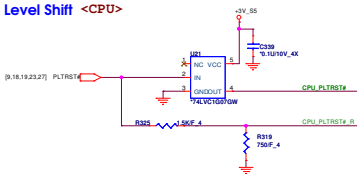
DP & PEG Compensation <CPU>



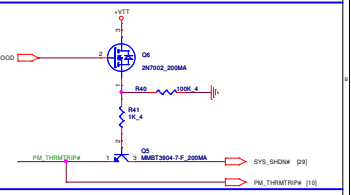
Processor pull-up <CPU>



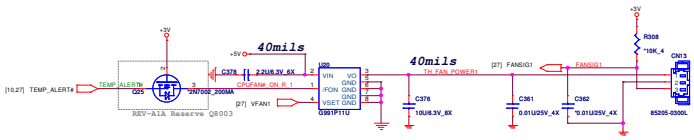
Level Shift <CPU>



Thermal Trip<CPU>

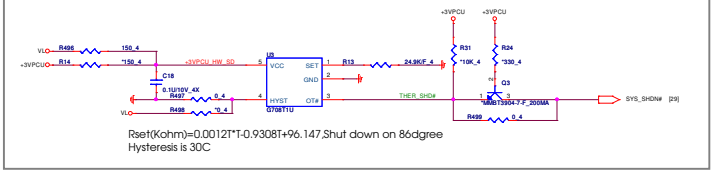


FAN Control-->For one FAN solution <THC>



REV-A1A Reserve Q8003

CPU Thermal sensor / MB Local TEMP <THC>



Rset(Kohm)=0.0012T*T-0.9308T+96.147,Shut down on 86dgree
Hysteresis is 30C

REV-C3A Change VCC PINS of U3 from +3VPCU to VL
Add R496,R497,R499
Reverse R14,R498,R31,R24,Q3

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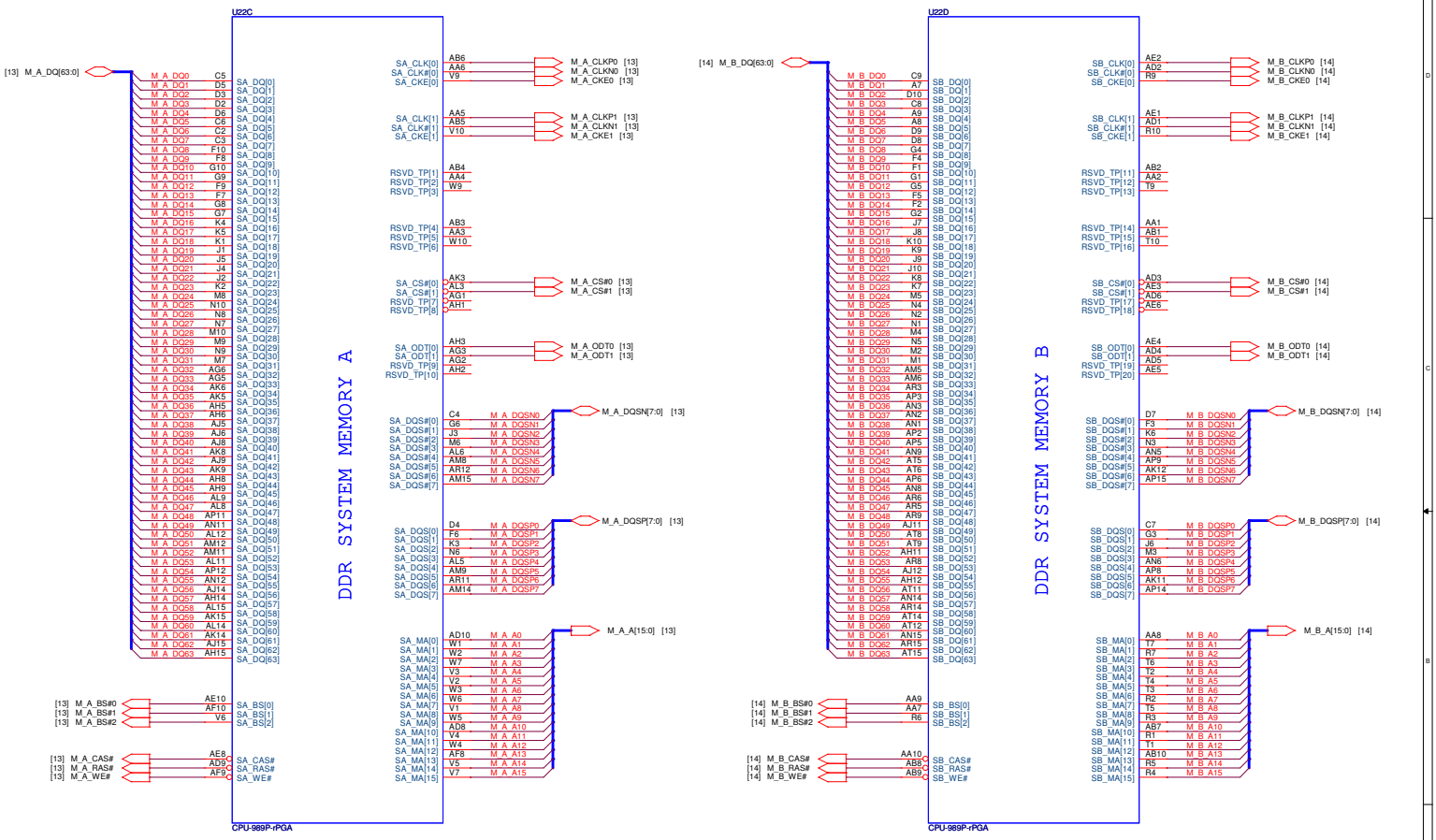
<CPU>

Sandy Bridge Processor (DDR3)

04



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	Sandy Bridge 2/4	2A

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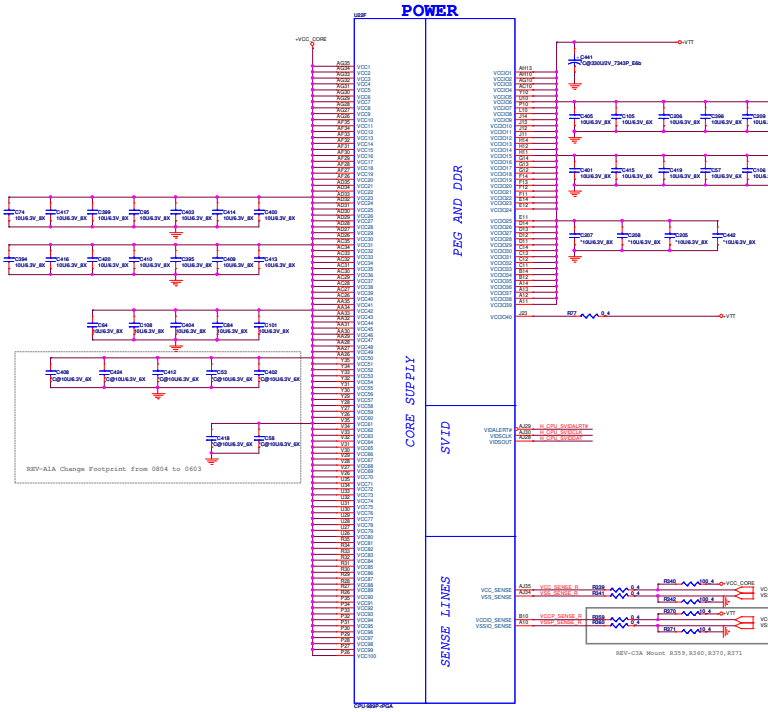
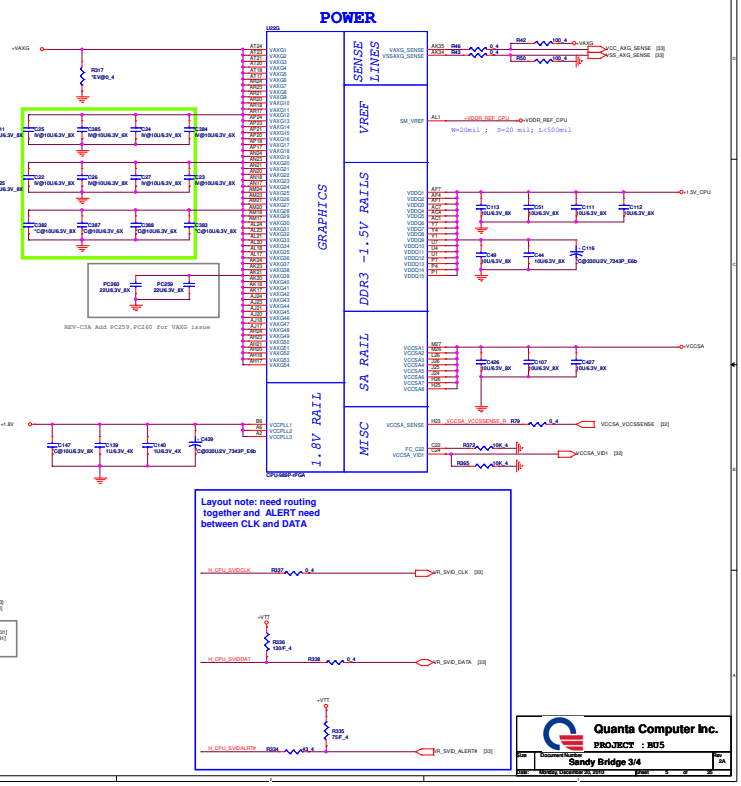
Sandy Bridge Processor (POWER)



Sandy Bridge Processor (GRAPHIC POWER)



Layout note: need routing together and ALERT need between CLK and DATA

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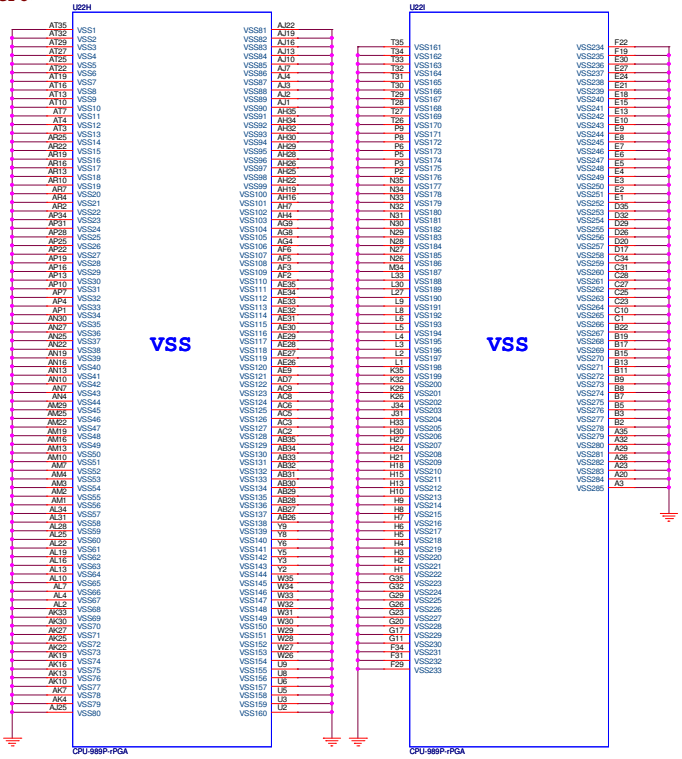
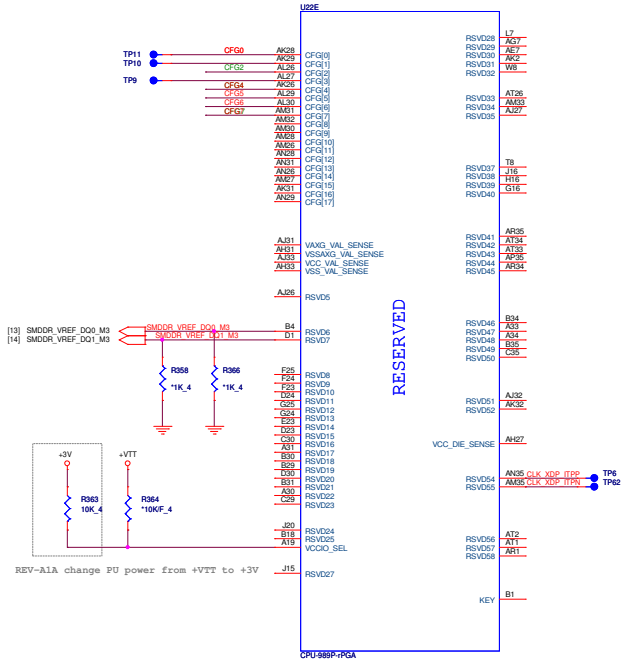
<CPU>

Sandy Bridge Processor (GND)



Sandy Bridge Processor (RESERVED, CFG)

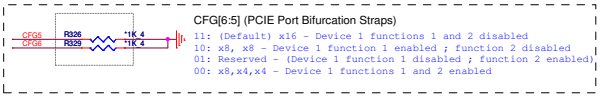


Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

REV-A1A change to 5% tolerance



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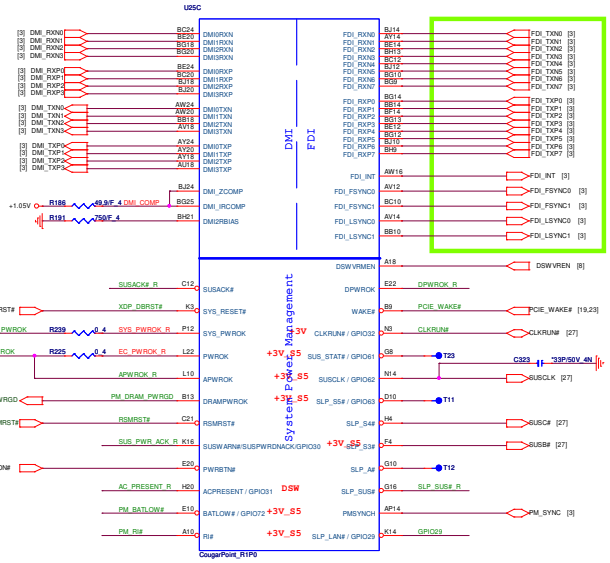
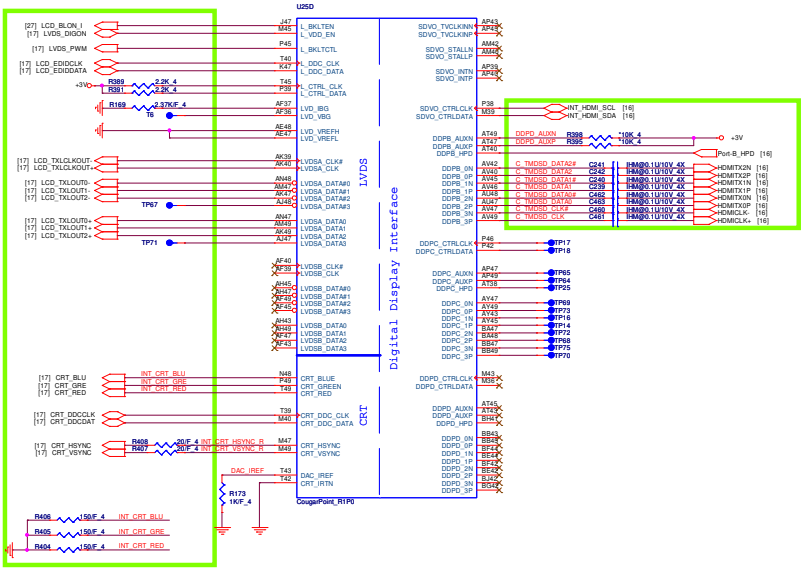
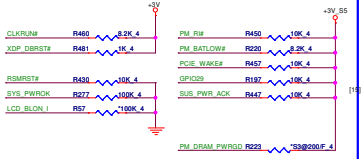
Cougar Point (DMI,FDI,PM)



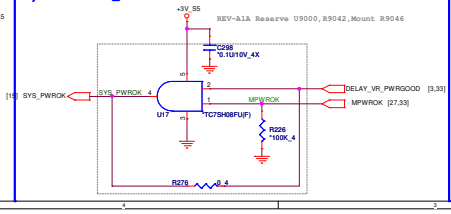
Cougar Point (LVDS,DDI)



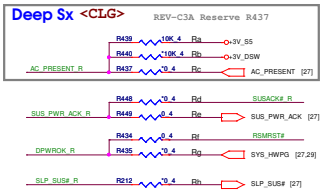
PCH Pull-high/low <CLG>



System PWR_OK <CLG>



Deep Sx <CLG>



Net Name	Deep Sx Support	Deep Sx No Support
AC_PRESENT	Rb,Rc stuff	Ra stuff
SUS_PWR_ACK	Rd stuff	Re stuff
DPWROK	Rg stuff	Rf stuff
SLP_SUS	Rh stuff	Rh No stuff

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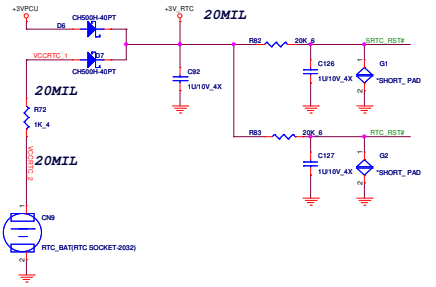
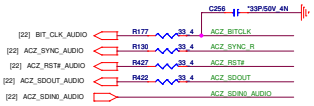
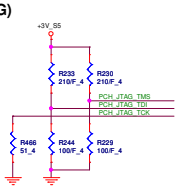
RTC Circuit <RTC>



HDA Bus <ADO>

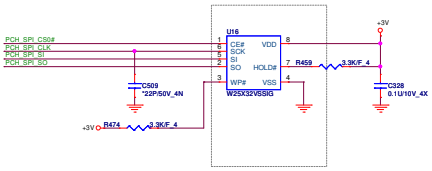


PCH JTAG Debug (CLG)



PCH Dual SPI (CLG)

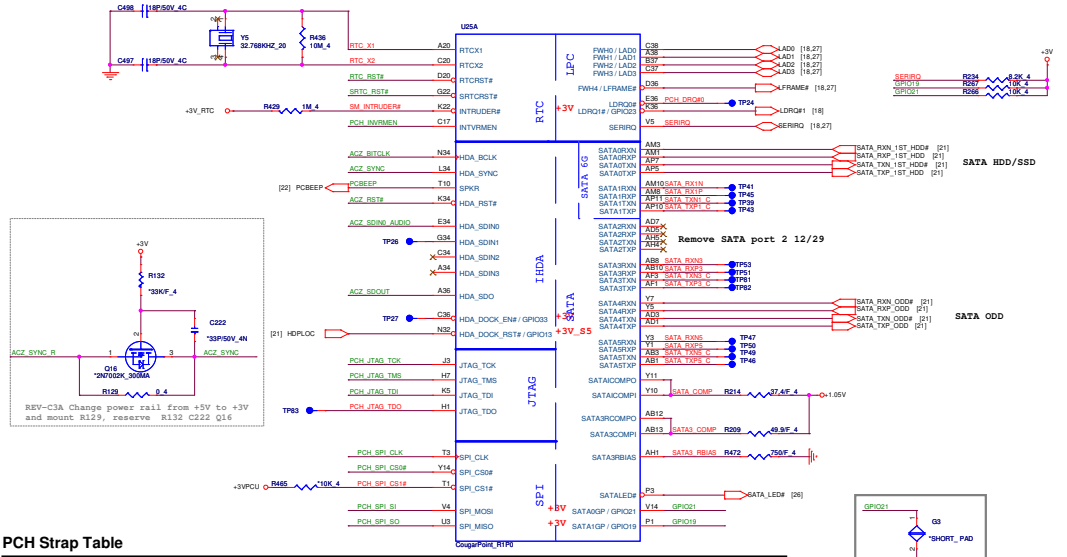
MX25L3205DM2I-12G: AKE39FP0Z00
W25X32VSSIG: AKE39ZP0N00



REV-A1A change footprint
from socket type to W25X32VSSIG

PCH2 <CLG> <ADO> <RTC>

Cougar Point (HDA,JTAG,SATA)



REV-B2A Add G3 for Clear CMOS password

PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V R238 *1K_4 PCBEEP
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R403 *1K_4 PCI_GNT3# [9]
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC R438 330K_4 PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GPIO19 / Boot Location 1 / 1 / SPI * 0 / 0 / LPC	R399 *1K_4 GNT1# [9] R478 *1K_4 GPIO19
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)	+3V R423 *1K_4 ACZ_SDOUT ACZ_SDOUT [27]
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)	R463 2.2K_4 R464 2.7K_4 1.8V DF_TVS [10] H_SNB_IVB# [3]
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	+3VPCU R222 *10K_4 R228 *1K_4 PLL_ODVR_EN [10]
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V_S5 R136 1K_4 ACZ_SYNC
GPIO15	TLS Confidentiality	RSMRST	0 = Default. TLS no Confidentiality 1 = TLS Confidentiality	+3V_S5 R462 1K_4 GPIO15 [10]
DSWVRMEN	Deep S4/S5 Well On -Die Voltage Regulator Enable	ALWAYS	0 = Disable 1 = Enable	DSWVRMEN [7] +3V_RTC R443 330K_4 R442 *330K_4
INIT3_3V#	Reserved	PWROK	1 = Default (weak pull-up 20K)	Should not pull low. leave as No Connect
GNT2#/ GPIO53	ESI Strap (Server Only)	PWROK	1 = Default. Should not be pulled low for desktop and mobile	Should not pull low for desktop and mobile
L_DDC_DATA	LVDS Detected	PWROK	0 = Default. Not Detected 1 = Detected	1= PU to 3V
SDVO_CTRLDATA	Port B Detected	PWROK	0 = Default. Not Detected 1 = Detected	1= PU to 3V
DDPC_CTRLDATA	Port C Detected	PWROK	0 = Default. Not Detected 1 = Detected	0=NC
DDPD_CTRLDATA	Port D Detected	PWROK	0 = Default. Not Detected 1 = Detected	0=NC
SATA3GP/ GPIO37	Reserved	PWROK	0 = Default	Should not be pulled high when strap is sampled
SATA2GP/ GPIO36	Reserved	PWROK	0 = Default	Should not be pulled high when strap is sampled

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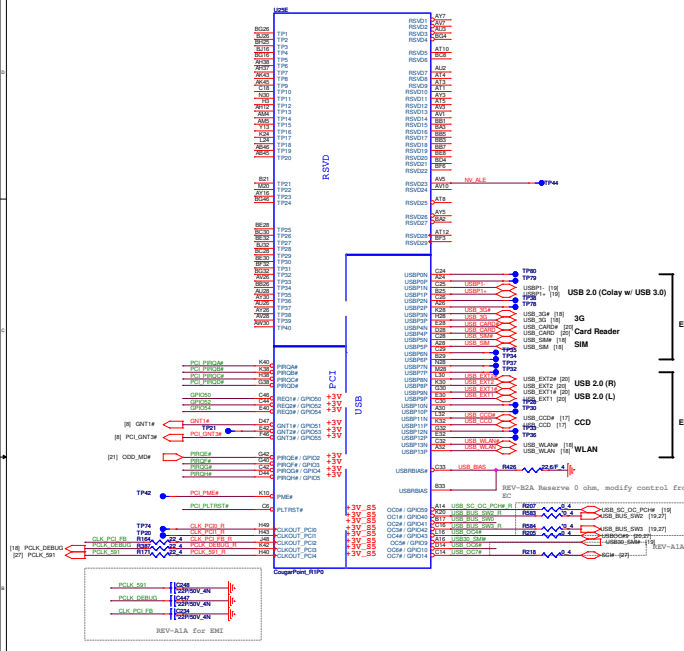
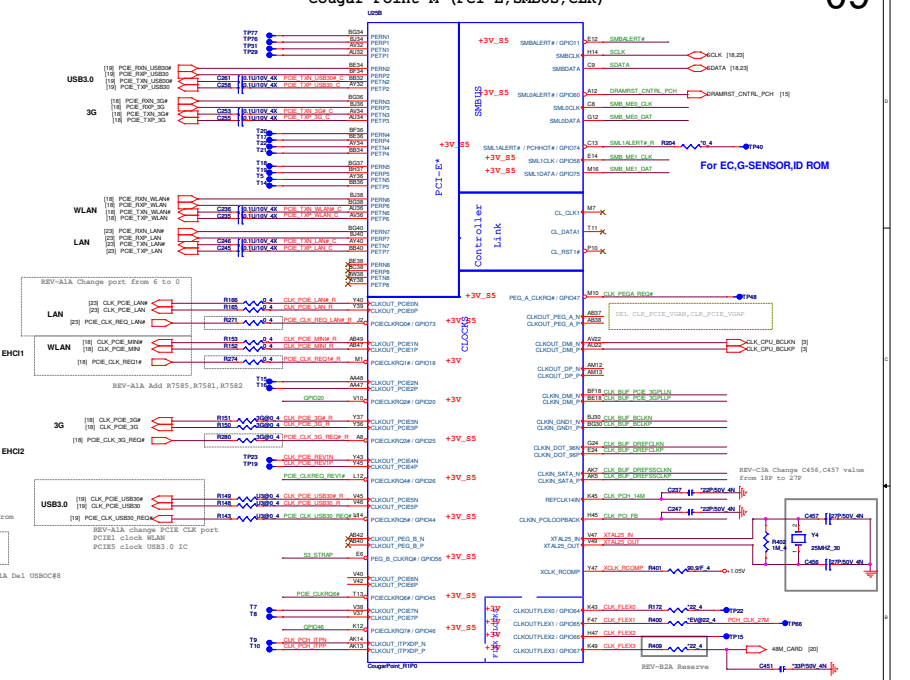
<CLG> <U3B> <USB> <MNW> <MNT> <LAN>

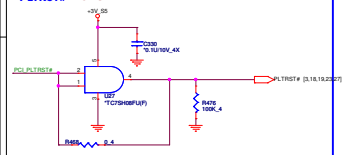
Cougar Point-M (PCI,USB,NVRAM)



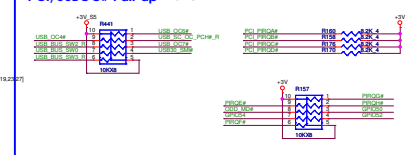
Cougar Point-M (PCI-E,SMBUS,CLK)



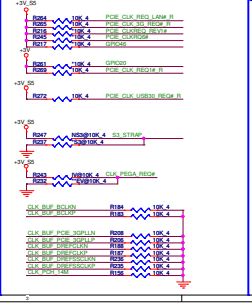
PLTRST# <CLG>



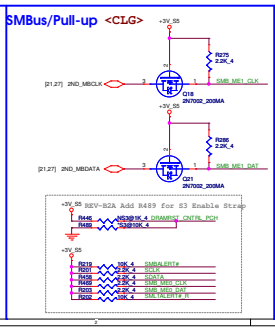
PCI/USBOC# Pull-up <CLG>



CLK_REQ/Strap Pin <CLG>



SMBus/Pull-up <CLG>



	33MHz	27MHz	48/24MHz	14.318MHz	25MHz
CLK_FLEX0	●	●	●	●	
CLK_FLEX1		●	●	●	
CLK_FLEX2	●	●	●	●	●
CLK_FLEX3		●	●	●	

Quanta Computer Inc.

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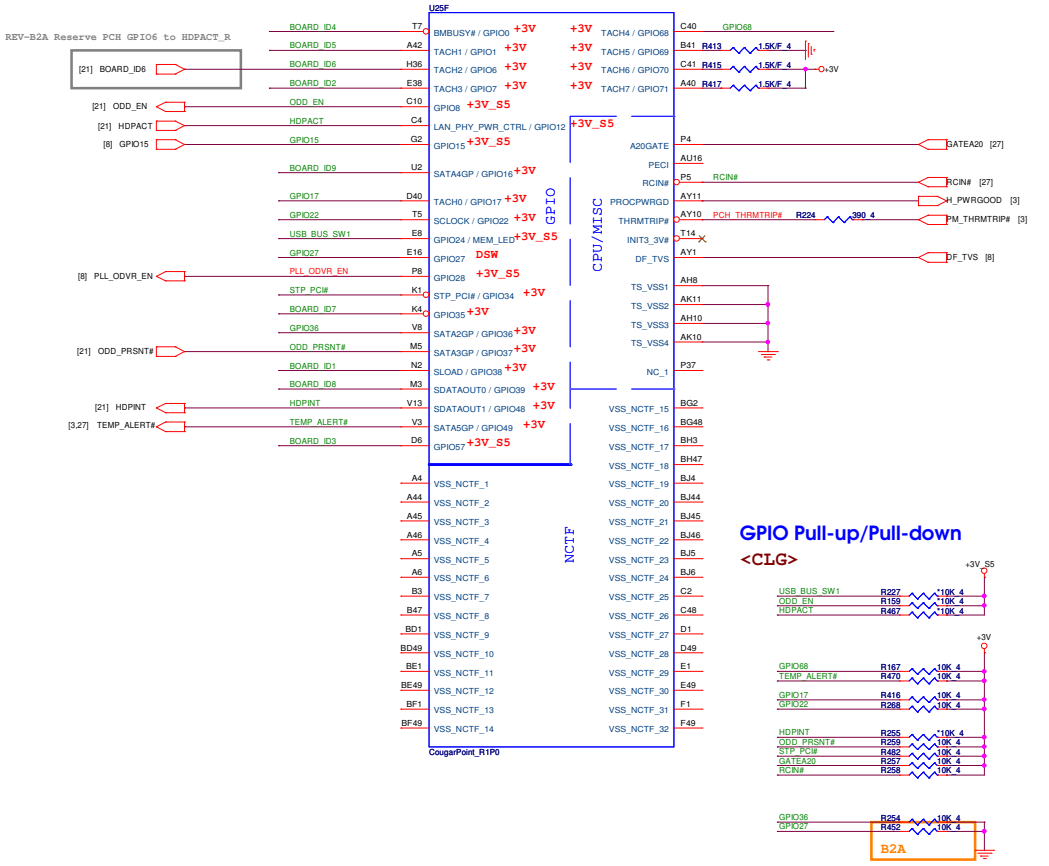
<CLG>

Cougar Point (GPIO,VSS_NCTF,RSVD)



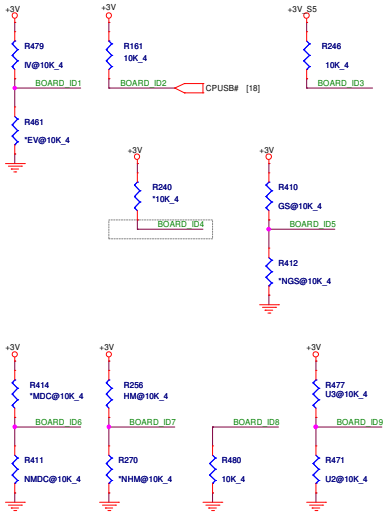
GPIO Pull-up/Pull-down

<CLG>

BOARD ID SETTING <CLG>

10

Board ID	ID1	ID2	ID3	ID4	ID5	ID6	ID7	ID8	ID9
UMA SKU VGA SKU	H L								
W/O 3G W/ 3G		H L							
W/O LED_KB W/ LED_KB			H L						
14" 15"				H L					
W G-SNR W/O G-SNR					H L				
W/ MDC W/O MDC						H L			
W/ HDMI W/O HDMI							H L		
NC 13"								H L	
W/ USB3.0 W/O USB3.0									H L



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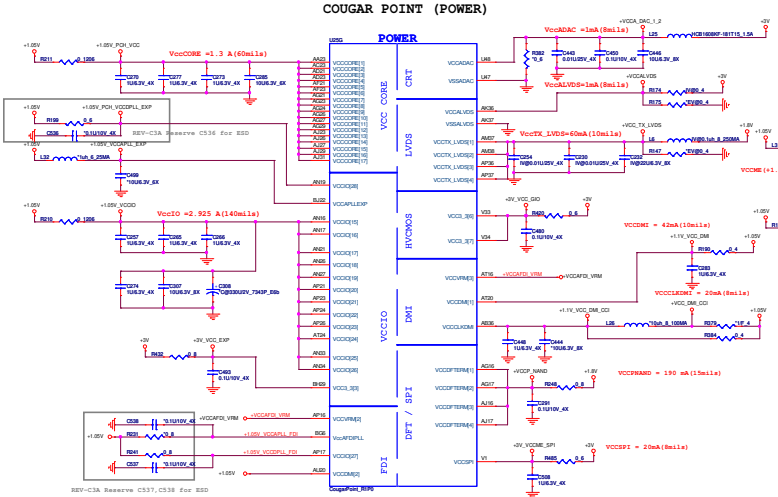
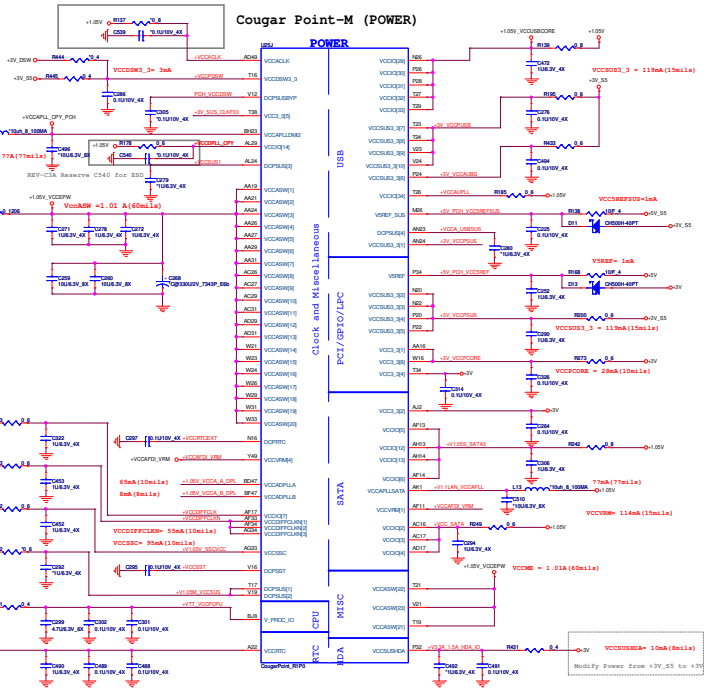
COUGAR POINT (POWER)



Cougar Point-M (POWER)



REV-C3A Add C533 and reserver C535,C534

REV-C3A Reserve D23

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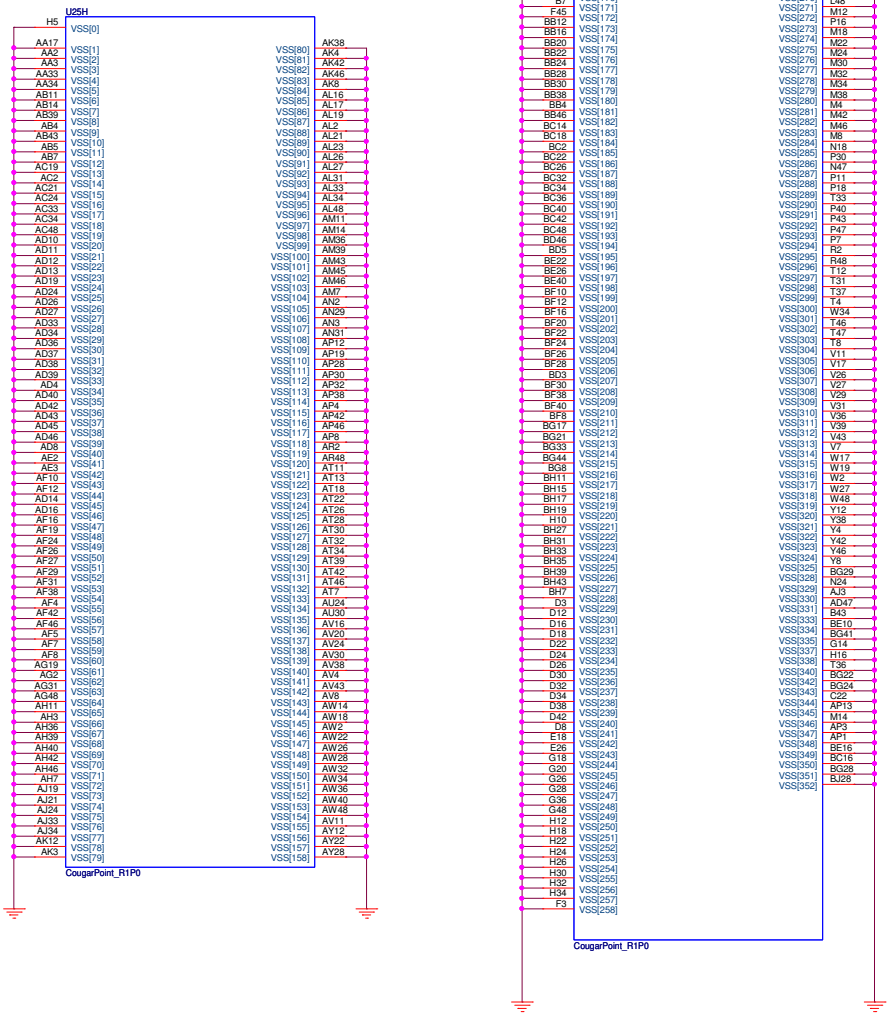
Date: Friday, December 17, 2010	Sheet 11 of 38	

IBEX PEAK-M (GND)



Quanta Computer Inc.

PROJECT : BU5

Size	Document Number	Rev
	Cougar Point 6/6	2A

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H=8

JDIM2A

[4] M_A_A[15:0]

SO-DIMMA SPD Address is 0XA0
SO-DIMMA TS Address is 0X30

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDRRK-20401-TP8D

M_A_DQ[63:0] [4]

[4] M_A_BS#0
[4] M_A_BS#1
[4] M_A_BS#2
[4] M_A_CS#0
[4] M_A_CS#1
[4] M_A_CLKP0
[4] M_A_CLKN0
[4] M_A_CLKP1
[4] M_A_CLKN1
[4] M_A_CKE0
[4] M_A_CKE1
[4] M_A_CAS#
[4] M_A_RAS#
[4] M_A_WE#

R296 10K/F_4 DIMM0_SA0
R295 10K/F_4 DIMM0_SA1

[14,18] CGCLK_SMB
[14,18] CGDAT_SMB

[4] M_A_ODT0
[4] M_A_ODT1

[4] M_A_DQSP[7:0]

[4] M_A_DQSN[7:0]

H=8

JDIM2B

+1.5VSUS

+3V

[14,15] DDR3_DRAMRST#
R309 *10K/F_4 PM_EXTTS#0
+1.5VSUS
R92 *1K/F_4

[6] SMDDR_VREF_DQ0_M3
R111 *0_4 SMDDR_VREF_DQ0
SMDDR_VREF_DIMM

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDRRK-20401-TP8D

+SMDDR_VTERM

SMDDR_VREF_DIMM [14]

C36 470P/50V_4X
R39 *10K/F_4
R36 0_4
R38 *10K/F_4
+SMDDR_VREF
+1.5VSUS

Place these Caps near So-Dimm0.

+1.5VSUS
C88 4.7U/6.3V_6X
C35 4.7U/6.3V_6X
C68 4.7U/6.3V_6X
C85 4.7U/6.3V_6X
C52 4.7U/6.3V_6X
C48 4.7U/6.3V_6X
C76 0.1U/10V_4X
C66 0.1U/10V_4X
C87 0.1U/10V_4X
C79 0.1U/10V_4X

SMDDR_VREF_DQ0
C197 0.1U/10V_4X
C171 2.2U/6.3V_6X

SMDDR_VREF_DIMM
C37 0.1U/10V_4X
C41 2.2U/6.3V_6X

+3V
C340 2.2U/6.3V_6X

+SMDDR_VTERM
C345 1U/6.3V_4X
C343 1U/6.3V_4X
C346 1U/6.3V_4X
C344 1U/6.3V_4X

+1.5VSUS
R107 1K/F_4
SMDDR_VREF_DQ0
R104 1K/F_4
C198 0.1U/10V_4X
C199 *0.047U/10V_4X

+1.5VSUS
+C62 *C@330U/2.5V_7343P_E9a

Quanta Computer Inc.
PROJECT : BU5

Size	Document Number	Rev
	DDR3 DIMM-0	2A

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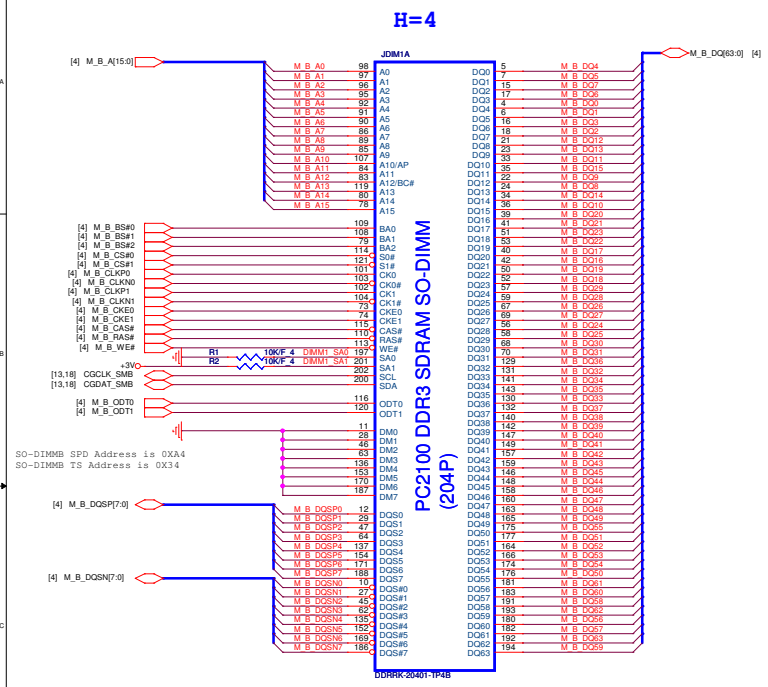
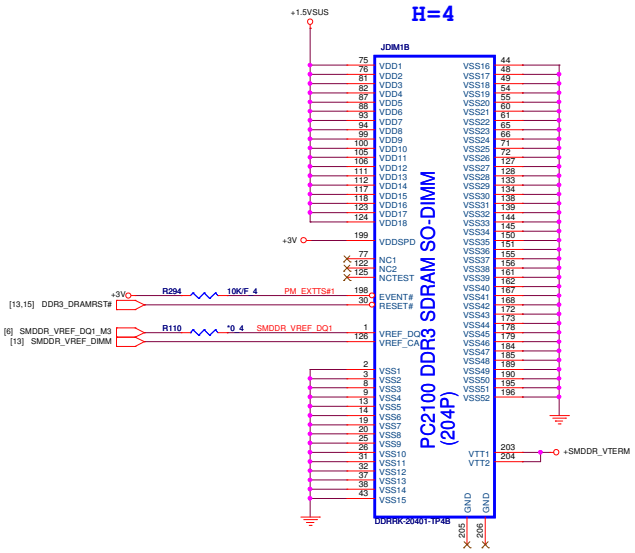
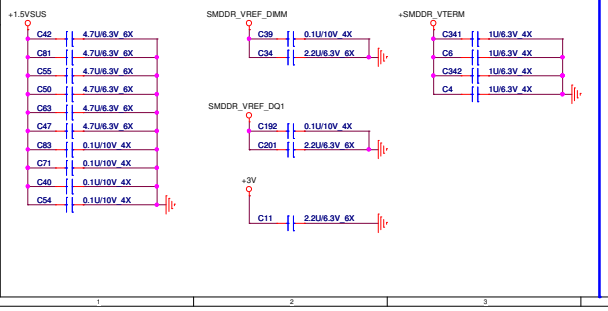
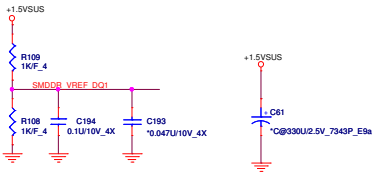




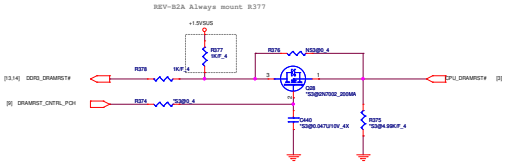
Place these Caps near So-Dimm1.



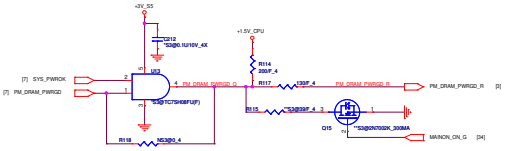


Quanta Computer Inc.			
PROJECT : BU5			
Size	Document Number		Rev
	DDR3 DIMM-1		2A
Date: Monday, December 20, 2010	Sheet 14 of 35		

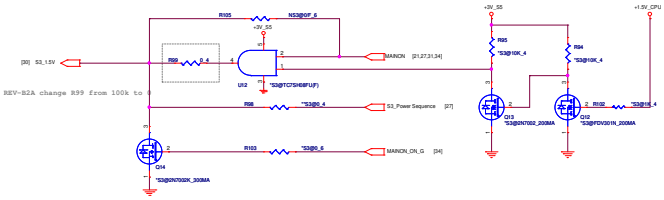
S3 power Reduction (SM_DRAMRST#) <S3P> <4>



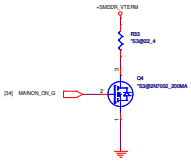
S3 power Reduction (SM_DRAMPWROK) <S3P> <3>



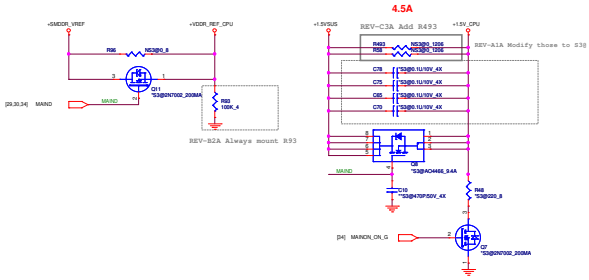
For S3 power Reduction Sequence <S3P> <3>



For S3 power Reduction VTT discharge <S3P> <13>



S3 power Reduction (CPU Power) <S3P> <5>



Quanta Computer Inc.

PROJECT : BU5

Size | Document Number | Rev

S3 power Reduction | 2A

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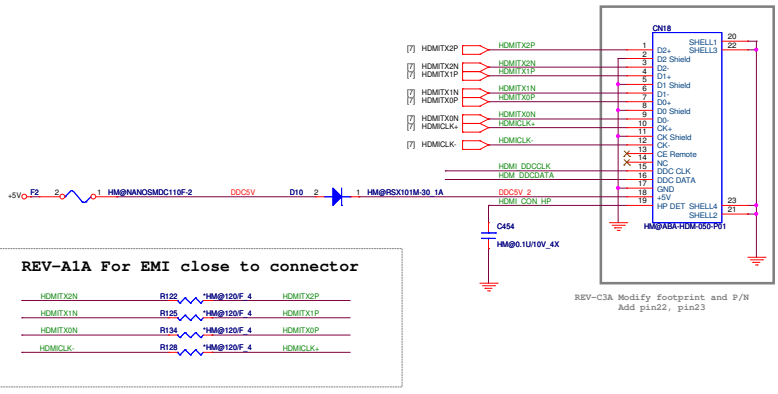
HDMI Conn <HDM>

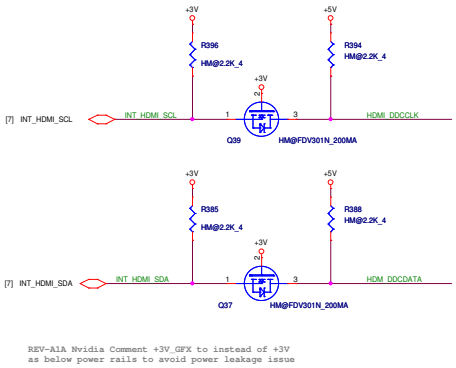


REV-C3A Modify footprint and P/N
Add pin22, pin23

REV-A1A For EMI close to connector

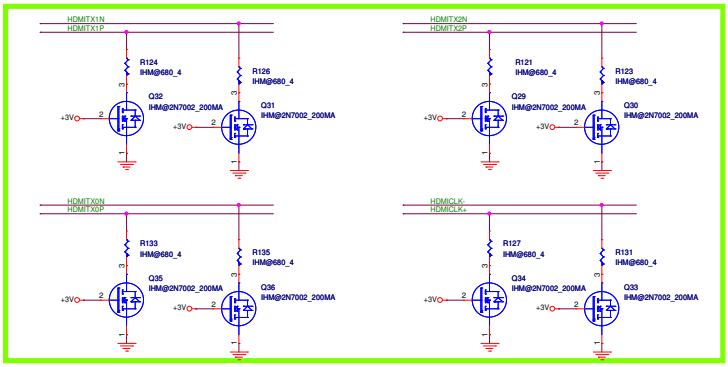
HDMITX2N	R122	*HM@120/F_4	HDMITX2P
HDMITX1N	R125	*HM@120/F_4	HDMITX1P
HDMITX0N	R134	*HM@120/F_4	HDMITX0P
HDMICLK-	R128	*HM@120/F_4	HDMICLK+

HDMI-SMBus <HDM>

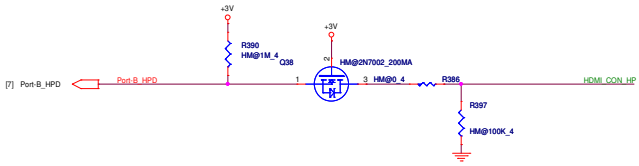


REV-A1A Nvidia Comment +3V_GFX to instead of +3V
as below power rails to avoid power leakage issue

HDMI-passive level shift <HDM>



HDMI-HPD <HDM>



REV-A1A Del External HDMI-HPD

Quanta Computer Inc.

PROJECT : BU5

Size	Document Number	Rev
	HDMI CONN	2A

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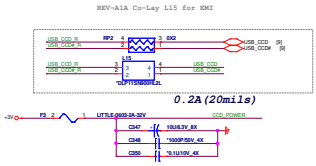
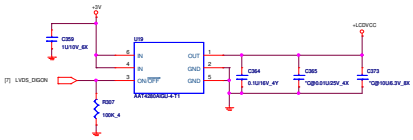
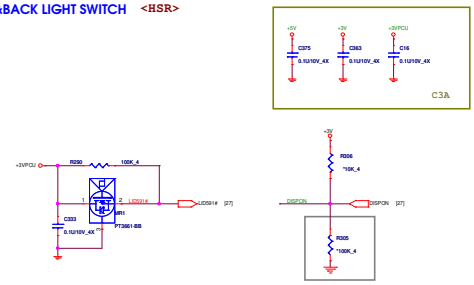
CCD <CCD>



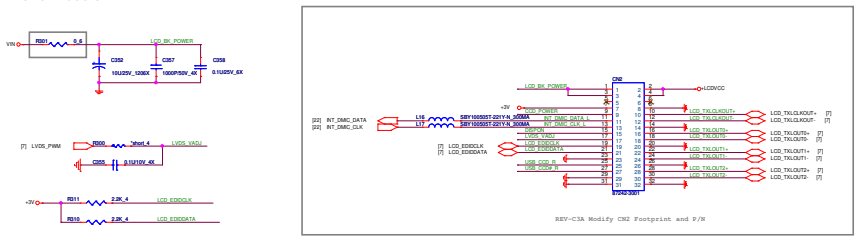
LCD POWER SWITCH <LDS>



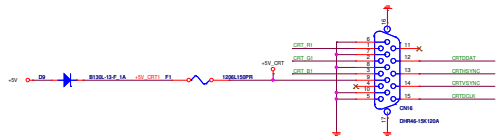
HALL SENSOR&BACK LIGHT SWITCH <HSR>



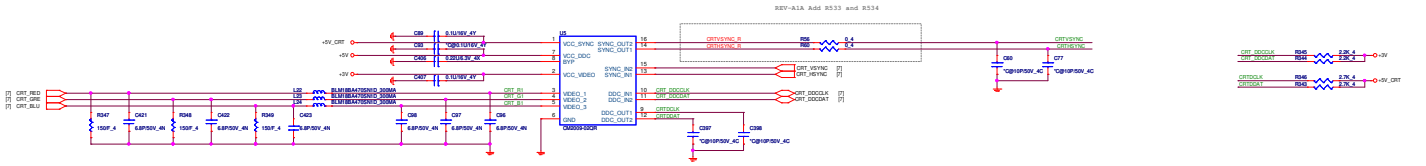
LCD Panel Module <LDS>



CRT CONN Interface <CRT>



<CRT>



Quanta Computer Inc.			
PROJECT : BU5			
Size	Document Number		Rev
	LCD/LED Panel/CCD		2A
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MINI Card Slot#1 <MNW>
(WiFi)

Before RAMP must to remove
debug card component

REV-C3A Mount C368

REV-C3A Modify R303 Value from 100K to 0

SMBus(DDR3/WLAN/3G)

MINI Card Slot#2 <MNT>
3G

2.75A (120mils)

REV-C3A Add R494

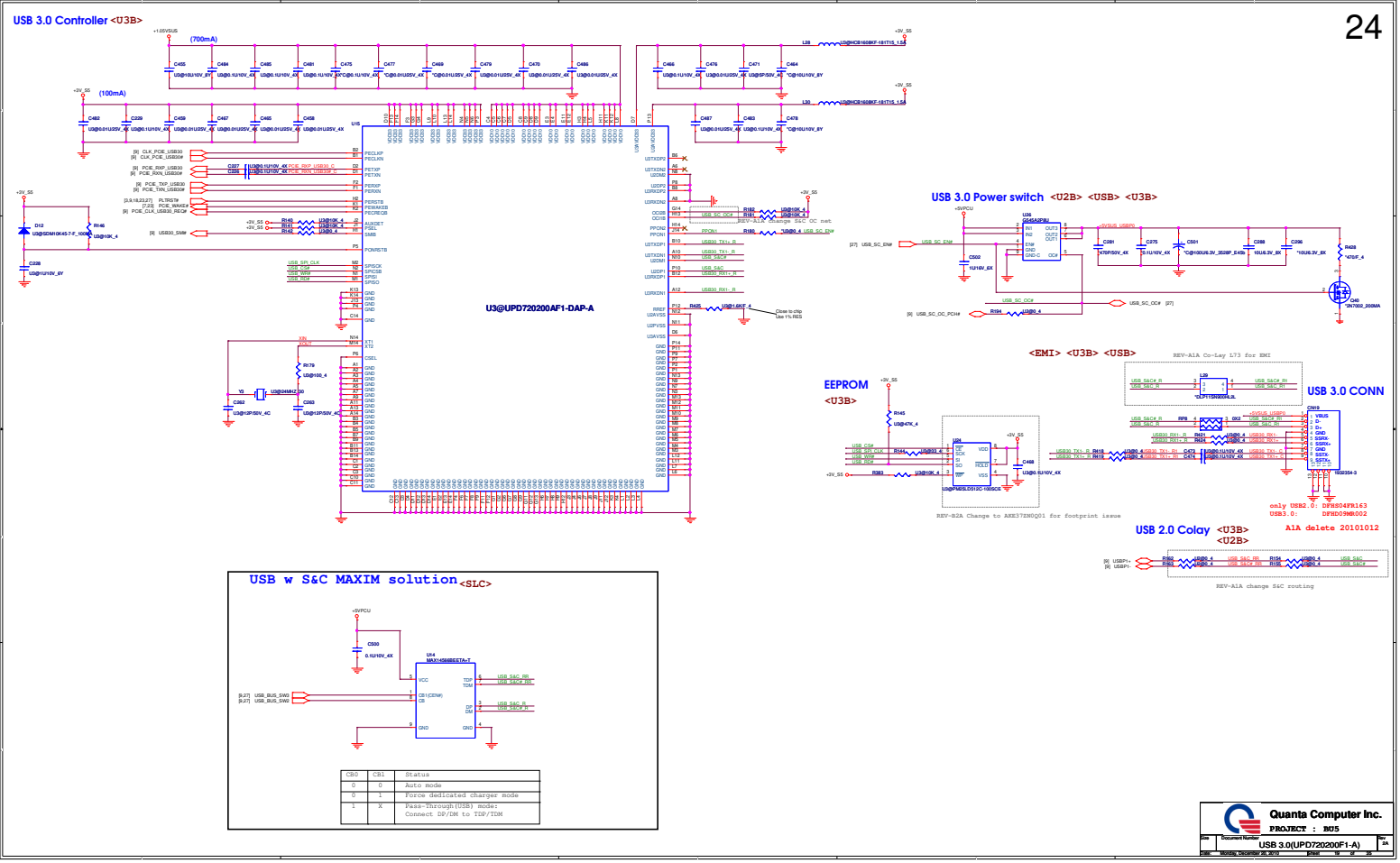
REV-A1A Add Q10,R7,R201 for CLK REQ#

For SIM Card on daughtor board

REV-A1A Co-Lay L77 for EMI

REV-B2A Modify CN14 Footprint and P/N,PIN define

Quanta Computer Inc.
PROJECT : BU5
Size: Document Number: MINI CARD(WLAN/3G/SIM Card) Rev: 2A
Date: Monday, December 20, 2010 Sheet 18 of 38



CB0	CB1	Status
0	0	Auto mode
0	1	Force dedicated charger mode
1	X	Pass-Through(USB) mode: Connect DP/DM to TDP/TDM

Quanta Computer Inc.
PROJECT : BU5
Size: A3 | Document Number: USB 3.0(UPD720200F1-A) | Rev: 2A
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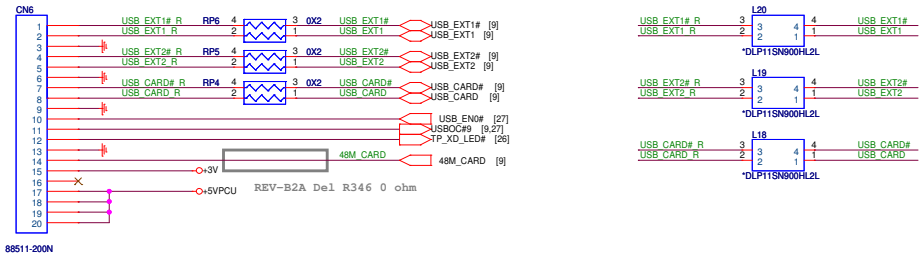
USB2.0 Left 1
USB2.0 Left 2 <U2B> <MMC> <USB> <EMI>



REV-A1A Co-Lay L74,L75,L76 for EMI

Quanta Computer Inc.
PROJECT : BU5

Size	Document Number	Rev
	HDMI CONN	2A

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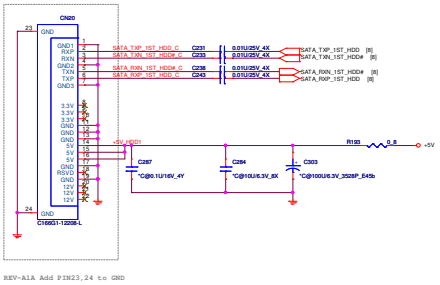
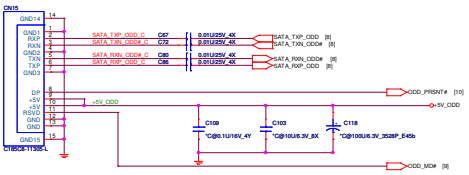
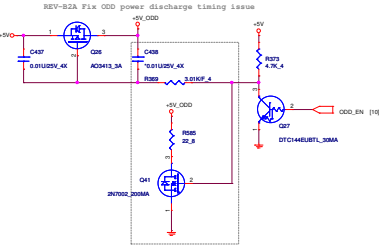
HDD Interface <H1D>



ODD Interface <ODD>

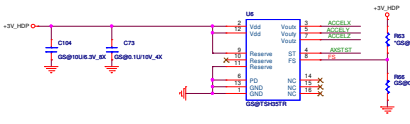


ODD Zero power . (Only for Intel) <OZP>



3D-LDO Power <GSR>

3D-Sensor IC <GSR>



FS (Full Scale) selection

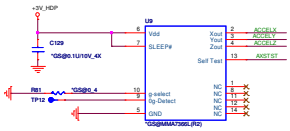
FS	0	1
	2g Full-Scale	6g Full-Scale

PD (Power Down) selection

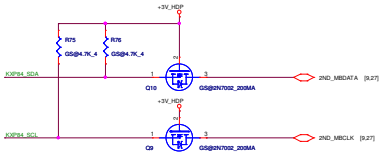
PD	0	1
	Normal Mode	Power-down mode

HDPPD selection

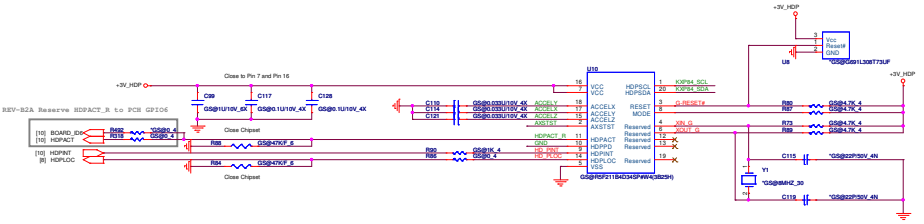
HDPPD	0	1
	Normal Mode	Power-down mode



3D-SMBus <GSR>

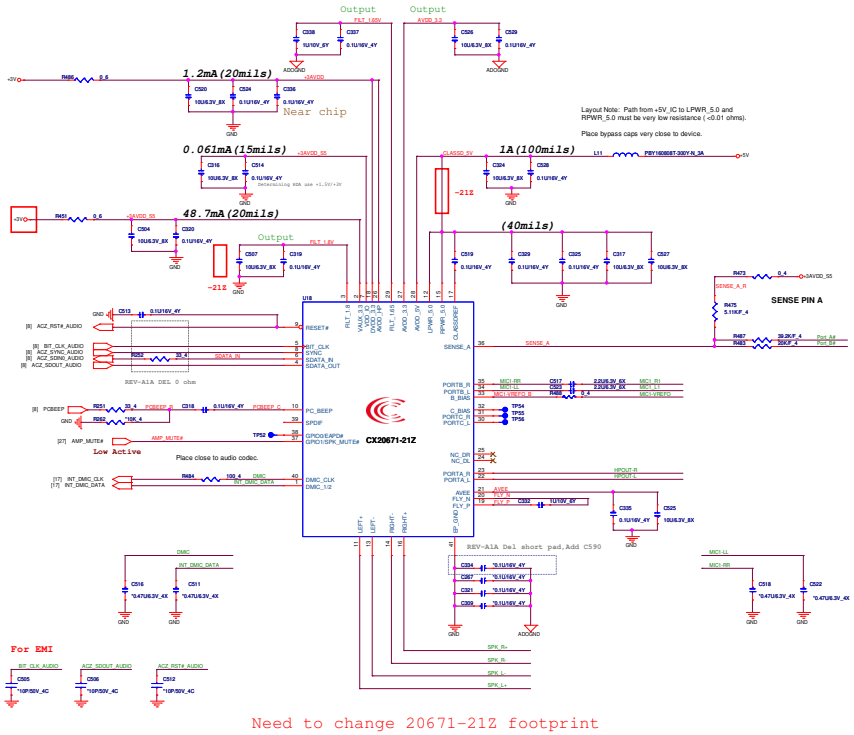


3D-u-micro P <GSR>

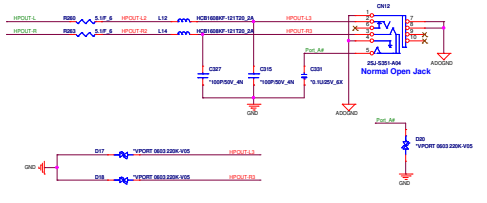


Quanta Computer Inc.
PROJECT : BU5
Size | Document Number: HDD/ODD/MDC | Rev: 0A
Date: Monday, December 20, 2010 | Sheet 21 of 35

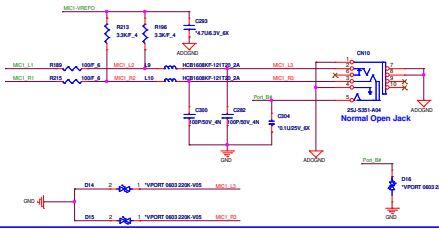
Codec (CX20671-21Z) <ADO> <EMI>



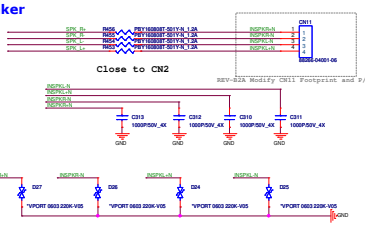
HP <ADO> <EMC>



External MIC <ADO> <EMC>



Internal Speaker <ADO> <EMC>



Quanta Computer Inc.

PROJECT : BU5

Size: A4 | Document Number: Audio Codec(CX20671-21Z) | Rev: 2A

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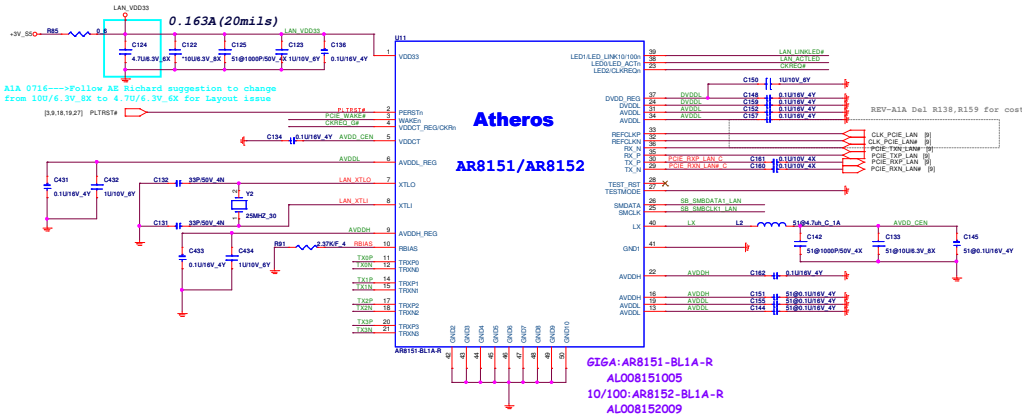
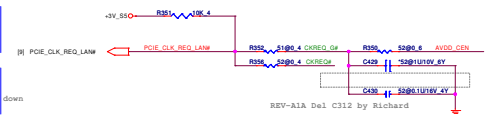
Atheros Lan <LAN> <LNG>

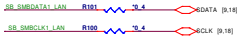


<LAN> <LNG> <LN1>

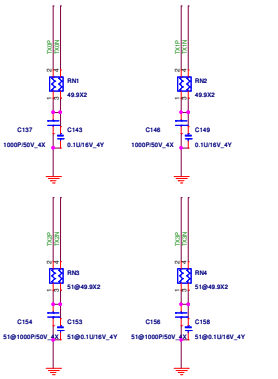


LAN-Wake up function <LAN>

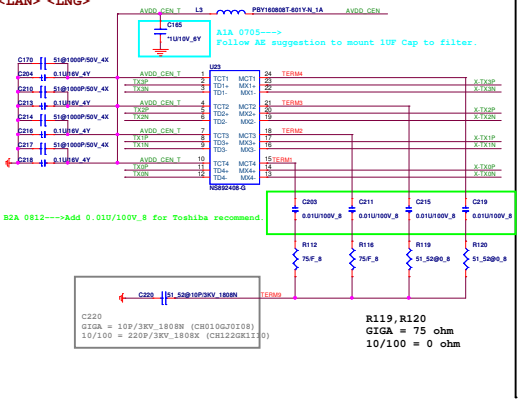
LAN-SM-Bus <LAN>



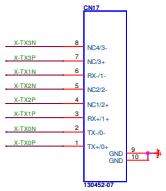
PLACE NEAR LAN IC SIDE <LAN> <LNG>



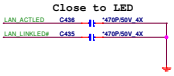
TRANSFORMER <LAN> <LNG>



RJ45 <LAN> <LNG> <LN1>



Close to LED



Power on Strapping pin

LED0 = LAN_ACTLED	1	Over-clocking enable (default = 1)
	0	Over-clocking disable
LED1 = LAN_LINKLED#	1	SWR switch-mode regulator select Giga LAN pull High (default = 1)
	0	LDO linear regulator select 10/100M LAN pull Low
CKREQ# or CKREQ_G#	1	Normal function
	0	ATE test mode

Quanta Computer Inc.

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Size	Document Number	Rev
	Atheros Lan	2A
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3 IN 1 CARD READER

REV-A1A change to daughtor board

3 IN 1 CARD READER

Quanta Computer Inc.

PROJECT : BU5

Size	Document Number	Rev
	Card Reader (RTS5138)	2A

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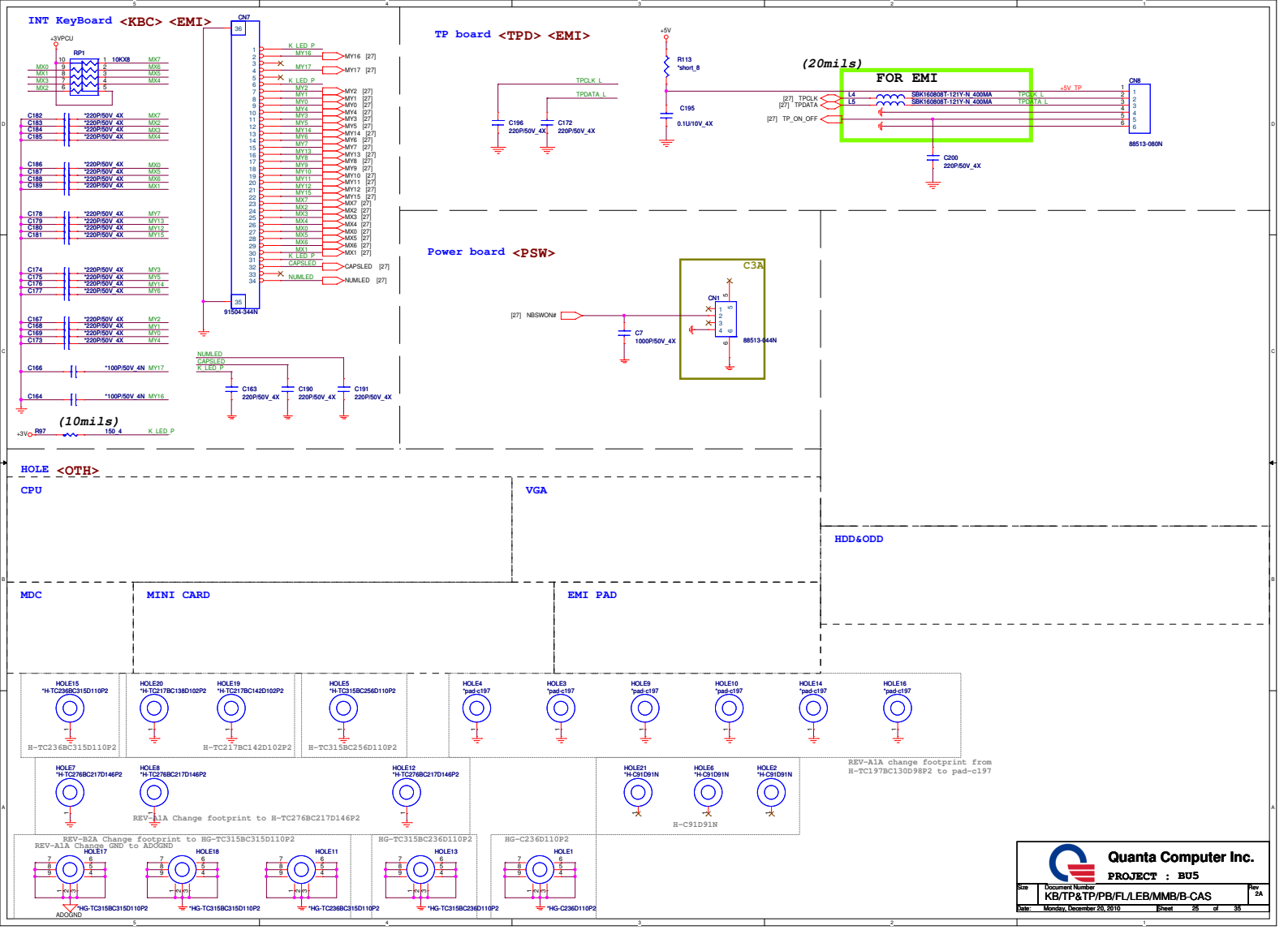
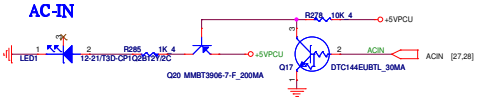

INT KeyBoard <KBC> <EMI>
TP board <TPD> <EMI>
Power board <PSW>
FOR EMI
(20mils)
(10mils)
HOLE <OTH>
CPU
VGA
HDD&ODD
MDC
MINI CARD
EMI PAD
REV-A1A Change footprint to H-TC276BC217D146P2
REV-B2A Change footprint to HG-TC315BC315D110P2
REV-A1A Change GND to ADGND
REV-A1A change footprint from H-TC197BC130D98P2 to pad-c197
H-C91D91N
Quanta Computer Inc.
PROJECT : BU5
KB/TP&TP/PB/FL/LEB/MMB/B-CAS
Monday, December 20, 2010

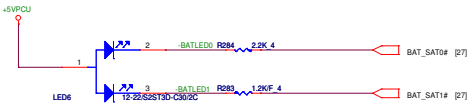
LED <LED>

AC-IN



BATERRY

D3A : LED luminance to light,1K-ohm change 2.2K-ohm.

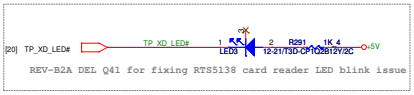


RF LED

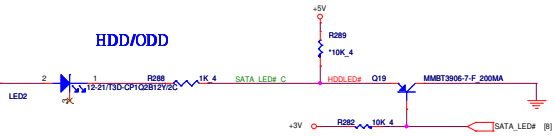
POWER

D3A : LED luminance to light,1K-ohm change 2.2K-ohm.

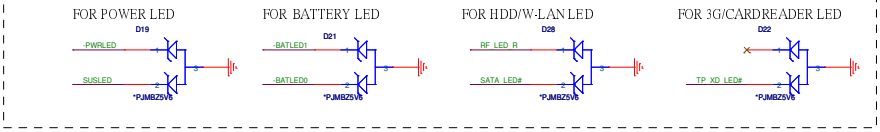
CARDREADER



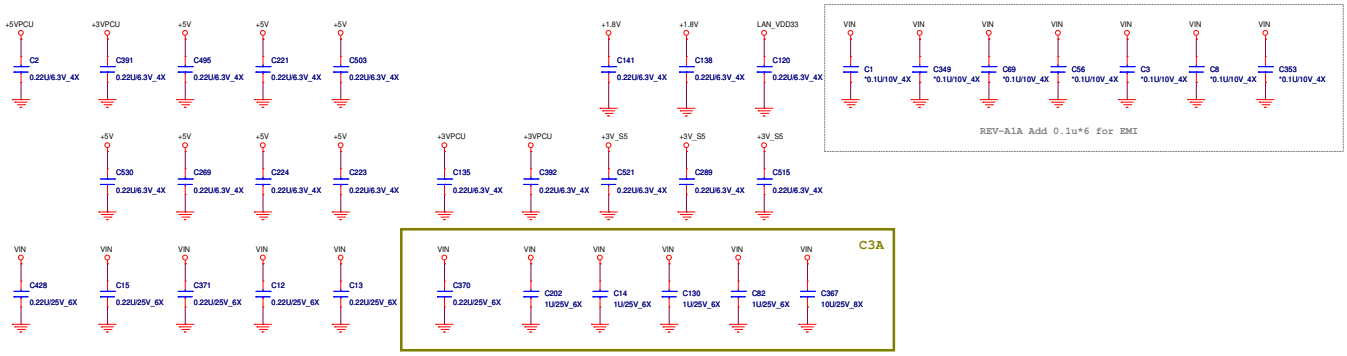
HDD/ODD



ESD Protect <EMC>



<EMI>



Quanta Computer Inc.

PROJECT : BU5

Size	Document Number	Rev
	LED/HOLE	2A
Date: Monday, December 20, 2010	Sheet 26 of 35	

EC <KBC>

Intel Turbo mode only <CPU>

SM BUS PU/Address <KBC>

3Cell Battery protect & K/B LED Control <KBC>

Strap <KBC>

ID EEPROM <KBC>

SPI FLASH <KBC>

INTERNAL KEYBOARD STRIP SET <KBC>

HWPG circuit <KBC>

SKU strap pin <KBC>

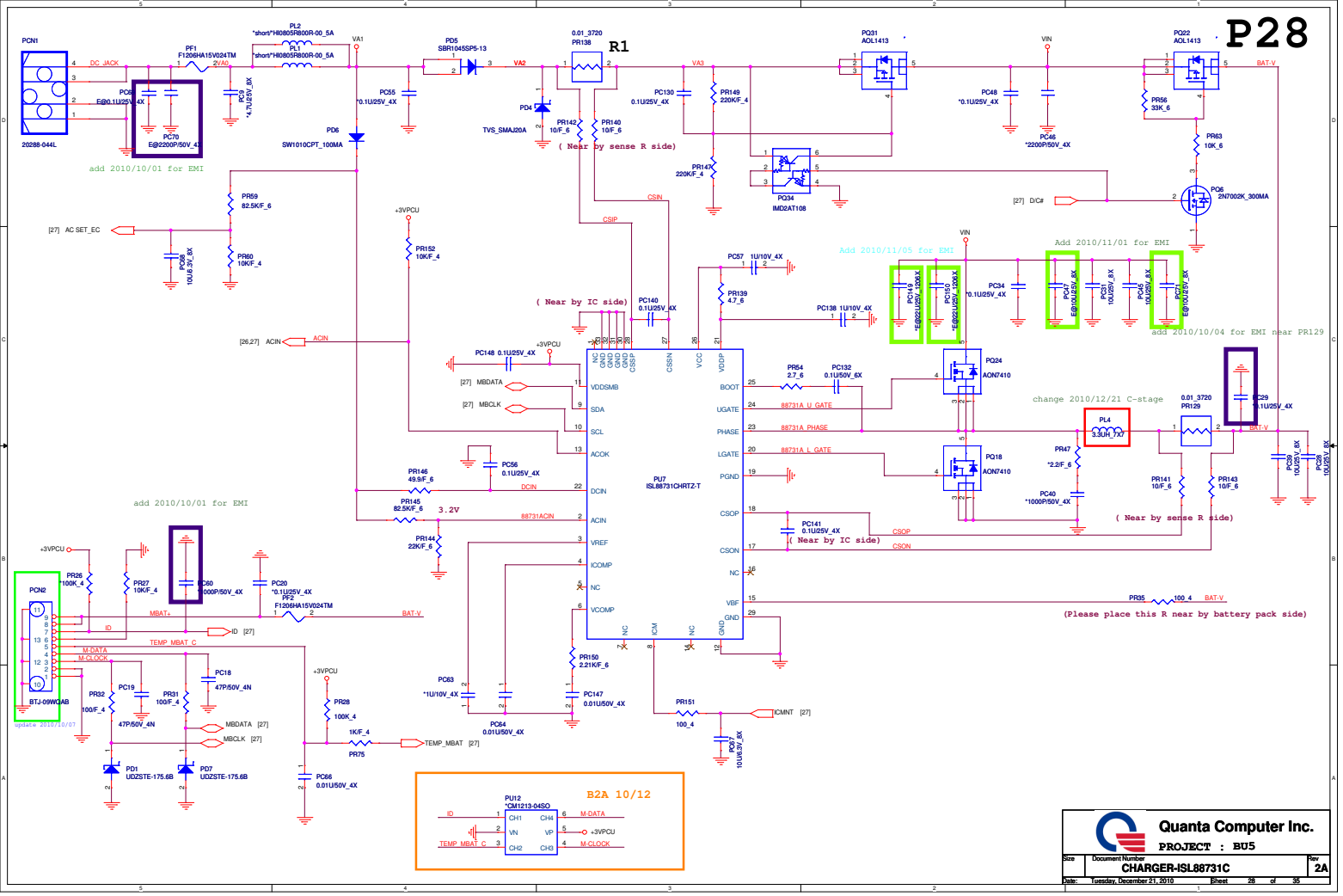
Power Button <KBC>

LED PU/PD <LED>

SMBUS Table

SMBUS	Devices	Address
1	Battery	12H
2	CPU Board Thermal Sensor	
	EC EEPROM	A0H
3	VGA Board Thermal Sensor	98H

Quanta Computer Inc.
PROJECT : BU5
EC NPCE791LA0DX
Date: Monday, December 20, 2010 Sheet 27 of 35


P28
R1
PCN1
20288-044L
DC_JACK
PF1
F1206HA15V024TM
2VA0
PL2
*short*HI0805R800R-00_5A
PL1
*short*HI0805R800R-00_5A
VA1
PD5
SBR1045SP5-13
VA2
0.01_3720
PR138
PD4
TVS_SMAJ20A
PR142
10/F_6
PR140
10/F_6
(Near by sense R side)
VA3
PC130
0.1U/25V_4X
PR149
220K/F_4
PR143
220K/F_4
PQ34
IMD2AT108
PQ31
AOL1413
VIN
PC48
*0.1U/25V_4X
PC46
*2200P/50V_4X
PQ22
AOL1413
BAT-V
PR56
33K_6
PR63
10K_6
PQ6
2N7002K_300MA
[27] D/C#
PC55
*0.1U/25V_4X
PD6
SW1010CPT_100MA
PC69
E@0.1U/25V_4X
PC70
E@2200P/50V_4X
PC68
*4.7U/25V_6X
add 2010/10/01 for EMI
PR59
82.5K/F_6
PR60
10K/F_4
[27] AC SET_EC
PC58
10U/6.3V_6X
+3VPCU
PR152
10K/F_4
CSIN
CSIP
(Near by IC side)
PC140
0.1U/25V_4X
PC57
1U/10V_4X
PR139
4.7_6
PC138
1U/10V_4X
Add 2010/11/05 for EMI
Add 2010/11/01 for EMI
PC149
*E@22U/25V_1206X
PC150
*E@22U/25V_1206X
PC34
*0.1U/25V_4X
PC47
E@10U/25V_6X
PC51
10U/25V_6X
PC45
10U/25V_6X
PC52
E@10U/25V_6X
add 2010/10/04 for EMI near PR129
[26,27] ACIN
ACIN
PC148
0.1U/25V_4X
[27] MBDATA
[27] MBCLK
PC56
0.1U/25V_4X
PR146
49.9/F_6
PR145
82.5K/F_6
3.2V
DCIN
88731ACIN
PR144
22K/F_6
PU7
ISL88731CHRTZ-T
NC
GND
GND
GND
CSSP
CSSN
VCC
VDDP
VDDSMB
SDA
SCL
ACOK
DCIN
ACIN
VREF
ICOMP
NC
VCOMP
BOOT
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC
VBF
GND
PR54
2.7_6
PC132
0.1U/50V_6X
88731A_U_GATE
88731A_PHASE
88731A_L_GATE
PQ24
AON7410
PQ18
AON7410
change 2010/12/21 C-stage
PL4
3.3UH_7X7
PR47
*2.2/F_6
PC40
*1000P/50V_4X
0.01_3720
PR129
PC29
0.1U/25V_4X
PR141
10/F_6
PR143
10/F_6
PC27
10U/25V_6X
PC28
10U/25V_6X
(Near by sense R side)
PC141
0.1U/25V_4X
(Near by IC side)
CSOP
CSON
PR35
100_4
BAT-V
(Please place this R near by battery pack side)
PR150
2.21K/F_6
PC147
0.01U/50V_4X
PR151
100_4
ICMNT [27]
PC63
*1U/10V_4X
PC64
0.01U/50V_4X
PC37
10U/6.3V_6X
add 2010/10/01 for EMI
PC60
*1000P/50V_4X
PC20
*0.1U/25V_4X
PF2
F1206HA15V024TM
MBAT+
BAT-V
PCN2
BTJ-099WCAB
update 2010/10/07
PR26
100K_4
PR27
10K/F_4
ID
ID [27]
TEMP_MBAT_C
M-DATA
M-CLOCK
PC19
47P/50V_4N
PC18
47P/50V_4N
PR32
100/F_4
PR31
100/F_4
MBDATA [27]
MBCLK [27]
PD1
UDZSTE-175.6B
PD7
UDZSTE-175.6B
+3VPCU
PR28
100K_4
1K/F_4
PR75
TEMP_MBAT [27]
PC66
0.01U/50V_4X
PU12
*CM1213-04SO
CH1
CH4
VN
VP
CH2
CH3
M-DATA
+3VPCU
M-CLOCK
B2A 10/12
Quanta Computer Inc.
PROJECT : BU5
Size
Document Number
CHARGER-ISL88731C
Rev
2A
Date: Tuesday, December 21, 2010
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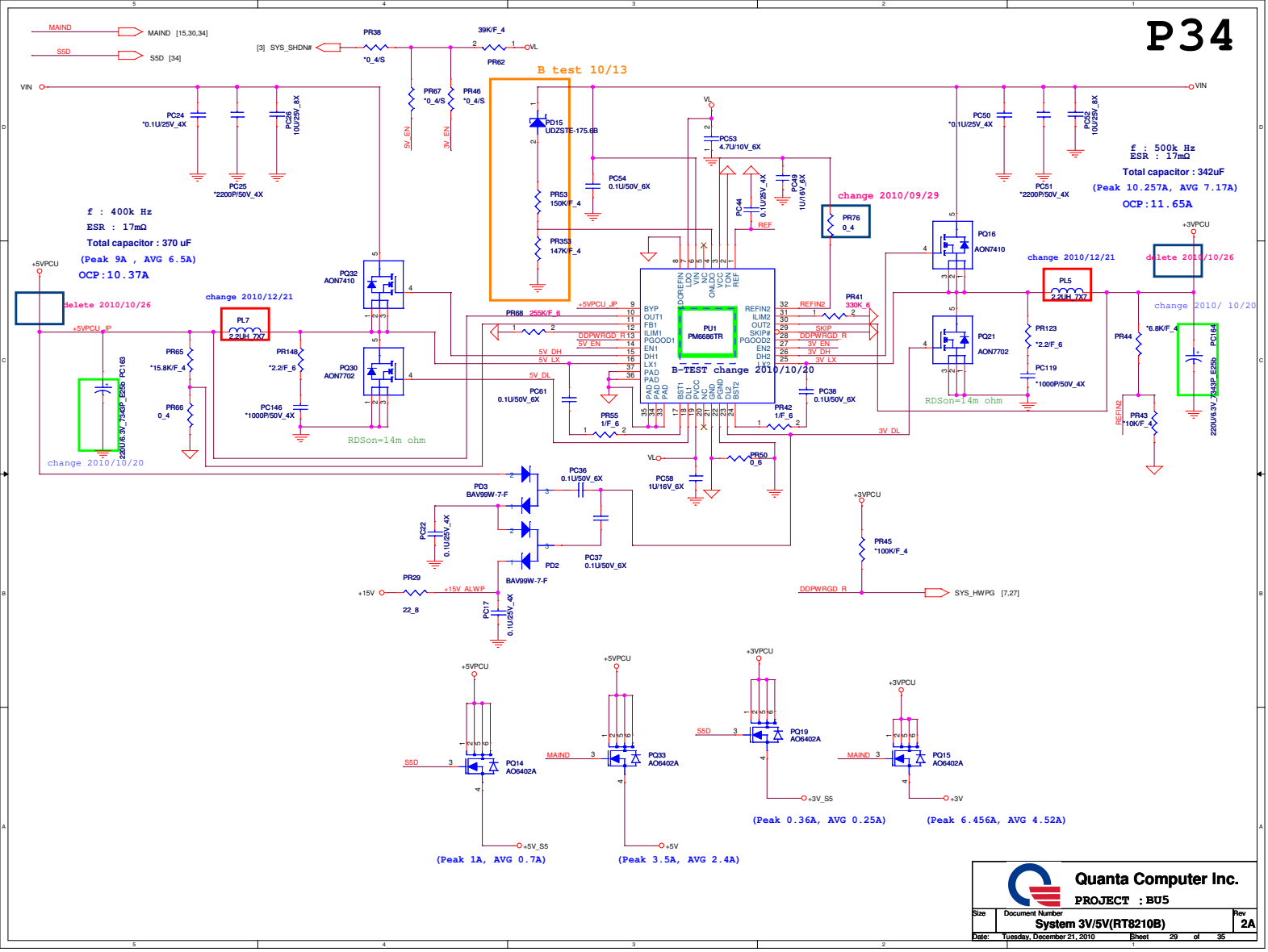
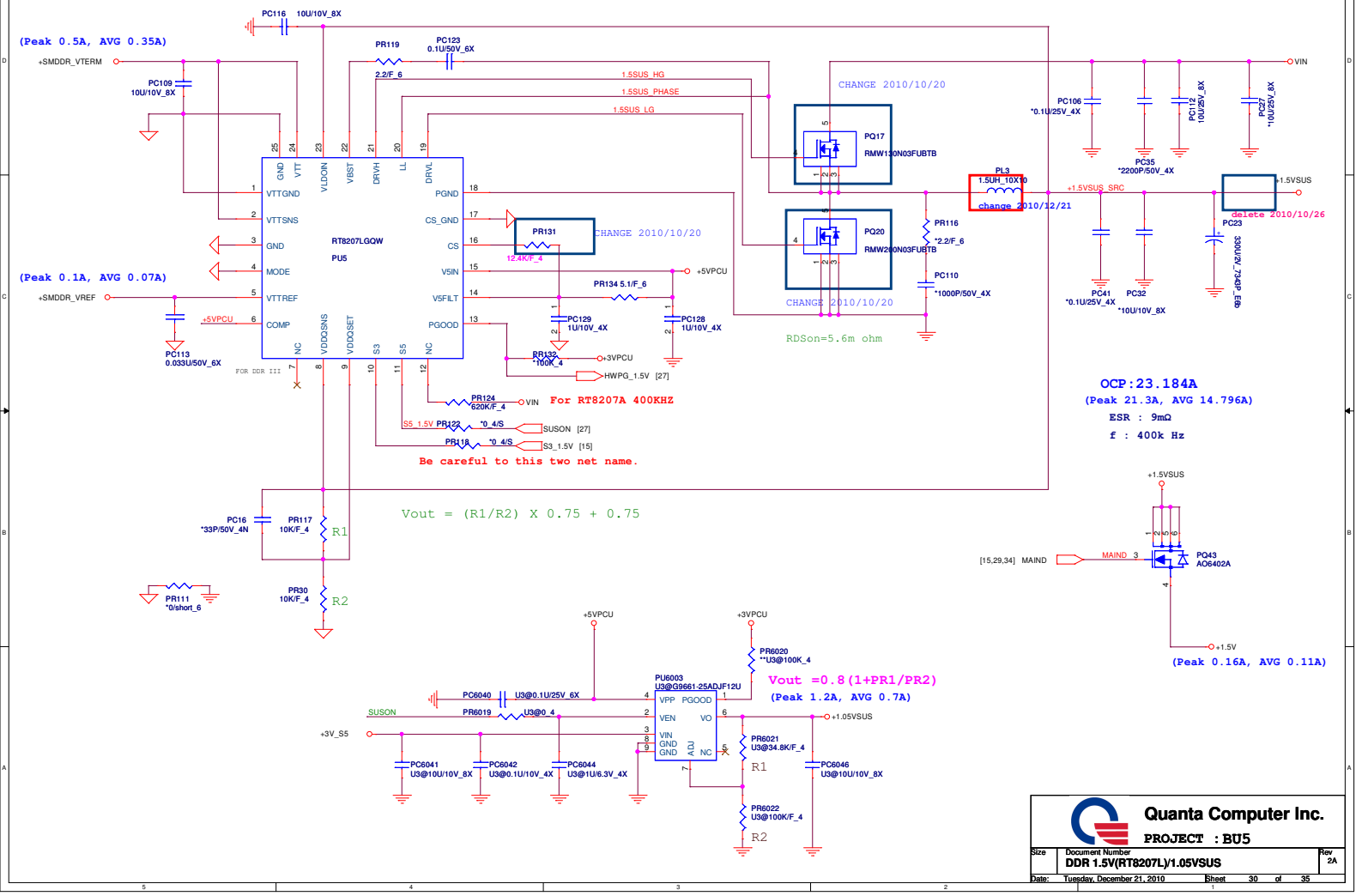


Quanta Computer Inc.

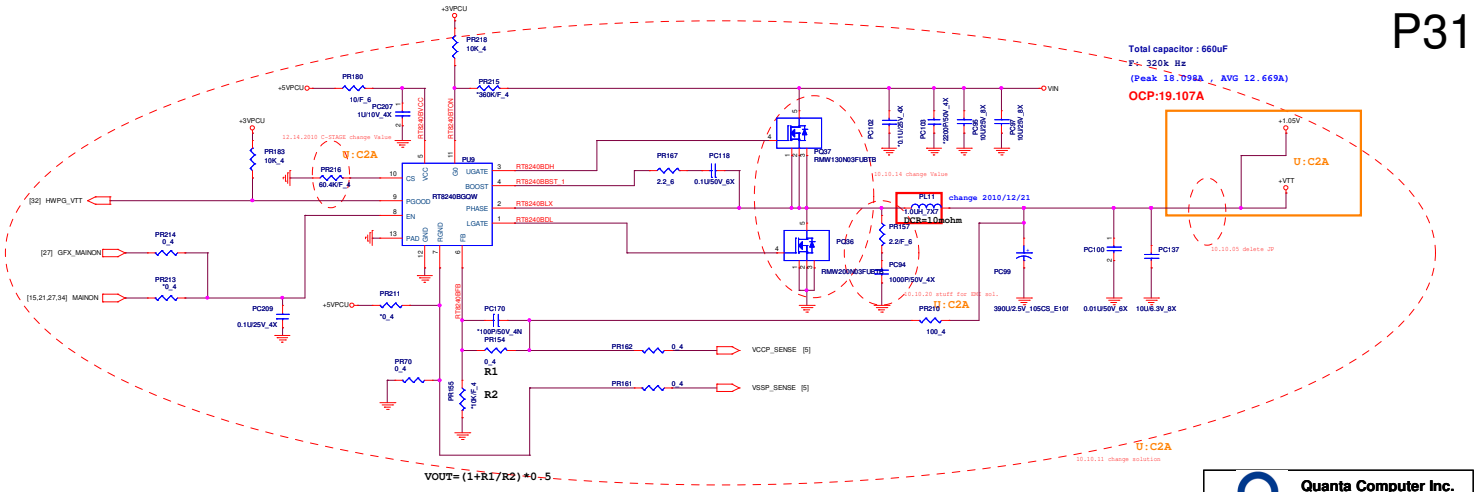
PROJECT : BU5

Size	Document Number	Rev
	System 3V/5V(RT8210B)	2A

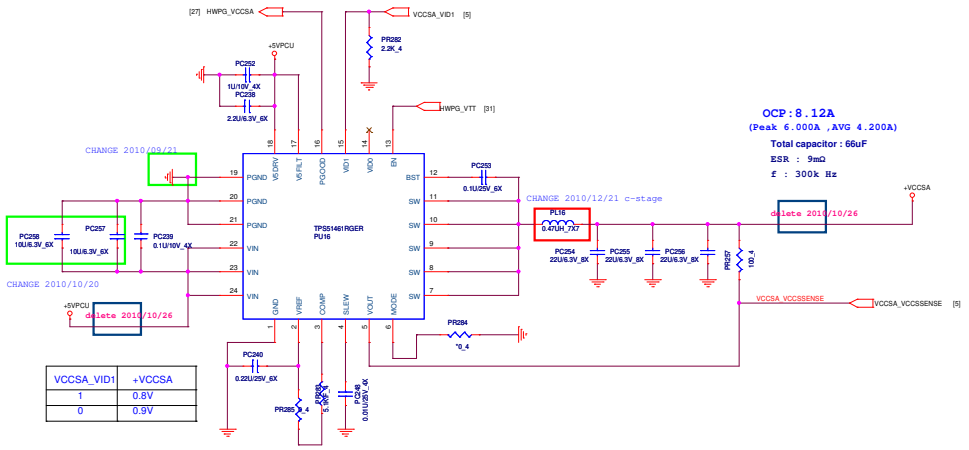
Date: Tuesday, December 21, 2010 Sheet 29 of 35



Quanta Computer Inc.		
PROJECT : BU5		
Size	Document Number: DDR 1.5V(RT8207L)/1.05VSUS	Rev: 2A
Date: Tuesday, December 21, 2010	Sheet 30 of 35	



Quanta Computer Inc.		
PROJECT : BU5		
Size	Document Number	Rev
	+VTT /+1.05V(RT8240B)	2A
Date: Tuesday, December 21, 2010	Sheet 31 of 35	



OCP : 8.12A
(Peak 6.000A ,AVG 4.200A)
Total capacitor : 66uF
ESR : 9mΩ
f : 300k Hz

VCCSA_VID1	+VCCSA
1	0.8V
0	0.9V

Quanta Computer Inc.
PROJECT : BU5

Size	Document Number	Rev
		2A

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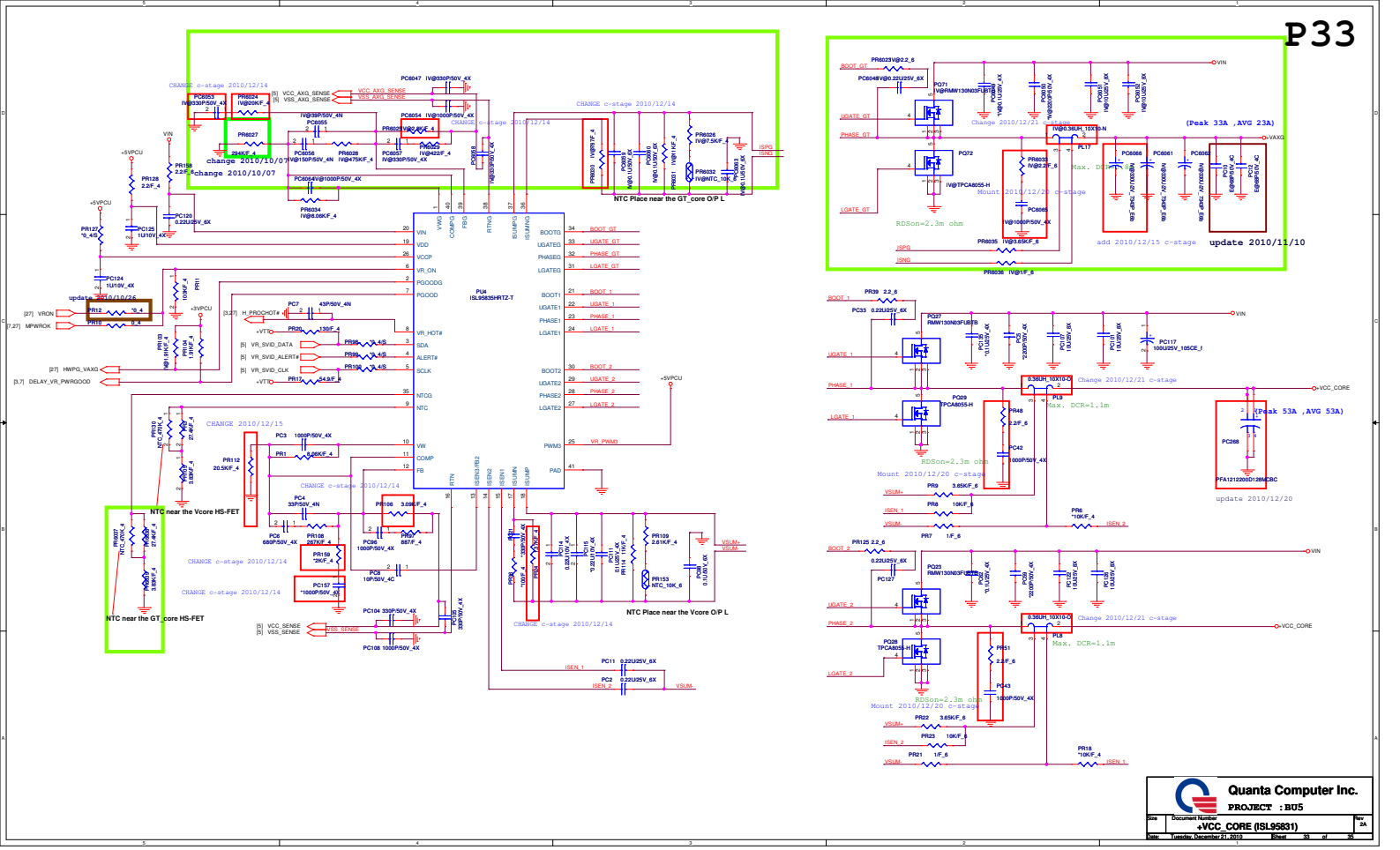

Quanta Computer Inc.			
PROJECT : BU5			
Size	Document Number		Rev
	+VCC_CORE (ISL95831)		2A
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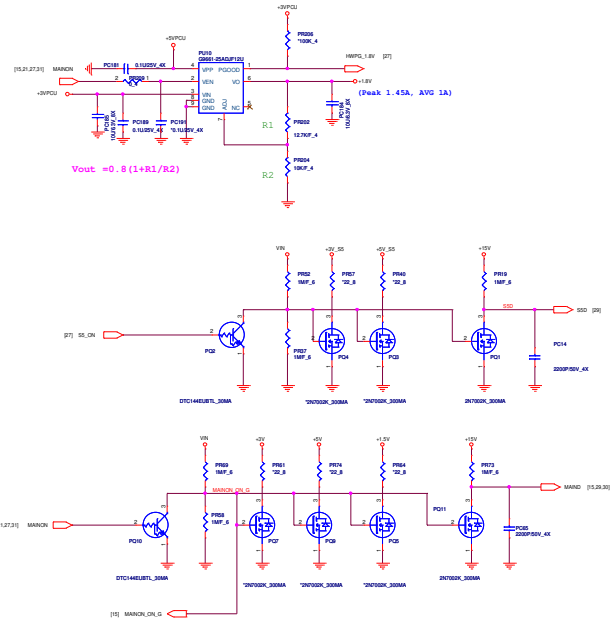
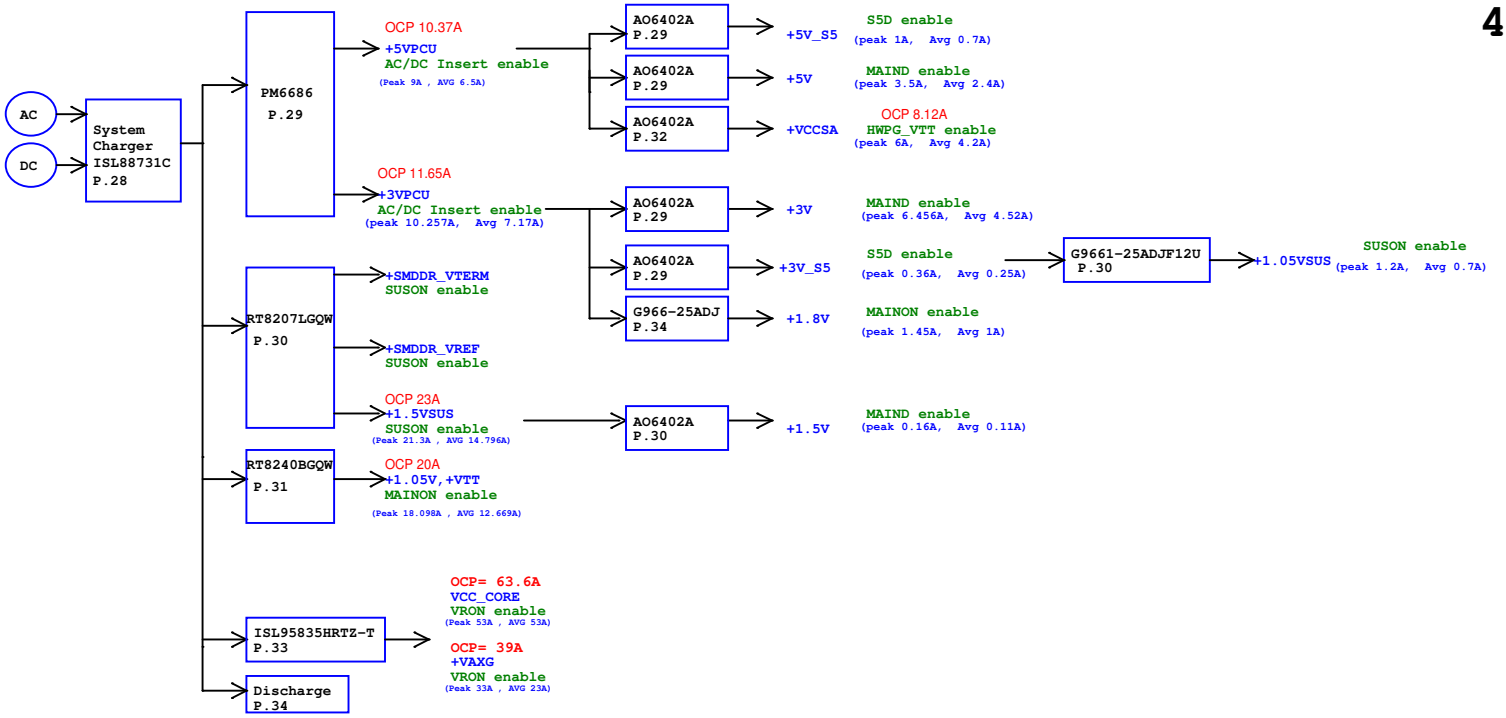
P34



Quanta Computer Inc.

PROJECT : BU5

Size	Document Number	Rev
	Discharge	2A
Date:	Tuesday, December 21, 2010	Sheet 34 of 35



Quanta Computer Inc.
PROJECT : BU5
Size | Document Number: POWER TREE TABLE | Rev 2A
Date: Tuesday, December 21, 2010 | Sheet 35 of 36