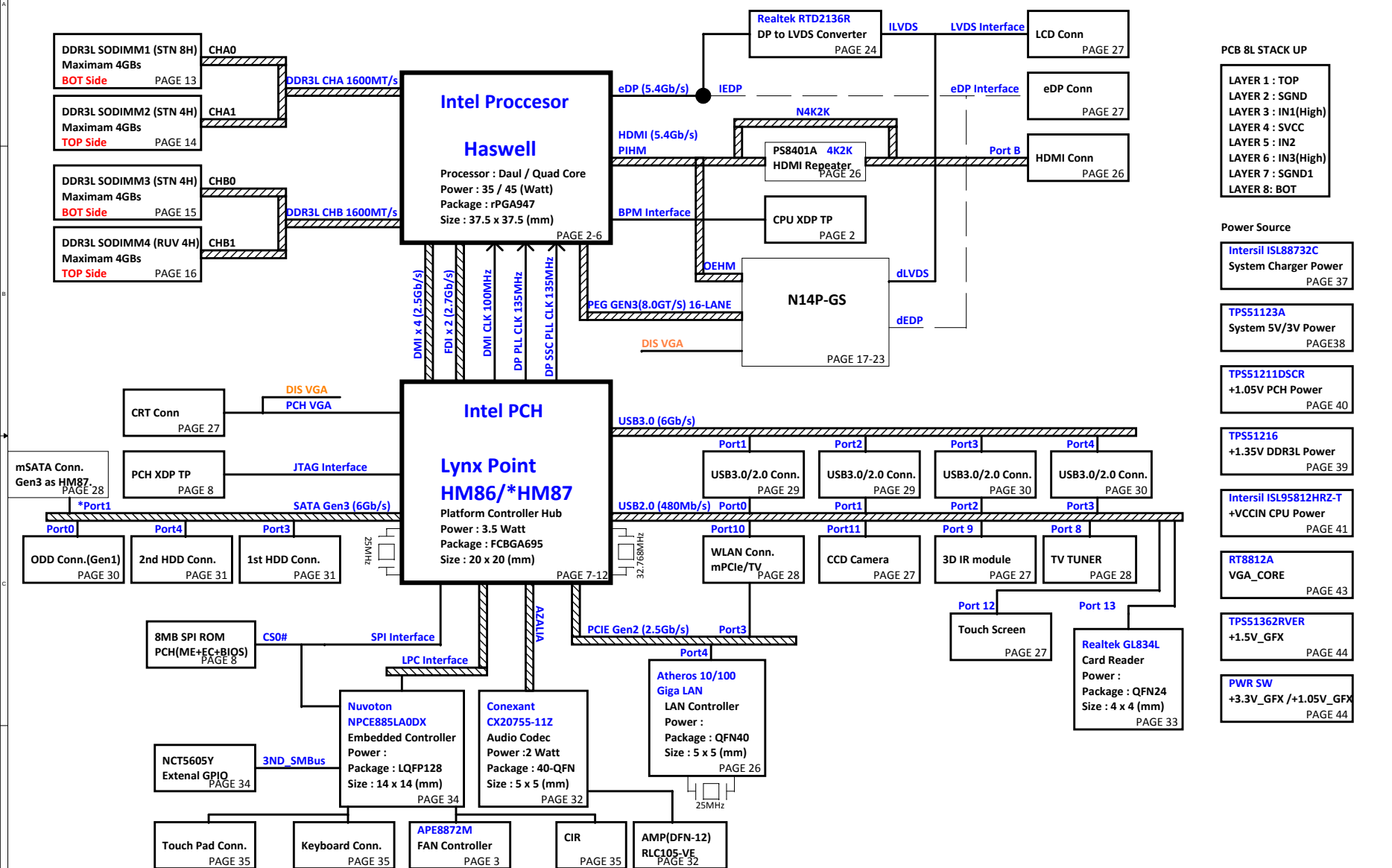
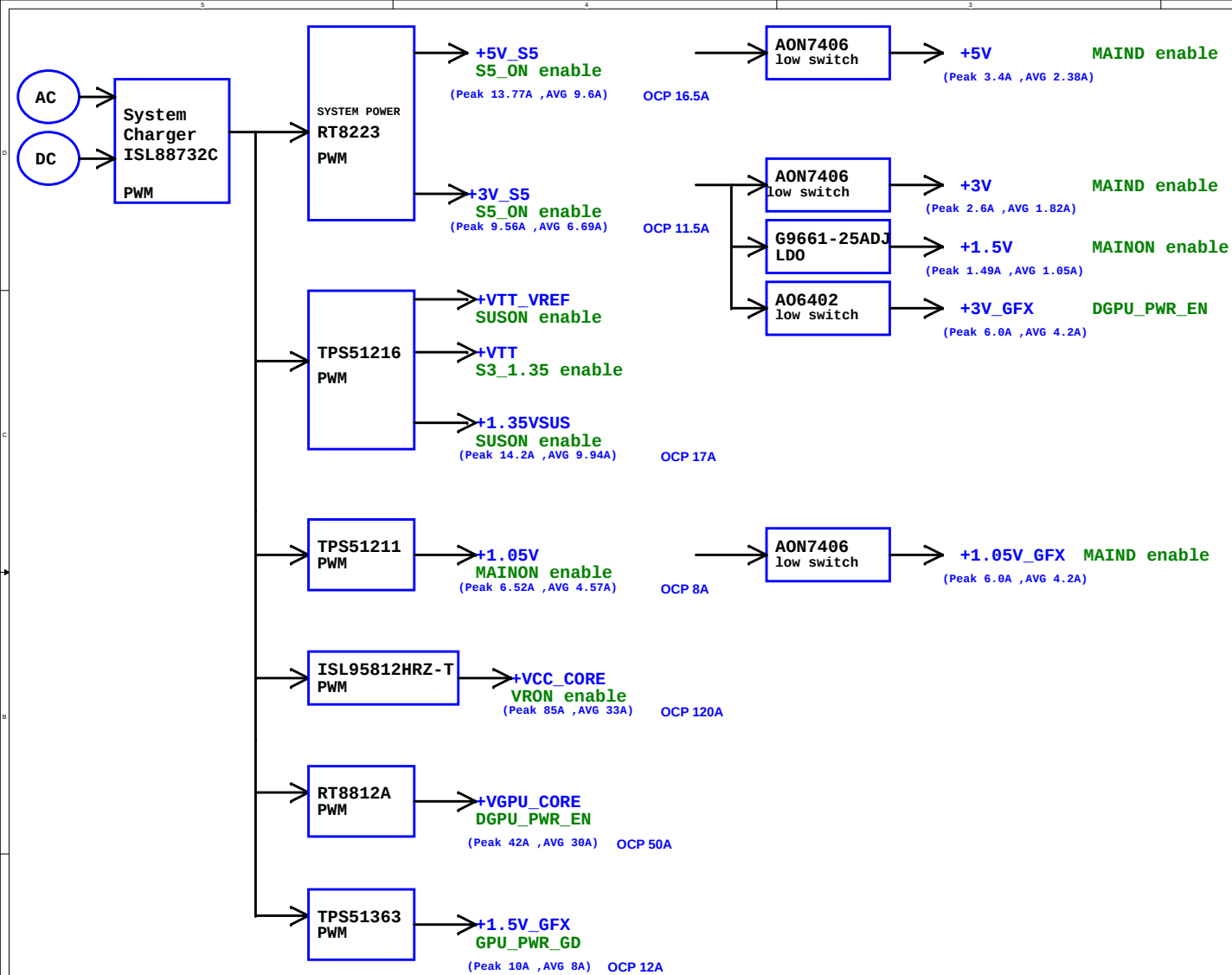


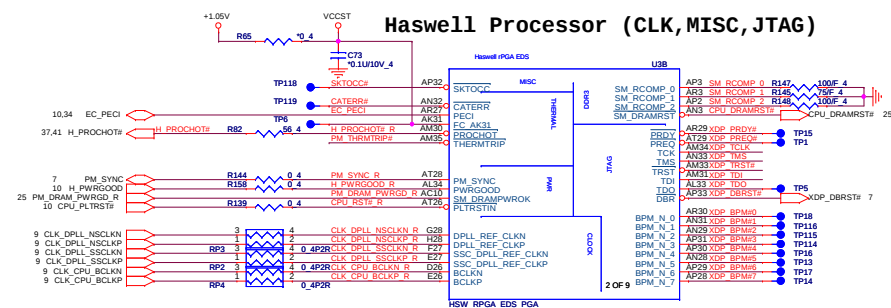
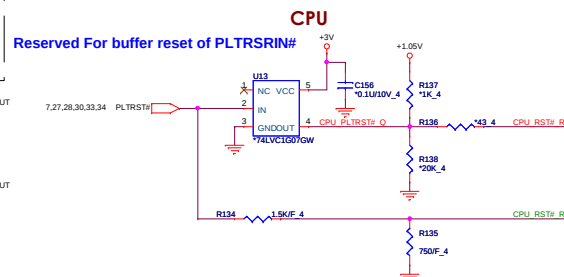
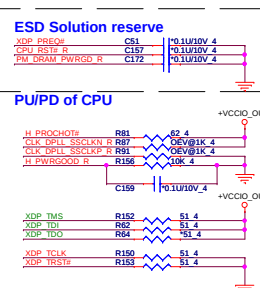
(17.3") Intel Shark Bay Platform Block Diagram

01

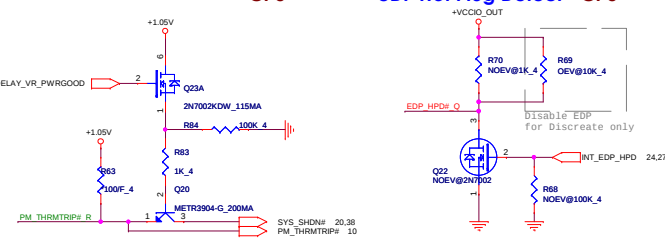




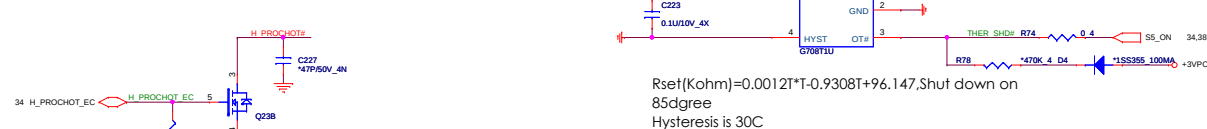
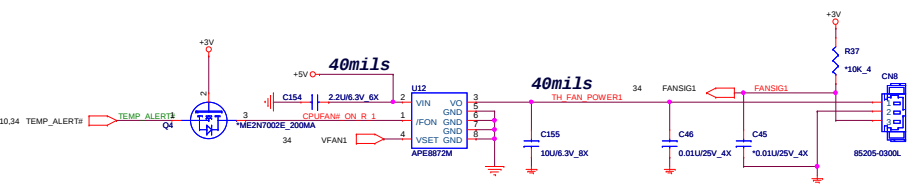
POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0-S5
+VCCRTC	+3.0V~+3.3V		S0-S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0-S5
+3V_HDP	+3.3V	MAIN_ON	S0
+3VPCU	+3.3V	AC/DC Insert enable	S0
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0-S5
+5VPCU	+5V	AC/DC Insert enable	S0-S5
WIMAX_P	+3.3V	WMAX_P for WLAN	
+1.5V	+1.5V	MAIN_ON	S0
+1.35V_SUS	+1.35V	SUSON	S0-S3
+VCC_CORE		VRON	S0
+1.05V	+1.05V	MAIN_ON	S0

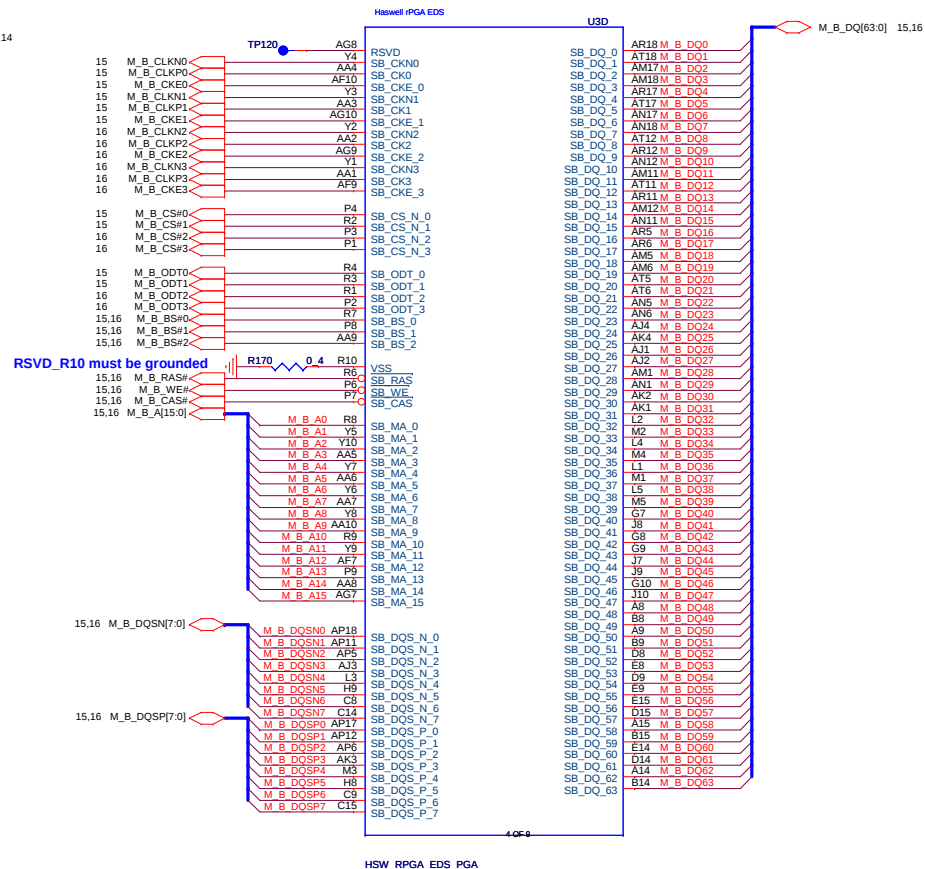
[illegible]

eDP Hot Plug Detect CPU



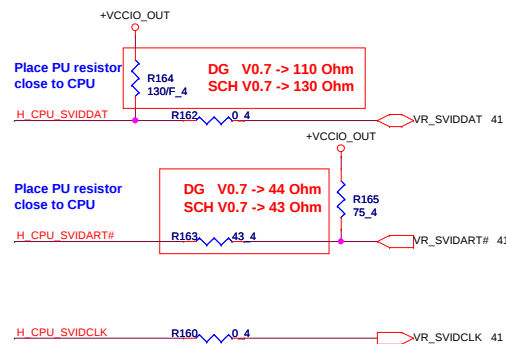
<THC>







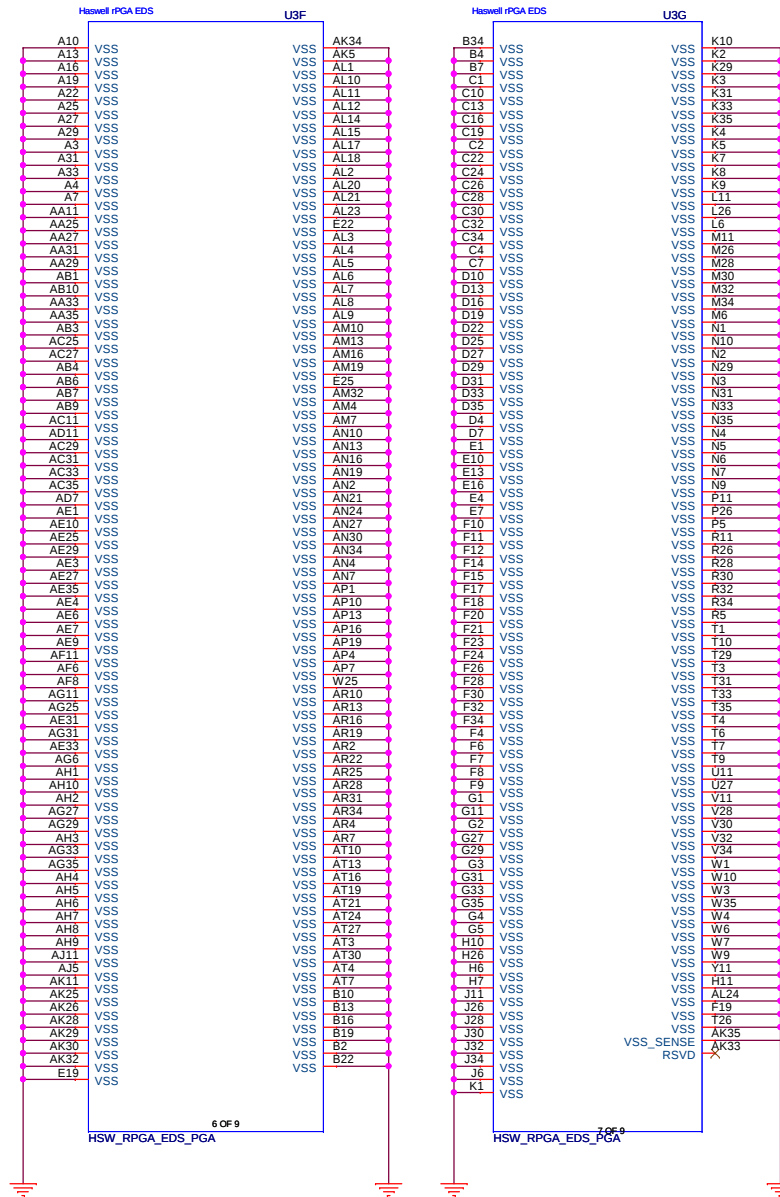
Layout note: need routing together and ALERT need between CLK and DATA.



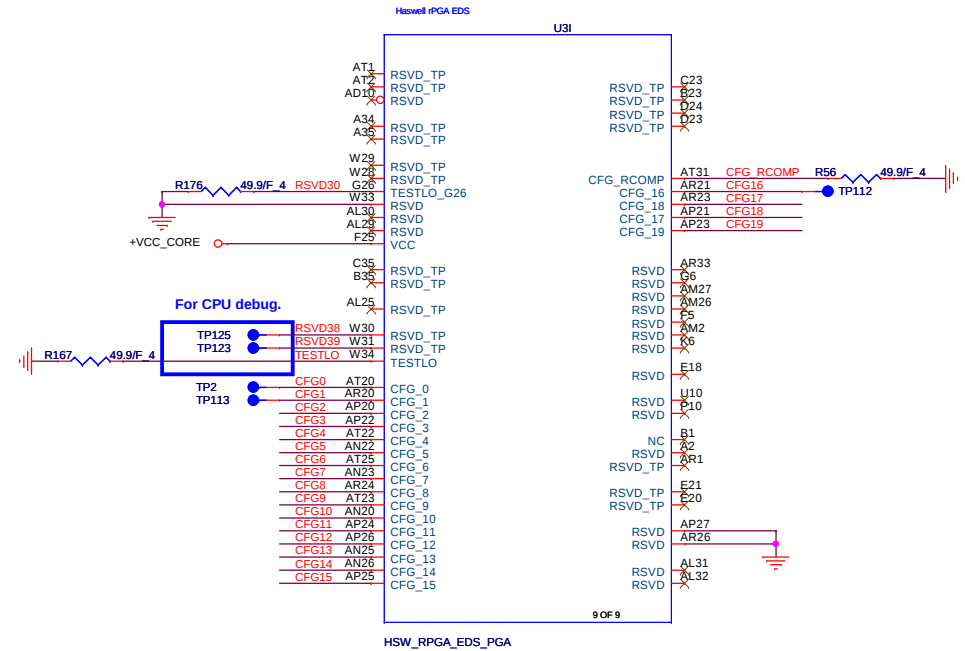
Quanta Computer Inc.
PROJECT : BDBE

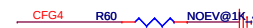
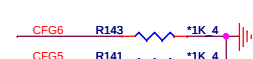
Size	Document Number	Revised
	Haswell 4/5 (POWER)	
Date:	Monday, December 17, 2012	Sheet 5 of 45

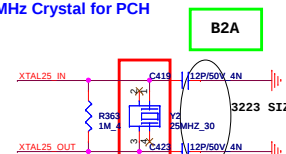
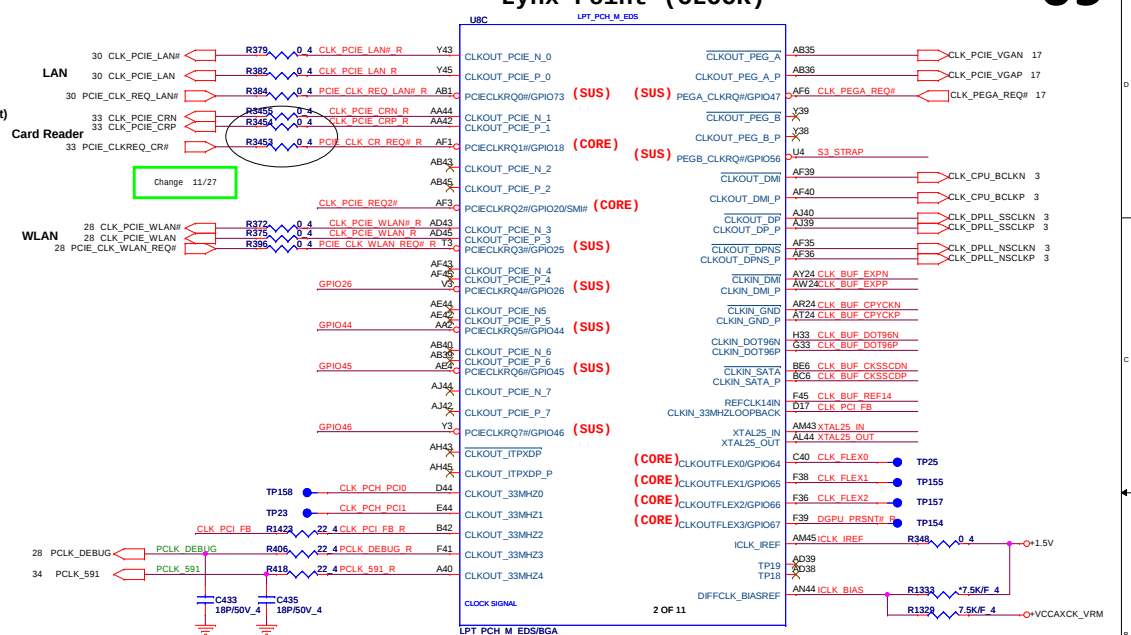
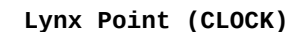
Haswell Processor (GND)



Haswell Processor (CFG, RSVD)

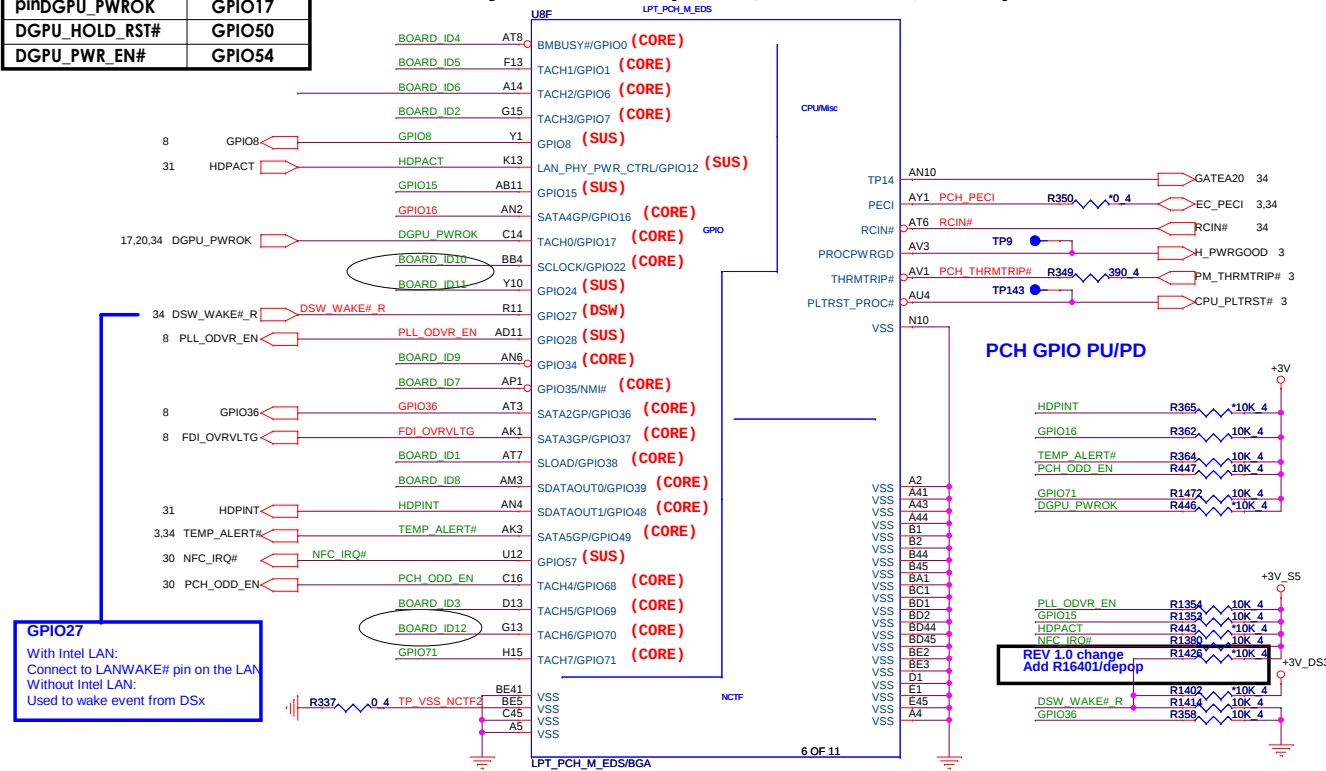


Configuration Signals:		The CFG signals have a default value of '1' if not terminated on the board.
CFG[2]	PCI Express Static Lane Reversal	x1 = Normal operation x0 = Lane numbers reversed 
CFG[4]	eDP enable	x1 = Disabled x0 = Enabled 
CFG[6:5]	PCI Express Bifurcation	x00 = 1 x8 & 2 x4 PCI Express x01 = reserved x10 = 2 x8 PCI Express x11 = 1 x16 PCI Express 
CFG[7]	PEG defer training	x1 = PEG train follow RESETB de-asserted x0 = PEG wait for BIOS fro training 



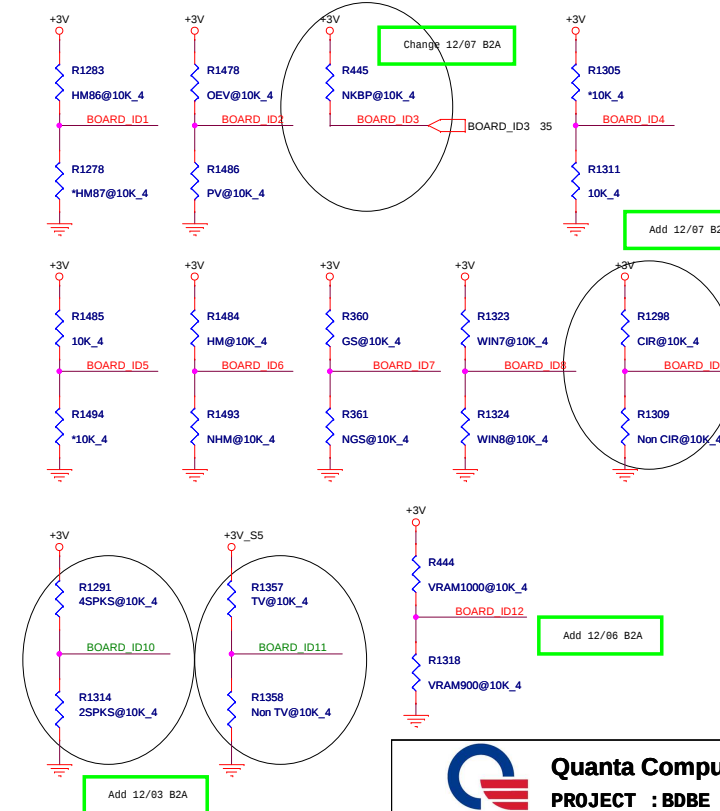
OPTIMUS POWER PCH control	
pinDGPU_PWROK	GPIO17
DGPU_HOLD_RST#	GPIO50
DGPU_PWR_EN#	GPIO54

Lynx Point (GPIO,CPU/MISC,NCTF)

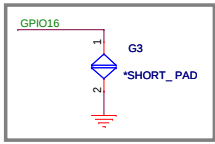


BOARD ID SETTING CLG/PX/OEV/UGA/CLG-Strap

Board ID	ID1	ID2	ID3	ID4	ID5	ID6	ID7	ID8	ID9	ID10	ID11	ID12
HM86 HM87	H L											
Only VGA OPTIMUS		H L										
W/O LED KB W/ LED KB			H L									
UMA Discrete				H L								
17" Premium 17" Gaming					H L							
W/ HDMI W/O HDMI						H L						
W/ G-sensor W/O G-sensor							H L					
WIN7 WIN8								H L				
W/ CIR W/O CIR									H L			
4 SPKS 2 SPKS										H L		
TV SKU SSD SKU											H L	
VRAM 1000 VRAM 900												H L



PU & Password Clear

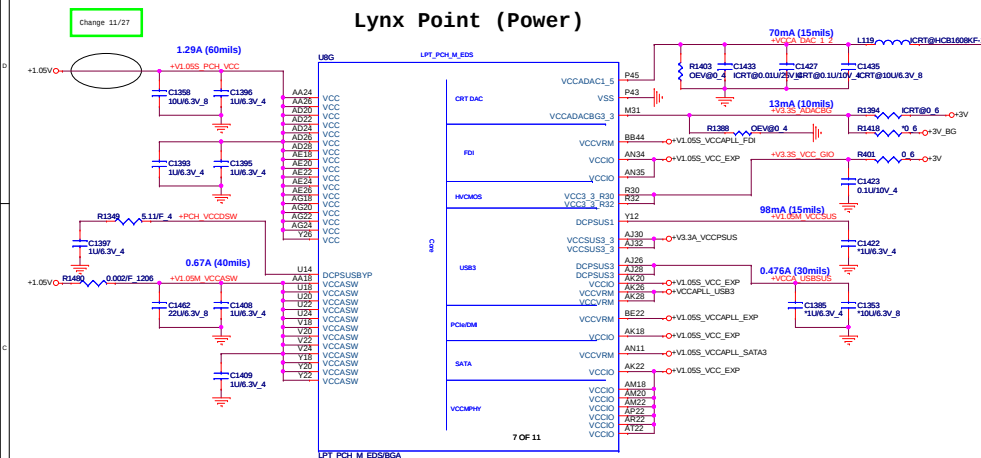


REV-B2A Add G3 for Clear CMOS password

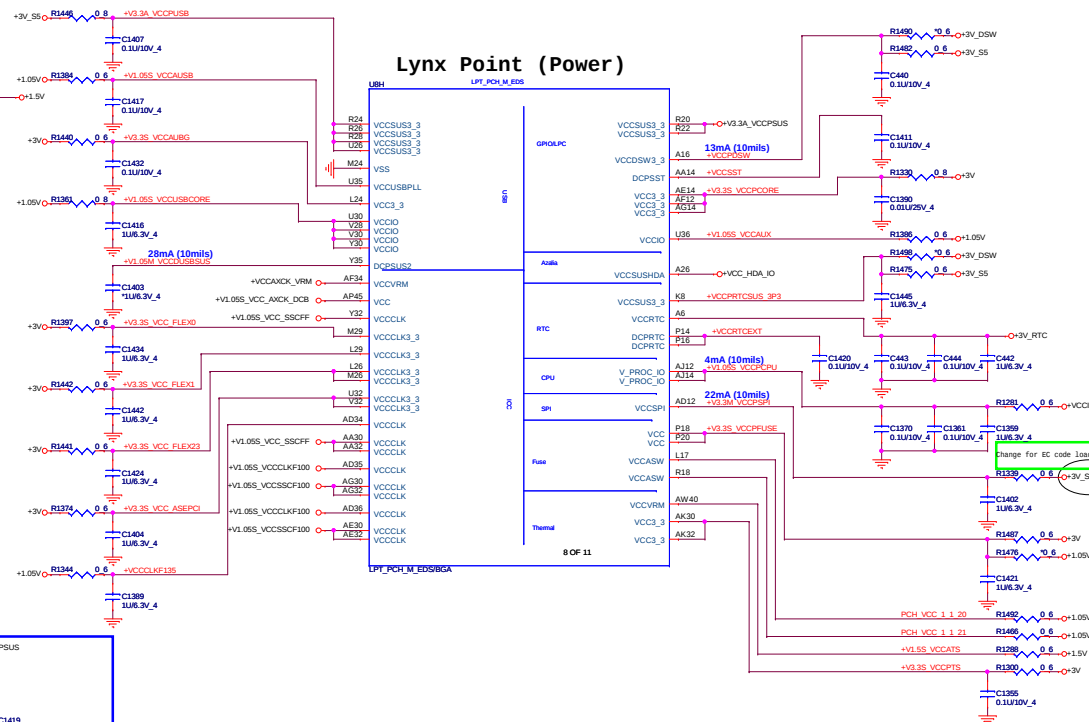
Quanta Computer Inc.
PROJECT : BDBE

Size	Document Number	Rev
	LPT 4/6 (GPIO/MISC)	1A
Date:	Monday, December 17, 2012	Sheet 10 of 45

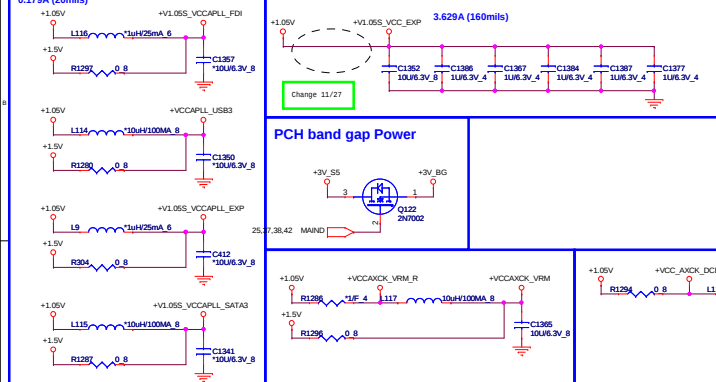
Lynx Point (Power)



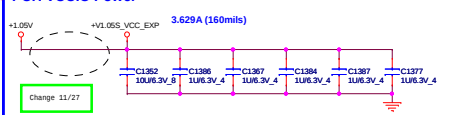
Lynx Point (Power)



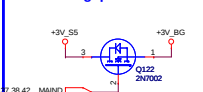
PCH VRM Power 1.05V OPTION IS PROVIDED FOR VALIDATION PURPOSES
0.179A (20mils)



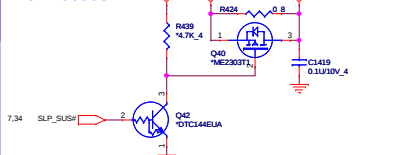
3 PCH VCCIO Power



PCH band gap Power



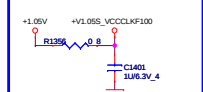
PCH VCCSUS

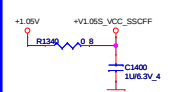


BCH HDA Power 0

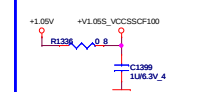


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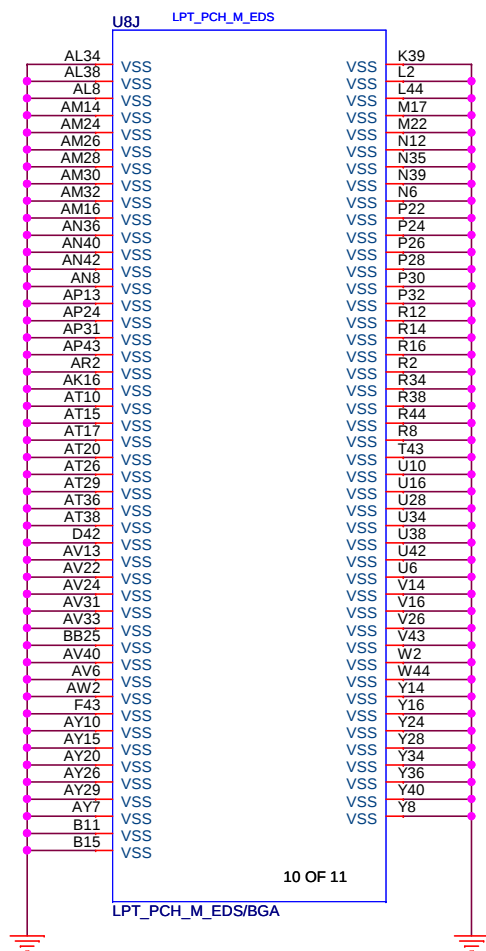




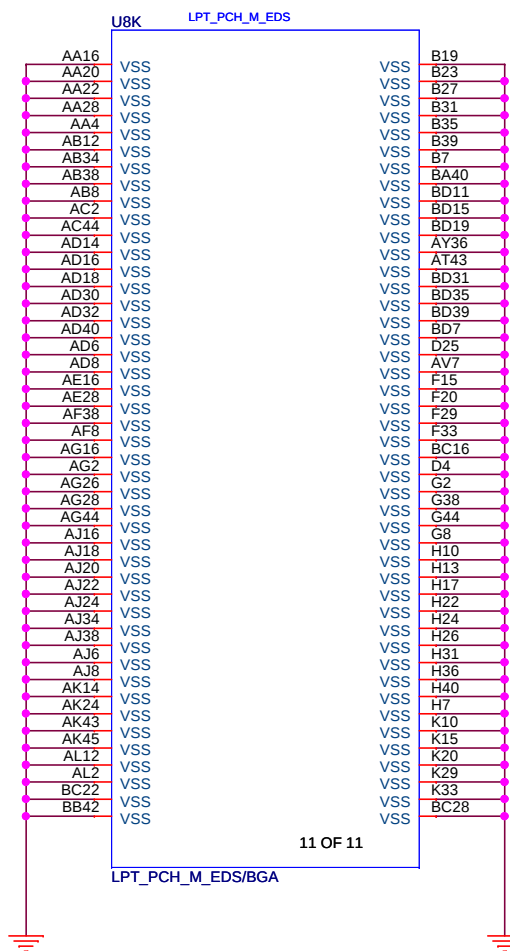
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Lynx Point (GND)



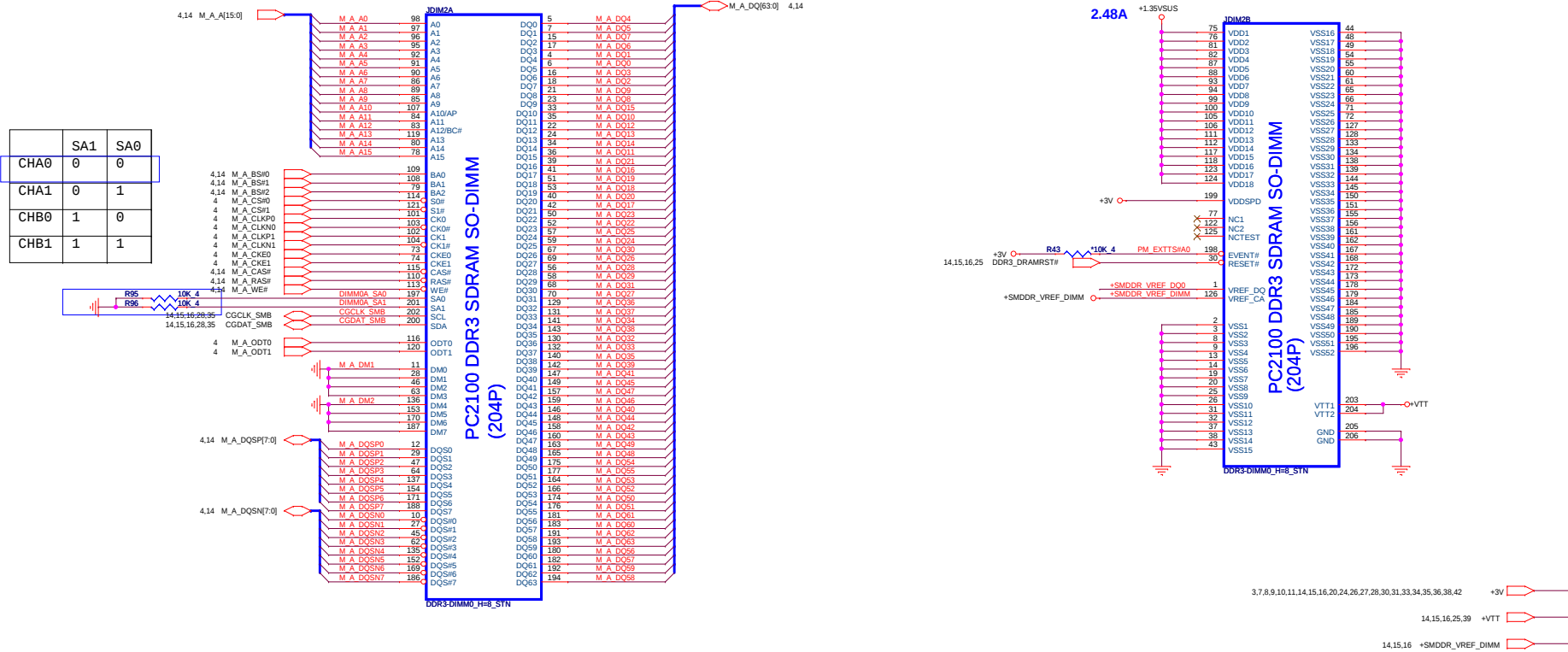
Lynx Point (GND)



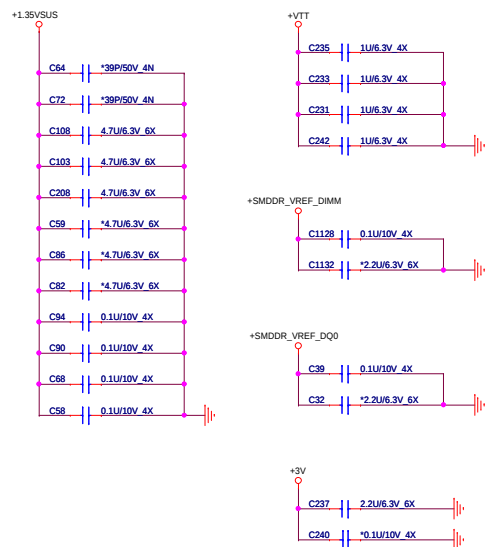
Quanta Computer Inc.
PROJECT : BDBE

Size	Document Number	Rev 1A
LPT 6/6 (GND)		
Date:	Monday, December 17, 2012	Sheet 12 of 45

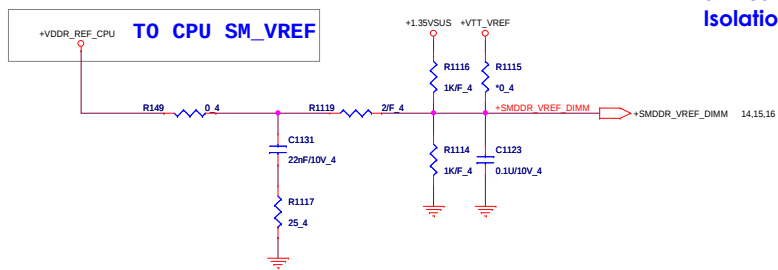
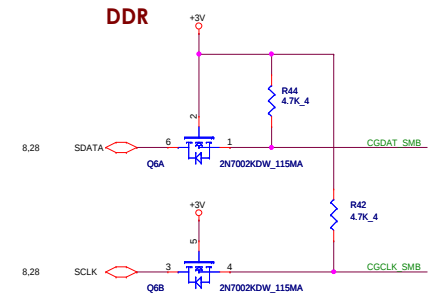
BOT Side Close to CPU



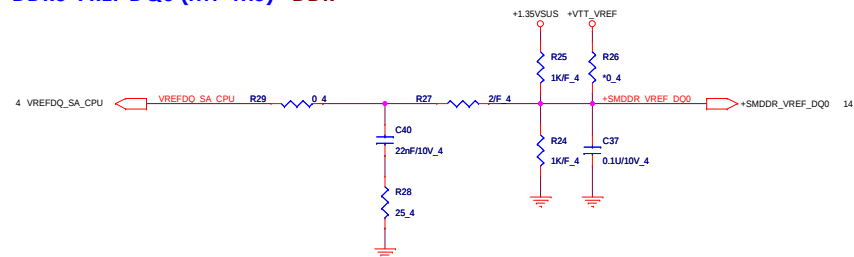
Place these Caps near So-Dimm0.

DDR3 VREF
CA

DDR

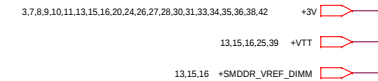
SMBus
Isolation

DDR3 VREF DQ0 (M1+M3) DDR



ESD Solution Reserve



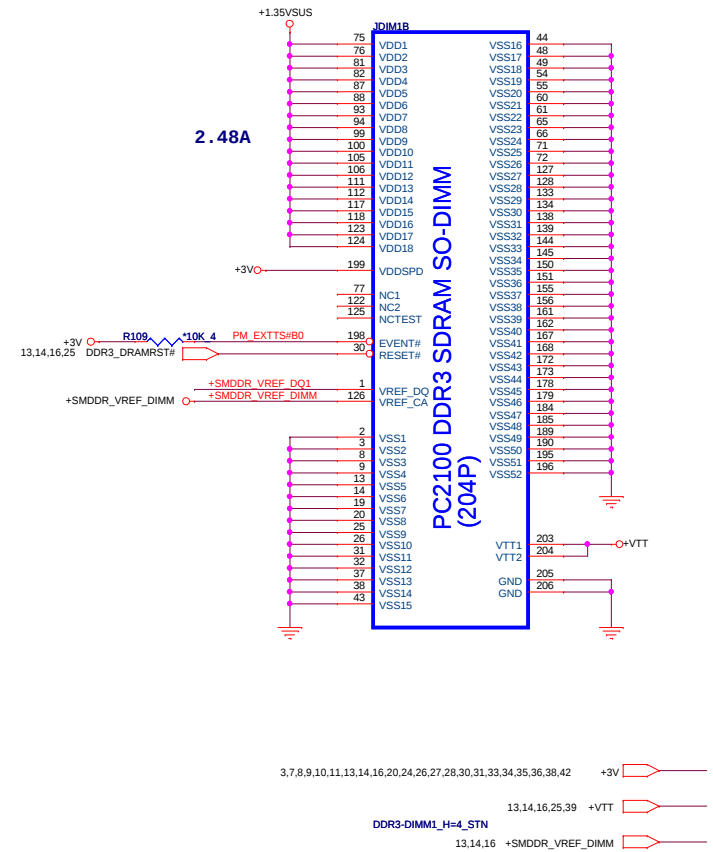
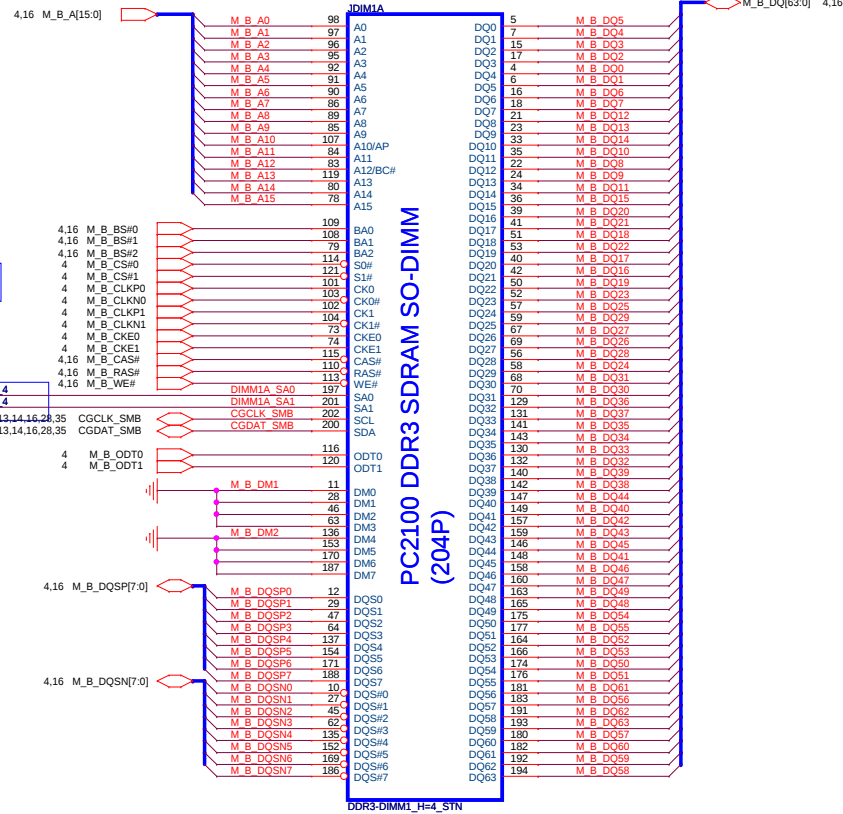
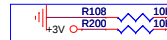


ESD Solution Reserve

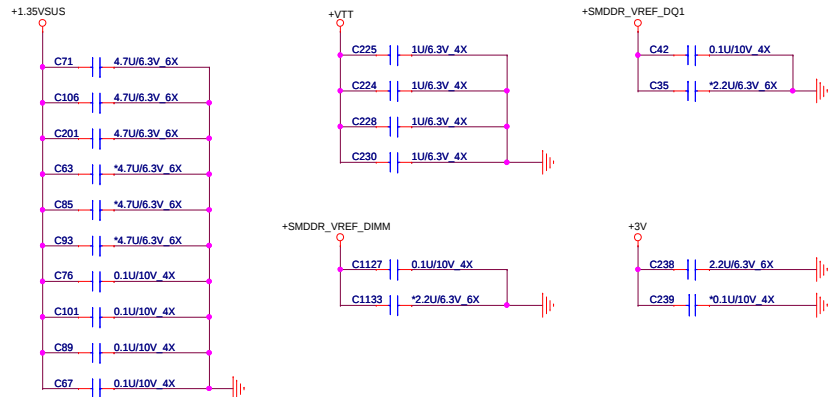


BOT Side Far away CPU

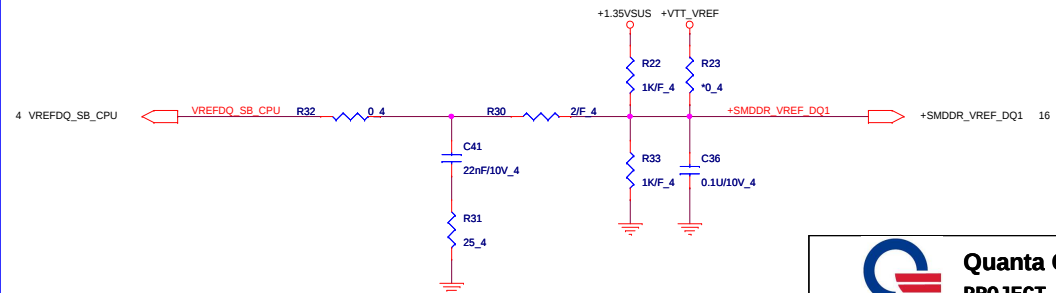
	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1



Place these Caps near So-Dimm1.

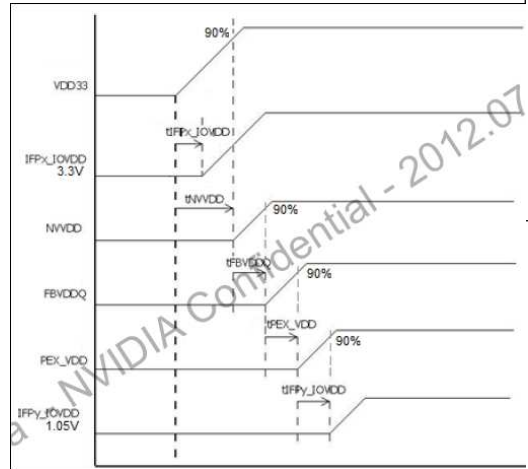
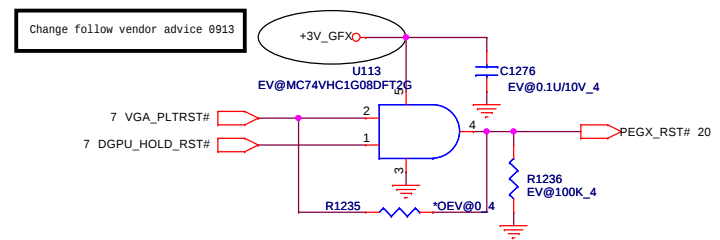
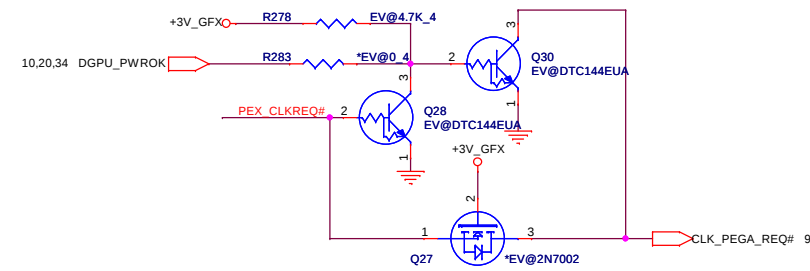


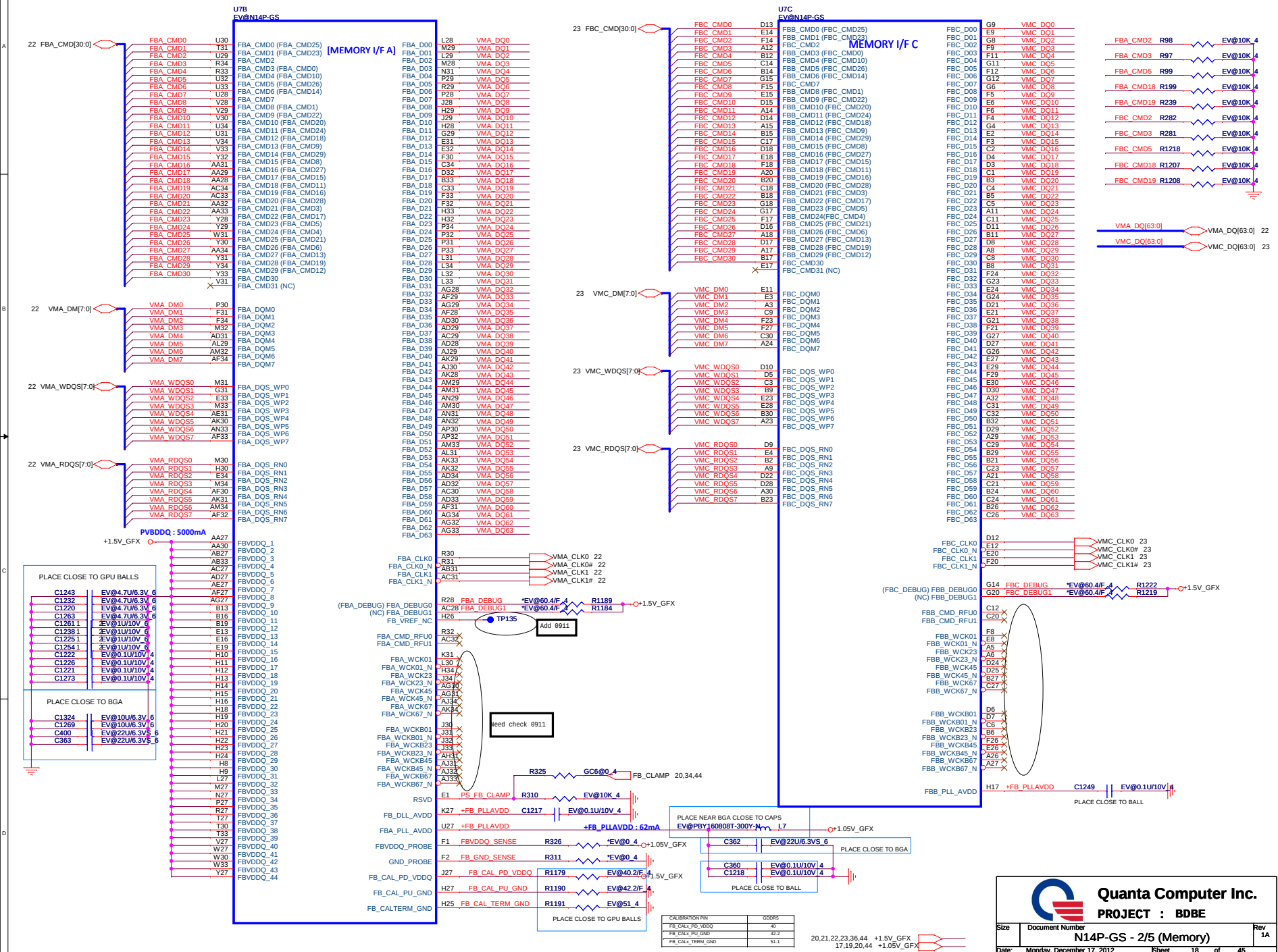
DDR3 VREF DQ1 (M1+M3) **DDR**

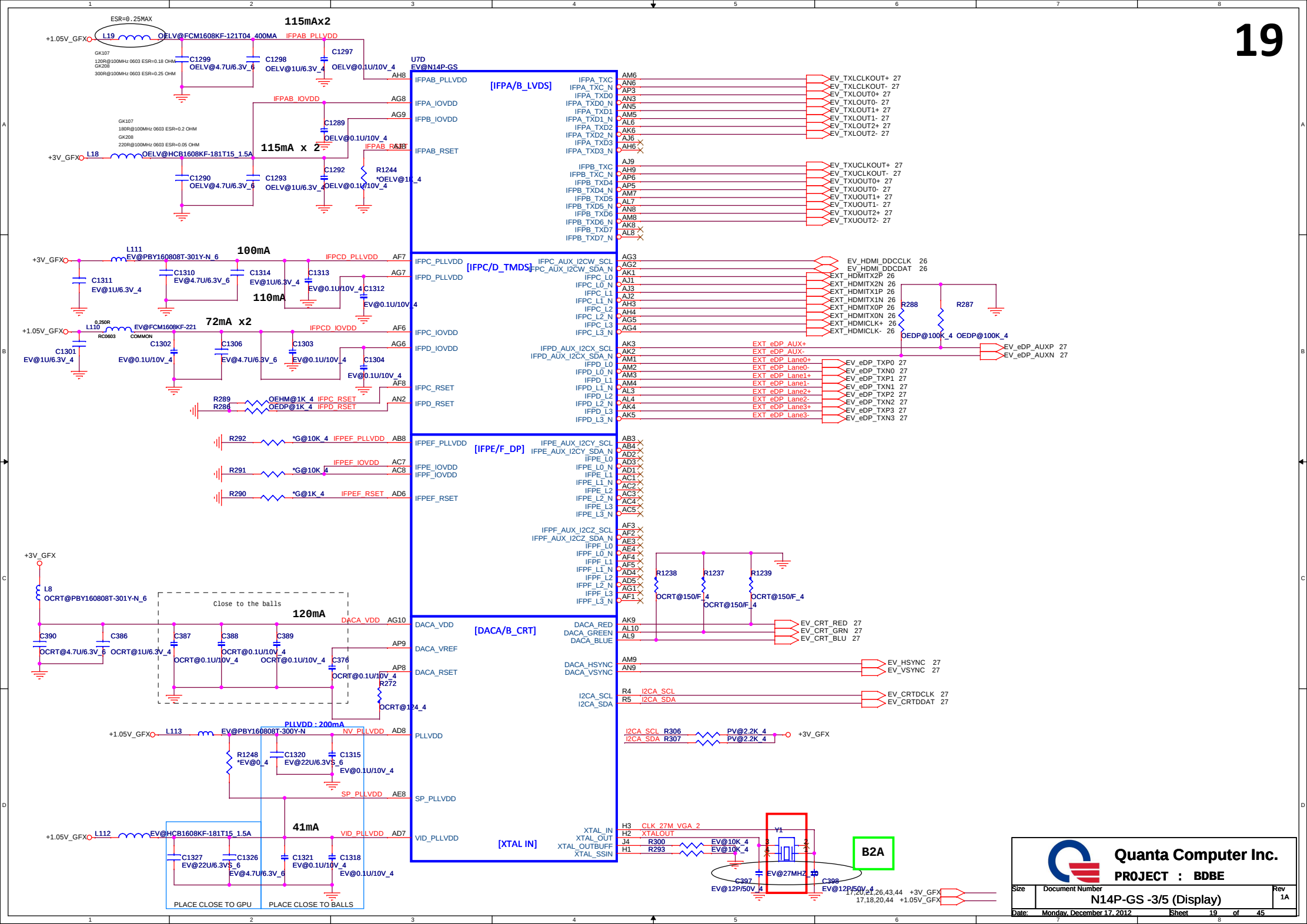


ESD Solution Reserve









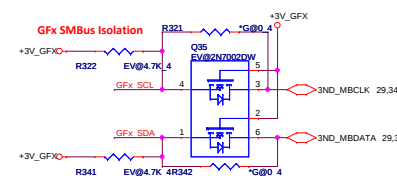
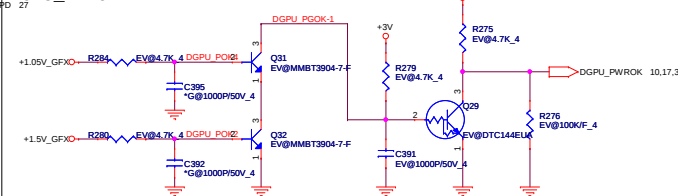


VRAM (DDR3L / 900MHz) Configuration Table ROM_SI	
2G Samsung 128Mx16	15K PU
2G Micron 128Mx16	5K PU

Default: SAM 2G VRAM

**VRAM (DDR3 / 1000MHZ
Configuration Table**

2G Samsung 128Mx16	45.3K
2G Micron 128Mx16	30.1K
2G Hynix 128Mx16	35K PD
4G Samsung 256Mx16	20K PD
4G Micron 256Mx16	10K PD



N14P-GS ID

Netname	N14P-GS
ROM_S0	0P 5K PU GS 10K PI
ROM_SCLK	15K PD
STRAP0	45K PU
STRAP1	5K PD
STRAP2	20K PD
STRAP3	GS:15K PI 0P:5K PD
STRAP4	45K PD

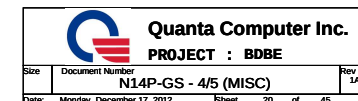
Logical Strap Bit Mapping

Resistor Values	Pull-up to VDD33	Pull-down to GND
4.99 k	1000	0000
10.0 k	1001	0001
15.0 k	1010	0010
20.0 k	1011	0011
24.9 k	1100	0100
30.1 k	1101	0101
34.8 k	1110	0110
45.3 k	1111	0111

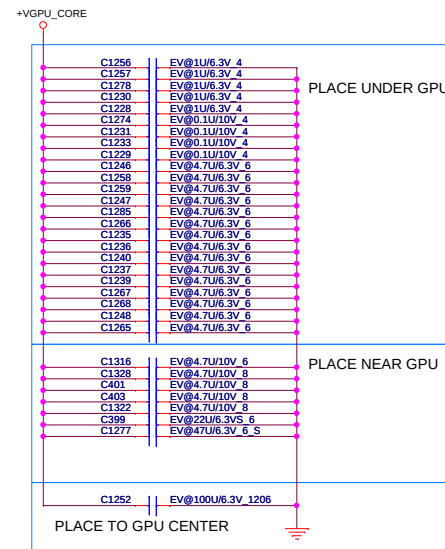
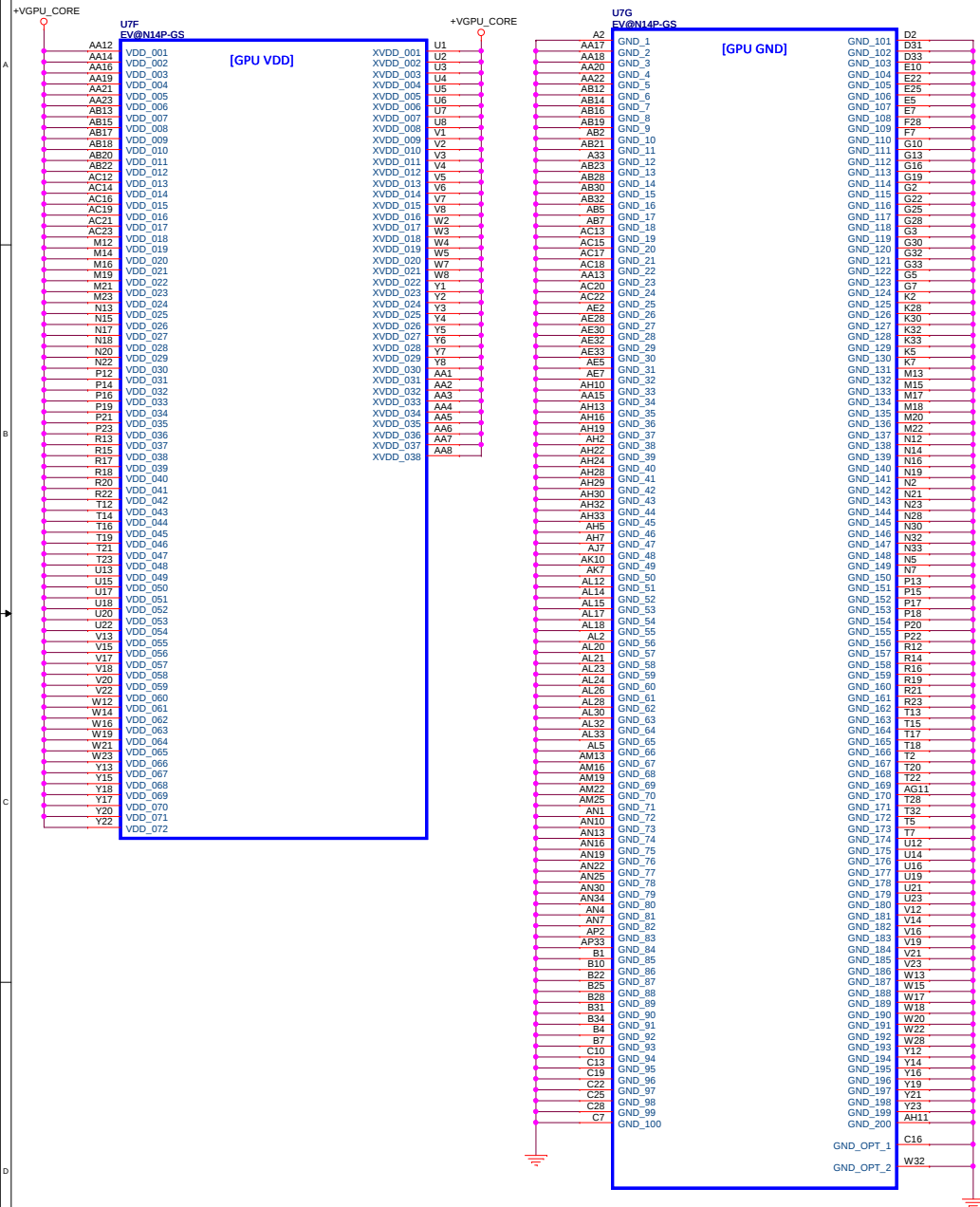
Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCL	PCL_DEVID[4]	SUB_VENDOR	PCL_DEVID[5]	PCL_PLR_EXT_TERM
ROM_S1	RAW_CFG[3]	RAW_CFG[2]	RAW_CFG[1]	RAW_CFG[0]
ROM_S0	FB[1]	FB[0]	SMBLALT_ADDR	VGA_DEVICE
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	3G0_PADCFG[3]	3G0_PADCFG[2]	3G0_PADCFG[1]	3G0_PADCFG[0]
STRAP2	PCL_DEVID[3]	PCL_DEVID[2]	PCL_DEVID[1]	PCL_DEVID[0]
STRAP3	S0R3_EXPOSED	S0R2_EXPOSED	S0R1_EXPOSED	S0R0_EXPOSED

GPIO ASSIGNMENTS

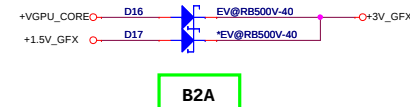
GPI0	Function
GPI0 0	Debug Service Header
GPI0 1	MEM_VDD_CTL/FAN_PWM
GPI0 2	LCD Brightness Control (BL_PWM)
GPI0 3	LCD Power Enable (PPEN)
GPI0 4	LCD Backlight Enable (BLEN)
GPI0 5	NVDDO_PWM_VID_BOOT_EN
GPI0 6	Remote Sensor Error Correction
GPI0 7	3D STEREO
GPI0 8	GPU Overtemp
GPI0 9	GPU Thermal Alert/FAN_PWM
GPI0 10	FB Vref Control
GPI0 11	NVDDO_PWM_VID
GPI0 12	PWR_Level AC Detect
GPI0 13	NVDDO PSI
GPI0 14	FB_CLAMP_TGL_REG/HPD for IFP AB (not used)
GPI0 15	HPD for IFP C (DP)
GPI0 16	Fan_PWM/MEM_VDD_CTL/NVDDO_PSI/FRAME LOCK
GPI0 17	HPD for IFP D (eDP)
GPI0 18	HPD for IFP E (DP)
GPI0 19	HPD for IFP F (DP)
GPI0 20	<not used>
GPI0 21	<not used>



VDD/XVDD : 25.72A



for meet Power down sequence for +3V_GFX



120808 Del DGPU_PWROK circuit
because all +1.05V_GFX/+1.5V_GFX
power solution have PG connector
to PCH

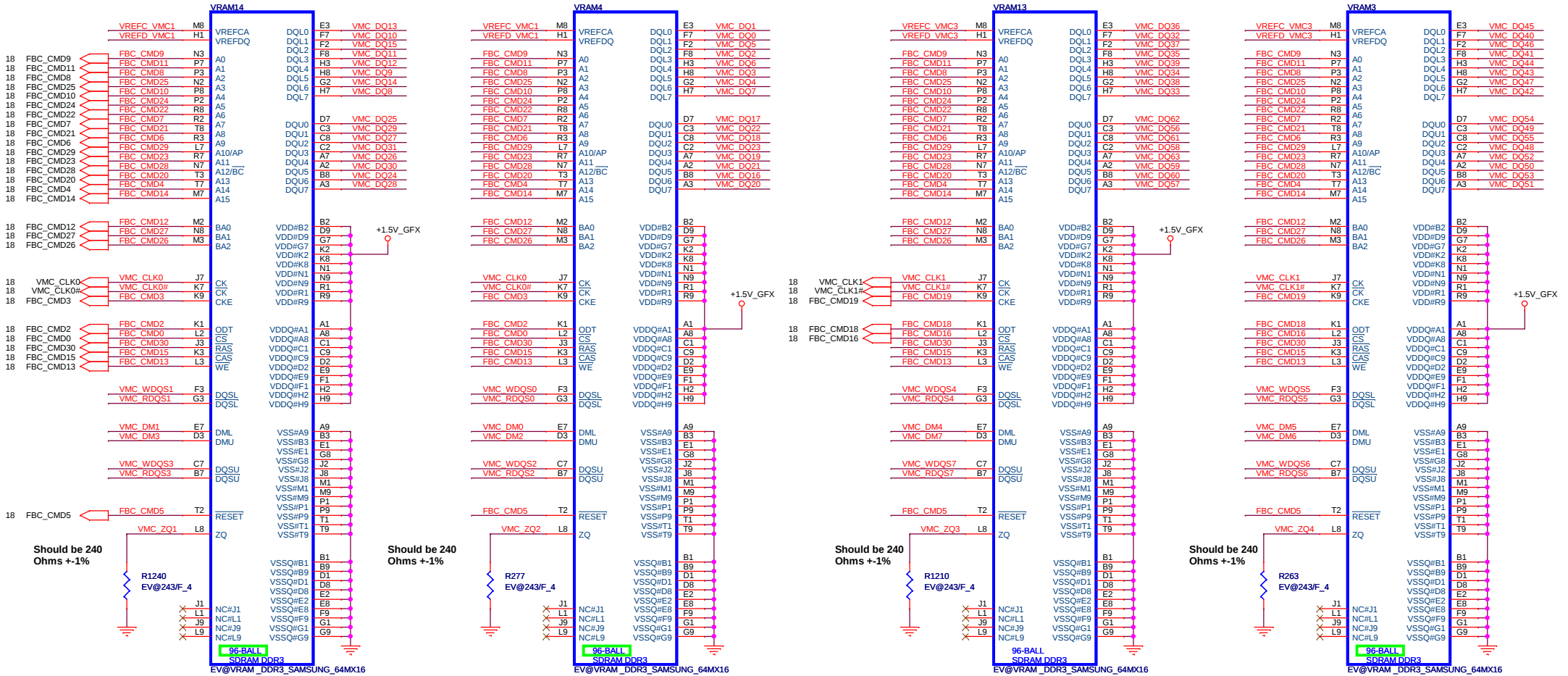
17,18,19,20,44
18,20,22,23,36,44
17,19,20,26,43,44
3,7,8,9,10,11,13,14,15,16,20,24,26,27,28,30,31,33,34,35,36,38,42

+VGA CORE
+1.05V_GFX
+1.5V_GFX
+3V_GFX
+3V

CHANNEL A: 512MB / 1024MB DDR3

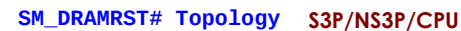
18 VMC_DQ[63:0]
18 VMC_DM[7:0]
18 VMC_WDQS[7:0]
18 VMC_RDQS[7:0]

CHANNEL B: 256MB/512MB DDR3

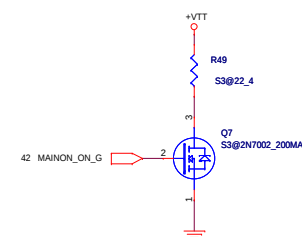


Fermi : Change to 160 ohm (WJ)
1 : CS11602JB00 ,RES CHIP 160 1/16W +5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +1%(0402)

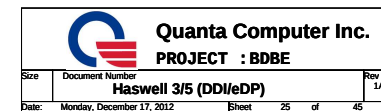
Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +1%(0402)



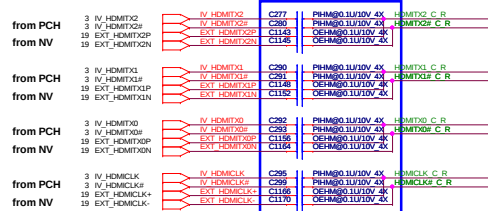
For S3 power Reduction VTT discharge S3P/NS3P/CPU



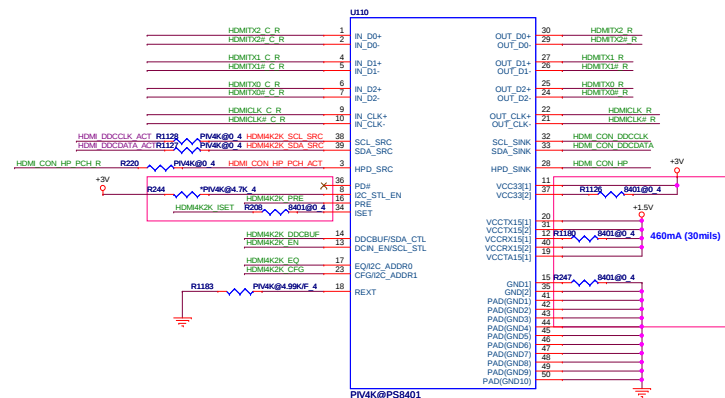
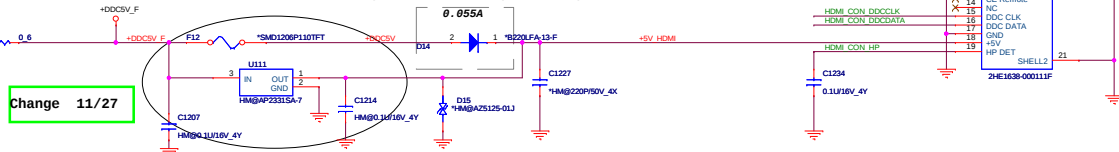
S3 power Reduction (CPU Power) S3P/NS3P/CPU



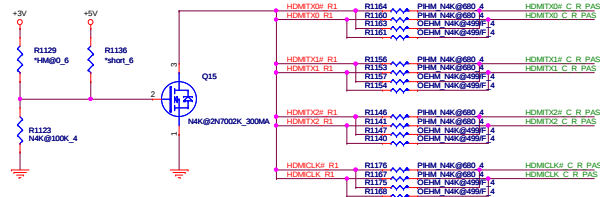
Close



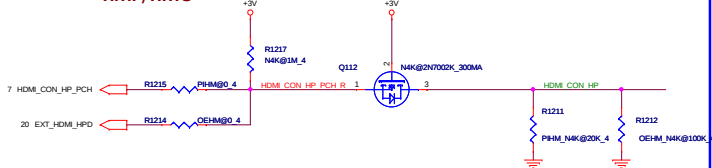
Change to correct diode (BC000220Z01)



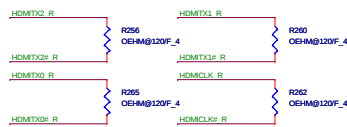
<HMP/HMG>



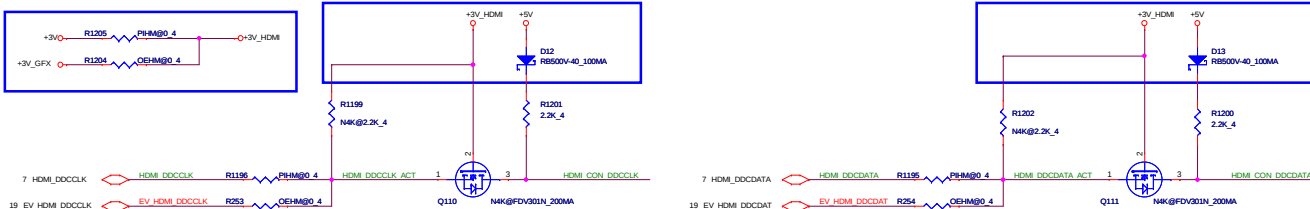
FOR EMI **<EMC>**



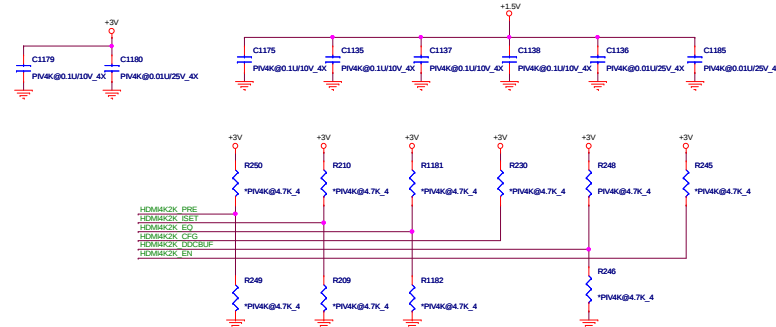
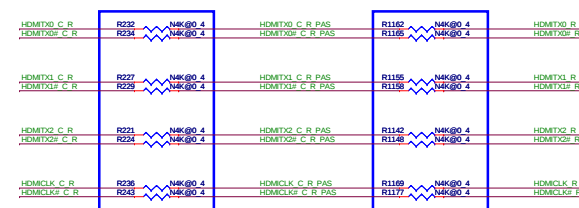
FOR EMI **<EMC>**



HDMI-SMBus <HDM>



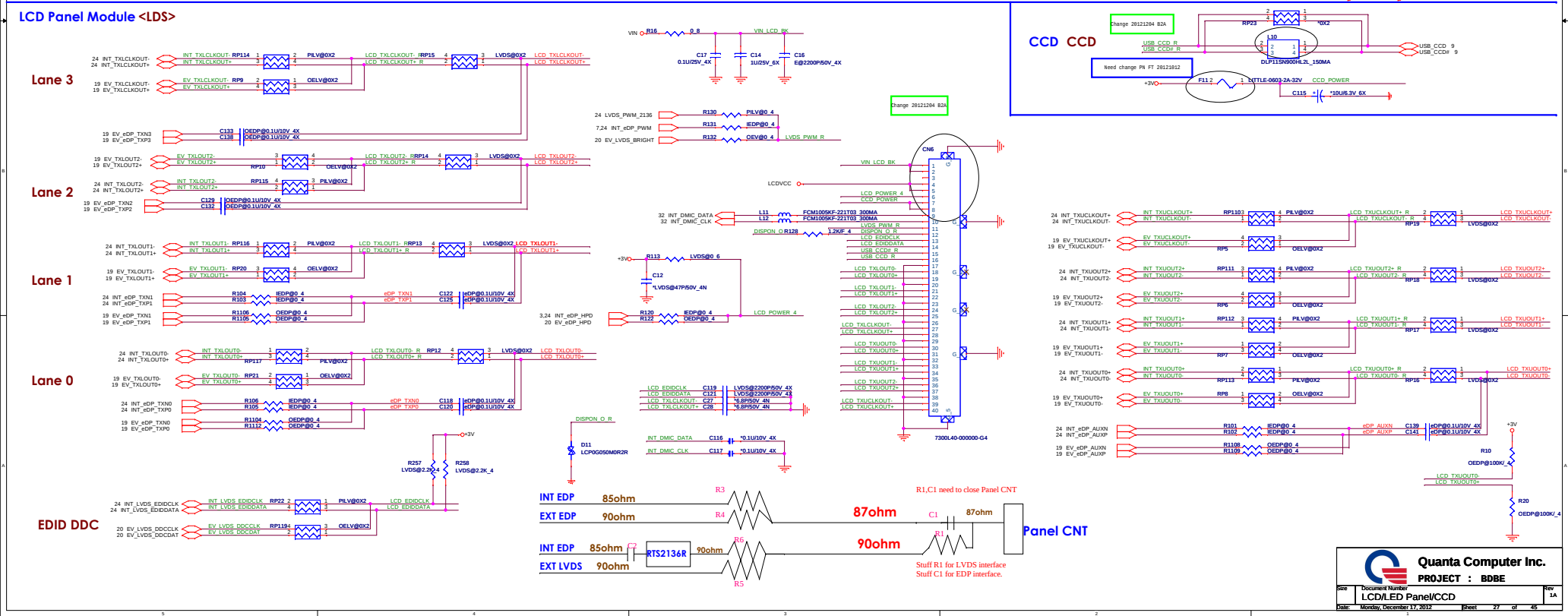
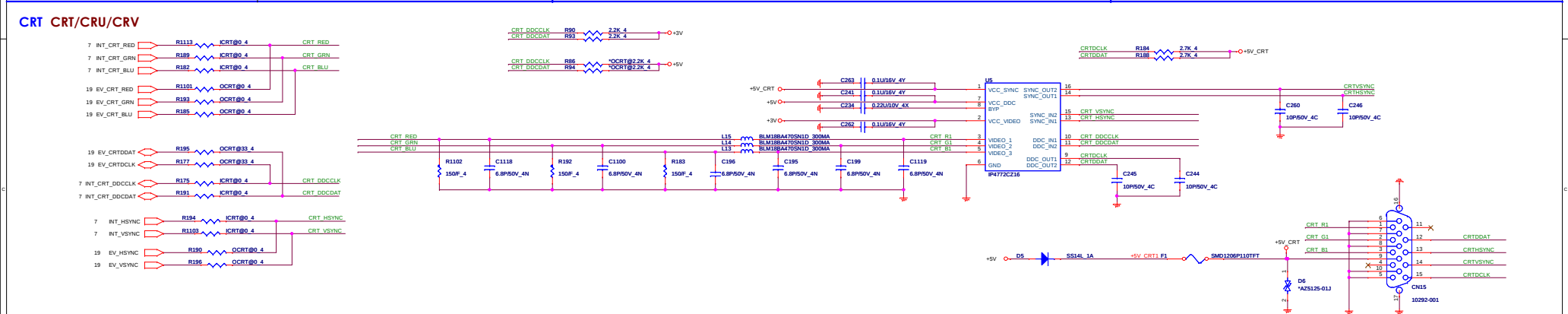
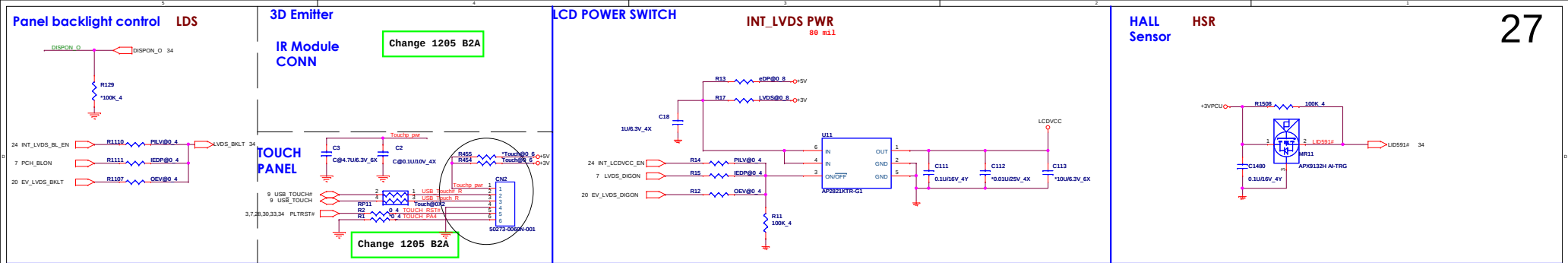
Close U2501

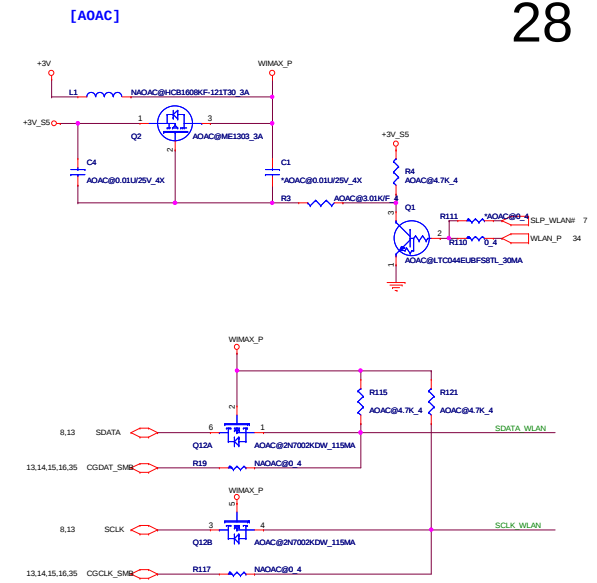
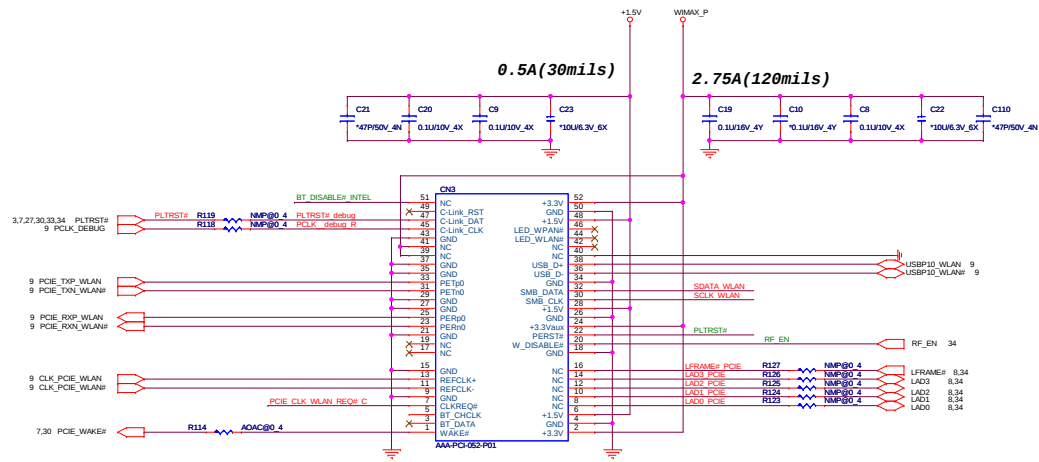
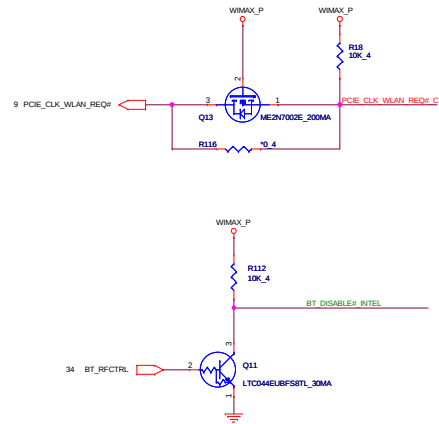


	Pre	ISet	Eq	CFG	DDCBUF	DCIN_EN
NC(Low)	0 dB	default	12.4 dB	HDMI ID disable	default	default, AC coupling input
1(High)	1.6 dB	+13%	4.3 dB	HDMI ID enable	active DDC buffer with default threshold	DC coupling input
M	2.5 dB	-13%	8.6 dB	N/A	active DDC buffer without internal pull up resistor	N/A

Pre	Output pre-emphasis setting
ISET	TMDS output swing adjustment
EQ	Receiver equalization setting
CFG	Configuration pin
DCBUIF	enable active DDC buffer
DCIN_EN	DC coupling enable

Pin	PS8401A	PS8201A
12	VDDRX	NC
15	GND	NC
34	ISET	NC
37	VDD33	NC

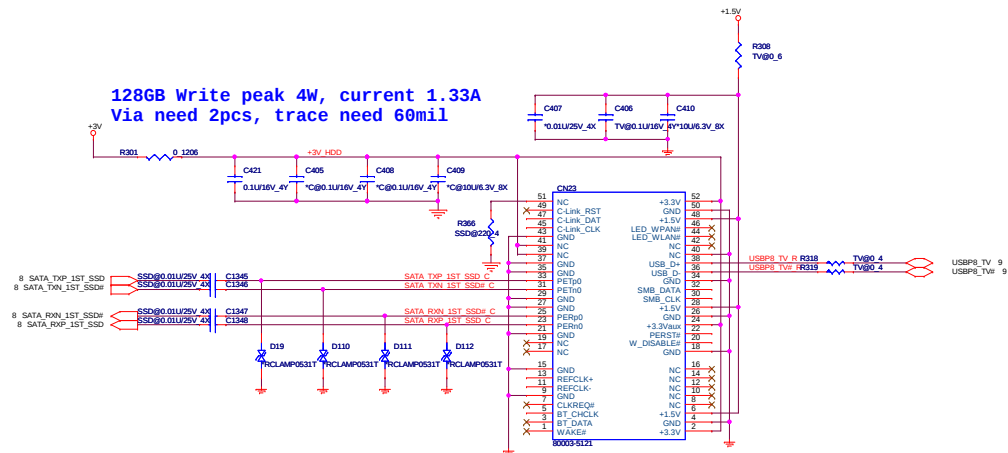




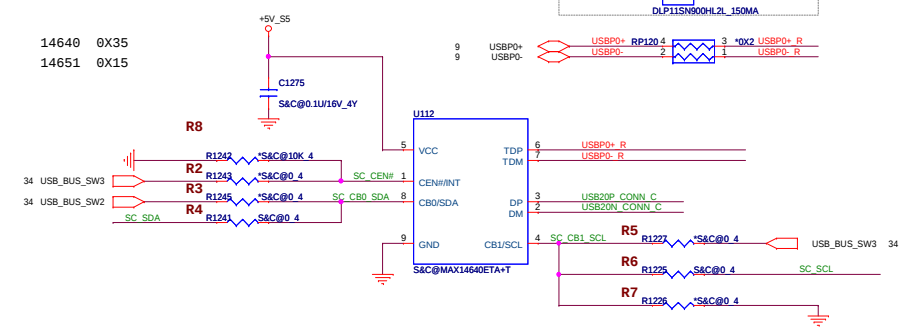
TV Tuner / MSATA

<SSD>

TV Tuner: 1.5V@240mA 3.3V@470mA



USB CONNECT <U3B/USB> RIGHT(UR)



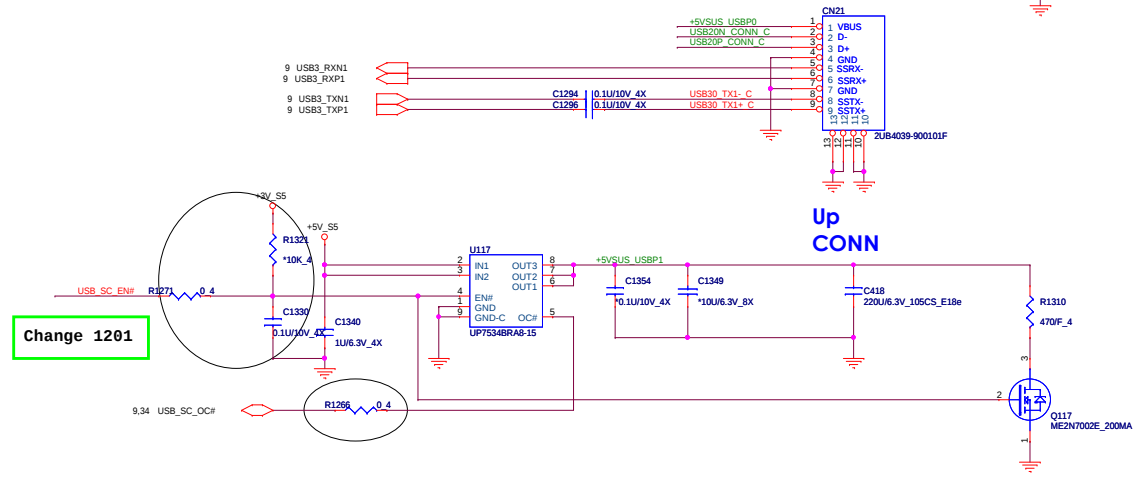
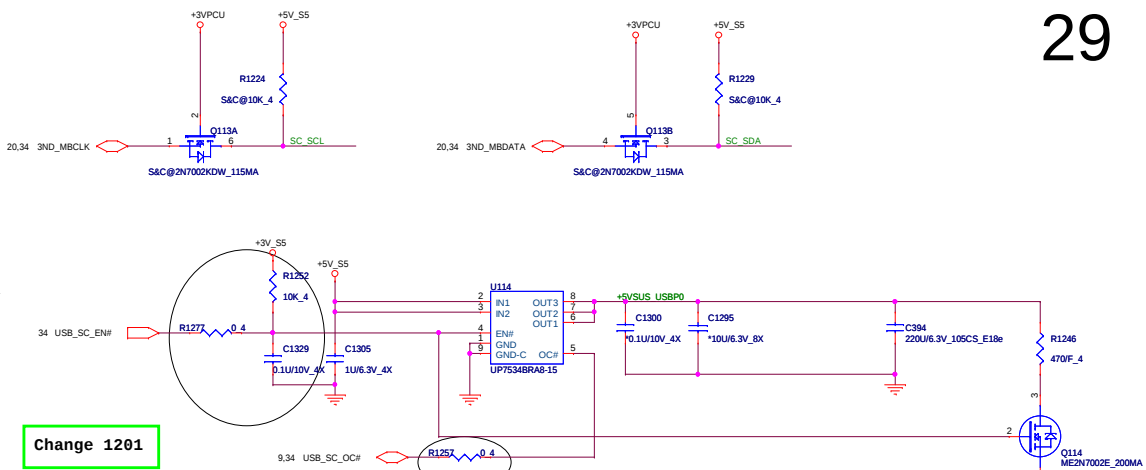
	R1	R2	R3	R4	R5	R6	R7	R8
14566		V	V				V	
14600					V			
14617(with CB2)	V		V		V			
14617(no CB2)			V		V			V
14641/42/44			V		V			
14640				V		V		

SW2	SW3	14600	Status	
0	0		Auto mode	Charger / AM
0	1		Force dedicated charger mode	Charger / FM
1	0		Pass-Through(USB) mode	USB / PM
1	1		Pass-Through(USB) mode with CDP Emulation	USB / CM

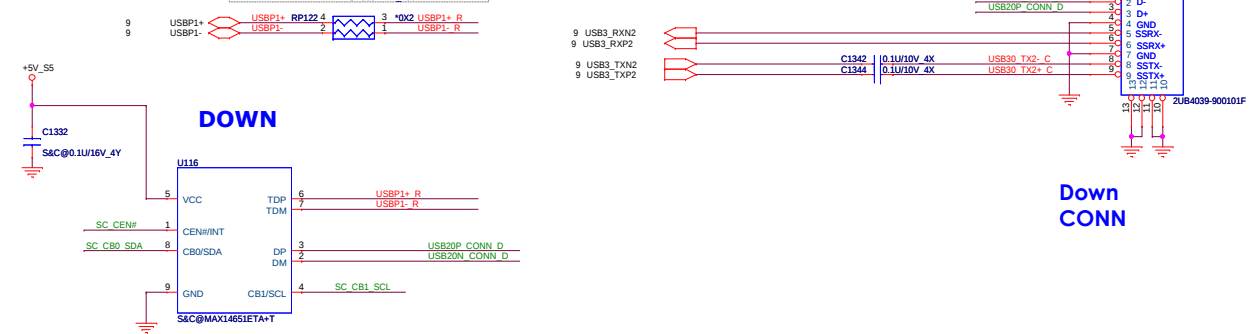
SW2	SW3	14644	Status	
0	0		2A Auto mode for Apple Device	Charger / AM2
1	0		Force dedicated charger mode	Charger / FM
0	1		Pass-Through(USB) mode	USB / PM
1	1		Pass-Through(USB) mode with CDP Emulation	USB / CM

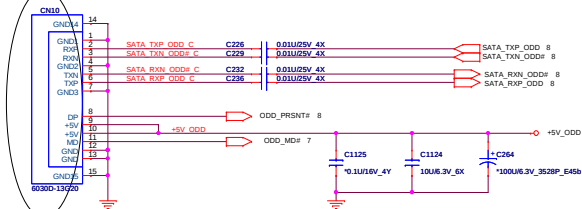
SW2	SW3	14641	Status	
0	0		2A Auto mode for Apple Device	Charger / AM2
1	0		Force 1A for Apple Device	Charger / AP1
0	1		Pass-Through(USB) mode	USB / PM
1	1		Pass-Through(USB) mode with CDP Emulation	USB / CM

SW2	SW3	14642	Status	
X	0		2A Auto mode for Apple Device	Charger / AM2
0	1		Pass-Through(USB) mode	USB / PM
1	1		Pass-Through(USB) mode with CDP Emulation	USB / CM

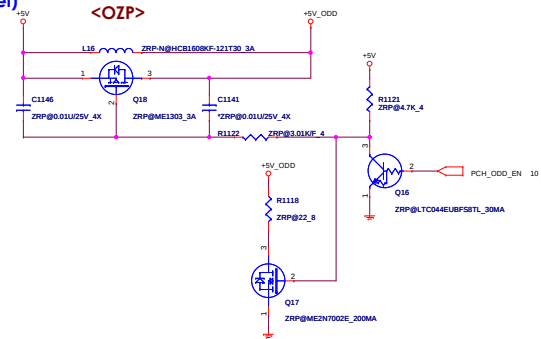


USB CONNECT RIGHT(DN)



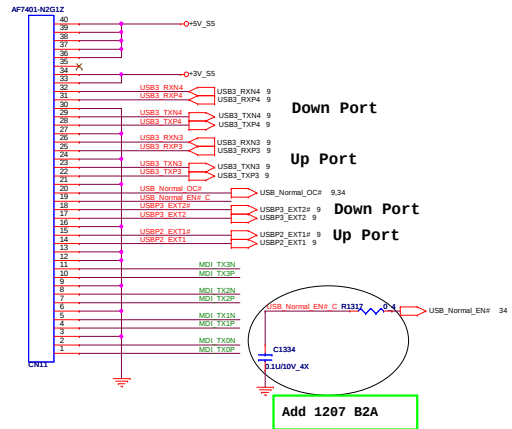


ODD Zero power
(Only for Intel)



<LAN/LN1.LNG>

Atheros Lan/USB3 CONN



Down Port

Up Port

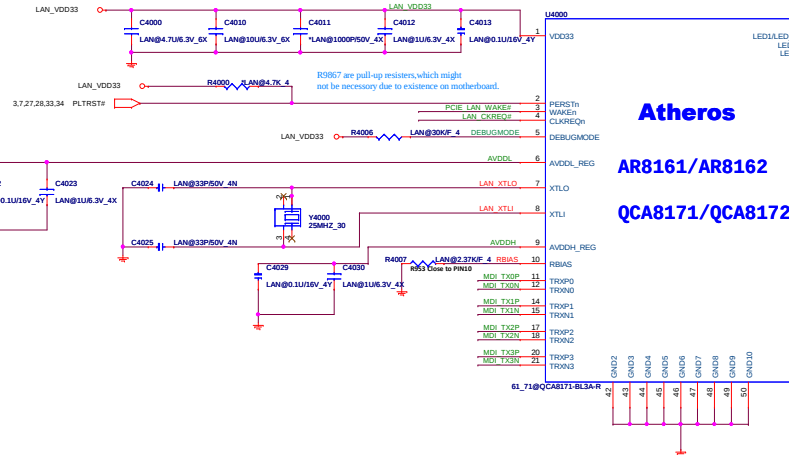
Down Port

Up Port

Add 1207 B2A

AR8161-BL3A-RL = AL008161003

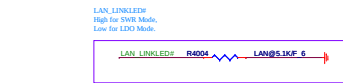
277mA(30mils)



Atheros

AR8161/AR8162

QCA8171/QCA8172



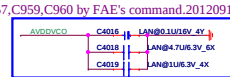
LAN_LINKLED#
High for SWR Mode
Low for LDO Mode

pin38, pin39 & pin23
(LED0, LED1 & LED2) has internal pull up.

AR8161/8162 Pin 23 for LAN LED, No use NC.

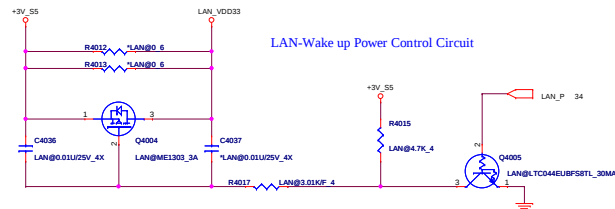
AVDDVCO add C957,C959,C960 by FAE's command.20120914

The pin 38 "LED0" doesn't pull down to choose low core voltage. (It's internal pull up) by FAE's command.20120914



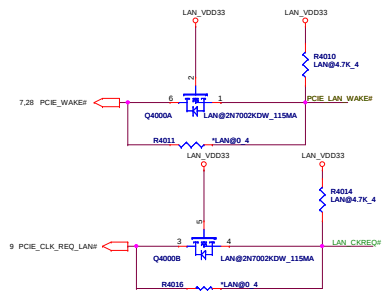
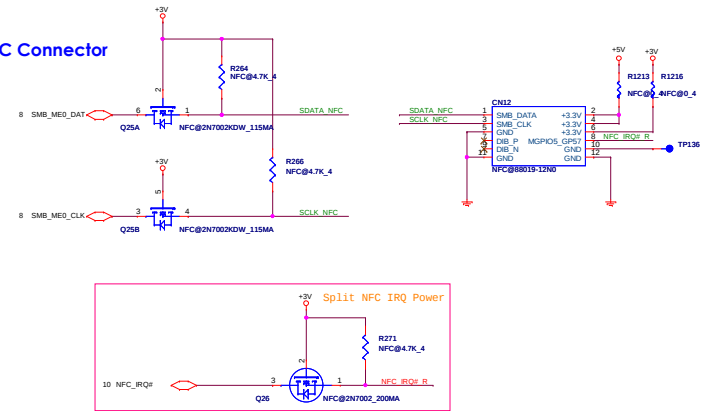
If AVDDL/DVDDL comes from internal SWR:
mount L5036.
But, if comes from internal LDO, no mount L5036.

If AVDDL/DVDDL comes from internal SW mount L5035,C5467,C5468,C5469.
But,if comes from internal LDO, no mount.

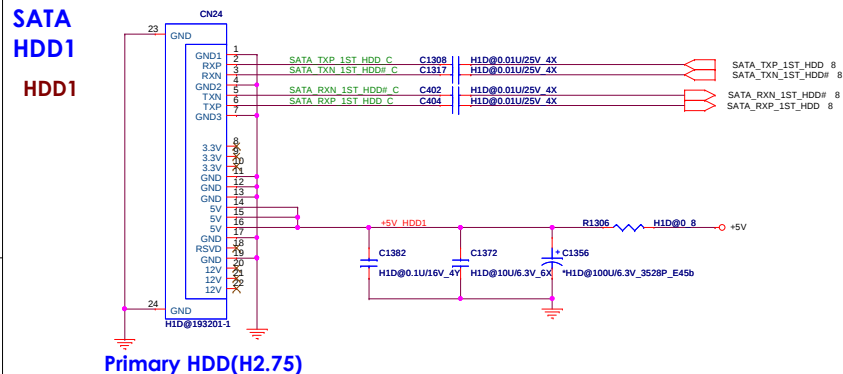


LAN-Wake up Power Control Circuit

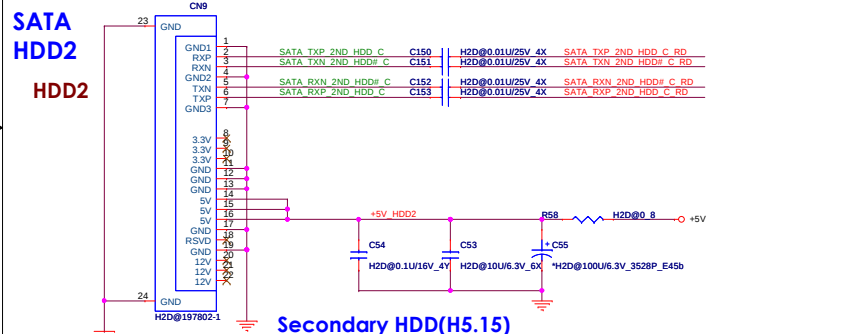
NFC Connector



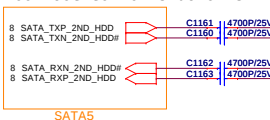
SATA
HDD1
HDD1



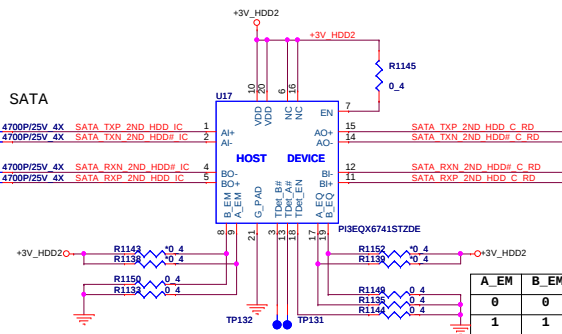
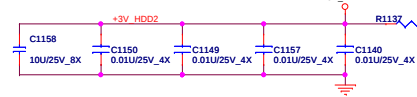
SATA
HDD2
HDD



2nd HDD SATA Re-driver



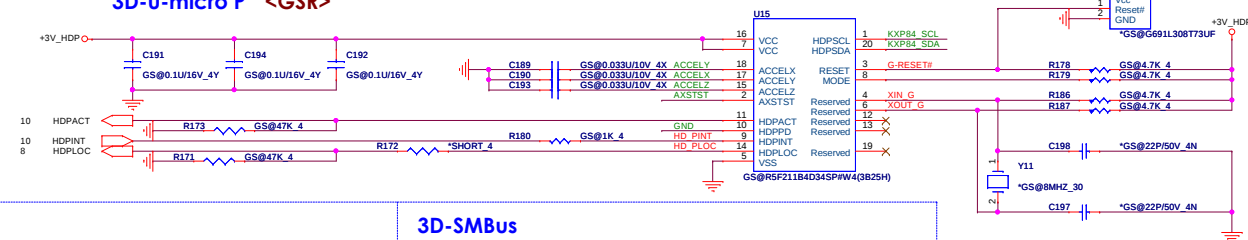
Layout Note: Closed to IC



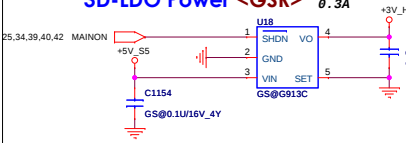
A_EQ	B_EQ	1.5 Gb/s	3 Gb/s	6 Gb/s
0	0	1 bB	2.5 bB	3 bB
1	1	4 bB	7.5 bB	9 bB
floating		2.5 bB	5 bB	6 bB

A_EM	B_EM	3 Gb/s	6 Gb/s
0	0	550mV pp	650mV pp
1	1	550mV pp+3dB Pre-emphasis	650mV pp+1.5dB Pre-emphasis

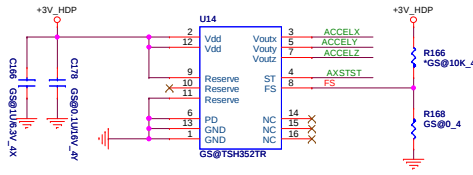
3D-u-micro P <GSR>



3D-LDO Power <GSR> 0.3A



3D-Sensor IC



FS (Full Scale) selection

FS	0	1
	2g Full-Scale	6g Full-Scale

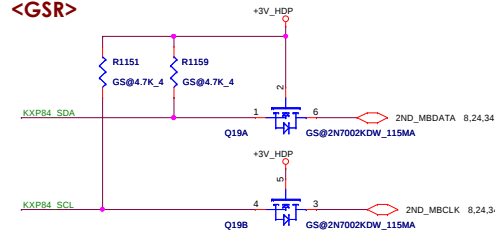
PD (Power Down) selection

PD	0	1
	Normal Mode	Power-down mode

HDPPD selection

HDPPD	0	1
	Normal Mode	Power-down mode

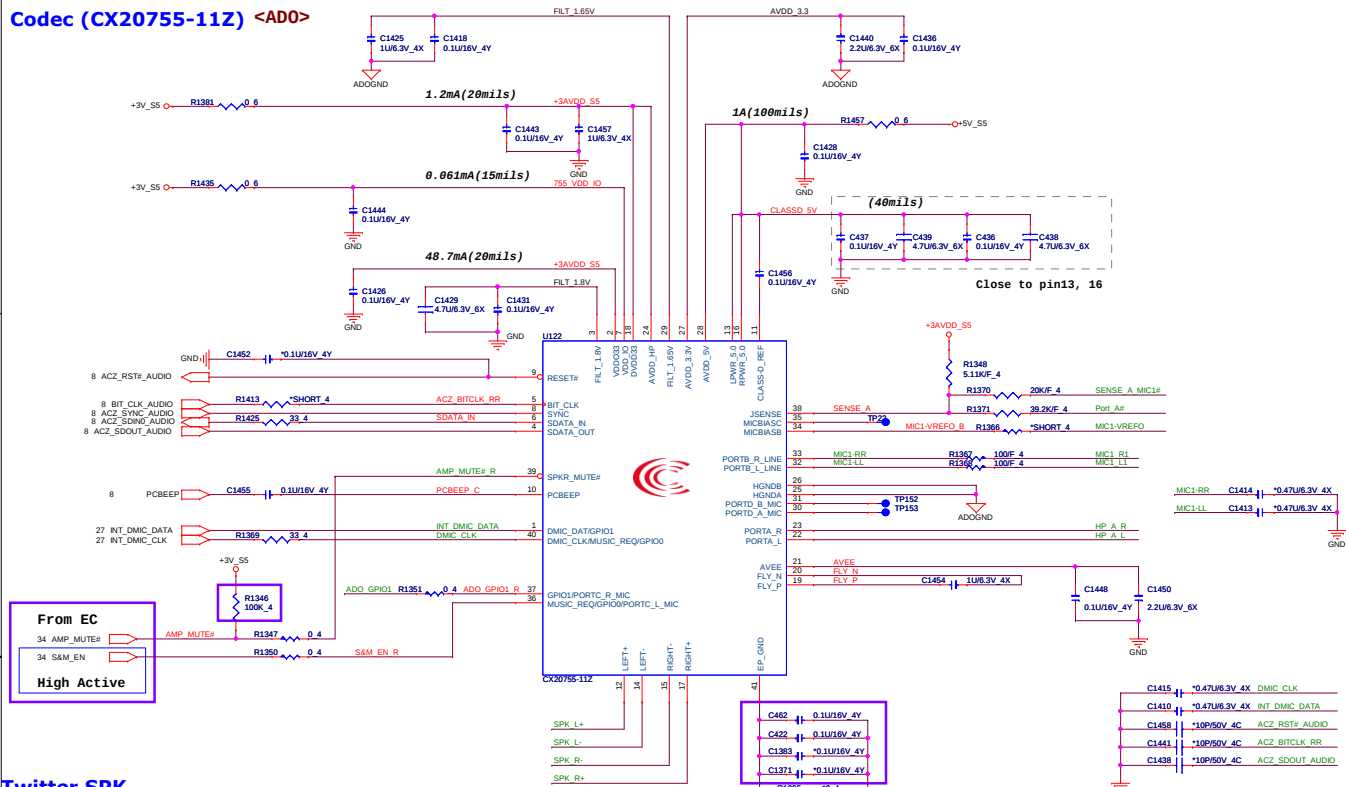
3D-SMBus
<GSR>



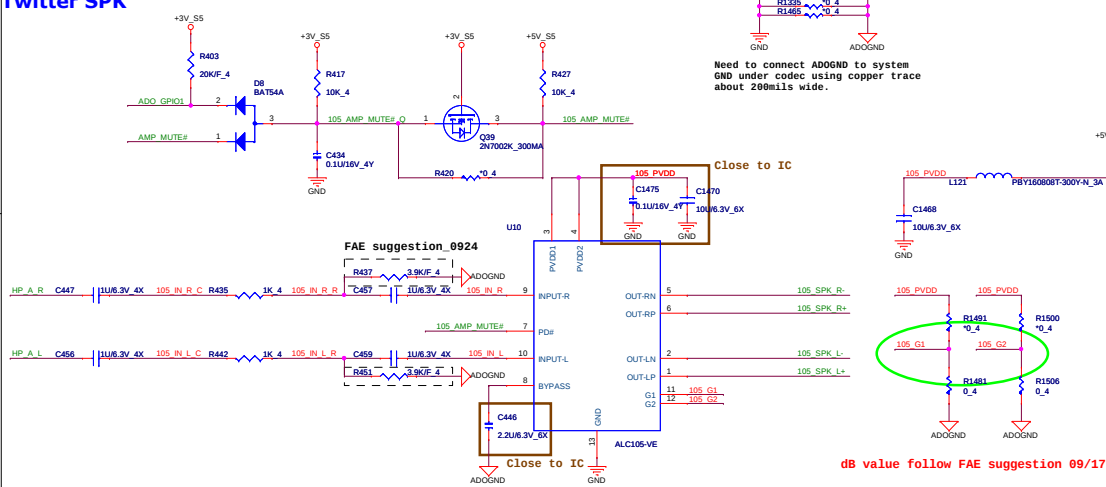
Quanta Computer Inc.
PROJECT : BDBE

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Codec (CX20755-11Z) <ADO>



Twitter SPK

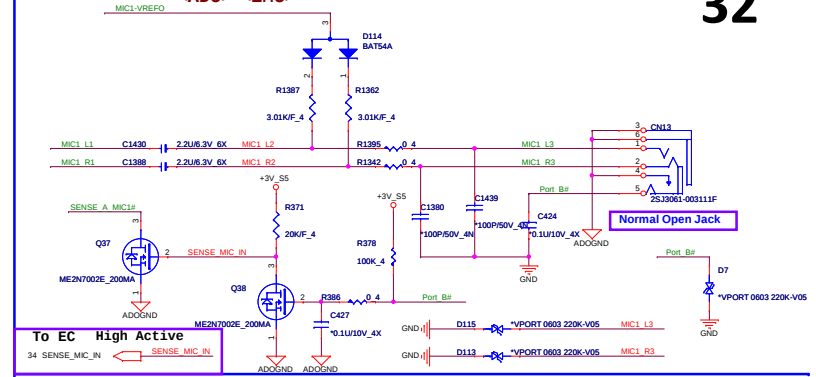


Output Gain Table

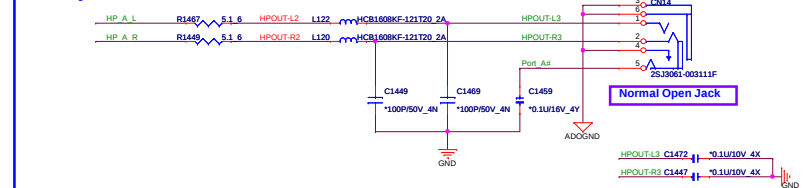
G1	G2	Gain
0	0	11dB
0	1	14dB
1	0	19dB
1	1	25dB

dB value follow FAE suggestion 09/17

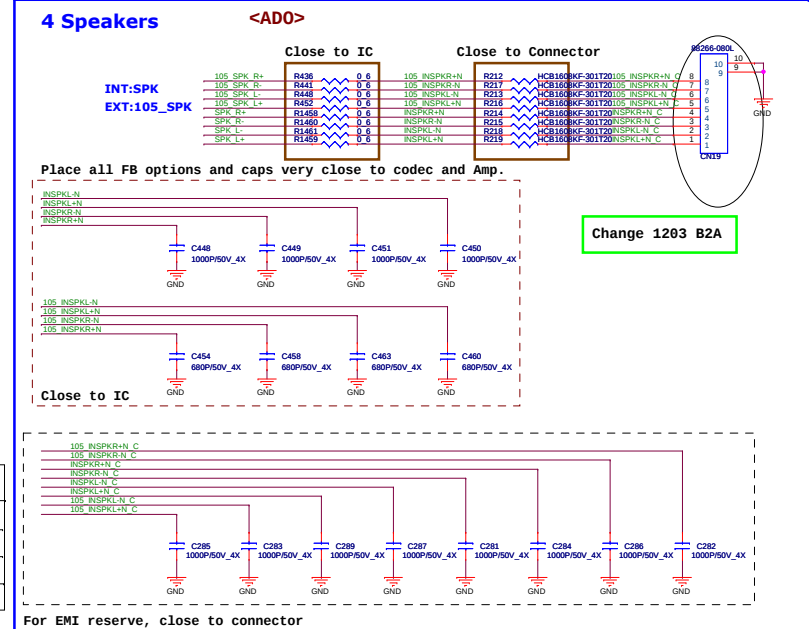
External MIC <ADO> <EMC>



Headphone <ADO>



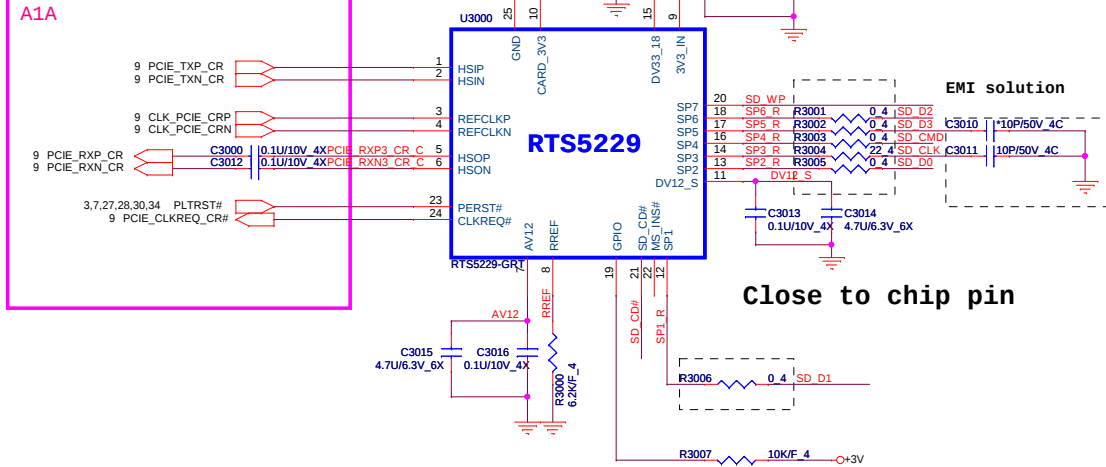
4 Speakers



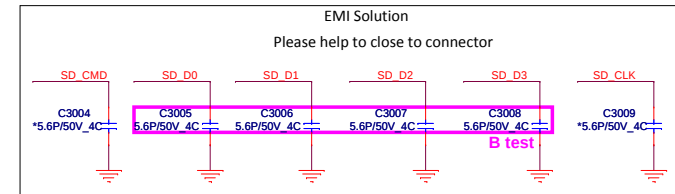
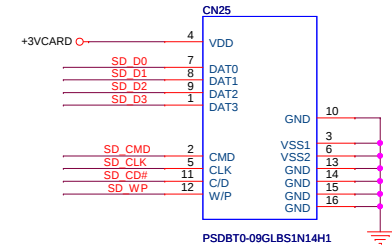
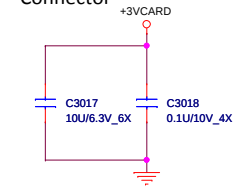
For EMI reserve, close to connector

Card Reader (GL834L) <MMC>

Change interface from USB3.0 to PCIe

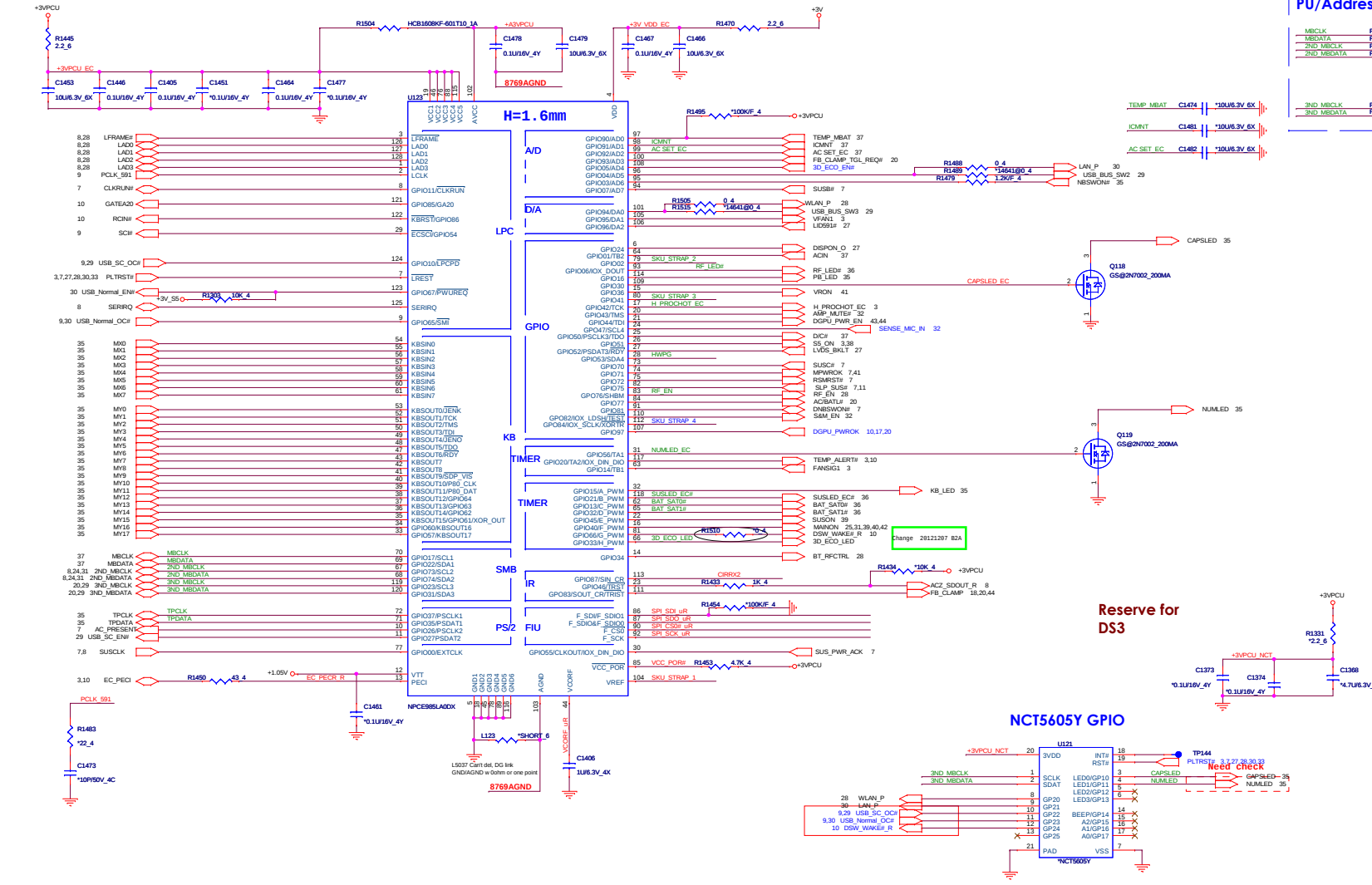


Share Pin

SD / MMC
CARD READERPlace close to
Connector

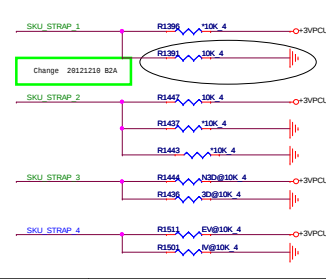
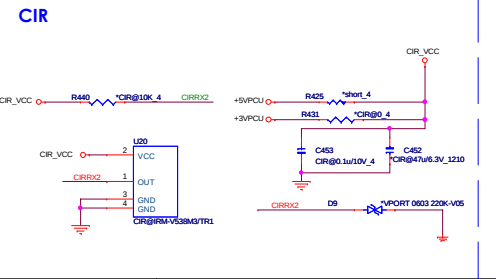
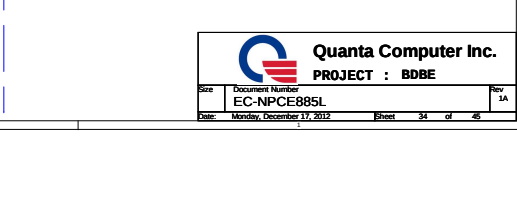
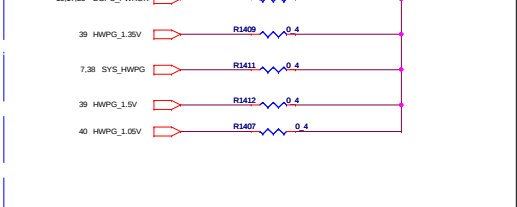
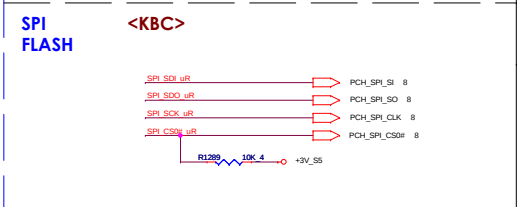
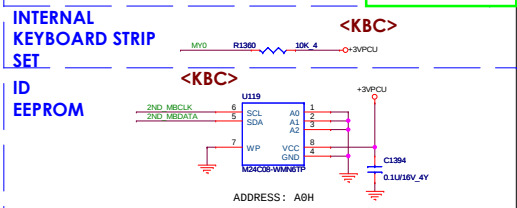
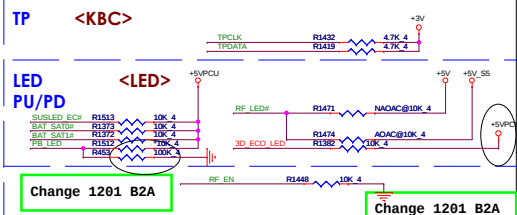
Quanta Computer Inc.
PROJECT : BDBE

Size	Document Number	Rev
	Card Reader(AU6437)	1A
Date:	Monday, December 17, 2012	Sheet 33 of 45

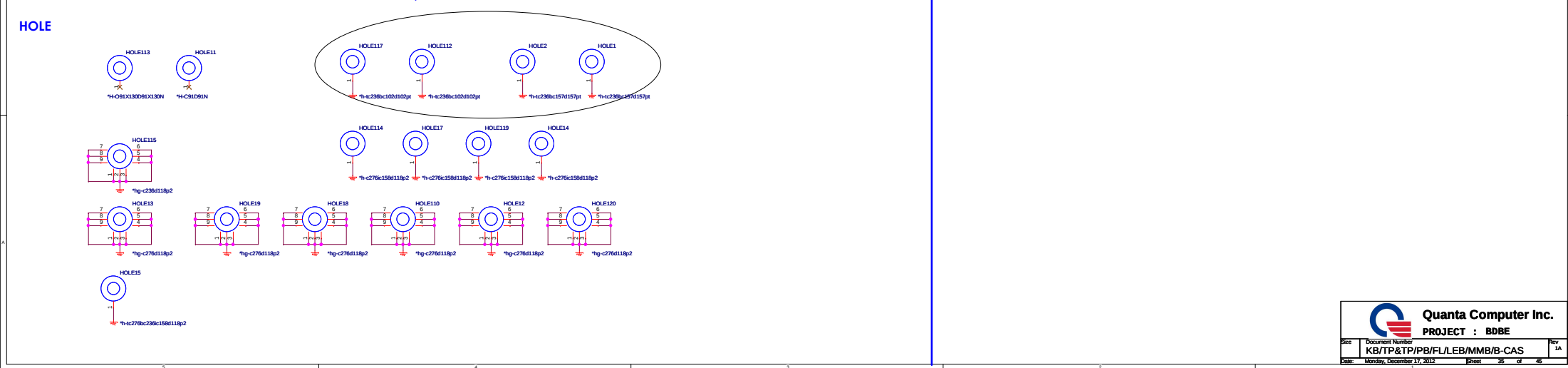
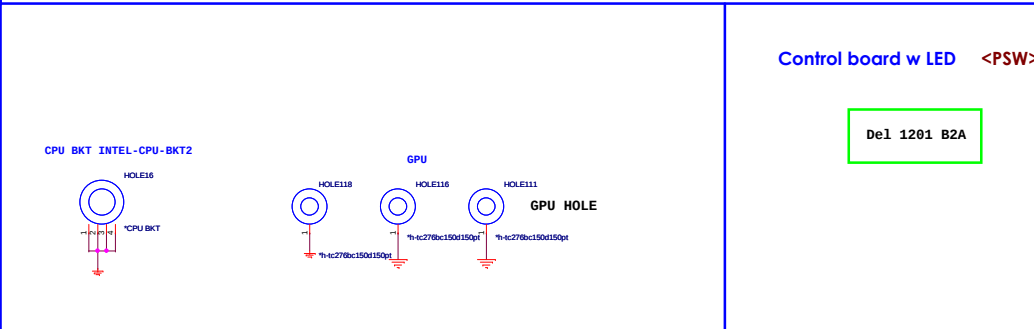
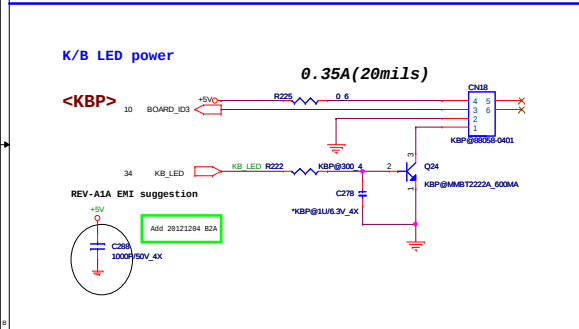
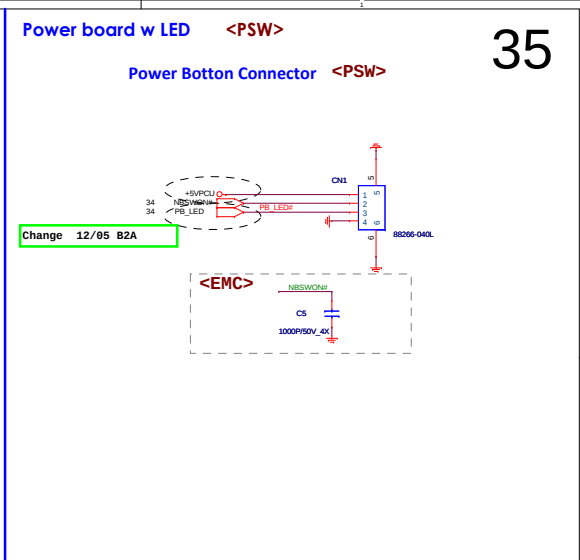
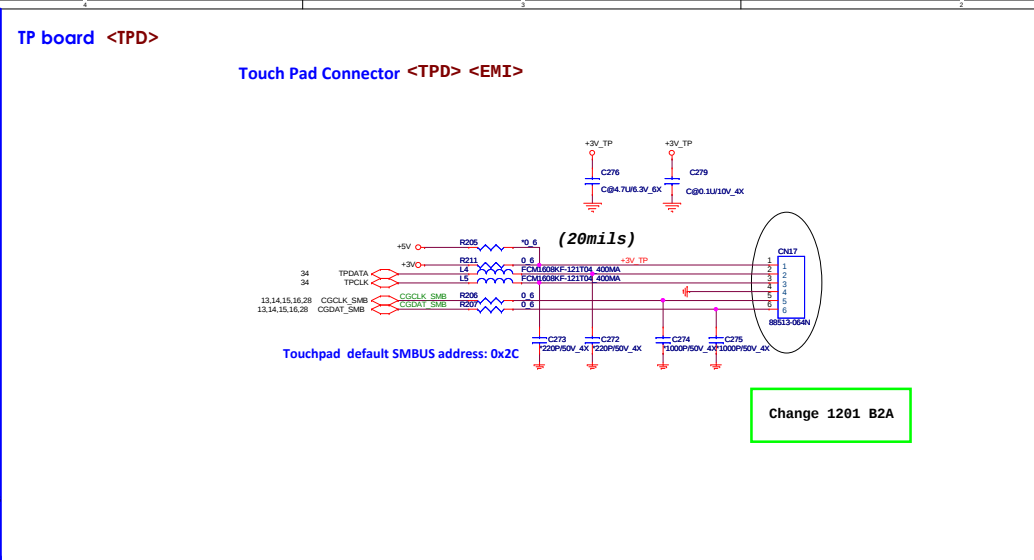
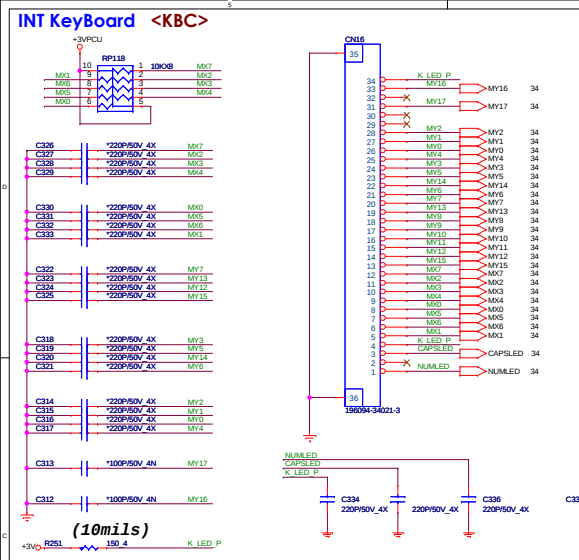


SM BUS PU/Address

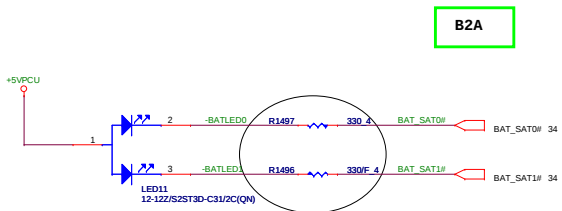
SM BUS PU/Address	Devices	Address
1	Battery(A)	
2	PCH(SS)	
3	G-sensor(S0)	
4	IDROM(A)	
5	EDP2LVDS IC	94H or 64H
6	VGA Thermal(A or S0)	98H
7	Extend GPIO	
8	S&C IC 14640 Up Port	35H
9	S&C IC 14651 Down Port	15H



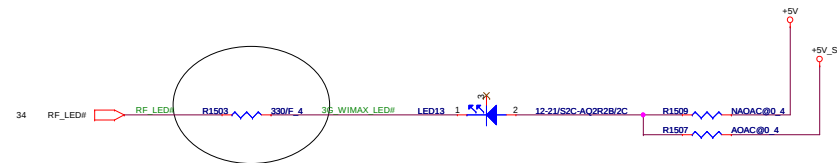
MS Strap	SKU_STRAP_1	SKU_STRAP_2	SKU_STRAP_3	SKU_STRAP_4
17°F	0			
17°G	1			
Chief River		0		
Shark Bay		1		
W/ 3D			0	
W/O 3D			1	
UMA				0
Discrete(Optimus)				1



LED BATTERY

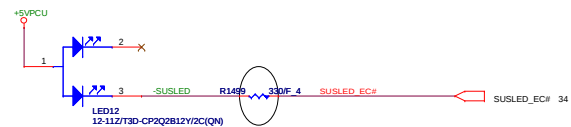


RF LED LED

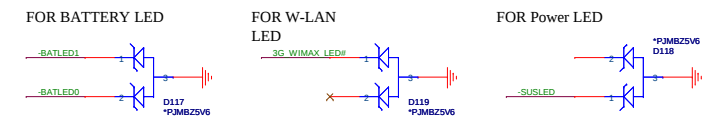


36

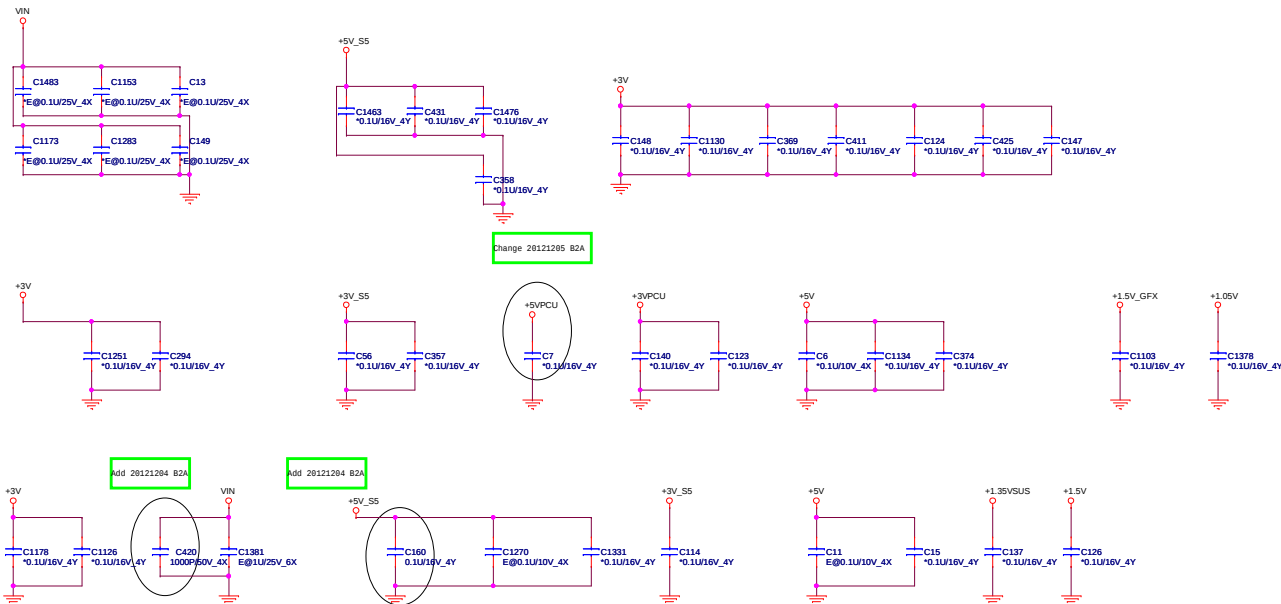
POWER LED



ESD Protect LED

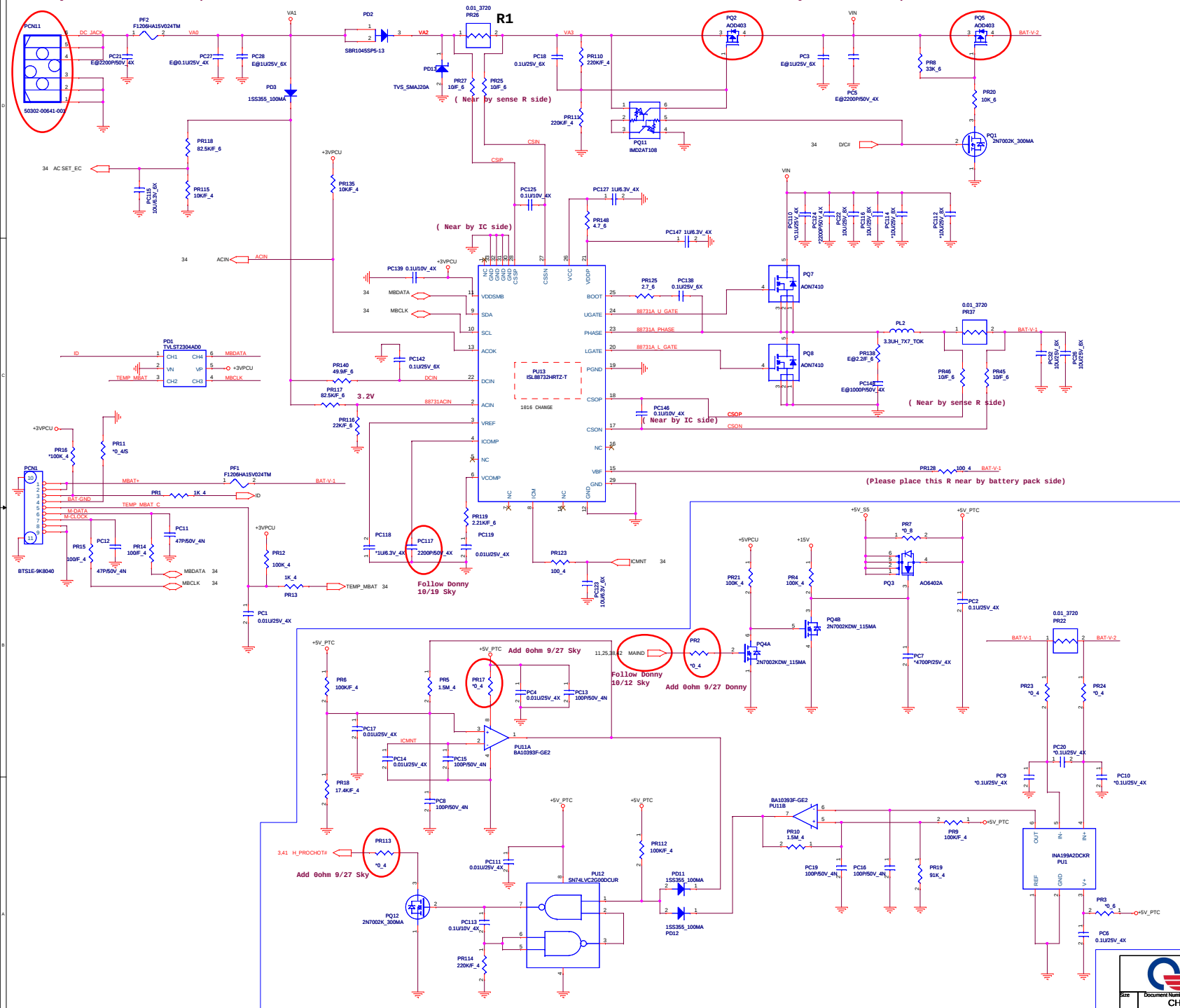


EMI EMI

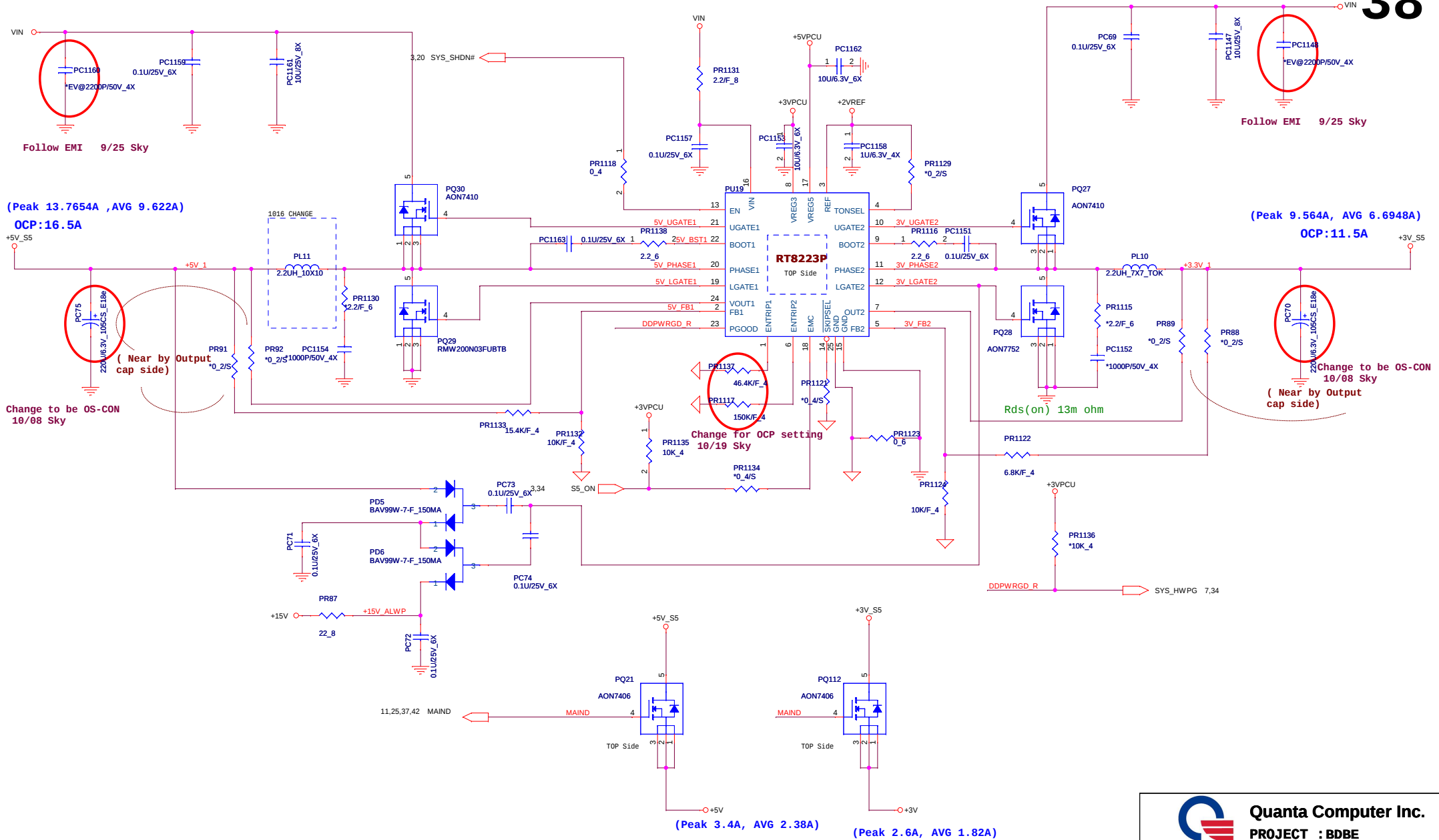


Change to be the same as BDA 10/08 Sky

Change to be A0D403 10/08 Sky



ADD
Follow BD6
Sky 09/24



Quanta Computer Inc.
PROJECT : BDDE

Size	Document Number	Rev
	System 3V/5V(TPS51123A)	1A
Date:	Monday, December 17, 2012	Sheet 38 of 45



Change enable signal from SUSON to be MAINON for EE just need 1.05V S0 power 09/27 Sky

Change for OCP setting 10/19 Sky

Follow EMI 9/25 Sky

OCP:8A

(Peak 6.523A, AVG 4.566A)

Total capacitor : 400uF
F: 320k Hz

$$V_{out} = 0.704V * (R1 + R2) / R2$$

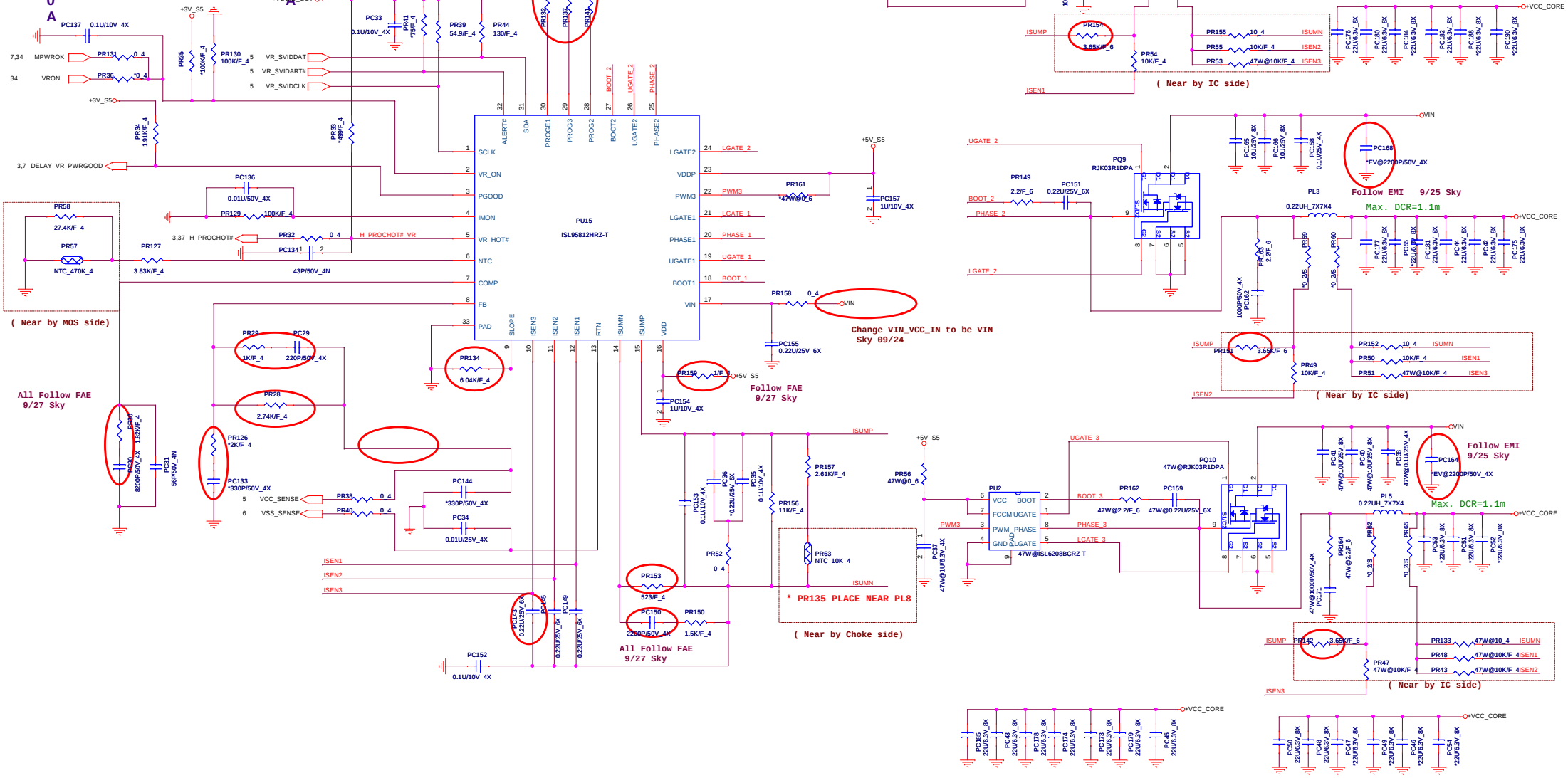
Delete PQ5064, PC405, PJP7 for EE just need 1.05V S0 power 09/27 Sky

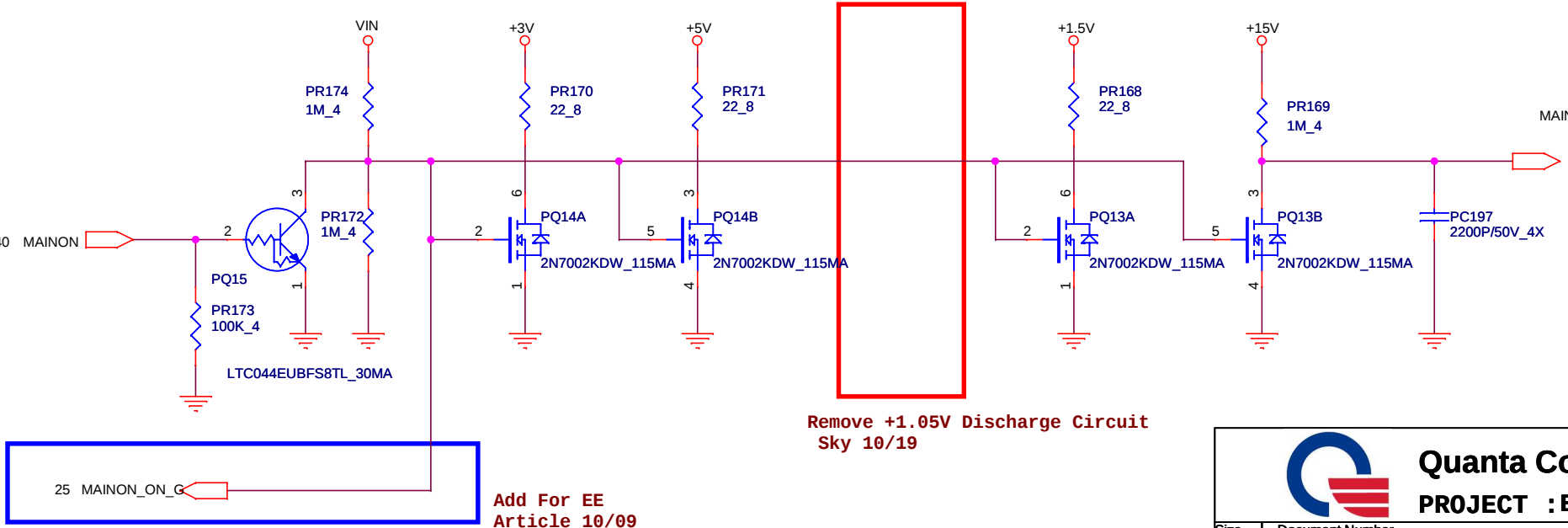
 Quanta Computer Inc. PROJECT : BDBE		
Size	Document Number +1.05V_A(TPSS51211DSCR)	Rev 1A
Date:	Monday, December 17, 2012	Sheet 40 of 45

CPU Core : Loadline =
-1.5mV/A
TDC = 26A
ICCMAX=55A

OCP = 120

O
C
P
=
6
6
A





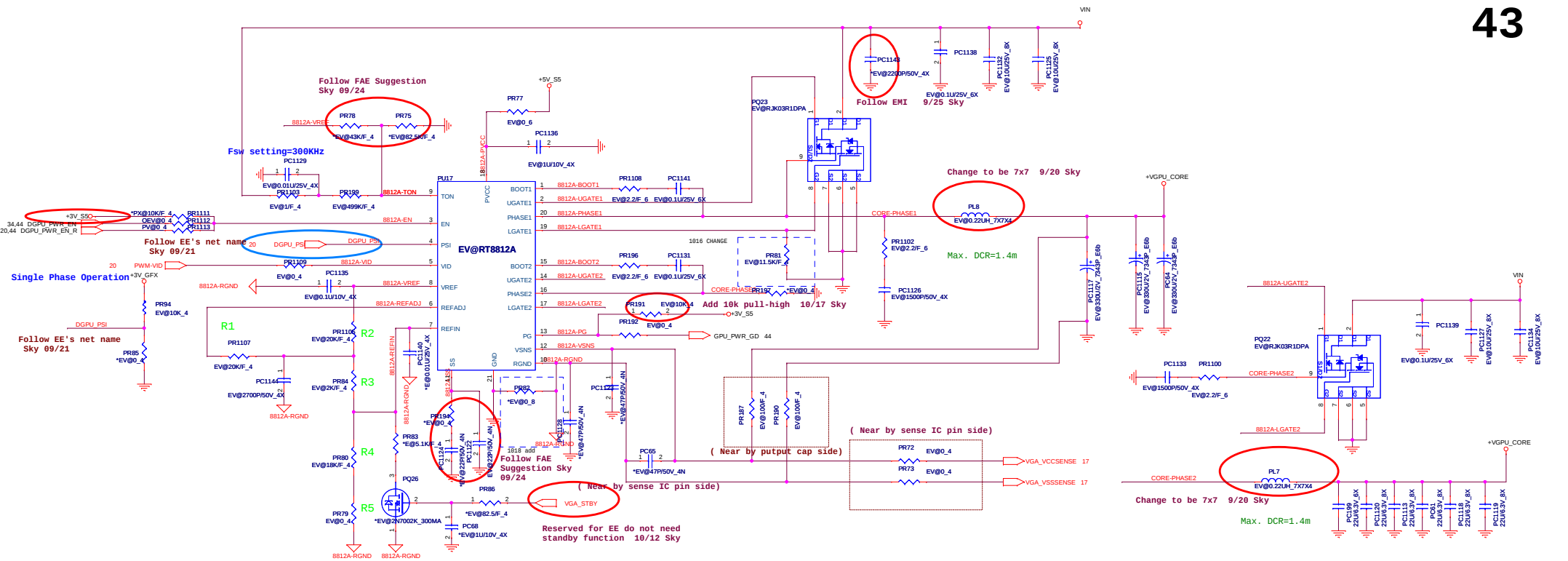
Remove +1.05V Discharge Circuit
Sky 10/19

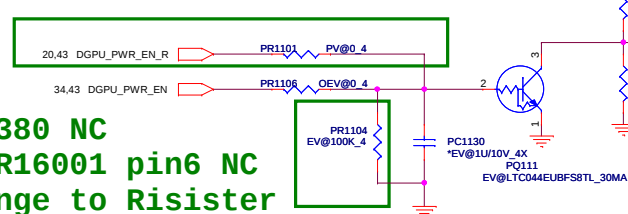
Add For EE
Article 10/09



Quanta Computer Inc.
PROJECT : BDBE

Size	Document Number	Rev
	+1.8V/Discharge	1A
Date:	Monday, December 17, 2012	Sheet 42 of 45





BD5 : R380 NC
BD6 : PR16001 pin6 NC
and change to Rister
These is initial low,
for sure that dGPU power Off

[illegible]