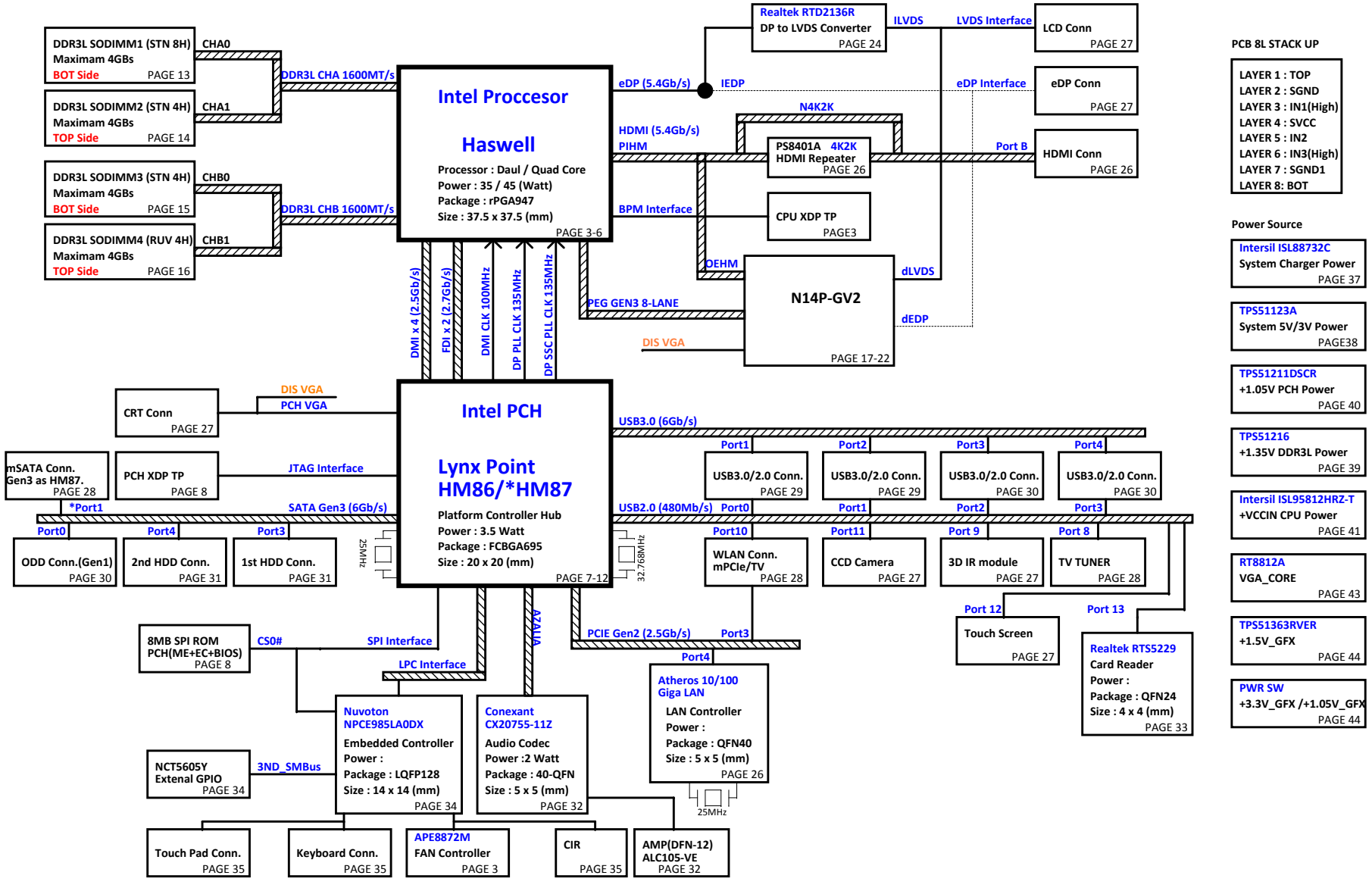
(17.3") Intel Shark Bay Platform Block Diagram

01

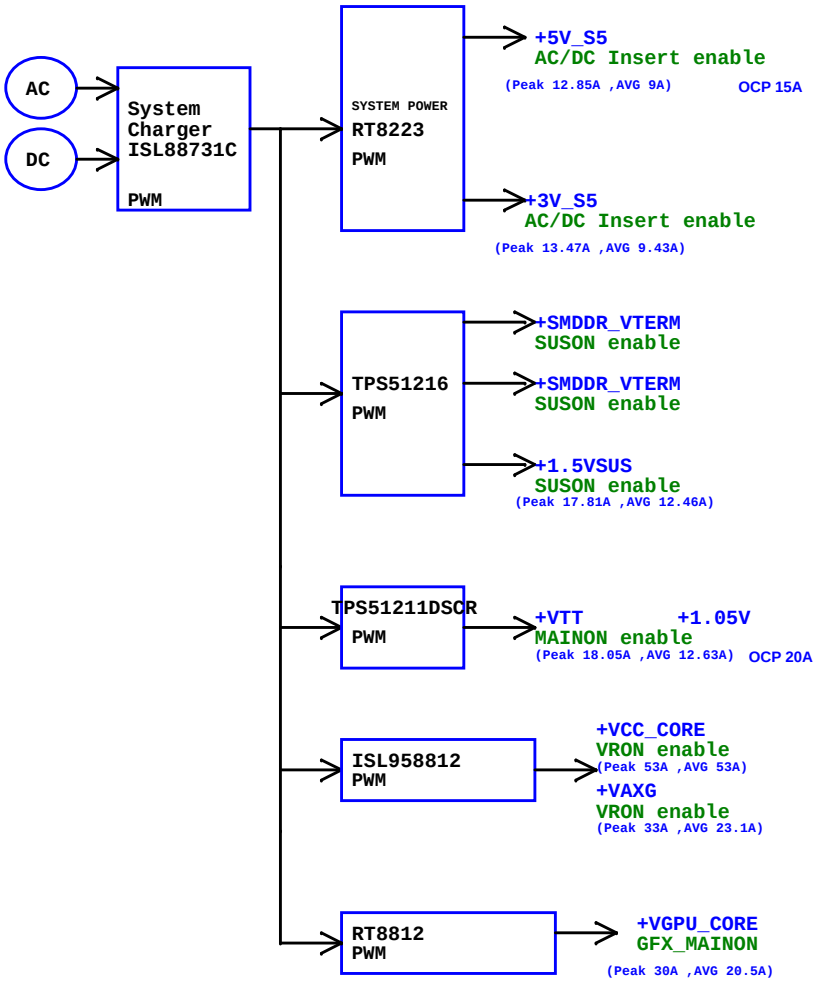


Quanta Computer Inc.

PROJECT : BDBD

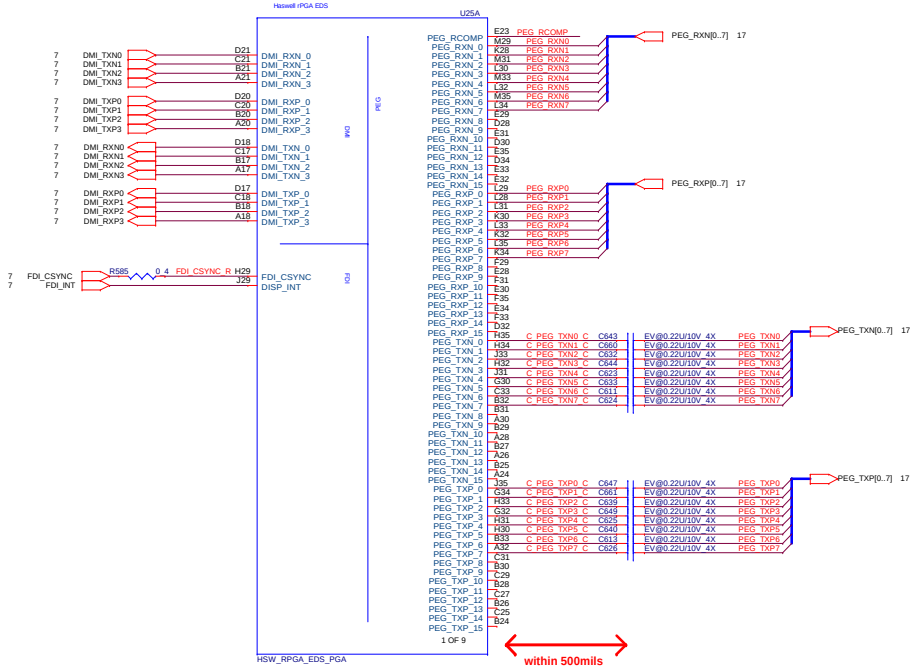
Size	Document Number	Rev
	Block Diagram	2A

Date: Monday, December 17, 2012 Sheet 1 of 45

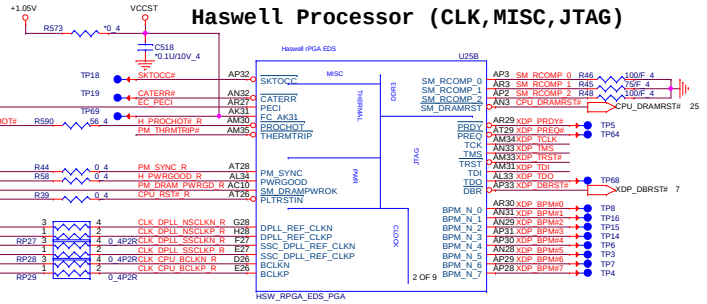


POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0~S5
+VCCRTC	+3.0V~+3.3V		S0~S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0~S5
+3V_HDP	+3.3V	MAIN_ON	S0
+3VPCU	+3.3V	AC/DC Insert enable	S0
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0~S5
+5VPCU	+5V	AC/DC Insert enable	S0~S5
WIMAX_P	+3.3V	WMAX_P for WLAN	
+1.8V	+1.8V	MAIN_ON	S0
+1.5V	+1.5V	MAIN_ON	S0
+1.5V_SUS	+1.5V	SUSON	S0~S3
+VCC_CORE		VRON	S0
+VTT	+1.05V	MAIN_ON	S0
+1.05V	+1.05V	MAIN_ON	S0
+VAXG		MPWROK	S0

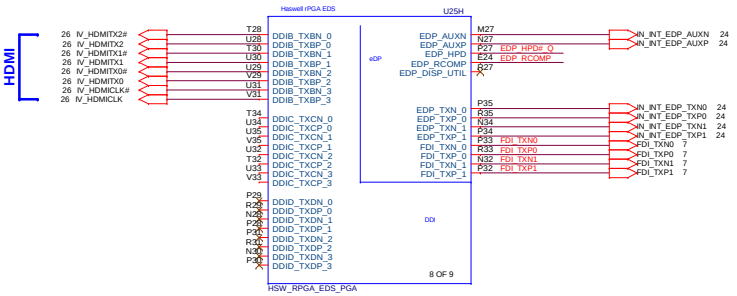
Haswell Processor (DMI,PEG,FDI)



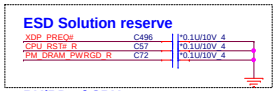
Haswell Processor (CLK,MISC,JTAG)



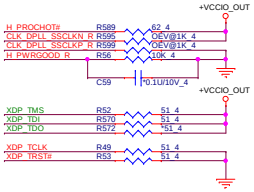
Haswell Processor (DDI,eDP,FDI)



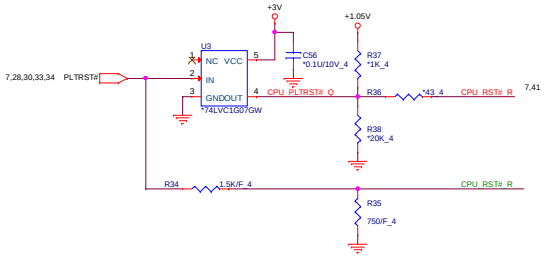
ESD Solution reserve



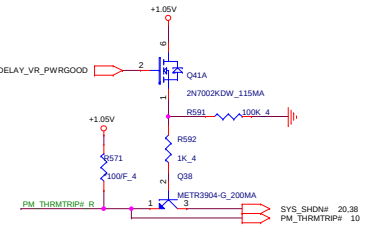
PU/PD of CPU



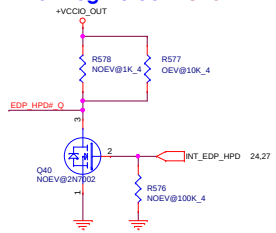
CPU



Thermal Trip & Process HOT CPU

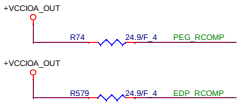


eDP Hot Plug Detect CPU

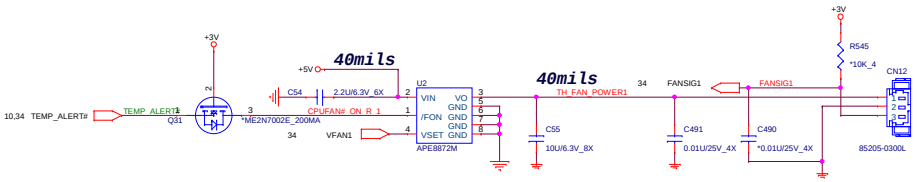


FDI Disabling (Discrete Only) <CPU>

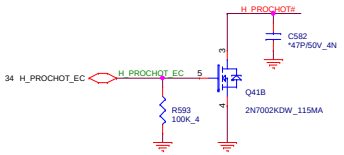
DP & PEG Compensation <CPU>



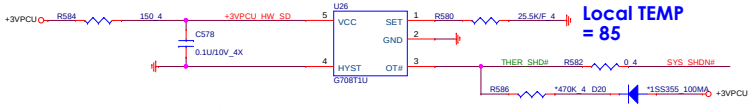
FAN Control-->For one FAN solution <THC>



Intel Turbo mode only CPU



CPU Thermal sensor / MB Local TEMP <THC>



Local TEMP = 85

Rset(Kohm)=0.0012T*T-0.9308T+96.147,Shut down on 85dgree
Hysteresis is 30C

Quanta Computer Inc.			
PROJECT : BDBD			
Size	Document Number		Rev
	Haswell 1/5 (PEG/DMI/FDI)		2A
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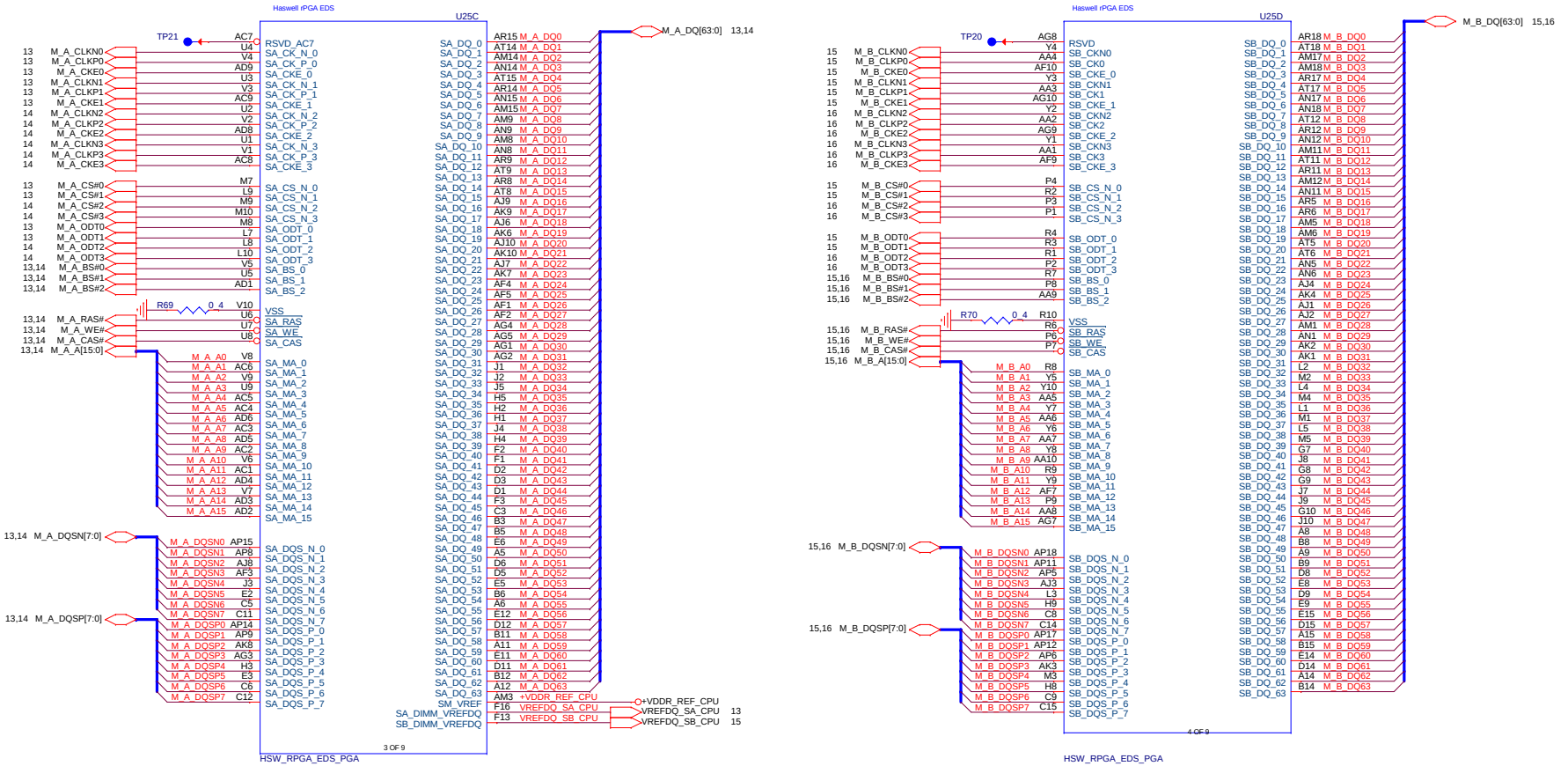
Haswell Processor (DDR3)



Quanta Computer Inc.		
PROJECT : BDBD		
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Haswell Processor (POWER)

05

+1.35V_CPU 4.2A

+VCCIN 95A

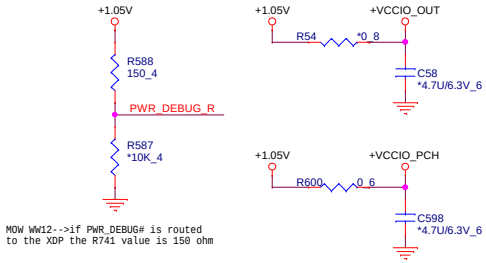
Haswell rPGA EDS

U25E

5 OF 9

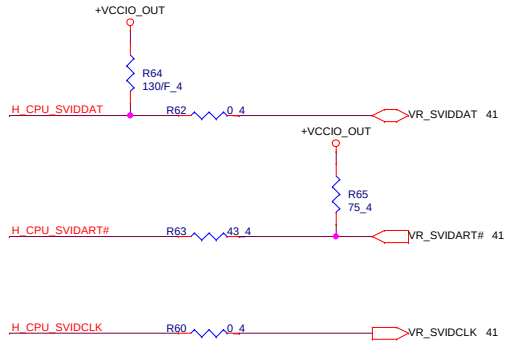
HSW_RPGA_EDS_PGA

Power Test Propose



MOW WW12-->if PWR_DEBUG# is routed to the XDP the R741 value is 150 ohm

SVID



Quanta Computer Inc.		
PROJECT : BDBD		
Size	Document Number: Haswell 4/5 (POWER)	Rev: 2A
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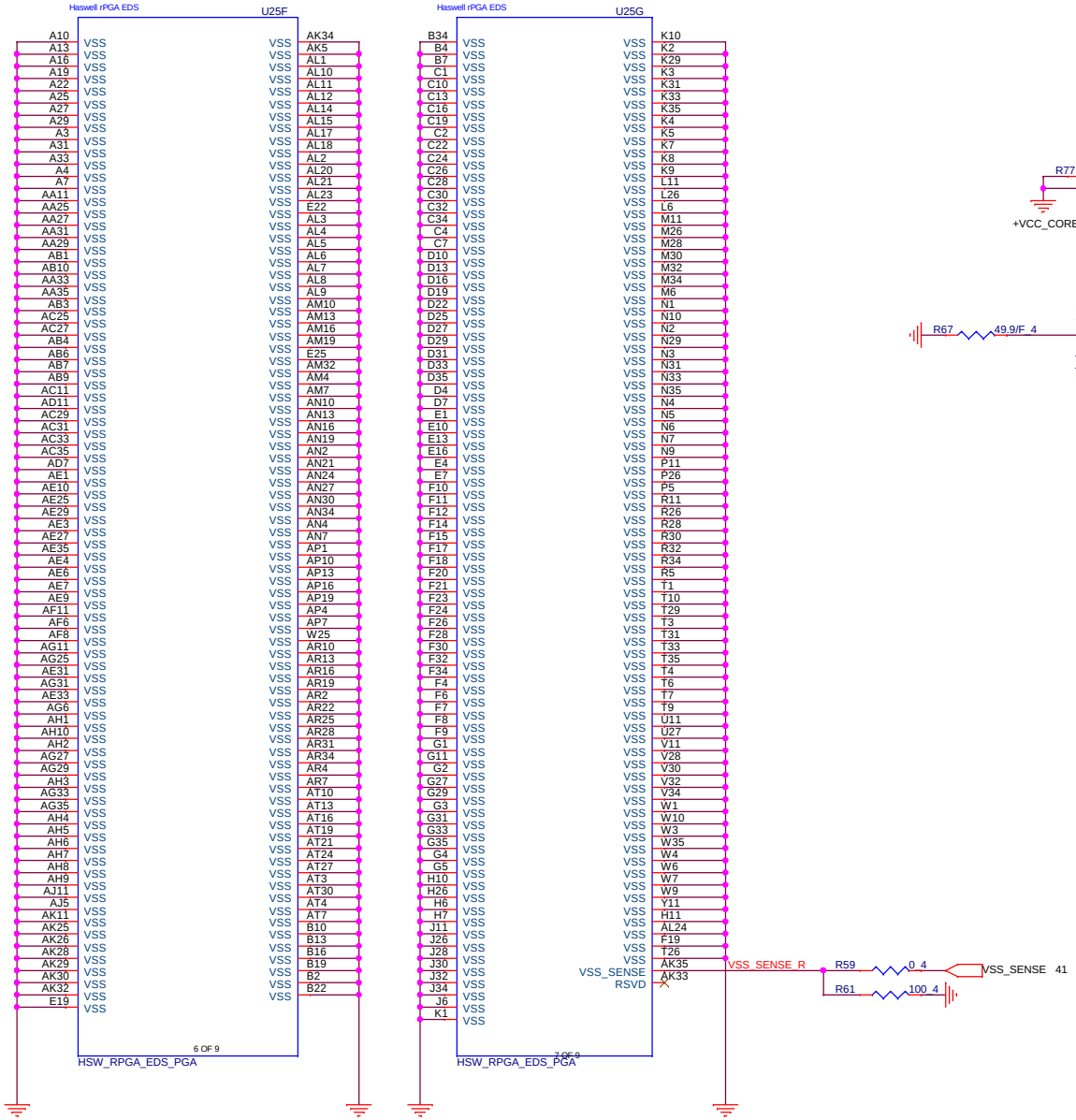
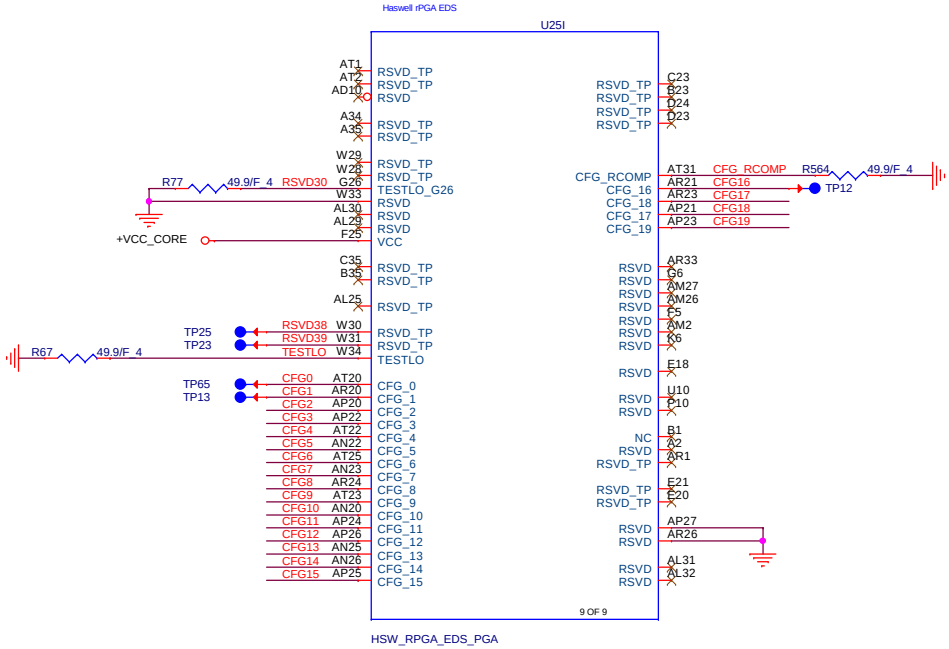
Haswell Processor (GND)



Haswell Processor (CFG,RSVD)



06

Quanta Computer Inc.		
PROJECT : BDBD		
Size	Document Number: Haswell 5/5 (CFG/GND)	Rev: 2A
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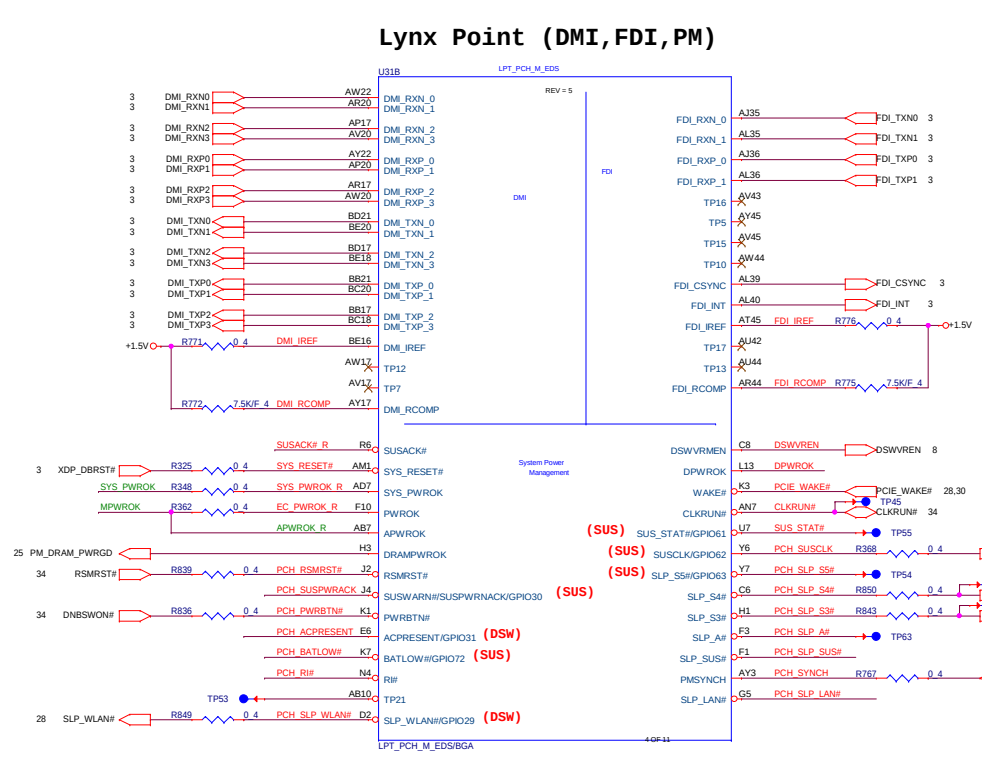
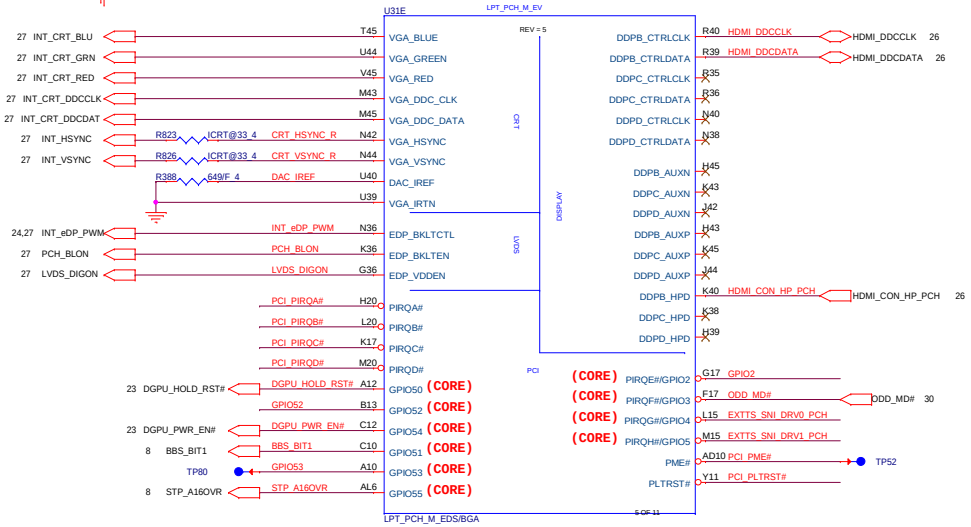
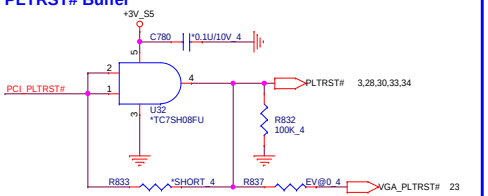
Lynx Point (DMI,FDI,PM)



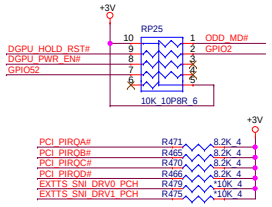
Lynx Point (CRT,PCI,DDI CNTL)

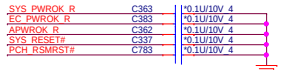


PLTRST# Buffer

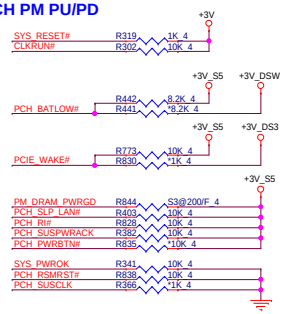


PCI PU

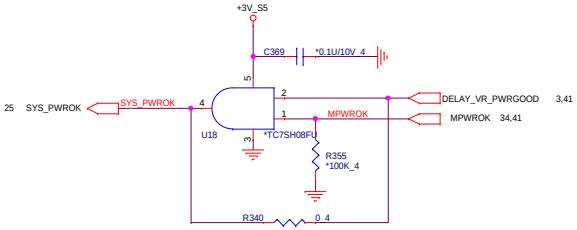




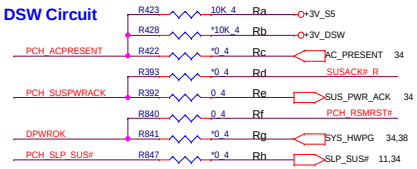
PCH PM PU/PD

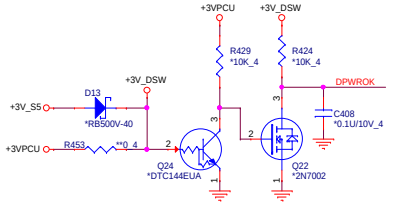


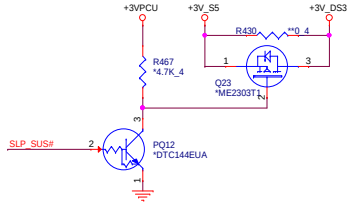
SYSPWOK



DSW Circuit







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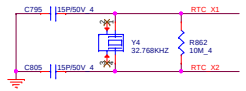
Lynx Point (RTC,IHDA,SATA,JTAG)

Lynx Point (LPC,SPI,SMBUS,C-LINK,THERMAL)

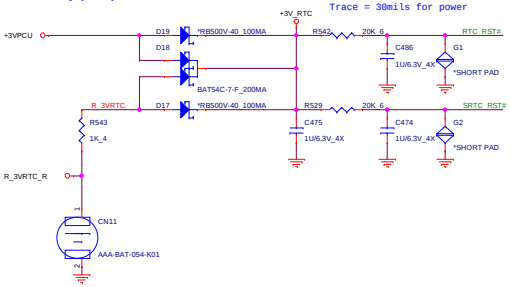
08

RTC Clock 32.768KHz (RTC)

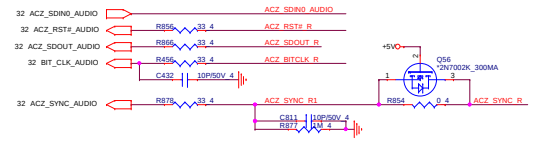


RTC Circuitry (RTC)

Trace = 30mils for power

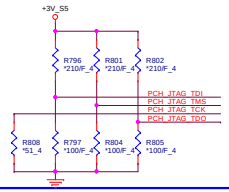


HDA

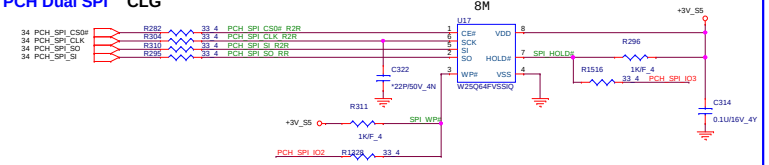


PCH JTAG

JTAG_TCK,JTAG_TMS
Trace Length < 9000mils

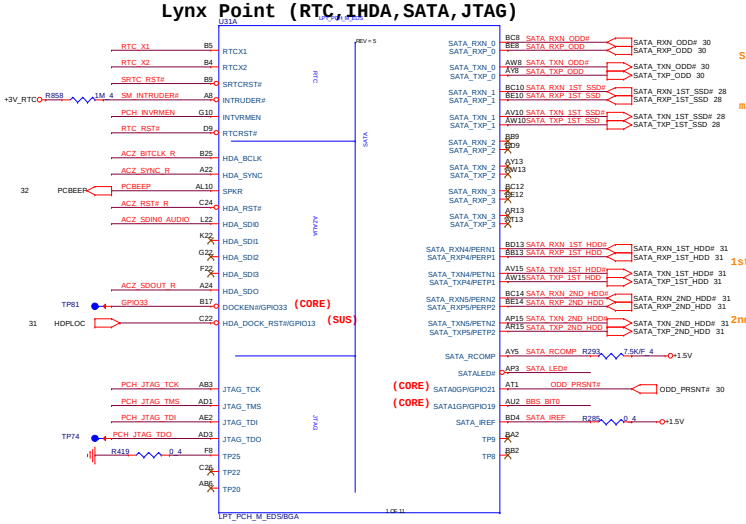


PCH Dual SPI CLG

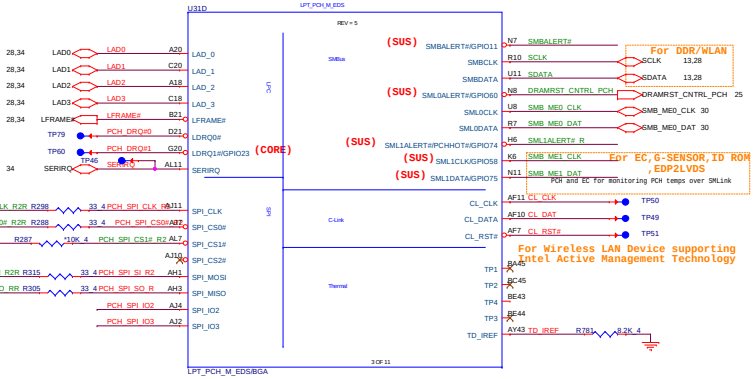


EC (EC+BIOS):SPI_CS0#

Lynx Point (RTC,IHDA,SATA,JTAG)

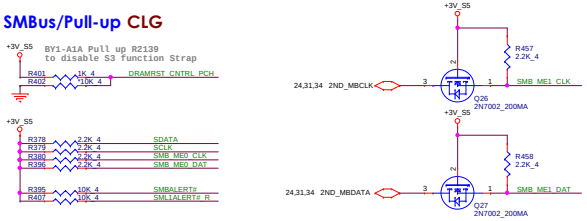


Lynx Point (LPC,SPI,SMBUS,C-LINK,THERMAL)



CLG

SMBus/Pull-up CLG



PCH STRAPING

Pin Name	Usage	Sampled	Configuration	Circuitry
SPKR	No Reboot	PWROK	0 = Disable (Int PD) 1 = Enable	PCBEEP R438 *1K_4 +3V
GPIO62 / SUSCLK	PLL On-Die Voltage Regulator Enable	RSMRST#	0 = Disable 1 = Enable (Int PU)	7,34 SUSCLK R367 *1K_4
GPIO55	Top-Block Swap Override	PWROK	0 = Top-Block Swap mode 1 = Default (Int PU)	7 STP_A16OVR R335 *1K_4
INTVRMEN	Integrated VRM Enable	Always	0 = Disable 1 = Enable	PCH_INVRMEN R431 330K_4 +3V_RTC
GPIO51	Boot BIOS Strap bit 1	PWROK	Bit1 Bit0 1 0 Resvered 1 1 SPI 0 0 LPC	7 BBS_BIT1 R432 *1K_4
SATA1GP/GPIO19	Boot BIOS Strap bit 0	PWROK		BBS_BIT0 R783 *1K_4
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Security Effect (Int PD) 1 = Can be Override	34 ACZ_SDOUT R851 *1K_4 VCC_HDA_IO
GPIO36	RSVD	PWROK	Internal PD	10 GPIO36 R786 *1K_4 +3V
SATA3GP/GPIO37	TLS Confidentiality	PWROK	0 = TLS no confidentiality (Int PD) 1 = TLS with confidentiality	10 FDI_OVRVLTG R795 *1K_4 +3V
GPIO8	RSVD	RSMRST#	Internal PU	10 GPIO8 R815 10K_4
GPIO28	PLL on die VR enable	RSMRST#	0 = Disable 1 = Enable (Int PU)	10 PLL_ODVR_EN R358 *1K_4
DSWVREN	On Die DSW VR Enable	Always	0 = Disable 1 = Enable Must be PU to VCCRTC	7 DSWVREN R857 330K_4 R862 330K_4 +3V_RTC

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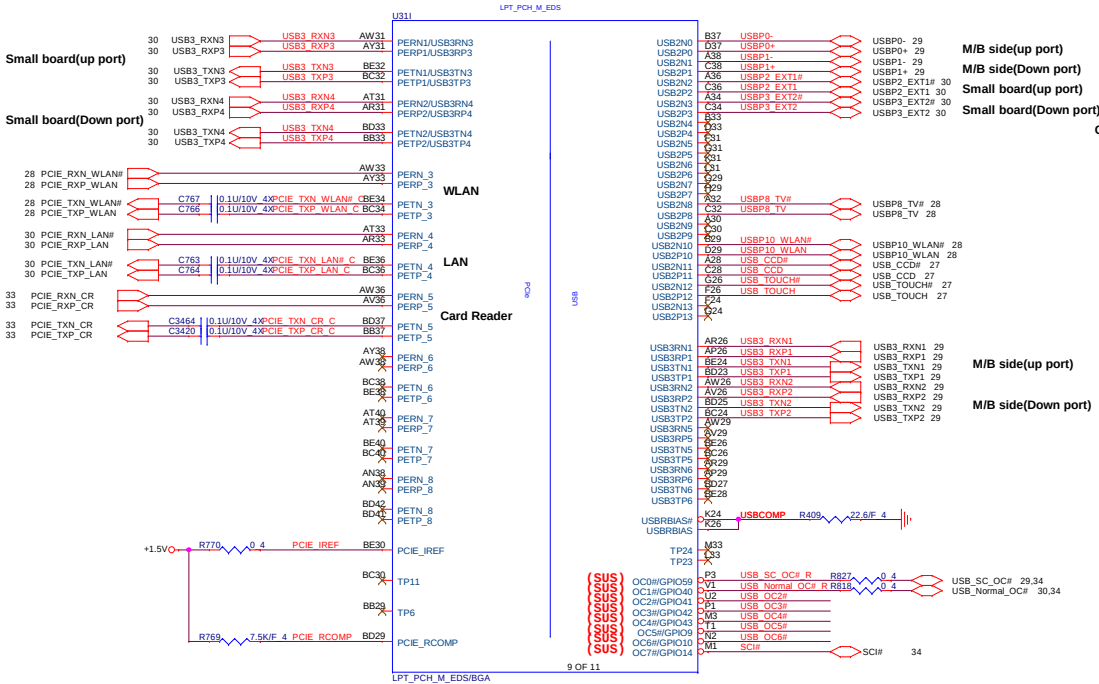
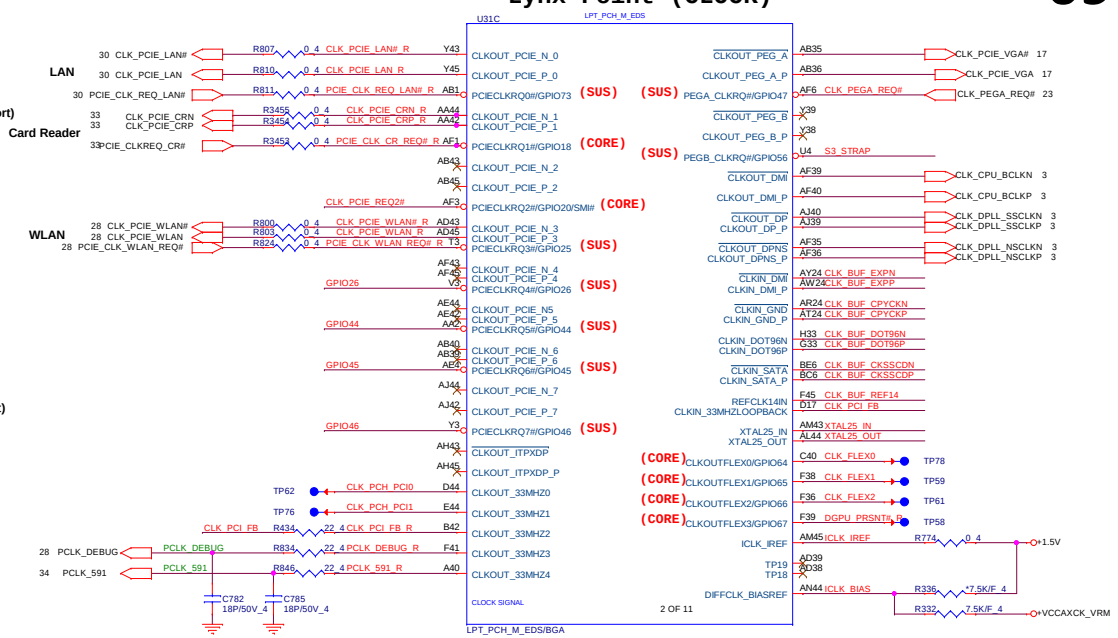
Lynx Point (PCIE,USB3.0,USB2.0)

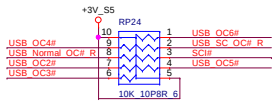
Lynx Point (CLOCK)

09

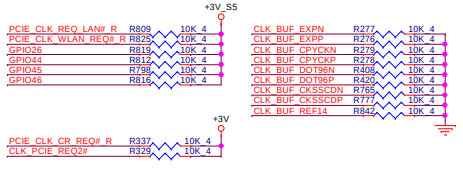


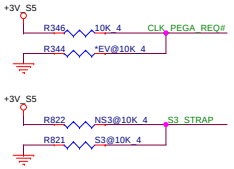


USB Overcurrent

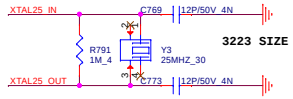


PCH Intenal Clock





25MHz Crystal for PCH



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Size	Document Number: LPT 3/6 (PCIE/USB/CLK)	Rev: 2A
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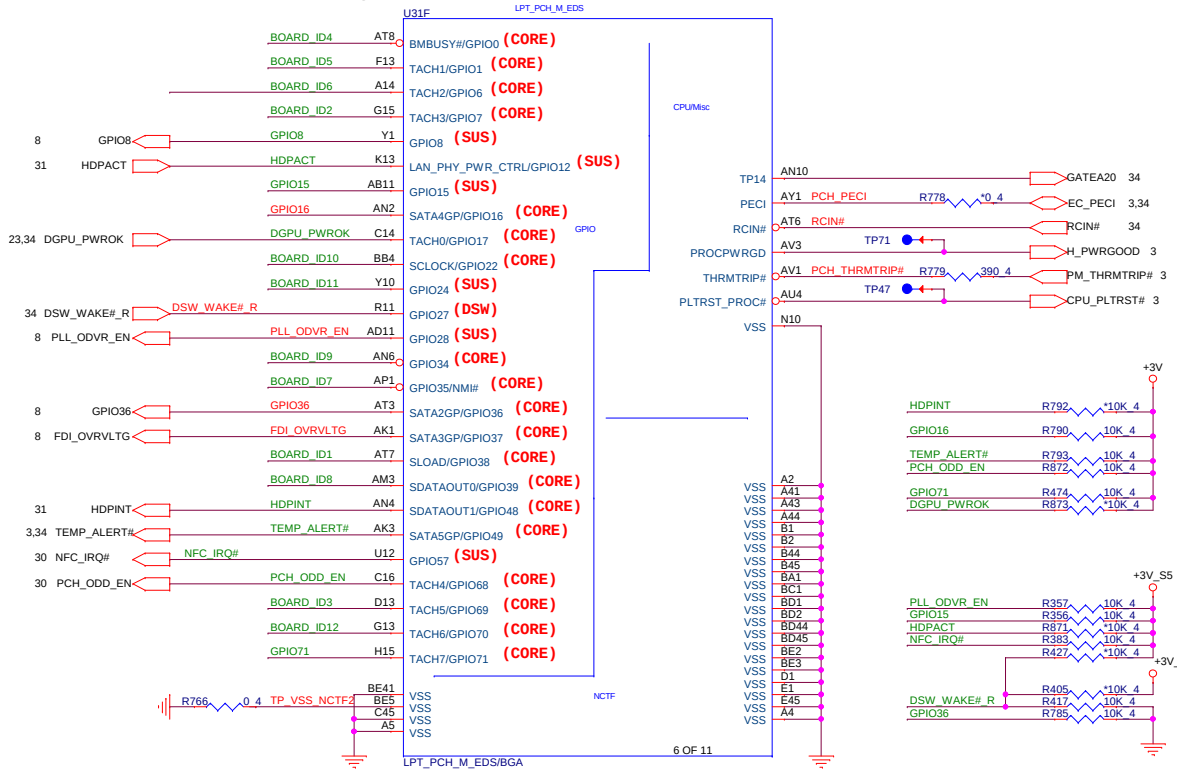
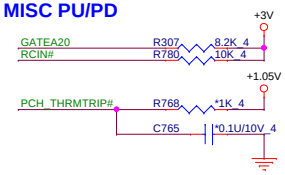
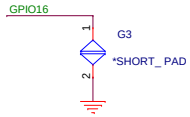
Lynx Point (GPIO,CPU/MISC,NCTF)



PCH MISC PU/PD

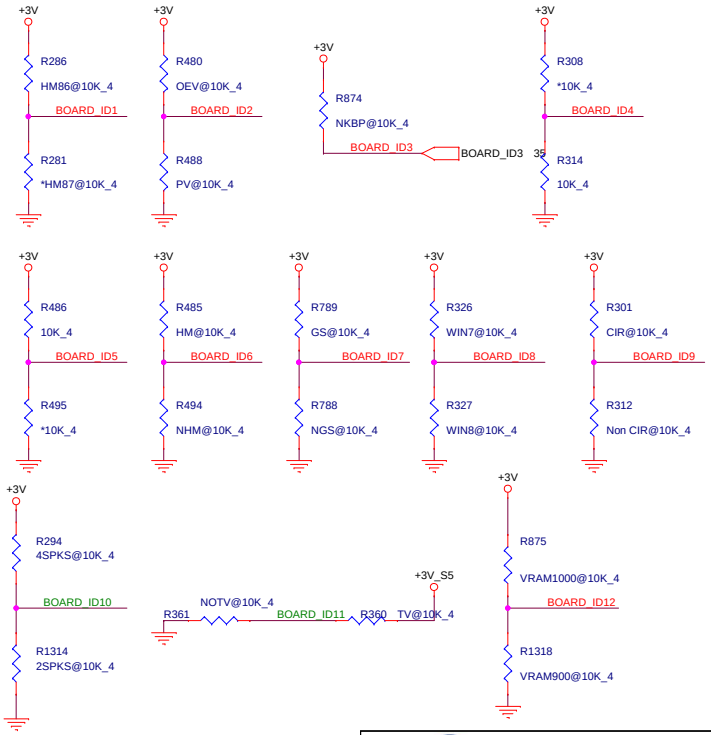


PU & Password Clear



BOARD ID SETTING CLG/PX/OEV/UGA/CLG-Strap

Board ID	ID1	ID2	ID3	ID4	ID5	ID6	ID7	ID8	ID9	ID10	ID11	ID12
HM86 HM87	H L											
Only VGA OPTIMUS		H L										
W/O LED KB W/ LED KB			H L									
UMA Discrete				H L								
17" Premium 17" Gaming					H L							
W/ HDMI W/O HDMI						H L						
W/ G-sensor W/O G-sensor							H L					
WIN7 WIN8								H L				
ECO Mode 3D Mode									H L			
4 SPKS 2 SPKS										H L		
TV SKU SSD SKU											H L	
VRAM 1000 VRAM 900												H L



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	LPT 4/6 (GPIO/MISC)	2A

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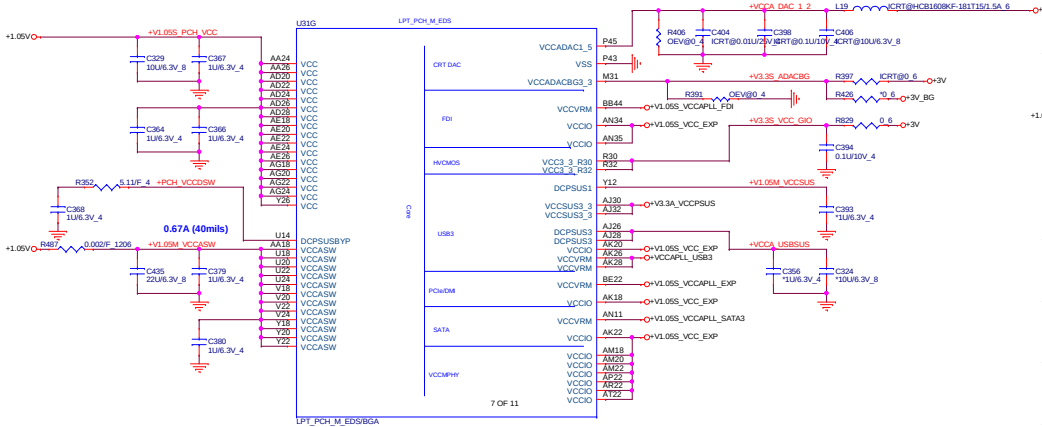
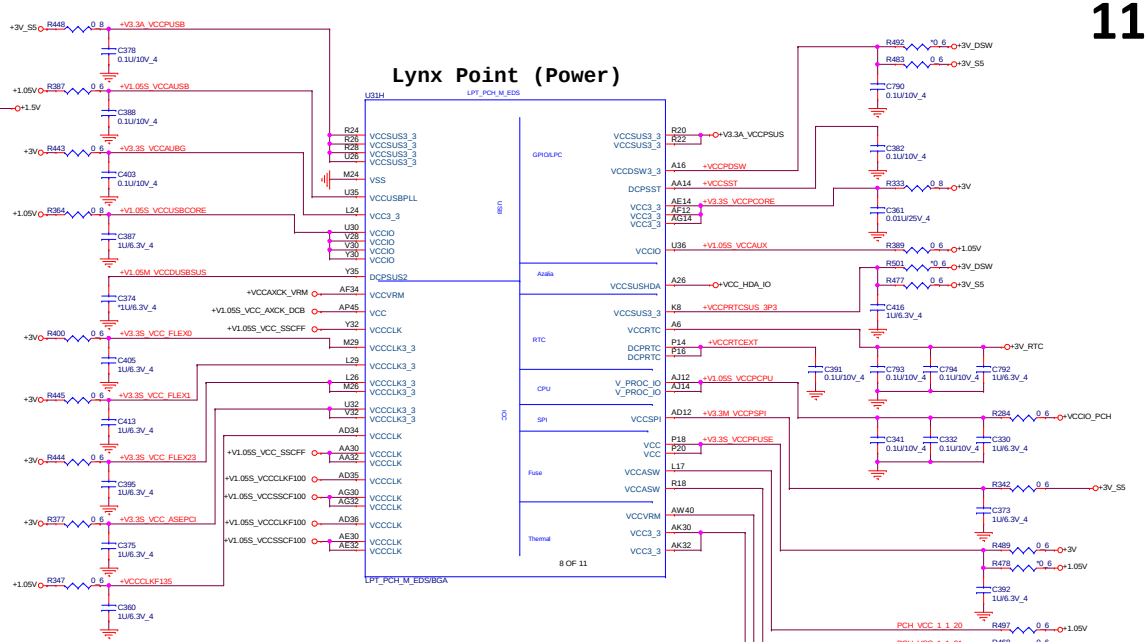
Lynx Point (Power)

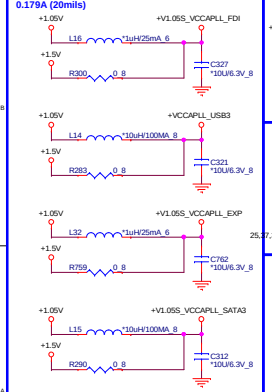




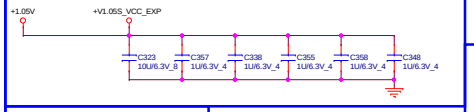
Lynx Point (Power)

PCH VRM Power

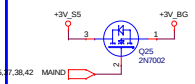
0.179A (20mils)



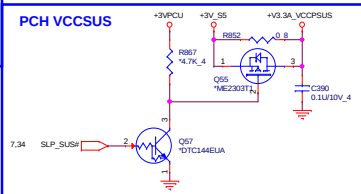
PCH VCCIO Power



PCH band gap Power

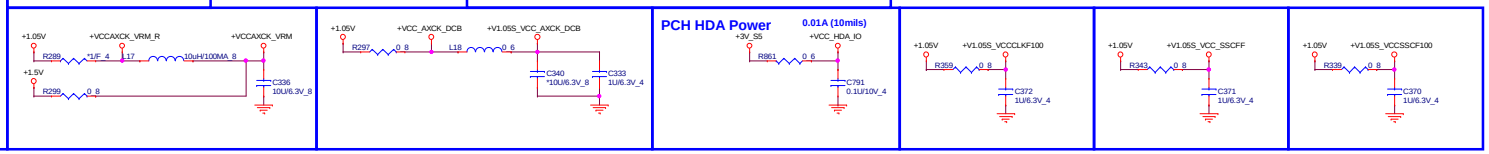


PCH VCCSUS



PCH HDA Power

0.01A (10mils)



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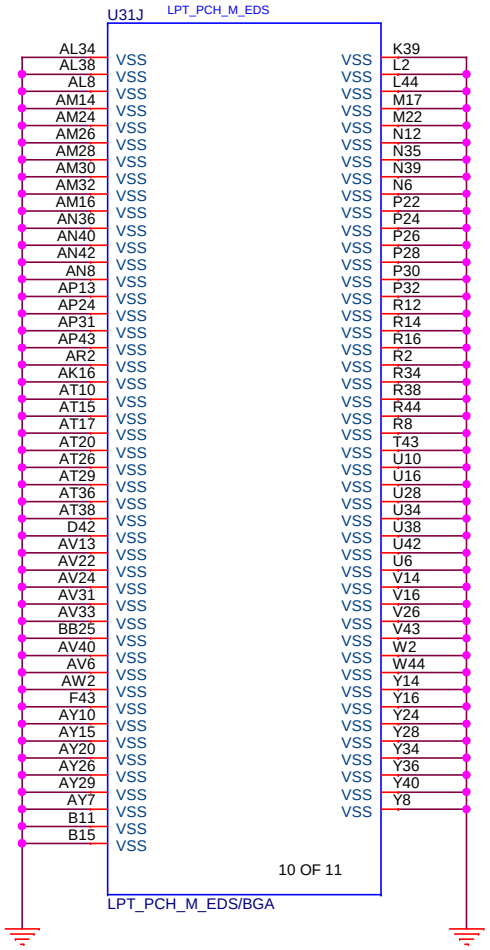
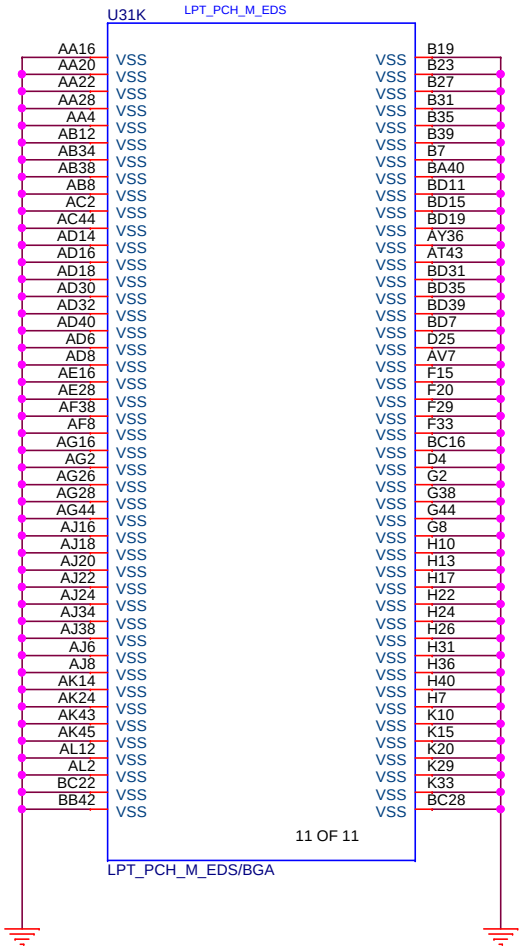
Lynx Point (GND)



Lynx Point (GND)



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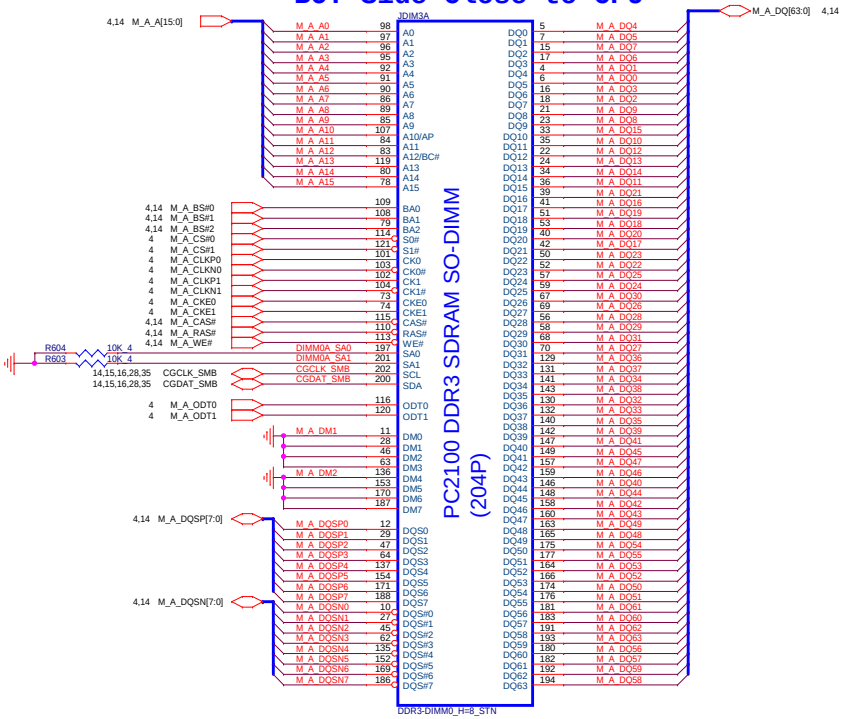
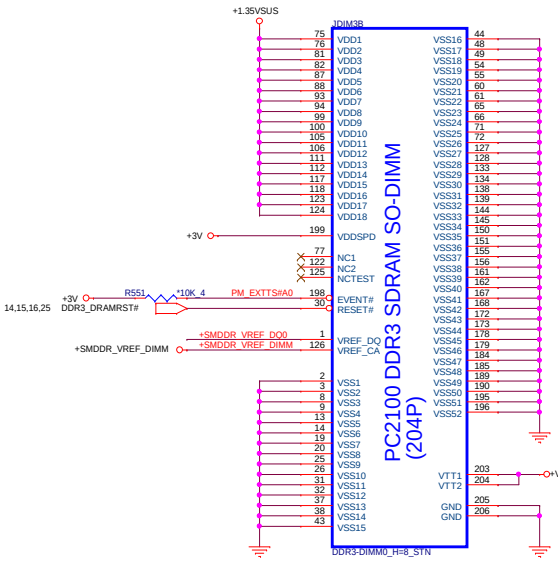
BOT Side Close to CPU



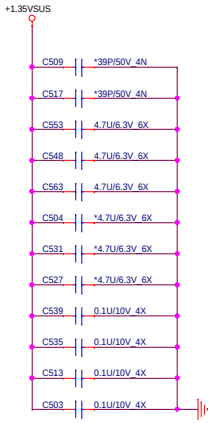


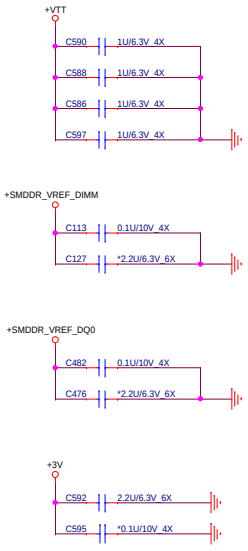
3,7,8,9,10,11,14,15,16,23,24,26,27,28,30,31,33,34,35,36,38,42 +3V

14,15,16,25,39 +VTT

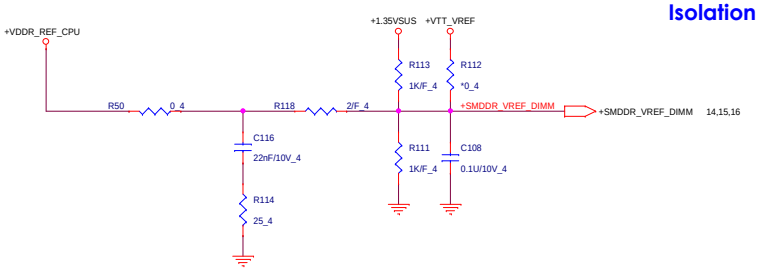
14,15,16 +SMDDR_VREF_DIMM

DDR3 VREF CA



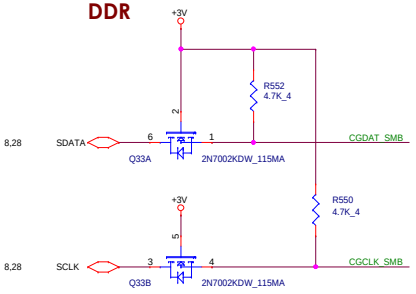


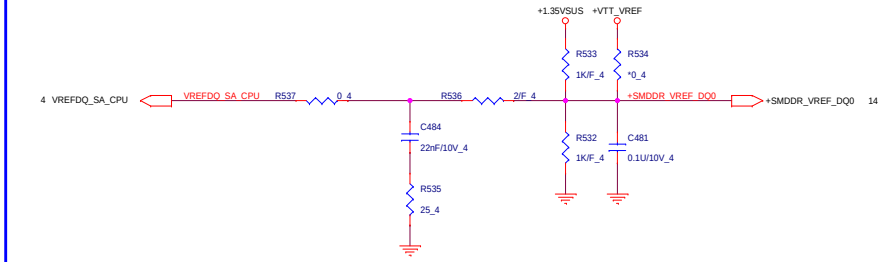
DDR



SMBus Isolation

DDR





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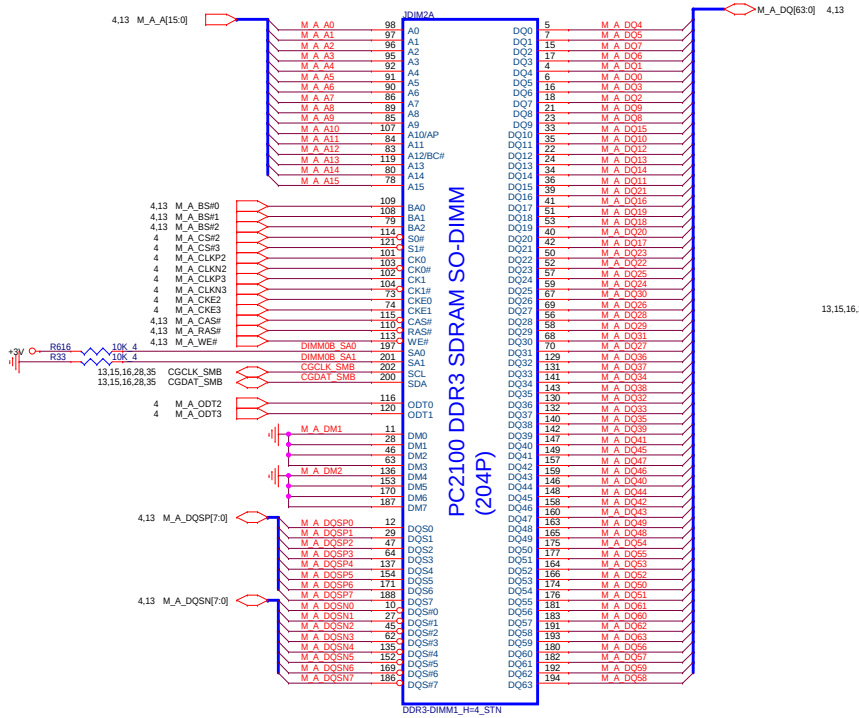
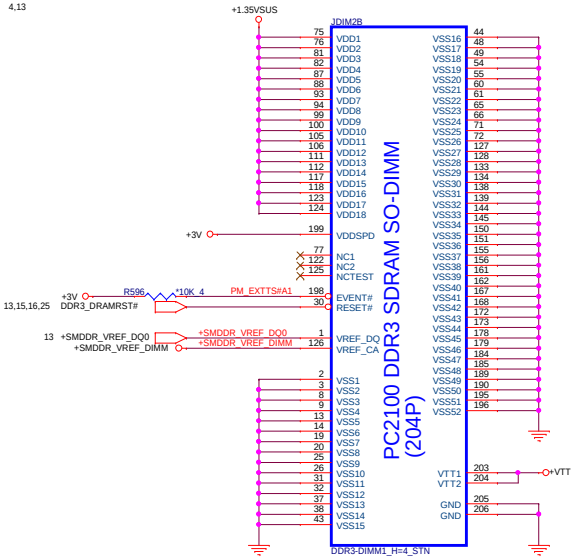
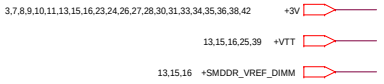
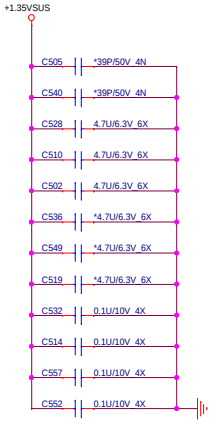
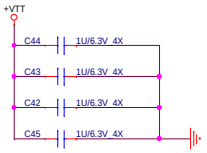
TOP Side Close to CPU

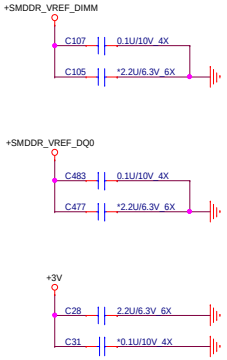












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Size	Document Number		Rev
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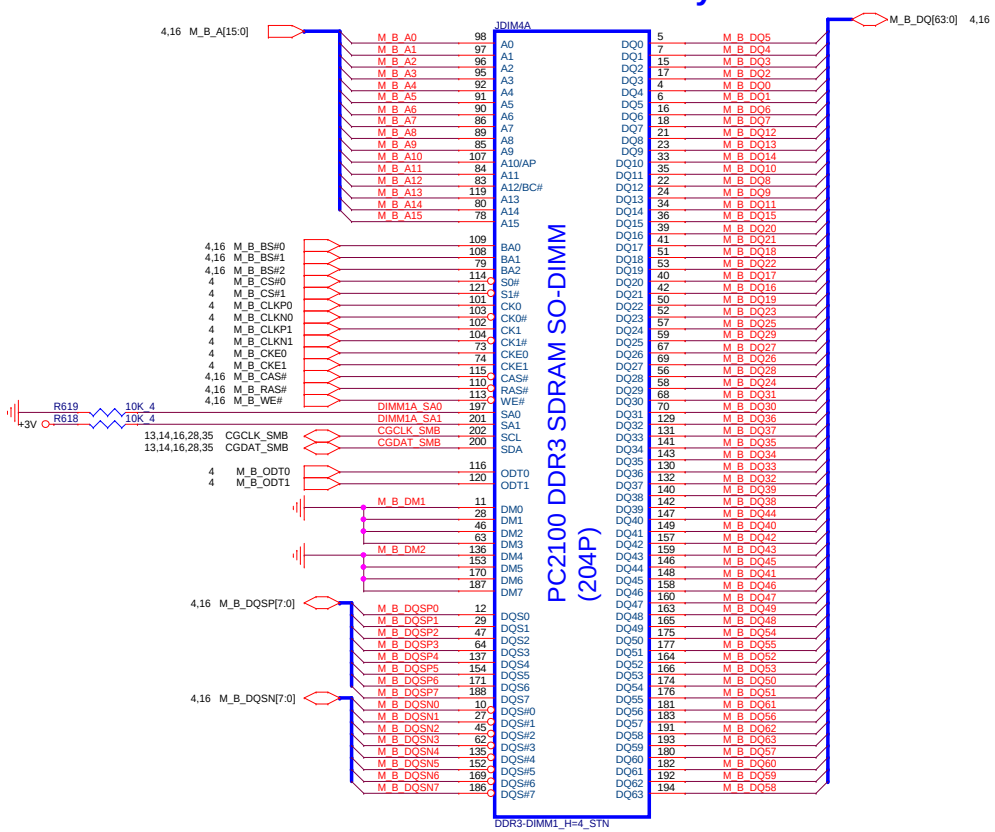
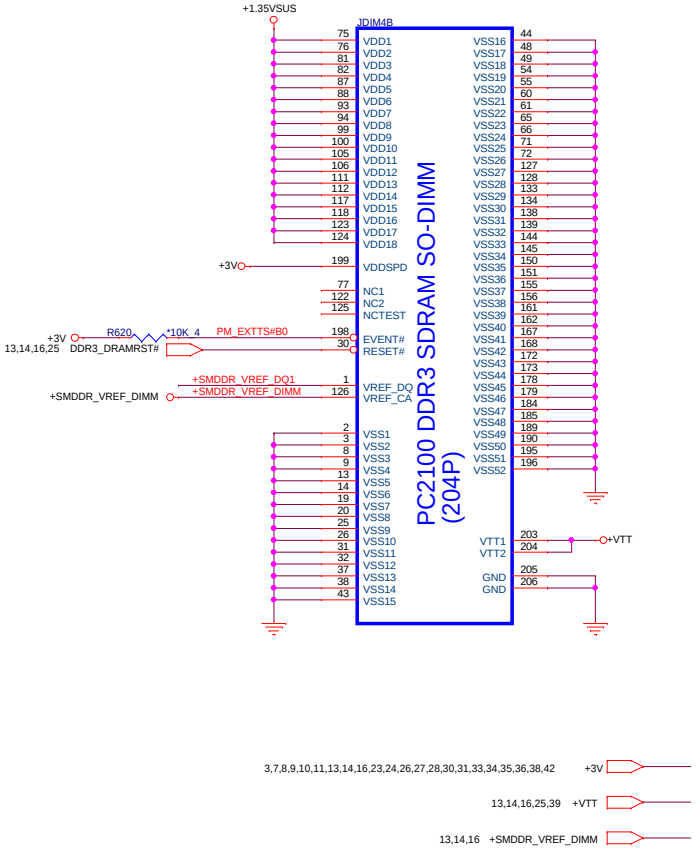
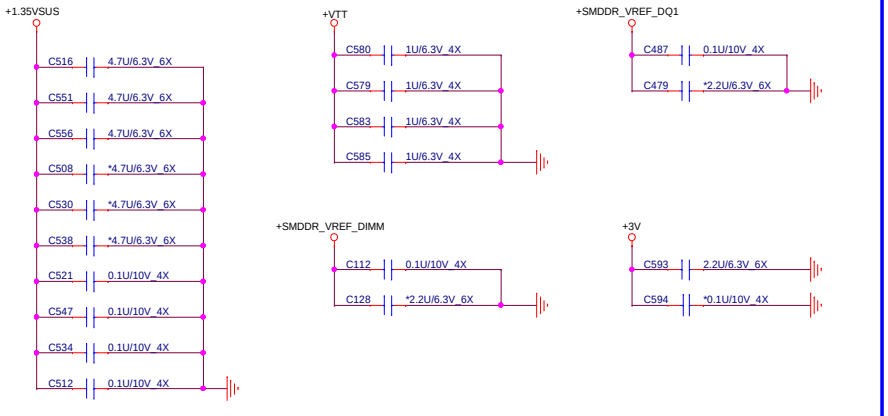
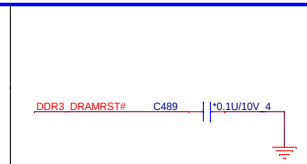
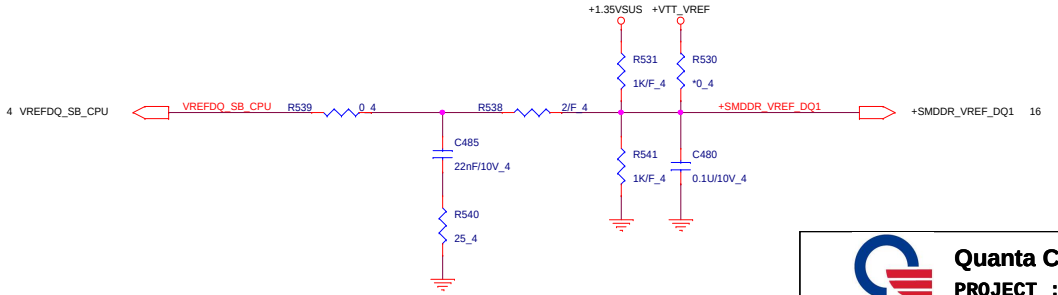
BOT Side Far away CPU











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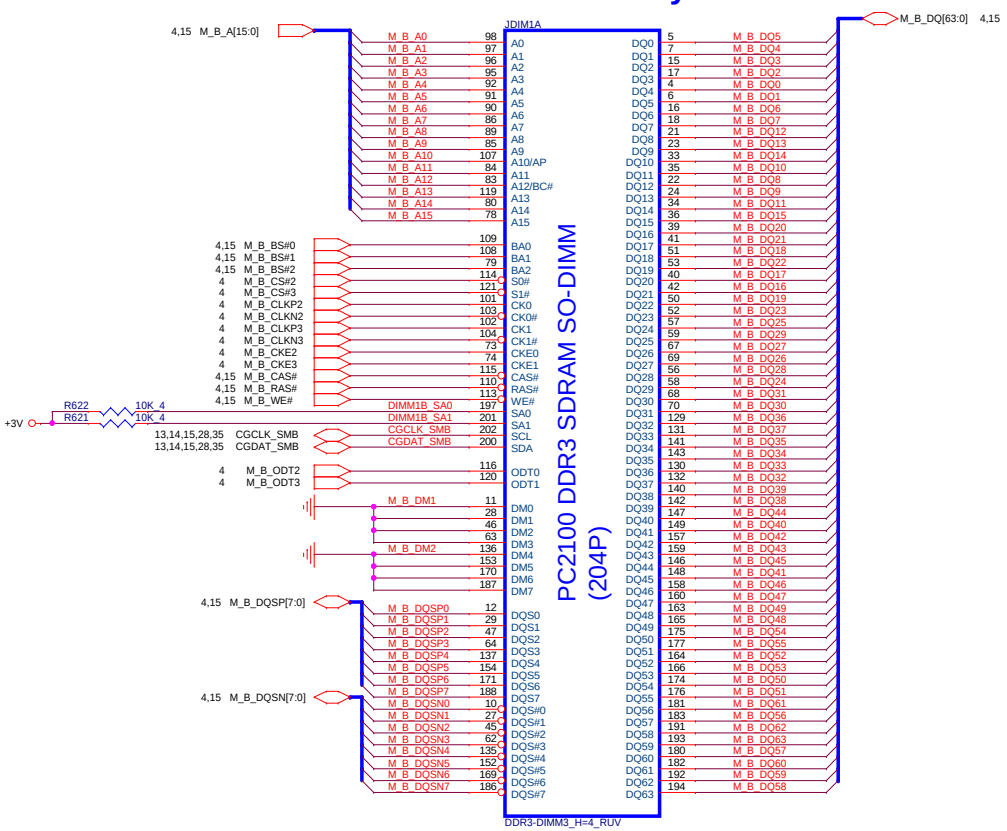
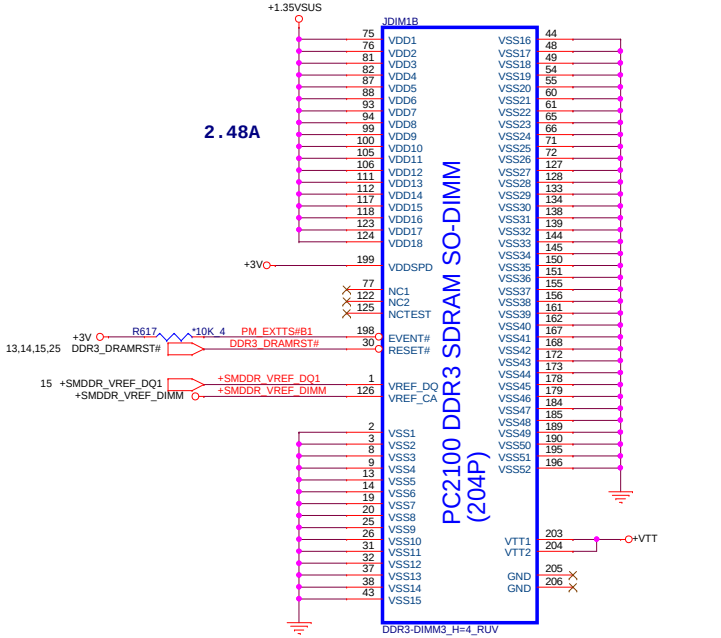
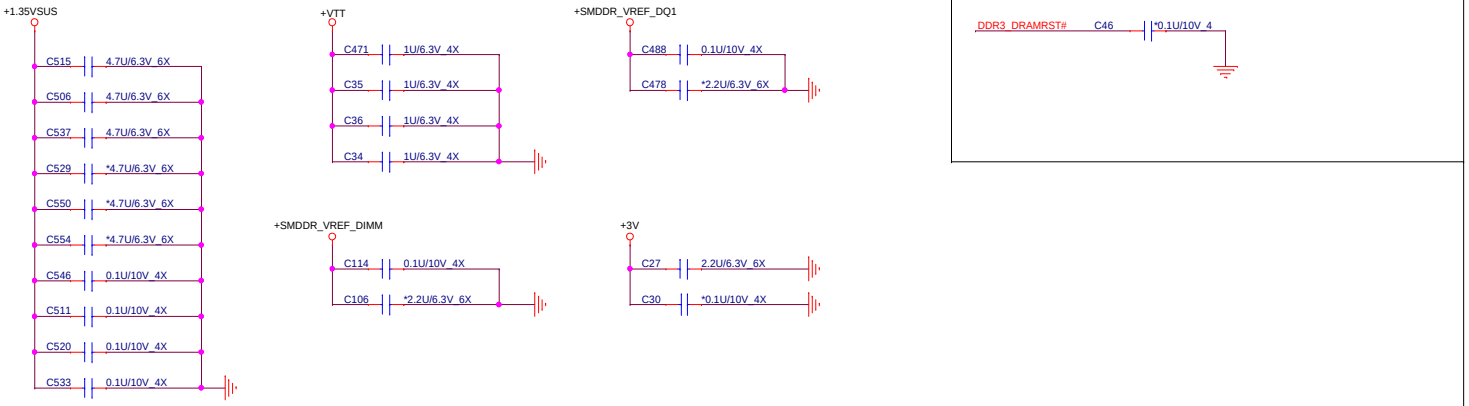
TOP Side Far away CPU







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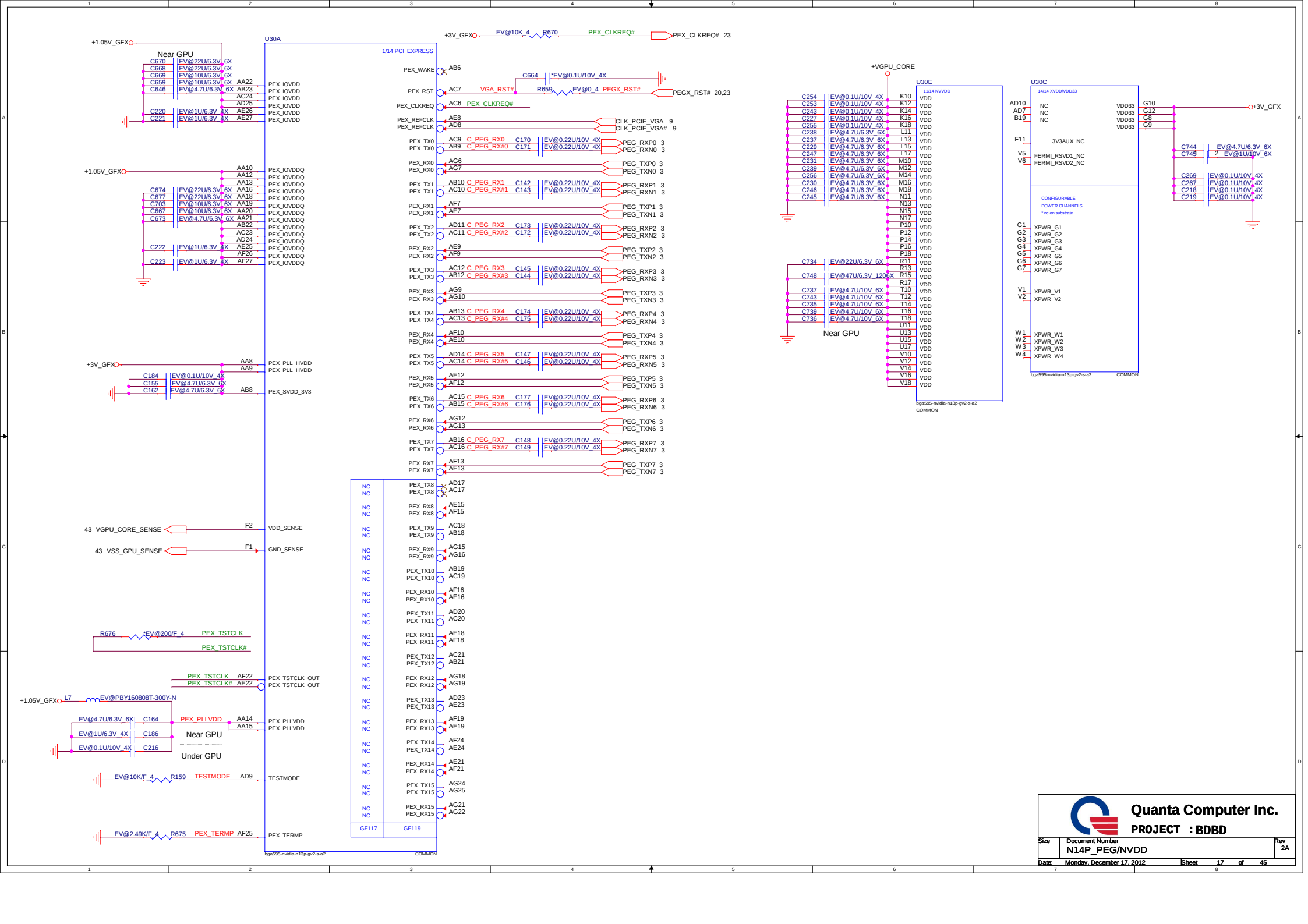
U30A
1/14 PCI_EXPRESS
Near GPU
Under GPU
+1.05V_GFX
+3V_GFX
+VGPU_CORE
U30E
11/14 NVVDD
U30C
14/14 XVDD/VDD33
3V3AUX_NC
CONFIGURABLE
POWER CHANNELS
* nc on substrate
bga595-nvidia-n13p-gv2-s-a2
COMMON
PEX_WAKE
PEX_RST
PEX_CLKREQ
PEX_REFCLK
PEX_REFCLK#
PEX_TX0
PEX_TX0#
PEX_RX0
PEX_RX0#
PEX_TX1
PEX_TX1#
PEX_RX1
PEX_RX1#
PEX_TX2
PEX_TX2#
PEX_RX2
PEX_RX2#
PEX_TX3
PEX_TX3#
PEX_RX3
PEX_RX3#
PEX_TX4
PEX_TX4#
PEX_RX4
PEX_RX4#
PEX_TX5
PEX_TX5#
PEX_RX5
PEX_RX5#
PEX_TX6
PEX_TX6#
PEX_RX6
PEX_RX6#
PEX_TX7
PEX_TX7#
PEX_RX7
PEX_RX7#
PEX_TX8
PEX_TX8#
PEX_RX8
PEX_RX8#
PEX_TX9
PEX_TX9#
PEX_RX9
PEX_RX9#
PEX_TX10
PEX_TX10#
PEX_RX10
PEX_RX10#
PEX_TX11
PEX_TX11#
PEX_RX11
PEX_RX11#
PEX_TX12
PEX_TX12#
PEX_RX12
PEX_RX12#
PEX_TX13
PEX_TX13#
PEX_RX13
PEX_RX13#
PEX_TX14
PEX_TX14#
PEX_RX14
PEX_RX14#
PEX_TX15
PEX_TX15#
PEX_RX15
PEX_RX15#
PEX_IOVDD
PEX_IOVDDQ
PEX_PLL_HVDD
PEX_SVDD_3V3
PEX_PLLVDD
PEX_TSTCLK_OUT
PEX_TSTCLK
PEX_TSTCLK#
TESTMODE
PEX_TERMP
VDD_SENSE
GND_SENSE
VGPU_CORE_SENSE
VSS_GPU_SENSE
PEX_CLKREQ#
VGA_RST#
PEGX_RST#
CLK_PCIE_VGA
CLK_PCIE_VGA#
PEG_RXP0
PEG_RXN0
PEG_TXP0
PEG_TXN0
PEG_RXP1
PEG_RXN1
PEG_TXP1
PEG_TXN1
PEG_RXP2
PEG_RXN2
PEG_TXP2
PEG_TXN2
PEG_RXP3
PEG_RXN3
PEG_TXP3
PEG_TXN3
PEG_RXP4
PEG_RXN4
PEG_TXP4
PEG_TXN4
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PEG_TXN5
PEG_RXP6
PEG_RXN6
PEG_TXP6
PEG_TXN6
PEG_RXP7
PEG_RXN7
PEG_TXP7
PEG_TXN7
XPWR_G1
XPWR_G2
XPWR_G3
XPWR_G4
XPWR_G5
XPWR_G6
XPWR_G7
XPWR_V1
XPWR_V2
XPWR_W1
XPWR_W2
XPWR_W3
XPWR_W4
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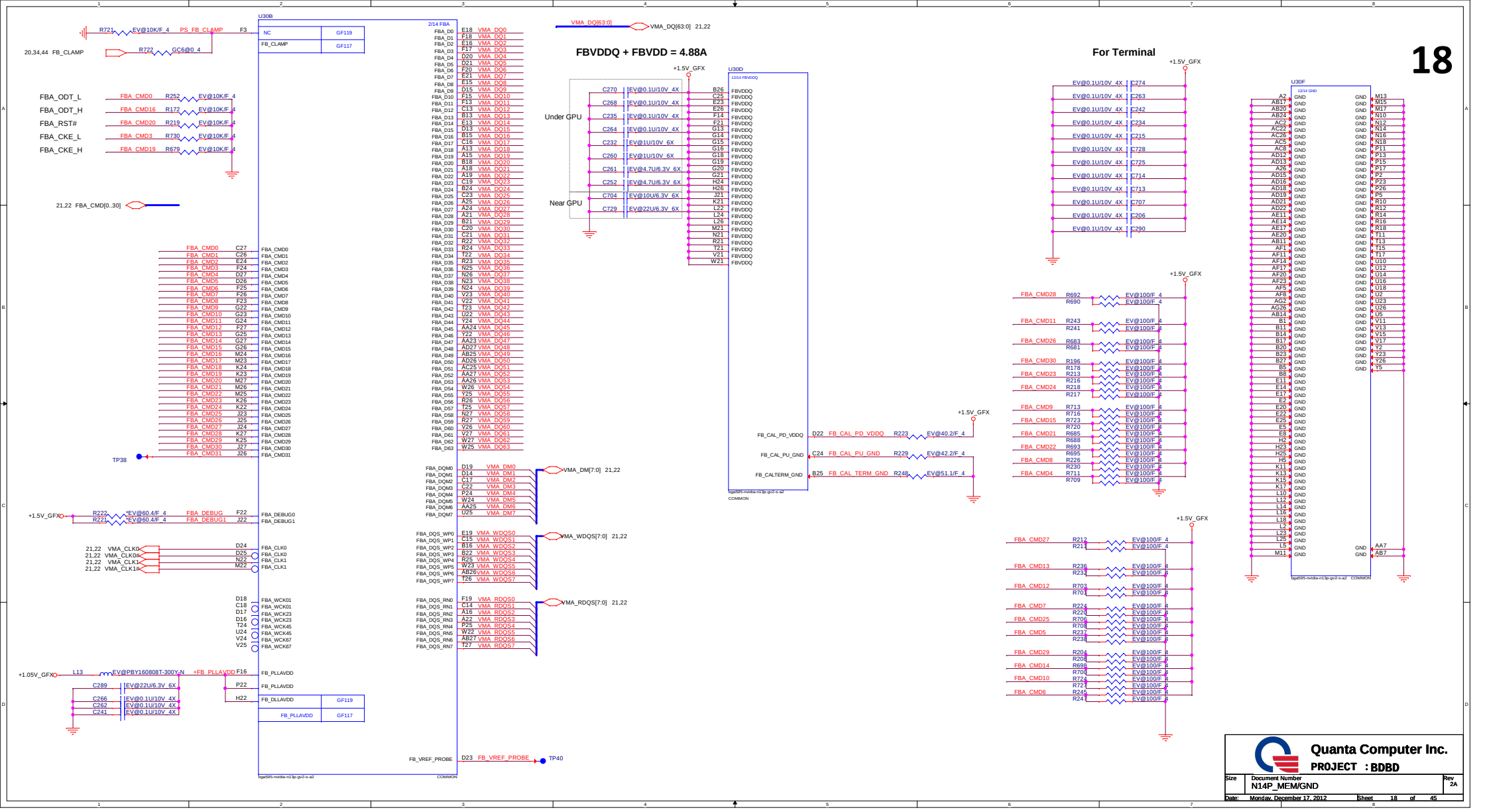

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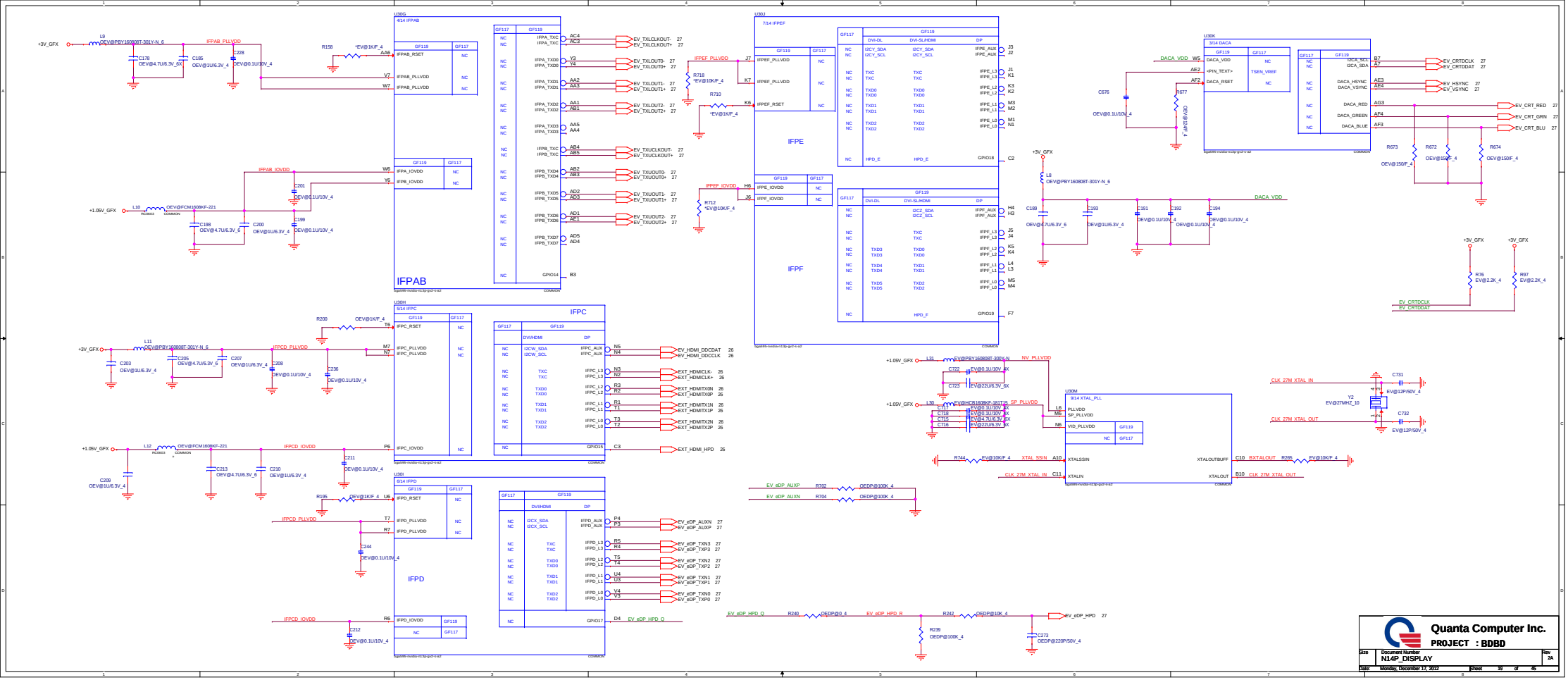
IFPAB
IFPE
IFPF
IFPC
IFPD
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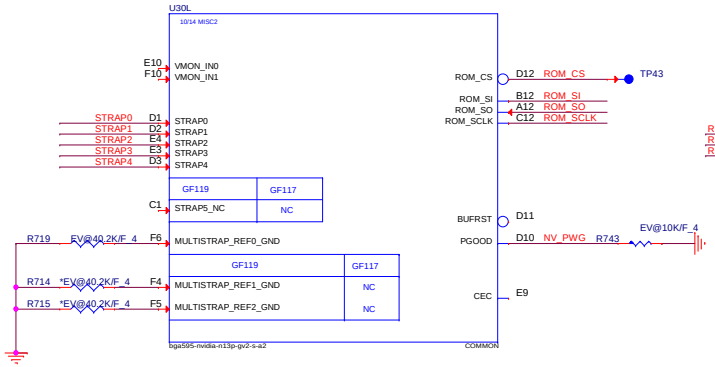
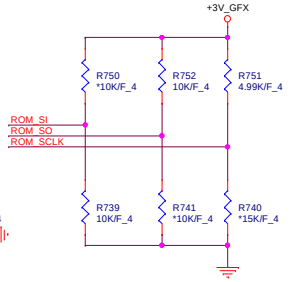
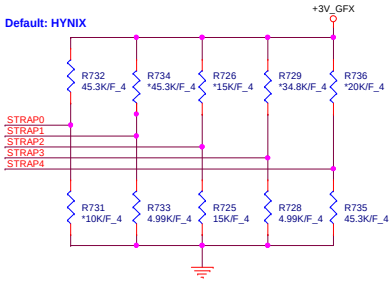
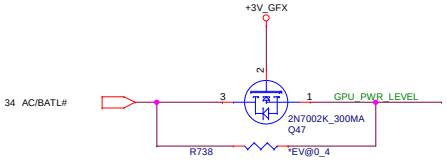
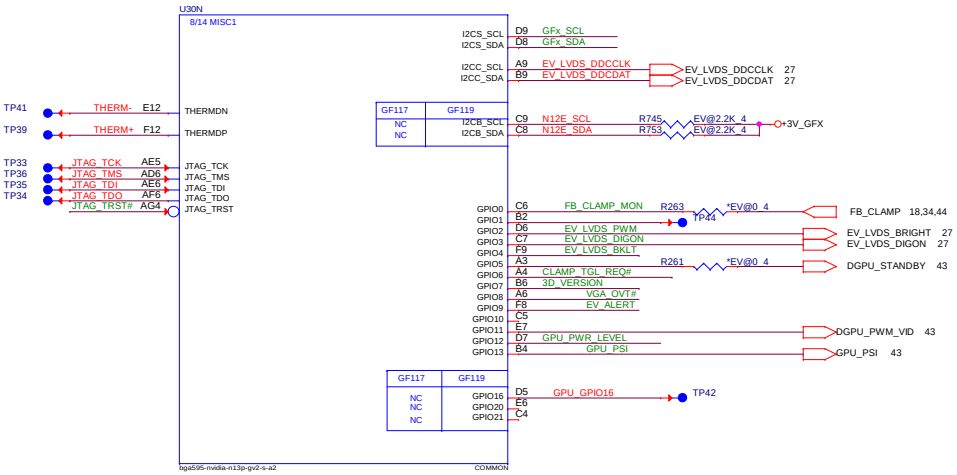
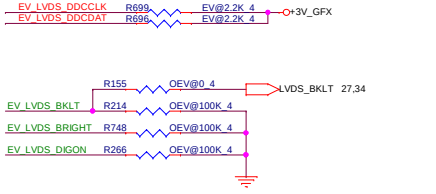




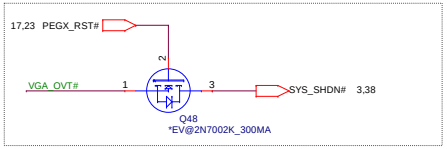


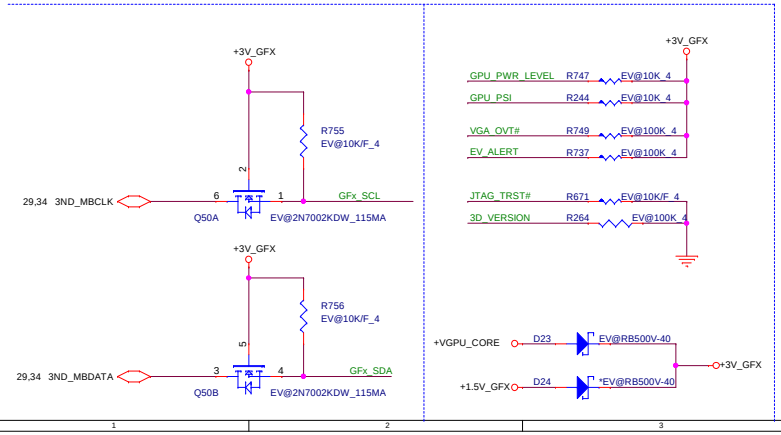


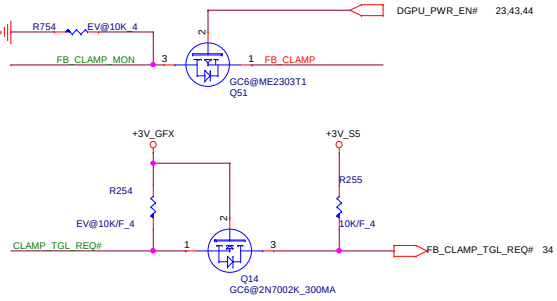




External LVDS control







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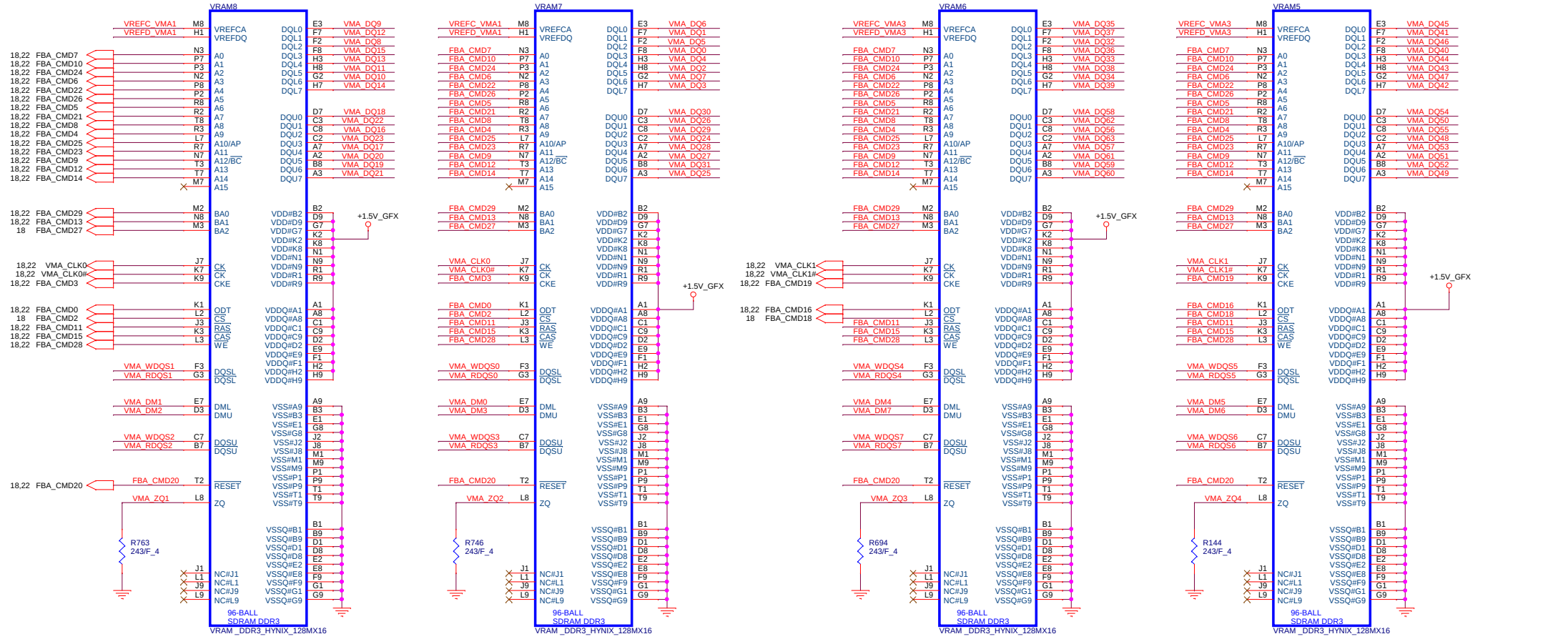
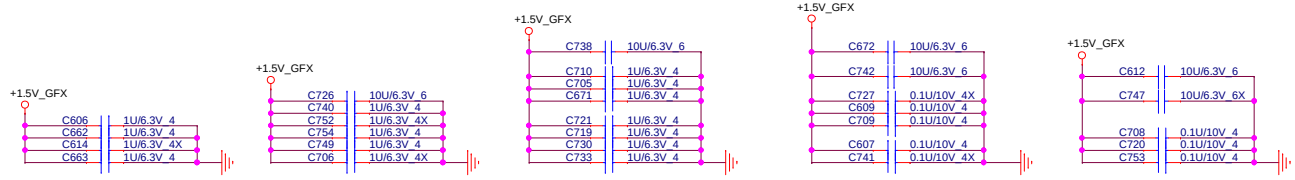
RANK 0

900MHz VRAM size:
Samsung 128Mx16, P/N = AKD5MGWT500
Hynix 128Mx16, P/N = AKD5MGWTW16

18,22 FBA_CMD[0..30]
18,22 VMA_DQ[63..0]
18,22 VMA_DM[7..0]
18,22 VMA_WDQS[7..0]
18,22 VMA_RDQS[7..0]





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	N14P_VRAM RANK0	2A
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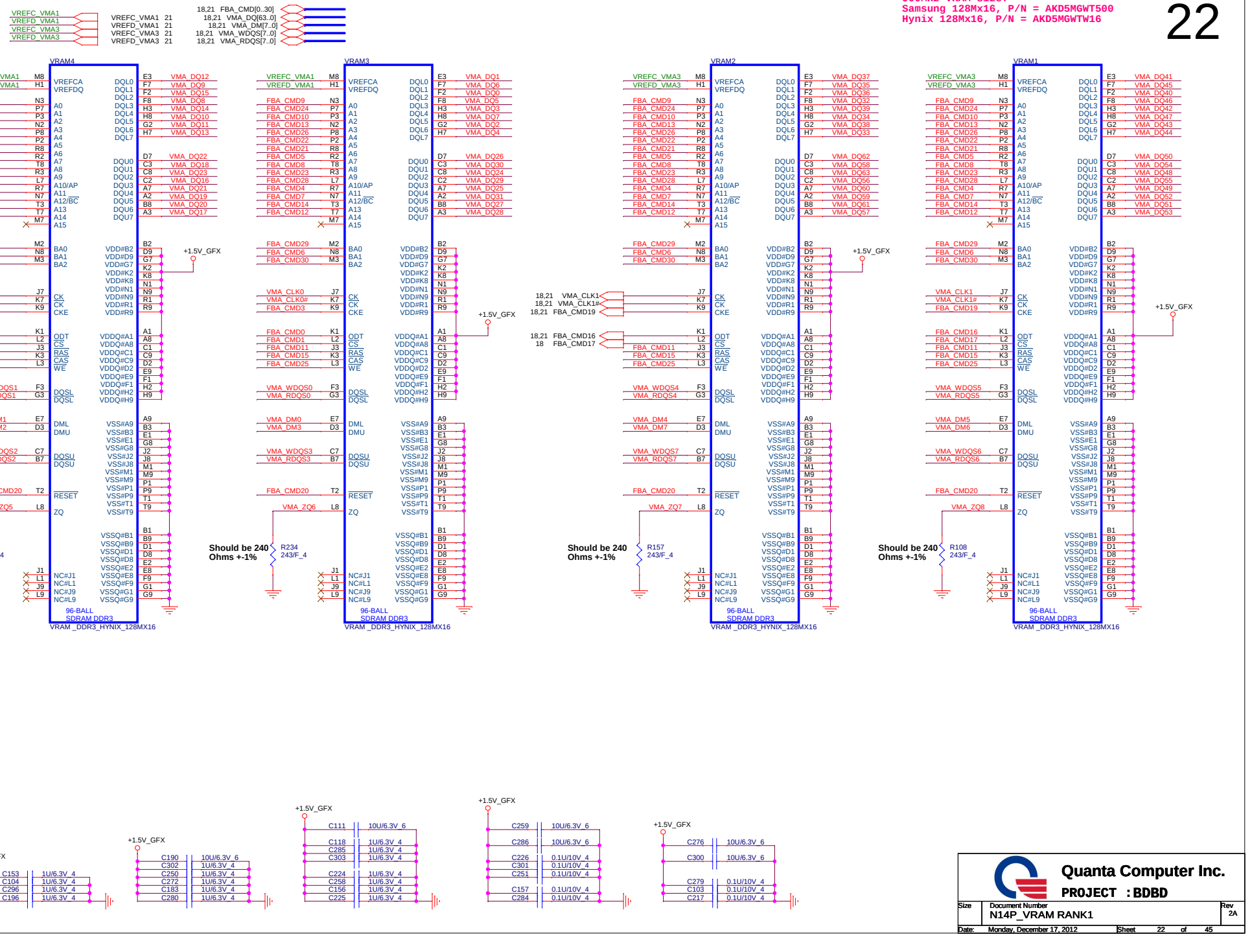
RANK 1

900MHz VRAM size:
Samsung 128Mx16, P/N = AKD5MGWT500
Hynix 128Mx16, P/N = AKD5MGWTW16



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Size	Document Number: N14P_VRAM RANK1 — Rev: 2A
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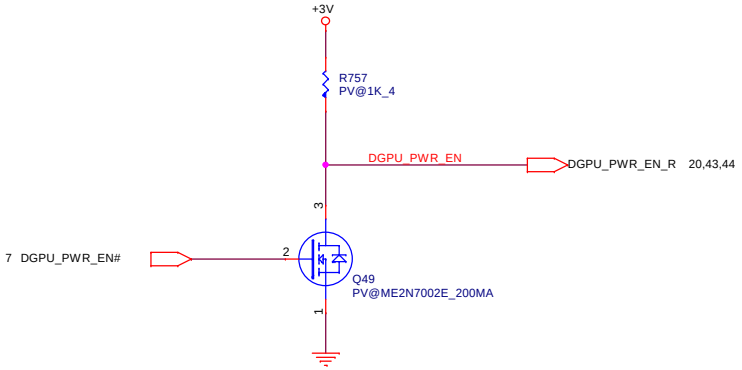

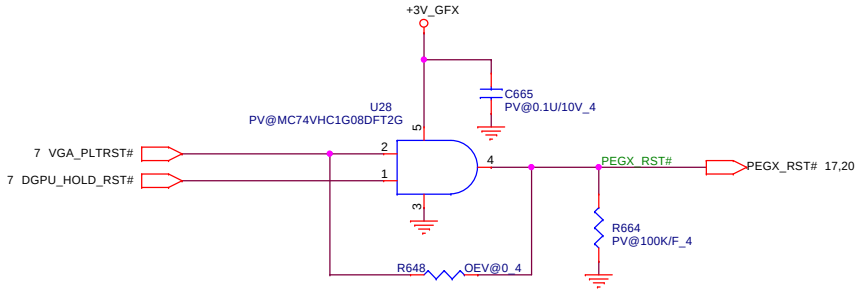

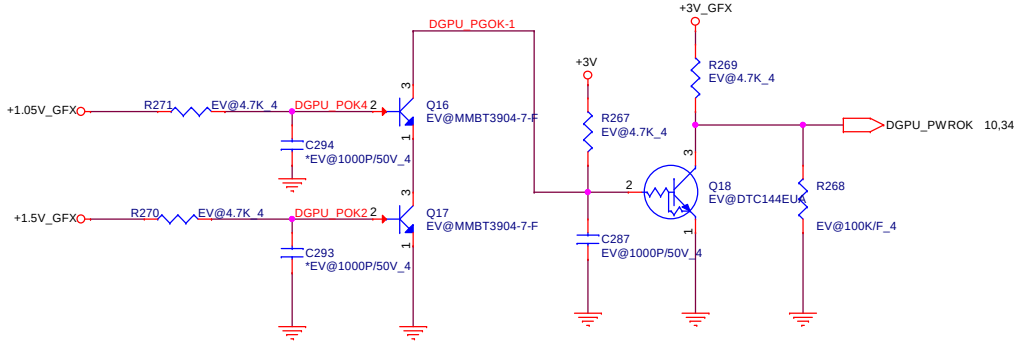

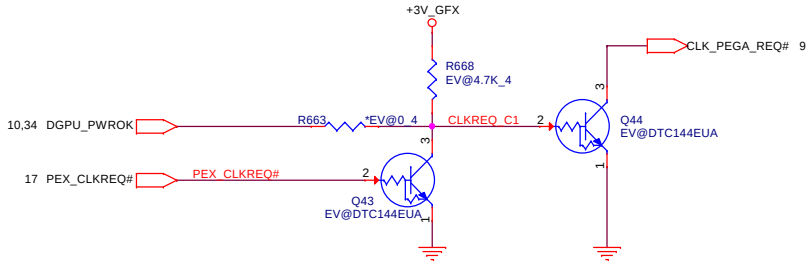

Quanta Computer Inc.

PROJECT : BDBD

Size	Document Number	Rev
	Blank	2A

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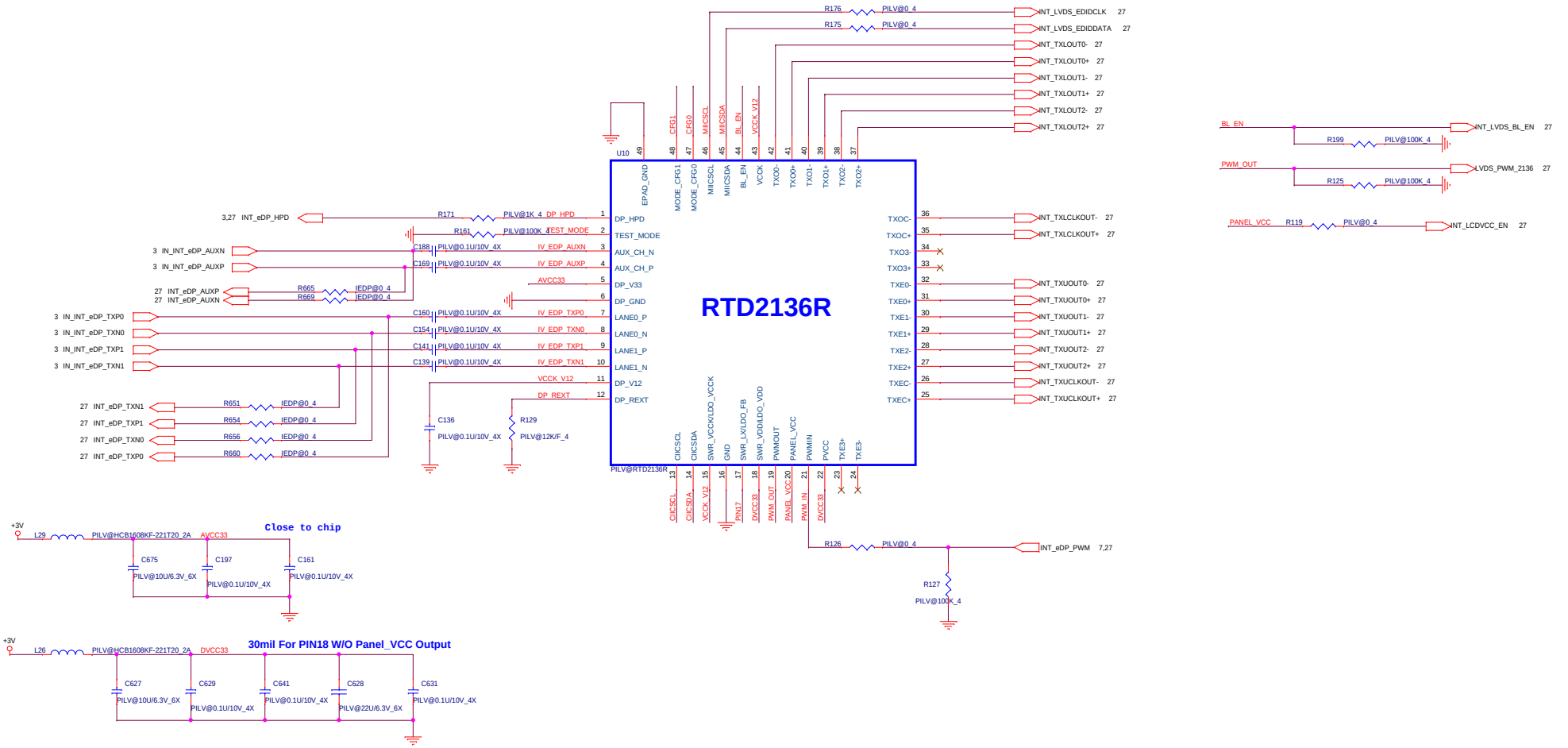
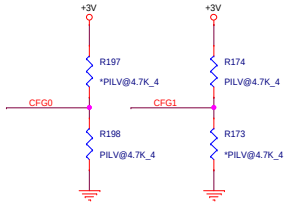


Mode Configure Table(Power On Latch)

		CFG0	
		0	1
CFG1	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

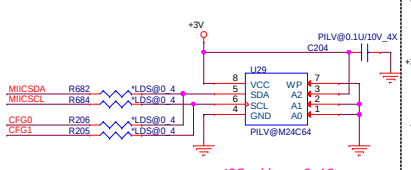
ROM ONLY Mode : CFG0 4.7K pull low, CFG1 4.7K pull high
EP Mode : CFG0 4.7K pull high, CFG1 4.7K pull low
EEPROM Mode : CFG0 4.7K pull high, CFG1 4.7K pull high



EEPROM Mode

In EEPROM mode, an additional EEPROM is needed.
EEPROM should configure with following condition.

1- EEPROM with a size 8K-Byte
2- EEPROM device should be 2-byte addressing device
3- Slave address should configure as 0xA8

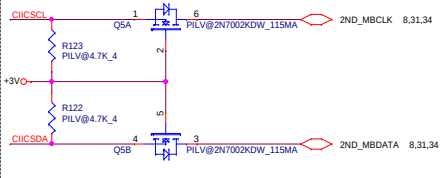


I2C address=0xA8

EP Mode

External device connect to DP2LVDS by
Pin13/Pin14, I2C protocol is used

Address=0x94&0x6A

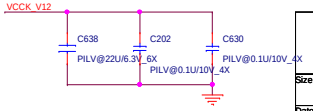


Dual Mode Regulator Configuration

	2.2-uH(L6)	0 Olm(R31)
SWR	Connect	NC
LDO	NC	Connect

SWR MODE

LDO MODE



Quanta Computer Inc.
PROJECT : BDBD

Size	Document Number	Rev
	Thames_M2/ Baco	2A
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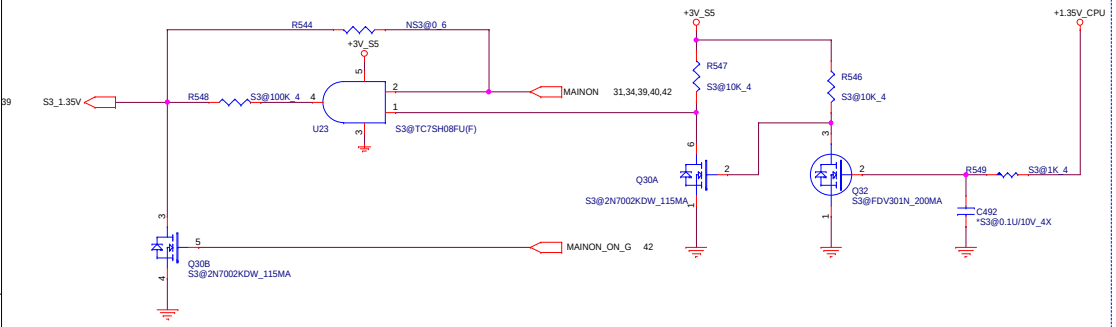
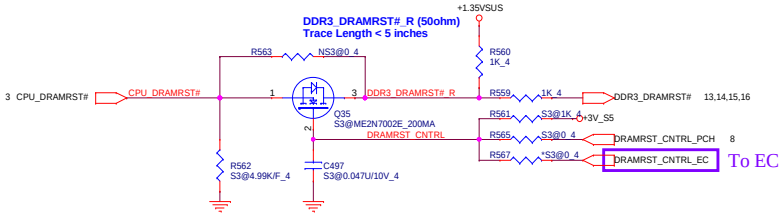
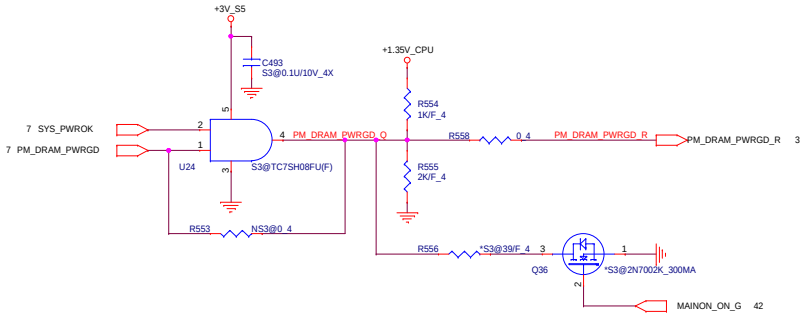
For S3 power Reduction Sequence S3P/NS3P/CPU



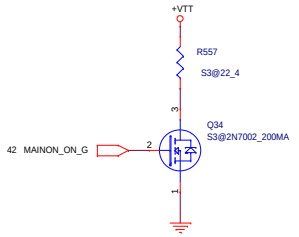
SM_DRAMRST# Topology S3P/NS3P/CPU



S3 power Reduction (SM_DRAMPWROK) S3P/NS3P/CPU

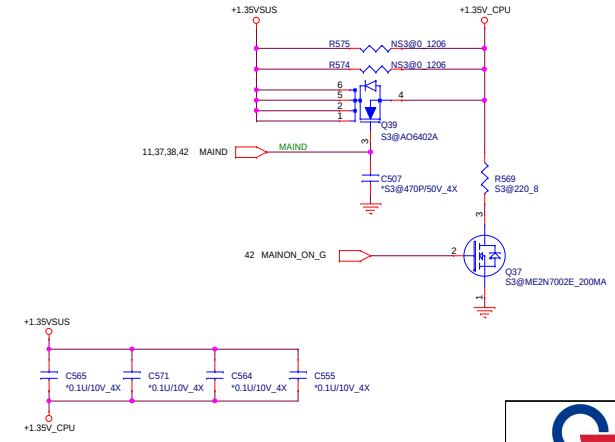


For S3 power Reduction VTT discharge S3P/NS3P/CPU



CPU SM_VREF S3P/NS3P/CPU

S3 power Reduction (CPU Power) S3P/NS3P/CPU



Quanta Computer Inc.
PROJECT : BDBD

Size	Document Number	Rev
	Haswell 3/5 (DDI/eDP)	2A
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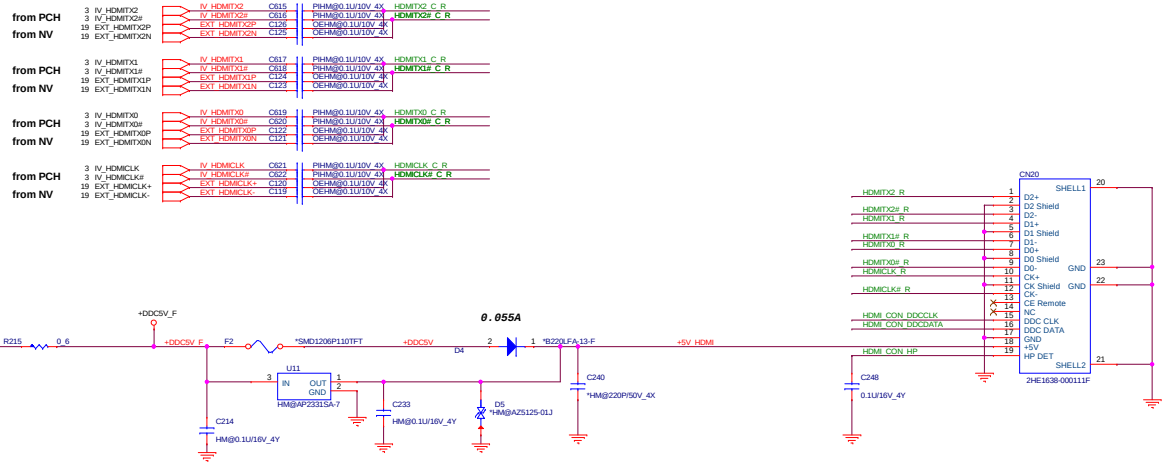
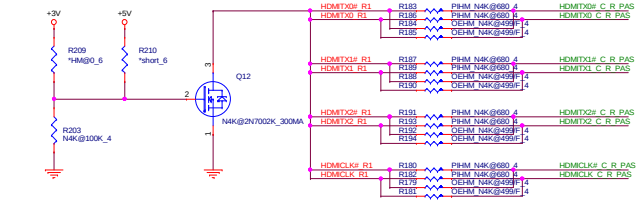
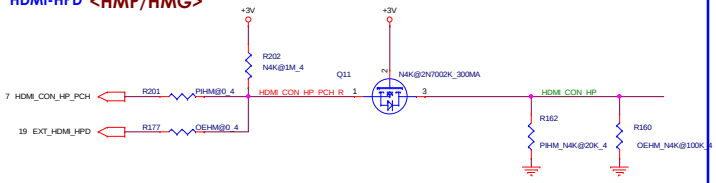
HDMI Conn <HDM>



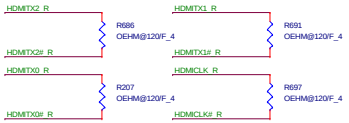
HDMI-passive level shift <HMP/HMG>



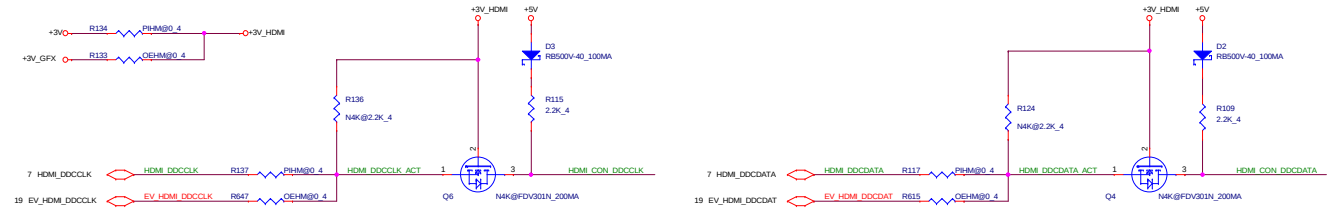
HDMI-HPD <HMP/HMG>

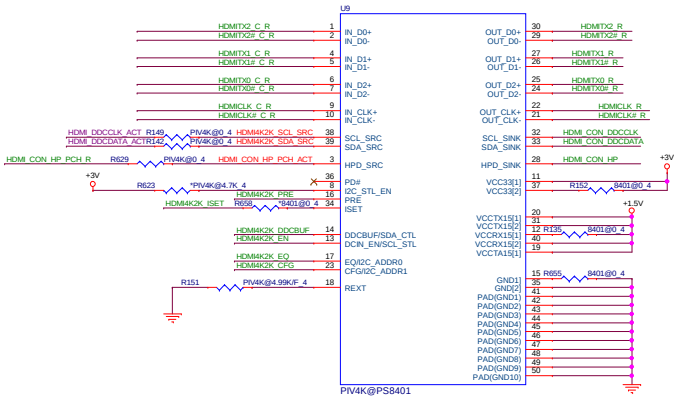


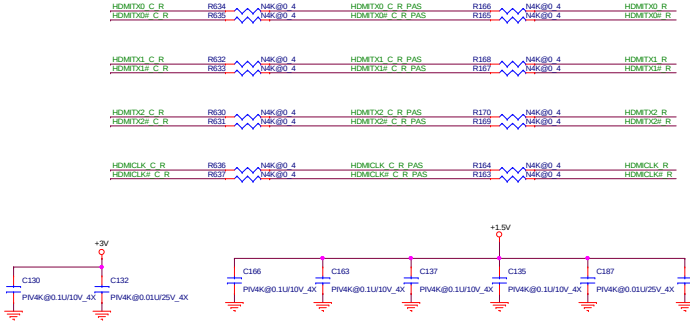
FOR EMI <EMC>

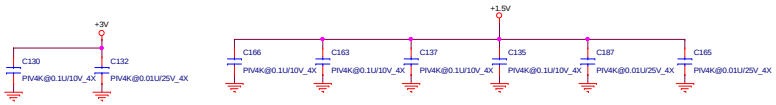


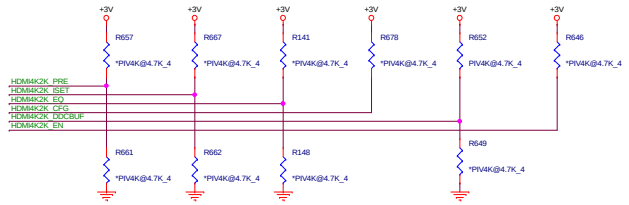
HDMI-SMBus <HDM>











	Pre	ISET	EQ	CFG	DDCBUF	DCIN_EN
NC(Low)	0 dB	default	12.4 dB	HDMI ID disable	default	default,AC coupling input
1(High)	1.6 dB	+13%	4.3 dB	HDMI ID enable	active DDC buffer with default threshold	DC coupling input
M	2.5 dB	-13%	8.6 dB	N/A	active DDC buffer without internal pull up resistor	N/A

Pre	Output pre-emphasis setting
ISET	TMDS output swing adjustment
EQ	Receiver equalization setting
CFG	Configuration pin
DDCBUF	enable active DDC buffer
DCIN_EN	DC coupling enable

Pin	PS8401A	PS8201A
12	VDDRX	NC
15	GND	NC
34	ISET	NC
37	VDD33	NC

Quanta Computer Inc.
PROJECT : BDBD
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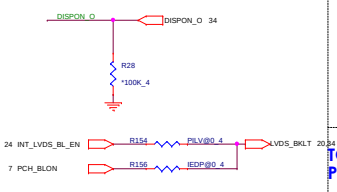
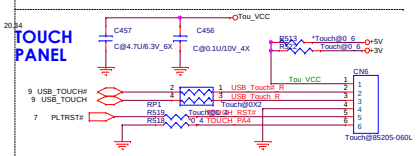
Panel backlight control LDS



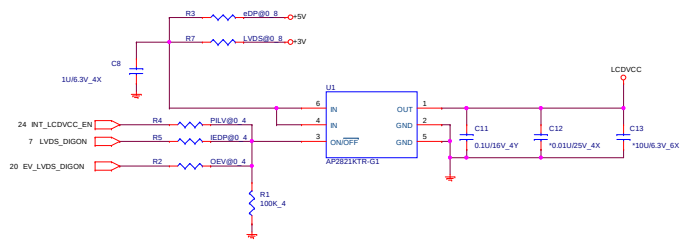
TOUCH PANEL



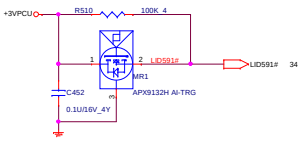
LCD POWER SWITCH

INT_LVDS PWR

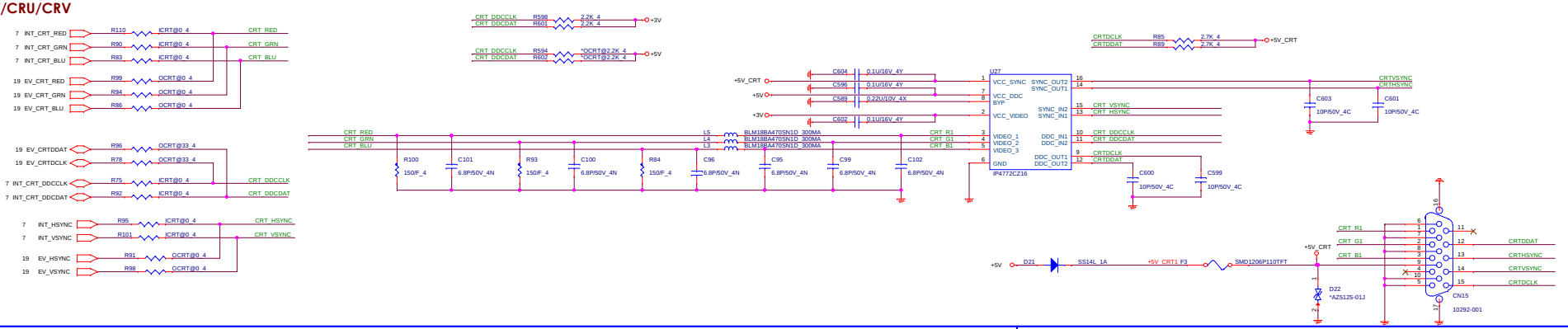
80 mil



HALL Sensor HSR

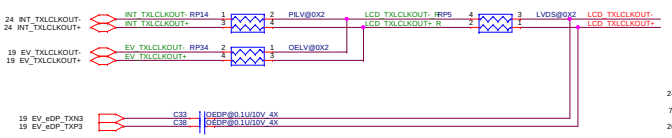


CRT CRT/CRU/CRV

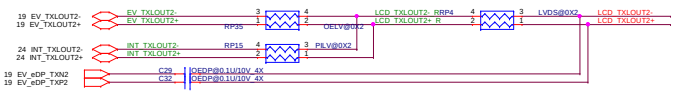


LCD Panel Module <LDS>

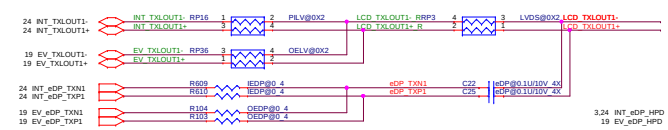
Lane 3



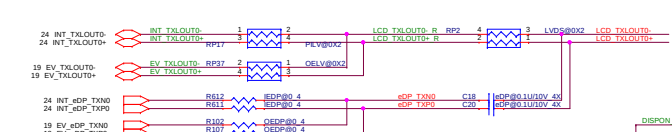
Lane 2



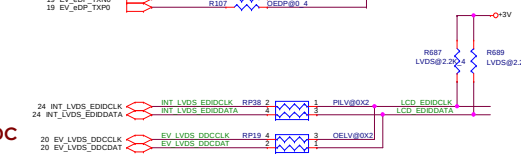
Lane 1

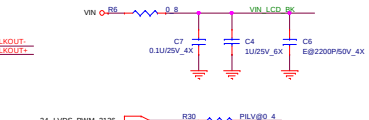


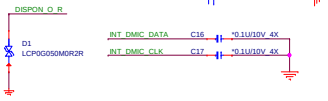
Lane 0

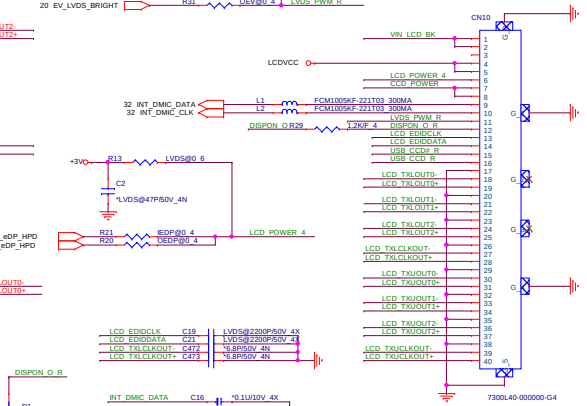


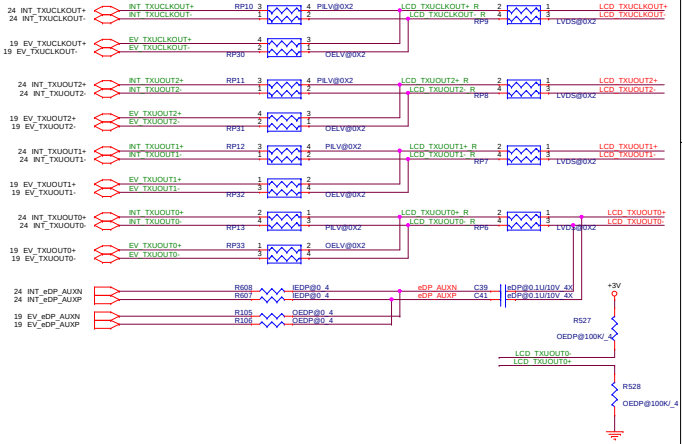
EDID DDC



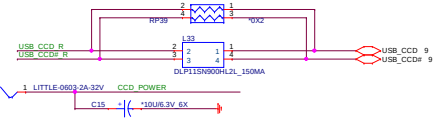








CCD



Quanta Computer Inc.
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	LCD/LED Panel/CCD	2A
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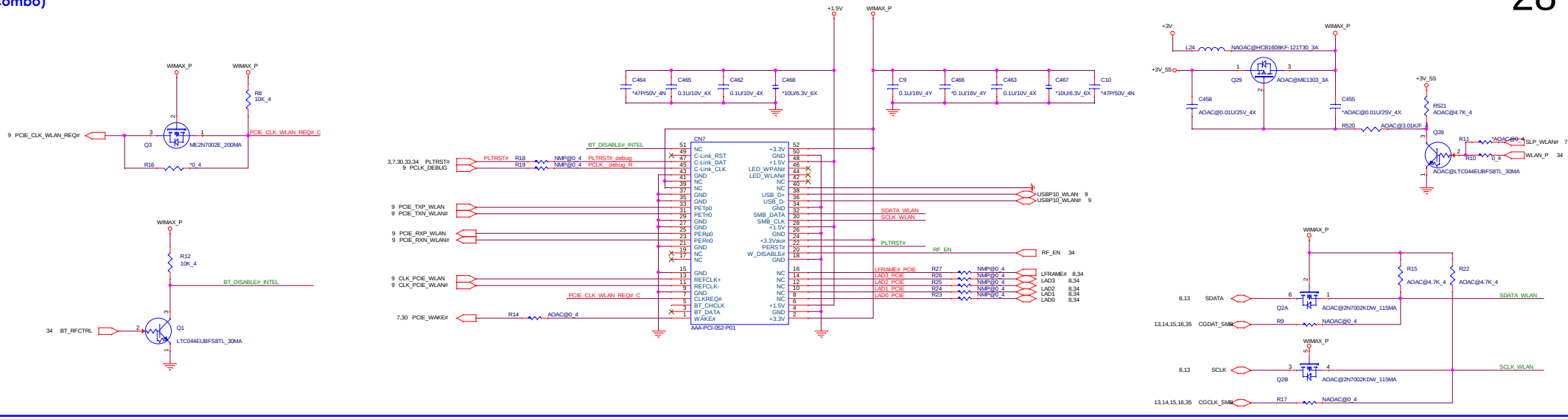
MINI Card Slot#1(WiFi / Wimax / Combo)

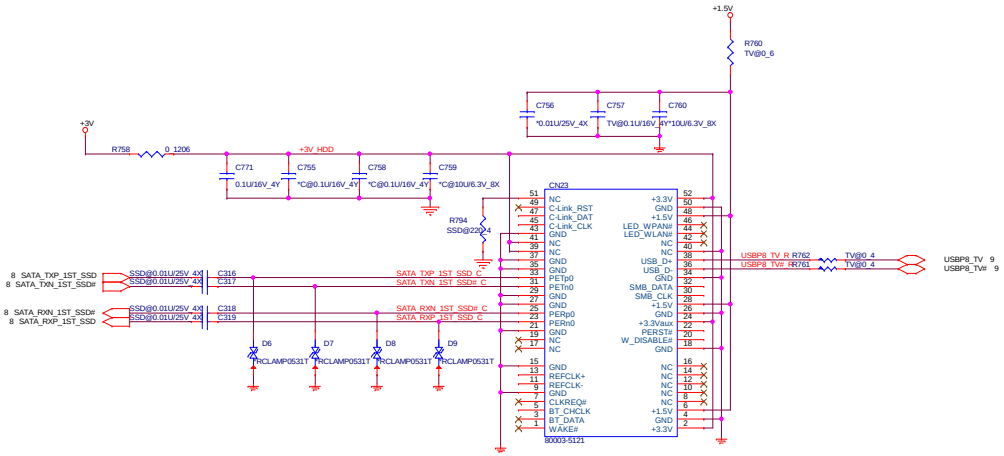
MNW/DEG



TV Tuner / MSATA

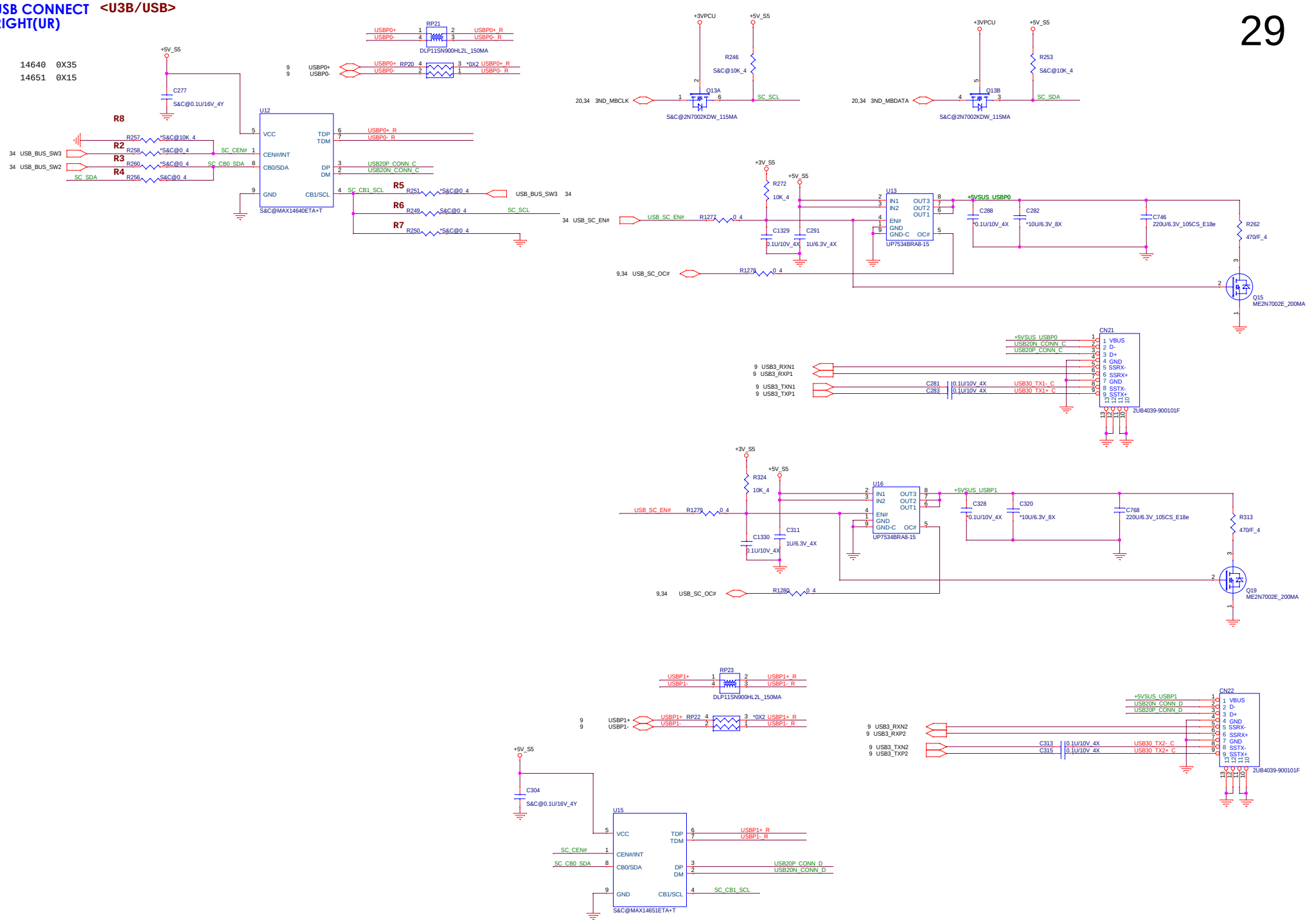
<SSD>

TV Tuner: 1.5V@240mA 3.3V@470mA



USB CONNECT RIGHT(UR) <U3B/USB>

14640 0X35
14651 0X15



Quanta Computer Inc.		
PROJECT : BDBD		
Size	Document Number: USB3 Redriver/S&C(Right side)	Rev 2A
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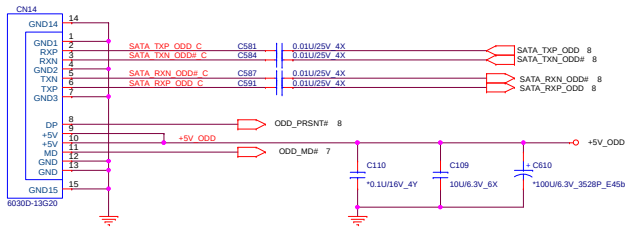
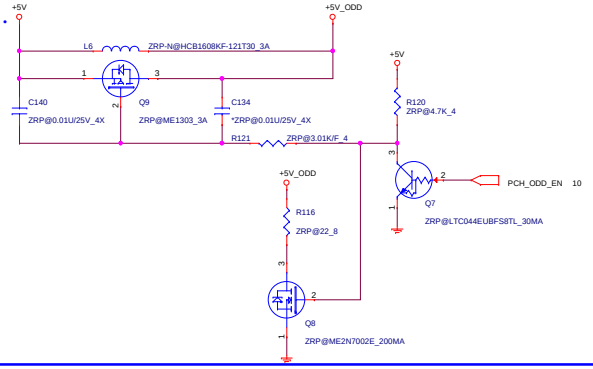
SATA ODD

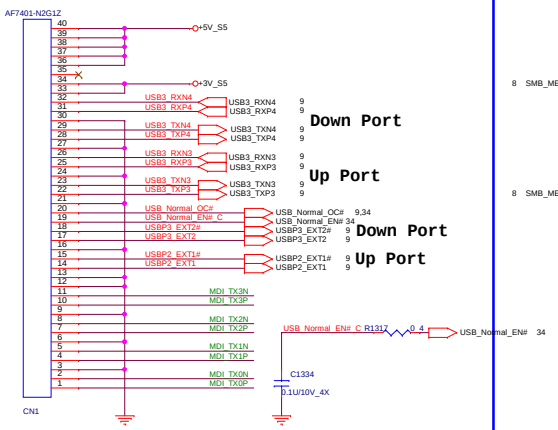


ODD Zero power . (Only for Intel)

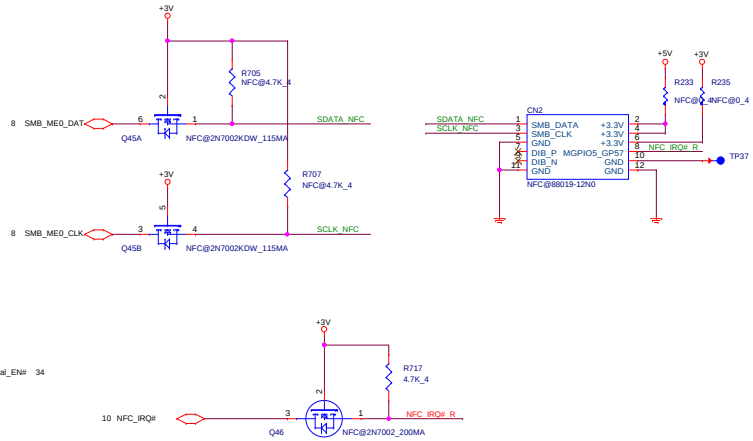


Atheros Lan/USB3 CONN

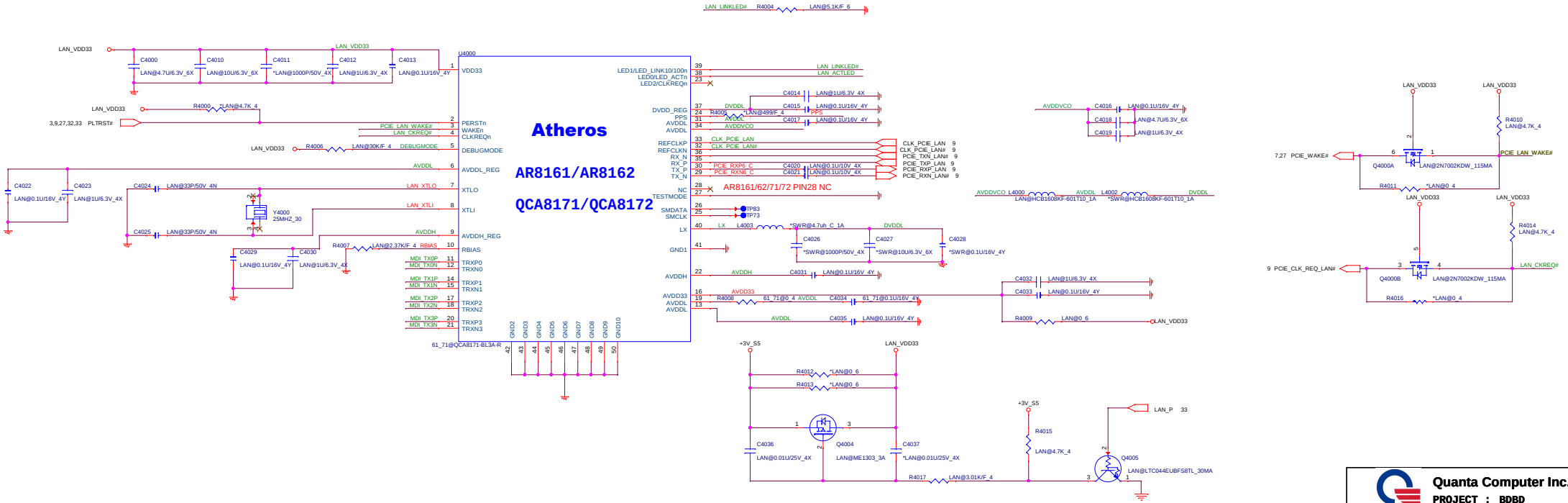
<LAN/LN1.LNG>



NFC Connector



Atheros AR8161/AR8162 QCA8171/QCA8172



Quanta Computer Inc.			
PROJECT : BDBD			
Size	Document Number		Rev
	USB3 Redriver/USB2_Left		2A
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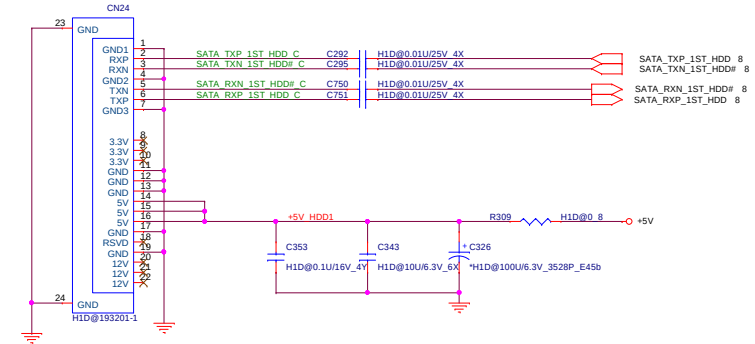
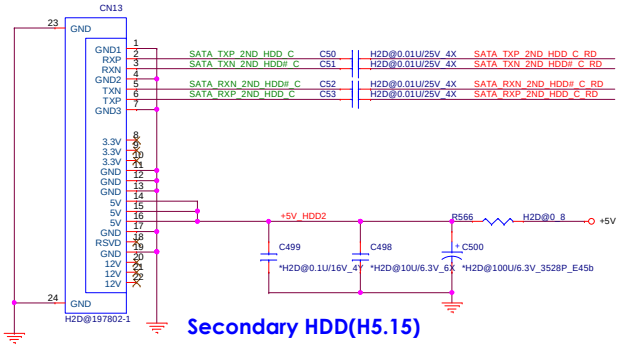
SATA HDD1



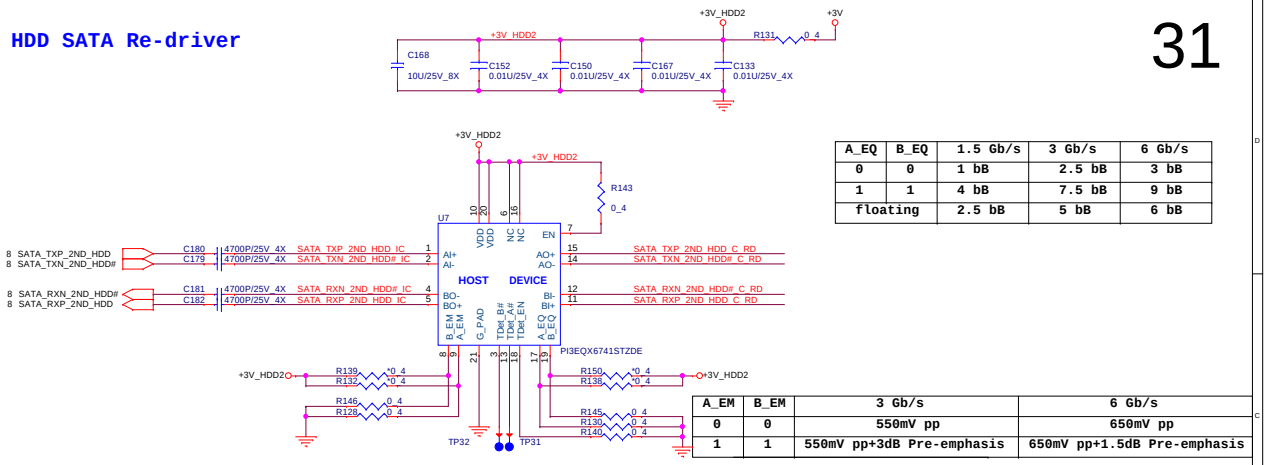
Primary HDD(H2.75)

SATA HDD2



Secondary HDD(H5.15)

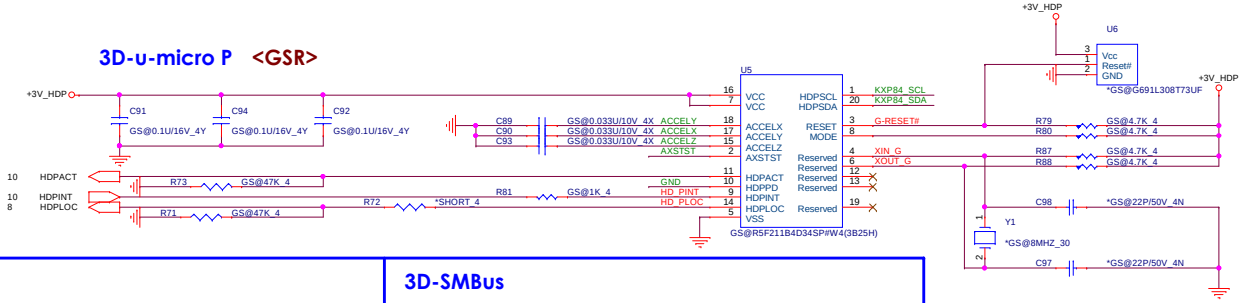
2nd HDD SATA Re-driver



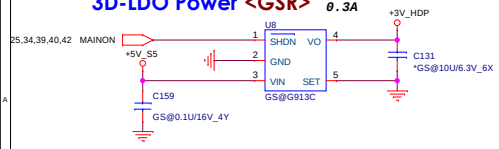
A_EQ	B_EQ	1.5 Gb/s	3 Gb/s	6 Gb/s
0	0	1 bB	2.5 bB	3 bB
1	1	4 bB	7.5 bB	9 bB
floating		2.5 bB	5 bB	6 bB

A_EM	B_EM	3 Gb/s	6 Gb/s
0	0	550mV pp	650mV pp
1	1	550mV pp+3dB Pre-emphasis	650mV pp+1.5dB Pre-emphasis

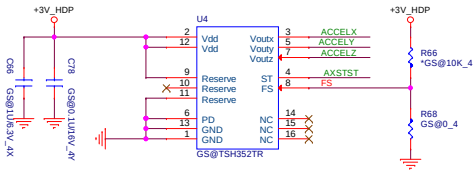
3D-u-micro P <GSR>



3D-LDO Power <GSR> 0.3A



3D-Sensor IC <GSR>



FS (Full Scale) selection

FS	0	1
	2g Full-Scale	6g Full-Scale

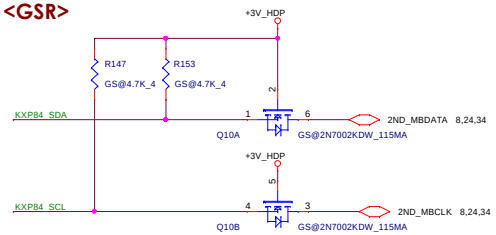
PD (Power Down) selection

PD	0	1
	Normal Mode	Power-down mode

HDPPD selection

HDPPD	0	1
	Normal Mode	Power-down mode

3D-SMBus <GSR>



Quanta Computer Inc.

PROJECT : BDBD

Size	Document Number	Rev
	HDD/ODD	2A

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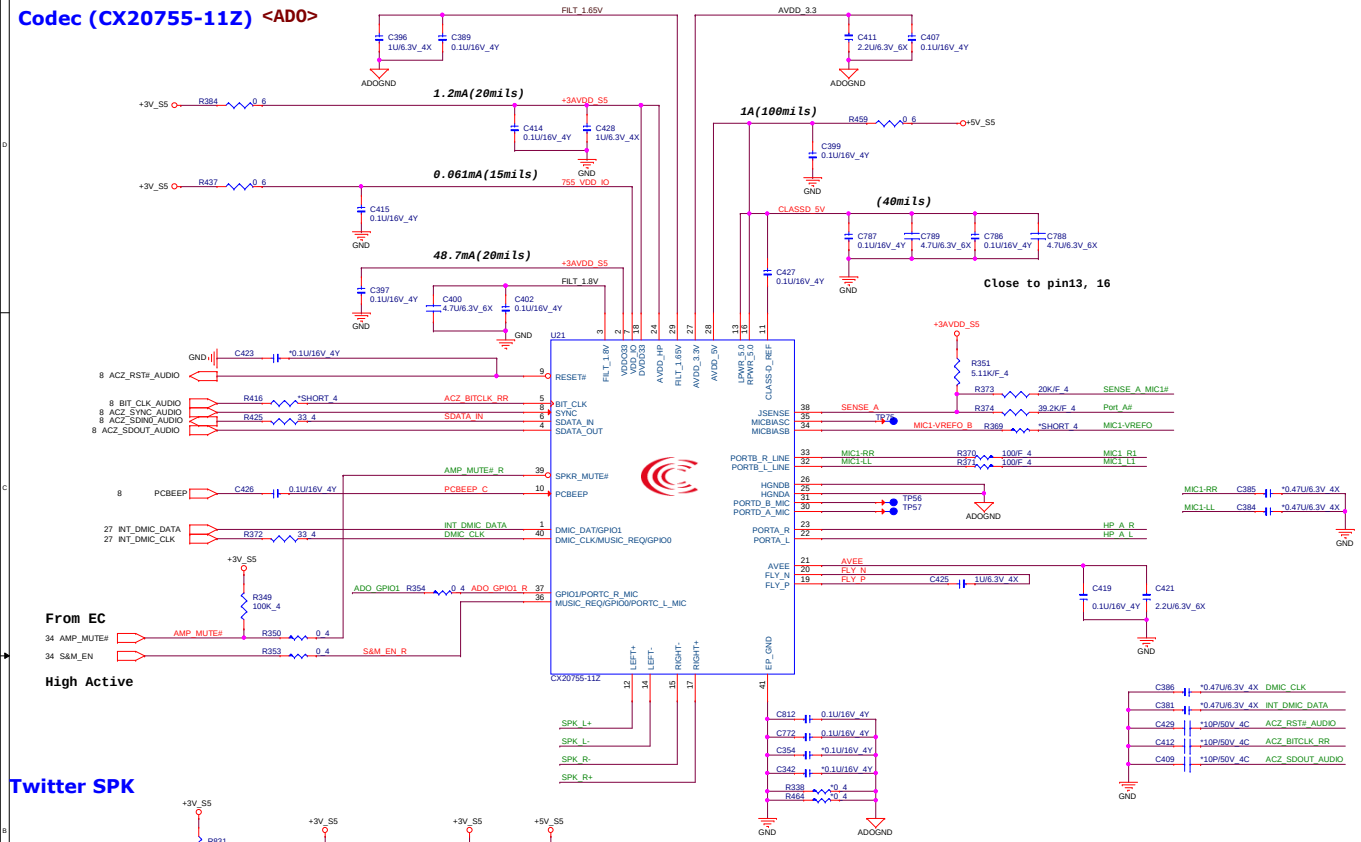
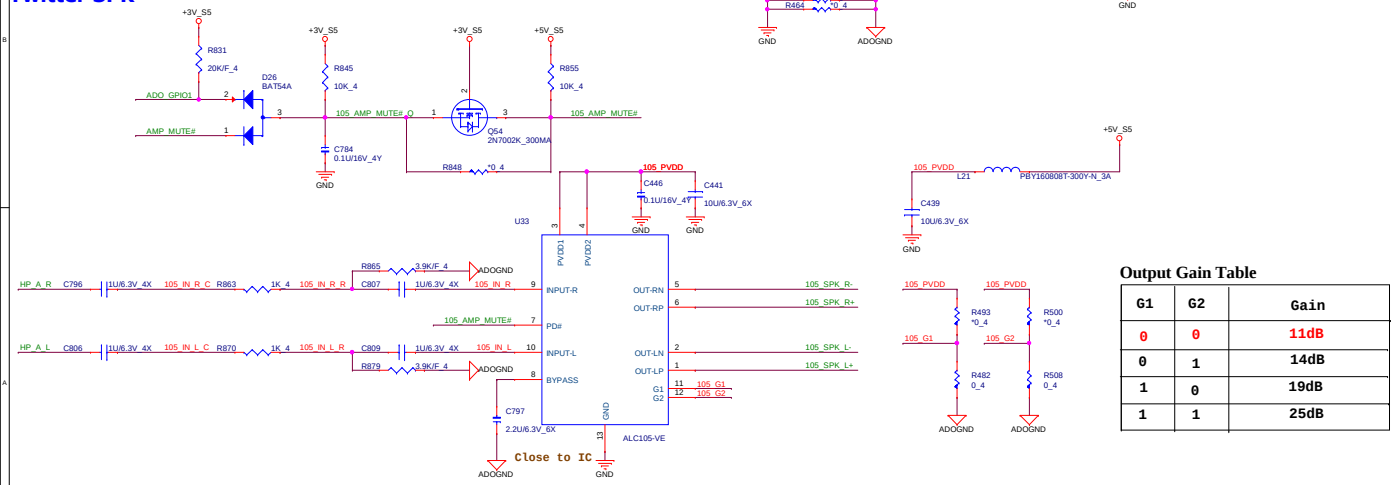
Codec (CX20755-11Z) <ADO>



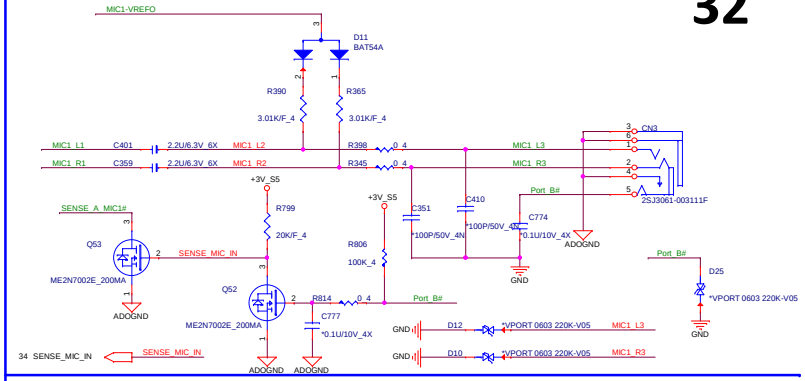
Twitter SPK



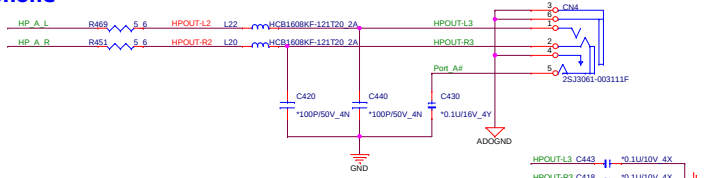
Output Gain Table

G1	G2	Gain
0	0	11dB
0	1	14dB
1	0	19dB
1	1	25dB

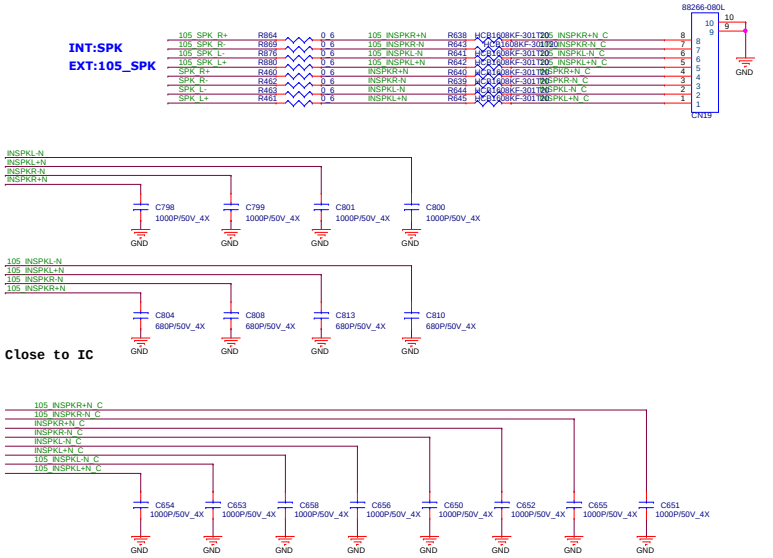
External MIC



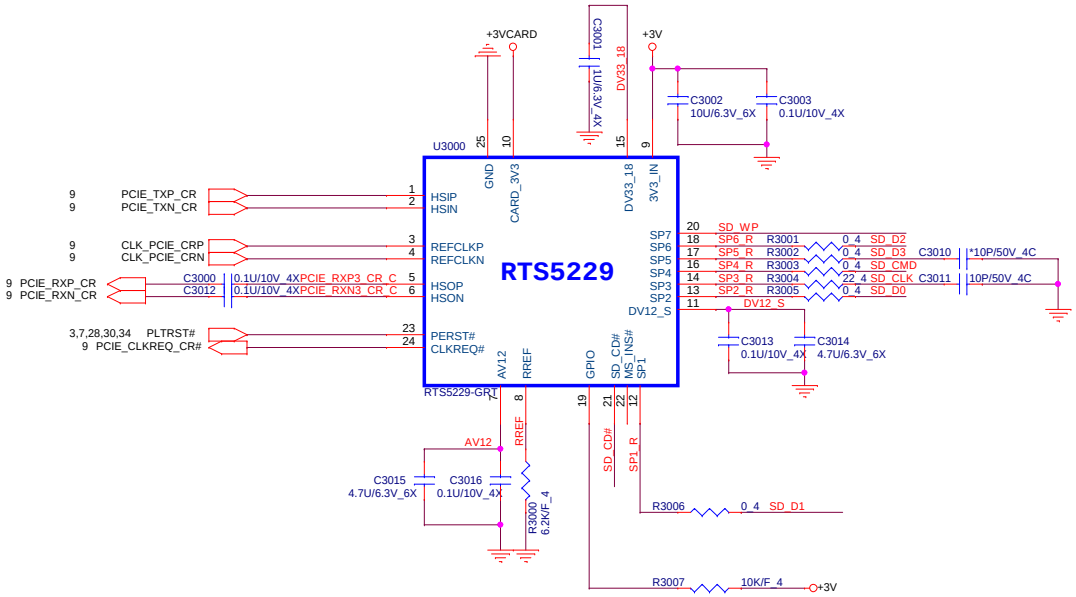
Headphone <ADO>

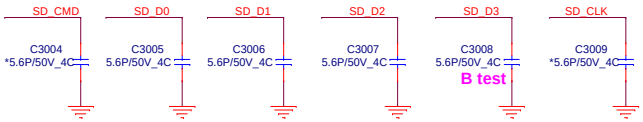


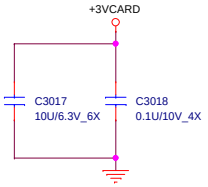
4 Speakers <ADO>



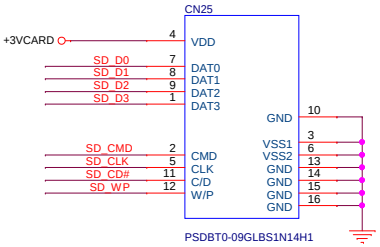
Quanta Computer Inc.	PROJECT : BDBD
Size	Document Number: Audio Codec (CX20755)
Rev	2A
Date: Monday, December 17, 2012	Sheet 32 of 45







SD / MMC CARD READER



Quanta Computer Inc.

PROJECT : BDBD

Size	Document Number	Rev
	Card Reader(AU6437)	2A

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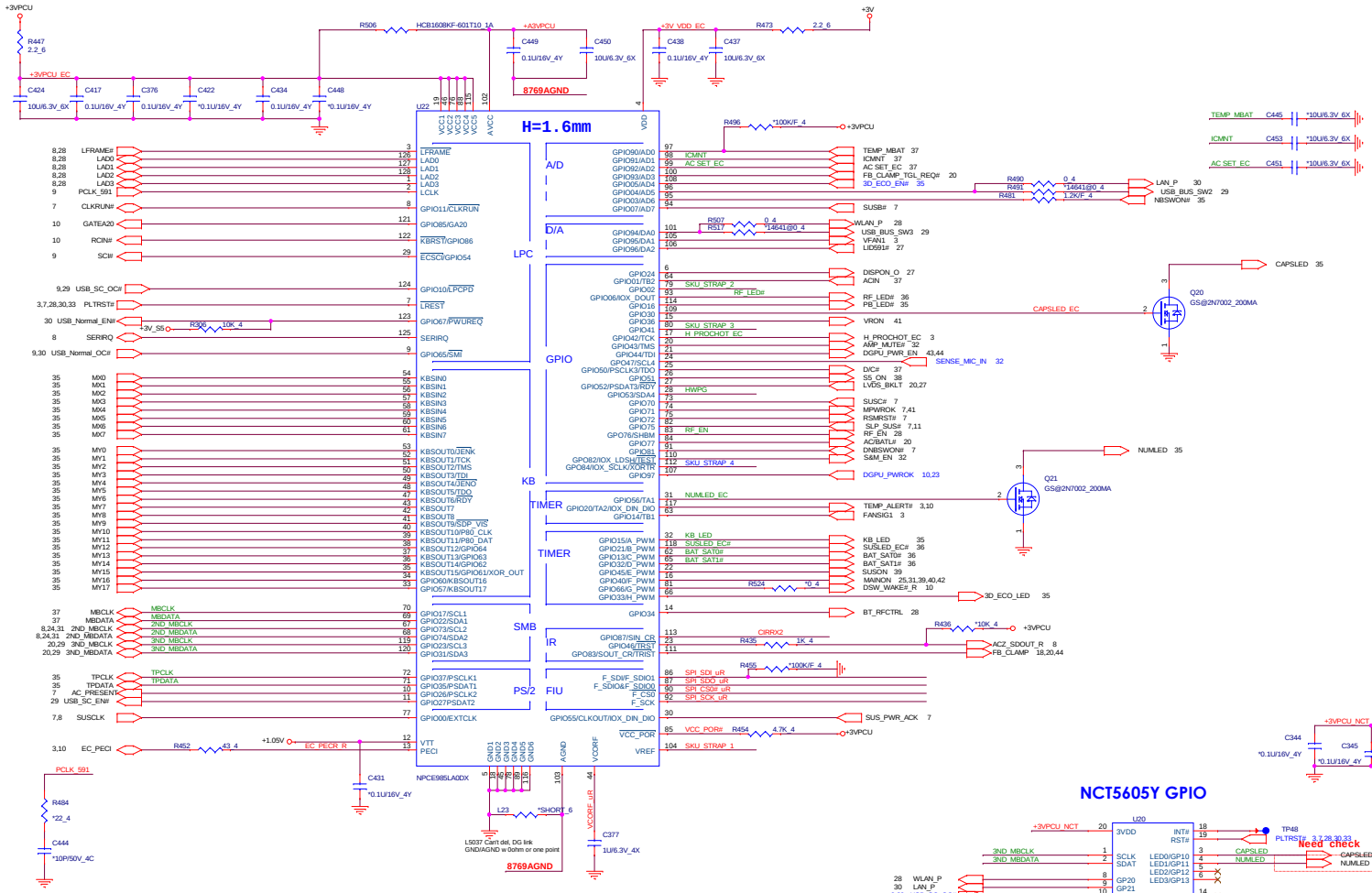
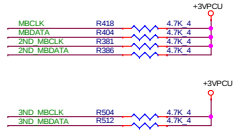
EC<KBC>



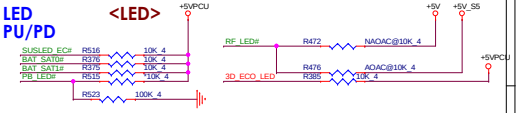
SM BUS PU/Address <KBC>



SMBUS	Devices	Address
1	Battery(A)	
2	PCH(S5)	
	G-sensor(S0)	
	IDROM(A)	
	EDP2LVDS IC	94H or 6AH
3	VGA Thermal(A or S0)	98H
	Extend GPIO	
	S&C IC 14640 Up Port	35H
	S&C IC 14651 Down Port	15H

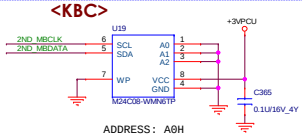
TP <KBC>

LED PU/PD <LED>

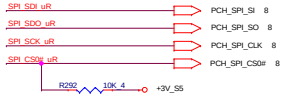


INTERNAL KEYBOARD STRIP SET <KBC>

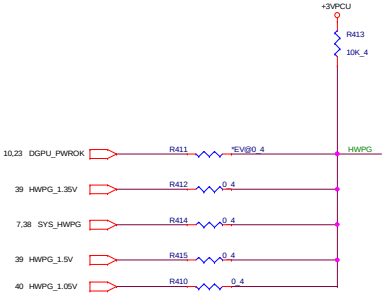
ID EEPROM <KBC>



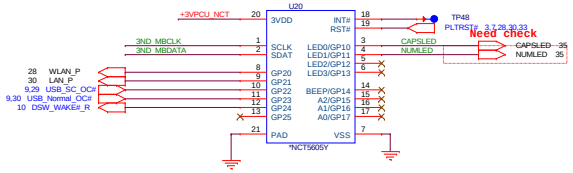
SPI FLASH <KBC>



HWPG circuit <KBC>

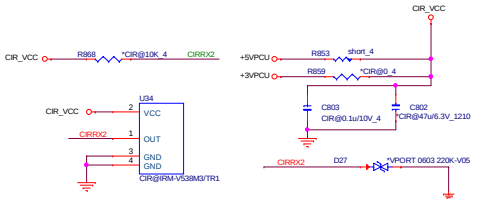


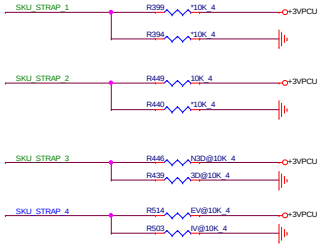
NCT5605Y GPIO



Power Button <KBC>

CIR





MS Strap	SKU_STRAP_1	SKU_STRAP_2	SKU_STRAP_3	SKU_STRAP_4
17"P	0			
17"G	1			
Chief River		0		
Shark Bay		1		
W/ 3D			0	
W/O 3D			1	
UMA				0
Discrete(Optmius)				1

Quanta Computer Inc.
PROJECT : BDBD

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	EC-NPCE885L	2A
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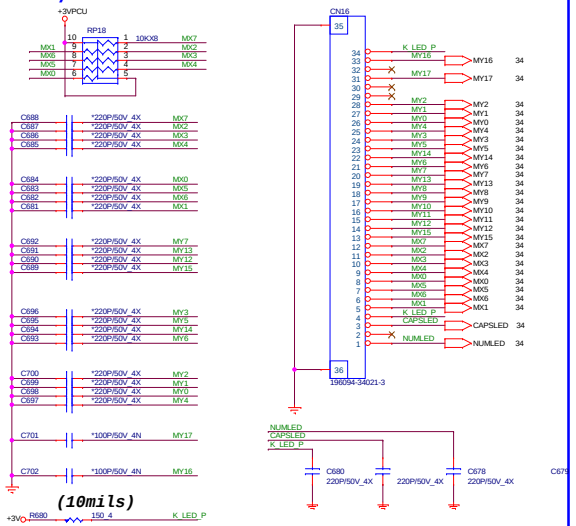
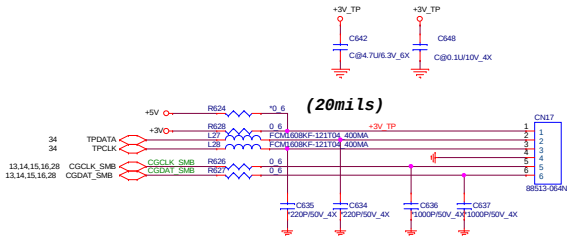
INT KeyBoard <KBC>



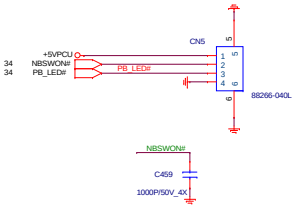
TP board <TPD>

Touch Pad Connector <TPD> <EMI>



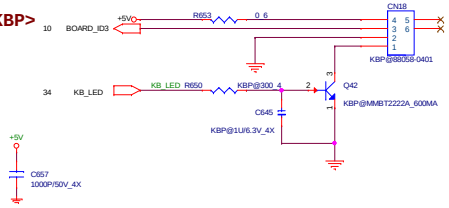
Power board w LED <PSW>

Power Botton Connector <PSW>

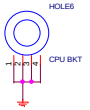


K/B LED power

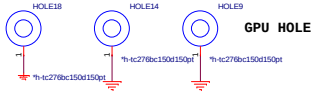
<KBP>



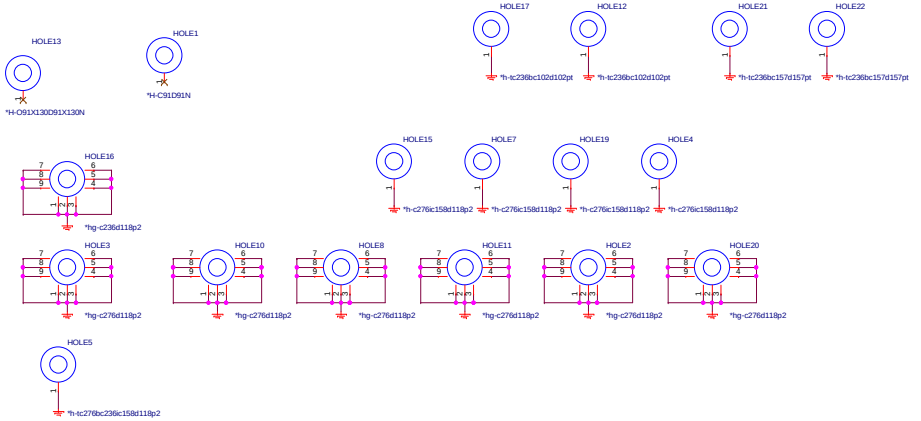
CPU BKT INTEL-CPU-BKT2



GPU



HOLE



Quanta Computer Inc.

PROJECT : BDBD

Size	Document Number	Rev
	KB/TP&TP/PB/FL/LEB/MMB/B-CAS	2A

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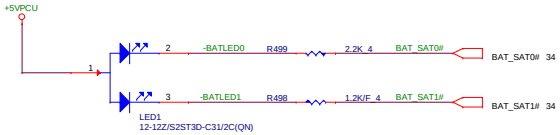
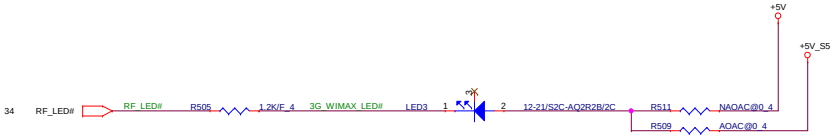
LED

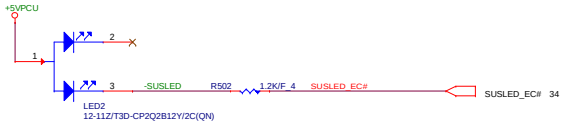
BATERRY



RF LED LED

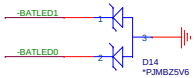


POWER LED

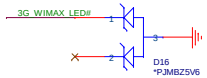


ESD Protect LED

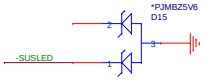
FOR BATTERY LED



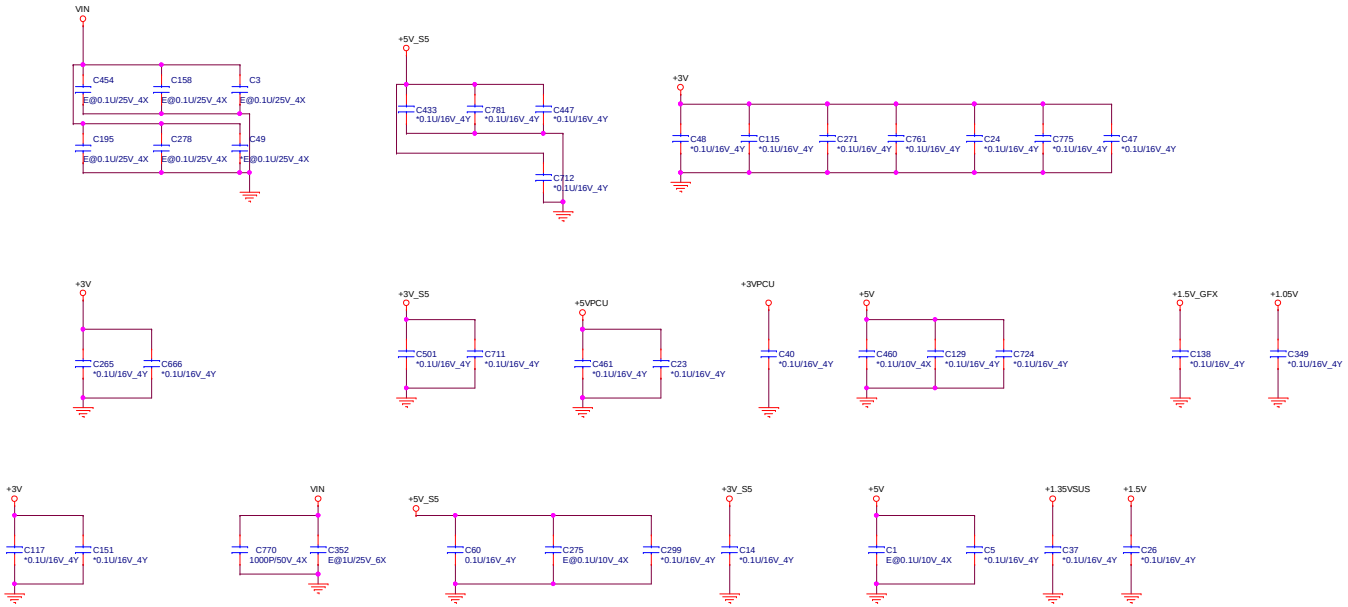
FOR W-LAN LED



FOR Power LED



EMI



Quanta Computer Inc.

PROJECT : BDBD

Size	Document Number	Rev
	LED/EMI/Green CLK	2A

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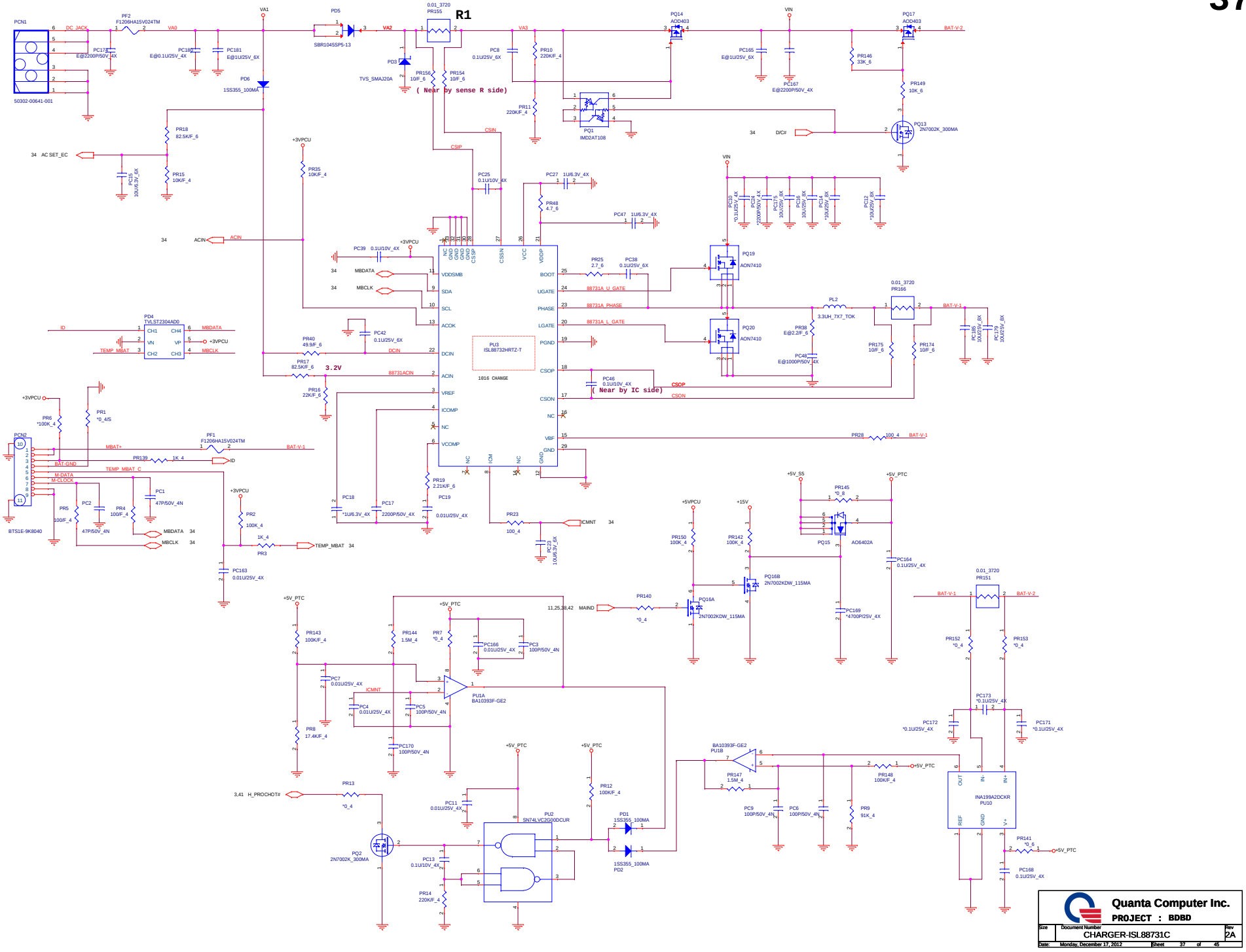
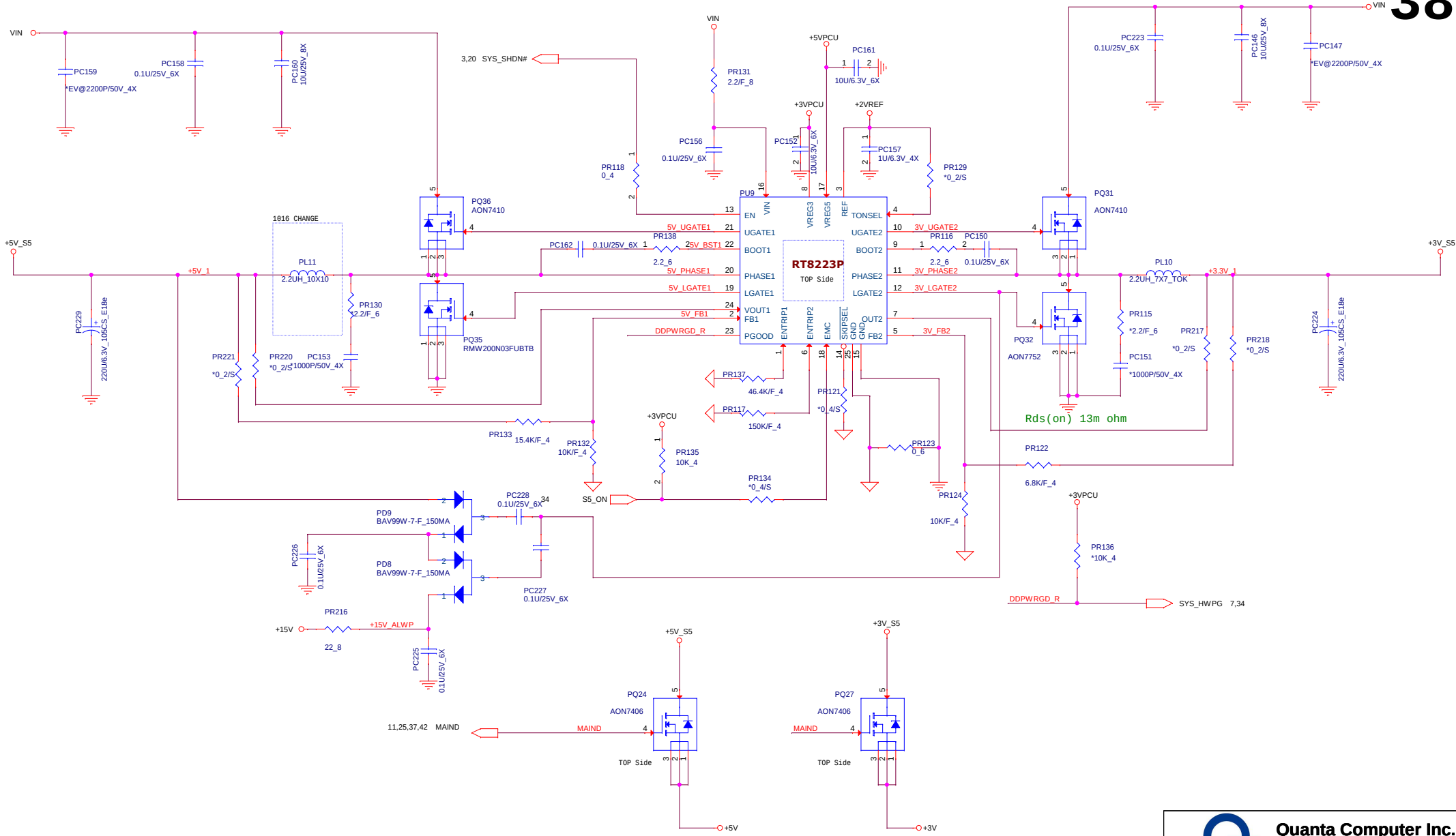
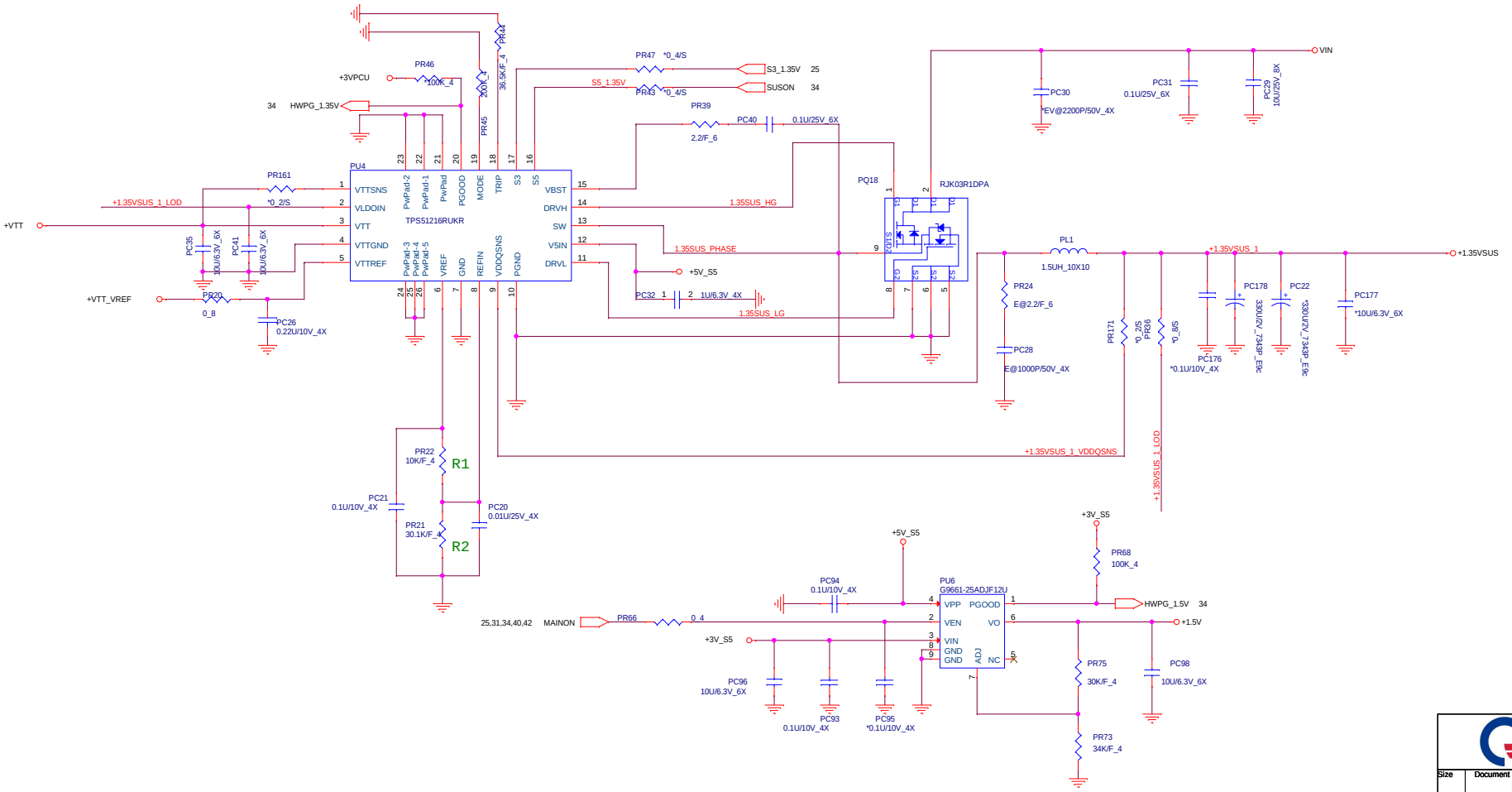


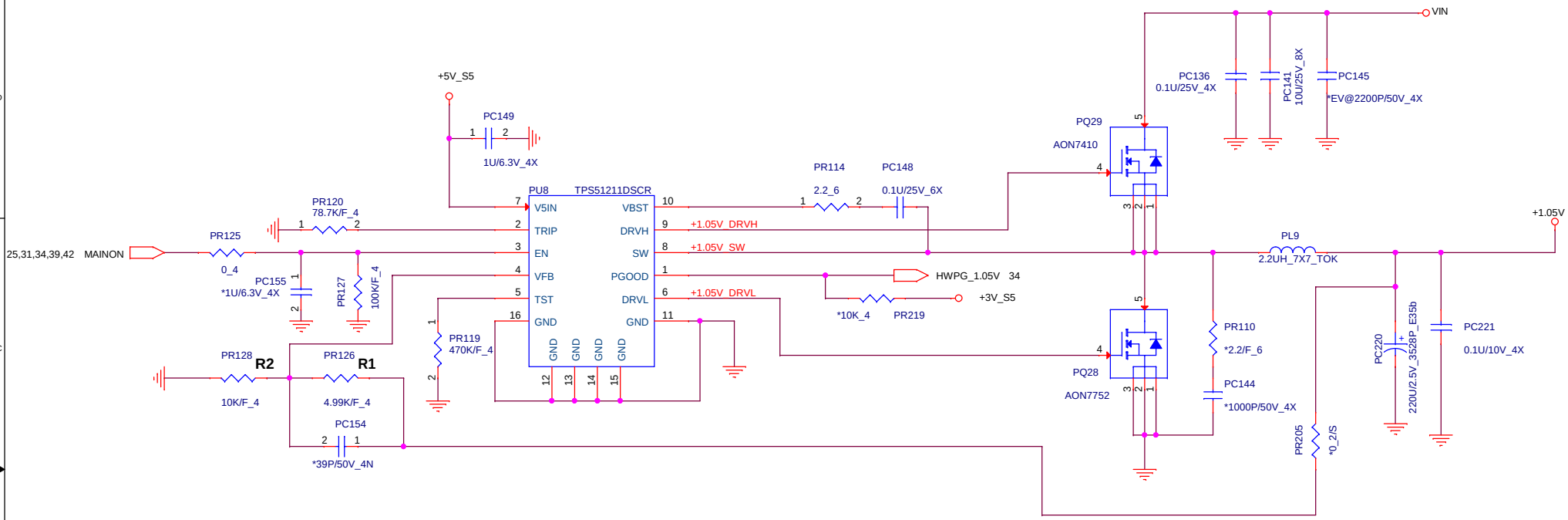
Quanta Computer Inc.			
PROJECT : BDBD			
Size	Document Number		Rev
	CHARGER-ISL88731C		2A
Date: Monday, December 17, 2012		Sheet 37 of 45	



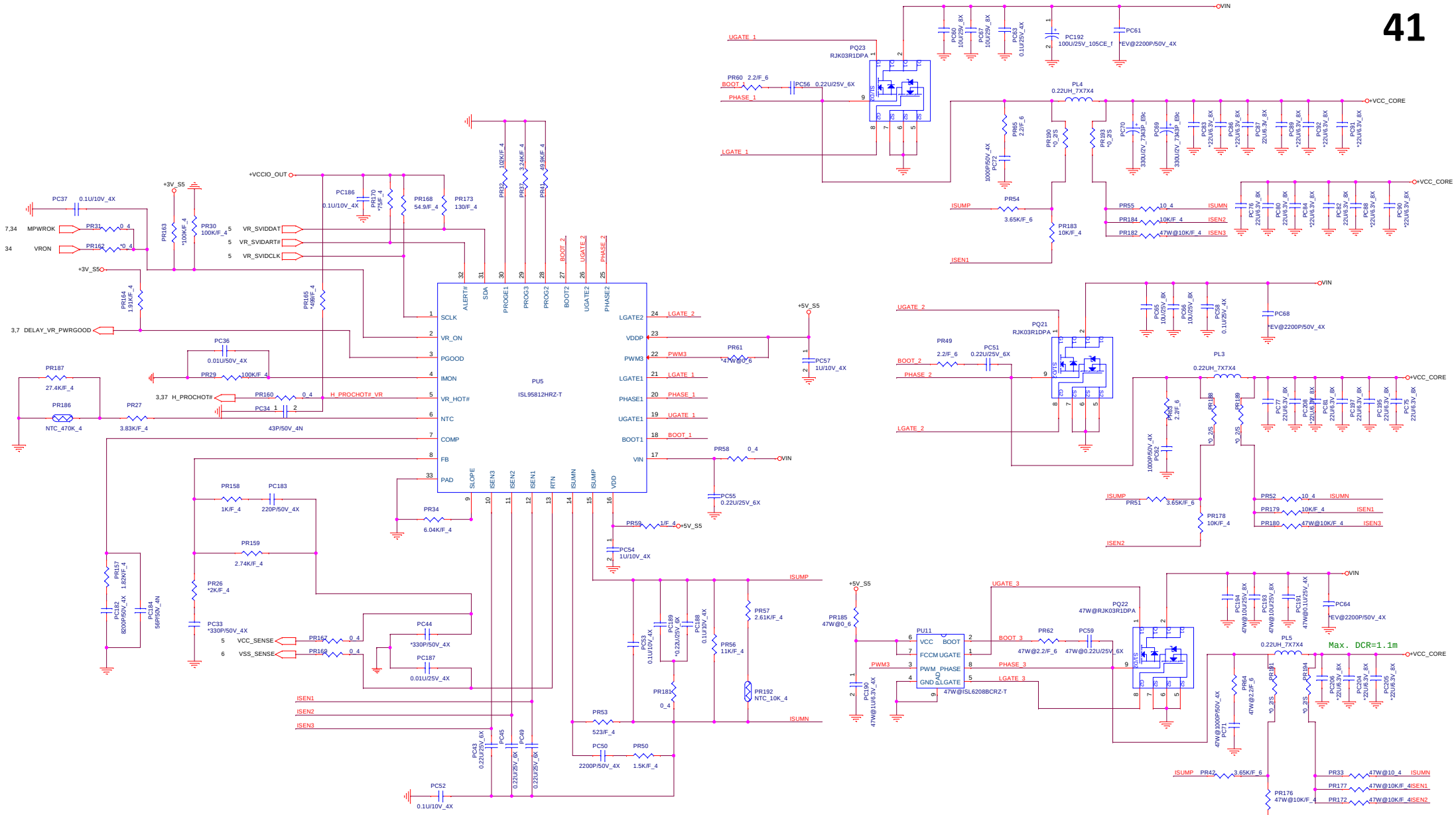
Quanta Computer Inc.		
PROJECT : BDBD		
Size	Document Number: System 3V/5V(TPS51123A)	Rev: 2A
Date: Monday, December 17, 2012	Sheet 38 of 45	



Quanta Computer Inc.		
PROJECT : BDBD		
Size	Document Number: DDR1.5V	Rev: 2A
Date: Monday, December 17, 2012	Sheet 39 of 45	



Quanta Computer Inc.		
PROJECT : BDBD		
Size	Document Number: +1.05V_A(TPS51211DSCR)	Rev: 2A
Date: Monday, December 17, 2012	Sheet 40 of 45	



Quanta Computer Inc.		
PROJECT : BDBD		
Size	Document Number	Rev
	+VCCIN (ISL95812) 47/57W	2A
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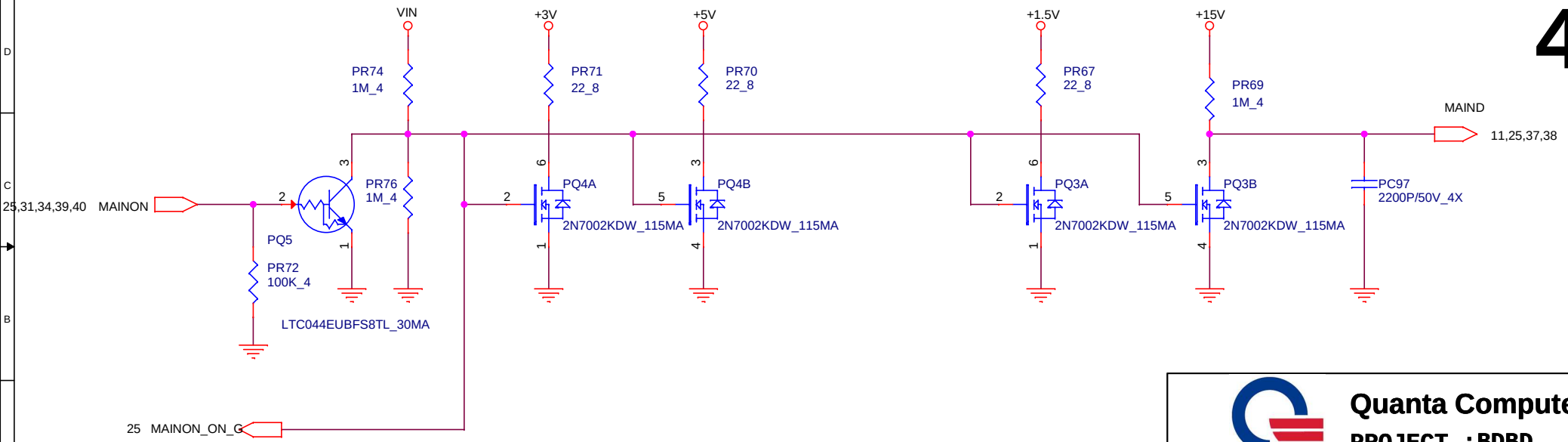

Quanta Computer Inc.

PROJECT : BDBD

Size	Document Number	Rev
	+1.8V/Discharge	2A

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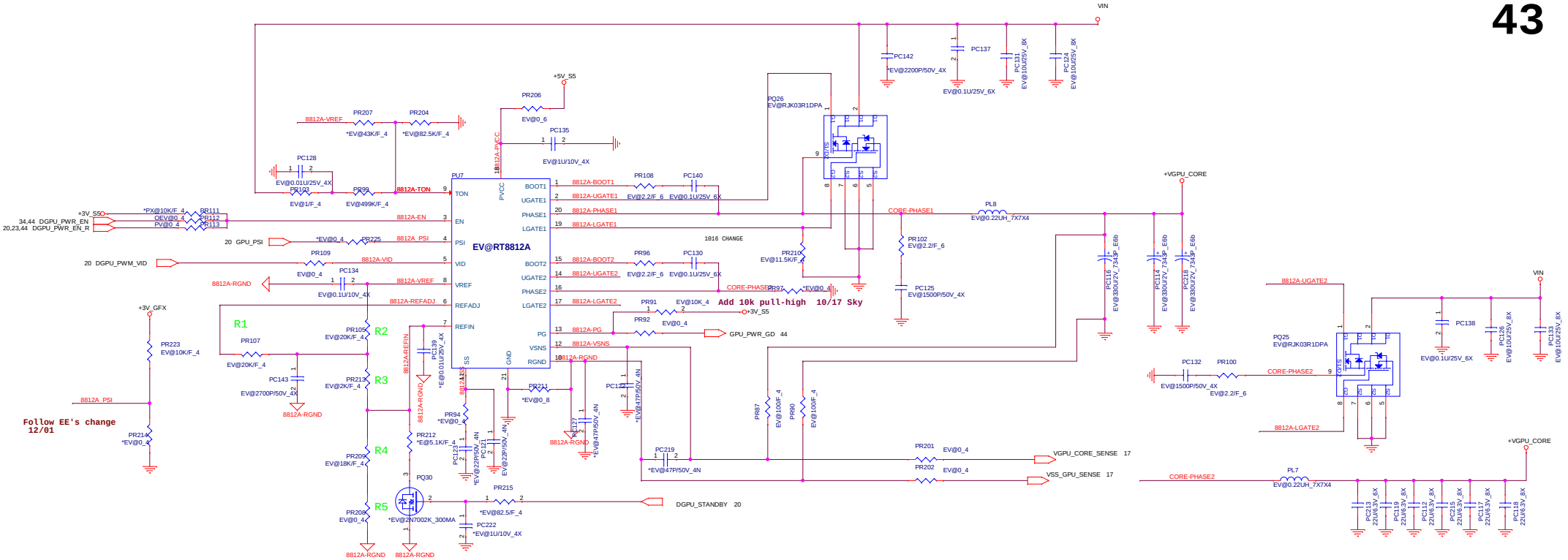
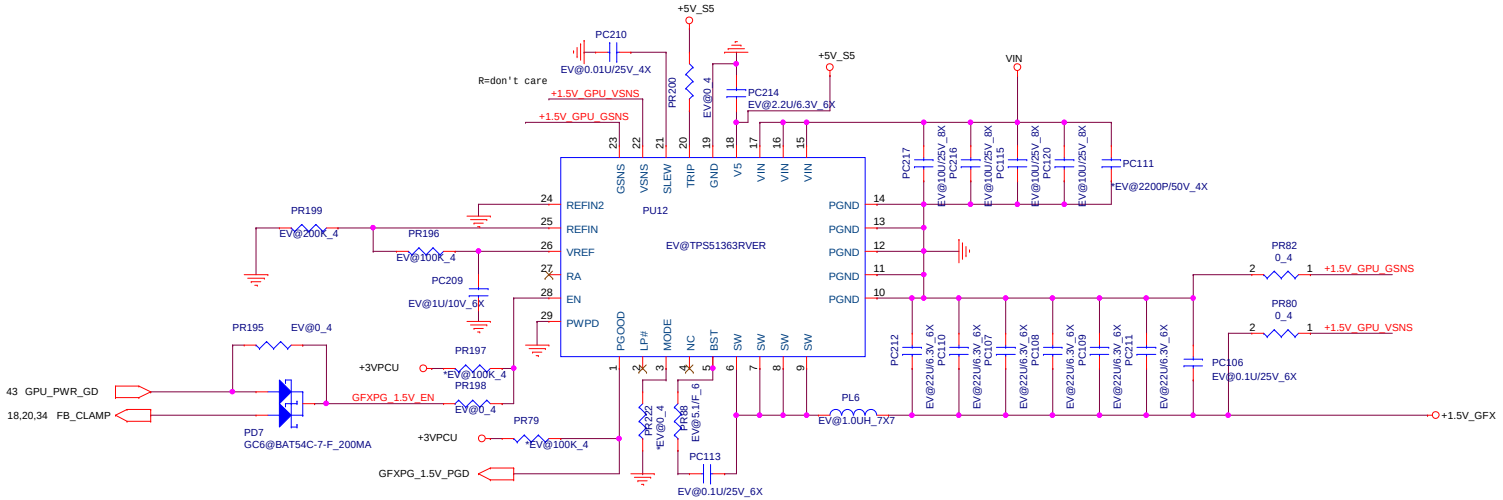
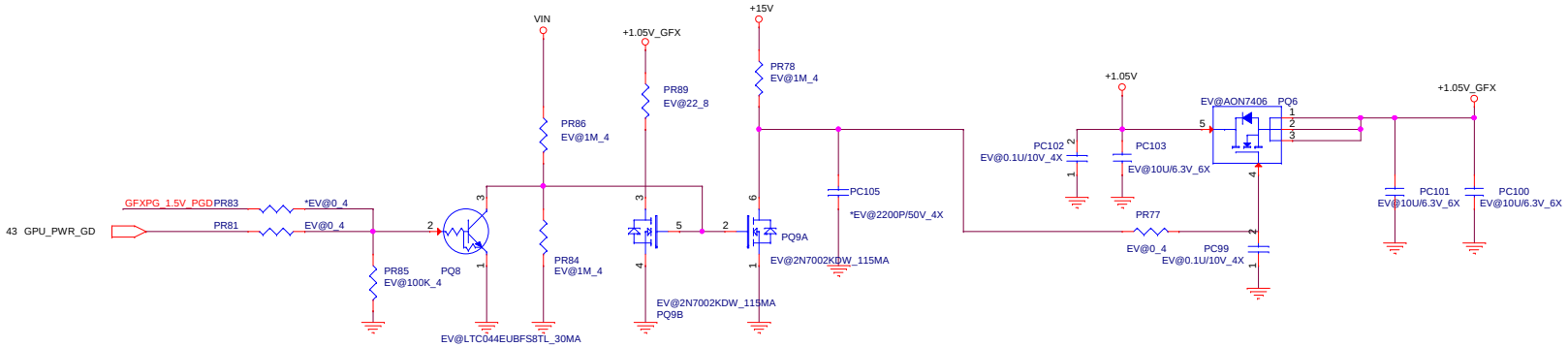
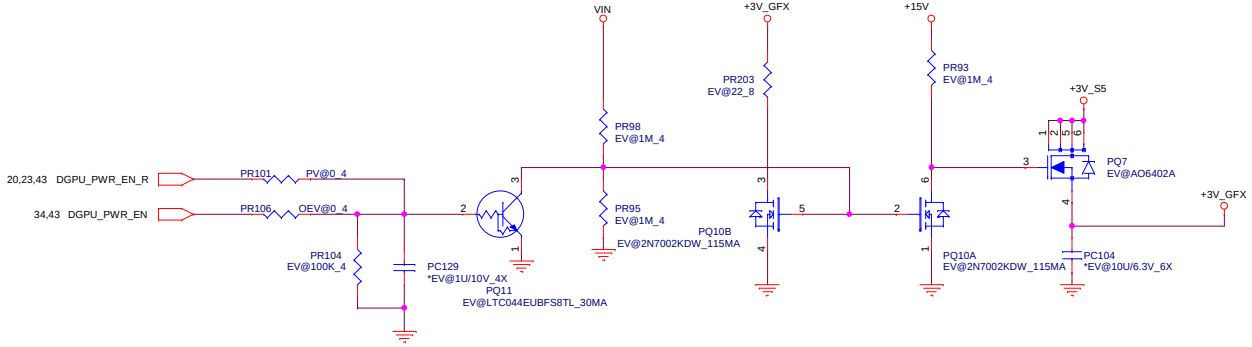


1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.







Quanta Computer Inc.

PROJECT : BDBD

Size	Document Number	Rev
	+VGACORE	2A

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Model	REV	CHANGE LIST
BDBD	B2A	PAGE 8: C795,C805 Change to 15pf PAGE 8: CN11 Change socket type PAGE 8:Add R1328 and R1516 for QUAD IO PAGE 9: Change C769,C763 to 12pf PAGE 10: Add board ID for SPK,CIR,TV PAGE 19: Change C731,C732 to 12pf PAGE 30: Add LAN IC PAGE 32: Change R638,R639,R640,R641,R642,R643,R644,R645 to bead PAGE 33: Change Card read to RTS5229 PAGE 34: Add R523 for PB_LED change to high active PAGE 34:Remove R411 for optimu PAGE 35: Change R499,R498,R505,R502 for LED brightness SPEC

MODEL BY3E

PAGE	FROM	To
1	1A	
2	1A	
3	1A	
4	1A	
5	1A	
6	1A	
7	1A	
8	1A	
9	1A	
10	1A	
11	1A	
12	1A	
13	1A	
14	1A	
15	1A	
16	1A	
17	1A	
18	1A	
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21	1A	
22	1A	
23	1A	
24	1A	
25	1A	
26	1A	
27	1A	
28	1A	
29	1A	
30	1A	

DOC NO. 20121217	PROJECT MODEL :	BDBD	APPROVED BY:		DATE:	
	PART NUMBER:		DRAWING BY:		REVISON:	

Quanta Computer Inc.
PROJECT : BDBD
Size | Document Number | Change list | Rev 2A
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