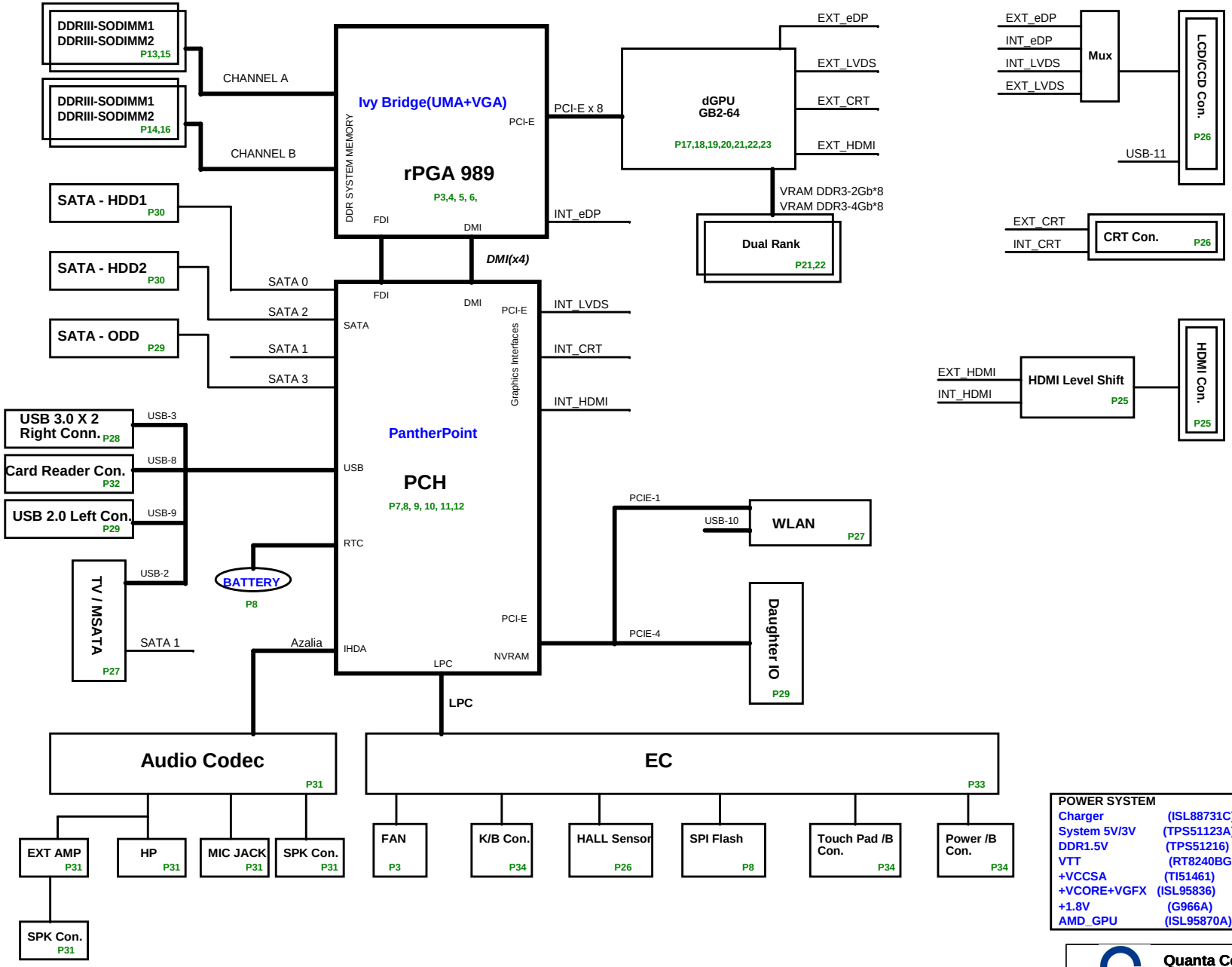
Chief River Block Diagram



POWER SYSTEM		
Charger	(ISL88731C)	P40
System 5V/3V	(TPS51123A)	P41
DDR1.5V	(TPS51216)	P42
VTT	(RT8240BGQW)	P43
+VCCSA	(TI51461)	P44
+VCORE+VGFX	(ISL95836)	P45
+1.8V	(G966A)	P46
AMD_GPU	(ISL95870A)	P47

Quanta Computer Inc.

PROJECT : BDAD

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	Block Diagram	A1A

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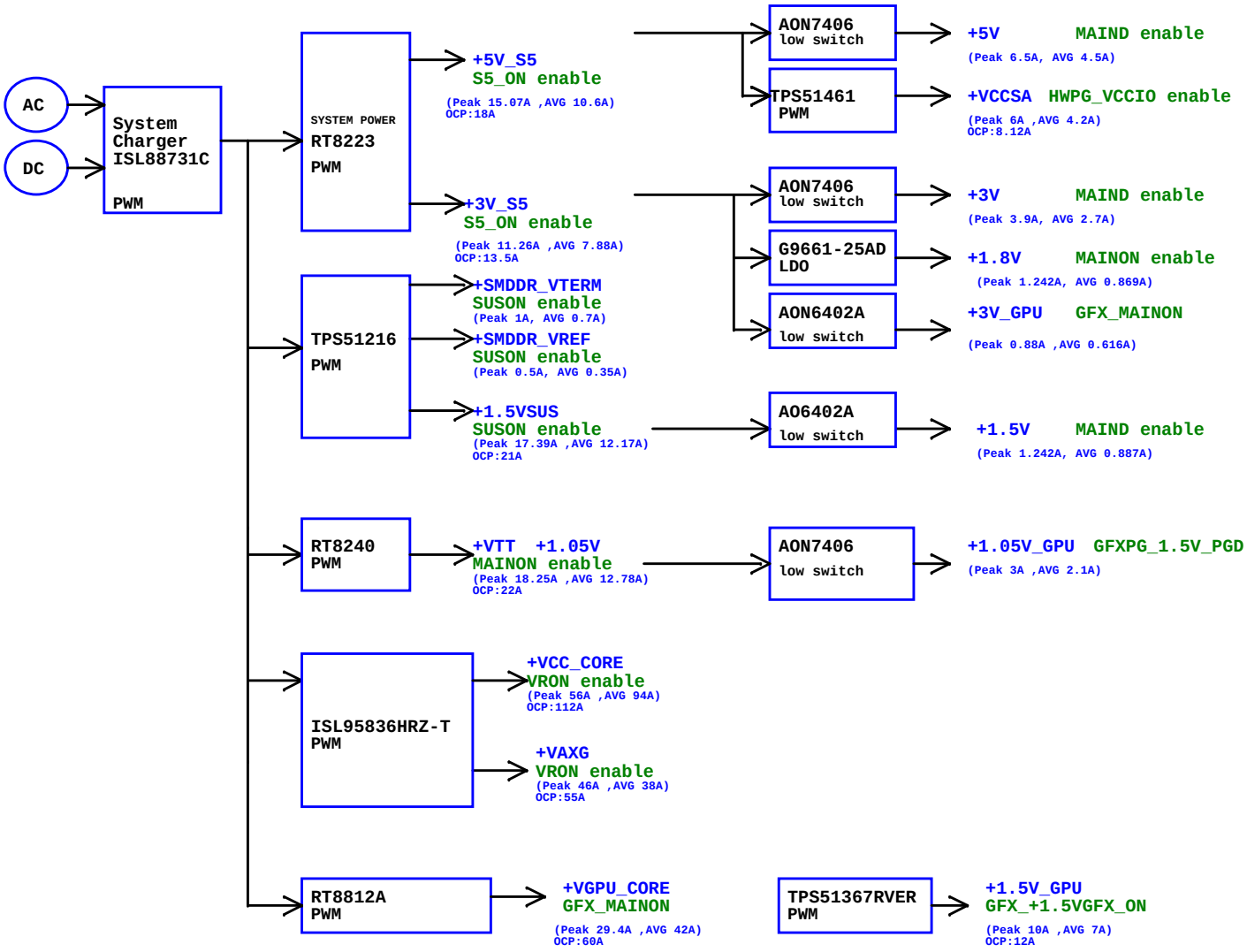
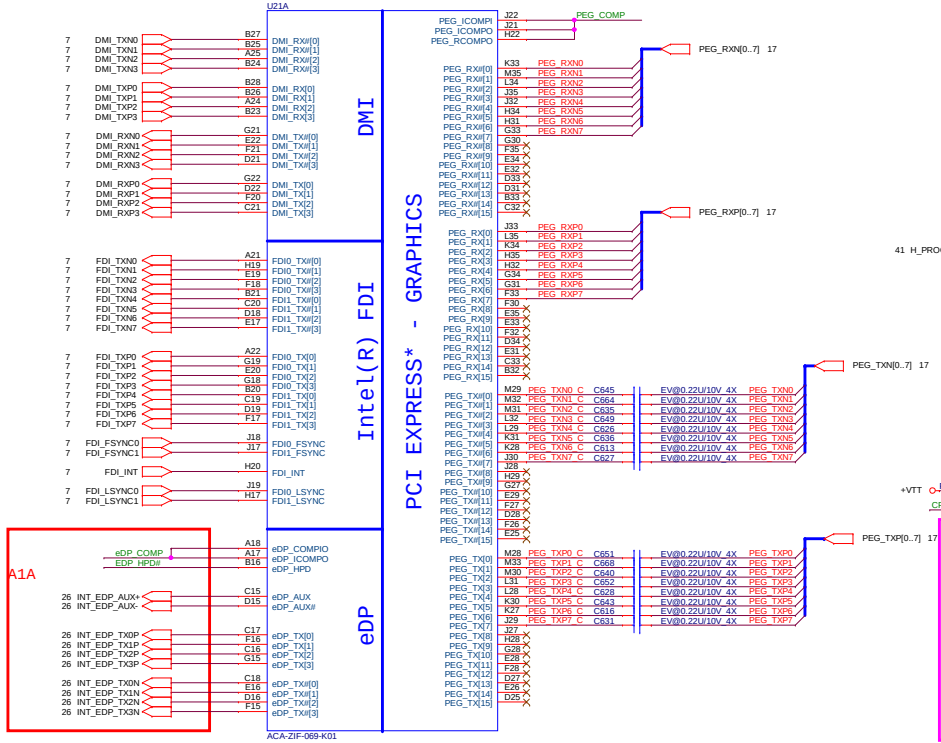
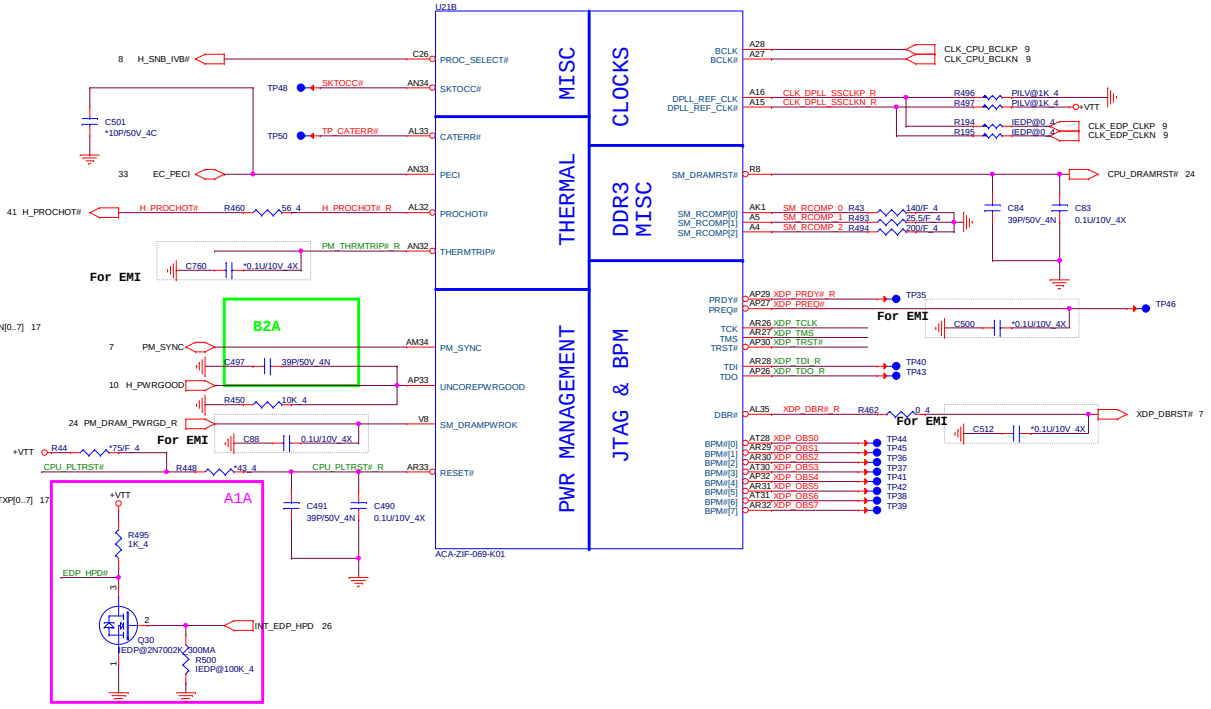


POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0~S5
+VCCRTC	+3.0V~+3.3V		S0~S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0~S5
+3V_HDP	+3.3V	MAIN_ON	S0
+3VPCU	+3.3V	AC/DC Insert enable	S0
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0~S5
+5VPCU	+5V	AC/DC Insert enable	S0~S5
WIMAX_P	+3.3V	WMAX_P for WLAN	
+1.8V	+1.8V	MAIN_ON	S0
+1.5V	+1.5V	MAIN_ON	S0
+1.5V_SUS	+1.5V	SUSON	S0~S3
+VCC_CORE		VRON	S0
+VTT	+1.05V	MAIN_ON	S0
+1.05V	+1.05V	MAIN_ON	S0
+VAXG		MPWROK	S0

Ivy Bridge Processor (DMI,PEG,FDI) CPU/VGA

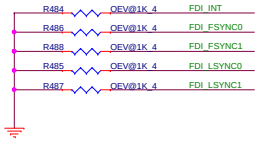


Ivy Bridge Processor (CLK,MISC,JTAG) CPU

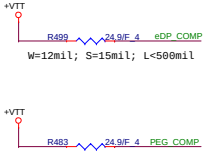


03

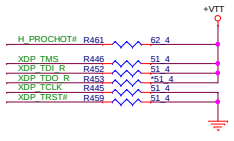
FDI Disabling (Discrete Only) OEV



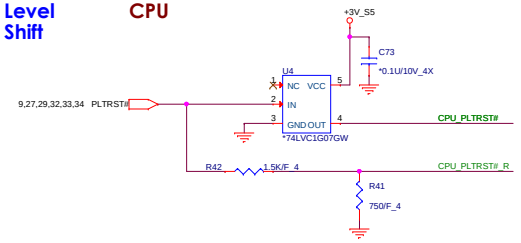
DP & PEG Compensation CPU



Processor pull-up CPU

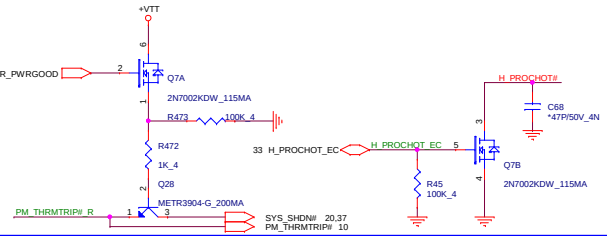


Level Shift CPU

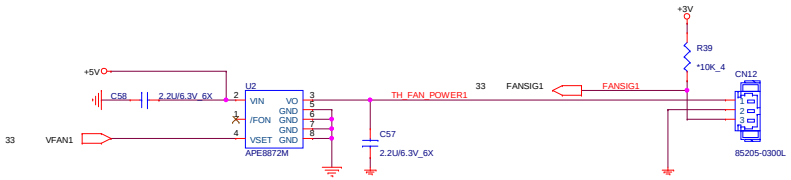


Thermal Trip & Process HOT CPU

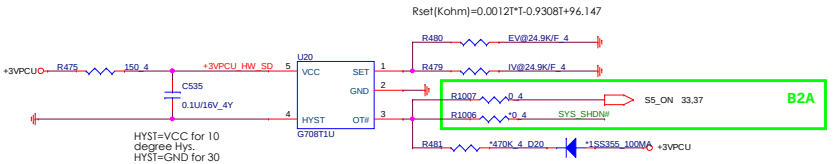
Intel Turbo mode only CPU



FAN Control-->For one FAN solution THC



CPU Thermal sensor / MB Local TEMP THP/UGA/VGA



Quanta Computer Inc.		
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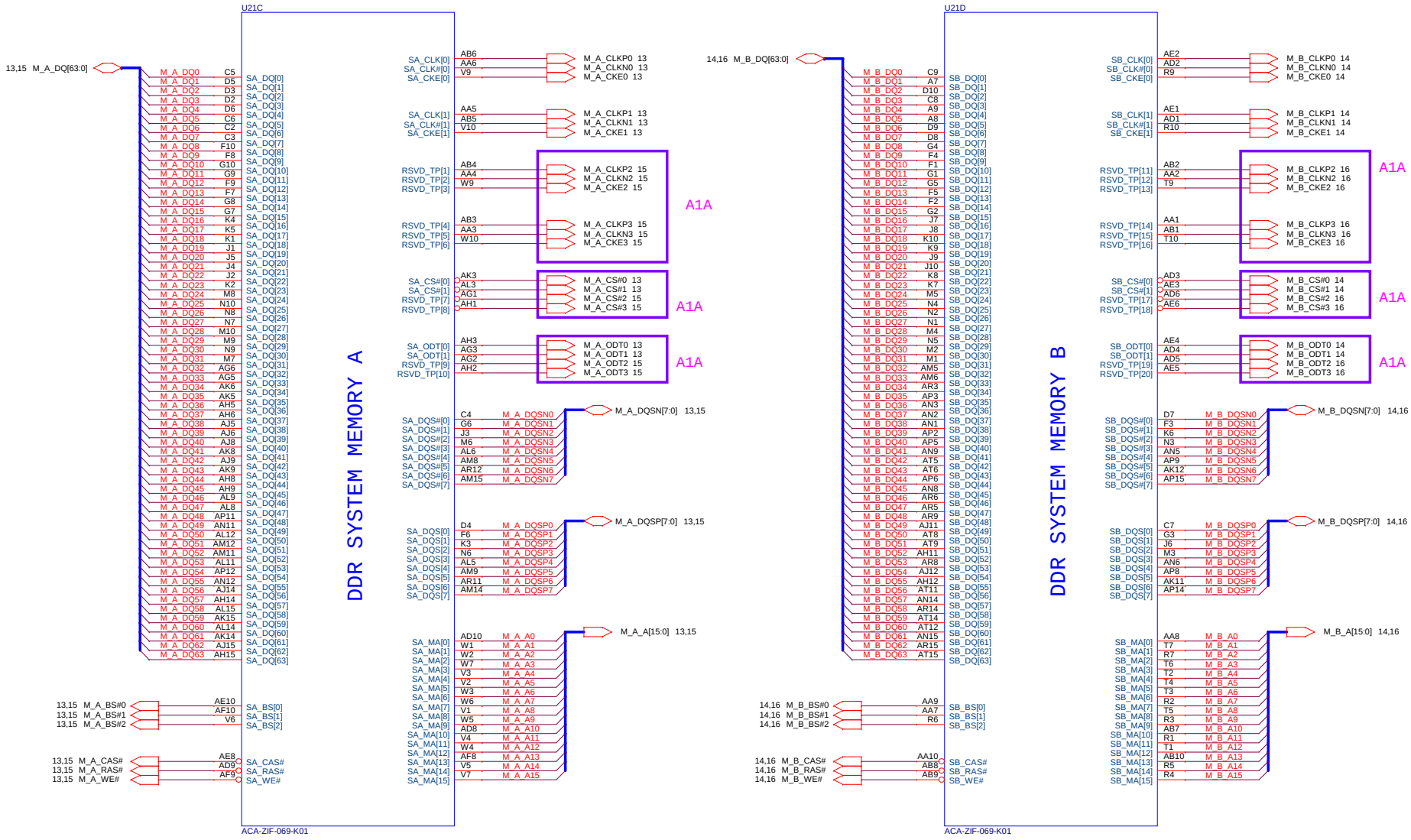
Ivy Bridge Processor (DDR3) CPU



Quanta Computer Inc.

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	Ivy Bridge 2/4	1A
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Ivy Bridge Processor (POWER) CPU

Ivy Bridge Processor (GRAPHIC POWER) CPU/OEV/PIV

POWER

IVB QC:94A

IVB:8.5A

U21F

+VCC_CORE

CORE SUPPLY

PEG AND DDR

SVID

SENSE LINES

ACA-ZIF-069-K01

U21G

+VAXG

GRAPHICS

SENSE LINES

VREF

DDR3 -1.5V RAILS

SA RAIL

MISC

1.8V RAIL

+1.8V

+VTT

+1.5V_CPU

+VCCSA

B2A

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Ivy Bridge 3/4

Rev 1A

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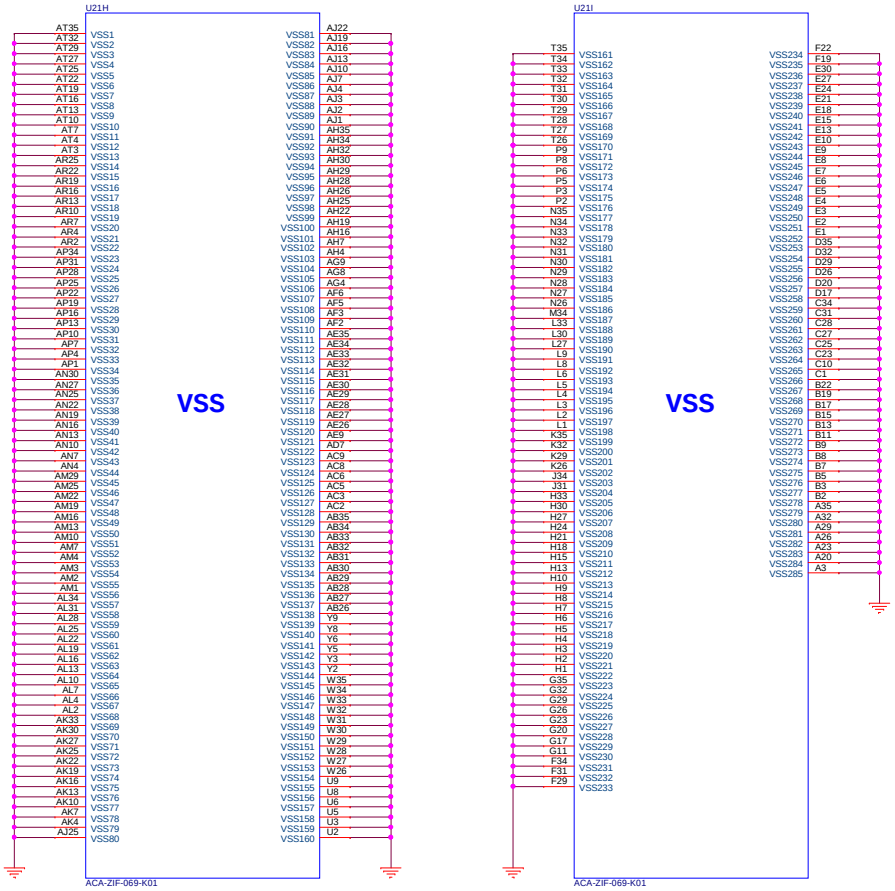
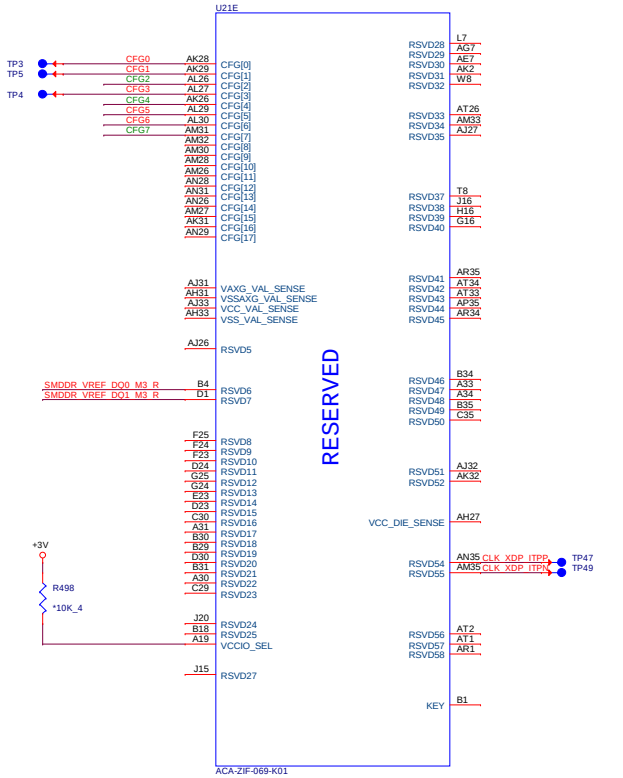
Ivy Bridge Processor (GND) CPU



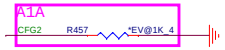
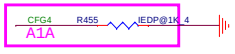
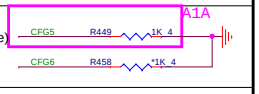
Ivy Bridge Processor (RESERVED, CFG) CPU

06

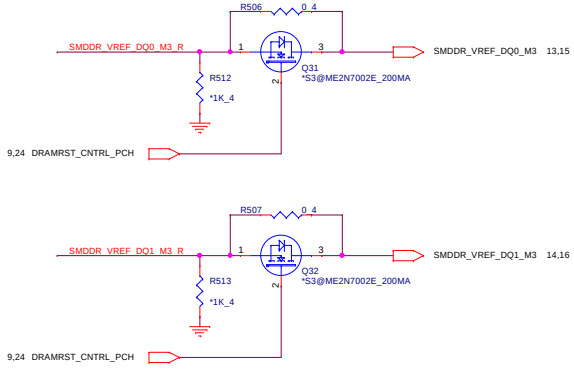


Processor Strapping CPU/VGA

The CFG signals have a default value of '1' if not terminated on the board.

Pin Name	Configuration	
CFG2 (PEG Static Lane Reversal --> 16 Lane)	1=Normal Operation 0=Lane Reversed	
CFG3 (Reserved)		
CFG4 (DP Presence Strap)	1=Disable; No physical DP attached to eDP 0=Enable; An ext DP device is connected to eDP	
CFG5 CFG6 (PCIE Bifurction)	00=x8,x4,x4 - Device 1 function 1 and 2 enable 01=Reserved - (Device 1 function 1 disable ; function 2 enable) 10=x8,x8 -Device 1 function 1 enable ; function 2 enable 11=(Default) x16 -Device 1 function 1 and 2 disable	
CFG7 (PEG Defer Training)	1=PEG train immediately following xxRESETB de assertion 0=PEG wait for BIOS training	

DDR3 VREF DQ (M3) S3P



Quanta Computer Inc.

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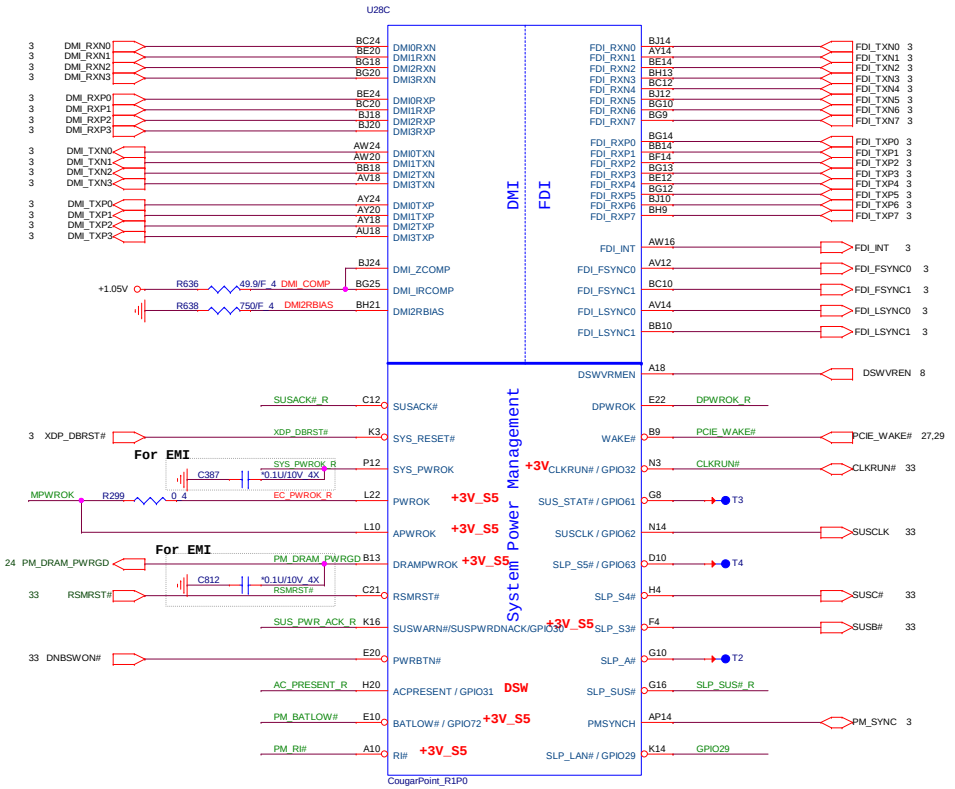
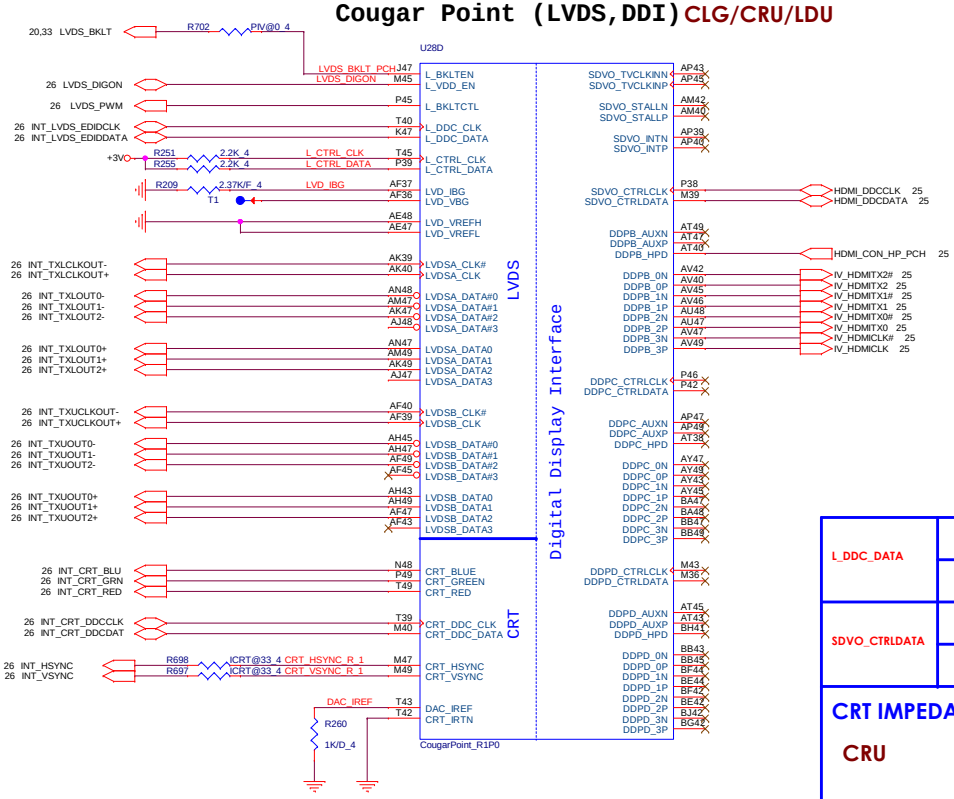
Cougar Point (DMI,FDI,PM) CLG



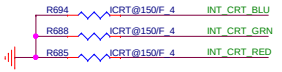
Cougar Point (LVDS,DDI) CLG/CRU/LDU



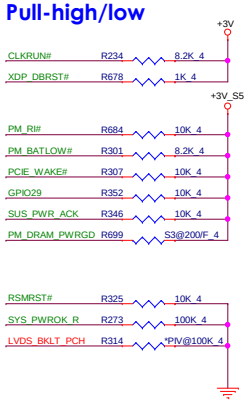
L_DDC_DATA	1 -- LVDS ENABLE
	0 -- LVDS DISABLE
SDVO_CTRLDATA	1 -- PORT B Detected
	0 -- PORT B Disable

CRT IMPEDANCE MATCHING

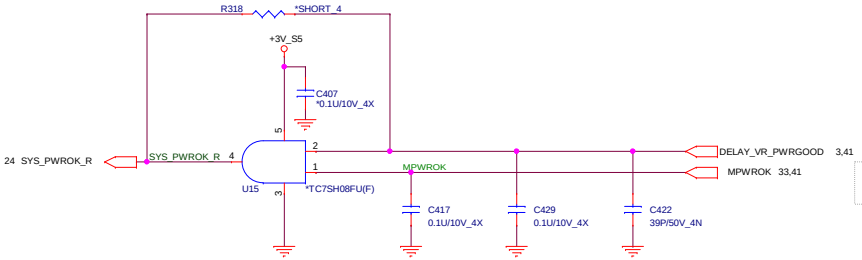
CRU



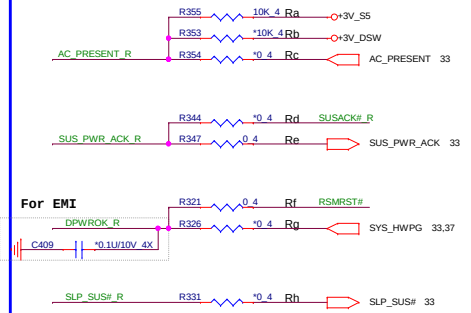
PCH Pull-high/low CLG/PIV/S3P



System PWR_OK CLG



Deep Sx CLG



Net Name	Deep Sx Support	Deep Sx No Support
AC_PRESENT	Rb,Rc stuff	Ra stuff
SUS_PWR_ACK	Rd stuff	Re stuff
DPWROK	Rg stuff	Rf stuff
SLP_SUS	Rh stuff	Rh No stuff

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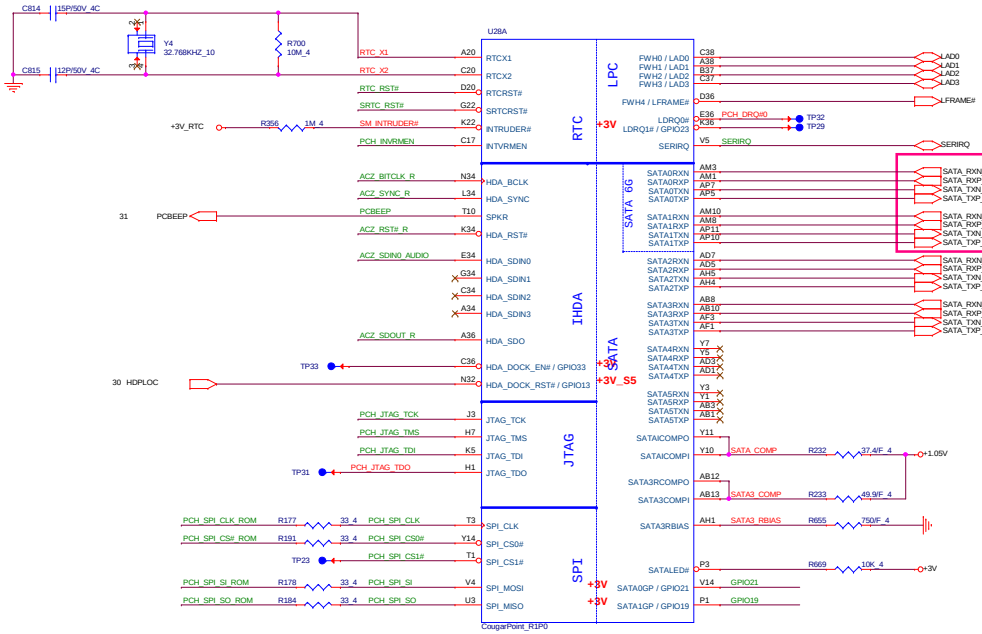
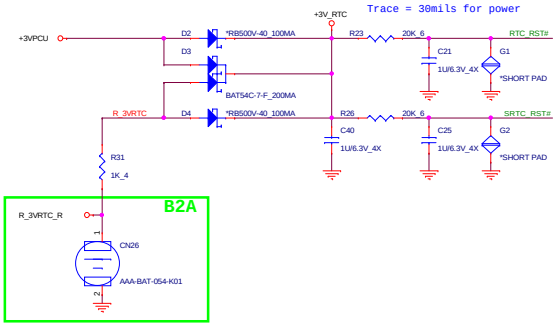
Cougar Point (HDA,JTAG,SATA) CLG/GCK

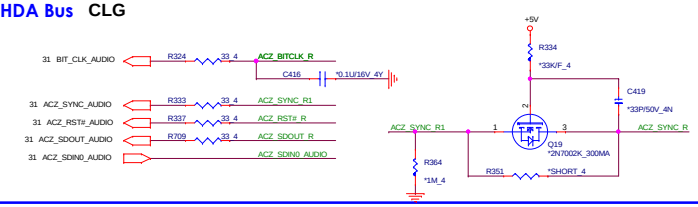


RTC Circuitry

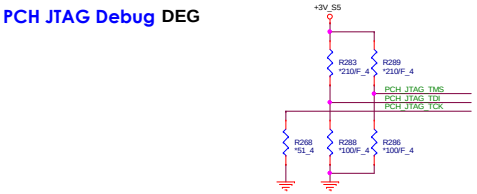


PU & Password Clear CLG

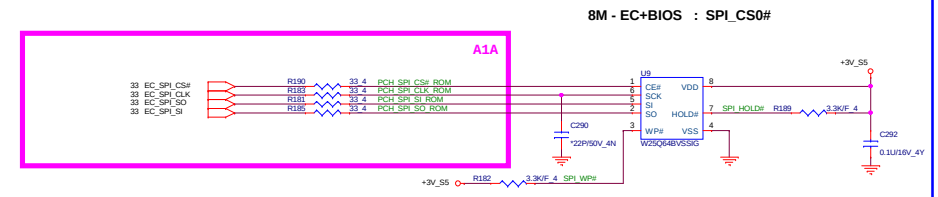
HDA Bus CLG



PCH JTAG Debug DEG



PCH Dual SPI CLG



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GPIO19 → Boot Location: 1/1 SPI *; 0/0 LPC
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK	
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)
DF_TVS	DMI/FDI Termination voltage	PWROK	**0 = Set to Vss** **1 = Set to Vcc (weak pull-down 20K)**
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	**0 = Support by 1.8V (weak pull-down)** **1= Support by 1.5V**
INIT3_3V#	Reserved	PWROK	1 = Default (weak pull-up 20K)	**Should not pull low. leave as No Connect**
GNT2#/ GPIO53	ESI Strap (Server Only)	PWROK	1 = Default. Should not be pulled low for desktop and mobile	**Should not pull low for desktop and mobile**
GPIO15	TLS Confidentiality	RSMRST	0 = Default. TLS no Confidentiality 1 = TLS Confidentiality
L_DDC_DATA	LVDS Detected	PWROK	0 = Default. Not Detected 1 = Detected	1= PU to 3V
SDVO_CTRLDATA	Port B Detected	PWROK	0 = Default. Not Detected 1 = Detected	1= PU to 3V
DDPC_CTRLDATA	Port C Detected	PWROK	0 = Default. Not Detected 1 = Detected	0=NC
DDPD_CTRLDATA	Port D Detected	PWROK	0 = Default. Not Detected 1 = Detected	0=NC
SATA3GP/ GPIO37	Reserved	PWROK	0 = Default	**Should not be pulled high when strap is sampled**
SATA2GP/ GPIO36	Reserved	PWROK	0 = Default	**Should not be pulled high when strap is sampled**
DSWVRMEN	Deep S4/S5 Well On -Die Voltage Regulator Enable	ALWAYS	0 = Disable 1 = Enable

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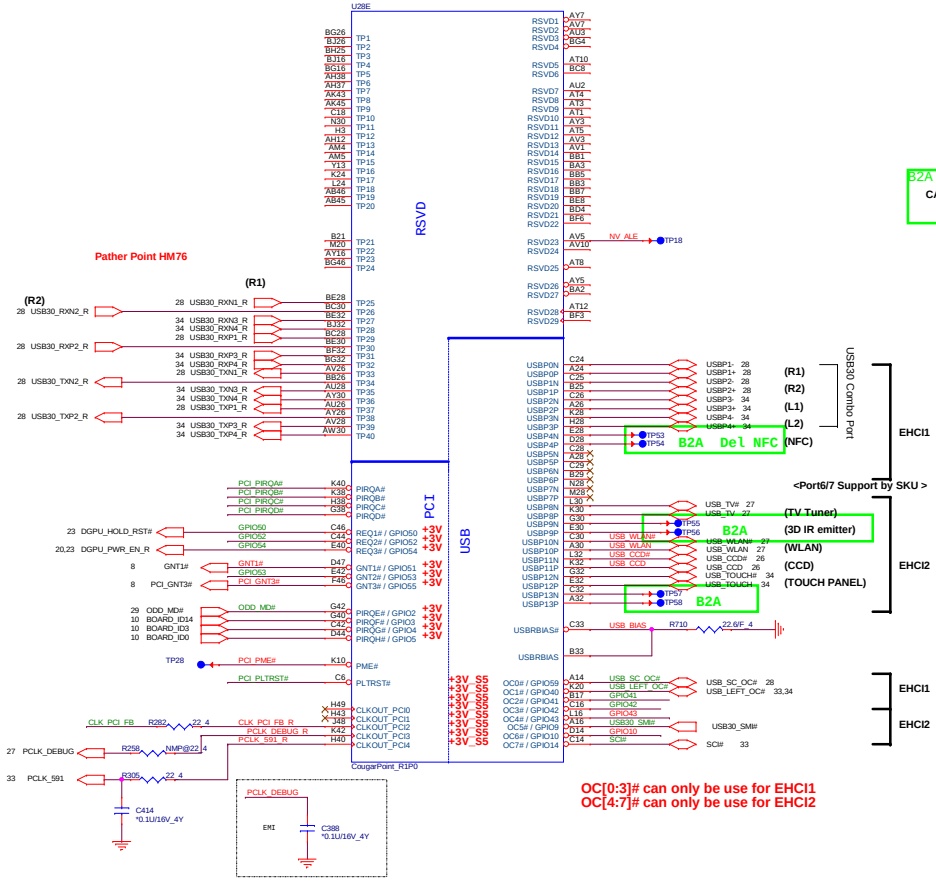
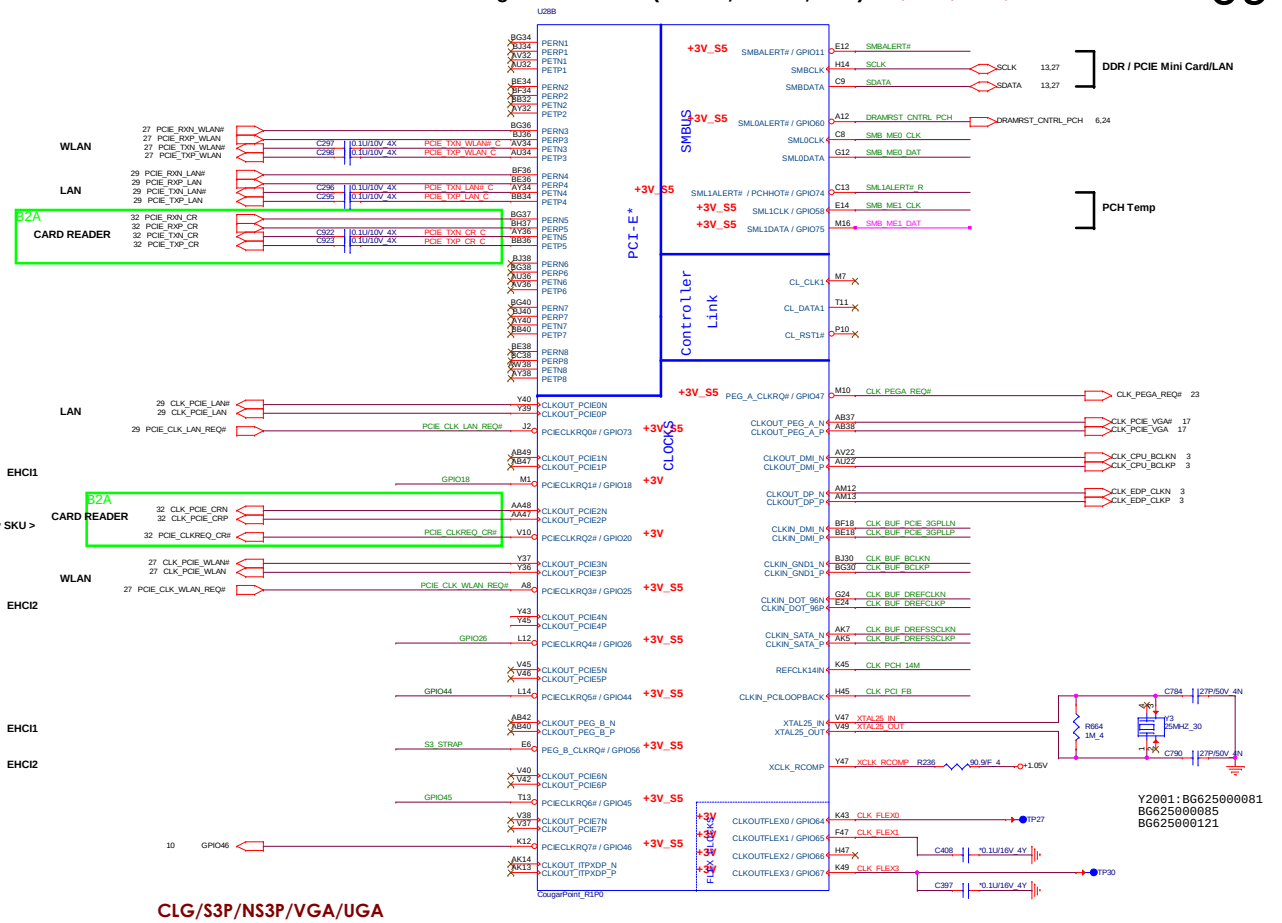
Cougar Point-M (PCI,USB,NVRAM) CLG/DEG

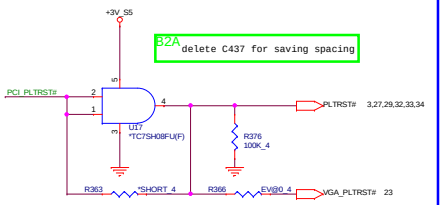


Cougar Point-M (PCI-E,SMBUS,CLK)CLG/GCK/MNG/U3C

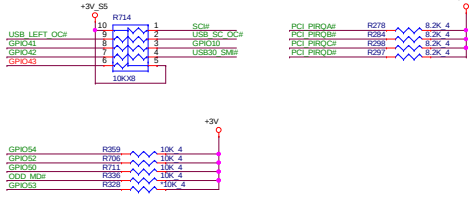


CLG/S3P/NS3P/VGA/UGA

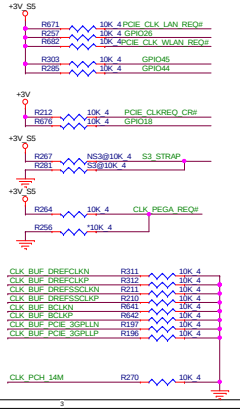
PLTRST# CLG



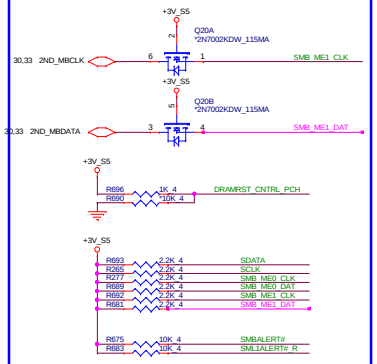
PCI/USBOC# Pull-up CLG



CLK_REQ/Strap Pin



SMBus/Pull-up CLG



	33MHz	27MHz	48/24MHz	14.318MHz	25MHz
CLK_FLEX0	●	●	●	●	
CLK_FLEX1		●	●	●	
CLK_FLEX2	●	●	●	●	●
CLK_FLEX3		●	●	●	

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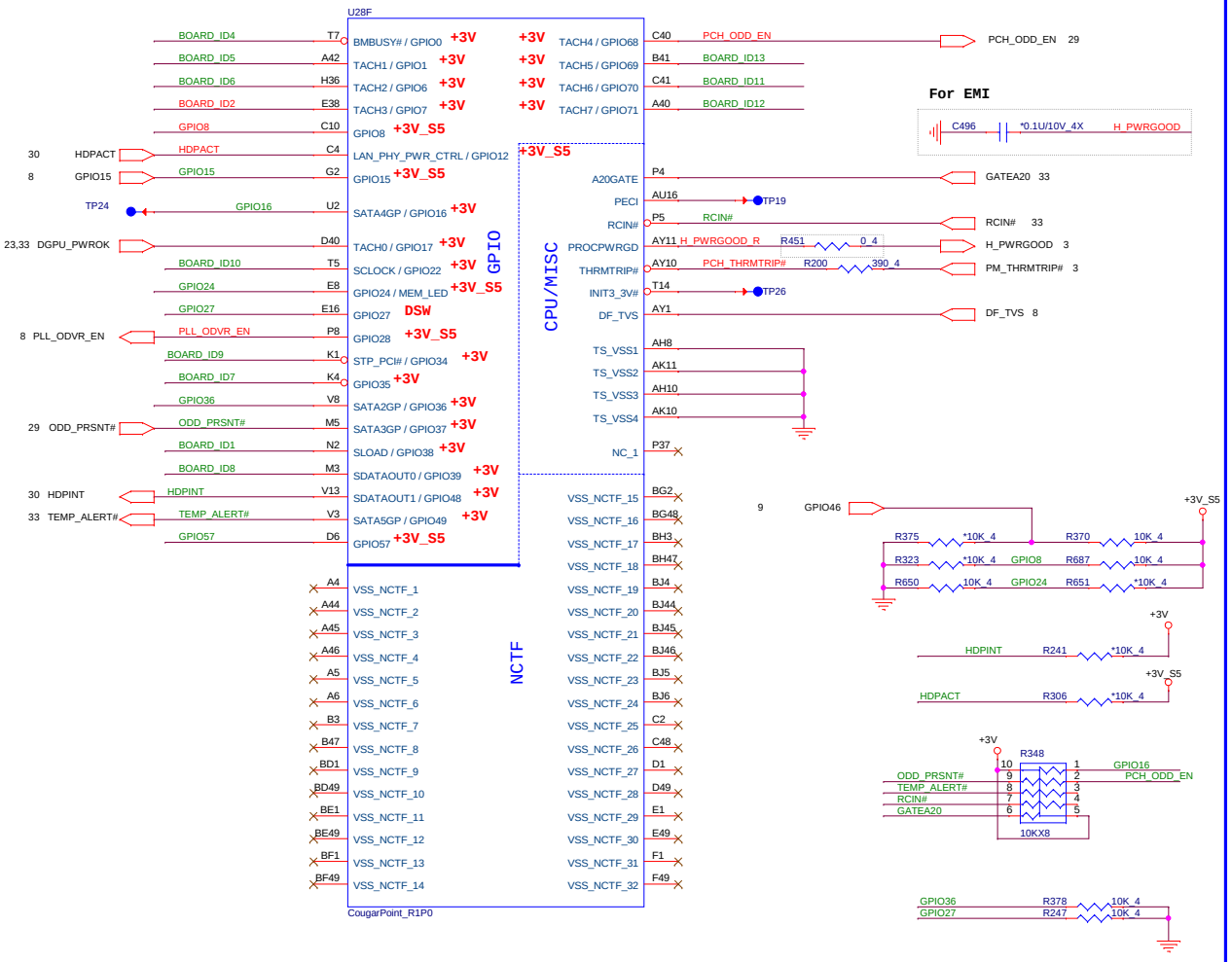
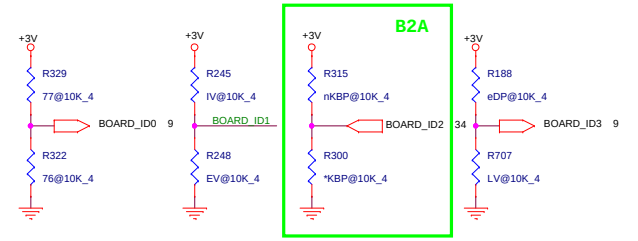
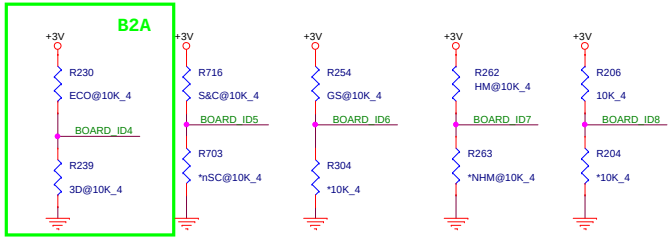
Cougar Point (GPIO,VSS_NCTF,RSVD) CLG

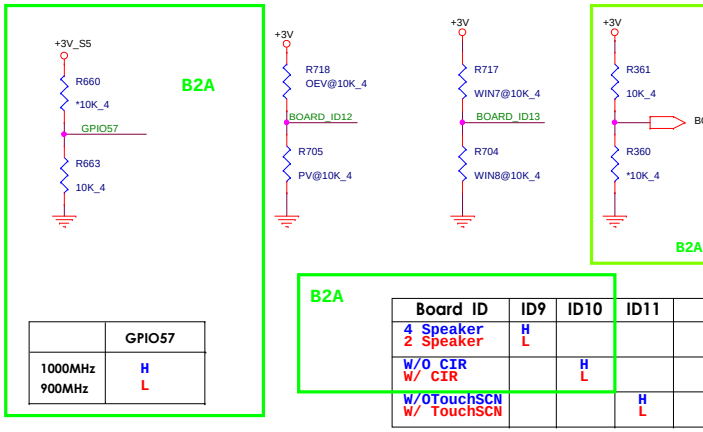


BOARD ID SETTING CLG/PX/OEV/UGA/CLG-Strap

Board ID	ID0	ID1	ID2	ID3	ID4	ID5	ID6	ID7	ID8	ID12	ID13	ID14
HM77 HM76	H L											
UMA SKU VGA SKU		H L										
W/O LED KB W/ LED KB			H L									
eDP LVDS				H L								
ECO Mode 3D Mode					H L							
S&C Non S&C						H L						
W/ G-sensor W/O G-sensor							H L					
W/ HDMI W/O HDMI								H L				
Premium Gaming									H L			
Only VGA Optimus mode										H L		
WIN7 WIN8											H L	
W/O TV W/ TV												H L







	GPIO57
1000MHz	H
900MHz	L

B2A

Board ID	ID9	ID10	ID11	
4 Speaker 2 Speaker	H L			
W/O CIR W/ CIR		H L		
W/OTouchSCN W/ TouchSCN			H L	

Quanta Computer Inc.

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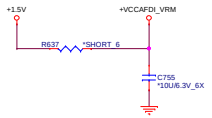
COUGAR POINT (POWER) CLG

CLG/PIV/OEV

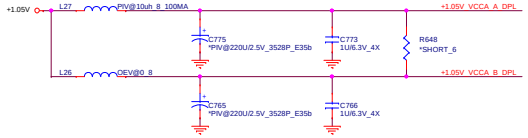
CLG

CLG

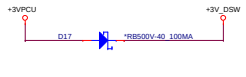
Internal PLL and VRMS CLG



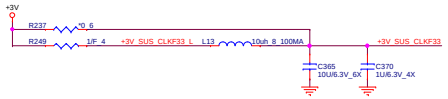
Display PLL A/B Analog Power CLG/PIV/OEV



Deep Sx power well CLG



Clock power on core well CLG



Quanta Computer Inc.
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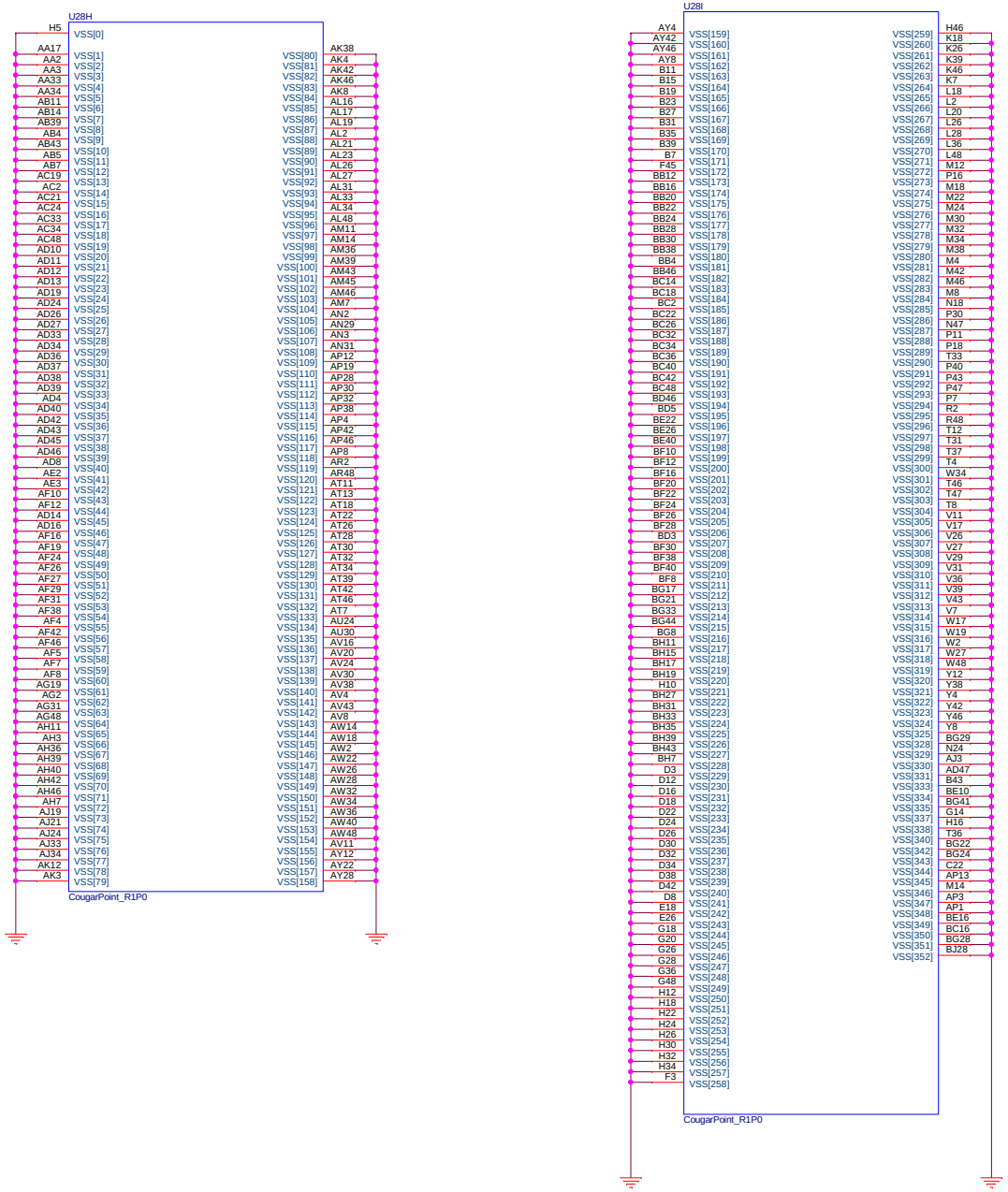

Quanta Computer Inc.

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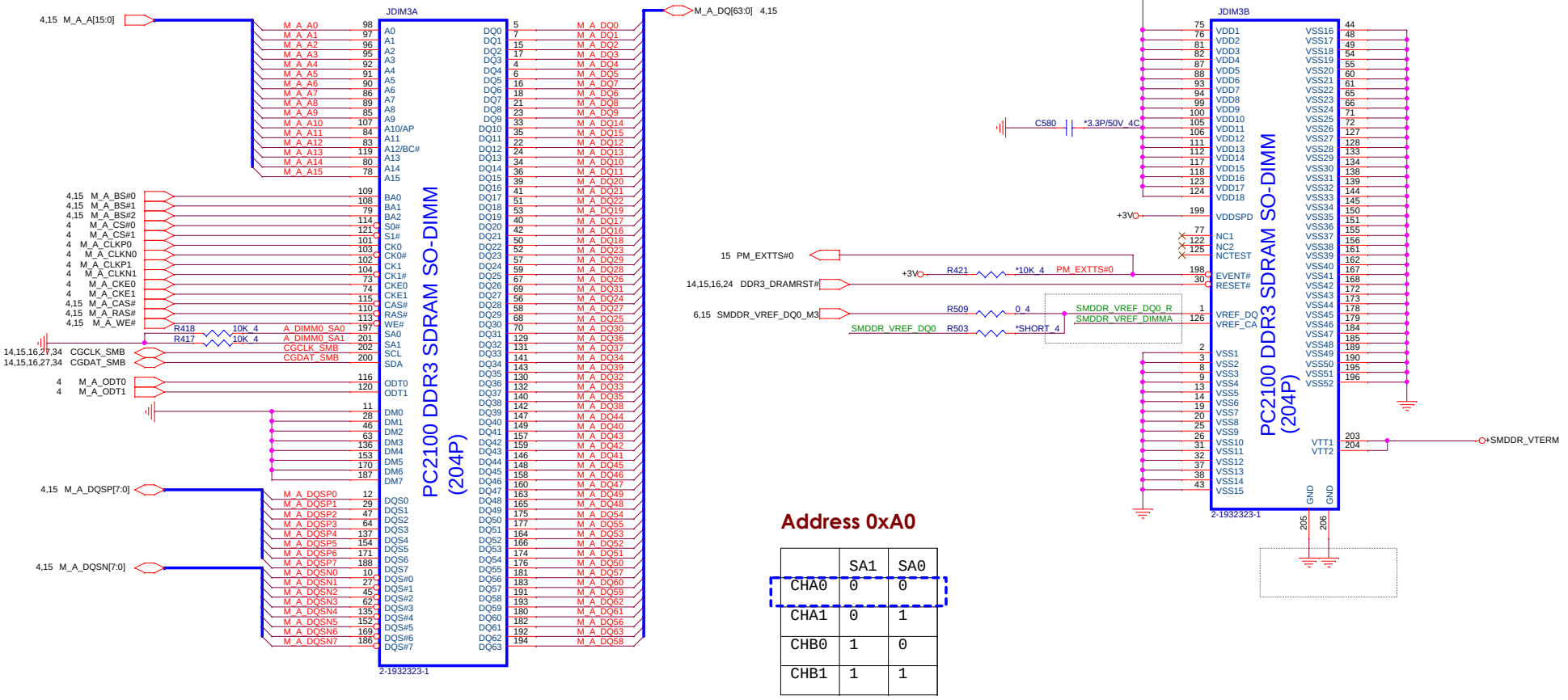
DDR

BOT side close to CPU

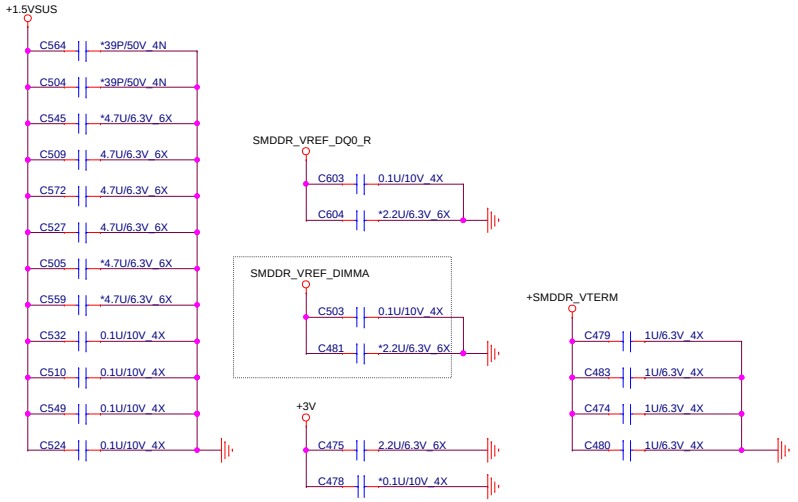
H=8 (Rev)



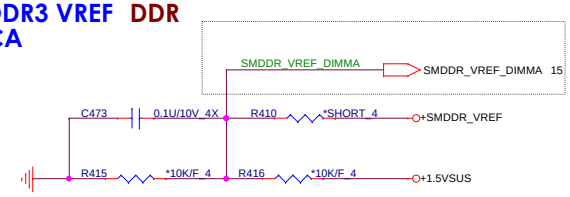
Address 0xA0

	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

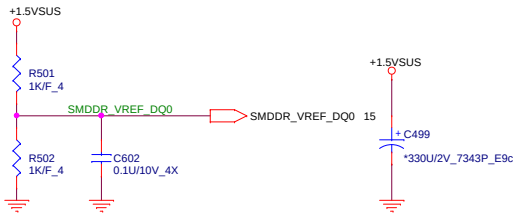
DDR Power Decoupling DDR



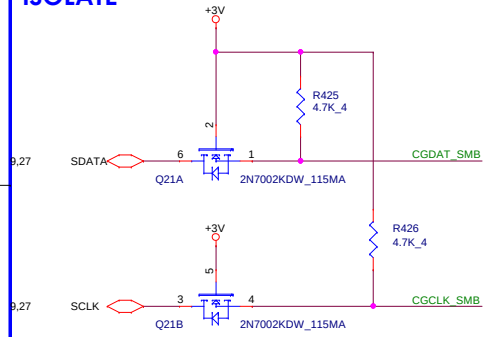
DDR3 VREF CA DDR



DDR3 VREF DQ (M1) DDR



SMBUS ISOLATE DDR



Quanta Computer Inc.

PROJECT : BDAD

Size	Document Number	Rev
	DDR3 DIMM-0	A1A

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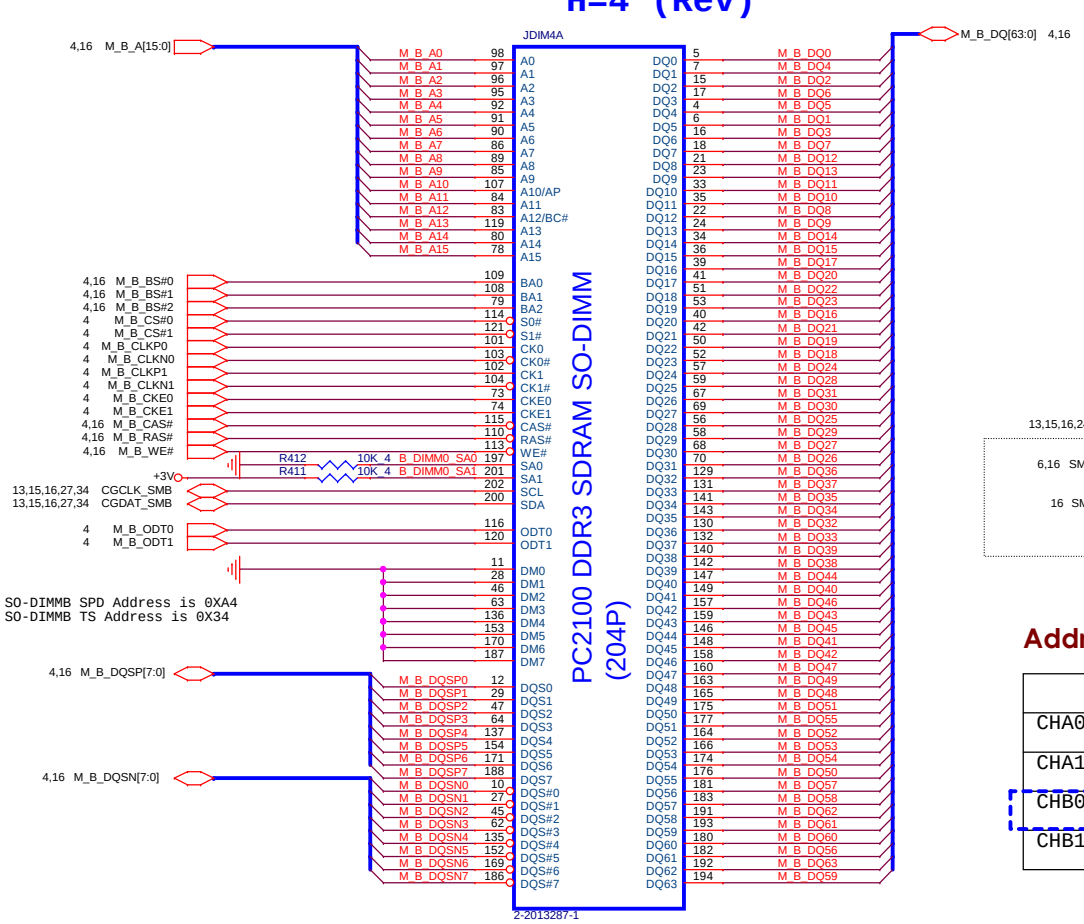
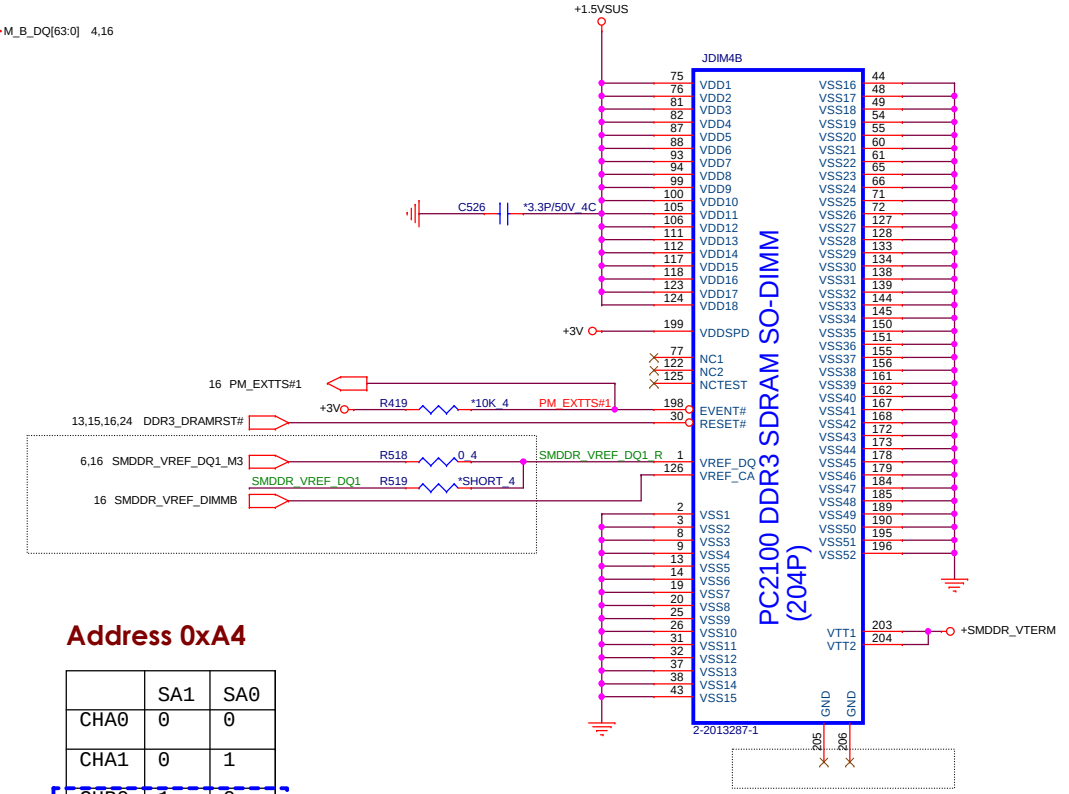
BOT Side Far Away CPU

H=4 (Rev)



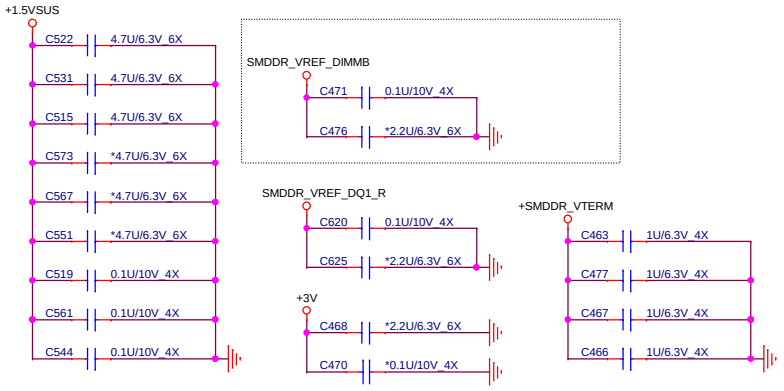
SO-DIMMB SPD Address is 0XA4
SO-DIMMB TS Address is 0X34



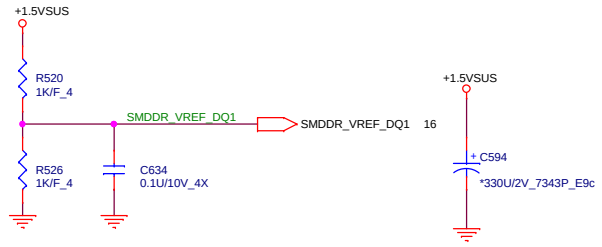
Address 0xA4

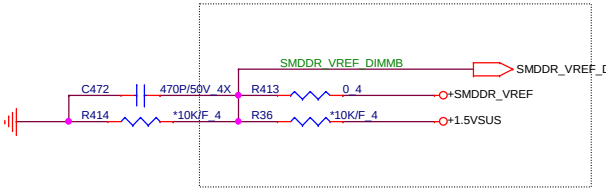
	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

DDR Power Decoupling DDR



DDR3 VREF DQ (M1) DDR





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Size	Document Number: DDR3 DIMM-1	Rev: A1A
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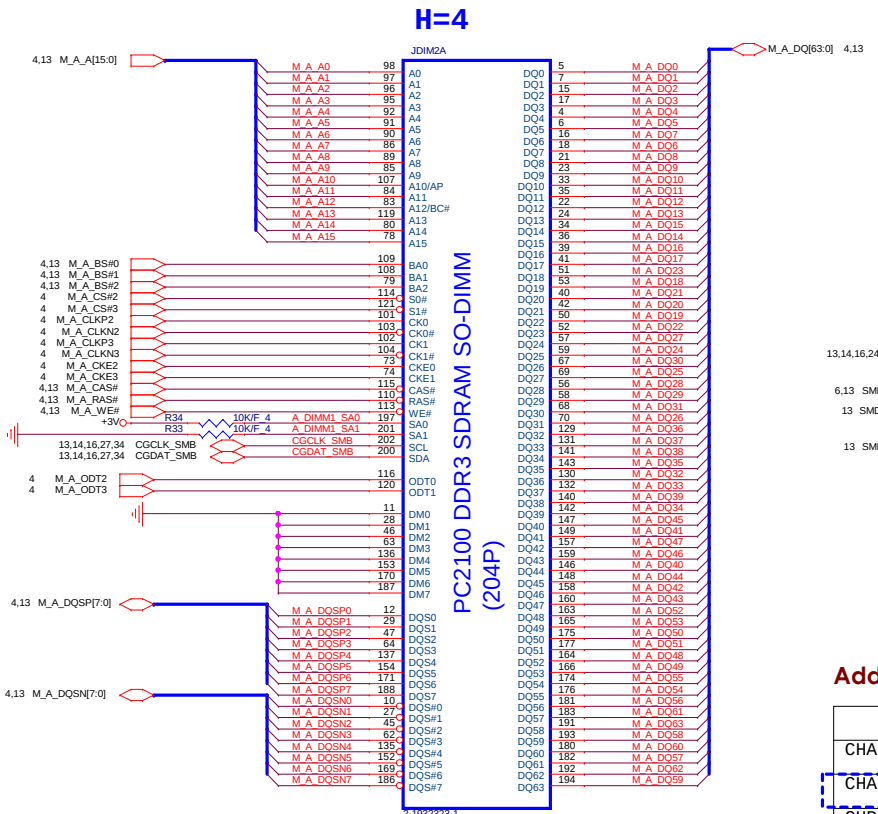
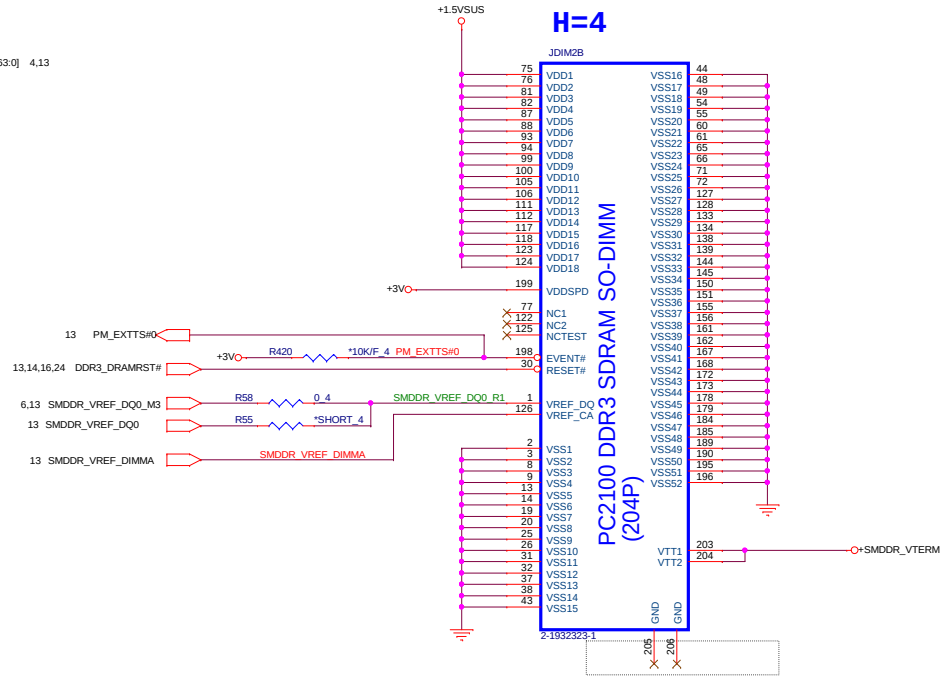
<DDR>

TOP side Face to CPU

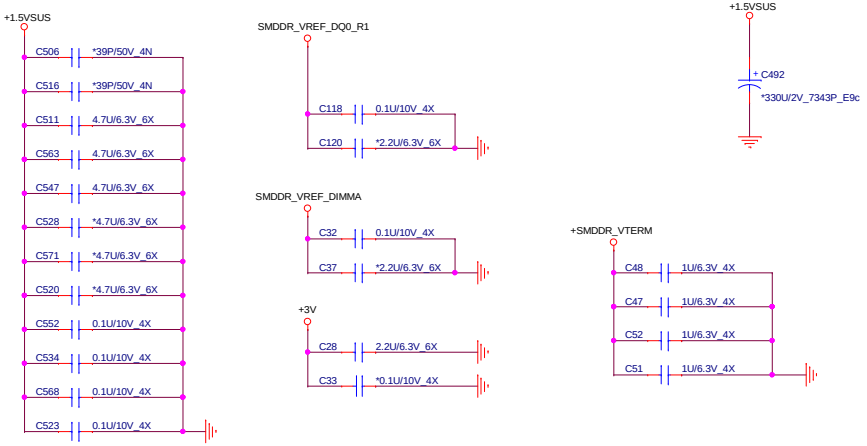




Address 0xA2

	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

Place these Caps near Memory Down-1



Quanta Computer Inc.
PROJECT : BDAD

Size	Document Number	Rev
	DDR3 DIMM-0	1A

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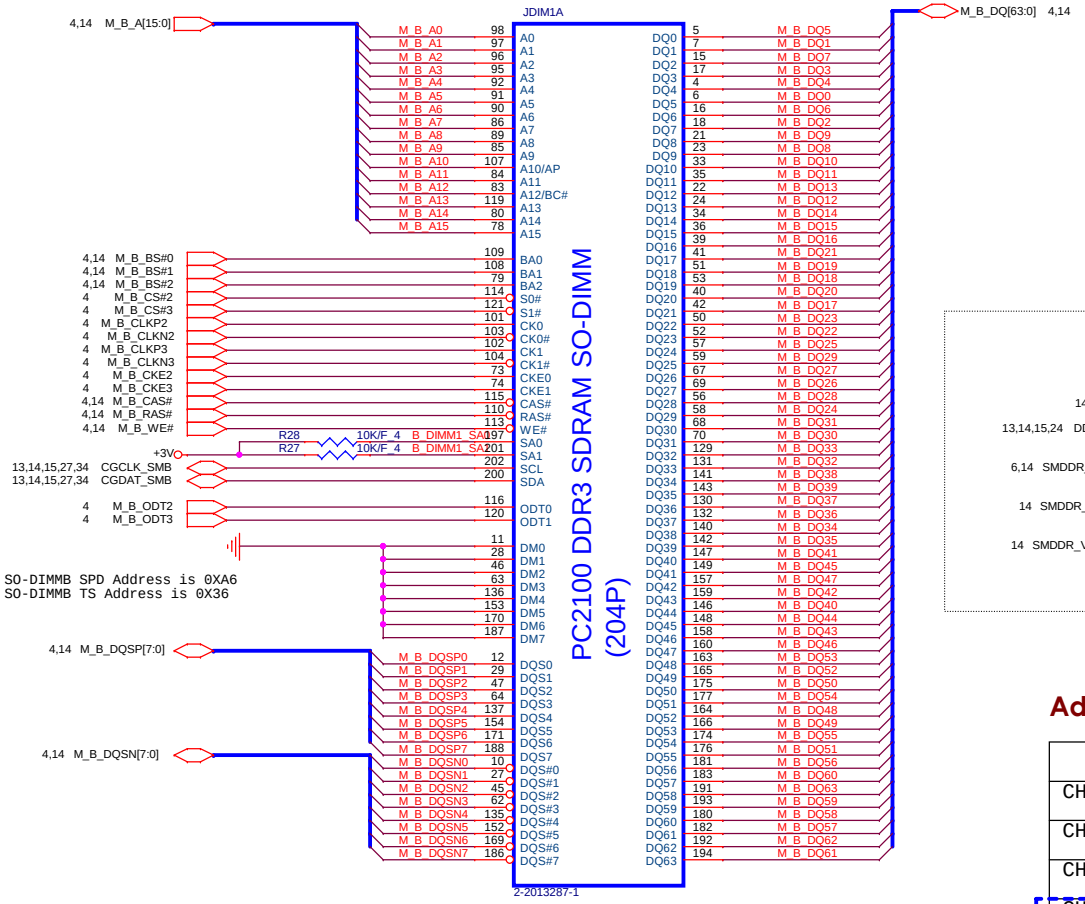
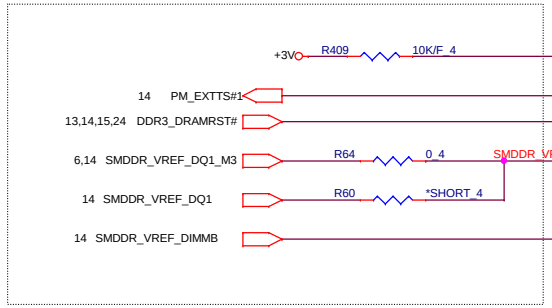
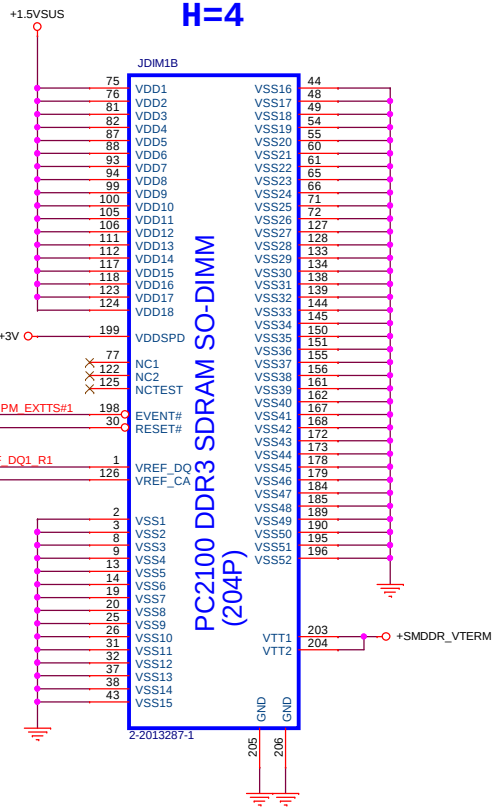
TOP Side Far Away CPU

H=4



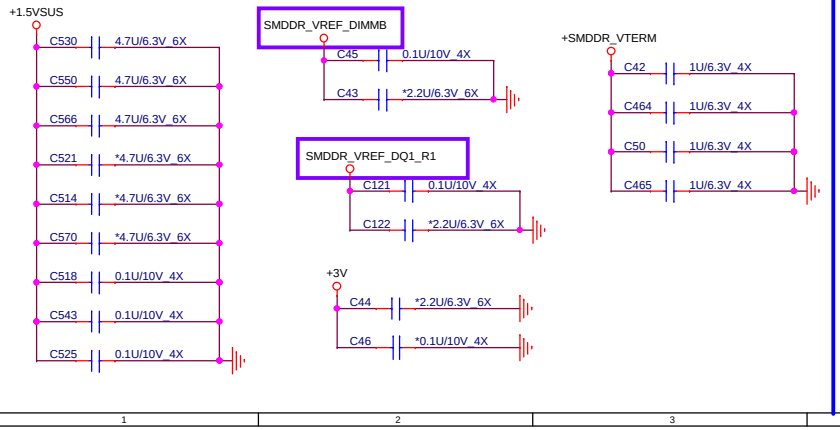


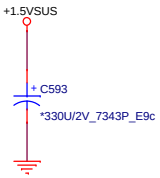


Address 0xA6

	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

Place these Caps near So-Dimm1.





Quanta Computer Inc.

PROJECT : BDAD

Size	Document Number	Rev
	DDR3 DIMM-1	3B

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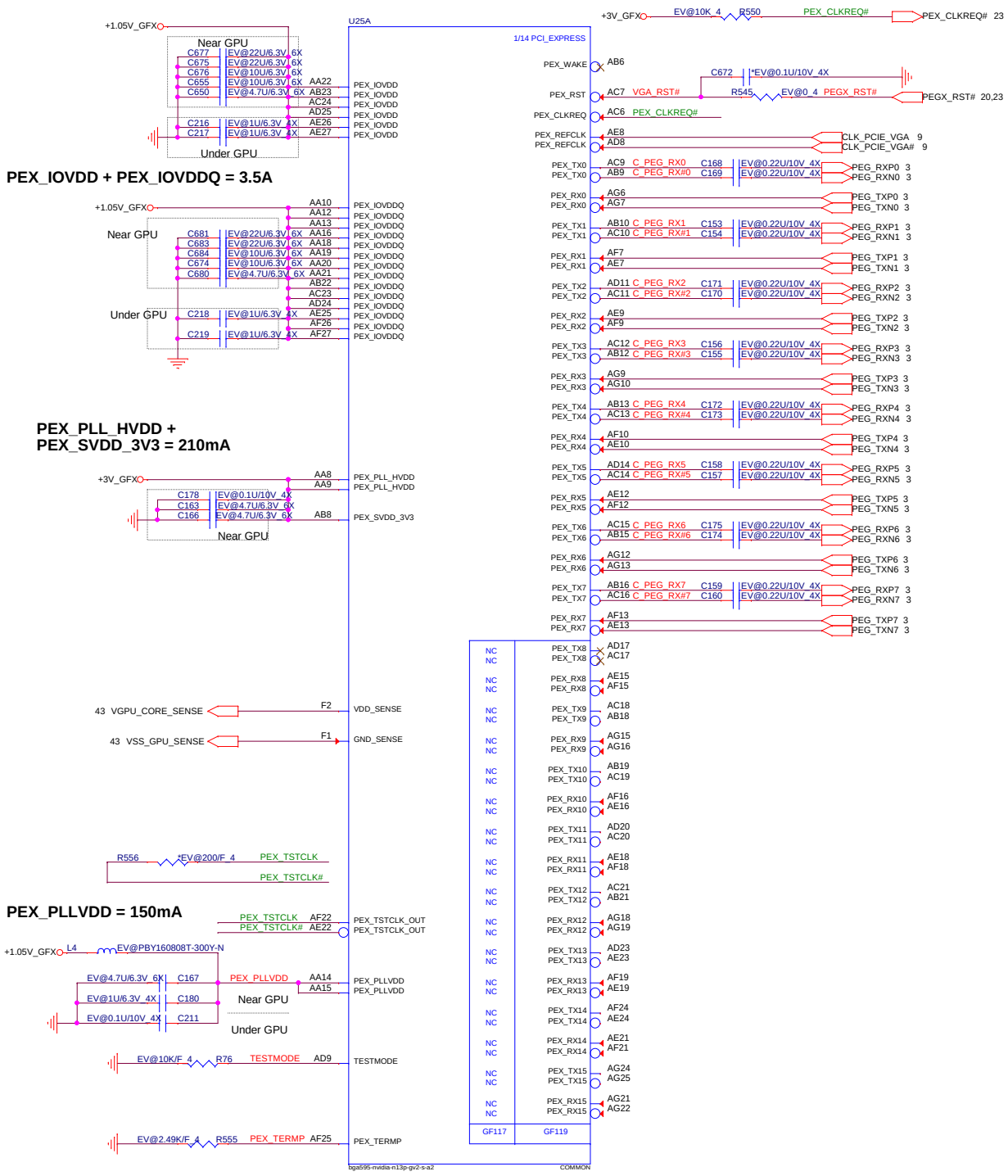
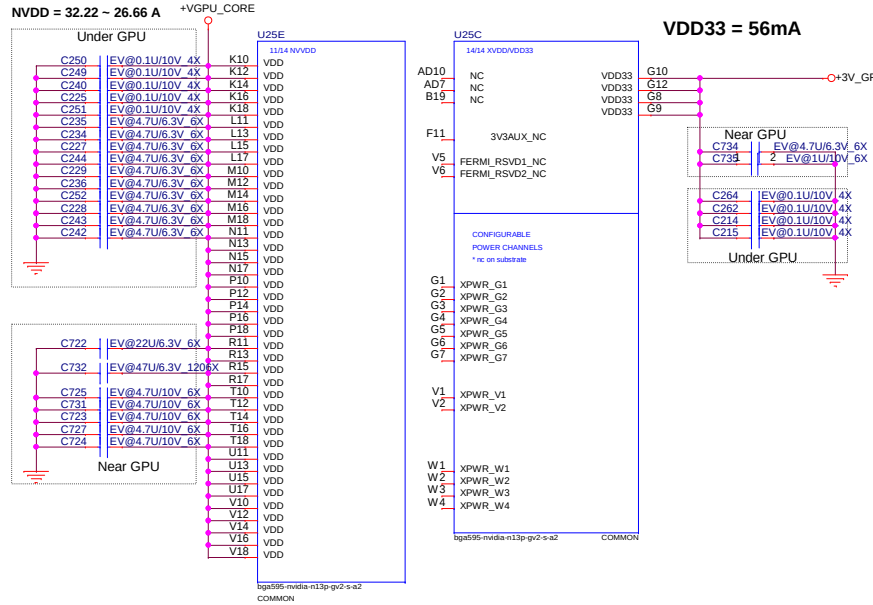
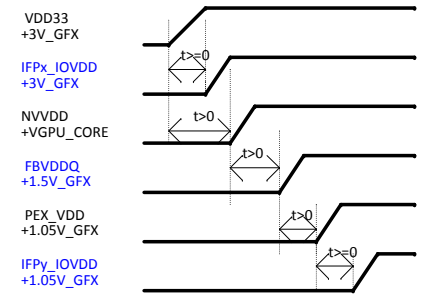
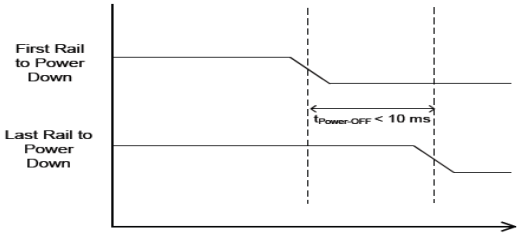




Power up sequence



Power down sequence



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FBVDDQ + FBVDD = 4.88A

For Terminal

FB_PLLAVDD = 62mA

FB_DLLAVDD = 35mA

Under GPU

Near GPU

Quanta Computer Inc.	
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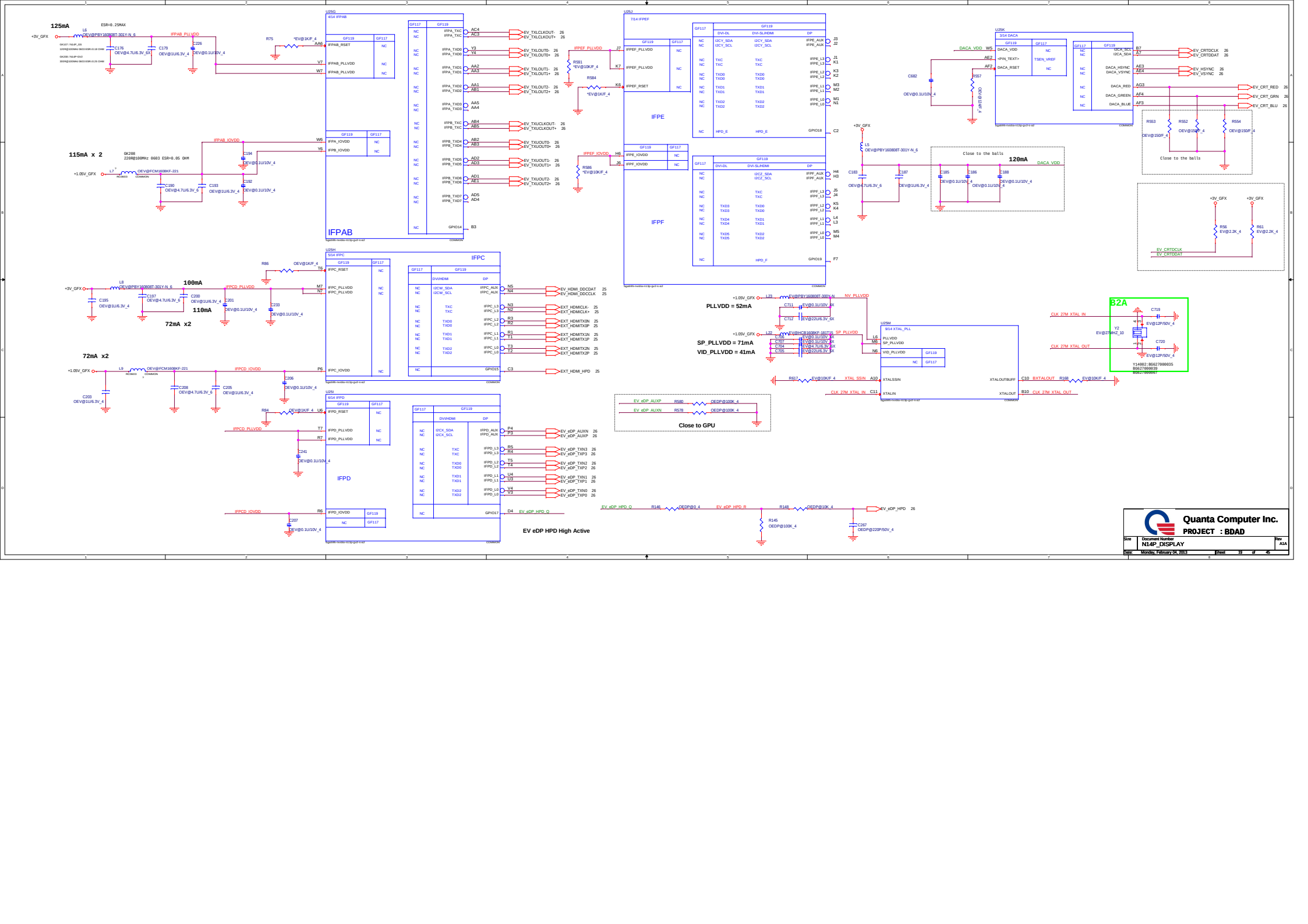
125mA
ESR=0.25MAX
L6
OEV@PBY1608B8T-301Y-N_6
+3V_GFX
IFPAB_PLLVDD
C176
OEV@4.7U/6.3V_6X
C179
OEV@1U/6.3V_4
C226
OEV@0.1U/10V_4
R75
*EV@1K/F_4
U25G
4/14 IFPAB
IFPAB
IFPA_TXC
IFPA_TXD0
IFPA_TXD1
IFPA_TXD2
IFPA_TXD3
IFPB_TXC
IFPB_TXD4
IFPB_TXD5
IFPB_TXD6
IFPB_TXD7
GPIO14
IFPAB_RSET
IFPAB_PLLVDD
IFPA_IOVDD
IFPB_IOVDD
EV_TXLCLKOUT-
EV_TXLCLKOUT+
EV_TXLOUT0-
EV_TXLOUT0+
EV_TXLOUT1-
EV_TXLOUT1+
EV_TXLOUT2-
EV_TXLOUT2+
EV_TXUCLKOUT-
EV_TXUCLKOUT+
EV_TXUOUT0-
EV_TXUOUT0+
EV_TXUOUT1-
EV_TXUOUT1+
EV_TXUOUT2-
EV_TXUOUT2+
IFPEF_PLLVDD
R591
*EV@10K/F_4
R584
*EV@1K/F_4
IFPEF_IOVDD
R586
*EV@10K/F_4
U25J
7/14 IFPEF
IFPE
IFPF
IFPE_PLLVDD
IFPEF_RSET
IFPE_IOVDD
IFPF_IOVDD
GPIO18
GPIO19
115mA x 2
GK288
220R@100MHz 0603 ESR=0.05 OHM
L7
C194
OEV@0.1U/10V_4
C190
OEV@4.7U/6.3V_6
C193
OEV@1U/6.3V_4
C192
OEV@0.1U/10V_4
U25K
3/14 DACA
DACA_VDD
DACA_RSET
DACA_RED
DACA_GREEN
DACA_BLUE
DACA_HSYNC
DACA_VSYNC
EV_CRTDCLK
EV_CRTDDAT
EV_CRT_RED
EV_CRT_GRN
EV_CRT_BLU
EV_HSYNC
EV_VSYNC
C682
OEV@0.1U/10V_4
R557
OEV@2K/F_4
R553
OEV@150F_4
R552
OEV@150F_4
R554
OEV@150F_4
Close to the balls
120mA
+3V_GFX
L5
OEV@PBY1608B8T-301Y-N_6
C183
OEV@4.7U/6.3V_6
C187
OEV@1U/6.3V_4
C185
OEV@0.1U/10V_4
C186
OEV@0.1U/10V_4
C188
OEV@0.1U/10V_4
R56
EV@2.2K_4
R61
EV@2.2K_4
EV_CRTDCLK
EV_CRTDDAT
U25H
5/14 IFPC
IFPC
IFPC_RSET
IFPC_PLLVDD
IFPC_AUX
IFPC_L3
IFPC_L2
IFPC_L1
IFPC_L0
IFPC_IOVDD
EV_HDMI_DDCDAT
EV_HDMI_DDCCLK
EXT_HDMICLK-
EXT_HDMICLK+
EXT_HDMITX0N
EXT_HDMITX0P
EXT_HDMITX1N
EXT_HDMITX1P
EXT_HDMITX2N
EXT_HDMITX2P
EXT_HDMI_HPD
100mA
110mA
72mA x2
L8
OEV@PBY1608B8T-301Y-N_6
C195
OEV@1U/6.3V_4
C197
OEV@4.7U/6.3V_6
C200
OEV@1U/6.3V_4
C201
OEV@0.1U/10V_4
C233
OEV@0.1U/10V_4
R86
OEV@1K/F_4
72mA x2
L9
OEV@FCM1608KF-221
C203
OEV@1U/6.3V_4
C208
OEV@4.7U/6.3V_6
C205
OEV@1U/6.3V_4
C206
OEV@0.1U/10V_4
U25I
8/14 IFPD
IFPD
IFPD_RSET
IFPD_PLLVDD
IFPD_AUX
IFPD_L3
IFPD_L2
IFPD_L1
IFPD_L0
IFPD_IOVDD
EV_eDP_AUXN
EV_eDP_AUXP
EV_eDP_TXN3
EV_eDP_TXP3
EV_eDP_TXN2
EV_eDP_TXP2
EV_eDP_TXN1
EV_eDP_TXP1
EV_eDP_TXN0
EV_eDP_TXP0
EV_eDP_HPD_O
R84
OEV@1K/F_4
C241
OEV@0.1U/10V_4
C207
OEV@0.1U/10V_4
EV eDP HPD High Active
+1.05V_GFX
PLLVDD = 52mA
SP_PLLVDD = 71mA
VID_PLLVDD = 41mA
L23
EV@PBY1608B8T-300Y-N
NV_PLLVDD
C711
EV@0.1U/10V_4X
C712
EV@22U/6.3V_6X
L22
EV@HCB1608KF-181T15_SP_PLLVDD
C701
C702
C704
C705
EV@0.1U/10V_4X
EV@4.7U/6.3V_6X
EV@22U/6.3V_6X
U25M
9/14 XTAL_PLL
PLLVDD
SP_PLLVDD
VID_PLLVDD
XTALSSIN
XTALIN
XTALOUTBUFF
XTALOUT
XTALSSIN
XTALIN
XTALOUTBUFF
XTALOUT
R617
EV@10K/F_4
C10
EXTALOUT
R168
EV@10K/F_4
B10
CLK_27M_XTAL_OUT
CLK_27M_XTAL_IN
B2A
C719
EV@12P/50V_4
Y2
EV@27MHZ_10
C720
EV@12P/50V_4
Y14602:B0627000035
B0627000039
B0627000057
EV_eDP_AUXP
EV_eDP_AUXN
R580
R578
OEDP@100K_4
Close to GPU
EV_eDP_HPD_O
R146
OEDP@0_4
EV_eDP_HPD_R
R148
OEDP@10K_4
EV_eDP_HPD
R145
OEDP@100K_4
C267
OEDP@220P/50V_4
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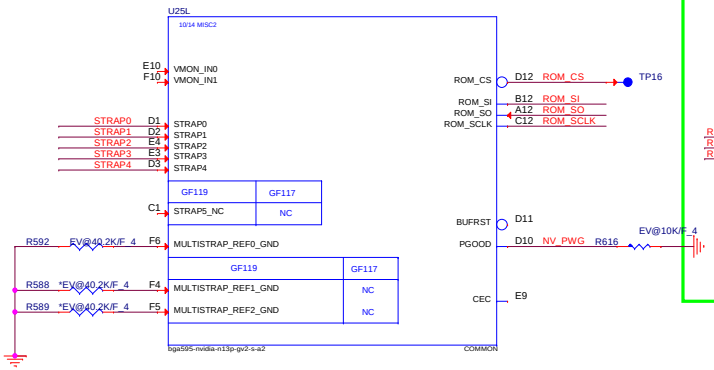
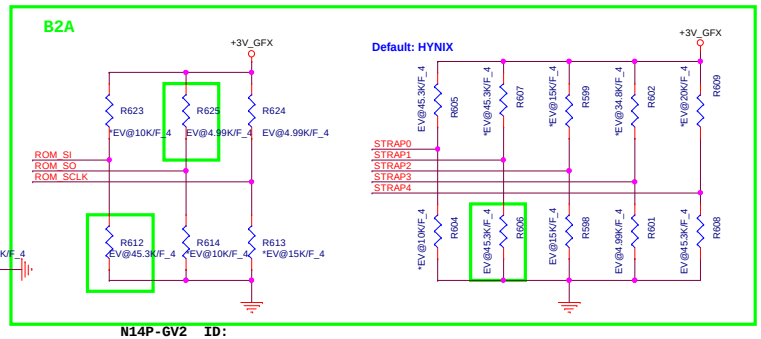
DDR3 Memory TYPE

Vendor	Vendor P/N	QCI P/N	Size	Max Speed CLK	ROM_SI
Samsung	K4W2G1646E-BC1A (128M*16) 0x7		2GB	1000MHZ	PD 45K
	K4W2G1646E-BC11 (128M*16) 0x7		2GB	900MHZ	PD 45K
	K4W4G1646B-HC11 (256M*16) 0x3		4GB	900MHZ	PD 20K
Micron	MT41J128M16JT-093G:K (128M*16) 0x5		2GB	1000MHZ	PD 30K
	MT41J128M16JT-107G:K (128M*16) 0x5		2GB	900MHZ	PD 30K
	MT41K256M16HA-107G:E (256M*16) 0x1		4GB	900MHZ	PD 10K
Hynix	H5TQ2G63DFR-N0C (128M*16) 0x6		2GB	1000MHZ	PD 35K
	H5TQ2G63DFR-11C (128M*16) 0x6		2GB	900MHZ	PD 35K

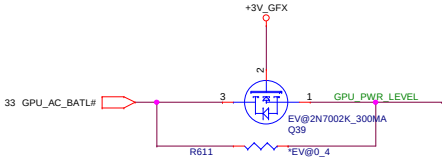
4.99K/F_4: CS24992FB26 RES CHIP 4.99K 1/16W +1%(0402)
10K/F_4: CS31002FB26 RES CHIP 10K 1/16W +1% (0402)
15K/F_4: CS31502FB24 RES CHIP 15K 1/16W +1% (0402)
20K/F_4: CS32002FB29 RES CHIP 20K 1/16W +-1%(0402)
30.1K/F_4: CS33012FB18 RES CHIP 30.1K 1/16W +-1%(0402)
34.8K/F_4: CS33482FB22 RES CHIP 34.8K 1/16W +-1% (0402)
45.3K/F_4: CS34532FB18 RES CHIP 45.3K 1/16W +-1% (0402)

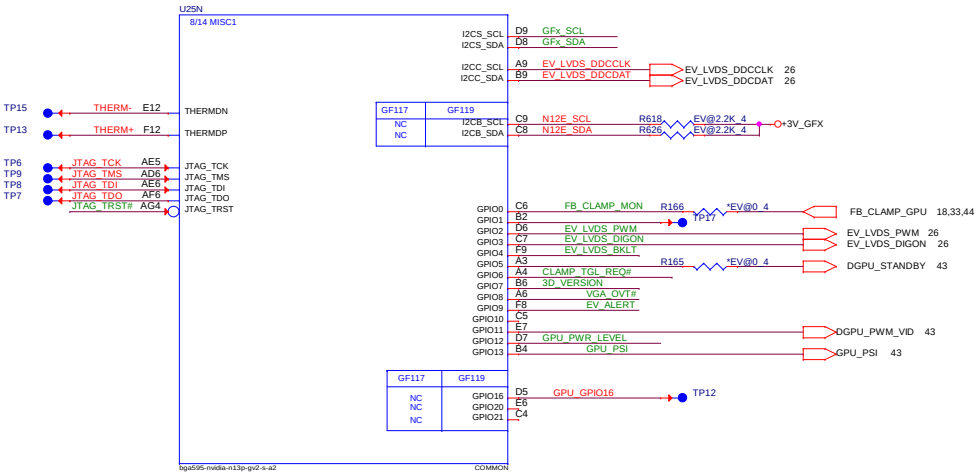


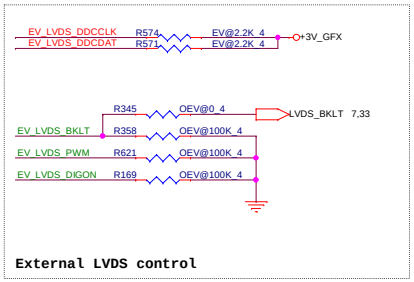


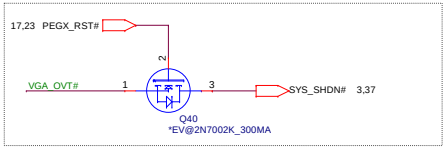
N14P-GV2 ID:

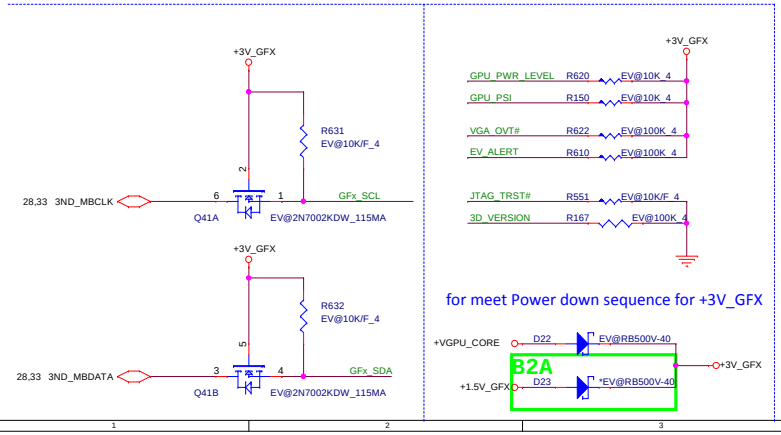
Netname	N14P-GV2	
ROM_SO	10K PU	5kohm PU for Optimus, 10K PU for Discrete
ROM_SCLK	5K PU	0x1000,0x8, 4.99kohm pull up
STRAP0	45K PU	user strap, 0xF, 45Kohm pull up
STRAP1	5K PD	5K PD for QS, 45K PD for after QS
STRAP2	15K PD	Device_ID, 0x0010_15K pull down
STRAP3	5K PD	0x0 for optimus, 5k PD. 0010 for DIscrete, 15K PD
STRAP4	45K PD	0x111, 45kohm pull down

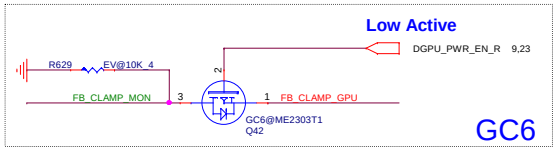


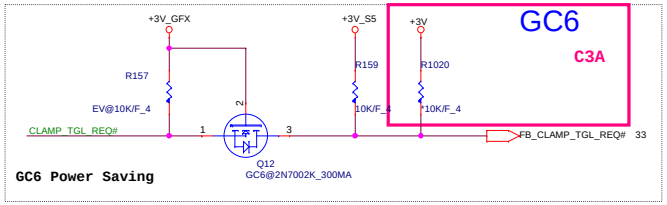












GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	OUT	GPU_VID4	GPU CORE_VDD VID4
1	OUT	GPU_VID3	GPU CORE_VDD VID3
2	OUT	LCD_BL_PWM	LCD BACKLIGHT PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	GPU_VID1	GPU CORE_VDD VID1
6	OUT	GPU_VID2	GPU CORE_VDD VID2
7	OUT	3D VISION	3D VISION LEFT/RIGHT VISION
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM VREF	MEMMORY VREF CONTROL
11	OUT	GPU_VID0	GPU CORE_VDD VID0
12	IN	PWR_LEVEL	Power Detect ,HIGH=AC, LOW=DC
13	OUT	GPU_VID5	GPU CORE_VDD VID5
14	IN	HPD_AB	HOT PLUG DETECT FOR IFPAB
15	IN	HPD_C	HOT PLUG DETECT FOR IFPC
16	OUT	MEM VDD	MEMMORY VDD CONTROL
17	IN	HPD_D	HOT PLUG DETECT FOR IFPD
18	IN	HPD_E	HOT PLUG DETECT FOR IFPE
19	IN	HPD_F	HOT PLUG DETECT FOR IFPF
20/21		RESERVE	

Quanta Computer Inc.
PROJECT : BDAD

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	N14P_GPIO	A1A

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RANK 0

900MHz VRAM size:
Samsung 128Mx16, P/N = AKD5MGWT500
Hynix 128Mx16, P/N = AKD5MGWTW16

18,22 FBA_CMD[0..30]
18,22 VMA_DQ[63..0]
18,22 VMA_DM[7..0]
18,22 VMA_WDQS[7..0]
18,22 VMA_RDQS[7..0]

VRAM8 / VRAM7 / VRAM6 / VRAM5

96-BALL SDRAM DDR3
VRAM _DDR3_HYNIX_128MX16

Should be 240 Ohms +-1%
R640 EV@243/F_4
R619 EV@243/F_4
R569 EV@243/F_4
R73 EV@243/F_4

R615 EV@162/F_4
R127 EV@1.33K/F_4
R131 EV@1.33K/F_4
C245 EV@0.1U/10V_4
R130 EV@1.33K/F_4
R135 EV@1.33K/F_4
C253 EV@0.1U/10V_4
R548 EV@162/F_4
R510 EV@1.33K/F_4
R505 EV@1.33K/F_4
C610 EV@0.1U/10V_4X
R511 EV@1.33K/F_4
R504 EV@1.33K/F_4
C605 EV@0.1U/10V_4

B2A

C606 C670 C623 C671 EV@1U/6.3V_4 / EV@1U/6.3V_4X
C714 C728 C751 C753 C743 C692 EV@10U/6.3V_6 / EV@1U/6.3V_4 / EV@1U/6.3V_4X
C726 C699 C690 C678 C710 C708 C718 C721 EV@10U/6.3V_6 / EV@1U/6.3V_4
C679 C730 C715 C611 C697 C607 C729 EV@10U/6.3V_6 / EV@0.1U/10V_4 / EV@0.1U/10V_4X
C614 C742 C696 C709 C752 EV@10U/6.3V_6 / EV@10U/6.3V_6X / EV@0.1U/10V_4

Quanta Computer Inc.
PROJECT : BDAD

Size	Document Number	Rev
	N14P_VRAM RANK0	A1A
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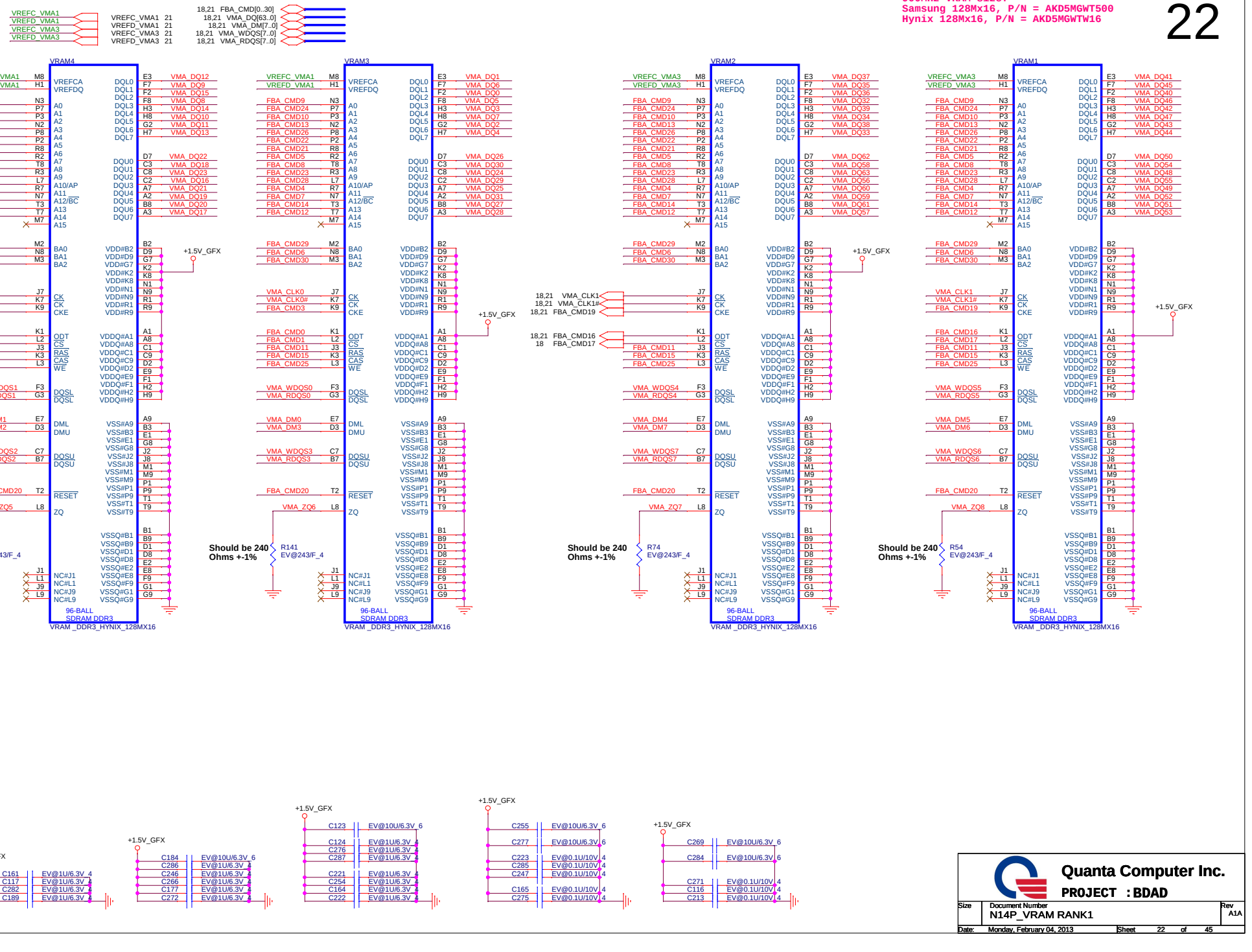
RANK 1

900MHz VRAM size:
Samsung 128Mx16, P/N = AKD5MGWT500
Hynix 128Mx16, P/N = AKD5MGWTW16



Quanta Computer Inc.
PROJECT : BDAD

Size	Document Number	Rev
	N14P_VRAM RANK1	A1A

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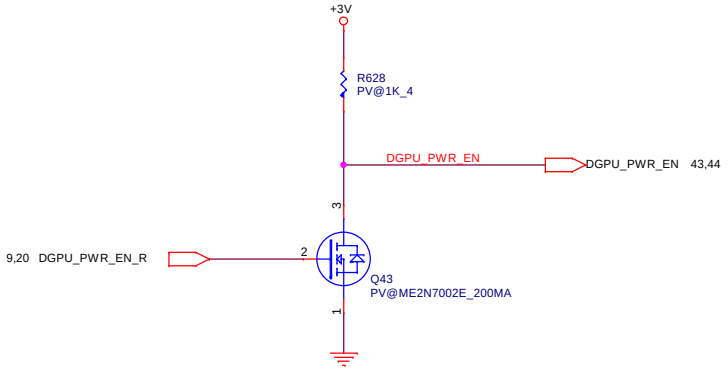
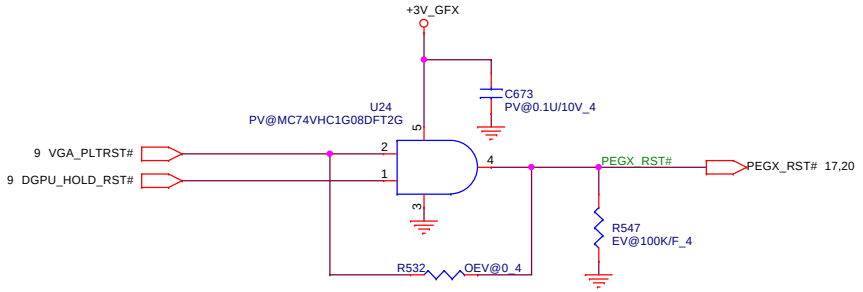
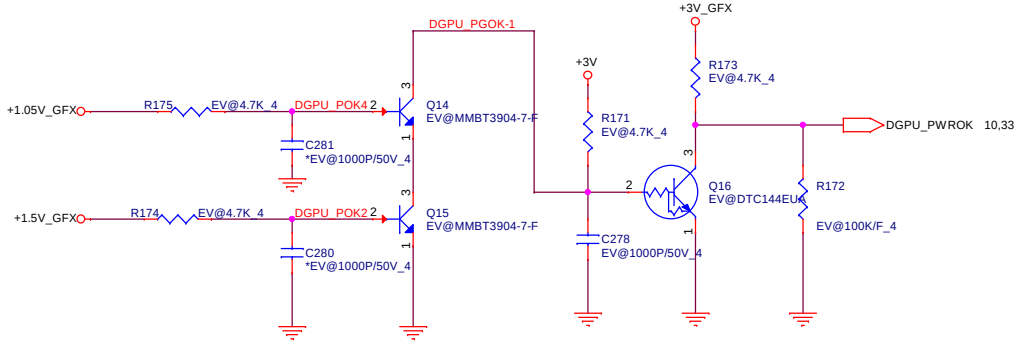
VGA Power Enable Reverse (Intel --> Low Active)



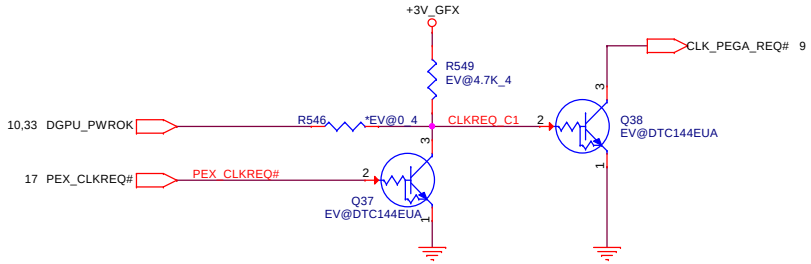
Platform Reset



GPU Power Good



GPU CLOCK REQ



Quanta Computer Inc.		
PROJECT : Chief River		
Size	Document Number: Blank	Rev: A1A
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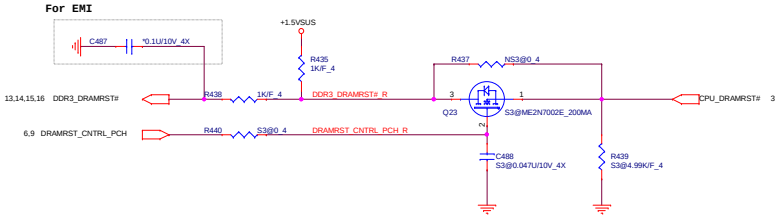
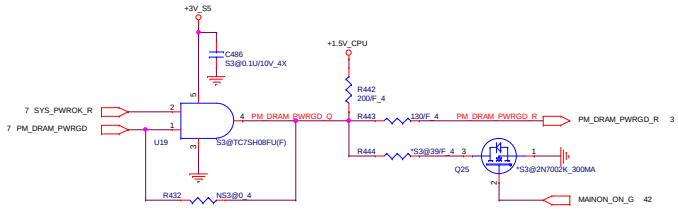
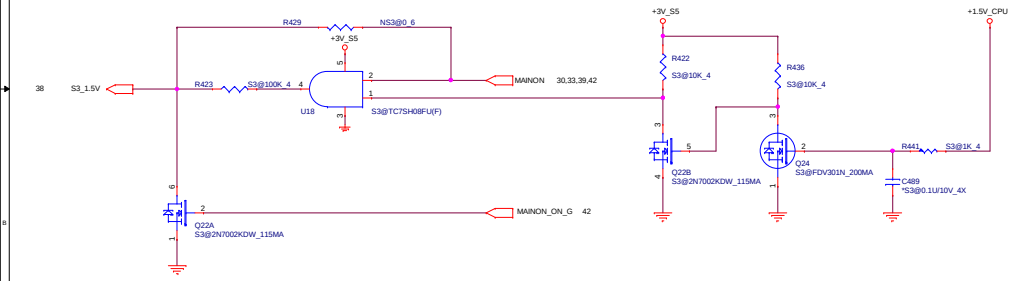
S3 power Reduction (SM_DRAMRST#) S3P/NS3P/CPU



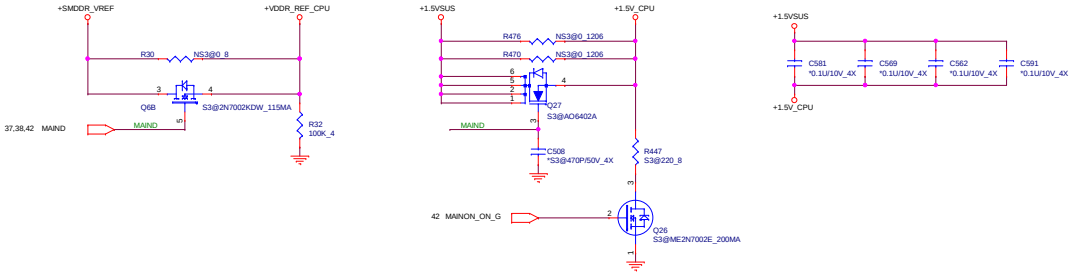
S3 power Reduction (SM_DRAMPWROK) S3P/NS3P/CPU



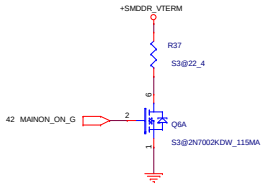
For S3 power Reduction Sequence S3P/NS3P/CPU



S3 power Reduction (CPU Power) S3P/NS3P/CPU



For S3 power Reduction VTT discharge S3P/NS3P/CPU

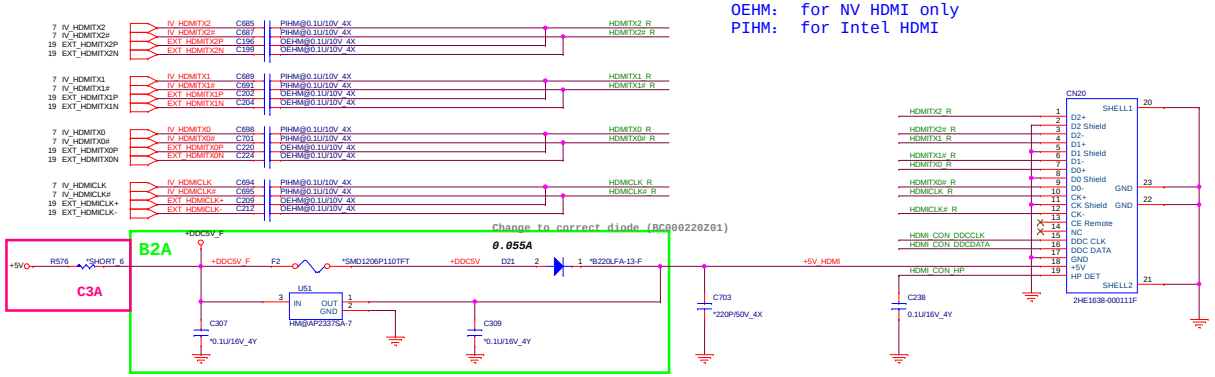


Quanta Computer Inc.
PROJECT : Chief River

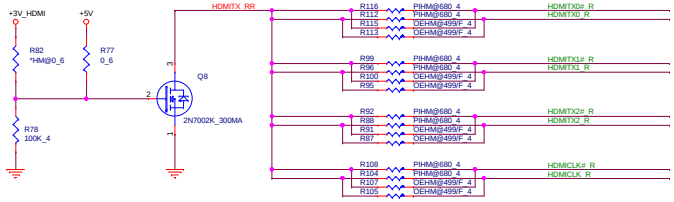
Size	Document Number	Rev
	S3 power Reduction	A1A
Date: Monday, February 04, 2013	Sheet 24 of 45	

HDMI Conn <HDM>

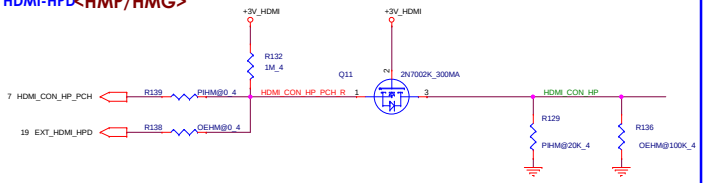
Notes:
PIHM 90ohm Intel HDMI output
OEHM 90ohm NV HDMI output
HM: for both Intel and NV HDMI
OEHM: for NV HDMI only
PIHM: for Intel HDMI



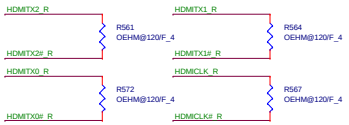
HDMI-passive level shift <HMP/HMG>



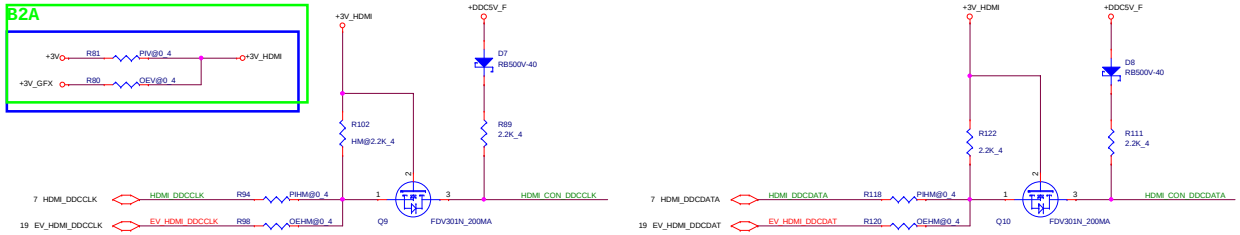
HDMI-HPD<HMP/HMG>



FOR EMI <EMC>



HDMI-SMBus <HDM>



Quanta Computer Inc.
PROJECT : BDAD

Size	Document Number	Rev
	HDMI CONN/CEC	1A

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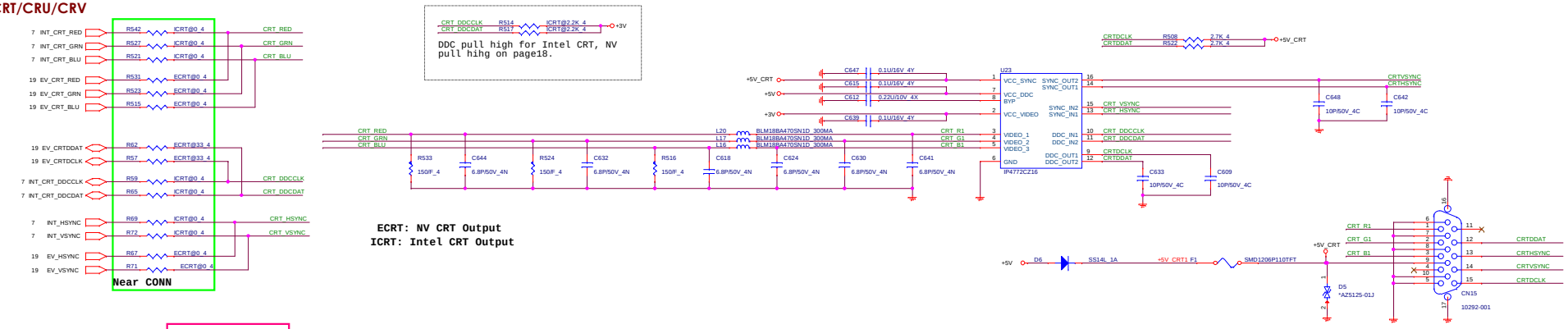
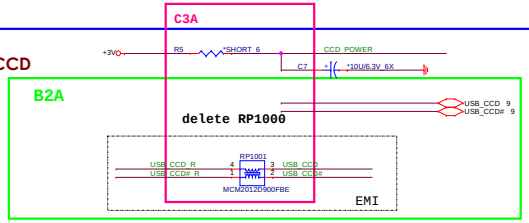
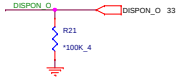
CRT CRT/CRU/CRV



CCD CCD

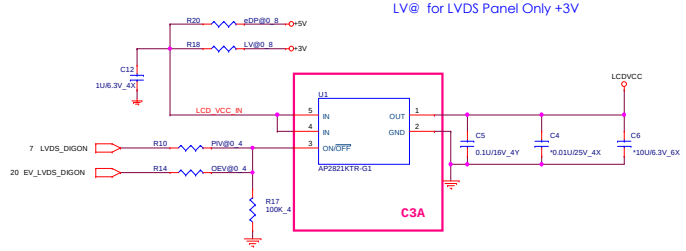


Panel backlight control LDS

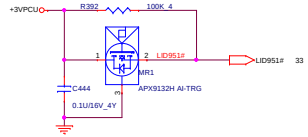


LCD POWER SWITCH LDS/LDU/LDV

eDP@ for eDP Panel Only +5V
LV@ for LVDS Panel Only +3V

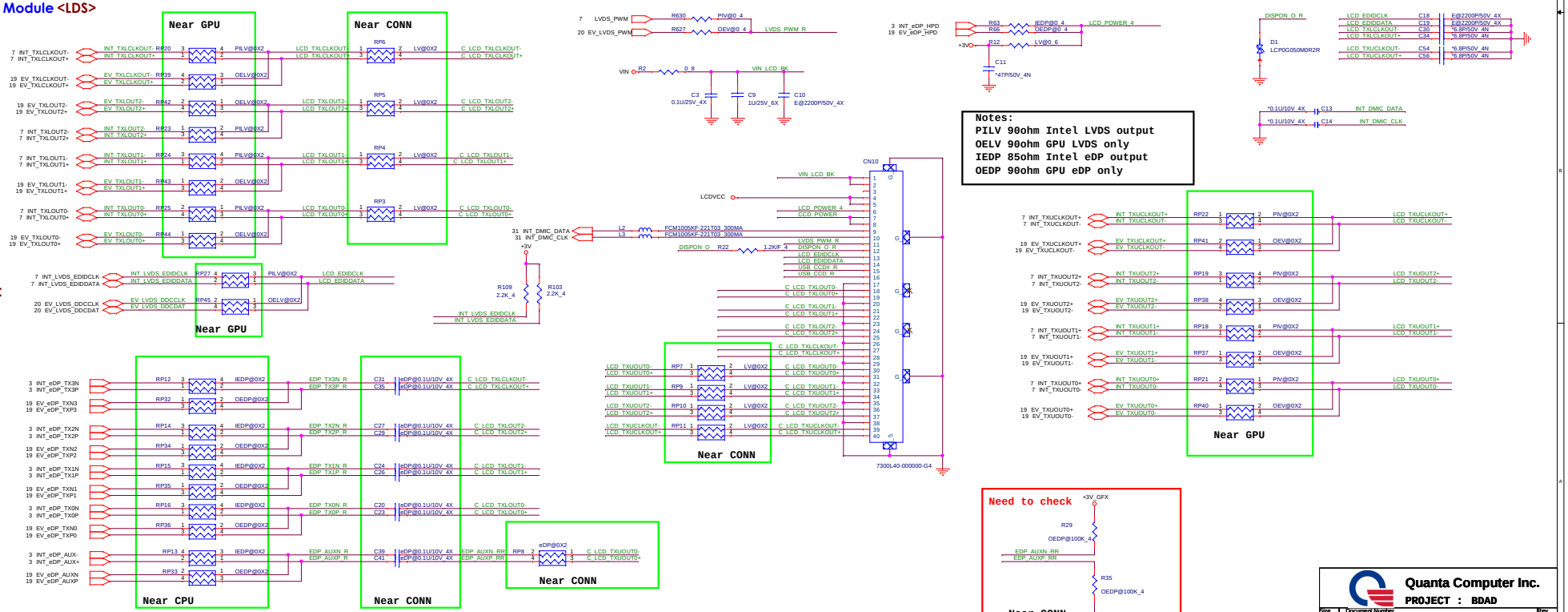


HALL Sensor HSR



LCD Panel Module <LDS>

LVDS
EDID DDC
eDP
Lane 3
Lane 2
Lane 1
Lane 0
AUX

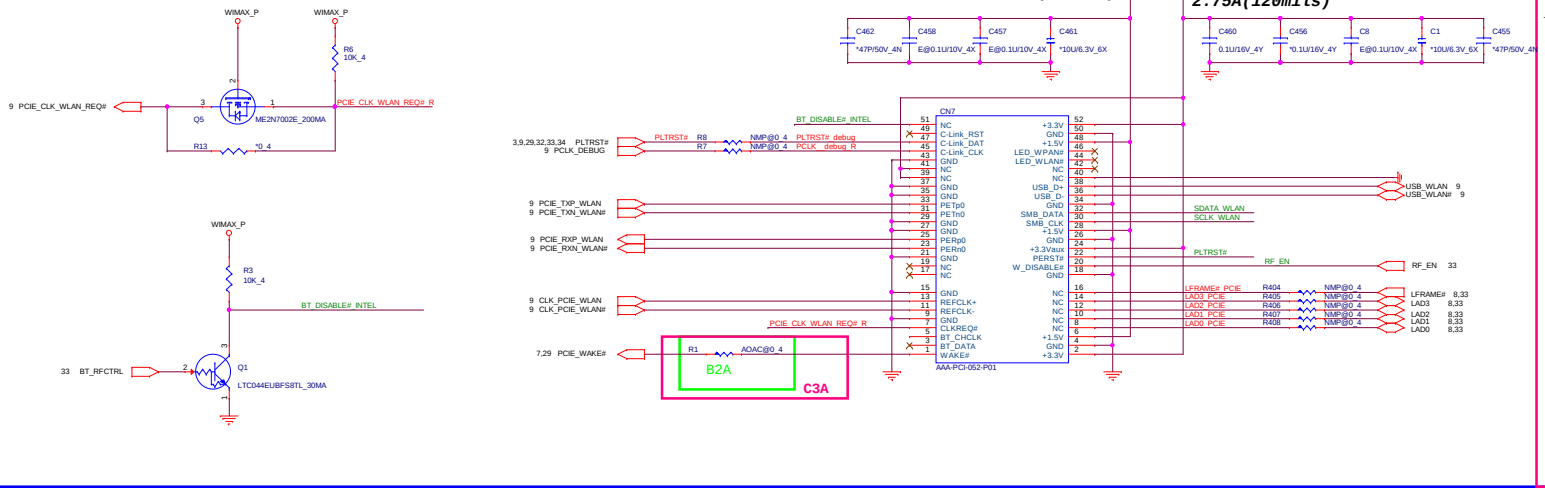


Need to check

Quanta Computer Inc.
PROJECT : BDAD
Size | Document Number: LCD/LED Panel/CCD | Rev: A1A
Date: Monday, February 04, 2013 | Sheet 26 of 45

MINI Card Slot#1(WiFi / Wimax / Combo)

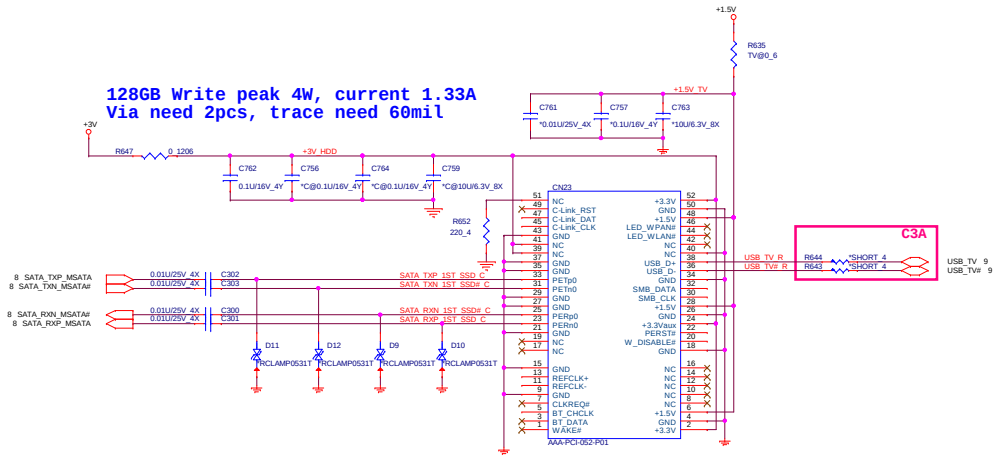
MNW/DEG



TV Tuner / MSATA

<SSD>

TV Tuner: 1.5V@240mA 3.3V@470mA



Quanta Computer Inc.		
PROJECT : BDAD		
Size	Document Number: MINI CARD(WLAN/3G/SIM Card)	Rev: A1A
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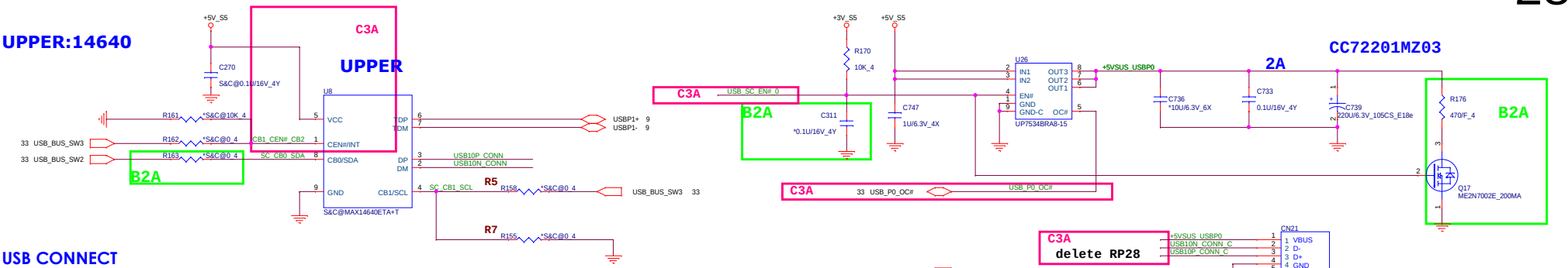
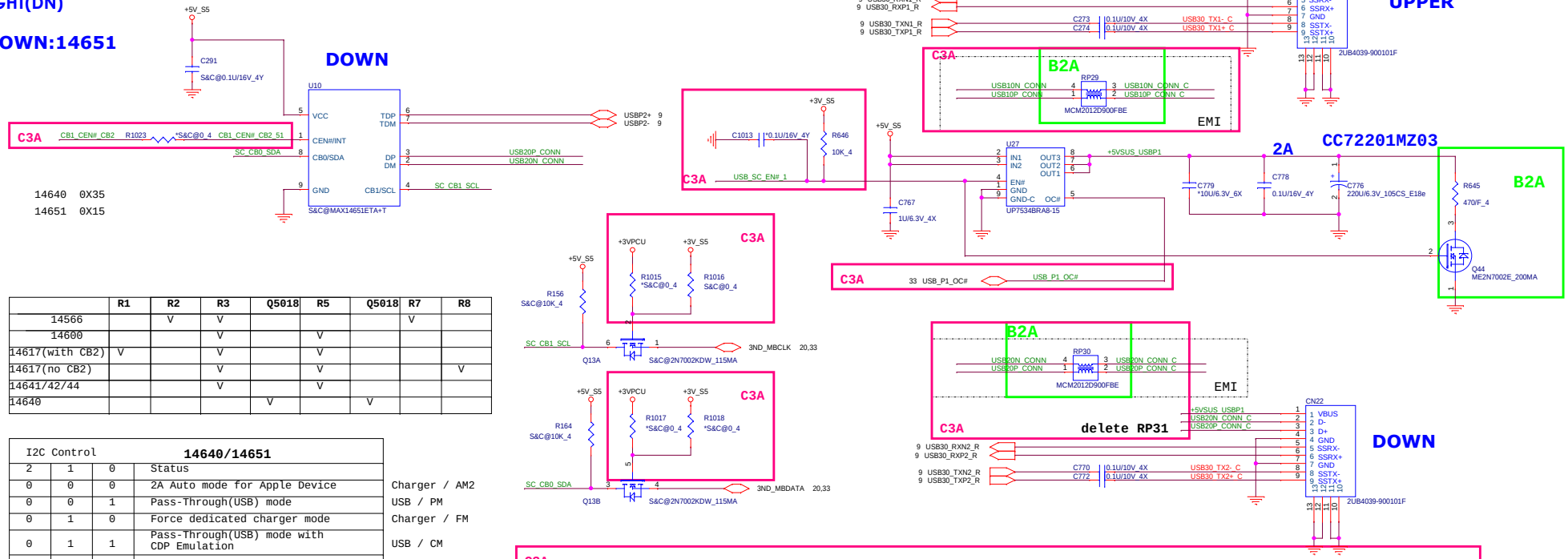
USB CONNECT RIGHT(UR) <U3B/USB>

UPPER:14640



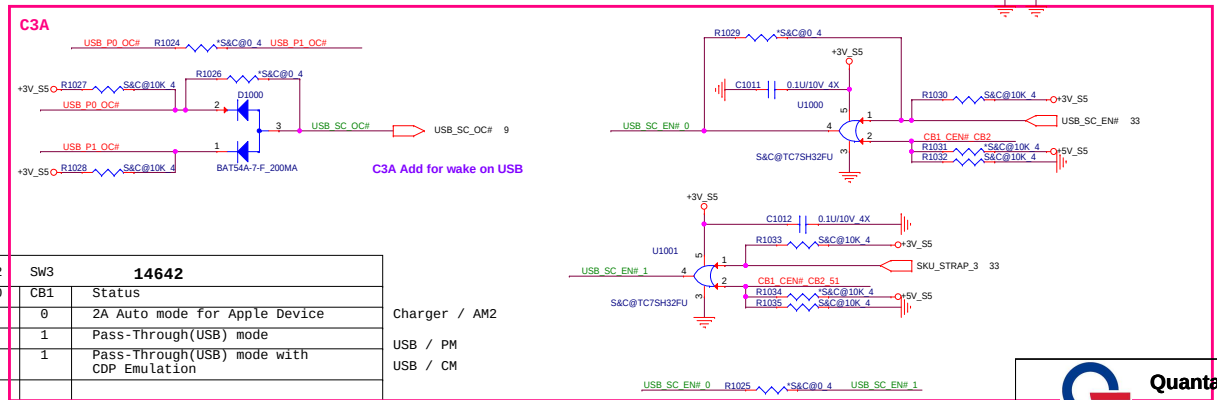
USB CONNECT RIGHT(DN)

DOWN:14651



	R1	R2	R3	Q5018	R5	Q5018	R7	R8
14566		V	V				V	
14600			V		V			
14617(with CB2)	V		V		V			
14617(no CB2)			V		V			V
14641/42/44			V		V			
14640				V		V		

I2C Control			14640/14651	
2	1	0	Status	
0	0	0	2A Auto mode for Apple Device	Charger / AM2
0	0	1	Pass-Through(USB) mode	USB / PM
0	1	0	Force dedicated charger mode	Charger / FM
0	1	1	Pass-Through(USB) mode with CDP Emulation	USB / CM
1	0	0	1A Auto mode for Apple Device	Charger / AM1
1	0	1	1A Forced mode for Apple Device	Charger / AP1
1	1	0	2A Forced mode for Apple Device	Charger / AP2
1	1	1	2A Forced mode for Samsung Device	Charger / SS



SW2	SW3	14644	
CB0	CB1	Status	
0	0	2A Auto mode for Apple Device	Charger / AM2
1	0	Force dedicated charger mode	Charger / FM
0	1	Pass-Through(USB) mode	USB / PM
1	1	Pass-Through(USB) mode with CDP Emulation	USB / CM

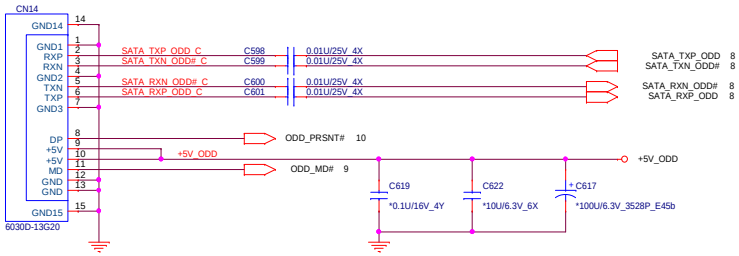
SW2	SW3	14642	
CB0	CB1	Status	
X	0	2A Auto mode for Apple Device	Charger / AM2
0	1	Pass-Through(USB) mode	USB / PM
1	1	Pass-Through(USB) mode with CDP Emulation	USB / CM

Quanta Computer Inc.
PROJECT : BDAD

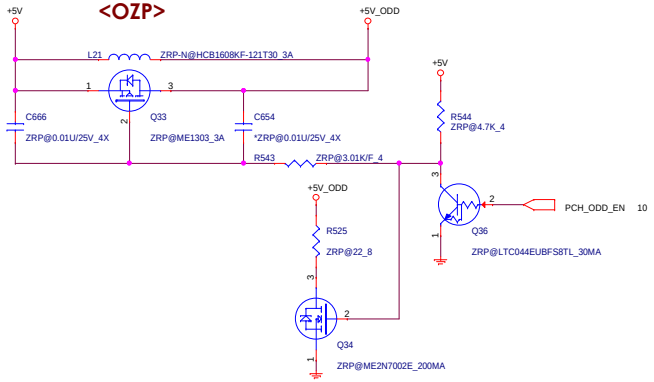
Size	Document Number	Rev
	USB3 Redriver/S&C/USB2	A1A
Date: Monday, February 04, 2013	Sheet 28 of 45	

SATA ODD <ODD>

ODD Zero power .
(Only for Intel)

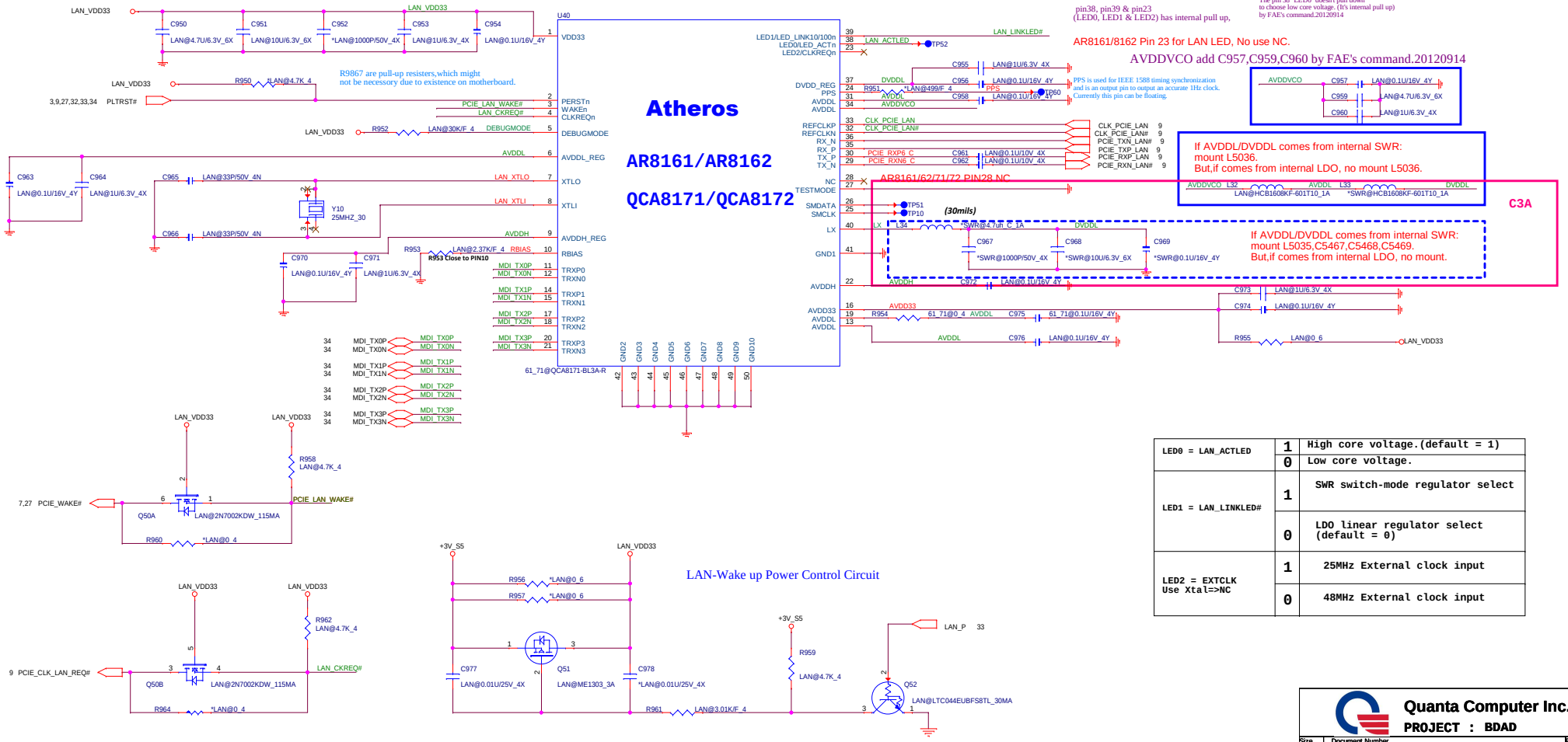


<OZP>



AR8161-BL3A-RL = AL008161003

277mA(30mils)



LED0 = LAN_ACTLED	1	High core voltage.(default = 1)
	0	Low core voltage.
LED1 = LAN_LINKLED#	1	SWR switch-mode regulator select
	0	LDO linear regulator select (default = 0)
LED2 = EXTCLK Use Xtal=>NC	1	25MHz External clock input
	0	48MHz External clock input

Quanta Computer Inc.
PROJECT : BDAD

Size	Document Number	Rev
	USB3 Redriver/USB2_Left	A1A
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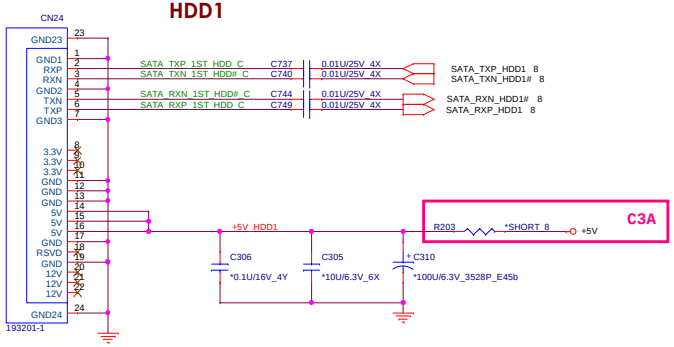
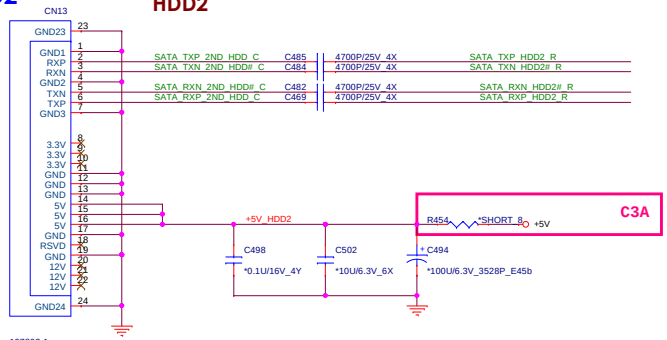
SATA HDD1

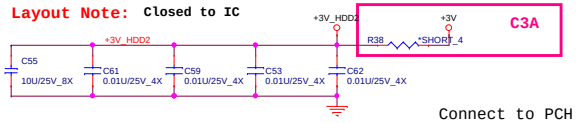


SATA HDD2



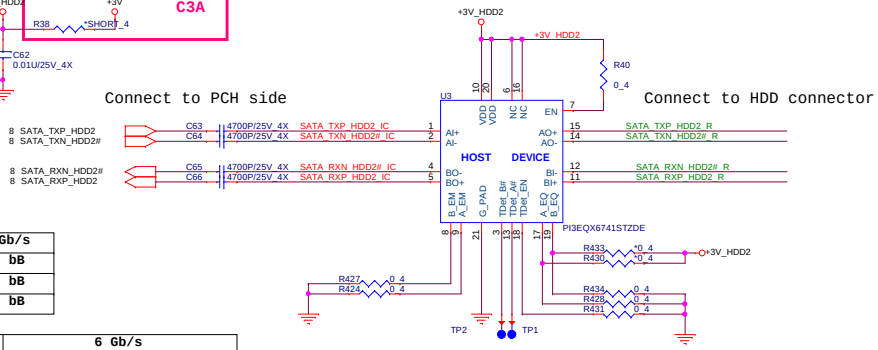
2nd HDD SATA Re-driver

Layout Note: Closed to IC



Connect to PCH side

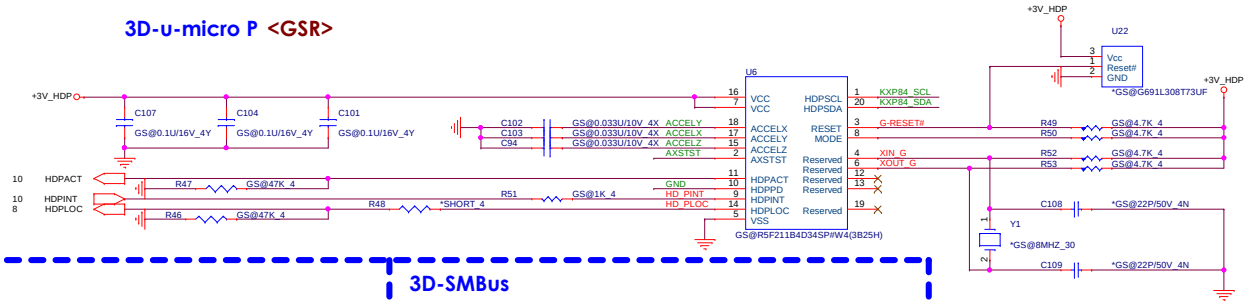
Connect to HDD connector



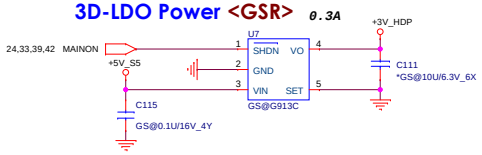
A_EQ	B_EQ	1.5 Gb/s	3 Gb/s	6 Gb/s
0	0	1 bB	2.5 bB	3 bB
1	1	4 bB	7.5 bB	9 bB
floating		2.5 bB	5 bB	6 bB

A_EM	B_EM	3 Gb/s	6 Gb/s
0	0	550mV pp	650mV pp
1	1	550mV pp+3dB Pre-emphasis	650mV pp+1.5dB Pre-emphasis

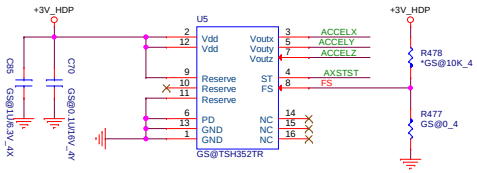
3D-u-micro P <GSR>



3D-LDO Power <GSR> 0.3A



3D-Sensor IC <GSR>



FS (Full Scale) selection

FS	0	1
	2g Full-Scale	6g Full-Scale

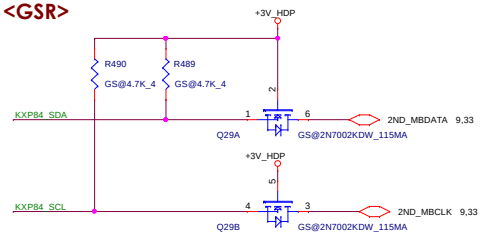
PD (Power Down) selection

PD	0	1
	Normal Mode	Power-down mode

HDPPD selection

HDPPD	0	1
	Normal Mode	Power-down mode

3D-SMBus <GSR>



Quanta Computer Inc.

PROJECT : BDAD

Size	Document Number	Rev
	HDD/ODD/G-Sensor	A1A

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Codec (CX20755-11Z) <ADO>

47.1+48.1mA(20mils)
0.156mA(15mils)
20.8mA(20mils)
1A(100mils)
(40mils)
Close to pin13, 16

From EC
33 AMP_MUTE#
33 S&M_EN
High Active

Need to connect ADOGND to system GND under codec using copper trace about 200mils wide.

Twitter SPK

C3A
FAE suggestion_0924
Close to IC 40mil
Close to IC
10/22

Output Gain Table

G1	G2	Gain
0	0	11dB
0	1	14dB
1	0	19dB
1	1	25dB

dB value follow FAE suggestion 09/17

External MIC <ADO> <EMC>

Normal Open Jack
To EC High Active
33 SENSE_MIC_IN

Headphone <ADO>

B2A
Normal Open Jack

4 Speakers <ADO>

EXT:105_SPK
INT:SPK
Close to Connector
B2A EMI
B2A EMI
For EMI reserve, close to connector
B2A EMI

Quanta Computer Inc.
PROJECT : BDAD
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Document Number
Audio Codec (CX20755)
Rev LA
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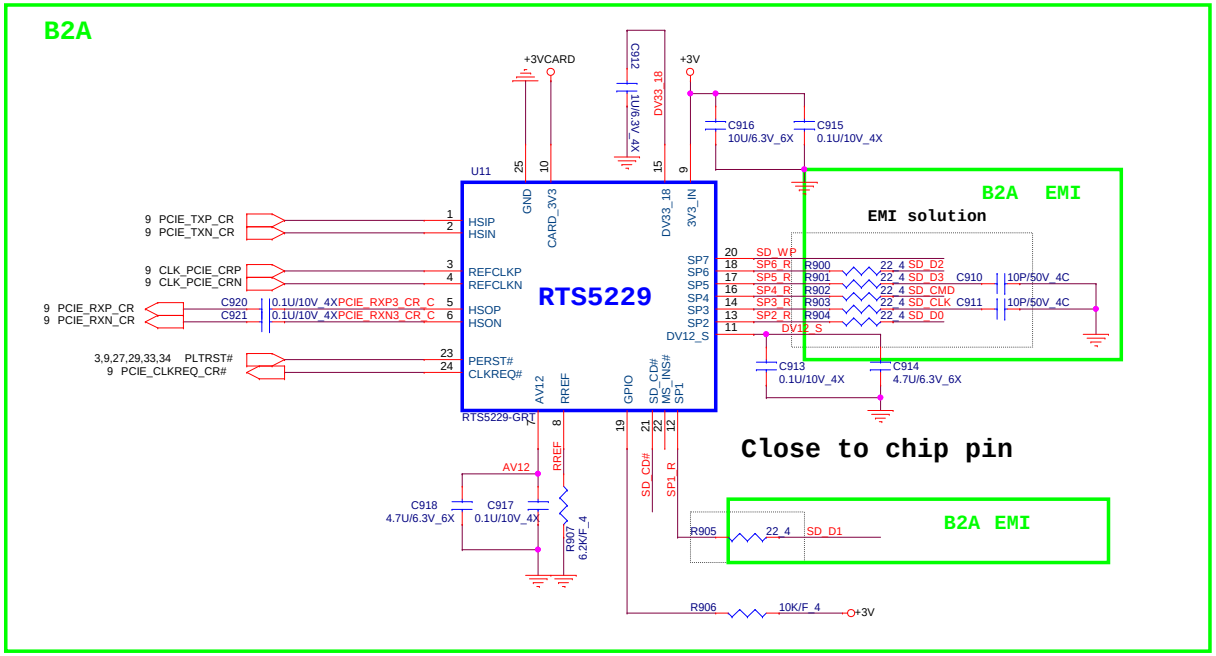
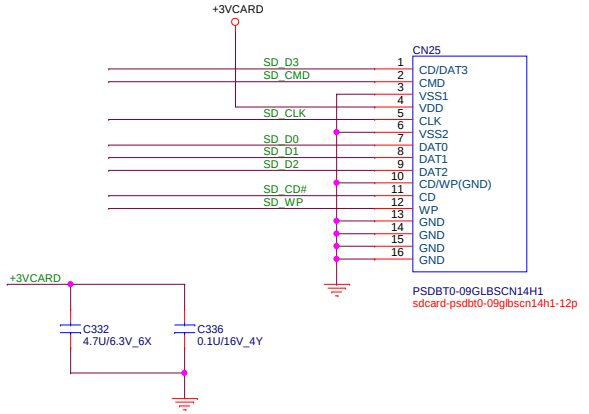
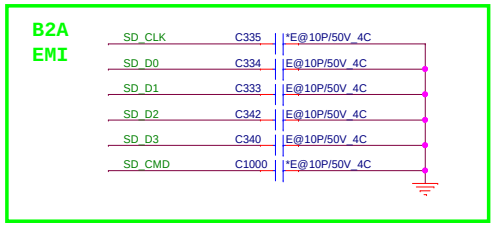
Card Reader (RTS5229) <MMC>



2 IN 1 Card Reader <MMC>

32





Quanta Computer Inc.

PROJECT : BDAD

Size	Document Number	Rev
	Card Reader(GL834L)	A1A

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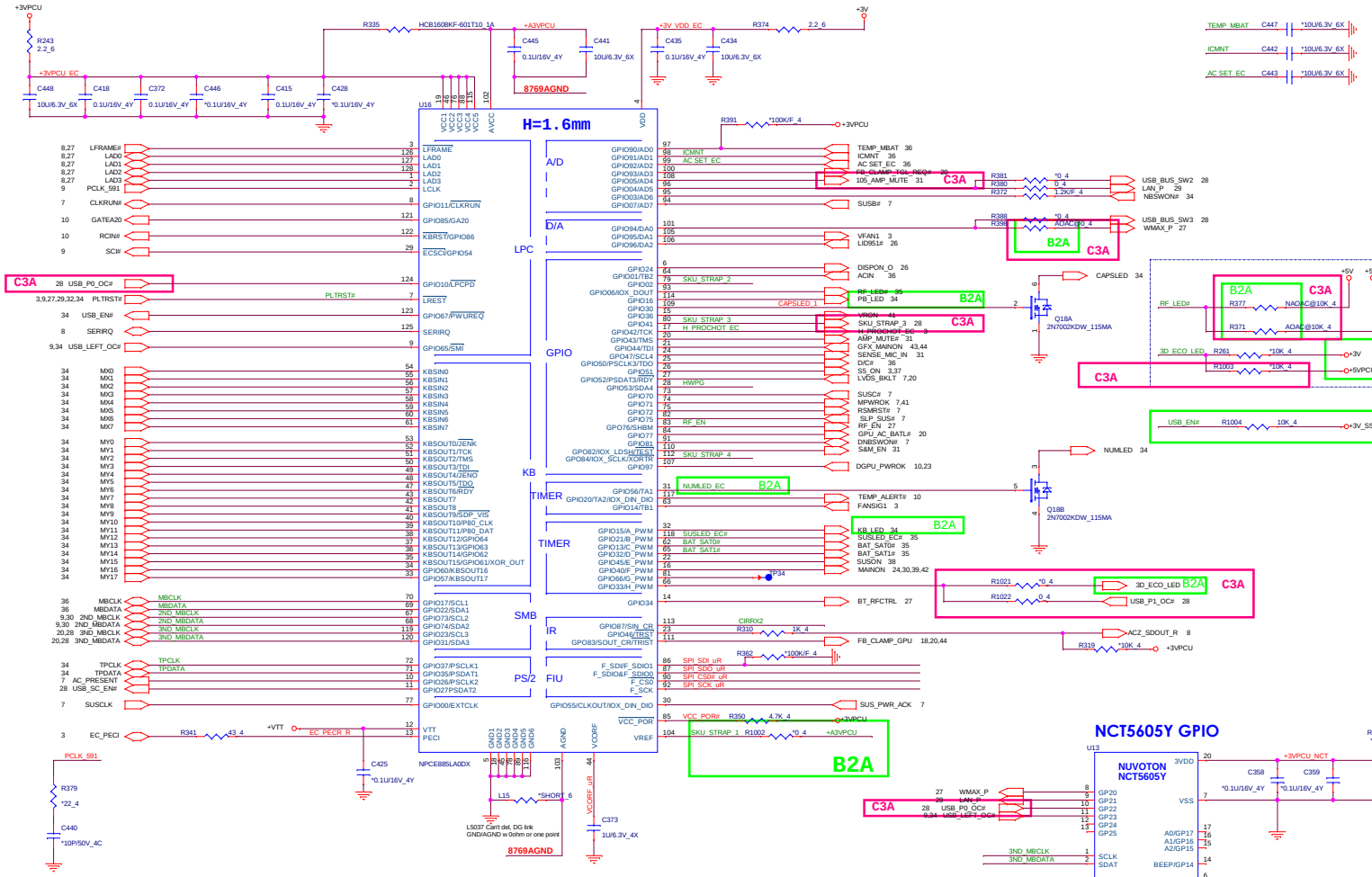
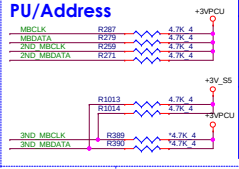
EC<KBC>



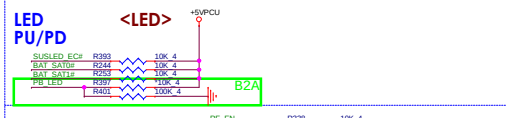
SM BUS PU/Address <KBC>



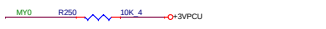
SMBUS	Devices	Address
1	Battery(A)	
2	PCH(S5)	
	G-sensor(S0)	
	CPU Thermal(A)	98H
	IDROM(A)	
3	VGA Thermal(A or S0)	98H
	CEC(A)	
	MMB(A)	

TP <KBC>

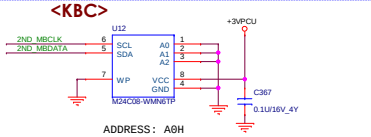
LED PU/PD <LED>



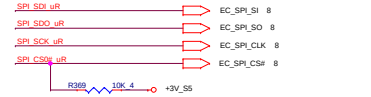
INTERNAL KEYBOARD STRIP SET <KBC>



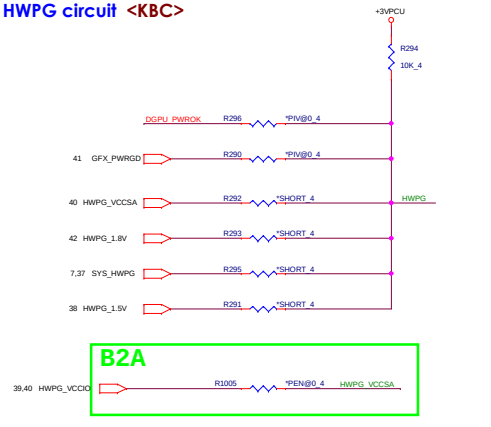
ID EEPROM <KBC>



SPI FLASH <KBC>



HWPG circuit <KBC>

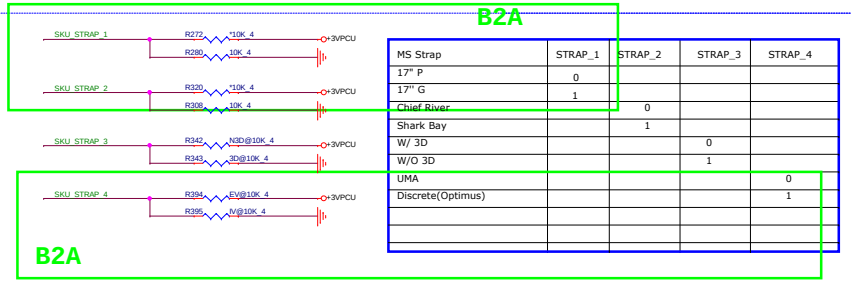


NCT5605Y GPIO

Power Button <KBC>

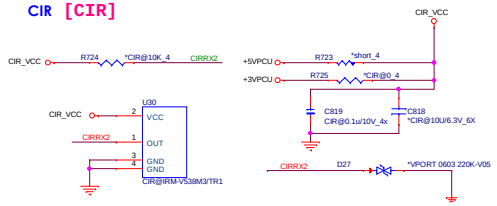
Place on easy use location

B2A



MS Strap	STRAP_1	STRAP_2	STRAP_3	STRAP_4
17" P	0			
17" G	1			
Chief River		0		
Shark Bay		1		
W/ 3D			0	
W/O 3D			1	
UMA				0
Discrete(Optimus)				1

CIR [CIR]



Quanta Computer Inc.
PROJECT : BDAD

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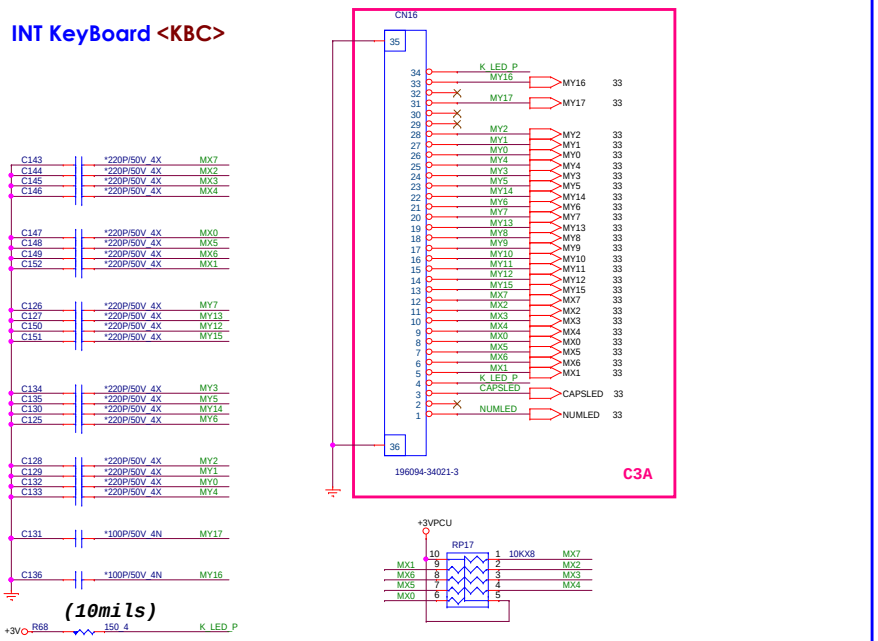
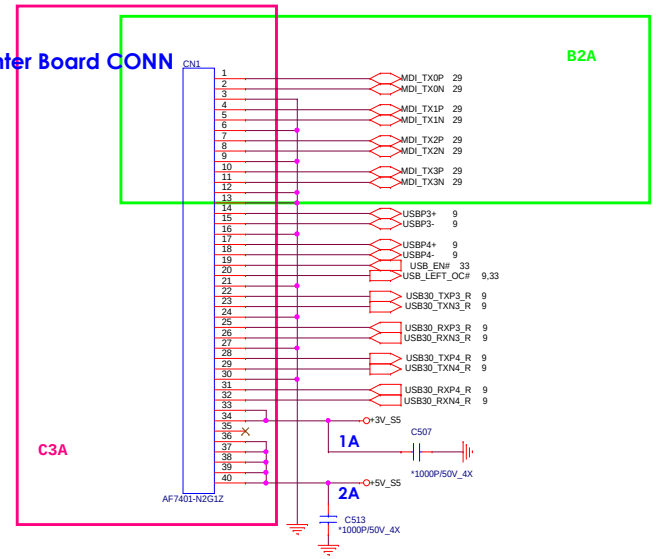
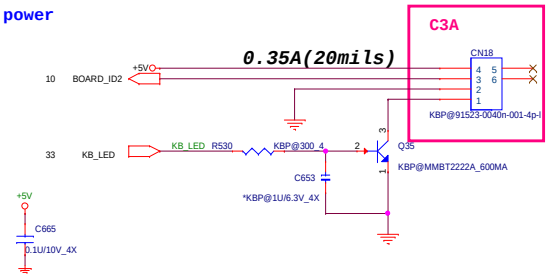
INT KeyBoard <KBC>



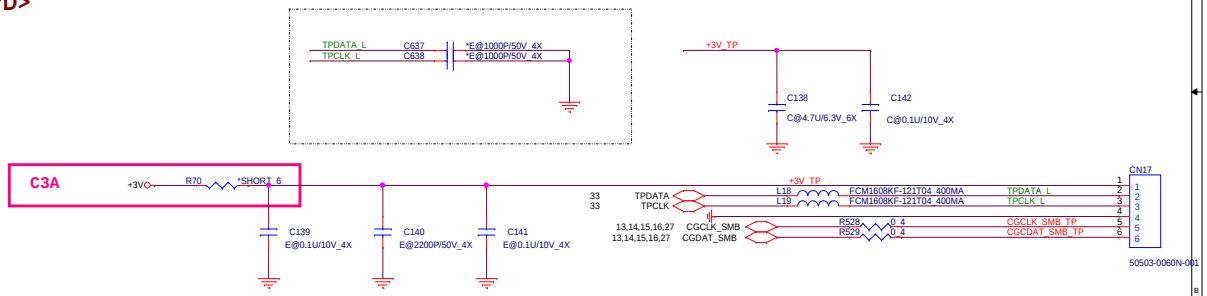
Daughter Board CONN



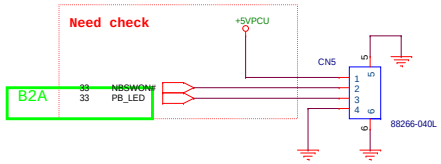
K/B LED power <KBP>



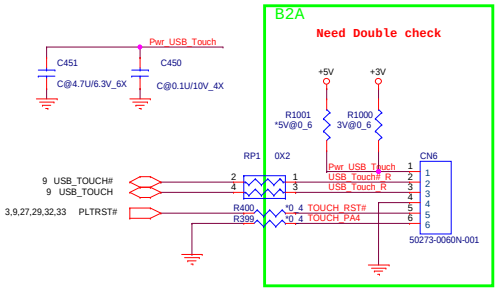
TP board <TPD>



Power board w LED <PSW>



TOUCH PANEL <TPP>



Quanta Computer Inc.		
PROJECT : BDAD		
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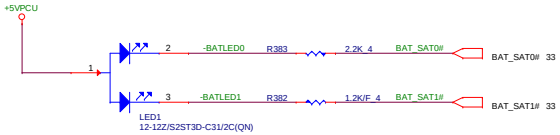
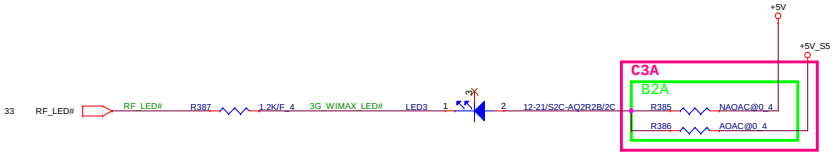
LED LED

BATERRY

BEW00011ZA0



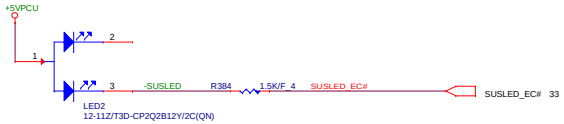
RF LED LED



POWER LED

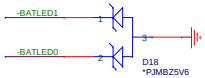
BEWH0139Z00

S0 Mode = Whilte ON
S3 Mode = Whilte BLINK

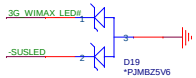


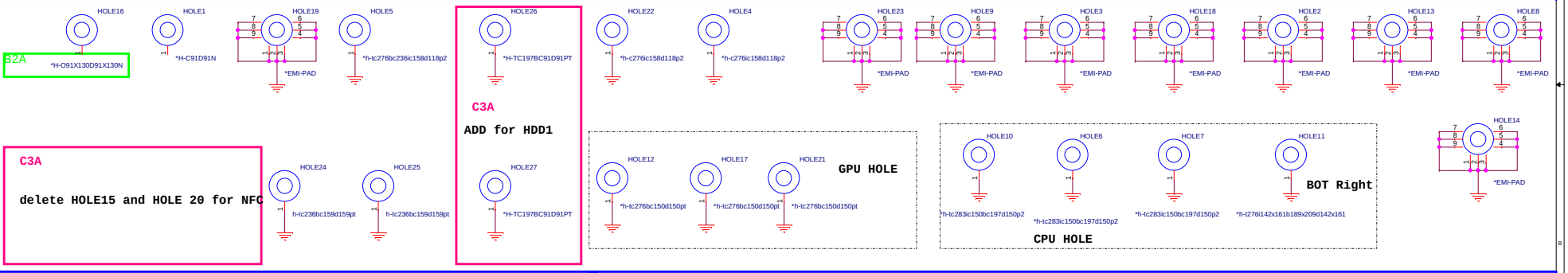
ESD Protect LED

FOR BATTERY LED

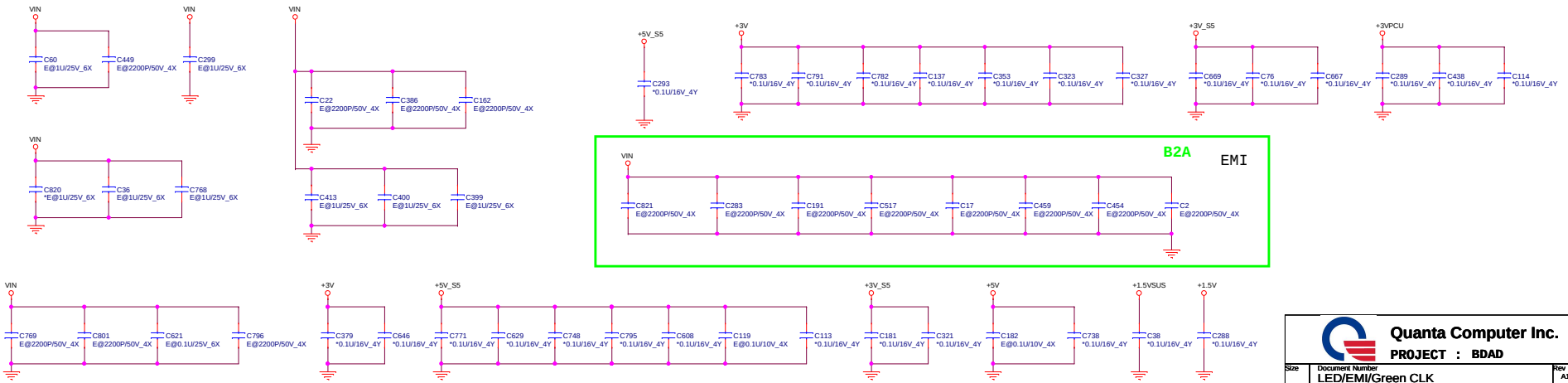


FOR W-LAN&POWER LED





EMI EMI



Quanta Computer Inc.
PROJECT : BDAD

Size	Document Number	Rev
	LED/EMI/Green CLK	A1A

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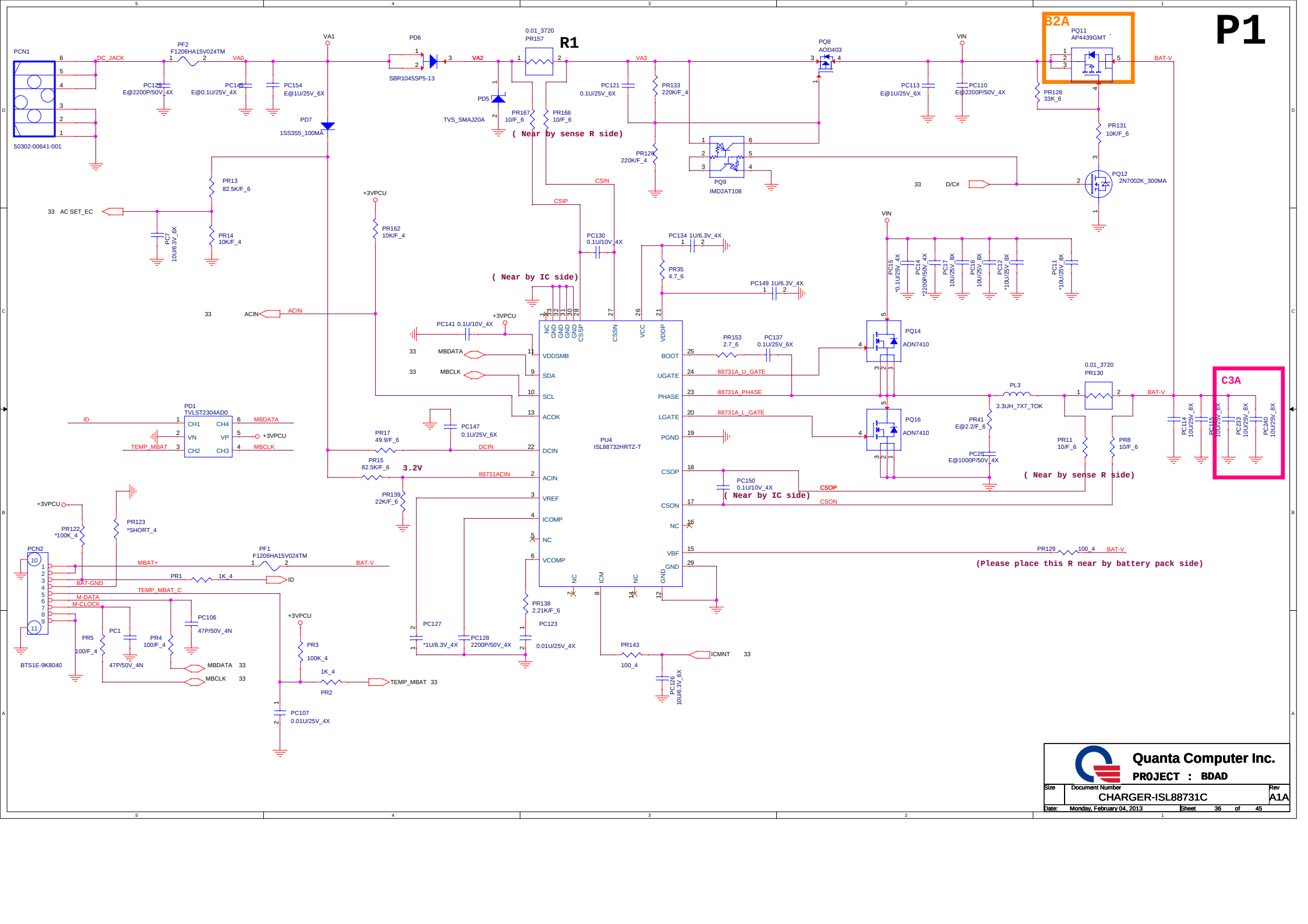
P1
B2A
C3A
R1
PCN1
50302-00641-001
DC_JACK
PF2
F1206HA15V024TM
VA0
VA1
PD6
SBR1045SP5-13
VA2
0.01_3720
PR157
PD5
TVS_SMAJ20A
PR167
10/F_6
PR166
10/F_6
(Near by sense R side)
VA3
PC121
0.1U/25V_6X
PR133
220K/F_4
PR128
220K/F_4
PQ8
AOD403
PQ9
IMD2AT108
VIN
PC113
E@1U/25V_6X
PC110
E@2200P/50V_4X
PQ11
AP4439GMT
BAT-V
PR128
33K_6
PR131
10K/F_6
PQ12
2N7002K_300MA
33 D/C#
PC129
E@2200P/50V_4X
PC145
E@0.1U/25V_4X
PC154
E@1U/25V_6X
PD7
1SS355_100MA
PR13
82.5K/F_6
33 AC SET_EC
PC7
10U/6.3V_6X
PR14
10K/F_4
+3VPCU
PR162
10K/F_4
CSIN
CSIP
PC130
0.1U/10V_4X
(Near by IC side)
PC134 1U/6.3V_4X
PR35
4.7_6
PC149 1U/6.3V_4X
33 ACIN
ACIN
PC141 0.1U/10V_4X
+3VPCU
33 MBDATA
33 MBCLK
PU4
ISL88732HRTZ-T
NC
GND
GND
GND
GND
CSSP
CSSN
VCC
VDDP
VDDSMB
SDA
SCL
ACOK
DCIN
ACIN
VREF
ICOMP
NC
VCOMP
BOOT
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC
VBF
GND
PR153
2.7_6
PC137
0.1U/25V_6X
88731A_U_GATE
88731A_PHASE
88731A_L_GATE
PQ14
AON7410
PQ16
AON7410
PL3
3.3UH_7X7_TOK
0.01_3720
PR130
PR41
E@2.2/F_6
PC25
E@1000P/50V_4X
PR11
10/F_6
PR8
10/F_6
(Near by sense R side)
PC15
*0.1U/25V_4X
PC14
*2200P/50V_4X
PC17
10U/25V_8X
PC16
10U/25V_8X
PC12
*10U/25V_8X
PC11
*10U/25V_8X
PC114
10U/25V_8X
PC115
10U/25V_8X
PC233
10U/25V_8X
PC240
10U/25V_8X
PD1
TVLST2304AD0
ID
TEMP_MBAT
CH1
CH2
CH3
CH4
VN
VP
MBDATA
+3VPCU
MBCLK
PR17
49.9/F_6
PC147
0.1U/25V_6X
DCIN
PR15
82.5K/F_6
3.2V
88731ACIN
PR139
22K/F_6
PC150
0.1U/10V_4X
(Near by IC side)
CSOP
CSON
PR129
100_4
BAT-V
(Please place this R near by battery pack side)
PR122
*100K_4
PR123
*SHORT_4
PCN2
MBAT+
BAT-GND
M-DATA
M-CLOCK
PF1
F1206HA15V024TM
PR1
1K_4
ID
TEMP_MBAT_C
BTS1E-9K8040
PC106
47P/50V_4N
PR5
100/F_4
PC1
47P/50V_4N
PR4
100/F_4
MBDATA 33
MBCLK 33
PR3
100K_4
1K_4
PR2
TEMP_MBAT 33
PC107
0.01U/25V_4X
PC127
*1U/6.3V_4X
PC128
2200P/50V_4X
PR138
2.21K/F_6
PC123
0.01U/25V_4X
PR143
100_4
ICMNT 33
PC126
10U/6.3V_6X
Quanta Computer Inc.
PROJECT : BDAD
Size
Document Number
CHARGER-ISL88731C
Rev
A1A
Date: Monday, February 04, 2013
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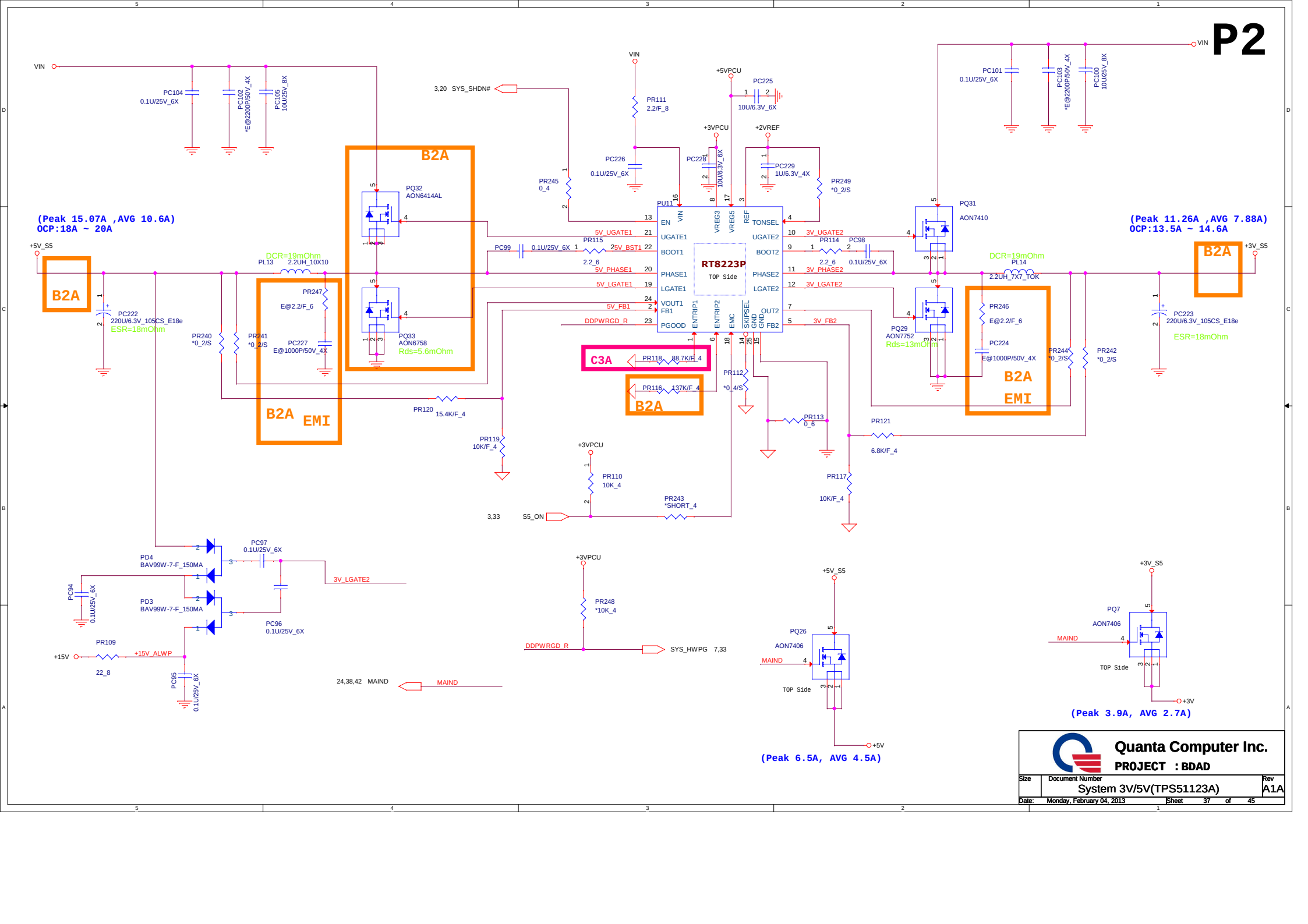
P2
VIN
PC104 0.1U/25V_6X
PC102 *E@2200P/50V_4X
PC105 10U/25V_8X
3,20 SYS_SHDN#
PR111 2.2/F_8
PC226 0.1U/25V_6X
PR245 0_4
+5VPCU
PC225 10U/6.3V_6X
+3VPCU
PC228 10U/6.3V_6X
+2VREF
PC229 1U/6.3V_4X
PR249 *0_2/S
PU11
RT8223P
TOP Side
EN
VIN
VREG3
VREG5
REF
TONSEL
UGATE1
UGATE2
BOOT1
BOOT2
PHASE1
PHASE2
LGATE1
LGATE2
VOUT1
FB1
PGOOD
ENTRIP1
ENTRIP2
EMC
SKIPSEL
GND
OUT2
FB2
5V_UGATE1
5V_BST1
5V_PHASE1
5V_LGATE1
5V_FB1
DDPWRGD_R
3V_UGATE2
3V_PHASE2
3V_LGATE2
3V_FB2
PR115 2.2_6
PC99 0.1U/25V_6X
PR114 2.2_6
PC98 0.1U/25V_6X
PC101 0.1U/25V_6X
PC103 *E@2200P/50V_4X
PC100 10U/25V_8X
PQ32 AON6414AL
PQ33 AON6758 Rds=5.6mOhm
PQ31 AON7410
PQ29 AON7752 Rds=13mOhm
(Peak 15.07A ,AVG 10.6A)
OCP:18A ~ 20A
(Peak 11.26A ,AVG 7.88A)
OCP:13.5A ~ 14.6A
+5V_S5
+3V_S5
B2A
DCR=19mOhm
PL13 2.2UH_10X10
PL14 2.2UH_7X7_TOK
PC222 220U/6.3V_105CS_E18e ESR=18mOhm
PC223 220U/6.3V_105CS_E18e ESR=18mOhm
PR240 *0_2/S
PR241 *0_2/S
PR247 E@2.2/F_6
PC227 E@1000P/50V_4X
PR246 E@2.2/F_6
PC224 E@1000P/50V_4X
PR244 *0_2/S
PR242 *0_2/S
EMI
C3A
PR118 88.7K/F_4
PR116 137K/F_4
PR120 15.4K/F_4
PR112 *0_4/S
PR113 0_6
PR121 6.8K/F_4
PR119 10K/F_4
PR110 10K_4
PR243 *SHORT_4
PR117 10K/F_4
3,33 S5_ON
PD4 BAV99W-7-F_150MA
PD3 BAV99W-7-F_150MA
PC97 0.1U/25V_6X
PC96 0.1U/25V_6X
PC94 0.1U/25V_6X
PC95 0.1U/25V_6X
PR109 22_8
+15V
+15V_ALWP
3V_LGATE2
PR248 *10K_4
DDPWRGD_R
SYS_HWPG 7,33
24,38,42 MAIND
MAIND
PQ26 AON7406
PQ7 AON7406
(Peak 6.5A, AVG 4.5A)
(Peak 3.9A, AVG 2.7A)
Quanta Computer Inc.
PROJECT : BDAD
Size
Document Number
System 3V/5V(TPS51123A)
Rev
A1A
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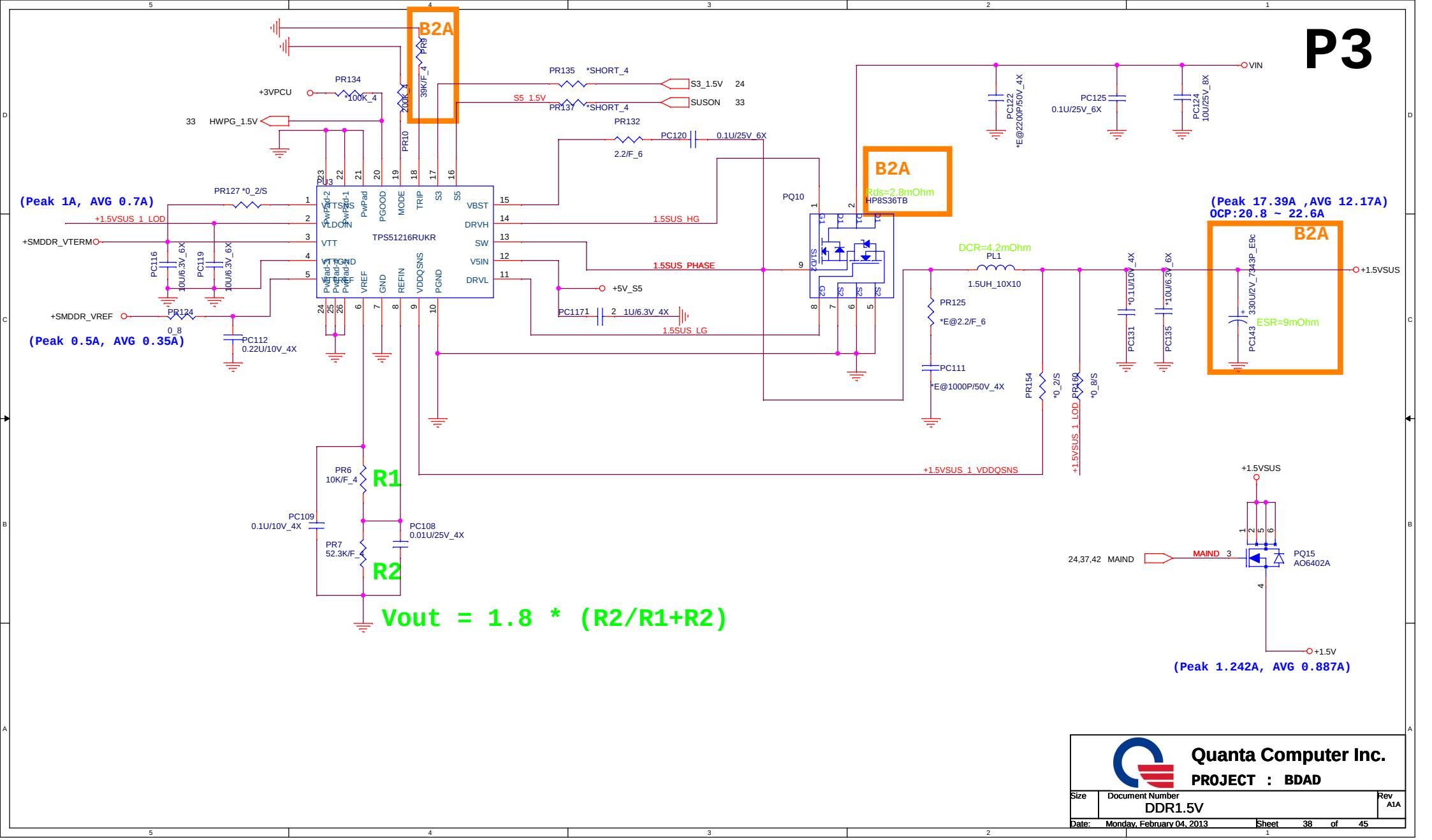
P3
B2A
PR9
39K/F_4
200K_4
PR134
+3VPCU
*100K_4
33 HWPG_1.5V
PR10
PR135 *SHORT_4
S3_1.5V 24
S5_1.5V
PR137 *SHORT_4
SUSON 33
PR132
2.2/F_6
PC120 0.1U/25V_6X
VIN
PC122 *E@2200P/50V_4X
PC125 0.1U/25V_6X
PC124 10U/25V_8X
B2A
Rds=2.8mOhm
HP8S36TB
PQ10
(Peak 1A, AVG 0.7A)
PR127 *0_2/S
+1.5VSUS_1_LOD
+SMDDR_VTERM
+SMDDR_VREF
PR124
0_8
(Peak 0.5A, AVG 0.35A)
PC116 10U/6.3V_6X
PC119 10U/6.3V_6X
PC112 0.22U/10V_4X
U3
TPS51216RUKR
PTTSNS
VLDOIN
VTT
VTTGND
PwPad-2
PwPad-1
PwPad
PGOOD
MODE
TRIP
S3
S5
VBST
DRVH
SW
V5IN
DRVL
VREF
GND
REFIN
VDDQSNS
PGND
1.5SUS_HG
1.5SUS_PHASE
1.5SUS_LG
+5V_S5
PC1171 2_1U/6.3V_4X
DCR=4.2mOhm
PL1
1.5UH_10X10
PR125
*E@2.2/F_6
PC111
*E@1000P/50V_4X
PR154 *0_2/S
PR155 *0_8/S
+1.5VSUS_1_LOD
+1.5VSUS_1_VDDQSNS
PC131 *0.1U/10V_4X
PC135 *10U/6.3V_6X
(Peak 17.39A ,AVG 12.17A)
OCP:20.8 ~ 22.6A
B2A
PC143 330U/2V_7343P_E9c
ESR=9mOhm
+1.5VSUS
PR6 10K/F_4
R1
PC109 0.1U/10V_4X
PC108 0.01U/25V_4X
PR7 52.3K/F_4
R2
Vout = 1.8 * (R2/R1+R2)
+1.5VSUS
24,37,42 MAIND
MAIND 3
PQ15
AO6402A
+1.5V
(Peak 1.242A, AVG 0.887A)
Quanta Computer Inc.
PROJECT : BDAD
Size
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DDR1.5V
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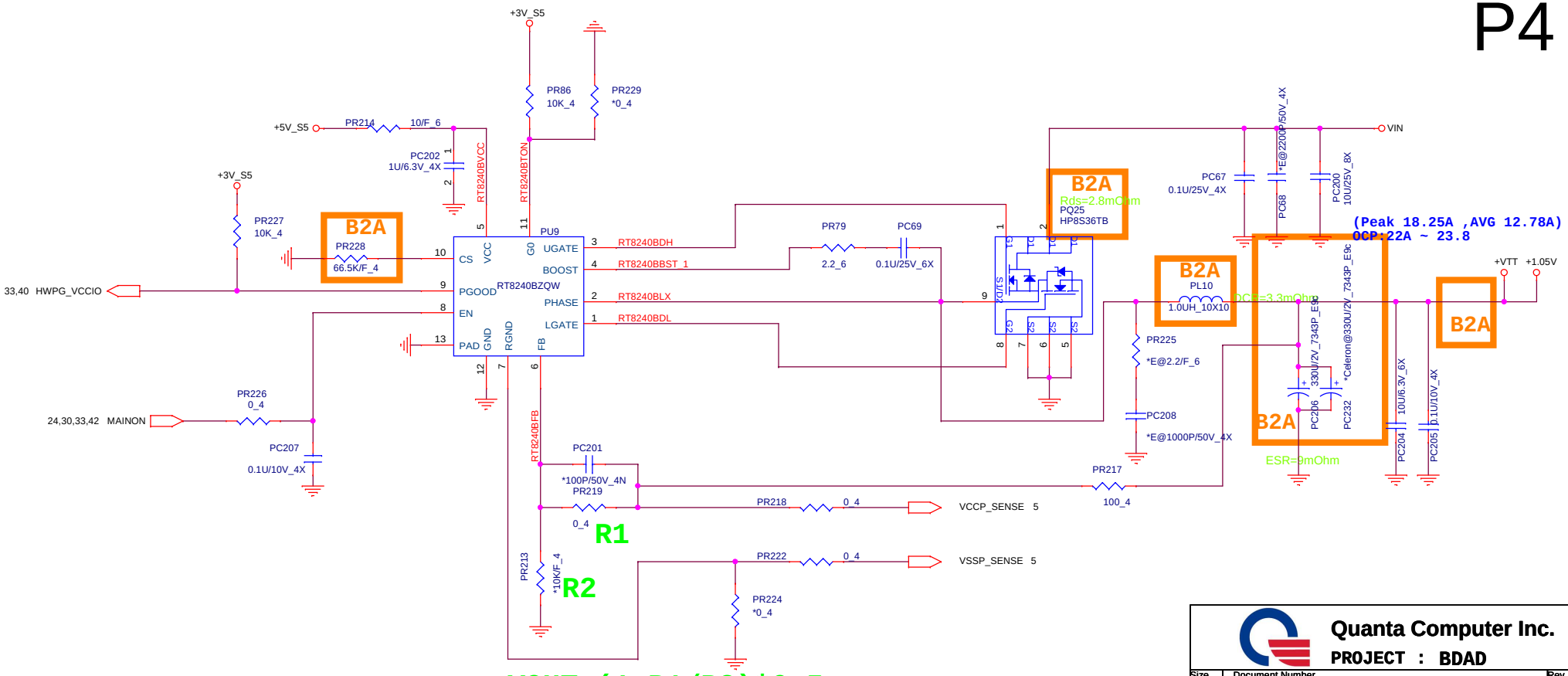
P4
+3V_S5
PR86
10K_4
PR229
*0_4
+5V_S5
PR214
10/F_6
PC202
1U/6.3V_4X
RT8240BVCC
RT8240BTON
PU9
RT8240BZQW
CS
VCC
GD
UGATE
BOOST
PGOOD
PHASE
EN
LGATE
PAD
GND
RGND
FB
RT8240BDH
RT8240BBST_1
RT8240BLX
RT8240BDL
RT8240BFB
PR227
10K_4
PR228
66.5K/F_4
B2A
33,40 HWPG_VCCIO
PR226
0_4
24,30,33,42 MAINON
PC207
0.1U/10V_4X
PR79
2.2_6
PC69
0.1U/25V_6X
B2A
Rds=2.8mOhm
PQ25
HP8S36TB
VIN
PC67
0.1U/25V_4X
*E@2200P/50V_4X
PC68
PC200
10U/25V_8X
(Peak 18.25A ,AVG 12.78A)
OCP:22A ~ 23.8
+VTT
+1.05V
B2A
PL10
1.0UH_10X10
DCR=3.3mOhm
PR225
*E@2.2/F_6
PC208
*E@1000P/50V_4X
B2A
330U/2V_7343P_E9c
*Celeron@330U/2V_7343P_E9c
PC206
PC232
ESR=9mOhm
PC204
10U/6.3V_6X
PC205
0.1U/10V_4X
B2A
PC201
*100P/50V_4N
PR219
0_4
R1
PR218
0_4
VCCP_SENSE 5
PR217
100_4
PR213
*10K/F_4
R2
PR222
0_4
VSSP_SENSE 5
PR224
*0_4
VOUT=(1+R1/R2)*0.5
Quanta Computer Inc.
PROJECT : BDAD
Size
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+VCCIO(RT8240BGQW)
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A1A
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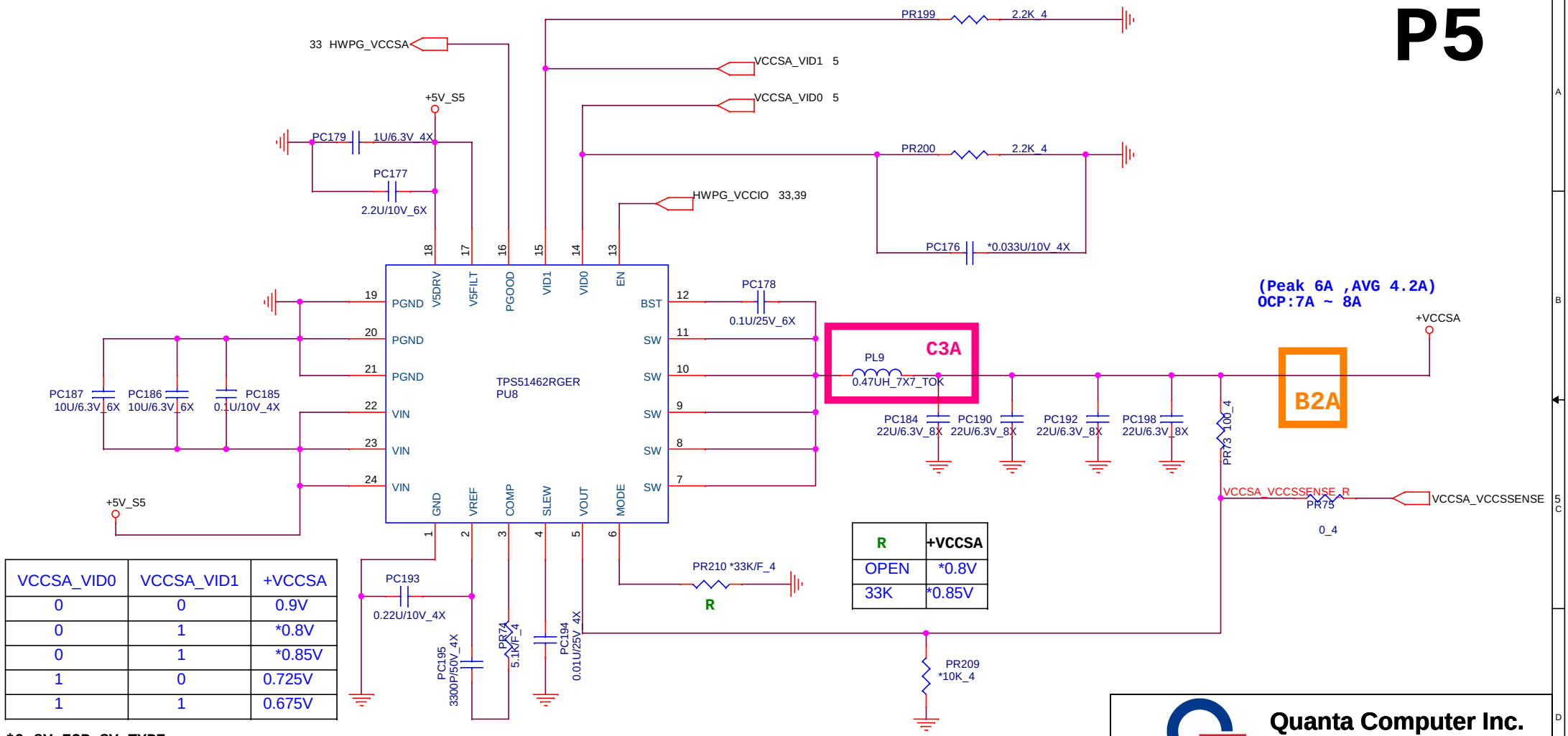

R	+VCCSA
OPEN	*0.8V
33K	*0.85V

VCCSA_VID0	VCCSA_VID1	+VCCSA
0	0	0.9V
0	1	*0.8V
0	1	*0.85V
1	0	0.725V
1	1	0.675V

***0.8V FOR SV TYPE**
***0.85V FOR LV/ULV TYPE**

Quanta Computer Inc.
PROJECT : BDAD

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	+VCCSA(TI51462)	A1A
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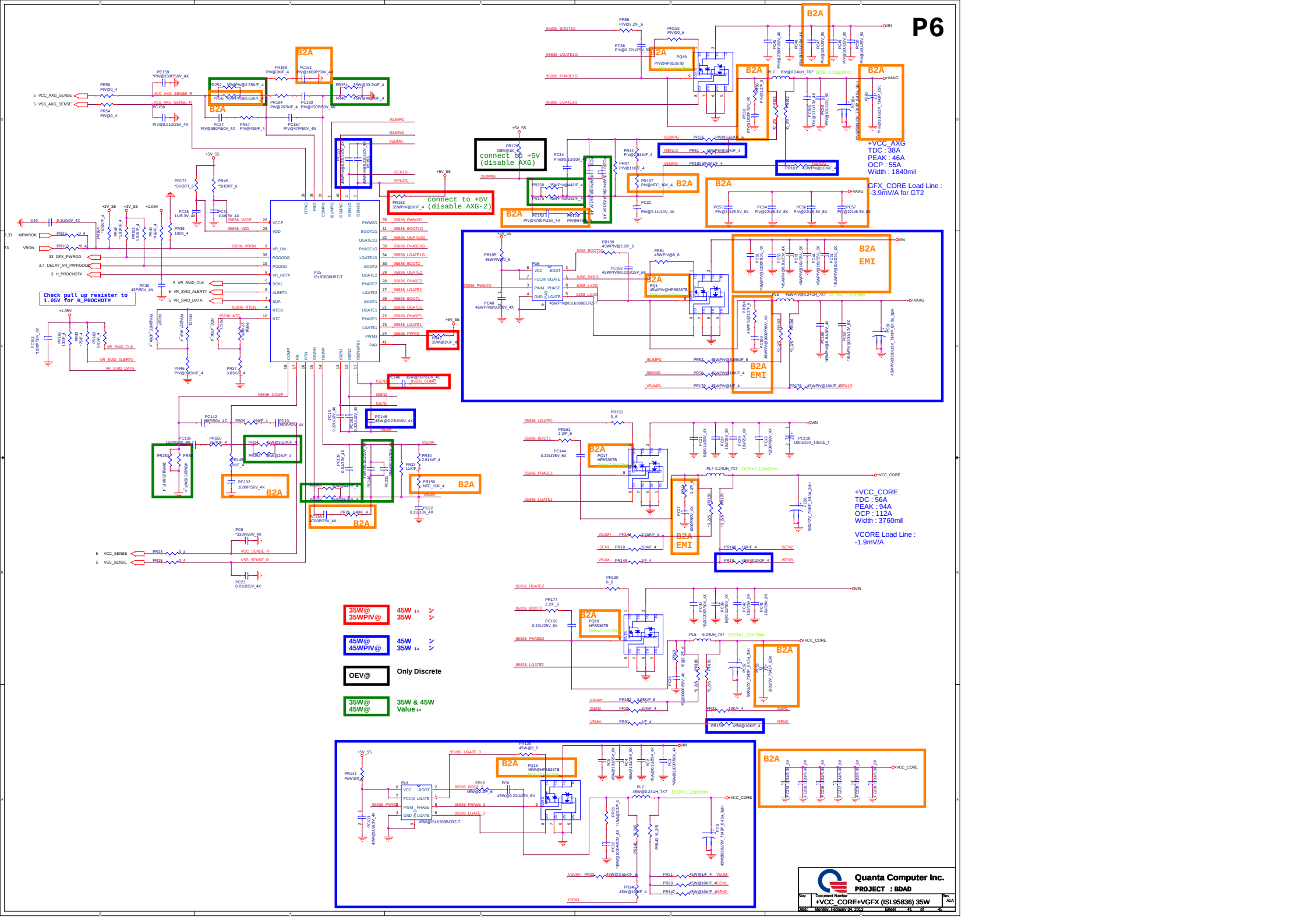
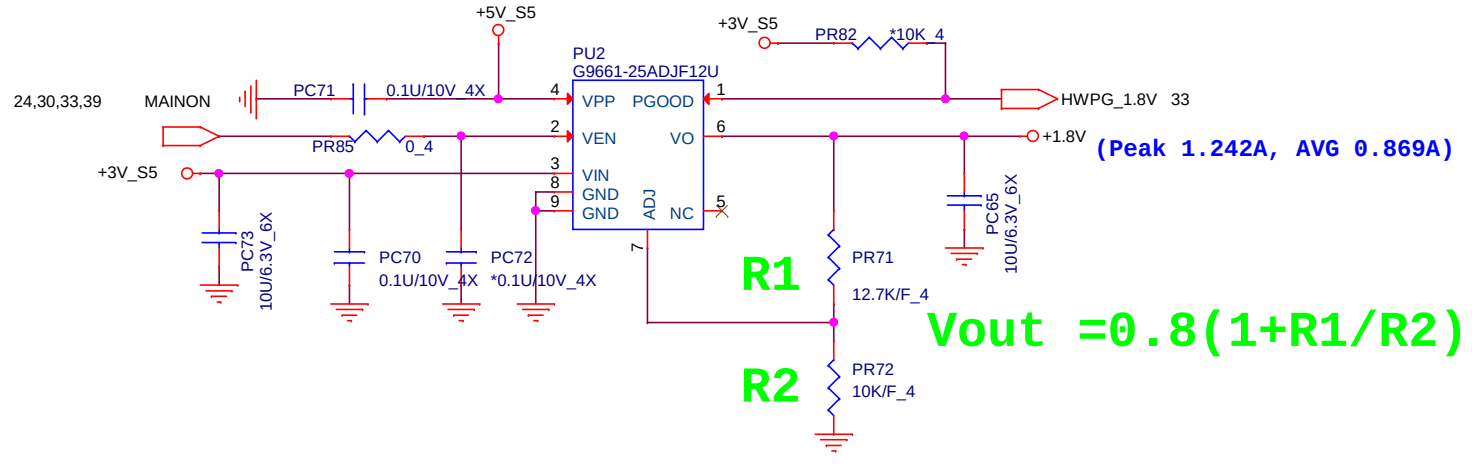
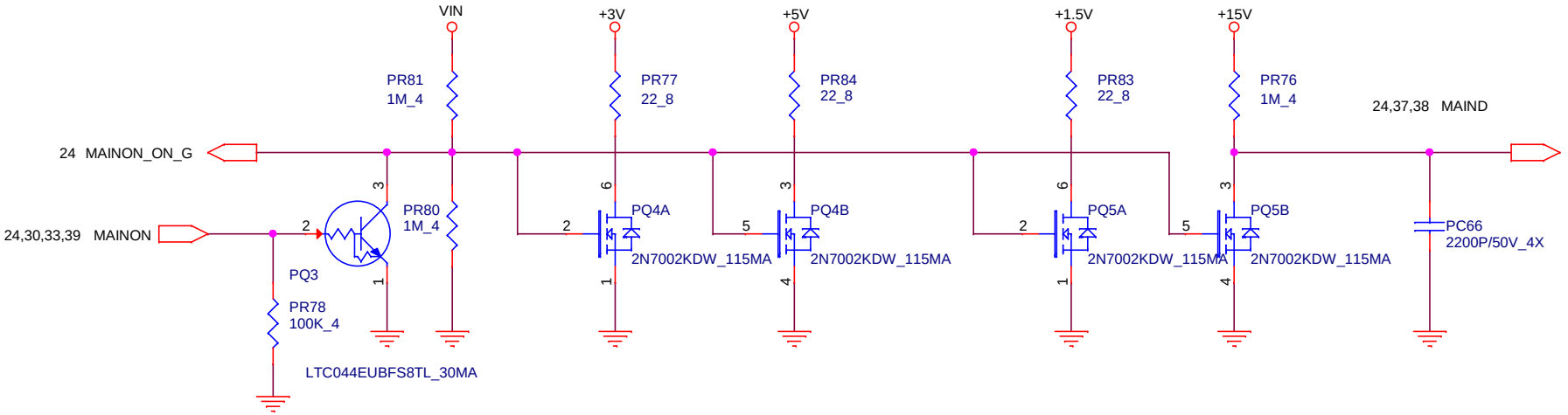

P6
+VCC_AXG
TDC : 38A
PEAK : 46A
OCP : 55A
Width : 1840mil
GFX_CORE Load Line : -3.9mV/A for GT2
+VCC_CORE
TDC : 56A
PEAK : 94A
OCP : 112A
Width : 3760mil
VCORE Load Line : -1.9mV/A
connect to +5V (disable AXG)
connect to +5V (disable AXG-2)
Check pull up resister to 1.05V for H_PROCHOT#
35W@ 35WPIV@ 45W
45W@ 45WPIV@ 35W
OEV@ Only Discrete
35W@ 45W@ 35W & 45W Value
Quanta Computer Inc.
PROJECT : BDAD
+VCC_CORE+VGFX (ISL95836) 35W
Monday, February 04, 2013





Quanta Computer Inc.		
PROJECT : BDAD		
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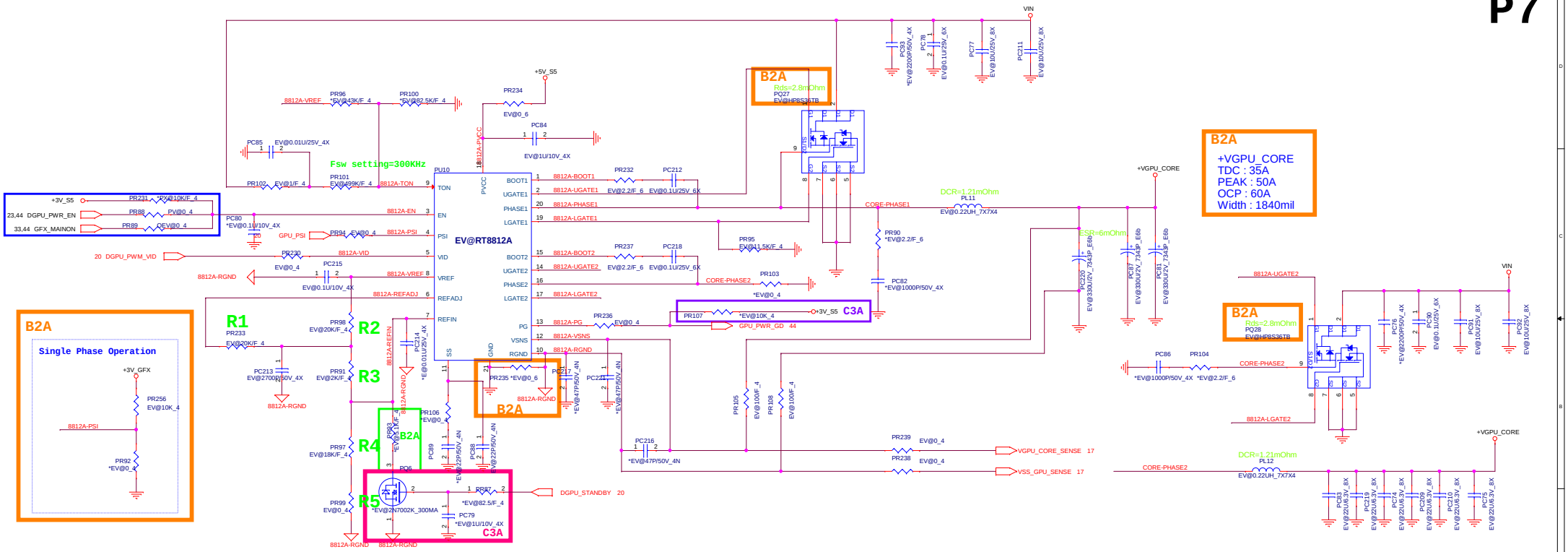
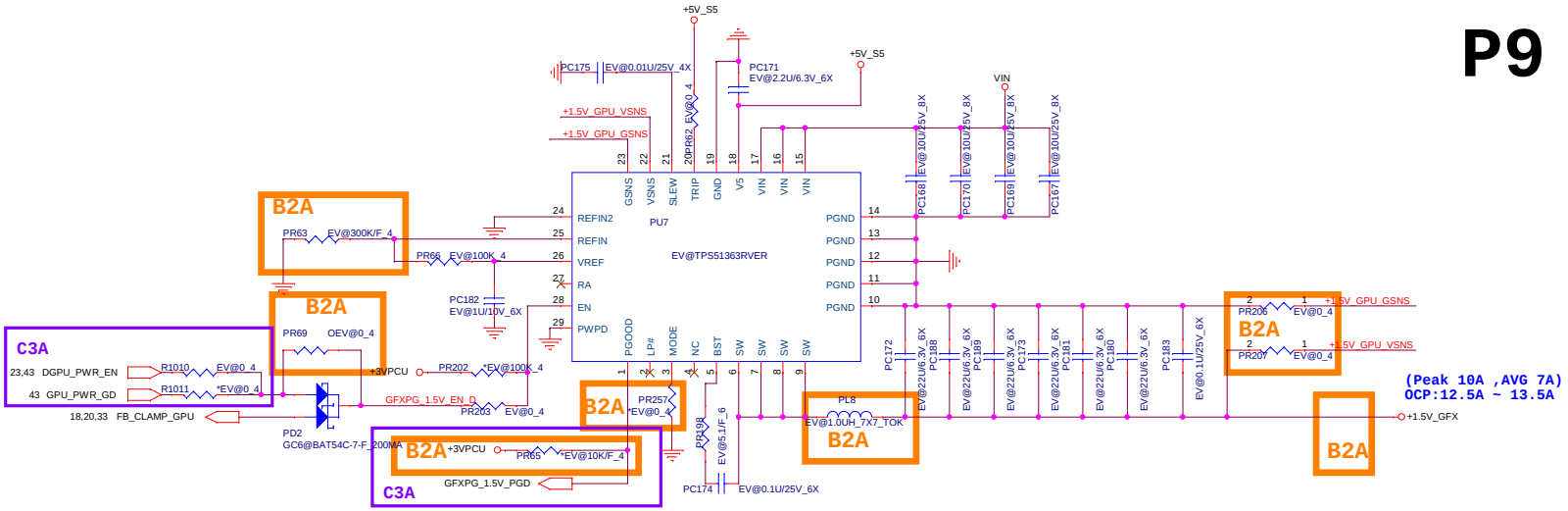
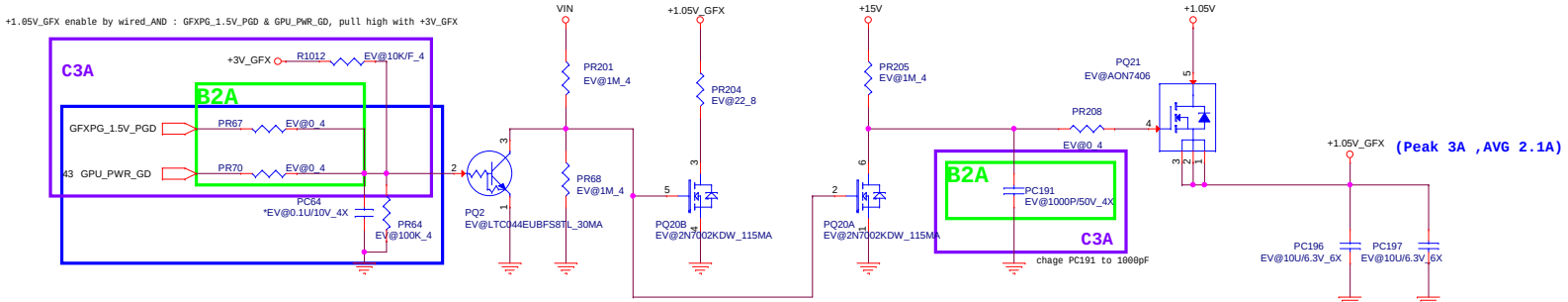
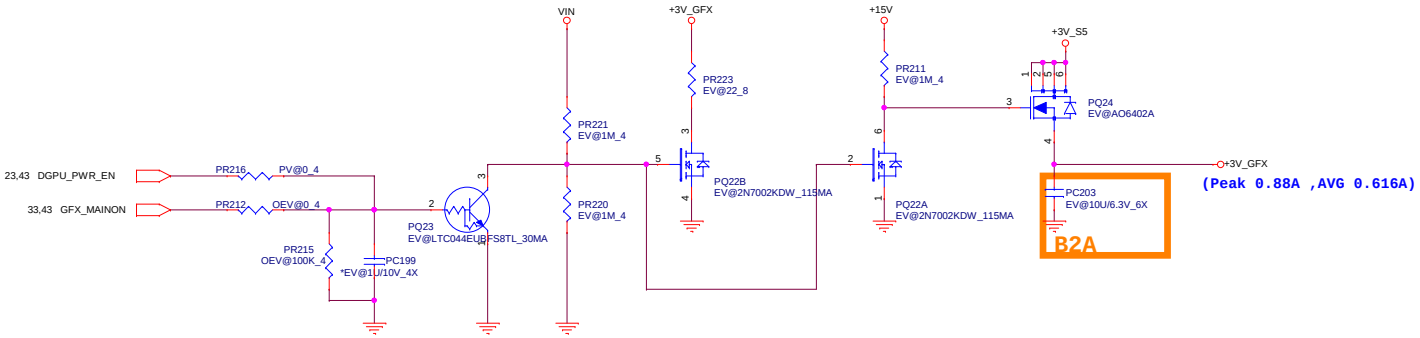


1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

P9







GPU Power On Sequence
1. DGPU_PWR_EN_R(delay) Enable +3V_GFX from +3V_S5
2. DGPU_PWR_EN Enable +VGPU_CORE
3. GPU_PWR_GD Enable +1.5V_GFX
4. GPU_PWR_GD Enable(Delay) +1.05V_GFX

Quanta Computer Inc.
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	+VGACORE	A1A
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Model REV

CHANGE LIST

MODEL BDAD

PAGE	FROM	To
1	1A	
2	1A	
3	1A	
4	1A	
5	1A	
6	1A	
7	1A	
8	1A	
9	1A	
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26	1A	
27	1A	
28	1A	
29	1A	
30	1A	

DOC NO. 204

PROJECT MODEL :	BY3E,BY4E	APPROVED BY:		DATE:	
PART NUMBER:		DRAWING BY:		REVISON:	

Quanta Computer Inc.

PROJECT : BDAD

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