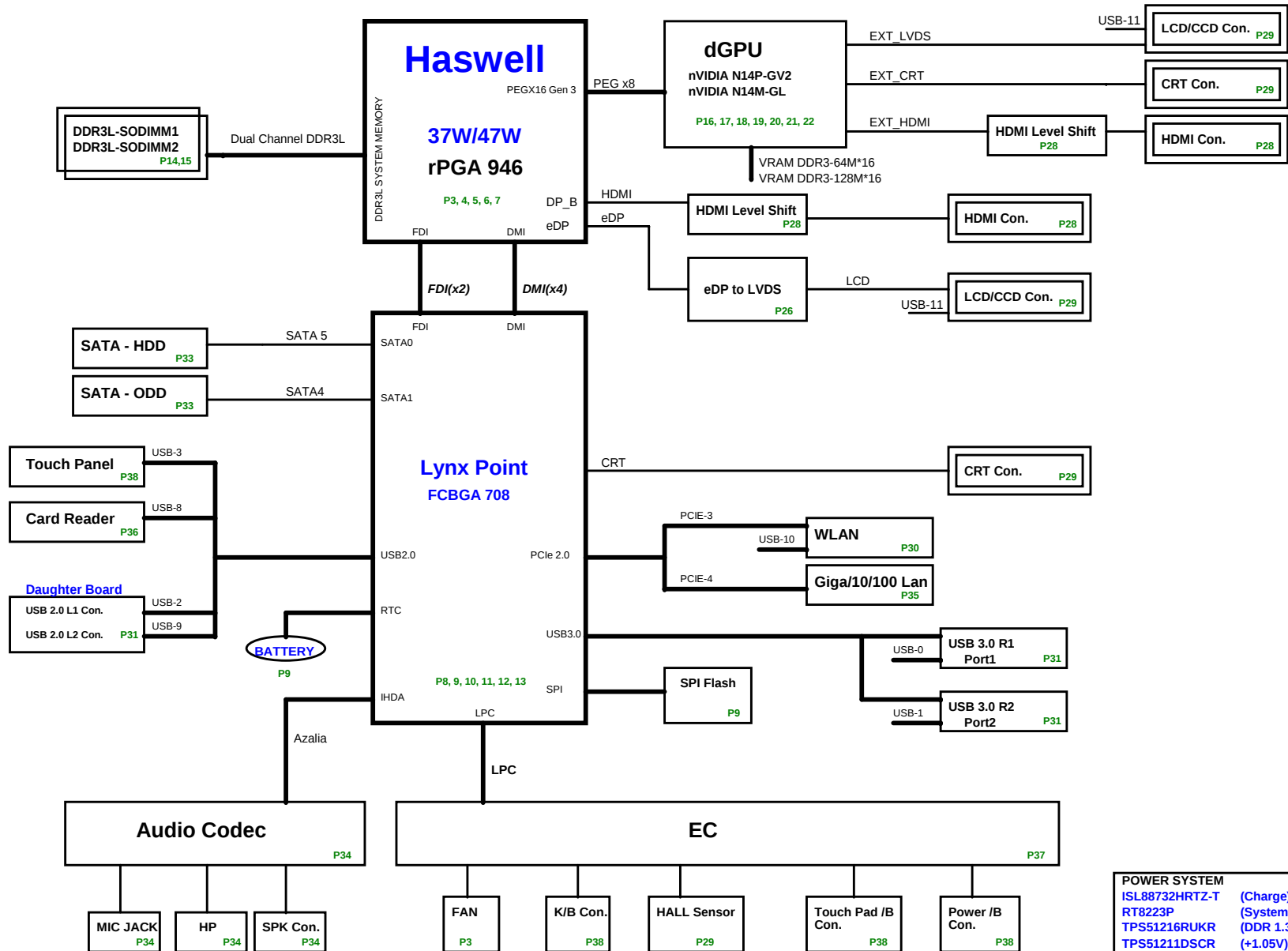
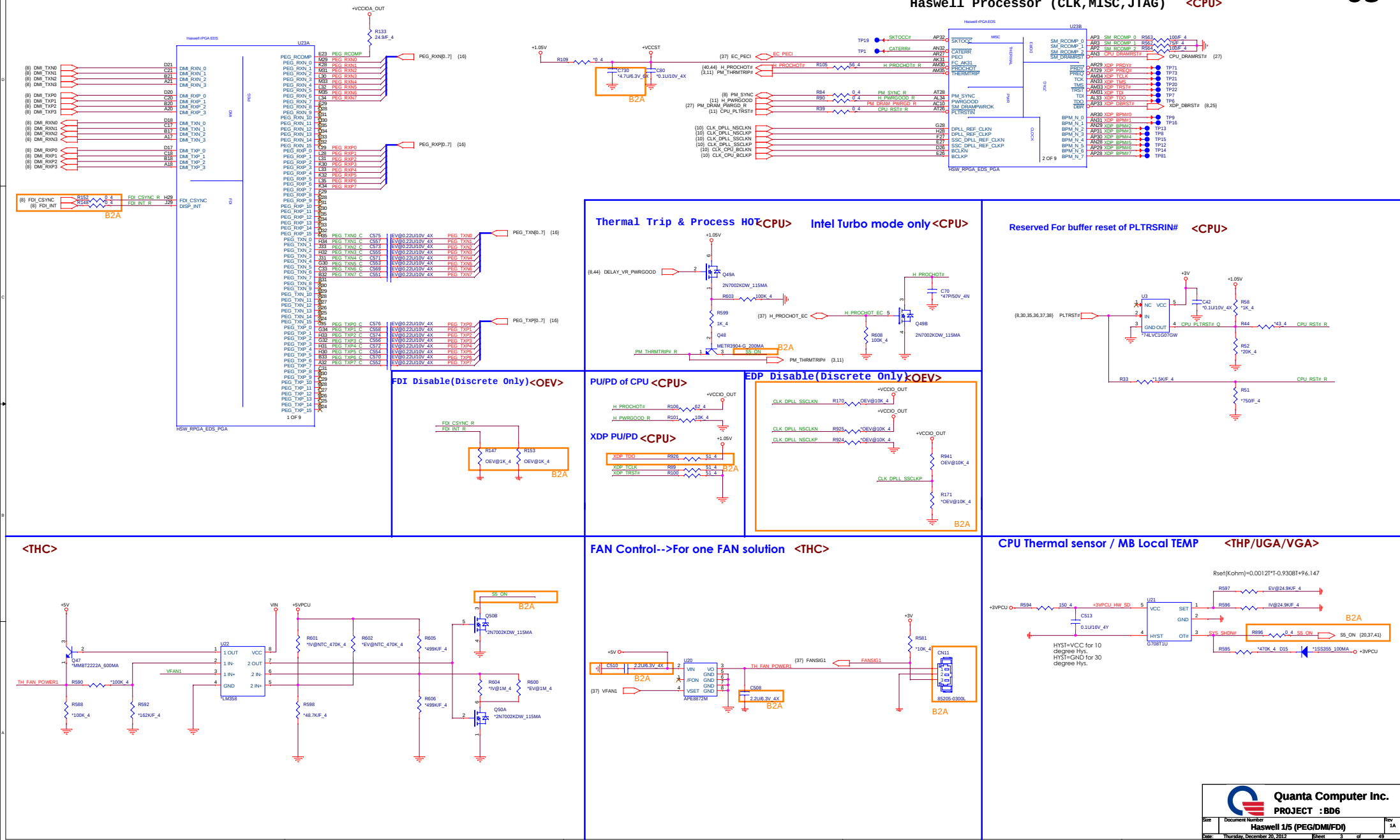


BD6 Shark Bay Block Diagram

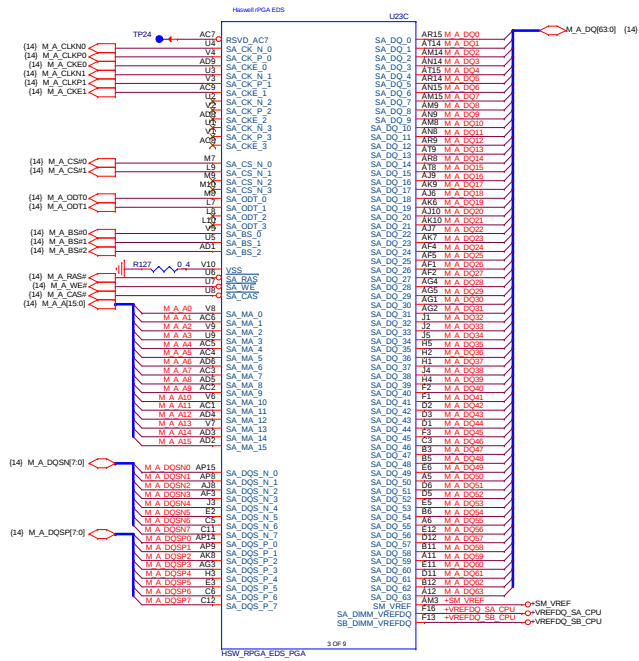
01



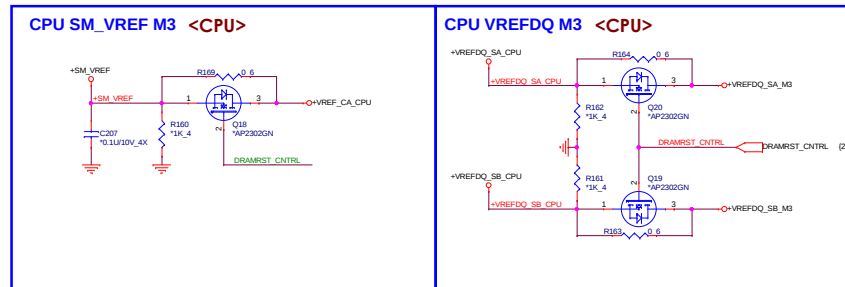
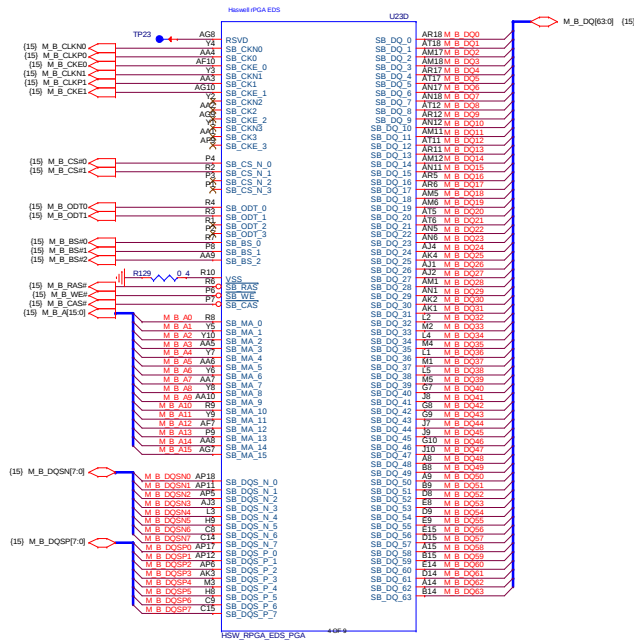
POWER SYSTEM		
ISL88732HRTZ-T	(Charge)	P40
RT8223P	(System 5V/3V)	P41
TPS51216RUKR	(DDR 1.35V)	P42
TPS51211DSCR	(+1.05V)	P43
ISL95812HRZ-T	(+VCC_CORE)	P44
RT8812A	(NV_VGPU_CORE)	P46
	(other GPU)	P47



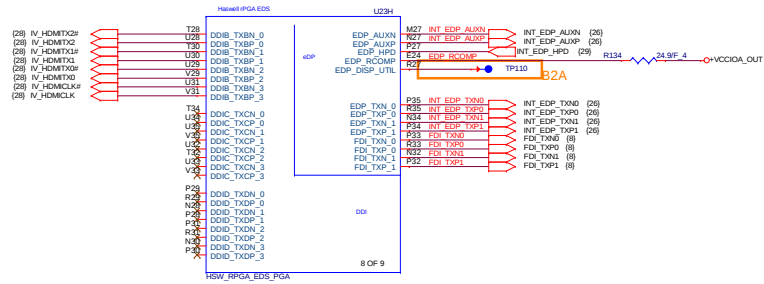
Haswell Processor (DDR3) <CPU>



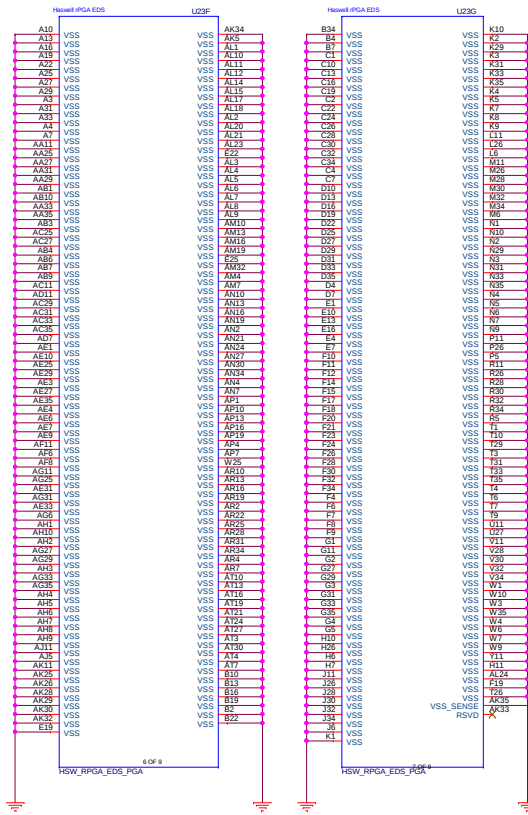
Haswell Processor (DDR3)CPU



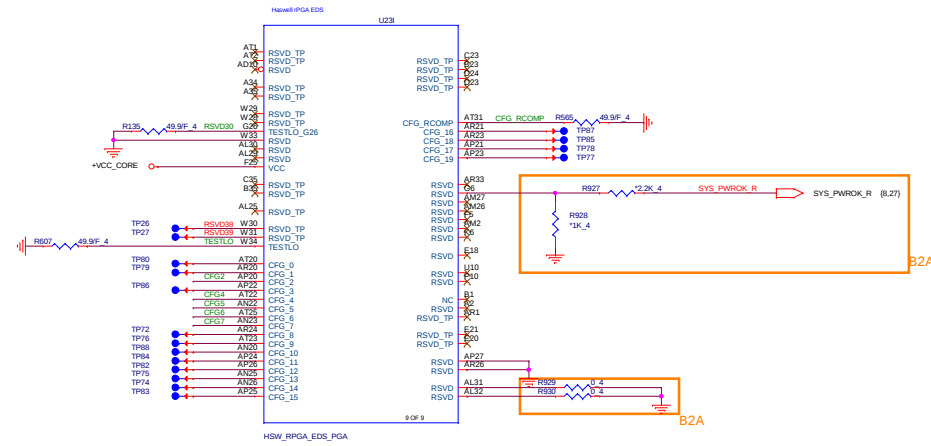
Haswell Processor (DDI,eDP,FDI) <CPU>



Haswell Processor (GND)<CPU>

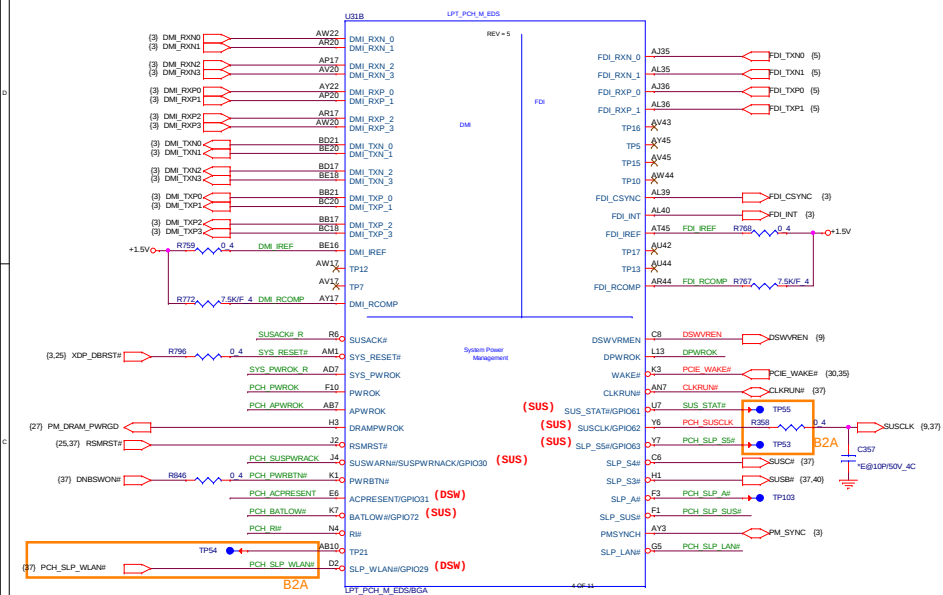


Haswell Processor (CFG,RSVD) <CPU>

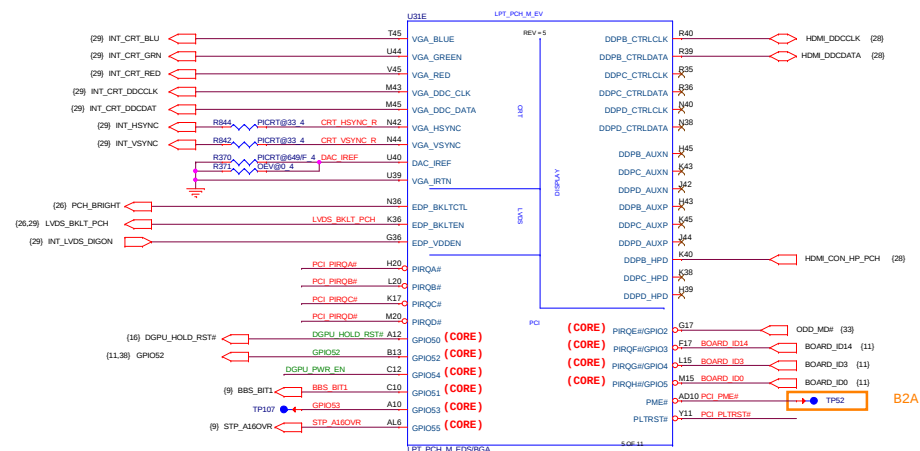


Configuration Signals:		The CFG signals have a default value of '1' if not terminated on the board.	
CFG[2]	PCI Express Static Lane Reversal	x1 = Normal operation x0 = Lane numbers reversed	CFG2 R82 EVB@1K 4
CFG[4]	eOP enable	x1 = Disabled x0 = Enabled	CFG4 R567 PWB@1K 4
CFG[6:5]	PCI Express Bifurcation	x00 = 1 x8 & 2 x4 PCI Express x01 = reserved x10 = 2 x8 PCI Express x11 = 1 x16 PCI Express	CFG6 R566 EVB@1K 4 CFG5 R81 EVB@1K 4
CFG[7]	PEG defer training	x1 = PEG train follow RESETB de-asserted x0 = PEG wait for BIOS for training	CFG7 R83 1K 4

Lynx Point (DMI, FDI, PM)<CLG>

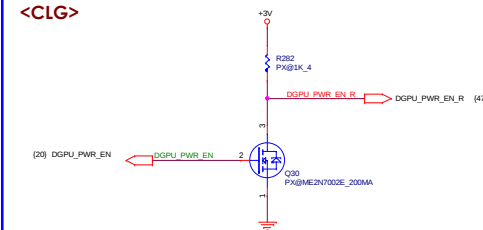


Lynx Point (CRT,PCI,DDI CNTL)<CLG>

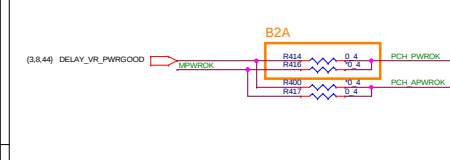


GPIO53 can not PD

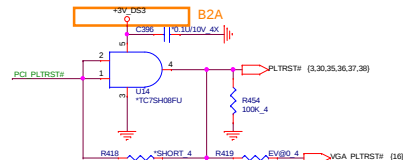
<CLG>



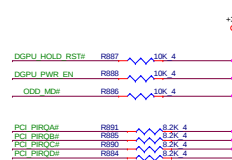
PCH PWROK&APWROK <CLG>



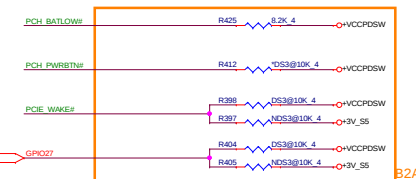
PLTRST# Buffer <CLG>



PCI PU <CLG>



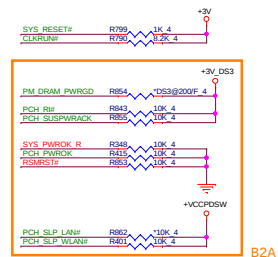
PCH WAKE EVENT<CLG>



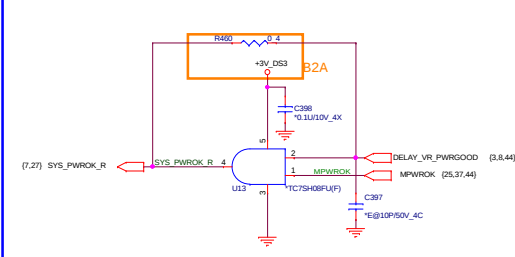
CRT IMPEDANCE MATCHING <CLG>



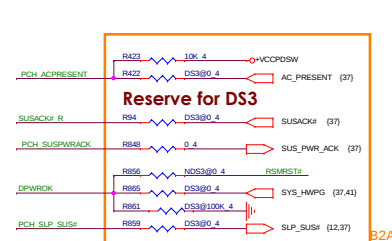
PCH PM PU/PD <CLG>



SYSPWOK <CLG>

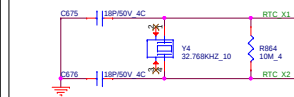


DSW Circuit <CLG>

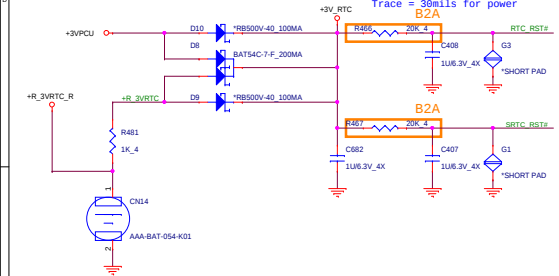


Net Name	Deep Sx Support	Deep Sx No Support
AC_PRESENT	V	NA
SUS_PWR_ACK	V	NA
SUSACK#_R	V	V
DPWROK	V	NA
SLP_SUS	V	NA

RTC Clock 32.768KHz (RTC) <CLG>



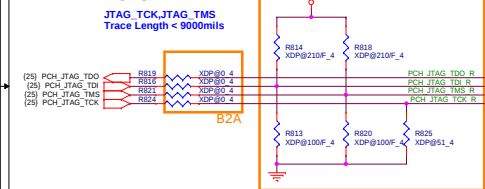
RTC Circuitry (RTC) <RTC>



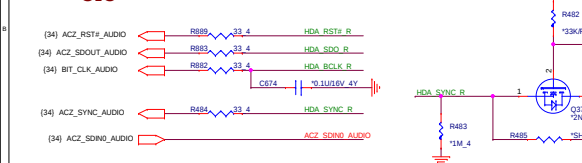
PU & Password Clear <CLG>



PCH JTAG <CLG>

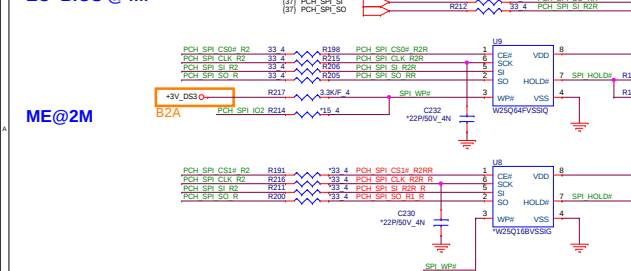


HDA <CLG>



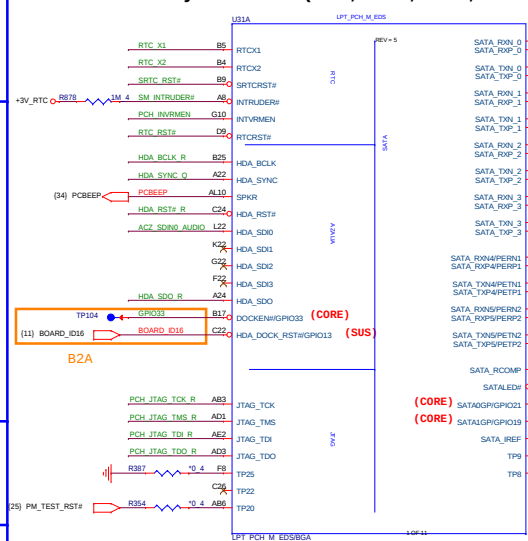
PCH Dual SPI <CLG>

EC+BIOS @4M

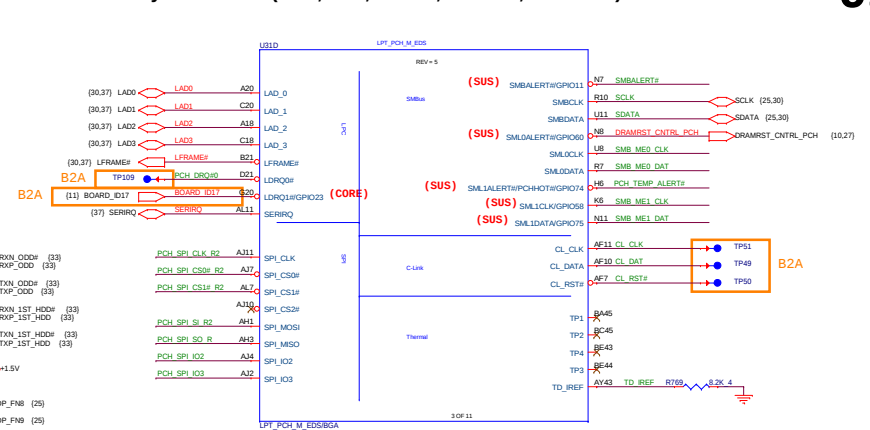


ME@2M

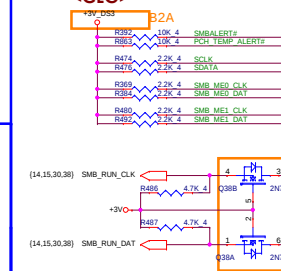
Lynx Point (RTC, I2DA, SATA, JTAG) <CLG>



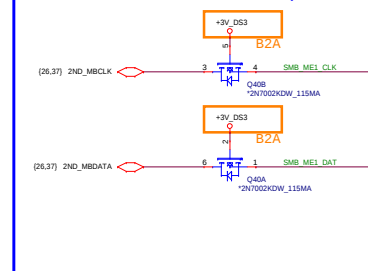
Lynx Point (LPC, SPI, SMBUS, C-LINK, THERMAL) <CLG>



SMBus <CLG>

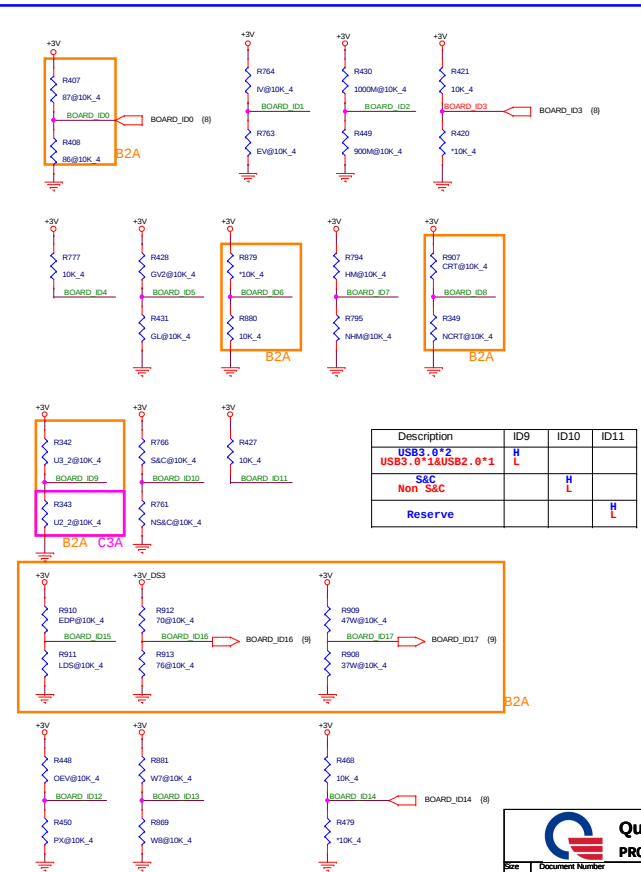
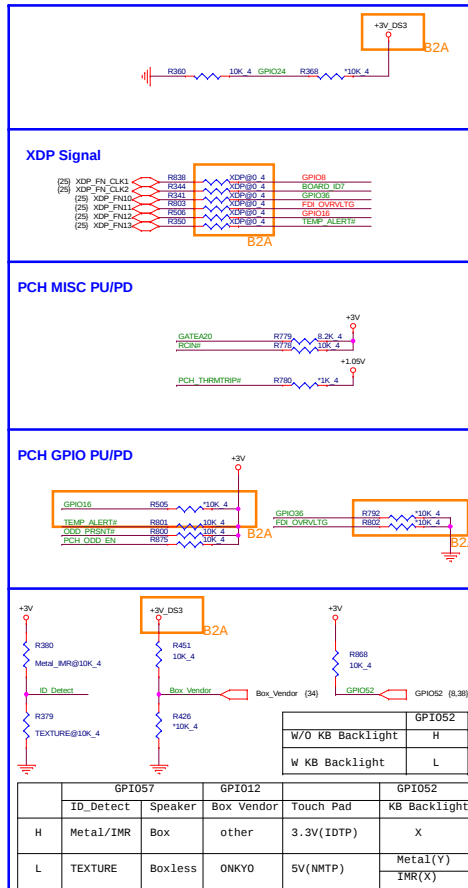
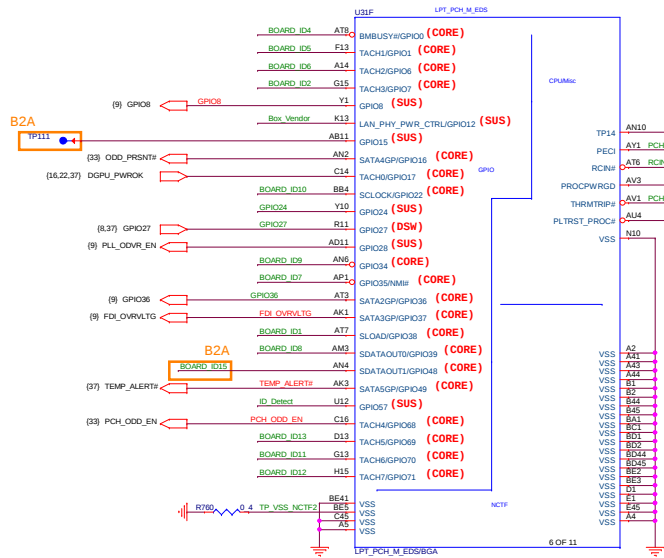


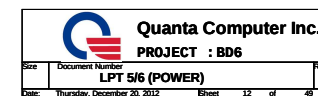
EC 2nd_SMB read SML1 Bus of PCH temps



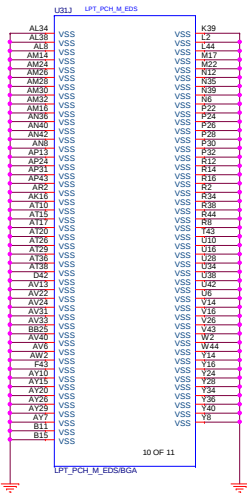
PCH STRAPPING

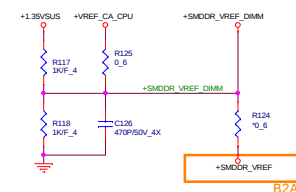
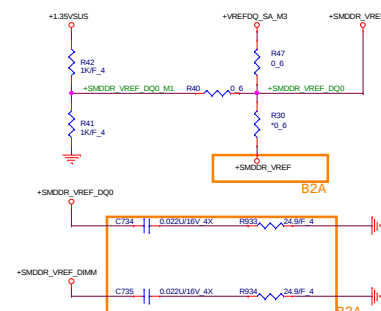
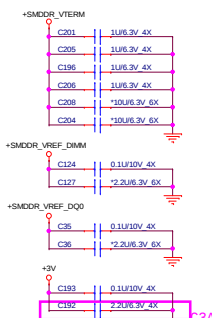
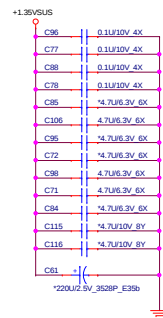
Pin Name	Usage	Sampled	Configuration	Circuitry
SPKR	No Reboot	PWROK	0 = Disable (Int PD) 1 = Enable	
GPI062 / SUSCLK	PLL On-Die Voltage Regulator Enable	RSMRST#	0 = Disable 1 = Enable (Int PU)	
GPI055	Top-Block Swap Override	PWROK	0 = Top-Block Swap mode 1 = Default (Int PU)	
INTVRMEN	Integrated VRM Enable	Always	0 = Disable 1 = Enable	
GPI051	Boot BIOS Strap bit 1	PWROK	Bt1 Bt0 1 0 Reversed 1 1 SPI 0 0 LPC	
SATA1GPGPI019	Boot BIOS Strap bit 0	PWROK	0 = Security Effect (Int PD) 1 = Can be Override	
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	Internal PD	
GPI036	RSVD	PWROK	Internal PU	
SATA3GPGPI037	TLS Confidentiality	PWROK	0 = TLS no confidentiality (Int PD) 1 = TLS with confidentiality	
GPI08	RSVD	RSMRST#	Internal PU	
GPI028	PLL on die VR enable	RSMRST#	0 = Disable 1 = Enable (Int PU)	
DSWVREN	On Die DSW VR Enable	Always	0 = Disable 1 = Enable Must be PU to VCCTRC	

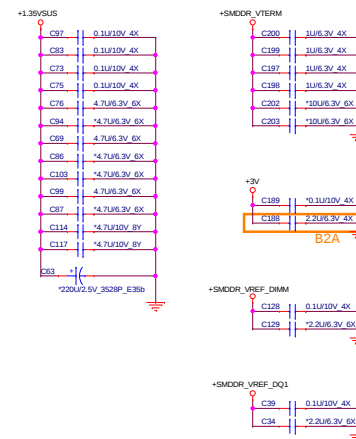
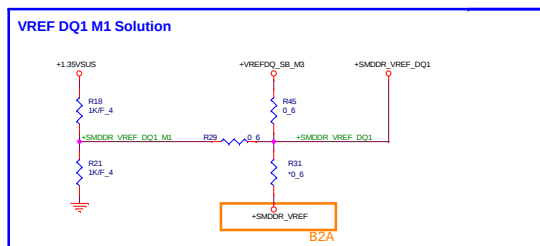
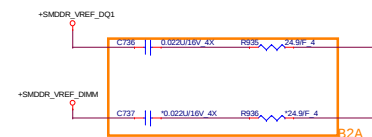
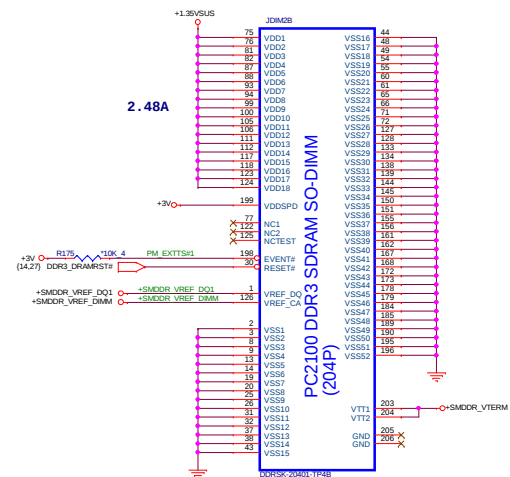
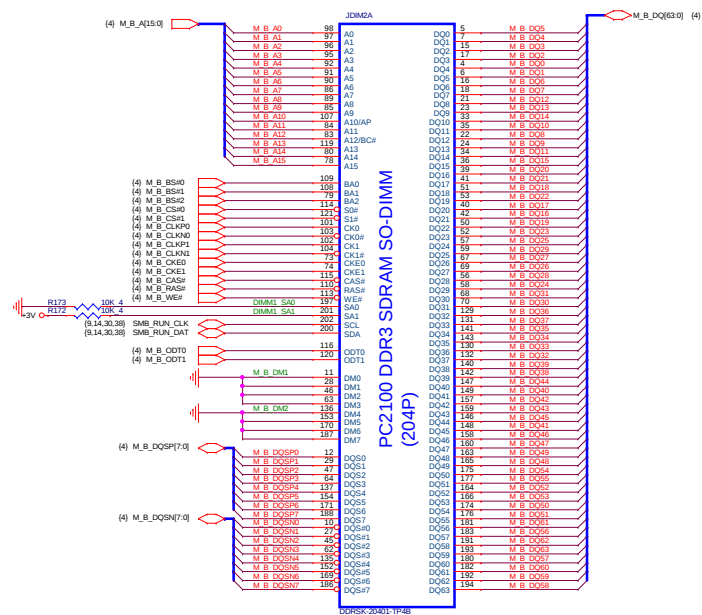


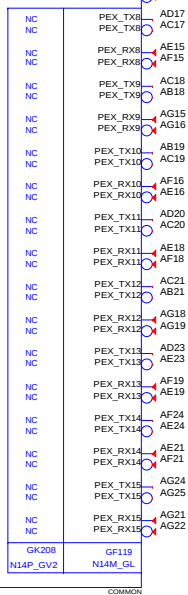
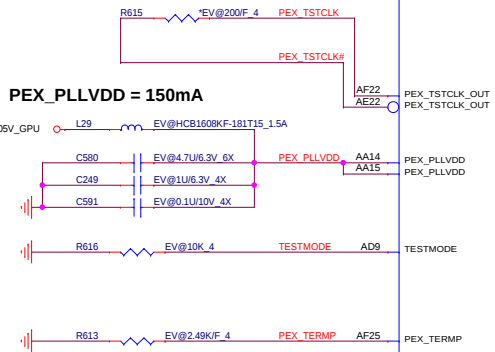


Lynx Point (GND)<CLG>

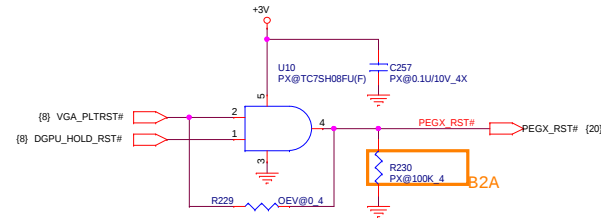




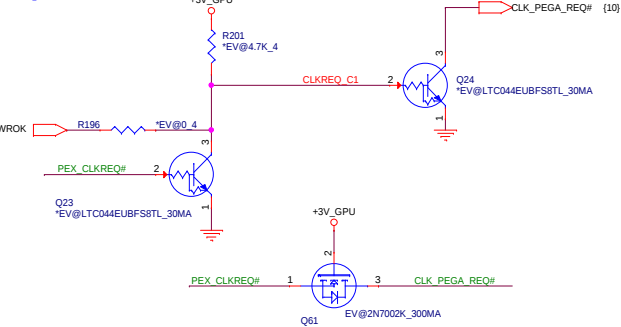


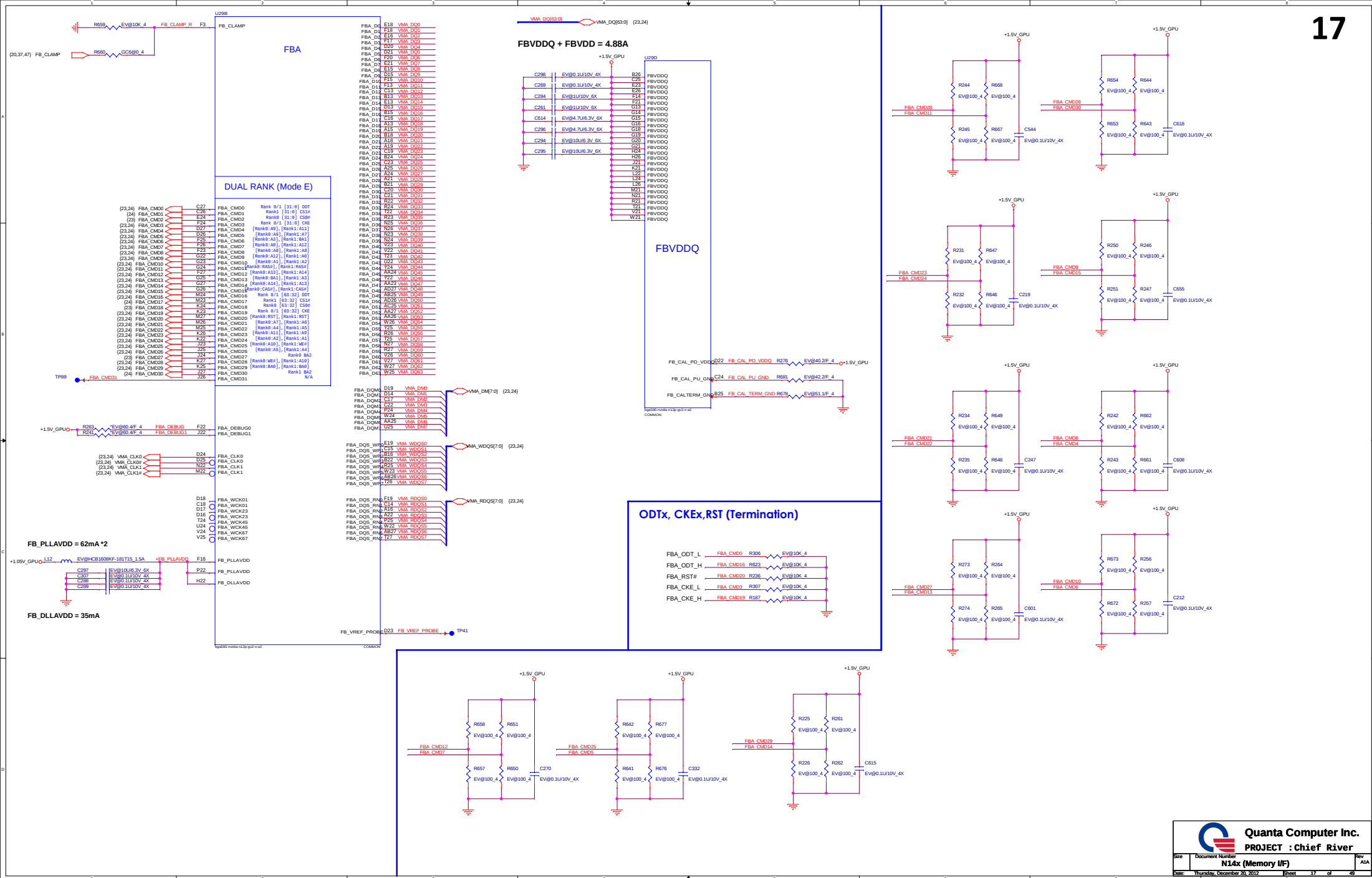


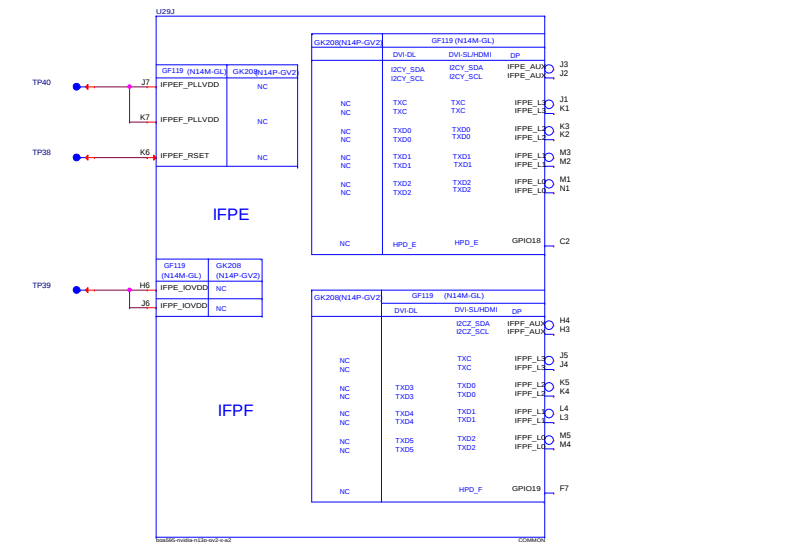
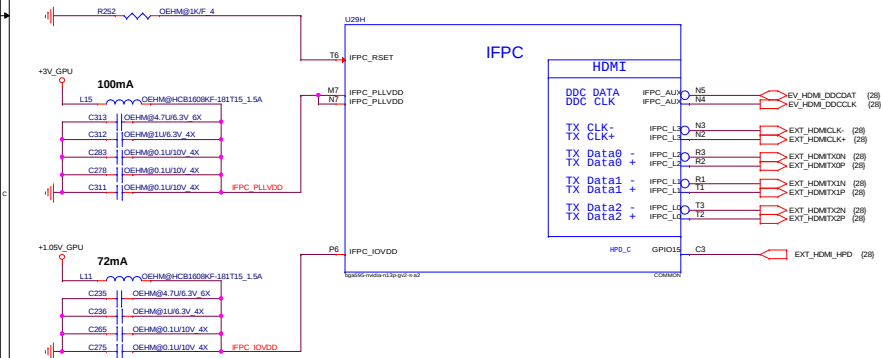
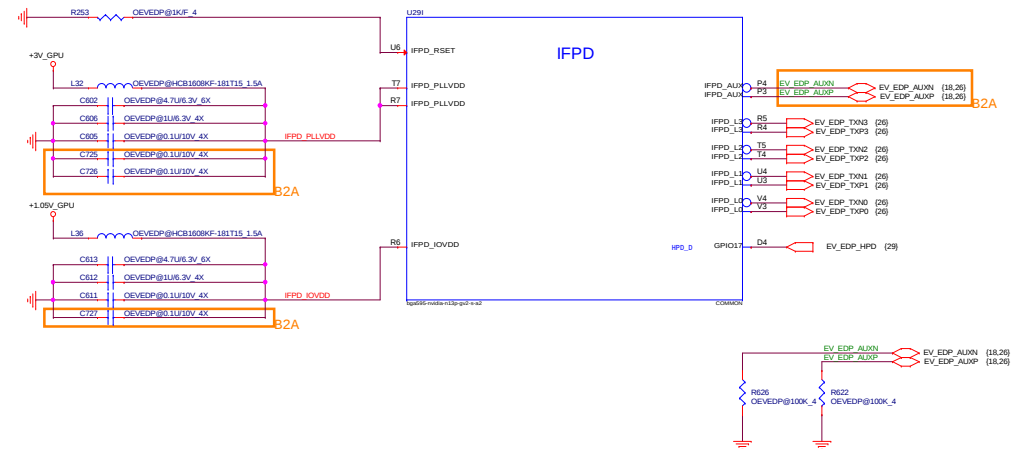
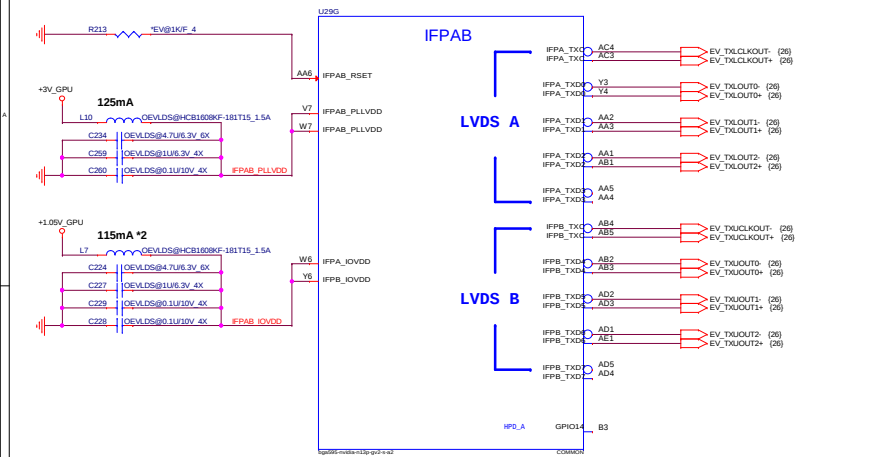
PCIE (RESET)

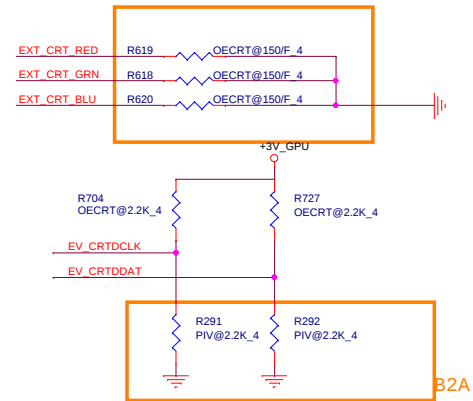
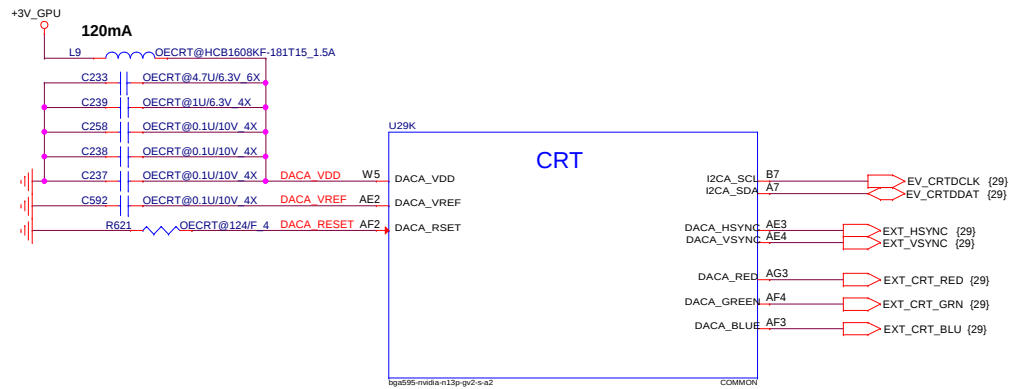
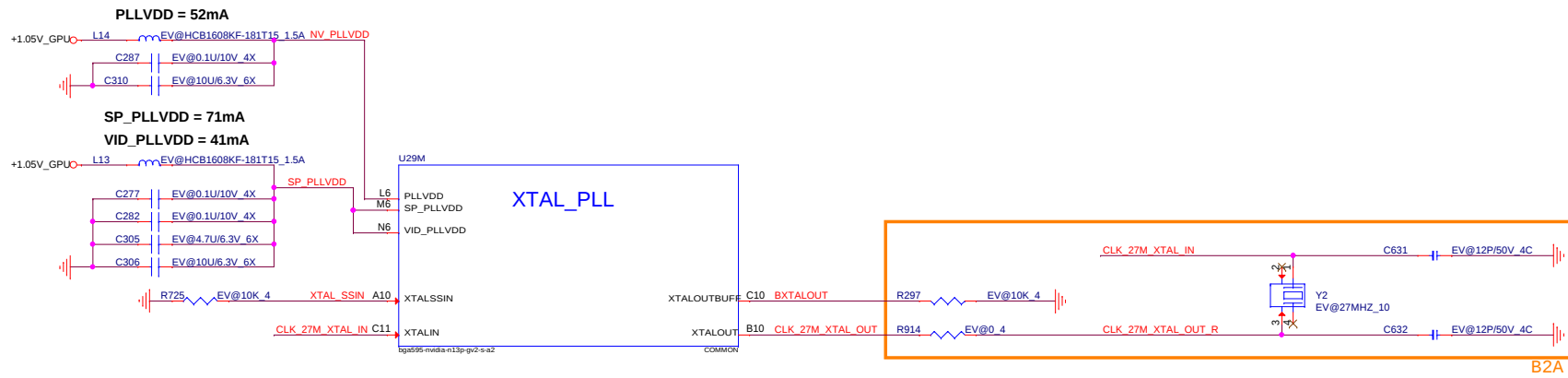


PCIE (CLK_REQ)



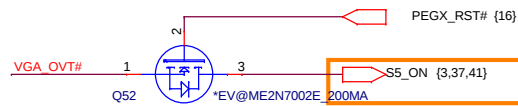
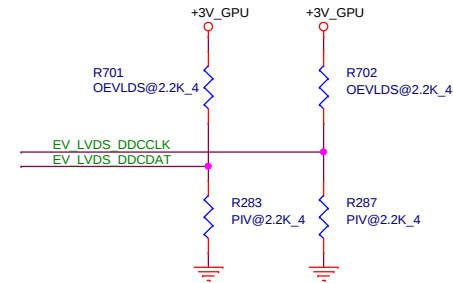
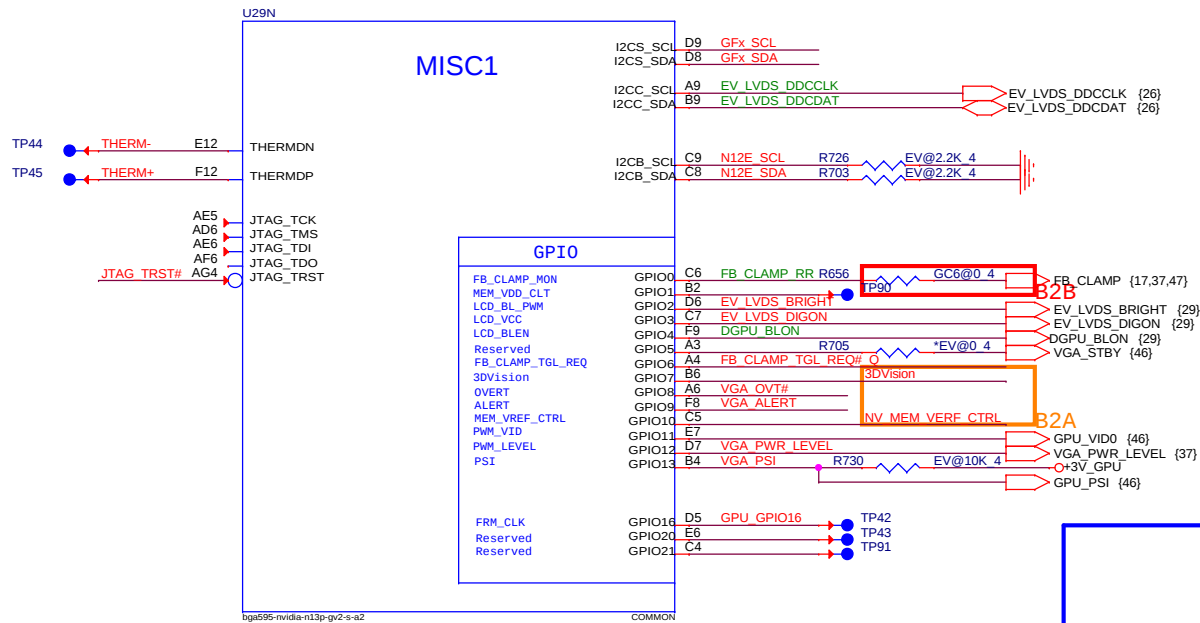




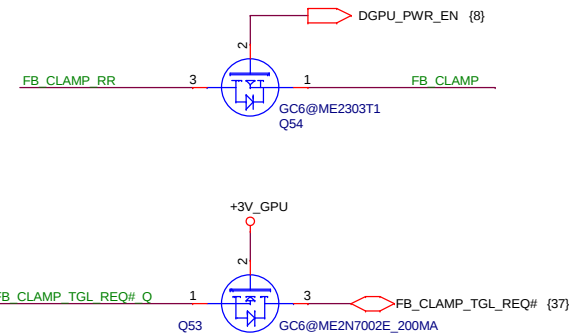
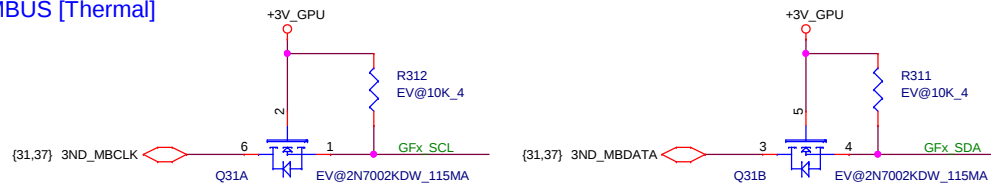


Quanta Computer Inc.
PROJECT :Chief River

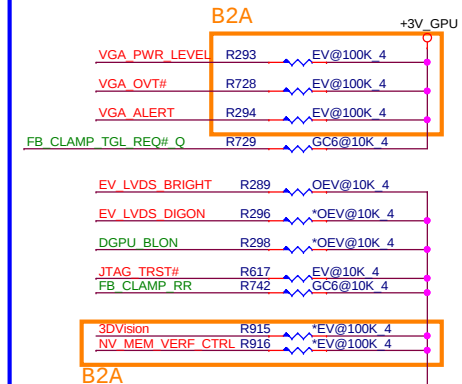
Size	Document Number	Rev
	N14x (XTAL/CRT I/F)	A1A
Date:	Thursday, December 20, 2012	Sheet 19 of 49



SMBUS [Thermal]

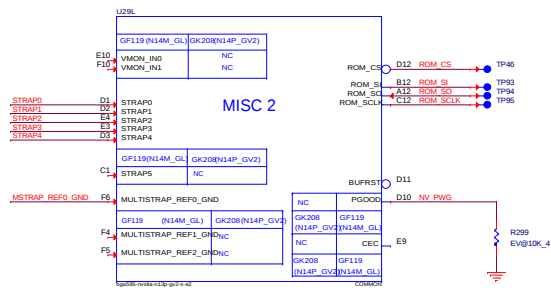


GPIO PU/PD



Quanta Computer Inc.
PROJECT :Chief River

Size	Document Number	Rev
	N14x (GPIO)	A1A
Date:	Friday, December 28, 2012	Sheet 20 of 49



		Vendor P/N	STN B/S P/N	Size	Strap	Note
128M (2G bit)	Hynix H1 H2	H5TQ2G63DFR-N0C (128M*16) 6L/6V2		x4=1GB	GL:0x06 0110	GV2:0x06 0110 1000MHz
				x8=2GB		GV2:0x06 0110 1000MHz
		H5TQ2G63DFR-11C (128M*16) 6L/6V2		x4=1GB	GL:0x06 0110	GV2:0x06 0110 900MHz
				x8=2GB		GV2:0x06 0110 900MHz
	Samsung S1 S2	K4W2G1646E-BC1A (128M*16) 6L/6V2		x4=1GB	GL:0x05 0101	GV2:0x07 0111 1000MHz
				x8=2GB		GV2:0x07 0111 1000MHz
		K4W2G1646E-BC11 (128M*16) 6L/6V2		x4=1GB	GL:0x05 0101	GV2:0x07 0111 900MHz
				x8=2GB		GV2:0x07 0111 900MHz
	Micron M1 M2	MT41JJ128M16JT-107G-K (128M*16) 6L/6V2		x4=1GB	GL:0x01 0001	GV2:0x05 0101 900MHz
				x8=2GB		GV2:0x05 0101 900MHz
		MT41JJ128M16JT-093G-K (128M*16) 6L/6V2		x4=1GB	GL:0x01 0001	GV2:0x05 0101 1000MHz
				x8=2GB		GV2:0x05 0101 1000MHz
256M (4Gbit)	Micron M3	MT41K256M16HA-107G:E (256M*16) 6L/6V2		x4=2GB	GL:0x0D 1101	GV2:0x01 0001 900MHz
				x8=4GB		GV2:0x01 0001 900MHz
	Samsung S3	K4W4G1646B-HC11 (256M*16) 6L/6V2		x4=2GB	GL:0x0B 1011	GV2:0x03 0011 900MHz
				x8=4GB		GV2:0x03 0011 900MHz
	Hynix H3 H4	H5TQ4G63MFR-11C (256M*16) 6L		x4=2GB	GL:0x03 0011	GV2:0x03 0011 900MHz
				N/A		
		H5TQ4G63AFR-11C (256M*16) 6L		x4=2GB	GL:0x04 0100	GV2:0x04 0100 900MHz
				N/A		

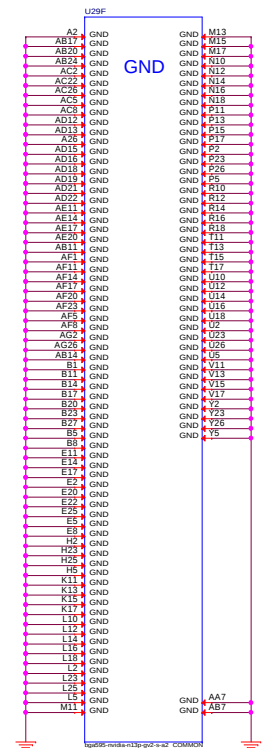
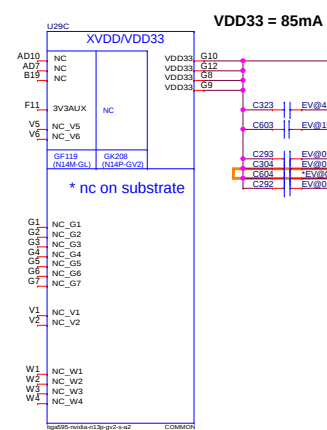
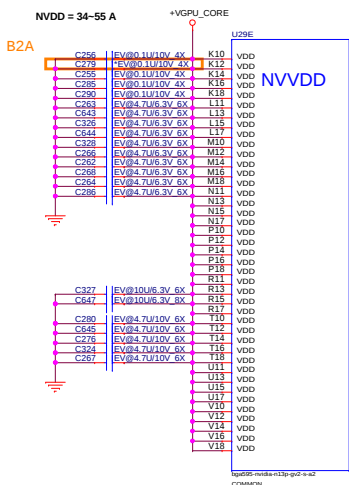
MULT STRIP [N14P_GV2]			
PCI_DEVICE STRAP	PCI DEVICE ID 0x1292 -->QS 0x12AD -->ES	DP_PLL_VDD33	1 [Default]
RAM_CFG	RAM_CFG[3:0] for memory configuration	PEX_PLL_EN_TERM	PCIE PLL termination 0:Disable [Default] ; 1:Enable
SUB_VENDOR	0:No vBIOS ROM ; 1: BIOS ROM [Default]	3GIO_PADCFG	[0000] --> Gen3 support
FB[1:0]	[1:0] --> 256MB	PCIE_MAX_SPEED	[1] --> Allow boot to PCIE Gen3
VGA_DEVICE	0:3D Device ; 1:VGA Device	PCIE_SPEED_CHANG_GEN3	[1] --> Enable Gen3
I2CS_Slave Address	0:9E [Default] ; 1:9C	SORx_EXPOSED	SOR0_EXP=0, SOR1_EXP=1 [BYPASS VDS] ; [FPC-HDM]
USER STRAP	Panel EDID Support		

Strap Pin name	Strapping Bits 3	Strapping Bits 2	Strapping Bits 1	Strapping Bits 0	SETTING	NOTE
ROM_SCLK	PCI_DEVICE[4]	SUB_VENDOR	PCI_DEVICE[5]	PEX_PLL_EN_TERM	ROM_SCLK +3V_GPU ○ R738 *15K/ 4 R717 *15K/ 4	
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]	ROM_SI +3V_GPU ○ R735 *15K/ 4 R714 Strap GV2@15K/ 4	
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE	ROM_SO +3V_GPU ○ R736 *15K/ 4 R715 Strap GV2@15K/ 4	
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	STRAP0 +3V_GPU ○ R693 *15K/ 4 R692 *15K/ 4	
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	STRAP1 +3V_GPU ○ R698 *15K/ 4 R697 Strap GV2@45.3K/ 4	
STRAP2	PCI_DEVICE[3]	PCI_DEVICE[2]	PCI_DEVICE[1]	PCI_DEVICE[0]	STRAP2 +3V_GPU ○ R666 *15K/ 4 R670 Strap GV2@15K/ 4	
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	STRAP3 +3V_GPU ○ R675 *15K/ 4 R674 DEV GV2@15K/ 4	
STRAP4	RESERVED	PCIE_SPEED_CHAN CE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V	STRAP4 +3V_GPU ○ R685 *15K/ 4 R684 PIV GV2@4.99K/ 4	
4.99K	1000	0000	24.9K	1100	0100	
10K	1001	0001	30.1K	1101	0101	
15K	1010	0010	34.8K	1110	0110	
20K	1011	0011	45.3K	1111	0111	
Resistor Value	VDD33	GND	Resistor Value	VDD33	GND	
					MSTRAP_REF0_GND R280 *15K/ 4 GV2@40.2K/ 4	

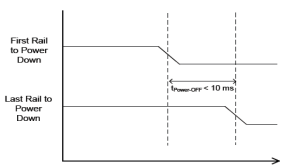
Binary Strap [N14M_GL]			
Strap Pin name	Strap Mapping	Polarity	SETTING
ROM_SCLK	SMB_ALT_ADDR	Pull-down to GND	ROM_SCLK +3V_GPU ○ R739 *10K/ 4 R718 CL@10K/ 4
ROM_SI	SUB_VENDOR	Pull-Up to 3V3 if vBIOS ROM Exist Pull-down to GND if no vBIO ROM	ROM_SI +3V_GPU ○ R734 *10K/ 4 R713 CL@10K/ 4
ROM_SO	VGA_DEVICE	Pull-down to GND (no dispaly)	ROM_SO +3V_GPU ○ R737 *10K/ 4 R716 CL@10K/ 4
STRAP0	RAMCFG[0]	USER defined	STRAP0 +3V_GPU ○ R690 Strap CL@10K/ 4 R689 A0 Strap CL@10K/ 4
STRAP1	RAMCFG[1]	USER defined	STRAP1 +3V_GPU ○ R709 Strap CL@10K/ 4 R708 B0 Strap CL@10K/ 4
STRAP2	RAMCFG[2]	USER defined	STRAP2 +3V_GPU ○ R671 Strap CL@10K/ 4 R665 C0 Strap CL@10K/ 4
STRAP3	RAMCFG[3]	USER defined	STRAP3 +3V_GPU ○ R680 Strap CL@10K/ 4 R679 D0 Strap CL@10K/ 4
STRAP4	PCIE_MAX_SPEED	Pull-down to GND	STRAP4 +3V_GPU ○ R719 CL@10K/ 4

N14P_GV2	H1/H2	S1/S2	M1/M2	S3	M3
ROM_SI	34.8K CS33482FB22	45.3K CS34532FB18	30.1K CS33012FB18	20K CS32002FB29	10K CS31002FB26

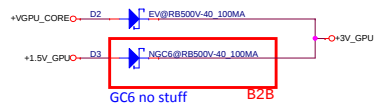
N14M_GL	Strap3	Strap2	Strap1	Strap0
H1	D0	C1	B1	A0
H2	D0	C1	B1	A0
H3	D0	C0	B1	A1
H4	D0	C1	B0	A0
S1	D0	C1	B0	A1
S2	D0	C1	B0	A1
S3	D1	C0	B1	A1
M1	D0	C0	B0	A1
M2	D0	C0	B0	A1
M3	D1	C1	B0	A1



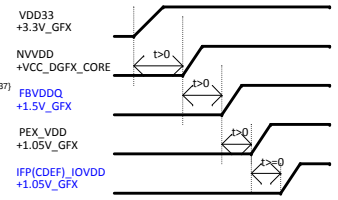
Power down sequence

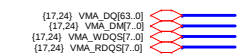


for meet Power down sequence for +3V_GFX



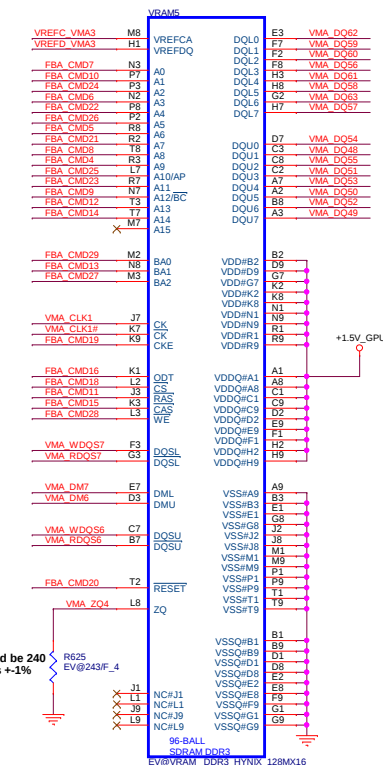
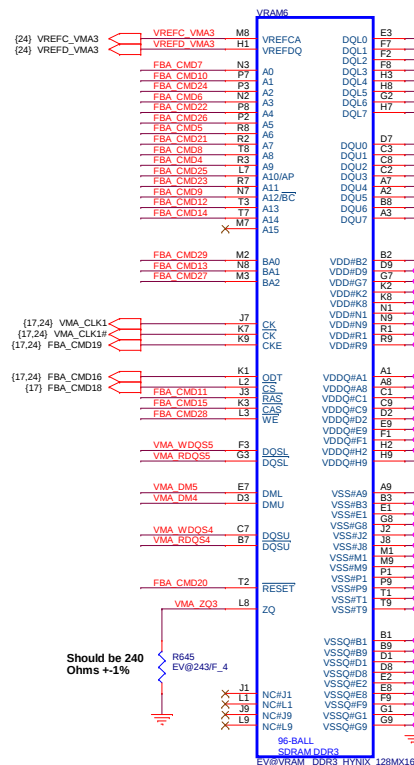
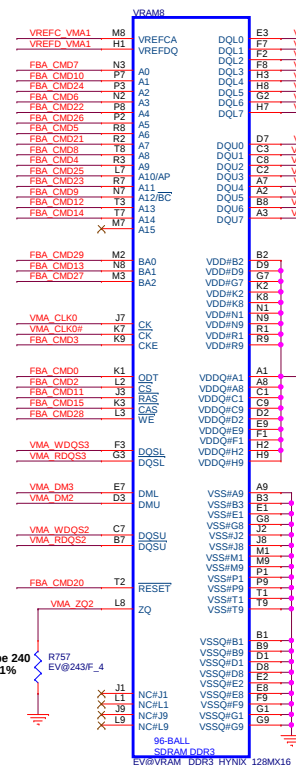
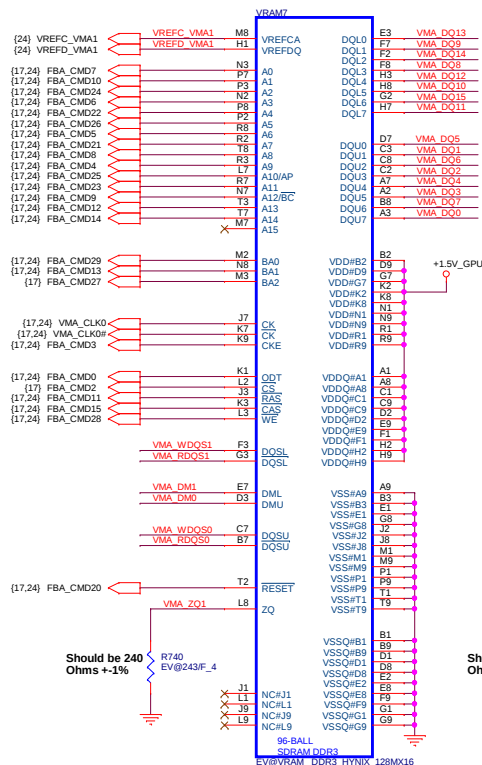
Power up sequence



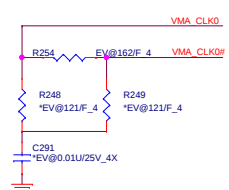


• DataBus [0:31]

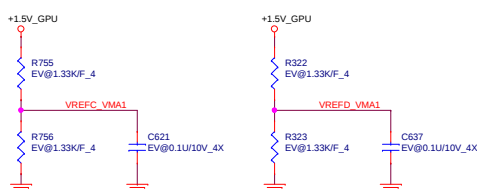
- DataBus [64:32]



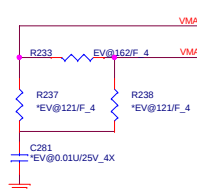
CLK-A0 Termination



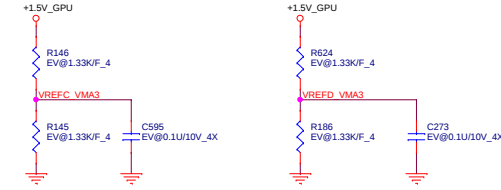
MEM Reference Voltage (Low)



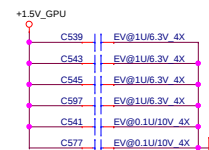
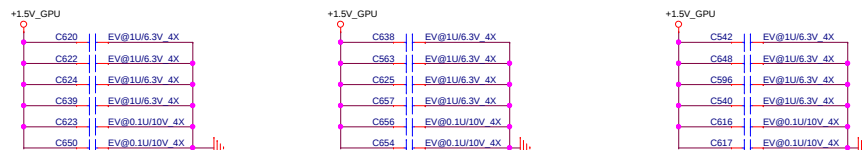
CLK-A1 Termination



MEM Reference Voltage (High Bus)



VRAM De-Coupling



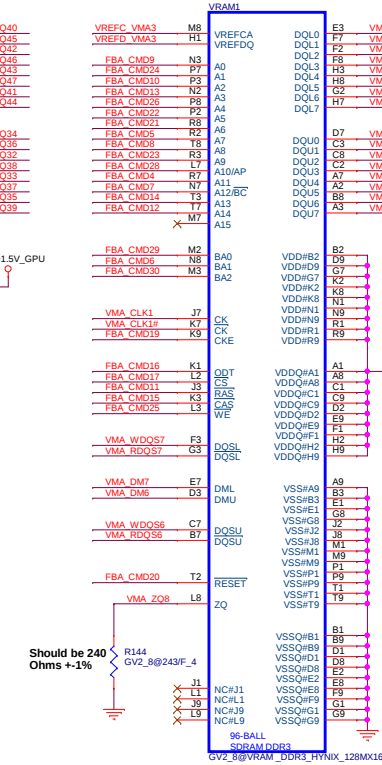
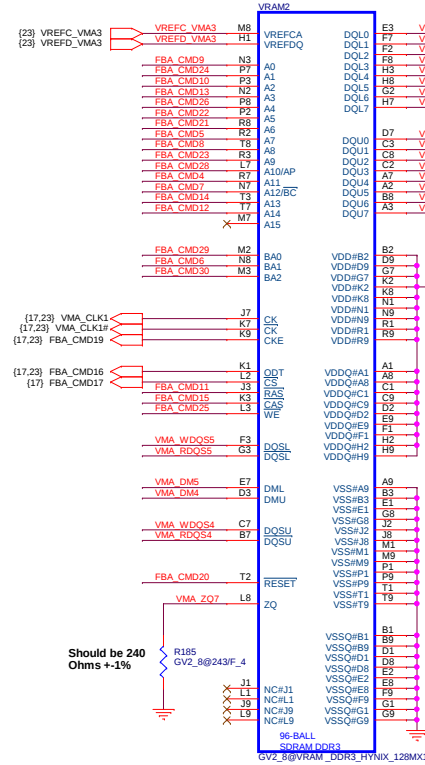
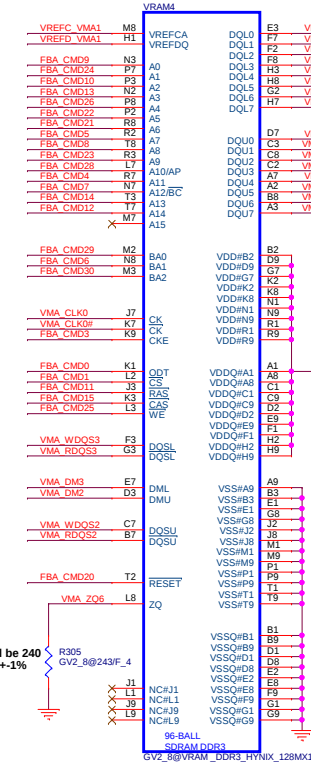
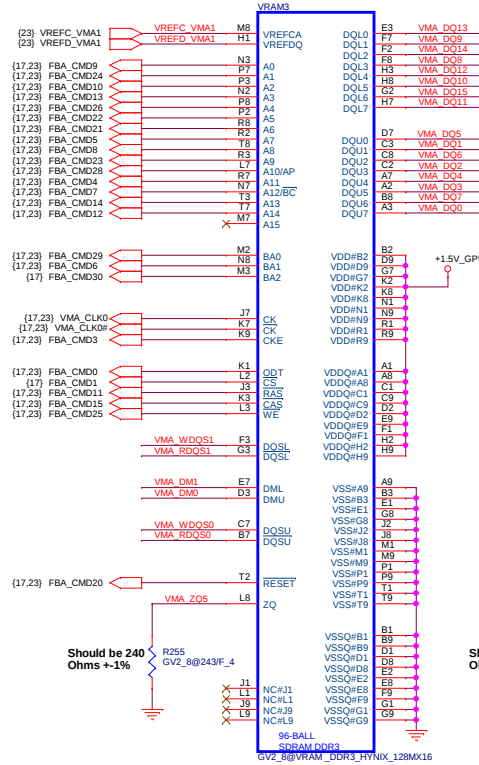
(17.23) VMA_DQ[63:0]
(17.23) VMA_DM[7:0]
(17.23) VMA_WDQS[7:0]
(17.23) VMA_RDQS[7:0]

RANK1: 256MB/512MB DDR3

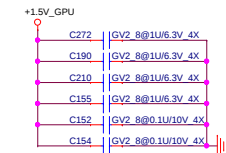
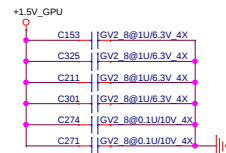
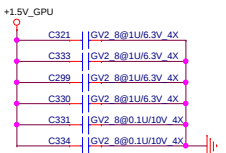
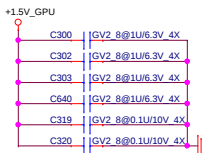
24

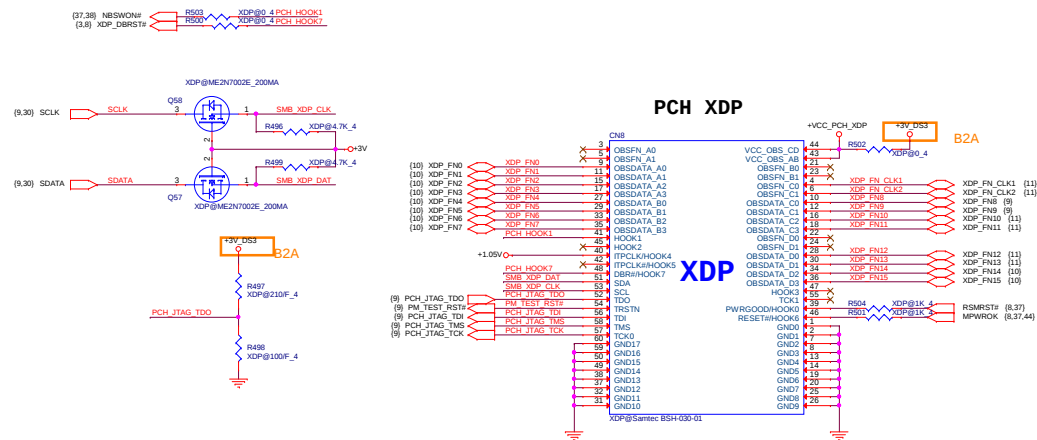
DataBus [0:31]

DataBus [64:32]



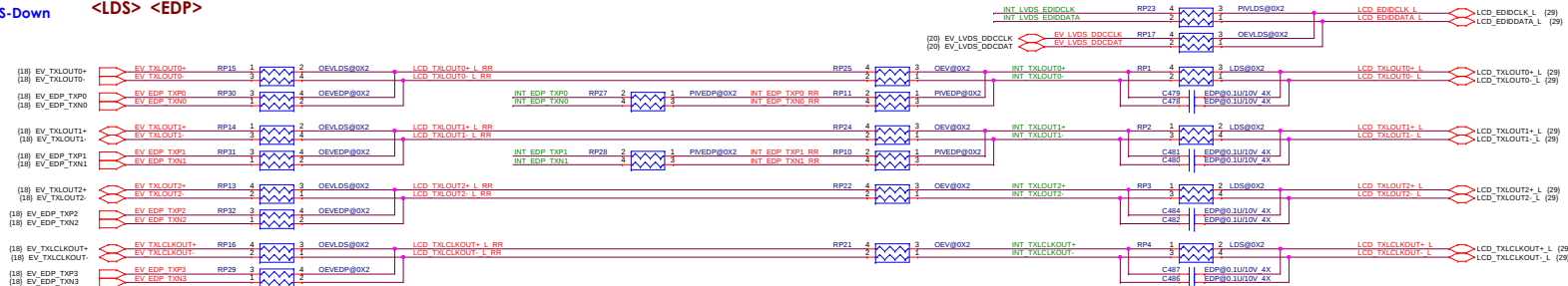
VRAM De-Coupling



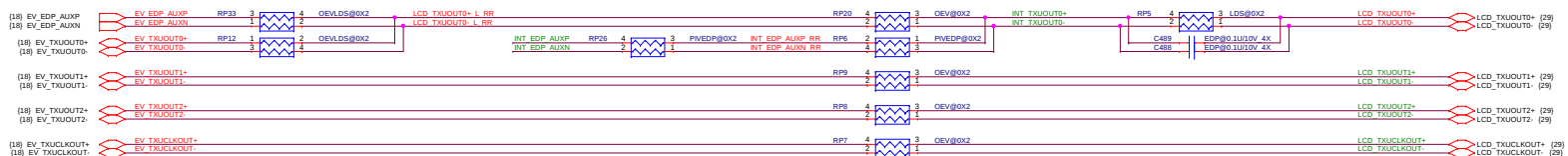


LVDS-Down

<LDS> <EDP>

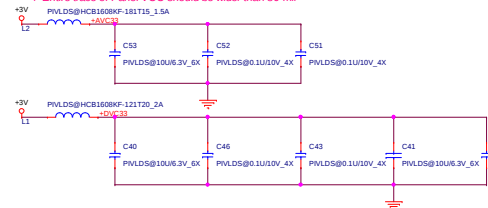


LVDS-Up



Note:

1. C1,C4,C7,C8,C9,C16 should be closed to chip
2. C9 should be X5R material
3. R8 should be 12K ohm with +/- 1%
4. Entire trace of Panel VCC should be wider than 80-mil

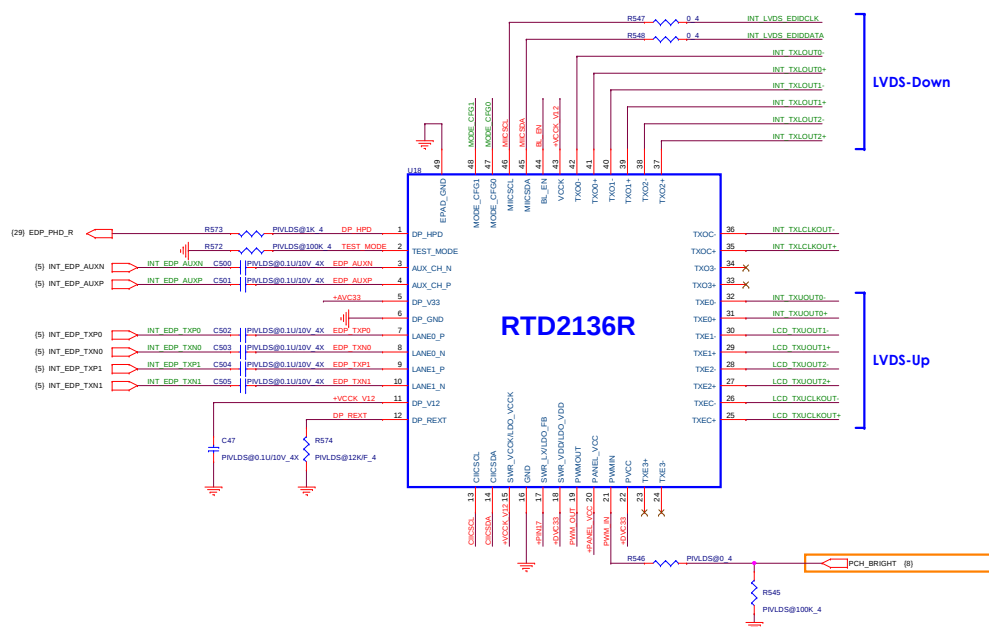


Mode Configure Table(Power On Latch)

		CFG0	
		0	1
CFG1	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

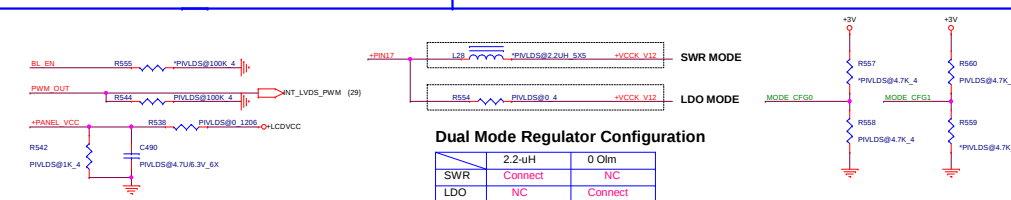
ROM ONLY Mode : CFG0 4.7K pull low, CFG1 4.7K pull high
 EP Mode : CFG0 4.7K pull high, CFG1 4.7K pull low
 EEPROM Mode : CFG0 4.7K pull high, CFG1 4.7K pull high

<LDS>



LVDS-Down

LVDS-Up

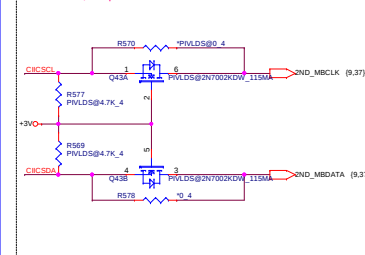


Dual Mode Regulator Configuration

	SWR	LDO
2.2-uH	Connect	NC
0 Ohm	NC	Connect

EP Mode

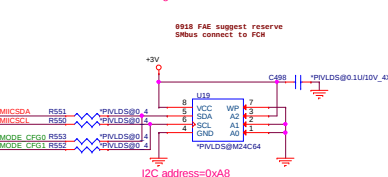
External device connect to DP2LVDS by Pin13/Pin14, I2C protocol is used



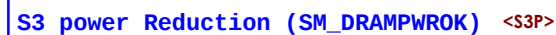
EEPROM Mode

In EEPROM mode, an additional EEPROM is needed. EEPROM should configure with following condition.

- 1- EEPROM with a size 8K-Byte
- 2- EEPROM device should be 2-byte addressing device
- 3- Slave address should configure as 0xA8



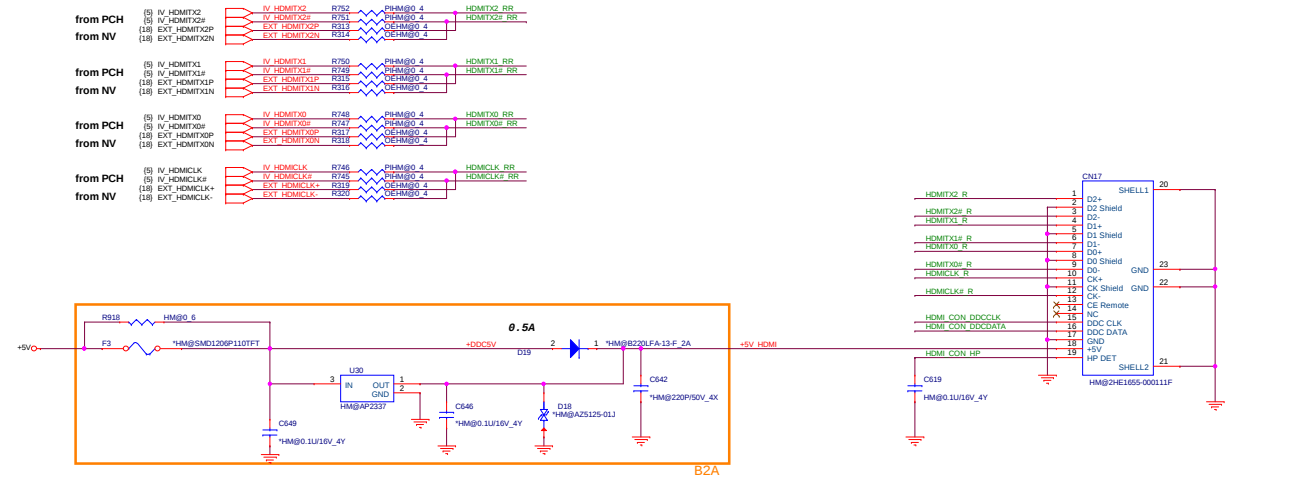
27



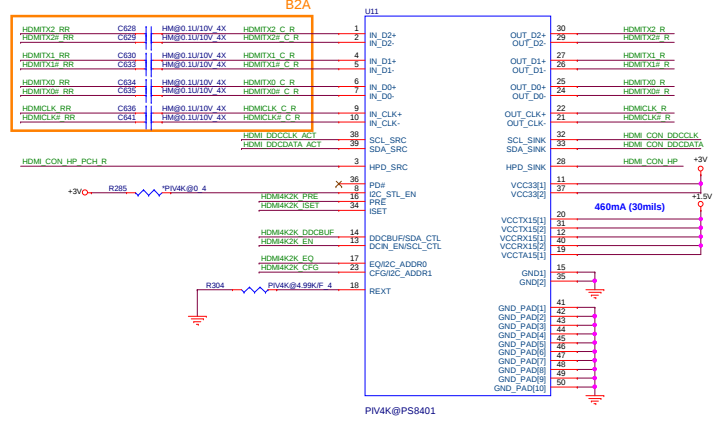
The three diagrams illustrate the connection of the MAIND pin to different power rails:

- Diagram 1 (Left):** Connects MAIND to +SMODR_VREF. It uses MOSFET Q6B (2N7002KDW, 115mA) with gate resistor R19 (0.8) and drain resistor R26 (100K_4).
- Diagram 2 (Middle):** Connects MAIND to +1.35V_CPU. It uses MOSFET Q12 (406402A) with gate resistor R128 (0.1206), drain resistor R114 (0.1206), and a drain capacitor C147 (470P550V_4K).
- Diagram 3 (Right):** Connects MAIND to +1.35V_CPU through a series of capacitors: C109 (0.1uF10V_4K), C104 (0.1uF10V_4K), C123 (0.1uF10V_4K), and C118 (0.1uF10V_4K). The MOSFET Q13 (ME2N7002E, 200mA) has a gate resistor R132 (220_8).

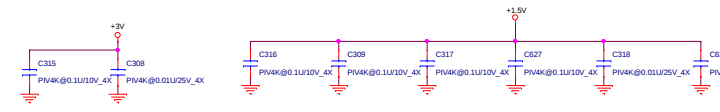
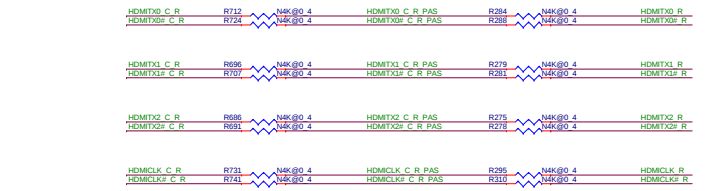
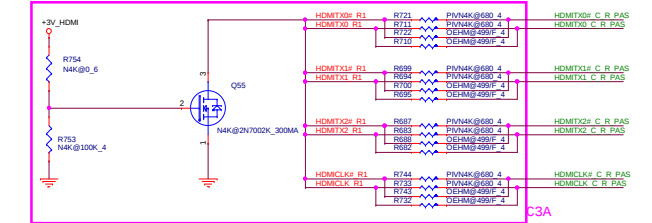
HDMI Conn <HDM>



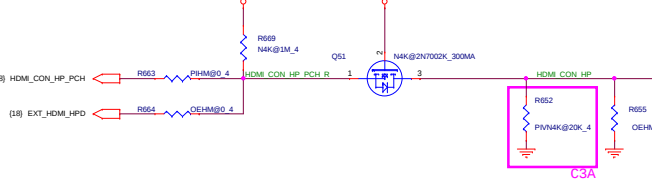
<HDM>



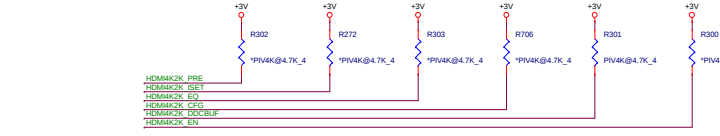
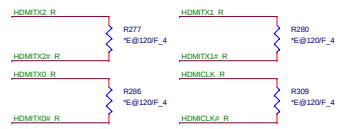
HDMI-passive level shift <HDM>



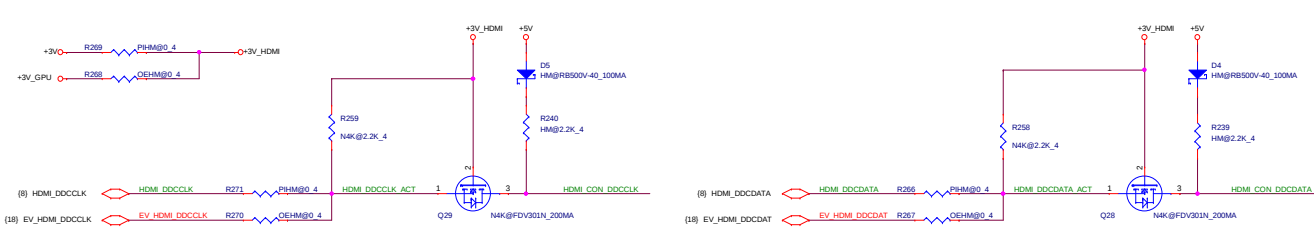
HDMI-HPD <HDM>



FOR EMI <EMC>



HDMI-SMBus <HDM>

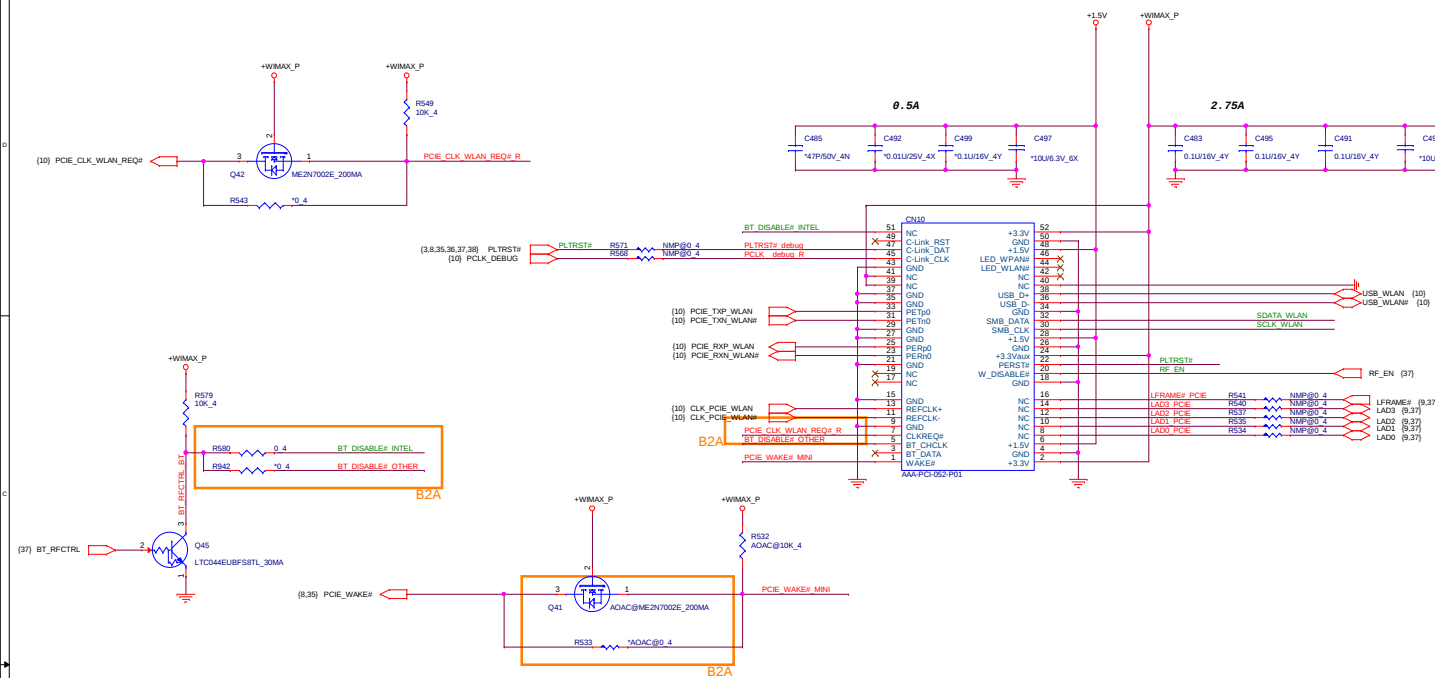


	Pre	ISET	EQ	CFG	DDCBUF	DCIN_EN
NC(Low)	0 dB	default	12.4 dB	HDMI ID disable	default	default, AC coupling input
1(High)	1.6 dB	+13%	4.3 dB	HDMI ID enable	active DDC buffer with default threshold	DC coupling input
M	2.5 dB	-13%	8.6 dB	N/A	active DDC buffer without internal pull up resistor	N/A

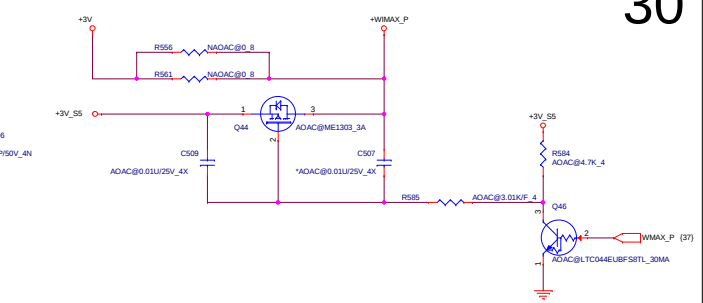
Pre	Output pre-emphasis setting
ISET	TMDS output swing adjustment
EQ	Receiver equalization setting
CFG	Configuration pin
DDCBUF	enable active DDC buffer
DCIN_EN	DC coupling enable

Pin	PS8401A	PS8201A
12	VDDRX	NC
15	GND	NC
34	ISET	NC
37	VDD33	NC

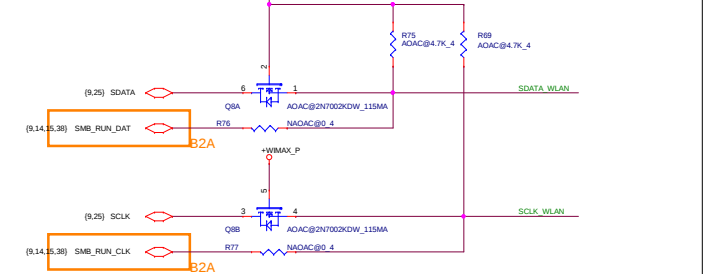
MINI Card Slot#1(WiFi / Wimax / Combo) <MNW>



AOAC <MNW>



SMBus(DDR3/WLAN/3G)

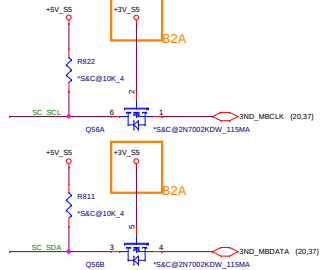


USB CONNECT RIGHT1 <U3B> <U2B> <SLC>

from PCH (10) USB20P_R1 USB20P_R1
(10) USB20P_R1 USB20P_R1

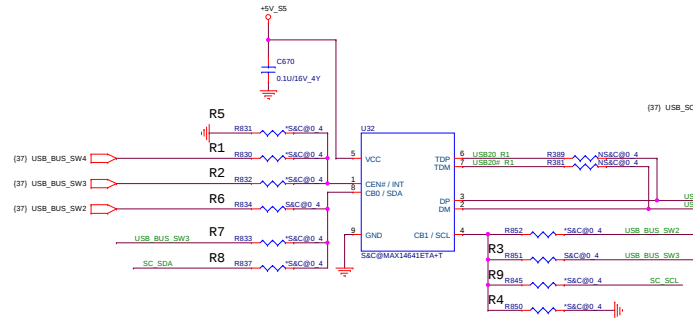
from PCH (10) USB30_RXN1_R USB30_RXN1_R
(10) USB30_RXP1_R USB30_RXP1_R

from PCH (10) USB30_TXN1_R USB30_TXN1_R
(10) USB30_TXP1_R USB30_TXP1_R



2012 Chief River/Brazos

2013 Shark bay / Kabini



	R1	R2	R3	R4	R5	R6	R7	R8	R9
14566		V	V	V					
14600		V	V			V			
14617(with CB2)		V	V			V			
14617(no CB2)			V		V	V			
14641/14642/14644			V			V			
14640							V	V	

SW2	SW3	14600
CB0	CB1	Status
0	0	Auto mode
0	1	Force dedicated charger mode
1	0	Pass-Through(USB) mode
1	1	pass-through(USB) with CDP Emulation

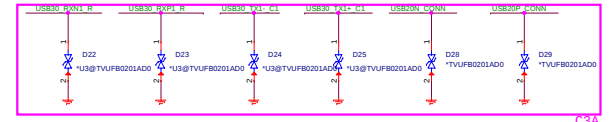
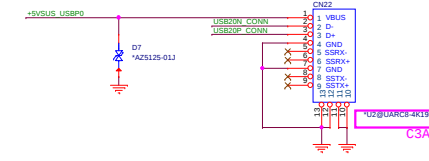
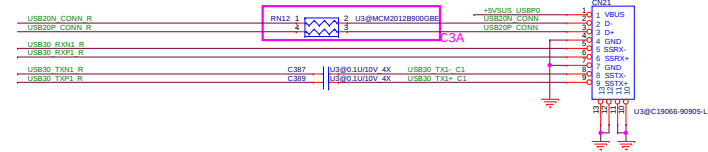
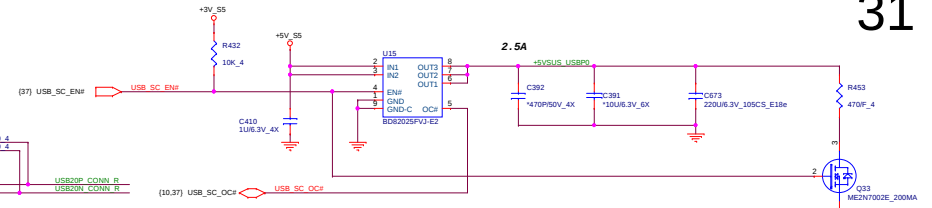
charger, AM
charger, FM
USB, PM
USB, CM

SW2	SW3	14641
CB1	CB0	Status
0	0	2A Auto mode for Apple device
1	0	Force 1A for Apple device
0	1	Pass-Through(USB) mode
1	1	pass-through(USB) with CDP Emulation

charger, AM2
charger, AP1
USB, PM
USB, CM

SW2	SW3	14642
CB1	CB0	Status
0	0	2A Auto mode for Apple device
X	1	Pass-Through(USB) mode
1	1	pass-through(USB) with CDP Emulation

Charger, AM2
Charger, FM
USB, PM
USB, CM

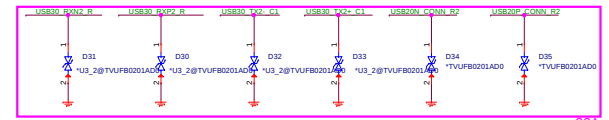
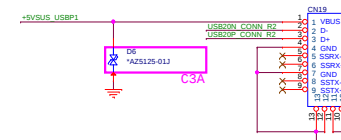
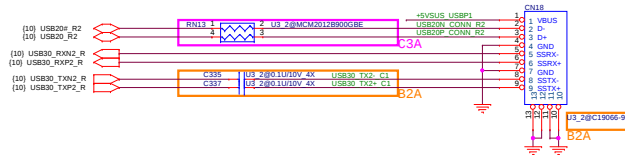


C3A

USB CONNECT Right2 <U3B>

from PCH

from PCH

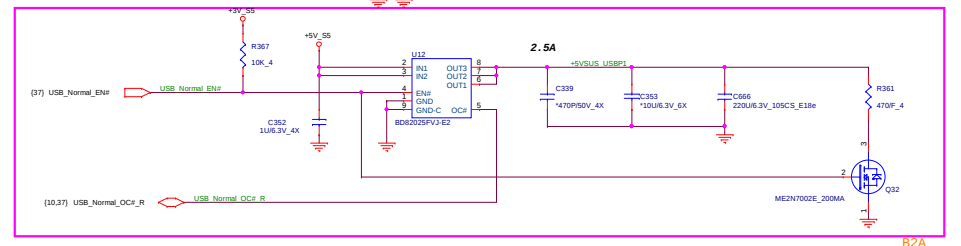
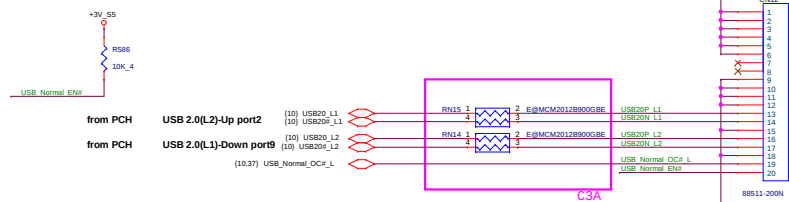


C3A

USB CONNECT Left1/Left2 <U2B>

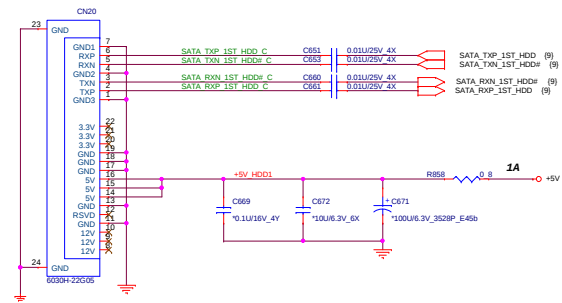
from PCH

from PCH

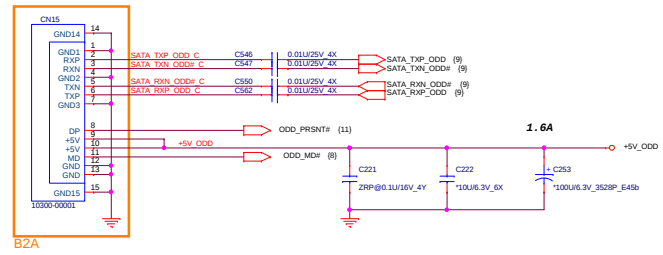


B2A

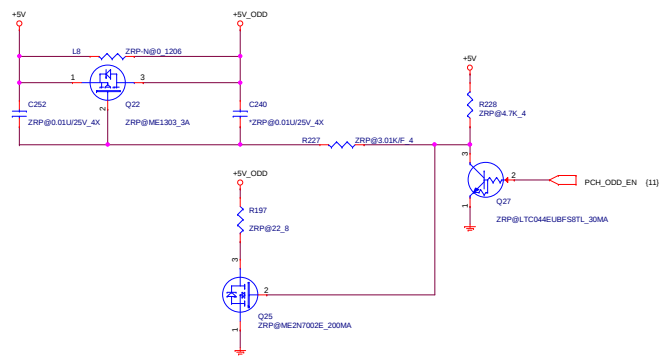
SATA HDD <HDD>

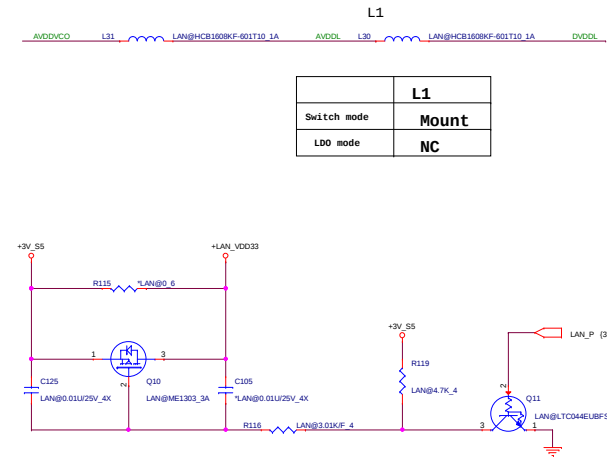


SATA ODD <ODD>

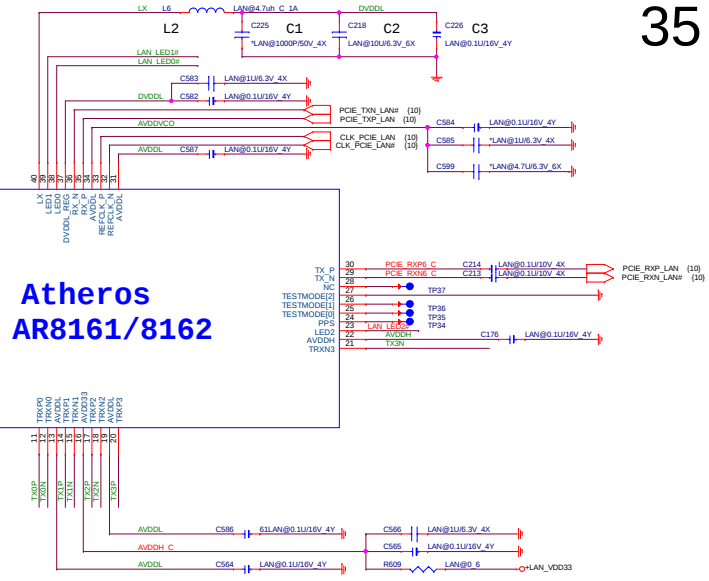


ODD Zero power . (Only for Intel) <OZP>

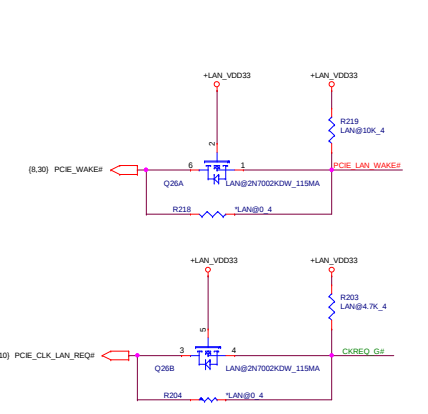




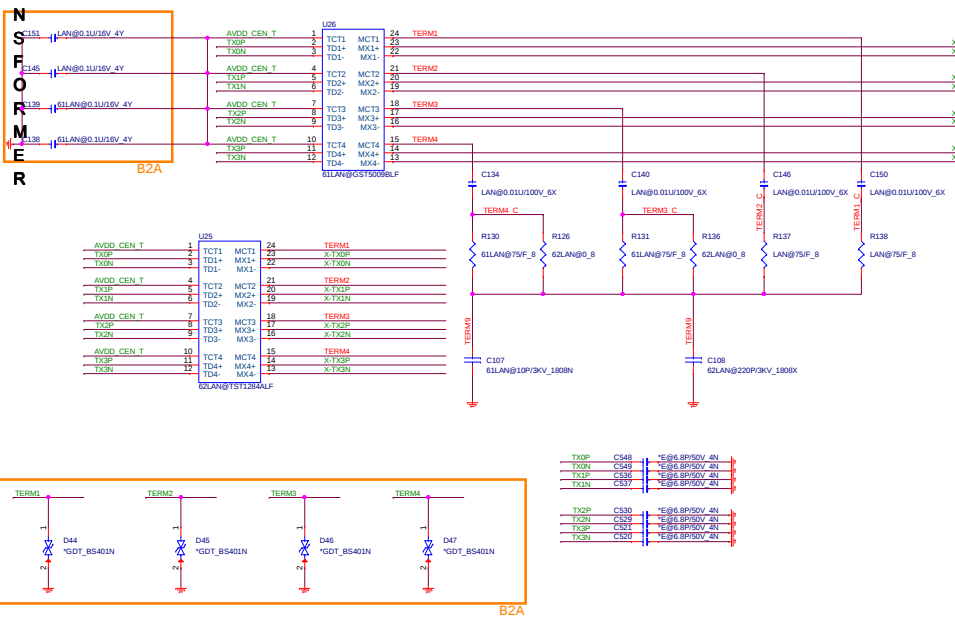
	L2, C1, C2, C3
Switch mode	Mount
LDO mode	NC



Atheros
AR8161/8162

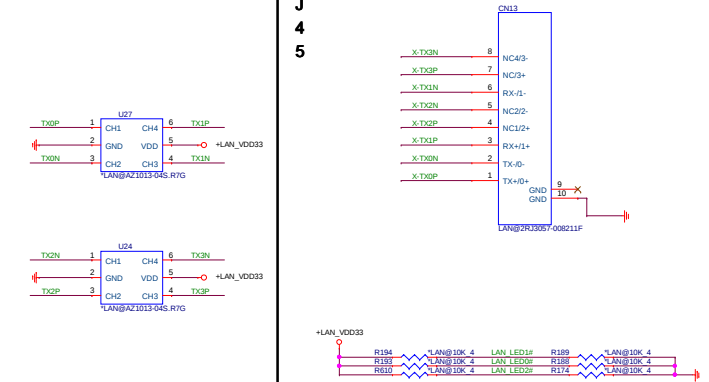


T	<LAN/LN1.LNG>
---	---------------



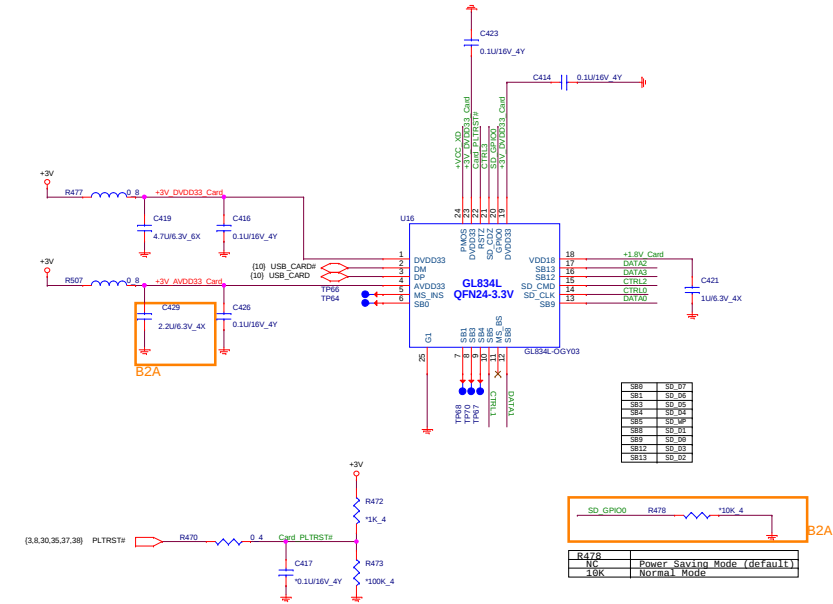
Quanta P/N : CYBS401N201

R <LAN>



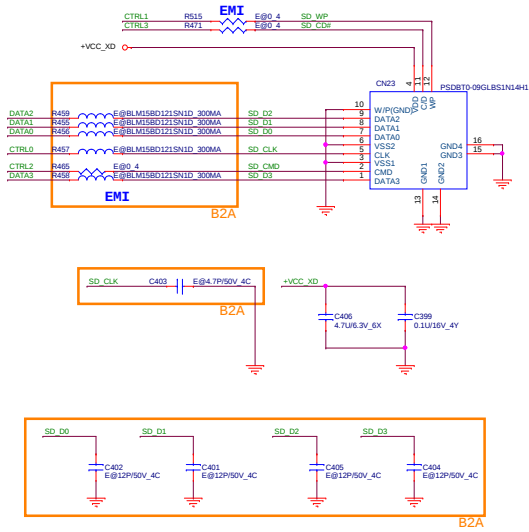
LED0 = LAN_ACTLED	1	High core voltage(default=1)
	0	Low core voltage
LED1 = LAN_LINKLED#	1	Switch mode regulator (SWR) select
	0	Linear regulator (LDO) select
LED2	1	25 MHz external clock input
	0	48 MHz external clock input

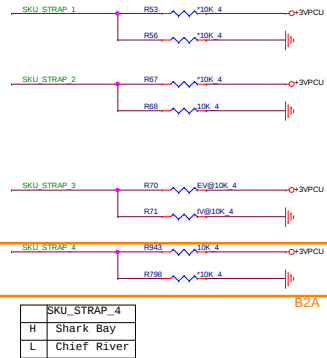
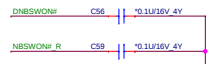
Card Reader (GL834L) <MMC>



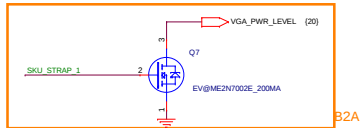
2 IN 1 Card Reader <MMC>

36

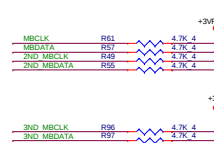




	Capetown@/Aswan@	EV@ / IV@
MS Strap	SKU_STRAP_2	SKU_STRAP_3
14" Capetown UMA	1	0
14" Capetown DIS	1	1
17" Aswan UMA	0	0
17" Aswan DIS	0	1



SM BUS PU/Address <KBC>

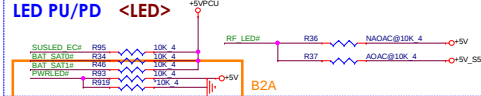
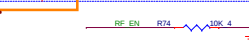


SMBUS	Devices	Address
1	Battery(A)	
2	PCH(S5)	
	G-sensor(S0)	
	IDROM(A)	
3	VGA Thermal(S0)	
	CEC(A)	

TP <KBC>



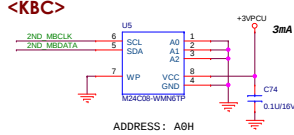
LED PU/PD <LED>

Strap(795) <KBC>
SHRM

INTERNAL KEYBOARD STRIP SET <KBC>



ID EEPROM <KBC>



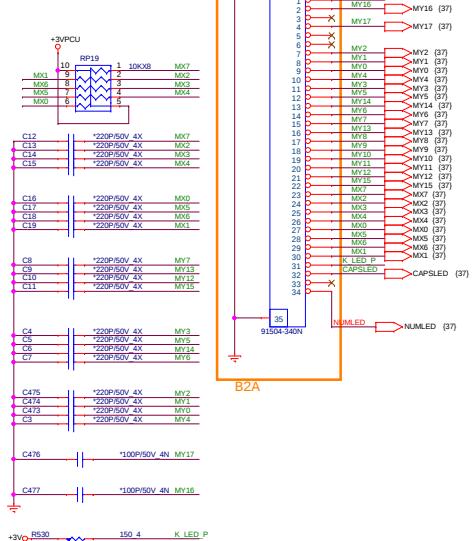
SPI FLASH <KBC>



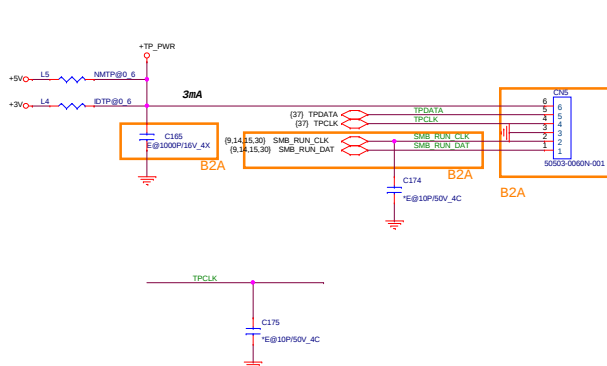
HWPG circuit <KBC>



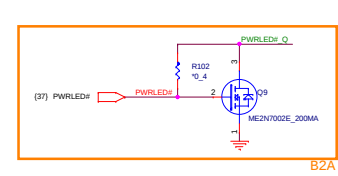
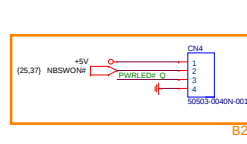
INT KeyBoard <KBC>



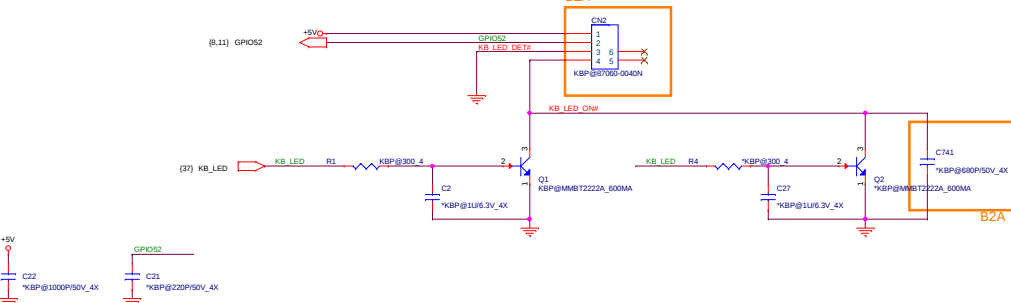
TP board <TPD>



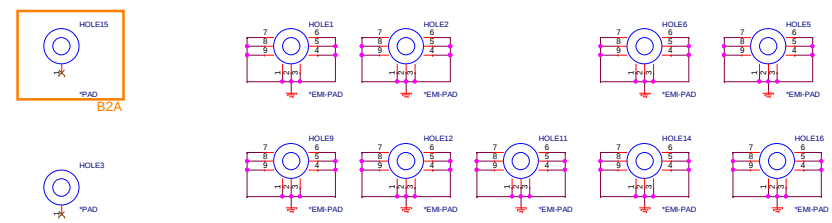
Power board w LED <PSW>



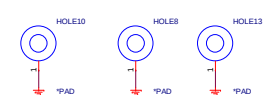
K/B LED power < KBF



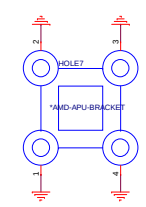
HOLE



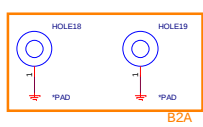
VGA HOLE



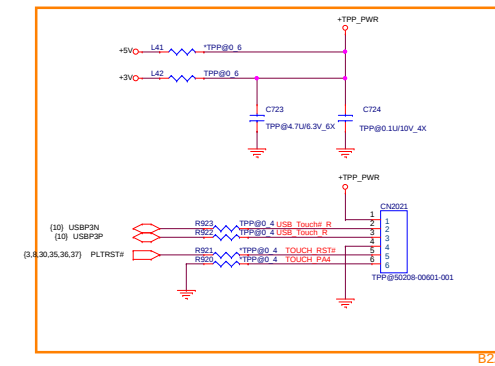
CPU HOLE



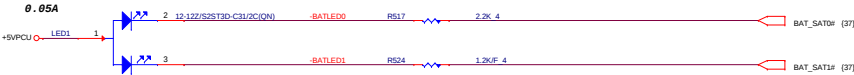
MINI Card NUT



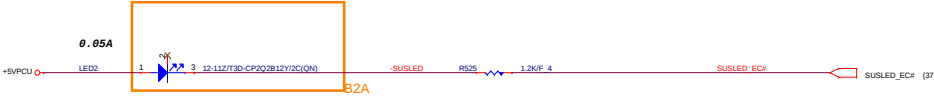
TOUCH PANEL <TPP>



LED-Battery <LED><W+A>



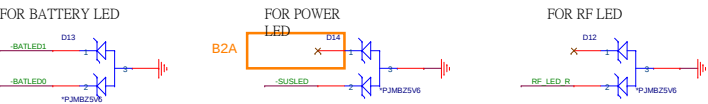
LED-Power <LED><W+A>



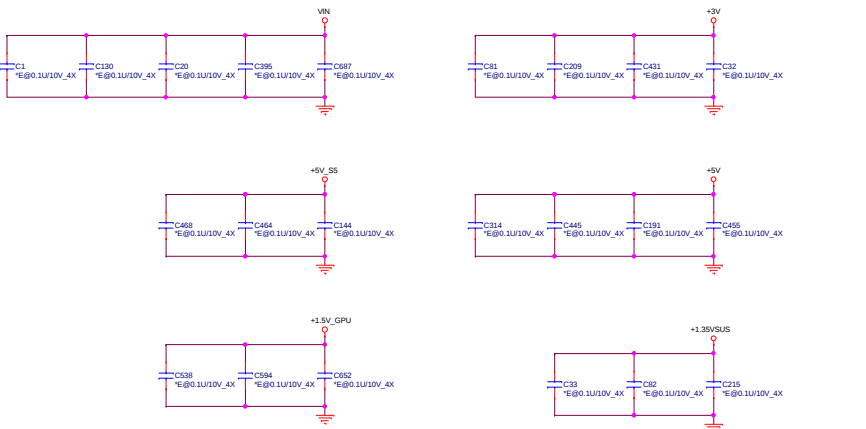
LED-WIFI <LED>

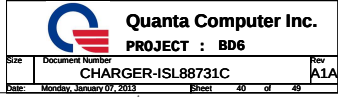


ESD Protect <EMC>



EMI <EMC>



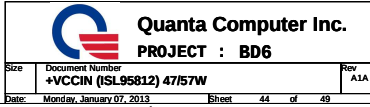


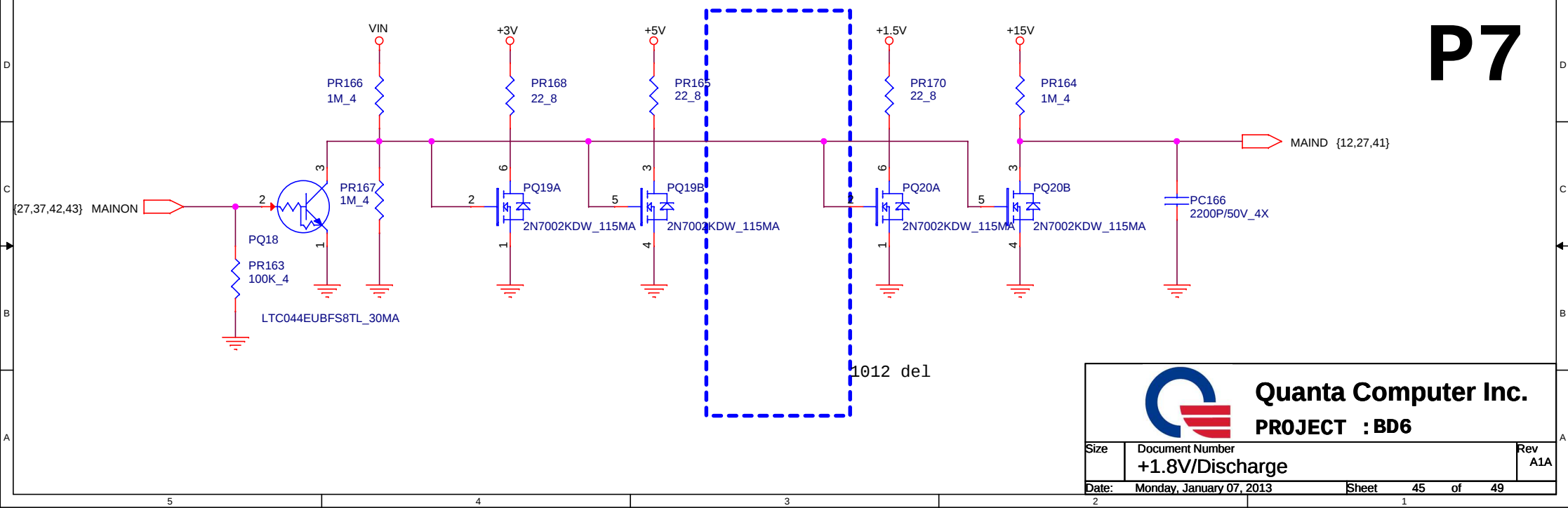




O

0



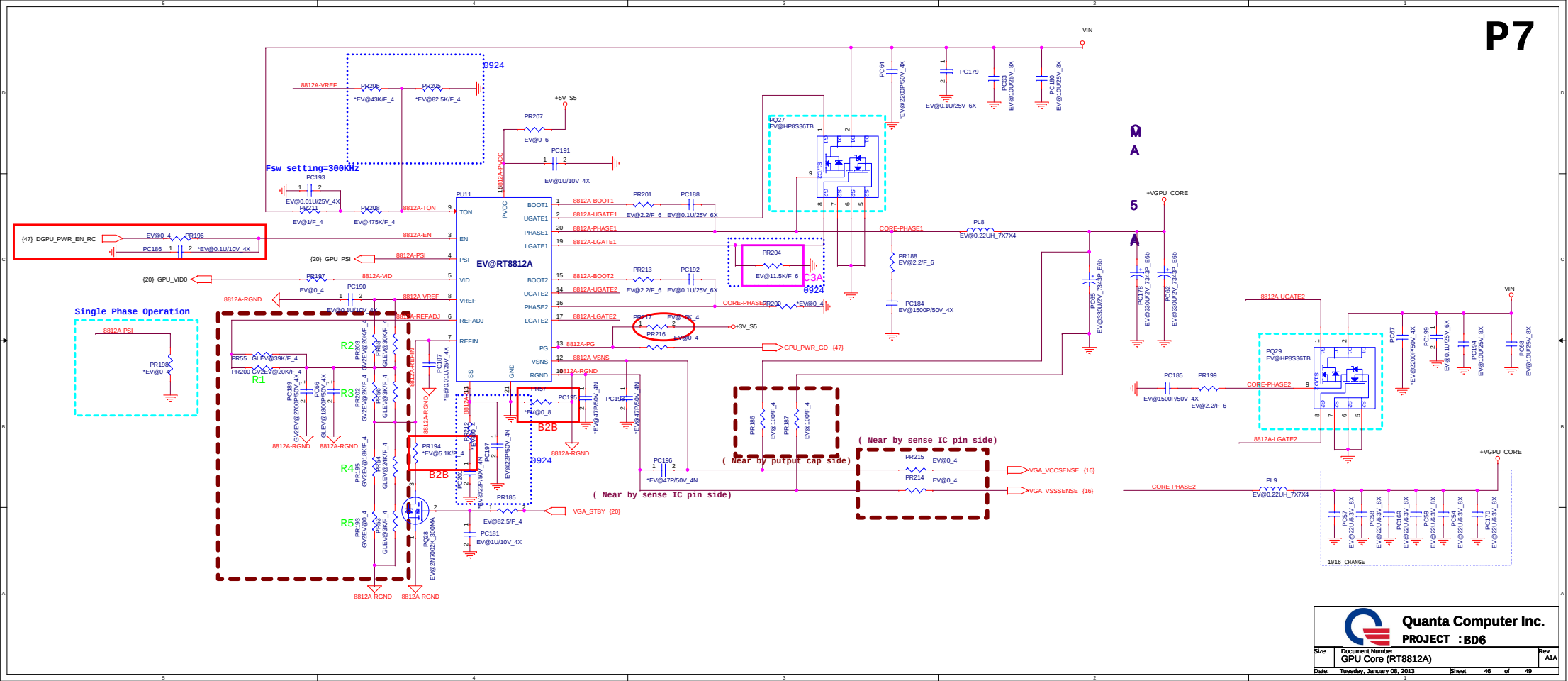




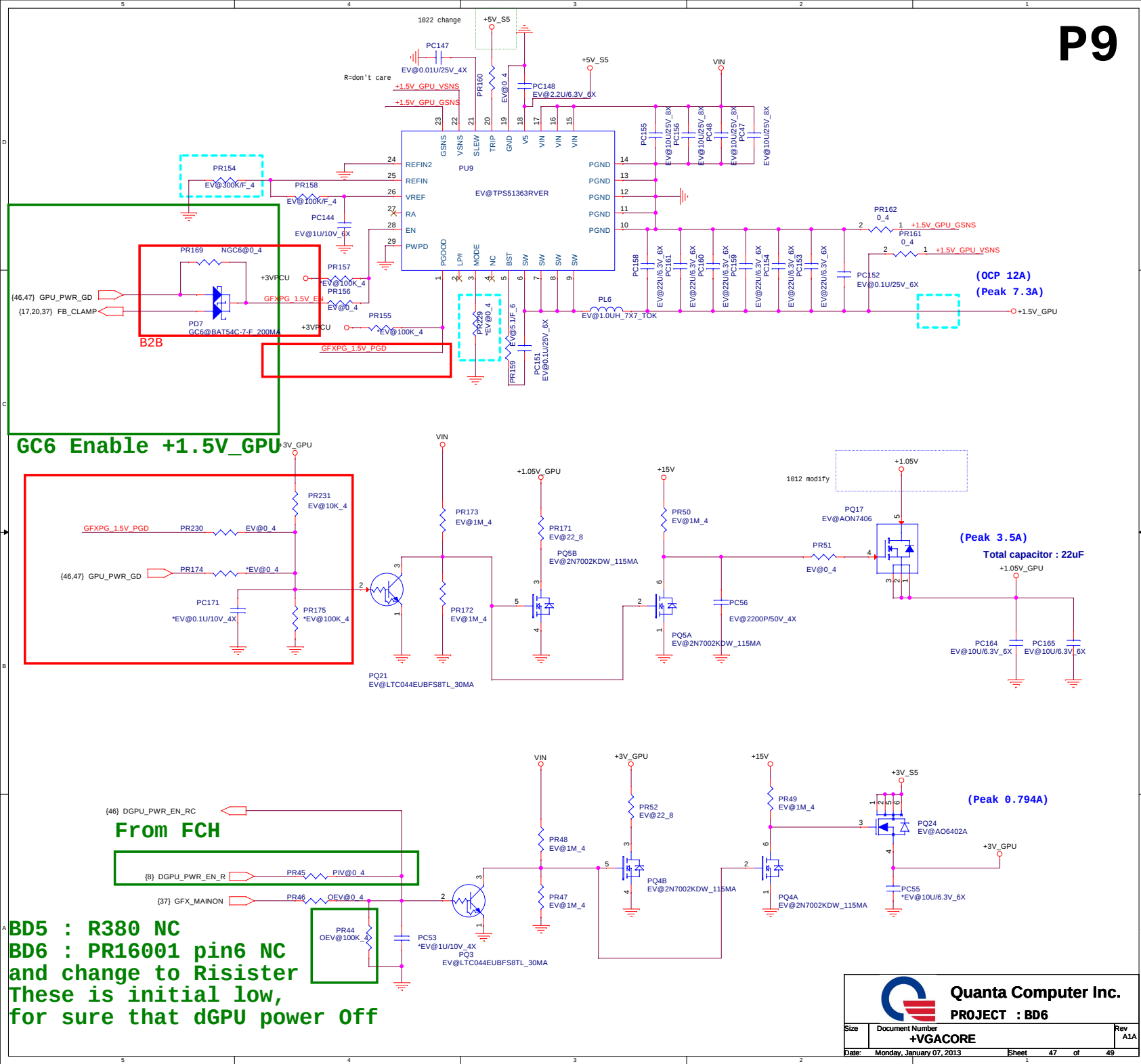
Quanta Computer Inc.

PROJECT : BD6

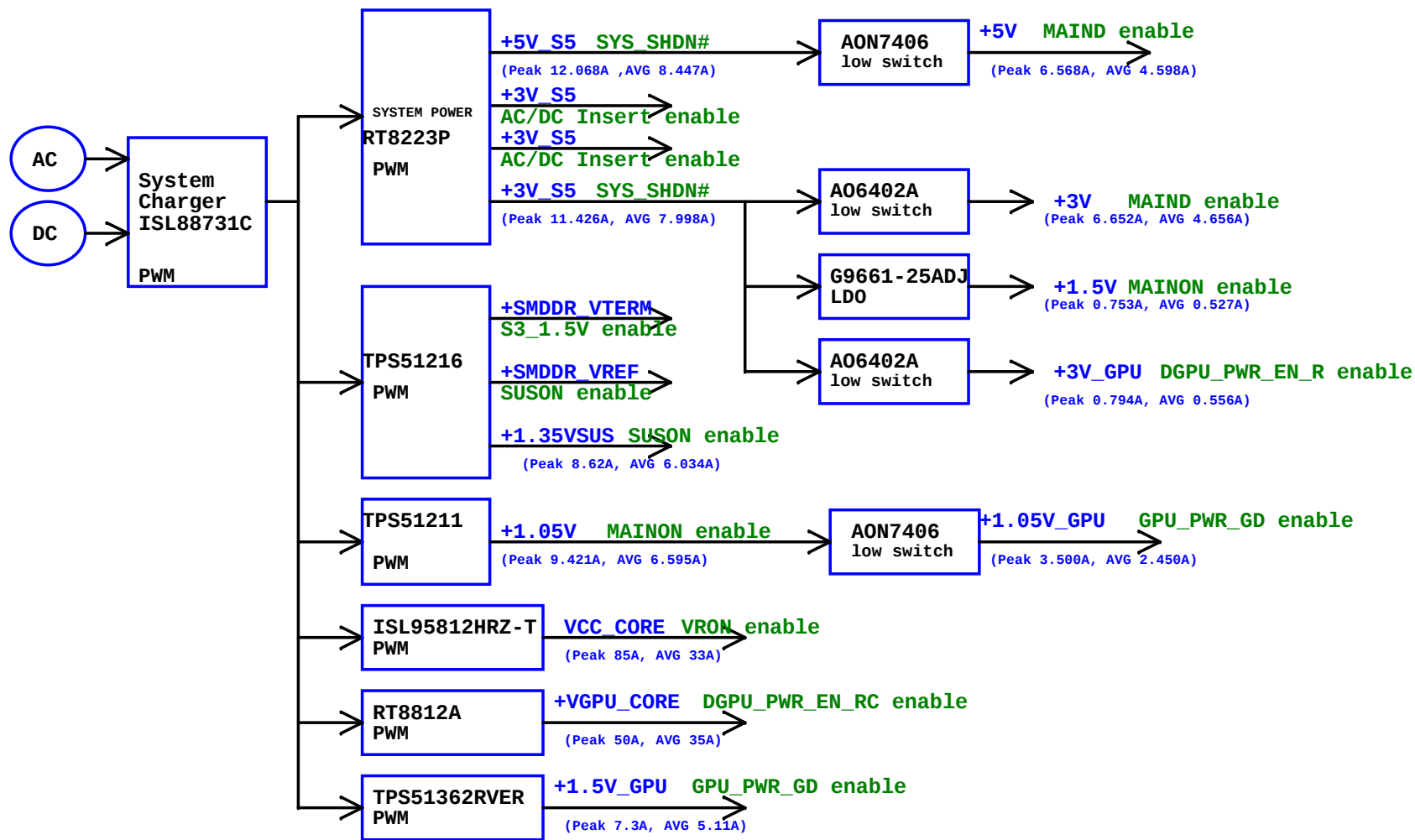
Size	Document Number	Rev
	+1.8V/Discharge	A1A
Date:	Monday, January 07, 2013	Sheet 45 of 49



 Quanta Computer Inc. PROJECT : BD6		
Size	Document Number	Rev
	GPU Core (RT8812A)	A1A
Date:	Tuesday, January 08, 2013	Sheet 46 of 49



BD5 : R380 NC
 BD6 : PR16001 pin6 NC
 and change to Resister
 These is initial low,
 for sure that dGPU power Off



Model		REV	CHANGE LIST				MODEL		BD6			
							PAGE	FROM	To			
BD6 MB	A1A	First Release						1				
	B2A	PAGE 3: Change C510,C508 size and stuff R926,add R148,R152						2				
		PAGE 6: add C728,C729						3				
		PAGE 7: add R929,R930,demount R927,R928,R82,R566,R81						4				
		PAGE 8: modify R425,R412,R398,R397,R404,R405,R414,R146,R854,R862 value to DS3						5				
		PAGE 9: change GPIO13 to BOARD_ID16,GPIO23 to BOARD_ID17,change R819,R816,R821,R824,R814,R818,R813,R823 value dor XDP						6				
		PAGE 10: add USB port3 for Touch Panel function,add R897,R901,R364,R902,R903,R905,R898,R906,Q60,Q59 for DS3,change C667,C668 to 12PF						7				
		PAGE 11: change R407,R408,R879,R880,R907,R349,R342,R343,R910,R911,R912,R913,R908,R909 for BOARD_ID select						8				
		PAGE 12: change R338,R328 size,change C411,D11,R436,Q35 value and add R434,R435 for DS3						9				
		PAGE 15: Change C188 size to 0402.						10				
		PAGE 16: Change R201,R196,Q23,Q61,Q24 value						11				
		PAGE 18: change C725,C726,C727 value						12				
		PAGE 19: add R914 for XTAL,and change R291,R292 value						13				
		PAGE 20: change R293,R728,R294,R915,R916 value						14				
		PAGE 21: add R917 for co-lay						15				
		PAGE 22: change C279,C604 value						16				
		PAGE 26: add U33,R938,C738						17				
		PAGE 27: add R939,C739,U34 for DS3						18				
		PAGE 28: change R918,F3,U30,D19,C628,C629,C630,C633,C634,C635,C636,C641 value for HDMI						19				
		PAGE 29: change R937,R64,R9,C26,C28,C29,MR1,F1,R24,R539,R25,R536,R22 value						20				
		PAGE 30: change R58,R942,Q41,R533 value for AOAC						21				
		PAGE 31: add D6,D22,D23,D24,D25,D28,D29,D31,D30,D32,D33,D34,D35 for ESD,change C339,C353,R361,R367,U12,C666,C335,C337,Q32 value						22				
		PAGE 33: change CN15 value						23				
		PAGE 34: add D36,D37,D38,D39,D40,D41,D42,D43 for ESD						24				
		PAGE 35: change C195,C179,C151,C145,C139,C138 value,add D44,D45,D46,D47 for ESD						25				
		PAGE 36: change R459,R455,R456,R457,R465,R458,R478,C403,C402,C401,C405,C404 value						26				
		PAGE 37: change R91,Q7 value,add R943,R798 for STRAP select						27				
		PAGE 38: change CN1,CN2,CN5,CN4,R102,Q9 value and change C165 value for EMI,and add L41,L42,C723,C724,CN2021,R920,R921,R922,R923 for Touch PAD Panel function						28				
		PAGE 39: change LED2 symbol						29				
		B2B	PAGE 20: change R656 value						30			
			PAGE 22: change D4 value						31			
		C3A	PAGE 14: change C192 size to 0402,chaneg C734,C735,R933,R934 value for DS3						32			
			PAGE 28: change Q55,R754,R753,R721,R711,R694,R699,R678,R683,R744,R733,R652 value for HDMI 4K2K						33			
			PAGE 31: change RN12,RN13,RN14,RN15 pin define						34			
			PAGE 34: change C490,C501 size to 0402						35			
			PAGE 36: change C476 size to 0402						36			
									37			
									38			
									39			
									40			
									41			
									42			
									43			
DOC NO. 204		PROJECT MODEL :		BD6	APPROVED BY:	Kent Su	DATE:	2012/12/14	 Quanta Computer Inc. PROJECT : BD6 Size: Document Number: Change list Rev: D2A Date: Thursday, January 03, 2013 Sheet: 50 of 50			
		PART NUMBER:			DRAWING BY:	Kent Su	REVISION:					