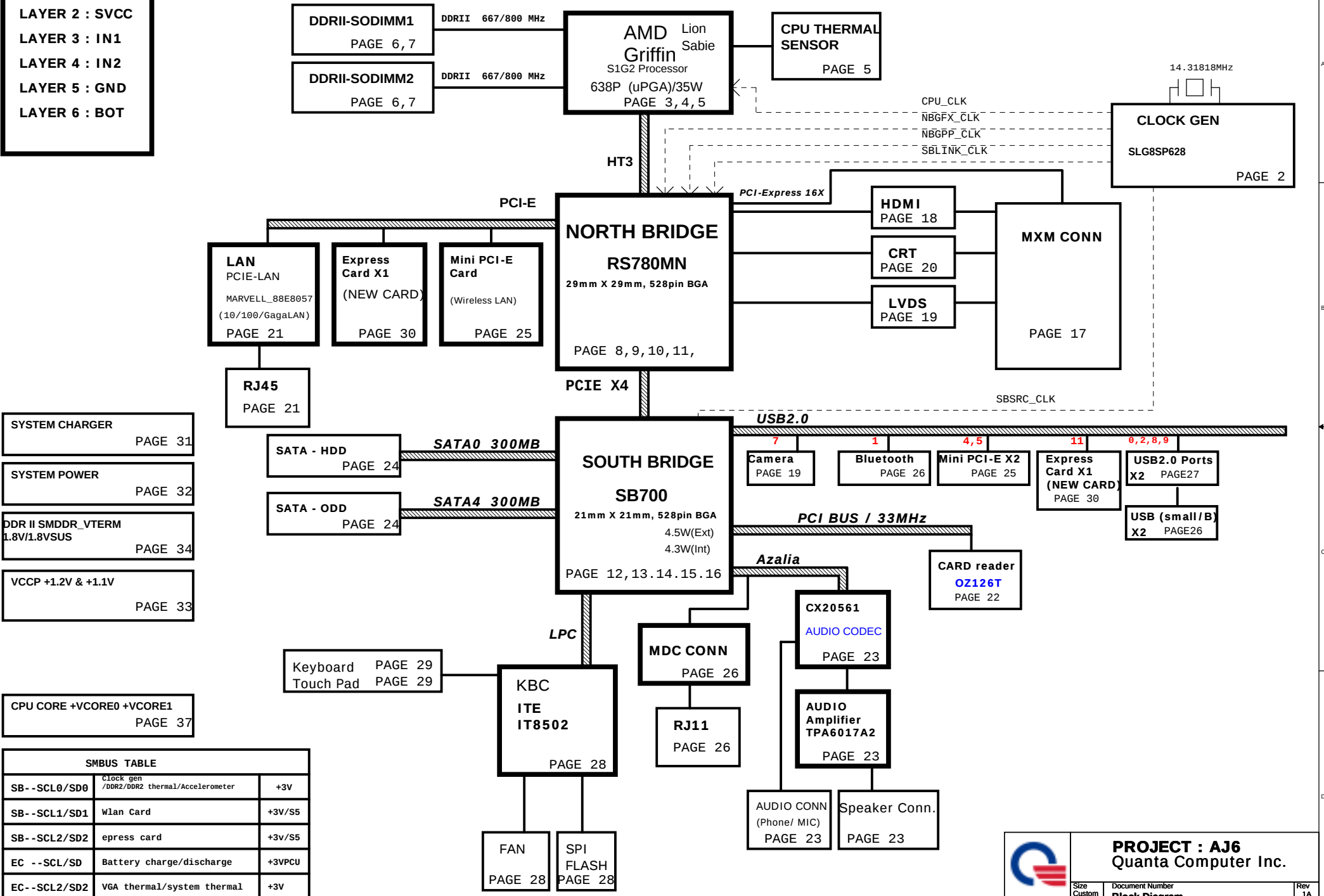


PCB STACK UP

LAYER 1 : TOP
LAYER 2 : SVCC
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : GND
LAYER 6 : BOT

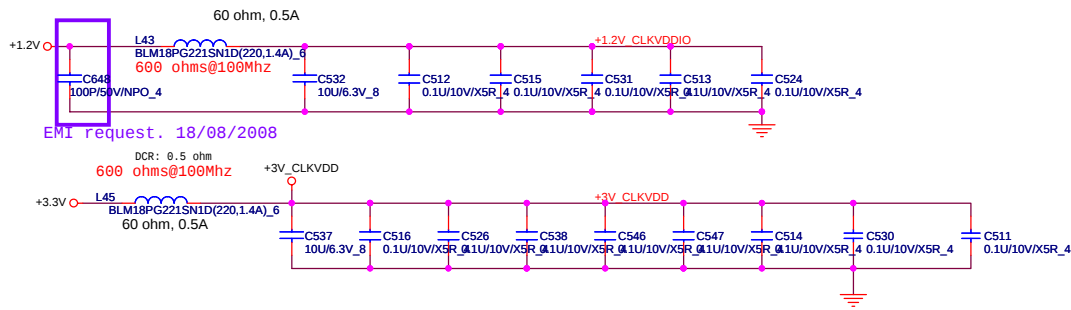
AJ6 SYSTEM DIAGRAM



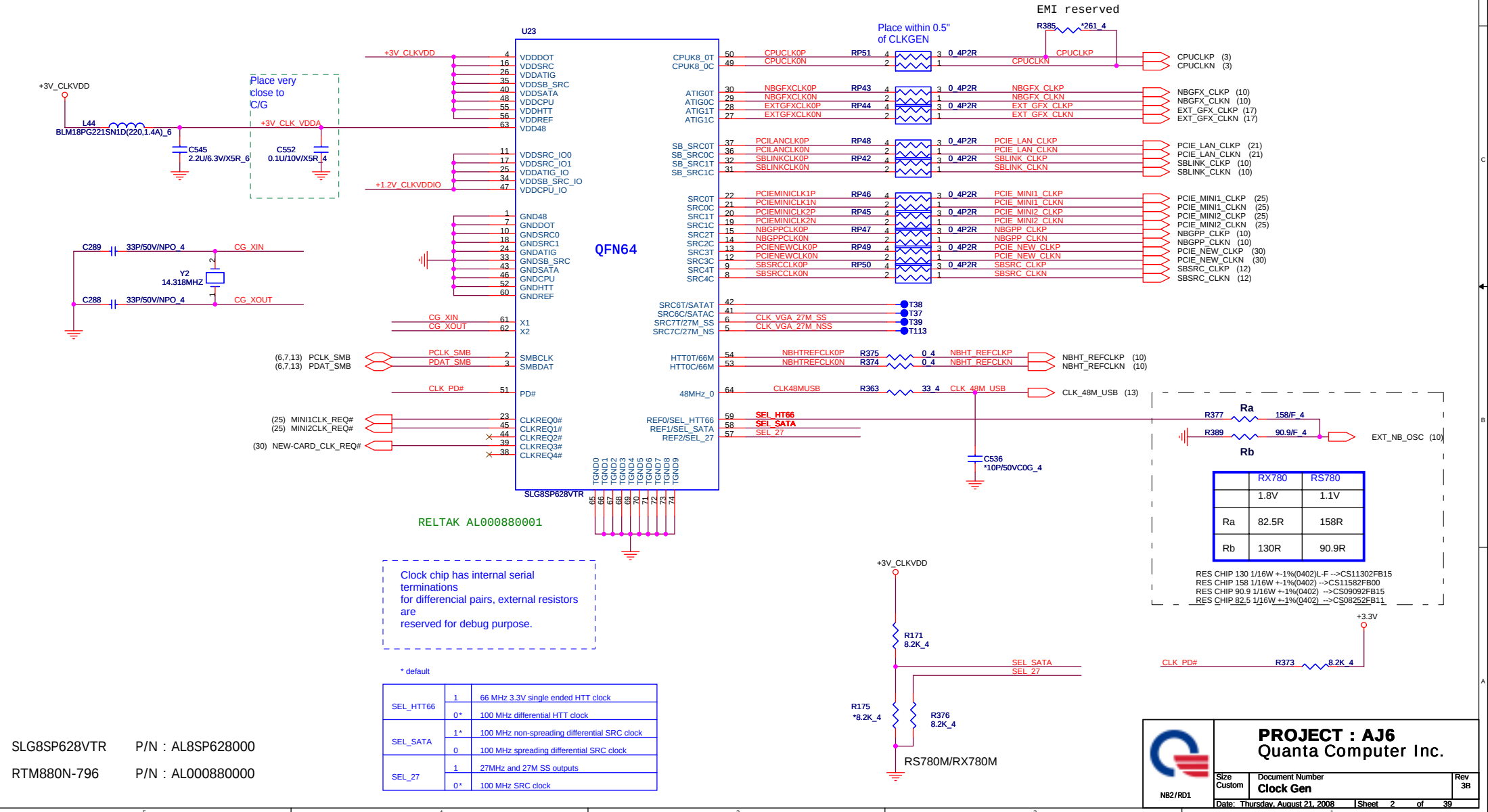
SMBUS TABLE			
SB--SCL0/SD0	Clock gen /DDR2/DDR2 thermal/Accelerometer	+3V	
SB--SCL1/SD1	Wlan Card	+3V/S5	
SB--SCL2/SD2	epress card	+3V/S5	
EC --SCL/SD	Battery charge/discharge	+3VPCU	
EC--SCL2/SD2	VGA thermal/system thermal	+3V	

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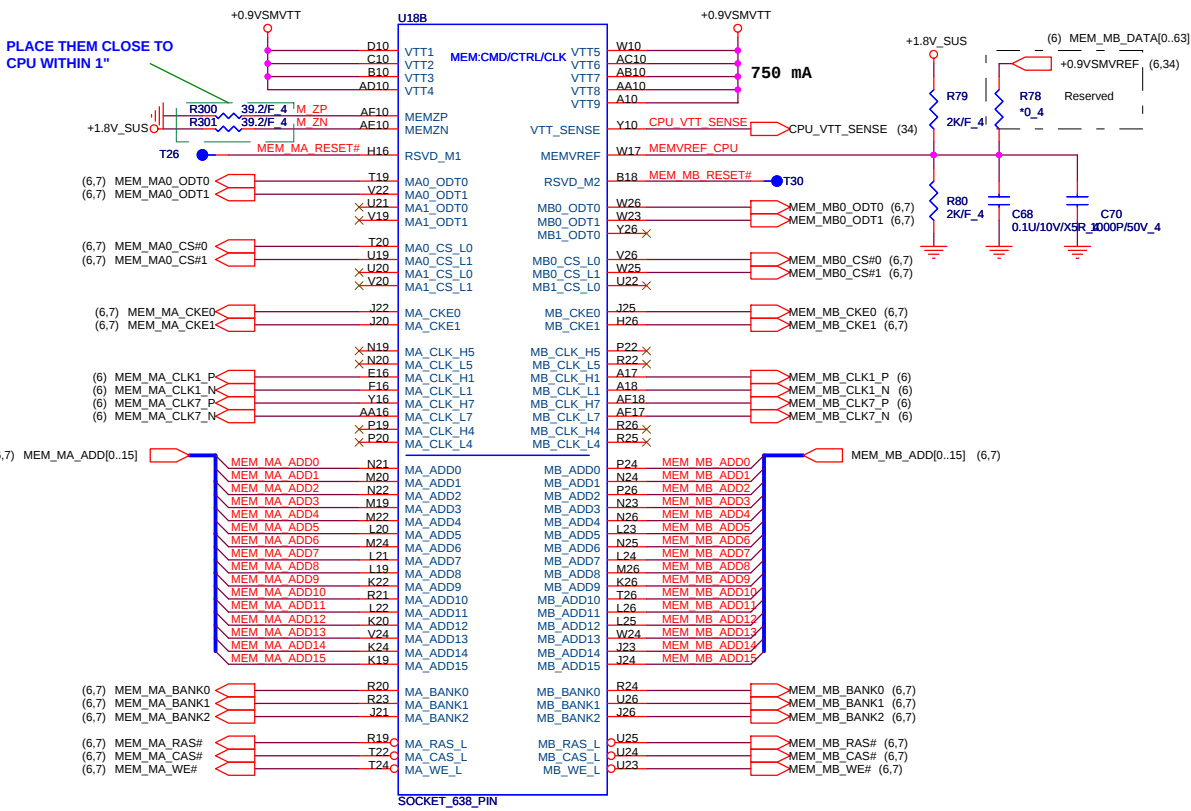
Size Custom	Document Number	Rev 1A
Block Diagram		
Date: Monday, August 18, 2008	Sheet 1 of 39	



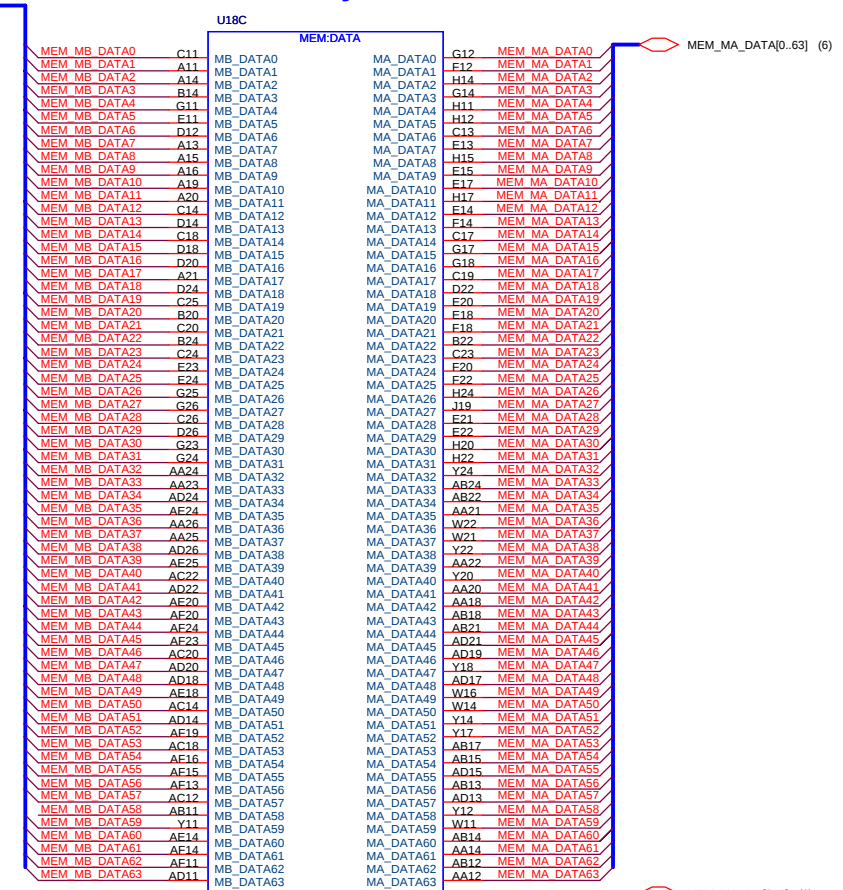
CLOCKS name	UMA	RS780	Clock pin function
NBGF_X_CLKP NBGF_X_CLKN	RP64 STUFF	RP64 STUFF	to NB for VGA reference clock
EXT_GFX_CLKP EXT_GFX_CLKN	RP5053 NC	RP5053 STUFF	to M86-M external reference clock
NBPPP_CLKP NBPPP_CLKN	RP70 STUFF	RP70 NC	to NB for RX780 for PCIEX2 interface reference clock only RS780 is internal share with AC-LINK clock, RS780 not need
SBLINK_CLKP SBLINK_CLKN	RP72 STUFF	RP72 STUFF	to NB for AC-LINK reference clock



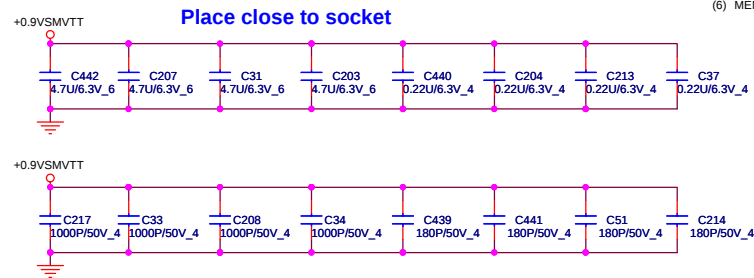
PLACE THEM CLOSE TO CPU WITHIN 1"



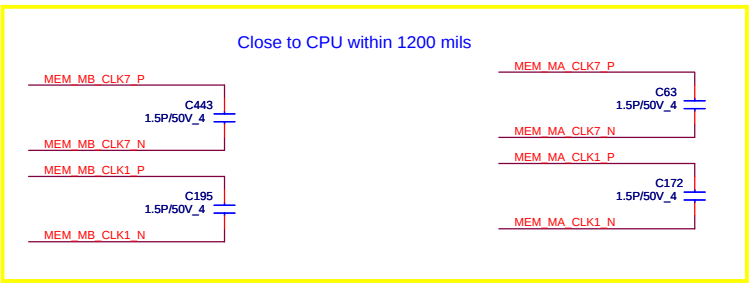
Processor Memory Interface



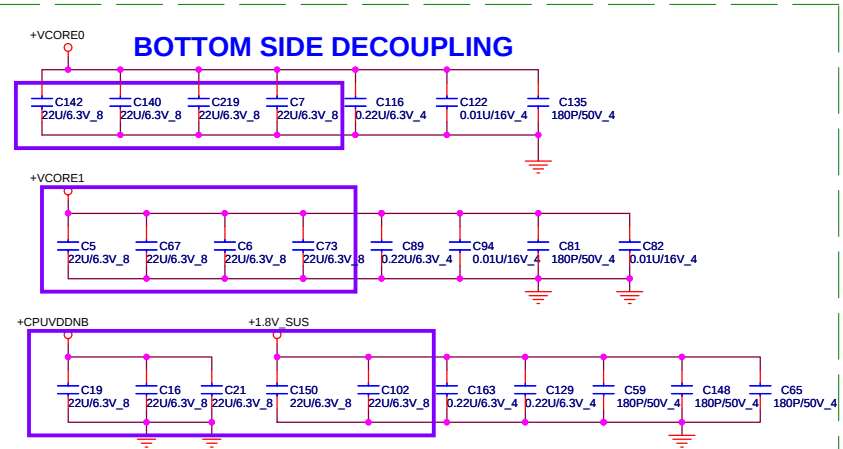
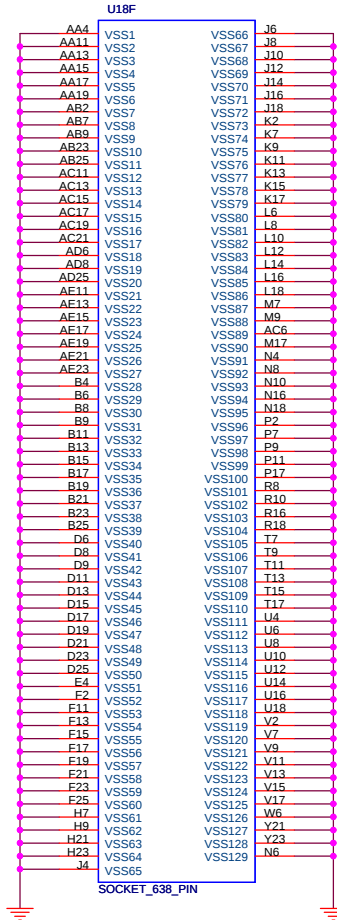
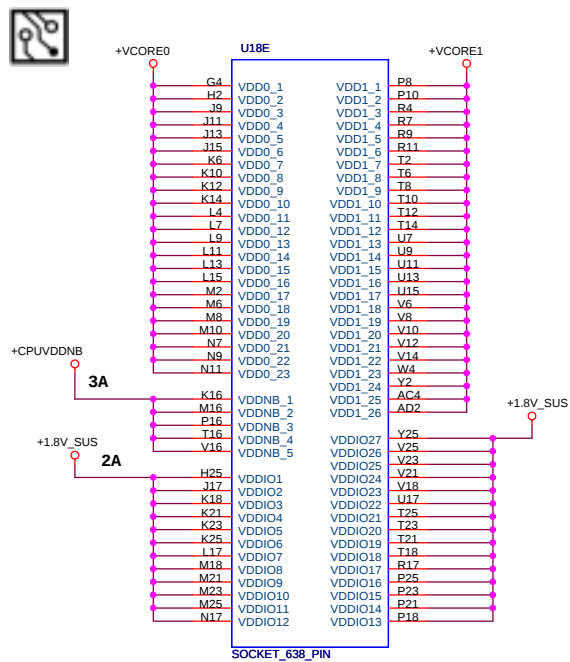
Place close to socket



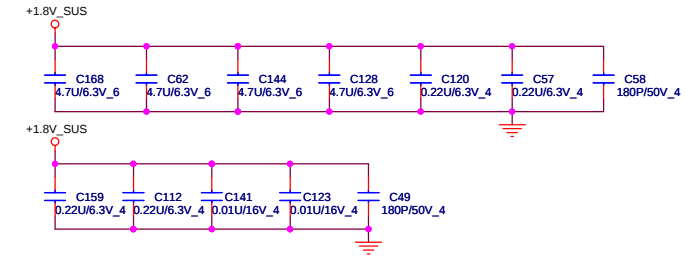
Close to CPU within 1200 mils



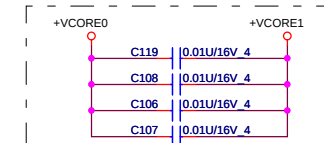
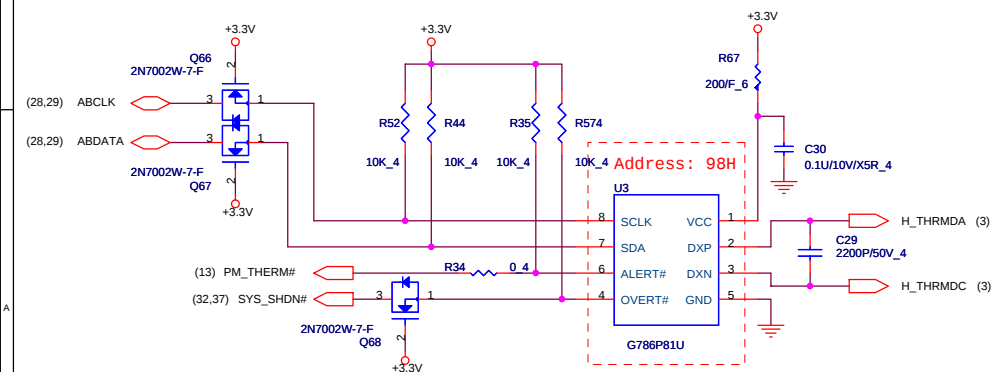
PROJECT : AJ6
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DECOUPLING BETWEEN PROCESSOR AND DIMMS PLACE CLOSE TO PROCESSOR AS POSSIBLE



PROCESSOR POWER AND GROUND

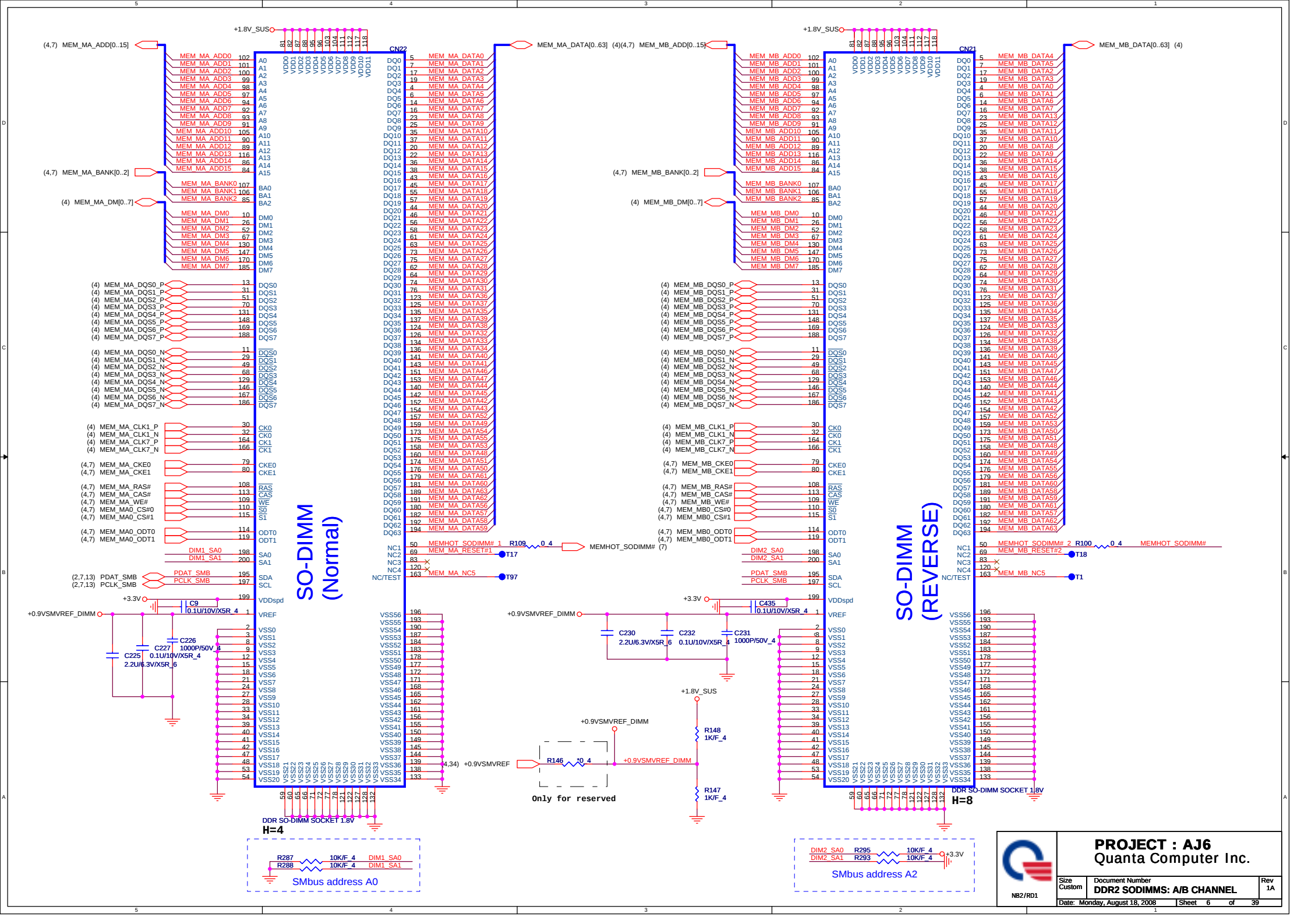


For fix HyperTransport nets
across plane splits



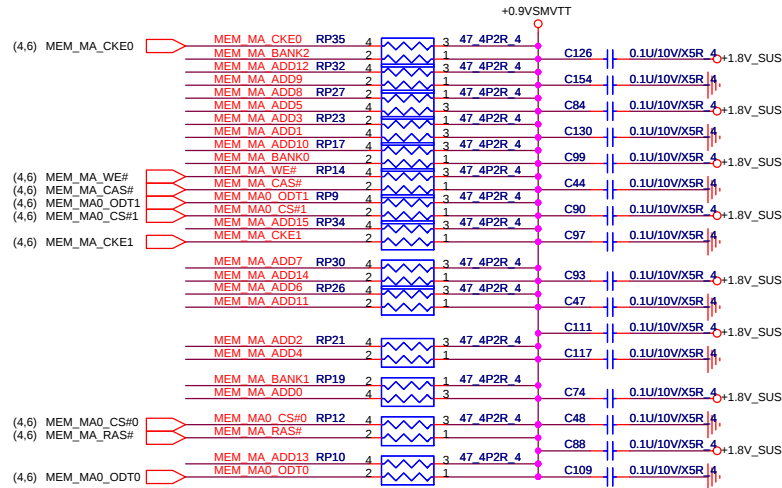
PROJECT : AJ6
Quanta Computer Inc.

Size Custom	Document Number S1G2 PWR & GND 3/3	Rev 2A
Date: Tuesday, August 19, 2008	Sheet 5 of 39	

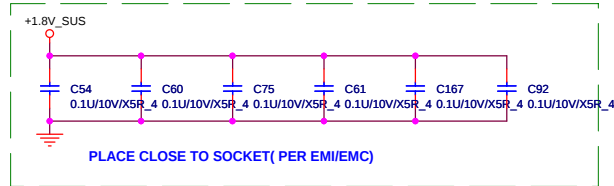




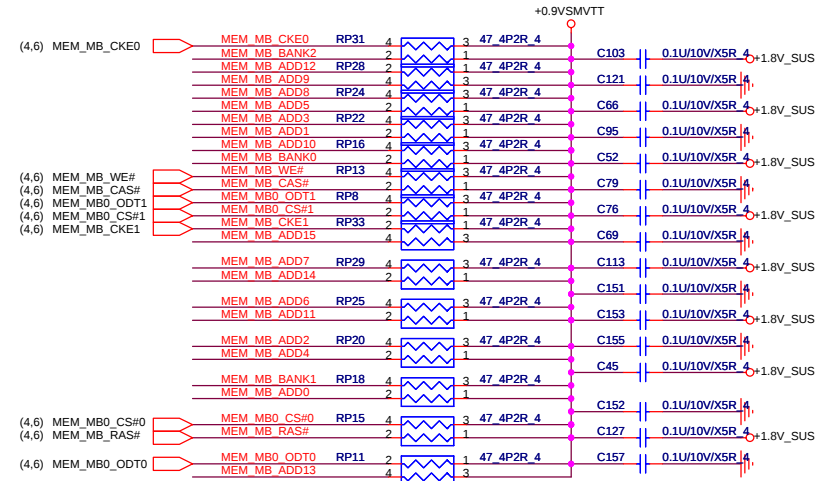
(4,6) MEM_MA_ADD[0..15] MEM_MA_ADD[0..15]
(4,6) MEM_MA_BANK[0..2] MEM_MA_BANK[0..2]



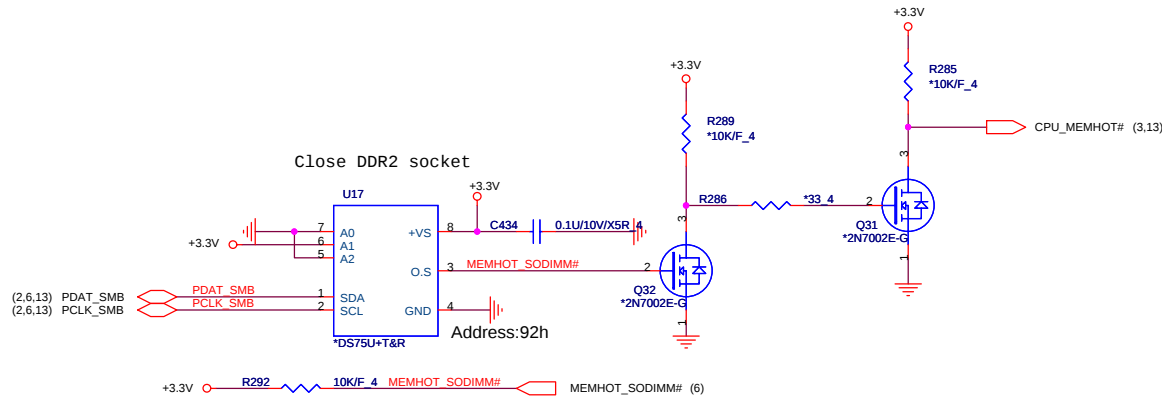
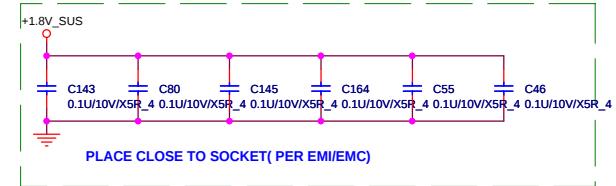
PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH



(4,6) MEM_MB_ADD[0..15] MEM_MB_ADD[0..15]
(4,6) MEM_MB_BANK[0..2] MEM_MB_BANK[0..2]

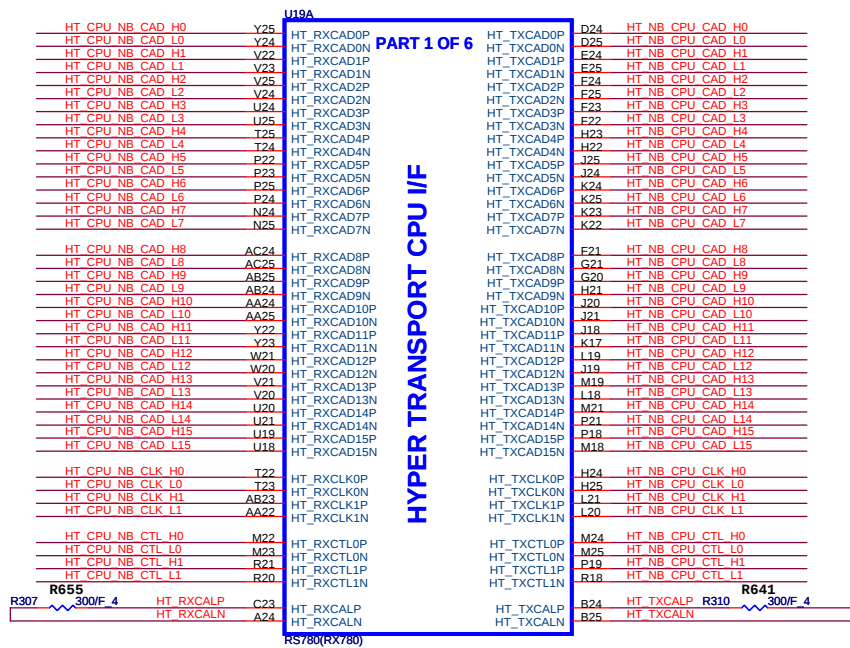


PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH



PROJECT : AJ6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR2 SODIMMS TERMINATIONS	1A
Date: Monday, August 18, 2008 Sheet 7 of 39		

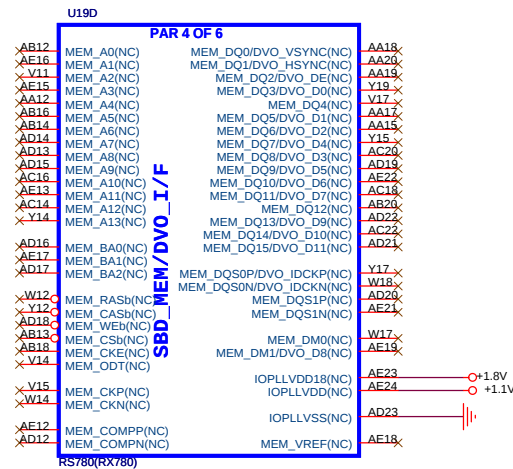


signals	RS780	RX780
HT_TXCALP	R641 300 ohm 1%	R641 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	R655 300 ohm 1%	R655 1.21k ohm 1%
HT_RXCALN		

RES CHIP 1.21K 1/16W +-1%(0402)
P/N : CS21212FB18

RES CHIP 300 1/16W +-1%(0402)
P/N : CS13002FB00

This block is for UMA RS780 only , RX780 NC

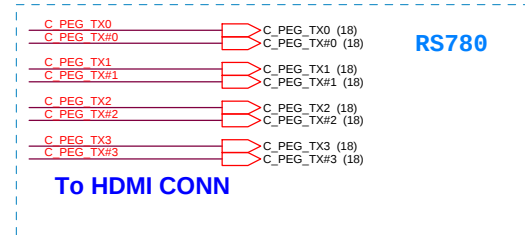


PROJECT : AJ6
Quanta Computer Inc.

Size Custom	Document Number RS780MN-HT LINK I/F 1/4	Rev 1A
Date: Monday, August 18, 2008	Sheet 8	of 39

(17) PEG_RXN[15:0]  PEG_RXN[15:0]  PEG_TXN[15:0] (17)

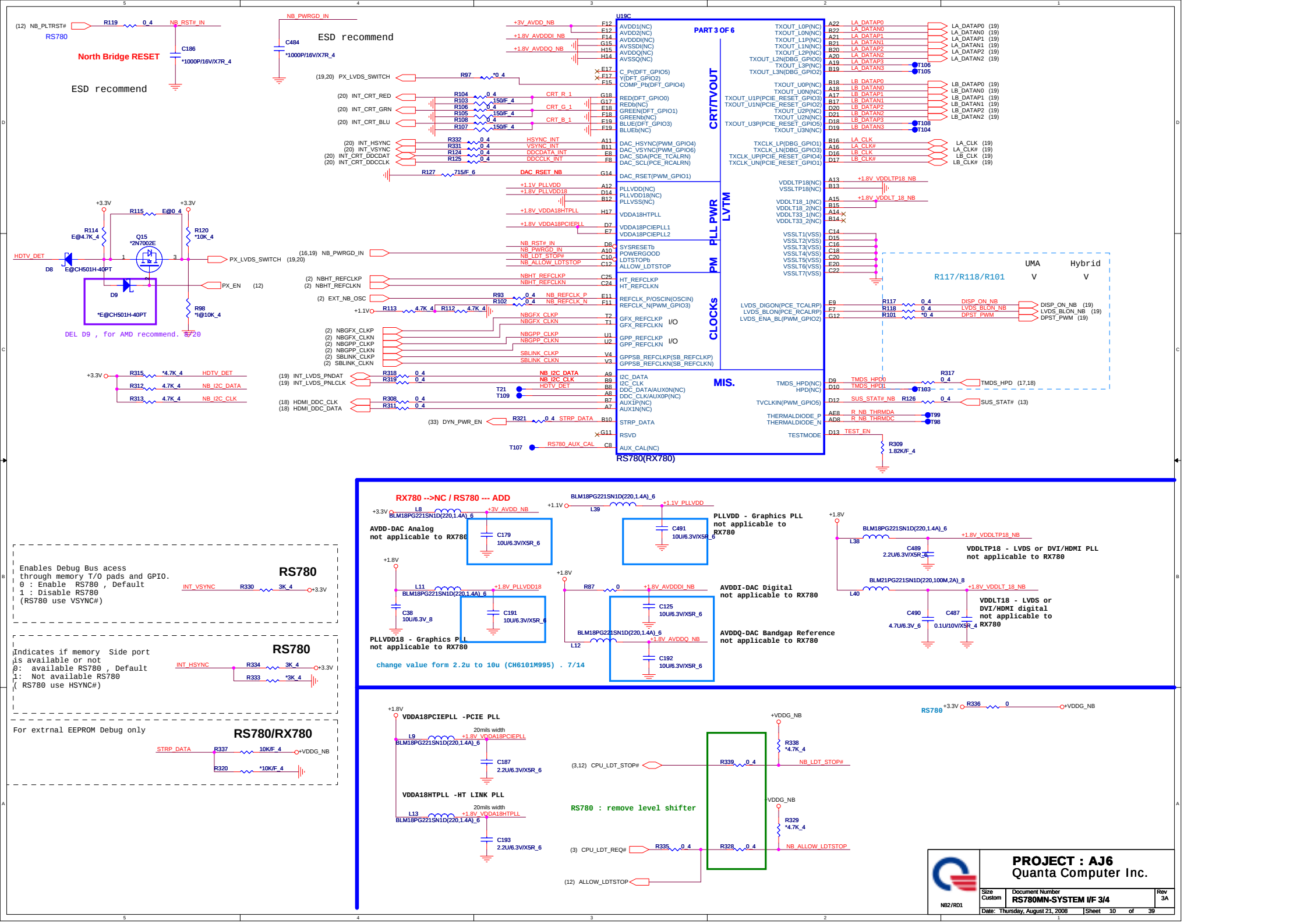
(17) PEG_RXP[15:0]  PEG_RXP[15:0]  PEG_TXP[15:0] (17)

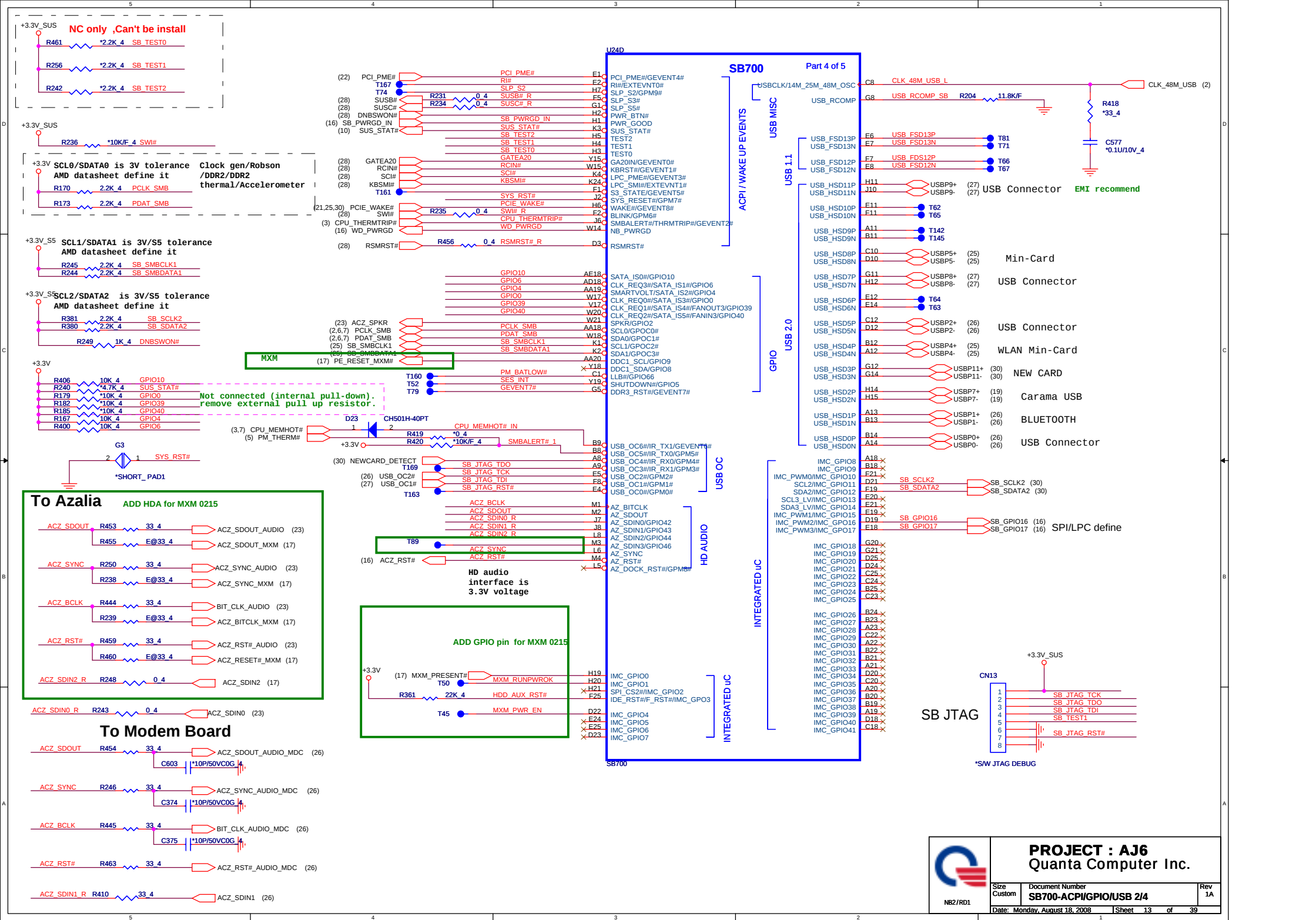


TO PCIE CARD READER

RS780 Display Port Support (muxed on GFX)

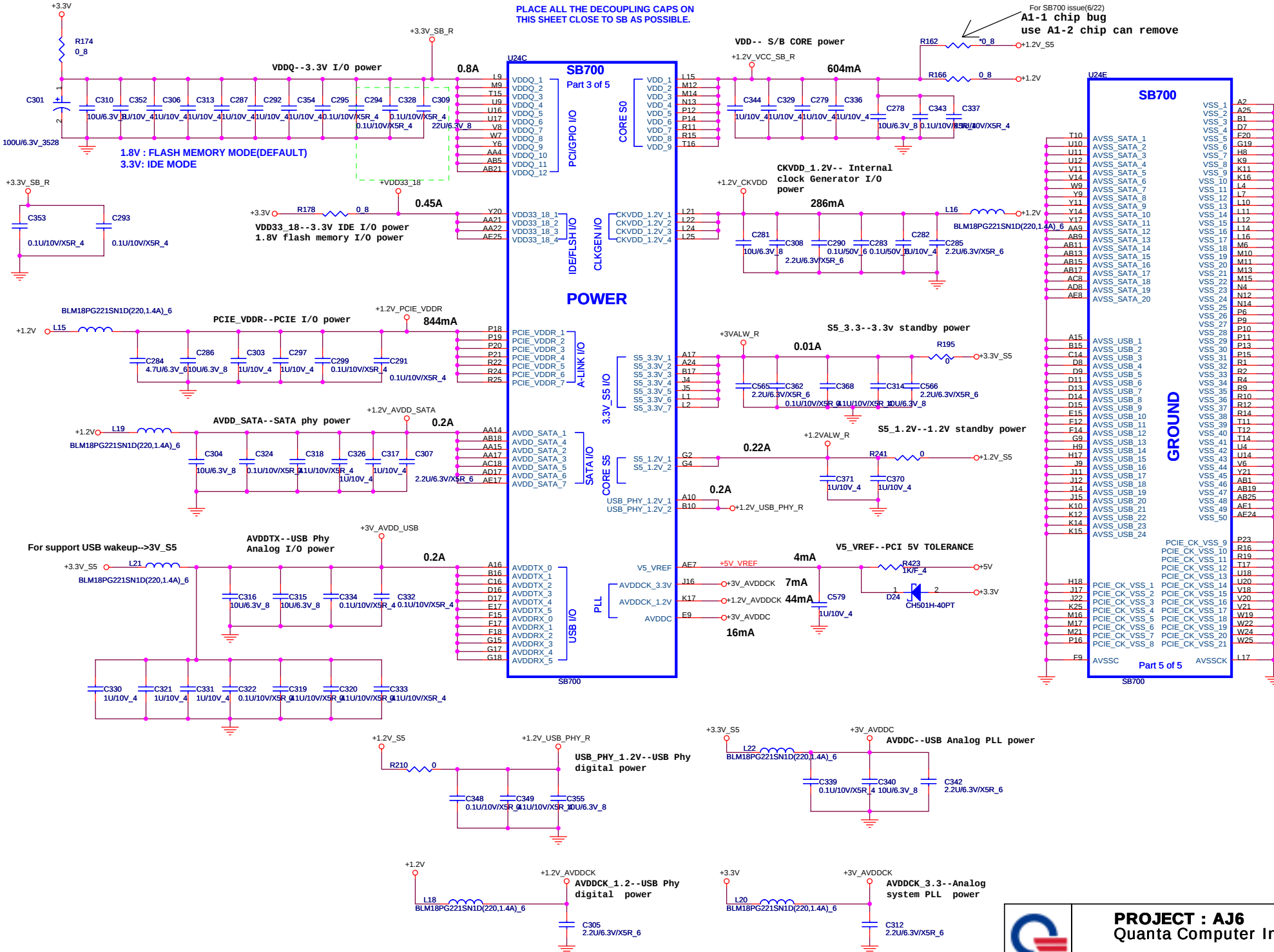
DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1





PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.

For SB700 issue(6/22)
A1-1 chip bug
use A1-2 chip can remove



PROJECT : AJ6
Quanta Computer Inc.

Size Custom	Document Number SB700-PWR/DECOUPLING 4/4	Rev 2A
Date: Monday, August 18, 2008	Sheet 15 of 39	



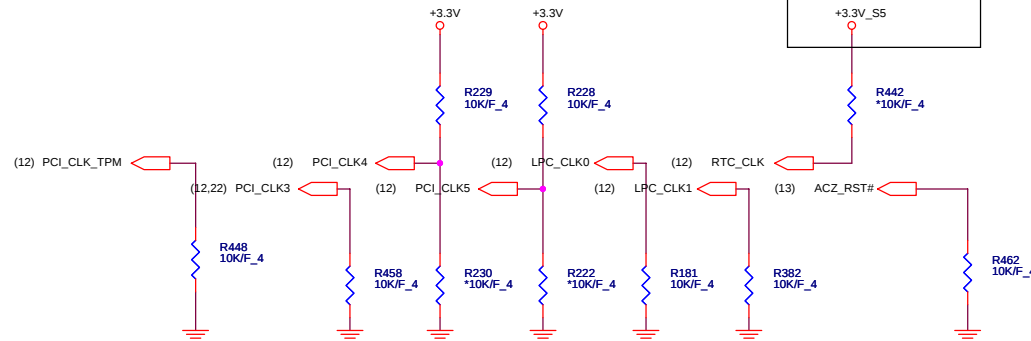
OVERLAP COMMON PADS WHERE
POSSIBLE FOR DUAL-OP RESISTORS.

16

For rev. A11

It must ready
refofe RSMRST#

REQUIRED STRAPS



	PCI_CLK_TPM	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT

(13) SB_GPIO17
(13) SB_GPIO16

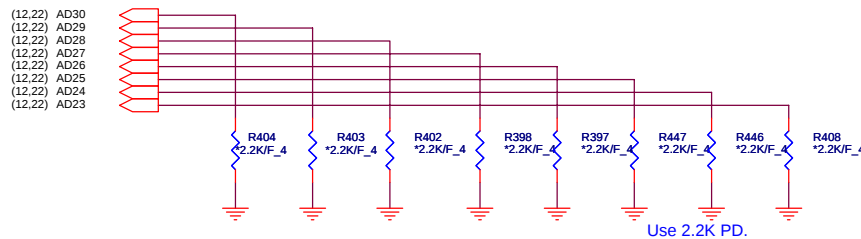
GPIO16

GPIO17

TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

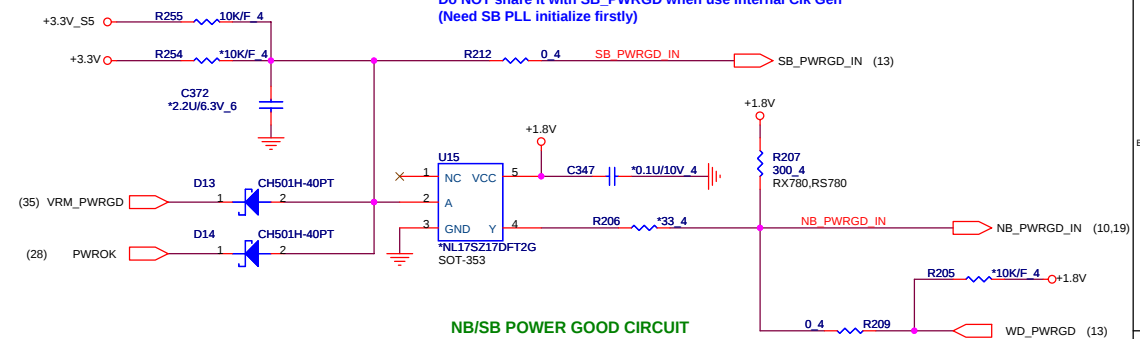
DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)

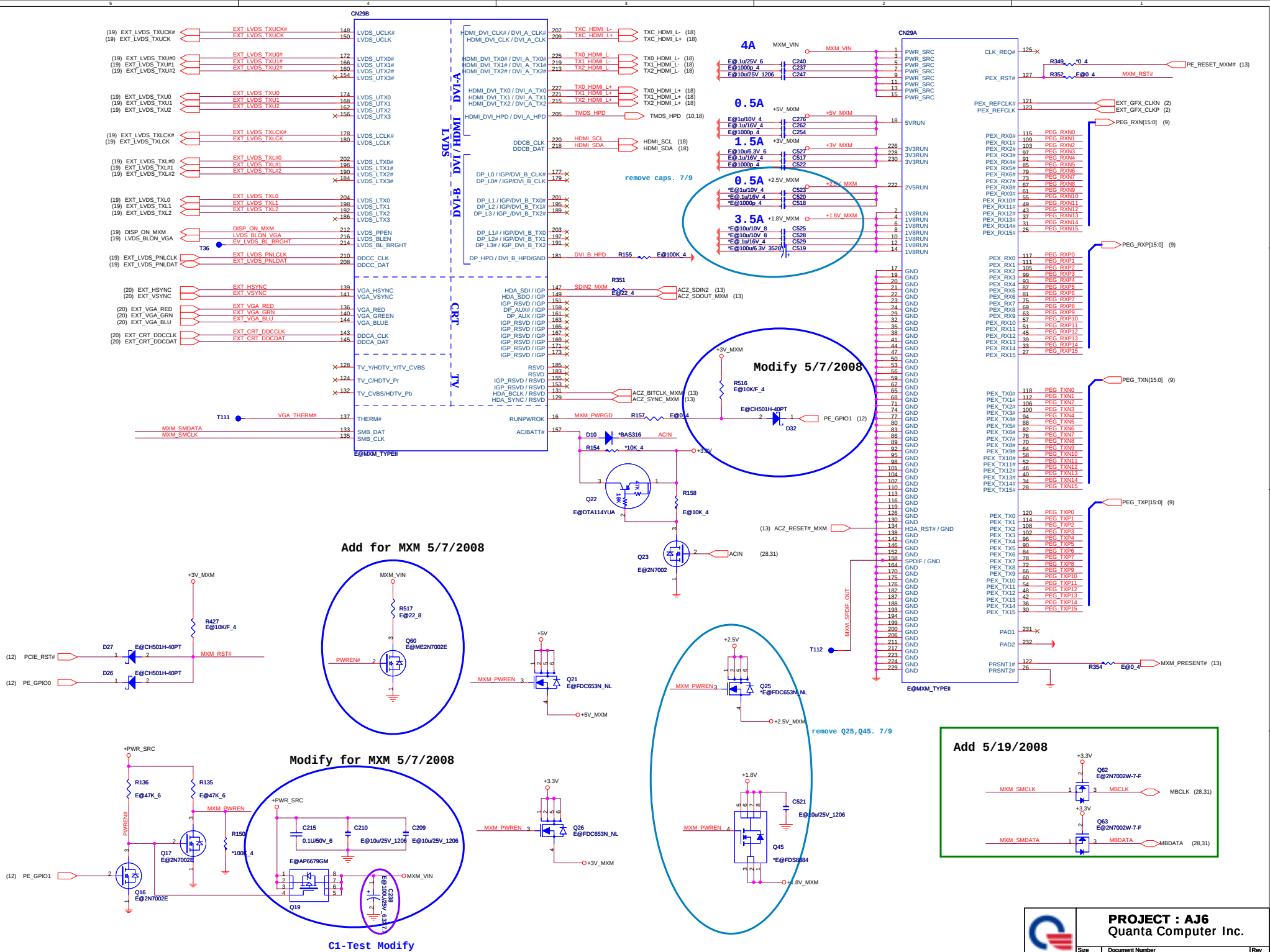


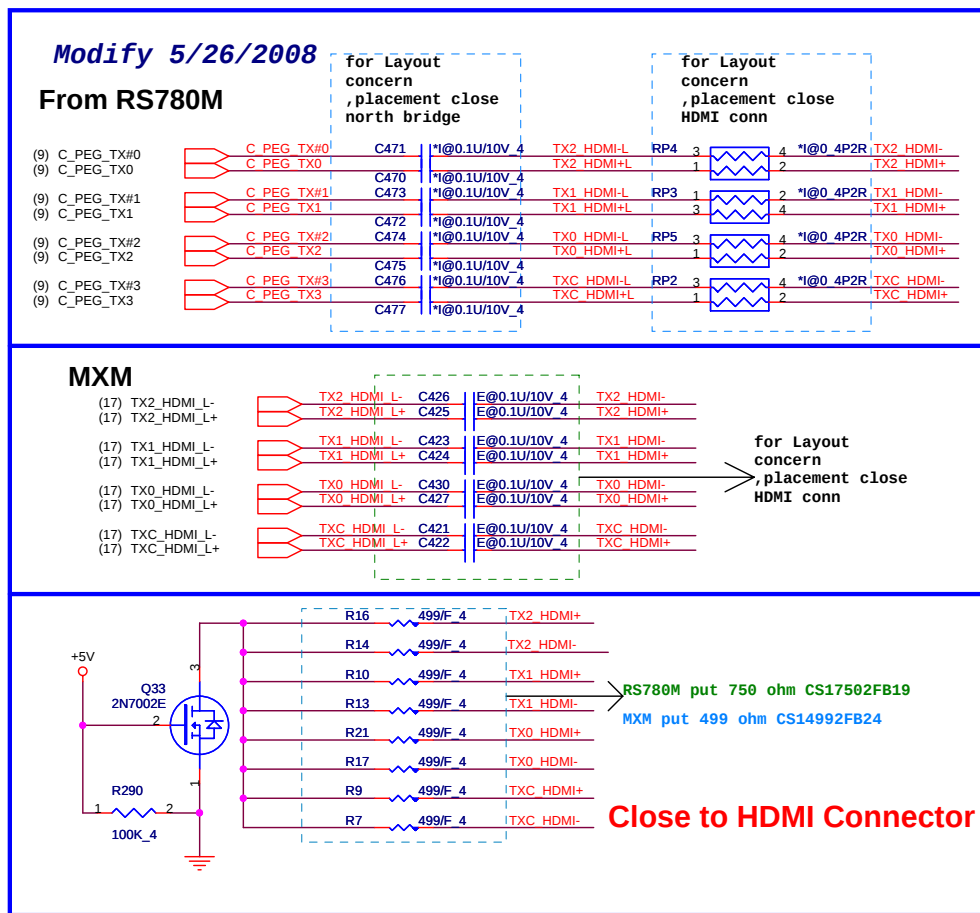
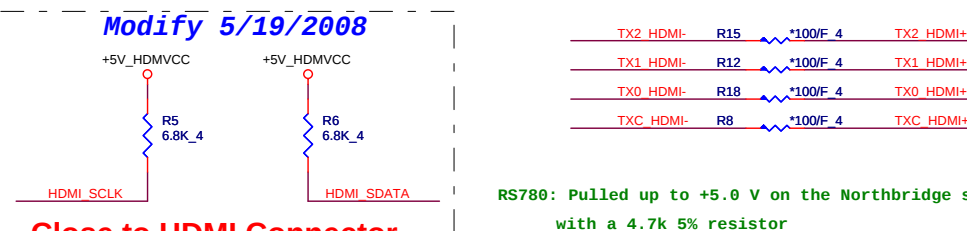
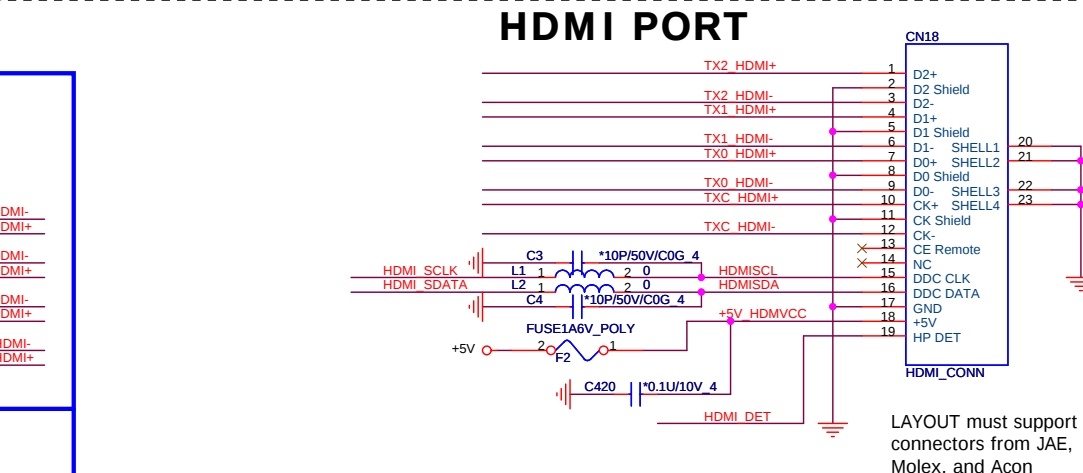
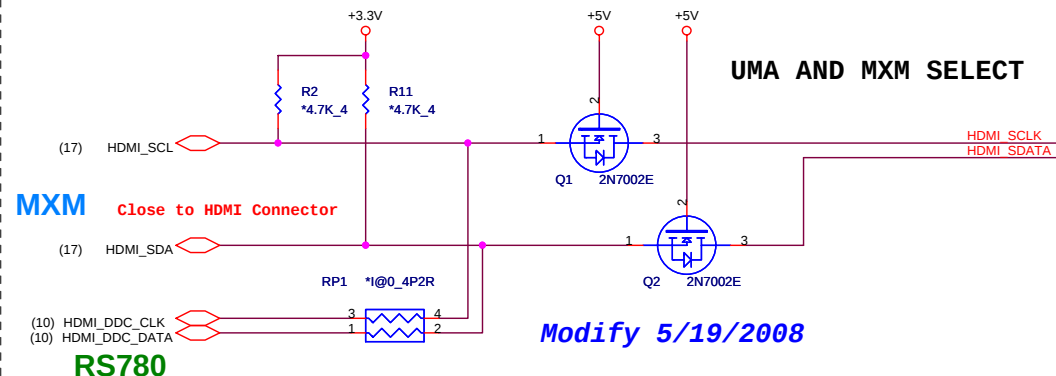
AL17SZ17000 IC(5P) NL17SZ17DFT2G(SOT-353) SOT-353
ALUC1G17000 IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5) SOT23-5

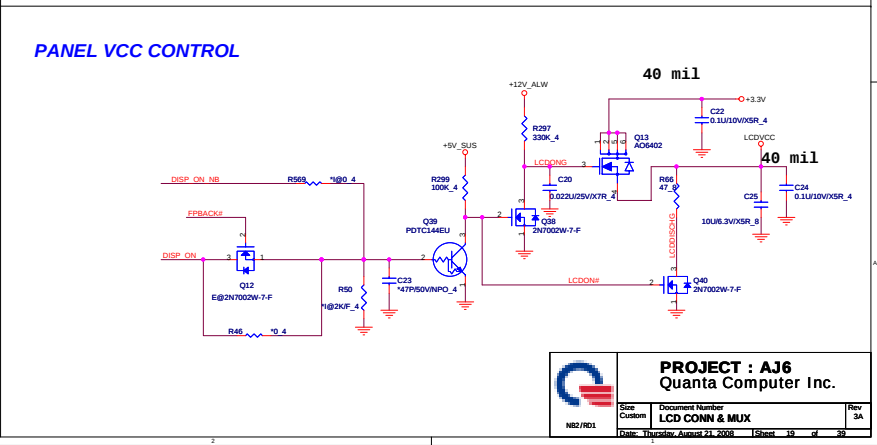
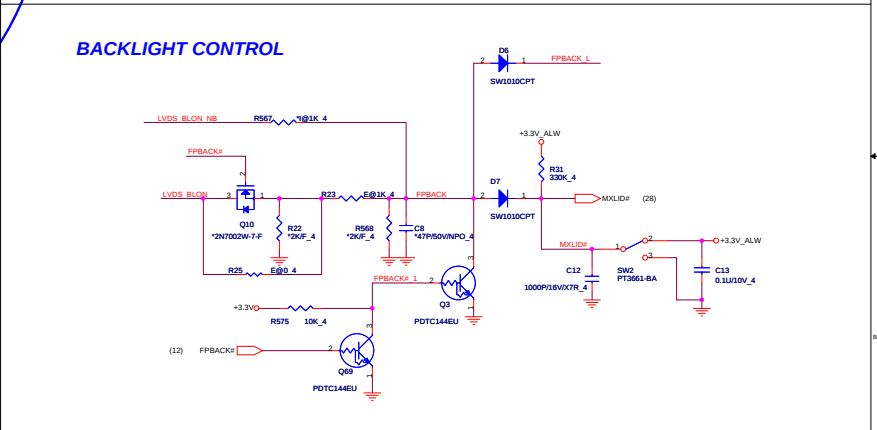
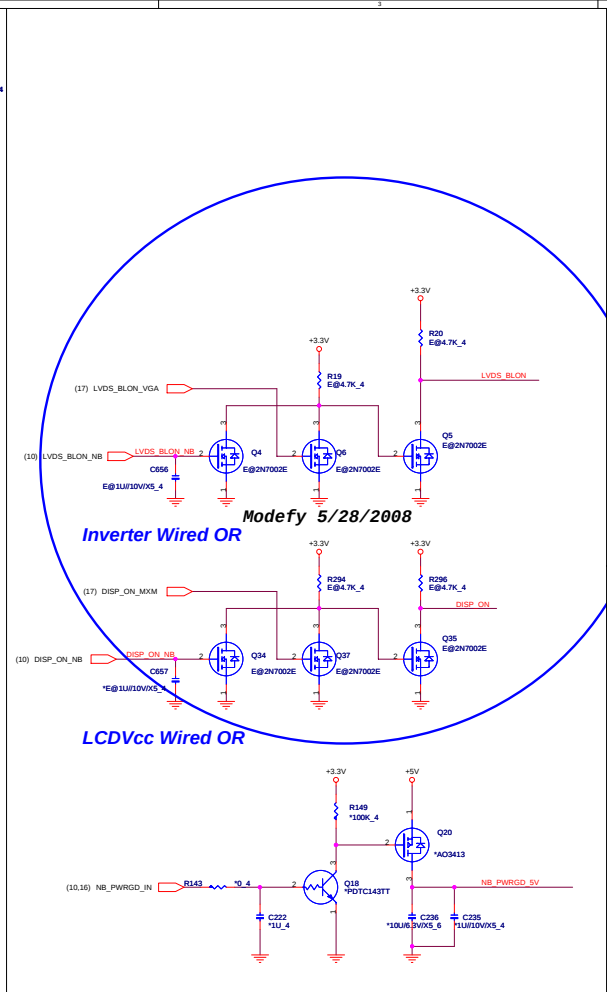


PROJECT : AJ6
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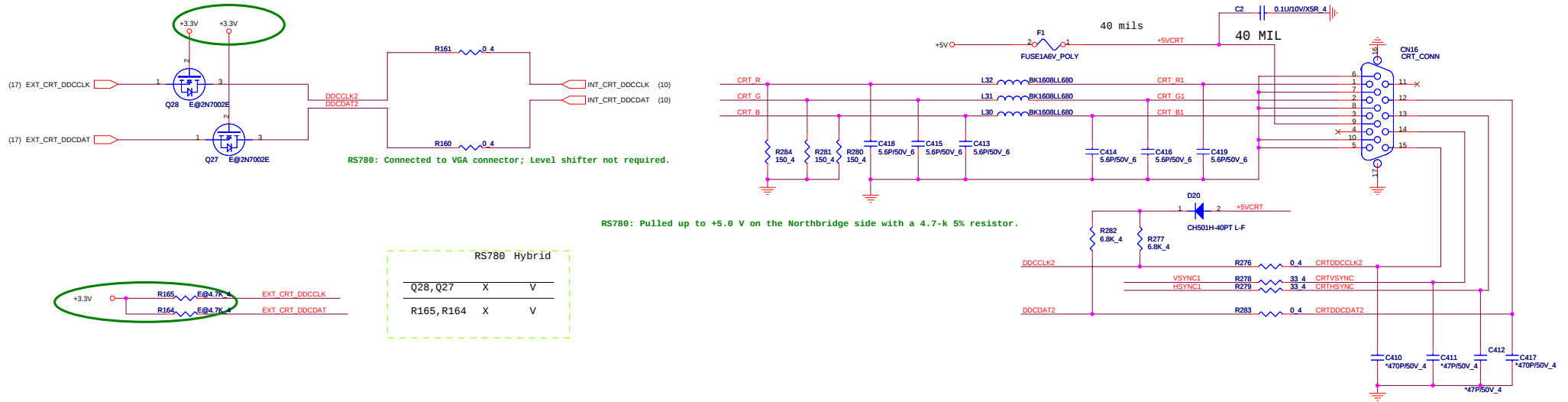
Size Custom Document Number
NB2/RD1 SB700-STRAPS Rev 1A
Date: Monday, August 18, 2008 Sheet 16 of 39



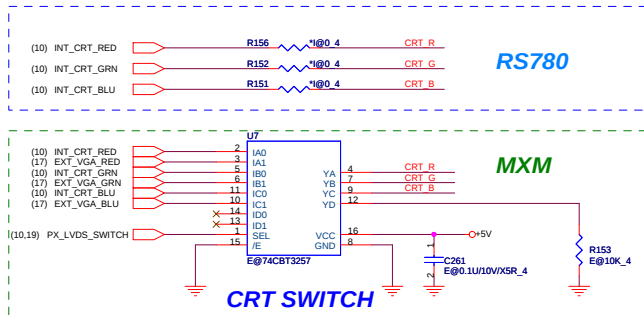
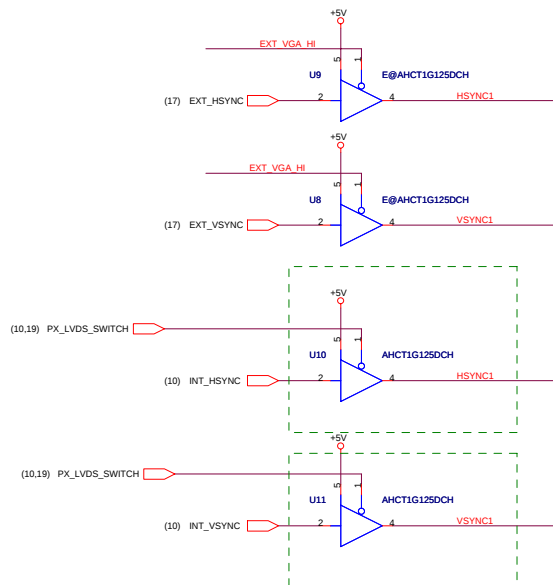




CRT PORT



U9/U8 FOR RS780 ONLY
U8/U9/U10/U11 FOR RS780+MXM HYBRID

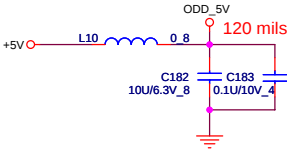
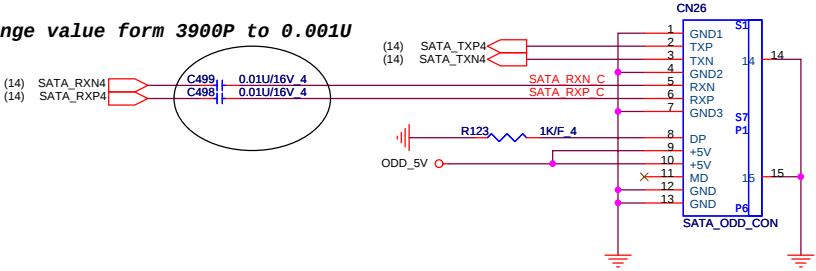


inputs	function
/E	SET
L	L
L	H
H	X
	Y - port 0
	Y - port 1
	Disconnect

SATA CD-ROM

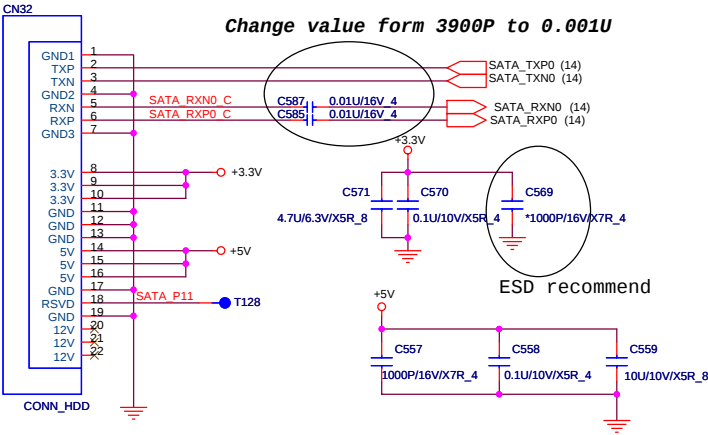
NEW PART check Pin define

Change value form 3900P to 0.001U



SATA CONNECTOR

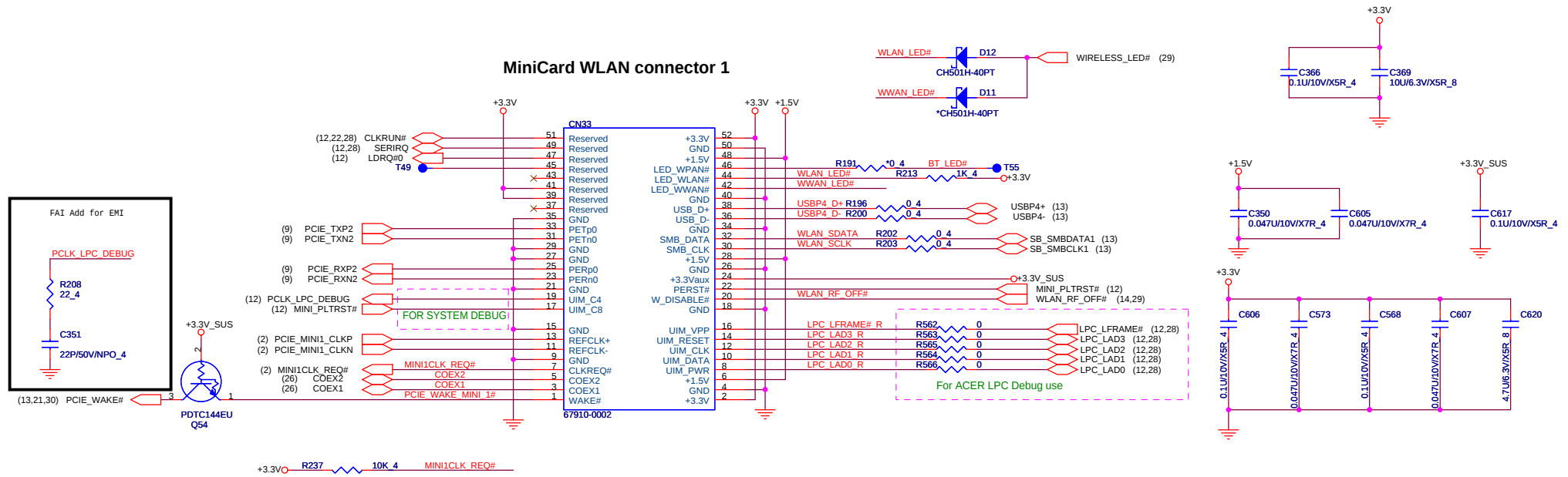
Change value form 3900P to 0.001U



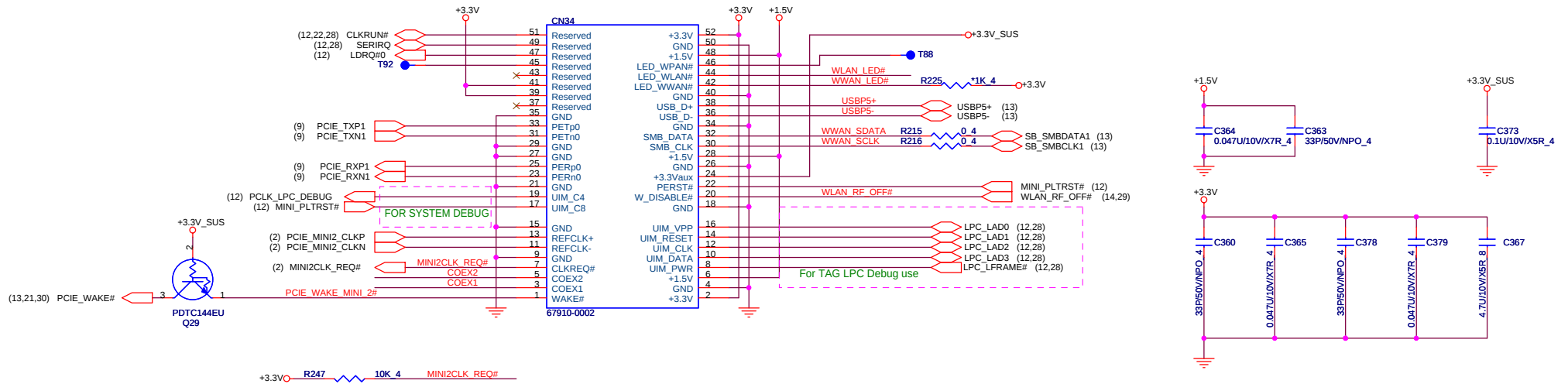
PROJECT : AJ6
Quanta Computer Inc.

Size Custom	Document Number SATA HDD ODD	Rev 3A
Date: Monday, August 18, 2008	Sheet 24 of 39	

MiniCard WLAN connector 1



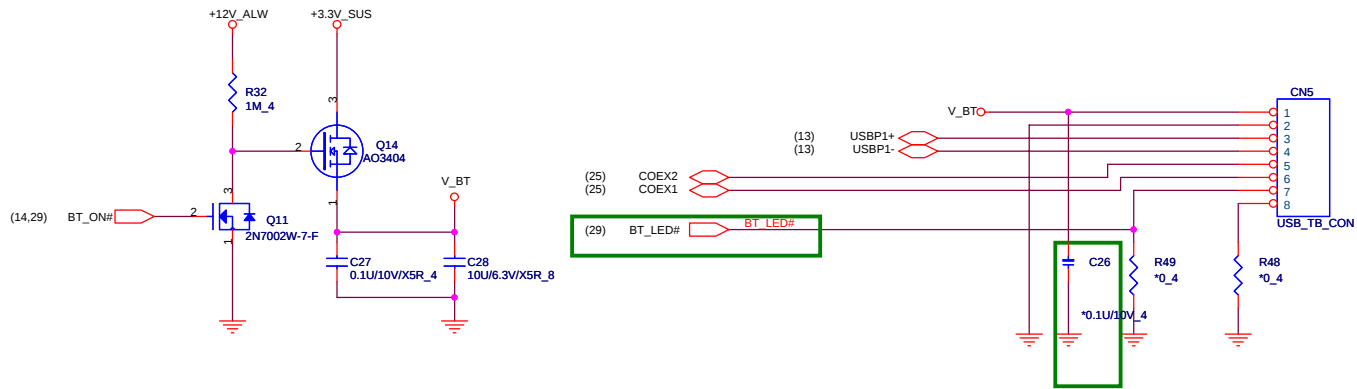
MiniCard connector 2



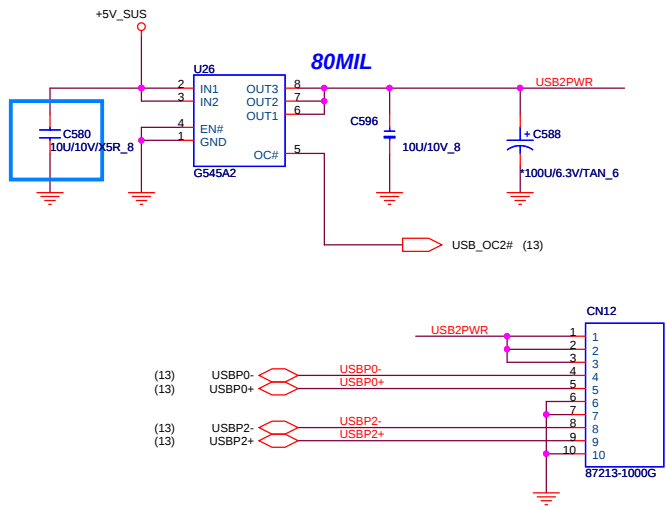
PROJECT : AJ6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MINI PCI-E Card X2	2A
Date: Monday, August 18, 2008	Sheet 25 of 39	

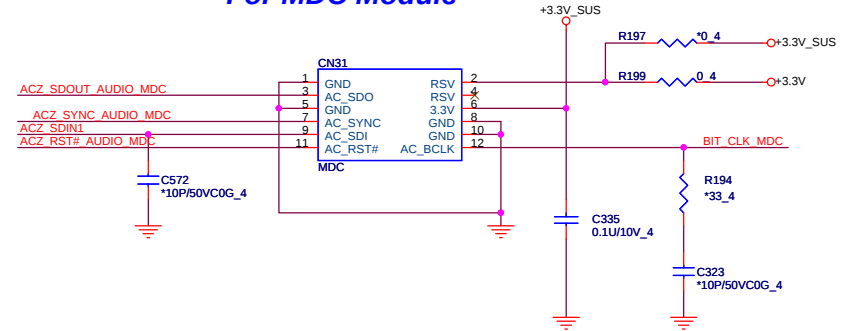
BLUETOOTH CONNECTOR



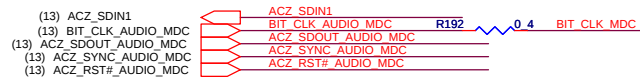
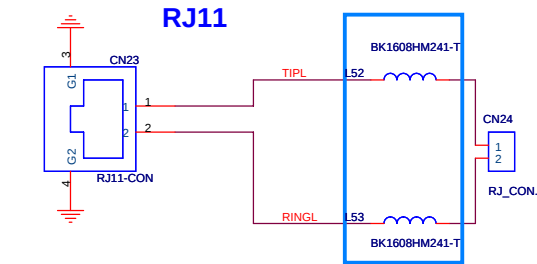
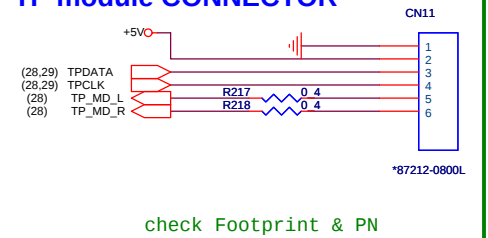
TO USB Board



For MDC Module

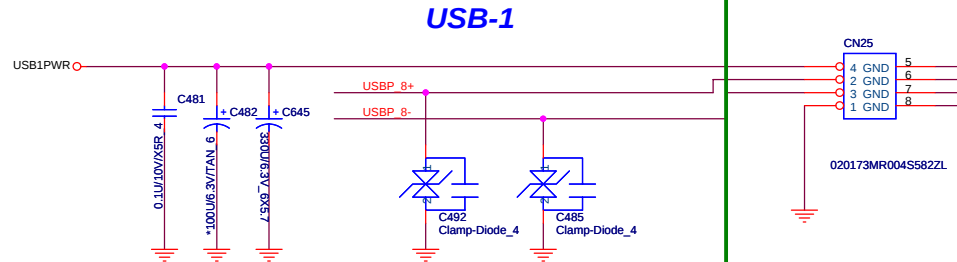
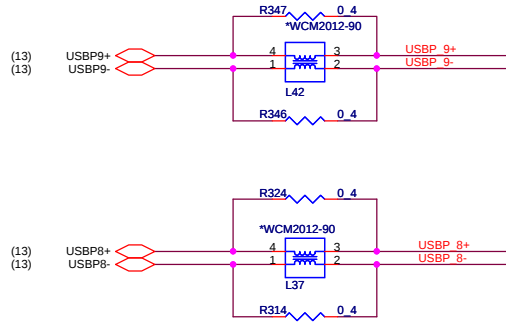
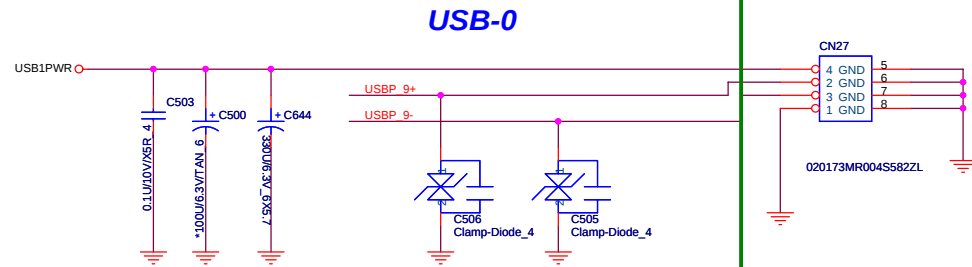
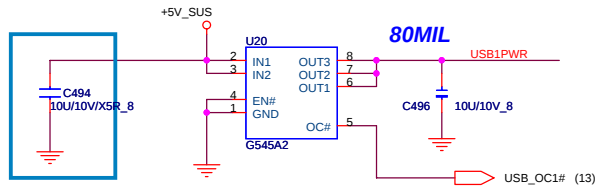


TP module CONNECTOR

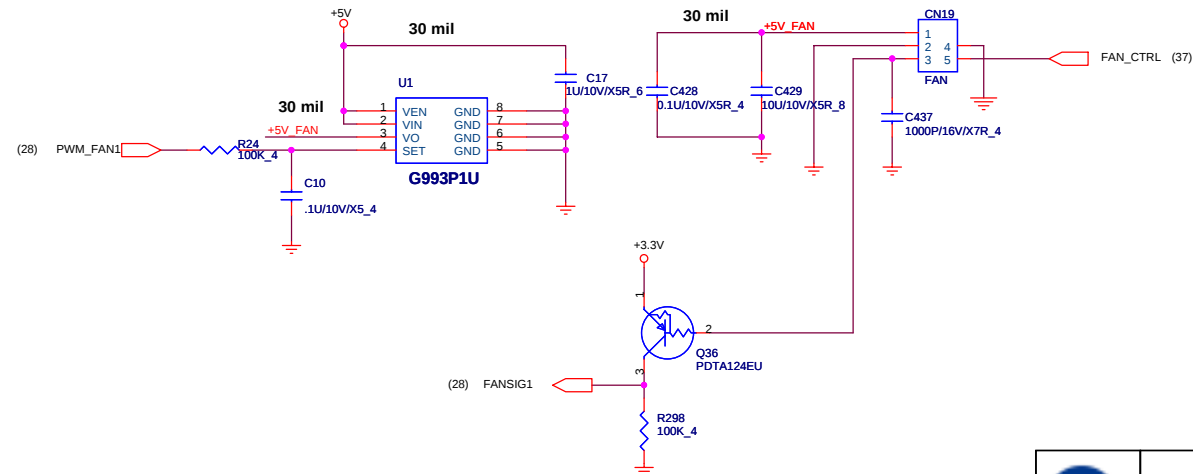


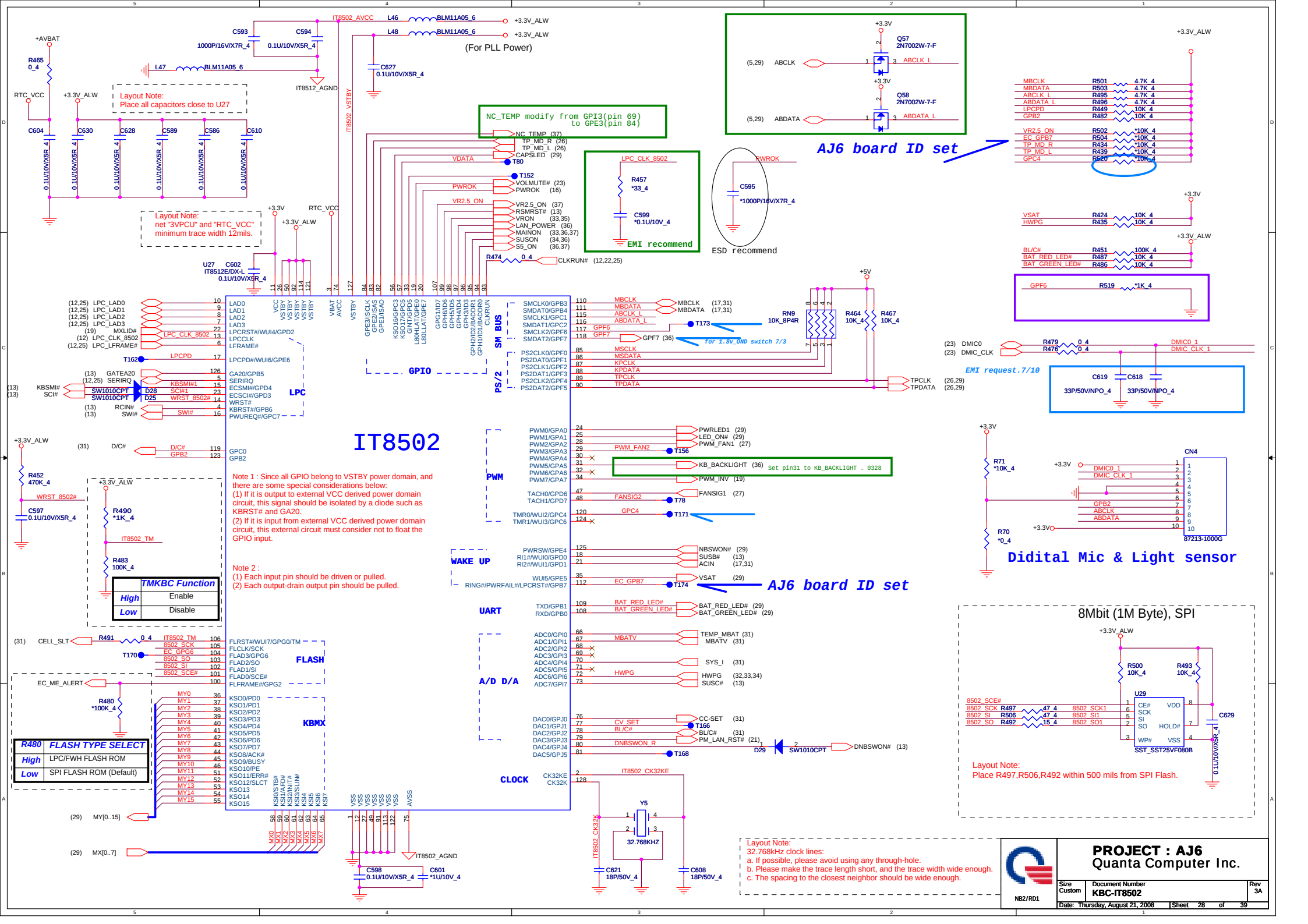
PROJECT : AJ6
Quanta Computer Inc.

Size Custom	Document Number Bluetooth,RJ11, MDC,Small/B	Rev 3A
Date: Thursday, August 21, 2008	Sheet 26 of 39	

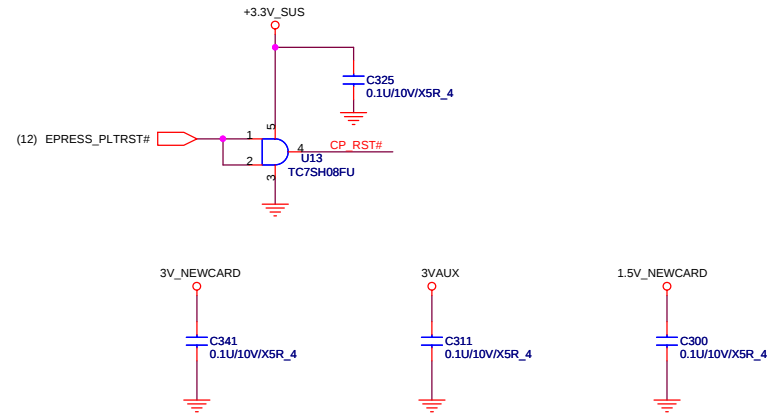
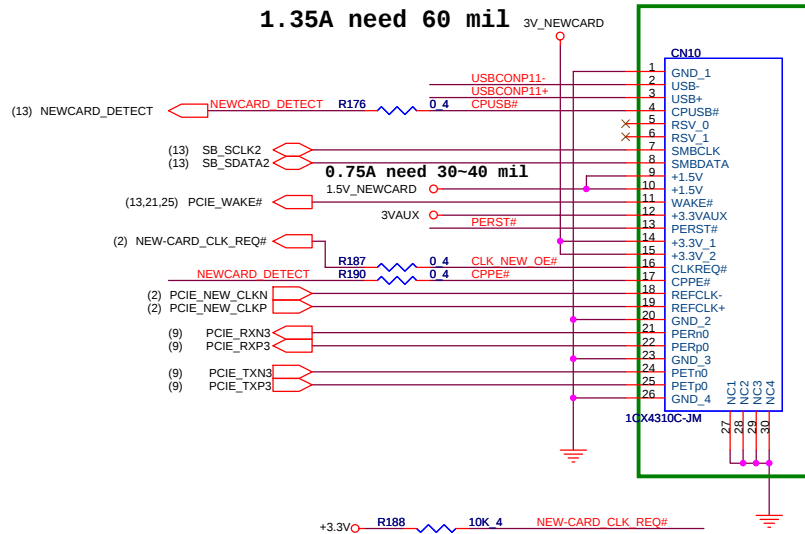
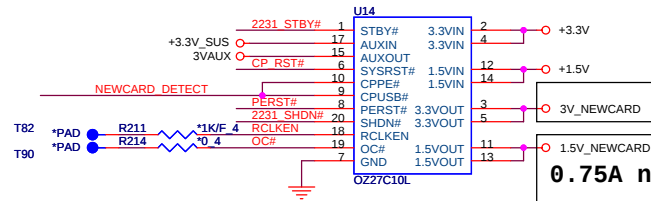
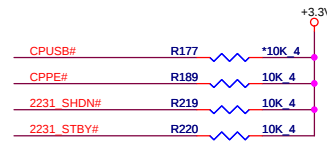


CPU FAN





NEWCARD



PROJECT : AJ6
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Size Custom	Document Number NEW CARD	Rev 1A
Date: Monday, August 18, 2008	Sheet 30 of 39	

BATTERY CHARGER

TOP DC JACK
MXM 90W (DFP305MR006) Blue
UMA 65W (DFP305MR007) yellow

CN15
DC/DC-756-X06-SP-H

PF2
LITTLE-7A-1206

PC1
0.1U/50V/X7R_6

PL4
HI080SR800R_5A_8

PC84
0.1U/50V/X7R_6

PD11
PDS1040-13

PD12
P4SMAJ20A

PR8
*0_4

PR121
RL3720WT-R020

PR122
P4SMAJ20A

PR123
P4SMAJ20A

PR124
P4SMAJ20A

PR125
P4SMAJ20A

PR126
P4SMAJ20A

PR127
P4SMAJ20A

PR128
P4SMAJ20A

PR129
P4SMAJ20A

PR130
P4SMAJ20A

PR131
P4SMAJ20A

PR132
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PR133
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PR134
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PR135
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PR136
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PR137
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PR139
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PR140
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PR141
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PR175
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PR176
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PR345
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PR346
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PR347
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PR348
P4SMAJ20A

PR349
P4SMAJ20A

+5Volt +/- 5%
Countinue current:7.5A
OCP minimum:10A

C-Test Modify

Vout=0.7(Ra+Rb)/Rb
Rb around 49.9k

I_lim*MOSFET(RDSN)=V_ILIM(mV)/10
V_ILIM(mV)=5uA*R_ILIM

C-Test Modify

B-Test Modify

C-Test Modify

C-Test Modify

+5VSUS
4A
S0-S3

+3V
5.76A
S0-S1

+3.3Volt +/- 5%
Countinue current:7.5A
OCP minimum:10A

C-Test Modify

C-Test Modify

+3V
5.76A
S0-S1



PROJECT : AJ6
Quanta Computer Inc.

Size Custom	Document Number +5V/+3V(ISL6237)	Rev 2A
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$T_{on} = 3.85p \cdot R_{TON} \cdot V_{OUT} / (V_{IN} - 0.5)$
 $Frequency = V_{out} / (V_{IN} \cdot T_{ON})$

C-Test Modify

(28,32,34) HWPG
 (28,35) VRON
 (28,36,37) MAINON

reserved for pwr seq -- andrew

2.0A
 S0-S1

C-Test Modify

$V_{out1} = (1+R1)/R2 \cdot 0.5$

Add 5/30/2008

EC2
 0.1U/50V/X7R_6

PU5
 RT8204AGQM

B-Test Modify

B-Test Modify

Place these CAPs close to FETs

+1.2V
 15A
 S0-S1

C-Test Modify

B-Test Modify

$V_o = 0.75(R1+R2)/R2$
 $R_{ILIM} = I_{LIMIT} \cdot R_{sense} / 20uA$
 Keep R2 higher than 10Kohm

+1.1V
 7.0A
 S0-S1

C-Test Modify

$V_o = 0.75(R1+R2)/R2$

DYN_PWR_EN	High	Low
+1.1V_DYN	1.0	1.1



PROJECT : AJ6
 Quanta Computer Inc.

Size B	Document Number +1.2V & +1.1V(RT8204)	Rev 2A
Date: Monday, August 18, 2008	Sheet 33 of 39	

+1.8VSUS
18A
S0-S3

+1.8V_SUS

C-Test Modify

$R_a = (V_{out} - 0.75) / 0.75 * R_b$
Rb value from 100K to 300K ohm

Fix 1.8V Output
FAI-Test Modify

Place these CAPs
close to FETs

B-Test modify

Rds(on) 7.25m ohm

+1.8V
6A
S0-S1

$I_{lim}(Valley) = 10\mu A * R_{ILIM} / R_{DS_ON}$
For OCP set.

C-Test Modify

+0.9VSMVT
1.53A
S0-S3

Mode	Discharge Mode
V5IN	No discharge
VDDQ	Tracking discharge
Gnd	Non-tracking discharge

$$V_{TRIP}(mV) = R_{TRIP}(Kohm) * 10(\mu A)$$

$$I_{OCP} = V_{trip} / R_{ds_on} + I_{Ripple} / 2$$

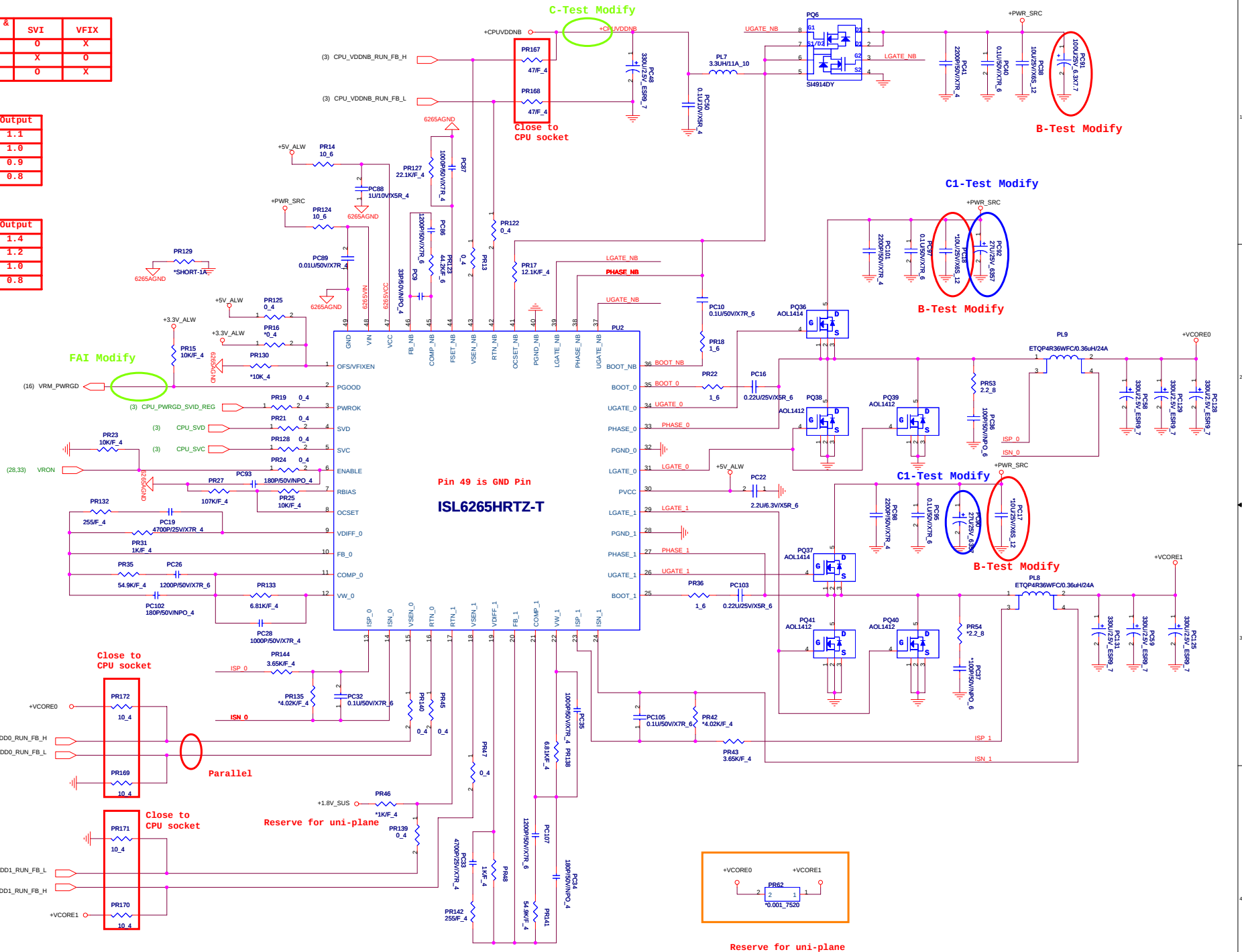
VDDQSET	VDDQ(V)	VTTREF and Vtt	Note
GND	2.5	$V_{_vddqsns} / 2$	DDR
V5IN	1.8	$V_{_vddqsns} / 2$	DDR2
FB	adjustable	$V_{_VDDQSNS} / 2$	$1.5V < VDDQ < 3V$

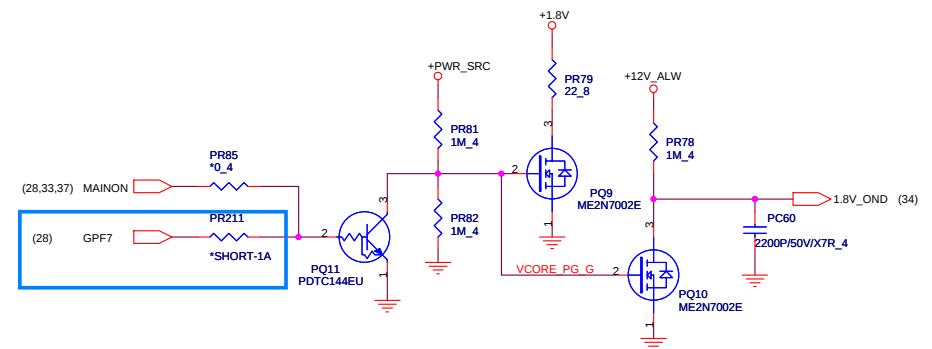
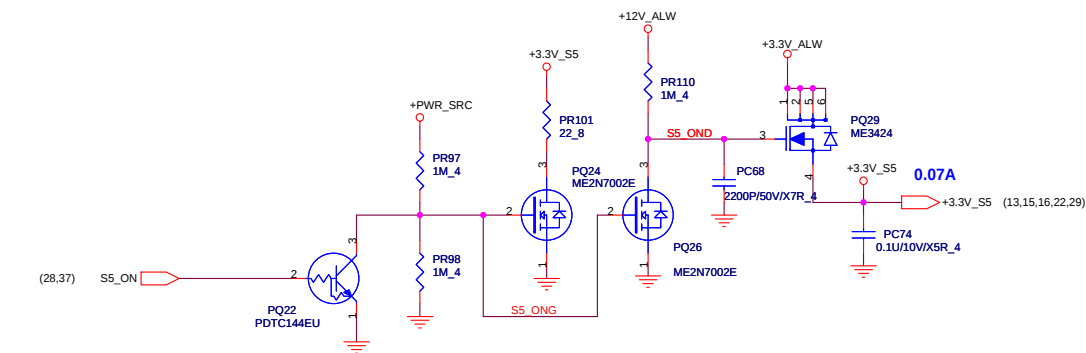
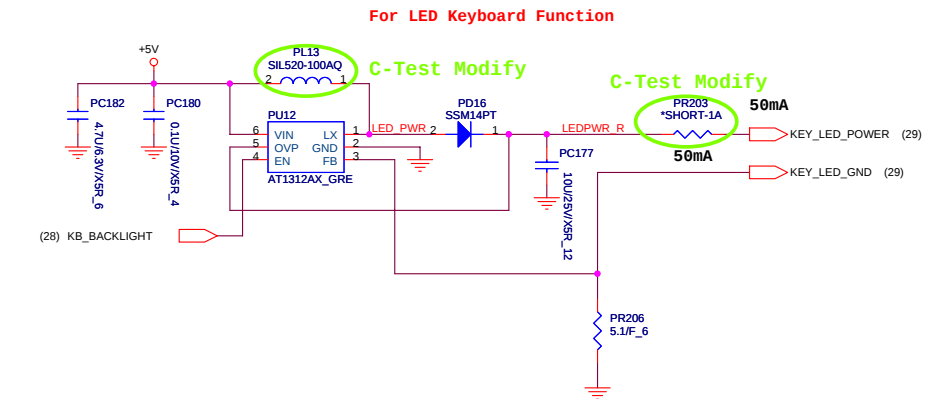
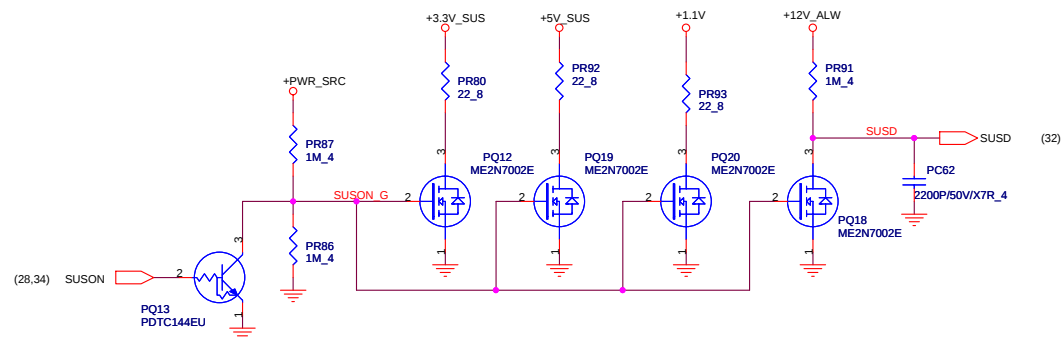
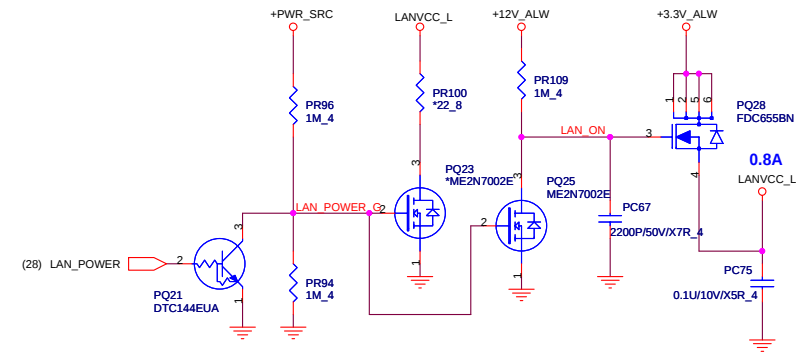
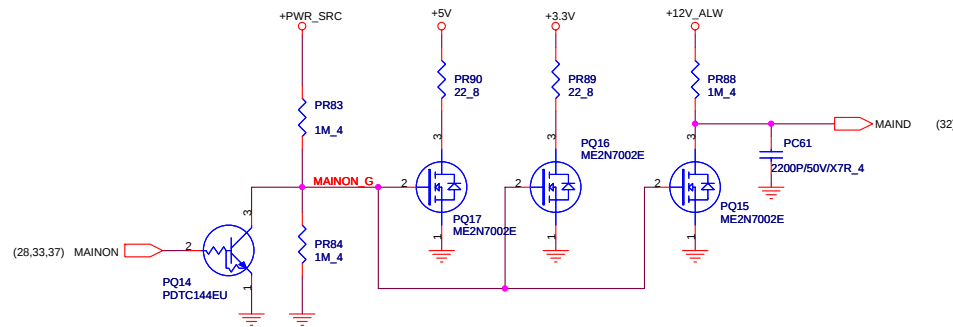
 NB2/RD1	PROJECT : AJ6		
	Quanta Computer Inc.		
	Size Custom	Document Number 1.8VSUS/DDR_VTER/+1.8V/2.5V	Rev 2A
Date: Tuesday, August 19, 2008 Sheet 34 of 39			

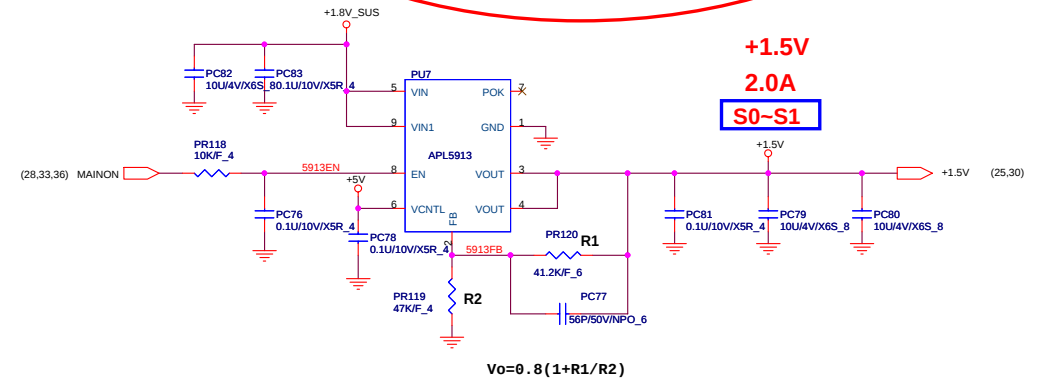
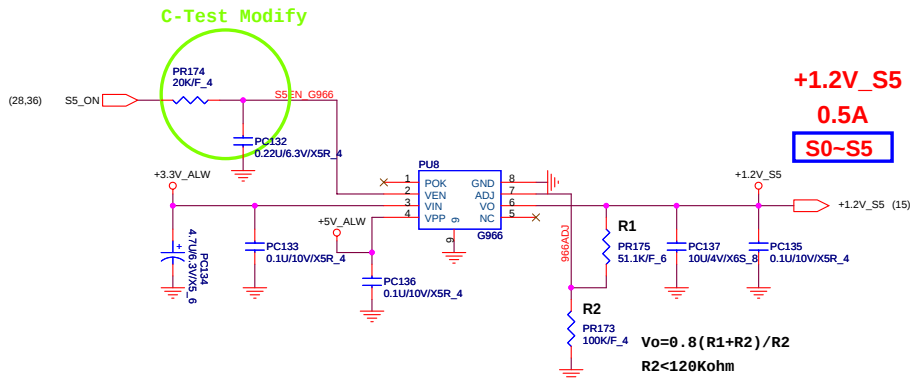
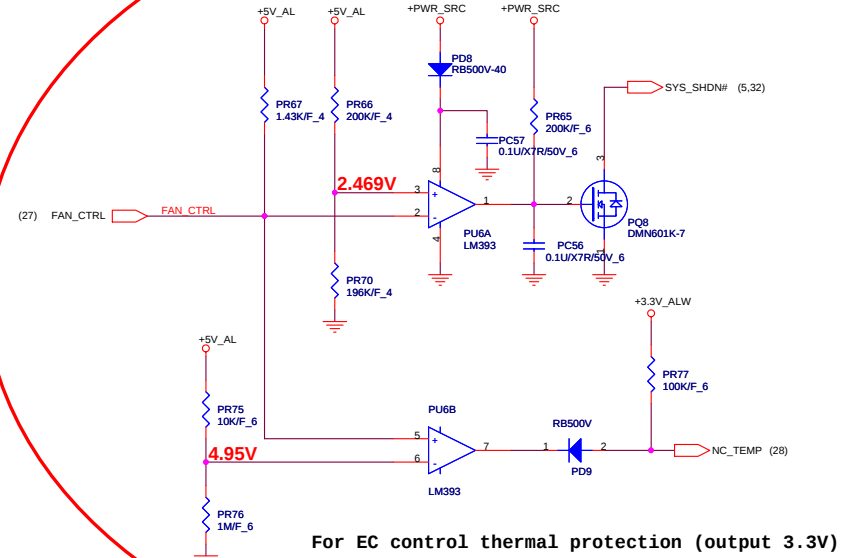
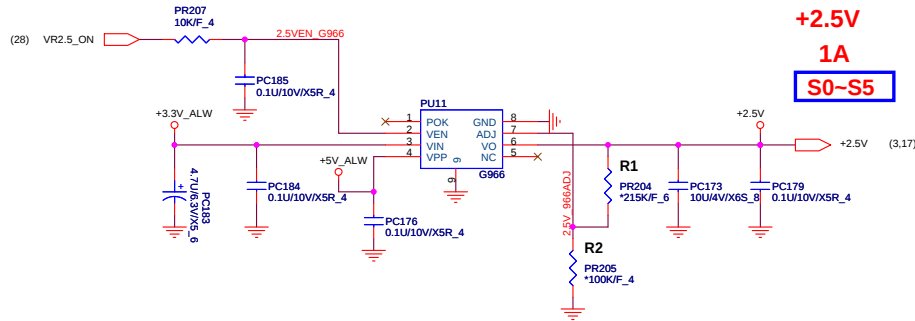
OFS/VFIXEN	Offset & Droop	SVC	VFIX
GND	0	0	X
+3.3V	X	X	0
+5V	X	0	X

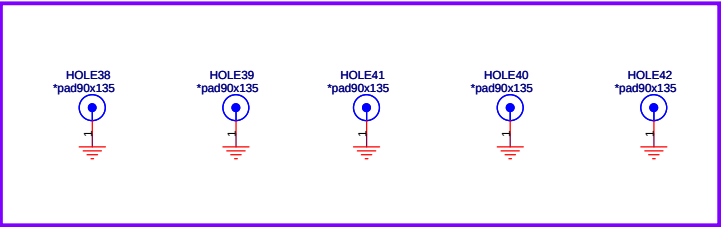
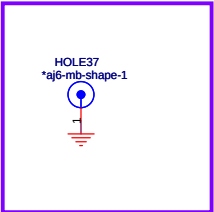
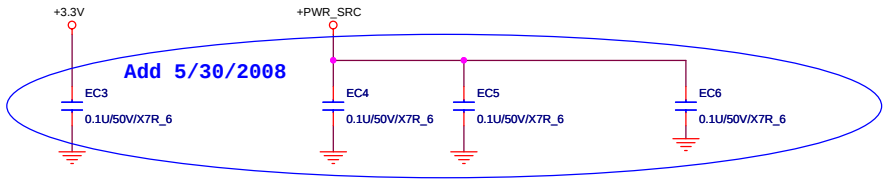
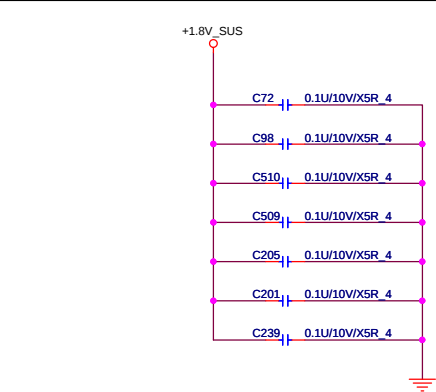
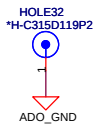
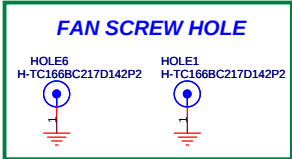
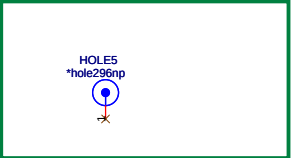
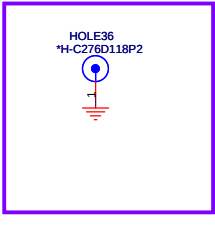
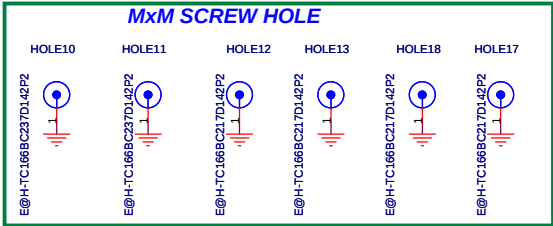
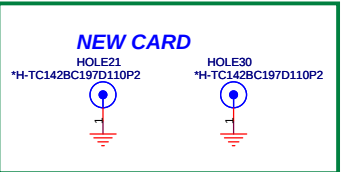
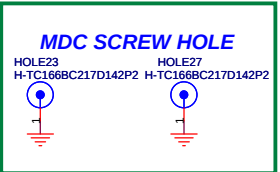
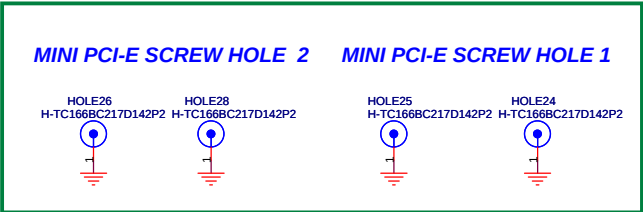
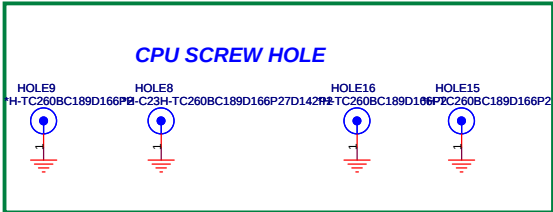
SVC	SVD	Output
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8









EMI request 19/08/2008



PROJECT : AJ6
Quanta Computer Inc.

Size Custom	Document Number EMI PAD &Hole	Rev 2A
Date: Tuesday, August 19, 2008	Sheet 38 of 39	

MODEL: REV		CHANGE LIST	MODEL		
			PAGE	AJ6 MB	
				FROM	TO
AJ6 MB	1A	First release	1	1A	
	2A	Page5:Add Q66,Q67 for EC drivinng / Add Q68,R574 & swap U3 pin4, pin6 for system shutdown Page9:Change PCIE CAP. from X5R to X7R & modify C_PEG_TX for UMA's HDMI detect issue Page10:Delet R115 for UMA SKU. Page15:Modify R83,R184,R368,R370,R371,R372,R,386,R387,R391,R392 for board ID / Chanhe C338,C327 for accuracy Page17:Add Q60,R517 for MXM discharge / Add R516,D32 for MXM timing / Modify C215,C210,C209,Q19,C238 for MXM power express /Add Q62,Q63 for MXM smbus Page18:Add Q61,R518 for HDMI HPD sense issue / modify Q1,Q2 for UMA HDMI smbus issue / delete D4,D5 & change R5,R6 value Page19:Modify & add Q69,C656,C657R567,R569 for LCD slight light issue / Add RP40 for MXM Page21:Add R95 for Lan chip power / change R60,R61,R62,R63 package Page23:Add Q64,Q65,R570,R571,R572 for SPDIF's LED issue / Change R271,R272,R265,R266 for volume issue /Change R473,R472,R471,R470 for EMI issue Page25:Add R562,R563,R564,R565,R566 for Acer LPC debug use / Add D12,R213 for WLAN LED Page26:Delete MODEM CAP. C166,C165 Page27:Add C644,C645 for USB Page28:Modify U27 pin112 to AJ6 board ID setting / Swap pin98 & pin107 / Delete C601 for IT8502 issue /Change C621, C608 of value for accuracy Page29:Swap NC7,CN3 connector & modify circuit / Modify CN8 circuit / Delete R357 is no use Page32:Add a resister to connect PU9 pin1 and pin32 / Add PC160 in the circuit. Page33:Change PU5 PN from AL008204000 to AL08204001 / Change PR159 PN to CS23402FB08 / Add PR20, PC13, PC127 in the circuit / Delete PC117, PC123, PC121 in the circuit Page34:Change PR191 from 51.1K/F_4 to 52.3K/F_4 (CS35232FB10). Page35:Delete PC17, PC18 in the circuit / Add PC91 in the circuit Page36:Add PR90,PR89,PR80,PR92,PR93,PR101,PR79,PQ17,PQ16,PQ12,PQ19,PQ20,PQ24,PQ9 in the circuit for discharge Page37:Add PR67, PR66, PD8, PC57, PR65, PQ8, PC56, PU6, PR70, PR75, PR76, PD9, PR77 in the circuit for Acer thermal protection Page38:Add EC3,EC4,EC5,EC6 for EMI	2	1A	3B
			3	1A	
			4	1A	
			5	2A	
			6	1A	
			7	1A	
			8	1A	
			9	3A	
			10	3A	
			11	1A	3B
			12	1A	
			13	1A	
			14	3A	
			15	2A	
			16	1A	
			17	3A	3B
			18	2A	
			19	3A	
			20	1A	
			21	3A	
			22	1A	
			23	3A	
			24	3A	
			25	2A	
	26	3A			
	27	2A			
	28	3A			
	29	3A	3B		
	30	1A			
	31	3A			
	32	2A			
	33	2A			
	34	2A			
	35	2A	3B		
	36	2A			
	37	2A			
	38	2A			
	39	3A	3B		
	3A	Page9:Add R45,R51,R64,R65,R68,R69,R72,E73 to solve the HDMI issue Page10 : for CRT filicker, change C179,C191,C491,C125,C192 value from 2.2u to 10u. Page14 : change the board ID. 7/10 Page17 : Duo to cost down, so to remove Q25 ,Q45 from MXM BOM. Page19 : add LCD panel circuit to fix white display when system boot up. Page21 : to solve the Lan issue, ADD C479,C480 Page23 : change Gain from 15.6 to 10 db. 7/8 Page24 : Change C498,C499 ,C585,C587 value form 3900P to 0.001U Page26 : to solve the EMI issue, ADD L52,L53 Page28 : For EMI request. add C618,C619 7/10 Page26 : to solve the EMI issue, ADD L52,L53 Page29 : Change R509 PN from 2M to 0ohm. Change R85,R86,R275 ,R273,R274 to 300 ohm, Del D31& C636 & D2 from BOM Page26 : to solve the EMI issue, ADD L52,L53 Page31 : PL13 PN change to CV01014TZ01			
3B	Page2 : ADD C648(CH11006JB00) , for EMI request (+1.2v) Page11 :Change C56 and C493 from 4.7u/6.3V to 330u/2V (CH733RY8802) to solve" HIGH POWER NOSIE ISSUE" Page17 :Add C238 (CC71004MZ81) to solve" HIGH POWER NOSIE ISSUE" Page29 :For slowly pulse" light to dark about 2 second, ADD R510,R576,R577, Q70,Q71,D34,D35 ,C636,C646,C647 ,R302 ,R521 ; DEL R273,R274,R509 Page35 :Change PC90 and PC92 from 10u/25V to 27u/25V (CC62704MZ02) to solve" HIGH POWER NOSIE ISSUE"				
Project :AJ6 MB		MB Assy' P/N: 31AJ6MB0030/40	Document No.:		
Approved by : Johnny_0		Drawing by :Kenneth Huang	DATE: 2008/8/19		
			 NB2/RD1 PROJECT : AJ6 Quanta Computer Inc. Size Custom Document Number EC Date: Thursday, August 21, 2008 Sheet 39 of 39 Rev 3B		