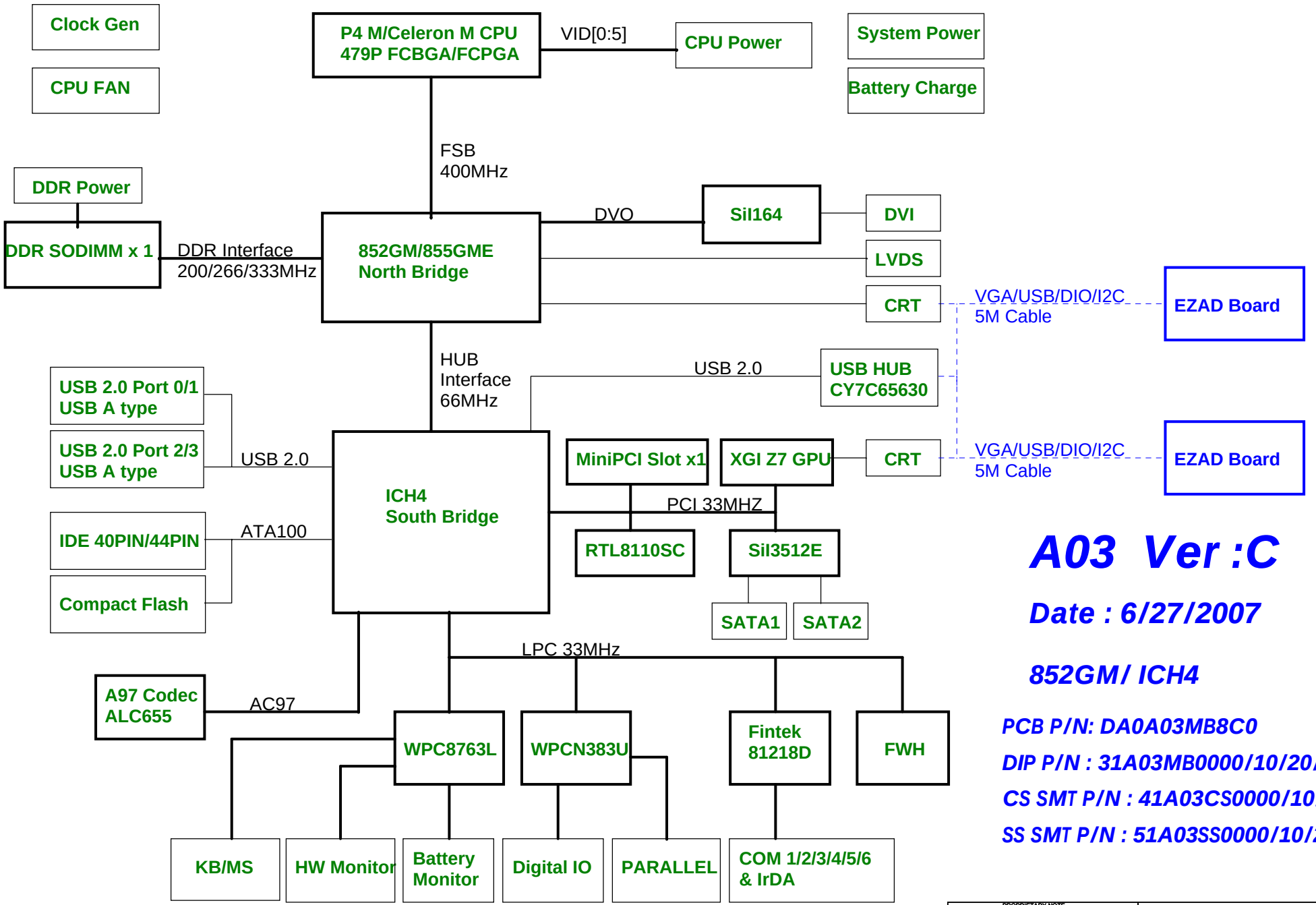

A03 Ver :C

Date : 6/27/2007

852GM/ ICH4

PCB P/N: DA0A03MB8C0

DIP P/N : 31A03MB0000/10/20/30

CS SMT P/N : 41A03CS0000/10/20/30

SS SMT P/N : 51A03SS0000/10/20/30

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Quanta Computer Inc.

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Figure 17-18. Power Sequencing and Reset Signal Timings

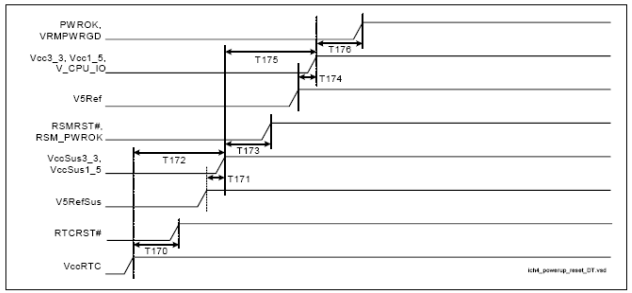
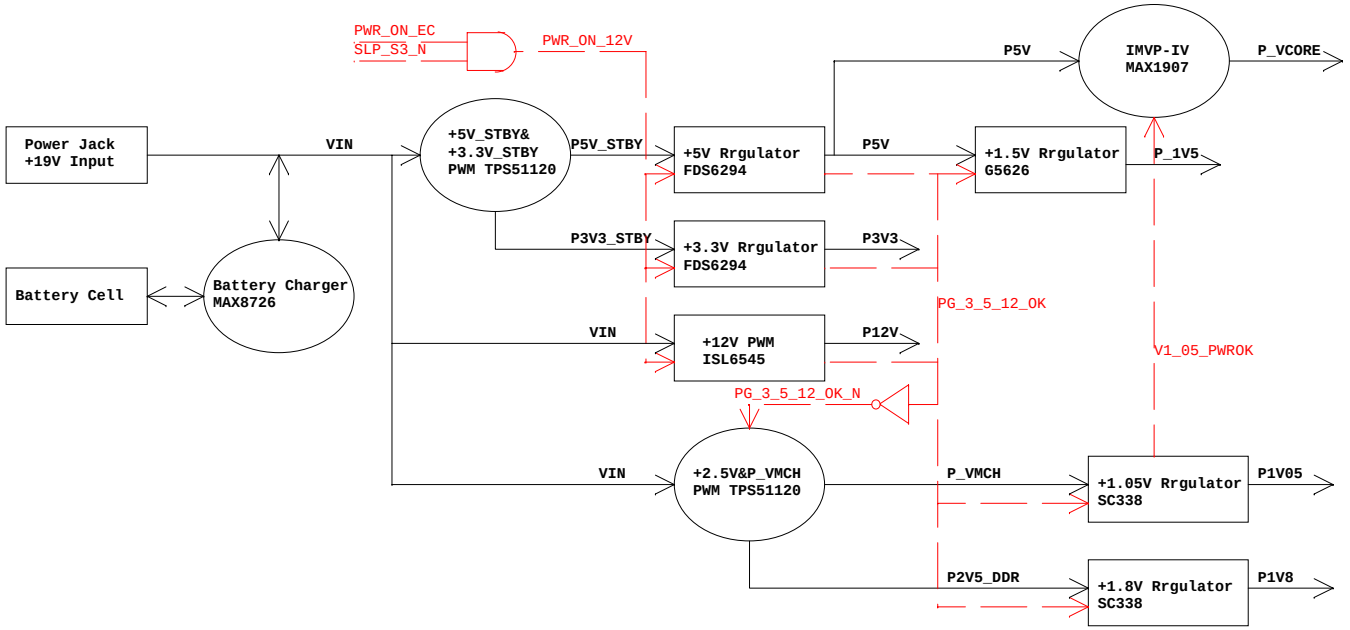


Table 17-19. Power Sequencing and Reset Signal Timings

Sym	Parameter	Min	Max	Units	Notes	Fig
t170	VccRTC active to RTCRST# inactive	5	—	ms		17-18
t171	V5RefSus active to VccSus3_3, VccSus1_5 active	0	—	ms	1	17-18
t172	VccRTC supply active to VccSus supplies active	0	—	ms	2	17-18
t173	VccSus supplies active to LAN_RST# active, RSMRST# inactive	10	—	ms		17-18 17-20
t174	V5Ref active to Vcc3_3, Vcc1_5, VccHI active	0	—	ms	1	17-18
t175	VccSus supplies active to Vcc supplies active	0	—	ms	2	17-18
t176	Vcc supplies active to PWROK, VRMPWRGD active	10	—	ms		17-18 17-20
t177	PWROK and VRMPWRGD and SYS_RESET#inactive to SUS_STAT# inactive	32	38	RTCCLK		17-20
t178	SUS_STAT# inactive to PCIRST# inactive	1	3	RTCCLK		17-20
t179	AC_RST# active low pulse width	1		us		
t180	AC_RST# inactive to BIT_CLK startup delay	162.8		ns		

NOTES:
1. The V5Ref supply must power up before or simultaneous with its associated 3.3 V supply, and must power down simultaneous with or after the 3.3 V supply. See Section 2.20.3 for details.
2. The VccSus supplies must **never** be active while the VccRTC supply is inactive. Likewise, the Vcc supplies must **never** be active while the VccSus supplies are inactive.



JP1 : Clear CMOS.		
	Function	Default setting
1 -- 2	Protect	V
2 -- 3	Clear CMOS	

JP2 : LCD Panel Voltage		
	Function	Default setting
1 -- 2	5V	
2 -- 3	3.3V	V

S1 : LCD Panel select				LCD Panel Type
1	2	3	4	
OFF	OFF	OFF	OFF	15",1024*768/24bit, 1-CH,Normal
OFF	OFF	ON	OFF	17/19",1280*1024/24bit, 2-CH,Normal
OFF	ON	OFF	OFF	10.4",800*600/18bit, 1-CH,Normal
ON	OFF	OFF	OFF	1024*768/18bit, 1-CH,Special
ON	OFF	ON	OFF	800*600/18bit, 1-CH,Special

Fintek 81218D GPIO						Fnction List
GP12		GP11		GP10		
R662	R667	R663	R666	R664	R675	
OFF	ON	OFF	ON	OFF	ON	W/ XGI Z7(64MB),SiI3512E(SATA), SiI164(DVI)
OFF	ON	OFF	ON	ON	OFF	W/O XGI Z7,SiI3512E(SATA),SiI164(DVI)
OFF	ON	ON	OFF	OFF	ON	W/ XGI Z7(32MB),SiI3512E(SATA), SiI164(DVI)
OFF	ON	ON	OFF	ON	OFF	W/O XGI Z7,SiI3512E(SATA),SiI164(DVI) ,WPCN383(Parallel Port)
ON	OFF	OFF	ON	OFF	ON	A05 Project feature

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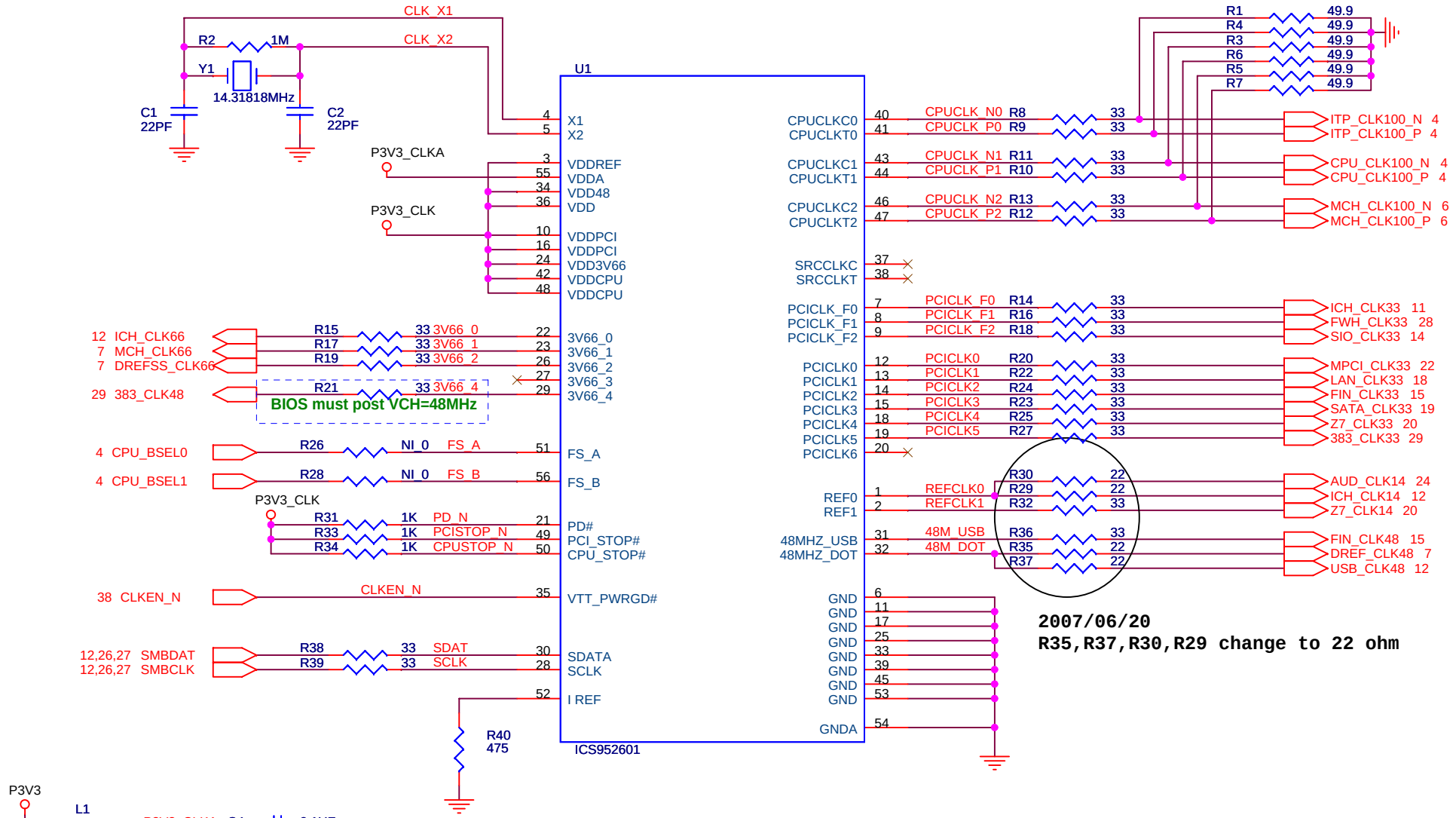
Power Sequence
Date: Wednesday, July 04, 2007 | Sheet 2 of 38



FS_A	FS_B	CPU SPEED
0	0	100MHz
0	1	200MHz
1	0	133MHz
1	1	166MHz

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Quanta Computer Inc.

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Clock Gen

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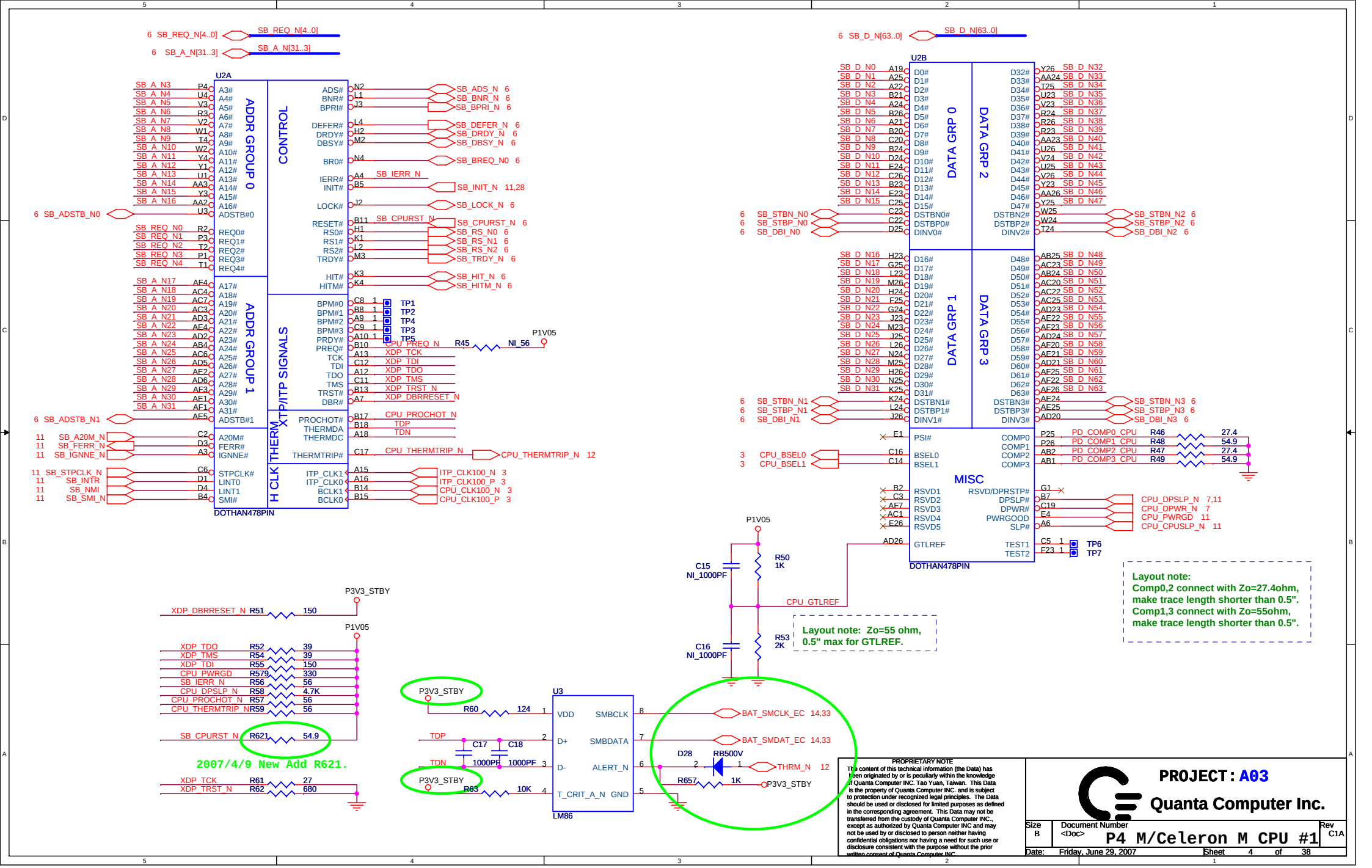
6 SB_REQ_N[4..0]
SB_REQ_N[4..0]
6 SB_A_N[31..3]
SB_A_N[31..3]
U2A
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XTP/ITP SIGNALS
THERM
H CLK
DOTHAN478PIN
6 SB_ADSTB_N0
6 SB_ADSTB_N1
11 SB_A20M_N
11 SB_FERR_N
11 SB_IGNNE_N
11 SB_STPCLK_N
11 SB_INTR
11 SB_NMI
11 SB_SMI_N
SB_ADS_N 6
SB_BNR_N 6
SB_BPRI_N 6
SB_DEFER_N 6
SB_DRDY_N 6
SB_DBSY_N 6
SB_BREQ_N0 6
SB_IERR_N
SB_INIT_N 11,28
SB_LOCK_N 6
SB_CPURST_N
SB_CPURST_N 6
SB_RS_N0 6
SB_RS_N1 6
SB_RS_N2 6
SB_TRDY_N 6
SB_HIT_N 6
SB_HITM_N 6
TP1
TP2
TP3
TP4
TP5
P1V05
CPU_PREQ_N
R45
NI_56
XDP_TCK
XDP_TDI
XDP_TDO
XDP_TMS
XDP_TRST_N
XDP_DBRRESET_N
CPU_PROCHOT_N
TDP
TDN
CPU_THERMTRIP_N
CPU_THERMTRIP_N 12
ITP_CLK100_N 3
ITP_CLK100_P 3
CPU_CLK100_N 3
CPU_CLK100_P 3
6 SB_D_N[63..0]
SB_D_N[63..0]
U2B
DATA GRP 0
DATA GRP 2
DATA GRP 1
DATA GRP 3
6 SB_STBN_N0
6 SB_STBP_N0
6 SB_DBI_N0
6 SB_STBN_N1
6 SB_STBP_N1
6 SB_DBI_N1
SB_STBN_N2 6
SB_STBP_N2 6
SB_DBI_N2 6
SB_STBN_N3 6
SB_STBP_N3 6
SB_DBI_N3 6
MISC
3 CPU_BSEL0
3 CPU_BSEL1
PD_COMP0_CPU
PD_COMP1_CPU
PD_COMP2_CPU
PD_COMP3_CPU
R46 27.4
R48 54.9
R47 27.4
R49 54.9
CPU_DPSLP_N 7,11
CPU_DPWR_N 7
CPU_PWRGD 11
CPU_CPUSLP_N 11
TP6
TP7
P3V3_STBY
P1V05
R51 150
R52 39
R54 39
R55 150
R579 330
R56 56
R58 4.7K
R57 56
R59 56
R621 54.9
2007/4/9 New Add R621.
R61 27
R62 680
C15 NI_1000PF
C16 NI_1000PF
R50 1K
R53 2K
CPU_GTLREF
Layout note: Zo=55 ohm, 0.5" max for GTLREF.
Layout note:
Comp0,2 connect with Zo=27.4ohm, make trace length shorter than 0.5".
Comp1,3 connect with Zo=55ohm, make trace length shorter than 0.5".
U3
LM86
VDD
D+
D-
T_CRIT_A_N
SMBCLK
SMBDATA
ALERT_N
GND
R60 124
R63 10K
C17 1000PF
C18 1000PF
BAT_SMCLK_EC 14,33
BAT_SMDAT_EC 14,33
THRM_N 12
D28 RB500V
R657 1K
PROPRIETARY NOTE
Quanta Computer Inc.
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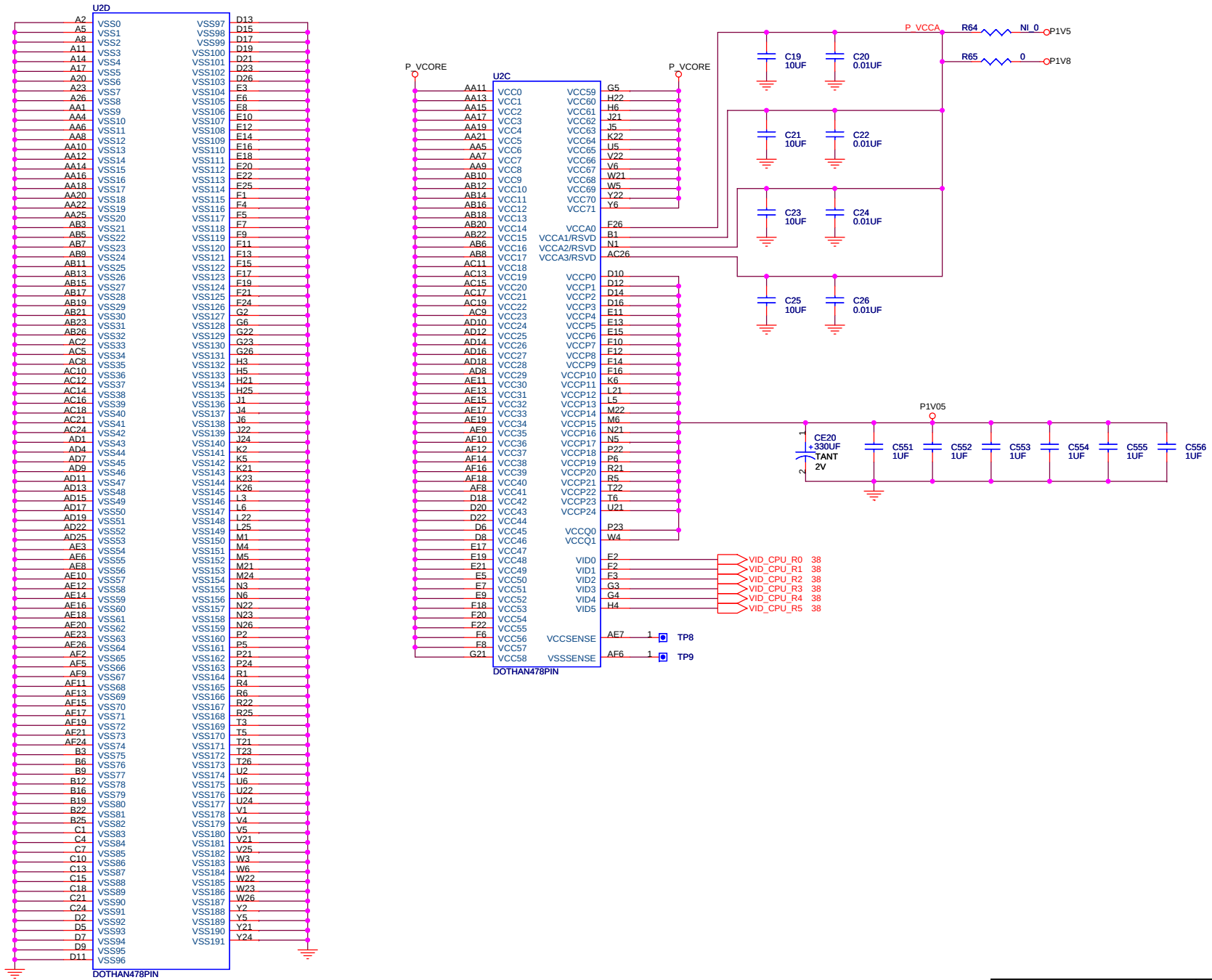

PROJECT: A03

Quanta Computer Inc.

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A3	<Doc> P4M/Celeron M CPU #2	C1A

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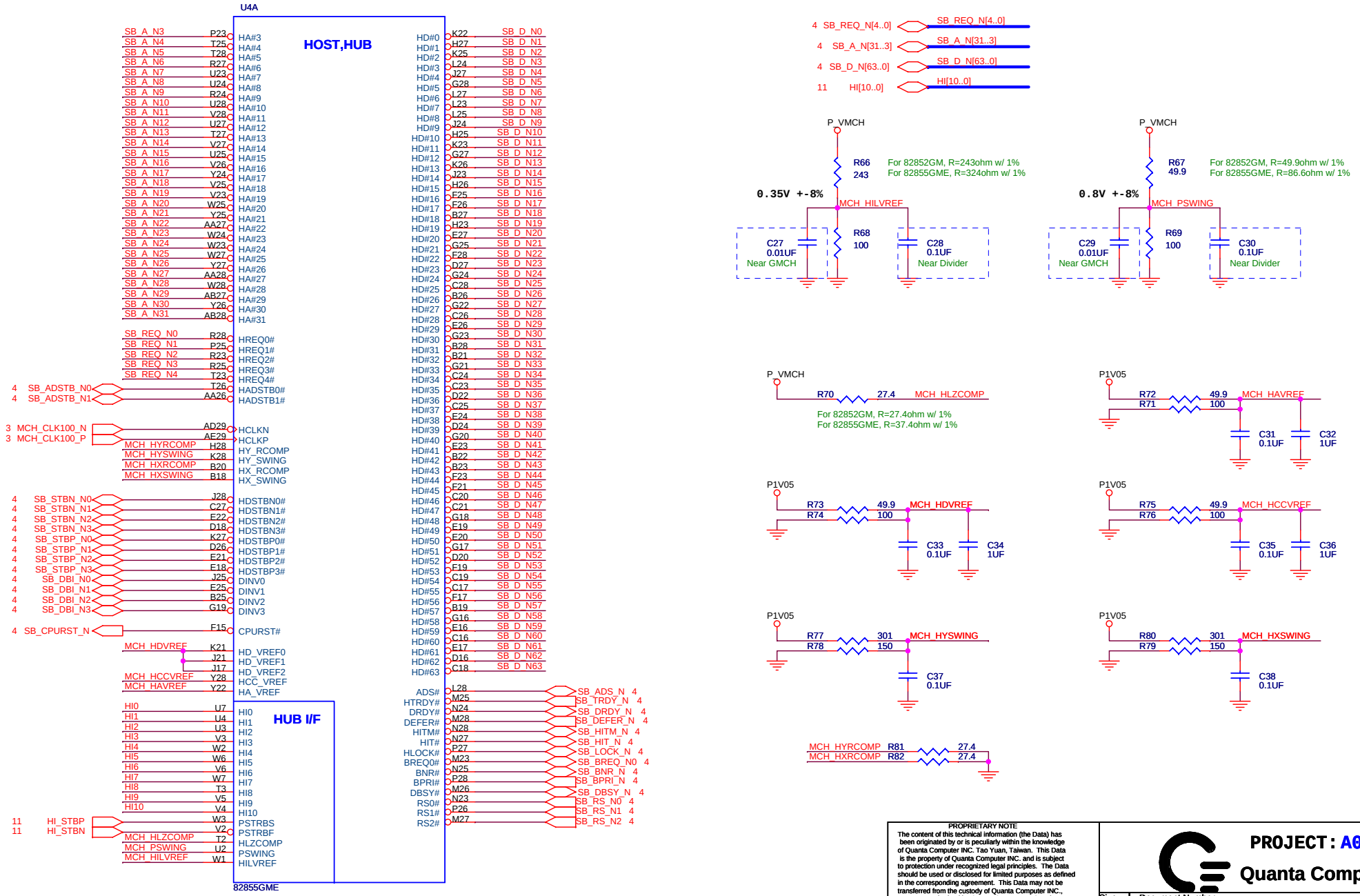
U4A
HOST,HUB
HUB I/F
82855GME
SB_A_N3
SB_A_N4
SB_A_N5
SB_A_N6
SB_A_N7
SB_A_N8
SB_A_N9
SB_A_N10
SB_A_N11
SB_A_N12
SB_A_N13
SB_A_N14
SB_A_N15
SB_A_N16
SB_A_N17
SB_A_N18
SB_A_N19
SB_A_N20
SB_A_N21
SB_A_N22
SB_A_N23
SB_A_N24
SB_A_N25
SB_A_N26
SB_A_N27
SB_A_N28
SB_A_N29
SB_A_N30
SB_A_N31
SB_REQ_N0
SB_REQ_N1
SB_REQ_N2
SB_REQ_N3
SB_REQ_N4
4 SB_ADSTB_N0
4 SB_ADSTB_N1
3 MCH_CLK100_N
3 MCH_CLK100_P
MCH_HYRCOMP
MCH_HYSWING
MCH_HXRCOMP
MCH_HXSWING
4 SB_STBN_N0
4 SB_STBN_N1
4 SB_STBN_N2
4 SB_STBN_N3
4 SB_STBP_N0
4 SB_STBP_N1
4 SB_STBP_N2
4 SB_STBP_N3
4 SB_DBI_N0
4 SB_DBI_N1
4 SB_DBI_N2
4 SB_DBI_N3
4 SB_CPURST_N
MCH_HDVREF
MCH_HCCVREF
MCH_HAVREF
HI0
HI1
HI2
HI3
HI4
HI5
HI6
HI7
HI8
HI9
HI10
11 HI_STBP
11 HI_STBN
MCH_HLZCOMP
MCH_PSWING
MCH_HILVREF
HA#3
HA#4
HA#5
HA#6
HA#7
HA#8
HA#9
HA#10
HA#11
HA#12
HA#13
HA#14
HA#15
HA#16
HA#17
HA#18
HA#19
HA#20
HA#21
HA#22
HA#23
HA#24
HA#25
HA#26
HA#27
HA#28
HA#29
HA#30
HA#31
HREQ0#
HREQ1#
HREQ2#
HREQ3#
HREQ4#
HADSTB0#
HADSTB1#
HCLKN
HCLKP
HY_RCOMP
HY_SWING
HX_RCOMP
HX_SWING
HDSTBN0#
HDSTBN1#
HDSTBN2#
HDSTBN3#
HDSTBP0#
HDSTBP1#
HDSTBP2#
HDSTBP3#
DINV0
DINV1
DINV2
DINV3
CPURST#
HD_VREF0
HD_VREF1
HD_VREF2
HCC_VREF
HA_VREF
HI0
HI1
HI2
HI3
HI4
HI5
HI6
HI7
HI8
HI9
HI10
PSTRBS
PSTRBF
HLZCOMP
PSWING
HILVREF
HD#0
HD#1
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HD#62
HD#63
ADS#
HTRDY#
DRDY#
DEFER#
HITM#
HIT#
HLOCK#
BREQ0#
BNR#
BPRI#
DBSY#
RS0#
RS1#
RS2#
SB_D_N0
SB_D_N1
SB_D_N2
SB_D_N3
SB_D_N4
SB_D_N5
SB_D_N6
SB_D_N7
SB_D_N8
SB_D_N9
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SB_D_N57
SB_D_N58
SB_D_N59
SB_D_N60
SB_D_N61
SB_D_N62
SB_D_N63
SB_ADS_N 4
SB_TRDY_N 4
SB_DRDY_N 4
SB_DEFER_N 4
SB_HITM_N 4
SB_HIT_N 4
SB_LOCK_N 4
SB_BREQ_N0 4
SB_BNR_N 4
SB_BPRI_N 4
SB_DBSY_N 4
SB_RS_N0 4
SB_RS_N1 4
SB_RS_N2 4
4 SB_REQ_N[4..0]
SB_REQ_N[4..0]
4 SB_A_N[31..3]
SB_A_N[31..3]
4 SB_D_N[63..0]
SB_D_N[63..0]
11 HI[10..0]
HI[10..0]
P_VMCH
R66
243
For 82852GM, R=243ohm w/ 1%
For 82855GME, R=324ohm w/ 1%
0.35V +-8%
MCH_HILVREF
R68
100
C27
0.01UF
Near GMCH
C28
0.1UF
Near Divider
P_VMCH
R67
49.9
For 82852GM, R=49.9ohm w/ 1%
For 82855GME, R=86.6ohm w/ 1%
0.8V +-8%
MCH_PSWING
R69
100
C29
0.01UF
Near GMCH
C30
0.1UF
Near Divider
P_VMCH
R70
27.4
MCH_HLZCOMP
For 82852GM, R=27.4ohm w/ 1%
For 82855GME, R=37.4ohm w/ 1%
P1V05
R72
R71
49.9
100
MCH_HAVREF
C31
0.1UF
C32
1UF
P1V05
R73
R74
49.9
100
MCH_HDVREF
C33
0.1UF
C34
1UF
P1V05
R75
R76
49.9
100
MCH_HCCVREF
C35
0.1UF
C36
1UF
P1V05
R77
R78
301
150
MCH_HYSWING
C37
0.1UF
P1V05
R80
R79
301
150
MCH_HXSWING
C38
0.1UF
MCH_HYRCOMP R81 27.4
MCH_HXRCOMP R82 27.4
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RG82852GM w/o DVO Channel B

U4C

DVO

DVOBD0 DVOBD1 DVOBD2 DVOBD3 DVOBD4 DVOBD5 DVOBD6 DVOBD7 DVOBD8 DVOBD9 DVOBD10 DVOBD11

DVOBCLK DVOBCLK# DVOBHSYNC DVOBVSYNC DVOBBLANK# DVOBFLDSTL

23 DVOBCINTR_N → DVOBCINTR_N / DVOBCCLKINT → DVOBCINTRB DVOBCCLKINT

DVOCD0 DVOCD1 DVOCD2 DVOCD3 DVOCD4 DVOCD5 DVOCD6 DVOCD7 DVOCD8 DVOCD9 DVOCD10 DVOCD11

23 DVOCD[11..0] → DVOCD[11..0]

23 DVOCCLK_P
23 DVOCCLK_N
23 DVOCHSYNC
23 DVOCVSYNC
23 DVOCBLANK_N

DVOCCLK DVOCCLK# DVOCHSYNC DVOCVSYNC DVOCBLANK# DVOCFLDSTL

23 MI2CCLK
23 MI2CDAT
23 MDVICLK
23 MDVIDAT

MI2CCLK MI2CDATA MDVICLK MDVIDATA MDDCCLK MDDCDATA

ADDID0 ADDID1 ADDID2 ADDID3 ADDID4 ADDID5 ADDID6 ADDID7 ADDETECT DPMS GVREF AGPBUSY# GRCOMP 66IN

R86 100K DVOBCCLKINT
R85 100K DVOBFLDSTL
R87 100K DVOCFLDSTL

R88 1K ADDID7
R89 1K ADDETECT

MCH_SUS_CLK

DVO_GVREF

P3V3 R91 8.2K MCH_AGPBUSY_N

MCH_DVORCOMP

3 MCH_CLK66

R92 40.2

Trace 10mils : Space 20mils

RVSD0 RVSD1 RVSD2 RVSD3 RVSD4 RVSD5 RVSD6 RVSD7 RVSD8 RVSD9 RVSD10 RVSD11

TP42 TP41 TP43

P1V5

R90 1K

MCH_SUS_CLK

Q97 BSS138LT1G

12 SUS_CLK

P1V5

R94 1K

DVO_GVREF → DVO_GVREF 23

R104 1K

C43 0.1UF

DAC

BLUE BLUE# GREEN GREEN# RED RED# HSYNC VSYNC REFSET DDCA_CLK DDCA_DATA

MCH_BLUE 26
MCH_GREEN 26
MCH_RED 26
MCH_HSYNC 26
MCH_VSYNC 26

MCH_REFSET R83 127

MCH_DDCACLK 26
MCH_DDCADAT 26

LVDS

IYAM0 IYAM1 IYAM2 IYAM3 IYAP0 IYAP1 IYAP2 IYAP3 IYBM0 IYBM1 IYBM2 IYBM3 IYBP0 IYBP1 IYBP2 IYBP3 ICLKAM ICLKAP ICLKBM ICLKBP

LVDS_TXL_N0 25
LVDS_TXL_N1 25
LVDS_TXL_N2 25
LVDS_TXL_N3 25
LVDS_TXL_P0 25
LVDS_TXL_P1 25
LVDS_TXL_P2 25
LVDS_TXL_P3 25
LVDS_TXU_N0 25
LVDS_TXU_N1 25
LVDS_TXU_N2 25
LVDS_TXU_N3 25
LVDS_TXU_P0 25
LVDS_TXU_P1 25
LVDS_TXU_P2 25
LVDS_TXU_P3 25
LVDS_TXLC_N 25
LVDS_TXLC_P 25
LVDS_TXUC_N 25
LVDS_TXUC_P 25

DDCPCLK DDCPDATA

LVDS_DDCPCLK
LVDS_DDCPDATA

PANELBKLTCTL PANELBKLTEN PANELVDDEN

R607 0
R564 0
R565 0

LVDS_BKLTCTL 14,25
LVDS_BKLTEN 14,25
LVDS_VDDEN 14,25

LVREFH LVREFL

LVBG LIBG

MCH_LIBG R84 1.5K

CLKS

DREFCLK DREFSSCLK LCLKCTLA LCLKCTLB

DREF_CLK48 3
DREFSS_CLK66 3

LCLKCTLB R593 1K P3V3

MISC

DPWR# DPSLP# RSTIN# PWROK EXTTS0 MCHDETECTVSS

CPU_DPWR_N 4
CPU_DPSLP_N 4,11
PCIRST_N 11,14,23,28,29
IMVPWRGD 12,14,37,38

MCH_EXTTS0 R594 10K P3V3

NC

NC0 NC1 NC2 NC3 NC4 NC5 NC6 NC7 NC8 NC9 NC10 NC11

82855GME

CPU_DPSLP_N R93 1K P1V05

MI2CCLK R95 2.2K
MI2CDAT R96 2.2K
MDVICLK R97 2.2K
MDVIDAT R98 2.2K
MDDCCLK R99 2.2K
MDDCDAT R103 2.2K

DVOBCINTR_N R105 100K

LVDS_DDCPCLK R110 2.2K
LVDS_DDCPDATA R109 2.2K

P3V3

P2V5_DDR

R100 60.4
R101 150
R102 604

MCH_SMRCOMP
MCH_SMVSWINGH
MCH_SMVSWINGL

R106 60.4
R107 604
R108 150

9 DM_MD[0..63] → DM_MD[0..63]
9 DM_CB[0..7] → DM_CB[0..7]
9 DM_SDM[0..8] → DM_SDM[0..8]
9 DM_SDQS[0..8] → DM_SDQS[0..8]

U4B

DDR

DM_MD0 DM_MD1 DM_MD2 DM_MD3 DM_MD4 DM_MD5 DM_MD6 DM_MD7 DM_MD8 DM_MD9 DM_MD10 DM_MD11 DM_MD12 DM_MD13 DM_MD14 DM_MD15 DM_MD16 DM_MD17 DM_MD18 DM_MD19 DM_MD20 DM_MD21 DM_MD22 DM_MD23 DM_MD24 DM_MD25 DM_MD26 DM_MD27 DM_MD28 DM_MD29 DM_MD30 DM_MD31 DM_MD32 DM_MD33 DM_MD34 DM_MD35 DM_MD36 DM_MD37 DM_MD38 DM_MD39 DM_MD40 DM_MD41 DM_MD42 DM_MD43 DM_MD44 DM_MD45 DM_MD46 DM_MD47 DM_MD48 DM_MD49 DM_MD50 DM_MD51 DM_MD52 DM_MD53 DM_MD54 DM_MD55 DM_MD56 DM_MD57 DM_MD58 DM_MD59 DM_MD60 DM_MD61 DM_MD62 DM_MD63 DM_CB0 DM_CB1 DM_CB2 DM_CB3 DM_CB4 DM_CB5 DM_CB6 DM_CB7

SDQ_0 SDQ_1 SDQ_2 SDQ_3 SDQ_4 SDQ_5 SDQ_6 SDQ_7 SDQ_8 SDQ_9 SDQ_10 SDQ_11 SDQ_12 SDQ_13 SDQ_14 SDQ_15 SDQ_16 SDQ_17 SDQ_18 SDQ_19 SDQ_20 SDQ_21 SDQ_22 SDQ_23 SDQ_24 SDQ_25 SDQ_26 SDQ_27 SDQ_28 SDQ_29 SDQ_30 SDQ_31 SDQ_32 SDQ_33 SDQ_34 SDQ_35 SDQ_36 SDQ_37 SDQ_38 SDQ_39 SDQ_40 SDQ_41 SDQ_42 SDQ_43 SDQ_44 SDQ_45 SDQ_46 SDQ_47 SDQ_48 SDQ_49 SDQ_50 SDQ_51 SDQ_52 SDQ_53 SDQ_54 SDQ_55 SDQ_56 SDQ_57 SDQ_58 SDQ_59 SDQ_60 SDQ_61 SDQ_62 SDQ_63 SDQ_64 SDQ_65 SDQ_66 SDQ_67 SDQ_68 SDQ_69 SDQ_70 SDQ_71

10 DDRVREF → AJ24 SMVREF

C39 0.1UF

SDQS0 SDQS1 SDQS2 SDQS3 SDQS4 SDQS5 SDQS6 SDQS7 SDQS8

DM_SDQS0 DM_SDQS1 DM_SDQS2 DM_SDQS3 DM_SDQS4 DM_SDQS5 DM_SDQS6 DM_SDQS7 DM_SDQS8

SMA_A0 SMA_A1 SMA_A2 SMA_A3 SMA_A4 SMA_A5 SMA_A6 SMA_A7 SMA_A8 SMA_A9 SMA_A10 SMA_A11 SMA_A12

DM_MAA0 9
RM_MAA1 9,10
RM_MAA2 9,10
DM_MAA3 9
RM_MAA4 9,10
RM_MAA5 9,10
DM_MAA6 9
DM_MAA7 9
DM_MAA8 9
DM_MAA9 9
DM_MAA10 9
DM_MAA11 9
DM_MAA12 9

SMA_B1 SMA_B2 SMA_B4 SMA_B5

SCKE0 SCKE1 SCKE2 SCKE3 SCS#0 SCS#1 SCS#2 SCS#3

RM_CKE0 9,10
RM_CKE1 9,10
RM_SCS0 9,10
RM_SCS1 9,10

SBA1 SBA0

DM_BS_N1 9
DM_BS_N0 9

SRAS# SCAS# SWE#

DM_RAS_N 9
DM_CAS_N 9
DM_WE_N 9

SCMD_CLK0 SCMD_CLK0# SCMD_CLK1 SCMD_CLK1# SCMD_CLK2 SCMD_CLK2# SCMD_CLK3 SCMD_CLK3# SCMD_CLK4 SCMD_CLK4# SCMD_CLK5 SCMD_CLK5#

MEMCLK_P0 10
MEMCLK_N0 10
MEMCLK_P1 10
MEMCLK_N1 10
MEMCLK_P2 10
MEMCLK_N2 10

SDM0 SDM1 SDM2 SDM3 SDM4 SDM5 SDM6 SDM7 SDM8

DM_SDM0 DM_SDM1 DM_SDM2 DM_SDM3 DM_SDM4 DM_SDM5 DM_SDM6 DM_SDM7 DM_SDM8

SRCVENOUT# SRCVENIN#

TP11 TP12

SMRCOMP

MCH_SMRCOMP

SMVSWINGL SMVSWINGH

MCH_SMVSWINGL MCH_SMVSWINGH

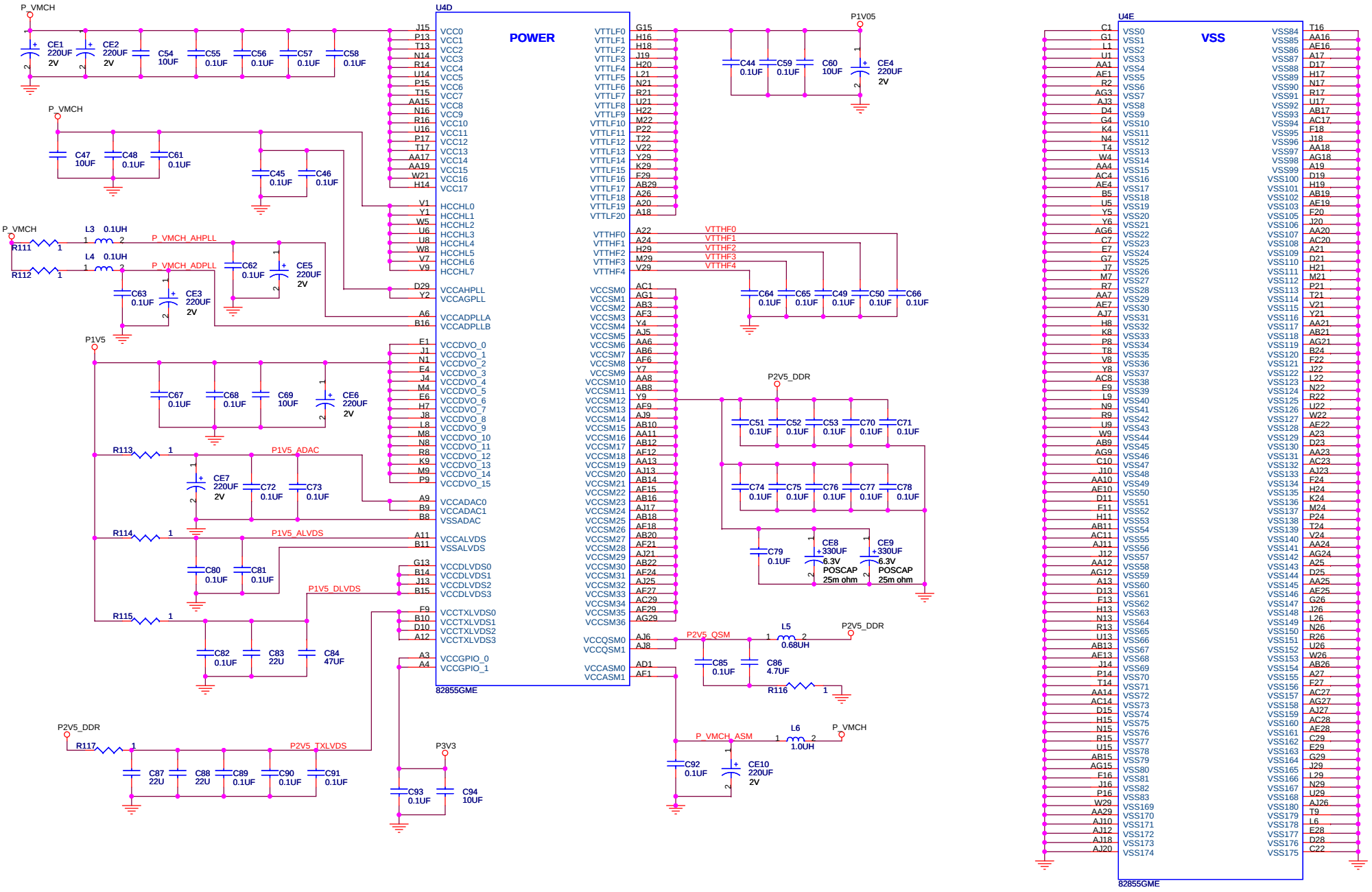
C40 0.1UF C41 0.1UF C42 0.1UF

82855GME

PROJECT : A03

Quanta Computer Inc.

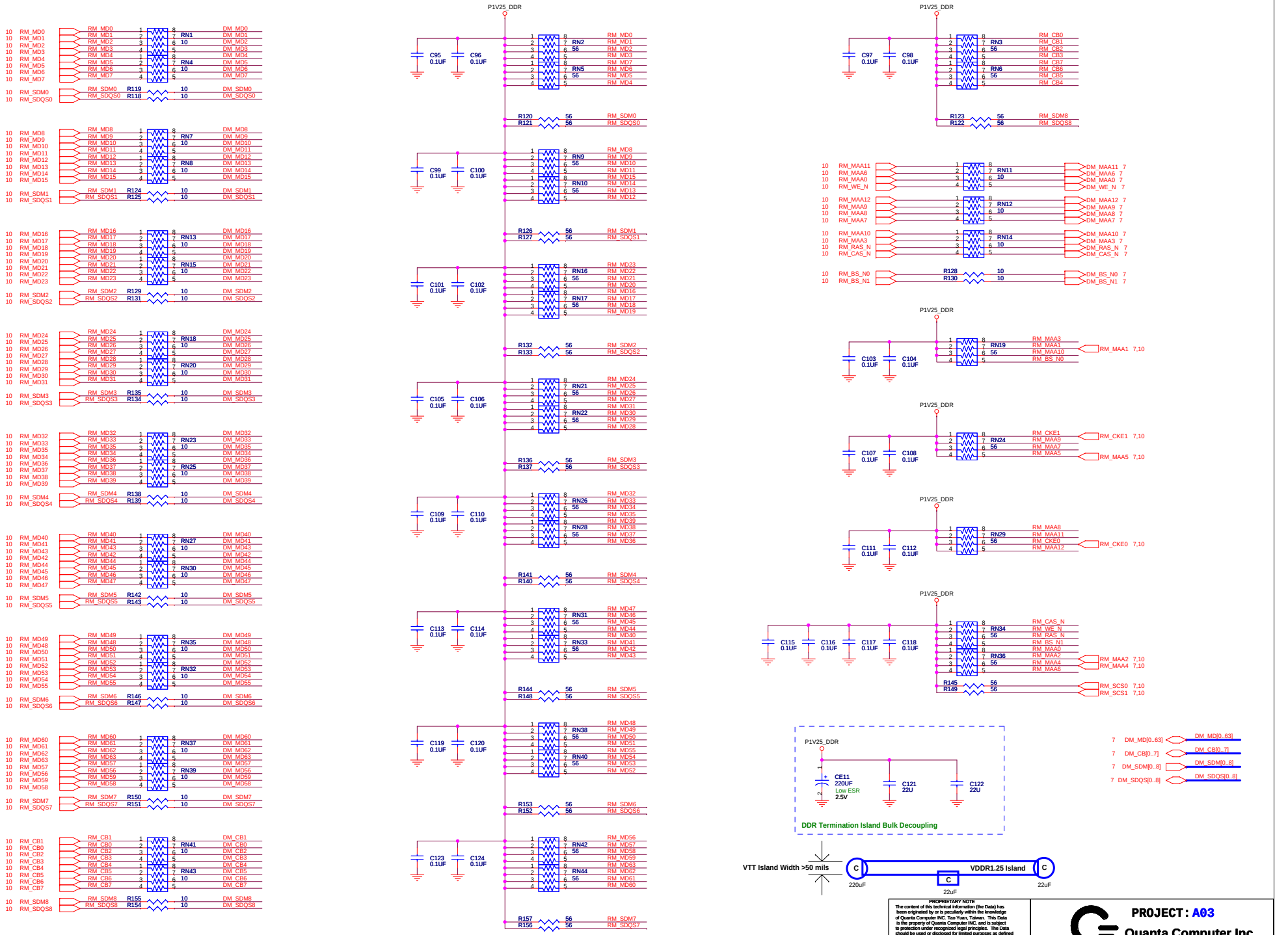
Size	Document Number	Rev
A3	<Doc> NB 82852GM/GME #2	C1A
Date: Friday, June 29, 2007	Sheet 7 of 38	



PROJECT: A03

Quanta Computer Inc.

Size	Document Number	Rev
A3	<Doc> NB 82852GM/GME #3	C1A
Date: Friday, June 29, 2007	Sheet 8 of 38	



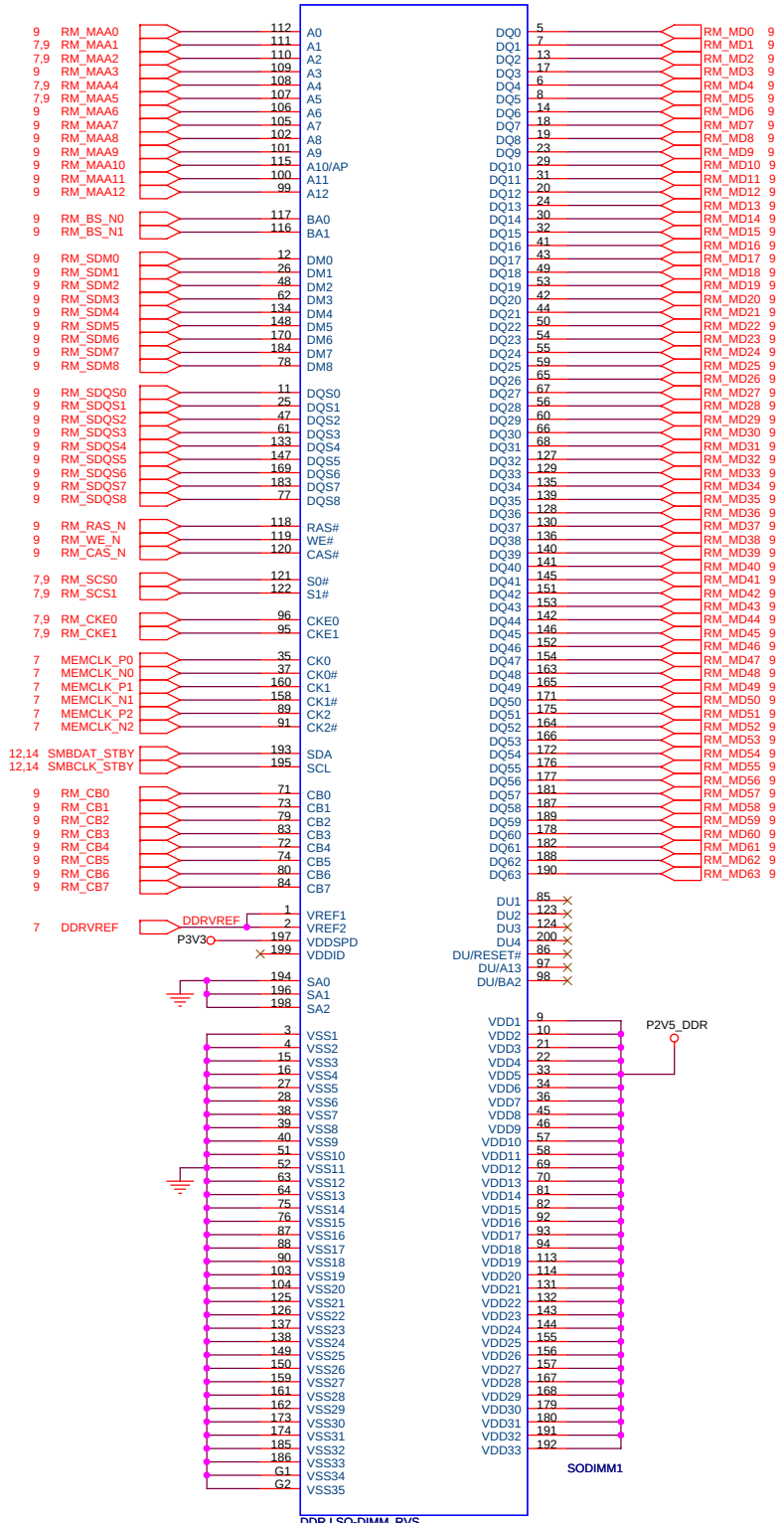
PROJECT: A03

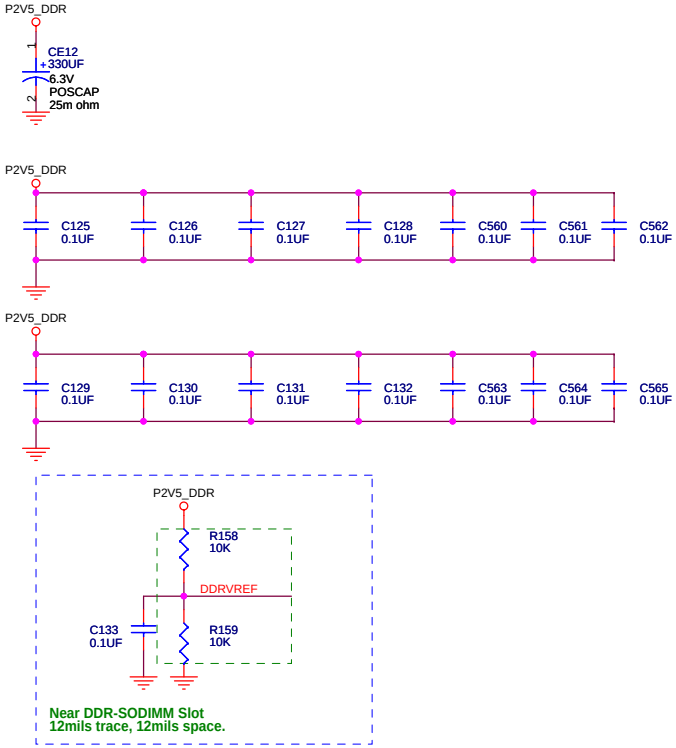
Quanta Computer Inc.

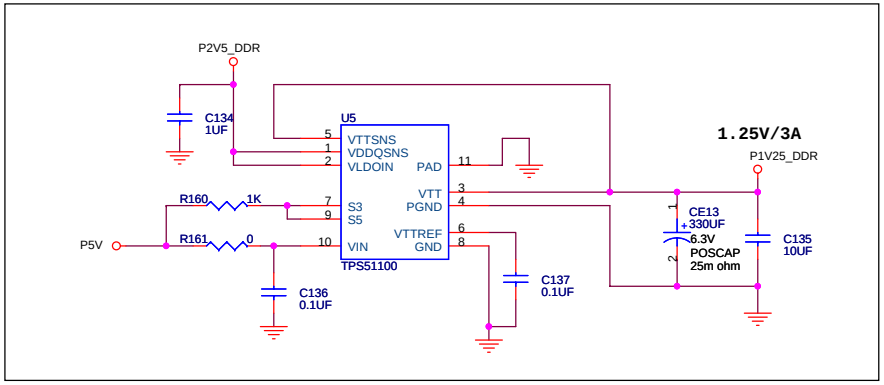
Size	Document Number	Rev
C	<Doc>	C1A

DDR Termination

Date: Friday, June 29, 2007 Sheet 9 of 38



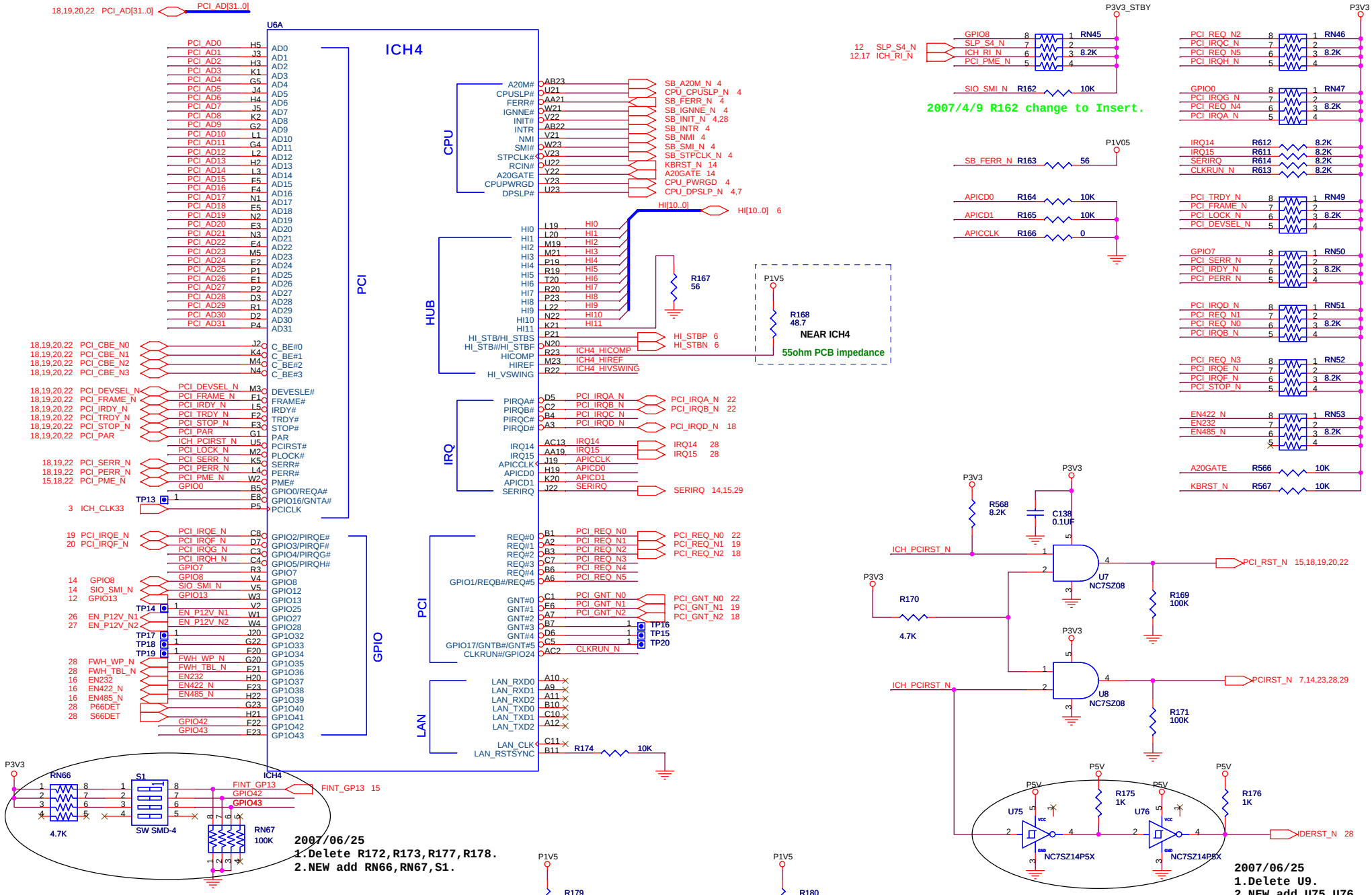




PROJECT: A03

Quanta Computer Inc.

Size	Document Number	Rev
A3	<Doc> DDR SODIMM	C1A
Date: Friday, June 29, 2007	Sheet 10 of 38	



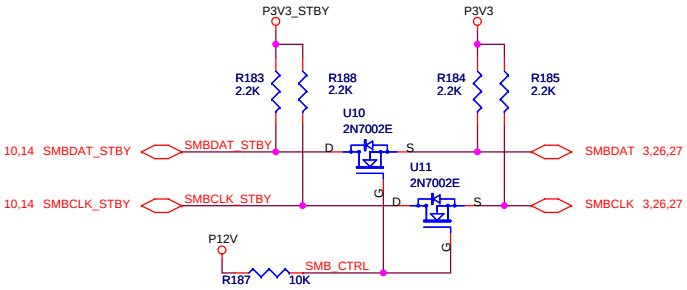
FINT_GP13	GPIO42	GPIO43	LCD Panel Setting
0	0	0	15",1024*768/24bit, 1-CH,Normal
0	0	1	17/19",1280*1024/24bit, 2-CH,Normal
0	1	0	10.4",800*600/18bit, 1-CH,Normal
1	0	0	1024*768/18bit, 1-CH, Special
1	0	1	800*600/18bit, 1-CH, Special

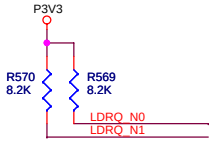
PROJECT: A03

Quanta Computer Inc.

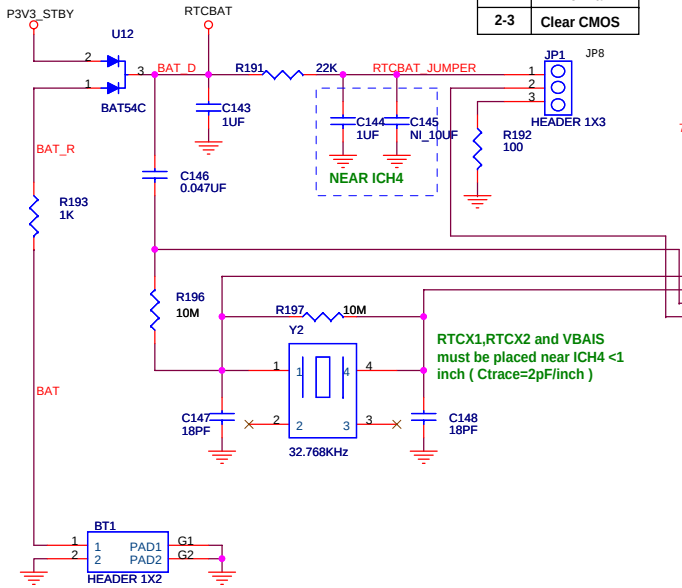
Size	Document Number	Rev
A3	<Doc> SB 82801 ICH4 #1	C1A
Date: Friday, June 29, 2007	Sheet 11 of 38	

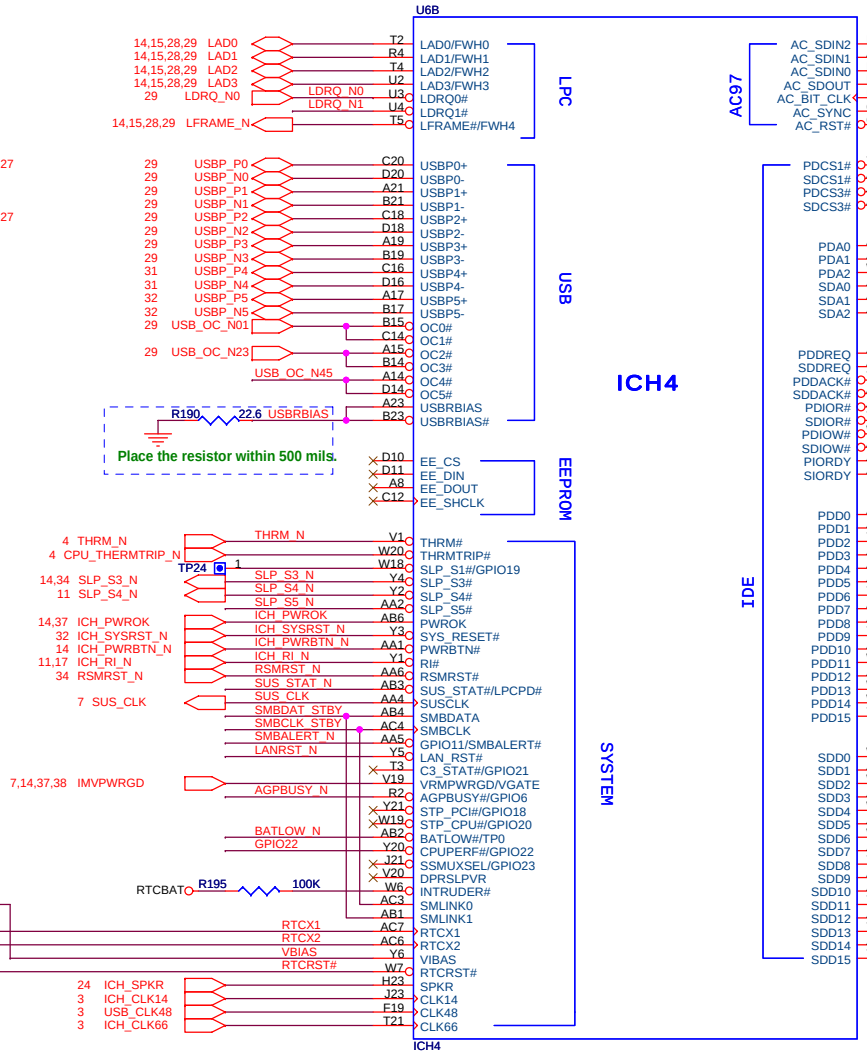
SMBUS Isolation

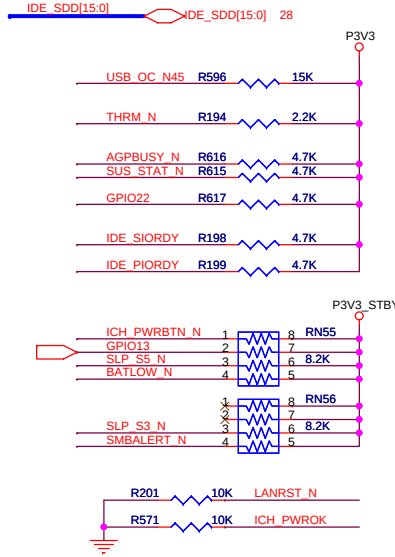




RTC	
1-2	Normal
2-3	Clear CMOS







2007/4/9 Delete U13,U14,R200,C149.

RSMRST_N
R204 100K

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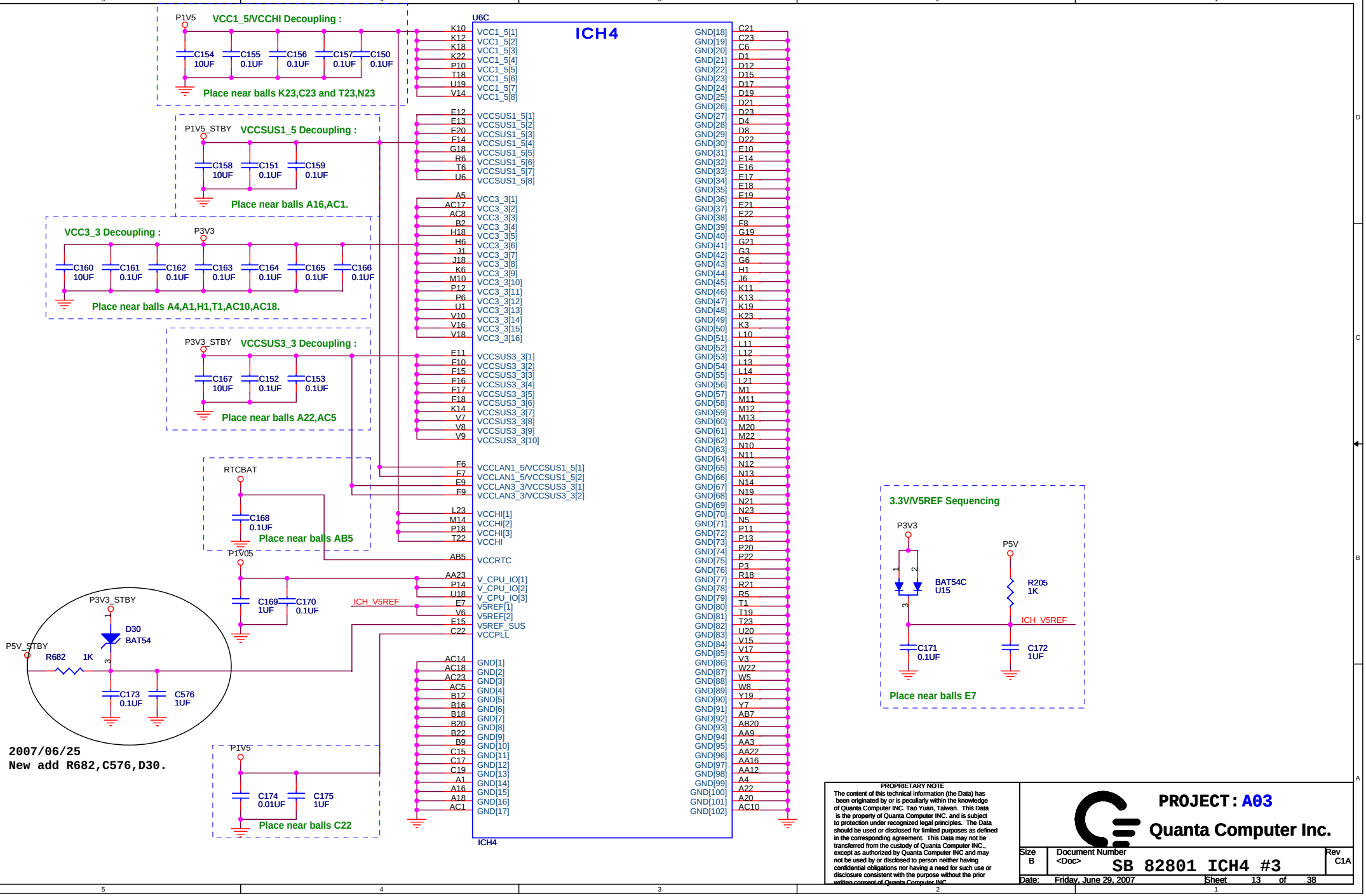
Quanta Computer Inc.

Size	Document Number	Rev
A3	<Doc> SB 82801 ICH4 #2	C1A
Date: Monday, July 02, 2007	Sheet 12 of 38	



PROJECT : A03

Quanta Computer Inc.

Size	Document Number	Rev
B	<Doc> SB 82801 ICH4 #3	C1A

Date: Friday, June 29, 2007 Sheet 13 of 38

Voltage Sensing

CPU FAN

U17 — WPC8763LDG

LPC: LAD0 LAD1 LAD2 LAD3 LRESET# LCLK LFRAME# GA20 SERIRQ SMI#/GPIO64 ECSCI# KBRST#
A/D: AD0/GPI90 AD1/GPI91 AD2/GPI92 AD3/GPI93 GPIO04 GPIO05
D/A: DA0/GPI94 DA1/GPI95 GPI96 GPI97
SPI: GPIO63/PWUREQ# F_SDI F_SD0 F_SCK F_CS0#
PWM: A_PWM0 A_PWM/GPIO21 B_PWM/GPIO13 TA2/GPIO20 CLKOUT/GPIO55 TB1/GPIO14/HGPIO04 GPIO01 GPIO03 GPIO06/HGPIO06
K/B: KBSIN0 KBSIN1 KBSIN2 KBSIN3 KBSIN4 KBSIN5 KBSIN6 KBSIN7 KBSOUT0/JENK# KBSOUT1/TCK KBSOUT2/TMS KBSOUT3/TDI KBSOUT4 KBSOUT5/TDO KBSOUT6/RDY# KBSOUT7 KBSOUT8 KBSOUT9 KBSOUT10 KBSOUT11 KBSOUT12/GPIO64 KBSOUT13/GPIO63 KBSOUT14/GPIO62 KBSOUT15/GPIO61/XOR_OUT KBSOUT16/GPIO60
GPIO: GPIO07/HGPIO07 LPCPD#/GPIO10/HGPIO00 CLKRUN#/GPIO11/HGPIO02 SCL1 SDA1 GPIO16/HGPIO04 GPIO23 GPIO24/HGPIO01 GPIO34 GPIO36 TA1/GPIO56 GPIO42/TCK GPIO43/TMS GPIO40 GPIO44/TDI GPIO45 GPIO46/TRST# GPIO47/JEN0# GPIO51 GPIO50/TDO GPIO52/RDY# GPIO53 KBSOUT17/GPIO57/HGPIO03 SWD/GPIO66 GPIO70 GPIO71 GPIO72 GPIO82/HGPIO00/TRIS# SOUT_CR/GPIO83/BADDR1 GPIO84/HGPIO01/BADDR0 SIN_CR/GPIO87 GPIO77 GPIO76/SHBM GPIO75 GPIO81 GPIO/62SDA2 GPIO61/SCL2 VREF VCC_POR# VCORF RESERVED AVCC AGND
PS/2: PSDAT3/GPIO12 PSCLK3/GPIO25 PSDAT2/GPIO27 PSCLK2/GPIO26 PSDAT1 PSCLK1 PSDAT1 PSCLK1
GPIO33 GPIO32 GPIO31 GPIO30
32KX1/32KCLKIN 32KX2
VCC_1 VCC_2 VCC_3 VCC_4 VCC_5 VDD
GND_1 GND_2 GND_3 GND_4 GND_5 GND_6

Y3 32.768KHz: C182 6.8PF, C183 6.8PF; R222 20M, R224 33K; SIO_32K1, SIO_32K2

P3V3: C186 10UF, C187 0.1UF

P3V3_STBY: C189 10UF, C192 0.1UF, C190 0.1UF, C191 0.1UF, C193 0.1UF

LED4 LED SMD GREEN; R618 330; R619 10K; Q99 FDV301N; EC_HEARTBEAT_N

D25 RB500V; D26 RB500V

TP46 TP45 TP47 TP48 TP49 TP50 TP40 TP51 TP52 TP44 TP53 TP54 TP55

F_SDI R586 33; F_SDO R587 33; F_SCK R589 33; F_CS_N R588 33

JENK_N TCK TMS TDI TDO RDY_N

EC_RESET_N

MBATV_O_EC 33; CCSET 33; WDT_RST_N R659 NI_0; R660 0; R622 10K; ICH_PWROK_EC; WDT_OUT_N 15; U72 NC7SZ08; R210 0; ICH_PWROK 12,37

2007/4/9 New Add 10K ohm R622,R656,R660, R208,R209,R210,R216 change to Insert, PU1 pin-13 connect to U17 pin-101.

FAN_CTL1 FAN_CTL2 FAN_TAC1 FAN_CTL2 25; FAN_TAC2 FAN_TAC2 25; R208 0; R209 0; PWRBTN_N 32; ACIN_OUT_EC 33; RSMRST_N_EC 34; PWR_ON_EC 34; SLP_S3_N 12,34

R216 0; ICH_PWROK_EC; R673 10K; R672 10K; R675 NI_0; R674 NI_0; SMBCLK_STBY 10,12; SMBDAT_STBY 10,12; IMVPWRGD 7,12,37,38

R212 0; R626 0; ICH_PWRBTN_N 12

2007/4/9 New Add R626.

BL_C_N 33; CHG_EC 33; SYS_CGINP_EC 33; COM5_5V_N 17; MAINON_EC 33

COM4_5V_N 17; COM4_12V_N 17; COM5_12V_N 17; JEN0_N; COM3_5V_N 17; COM3_12V_N 17; D_C_N_EC 33

PWR_ON_LED 32; CHG_LED 32; R572 NI_0; LVDS_BKLTEN 7,25; COM6_5V_N 17; R573 NI_0; COM6_12V_N 17; LVDS_VDDEN 7,25; TRIS_N; BADDR1; BADDR0; EC_SIN

R608 NI_0; SHBM; LVDS_BKLTCTL 7,25; BAT_TEMP_EC 33; R226 100; R227 100; BAT_SMDAT_EC 4,33; BAT_SMCLK_EC 4,33

C184 0.1UF; R230 10K; WDT_RST_N; C185 1UF; L7 BLM11B121SB; C188 0.1UF; L59 0

2007/06/25
1.New add R678,R679 8.2K ohm pull up to P3V3_STBY.
2.New add EC_RESET_N net and R676,R677,C573,D29.
3.New add R672,R673,R674,675.

2007/4/9 R228 change to NI, R231 change to Insert.

PWRBTN_N R228 NI_0 ICH_PWRBTN_N
TRIS_N R590 NI_10K
JEN0_N R591 NI_10K
JENK_N R231 10K

JTAG SELECT CONFIGURATION

JEN0(PIN24)	JENK(PIN53)	Functionality of PINs (17,20,21,23,25,27)	Functionality of PINs (47,48,50,51,52)
NC	NC	GPIO	KEYBOARD OUTPUT
10K PD	NC	JTAG Signal	KEYBOARD OUTPUT
NC	10K PD	GPIO	JTAG Signal
10K PD	10K PD	Illegal Strap combination	

P_VCORE R206 10K; P3V3 R207 10K; P3V3_STBY R215 10K
VIN_VCORE VIN_P3V3 VIN_P3V3_SBY
C176 0.1UF, C177 0.1UF, C178 0.1UF; AGND

P12V; R211 4.7K; Q1 SI4435; R217 1K; Q2 2N7002E; R219 33 FAN_CTL1
FAN1 HF2803E-P1; C180 NI_10uF; R220 51K; P5V; C181 0.01UF; R221 1K FAN_TAC1

2007/4/9 Delete R218.

P3V3_STBY: R676 10K; 7,11,23,28,29 PCIRST_N; R677 NI_0; D29 RB500V; EC_RESET_N; C573 1UF

PSDAT1 R678 8.2K; PSCLK1 R679 8.2K

BAT_SMDAT_EC R223 8.2K; BAT_SMCLK_EC R225 8.2K; SHBM R229 10K

0 : Enable Shared BIOS memory *
1 : Disable Shared BIOS memory.

BADDR1 R232 NI_10K; BADDR0 R233 NI_10K

BADDR 1	BADDR 0	SELECTION
0	0	XOR-Tree Test Mode
0	1	Core Defined
1	0	2Eh - 2Fh
1	1	164Eh - 164Fh *

'1' - pin is left open.
'0' - pin is pulled down.

SPI Flash — U16 W25X80: C179 0.1UF; R213 1K; R214 1K; R592 10K; F_CS_N; F_SCK; F_SDO; F_SDI

W25X10/20/40, W25X80-AKE3GFP0N08

2007/4/9 Delete JP3,CN1.

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Quanta Computer Inc.

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A3	SIO WPC8763L	C1A

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(Power On Setting Pin)

U18

F81218DG

P3V3

C199 0.1UF

C201 0.1UF

R623 4.7K

R625 4.7K

R624 4.7K

2007/4/9 New add R623,R624, R625.R661~R668.

IrDA

IR1

HEADER 1X5_2

C212 0.1UF

2007/4/9 Change header

R662 NI_4.7K

R663 NI_4.7K

R664 NI_4.7K

R665 4.7K

R666 4.7K

R667 4.7K

2007/06/25 Delete R661,R668.

R234 TXD_6 4.7K

R234 on: UART 6 addr:0x238 IRQ11/F; off:UART 6 disabled.

R235 TXD_5 4.7K

R235 on: UART 5 addr:0x338 IRQ10/E; off:UART 5 disabled.

R237 TXD_4 4.7K

R237 on: UART 4 addr:0x2e8 IRQ9; off:UART 4 disabled.

R236 TXD_3 4.7K

R236 on: UART 3 addr:0x3e8 IRQ5; off:UART 3 disabled.

R239 DTR_N2 NI_4.7K

R238 TXD_2 4.7K

R238 on : UART 2 addr:0x2f8 irq4; R238on and R2390 off: UART 2 addr:0x2e0 IRQ4; R239 off and R238 off:UART 2 disabled.

R241 DTR_N1 NI_4.7K

R240 TXD_1 4.7K

R240 on : UART 1 addr:0x3f8 irq3; R241 on and R240off: UART 1 addr:0x3e0 IRQ3; R240 off and R241off:UART 1 disabled.

R242 DTR_N4 4.7K

R242 on:LPC interface; Off:ISA intreface

R244 DTR_N3 4.7K

R243 RTS_N2 4.7K

R245 WDT_OUT_N 4.7K

RTS_N2	RTS_N3	RTS_N1	Address	Entry Key
0	0	0	0x4e/0x4f	0x77
0	0	1	0x2e/0x2f	0x77
0	1	0	0x4e/0x4f	0xa0
0	1	1	0x2e/0x2f	0xa0
1	0	0	0x4e/0x4f	0x87
1	0	1	0x2e/0x2f	0x87
1	1	0	0x4e/0x4f	0x67
1	1	1	0x2e/0x2f	0x67

U19

U20

U21

U22

ADM213EARSZ

C194 0.1UF

C195 0.1UF

C196 0.1UF

C197 0.1UF

C198 0.1UF

C200 0.1UF

C202 0.1UF

C203 0.1UF

C204 0.1UF

C205 0.1UF

C206 0.1UF

C208 0.1UF

C209 0.1UF

C210 0.1UF

C214 0.1UF

C207 0.1UF

C213 0.1UF

C215 0.1UF

C216 0.1UF

C211 0.1UF

COM3

COM4

COM5

COM6

HEADER 2X5_9

CP1 220PF

CP2 220PF

CP3 220PF

CP4 220PF

R246 10K

R247 10K

R248 10K

R251 10K

R255 10K

R256 10K

R258 10K

R259 10K

R249 4.7K

R250 4.7K

R254 4.7K

R257 4.7K

R252 4.7K

R253 4.7K

R260 4.7K

R261 4.7K

Q3 AO3404

Q4A MBT3904

Q4B MBT3904

Q5A MBT3904

Q5B MBT3904

Q6 AO3404

Q7A MBT3904

Q7B MBT3904

Q8 AO3404

Q9A MBT3904

Q9B MBT3904

Q10 AO3404

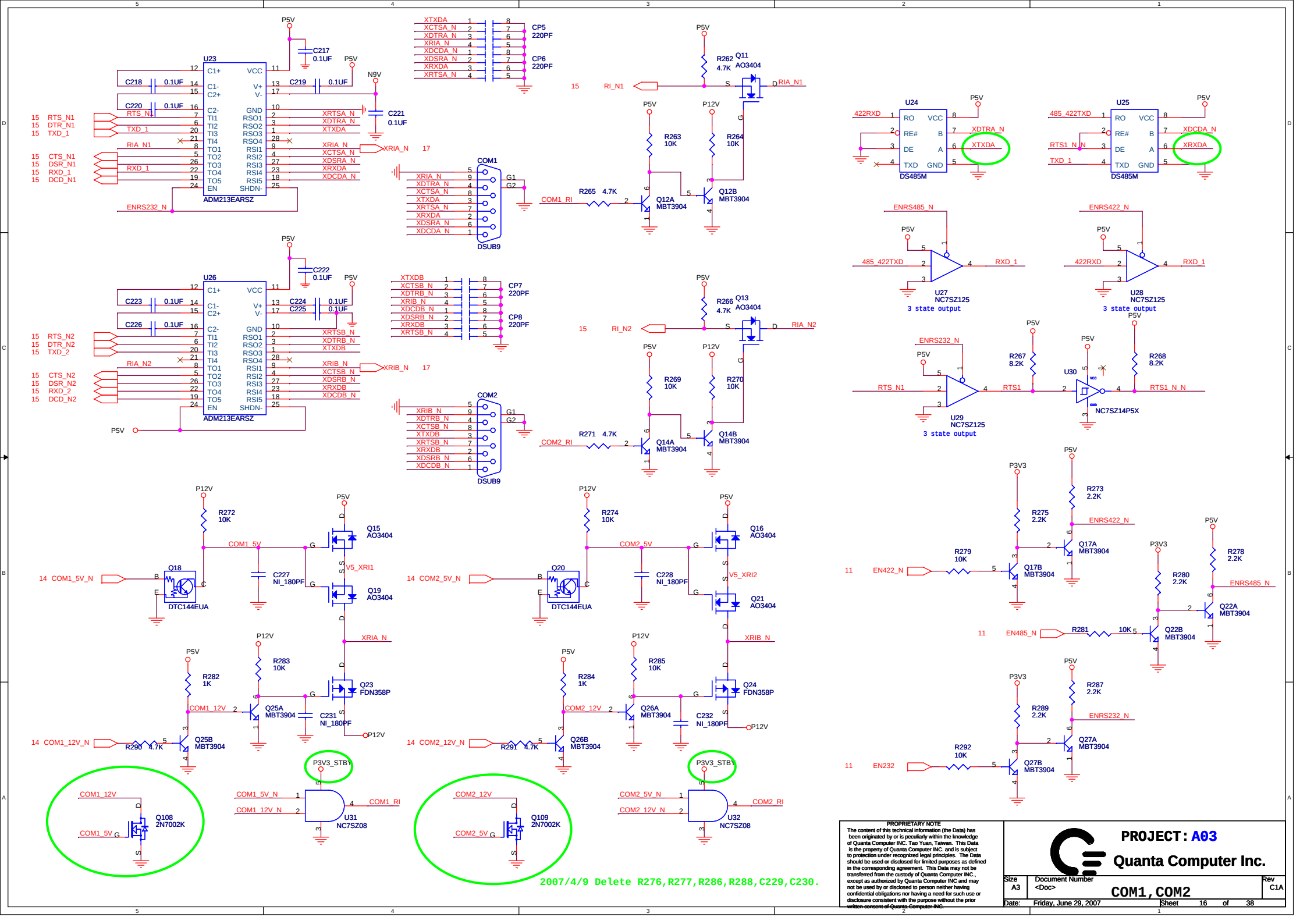
CON1X15-R

CON1X8

PROJECT: A01

Quanta Computer Inc.

Size	Document Number	Rev
A3	<Doc> SIO F81218D, COM3/4/5/6	C1A
Date: Friday, June 29, 2007	Sheet 15 of 38	


U23
ADM213EARSZ
C217 0.1UF
C218 0.1UF
C219 0.1UF
C220 0.1UF
C221 0.1UF
P5V
N9V
RTS_N1
DTR_N1
TXD_1
RIA_N1
CTS_N1
DSR_N1
RXD_1
DCD_N1
ENRS232_N
XRTSA_N
XDTRA_N
XTXDA
XRIA_N
XCTSA_N
XDSRA_N
XRXDA
XDCDA_N
XRIA_N 17
CP5 220PF
CP6 220PF
COM1
DSUB9
R262 4.7K
Q11 AO3404
RI_N1
R263 10K
R264 10K
R265 4.7K
COM1_RI
Q12A MBT3904
Q12B MBT3904
U24
U25
422RXD
485_422TXD
RXD_1
RTS1_N_N
DS485M
U26
ADM213EARSZ
C222 0.1UF
C223 0.1UF
C224 0.1UF
C225 0.1UF
C226 0.1UF
RTS_N2
DTR_N2
TXD_2
RIA_N2
CTS_N2
DSR_N2
RXD_2
DCD_N2
XRTSB_N
XDTRB_N
XTXDB
XRIB_N
XCTSB_N
XDSRB_N
XRXDB
XDCDB_N
XRIB_N 17
CP7 220PF
CP8 220PF
R266 4.7K
Q13 AO3404
RI_N2
R269 10K
R270 10K
R271 4.7K
COM2_RI
Q14A MBT3904
Q14B MBT3904
ENRS485_N
ENRS422_N
U27 NC7SZ125
U28 NC7SZ125
3 state output
U29 NC7SZ125
U30 NC7SZ14P5X
R267 8.2K
R268 8.2K
RTS1
RTS1_N_N
R272 10K
Q15 AO3404
COM1_5V
Q18
DTC144EUA
C227 NI_180PF
Q19 AO3404
V5_XRI1
XRIA_N
R282 1K
R283 10K
Q23 FDN358P
COM1_12V
Q25A MBT3904
Q25B MBT3904
C231 NI_180PF
R290 4.7K
P12V
P3V3_STB
Q108 2N7002K
U31 NC7SZ08
COM1_5V_N
COM1_12V_N
R274 10K
Q16 AO3404
COM2_5V
Q20
C228 NI_180PF
Q21 AO3404
V5_XRI2
XRIB_N
R284 1K
R285 10K
Q24 FDN358P
COM2_12V
Q26A MBT3904
Q26B MBT3904
C232 NI_180PF
R291 4.7K
Q109 2N7002K
U32 NC7SZ08
COM2_5V_N
COM2_12V_N
R273 2.2K
R275 2.2K
Q17A MBT3904
Q17B MBT3904
R279 10K
EN422_N
R278 2.2K
R280 2.2K
Q22A MBT3904
Q22B MBT3904
R281 10K
EN485_N
R287 2.2K
R289 2.2K
Q27A MBT3904
Q27B MBT3904
R292 10K
EN232
2007/4/9 Delete R276,R277,R286,R288,C229,C230.
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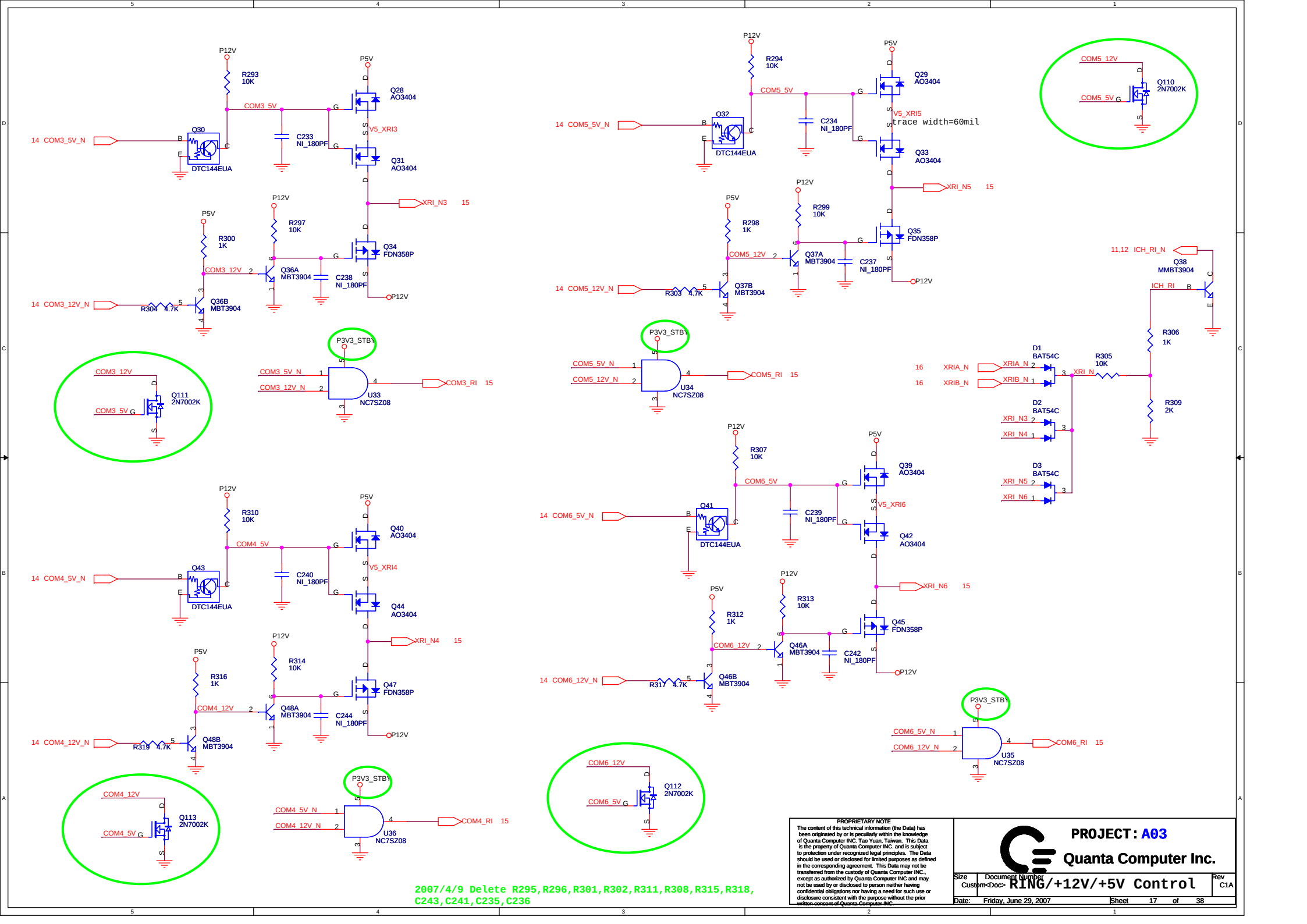
PROJECT: A03
Quanta Computer Inc.
Size A3
Document Number <Doc>
COM1,COM2
Rev C1A
Date: Friday, June 29, 2007
Sheet 16 of 38


P12V
R293 10K
P5V
Q28 AO3404
COM3_5V
14 COM3_5V_N
Q30
DTC144EUA
C233 NI_180PF
V5_XRI3
Q31 AO3404
XRI_N3 15
R297 10K
R300 1K
COM3_12V
Q36A MBT3904
C238 NI_180PF
Q34 FDN358P
14 COM3_12V_N
R304 4.7K
Q36B MBT3904
P3V3_STBY
COM3_5V_N
COM3_12V_N
U33 NC7SZ08
COM3_RI 15
COM3_12V
COM3_5V
Q111 2N7002K
R294 10K
Q29 AO3404
COM5_5V
14 COM5_5V_N
Q32
DTC144EUA
C234 NI_180PF
V5_XRI5
trace width=60mil
Q33 AO3404
XRI_N5 15
R298 1K
R299 10K
COM5_12V
Q37A MBT3904
C237 NI_180PF
Q35 FDN358P
14 COM5_12V_N
R303 4.7K
Q37B MBT3904
COM5_5V_N
COM5_12V_N
U34 NC7SZ08
COM5_RI 15
COM5_12V
COM5_5V
Q110 2N7002K
11,12 ICH_RI_N
Q38 MMBT3904
ICH_RI
R306 1K
R309 2K
D1 BAT54C
D2 BAT54C
D3 BAT54C
R305 10K
16 XRIA_N
16 XRIB_N
XRI_N3
XRI_N4
XRI_N5
XRI_N6
R310 10K
COM4_5V
14 COM4_5V_N
Q43
DTC144EUA
C240 NI_180PF
V5_XRI4
Q44 AO3404
XRI_N4 15
R314 10K
R316 1K
COM4_12V
Q48A MBT3904
C244 NI_180PF
Q47 FDN358P
14 COM4_12V_N
R319 4.7K
Q48B MBT3904
COM4_5V_N
COM4_12V_N
U36 NC7SZ08
COM4_RI 15
COM4_12V
COM4_5V
Q113 2N7002K
R307 10K
COM6_5V
14 COM6_5V_N
Q41
DTC144EUA
C239 NI_180PF
V5_XRI6
Q39 AO3404
Q42 AO3404
XRI_N6 15
R312 1K
R313 10K
COM6_12V
Q46A MBT3904
C242 NI_180PF
Q45 FDN358P
14 COM6_12V_N
R317 4.7K
Q46B MBT3904
COM6_5V_N
COM6_12V_N
U35 NC7SZ08
COM6_RI 15
COM6_12V
COM6_5V
Q112 2N7002K
2007/4/9 Delete R295,R296,R301,R302,R311,R308,R315,R318,
C243,C241,C235,C236
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PROJECT: A03
Quanta Computer Inc.
Size Custom<Doc>
Document Number RING/+12V/+5V Control
Rev C1A
Date: Friday, June 29, 2007
Sheet 17 of 38

PREQ=2
PGNT=2
ID=AD20
INT=PIRQ#D

RTL8110SBL	
AVDDH	+3.3V
V_12P	+3.3V
AVDDL	+2.5V
V_DAC	+2.5V
DVDD	+1.2V
DVDD_A	+1.2V

2007/4/9 R328 change to NI.

2007/04/10 RTL8110SCL change to RTL8110SBL, New add R658.

Active LED

10/100M use P/N:DFHS17FR129
1000M use P/N:DFHS17FR056

RTL8110SCL-GR

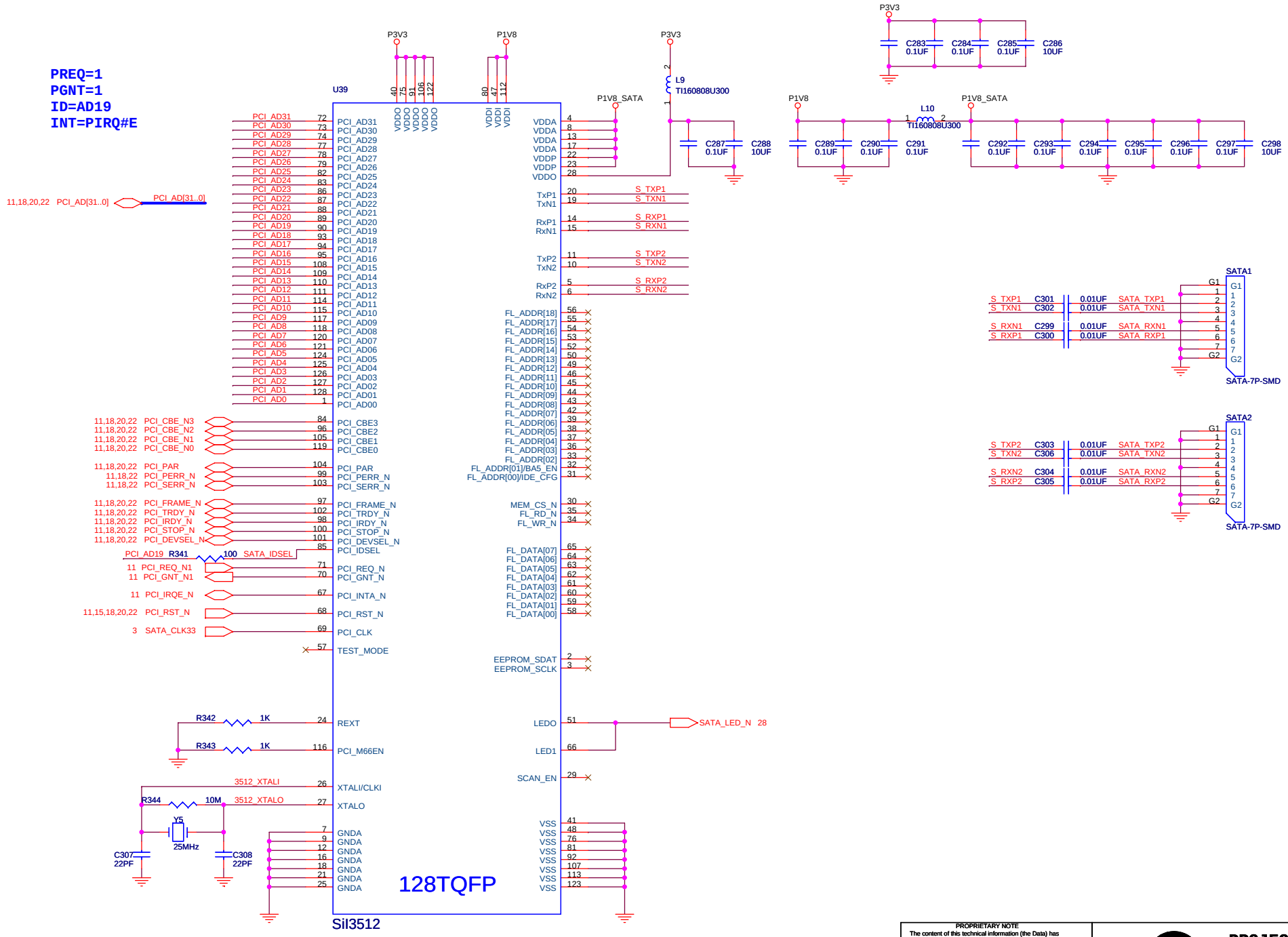
For RTL8110SC AVDDH pins, such as 10 and 120.

For RTL8110S(B)/8100C pin12.

For RTL8110SC AVDDL pins, such as 3,7,16 and 20.

For RTL8110SC/8100C DVDD pins, such as 24,32,45,54,64,78,99,110 and 116.

PROJECT: A03
Quanta Computer Inc.
Size: Custom<Doc> | Document Number: LAN RTL8110SC | Rev: C1A
Date: Friday, June 29, 2007 | Sheet 18 of 38



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PROJECT: A03

Quanta Computer Inc.

Size	Document Number	Rev
A3	<Doc> SATA SiI3512	C1A
Date: Friday, June 29, 2007	Sheet 19 of 38	

ID=AD21
INT=PIRQ#F

Close to Z7

Z7 POWER BUDGET:
1.8V~470mA
2.5V~90mA+460mA(64MB)
3.3V~160mA

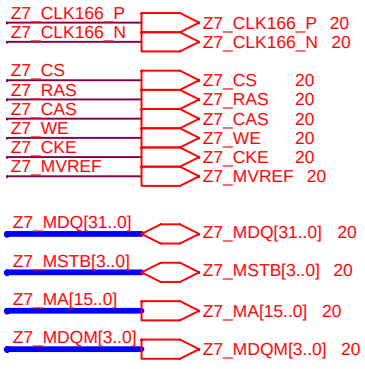
1.8V~800mA

2.5V~800mA

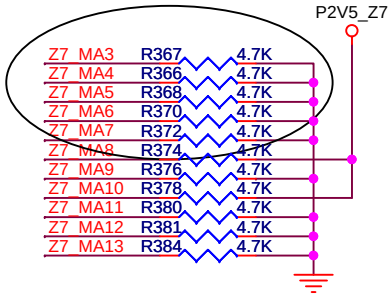
2007/06/25
1.New add SPI EEPRM U78,R680,C574,C575.
2.New add U77,R681.

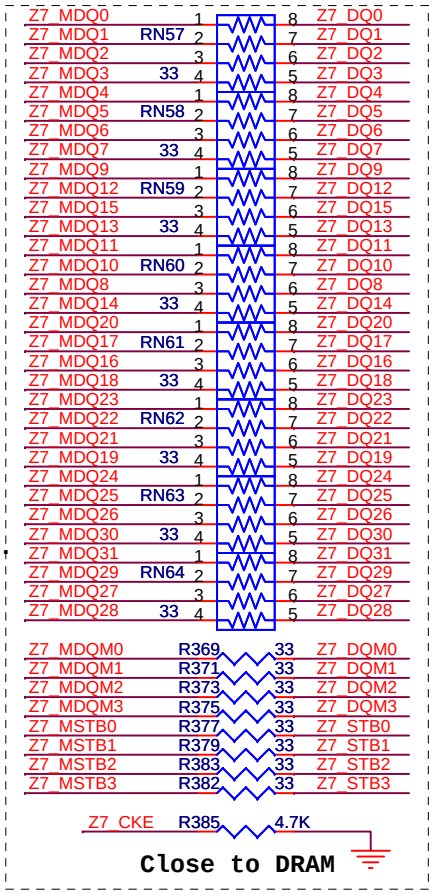
PROJECT: A03
Quanta Computer Inc.

Size	Document Number	Rev
A3	<Doc> XGI Z7	C1A
Date: Friday, June 29, 2007	Sheet 20 of 38	

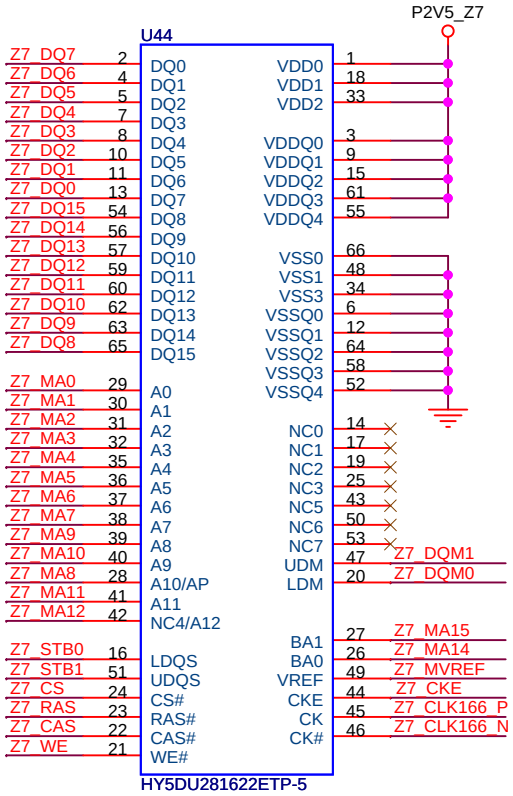


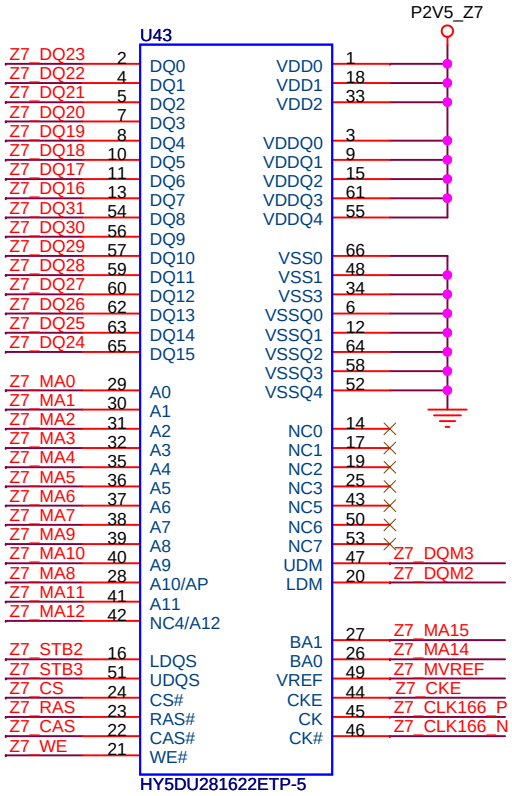
2007/06/25
R367,R370 change to pull down.

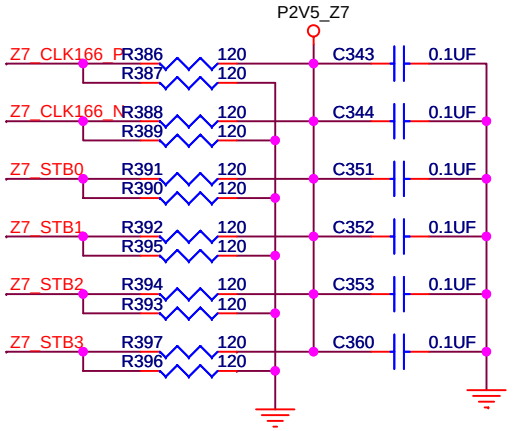


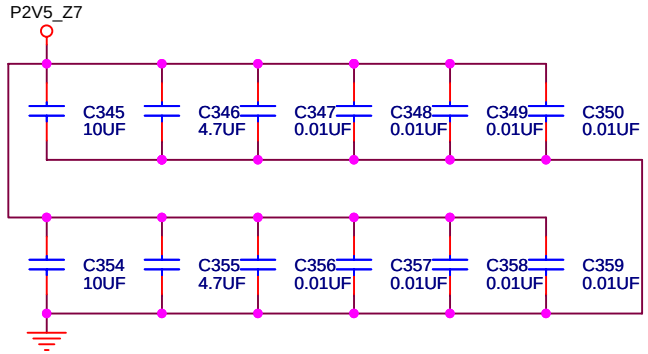


16M*16bit:AKD3JG-KW08
8M*16bit:AKD3DG-KW02









Pin Name	Value	Description	Default
MAA 3	0 1	Enable SPI Disable SPI	0
MAA4	0 1	32KB ROM decoding 64KB ROM decoding	0
MAA5	0 1	Disable PCI AD Bus Reverse Enable PCI AD Bus Reverse	0
MAA6	0 1	Sub-system ID auto-fetch Sub-system ID programmable	0
MAA7	0 1	D2 state Enable D2 state Disable	0
MAA8	0 1	Local Frame Buffer Size -- MAA[10:8] 0 0 0: 2MB 1 0 1: 64MB	0
MAA9	0 1	0 0 1: 4MB 1 1 0: 128MB 0 1 0: 8MB 1 1 1: 256MB	0
MAA10	0 1	0 1 1: 16MB 1 0 0: 32MB	1
MAA11	0 1	PCI I/O interface driving control 0: Weak 1: Strong	0
MAA12	0 1	Select internal clock generator Select external clock generator	0
MAA13	0 1	BCLK DLL Enable BCLK DLL Disable	0

Note: 1. If the serial ROM is not used (integrated system BIOS), then MAA3 and MAA6 both need to be high.

2. The hardware trapping signal needs to be set high or low, depending on the system configuration. These pins cannot be left floating or open.

PROJECT : A03

Quanta Computer Inc.

Size	Document Number	Rev
A4	<Doc> XGI Z7 DDR SDRAM	C1A

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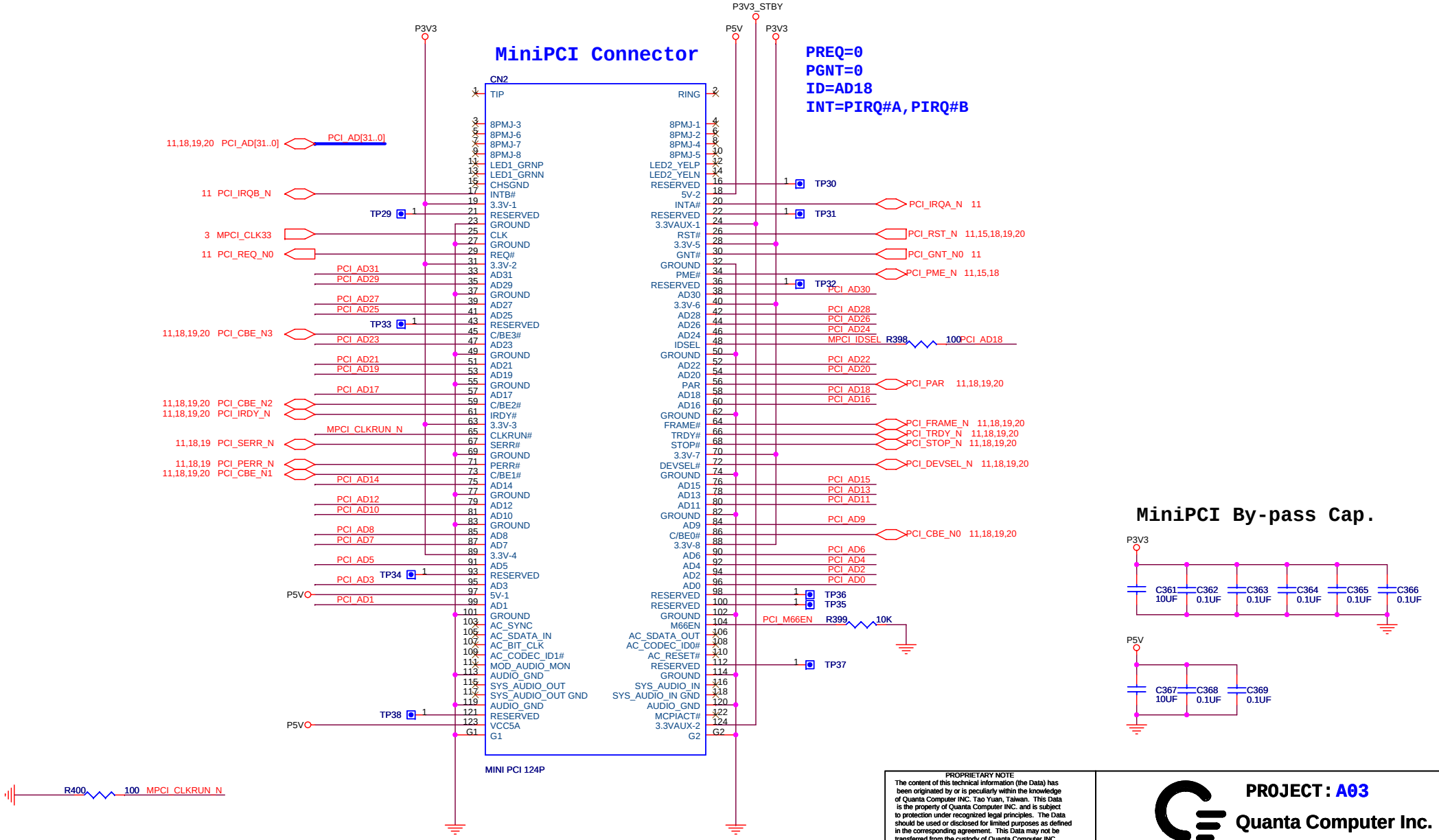
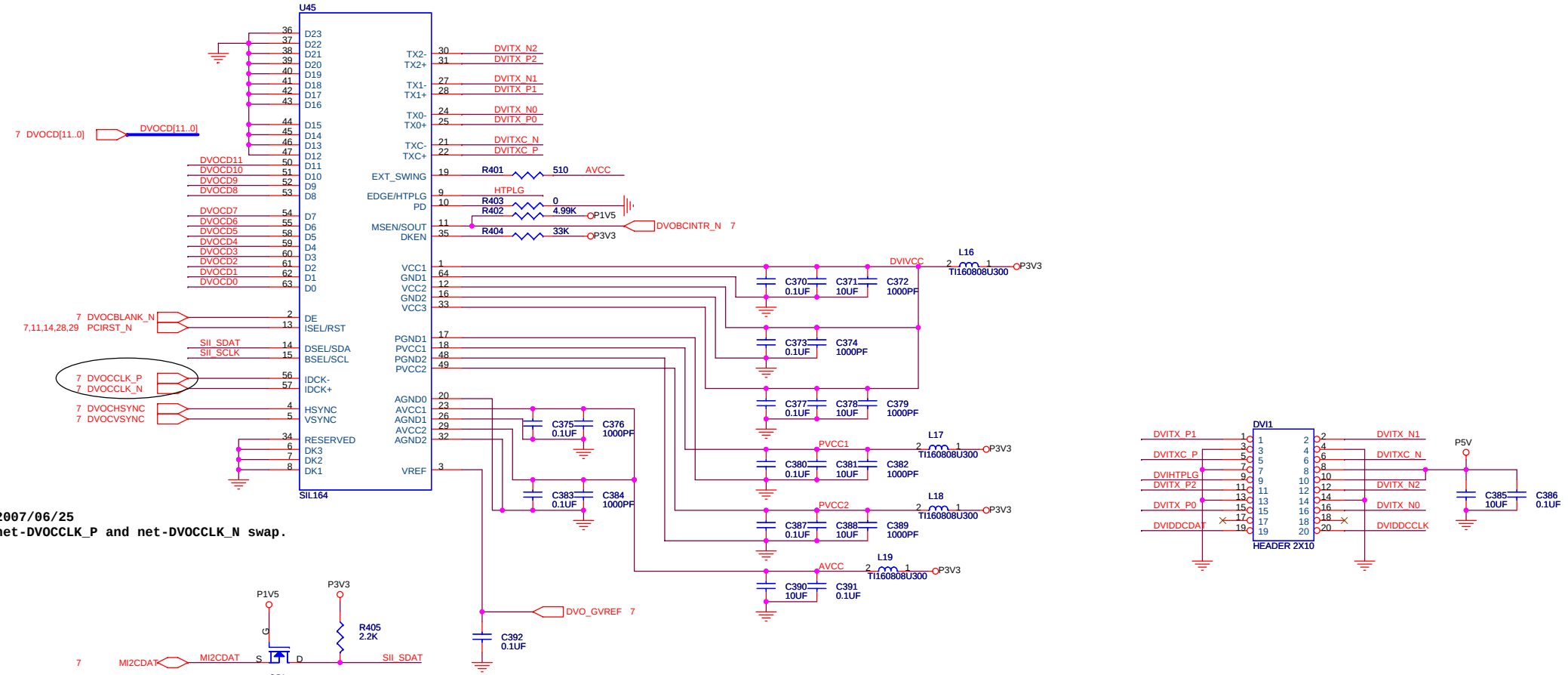


PROJECT: A03

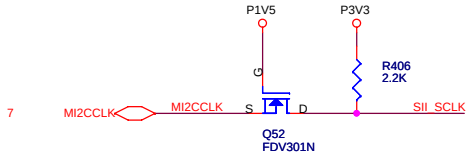
Quanta Computer Inc.

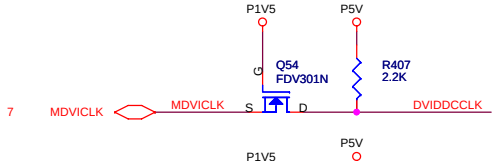
Size	Document Number	Rev
B	<Doc> MINIPCI_SLOT	C1A

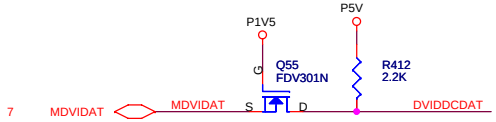
Date: Friday, June 29, 2007 Sheet 22 of 38

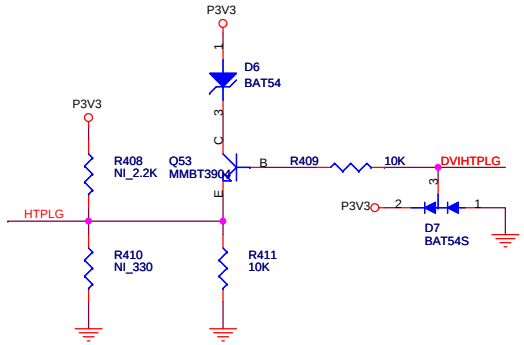


2007/06/25
net-DVOCCLK_P and net-DVOCCLK_N swap.





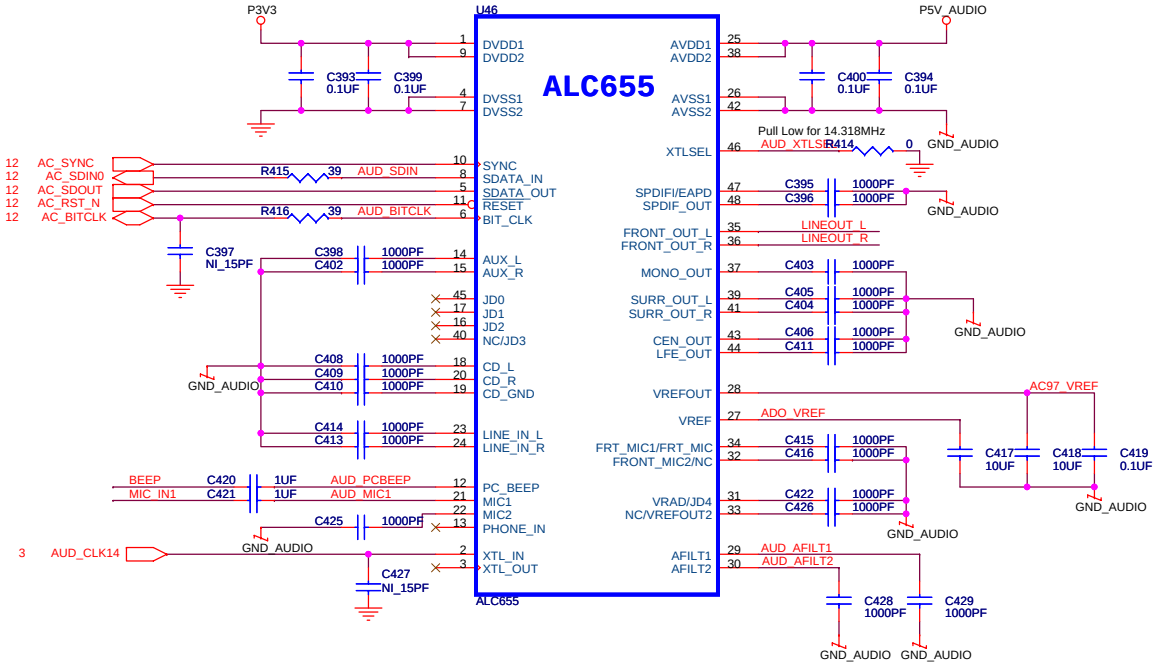




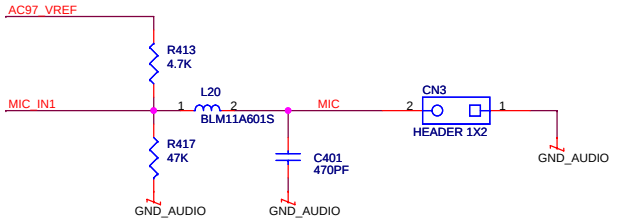
PROJECT: A03
Quanta Computer Inc.

Size	Document Number	Rev
A3	<Doc> DVI SiI164	C1A
Date: Friday, June 29, 2007	Sheet 23 of 38	

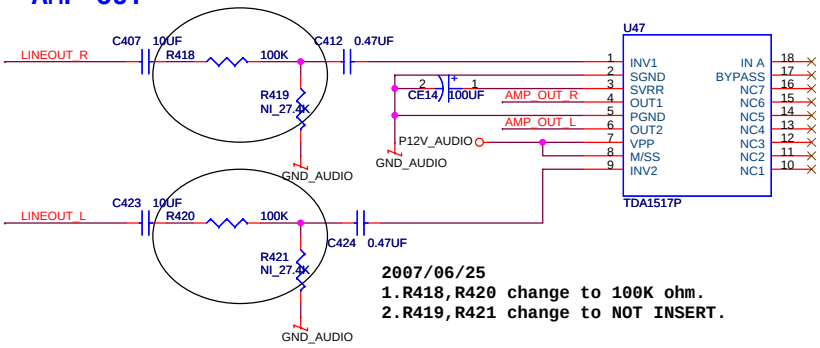
AC'97 CODEC



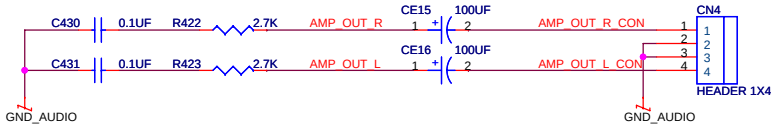
MIC IN



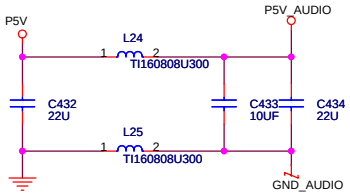
AMP OUT

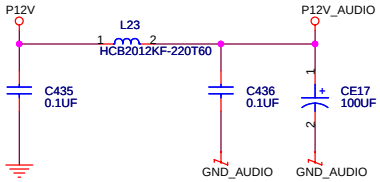


2007/06/25
1.R418,R420 change to 100K ohm.
2.R419,R421 change to NOT INSERT.

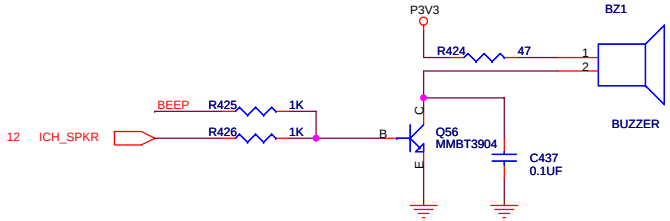


ANALOG POWER



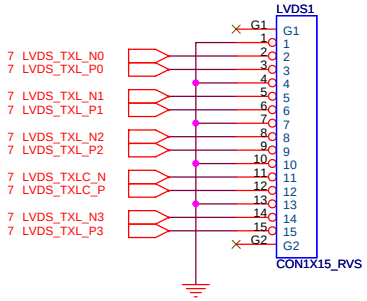


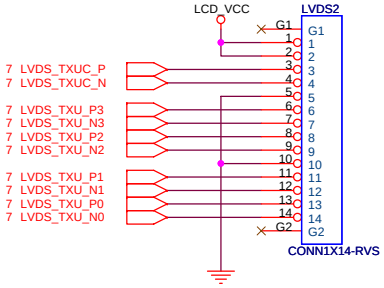
BUZZER



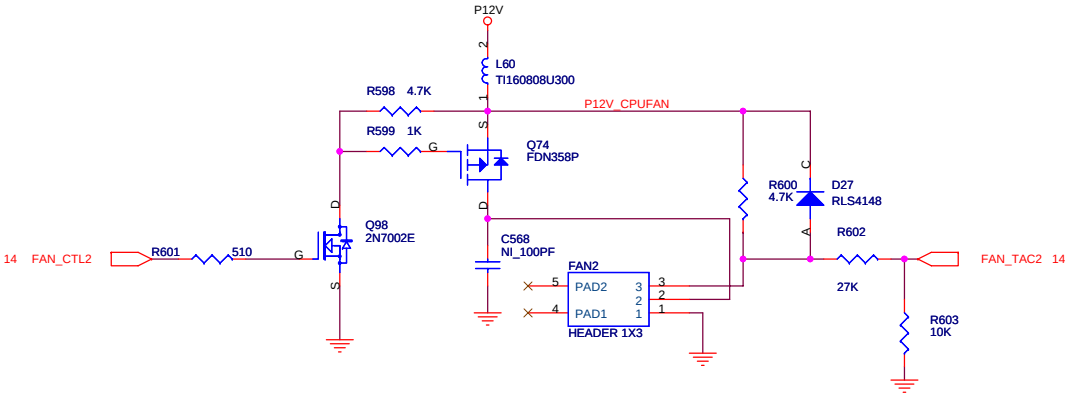
PROJECT : A03
Quanta Computer Inc.

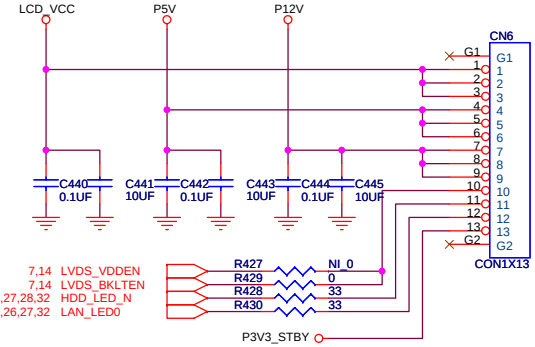
Size	Document Number	Rev
A3	<Doc> ALC655	C1A
Date: Friday, June 29, 2007	Sheet 24 of 38	

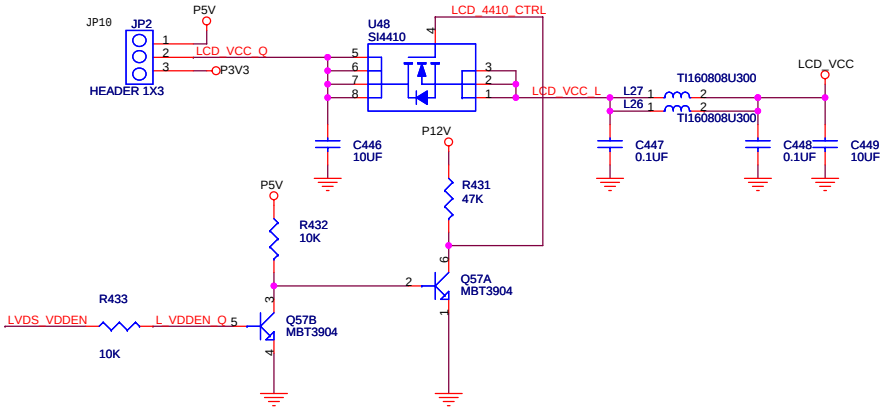


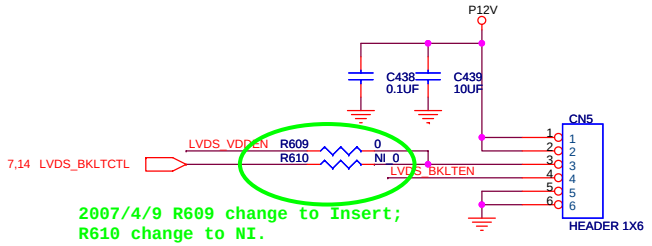


CPU FAN-2







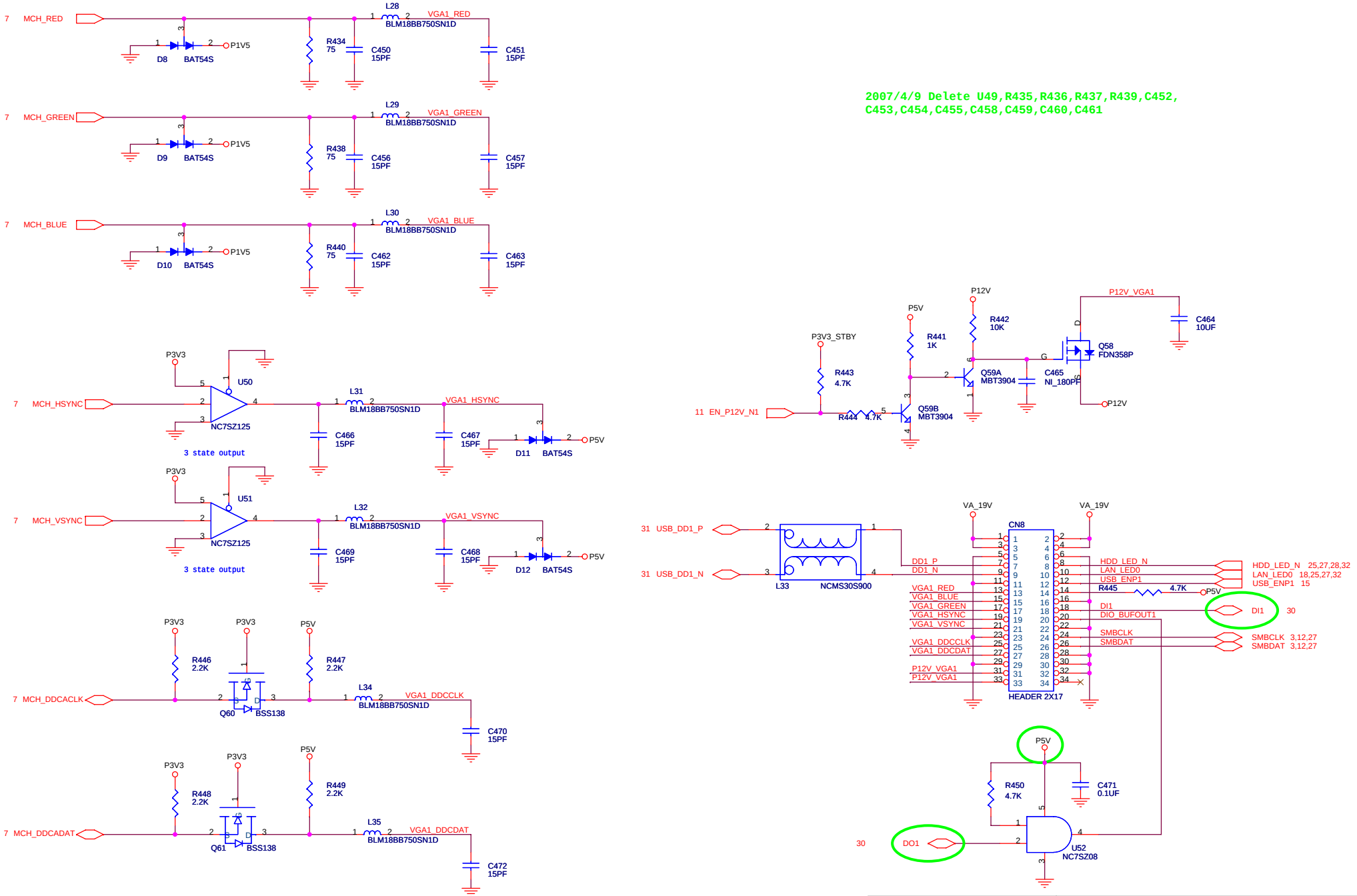


2007/4/9 R609 change to Insert;
R610 change to NI.

PROJECT: A03

Quanta Computer Inc.

Size	Document Number	Rev
A3	<Doc> LVDS	C1A
Date: Friday, June 29, 2007	Sheet 25 of 38	



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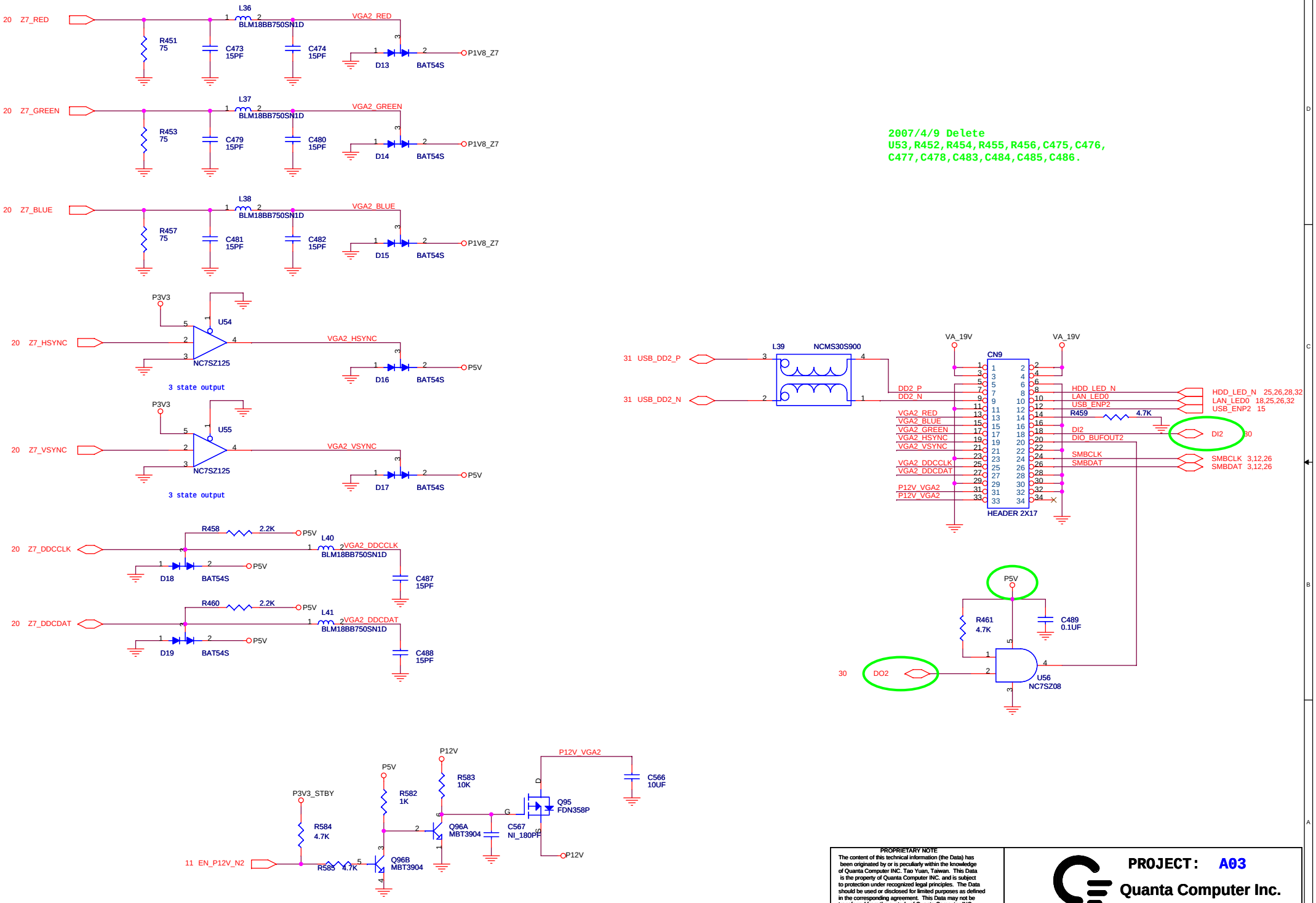
PROJECT: A03

Quanta Computer Inc.

Size	Document Number	Rev
A3	<Doc> VGA1 From NB	C1A
Date: Friday, June 29, 2007	Sheet 26 of 38	

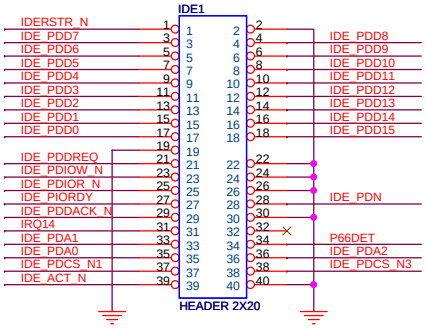


PROJECT: A03

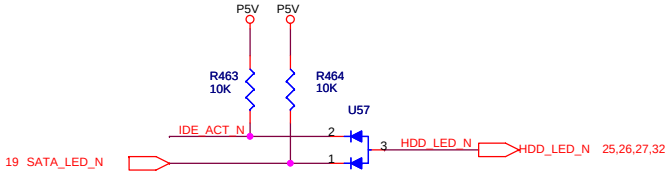
Quanta Computer Inc.

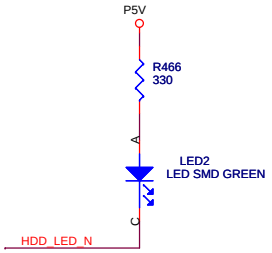
Size	Document Number	Rev
A3	<Doc> VGA1 From Z7	C1A
Date: Friday, June 29, 2007	Sheet 27 of 38	

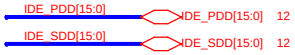
IDE1



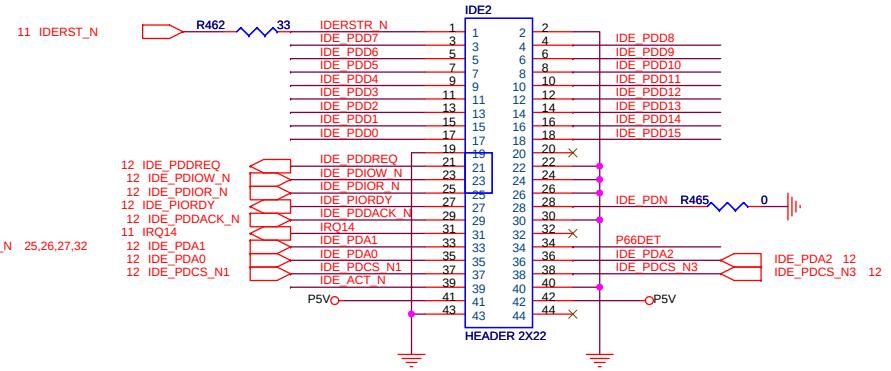
IDE Activity LED

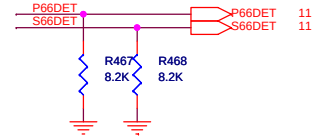




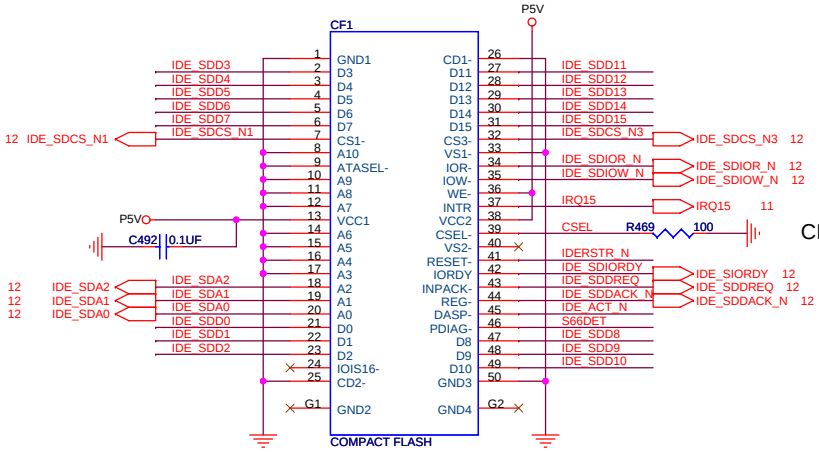


IDE2



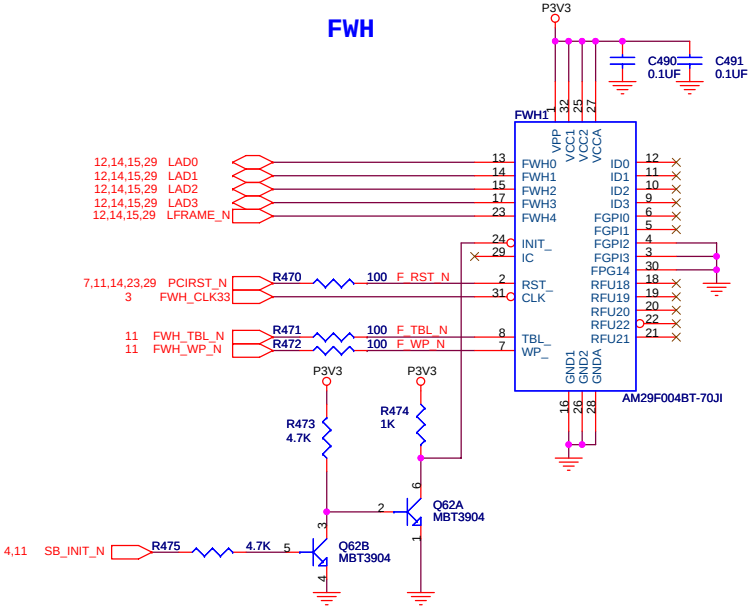


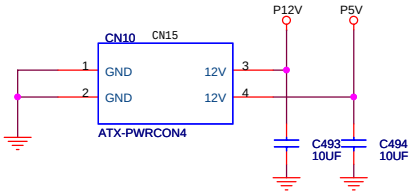
Compact Flash



CFMS : MASTER

FWH





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A3	<Doc> IDE, CF, FWH	C1A
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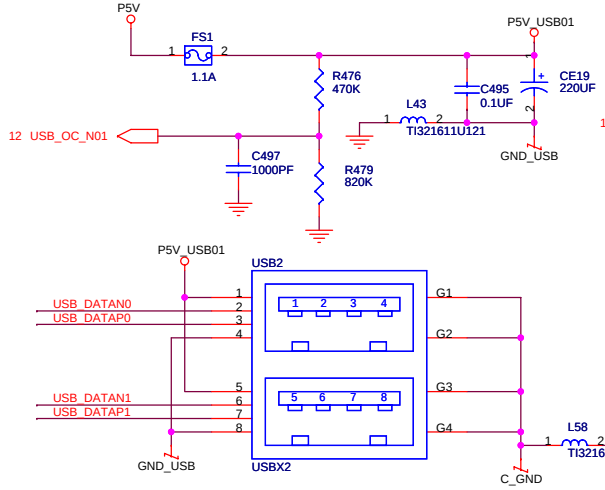
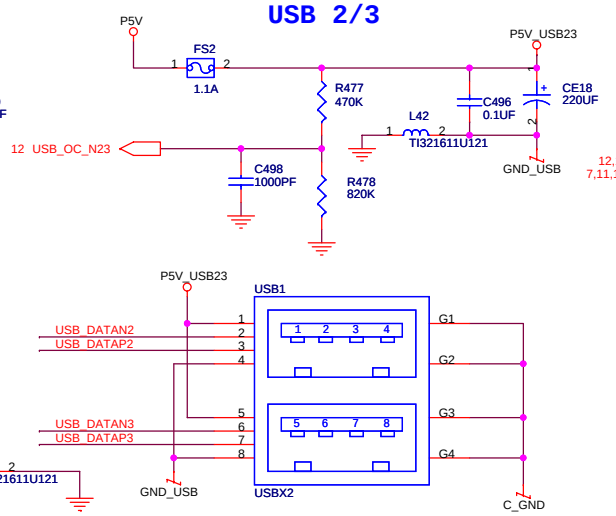
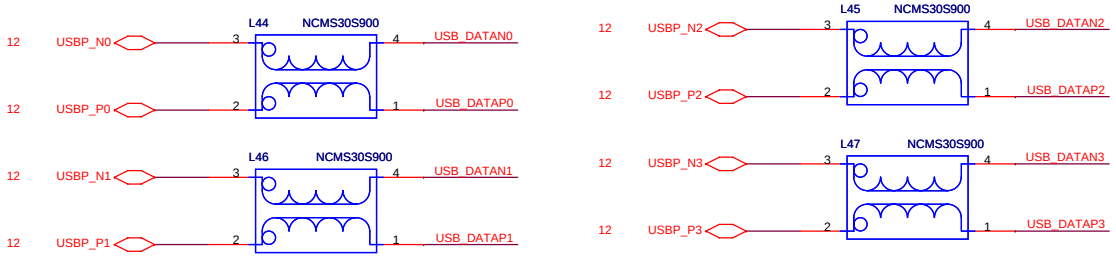
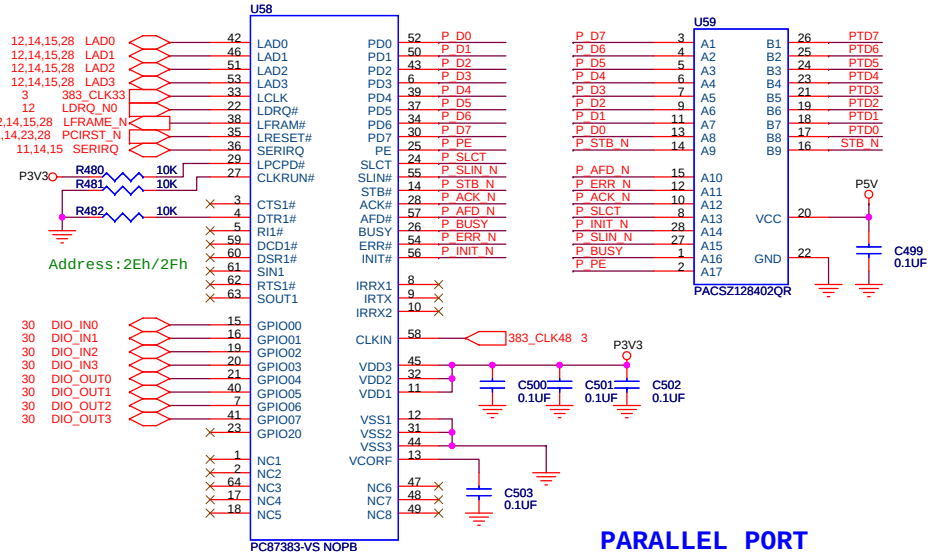
USB 0/1



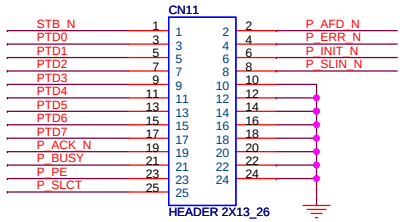
USB 2/3



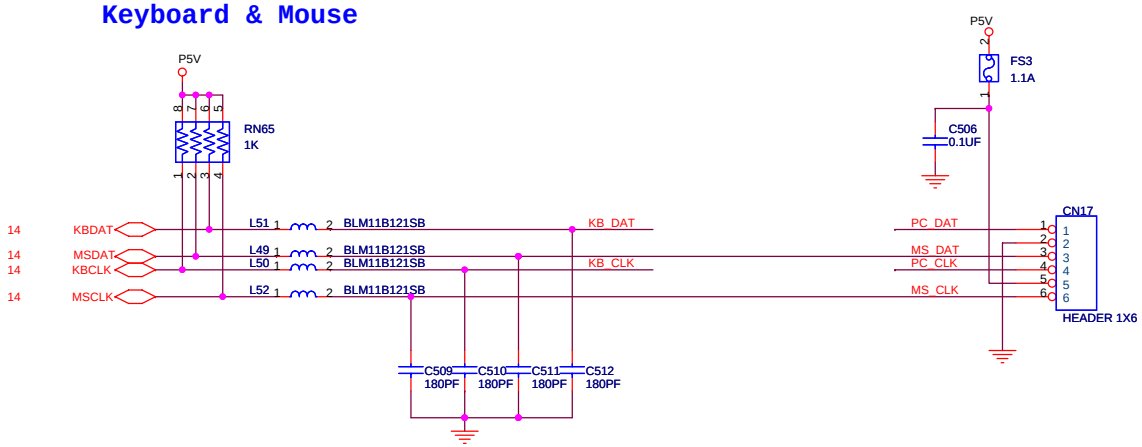


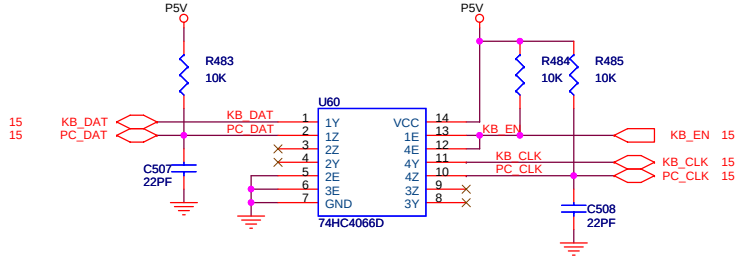


PARALLEL PORT



Keyboard & Mouse





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A3	<Doc> USB, KB/MS, PARALLEL	C1A
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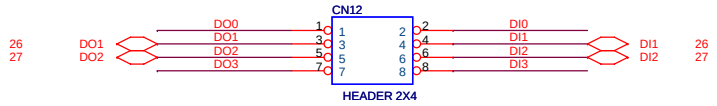
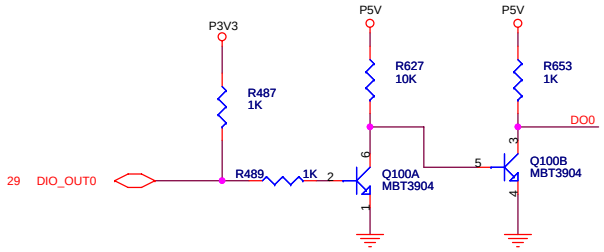
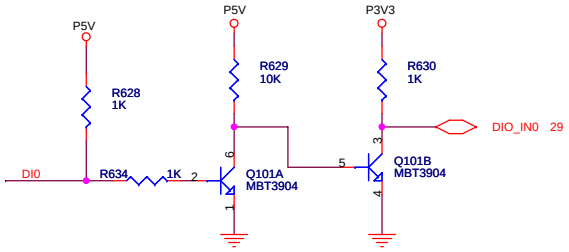
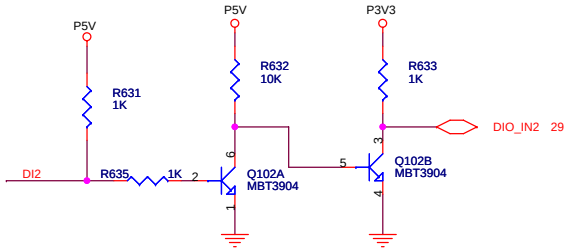
Digital IO: 4 IN / 4 OUT

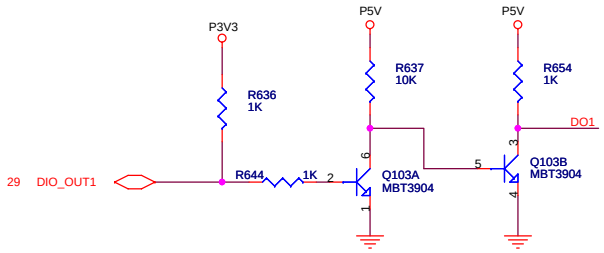


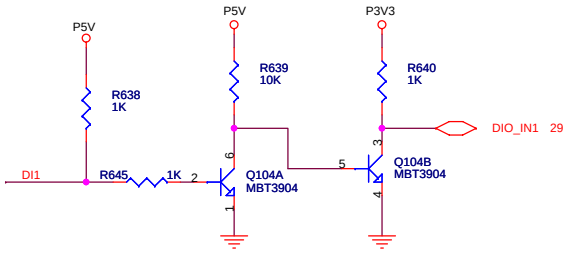
2007/4/9 Delete RN66,RN67,
New Add GPIO Level shift circuitry.

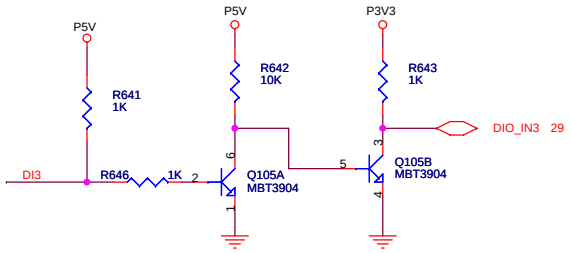


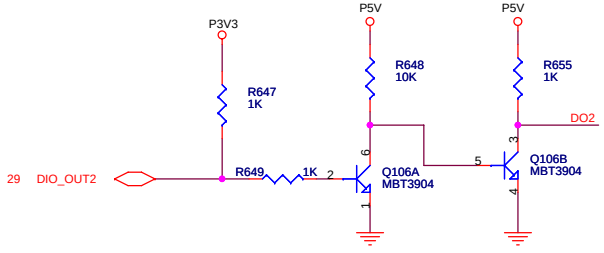


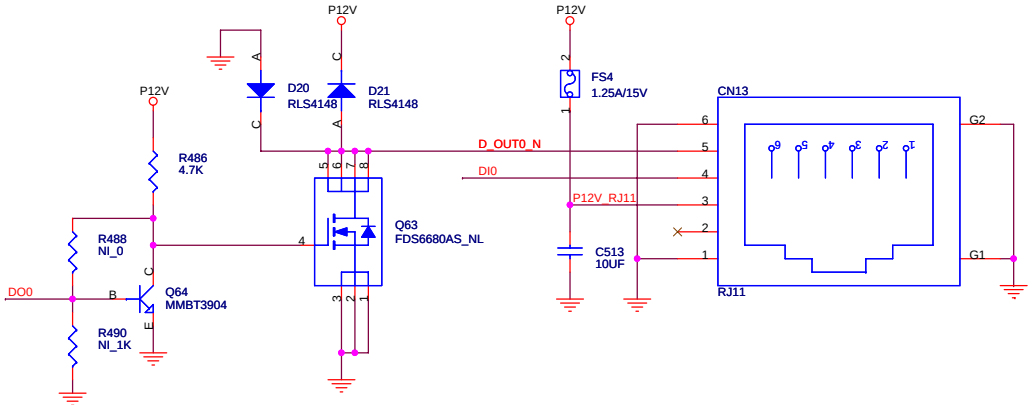


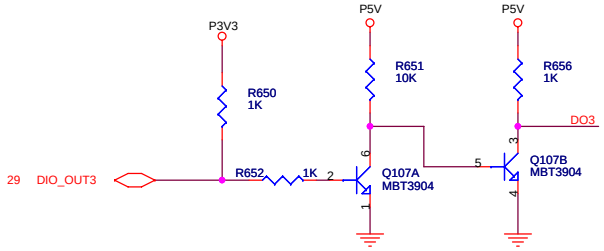












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A3	<Doc> RJ-11, DIO	C1A
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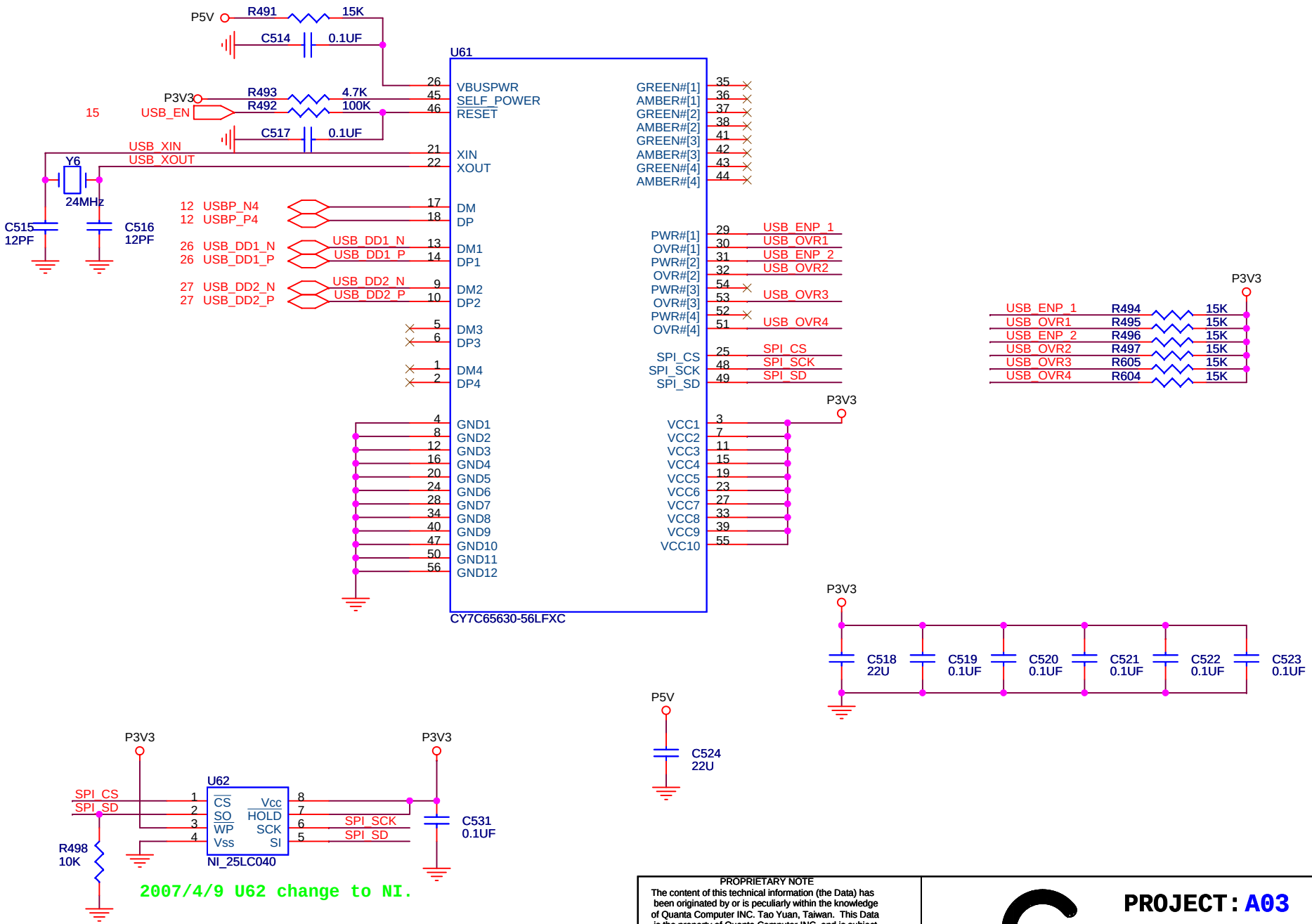

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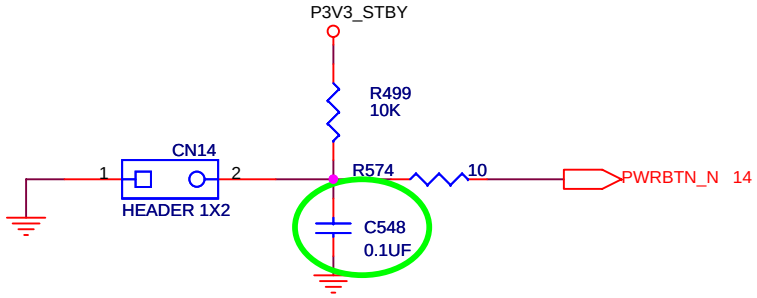
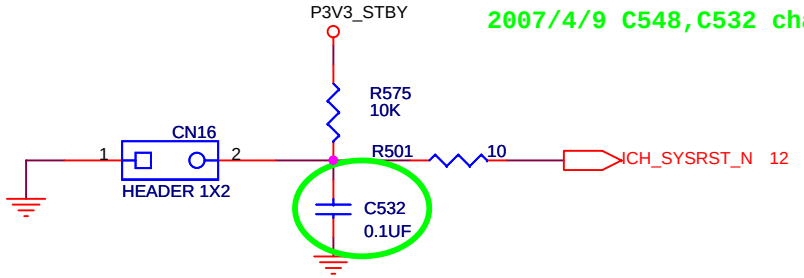
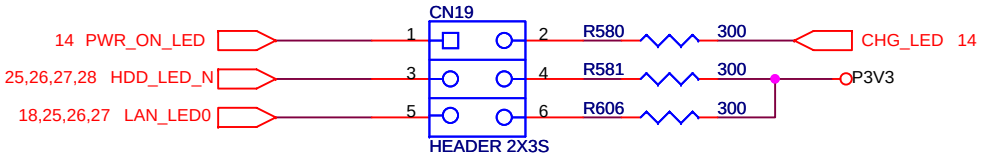
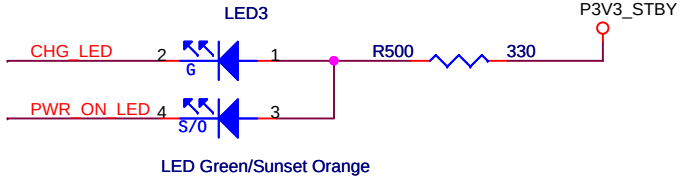
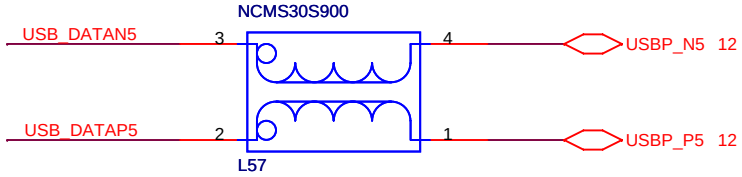


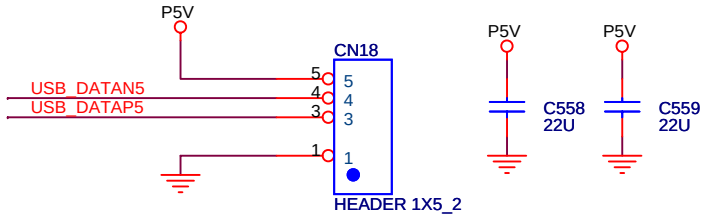


2007/4/9 C548,C532 change to 0.1uF.



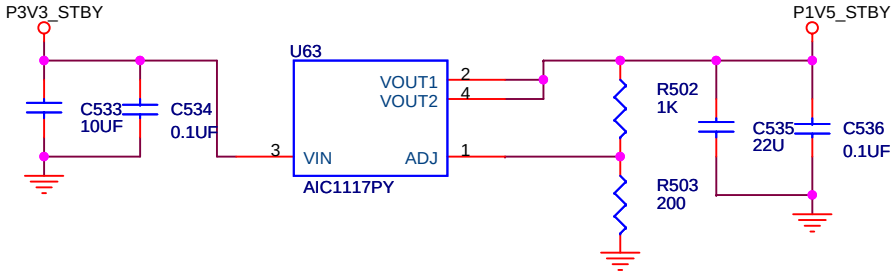






2007/4/9 Delete U75,R577,R578,C549,C550,C557.

+1.5V~800mA



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Power Buttom

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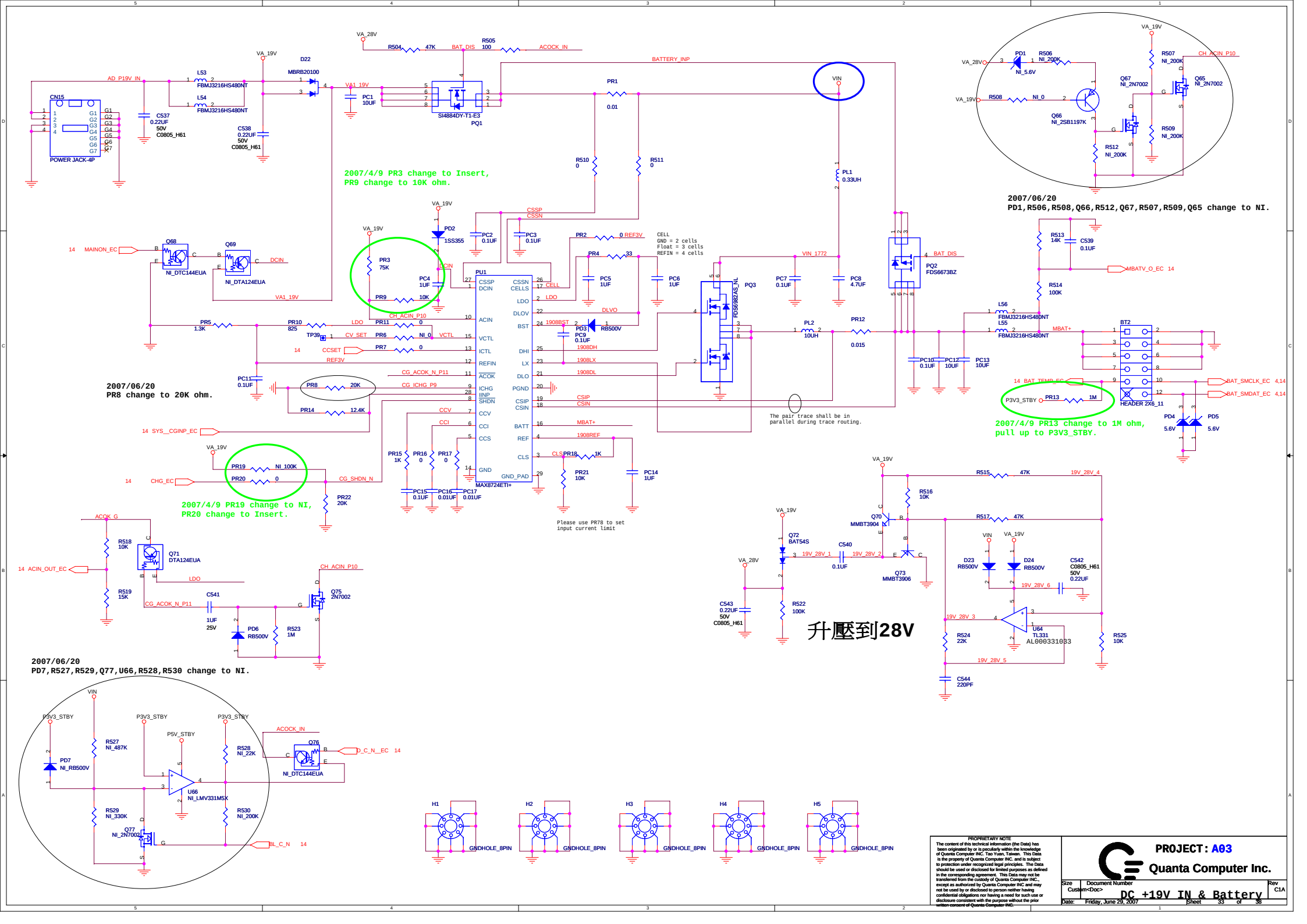
2007/4/9 PR3 change to Insert,
PR9 change to 10K ohm.
2007/06/20
PR8 change to 20K ohm.
2007/4/9 PR19 change to NI,
PR20 change to Insert.
2007/06/20
PD7,R527,R529,Q77,U66,R528,R530 change to NI.
2007/06/20
PD1,R506,R508,Q66,R512,Q67,R507,R509,Q65 change to NI.
2007/4/9 PR13 change to 1M ohm,
pull up to P3V3_STBY.
升壓到28V
The pair trace shall be in
parallel during trace routing.
Please use PR78 to set
input current limit
CELL
GND = 2 cells
Float = 3 cells
REFIN = 4 cells
PROPRIETARY NOTE
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DC +19V IN & Battery
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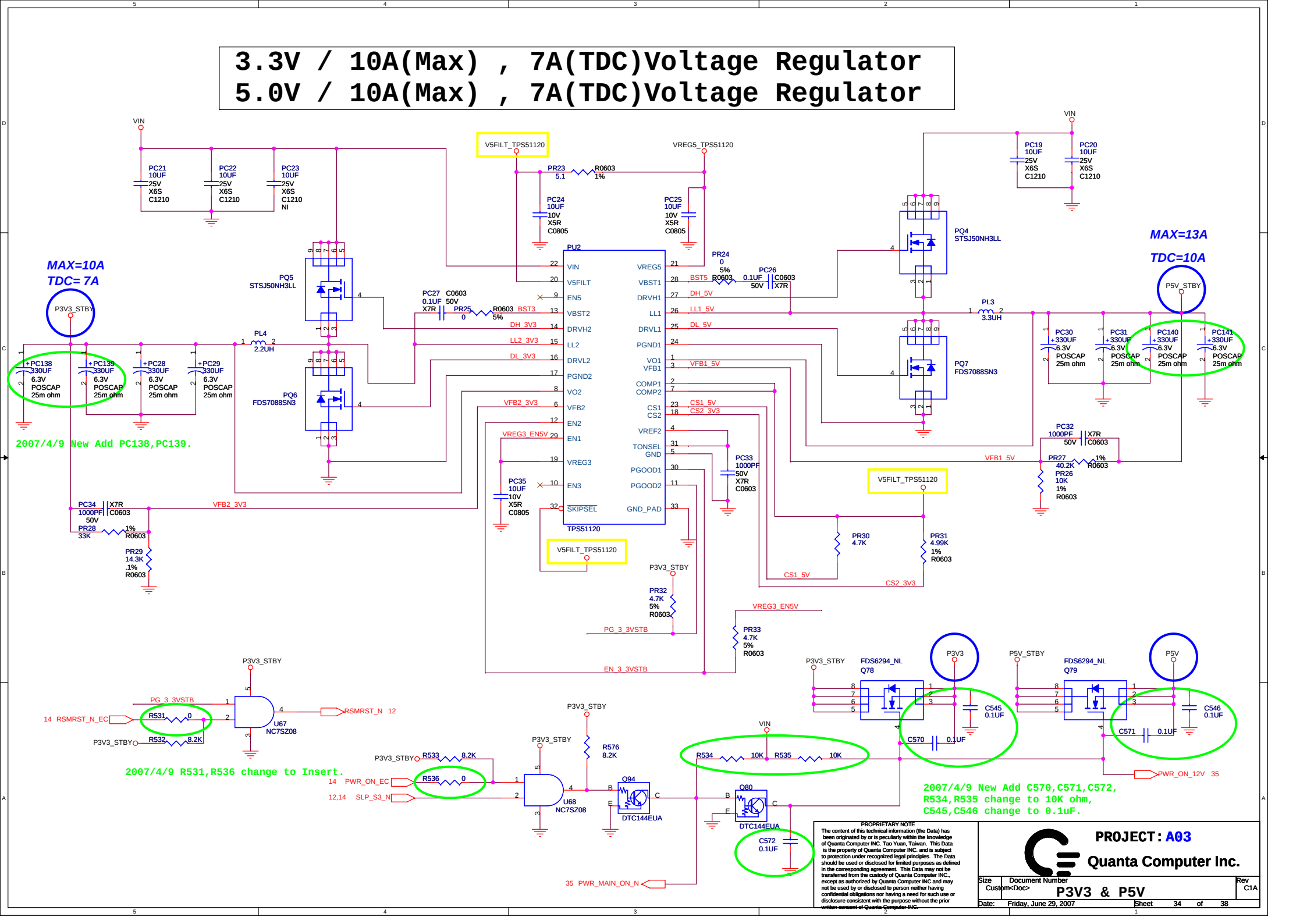
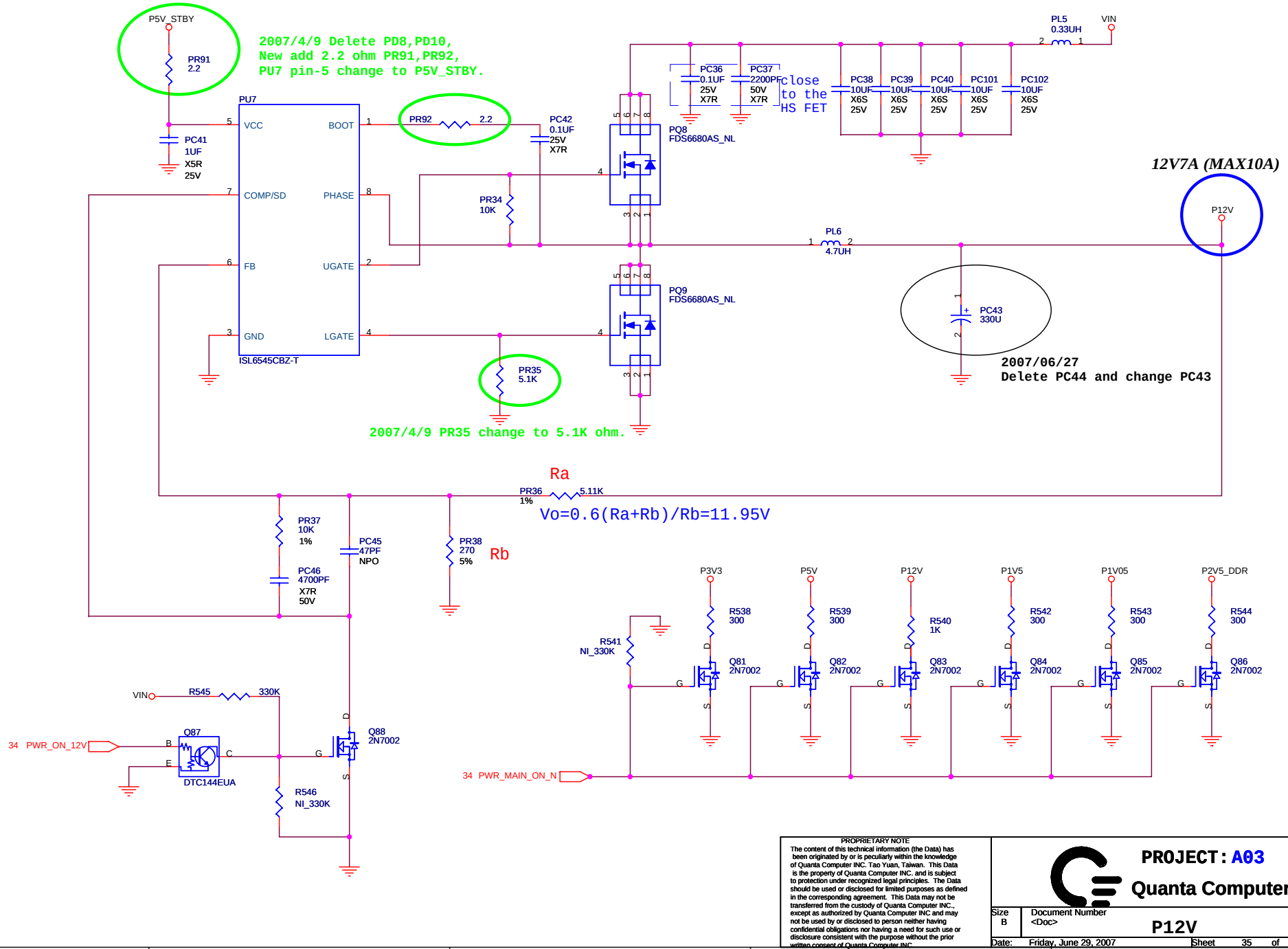
3.3V / 10A(Max) , 7A(TDC)Voltage Regulator
5.0V / 10A(Max) , 7A(TDC)Voltage Regulator





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P12V

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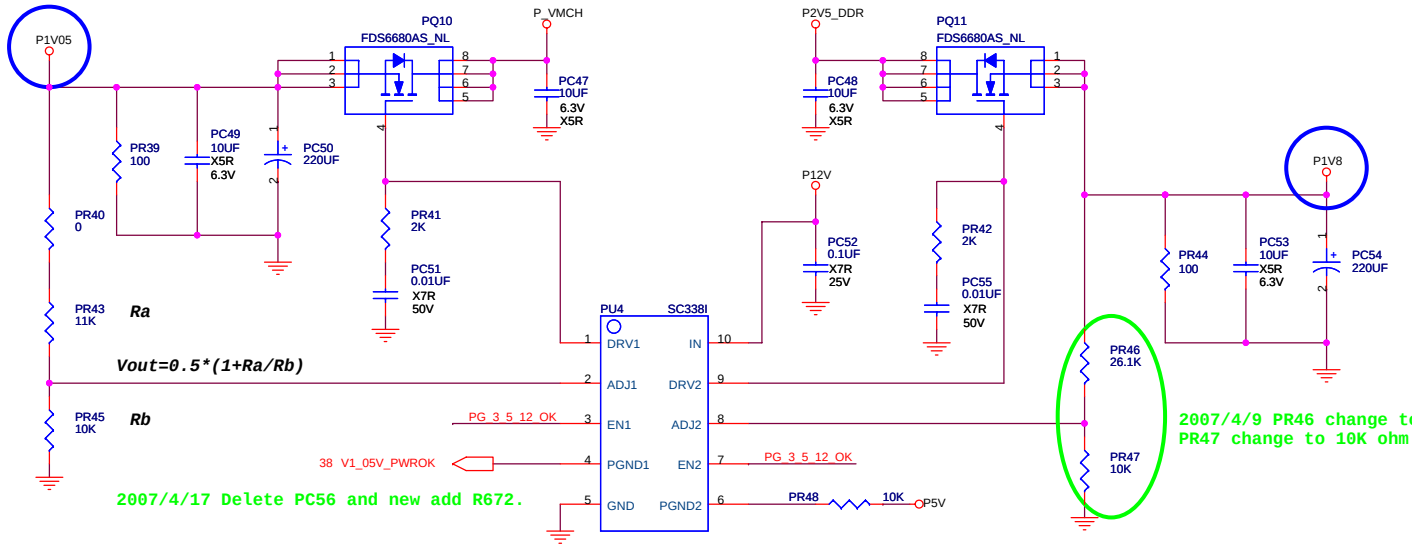
P1V05/3.3A (MAX)
2A (Sustained)



2007/4/17 Delete PC56 and new add R672.

2007/4/9 PR46 change to 26.1K ohm,
PR47 change to 10K ohm.

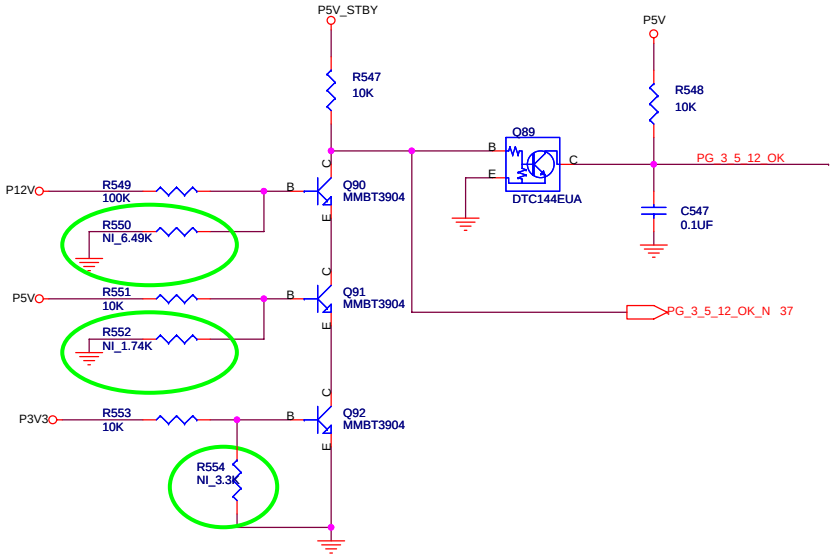
<11.4 = SD

OR

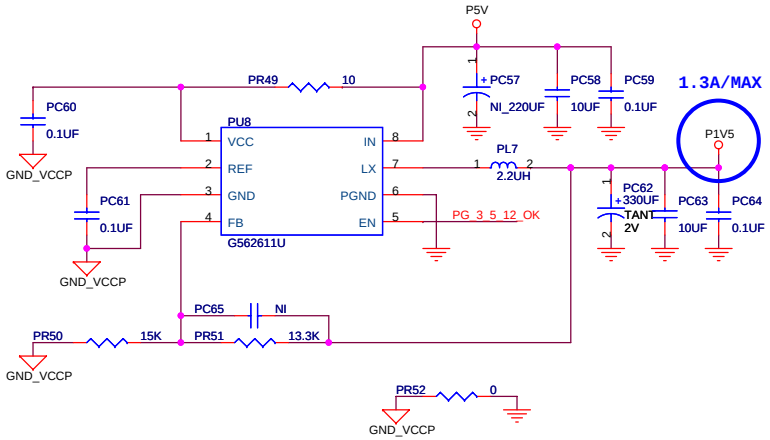
<4.75 = SD

OR

<2.8 = SD



2007/4/9 R550,R552,R554 change to NI.



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A3	<Doc> 1.05/1.5/1.8V Linear Regulator	C1A
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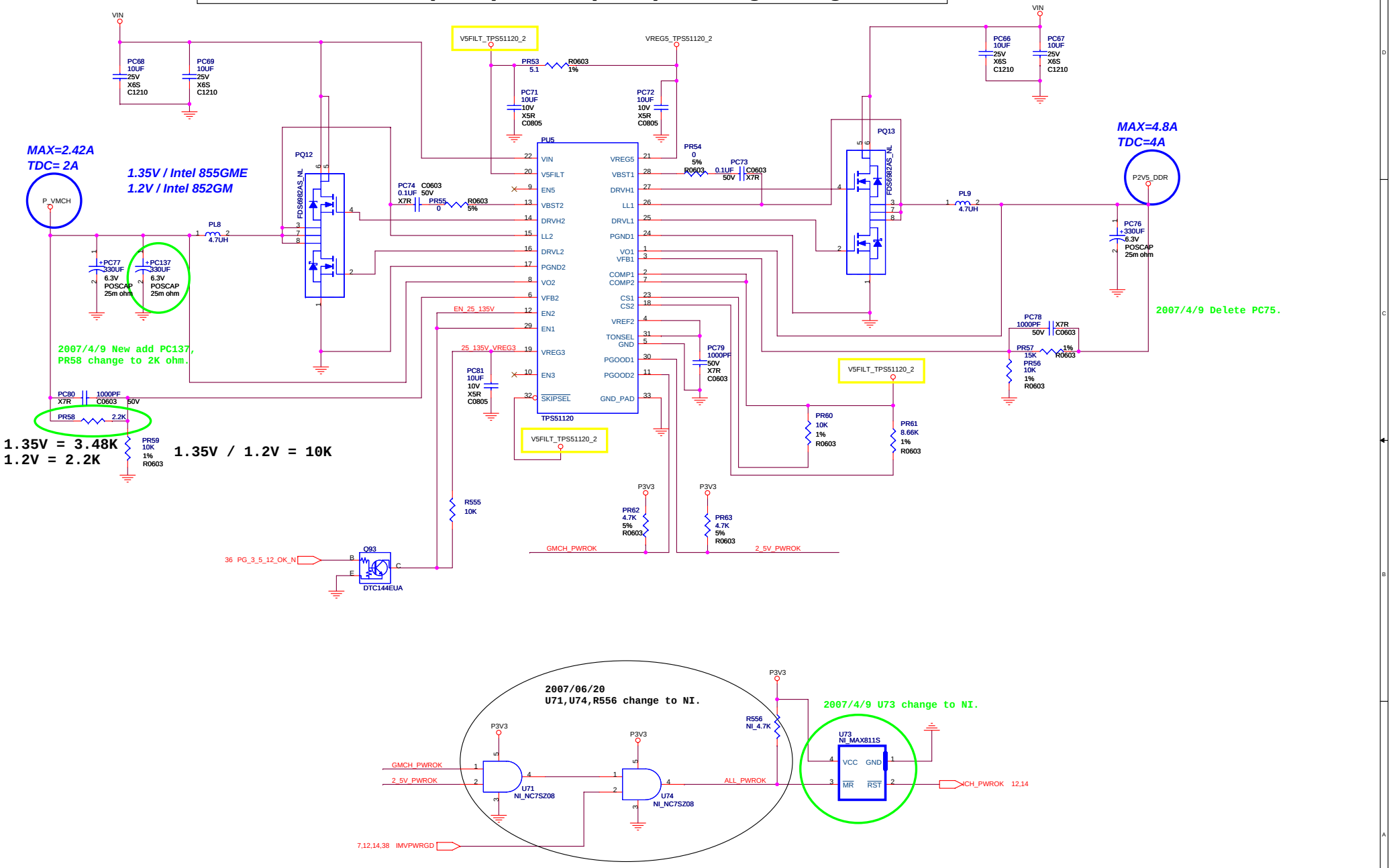
2.5V / 4.8A(Max) , 4A(TDC)Voltage Regulator
1.35V / 2.42A(Max) , 2A(TDC)Voltage Regulator



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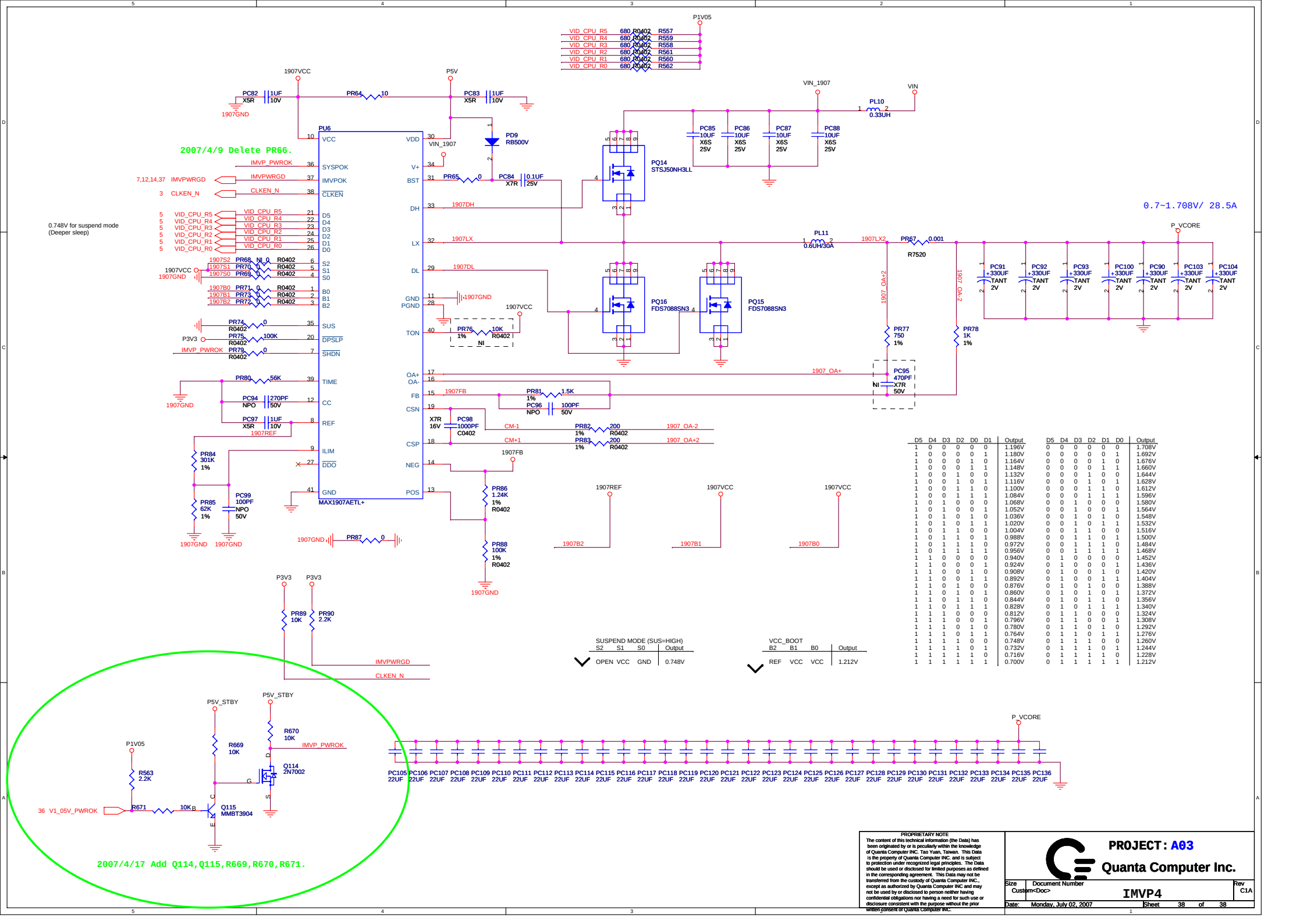
P2V5 & PVMCH


P1V05
VID_CPU_R5 680 R0402 R557
VID_CPU_R4 680 R0402 R559
VID_CPU_R3 680 R0402 R558
VID_CPU_R2 680 R0402 R561
VID_CPU_R1 680 R0402 R560
VID_CPU_R0 680 R0402 R562
1907VCC
P5V
PC82 1UF X5R 10V
PR64 10
PC83 1UF X5R 10V
1907GND
PD9 RB500V
VIN_1907
VIN
PL10 0.33UH
PC85 10UF X6S 25V
PC86 10UF X6S 25V
PC87 10UF X6S 25V
PC88 10UF X6S 25V
PQ14 STSJ50NH3LL
PU6
MAX1907AETL+
2007/4/9 Delete PR66.
0.7~1.708V/ 28.5A
0.748V for suspend mode (Deeper sleep)
PL11 0.6UH/30A
PR67 0.001 R7520
P_VCORE
PC91 +330UF TANT 2V
PC92 +330UF TANT 2V
PC93 +330UF TANT 2V
PC100 +330UF TANT 2V
PC90 +330UF TANT 2V
PC103 +330UF TANT 2V
PC104 +330UF TANT 2V
PQ16 FDS7088SN3
PQ15 FDS7088SN3
PR77 750 1%
PR78 1K 1%
PC95 470PF X7R 50V
PR76 10K 1% R0402
PR81 1.5K 1%
PC96 100PF NPO 50V
PC98 1000PF C0402
PR82 200 1% R0402
PR83 200 1% R0402
PR84 301K 1%
PR85 62K 1%
PC99 100PF NPO 50V
PC94 270PF NPO 50V
PC97 1UF X5R 10V
PR86 1.24K 1% R0402
PR88 100K 1% R0402
PR87 0
PR89 10K
PR90 2.2K
IMVPWRGD
CLKEN_N
SUSPEND MODE (SUS=HIGH)
S2 S1 S0 Output
OPEN VCC GND 0.748V
VCC_BOOT
B2 B1 B0 Output
REF VCC VCC 1.212V
D5 D4 D3 D2 D0 D1 Output
1 0 0 0 0 0 1.196V
1 0 0 0 0 1 1.180V
1 0 0 0 1 0 1.164V
1 0 0 0 1 1 1.148V
1 0 0 1 0 0 1.132V
1 0 0 1 0 1 1.116V
1 0 0 1 1 0 1.100V
1 0 0 1 1 1 1.084V
1 0 1 0 0 0 1.068V
1 0 1 0 0 1 1.052V
1 0 1 0 1 0 1.036V
1 0 1 0 1 1 1.020V
1 0 1 1 0 0 1.004V
1 0 1 1 0 1 0.988V
1 0 1 1 1 0 0.972V
1 0 1 1 1 1 0.956V
1 1 0 0 0 0 0.940V
1 1 0 0 0 1 0.924V
1 1 0 0 1 0 0.908V
1 1 0 0 1 1 0.892V
1 1 0 1 0 0 0.876V
1 1 0 1 0 1 0.860V
1 1 0 1 1 0 0.844V
1 1 0 1 1 1 0.828V
1 1 1 0 0 0 0.812V
1 1 1 0 0 1 0.796V
1 1 1 0 1 0 0.780V
1 1 1 0 1 1 0.764V
1 1 1 1 0 0 0.748V
1 1 1 1 0 1 0.732V
1 1 1 1 1 0 0.716V
1 1 1 1 1 1 0.700V
D5 D4 D3 D2 D1 D0 Output
0 0 0 0 0 0 1.708V
0 0 0 0 0 1 1.692V
0 0 0 0 1 0 1.676V
0 0 0 0 1 1 1.660V
0 0 0 1 0 0 1.644V
0 0 0 1 0 1 1.628V
0 0 0 1 1 0 1.612V
0 0 0 1 1 1 1.596V
0 0 1 0 0 0 1.580V
0 0 1 0 0 1 1.564V
0 0 1 0 1 0 1.548V
0 0 1 0 1 1 1.532V
0 0 1 1 0 0 1.516V
0 0 1 1 0 1 1.500V
0 0 1 1 1 0 1.484V
0 0 1 1 1 1 1.468V
0 1 0 0 0 0 1.452V
0 1 0 0 0 1 1.436V
0 1 0 0 1 0 1.420V
0 1 0 0 1 1 1.404V
0 1 0 1 0 0 1.388V
0 1 0 1 0 1 1.372V
0 1 0 1 1 0 1.356V
0 1 0 1 1 1 1.340V
0 1 1 0 0 0 1.324V
0 1 1 0 0 1 1.308V
0 1 1 0 1 0 1.292V
0 1 1 0 1 1 1.276V
0 1 1 1 0 0 1.260V
0 1 1 1 0 1 1.244V
0 1 1 1 1 0 1.228V
0 1 1 1 1 1 1.212V
P5V_STBY
R669 10K
R670 10K
IMVP_PWROK
Q114 2N7002
P1V05
R563 2.2K
R671 10K
Q115 MMBT3904
36 V1_05V_PWROK
2007/4/17 Add Q114,Q115,R669,R670,R671.
PC105 22UF
PC106 22UF
PC107 22UF
PC108 22UF
PC109 22UF
PC110 22UF
PC111 22UF
PC112 22UF
PC113 22UF
PC114 22UF
PC115 22UF
PC116 22UF
PC117 22UF
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PC131 22UF
PC132 22UF
PC133 22UF
PC134 22UF
PC135 22UF
PC136 22UF
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