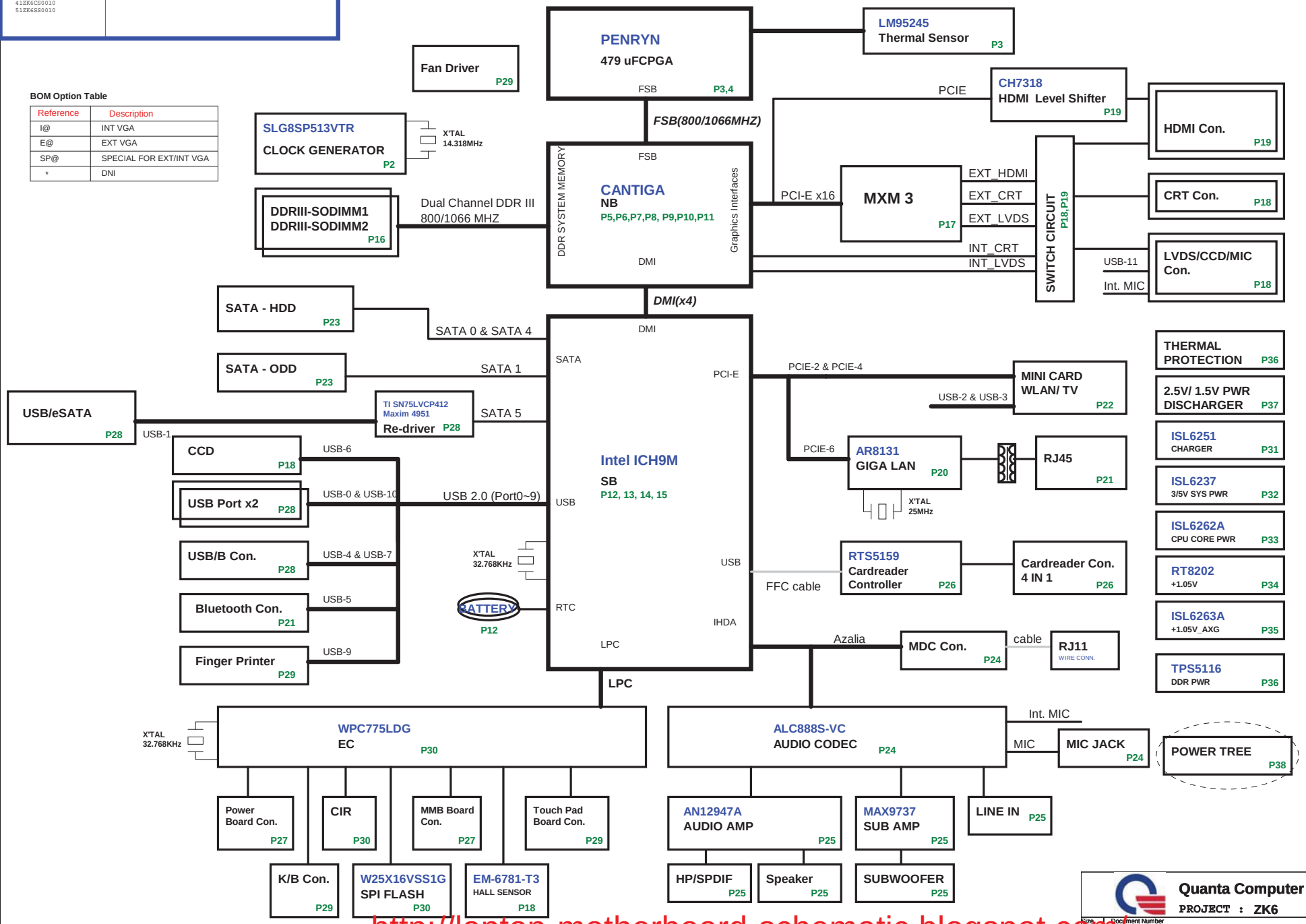
VER : 1A

BOM P/N	Description
31ZK6MB0000 41ZK6CS0000 51ZK6SS0000 31ZK6MB0010 41ZK6CS0010 51ZK6SS0010	uma / mxm 00 / 10

ZK6 MB Block Diagram

BOM Option Table

Reference	Description
I@	INT VGA
E@	EXT VGA
SP@	SPECIAL FOR EXT/INT VGA
*	DNI



Quanta Computer Inc.
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Size: Document Number: Block Diagram Rev 1A
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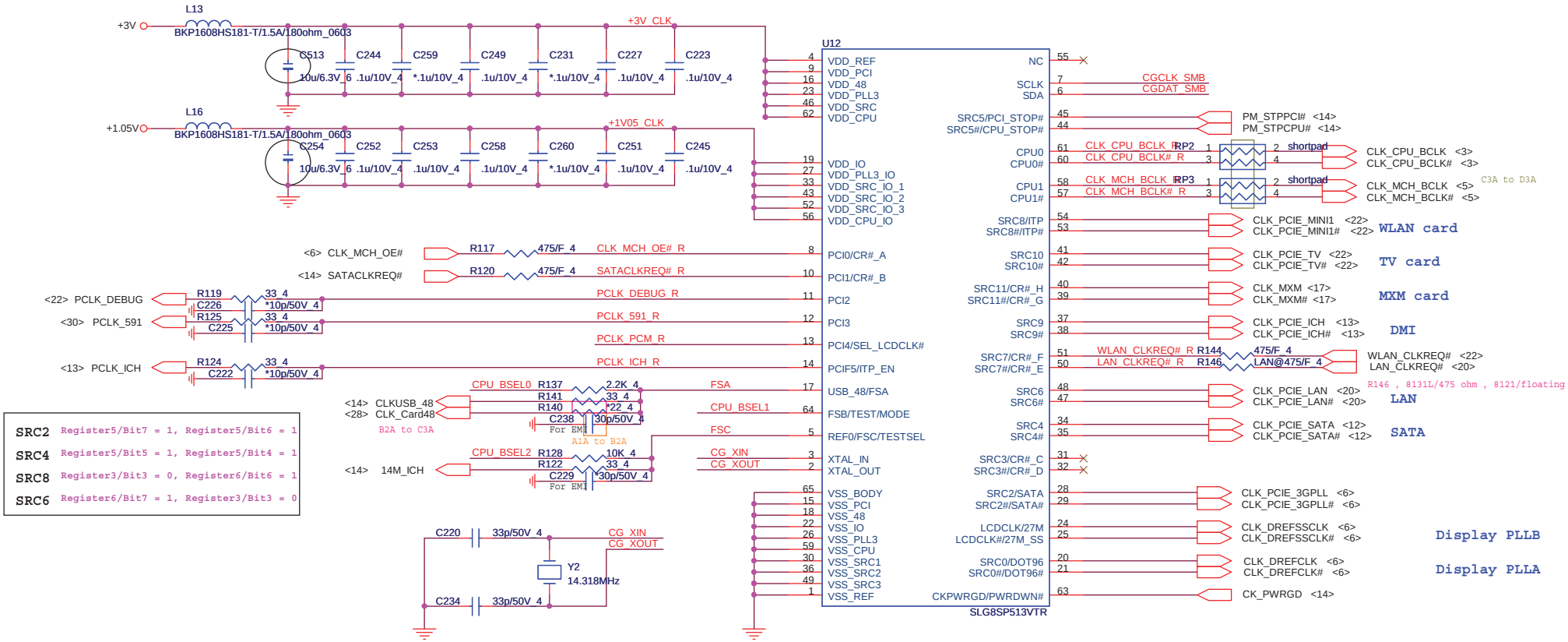
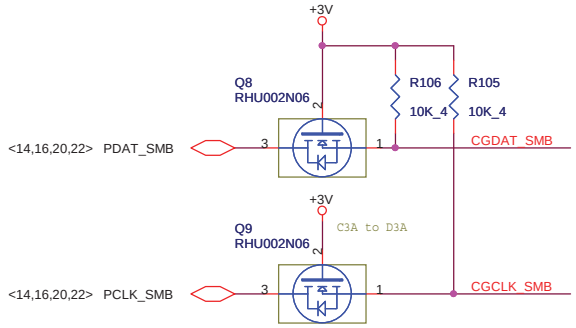
Clock Generator

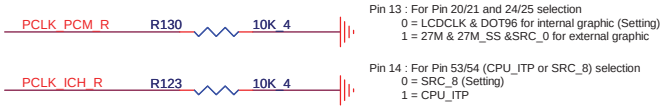


CPU Clock select

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz



Clock Generator Strap table



Quanta Computer Inc.
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Size	Document Number	Rev
	CLOCK GENERATOR	1A
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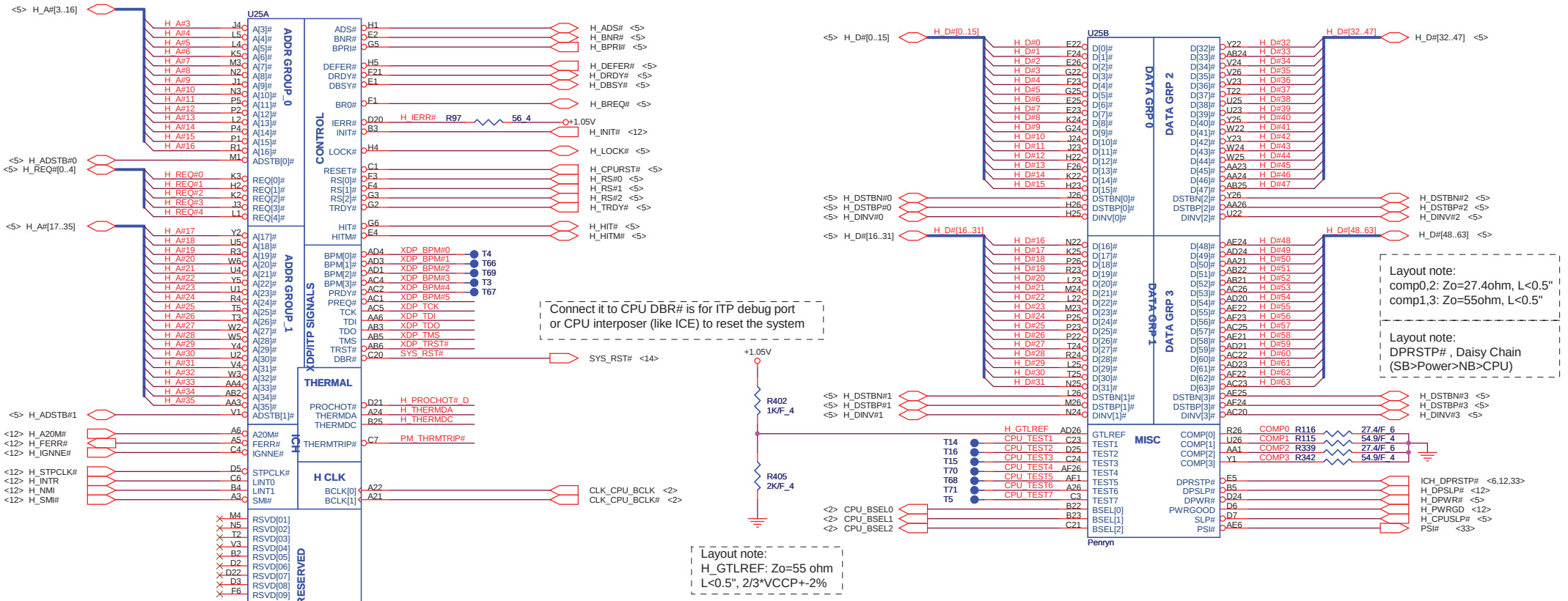
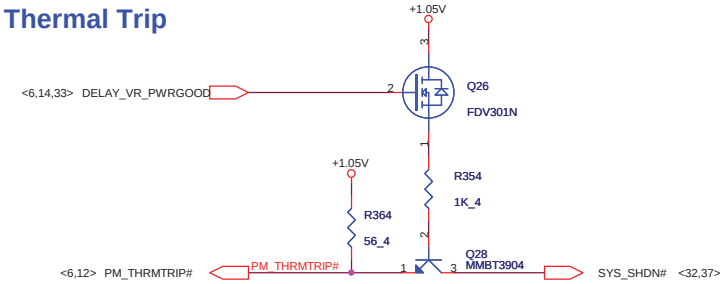
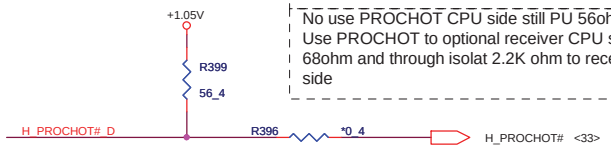


Thermal Trip



Processor hot

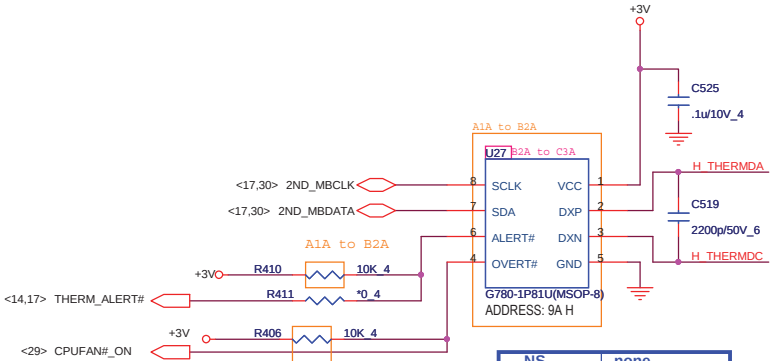


No use Thermal trip CPU side still PU 56ohm.
Use Thermal trip can share PU at SB side

No use PROCHOT CPU side still PU 56ohm.
Use PROCHOT to optional receiver CPU side PU 68ohm and through isolat 2.2K ohm to receiver side

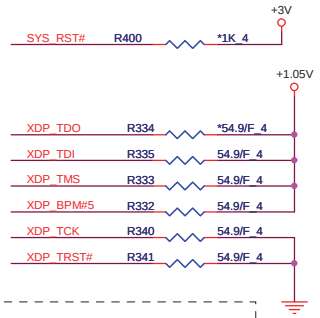
CPU 1/2

CPU Thermal monitor



NS	none
WINDBOND	AL83L771K02
GMT	AL000780003

XDP PU/PD



XDP_DBRESET# and XDP_TDO reserve for XDP

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Size	Document Number	Rev
	CPU Host Bus	1A
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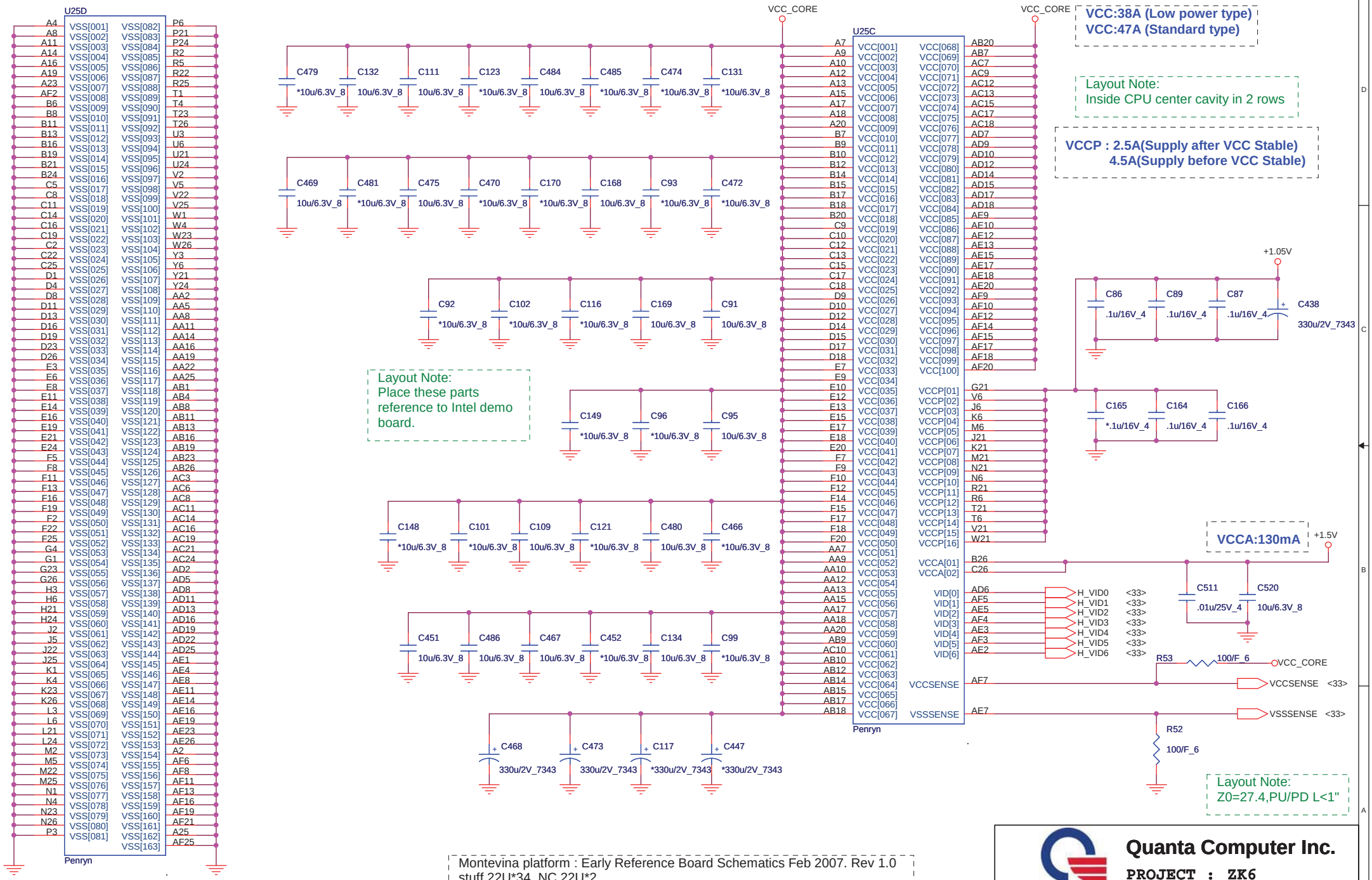
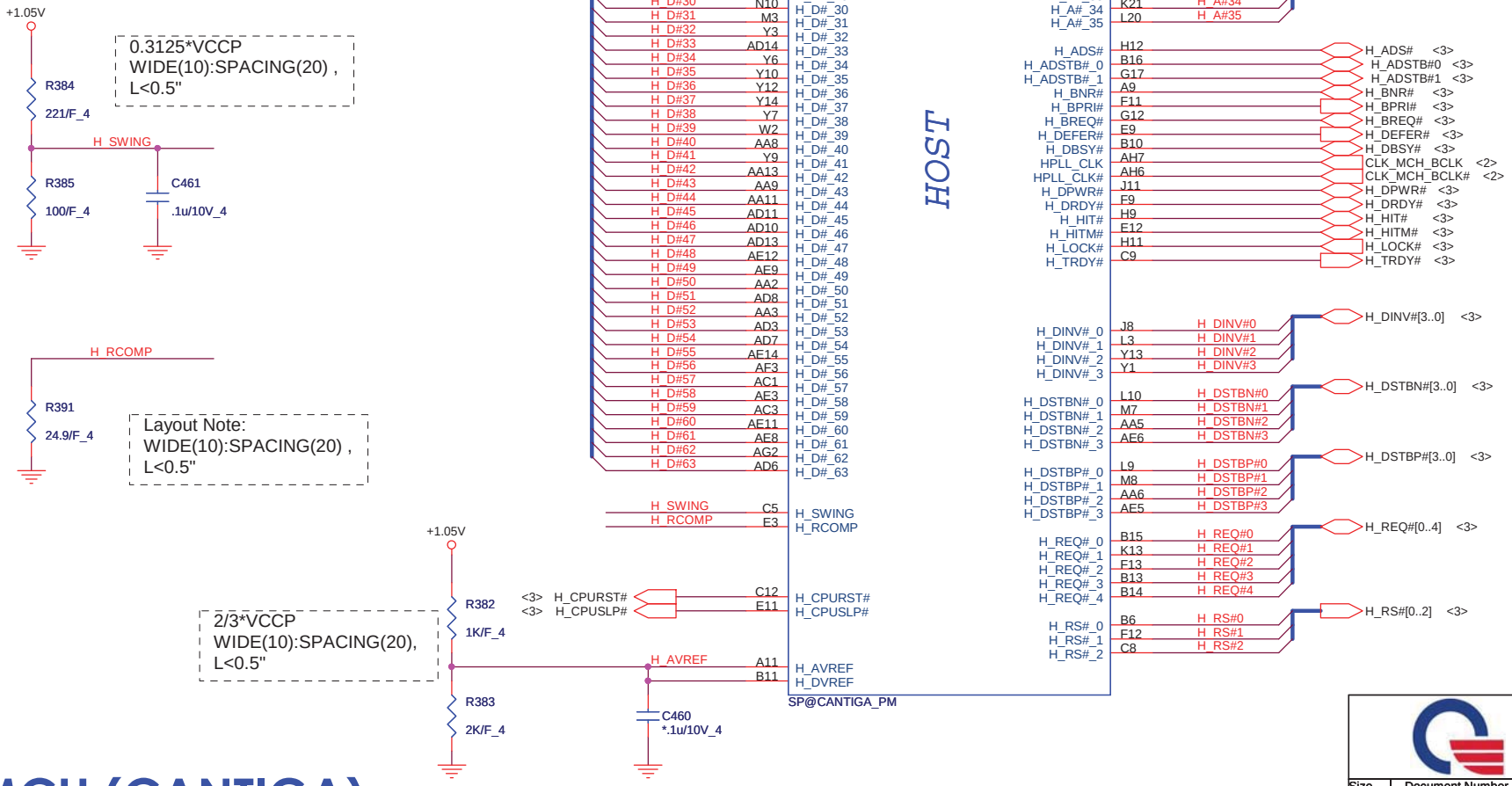


	QCI P/N
Intel Cantiga (G)M	AJSLB940T04
Intel Cantiga (P)M	AJSLB970T06



Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	GMCH HOST	1A
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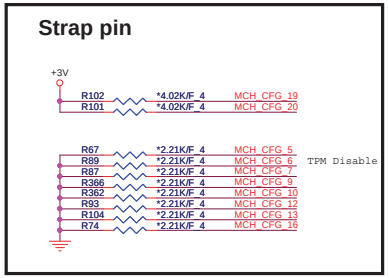
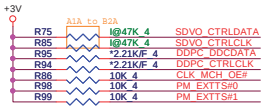
IV@
EV@

Strap table

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	000= FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)
CFG7	ME TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)
CFG8	Reserved	
CFG9	PCIE Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG10	PCIE Loopback enable	0 = Enabled 1 = Disabled (Default)
CFG11	Reserved	
CFG12	ALLZ	0 = ALLZ mode enable 1 = disable(Default)
CFG13	XOR	0 = XOR mode enable 1 = disable(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display port (SDVO/DP/iHDMI) or PCIE is operational (Default) 1 = Digital Display port (SDVO/DP/iHDMI) and PCIE are operating simultaneously via PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/HDMI Device Present(Default) 1 = SDVO/HDMI Device present
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent(Default) 1 = Digital display(HDMI/DP) device present

Strap pin





U26B

RSVD
RSVD1 M36
RSVD2 N36
RSVD3 R33
RSVD4 T33
RSVD5 AH9
RSVD6 AH10
RSVD7 AH12
RSVD8 AH13
RSVD9 K12
RSVD14 T24
RSVD15 B31
RSVD17 M1
RSVD20 AY21
RSVD21 B2
RSVD22 BG23
RSVD23 BF23
RSVD24 BH18
RSVD25 BF18

JTAG
JTAG_TCK T18 AL34 ME_JTAG_TCK
JTAG_TDI T19 AK34 ME_JTAG_TDI
JTAG_TDO T20 AN35 ME_JTAG_TDO
JTAG_TMS T17 AM35 ME_JTAG_TMS

CFG
<2> MCH_BSEL0 T25 CFG_0
<2> MCH_BSEL1 R25 CFG_1
<2> MCH_BSEL2 P25 CFG_2
MCH_CFG_3 T11 P20 CFG_3
MCH_CFG_4 T13 P24 CFG_4
MCH_CFG_5 C25 CFG_5
MCH_CFG_6 N24 CFG_6
MCH_CFG_7 M24 CFG_7
MCH_CFG_8 T6 F21 CFG_8
MCH_CFG_9 C23 CFG_9
MCH_CFG_10 C24 CFG_10
MCH_CFG_11 T9 N21 CFG_11
MCH_CFG_12 P21 CFG_12
MCH_CFG_13 T21 CFG_13
MCH_CFG_14 T12 R20 CFG_14
MCH_CFG_15 T8 M20 CFG_15
MCH_CFG_16 L21 CFG_16
MCH_CFG_17 T7 H21 CFG_17
MCH_CFG_18 T10 P29 CFG_18
MCH_CFG_19 R28 CFG_19
MCH_CFG_20 T28 CFG_20

PM
<14> PM_SYNC# R29 PM_SYNC#
<3,12,33> ICH_DPRSTP# B7 PM_DPRSTP#
<16> PM_EXTTS#0 N33 PM_EXT_TS#_0
<16> PM_EXTTS#1 P32 PM_EXT_TS#_1
<3,14,33> DELAY_VR_PWRGOOD AT40 PWROK
<13> PLT_RST# AT11 RSTIN#
<3,12> PM_THRMTRIP# T20 THERMTRIP#
<14,33> PM_DPRSLPVR R32 DPRSLPVR
R126 100/F_4 RST_IN# MCH
R100 *0_4 THRMTRIP#_R

NC
BG48 NC_1
BF48 NC_2
BD48 NC_3
BC48 NC_4
BH47 NC_5
BG47 NC_6
BE47 NC_7
BH46 NC_8
BF46 NC_9
BG45 NC_10
BH44 NC_11
BH43 NC_12
BH6 NC_13
BH5 NC_14
BG4 NC_15
BH3 NC_16
BF3 NC_17
BH2 NC_18
BG2 NC_19
BE2 NC_20
BG1 NC_21
BF1 NC_22
BD1 NC_23
BC1 NC_24
F1 NC_25

SP@CANTIGA_PM

NB Thermal trip pin
No use Thermal trip NB side can NC.(NB has ODT)

PM_DPRSTP#
The Daisy chain topology should be routed from ICH9M to IMVP , then to (G)MCH and CPU, in that order.

CLK/ DDR CONTROL/COMPENSATION
SA_CK_0 AP24 M_CLK0 <16>
SA_CK_1 AT21 M_CLK1 <16>
SB_CK_0 AV24 M_CLK2 <16>
SB_CK_1 AU20 M_CLK3 <16>
SA_CK#_0 AR24 M_CLK#0 <16>
SA_CK#_1 AR21 M_CLK#1 <16>
SB_CK#_0 AU24 M_CLK#2 <16>
SB_CK#_1 AV20 M_CLK#3 <16>
SA_CKE_0 BC28 M_CKE0 <16>
SA_CKE_1 AY28 M_CKE1 <16>
SB_CKE_0 AY36 M_CKE2 <16>
SB_CKE_1 BB36 M_CKE3 <16>
SA_CS#_0 BA17 M_CS#0 <16>
SA_CS#_1 AY16 M_CS#1 <16>
SB_CS#_0 AV16 M_CS#2 <16>
SB_CS#_1 AR13 M_CS#3 <16>
SA_ODT_0 BD17 M_ODT0 <16>
SA_ODT_1 AY17 M_ODT1 <16>
SB_ODT_0 BF15 M_ODT2 <16>
SB_ODT_1 AY13 M_ODT3 <16>
SM_RCOMP BG22 M_RCOMP
SM_RCOMP# BH21 M_RCOMP#
SM_RCOMP_VOH BF28 SM_RCOMP_VOH
SM_RCOMP_VOL BH28 SM_RCOMP_VOL
SM_VREF AV42 SM_VREF
SM_PWROK AR36 SM_POK
SM_REXT BF17 SM_REXT R139 499/F_4
SM_DRAMRST# BC36 DDR3_RST# <16>

SM_VREF=0.5*VCC_SM
SM_PWROK only for DDR3.(DDR2 PD only)
SM_DRAMRST# only for DDR3.(DDR2:NC)

CLK
DPLL_REF_CLK B38 CLK_DREFCLK <2>
DPLL_REF_CLK# A38 CLK_DREFCLK# <2>
DPLL_REF_SSCLK E41 CLK_DREFSSCLK <2>
DPLL_REF_SSCLK# F41 CLK_DREFSSCLK# <2>
PEG_CLK F43 CLK_PCIE_3GPLL <2>
PEG_CLK# E43 CLK_PCIE_3GPLL# <2>

DMI
DMI_RXN_0 AE41 DMI_TXN0
DMI_RXN_1 AE37 DMI_TXN1
DMI_RXN_2 AE47 DMI_TXN2
DMI_RXN_3 AH39 DMI_TXN3
DMI_TXP[3:0] <13>
DMI_RXP_0 AE40 DMI_TXP0
DMI_RXP_1 AE38 DMI_TXP1
DMI_RXP_2 AE48 DMI_TXP2
DMI_RXP_3 AH40 DMI_TXP3
DMI_RXN[3:0] <13>
DMI_TXN_0 AE35 DMI_RXN0
DMI_TXN_1 AE43 DMI_RXN1
DMI_TXN_2 AE46 DMI_RXN2
DMI_TXN_3 AH42 DMI_RXN3
DMI_RXP[3:0] <13>
DMI_TXP_0 AD35 DMI_RXP0
DMI_TXP_1 AE44 DMI_RXP1
DMI_TXP_2 AE46 DMI_RXP2
DMI_TXP_3 AH43 DMI_RXP3

GRAPHICS VID
GFX_VID_0 B33 GPU_VID0 <35>
GFX_VID_1 B32 GPU_VID1 <35>
GFX_VID_2 G33 GPU_VID2 <35>
GFX_VID_3 F33 GPU_VID3 <35>
GFX_VID_4 E33 GPU_VID4 <35>
GFX_VR_EN C34 GFX_VR_EN

Check list note : CL_VREF=0.35V

ME
CL_CLK AH37 CL_CLK0 <14>
CL_DATA AH36 CL_DATA0 <14>
CL_PWROK AN36 MPWROK <14,30>
CL_RST# AJ35 CL_RST#0 <14>
CL_VREF AH34 MCH_CLVREF_R

MISC
DDPC_CTRLCLK N28 DDPC_CTRLCLK
DDPC_CTRLDATA M28 DDPC_DDCDATA
SDVO_CTRLCLK G36 SDVO_CTRLCLK <19>
SDVO_CTRLDATA E36 SDVO_CTRLDATA <19>
CLKREQ# K36 CLK_MCH_OE# <2>
ICH_SYNC# H36 MCH_ICH_SYNC# <14>
TSATN# B12 TSATN# R63 56_4 +1.05V

HDA
HDA_BCLK B28 HDA_BIT_CLK_HDMI
HDA_RST# B30 HDA_RST#_HDMI
HDA_SDI B29 HDA_SDIN_HDMI
HDA_SDO C29 HDA_SDOUT_HDMI
HDA_SYNC A28 HDA_SYNC_HDMI
HDA_BIT_CLK_HDMI <12>
HDA_RST#_HDMI <12>
HDA_SDIN_HDMI <12>
HDA_SDOUT_HDMI <12>
HDA_SYNC_HDMI <12>

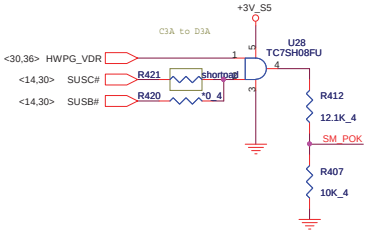
If HDMI not support
HDA --> NC
VCC_HDA-->GND
Differential signal-->NC

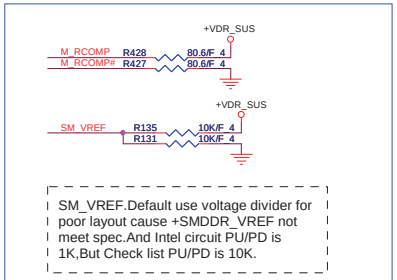
Impact ICH9M VCCHDA and VCCSUSHDA supply 1.5V/3.3V

NOTE:
If (G)MCH's HD Audio signals are connected to ICH9M for iHDMI, VCCHDA and VCCSUSHDA on ICH9M should be only on 1.5V. These power pins on ICH9M can be supplied with 3.3V if and only if (G)MCH's HDA is not connected to ICH9M. Consequently, only 1.5V audio/modem codecs can be used on the platform.

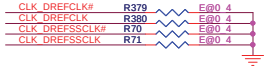
R108 1K/F_4
C198 .1u/10V_4
R112 511/F_4

DDR3 PWROK

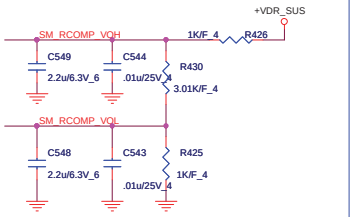




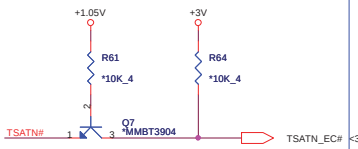
SM_VREF.Default use voltage divider for poor layout cause +SMDDR_VREF not meet spec.And Intel circuit PU/PD is 1K,But Check list PU/PD is 10K.



INTEL FAE Suggest PD for Ext graphics



NB Thermaltrip



DDPC_CTRL for HDMI port C
SDVO_CTRL for HDMI port B

<Checklist ver0.8>
If TSATN# is not used, then it must be terminated with a 56-Ω pull-up resistor to VCCP.

<Pin out check issue>
Cantiga EDS 0.7 change Ball B12 to TSATN# from TSATN

Quanta Computer Inc.
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Size	Document Number	Rev
	GMCH DMI	1A

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GMCH (CANTIGA)

IV@

EV@

SP@

IV&EV Dis/Enable setting

If LVDS no use,all signal can NC

U26C

<18> L_BKLT_CTRL
<18> INT_LVDS_BLON
R92 I@10K_4 L_CTRL_CLK
+3V
R91 I@10K_4 L_CTRL_DATA
<18> INT_LVDS_EDIDCLK
<18> INT_LVDS_EDIDDATA
<18> INT_LVDS_DIGON
R65 I@2.37K/F_4

L32 L_BKLT_CTRL
G32 L_BKLT_EN
M32 L_CTRL_CLK
M33 L_CTRL_DATA
K33 L_DDC_CLK
J33 L_DDC_DATA
M29 L_VDD_EN
C44 LVDS_IBG
B43 LVDS_VBG
E37 LVDS_VREFH
E38 LVDS_VREFL

<17> INT_TXLCLKOUT-
<17> INT_TXLCLKOUT+
<17> INT_TXUCLKOUT-
<17> INT_TXUCLKOUT+
INT_TXLCLKOUT- C41 LVDSA_CLK#
INT_TXLCLKOUT+ C40 LVDSA_CLK
INT_TXUCLKOUT- B37 LVDSB_CLK#
INT_TXUCLKOUT+ A37 LVDSB_CLK

<17> INT_TXLOUT0-
<17> INT_TXLOUT1-
<17> INT_TXLOUT2-
INT_TXLOUT0- H47 LVDSA_DATA#_0
INT_TXLOUT1- E46 LVDSA_DATA#_1
INT_TXLOUT2- G40 LVDSA_DATA#_2
A40 LVDSA_DATA#_3

<17> INT_TXLOUT0+
<17> INT_TXLOUT1+
<17> INT_TXLOUT2+
INT_TXLOUT0+ H48 LVDSA_DATA_0
INT_TXLOUT1+ D45 LVDSA_DATA_1
INT_TXLOUT2+ F40 LVDSA_DATA_2
B40 LVDSA_DATA_3

<17> INT_TXUOUT0-
<17> INT_TXUOUT1-
<17> INT_TXUOUT2-
INT_TXUOUT0- A41 LVDSB_DATA#_0
INT_TXUOUT1- H38 LVDSB_DATA#_1
INT_TXUOUT2- G37 LVDSB_DATA#_2
J37 LVDSB_DATA#_3

<17> INT_TXUOUT0+
<17> INT_TXUOUT1+
<17> INT_TXUOUT2+
INT_TXUOUT0+ B42 LVDSB_DATA_0
INT_TXUOUT1+ G38 LVDSB_DATA_1
INT_TXUOUT2+ F37 LVDSB_DATA_2
K37 LVDSB_DATA_3

R68 75_4 INT_TV_COMP F25 TVA_DAC
R69 75_4 INT_TV_Y/G H25 TVB_DAC
R84 75_4 INT_TV_C/R K25 TVC_DAC
H24 TV_RTN
C31 TV_DCONSEL_0
E32 TV_DCONSEL_1

<17> INT_CRT_BLU INT_CRT_BLU E28 CRT_BLUE
<17> INT_CRT_GRN INT_CRT_GRN G28 CRT_GREEN
<17> INT_CRT_RED INT_CRT_RED J28 CRT_RED
G29 CRT_IRTN
H32 CRT_DDC_CLK
J32 CRT_DDC_DATA
INT_HSYNC J29 CRT_HSYNC
CRTIREF E29 CRT_TVO_IREF
INT_VSYNC L29 CRT_VSYNC

<17> INT_CRT_DDCCLK
<17> INT_CRT_DDCDAT
<17> INT_HSYNC
<17> INT_VSYNC

SP@CANTIGA_PM

SDVO
PCI-EXPRESS GRAPHICS
VGA

L<0.5" , If PCIE not support still connect to +VCC_PEG

+1.05V
T37 EXP_A_COMPX R103 49.9/F_4
T36

PEG_COMPI
PEG_COMPO

PEG_RX#_0 H44 PEG_RXN0
PEG_RX#_1 J46 PEG_RXN1
PEG_RX#_2 L44 PEG_RXN2
PEG_RX#_3 L40 PEG_RXN3
PEG_RX#_4 N41 PEG_RXN4
PEG_RX#_5 P48 PEG_RXN5
PEG_RX#_6 N44 PEG_RXN6
PEG_RX#_7 T43 PEG_RXN7
PEG_RX#_8 U43 PEG_RXN8
PEG_RX#_9 Y43 PEG_RXN9
PEG_RX#_10 Y48 PEG_RXN10
PEG_RX#_11 Y36 PEG_RXN11
PEG_RX#_12 AA43 PEG_RXN12
PEG_RX#_13 AD37 PEG_RXN13
PEG_RX#_14 AC47 PEG_RXN14
PEG_RX#_15 AD39 PEG_RXN15
PEG_RXN[15:0] <17>

PEG_RX_0 H43 PEG_RXP0
PEG_RX_1 J44 PEG_RXP1
PEG_RX_2 L43 PEG_RXP2
PEG_RX_3 L41 PEG_RXP3
PEG_RX_4 N40 PEG_RXP4
PEG_RX_5 P47 PEG_RXP5
PEG_RX_6 N43 PEG_RXP6
PEG_RX_7 T42 PEG_RXP7
PEG_RX_8 U42 PEG_RXP8
PEG_RX_9 Y42 PEG_RXP9
PEG_RX_10 W47 PEG_RXP10
PEG_RX_11 Y37 PEG_RXP11
PEG_RX_12 AA42 PEG_RXP12
PEG_RX_13 AD36 PEG_RXP13
PEG_RX_14 AC48 PEG_RXP14
PEG_RX_15 AD40 PEG_RXP15
PEG_RXP[15:0] <17>

PEG_TX#_0 J41 C_PEG_TXN0 C103 .1u/10V_4 PEG_TXN0
PEG_TX#_1 M46 C_PEG_TXN1 C119 .1u/10V_4 PEG_TXN1
PEG_TX#_2 M47 C_PEG_TXN2 C125 .1u/10V_4 PEG_TXN2
PEG_TX#_3 M40 C_PEG_TXN3 C133 .1u/10V_4 PEG_TXN3
PEG_TX#_4 M42 C_PEG_TXN4 C105 E@.1u/10V_4 PEG_TXN4
PEG_TX#_5 R48 C_PEG_TXN5 C141 E@.1u/10V_4 PEG_TXN5
PEG_TX#_6 N38 C_PEG_TXN6 C154 E@.1u/10V_4 PEG_TXN6
PEG_TX#_7 T40 C_PEG_TXN7 C186 E@.1u/10V_4 PEG_TXN7
PEG_TX#_8 U37 C_PEG_TXN8 C197 E@.1u/10V_4 PEG_TXN8
PEG_TX#_9 U40 C_PEG_TXN9 C201 E@.1u/10V_4 PEG_TXN9
PEG_TX#_10 Y40 C_PEG_TXN10 C211 E@.1u/10V_4 PEG_TXN10
PEG_TX#_11 AA46 C_PEG_TXN11 C215 E@.1u/10V_4 PEG_TXN11
PEG_TX#_12 AA37 C_PEG_TXN12 C208 E@.1u/10V_4 PEG_TXN12
PEG_TX#_13 AA40 C_PEG_TXN13 C230 E@.1u/10V_4 PEG_TXN13
PEG_TX#_14 AD43 C_PEG_TXN14 C237 E@.1u/10V_4 PEG_TXN14
PEG_TX#_15 AC46 C_PEG_TXN15 C239 E@.1u/10V_4 PEG_TXN15
PEG_TXN[15:0] <17>

PEG_TX_0 J42 C_PEG_TXP0 C100 .1u/10V_4 PEG_TXP0
PEG_TX_1 L46 C_PEG_TXP1 C113 .1u/10V_4 PEG_TXP1
PEG_TX_2 M48 C_PEG_TXP2 C122 .1u/10V_4 PEG_TXP2
PEG_TX_3 M39 C_PEG_TXP3 C130 .1u/10V_4 PEG_TXP3
PEG_TX_4 M43 C_PEG_TXP4 C112 E@.1u/10V_4 PEG_TXP4
PEG_TX_5 R47 C_PEG_TXP5 C147 E@.1u/10V_4 PEG_TXP5
PEG_TX_6 N37 C_PEG_TXP6 C151 E@.1u/10V_4 PEG_TXP6
PEG_TX_7 T39 C_PEG_TXP7 C184 E@.1u/10V_4 PEG_TXP7
PEG_TX_8 U36 C_PEG_TXP8 C194 E@.1u/10V_4 PEG_TXP8
PEG_TX_9 U39 C_PEG_TXP9 C199 E@.1u/10V_4 PEG_TXP9
PEG_TX_10 Y39 C_PEG_TXP10 C202 E@.1u/10V_4 PEG_TXP10
PEG_TX_11 Y46 C_PEG_TXP11 C213 E@.1u/10V_4 PEG_TXP11
PEG_TX_12 AA36 C_PEG_TXP12 C207 E@.1u/10V_4 PEG_TXP12
PEG_TX_13 AA39 C_PEG_TXP13 C221 E@.1u/10V_4 PEG_TXP13
PEG_TX_14 AD42 C_PEG_TXP14 C232 E@.1u/10V_4 PEG_TXP14
PEG_TX_15 AD46 C_PEG_TXP15 C243 E@.1u/10V_4 PEG_TXP15
PEG_TXP[15:0] <17>

IV&EV Dis/Enable setting

<5/31>Montevina_Schematics_Checklist_Rev0_8
a)For TVOUT Disabled, TV_DCONSEL[1:0] Connect to GND. But design guide Rev0.7 show NC.What is correct.
b)For CRT DAC Disable, CRT_DDC_CLK, CRT_DDC_DATA . CRT_HSYNC, CRT_VSYNCThese signals should be connected to GND. But design guide Rev0.7 show NC, Intel suggest follow Design guide.

<check list>	<check list>
For EV@	For IV@
CRT R/G/B 0ohm to GND	CRT R/G/B 150ohm to GND
CRTIREF 0ohm to GND	CRTIREF 976 ohm to GND (>12")

CRTIREF
For IV: 1.02Kohm
For EV:0ohm
R72 SP@1K/F_4 CRTIREF

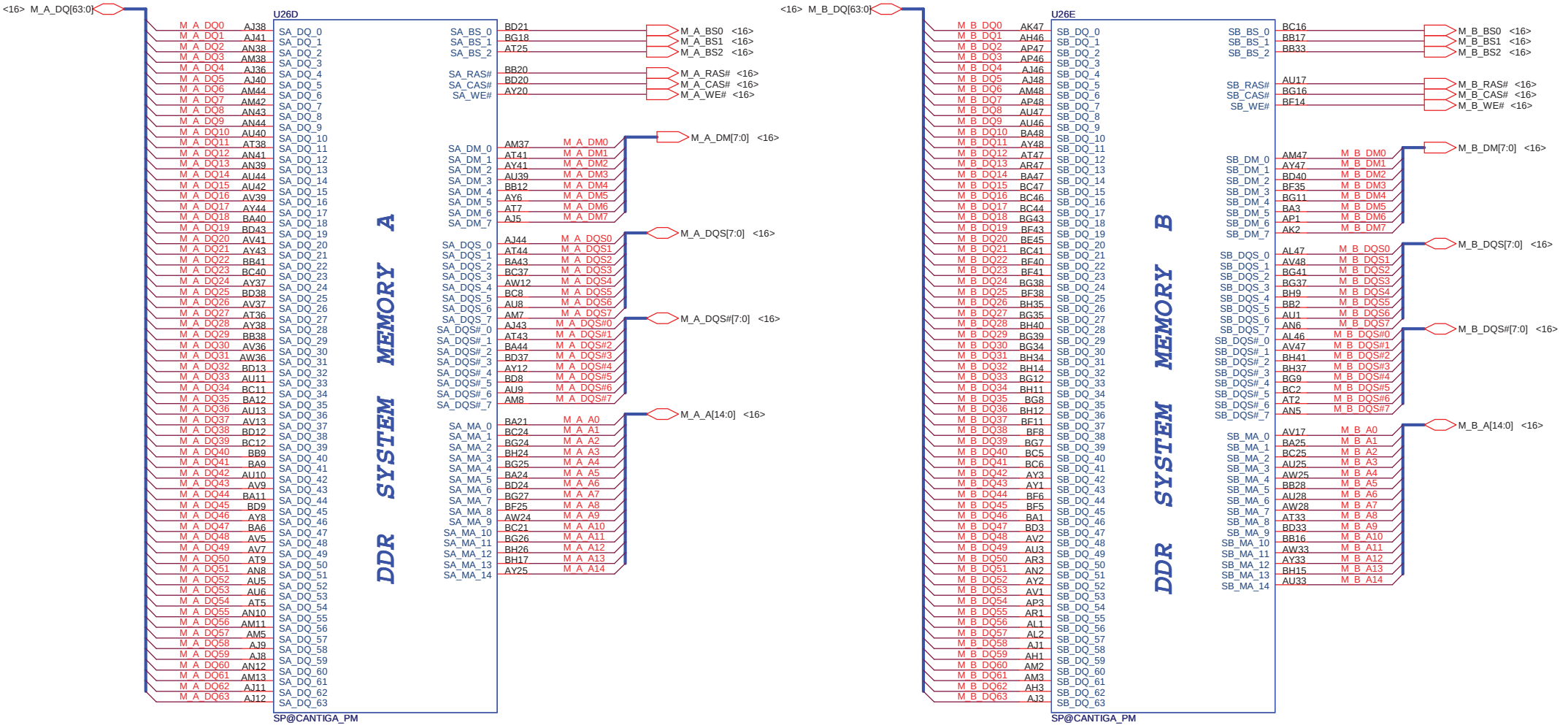
SP@
CRT_R/G/B
For IV: 150ohm
For EV:0ohm
R73 SP@150_4 INT_CRT_BLU
R83 SP@150_4 INT_CRT_GRN
R88 SP@150_4 INT_CRT_RED

MXM STUFFED.

INT_HSYNC
INT_VSYNC
R82 E@0_4
R80 E@0_4

CRTIREF pull down for IV cantiga 1.02k ohm/F

Quanta Computer Inc.			
PROJECT : ZK6			
Size	Document Number		Rev
	GMCH VGA		1A
Date: Friday, April 24, 2009		Sheet 7 of 42	



GMCH (CANTIGA)

Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	GMCH DDRIII	1A
Date: Friday, April 24, 2009	Sheet 8 of 42	

IV@

SP@

VCC_SM(1.5VSUS)
DDR3(800M) : 3162.5mA
DDR3(1067M) : 4140mA

Intel check list(Rev 0.8)
No description for VCC_SM bulk CAP
Intel CRB(Rev 0.7)
330U*1 Reserve near to power
330U*1 near to NB

Intel check list(Rev 0.8)
270U*1 near to power(+V1.05M).
270U*2 near to NB
Intel CRB(Rev 0.7)
270U*3 near to power(+V1.05M).
270U*1 near to NB
ESR=12m ohm

+VDR_SUS
C247 22u/6.3V_8
C217 22u/6.3V_8
C218 .1u/10V_4
C539 330u/2V_7343

U26G
VCC_SM_1 … VCC_SM_42
VCC_SM_36/NC … VCC_SM_42/NC
POWER
VCC SM

+1.05V_AXG
VCC_AXG_NCTF_1 … VCC_AXG_NCTF_60
VCC GFX NCTF

1.05V
Graphics core
VCC_AXG
VCC_AXG_NCTF
6326.84mA

+1.05V_AXG
VCC_AXG_1 … VCC_AXG_42
VCC GFX

Voltage regulator is shared between the Graphics Core Rail, VCCA_HPLL,VCCA_MPLL,VCCA_PEG_PLL,VCCD_PEG_PLL, VCCA_SM_CK, VCCA_DPLLA, VCCA_DPLLB, VCCD_HPLL, VCCA_SM, VCC_AXF

IV@
+1.05V_AXG
Differential routing
<35> GFX_VCCSENSE
<35> GFX_VSSSENSE
R114 I@10/F_4
R110 I@10/F_4
AJ14 VCC_AXG_SENSE
AH14 VSS_AXG_SENSE

1. Route VCC_AXG_SENSE and VSS_AXG_SENSE differentially
2. VCC_AXG_SENSE PU to +VGFX_CORE_INT with 10ohm and VSS_AXG_SENSE PD with 10ohm for Intel suggest

SP@CANTIGA_PM

1.8V
Internal connect to power
VCC_SM_LF1 … VCC_SM_LF7
VCC SM LF
C240 .1u/10V_4
C206 .1u/10V_4
C233 .22u/6.3V_4
C228 .22u/6.3V_4
C204 .47u/6.3V_4
C242 1u/10V_4
C236 1u/10V_4

+1.05V
C190 .1u/10V_4
C210 .22u/6.3V_4
C212 .22u/6.3V_4
C161 22u/6.3V_8
C188 330u/2V_7343
Place close to the GMCH

U26F
VCC_1 … VCC_35
VCC CORE
POWER
VCC NCTF
VCC_NCTF_1 … VCC_NCTF_44

+1.05V
+1.05V_AXG
+1.05V_AXG_POWER
IV@
R357 I@0 8
R346 I@0 8
R353 I@0 8
R345 *0 8
R343 *0 8
R344 *0 8

IV&EV Dis/Enable setting
Design guide(Table 72)
For INT VGA diasble.VCC_AXG power can connect to GND

+1.05V_AXG
+C189 I@330u/2V_7343
+C504 I@330u/2V_7343
C177 I@.47u/6.3V_4
SP@
C187 SP@1u/10V_6
C181 I@10u/6.3V_8
C176 I@22u/6.3V_8
C183 I@.1u/10V_4
C179 I@.1u/10V_4
C178 I@.1u/10V_4
Place close to the GMCH
SP@IV Sutff 1uf
EVstuff 0 ohm
Cavity Capacitors

Intel check list(Rev 0.8)
220U*2 near to NB(ESR=15m ohm)
Intel CRB(Rev 0.7)
270U*4 near to power(+V1.05S).
330U*2 near to NB

SP@CANTIGA_PM

VCC
VCC_NCTF
1210.34mA_EV
1930.4mA_IV
ME Engine
508.12mA
Total Max=2438.52mA

GMCH (CANTIGA)

Quanta Computer Inc.
PROJECT : ZK6
Size | Document Number: GMCH VCC,NCTF | Rev 1A
Date: Friday, April 24, 2009 | Sheet 9 of 42

Power consumption reference to Intel Cantiga chipset EDS Volume1. Section 10

IV@
EV@
SP@

External Graphics (GMCH Integrated Graphics Disable)

VCCSYNC_CRT	GND
VCCA_CRT_DAC	GND
VCCD_LVDS	GND
VCC_TX_LVDS	GND
VCCA_LVDS	GND
VCCA_TVDAC	GND
VCCD_QDAC	GND
VCCA_DAC_BG	GND
VCC_AXG	GND
VCC_AXG_NCTF	GND

IV&EV Dis/Enable setting
SP@:INT use 0.01U
EXT use 0 ohm

1210 10UH, 10%
0.45A DCR_max = 0.39

1.05V
64.8mA for DPLL_A/B

3.3V
73mA

3.3V
5mA

VCCA_DPLLA/B always keep to +1.05V
(If no use IV dynamic core power)

1.05V
FSB-1067
852mA

ESR= 12m ohm

1.05V
24mA

1.8V
13.2mA

1.5V
414uA

ESR=15 m

1.05V
321.35mA

Check list : 0.1UH
CRB : 0 ohm
1210 0.1 ?H, 20% 1A
DCR max = 78 m

Clock supply(1.5V)
DDR3(1066):149.5mA

ESR = 60 m

1.05V
139.2mA

1.05V
DDR2-800
720mA

1.05V
50mA

3.9 nH, 0.2 nH, 1A
DCR_max=32 m

VCCA_PEG_PLL
+1.25V for Teenah use(100mA)

1210 0.1uH, 20%, 1A,
DCR_max=0.078Ω

0805 1UH , Rdc = 0.14 - 0.26.
Max rated current = 220 mA

3.3V
24.15mA for VCCA_TVA_DAC
39.48mA for VCCA_TVB_DAC
24.15mA for VCCA_TVC_DAC
Total 87.78mA

1.05V
DDR2-800
26mA

IV&EV Dis/Enable setting
SP@:INT use 1000pf
EXT use 0 ohm

0805 100 nH, DCR=160 m

LVDS Transmitter(1.8V)
118.8mA

CRB : 0 ohm
Check list : 2.2nH

FB 180@100 MHz, 25% 1.5A
DCR_max=90 m

3.3V
79mA

IV&EV Dis/Enable setting
SP@:INT use 0.01U
EXT use 0 ohm

3.3V
105.3mA

CRB no 10U
Check list need min 10U~100U for VCCA_TV_DAC

1.5V
50mA

SP@:INT use 0.1U
EXT use 0 ohm

1.05V
1782mA

VCCD_QDAC share to TV and CRT

VCCD_TVDAC always keep 0.1U/0.022U/10U to +1.5V

1.5V
35mA

1.05V
157.2mA

1.05V
456mA

1.5V
48.363mA for CRT
5mA for TV

FB 180@100 MHz, 25% 1.5A
DCR_max=90 m

1.5V
0.5mA

CRB no 10U
Check list need min 10U~100U
for VCCA_QDAC

FB 220 @100 MHz, 25%, 2A

1.05V
50mA

1.05V
Internal connect to power

IV&EV Dis/Enable setting
SP@:INT use 1 U
EXT use 0 ohm

LVDS digital(1.8V)
60.31mA

Power Net Name	Cantiga(V)
VCC_AXG_# VCC_AXG_NCTF_#	1.05V
VCCA_PEG_BG	1.5V
VCCA_DPLLA	1.05V
VCCA_DPLLB	1.05V
VCCA_SM_#	1.05V
VCCA_HPLL	1.05V
VCCA_MPLL	1.05V
VCCA_SM_CK_#	1.05V
VCCA_PEG_PLL	1.05V
VCC_AXF_#	1.05V
VCCD_HPLL	1.05V
VCCD_PEG_PLL	1.05V

GMCH (CANTIGA)

Quanta Computer Inc.
PROJECT : ZK6

Size	Document Number	Rev
	GMCH POWER	1A

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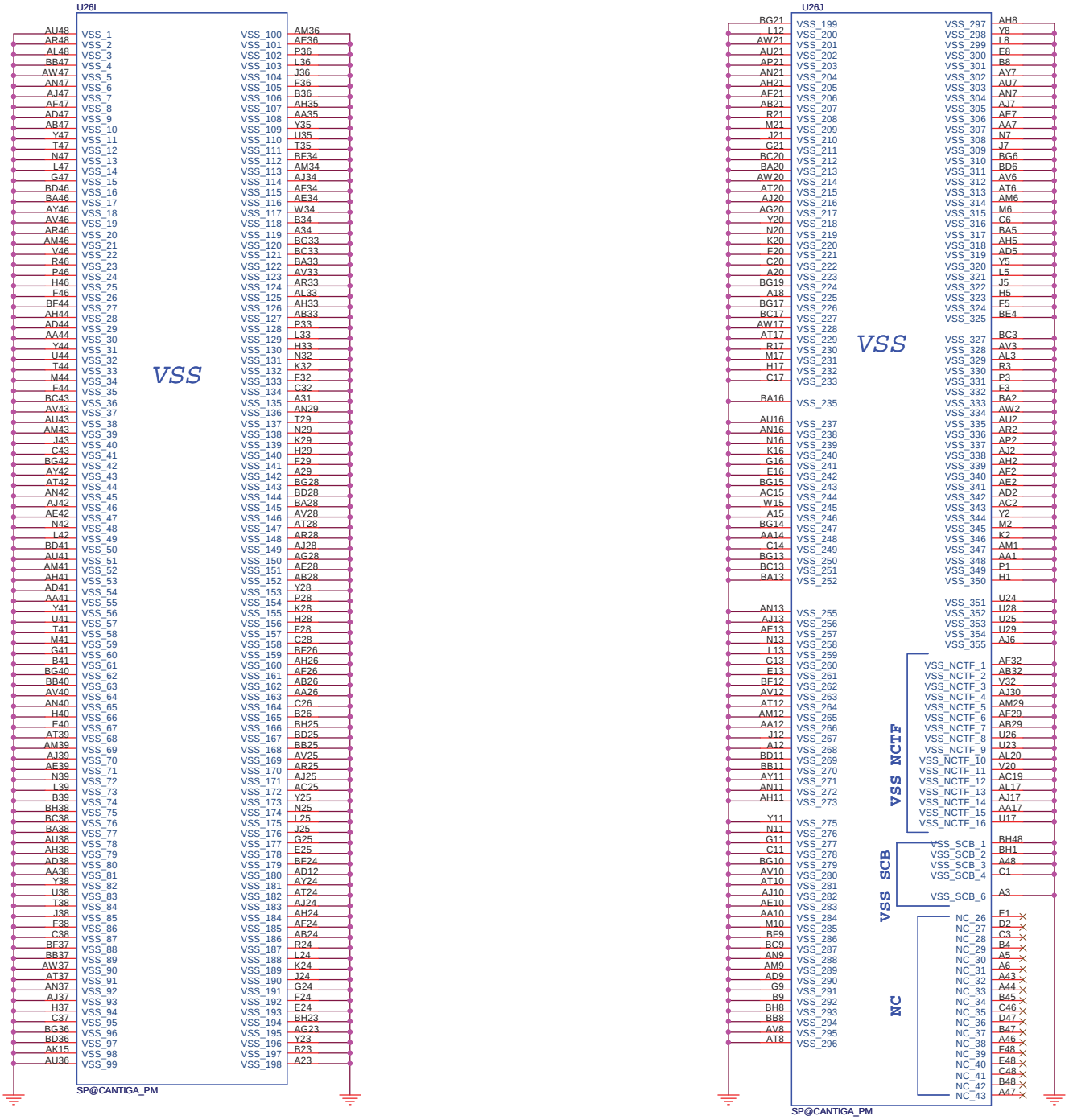

GMCH (CANTIGA)

Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	GMCH VSS	1A
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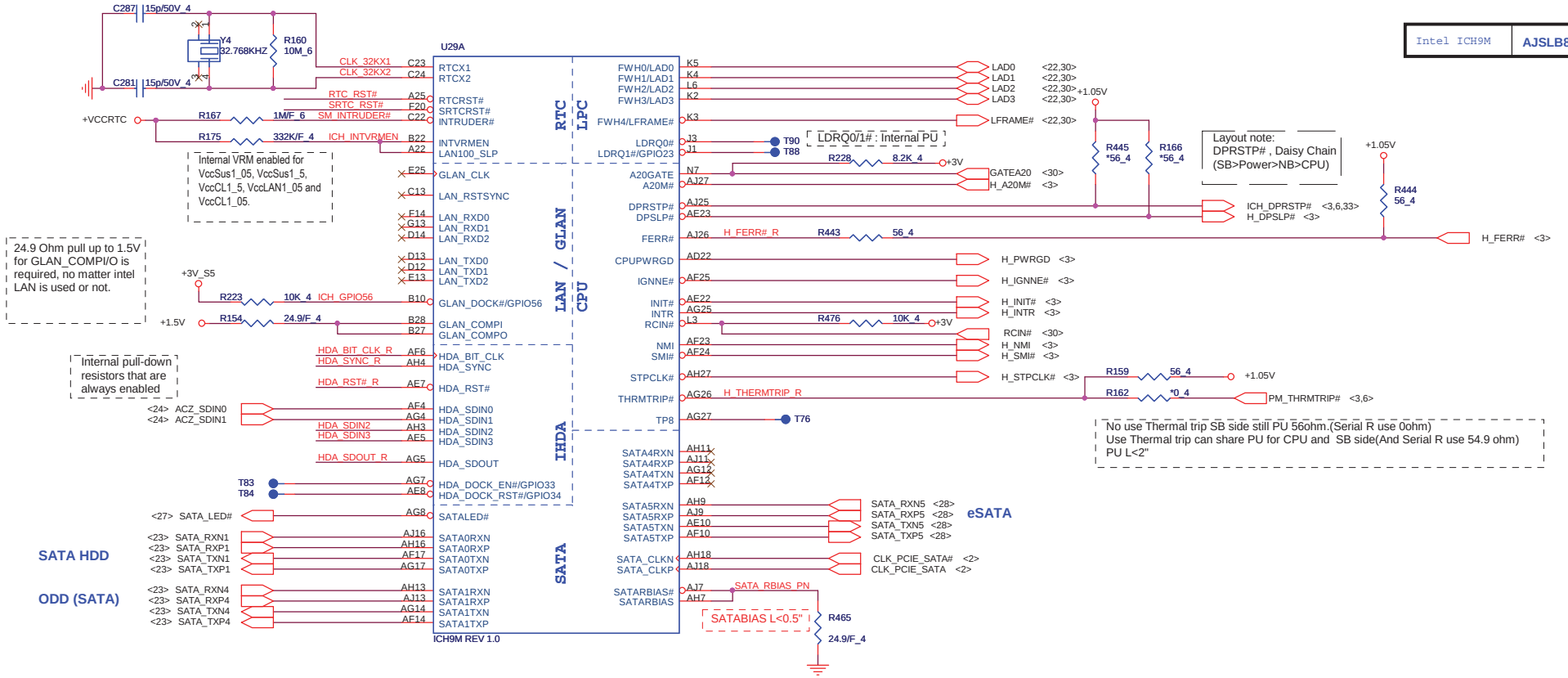
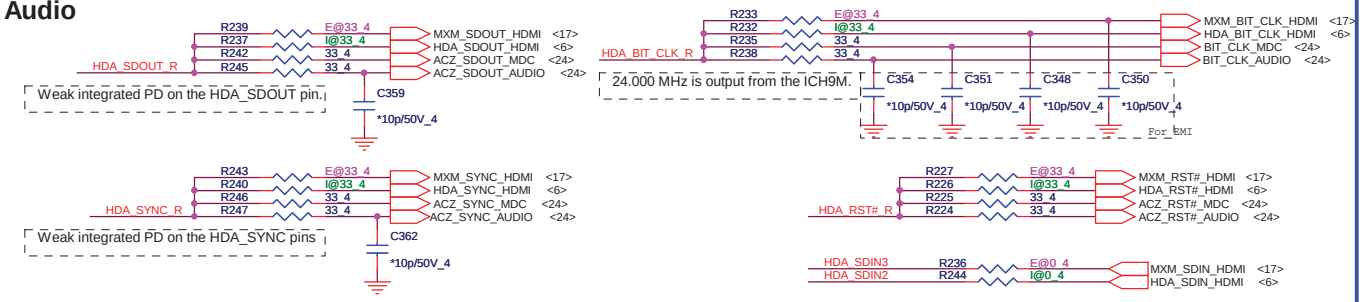
ICH9M
IV@
EV@

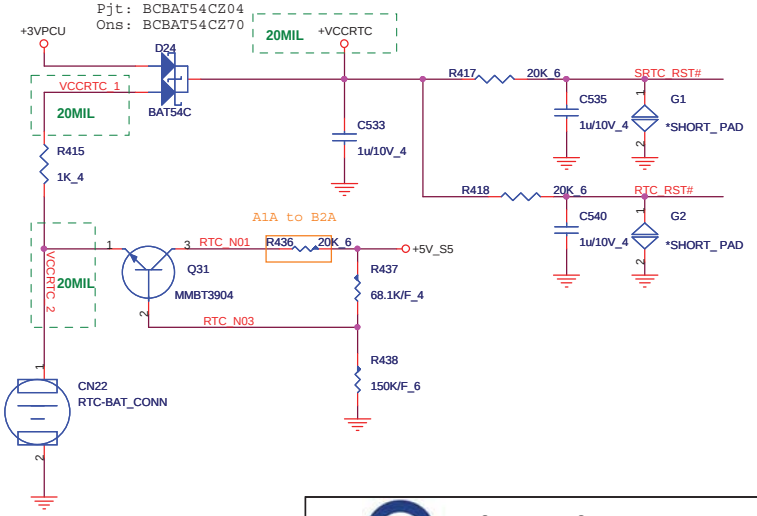
Intel ICH9M | AJSLB8Q0T03



HD Audio



RTC



South Bridge Strap Pin (1/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect	This strap should only be enabled in manufacturing environments using an external pull-up resistor.
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU	
TP3	XOR Chain Entrance	PWROK	ICH_TP3 / HDA_SDOUT: 0/0 RSVD; 0/1 Enter XOR Chain; 1/0 Normal opration(Default); 1/1 Set PCIE port config bit	<14> ICH_TP3 — ICH_TP3 — R182 *1K_4
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK		HDA_SDOUT_R — R234 *1K_4 — +3V

Quanta Computer Inc.
PROJECT : ZK6

Size	Document Number	Rev
	ICH9M HOST	1A
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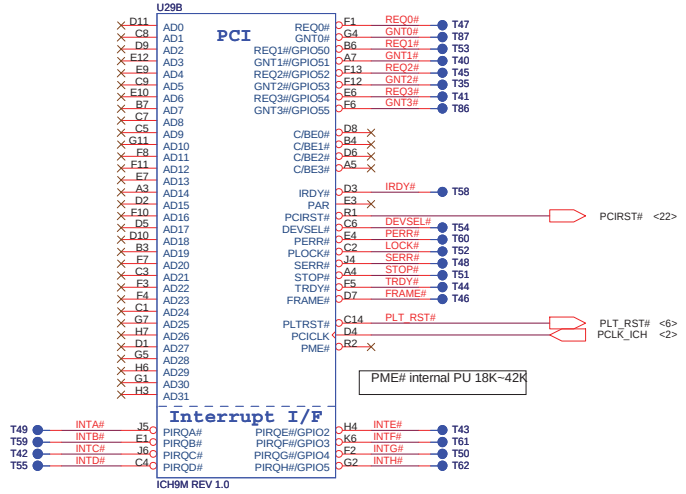
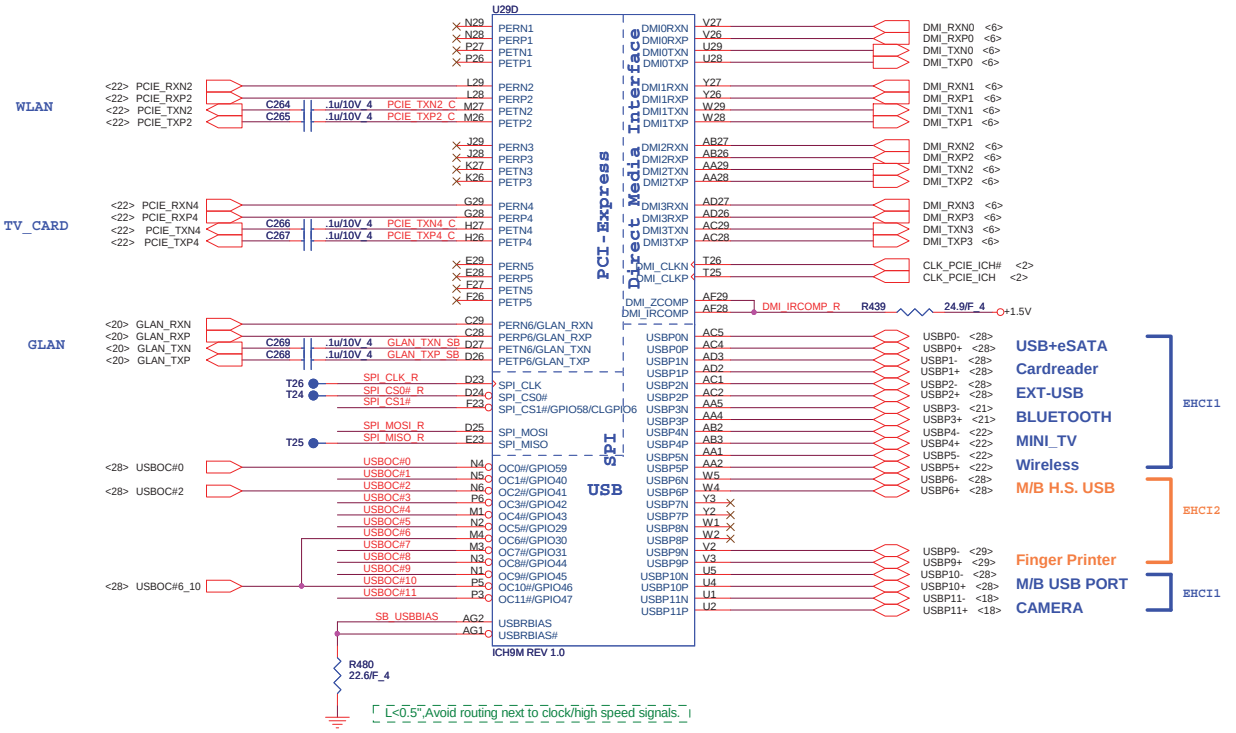
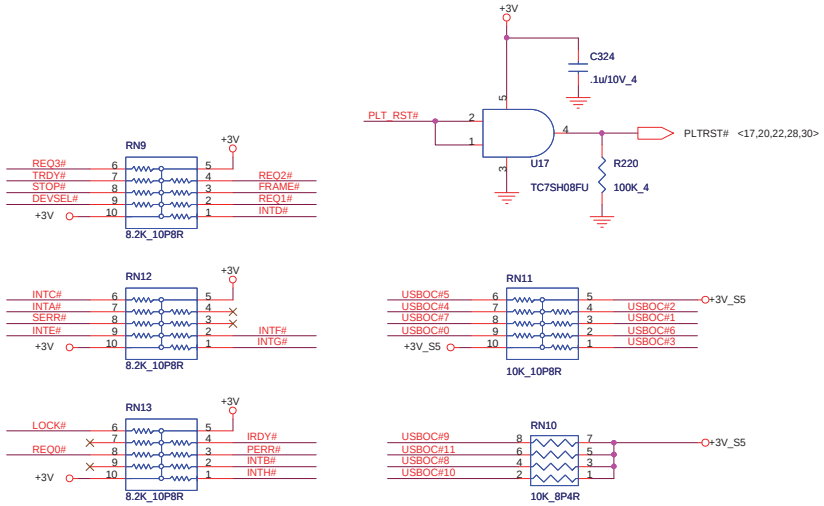
ICH9M







South Bridge Strap Pin (2/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0	
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default	
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default	GNT3# R485 *1K_4
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable	SPI_MOSI_R R156 *10K_4 +3V_S5
GNT0#	Boot BIOS Selection 0	PWROK	PCI_GNT#0 / SPI_CS#1 / Boot Location 0 / 1 / SPI	GNT0# R486 *1K_4
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK	1 / 0 / PCI 1 / 1 / **LPC(Default)**	SPI_CS1# R177 *1K_4

Quanta Computer Inc.
PROJECT : ZK6
Size | Document Number: ICH9M PCIE / PCI / USB | Rev 1A
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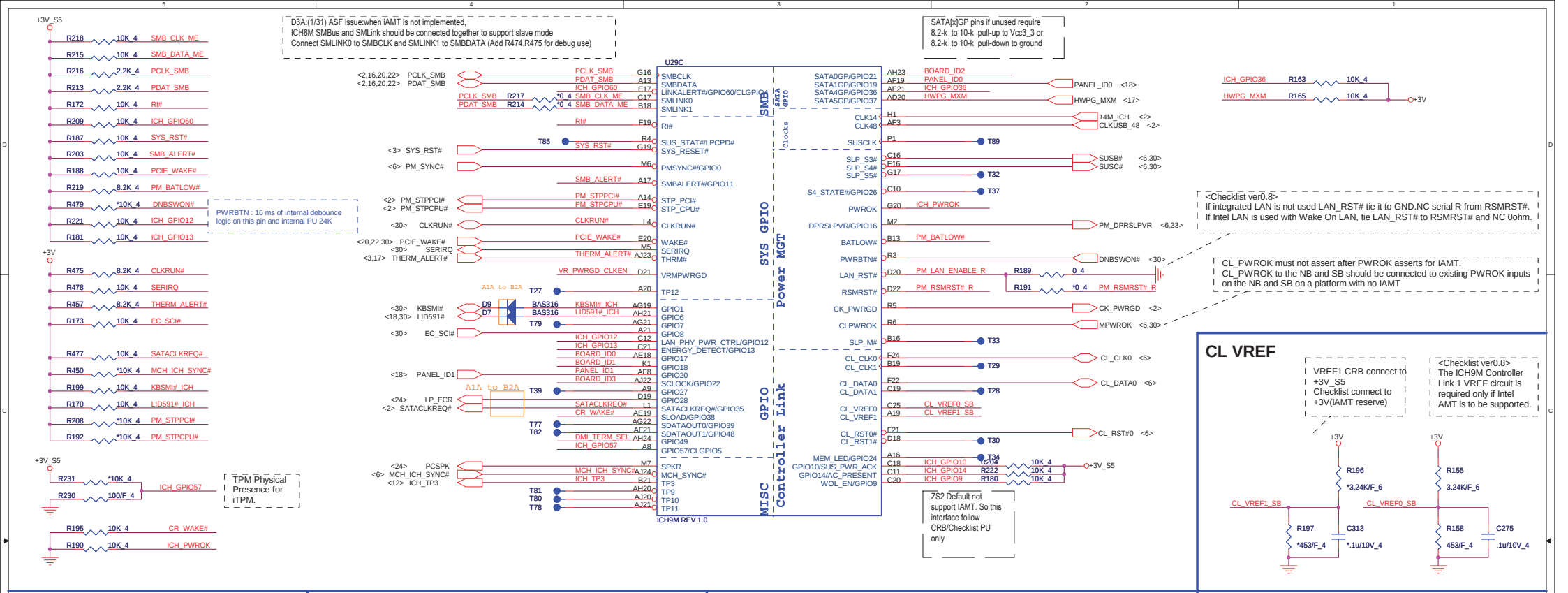
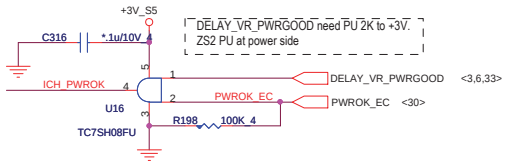
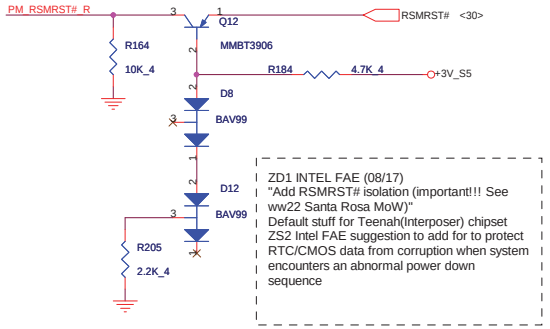


ICH PWROK

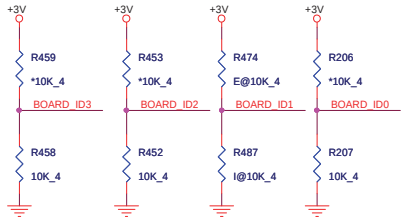


Resume RST



M/B ID

ID0 :: ZK=0 , ZR=1
ID1 :: UMA=0 , MXM=1

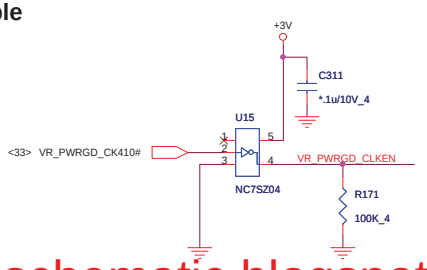


Board ID	ID3	ID2	ID1	ID0
default	0	0	0	0
	0	0	0	1
	0	0	1	0
	0	0	1	1
	0	1	0	0

South Bridge Strap Pin (3/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
SPKR	No Reboot	PWROK	0 = Default 1 = No Reboot mode	PCSPK R229 *1K_4 +3V
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	DMI_TERM_SEL R446 *1K_4

CLK Enable



Quanta Computer Inc.
PROJECT : ZK6
Size | Document Number | ICH9M GPIO | Rev 1A
Date: Friday, April 24, 2009 | Sheet 14 of 42

ICH9M

IV@

EV@

Power consumption reference to Intel ICH9 Family EDS Rev 1.6

2~3.456v 3.6uA_G3

PER INTEL SUGGESTION: CHANGE TO 100OHM & 1UF

5V 2mA

5V S0:2mA S3/4/5:1mA

1.5V 646mA

1.5V 47mA

1.5V 11mA

VCC1_5_A 1.5V 1342mA

1.05V , Powered by VCC1_05 in S0

3.3V S0:19mA S3/4/5:78mA

If use SB MAC for LAN function. And support wake up need connect to relation power.

1.5V 23mA

1.5V 80mA

3.3V 1mA

1.05V 1634mA

1.5V 23mA

1.05V 50mA

1.05V 2mA

3.3V 308mA

VCCSUS1_05 power by VCC1_05 in S0 / VCCSUS3_3 in S3/S4/S5

VCCSUS1_5 power by VCC1_5_A in S0 / VCCSUS3_3 in S3/S4/S5

3.3V S0:212mA S3/4/5:53mA

VCCCL1_05 power by VCC1_05_A in S0

VCCCL1_5 power by VCC1_5_A in S0

3.3V S0:19mA S3/4/5:73mA

If use SB MAC for LAN function. And support wake up need connect to relation power.

Impact ICH9M VCCHDA and VCCSUSHDA supply 1.5V/3.3V

Support INT HDMI HDA interface. These power only support 1.5V.Device must to meet.

NOTE: If (G)MCH's HD Audio signals are connected to ICH9M for iHDMI, VCCHDA and VCCSUSHDA on ICH9M should be only on 1.5V. These power pins on ICH9M can be supplied with 3.3V if and only if (G)MCH's HDA is not connected to ICH9M. Consequently, only 1.5V audio/modem codecs can be used on the platform.

ICH9M REV 1.0

Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	ICH9 POWER	1A

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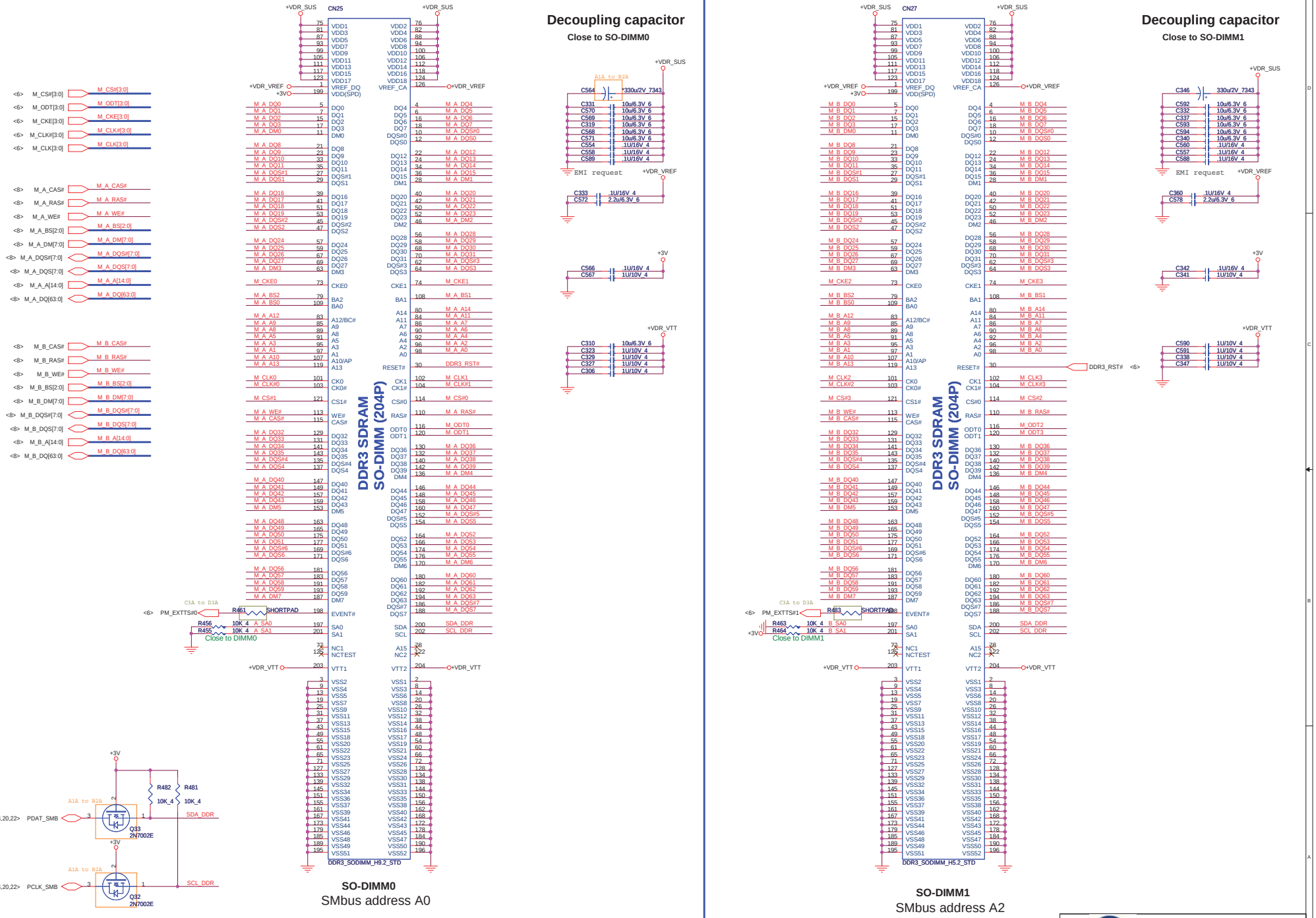
H=9.2mm / DGMK4000058

H=5.2mm / DGMK4000059



Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	DDRIII SO-DIMM	1A

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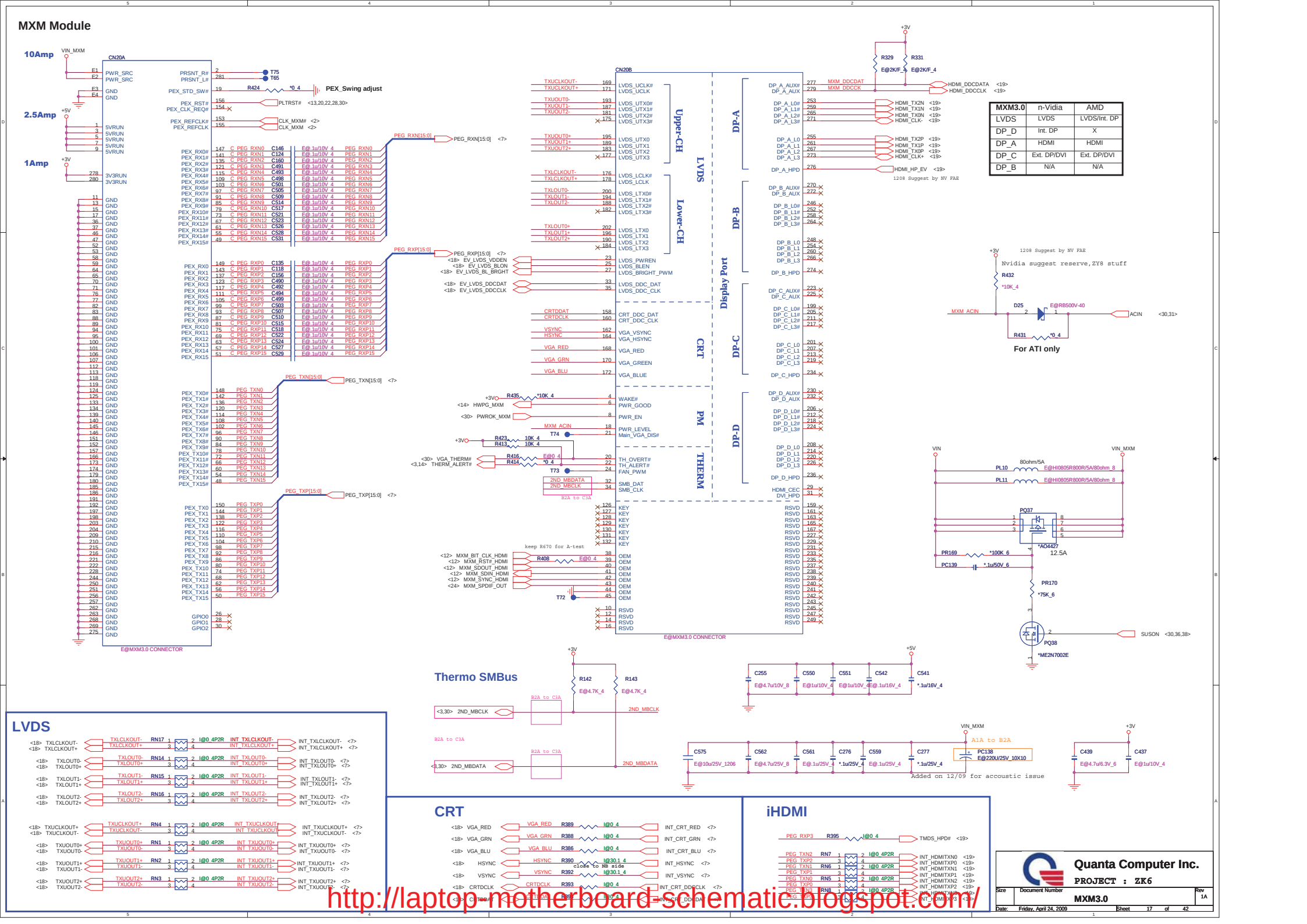
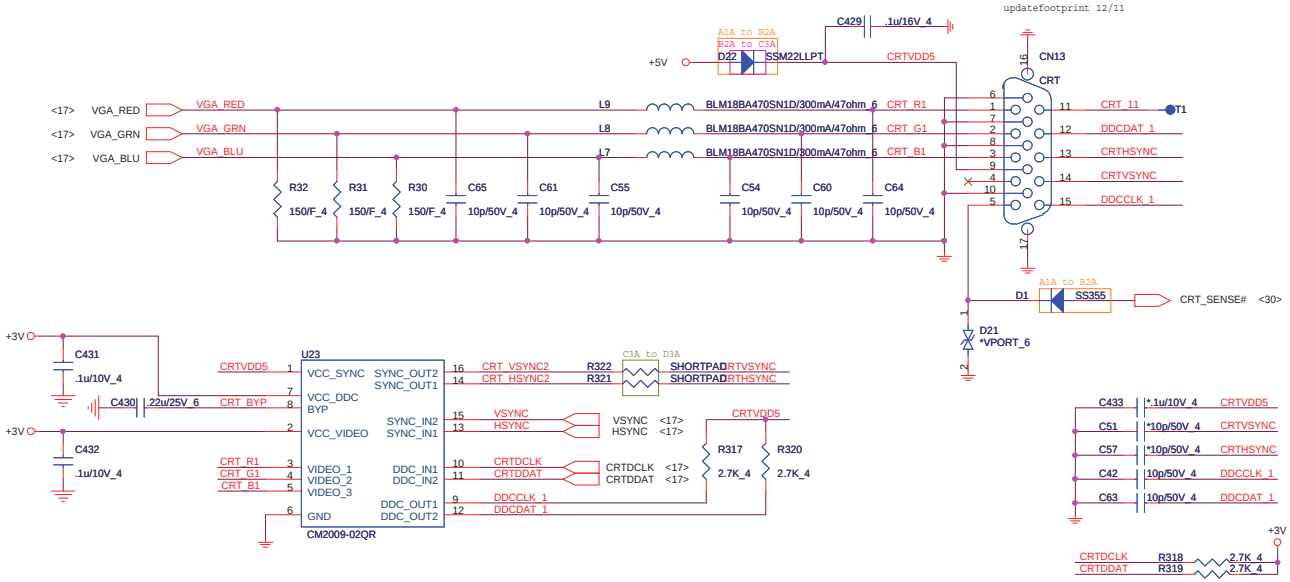
MXM Module



MXM3.0	n-Vidia	AMD
LVDS	LVDS	LVDS/Int. DP
DP_D	Int. DP	X
DP_A	HDMI	HDMI
DP_C	Ext. DP/DVI	Ext. DP/DVI
DP_B	N/A	N/A

CRT

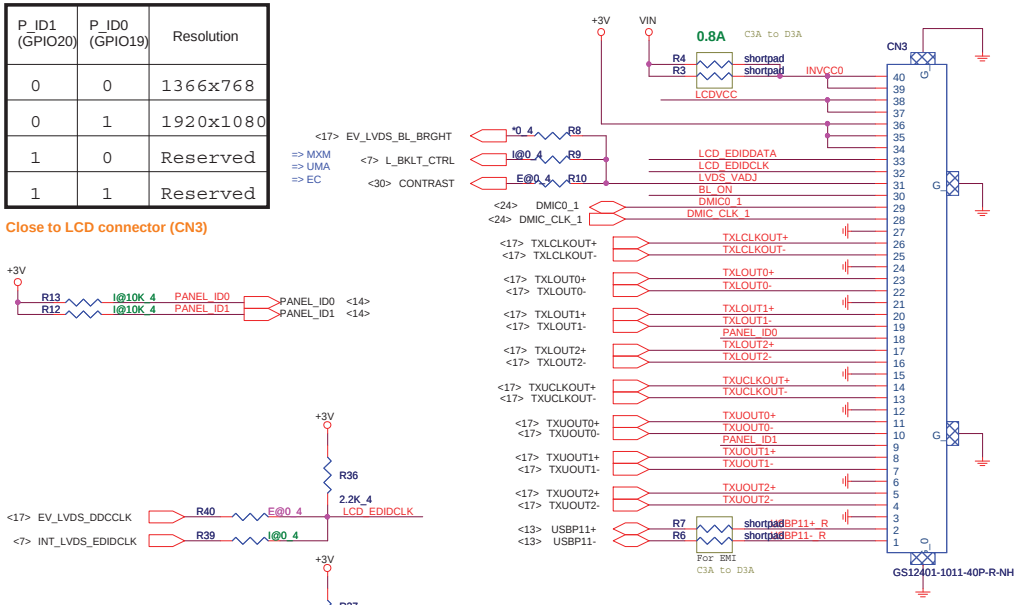
IV@
EV@



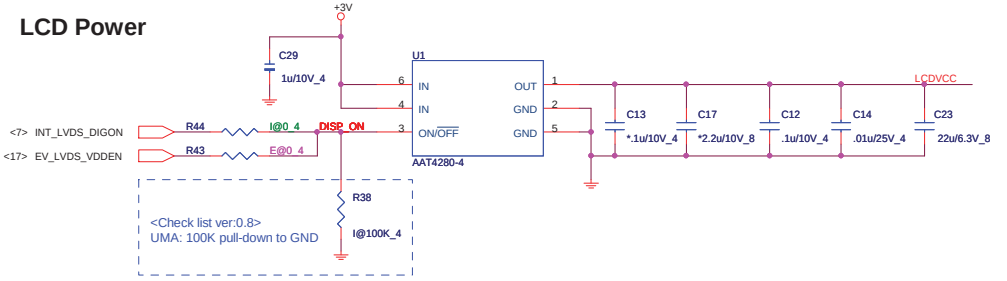
LVDS Panel ID (UMA only)

P_ID1 (GPIO20)	P_ID0 (GPIO19)	Resolution
0	0	1366x768
0	1	1920x1080
1	0	Reserved
1	1	Reserved

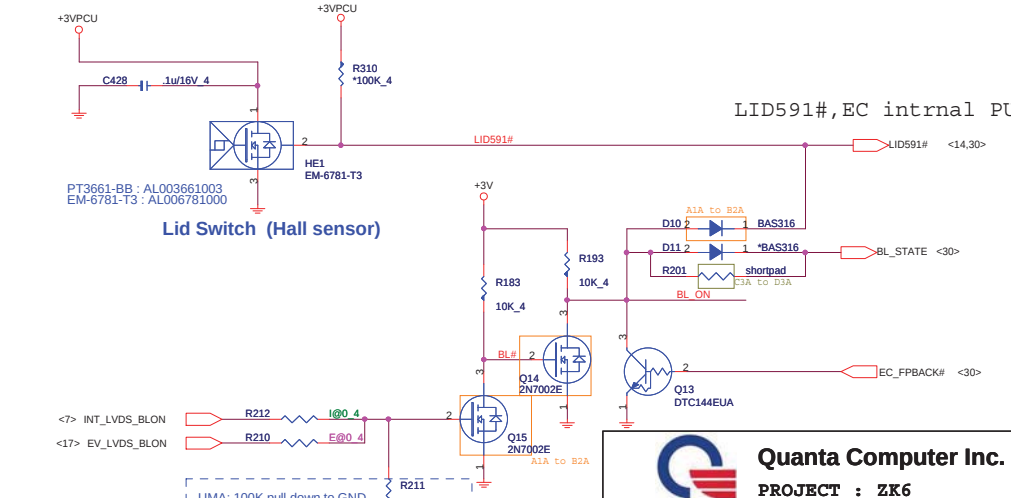
Close to LCD connector (CN3)



LCD Power



Backlight Control & LID



Quanta Computer Inc.
PROJECT : ZK6

Size	Document Number	Rev
	CRT/LVDS/CAMERA/LID	1A
Date: Friday, April 24, 2009	Sheet 18 of 42	

I@ HDMI LEVEL SHIFTER

CH7318C :: AL007318002
PS8101T :: AL008101001

IV@
EV@
SP@

I@HDMI-detect

To GMCH
<17> TMDS_HPD#
Voltage level 0.9V

R330 *20K/F_6
R338 I@0_4
Q24 *RHU002N06
R328 *7.5K/F_4
R337 *100K_4
Control by pin4 HPDEN_R
HDMI_HP_SW#

To GMCH
<6> SDVO_CTRLDATA
<6> SDVO_CTRLCLK
R377 I@0_4 HDMI_DDCDATA_SW
R378 I@0_4 HDMI_DDCCLK_SW

C459 I@2.2u/6.3V_6
C84 I@.1u/16V_4
C80 I@.1u/16V_4
C94 I@.1u/16V_4
C441 I@.1u/16V_4

R374 I@4.7K_4 TRIM_R
R373 *4.7K_4
R375 *4.7K_4 HPDEN_R
R350 *4.7K_4 CCT1_R
R349 *4.7K_4
R347 *4.7K_4 CCT2_R
R348 *4.7K_4

R351 I@4.7K_4
CCT1_R
CCT2_R
Active Buffer

HDMI_MB_HP
MB_HDMI_DDCDATA
MB_HDMI_DDCCLK
HDMI_OE#

PC0 PIN3
PC1 PIN4

From GMCH
<17> INT_HDMITXN3
<17> INT_HDMITXP3
<17> INT_HDMITXN0
<17> INT_HDMITXP0
<17> INT_HDMITXN1
<17> INT_HDMITXP1
<17> INT_HDMITXN2
<17> INT_HDMITXP2

U24
GND IN_D1- IN_D1+ VCC IN_D2- IN_D2+ GND IN_D3- IN_D3+ VCC IN_D4- IN_D4+ GND
GND OUT_D1- OUT_D1+ VCC OUT_D2- OUT_D2+ GND OUT_D3- OUT_D3+ VCC OUT_D4- OUT_D4+
MB_HDMICLK- MB_HDMICLK+ MB_HDMITX0N MB_HDMITX0P MB_HDMITX1N MB_HDMITX1P MB_HDMITX2N MB_HDMITX2P
I@PS8101T

TRIM_R
HPDEN_R
R376 I@499/F_4
A1A to B2A
LS REXT

OE# control for power saving
R352 I@10K_4
HDMI_OE#
Q25 I@2N7002E
HDMI_MB_HP

Equalization Control

PC1 PIN4	PC0 PIN3	EQ Control
L	L	8dB
L	H	4dB
H	L	12dB
H	H	0dB

E@HDMI-detect

To MXM
HDMI_HP_EV <17>
R45 E@10K_4
R48 E@10K_4
HP_EV
Q5 E@2N7002E
HDMI_MB_HP
Q6 E@2N7002E
A1A to B2A

Switch I2C E@ or I@

NV suggestion near HDMI connector

To MXM
<17> HDMI_DDCCLK
Q4 E@2N7002E
R35 *0_4
D3 RB501V-40
R34 1.5K_4
MB_HDMI_DDCCLK
L11 SP@BLM18AG601/200mA/600ohm_6
HDMI_DDCCLK_MB
C72 *.1u/10V_4

To MXM
<17> HDMI_DDCDATA
Q23 E@2N7002
R336 *0_4
D2 RB501V-40
R33 1.5K_4
MB_HDMI_DDCDATA
L10 SP@BLM18AG601/200mA/600ohm_6
HDMI_DDCDATA_MB
C71 *.1u/10V_4

Switch E@ or I@

To MXM
<17> HDMI_TX0N
<17> HDMI_TX0P
<17> HDMI_TX2N
<17> HDMI_TX2P
<17> HDMI_TX1P
<17> HDMI_TX1N
<17> HDMI_CLK+
<17> HDMI_CLK-
C79 C81 C85 C88 C83 C82 C78 C77 E@.1u/10V_4

MB_HDMITX0N MB_HDMITX0P MB_HDMITX2N MB_HDMITX2P MB_HDMITX1P MB_HDMITX1N MB_HDMICLK+ MB_HDMICLK-

R355 R356 R361 R365 R369 R367 R360 R358 E@499/F_4

R381 E@100K_4 Q30 E@2N7002E

ESD Protect

U7 *RClamp0524P
U6 *RClamp0524P
U5 *RClamp0524P
GND_3/8

HDMI_DDCCLK_MB
HDMI_DDCDATA_MB
HDMI_MB_HP

EMI

R529 R530 R531 R532 *100/F_4

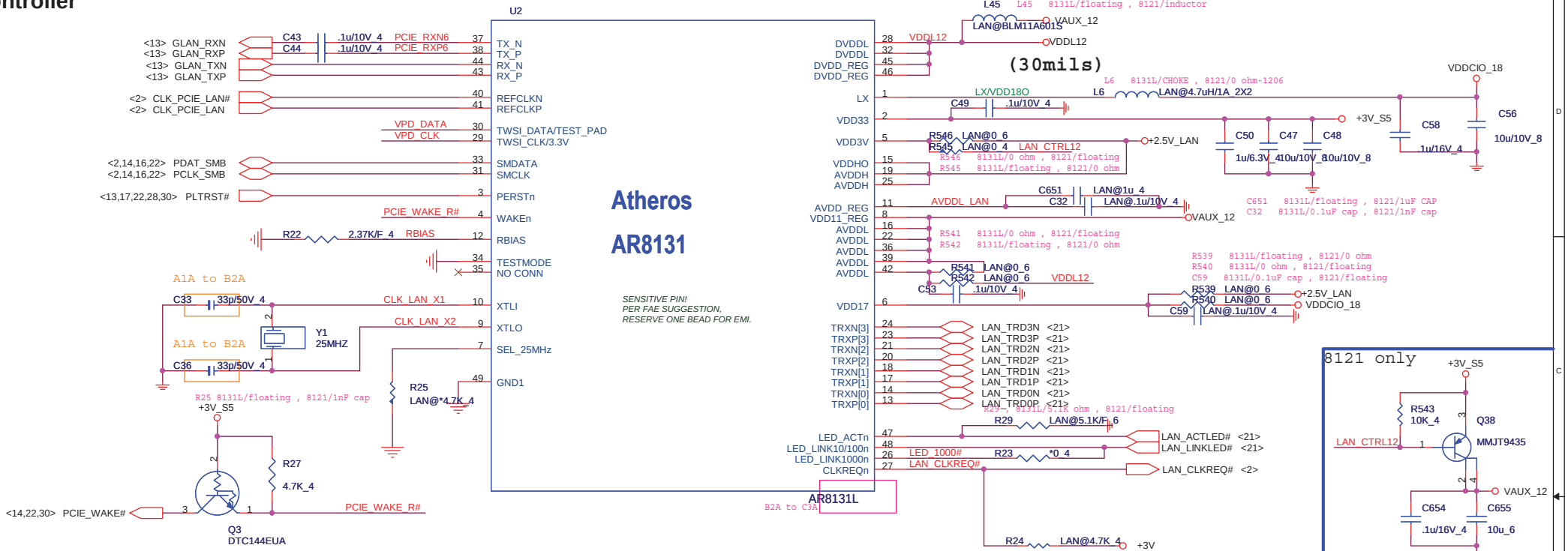
R55 *10K_4
D23 SSM22LLPT
C70 .1u/16V_4
R54 SHORTPAD
R50 *10K_4
HDMI_MB_HP
C3A to D3A
A1A to B2A
B2A to C3A

HDMI connector

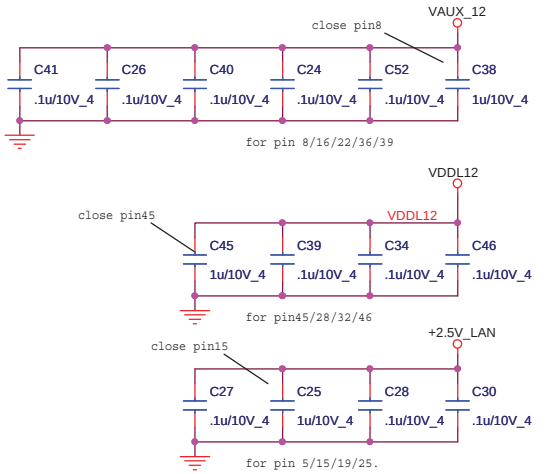
CN17 HDMI
SHELL1 SHELL2 GND GND
D2+ D2 Shield D2- D1+ D1 Shield D1- D0+ D0 Shield D0- CK+ CK Shield CK- CE Remote NC DDC CLK DDC DATA GND +5V HP DET

Quanta Computer Inc.
PROJECT : ZK6
Size | Document Number: HDMI (CH7318C) | Rev 1A
Date: Friday, April 24, 2009 | Sheet 19 of 42

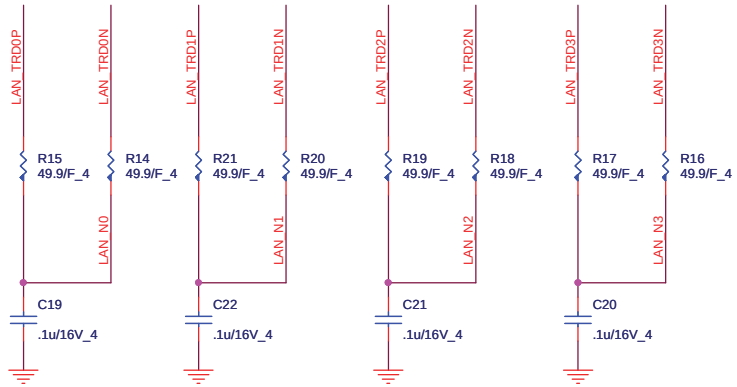
LAN Controller



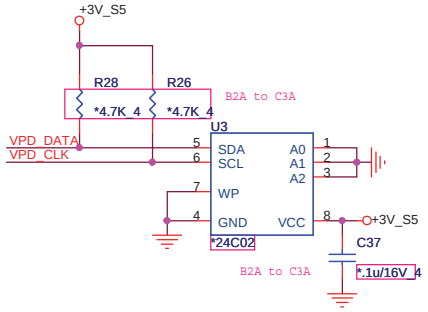
Decoupling CAP



PLACE NEAR IC SIDE



EEPROM



Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	AR8131 GLAN	1A

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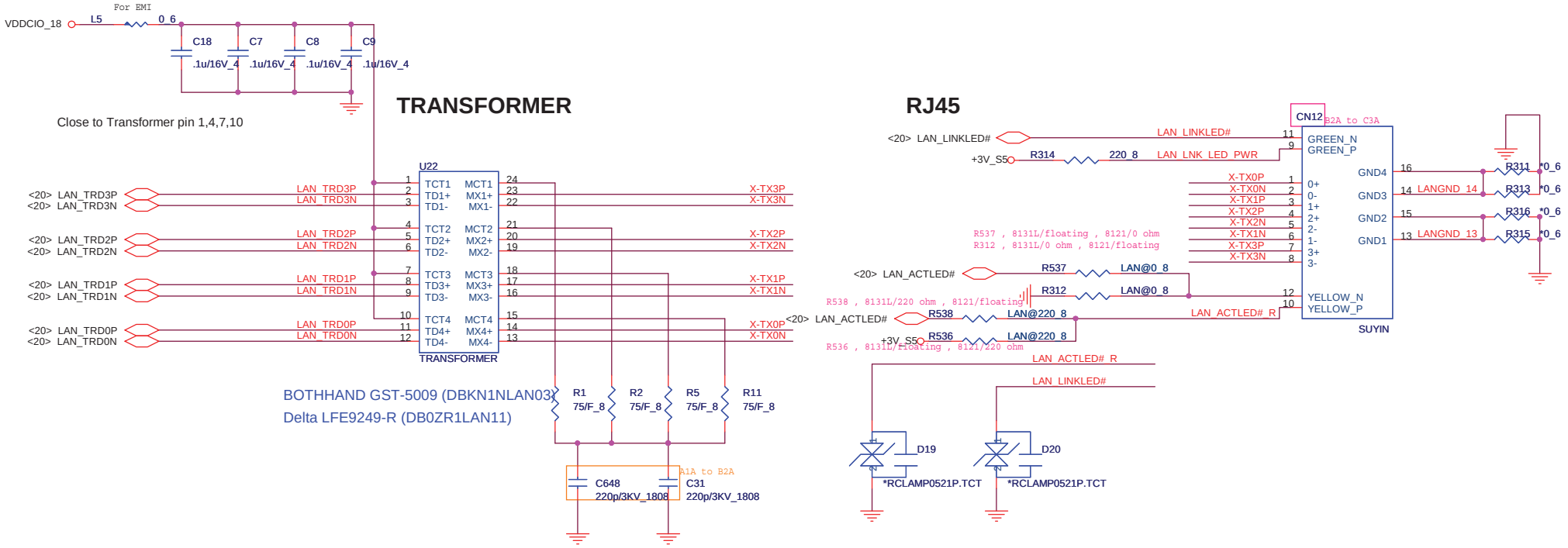
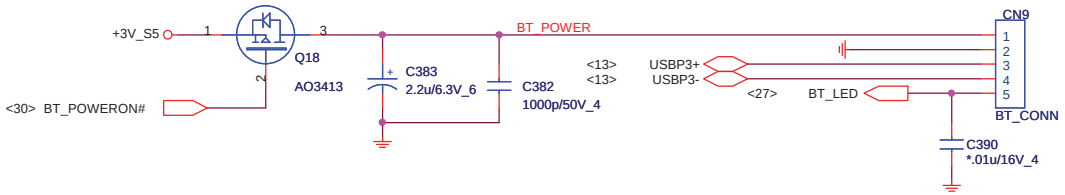


BLUETOOTH CONNECTOR

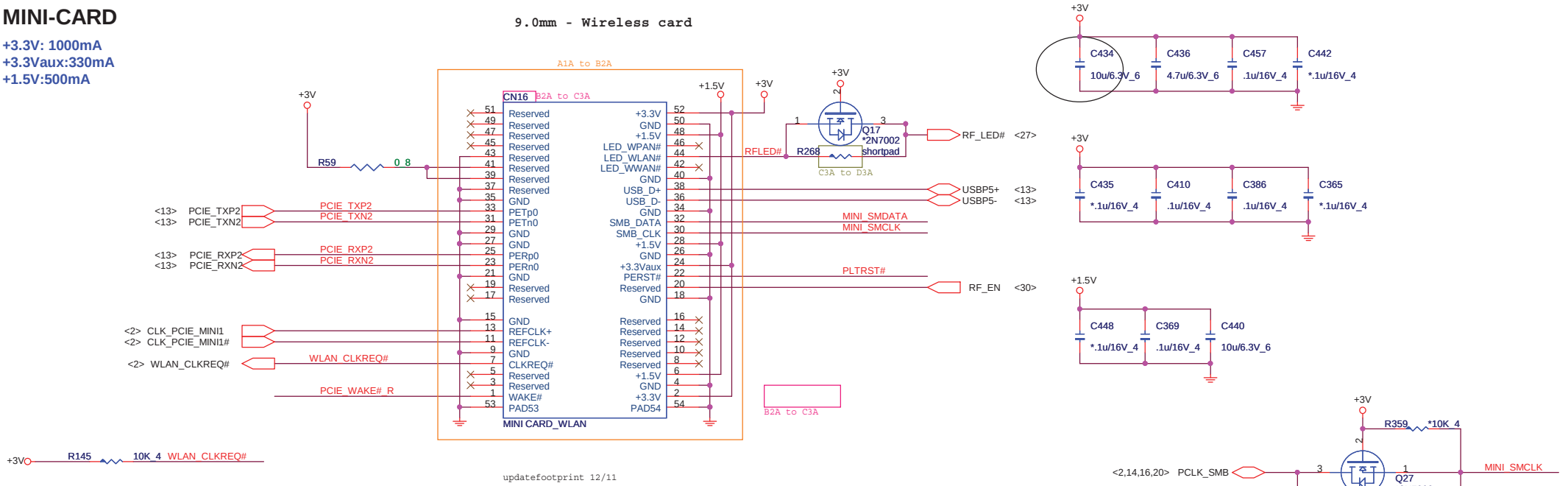


Quanta Computer Inc.		
PROJECT : ZK6		
Size	Document Number: LAN Transformer and RJ45/BT	Rev 1A
Date: Friday, April 24, 2009	Sheet 21 of 42	

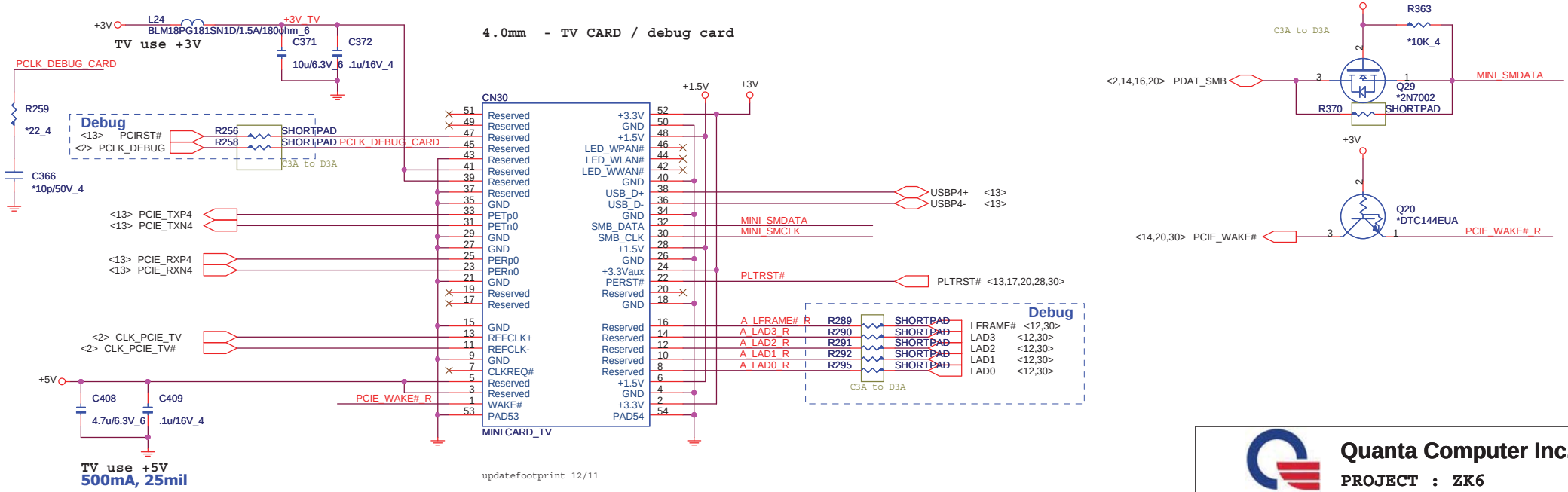
MINI-CARD

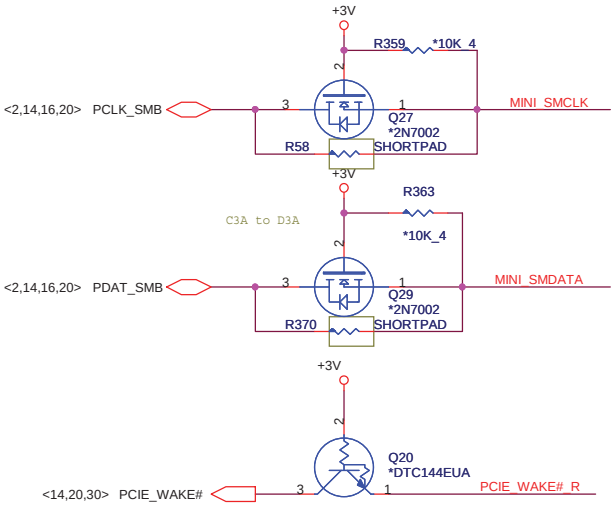
+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

9.0mm - Wireless card



4.0mm - TV CARD / debug card





Quanta Computer Inc.			
PROJECT : ZK6			
Size	Document Number		Rev
	MINI PCI-E card/TV		1A
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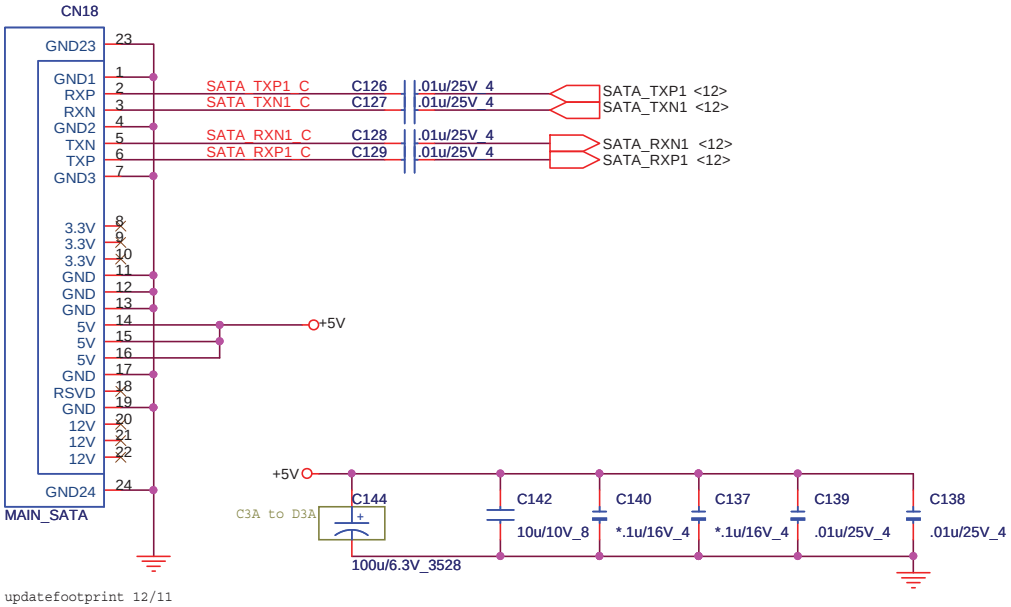
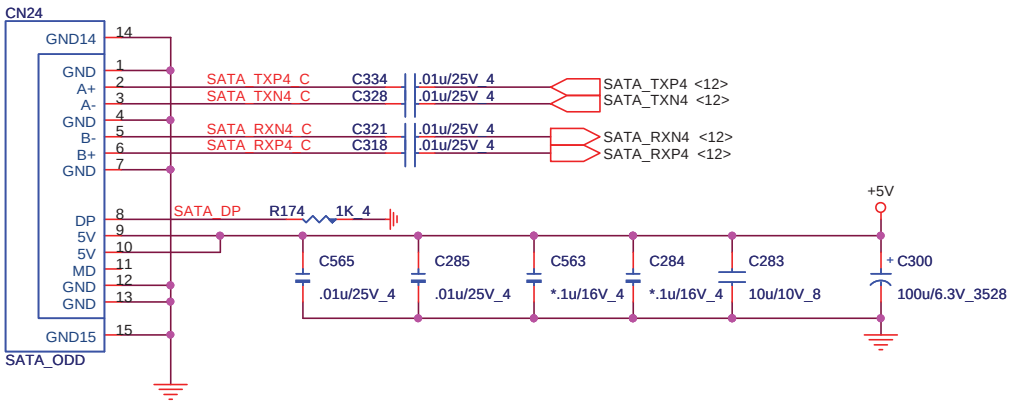
MAIN SATA HDD



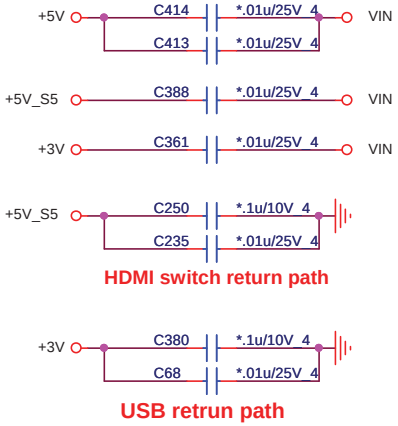
updatefootprint 12/11

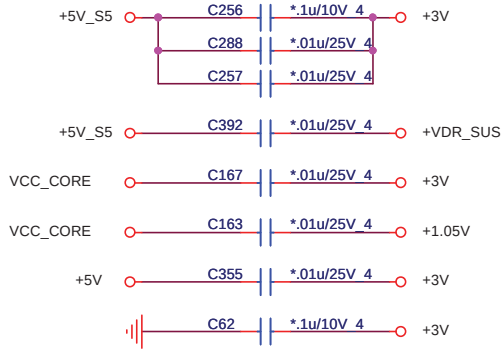
ODD (SATA)

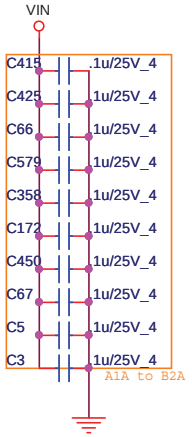


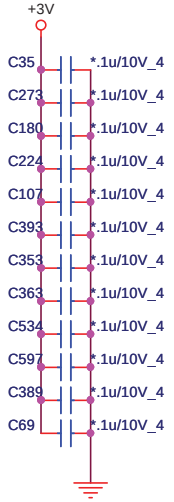
updatefootprint 12/11

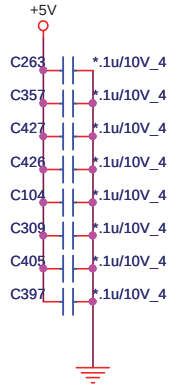
EE RETURN-PATH CAPACITORS











Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	SATA-HDD/ODD/USB-ESATA	1A
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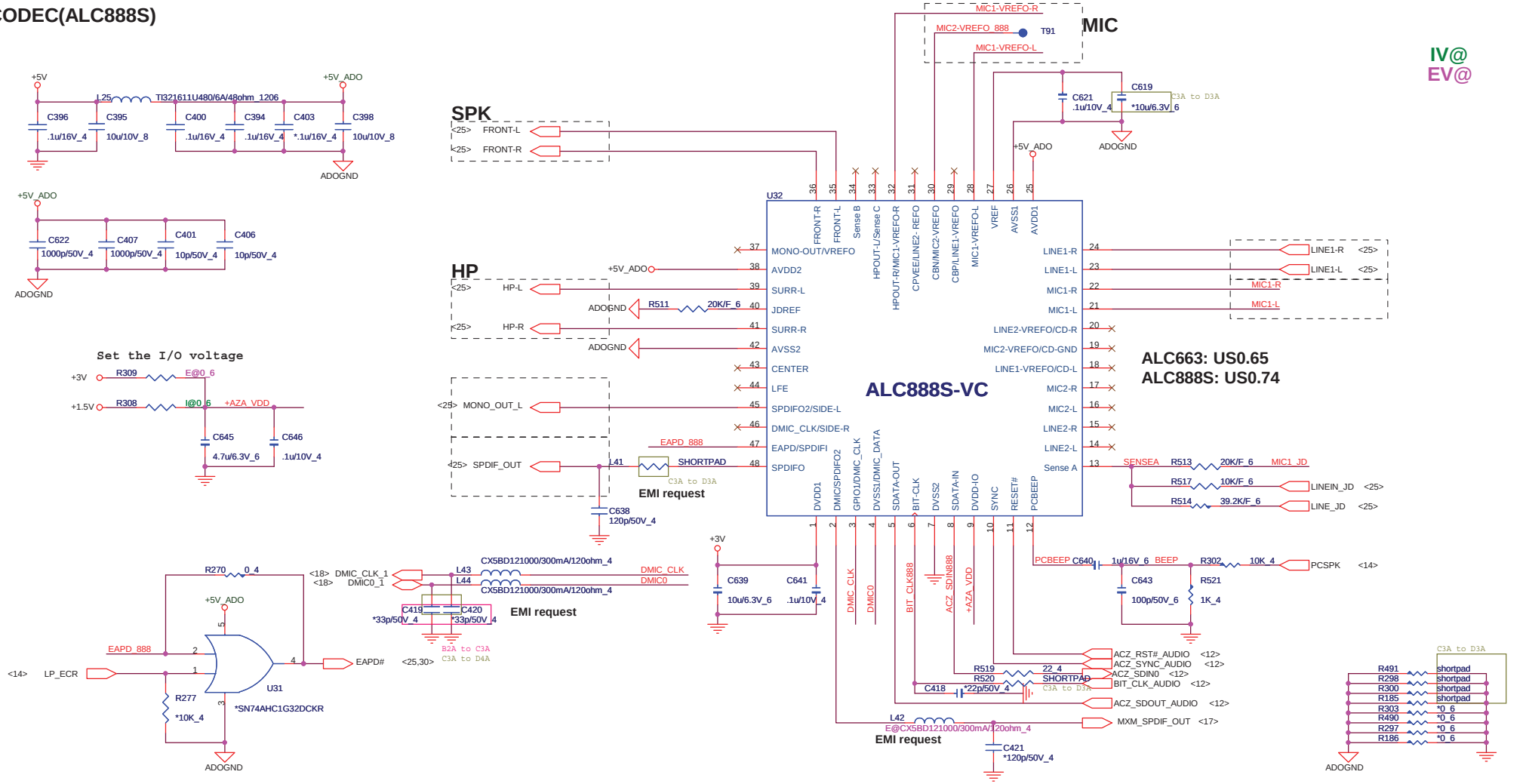
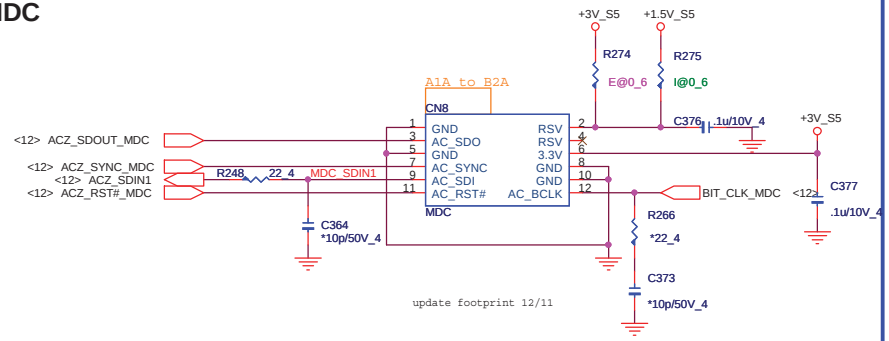
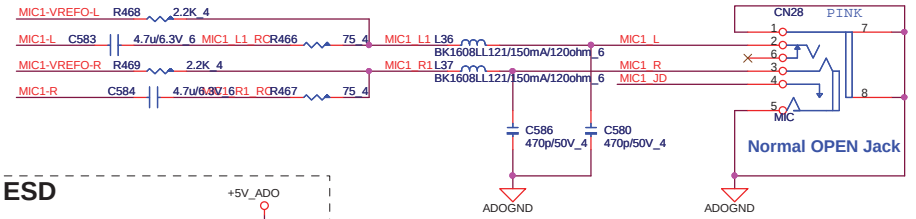
CODEC(ALC888S)



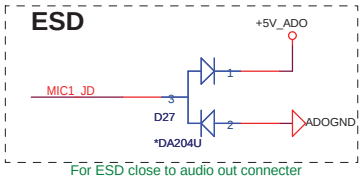
MDC



MIC



ESD



CODEC & MDC

Quanta Computer Inc.		
PROJECT : ZK6		
Size	Document Number: REALTEK ALC663&888/MDC	Rev: 1A
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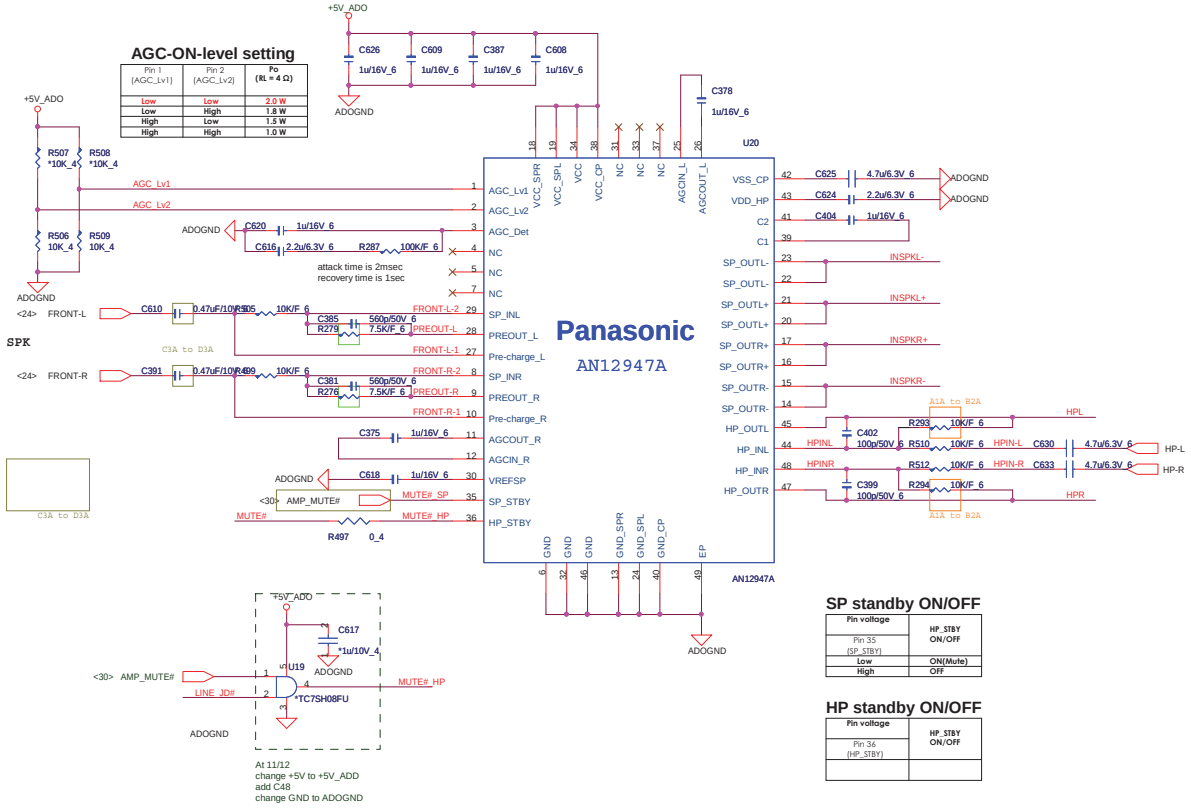
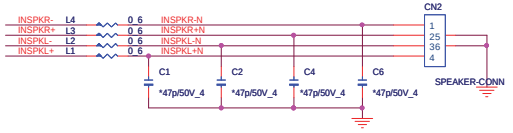
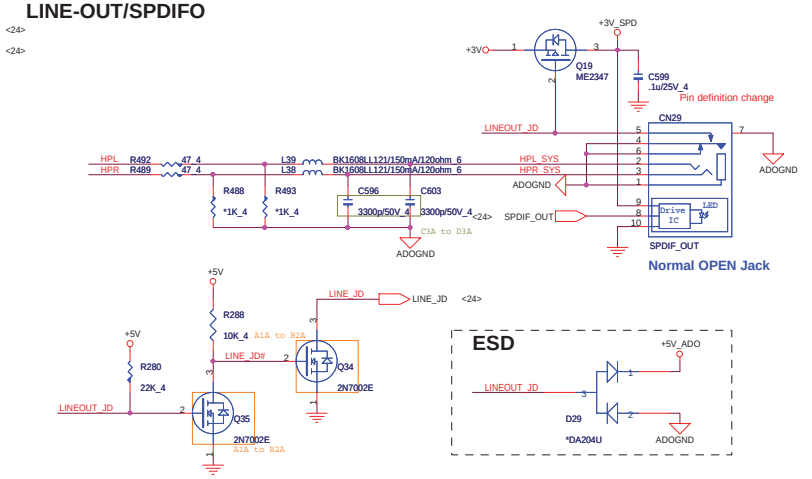
SPEAKER/HP AMP.



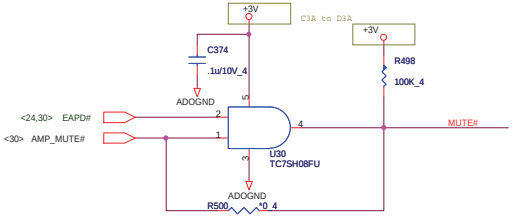
SPEAKER



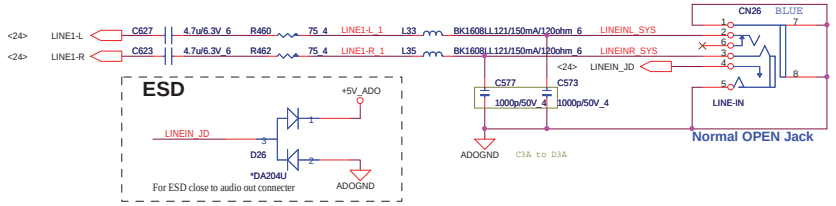
LINE-OUT/SPDIFO



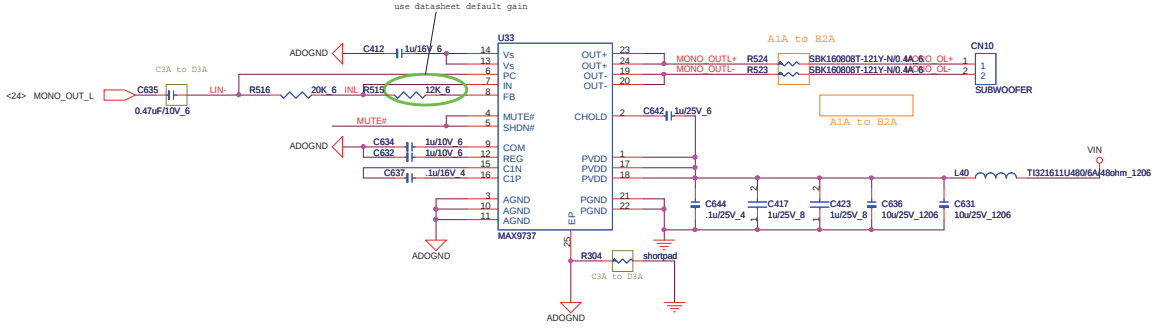
MUTE



LINE IN



SUBWOOFER



AMP& PHONE JACK & SUBWOOFER

Quanta Computer Inc.
PROJECT : ZK6
Size | Document Number | Rev 1A
AMP /AUDIO JACK CONN
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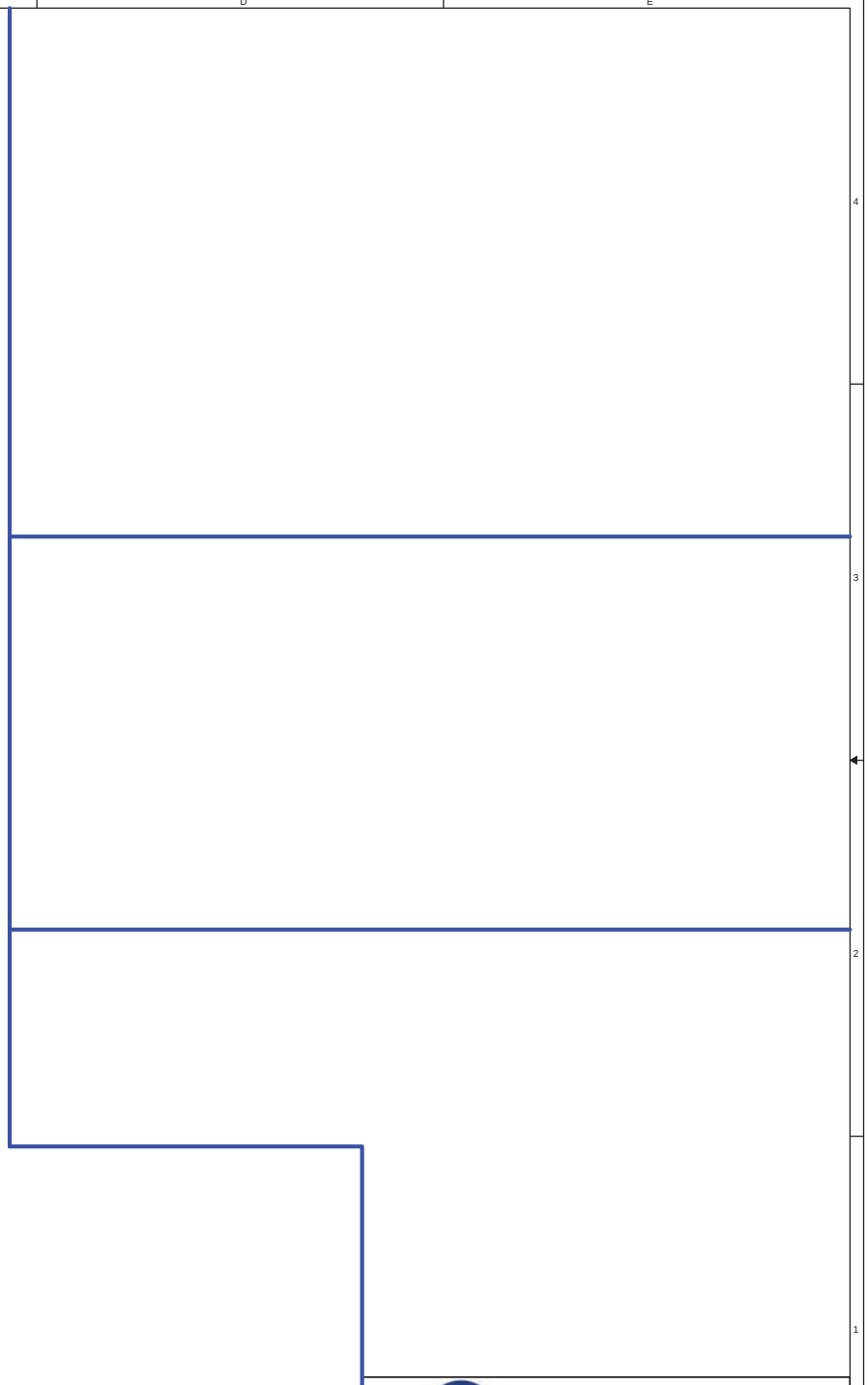

Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	CARD READER RTS5159	1A

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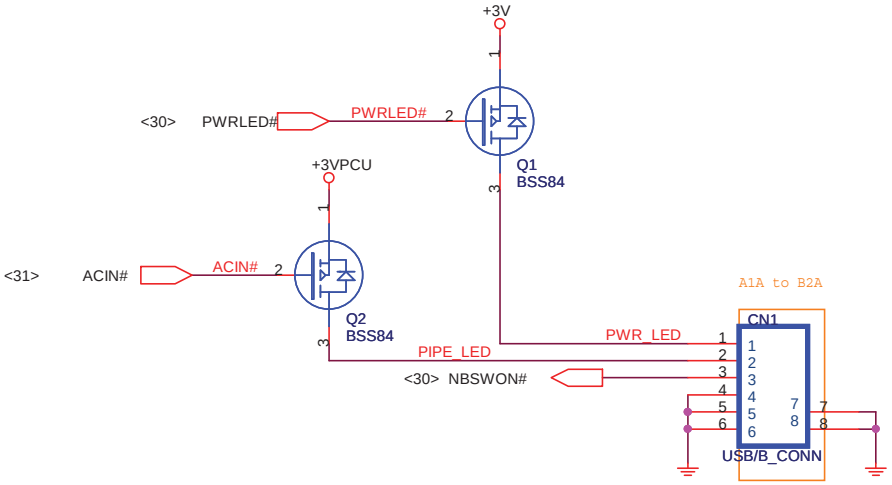
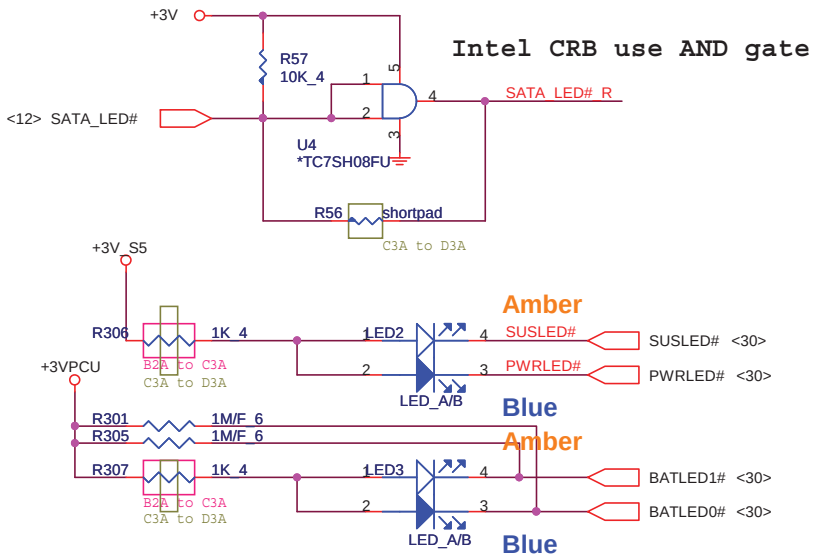
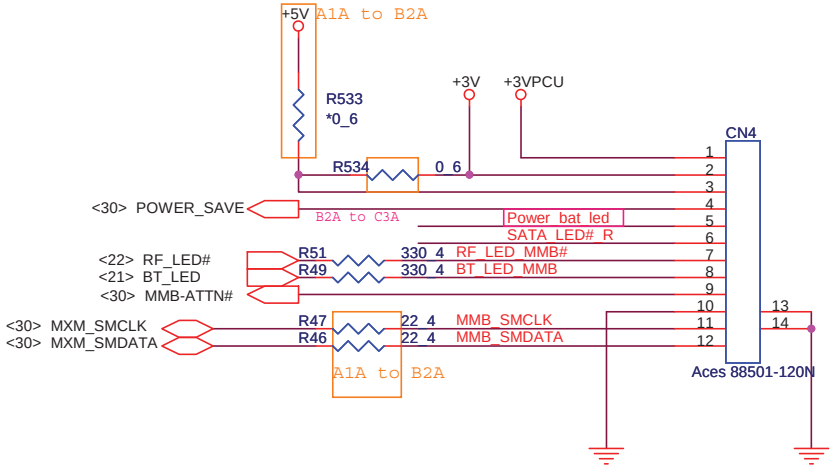
POWER BOARD

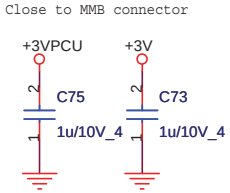


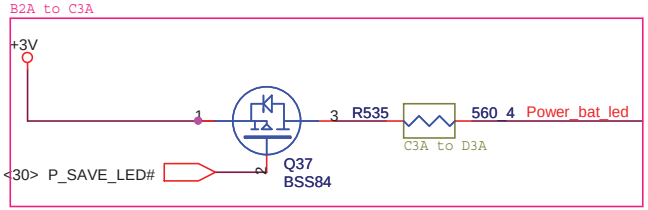
LED



MMB





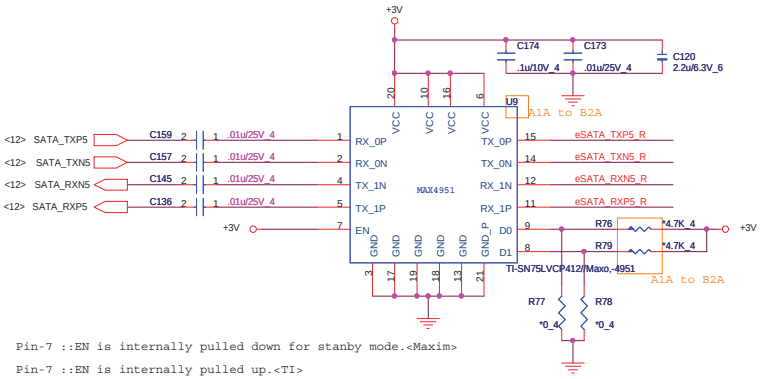


Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	POWER/MMB/LAUNCH/LED	1A
Date: Friday, April 24, 2009	Sheet 27 of 42	

ESATA



Pin-7 ::EN is internally pulled down for stanby mode.<Maxim>

Pin-7 ::EN is internally pulled up.<TI>

Pin-8 ::BB is internally pulled down.<TI/MAXIM>

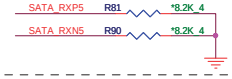
Pin-9 ::BA is internally pulled down.<TI/MAXIM>

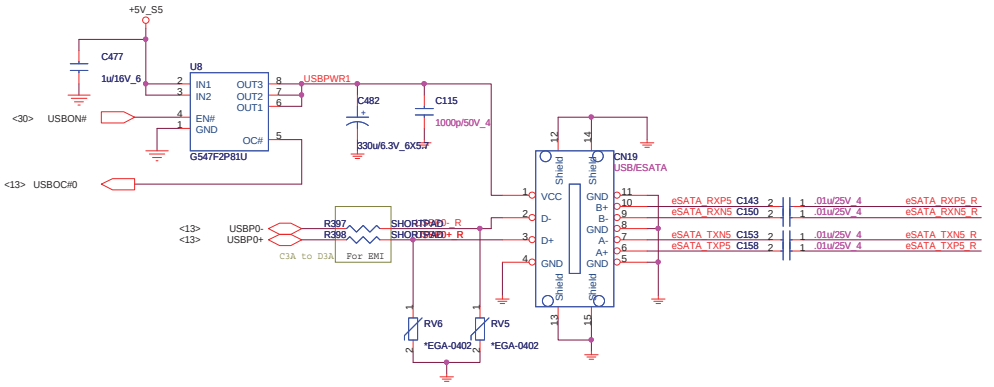
EN	BA/D0	BB/D1	CH-0/A	CH-1/B
0	X	X	Standby	Standby
1	0	0	0dB	0dB
1	1	0	Pre-emphasis (5dB)	0dB
1	0	1	0dB	Pre-emphasis (5dB)
1	1	1	Pre-emphasis (5dB)	Pre-emphasis (5dB)

X=don't care

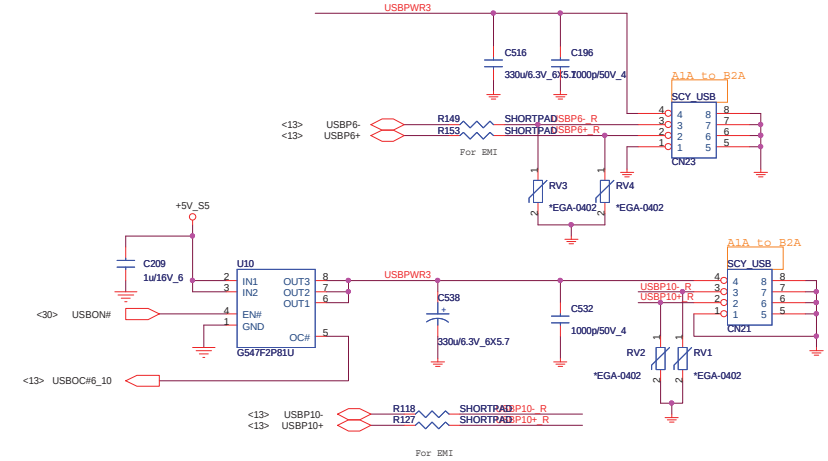
DG2.1 4.2.4 Terminating Unused SATA Interface

SATA[1:0]RXp/n, SATA[5:4]RXp/n connect to GND while SATA not be implemented





USB PORT



HOLES

H-C276D118P2-8 -- 1 pcs

HOLE12 *H-C276D118P2-8

H-C315D118P2-8-- 12 pcs

HOLE3 HOLE8 HOLE5 HOLE7 HOLE30 HOLE24 HOLE1 HOLE21 *H-C315D118P2-8

HOLE27 HOLE29 HOLE28 HOLE23 *H-C315D118P2-8

ADOGND

HOLE2 HOLE9 HOLE19 HOLE14 *H-C236D146P2-8

HOLE15 HOLE20 HOLE22 HOLE13 *H-C236D146P2-8

H-C236D146P2-8 -- 8 pcs

HOLE25 HOLE26 *H-TC236BC197D146P2

C3A to D3A

B2A to C3A

H-TC236BC197D146P2 -- 2 pcs

A1A to B2A

HOLE10 HOLE11 *h-c197d55pb

HOLE16 HOLE17 *H-C197D55P2-8

H-C197D55P2-8 --2 pcs

H-C197D55PB --2 pcs

HOLE31 *H-C354D295P2-8

H-C354D295P2-8 -- 1 pcs

HOLE18 *H-TC236BC276D118P2-8

H-TC236BC276D118P2-8 -- 1 pcs

PAD4 PAD7 PAD3 PAD1 PAD8 PAD10 *PAD-C157

PAD9 PAD13 PAD12 PAD5 PAD6 PAD2 PAD11 *PAD-C157

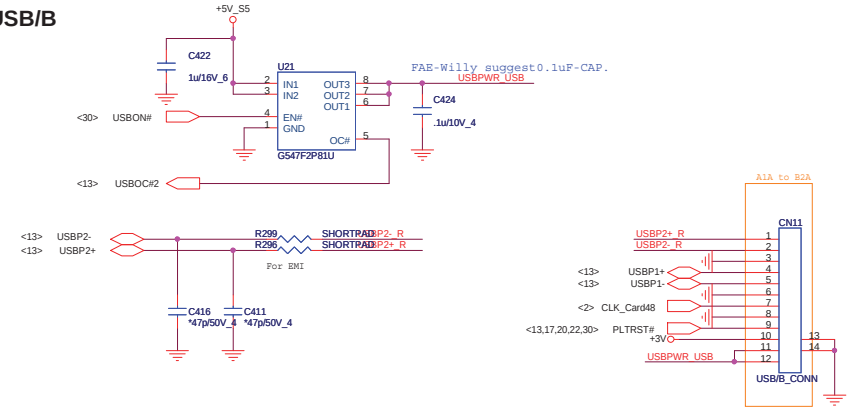
NONGND

HOLE6 *h-c98d98n

NONGND-Fan hole

HOLE4 O-ZK6-1

USB/B



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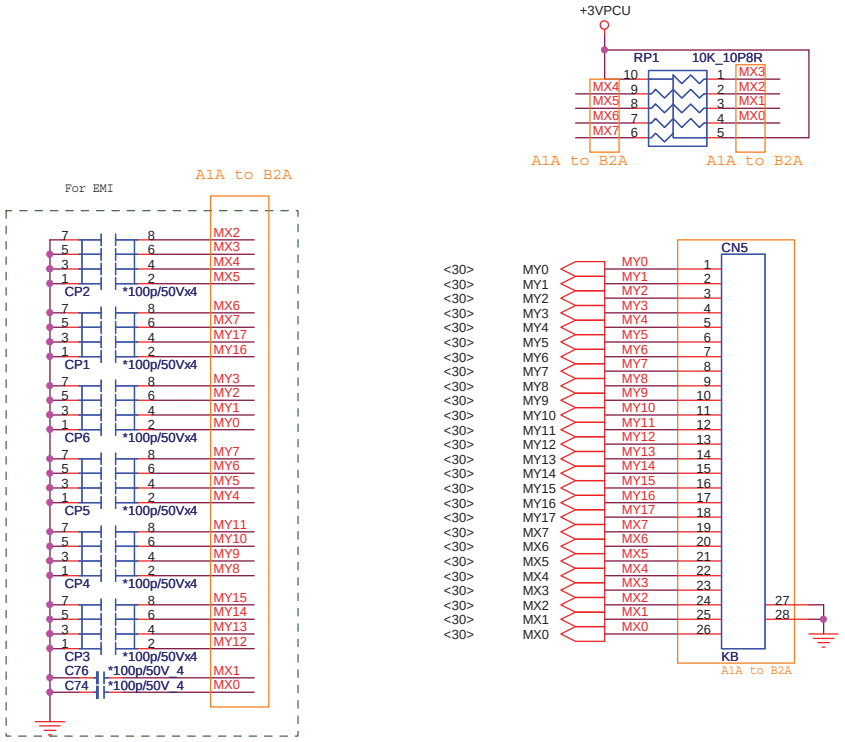
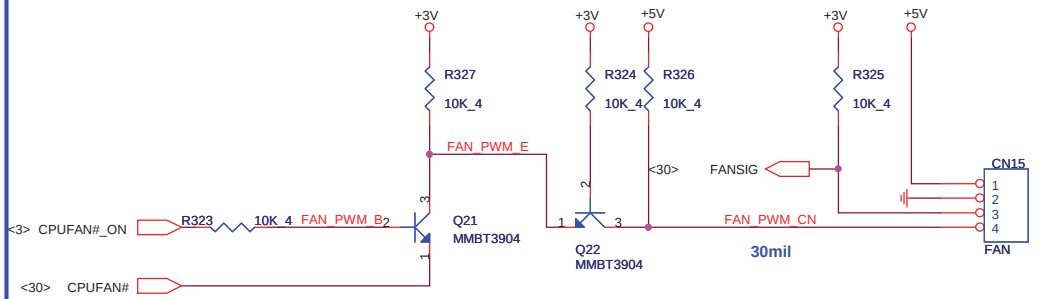
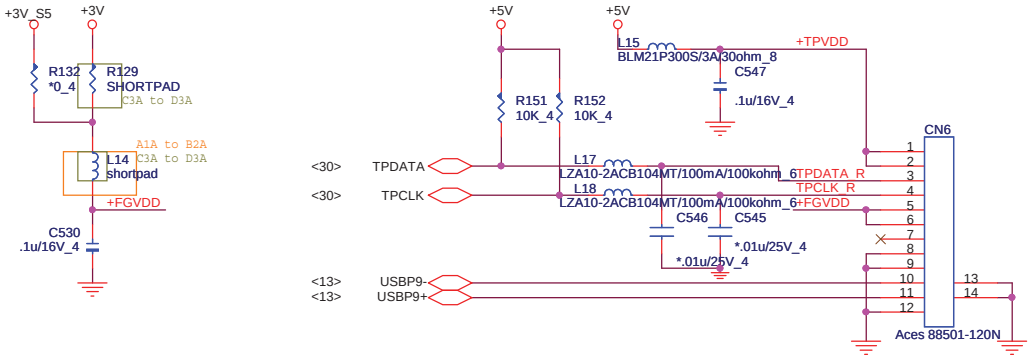
K/B



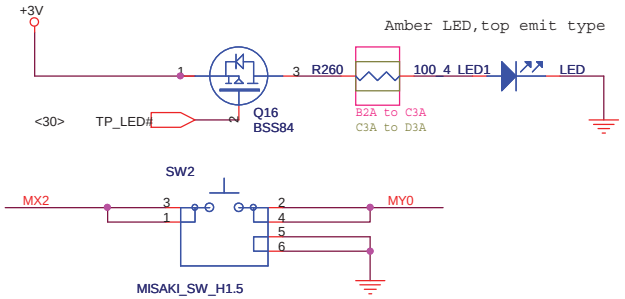
CPU FAN



TOUCHPAD & Finger-Printer CONN.



TP LOCK Button



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EC

I/O ADDRESS SETTING

	I/O Address	
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

BADDR0 — BADDR0_EC_R — R179 — 10K_4
BADDR1 — BADDR1_EC_R — R178 — *10K_4
SHBM — SHBM_R — R440 — 10K_4

1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

SM BUS PU

2ND_MBCLK — R419 — 10K_4
2ND_MBDATA — R429 — 10K_4
MBCLK — R434 — 10K_4
MBDATA — R433 — 10K_4
MXM_SMCLK — R168 — 10K_4
MXM_SMDATA — R169 — 10K_4
CRT_SENSE# — R441 — 4.7K_4

ACER ID

MXM_SMCLK, MXM_SMDATA → U11 (24C02: SCL, SDA, WP, A0, A1, A2, VCC, GND)
R134, R133 shorpad *0_4
C241 *.1u/16V_4

SPI FLASH

U14 (W25X16AVSSIG: SO, SI, SCK, CE, VDD, HOLD, WP, VSS)
SPI_SDI_uR — R447 — 22_4 — SPI_SDI_uR_R
SPI_SDO_uR
SPI_SCK_uR
SPI_CS0#_uR — R448 — 10K_4
C292 .1u/16V_4

1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

HWPG

<38> HWPG_1.8V — D14 BAS316
<34> HWPG_1.05V — D15 BAS316
<6,36> HWPG_VDR — D17 BAS316
<32> SYS_HWPG — D13 BAS316
<35> HWPG_GFX — D16 BAS316
R194 10K_4
R202 shorpad
HWPG → MPWROK <6,14>

INTERNAL KEYBOARD STRIP SET

MY0 — R138 — 10K_4 — +3VPCU

CIR

Q36 *RHU002N06
R518 *10K_4
R522 *10K_4
R525 47_6
R526 *47_6 CIR_LED_PWR
R527 shortpad
C647 4.7u/10V_8
U34 (IRM-V538-TR1: VCC, OUT, GND, GND)
D30 *VPORT
CIRR_X2 ↔ CIRRX2

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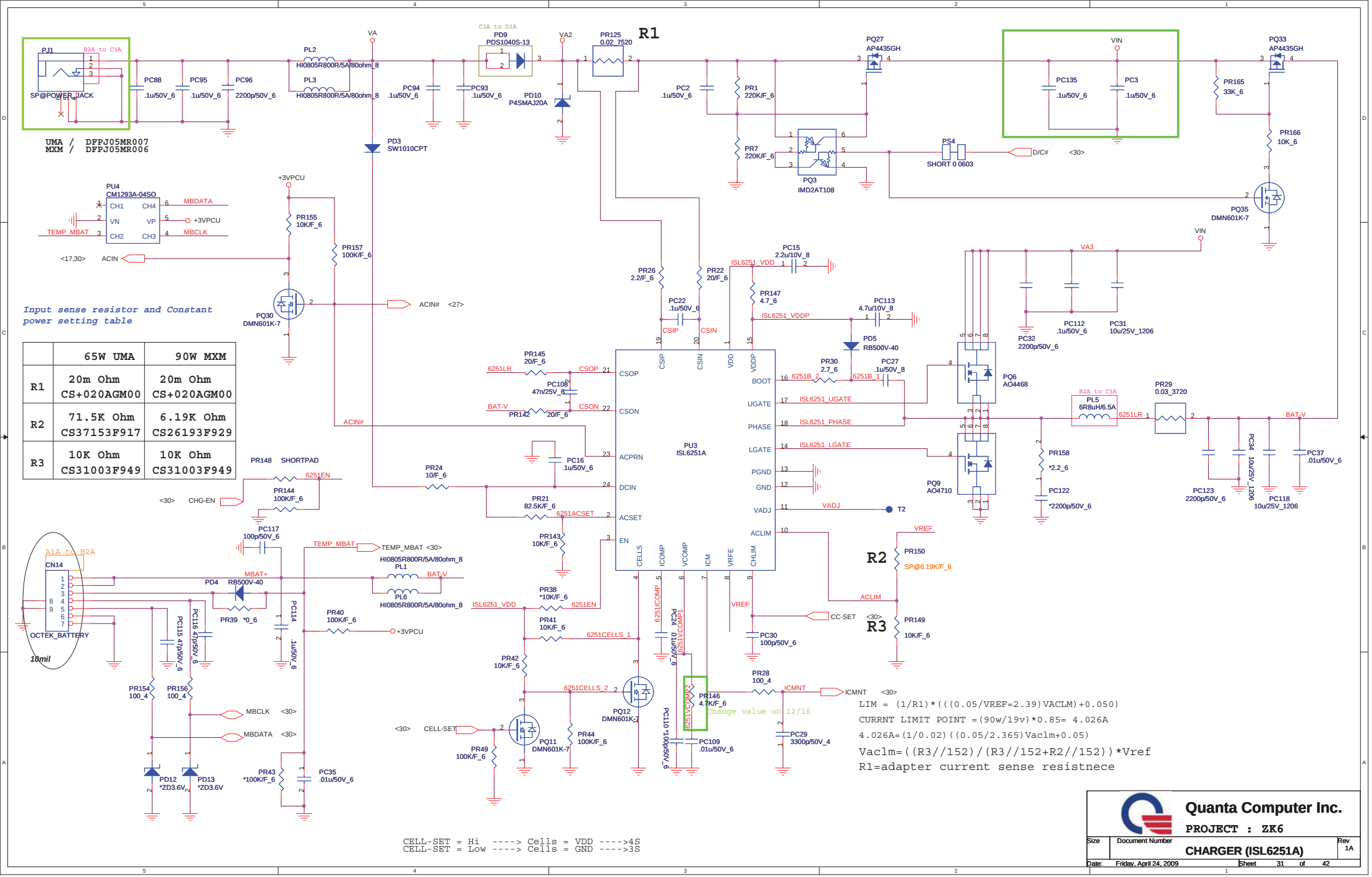
R1
R2
R3
UMA / DFPJ05MR007
MXM / DFPJ05MR006
Input sense resistor and Constant power setting table
65W UMA
90W MXM
R1 20m Ohm CS+020AGM00 20m Ohm CS+020AGM00
R2 71.5K Ohm CS37153F917 6.19K Ohm CS26193F929
R3 10K Ohm CS31003F949 10K Ohm CS31003F949
PU3 ISL6251A
PU4 CM1293A-04SO
OCTEK_BATTERY
SP@POWER_JACK
IMD2AT108
AP4435GH
AO4468
AO4710
DMN601K-7
RB500V-40
P4SMAJ20A
SW1010CPT
HI0805R800R/5A/80ohm_8
SHORT 0 0603
LIM = (1/R1)*(((0.05/VREF=2.39)VACLM)+0.050)
CURRNT LIMIT POINT =(90w/19v)*0.85= 4.026A
4.026A=(1/0.02)((0.05/2.365)Vaclm+0.05)
Vaclm=((R3//152)/(R3//152+R2//152))*Vref
R1=adapter current sense resistnece
Change value on 12/16
CELL-SET = Hi ----> Cells = VDD ---->4S
CELL-SET = Low ----> Cells = GND ---->3S
Quanta Computer Inc.
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CHARGER (ISL6251A)
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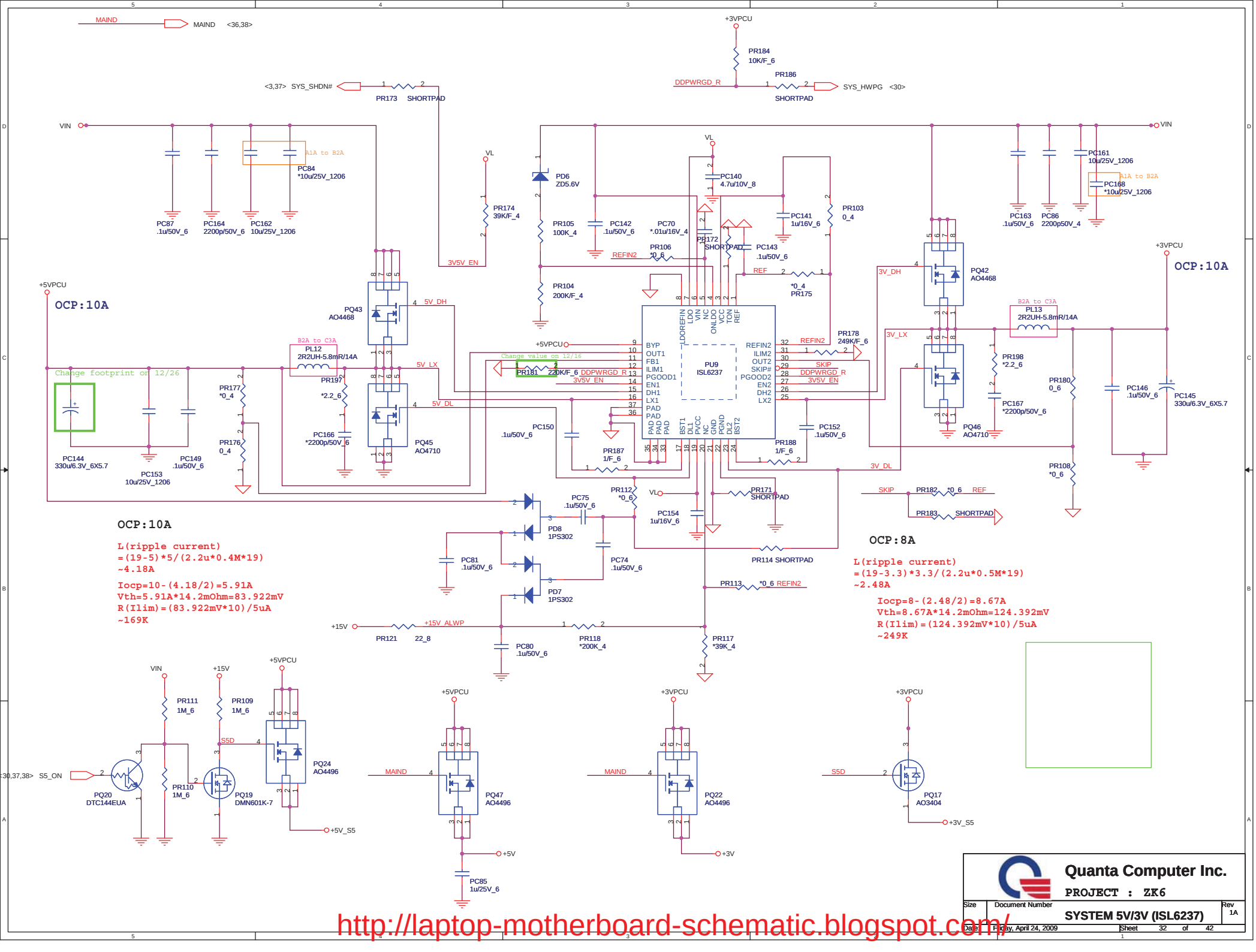
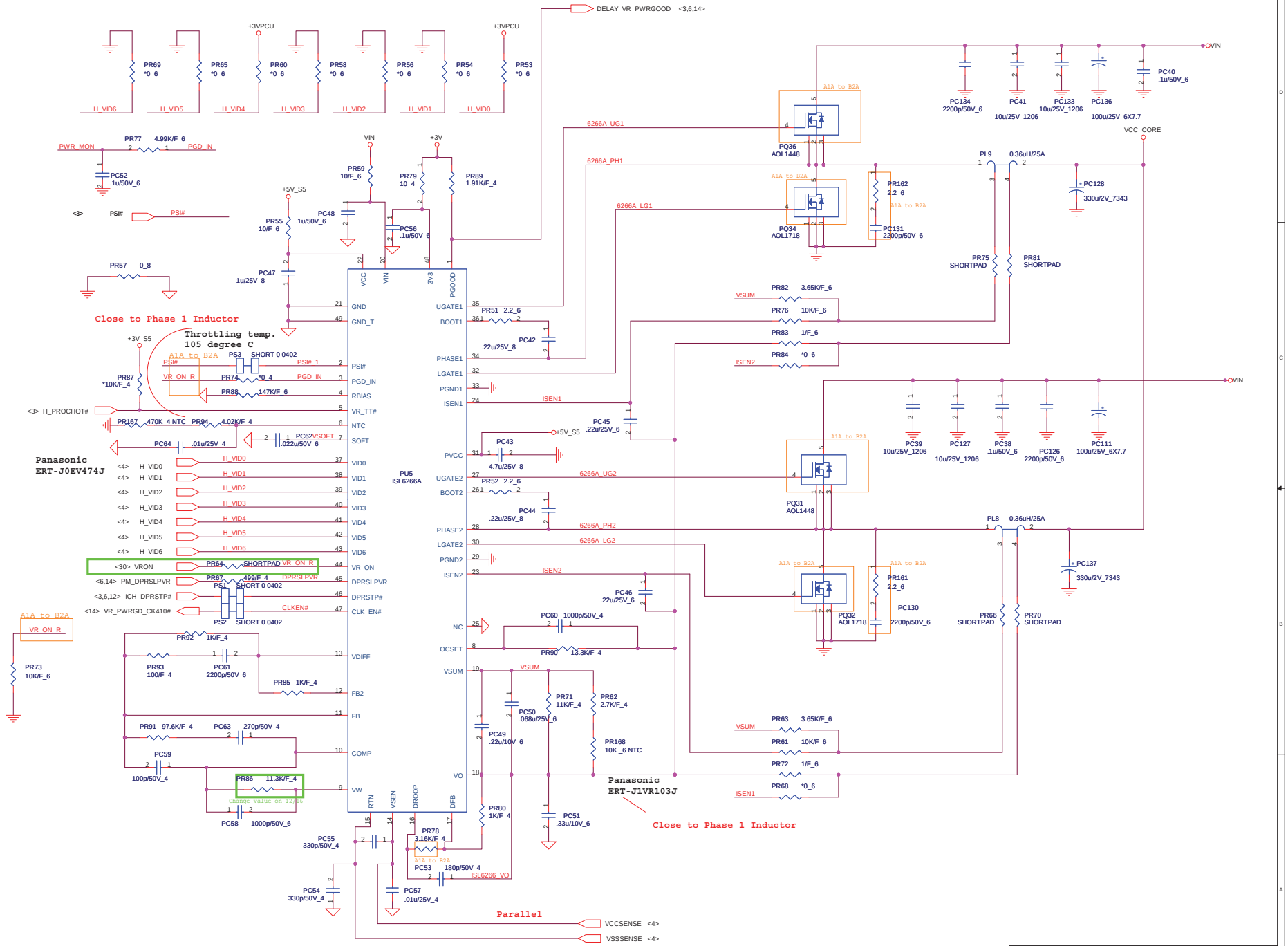
http://laptop-motherboard-schematic.blogspot.com/





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PROJECT : ZK6		
Size	Document Number: CPU CORE(ISL6266A)	Rev: 1A
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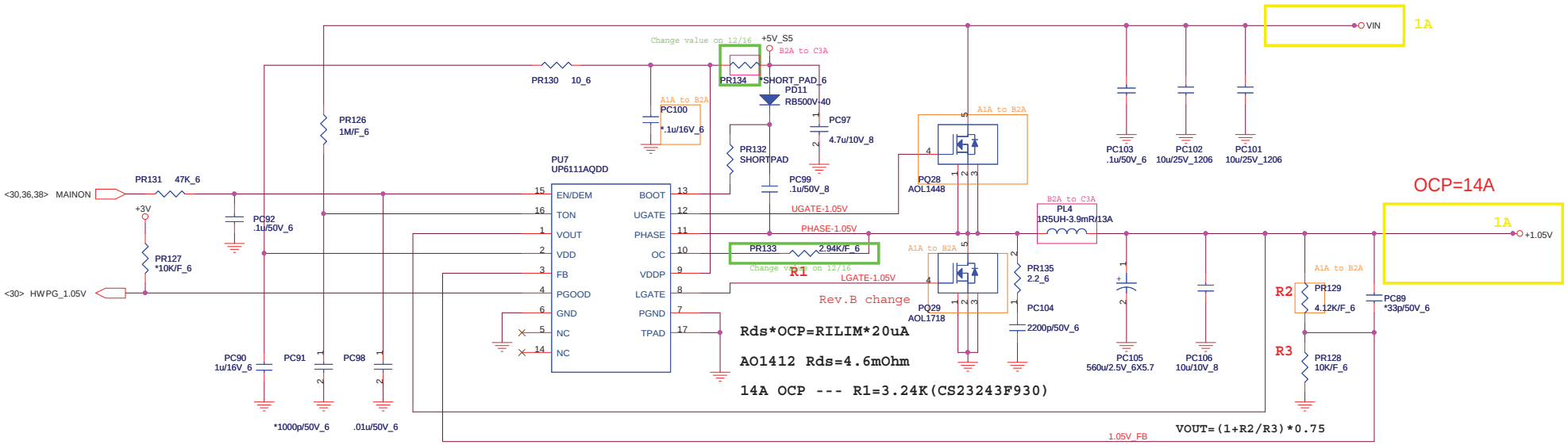

TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

Quanta Computer Inc.		
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Size	Document Number	Rev
	VTT 1.05V (RT8202)	1A
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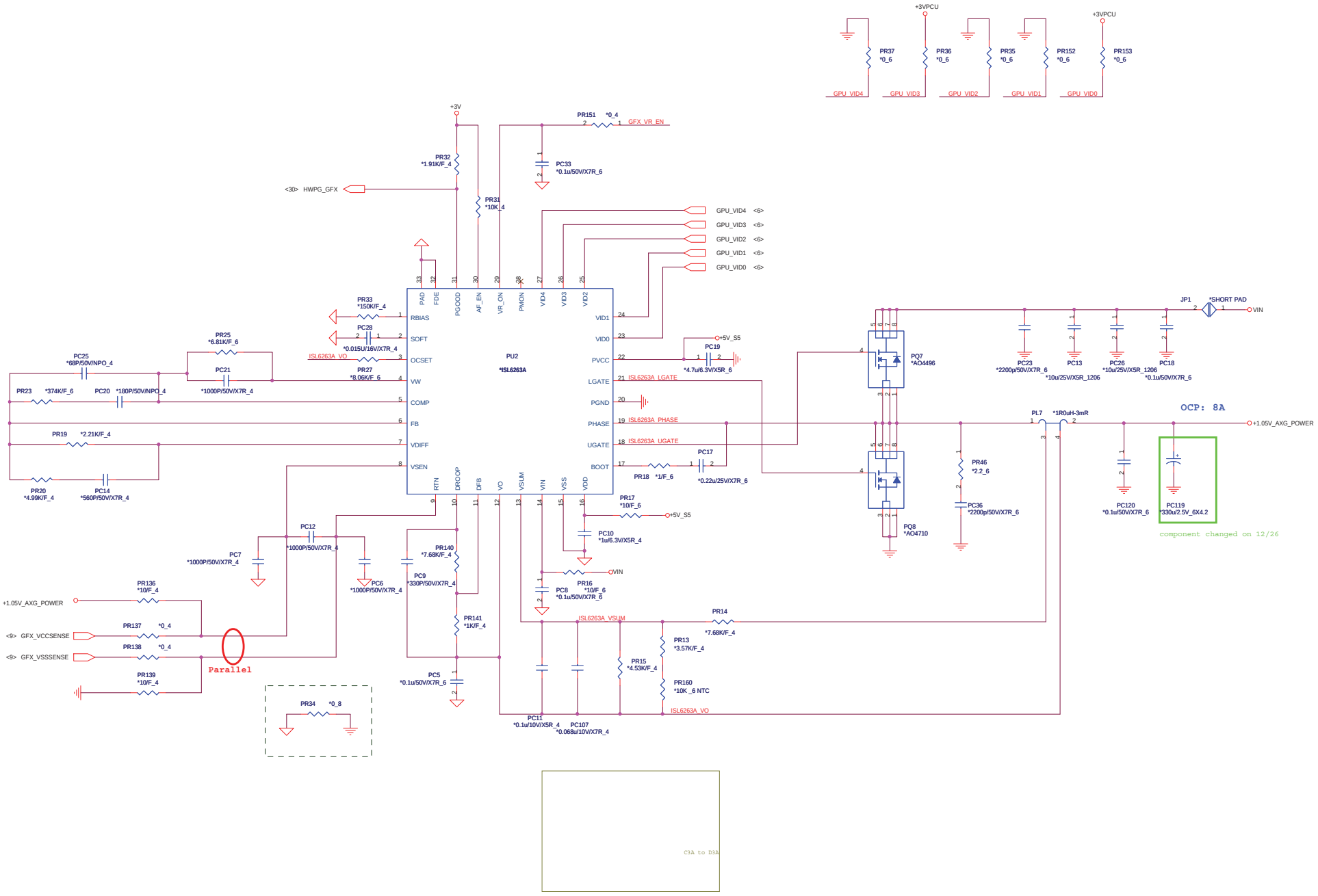
all component in this page would be stuff for UMA only



Quanta Computer Inc.
PROJECT : ZK6
Size | Document Number: +1.05V_GFX-ISL6263A | Rev: 1A
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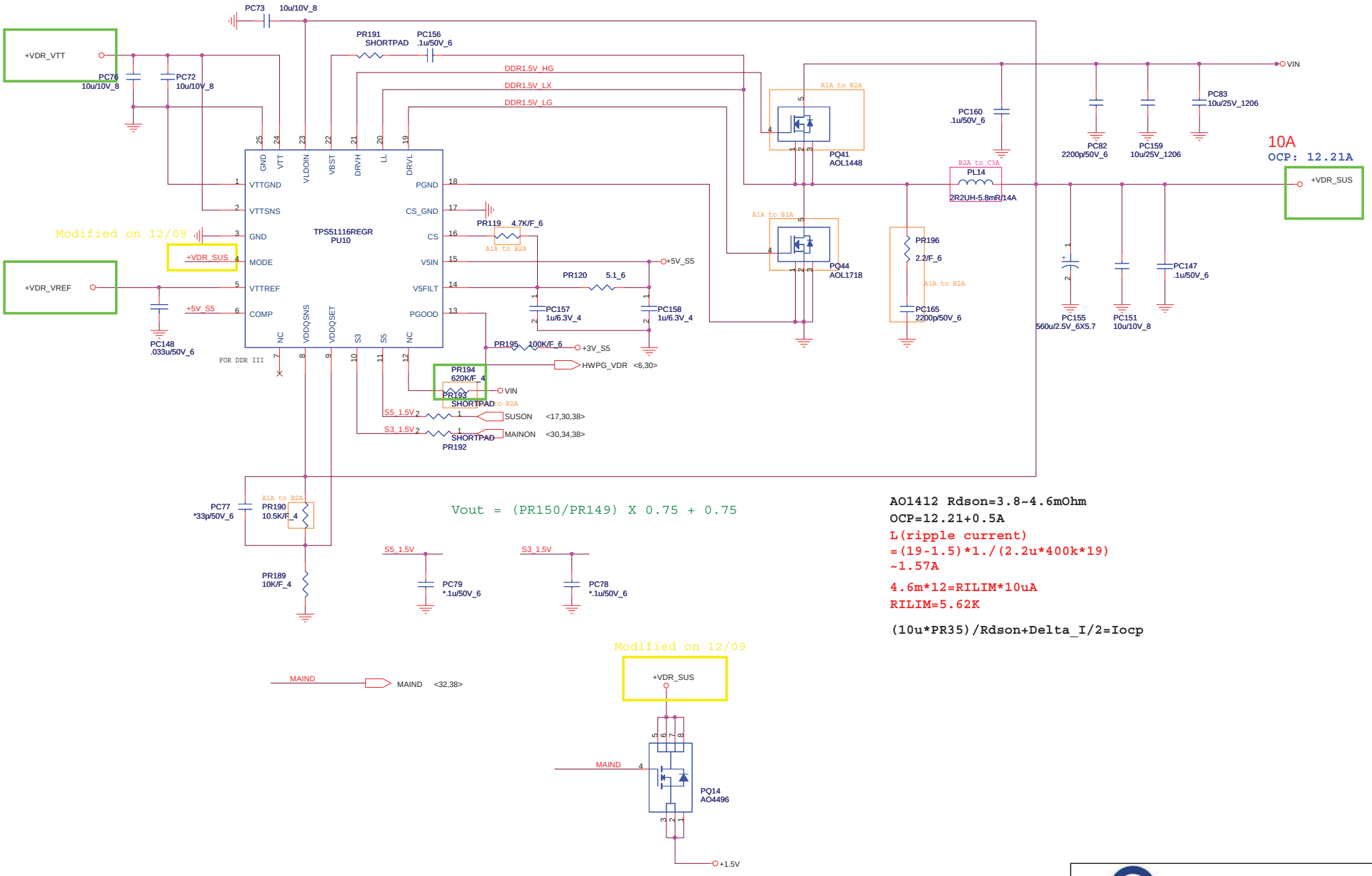

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	DDR 1.8V(TPS51116)	1A
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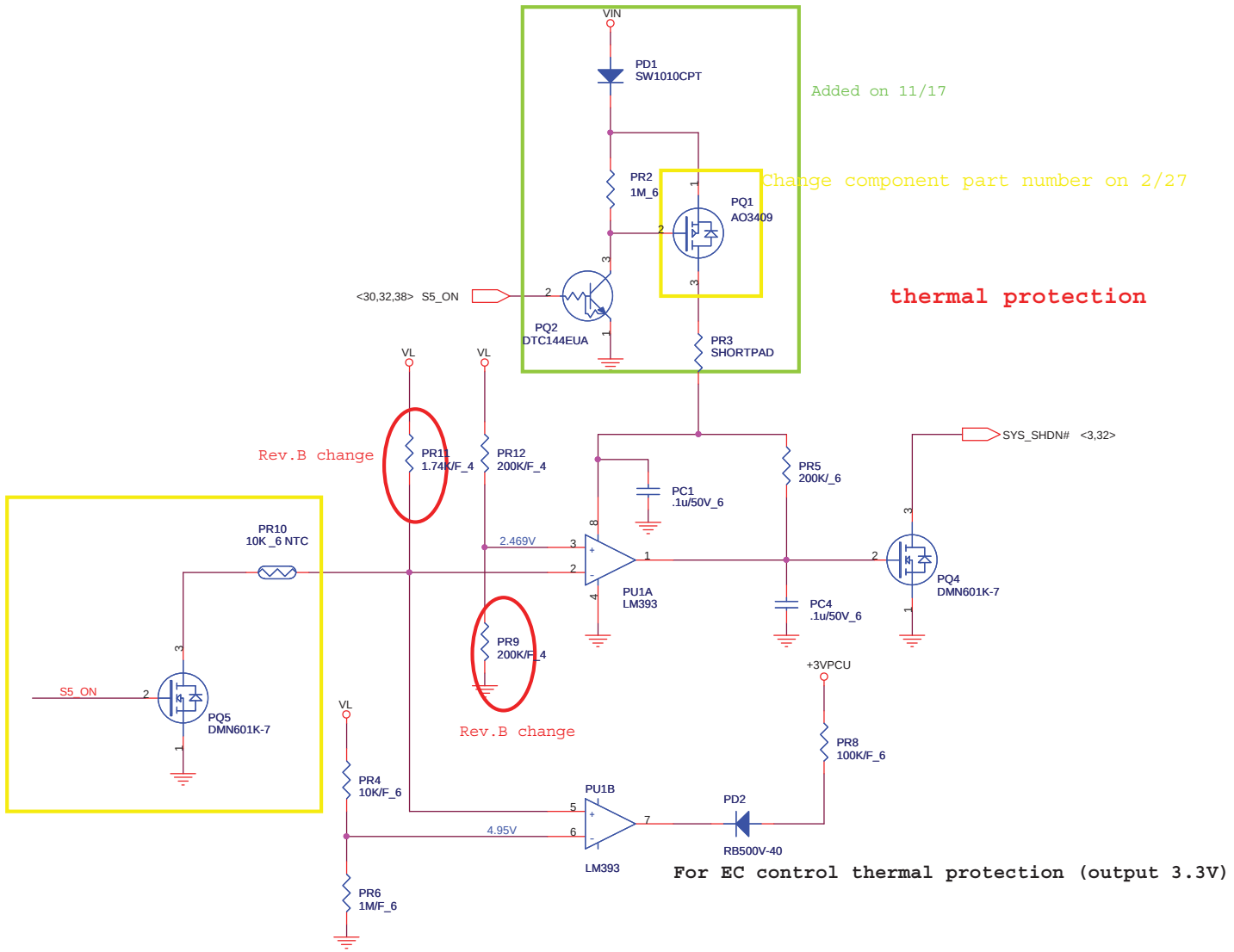

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	Thermal protect	1A
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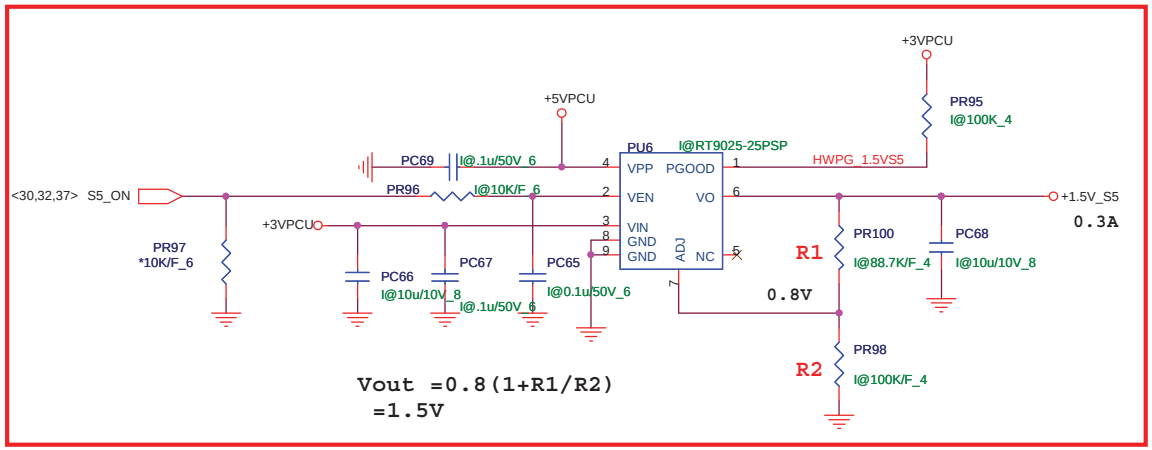

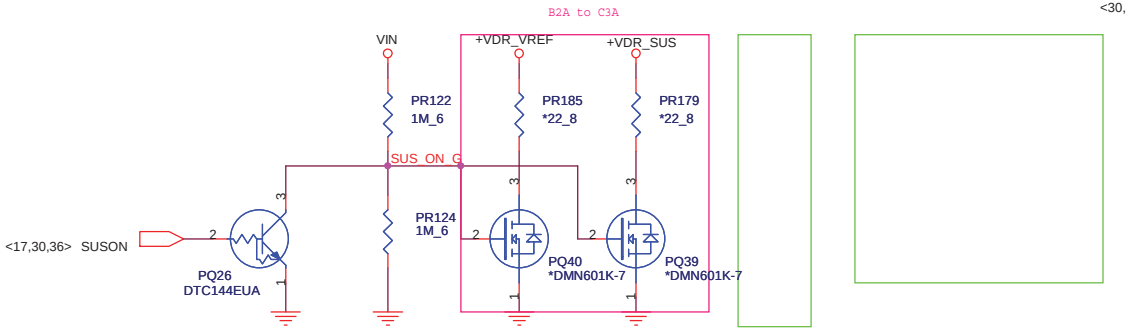

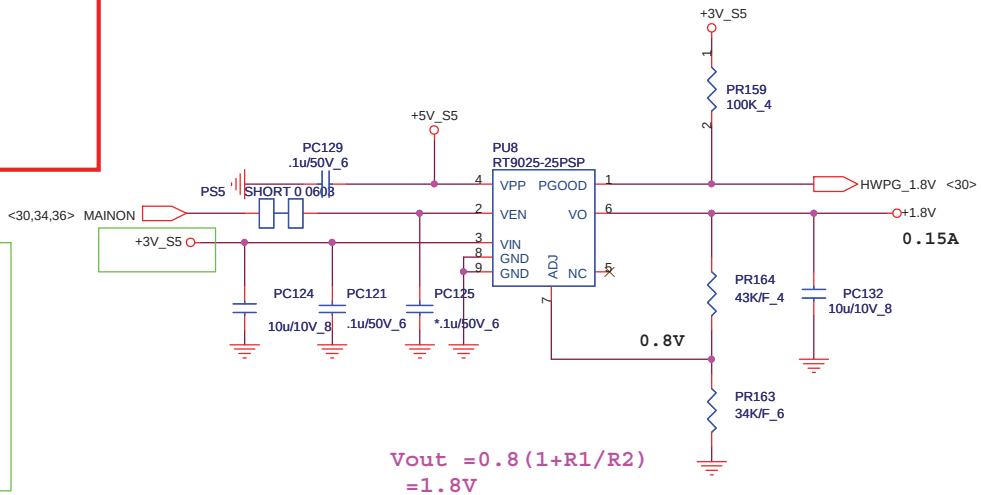

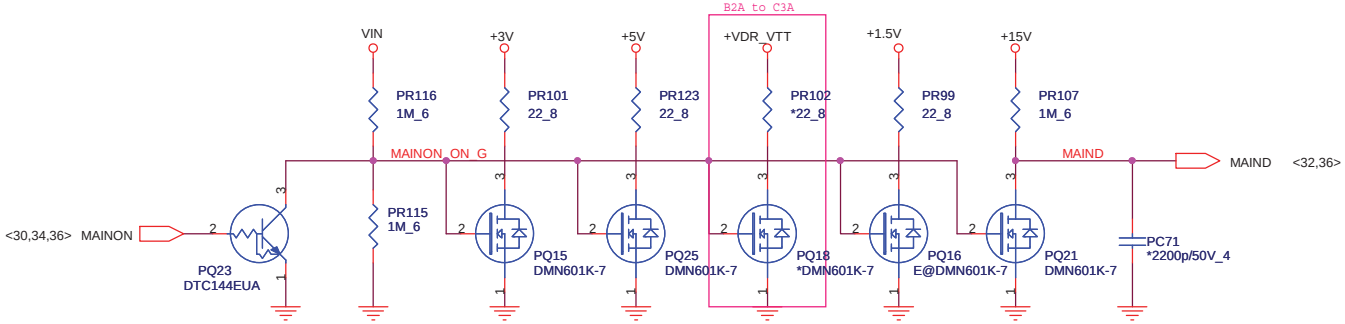

Quanta Computer Inc.

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Size	Document Number	Rev
	Discharge (2.5V/1.5V)	1A
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