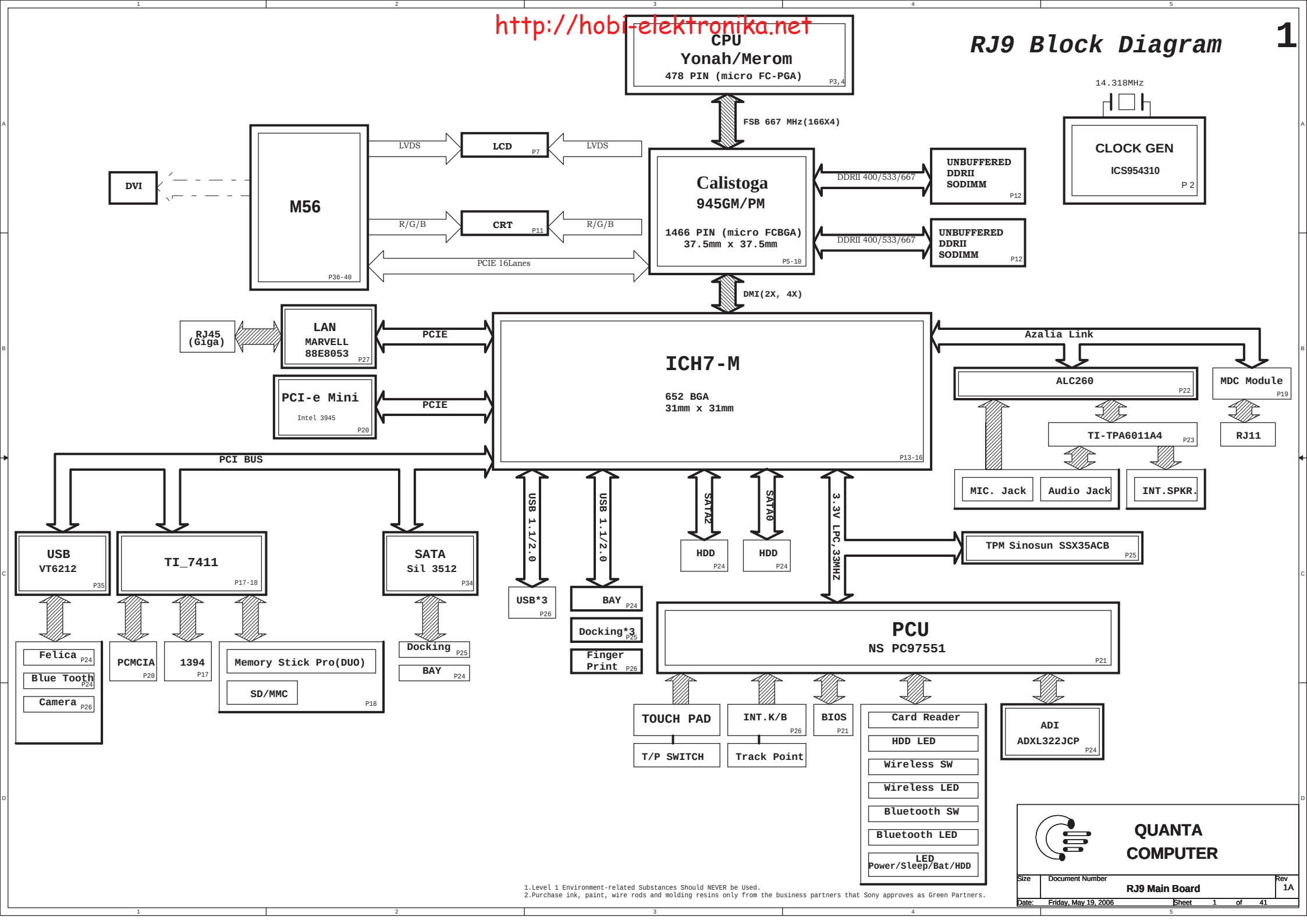
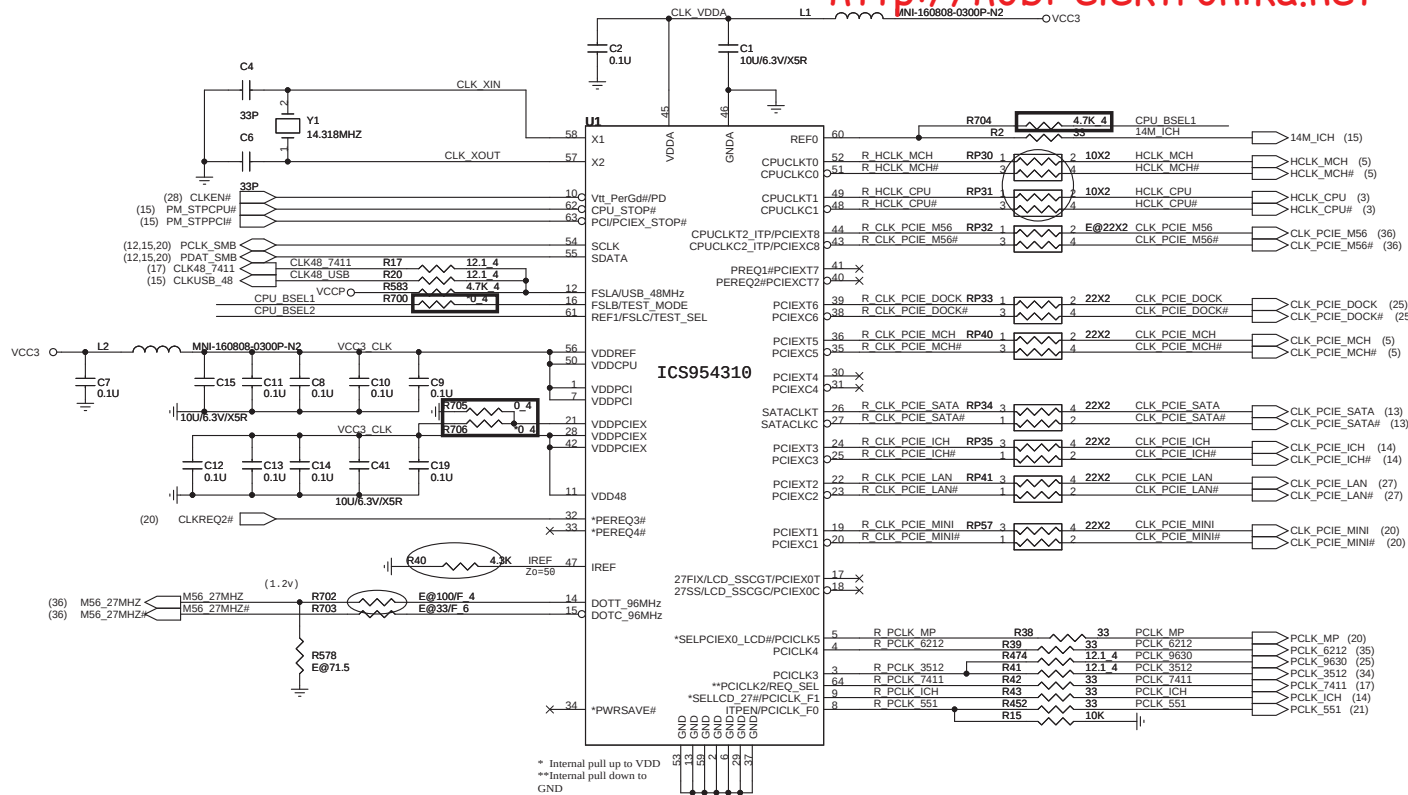
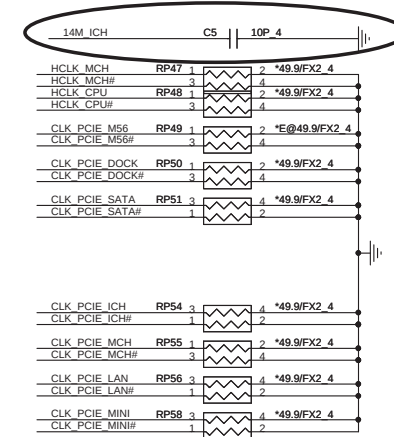




1. Level 1 Environment-related Substances should NEVER be Used.
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Add for EMI 3/30



Add for EMI 3/30

SATA Spread and Frequency Selection Table (SEL_SATA) :

SEL_SATA	SS3	SS2	VC0 MHZ	27, 26 MHZ	Spread %
1	0	0	tbd	100	-0.2 Down
1	0	1	tbd	100	-0.3 Down
1	1	0	tbd	100	-0.4 Down
1	1	1	tbd	100	-0.5 Down

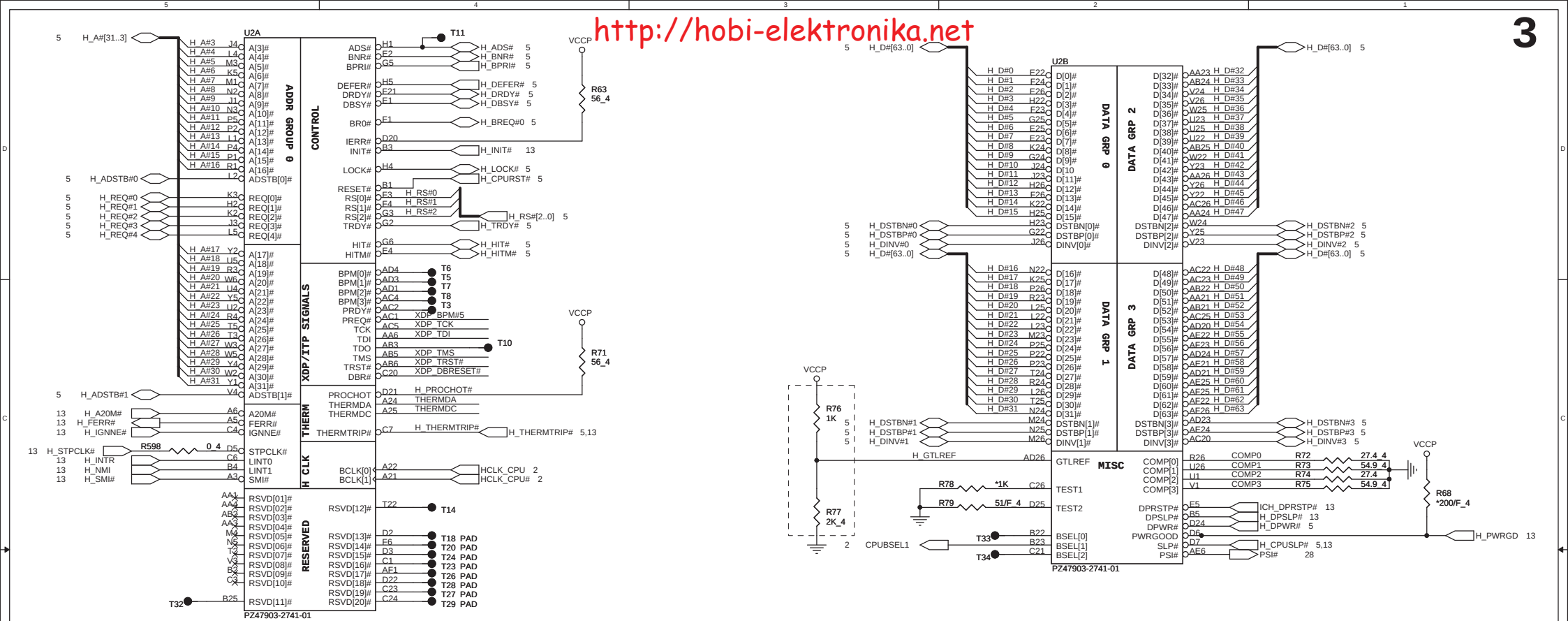
LCDClock Spread and Frequency Selection Table (SEL_LCD) :

SEL_LCD	SS3	SS2	SS1	SS0	17, 18 MHZ	Spread %	SEL_LCD	SS3	SS2	SS1	SS0	17, 18 MHZ	Spread %
1	0	0	0	0	96	+/-1.5	0	0	0	0	0	27	+/-0.25
1	0	0	0	1	96	+/-1.25	0	0	0	0	1	27	+/-0.5
1	0	0	1	0	96	+/-1.0	0	0	0	1	0	27	+/-0.75
1	0	0	1	1	96	+/-0.8	0	0	0	1	1	27	+/-1
1	0	1	0	0	96	+/-0.6	0	0	1	0	0	27	+/-1.25
1	0	1	0	1	96	+/-0.5	0	0	1	0	1	27	+/-1.5
1	0	1	1	0	96	+/-0.4	0	0	1	1	0	27	+/-1.75
1	0	1	1	1	96	+/-0.3	0	0	1	1	1	27	+/-2
1	1	0	0	0	96	3	0	1	0	0	0	27	-0.5
1	1	0	0	1	96	2.5	0	1	0	0	1	27	-1
1	1	0	1	0	96	2	0	1	0	1	0	27	-1.25
1	1	0	1	1	96	1.75	0	1	0	1	1	27	-1.5
1	1	1	0	0	96	1.5	0	1	1	0	0	27	-1.75
1	1	1	0	1	96	1.25	0	1	1	0	1	27	-2
1	1	1	1	0	96	1	0	1	1	1	0	27	-2.5
1	1	1	1	1	96	0.8	0	1	1	1	1	27	-3

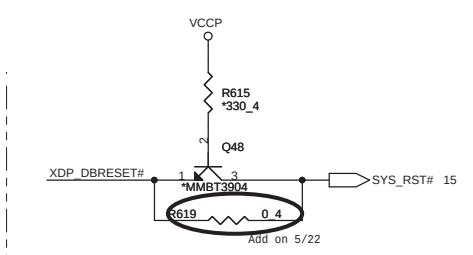
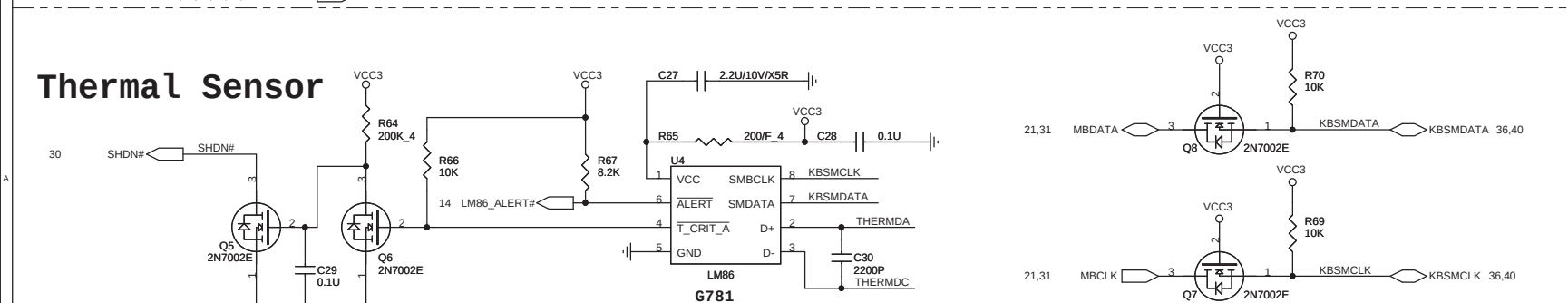
Signal		9456M	945PM
CLK_PCIE_M56	RP32	NI	33X2
DREFSSCLK	RP49	NI	49.9
	RP36	33X2	NI
	RP52	49.9X2	NI
	R528	NI	121
	R529	NI	33
DREFCLK	RP37	33X2	NI
	RP53	49.9X2	NI
R_PCLK_ICH	R6	NI	10K

SEL_SRC0(Pin 17,18)(R4)	REQ_SEL(Pin 40,41)(R44)
0: LCDClock pair	0: PCIEXT7/PCIEXC7
1: SRCCLK0 pair	1: PREQ#

FSC BSEL2	FSB BSEL1	FSA BSEL0	CPU	SRC	PCI	REF	USB	DOT	Spread %
0	0	0	266.66	100	33.33	14.318	48	96	0.5 Down
0	0	1	133.33	100	33.33	14.318	48	96	0.5 Down
0	1	0	200.00	100	33.33	14.318	48	96	0.5 Down
* 0	1	1	166.66	100	33.33	14.318	48	96	0.5 Down
1	0	0	333.33	100	33.33	14.318	48	96	0.5 Down
1	0	1	100.00	100	33.33	14.318	48	96	0.5 Down
1	1	0	400.00	100	33.33	14.318	48	96	0.5 Down
1	1	1	200.00	100	33.33	14.318	48	96	0.5 Down



Thermal Sensor



QUANTA COMPUTER

Rev 1A

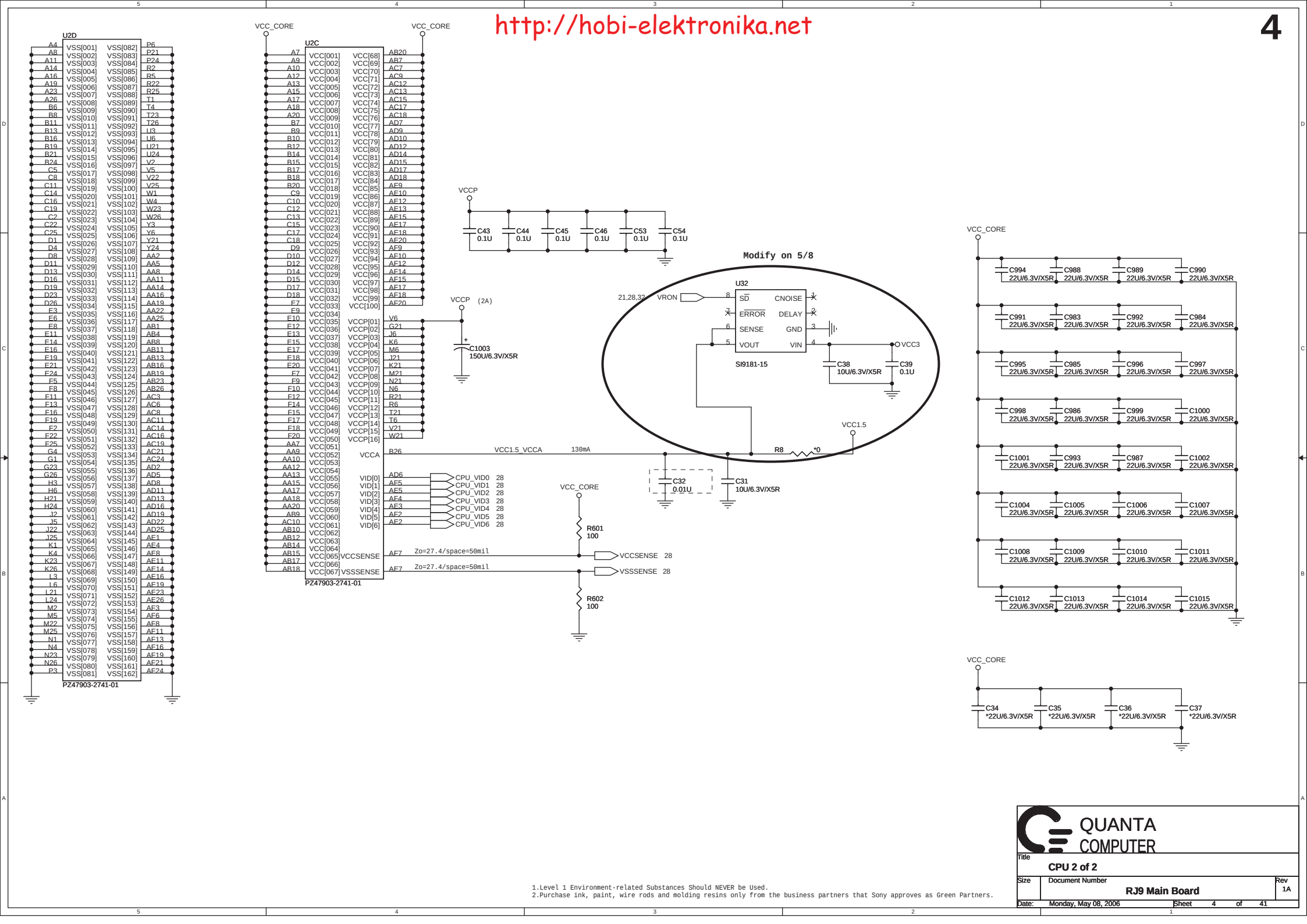
Document Number

RJ9 Main Board

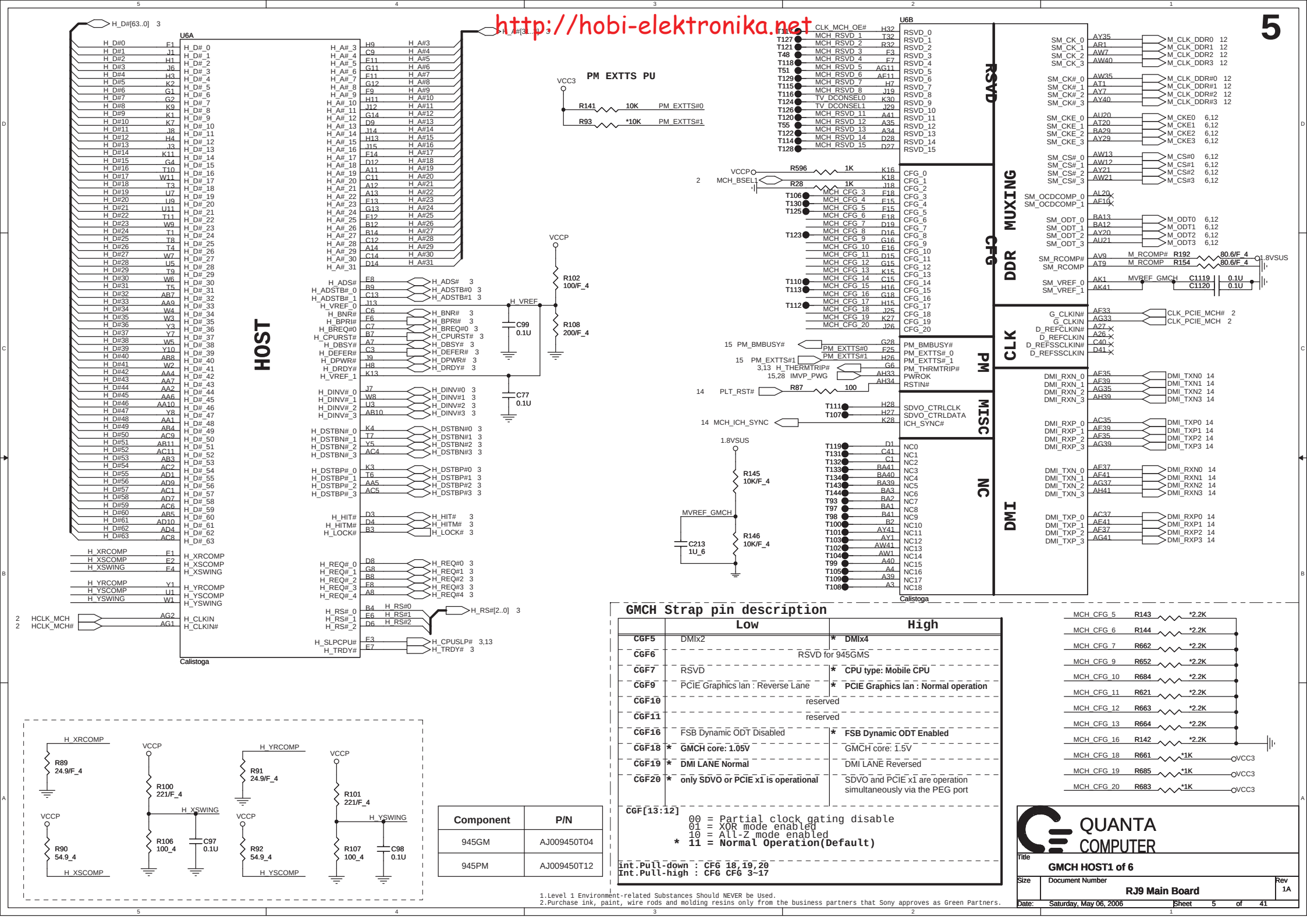
Monday, May 22, 2006

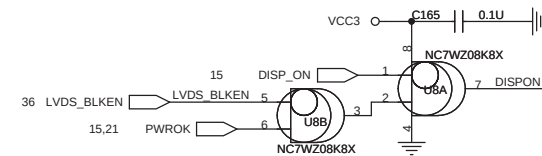
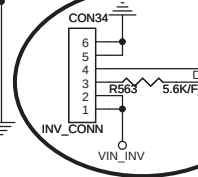
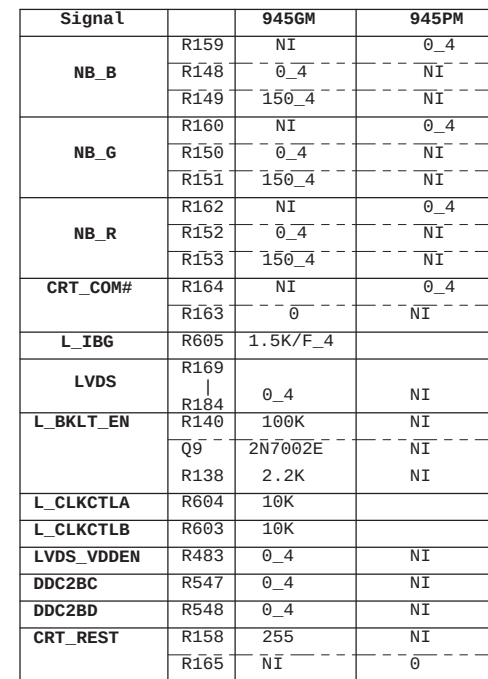
Sheet 3 of 41

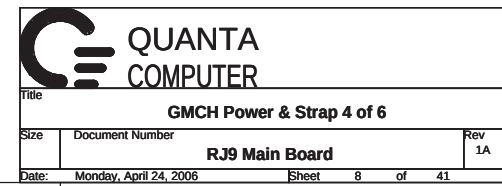
1.Level 1 Environment-related Substances Should NEVER be Used.
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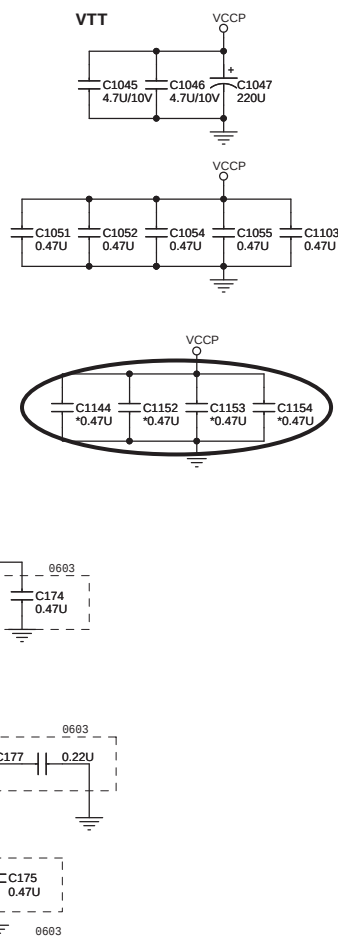


1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods and molding resins only from the business partners that Sony approves as Green Partners.

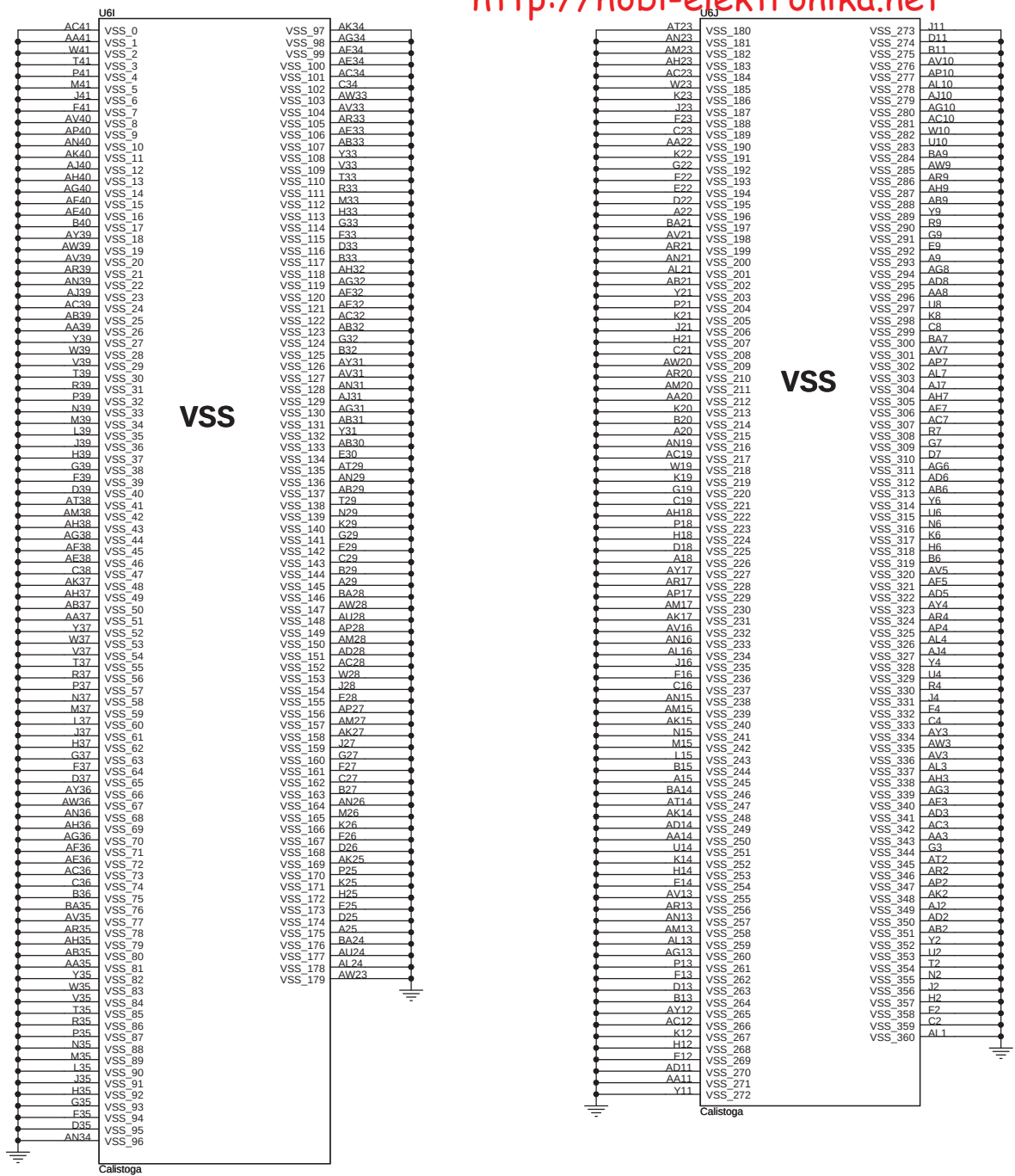






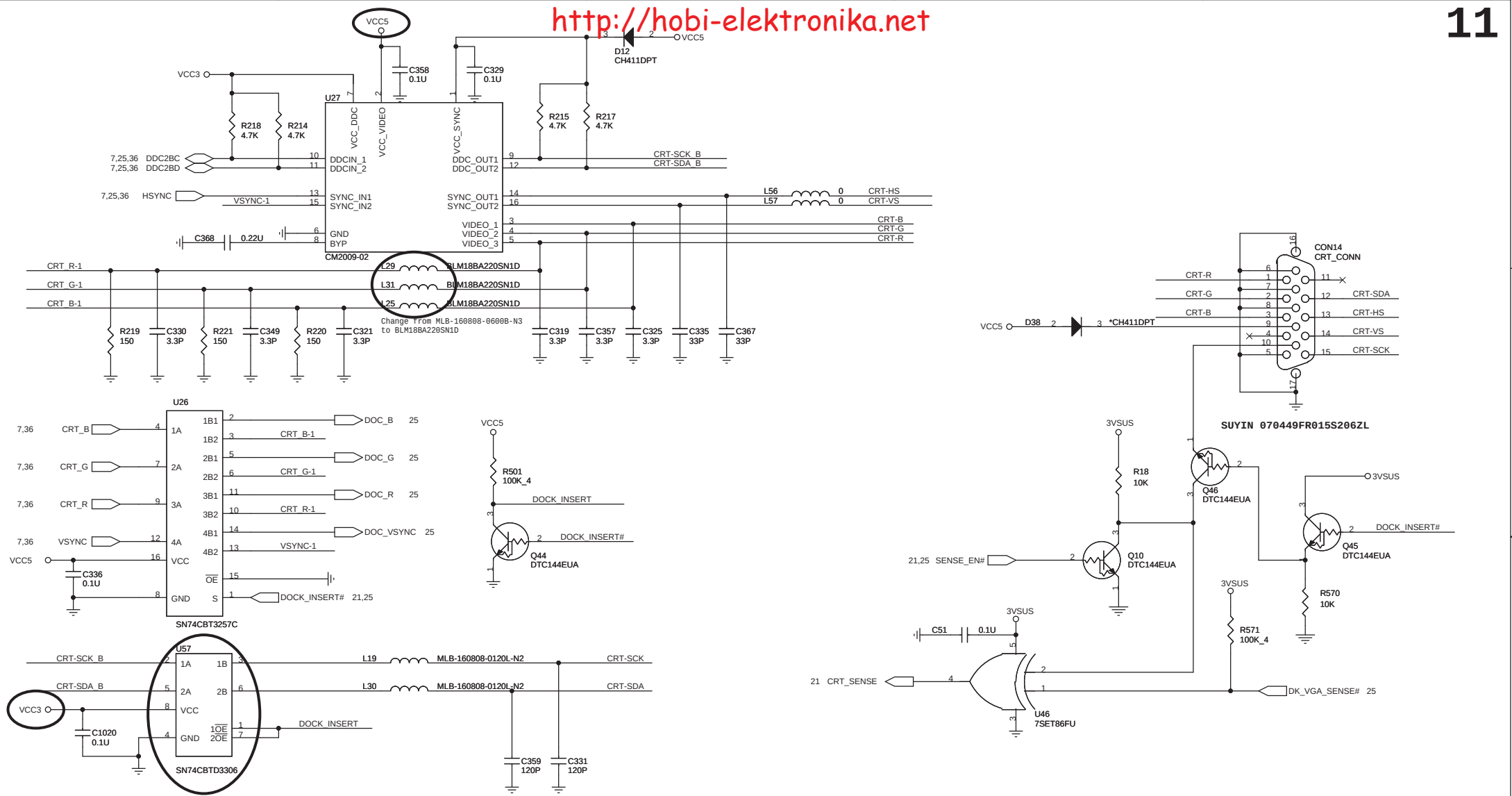


 QUANTA COMPUTER				
Title				
GMCH Power 2 5 of 6				
Size	Document Number			Rev
	RJ9 Main Board			1A
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Title			
GMCH GND 6 of 6			
Size	Document Number		Rev
	RJ9 Main Board		1A
Date	Monday, March 27, 2006		Sheet 10 of 41

1.Level 1 Environment-related Substances Should NEVER be Used.
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	SENSE_EN#	MB CRT	DOCK CRT	DOCK DVI	CRT_SENSE
All no Plug	L	H	H	L	L
MB CRT Plug	L	L	H	L	H
DOCK CRT Plug	L	H	L	L	H
DOCK DVI Plug	L	H	H	H	H
SENSE EN	H	X	X	X	L
DOCK CRT/DVI Plug	L	H	L	H	L
DOCK CRT/MB CRT Plug	L	L	L	L	L

7SET86FU

A	B	Y
H	H	L
H	L	H
L	H	H
L	L	L

QUANTA
COMPUTER

Title: CRT

Size: Document Number

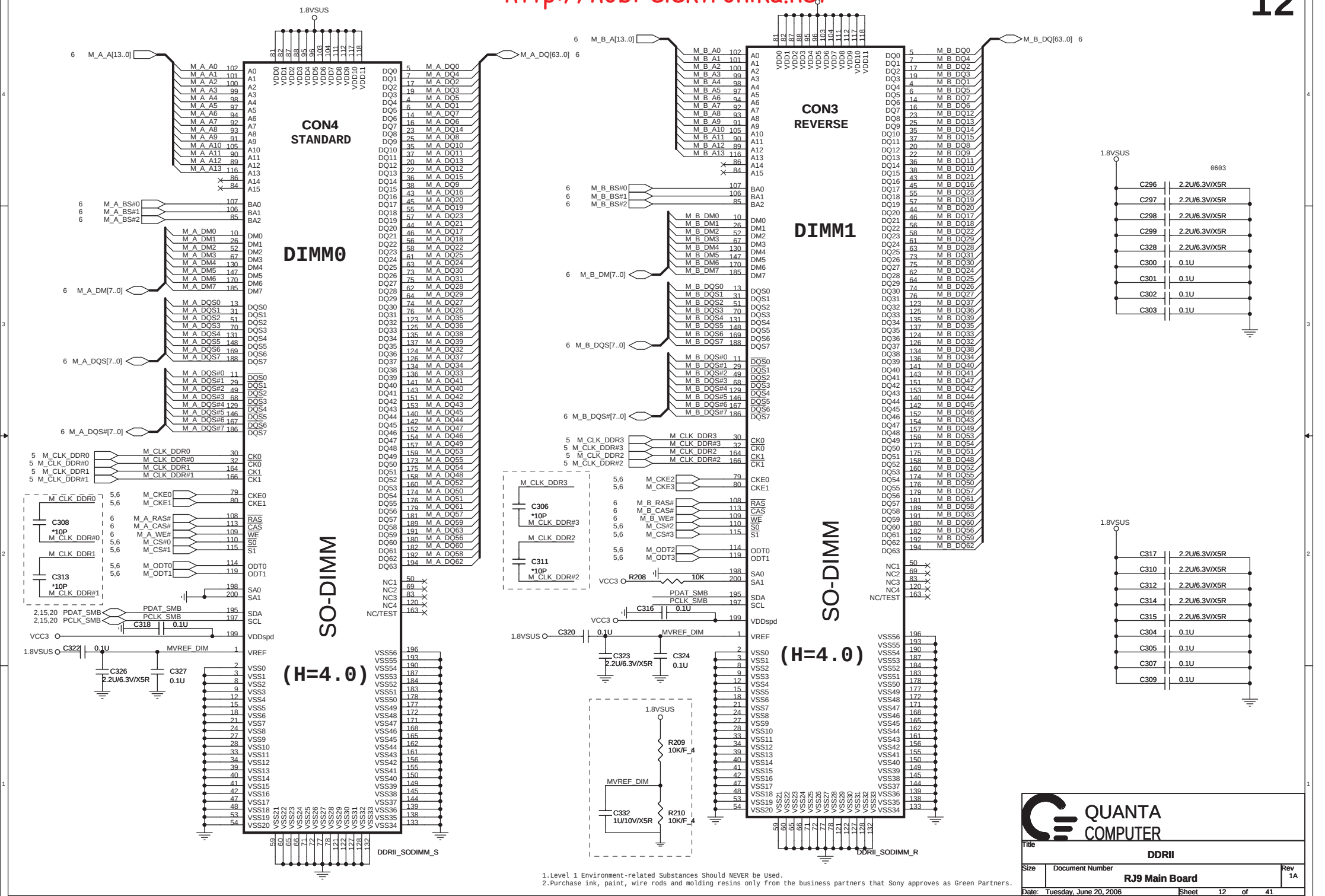
Date: Tuesday, May 23, 2006

Rev: 1A

Sheet: 11 of 41

RJ9 Main Board

1.Level 1 Environment-related Substances Should NEVER be Used.
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QUANTA
COMPUTER

DDRII

Size Document Number Rev 1A

Date: Tuesday, June 20, 2006 Sheet 12 of 41

VCC3

IDE PU

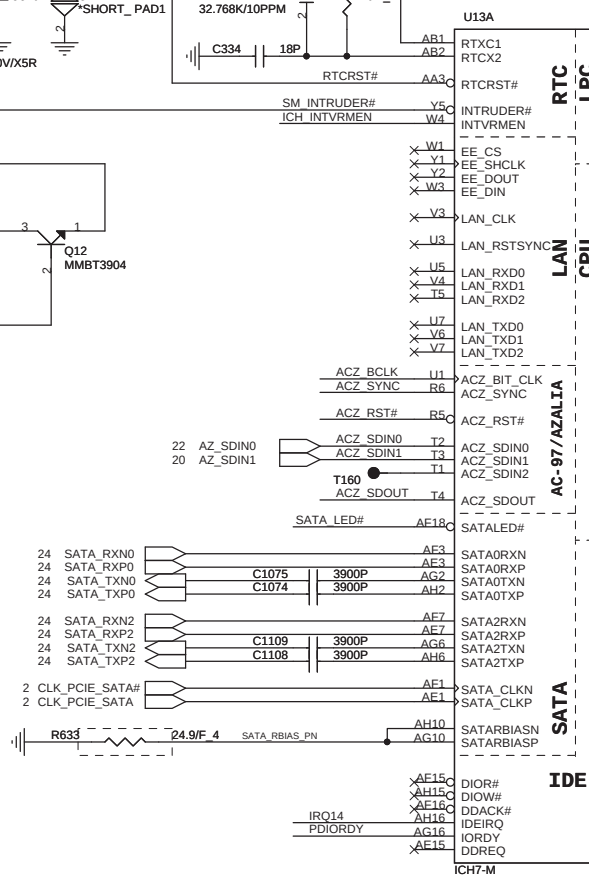
R639
8.2K

R640
4.7K

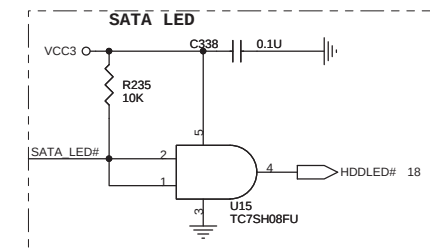
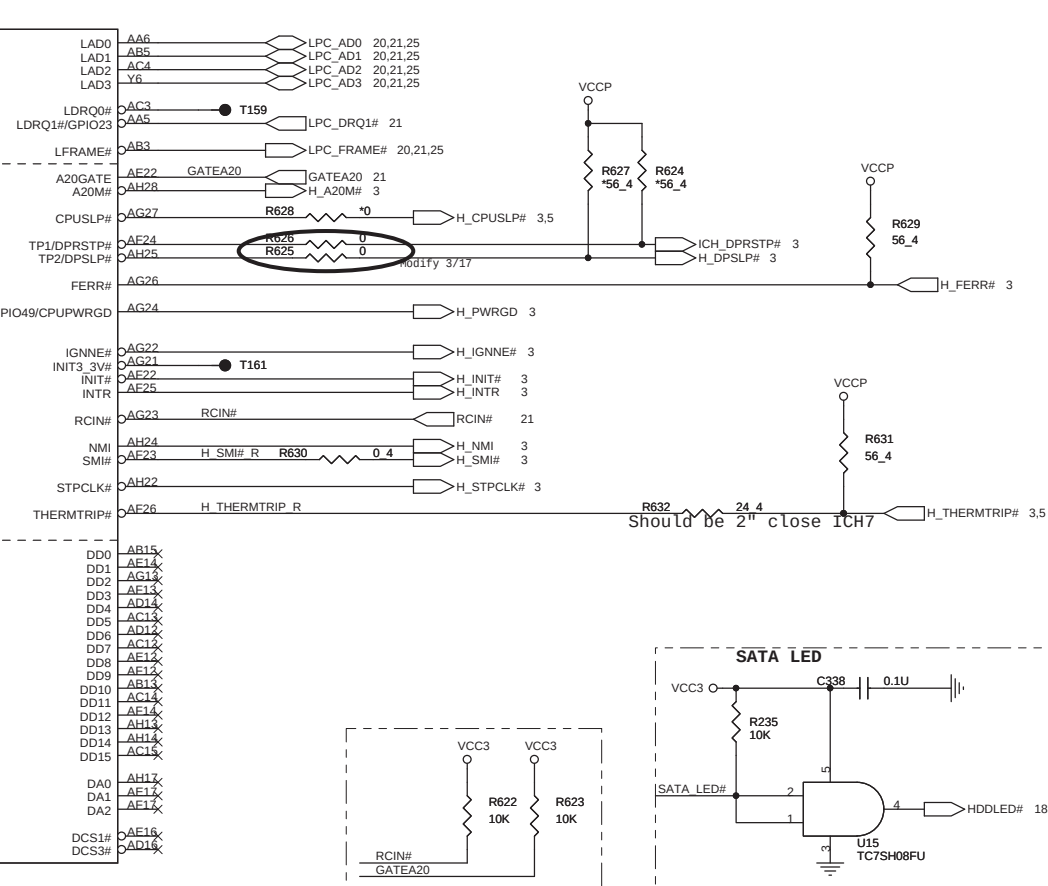
PDIORDY
IRQ14

The diagram shows the INTVRMEN pin configuration. The pin is connected to VCC_RTC through a 332kΩ resistor (R638). The pin is also connected to the ICH_INTVRMEN pin through a 0.4Ω resistor (R643). The pin is pulled up to VCC_RTC and pulled down to ground.

	INTVRMEN
Enable (default)	1
Disable	0



The schematic diagram illustrates the HD Audio I/O connector circuit. It shows two input signals, ACZ_SDOUT and ACZ_SYNC, connected to a set of output pins. The ACZ_SDOUT signal is connected to R634 and R635, which are 39-ohm resistors. R634 connects to AZ_SDOUT1 (pin 20), and R635 connects to AZ_SDOUT0 (pin 22). The ACZ_SYNC signal is connected to R636 and R637, which are also 39-ohm resistors. R636 connects to AZ_SYNC1 (pin 20), and R637 connects to AZ_SYNC0 (pin 22). Each output pin is connected to a 10pF capacitor (C1076, C1077, C1078, and C1079) to ground. The diagram is labeled 'level 1 Environment-relate' at the bottom.



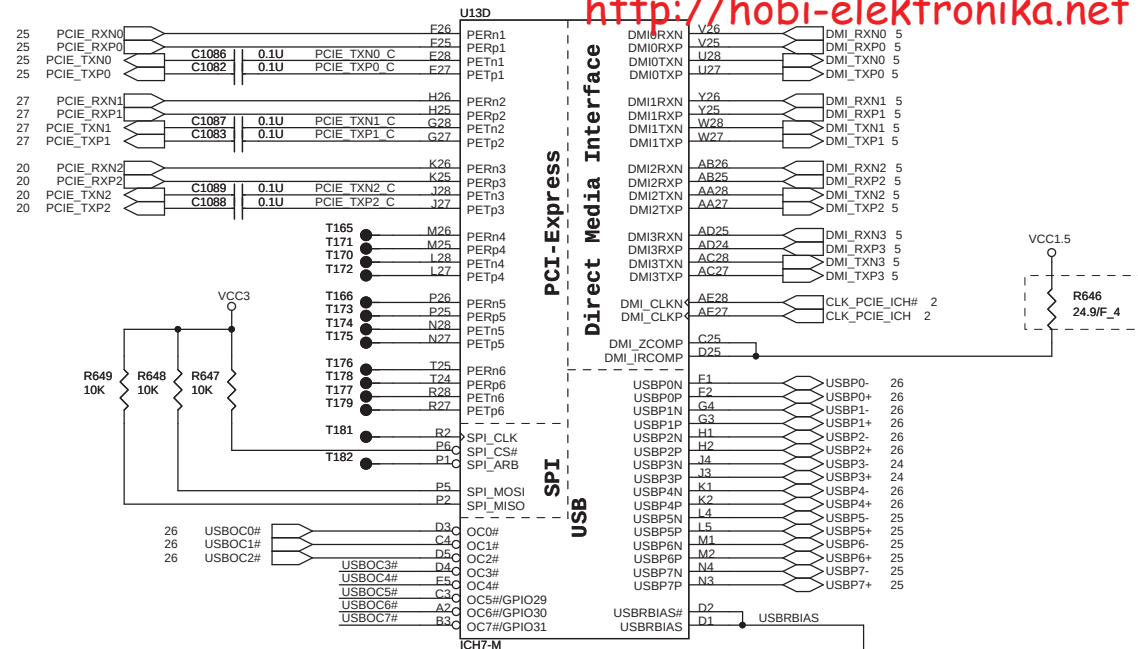
	INTVRMEN
Enable (default)	1
Disable	0

2. Purchase ink, paint, wire rods and molding resins only from the business partners that Sony approves as Green Partners.

Docking

Giga LAN

PCIe Mini

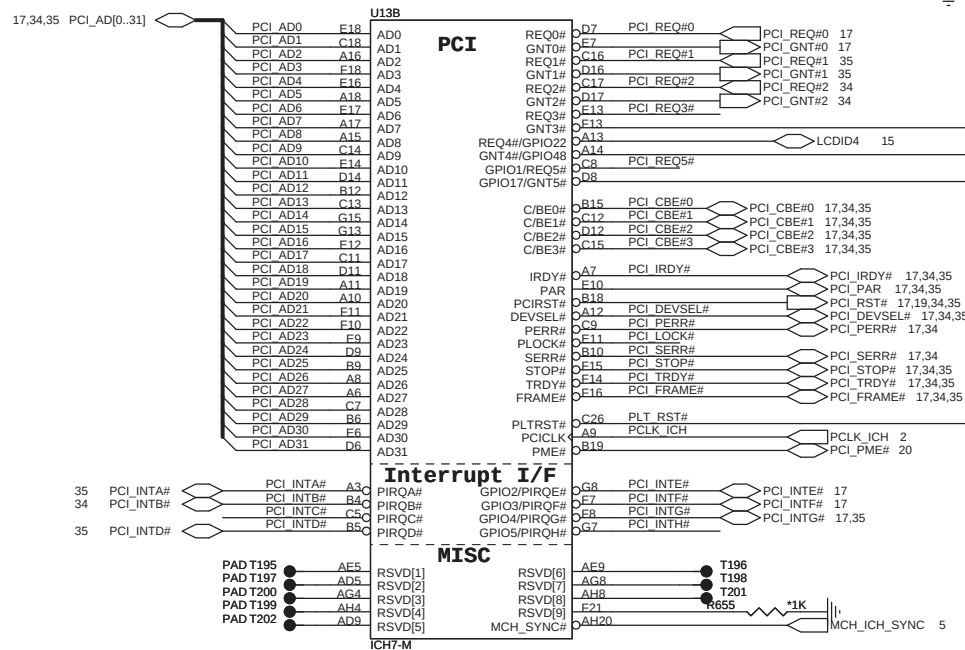


ICH7 Boot BIOS select

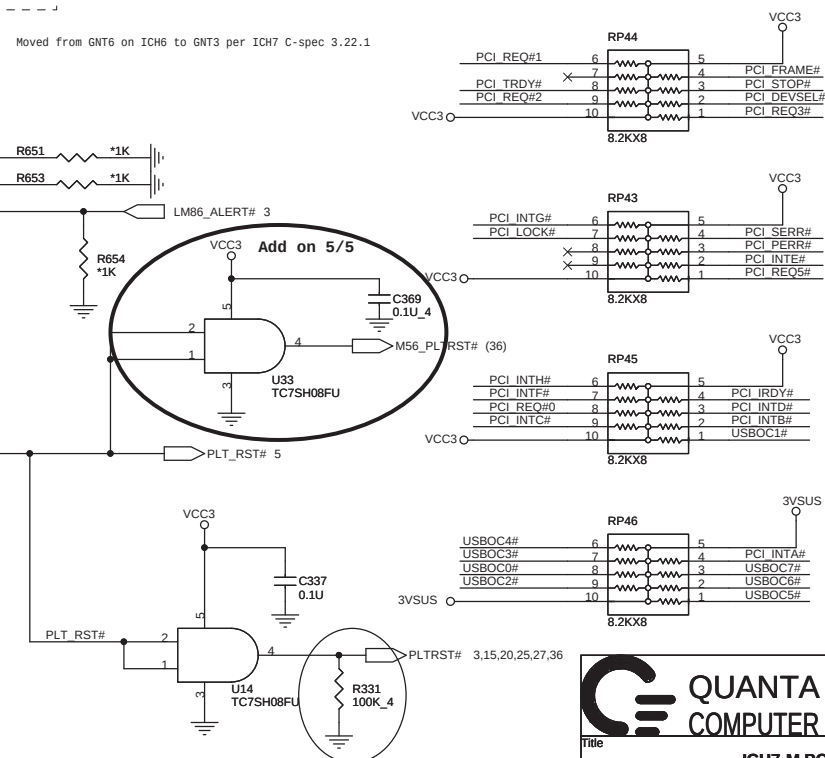
	STRAP	GNT5# R1	GNT4# R2
LPC (default)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF

PCI bus info.

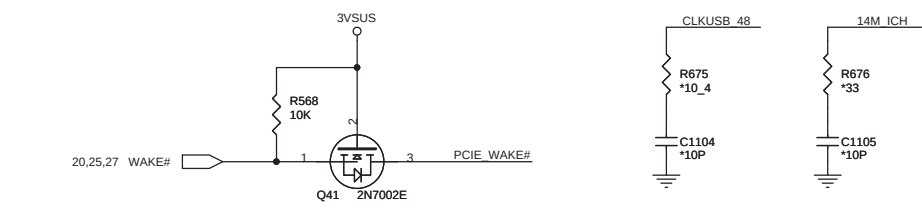
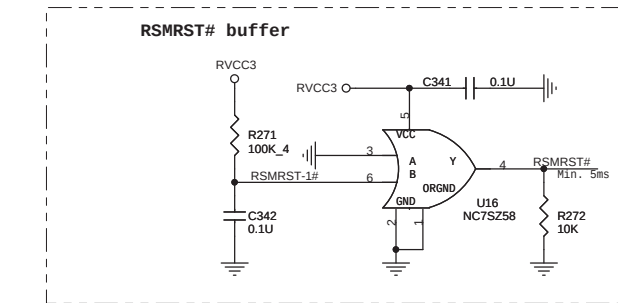
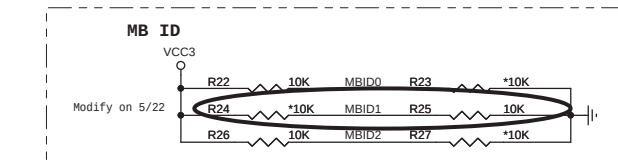
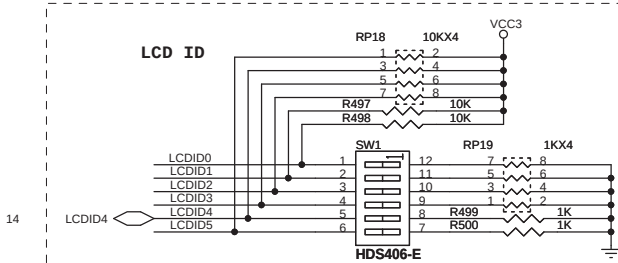
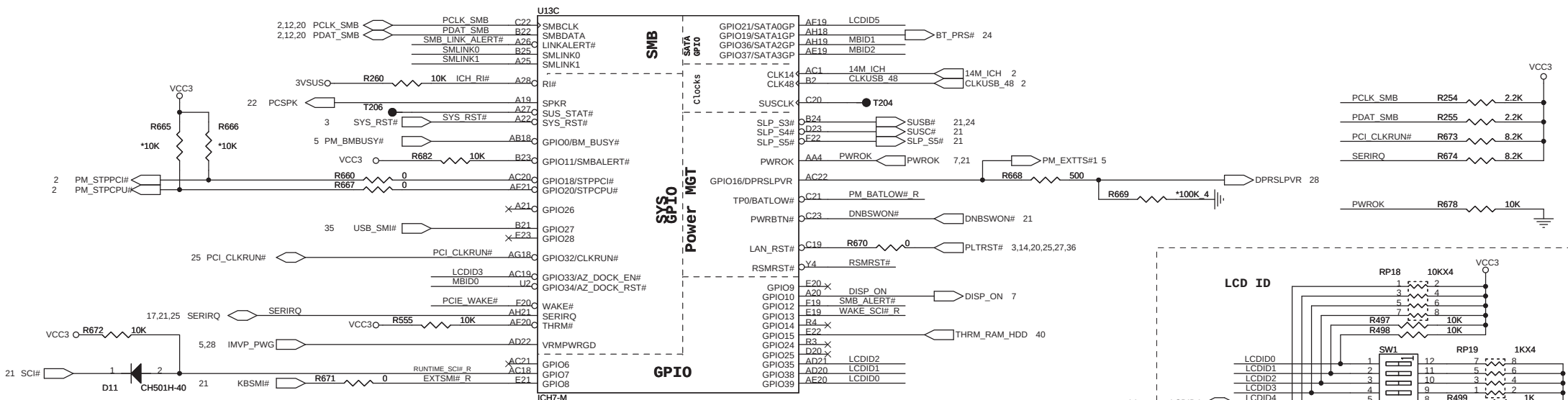
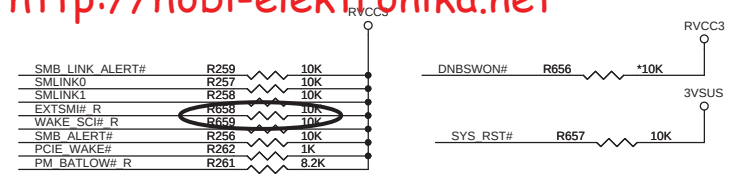
PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
PCI7411	AD25	REQ0# / GNT0#	PIRQ E/F/G
MINI-PCI_A	AD26	REQ3# / GNT3#	PIRQ C/H
SiI3512	AD24	REQ2# / GNT2#	PIRQ B
VT6212	AD27	REQ1# / GNT1#	PIRQ A/D

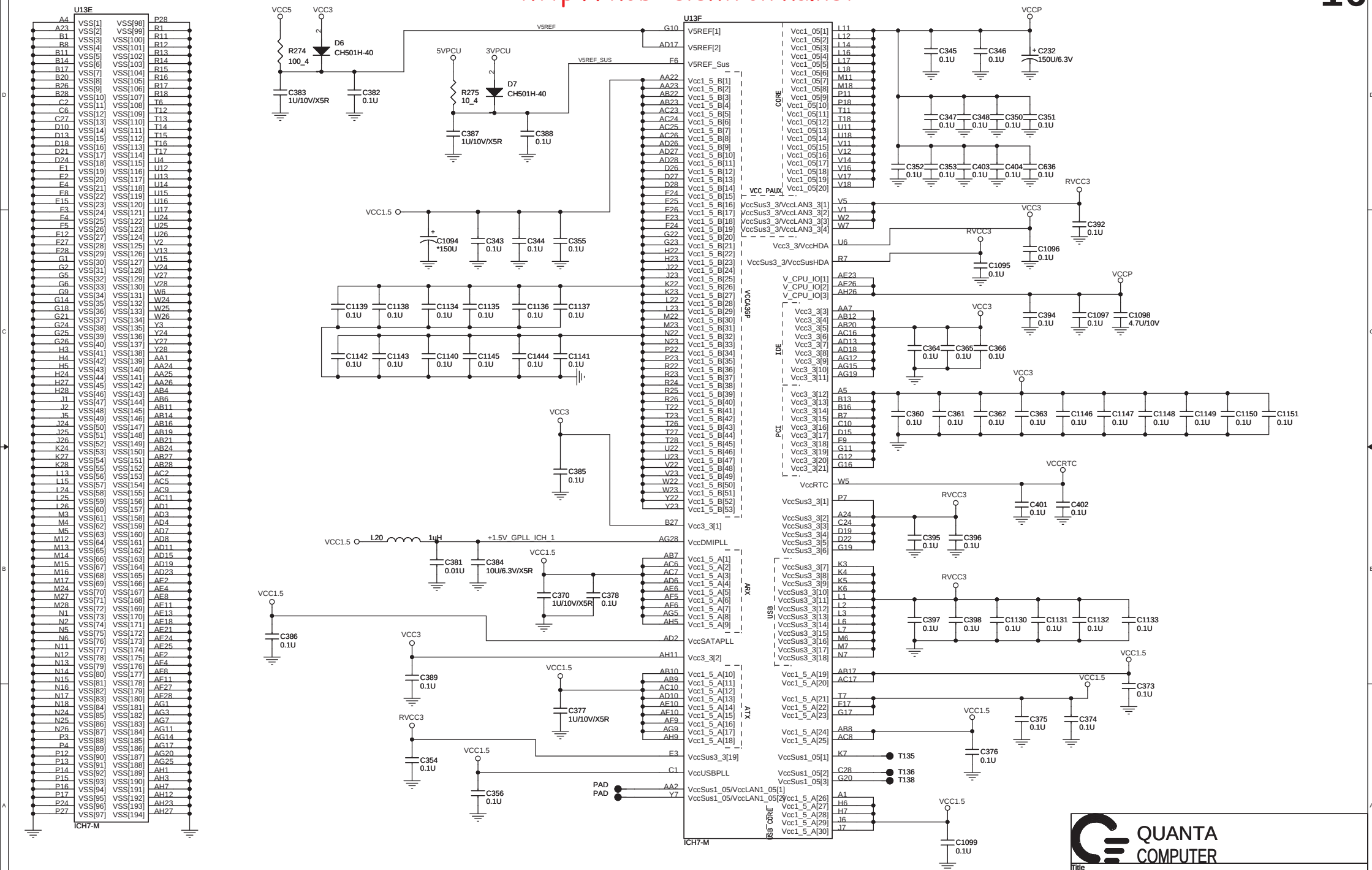


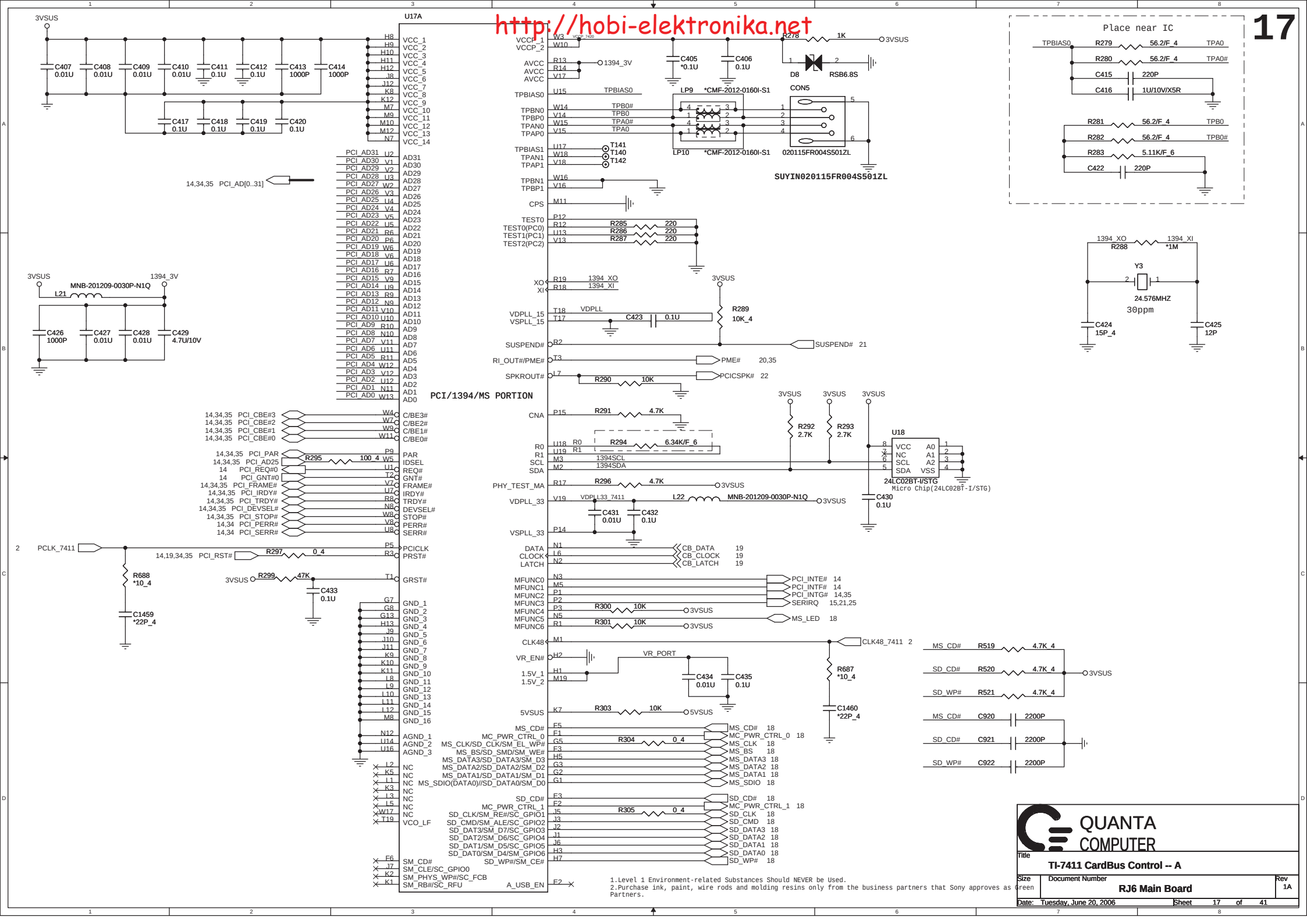
Moved from GNT6 on ICH6 to GNT3 per ICH7 C-spec 3.22.1

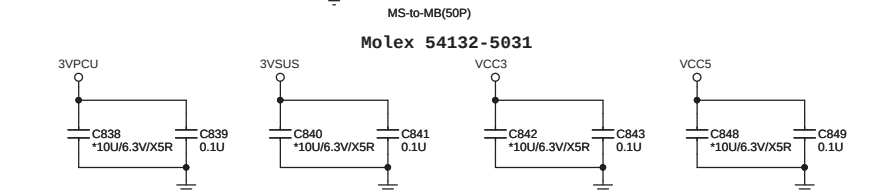
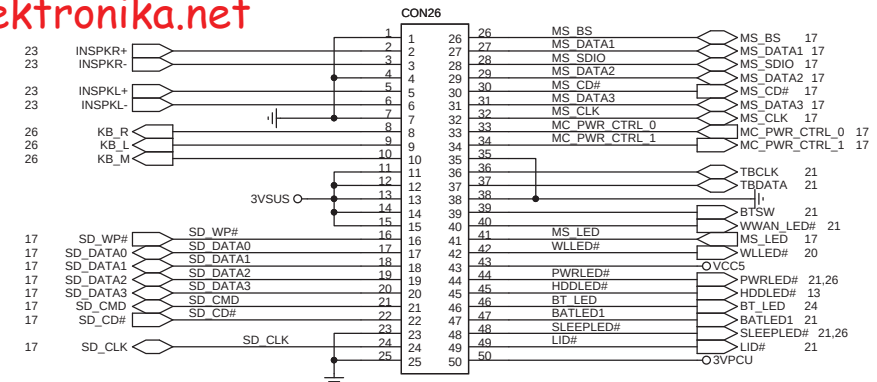
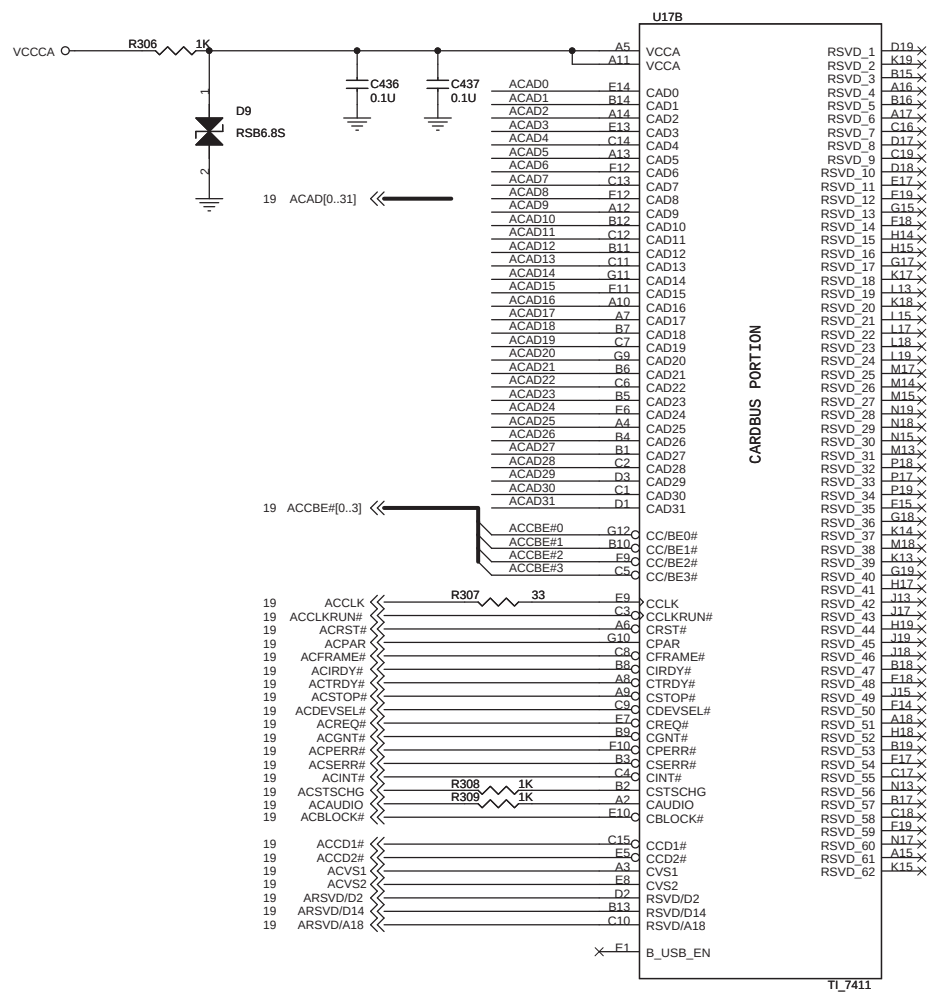
QUANTA
COMPUTER

Title			ICH7-M PCIE 2 of 4		
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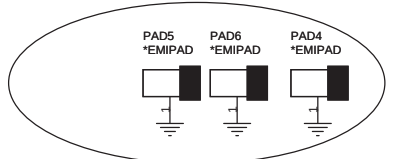
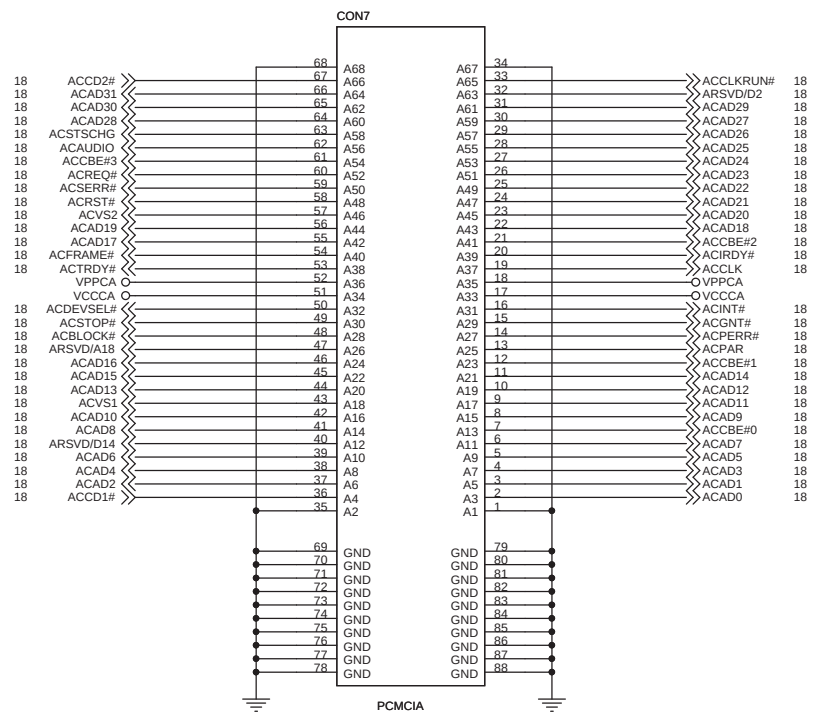




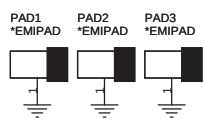


1.Level 1 Environment-related Substances Should NEVER be Used.
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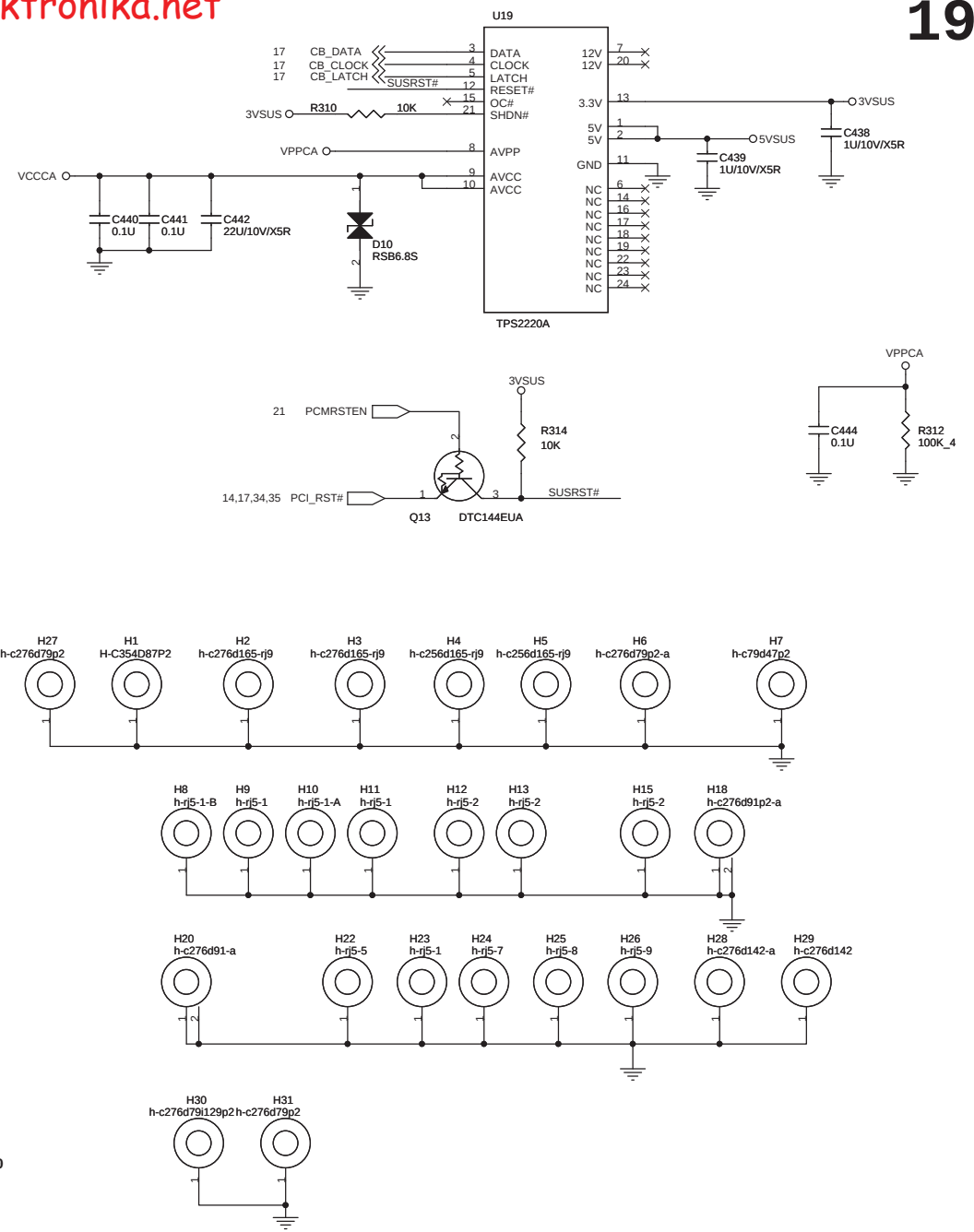
18 ACAD[0..31] <<==
18 ACCBE#[0..3] <<==



For Docking



Reserve for EMI 3/30





QUANTA
COMPUTER

Title
CARDBUS SLOT

Size
Document Number

RJ9 Main Board

Rev
1A

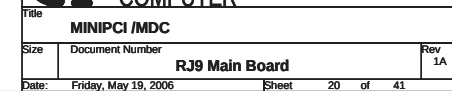
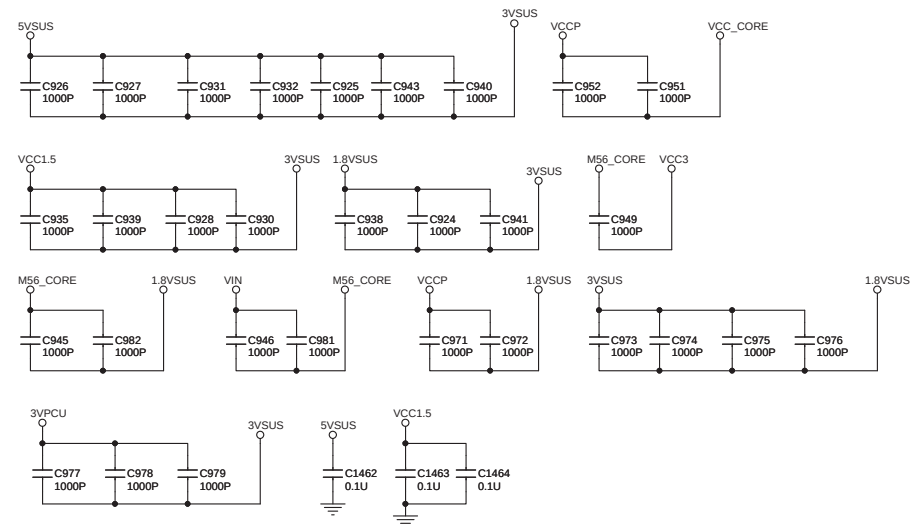
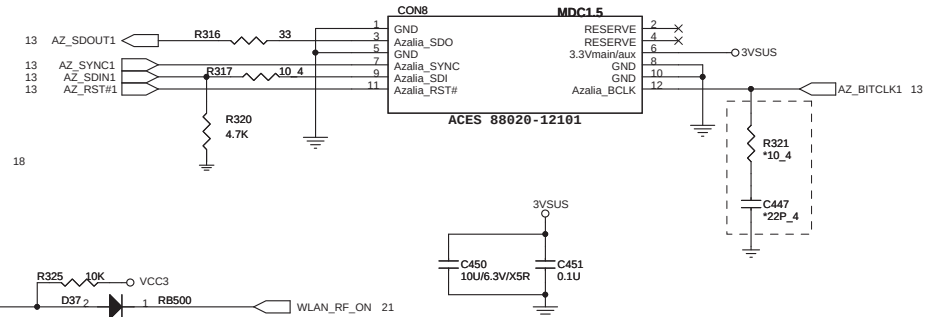
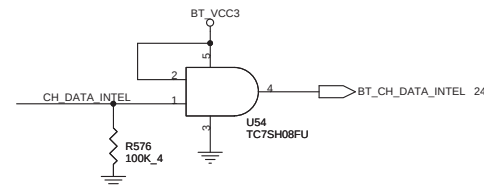
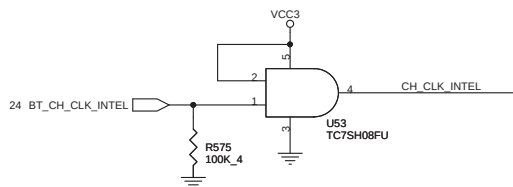
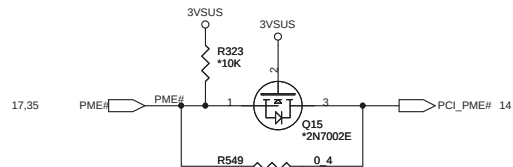
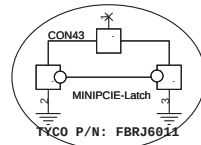
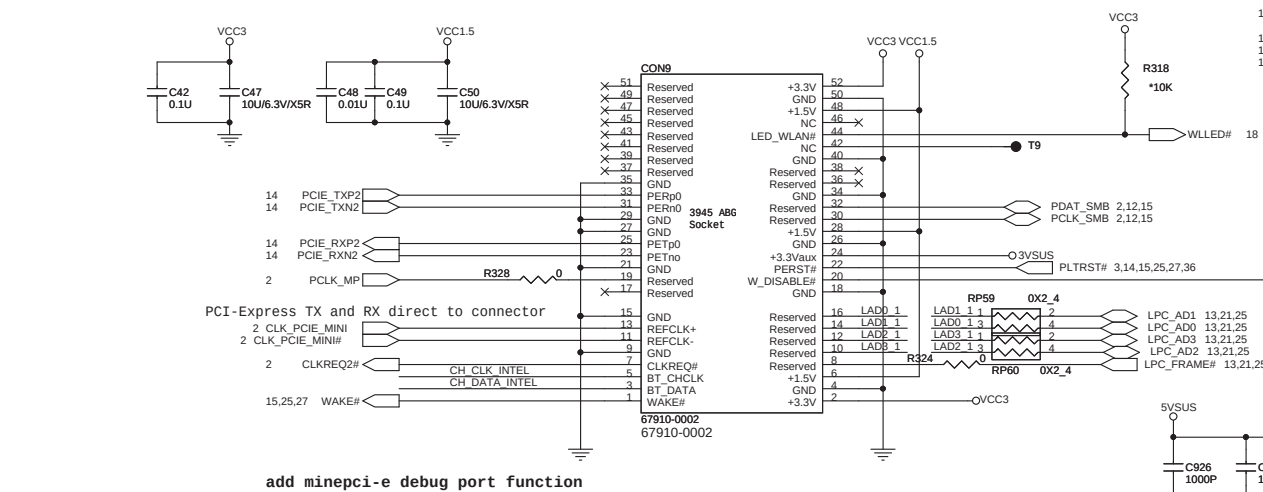
Date: Tuesday, June 20, 2006

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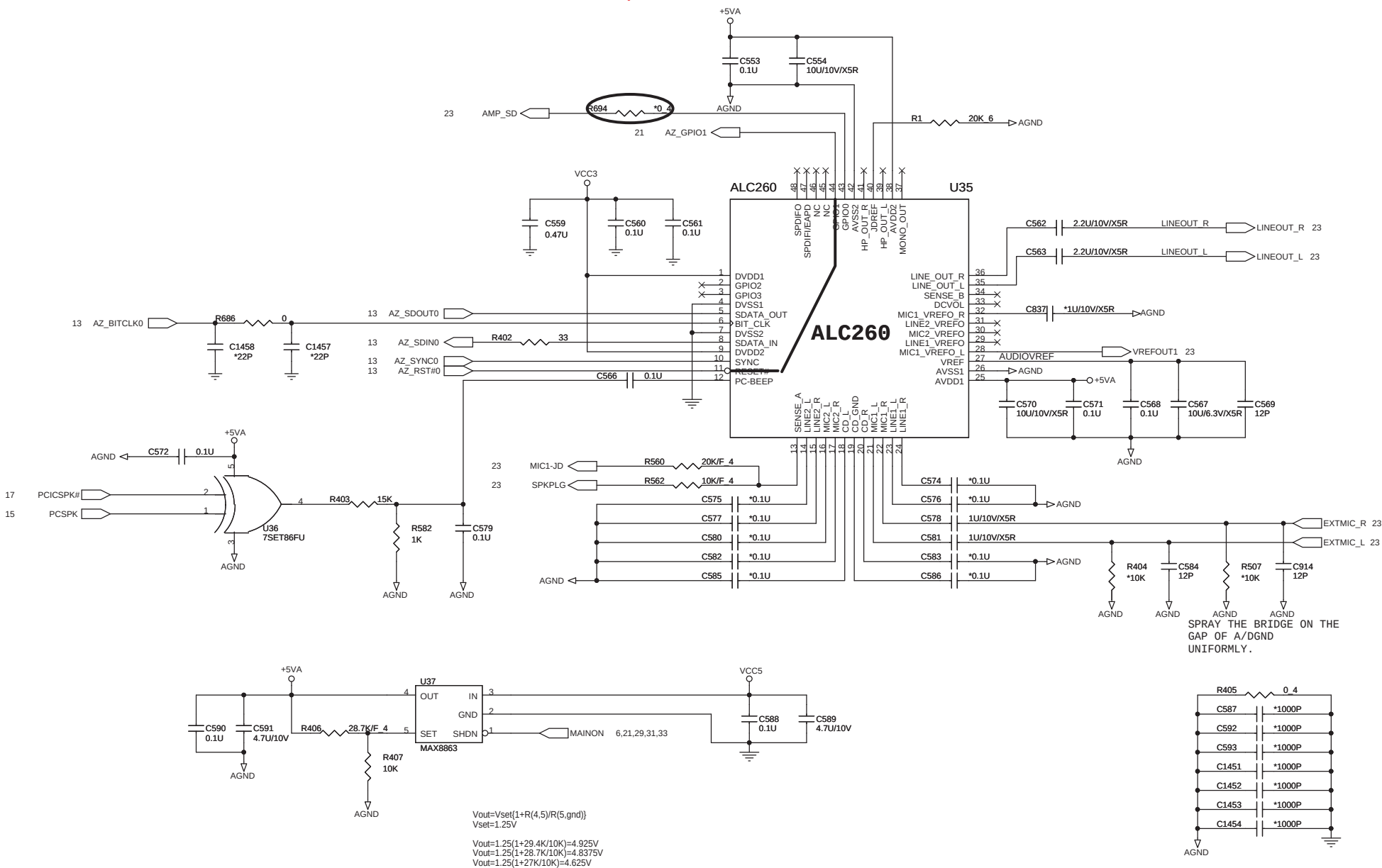
1.Level 1 Environment-related Substances Should NEVER be Used.
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```
WLSW:
Low  : disable the radio.
High : Enable the radio.
```

Mini PCI-E Card



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$$V_{out} = V_{set} \left(1 + R(4,5) / R(5, gnd) \right)$$

$$V_{set} = 1.25V$$

$$V_{out} = 1.25(1 + 29.4K / 10K) = 4.925V$$

$$V_{out} = 1.25(1 + 28.7K / 10K) = 4.8375V$$

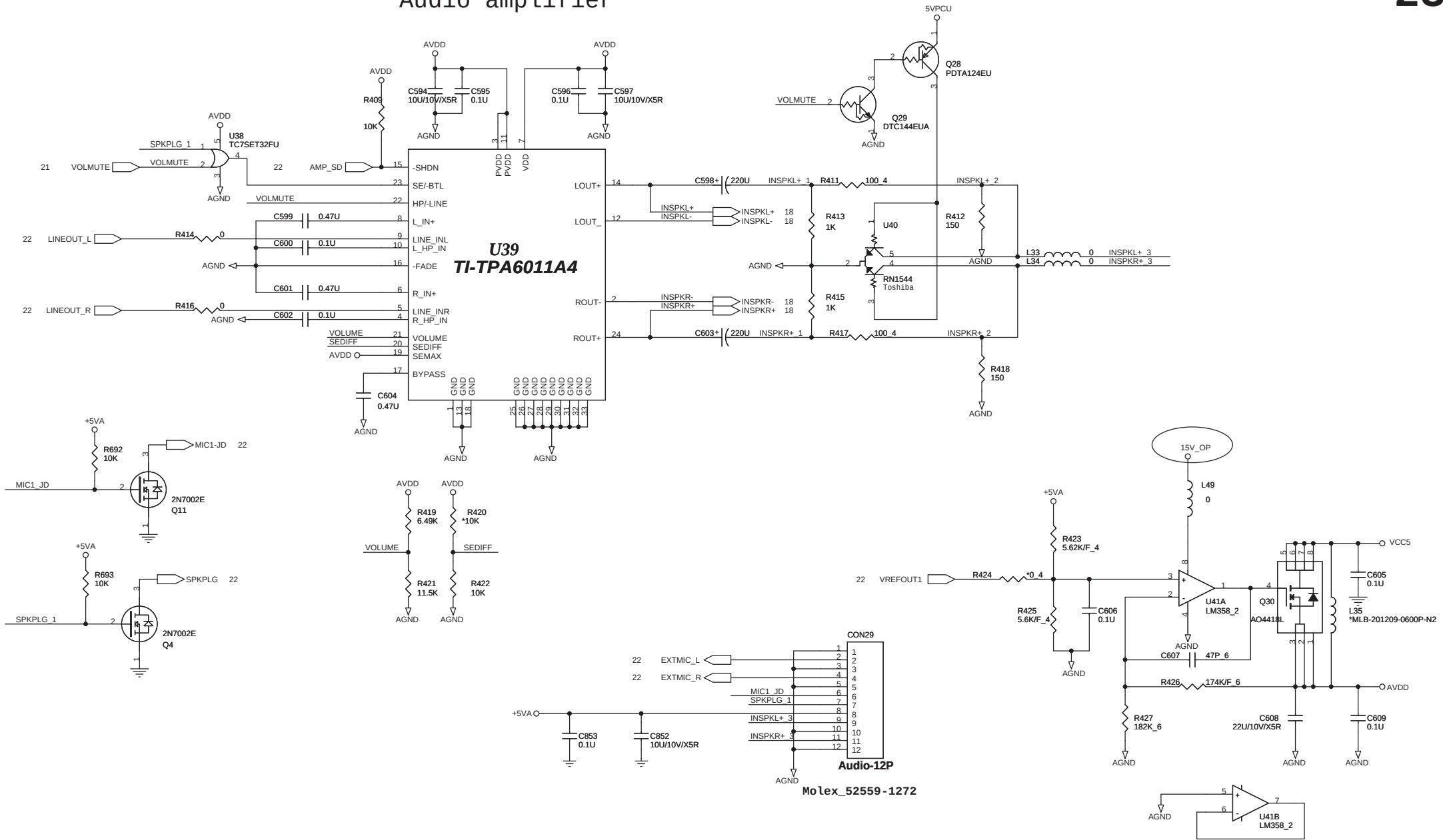
$$V_{out} = 1.25(1 + 27K / 10K) = 4.625V$$

QUANTA COMPUTER

Title: **Audio ALC260**

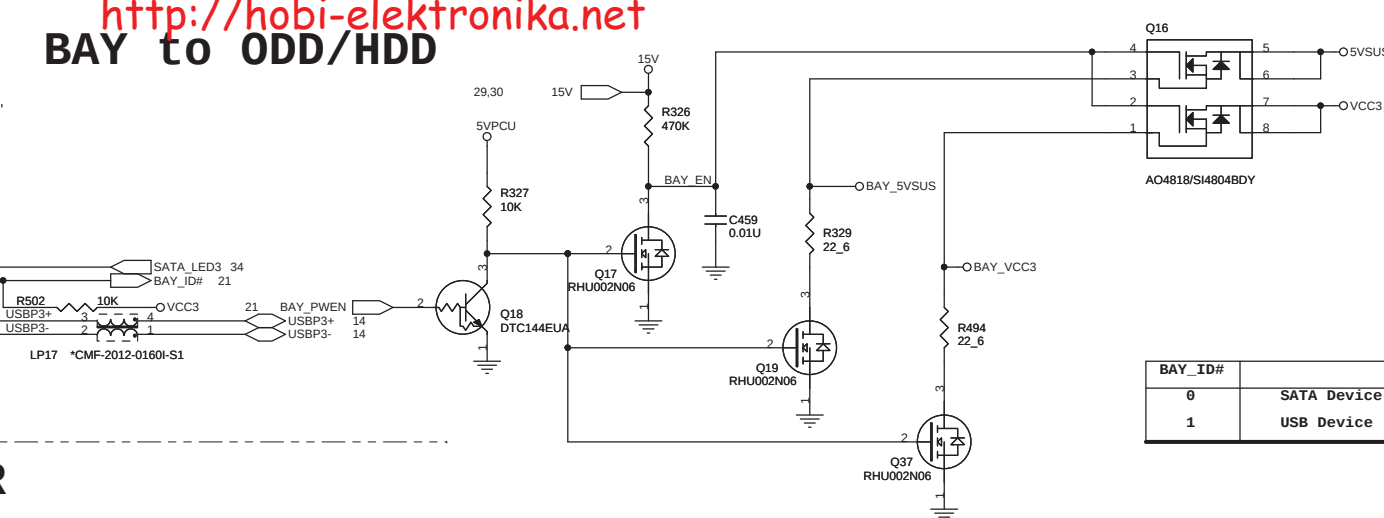
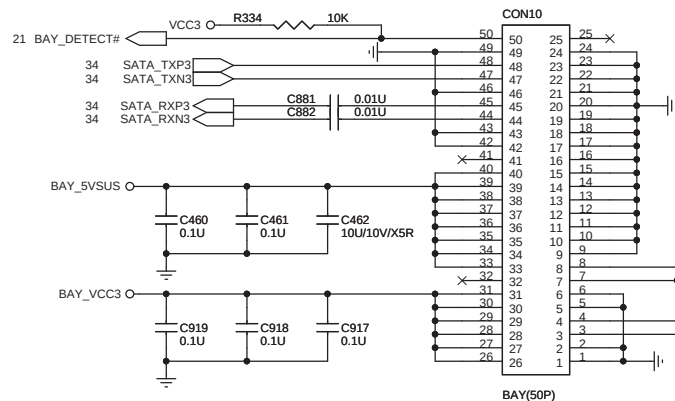
Size: Document Number **RJ6 Audio Board** Rev 1A

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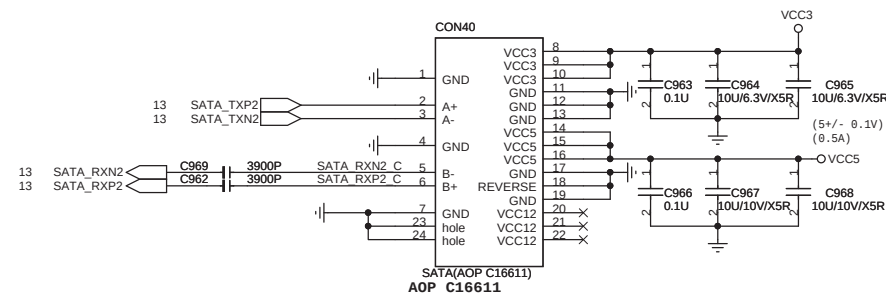
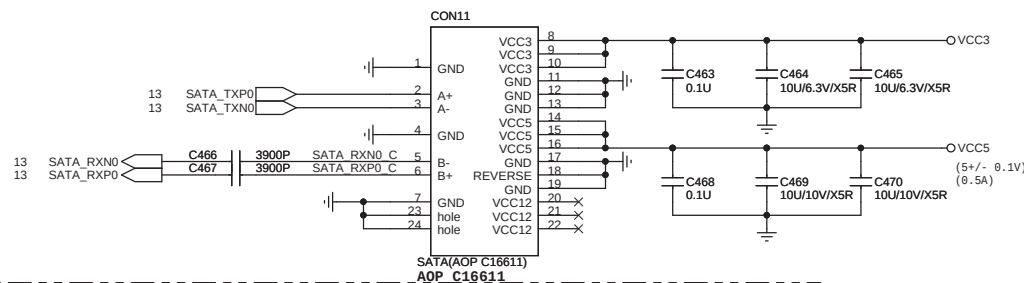


R419	FROM	TO	GAIN
7.5K	2.85	2.89	8 dB
6.49K	2.96	3.0	10 dB

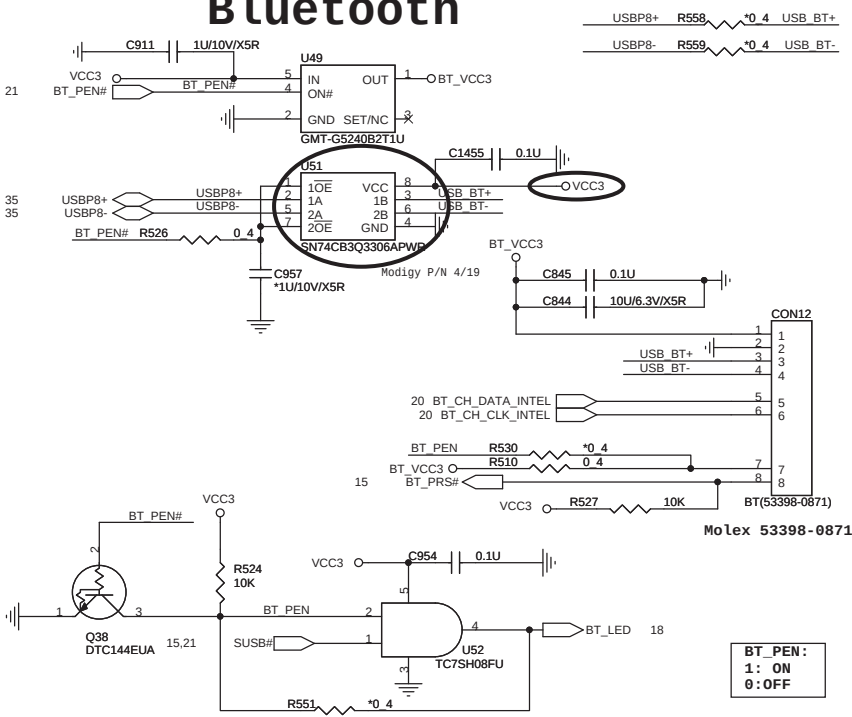
1.Level 1 Environment-related Substances Should NEVER be Used.
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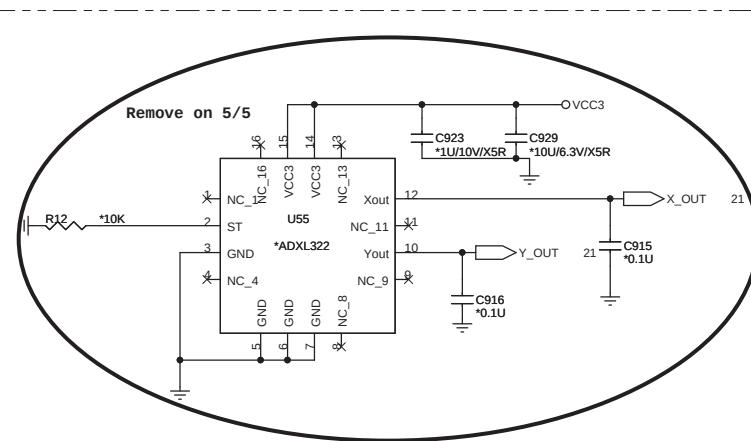
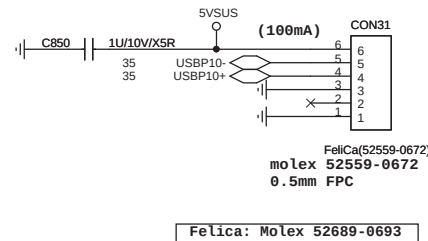
HDD CONNECTOR



Bluetooth



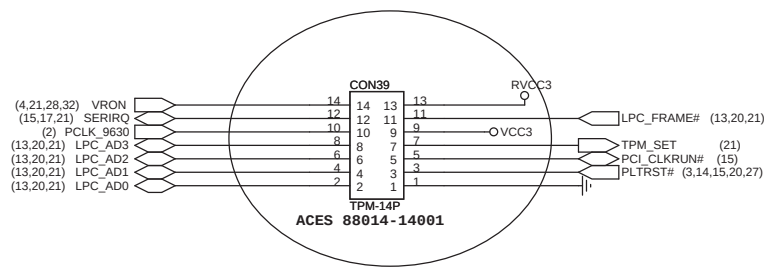
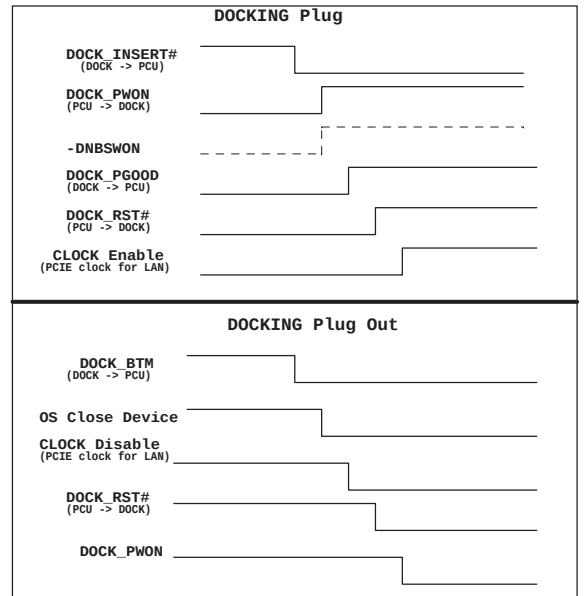
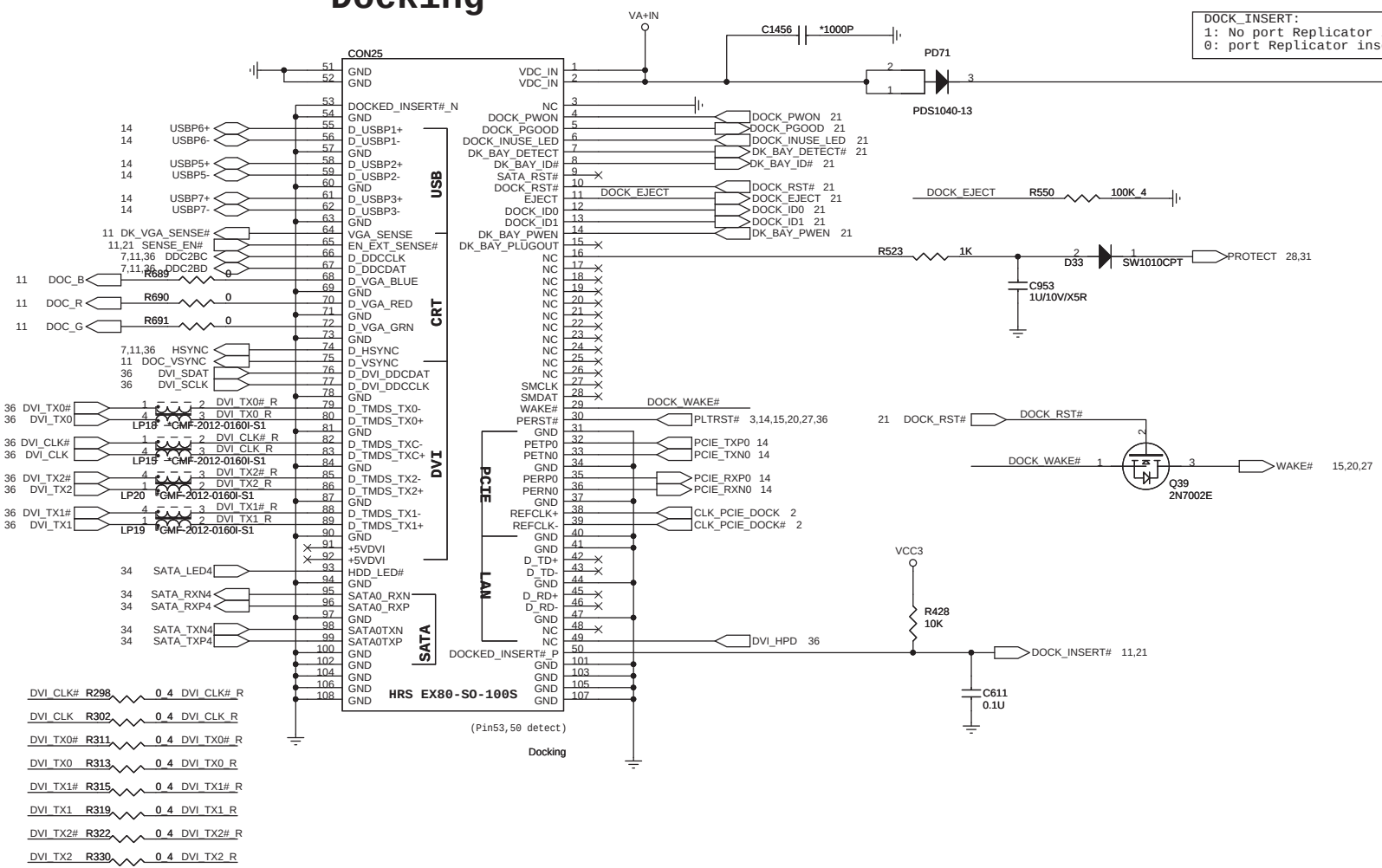
Felica



QUANTA
COMPUTER

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Docking





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Title

Docking/TPM

Size

Document Number

Rev 1A

Date

Tuesday, June 20, 2006

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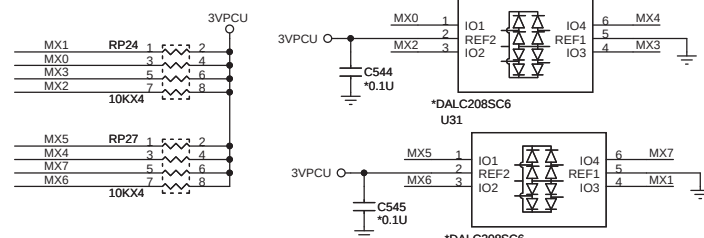
Rev 1A

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MOLEX(52610-2871)

Mollex 52610-2871



5VSUS

C958 1U/10V/X5R

C847 0.1U

CON27

1 1

2 2

3 3

4 4

5 5

USBP9- 3 USBP9- 4

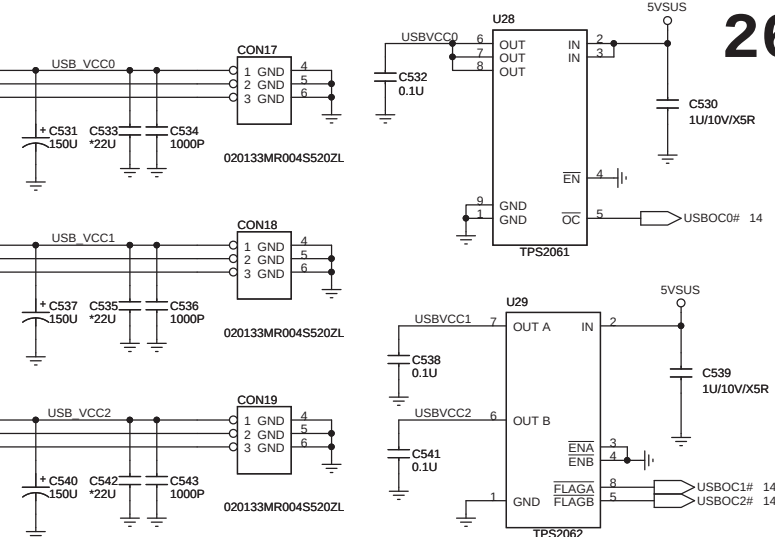
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LP16 *CMF-2012-0160L-S1

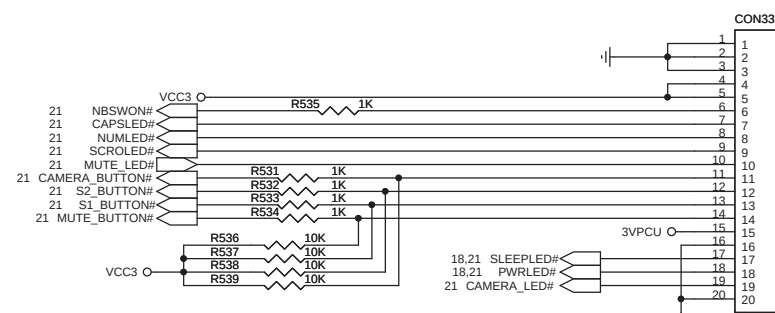
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Camera(53398-0571)

Molex 53398-0571

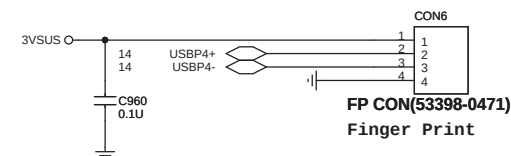
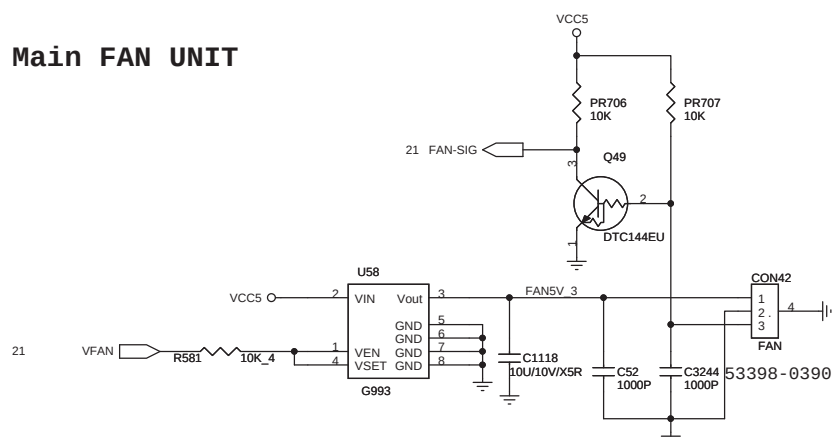


POWER SW BOARD



PS CON(52559-2070)
Mollex 52559-2070

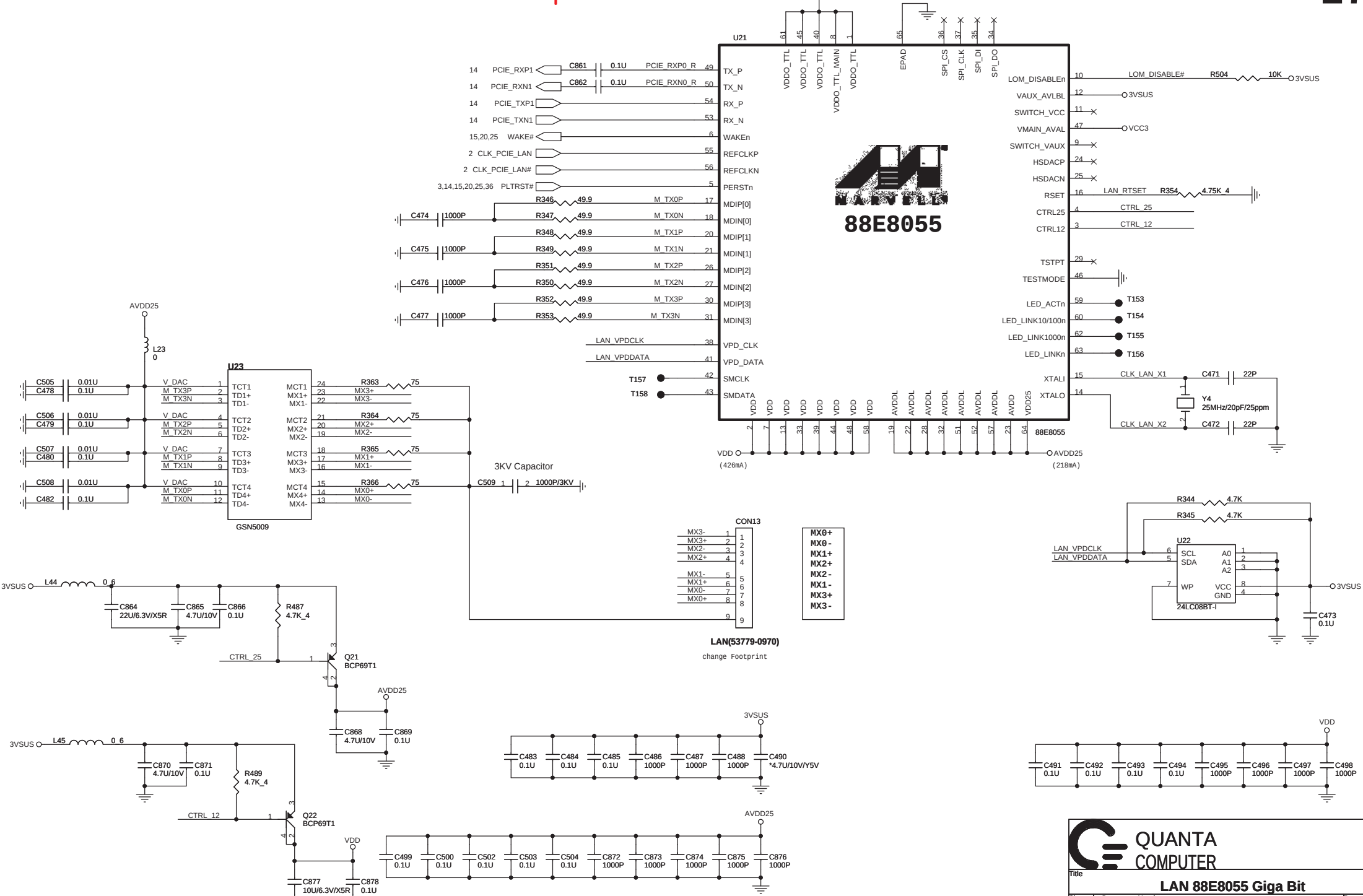
Main FAN UNIT



FP CON(53398-0471)
Finger Print



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K/B ,USB			
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Title

LAN 88E8055 Giga Bit

Size

Document Number

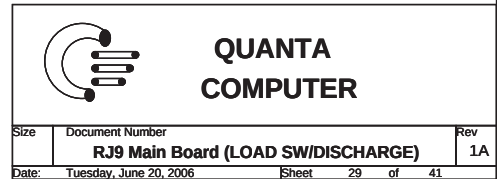
Rev 1A

Date

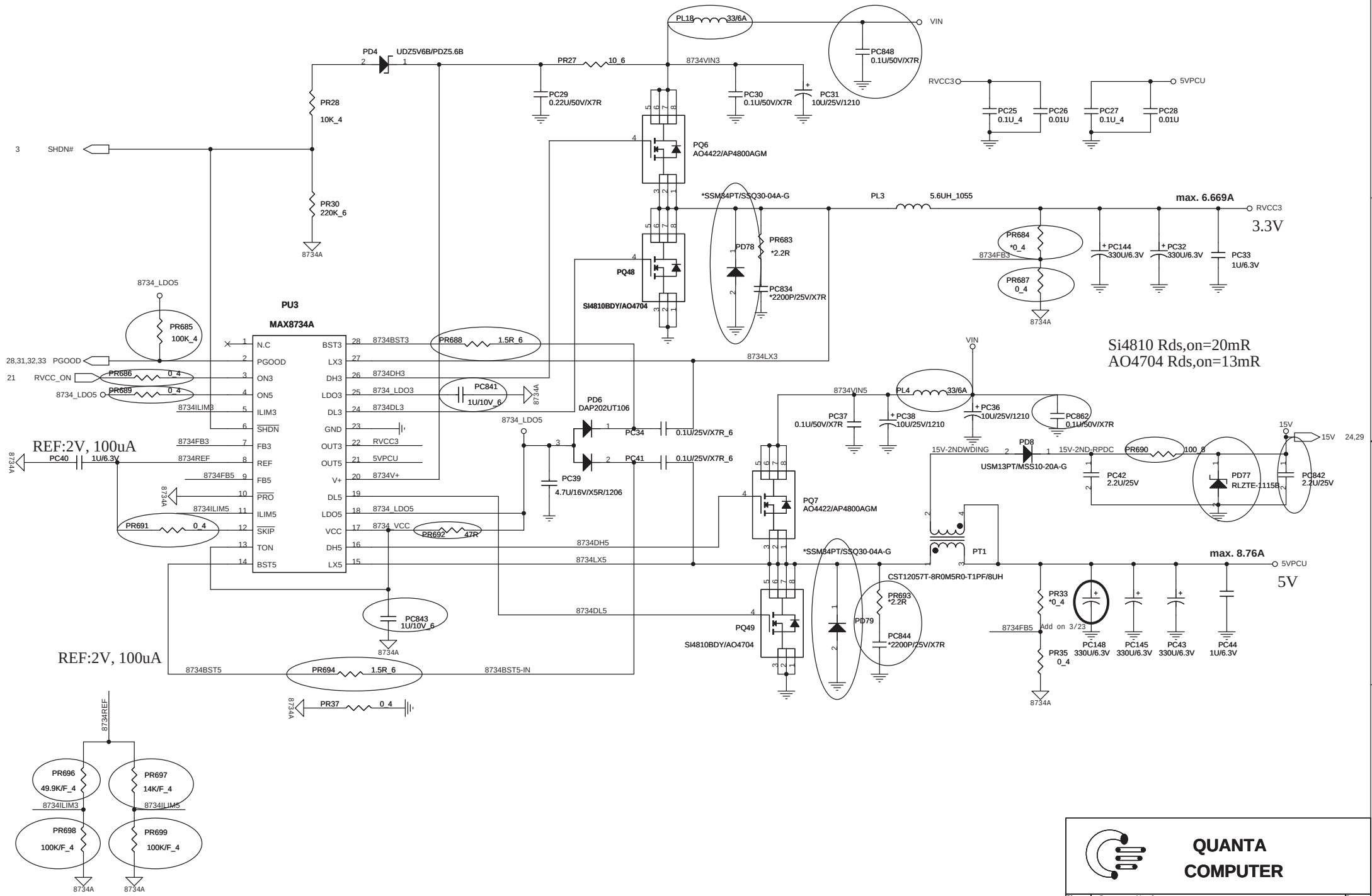
Tuesday, June 20, 2006

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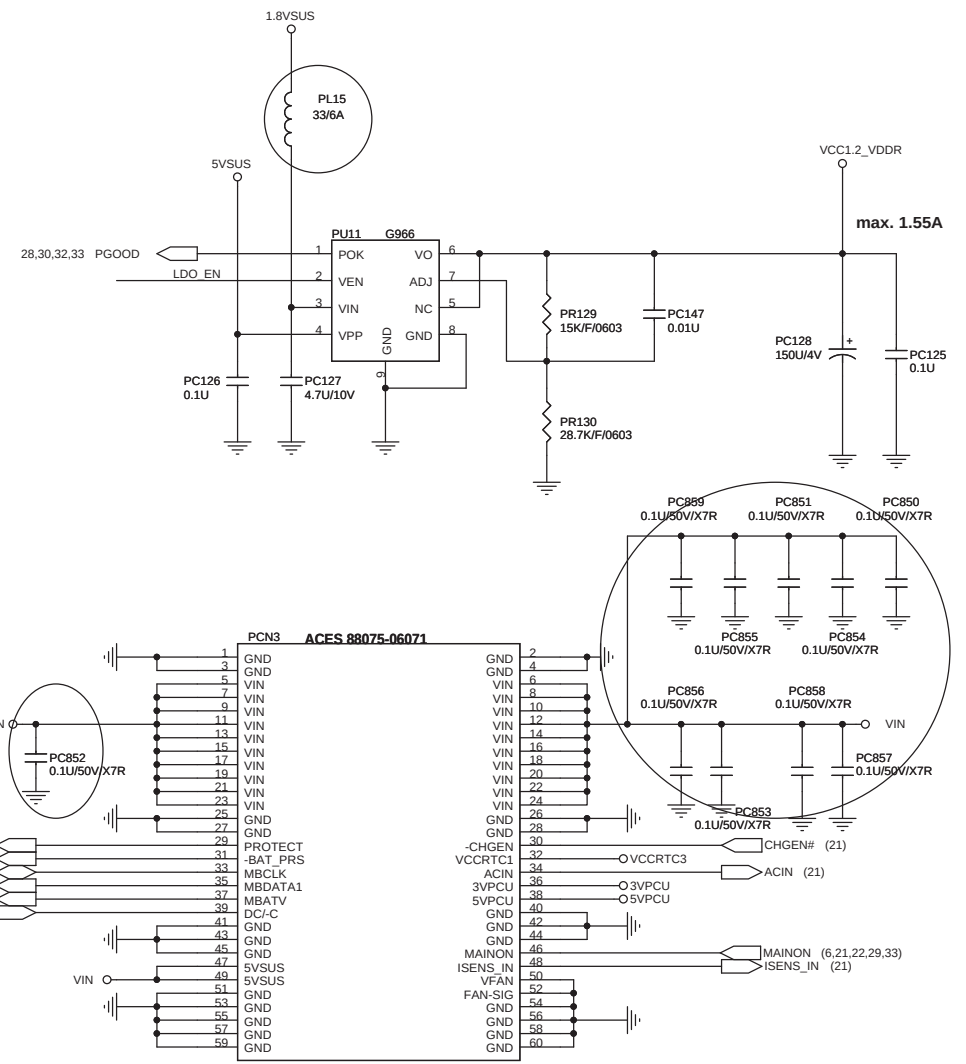
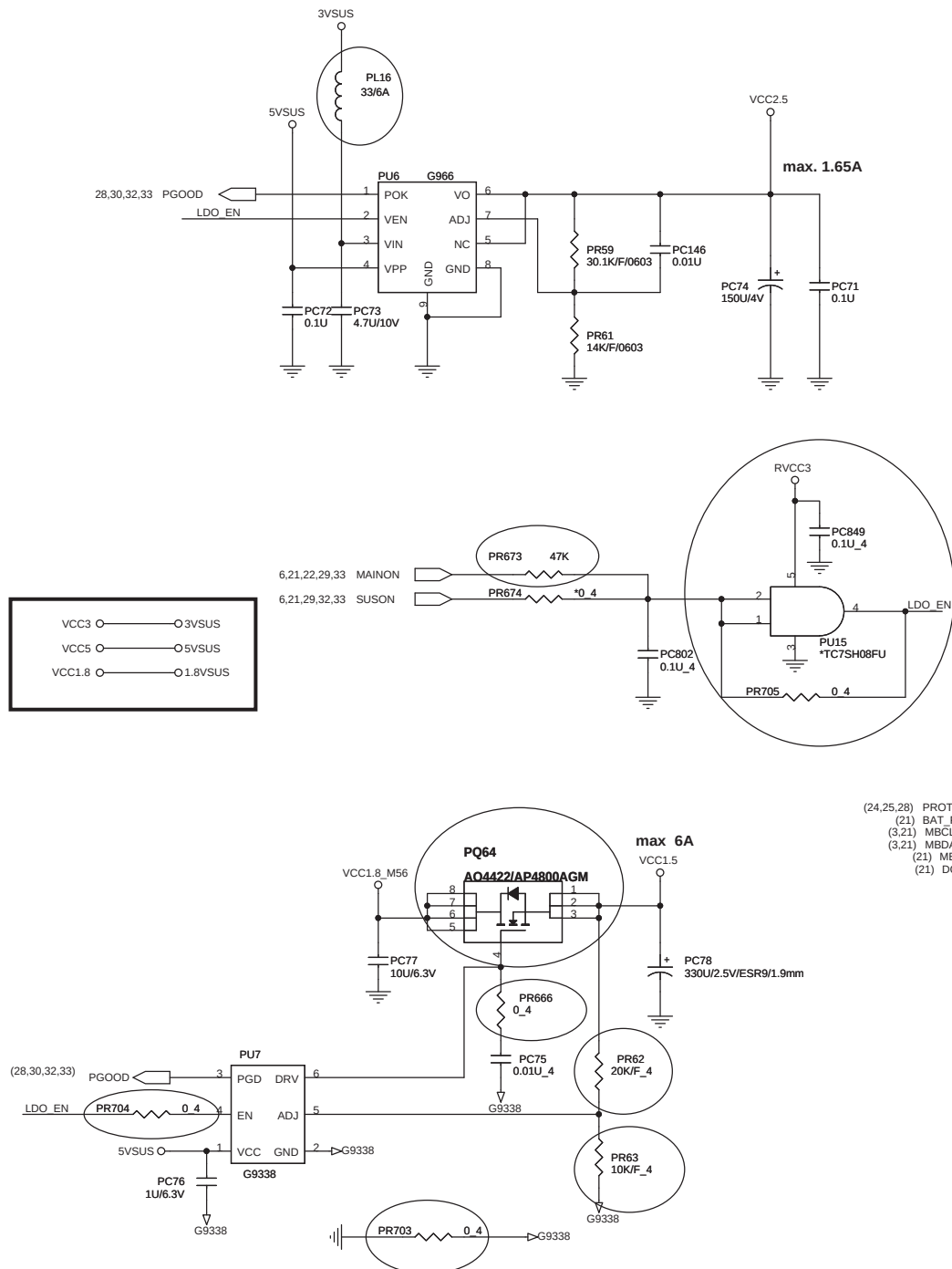
1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods and molding resins only from the business partners that Sony approves as Green Partners.



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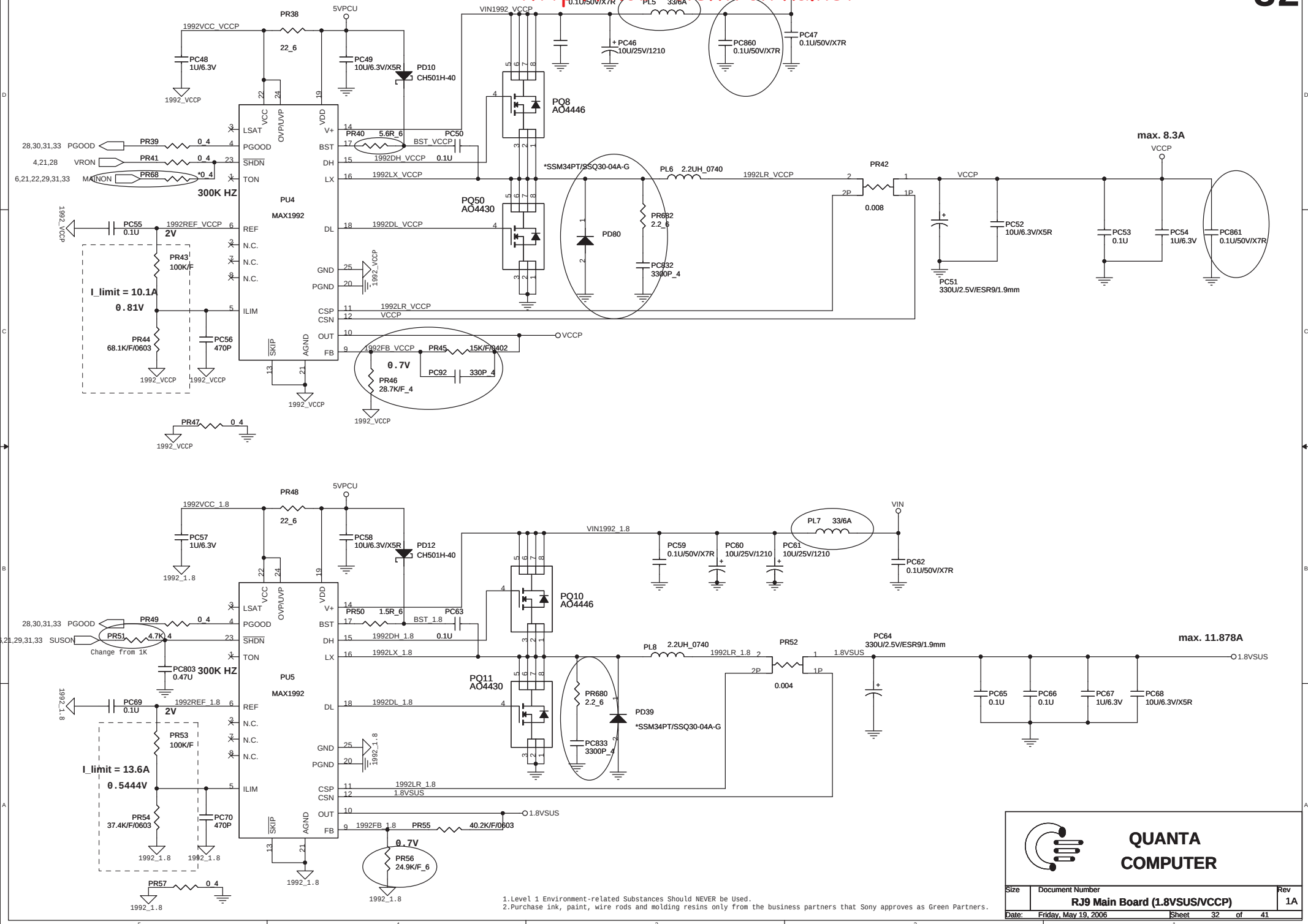




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1. Level 1 Environment-related Substances Should NEVER be Used.
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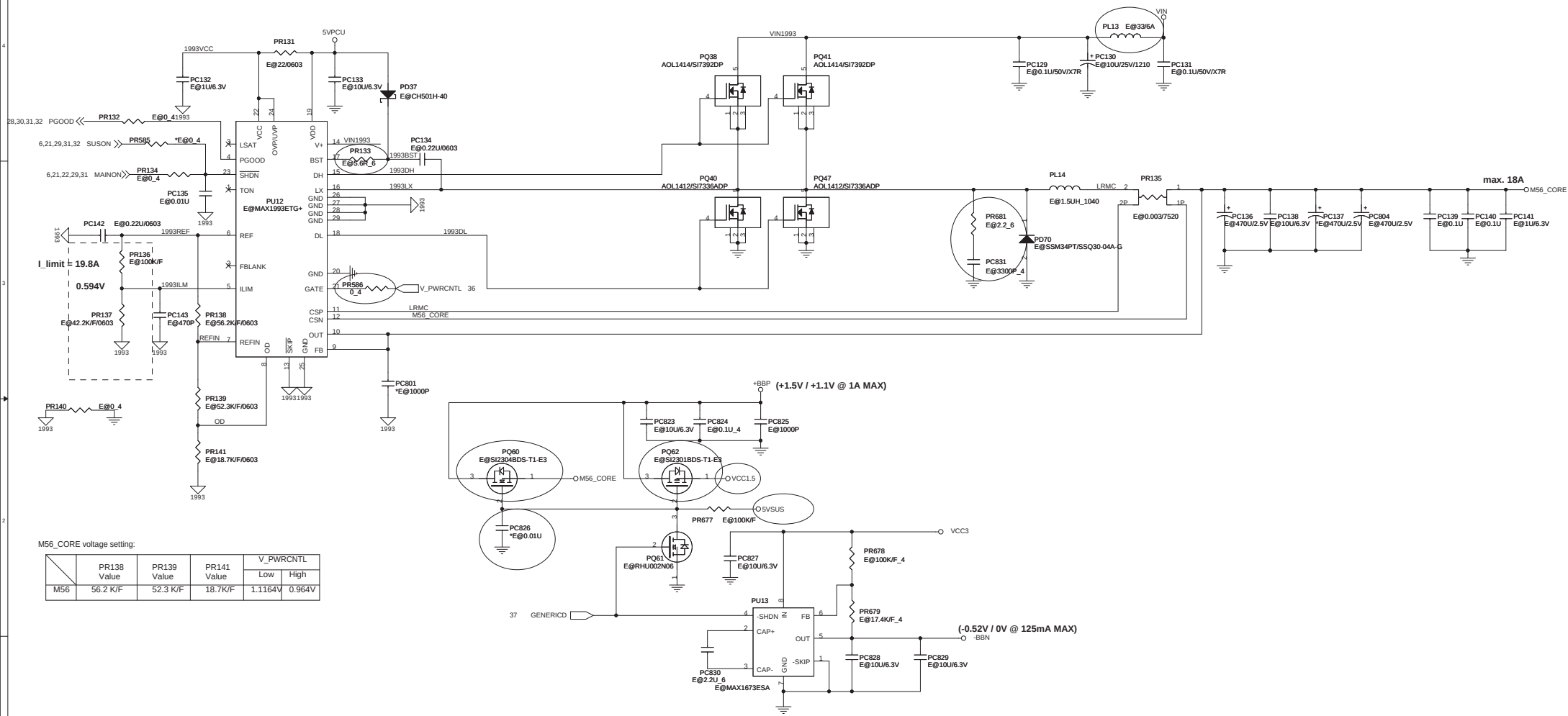


1.Level 1 Environment-related Substances should NEVER be Used.
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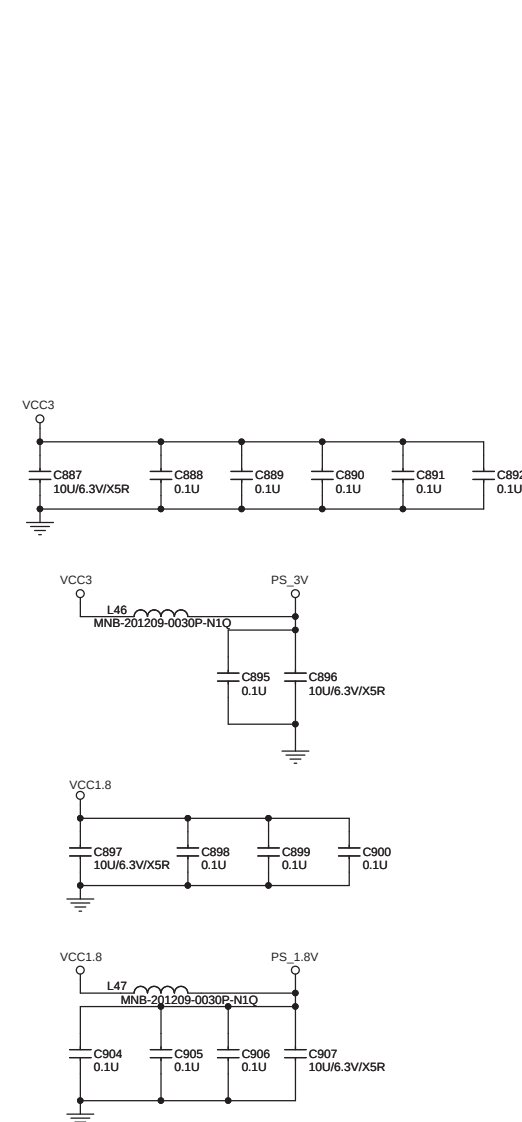


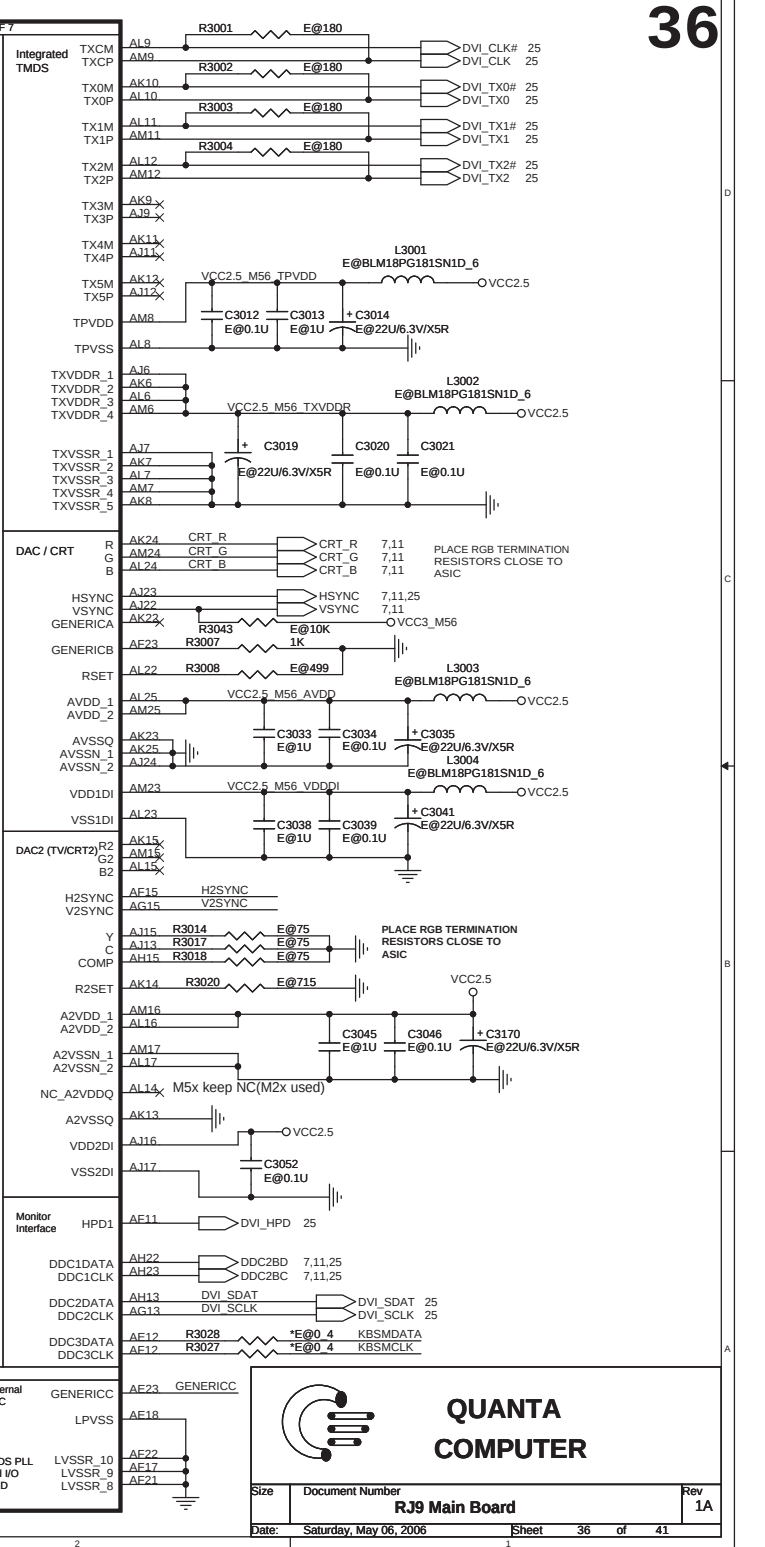
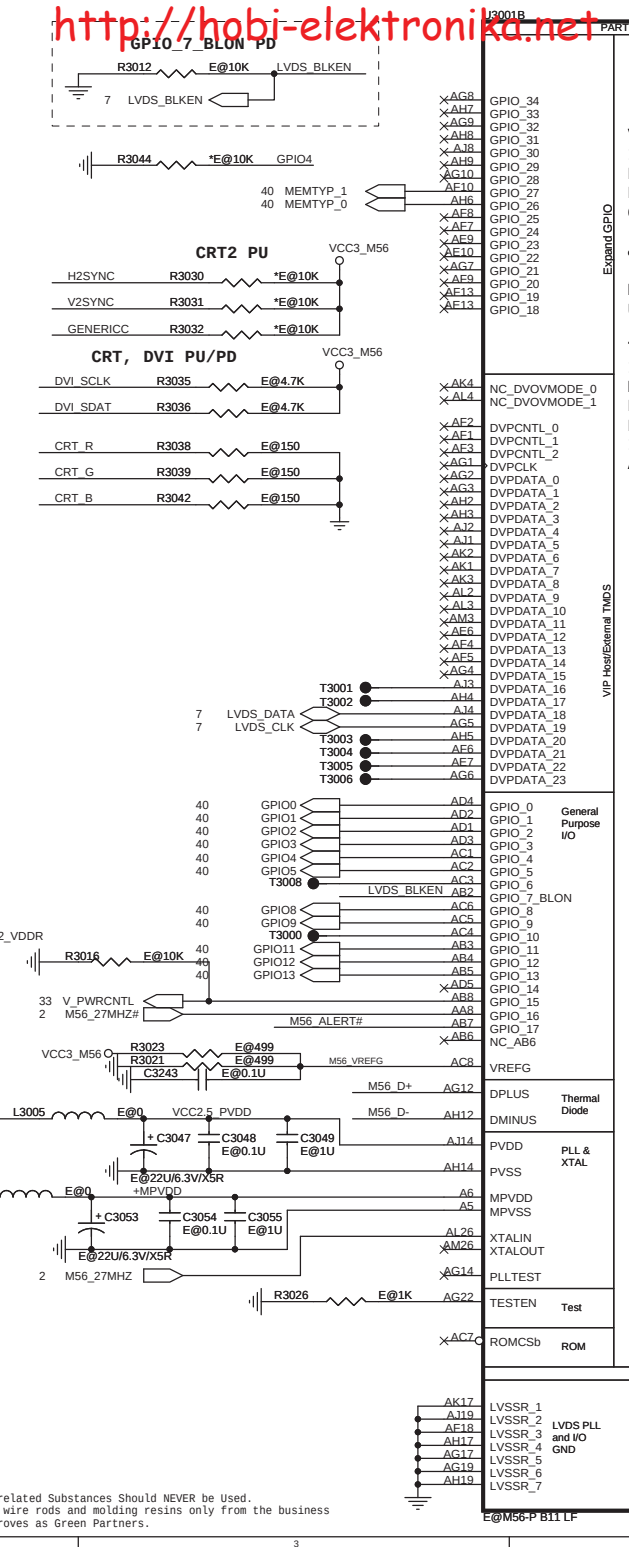
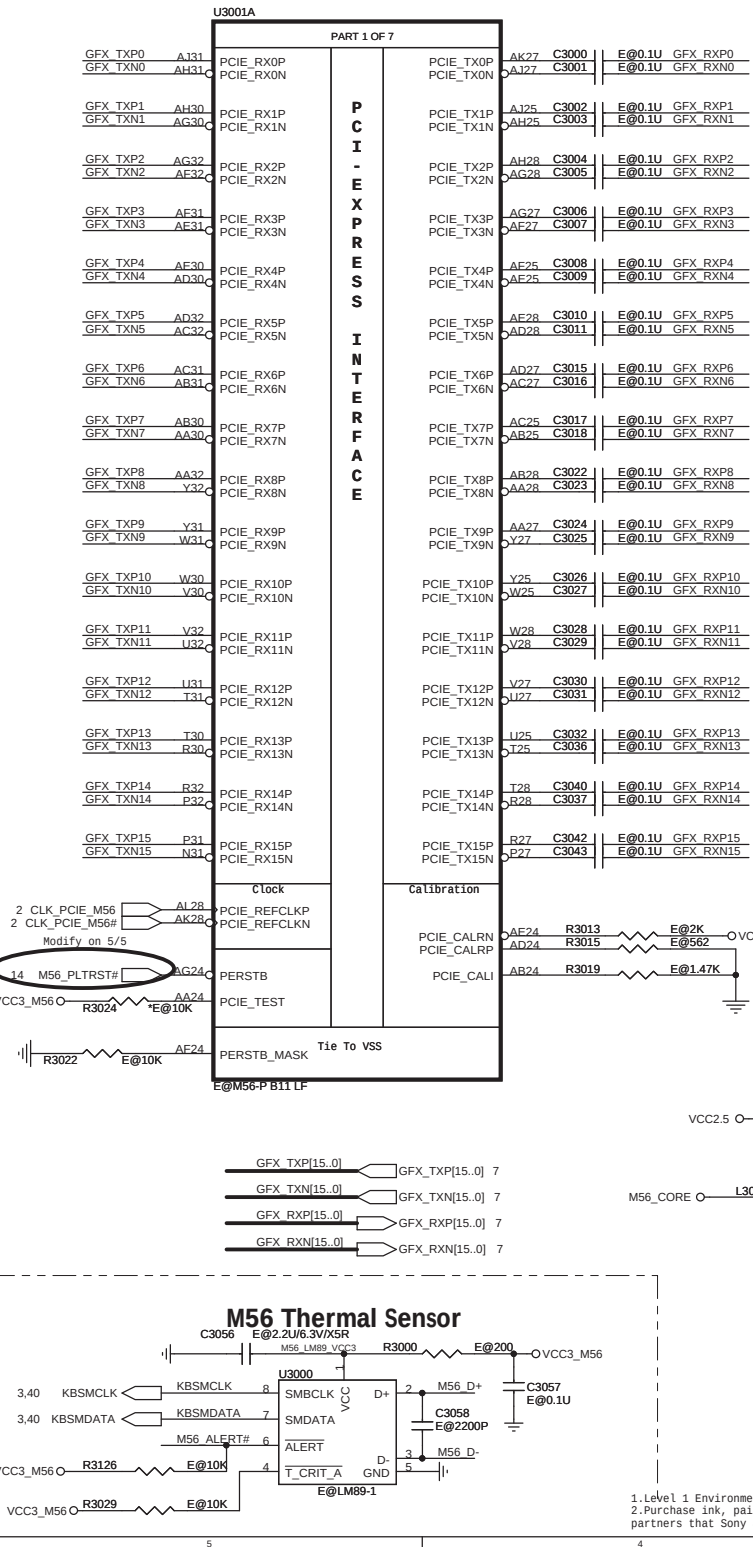
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	R.J9 Main Board (1.8VSUS/VCCP)	1A
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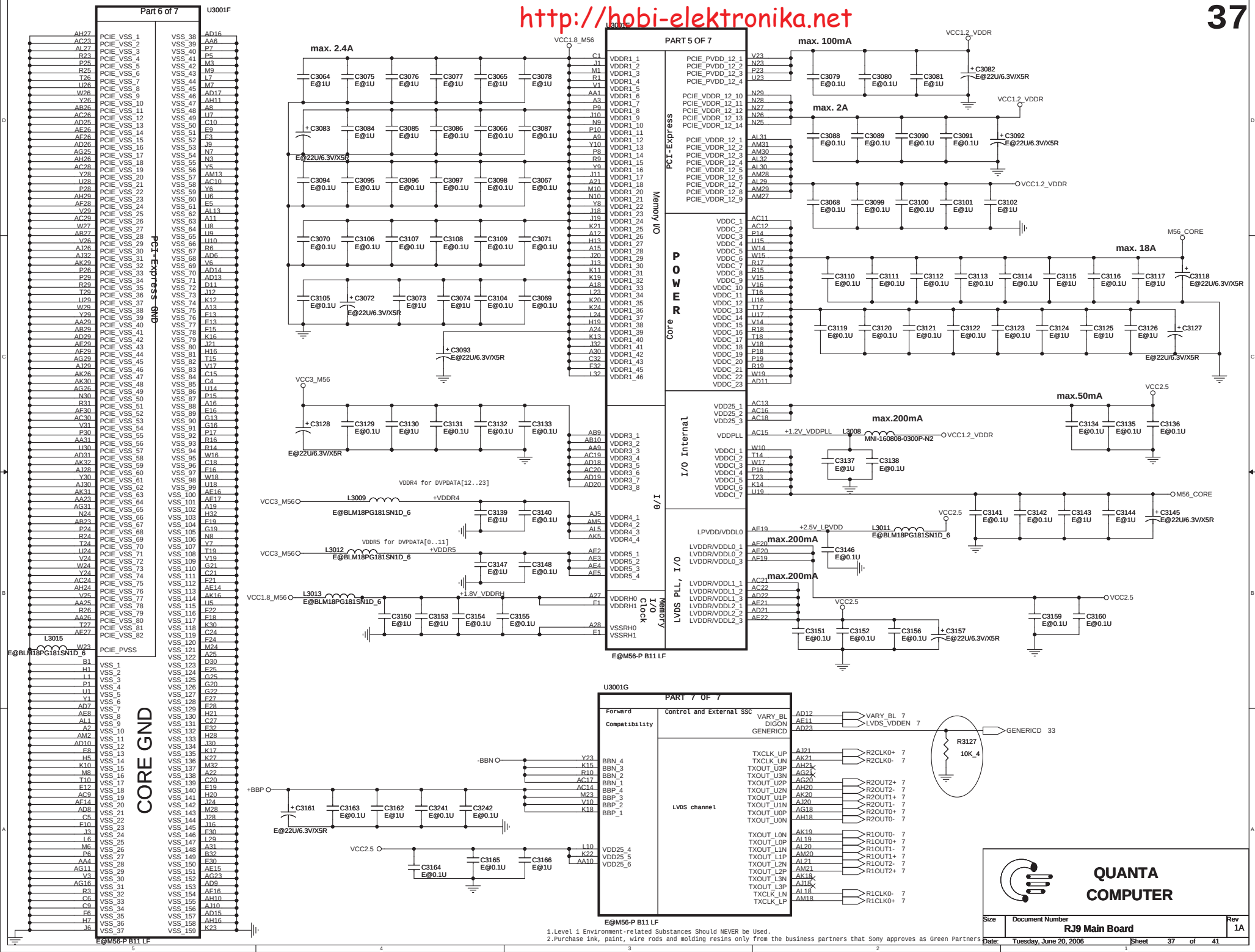


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1. Level 1 Environment-related Substances Should NEVER be Used.
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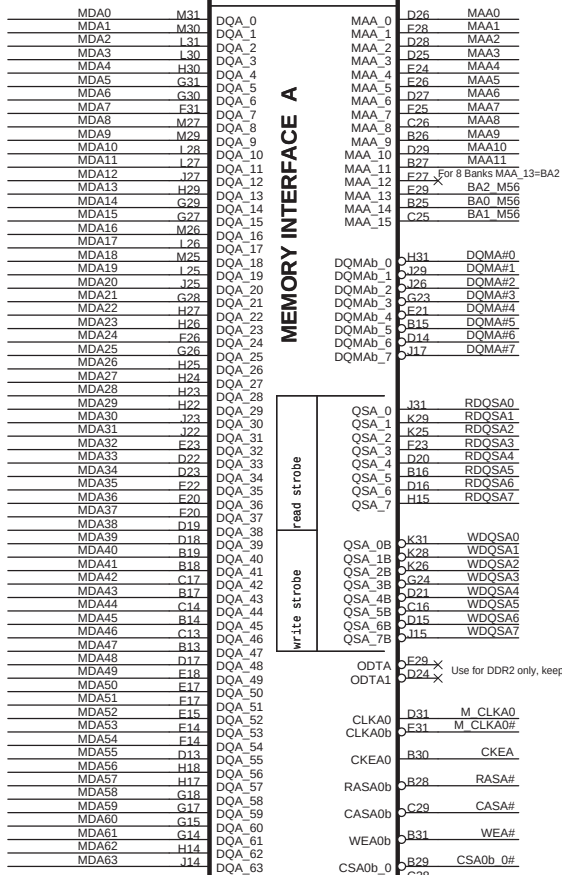


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Channel A

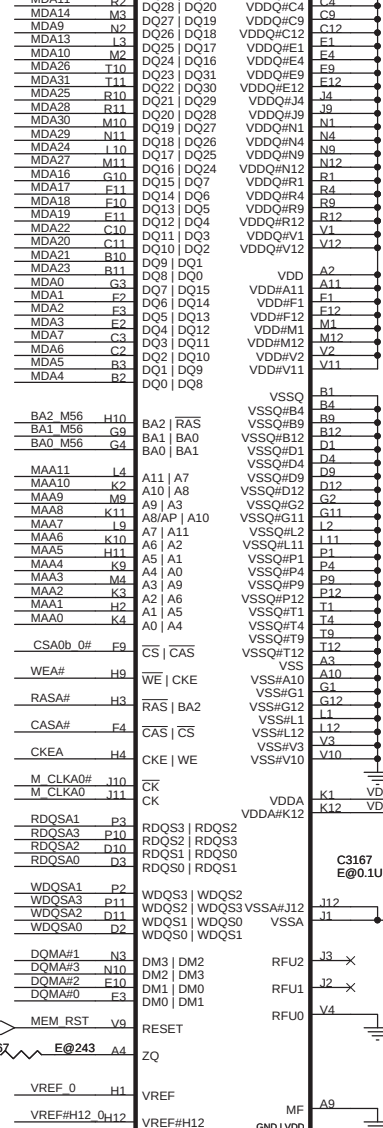
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MEMORY INTERFACE A

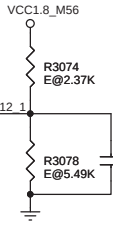
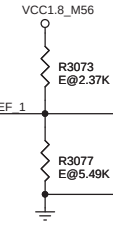
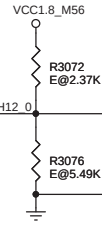
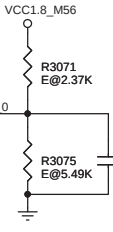


E@M56-P B11 LF

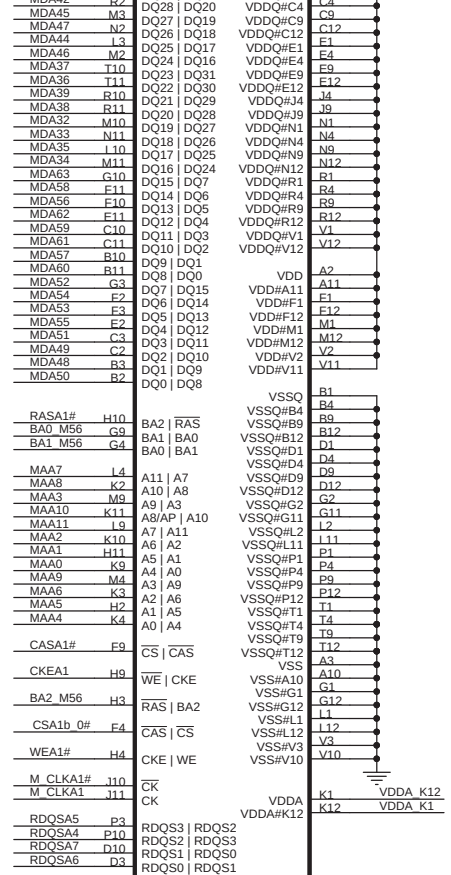
Signal	DDR1, 2	DDR3
MVREF to 1.8V	100R	40.2R
MVREF to GND	100R	100R



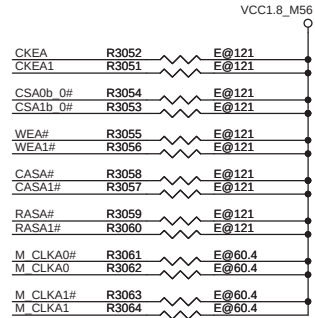
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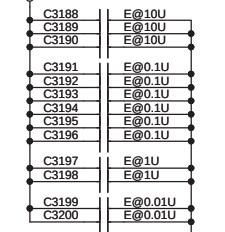
VRAM_256Mb



VRAM_256Mb



VCC1.8_M56

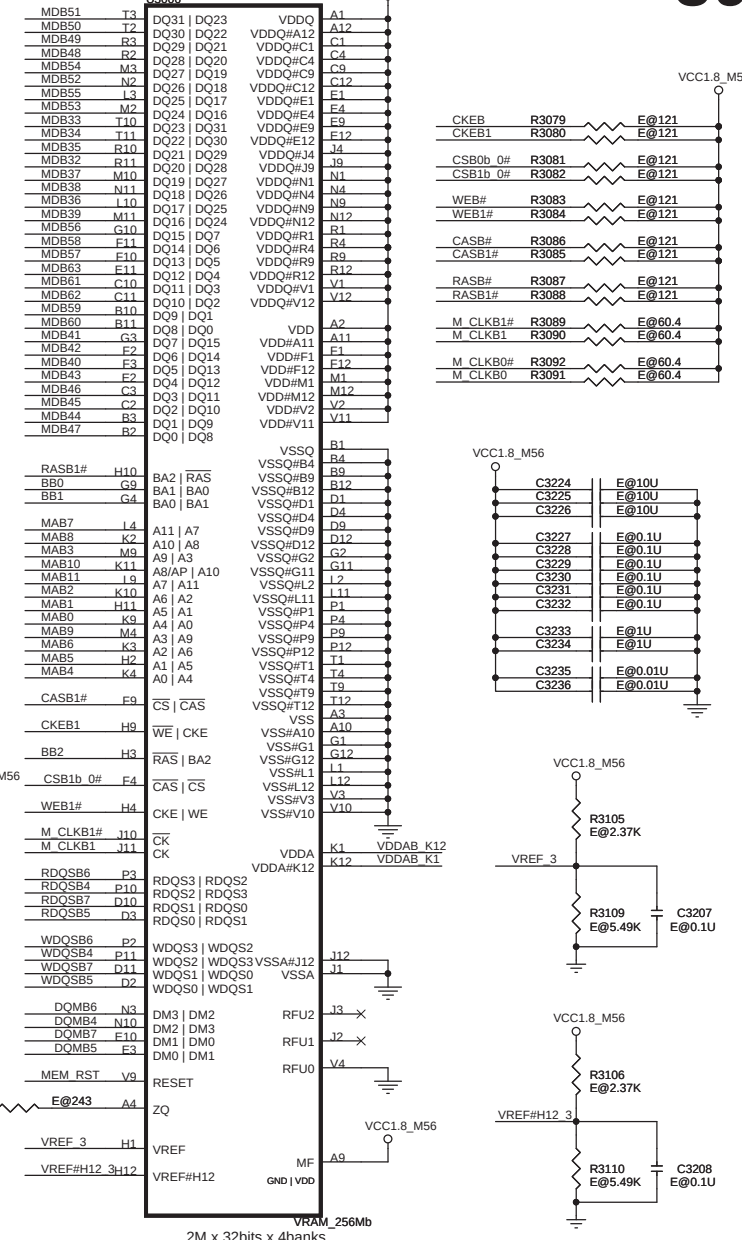
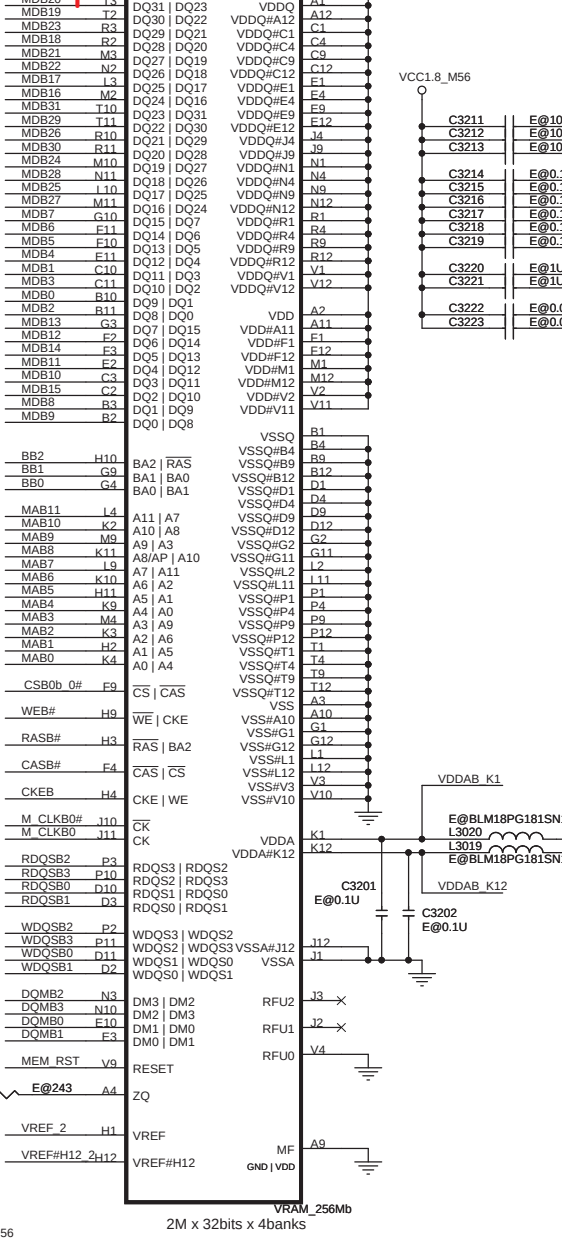
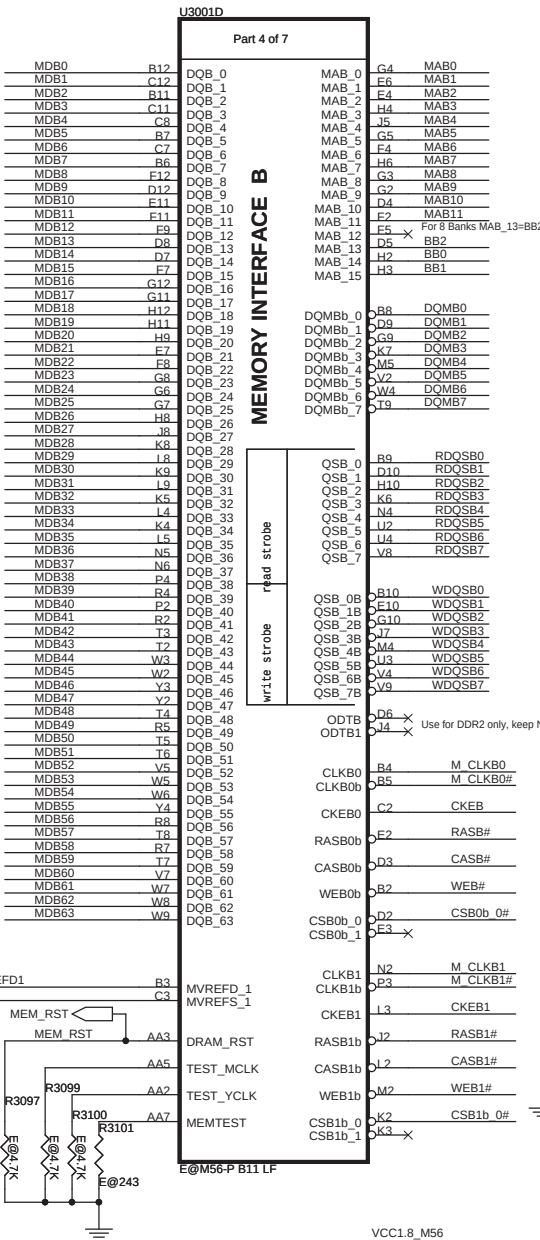


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1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods and molding resins only from the business partners that Sony approves as Green Partners.

Channel B



Signal	DDR1,2	GDDR3
MVREF to 1.8V	100R	40.2R
MVREF to GND	100R	100R

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**QUANTA
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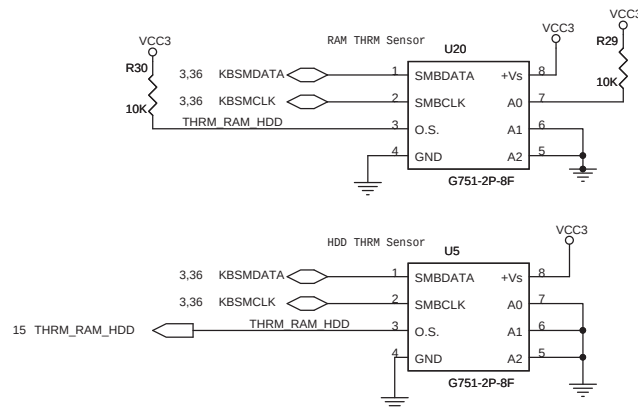
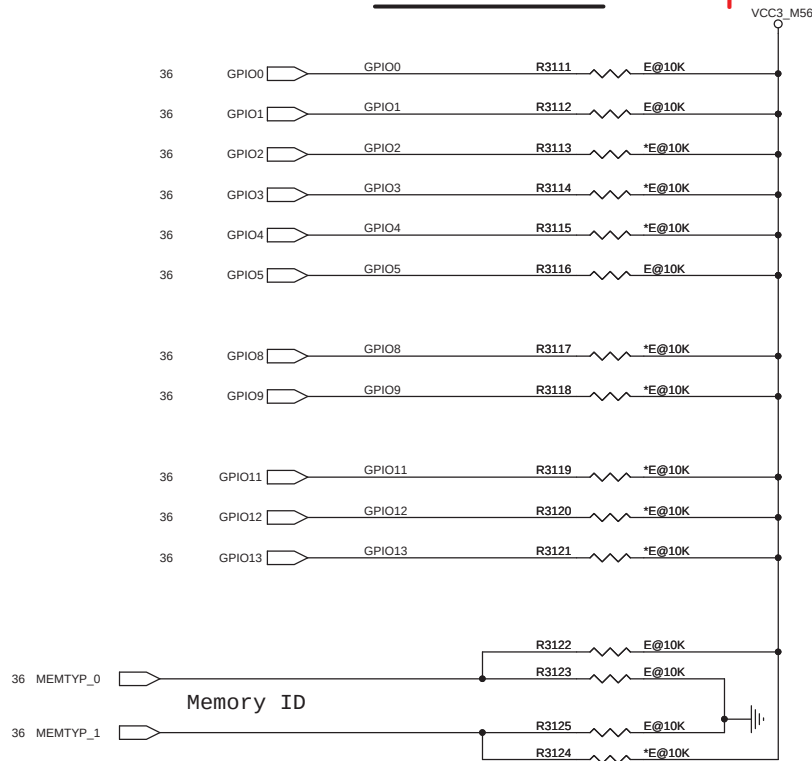
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OPTION STRAPS

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M56-P Strap

STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: full Tx output swing (recommended)	0 (internal pull-down)
TX_DEEMPH_EN	GPIO1	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled (recommended)	0 (internal pull-down)
Reserved	GPIO(3:2)	ATI internal use only. Other logic must not affect this signal during RESET.(GPIO2=VDD_VCL)	00
DEBUG_ACCESS	GPIO4	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible	0 (internal pull-down)
PLL_IBIAS_RD	GPIO[6:5]	Bias Current for the PCI Express PHY PLL	01
Reserved	GPIO8	ATI internal use only. Other logic must not affect this signal during RESET.(Serial ROM Output from ROM)	0
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, controls chip IDIs. If rom attached identifies ROM type 000x - No ROM, MEM_AP_SIZE=00 128MB(Default) 001x - No ROM, MEM_AP_SIZE=01 256MB 010x - No ROM, MEM_AP_SIZE=10 64MB 011x - No ROM, MEM_AP_SIZE=11 Reserved 1000 - Parallel ROM, chip IDIs from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDIs from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDIs from ROM 1011 - Serial M25P10 ROM (ST), chip IDIs from ROM 1100 - Serial M25P05 ROM (ST), chip IDIs from ROM 1100 - Serial NX25F011B ROM (ISSI), chip IDIs from ROM	GPIO[9,13,12,11] 0000 (internal pull-down)
VIP_DEVICE	VSYN	Indicates if any slave VIP host devices drove this pin low during reset. 0- Slave VIP host port device present. 1-No slave VIP port devices reporting presence during reset	0 (internal pull-down)
Reserved	PCIE_TEST	ATI internal use only. Other logic must not affect this signal during RESET.(Serial ROM Output from ROM)	0
Reserved	HSYN	ATI internal use only. Other logic must not affect this signal during RESET.(Serial ROM Output from ROM)	0

Board Straps

REV. 0.1

STRAPS	PIN	DESCRIPTION	VALUE
MEMTYPE(1:0)	GPIO 27,26	Memory identification for BIOS 00 - Infineon GDDR3 : 8M x 32 bits x 4 banks(Default) 01 - Samsung 10 - TBD 11 - TBD	00



**QUANTA
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RJ9
MotherBoard

CHANGE LIST:

DVT Revise:

1. Swap Q20 Pin 1 and Pin 3 connection, keep R619 stuff.....Page3
2. Change U10,R10,R383 from Nonstuff to Stuff, change R9,R377,R384 from Stuff to Nonstuff to support PWM Inv bright control.....Page7
3. Change R625,R626 from Nonstuff to Stuff, Add C1461(10p) for EMI.....Page13
4. Change PU3 from MAX1632 to MAX8734, Remove PR29, PR31, PR32, PR34, PC35, PD5,PD7, PD9, PD73, PD74.....Page30
Add PR685, PR686, PR687, PR688, PR689, PR690, PR691, PR692, PR694, PR696, PR697, PR698, PR699, PC148, PC841, PC842, PC843, PD77
Change PC39 from 10u to 4.7u, PC42 from 4.7u to 2.2u
5. Change PU1 from MAX8771 to MAX8770, Remove PR4, PR16, PR10, PR672, PR64, PQ59, PC79, Add PR65.....Page28
6. Change PR673 from 100 to 2K, change PC802 from Nonstuff to stuff and change value from 0.01u to 0.1uPage31
7. Change PR51 from 1K to 4K.....Page32
8. Change U21 P/N to AJ080550002Page27
9. Change U57 P/N from ALTD3306K00 to AL3Q3306K04; Change L25,L29,L31 P/N to CX8BA220007.....Page11
10. Change PQ58, PQ60, PQ62 from Nonstuff to Stuff, Remove PR684, PC826,Page33
11. Change U1 from ICS954310 to ICS9LPR310 for thermal considerationPage2
Add R702, R703, R704, R705; Remove R700, R528, R529
Remove RP47, RP48, RP49, RP50, RP51, RP54, RP55, RP56, RP58, R4
Change R40 to 4.3Kohm, Change R702 to 100ohm, Change RP30,RP31 to 10ohm, Change RP32,RP33,RP34,RP35,RP40,RP41,RP57 to 22ohm, Change R704 to 4.7k
12. Change VCC_CORE and M56_CORE high side and low side MOSFET for thermal consideration
Remove PQ1, PQ2, PQ3, PQ4, PQ54, PQ55, PQ56, PQ57; Add PQ5, PQ9, PQ12, PQ13, PQ14, PQ15, PQ18, PQ19.....Page28
Remove PQ46, PQ47, PQ53, PQ58; Add PQ38, PQ39, PQ40, PQ41.....Page33
13. Change PL1, PL19 P/N from CX1PG220004 to CX330T60001, Change PR5, PR21 P/N to CS-5603J908, Change PR14 from 100ohm to 10ohm, Change PC19 from 1000p to 4700p.....Page28
Add PR675, PR676 (2.2ohm), Add PC821, PC822 (3300p), Add PC845, PC847 (0.1u), Change PR14, PR669 P/N to CS01002FB12.....Page28
14. Add PQ65, PQ66, PQ67, PQ68, PQ69, PR695, PR700, PR701, PR702.....Page29
Add PR622, Remove PR621, Change PR142, PR86, PR700, PR80 from 10ohm to 22ohm.....Page29
15. Change PL4, PL18 P/N from CX1PG220004 to CX330T60001; Add PC848, PC862 (CH41006K911).....Page30
16. Change PU7 from APL5912 to G9338, Remove PL17, Add PR703, PR704, PR705, PC849, PQ64, Change PR666 to 0ohm, PR62 to 20k, PR63 to 10k, Change PL15, PL16 P/N to CX330T60001.....Page31
Change PCN3 from 50pin to 60pin, Add PC850,PC851, PC852, PC853, PC854, PC855, PC856, PC857, PC858, PC859 (CH41006K911).....Page31
17. Add PR680, PR682, PC832, PC833, PC860, PC861,PC92, Change PL5, PL7 P/N to CX330T60001, Change PR40 P/N to CS-5603J908, Change PR46 from 30.9K to 30K.....Page32
18. Change PR133 P/N to CS-5603J908, Change PL13 P/N to CX330T60001, Add PR586, PR681, PC831.....Page33
19. Add R658 (CS31002FB26), Unstuff R24, Stuff R25.....Page15
20. Remove R512, R561.....Page21
21. Change U51 P/N from ALTD3306K00 to AL3Q3306K04Page24
22. Change CON39 P/N from DFHS12FS602 to DFHS14FS288Page25
23. Change PQ64 P/N from BAM44040012 to BAM44220002Page31
24. Add U33 and C369 for M56_PLTRST# bufferPage14
25. Remove G-sensor (U55)Page24
26. Add U32, C38, C39, Remove R8.....Page4

PVT Revise:

1. Add R697, R698, C1155, C1156, Change PR95 from 1M to 100k.....Page29
2. Add R3127 10K to pull down GENERICD.....Page37
3. Add R331 100K to pull down PLTRST#.....Page14
4. Change PR673 to 47k to delay LD0_EN.....Page31
5. Change PR11 to 15K to delay VCC_CORE.....Page28

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