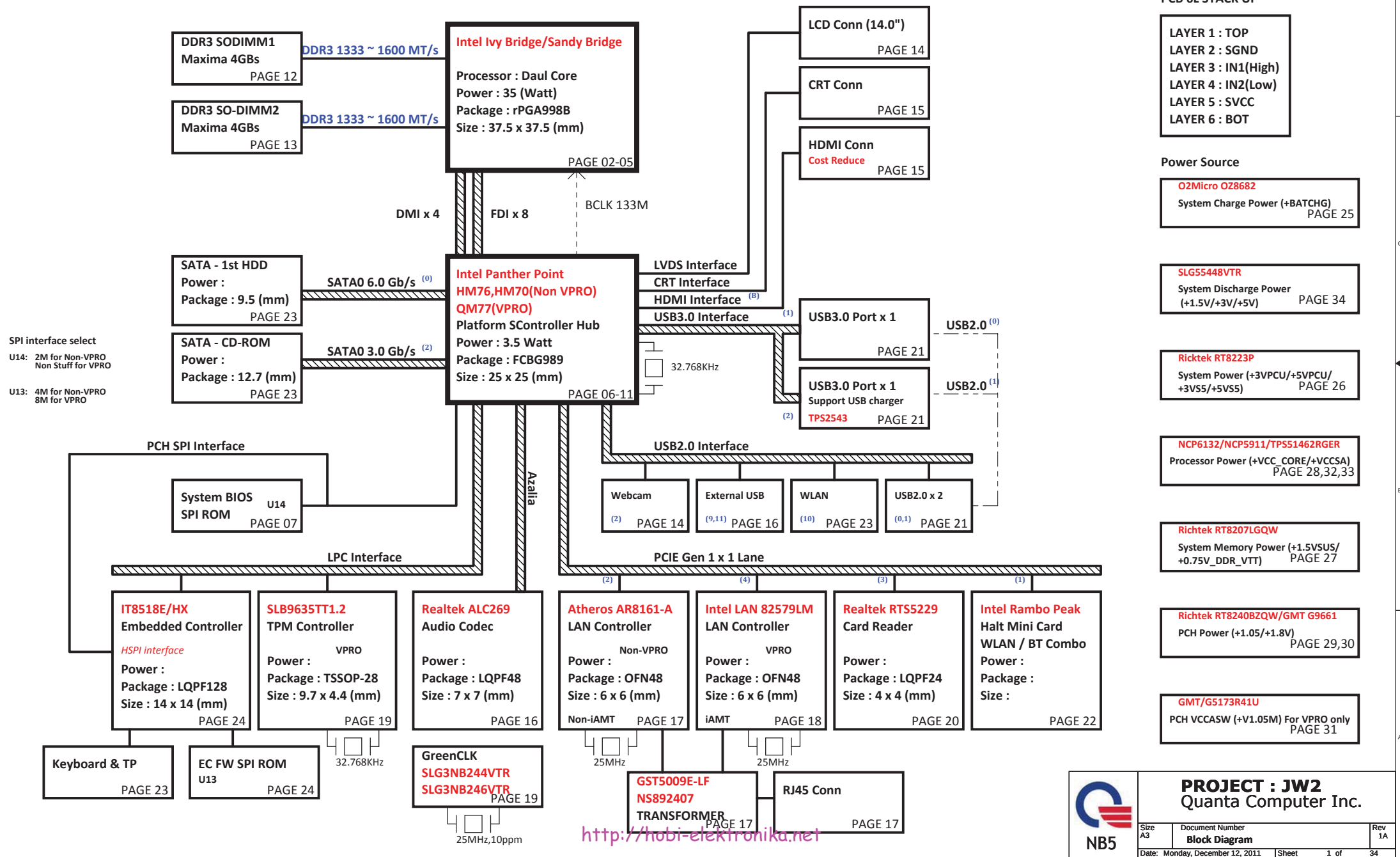
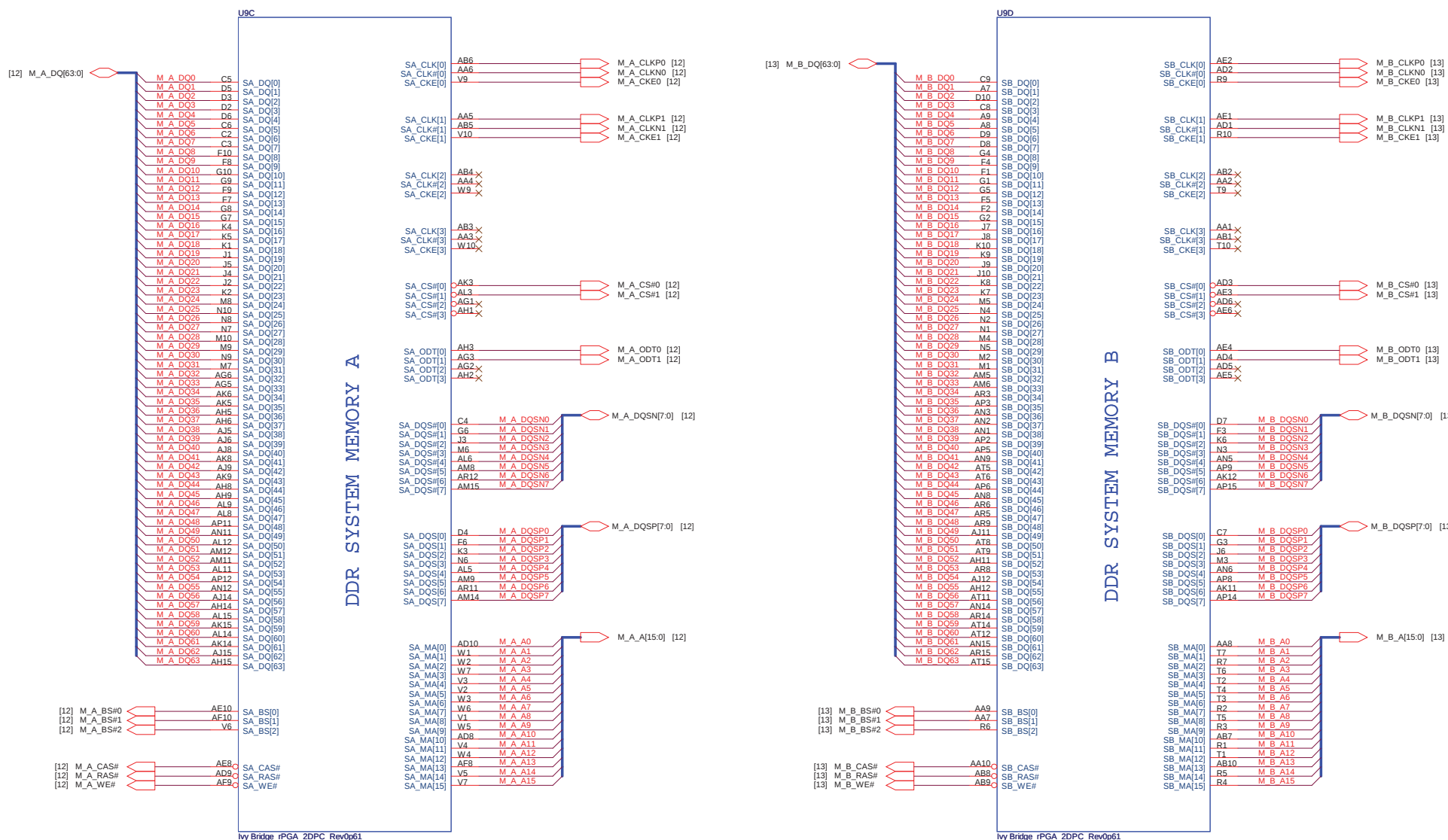


JW2 UMA (14.0") Intel Chief River Block Diagram



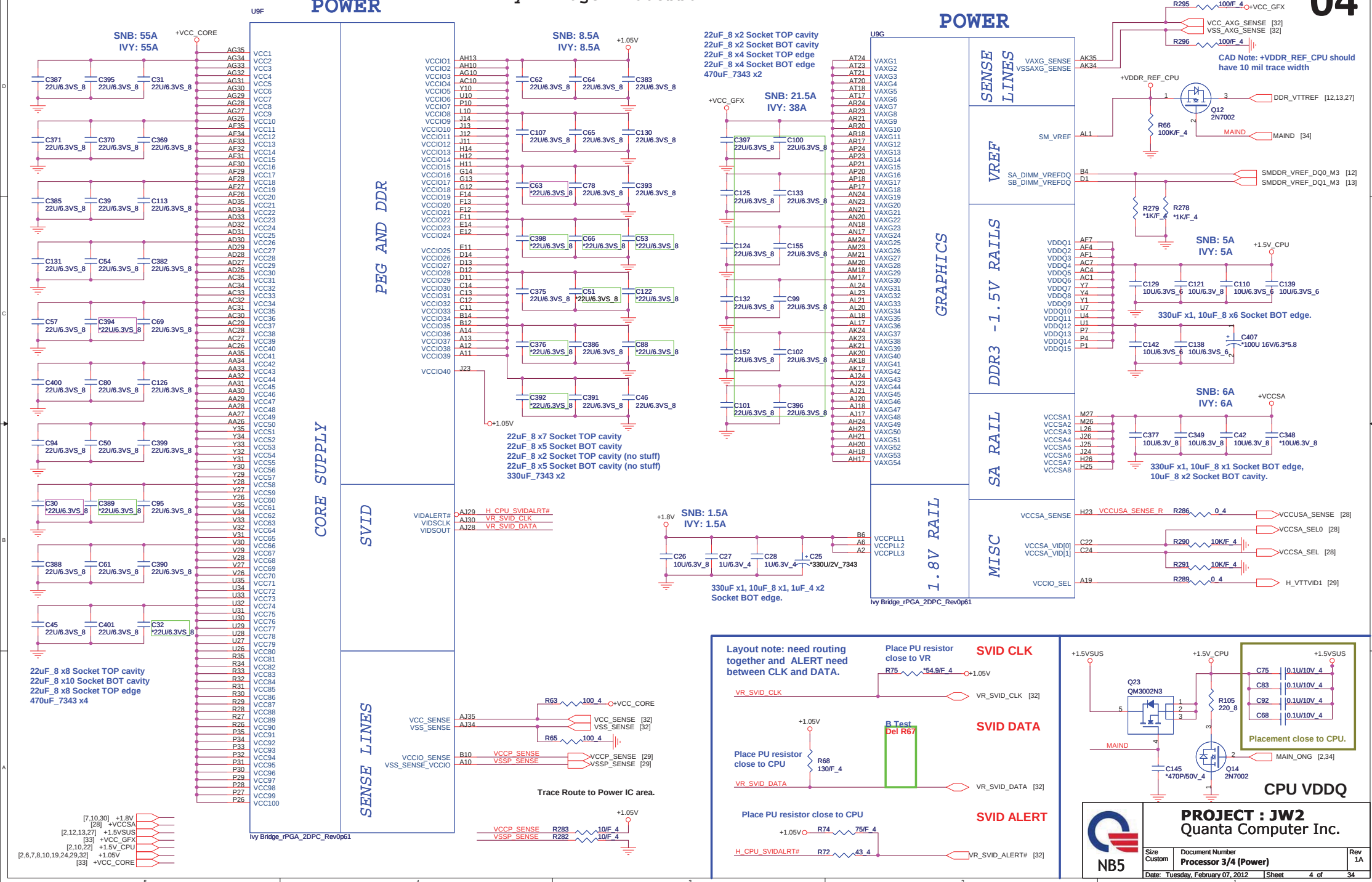


Ivy Bridge Processor (DDR3)

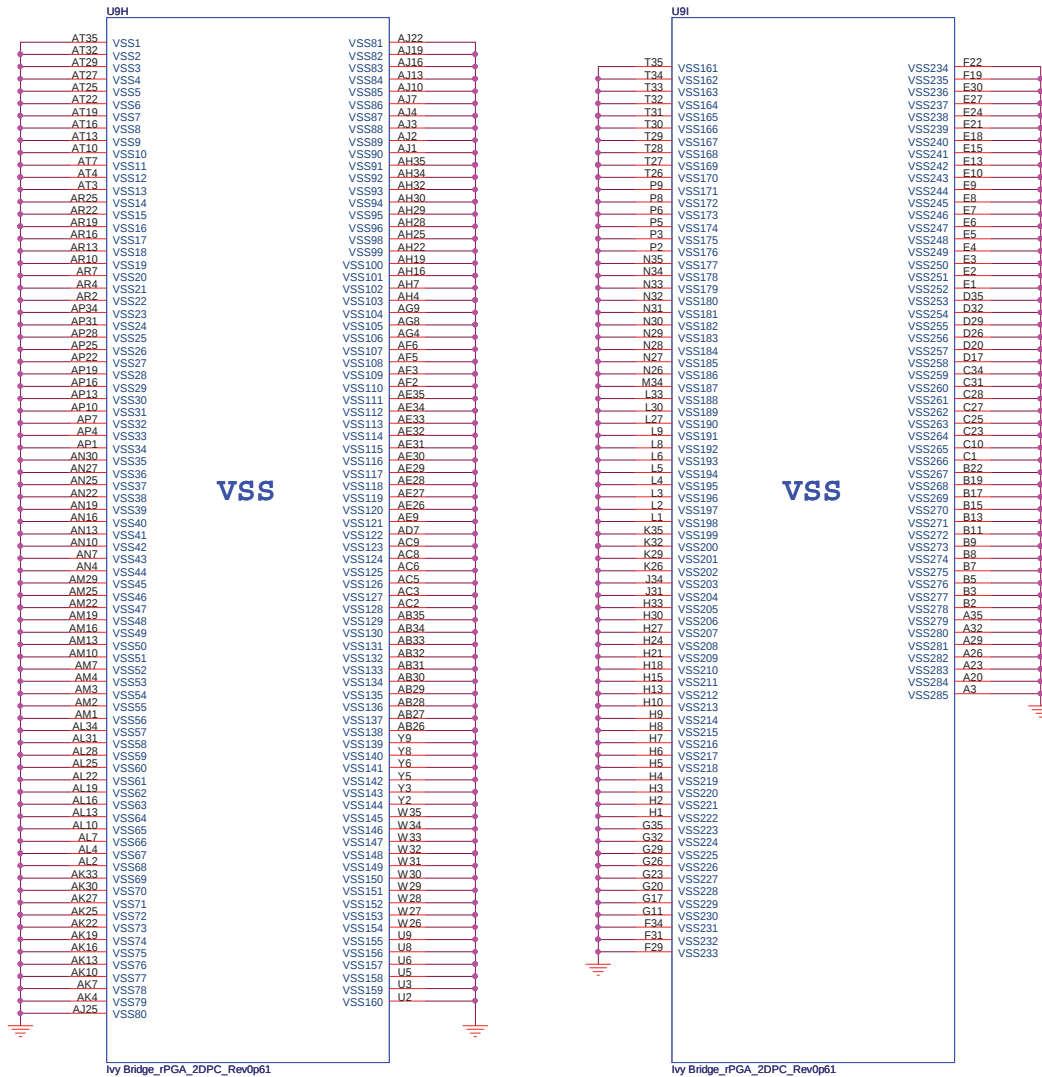


POWER

POWER

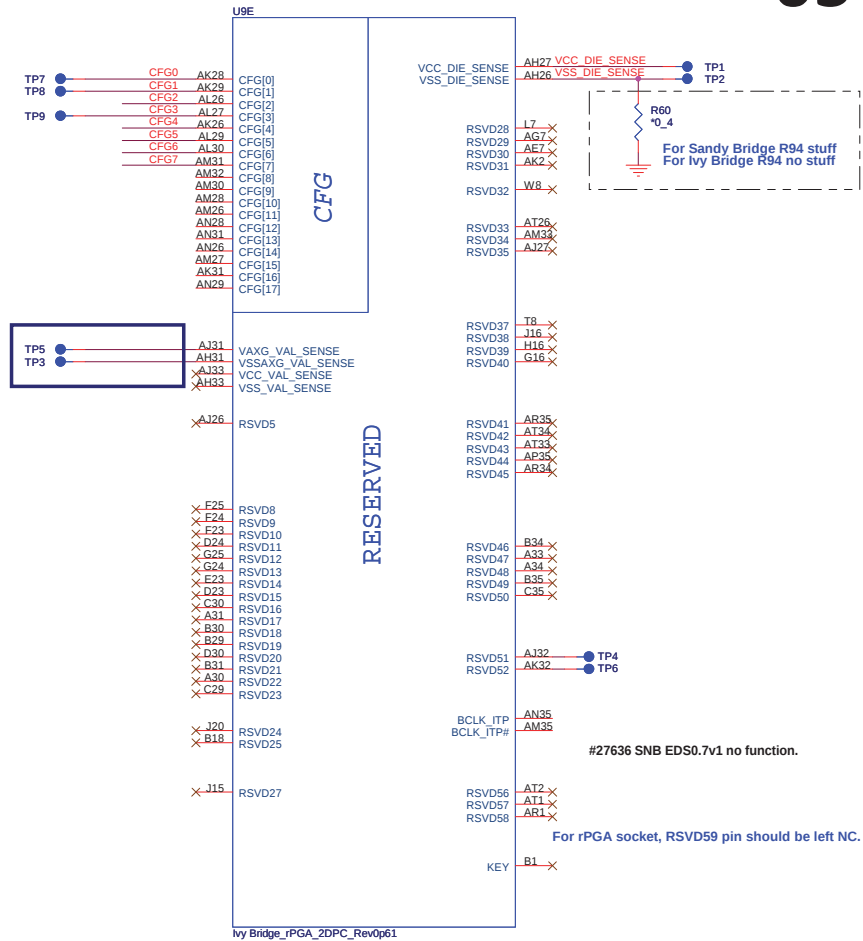


Ivy Bridge Processor (GND)



Ivy Bridge Processor (RESERVED, CFG)

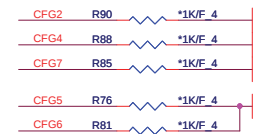
05



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



CFG[6:5] (PCIe Port Bifurcation Straps)

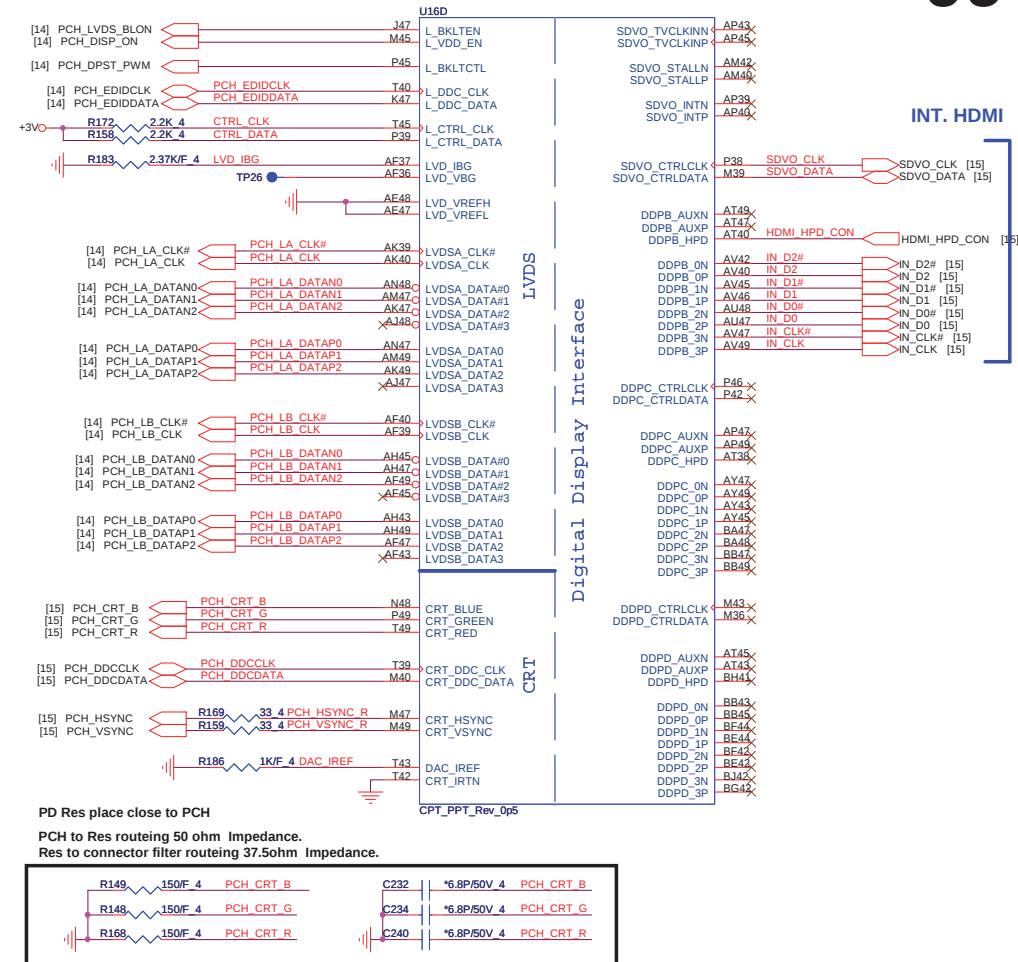
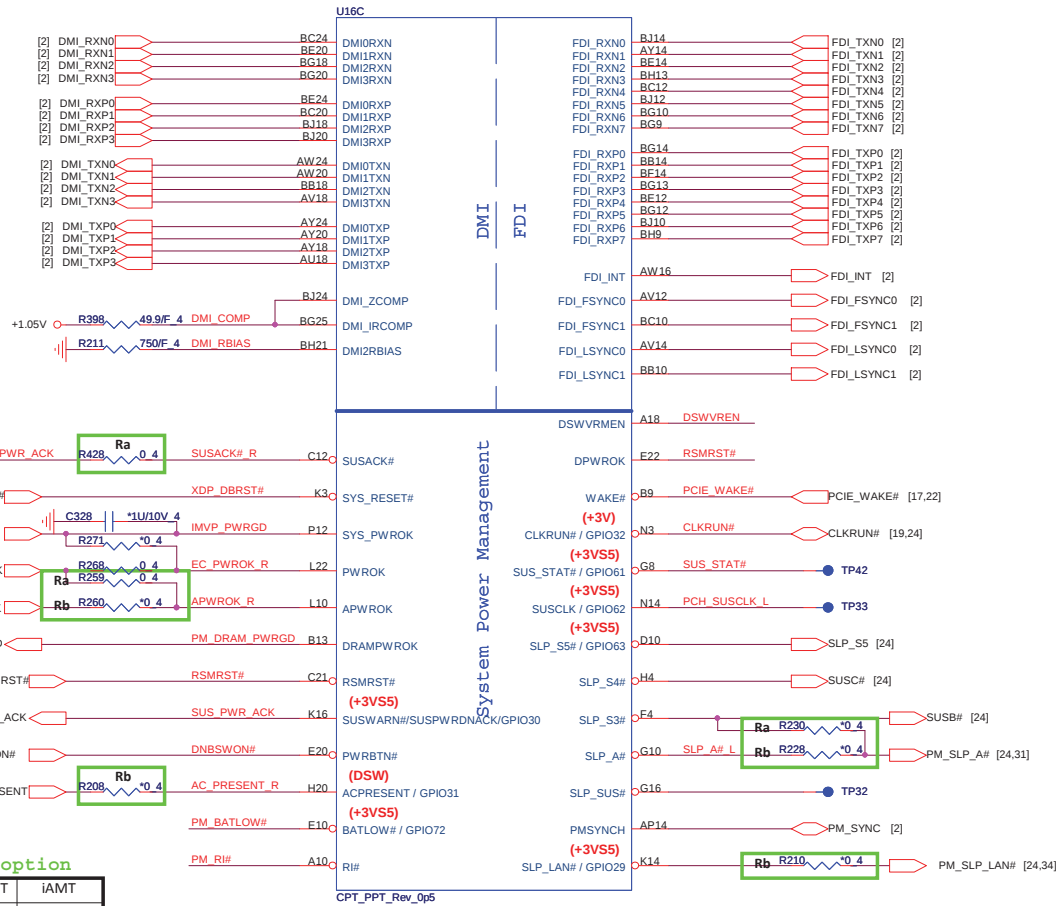
11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

	PROJECT : JW2 Quanta Computer Inc.	
	Size Custom	Document Number
	Processor 4/4 (Ground)	
Date: Thursday, December 08, 2011		Sheet 5 of 34

Cougar Point/Panther Point (DMI,FDI,PM)

Cougar Point/Panther Point (LVDS,DDI)

06



INT. HDMI

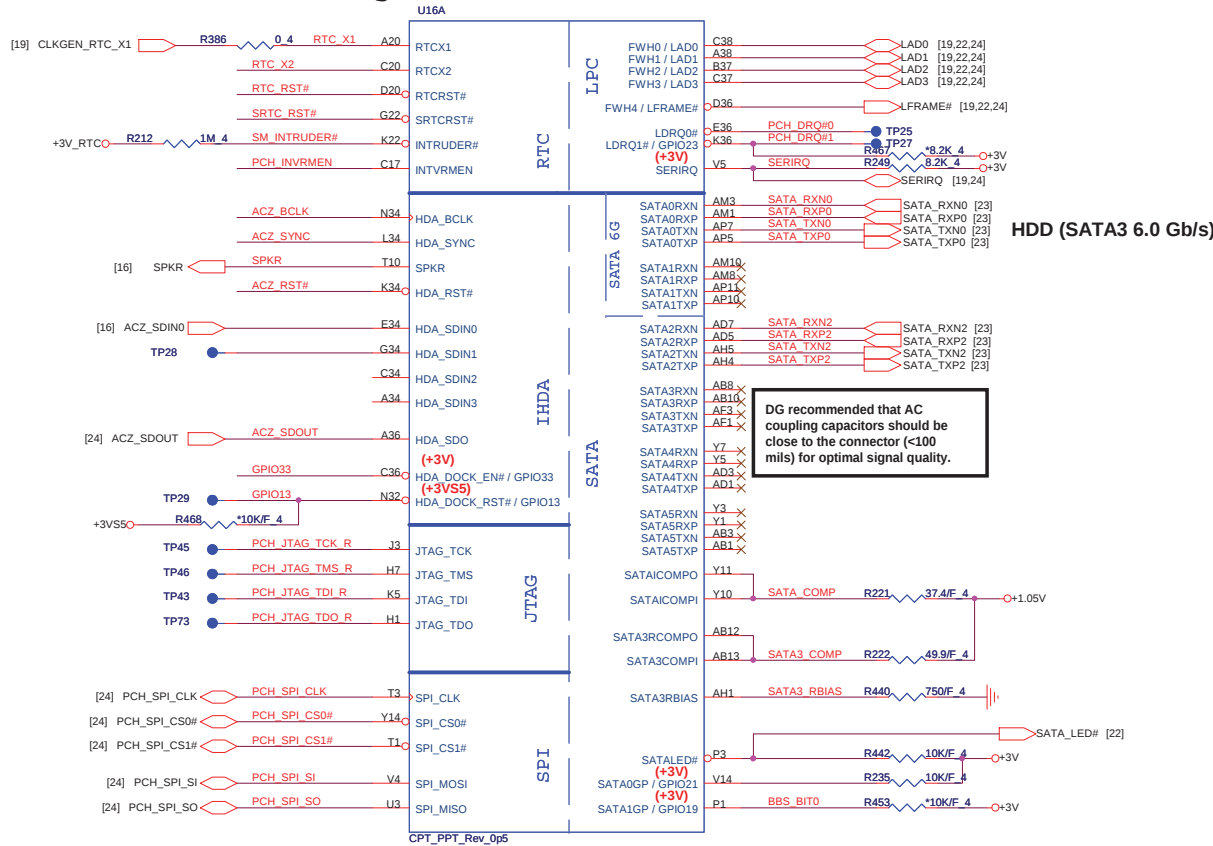


PROJECT : JW2
Quanta Computer Inc.

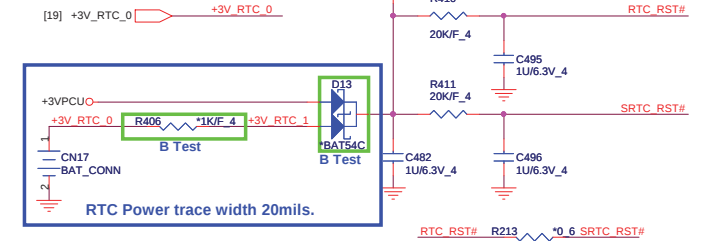
Size Custom Document Number PCH 1/6 (Host/Display) Rev 1A
Date: Tuesday, February 07, 2012 Sheet 6 of 34

Cougar Point/Panther Point (HDA,JTAG,SATA)

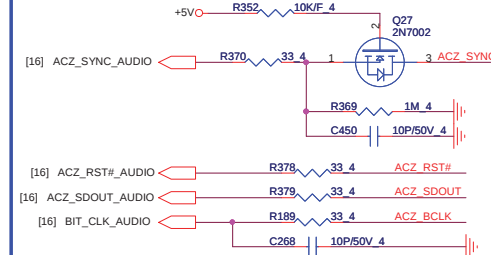
07



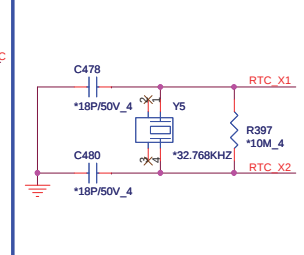
RTC Circuitry(RTC)



HDA Bus(CLG)

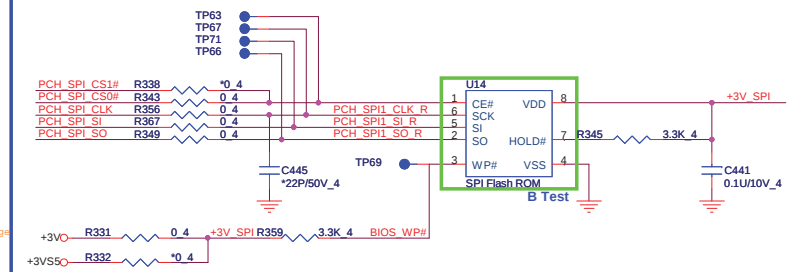


RTC Clock 32.768KHz



PCH SPI ROM(CLG)

Vender	Size	P/N
EON	2MB	AKE38ZN0Q00 (EN25QH16-104HIP)
AMIC	2MB	AKE38ZN0802 (A25LQ16M-F/Q)
Socket		DFHS08FS023



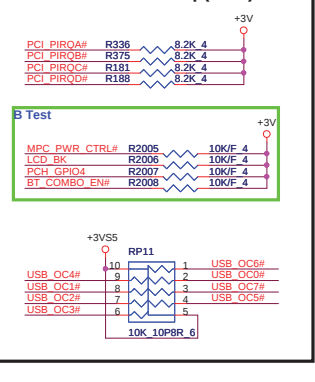
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	Different from Calpella No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	SPKR → R238 → *1K/F → 4 → +3V
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R339 → *1K/F → 4 → +3V R340 → 10K/F → 4
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN → R395 → 330K/F → 4 → +3V_RTC
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 → R383 → *1K/F → 4 → ACZ_SDOUT
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#	GNT1# → R437 → *1K/F → 4 → SPI LPC
GPIO19	Different from Calpella Boot BIOS Selection 0 [bit-0]	PWROK		R344 → *1K/F → 4 → BBS_BIT1 [8]
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V → R232 → *1K/F → 4 → NV_ALE [8]
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm	+1.8V → R426 → 2.2K → 4 → R425 → 1K/F → 4 → NV_CLE [9] H_SNB_IVB# [2] → sandy/ivy btl/dg
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3VSS → R354 → 1K/F → 4 → ACZ_SYNC
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	ACZ_SDOUT → R382 → *1K/F → 4 → +3VSS
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	R446 → *1K/F → 4 → ICC_EN# [9]
GPIO28	Different from Calpella On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R265 → *1K/F → 4 → PLL_ODVR_EN [9]
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	PCH_SPI_SI → R438 → *1K/F → 4 → +3V

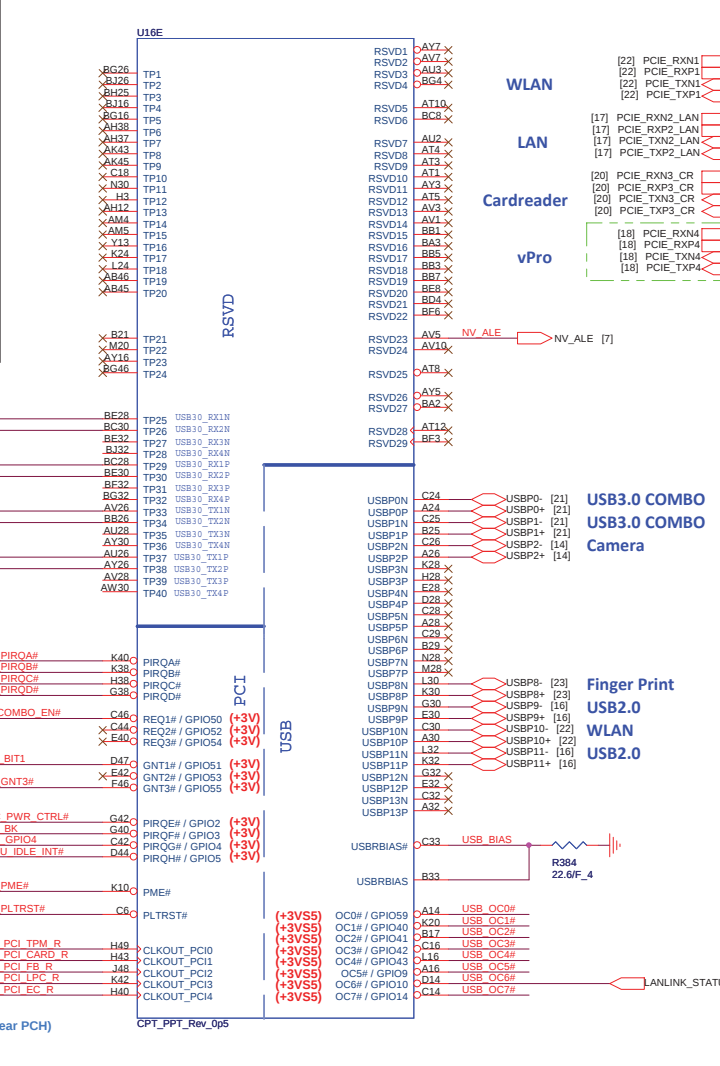
PROJECT : JW2
Quanta Computer Inc.

Size Custom	Document Number PCH 2/6 (HDA/RTC/SATA/SPI)	Rev 1A
Date: Tuesday, February 07, 2012	Sheet	7 of 34

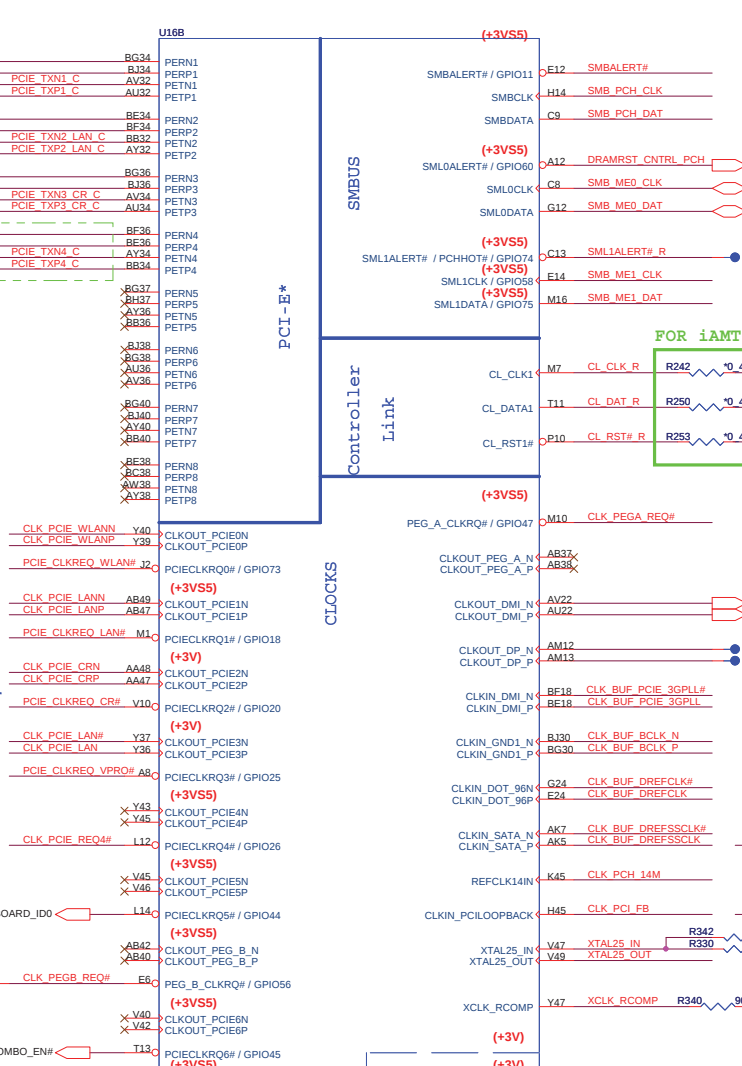
PCI/USBOC# Pull-up(CLG)



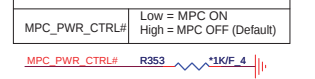
Cougar Point-M/Panther Point (PCI,USB,NVRAM)



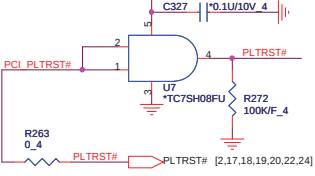
Cougar Point-M/Panther Point (PCI-E,SMBUS,CLK)



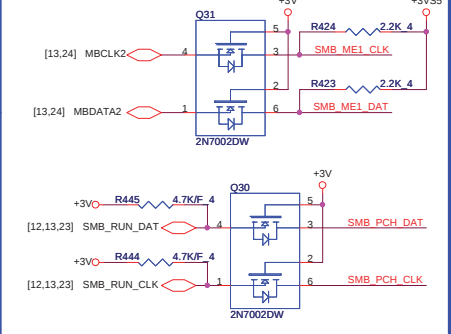
MPC Switch Control



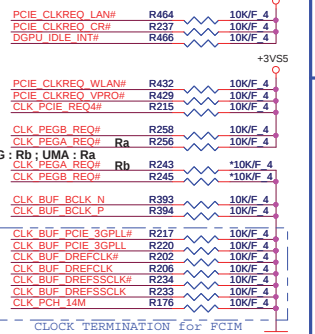
PLTRST#(CLG)



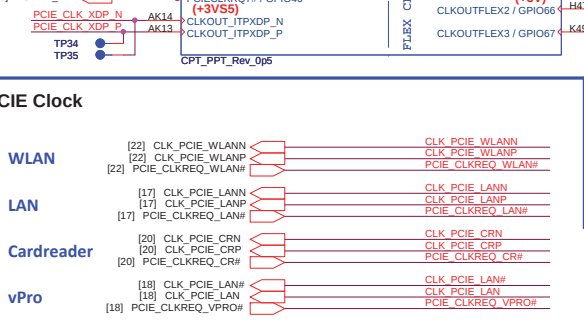
SMBus/Pull-up(CLG)



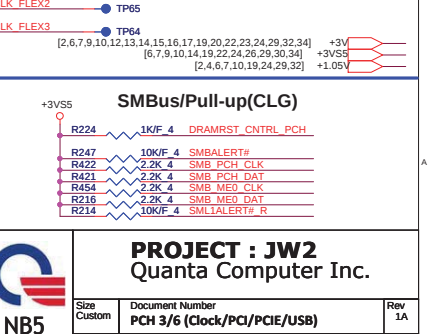
CLK_REQ/Strap Pin(CLG)



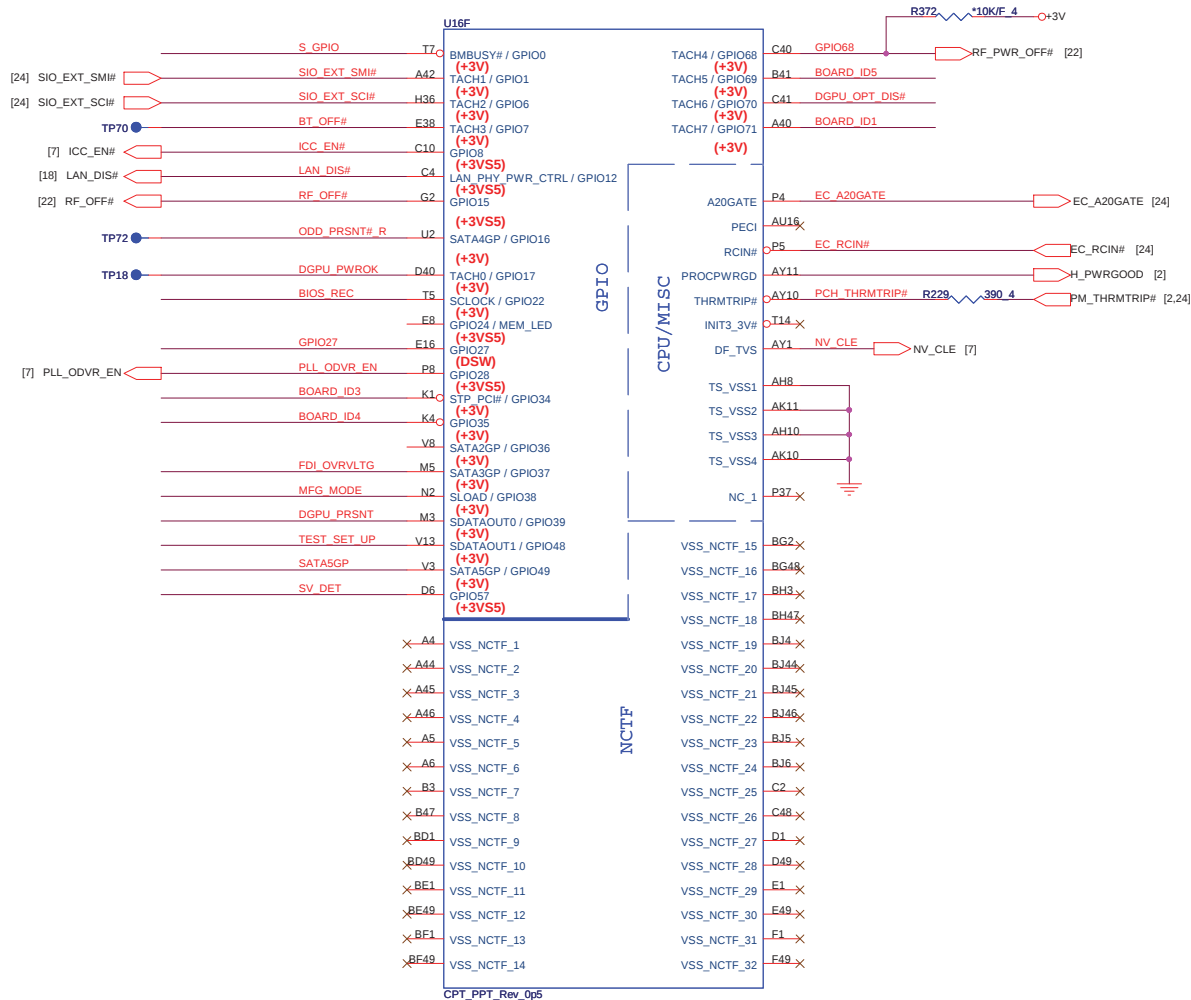
PCI-E Clock



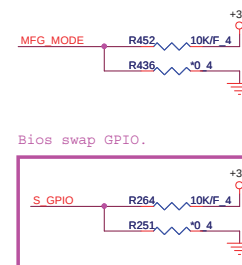
SMBus/Pull-up(CLG)



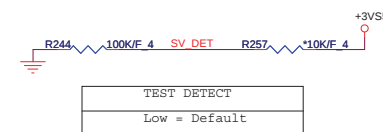
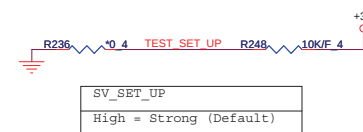
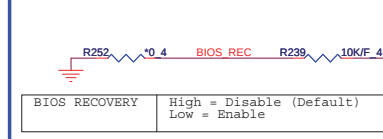
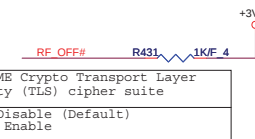
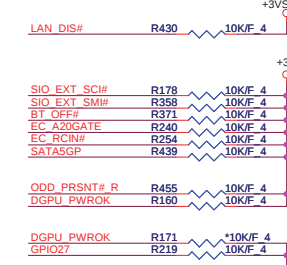
Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)



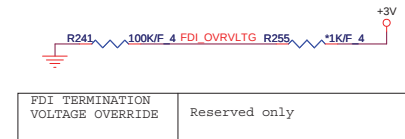
MFG-TEST



GPIO Pull-up/Pull-down(CLG)



上DGPU_PWR_EN_R pull high
+3V 200K, 200K 是不上件。



BOARD_ID[3:0]	Model Name
0000	QLGA
0001	TWC
0010	JW2
0011	T8D
0100	LG3
0101	LG5
0110	LG2C
0111	LG4C

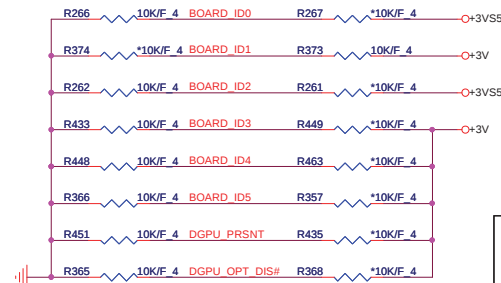
Chief River BOARD ID SETTING

BOARD_ID0	GPIO44	MODEL BIT0
BOARD_ID1	GPIO71	MODEL BIT1
BOARD_ID2	GPIO46	MODEL BIT2
BOARD_ID3	GPIO34	MODEL BIT3
BOARD_ID4	GPIO35	No Dolby=0, Dolby=1
BOARD_ID5	GPIO69	HM76=0, HM70=1
DGPU_PRSN#	GPIO39	Optimus=1, UMA=0
DGPU_OPT_DIS#	GPIO70	Optimus=0, Dis only=1

20110816 Define BRD_ID[3:0]

[8] BOARD_ID0 BOARD_ID0

[8] BOARD_ID2 BOARD_ID2



0804 Board_ID1 change to +3V
Board_ID5 change to +3V

[2,6,7,8,10,12,13,14,15,16,17,19,20,22,23,24,29,32,34] +3V

[6,7,8,10,14,19,22,24,26,29,30,34] +3VSS

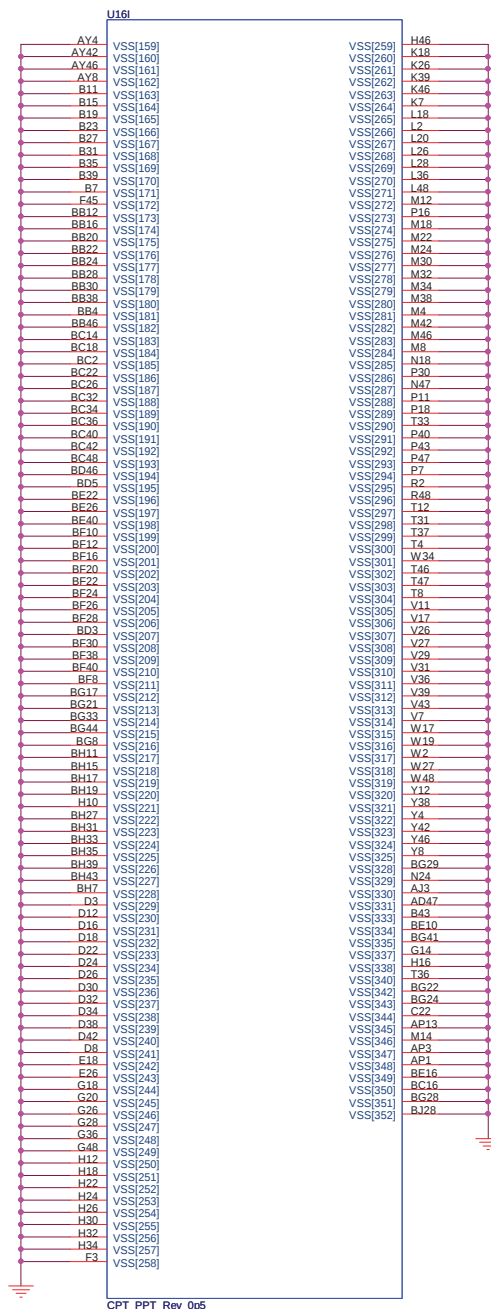


PROJECT : JW2
Quanta Computer Inc.

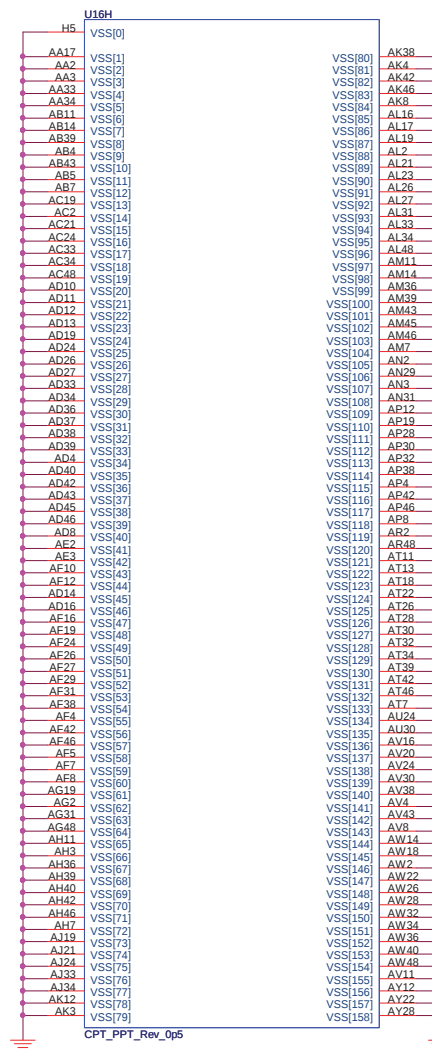
Size	Document Number	Rev
Custom	PCH 4/6 (GPIO)	1A
Date: Tuesday, February 07, 2012	Sheet	9 of 34



Cougar Point/Panther Point (GND)

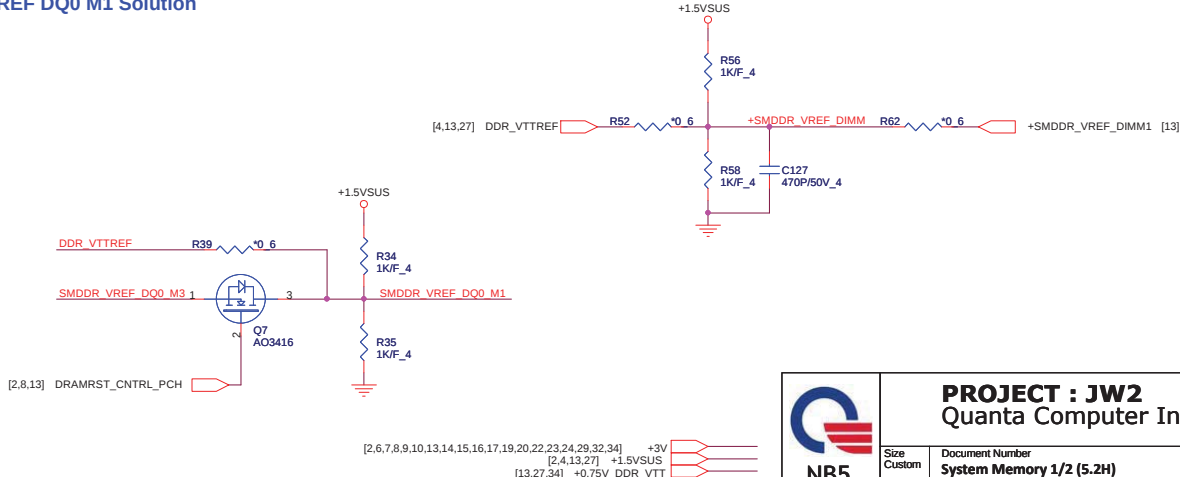
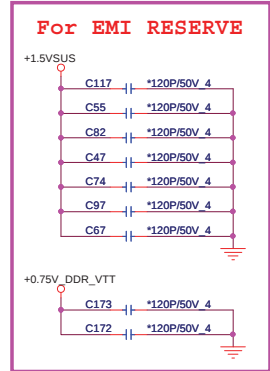
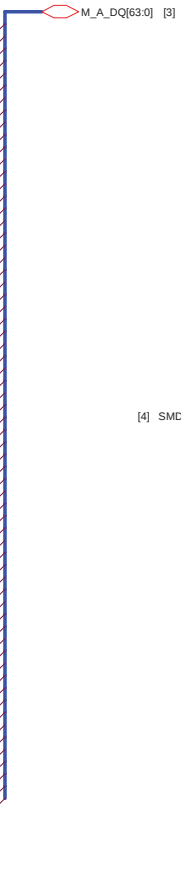


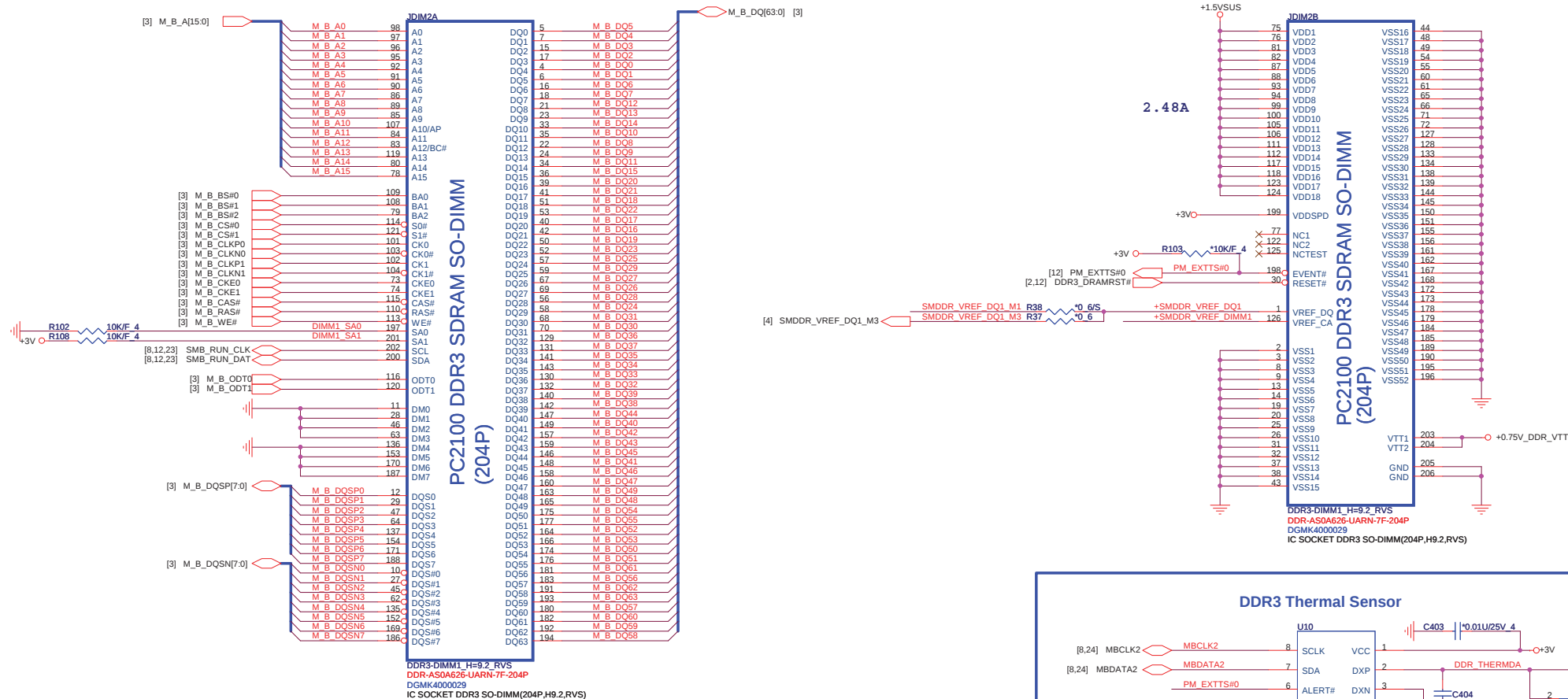
Cougar Point/Panther Point (GND)



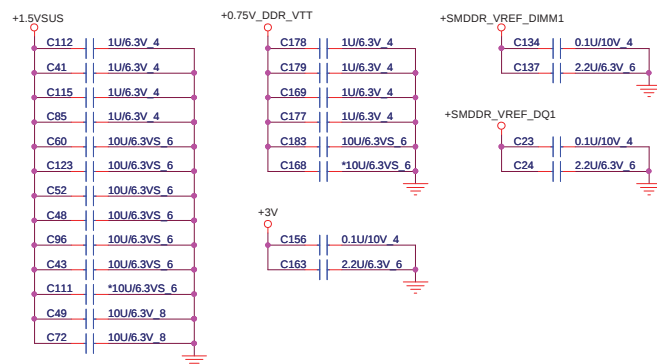
PROJECT : JW2
Quanta Computer Inc.

Size Custom	Document Number PCH 6/6 (Ground)	Rev 1A
Date: Thursday, January 12, 2012	Sheet 11 of	34





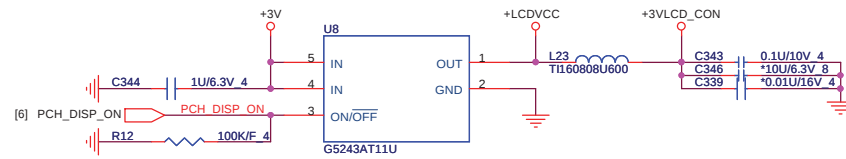
Place these Caps near So-Dimm1.



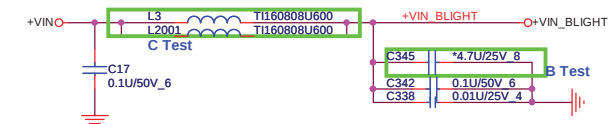
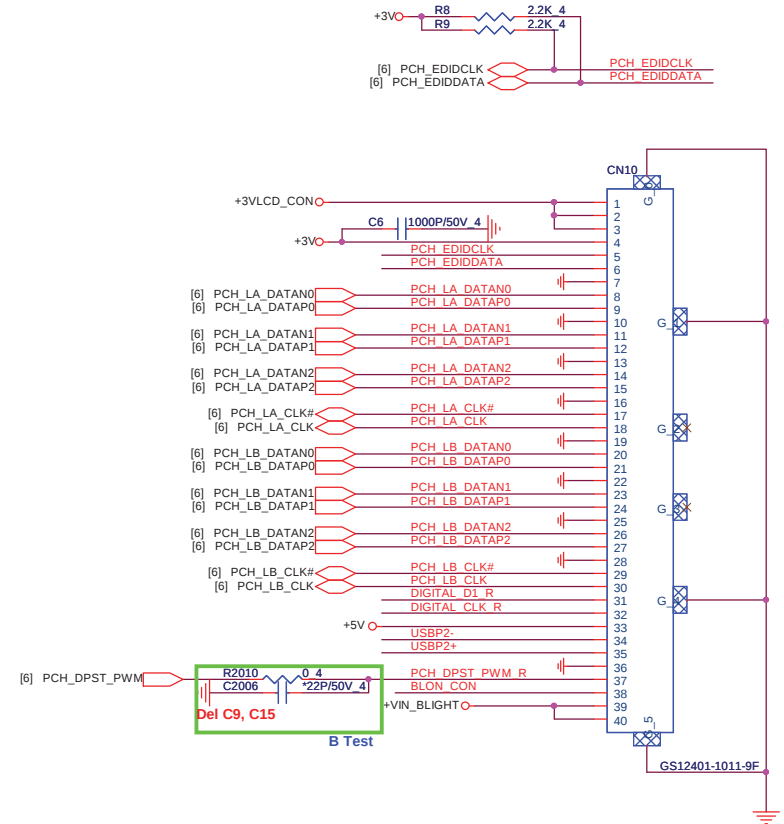
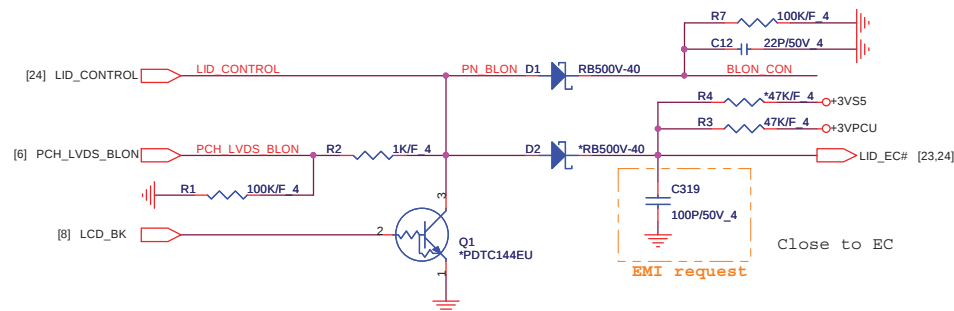
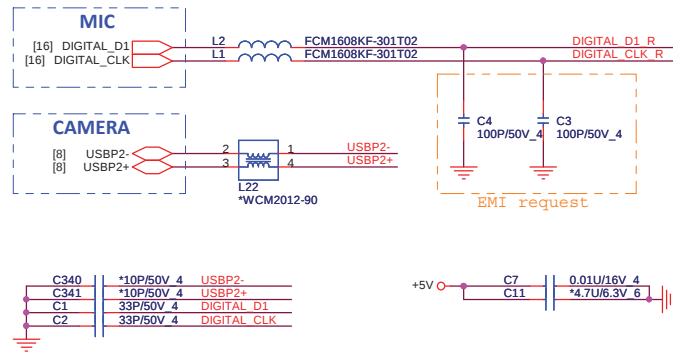
VREF DQ1 M1 Solution

PROJECT : JW2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	System Memory 2/2 (9.2H)	1A
Date: Tuesday, February 07, 2012	Sheet	13 of 34



USB Camera Connector



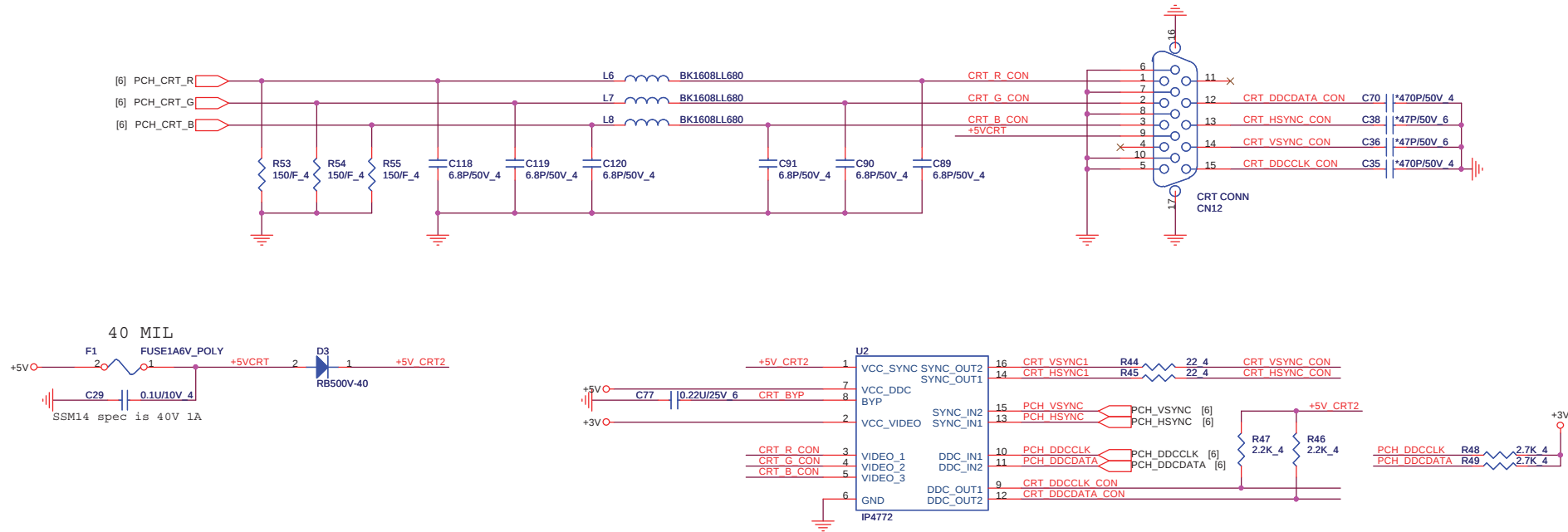
[2,6,7,8,9,10,12,13,15,16,17,19,20,22,23,24,29,32,34] +3V
[7,10,15,16,22,23,34] +5V
[19,25,26,27,29,33,34] +VIN
[7,19,22,23,24,25,26] +3VPCU



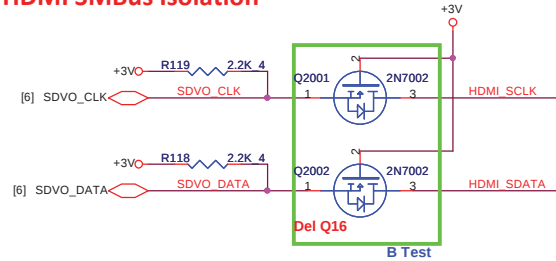
PROJECT : JW2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD Connector (LVDS)	1A
Date: Tuesday, February 07, 2012	Sheet 14 of 34	

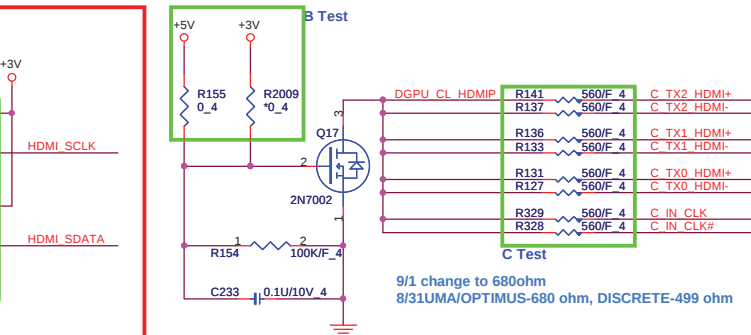
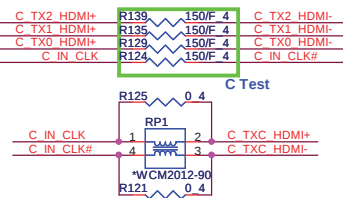
CRT PORT



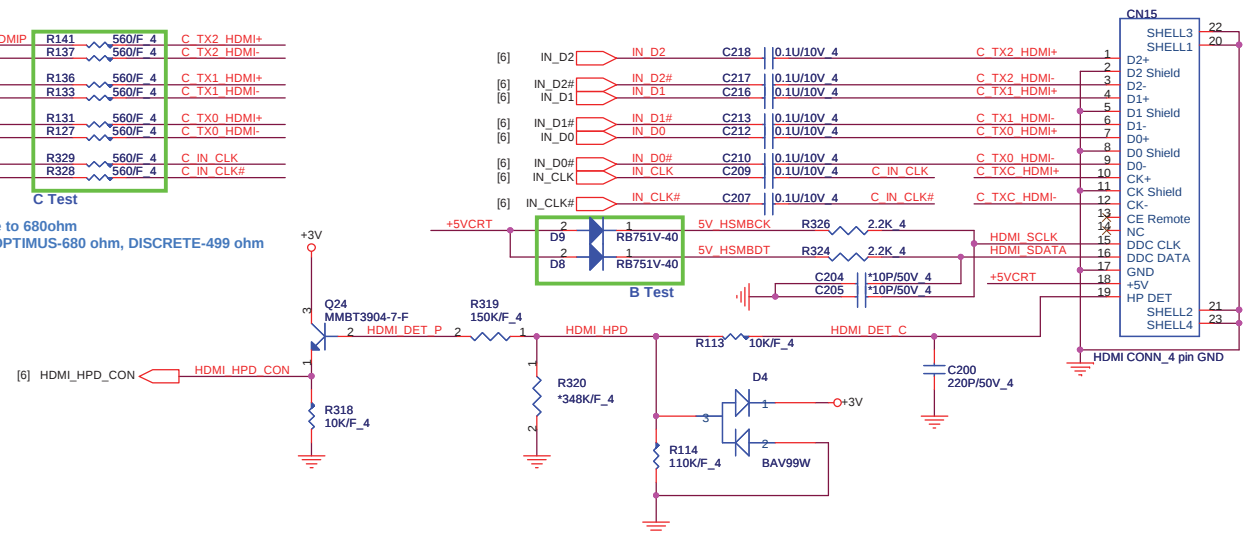
HDMI SMBus Isolation



EMI Solution

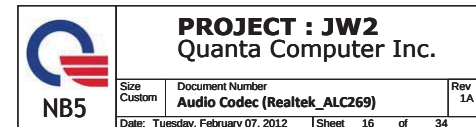


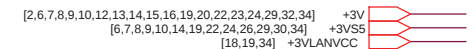
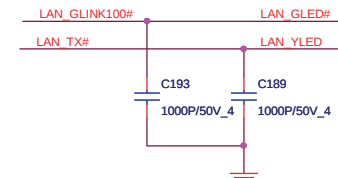
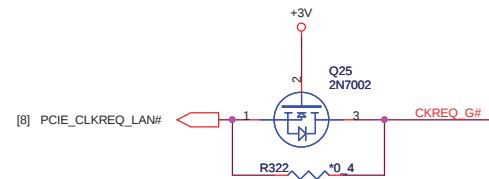
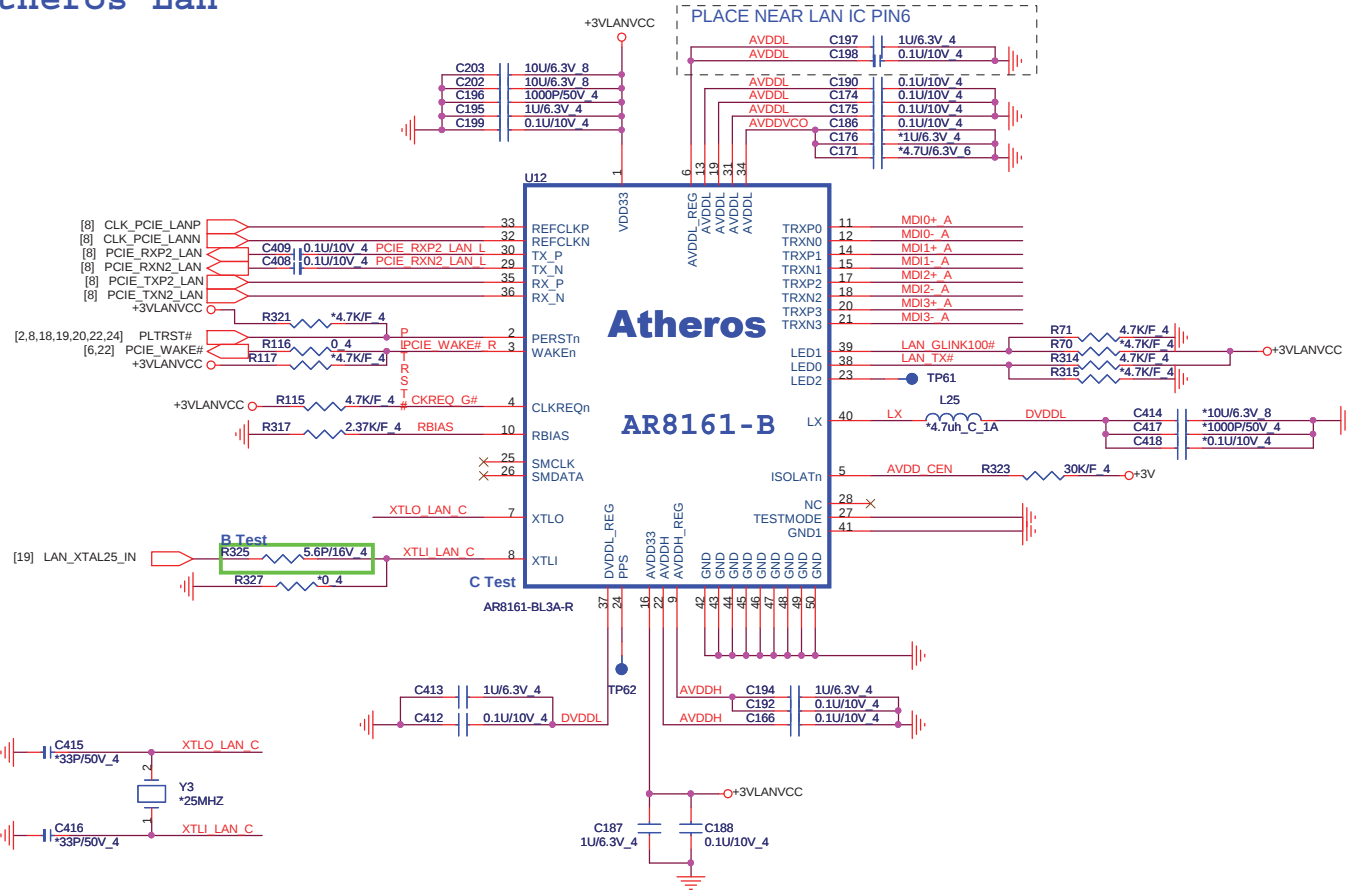
HDMI PORT



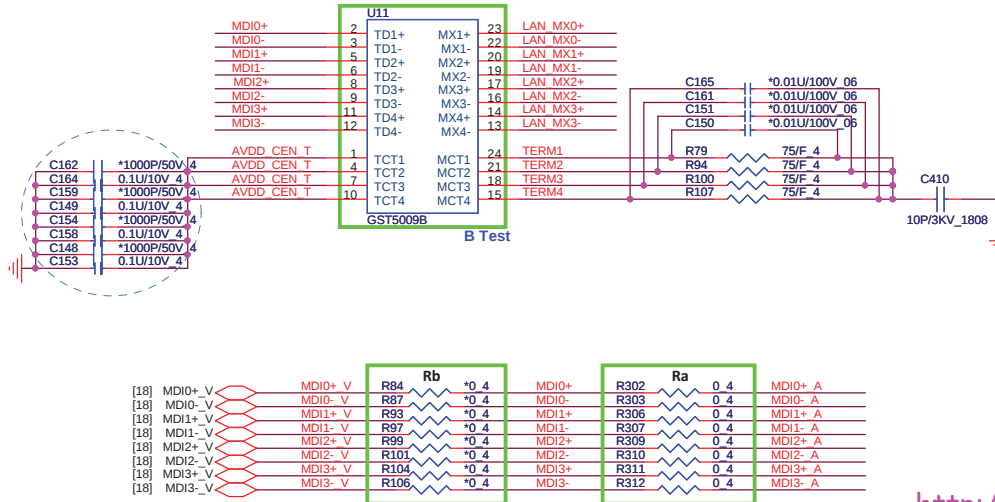
PROJECT : JW2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT/HDMI Connector	1A
Date: Tuesday, February 07, 2012	Sheet 15 of 34	

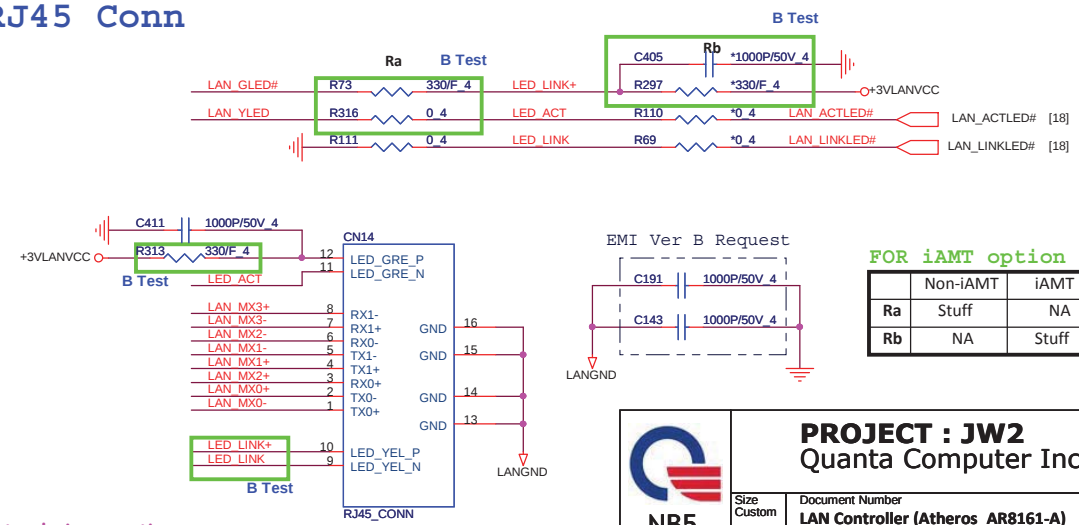




TRANSFORMER

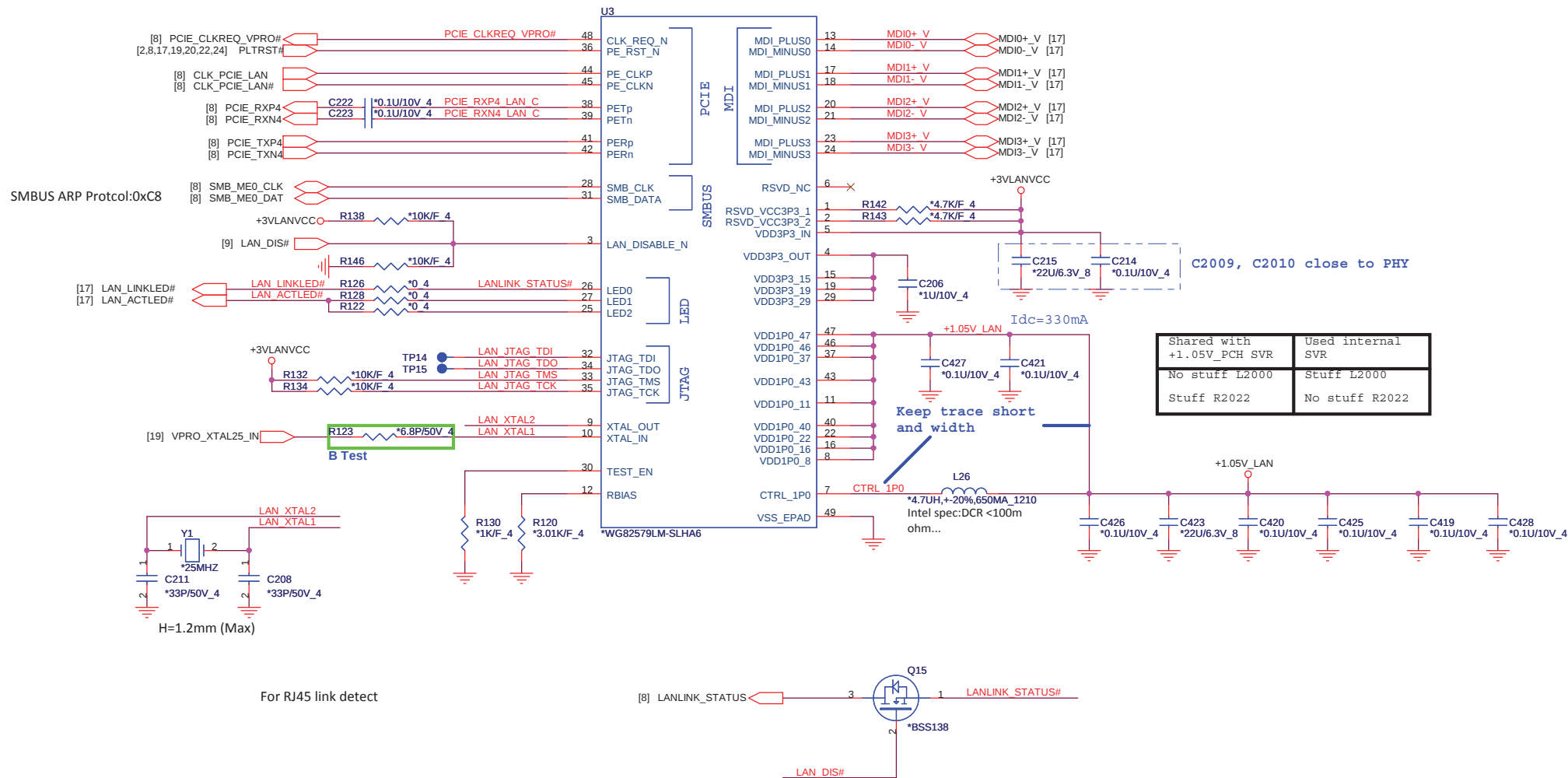


RJ45 Conn



FOR iAMT option

	Non-iAMT	iAMT
Ra	Stuff	NA
Rb	NA	Stuff



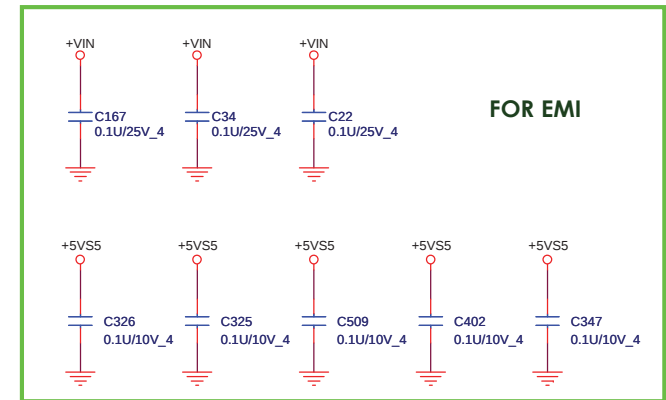
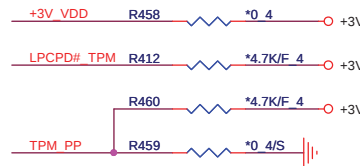
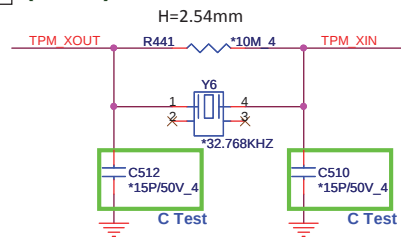
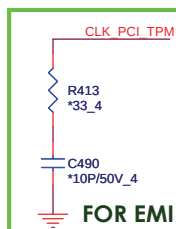
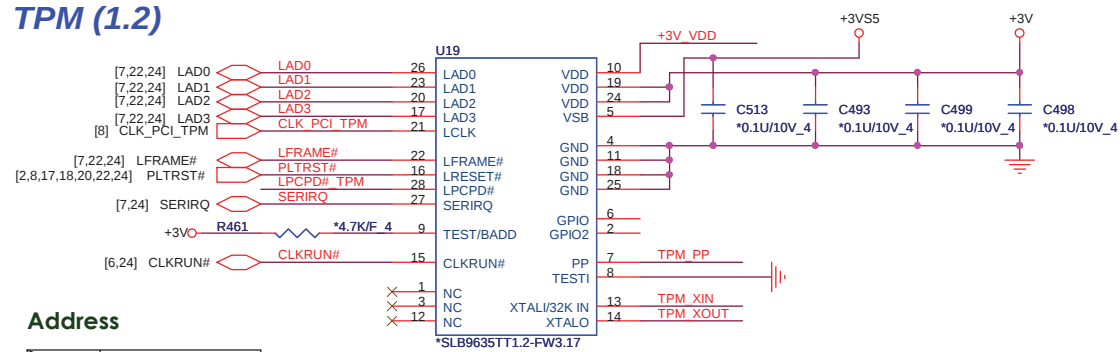
Shared with +1.05V_PCH SVR	Used internal SVR
No stuff L2000	Stuff L2000
Stuff R2022	No stuff R2022



PROJECT : JW2
Quanta Computer Inc.

Size B	Document Number Intel Lewisville 82579LM	Rev 1A
Date: Tuesday, February 07, 2012	Sheet 18 of 34	

TPM (1.2)



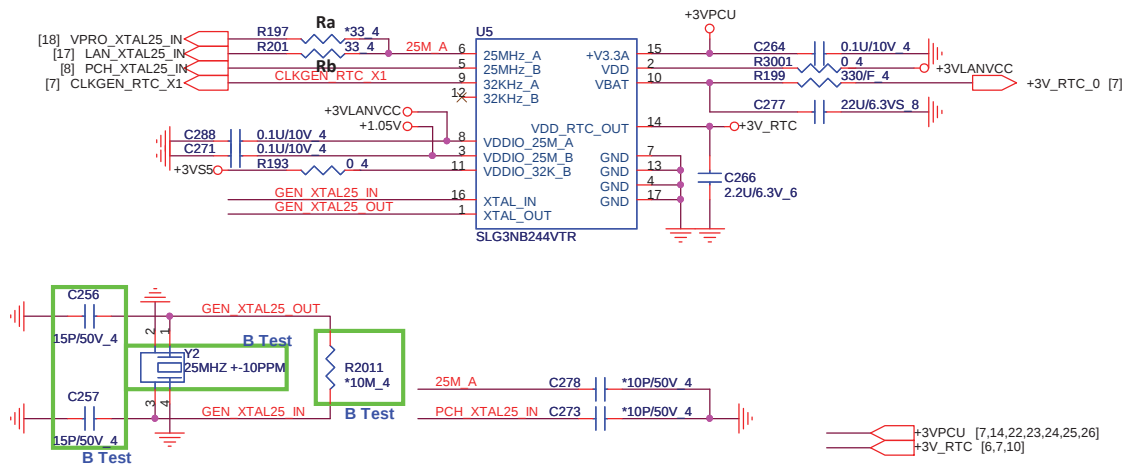
Green CLK

FOR LAN CLK option

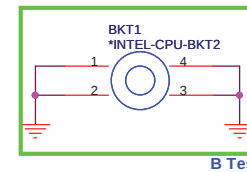
	Atheros	vPRO
Ra	NA	Stuff
Rb	Stuff	NA

FOR TPM option

	TPM	Non-TPM
R419	Stuff	NA
U5	AL3NB246000	AL3NB244000



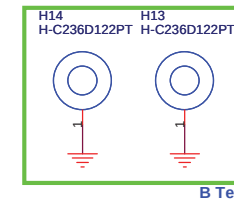
CPU Bracket



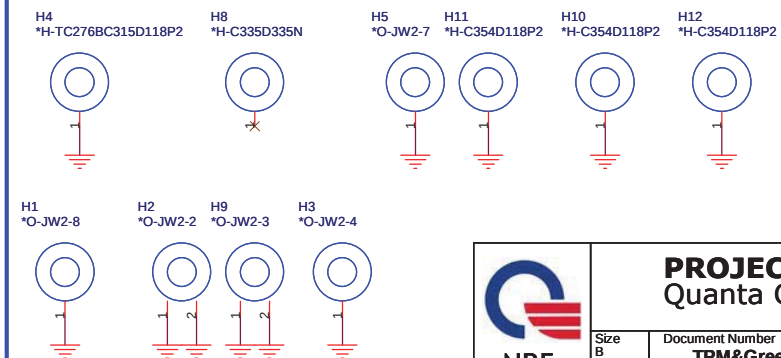
MINI PCI Pad



PCH NU Screw Hold



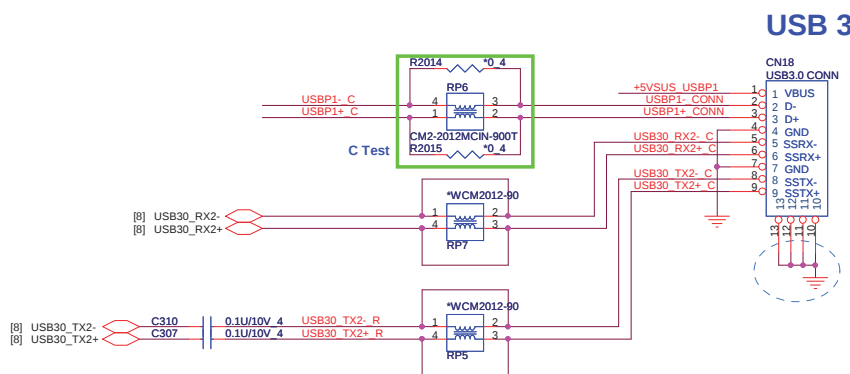
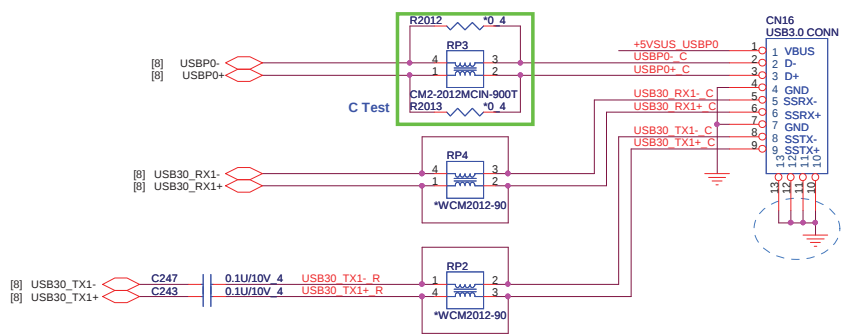
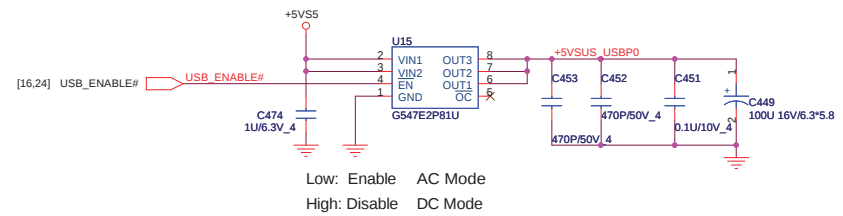
System Screw Hold



PROJECT : JW2
Quanta Computer Inc.

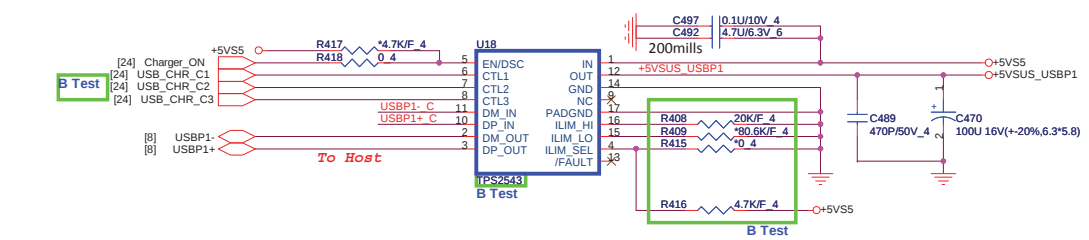
Size	Document Number	Rev
B	TPM&Green CLK	1A
Date: Tuesday, February 07, 2012	Sheet 19 of 34	

USB3.0 / USB2.0 COMBO X 2



USB Charger

high active
80 mils (lout=2A)
IOS = 48000/RILIMO
default: Auto-detect



TPS2543/45 Control Truth Table

CTL1	CTL2	CTL3	ILIM_SEL	Charging Mode	Current Limit Setting	TPS2543 STATUS Output (active low)
0	0	0	1	Discharge	NA	off
0	0	1	1	DCP/auto	IOS_PW & ILIM_HI (1)	DCP load present
0	1	0	1	SDP	ILIM_HI	off
0	1	1	1	DCP/auto	ILIM_HI	DCP load present
1	1	0	1	SDP	ILIM_HI	off
1	1	1	1	CDP	ILIM_HI	CDP load present

(1) ILIM_HI: 20K(R408), 2.4A

USB Charger option

U18	Ra	Rb	Rc
stuff	unstuff	unstuff	unstuff
unstuff	stuff	stuff	stuff

LGE SPEC	S0/S3		S4/S5	
	AC Mode	DC Mode	AC Mode	DC Mode
charge mode	CDP	CDP	DCP	DCP
user define and wake up		SDP		OFF



PROJECT : JW2
Quanta Computer Inc.

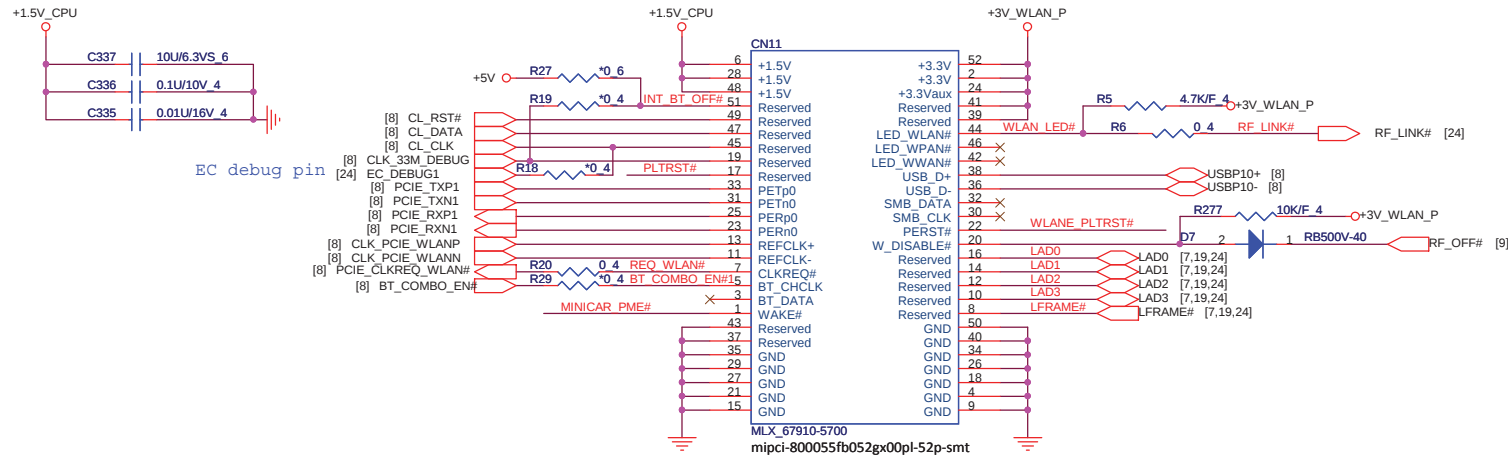
Size Custom

Document Number **USB 3.0 Connector**

Date: Tuesday, February 07, 2012 | Sheet 21 of 34

Rev 1A

Mini Card/WLAN/BT(Optional)

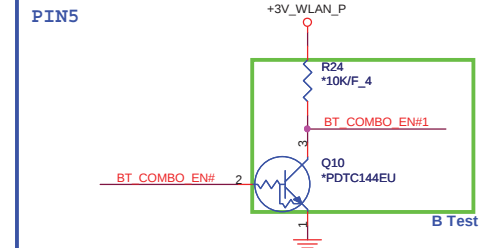
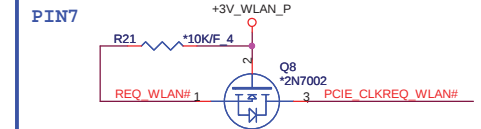
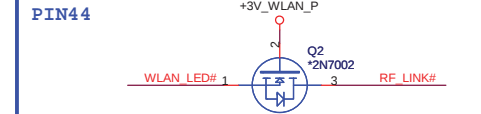


LGE mini-pcie power status		
WLAN	Bluetooth	+3V_WLAN_P
Radio-ON	Radio-ON	Power-ON
Radio-ON	Radio-OFF	Power-ON
Radio-OFF	Radio-ON	Power-ON
Radio-OFF	Radio-OFF	Power-OFF

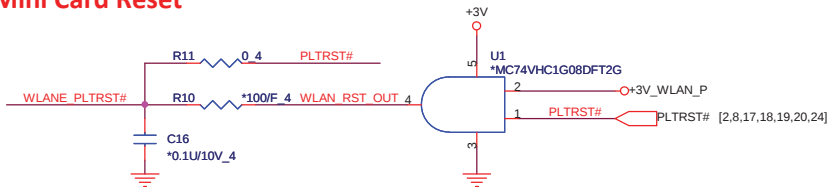
For EMI Suggestion



Avoid leakage issue

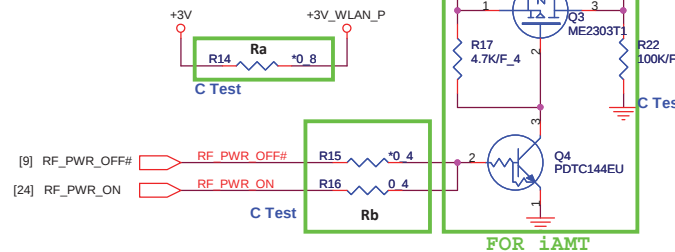


Mini Card Reset

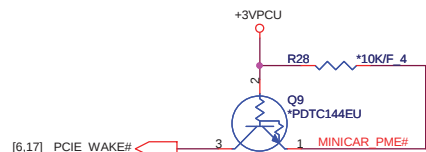


FOR iAMT option

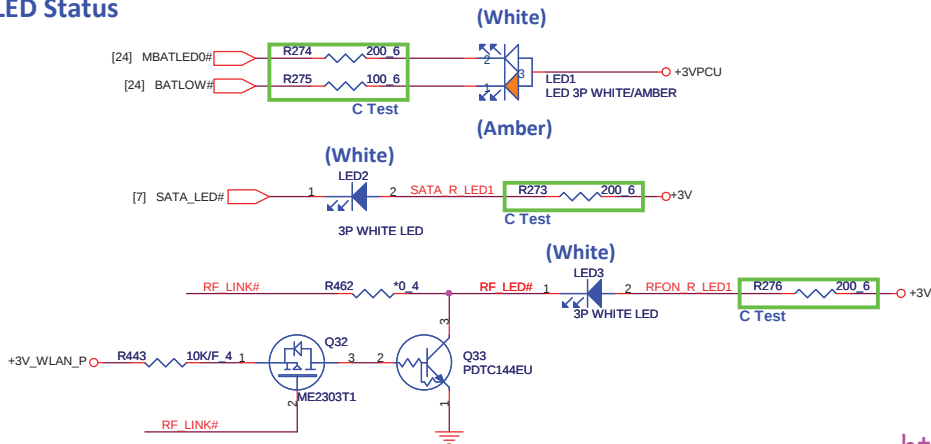
	Non-iAMT	iAMT
Ra	Stuff	NA
Rb	NA	Stuff
Q3,Q4,R17	NA	Stuff



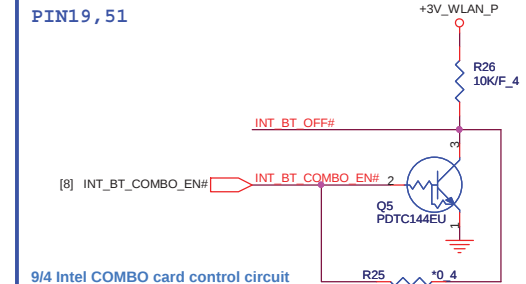
Support Wake Function(Reserve)



LED Status



Capacity module Connector



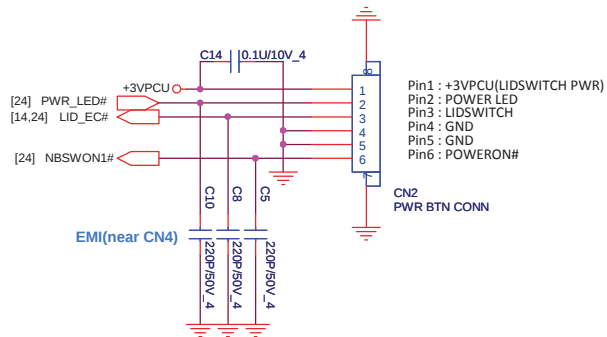
9/4 Intel COMBO card control circuit
1.add R1001,R1002,Q1001
2.add net name "INT_BT_COMBO_EN#" -> "INT_BT_OFF#"



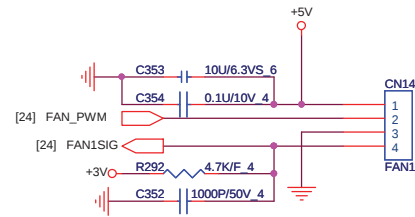
PROJECT : JW2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MINI PCIE CONN/LED	1A
Date: Tuesday, February 07, 2012	Sheet 22 of 34	

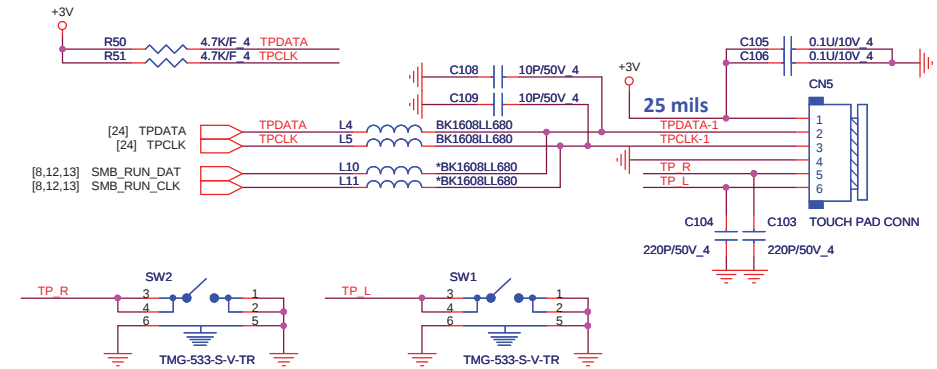
Power Button Connector



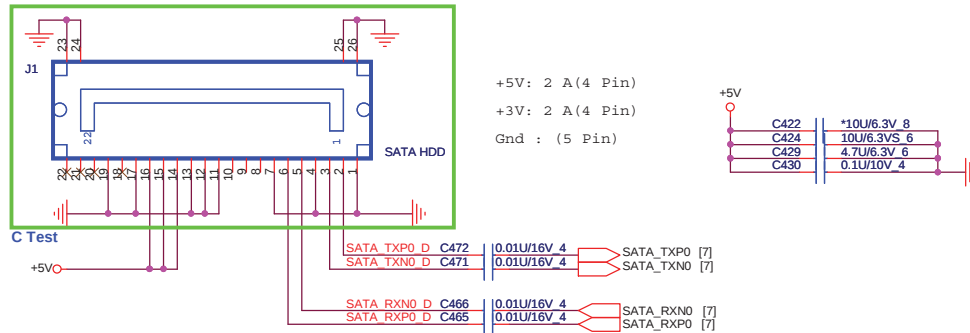
CPU FAN



Touch Pad Connector

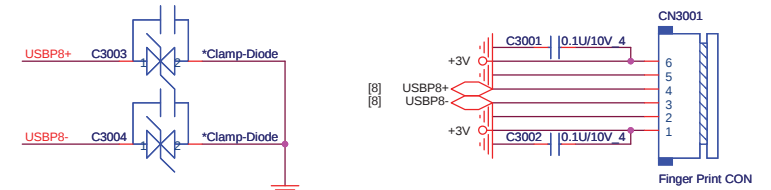


SATA HDD Connector

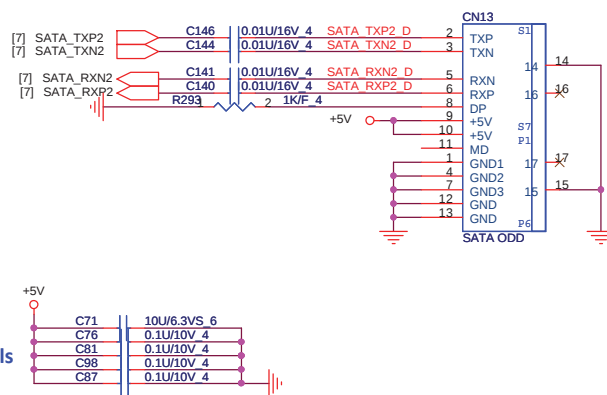


DG recommended that AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

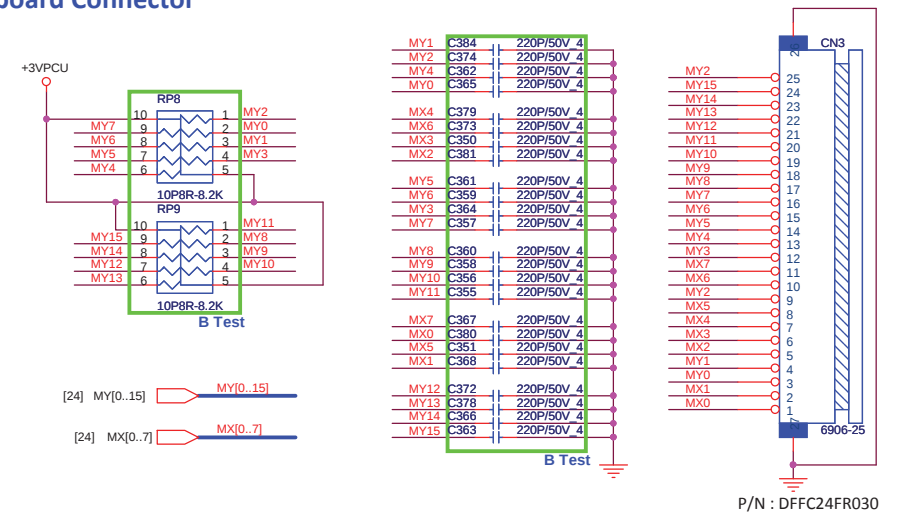
Finger Print Connector



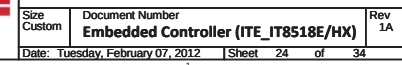
SATA ODD Connector



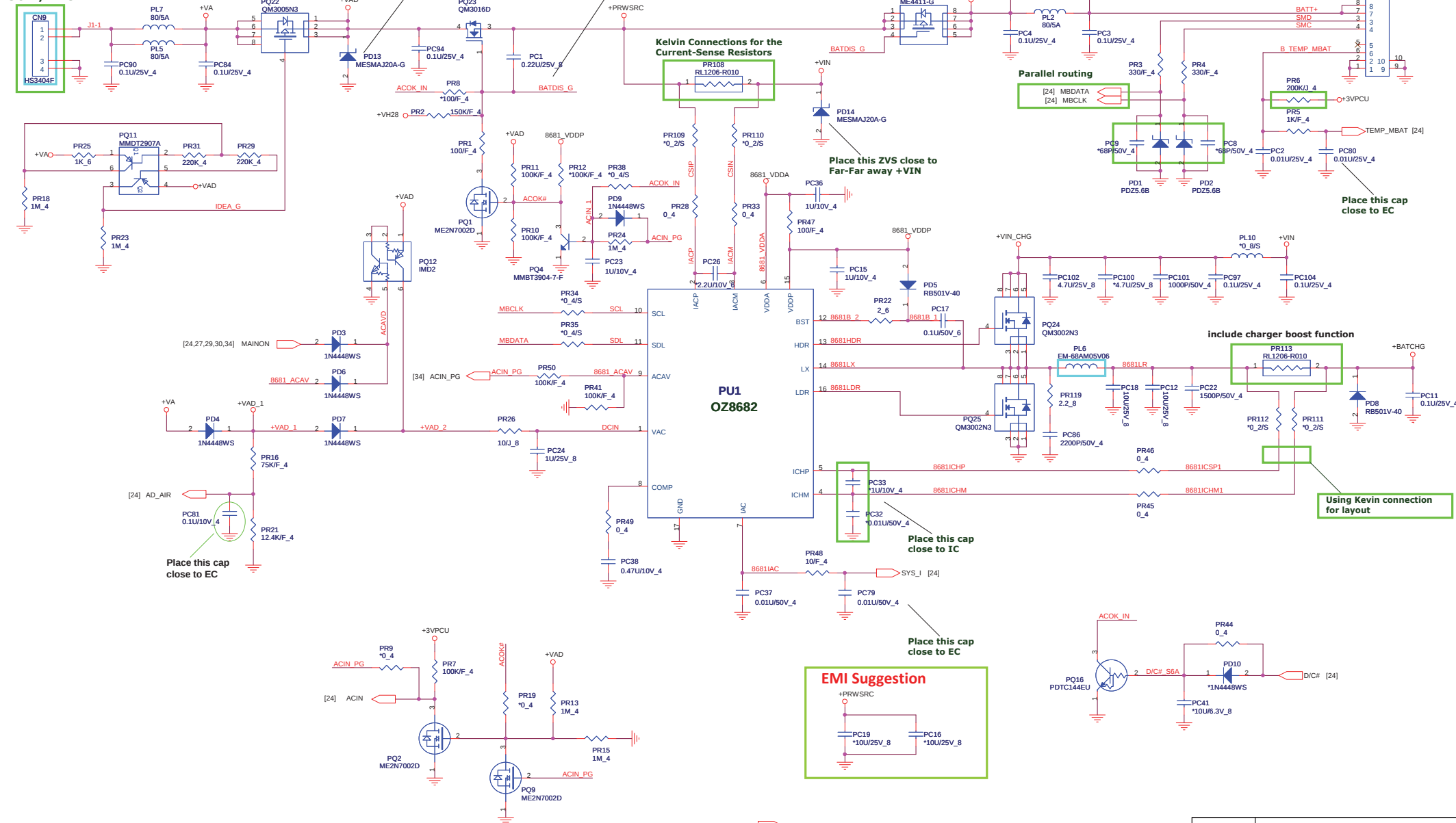
Keyboard Connector



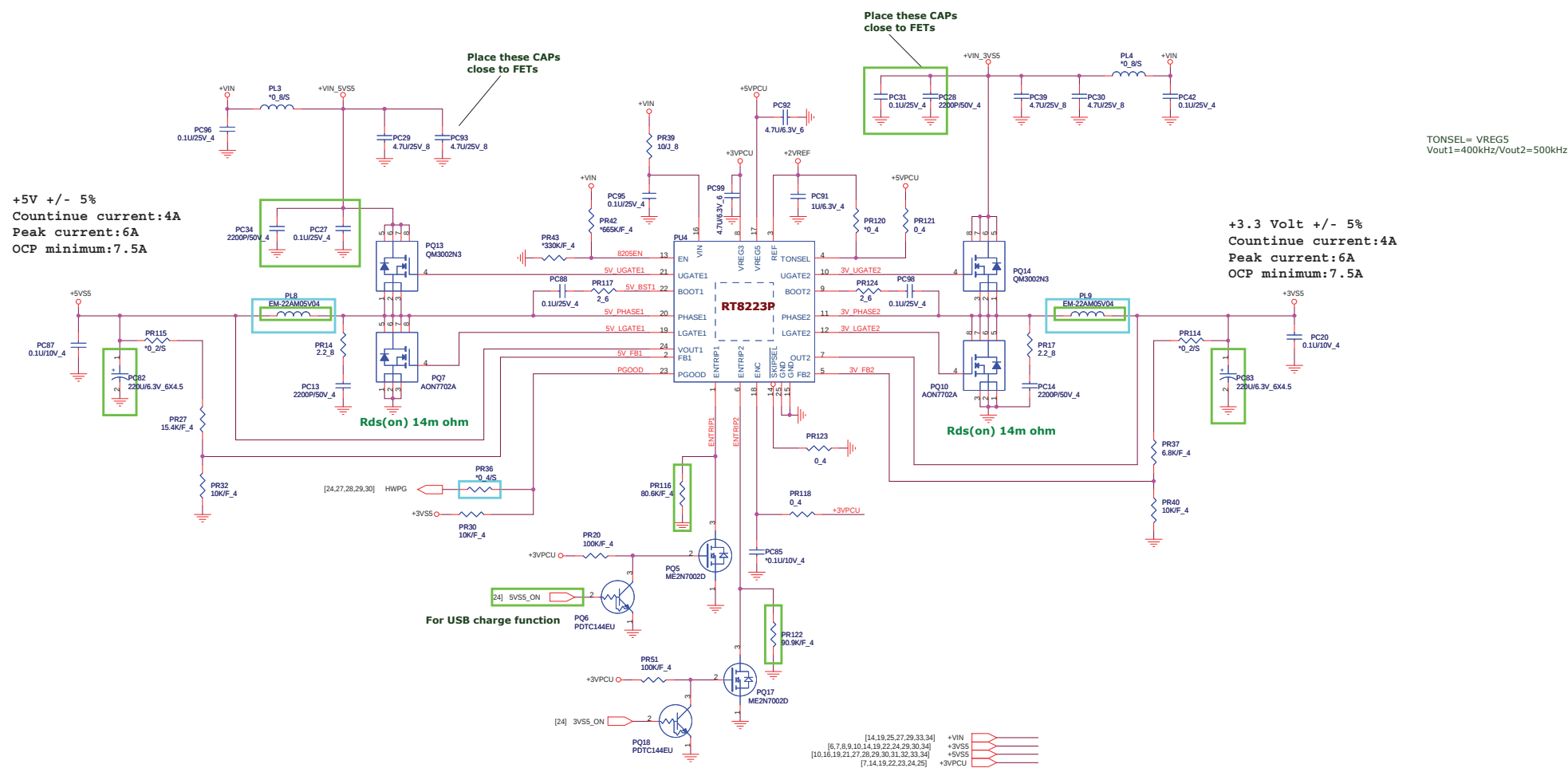
[2,6,7,8,9,10,12,13,14,15,16,17,19,20,22,24,29,32,34] +3V
[7,10,14,15,16,22,34] +5V
[7,14,19,22,24,25,26] +3VPCU

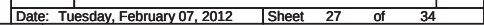


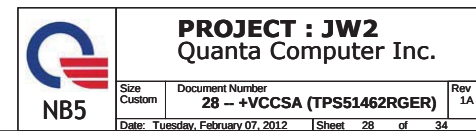
TOP DC_JACK
90W/4.75A

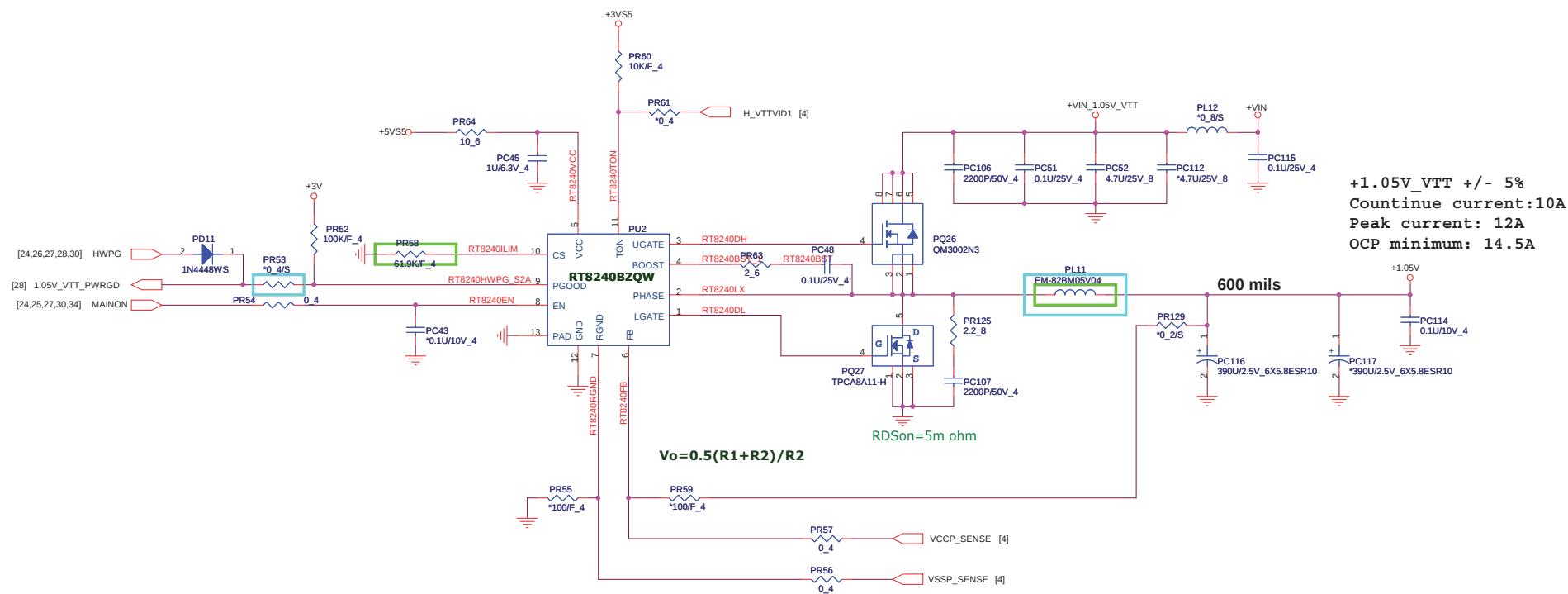


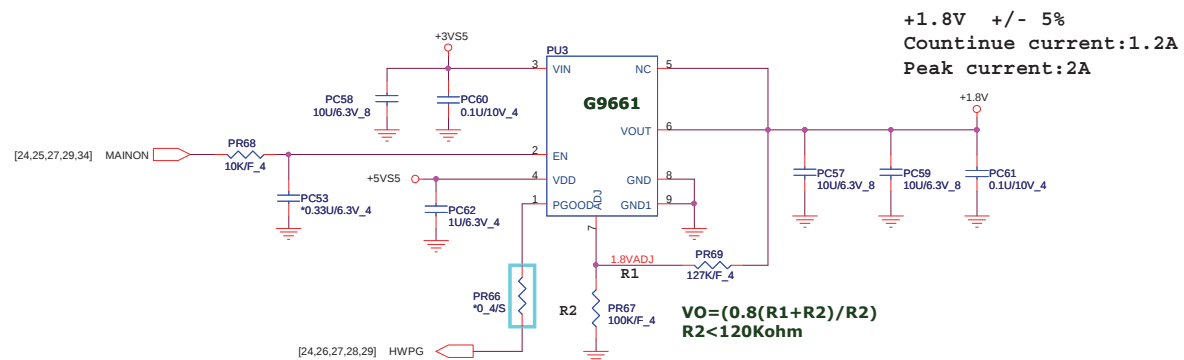
[14,19,26,27,29,33,34]	+VIN	
[34]	+VAD	
[34]	+VH28	
[34]	+VAD_1	
[7,14,19,22,23,24,26]	+3VPCU	

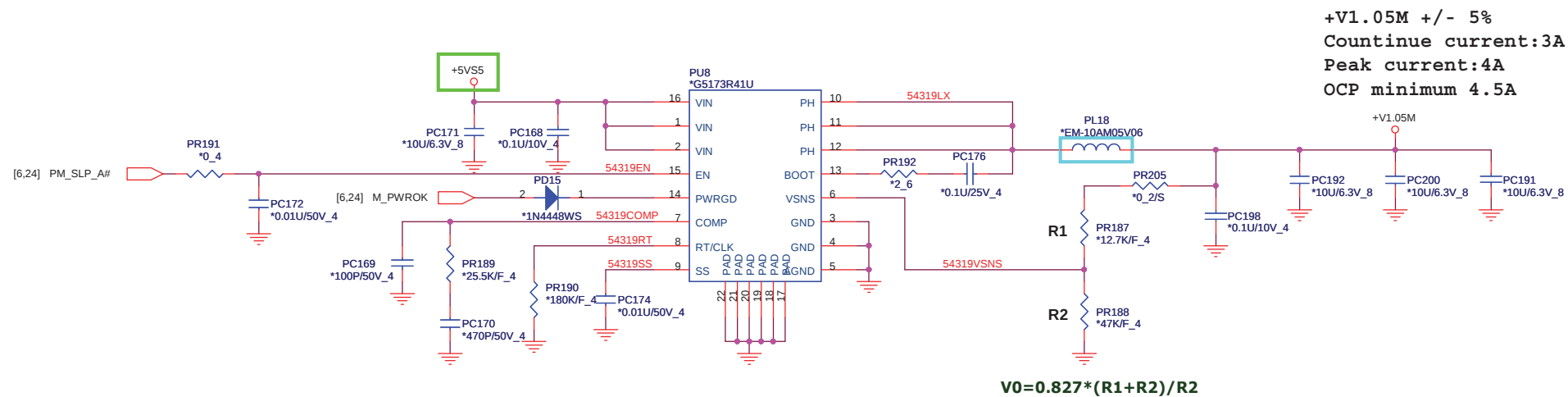












PROJECT : JW2
Quanta Computer Inc.

Size B	Document Number 31 -- +V1.05M (G5173)	Rev 1A
Date: Tuesday, February 07, 2012 Sheet 31 of 34		

