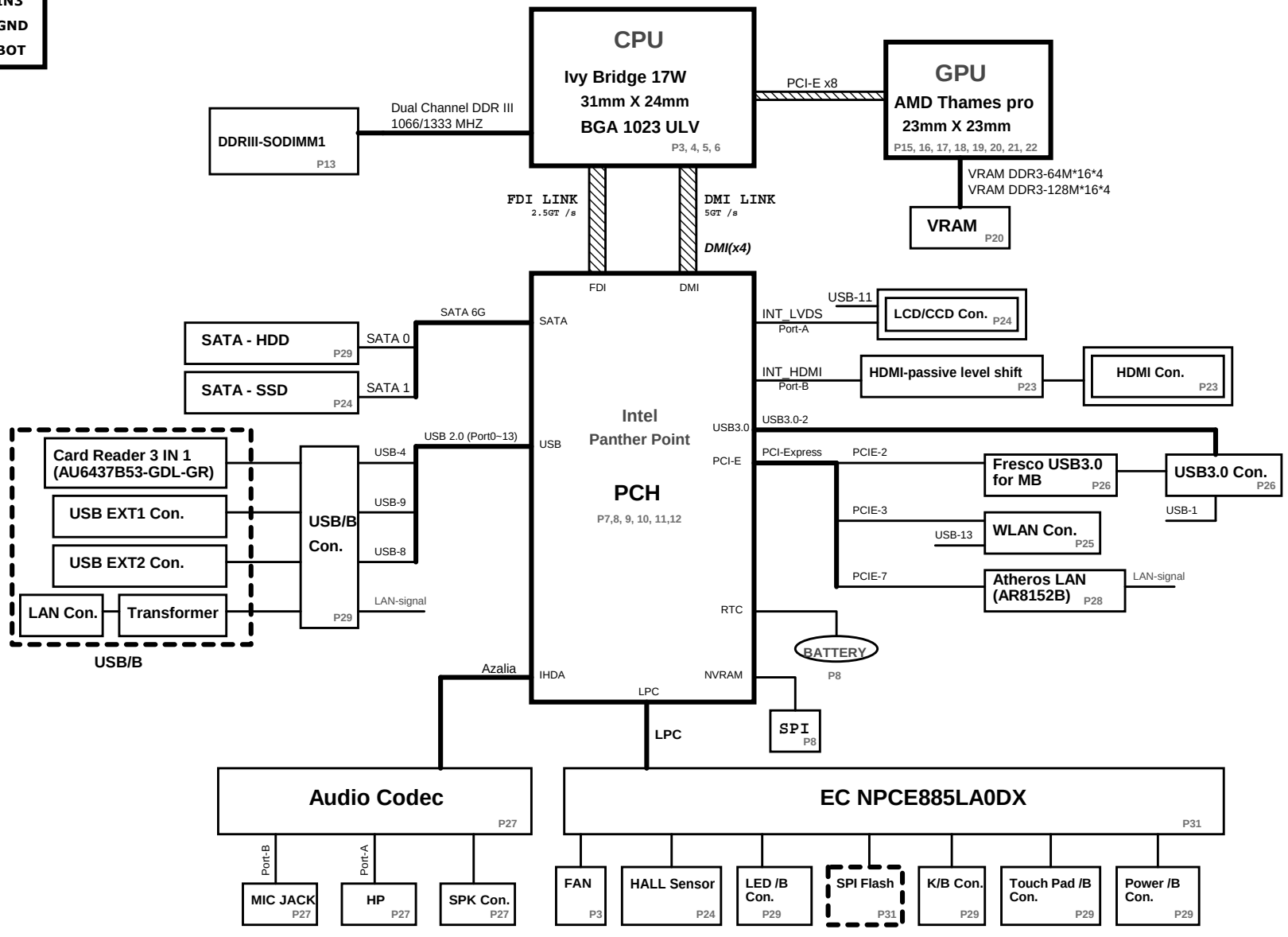
PCB 8 layer Stackups

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : SVCC
- LAYER 5 : IN2
- LAYER 6 : IN3
- LAYER 7 : GND
- LAYER 8 : BOT

BY2D Block Diagram



POWER SYSTEM

ISL88731CHRTZ-T	P32
RT8223P	P33
TPS51216RUKR	P34
OZ80116	P35
RT9046GE	P36
ISL95837HRZ-T	P37
G966A	P38
ISL95870A	P37

+VCC_CORE

+1.5V
+1.5VSUS

+VTT
+1.05V

+1.8V

+1.5V_S5
+3VPCU
+3V_S5
+3V
+5VPCU
+5V_S5
+5V
+SMDDR_VTERM
+SMDDR_VREF
+VCCSA

+VCORE_GFX
+3V_GFX
+1.05V_GFX
+1.5V_GFX

Quanta Computer Inc.
PROJECT : BY2D

Size	Document Number	Rev
	Block Diagram	3B

Date: Monday, March 26, 2012 Sheet 1 of 42

02

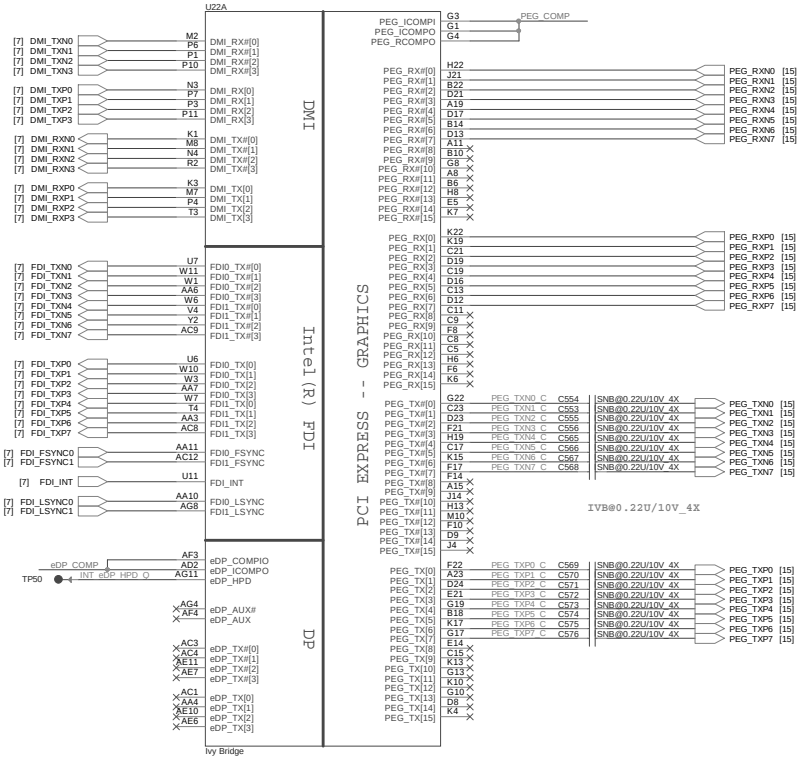
Table of Contents

Power plant table

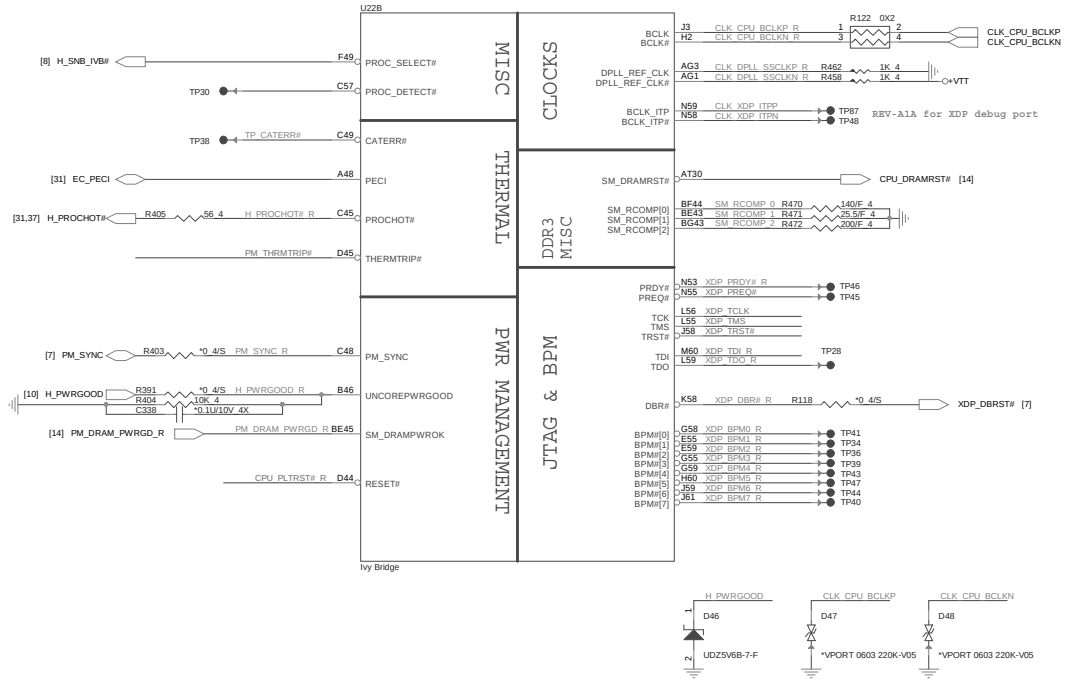
POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	6V~+19V		S0~S5
+VCCRTC	+3.0V~+3.3V		S0~S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0~S5
+3V_HDP	+3.3V	MAIN_ON	S0
+3VPCU	+3.3V	AC/DC Insert enable	S0
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0~S5
+5VPCU	+5V	AC/DC Insert enable	S0~S5
WIMAX_P	+3.3V	WMAX_P for EC	
+1.8V	+1.8V	MAIN_ON	S0
+1.5V	+1.5V	MAIN_ON	S0
+1.5V_SUS	+1.5V	SUSON	S0~S3
+VCC_CORE		VRON	S0
+VTT/+1.05V	+1.05V	MAIN_ON	S0
+VCCSA	+0.75V~+0.9V	HWPG_VCCIO	S0
+VAXG		GFXVR_EN	S0
+3V_GPU	+3.3V	DGPU_PWR_EN#	S0
+1.8V_GPU	+1.8V	DGPU_PWR_EN	S0
+1.5V_GPU	+1.5V	DGPU_PWROK	S0
+1V_GPU	+1V	DGPU_PWR_EN	S0
+BIF_VDDC	+0.875V~+1V	DGPU_PWROK	S0
+VGPU_CORE	+0.875V~+1V	PX_PWRGOOD	S0

<CPU>

Ivy/Sandy Bridge Processor (DMI,PEG,FDI)

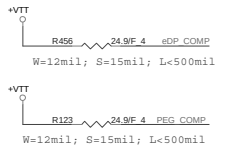


Ivy/Sandy Bridge Processor (CLK,MISC,JTAG)

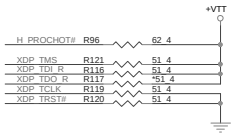


FDI Disabling (Discrete Only) <CPU>

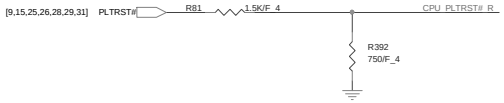
DP & PEG Compensation <CPU>



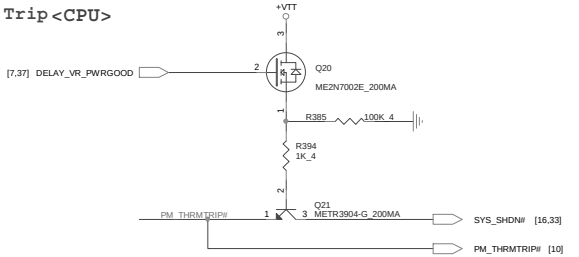
Processor pull-up <CPU>



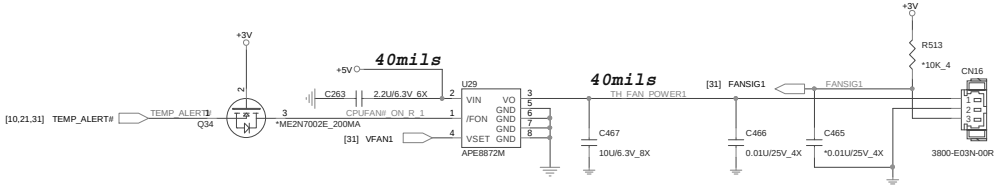
Level Shift <CPU>



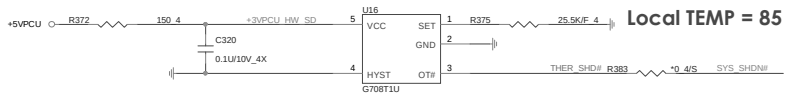
Thermal Trip <CPU>



FAN Control-->For one FAN solution <THC>



CPU Thermal sensor / MB Local TEMP <THC>



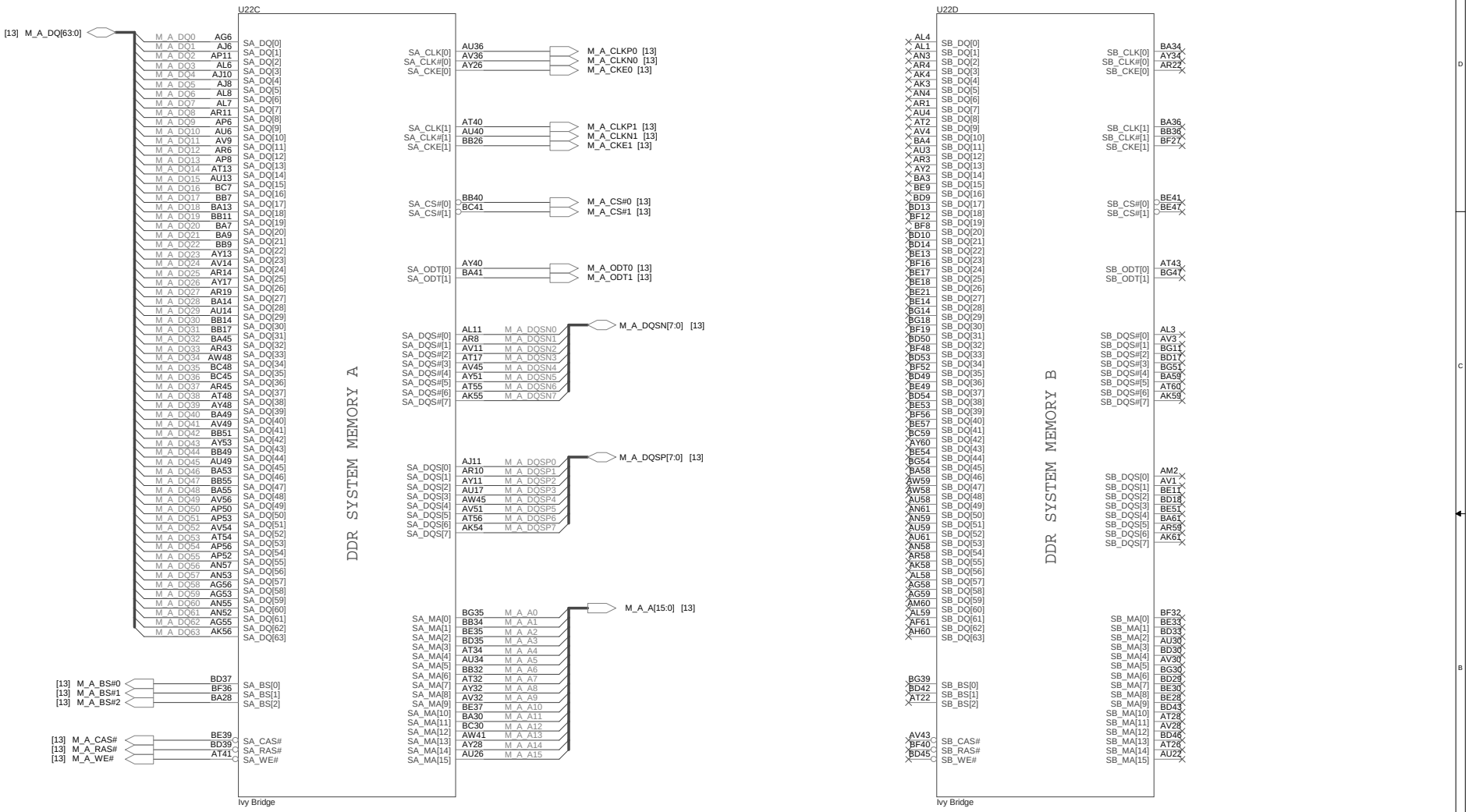
Rset(Kohm)=0.0012T*T-0.9308T+96.147,Shut down on 85dgree
Hysteresis is 30C

Quanta Computer Inc.	
PROJECT : BY2D	
Size	Document Number: Ivy/Sandy Bridge 1/4 — Rev: 3B
Date: Monday, March 26, 2012	Sheet 3 of 42

03

<CPU>

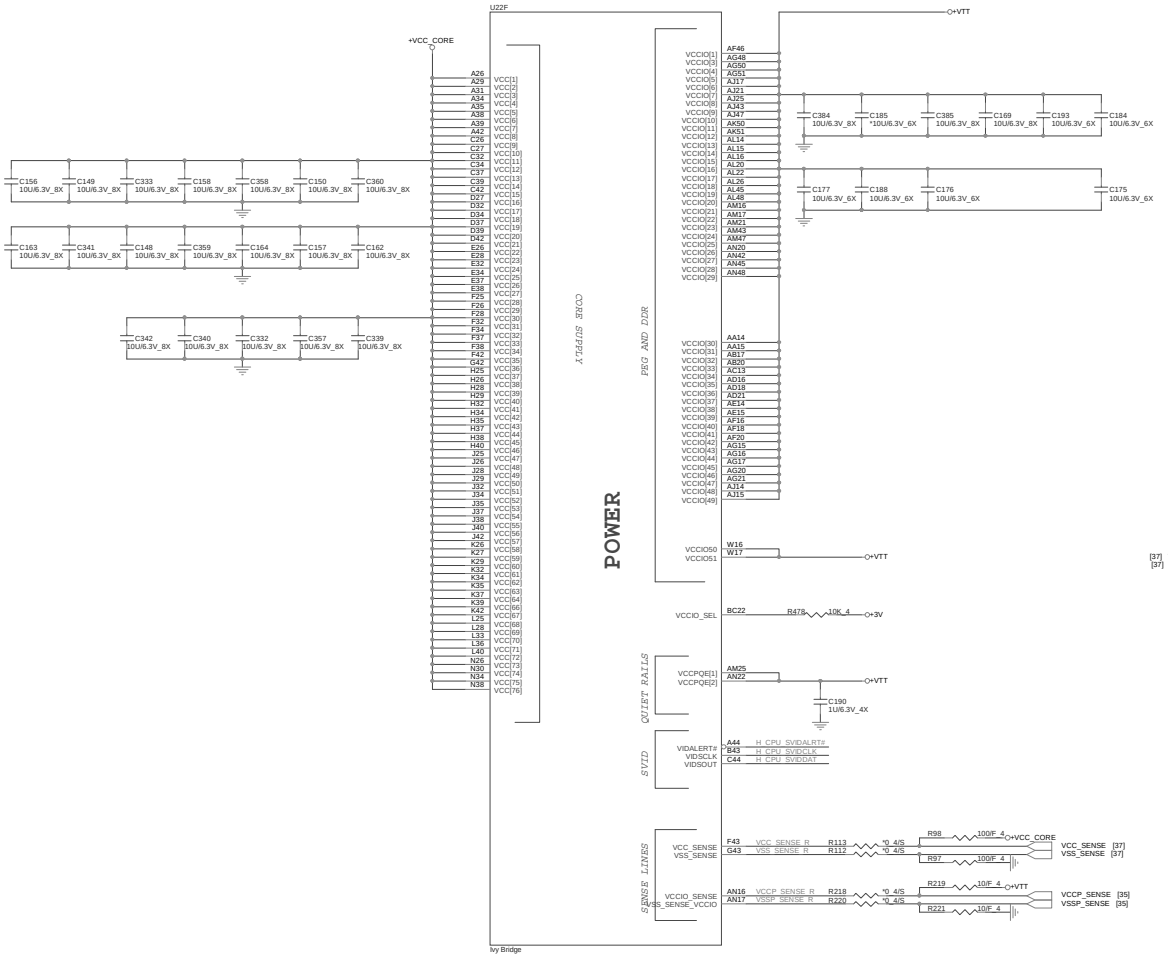
Ivy/Sandy Bridge Processor (DDR3)



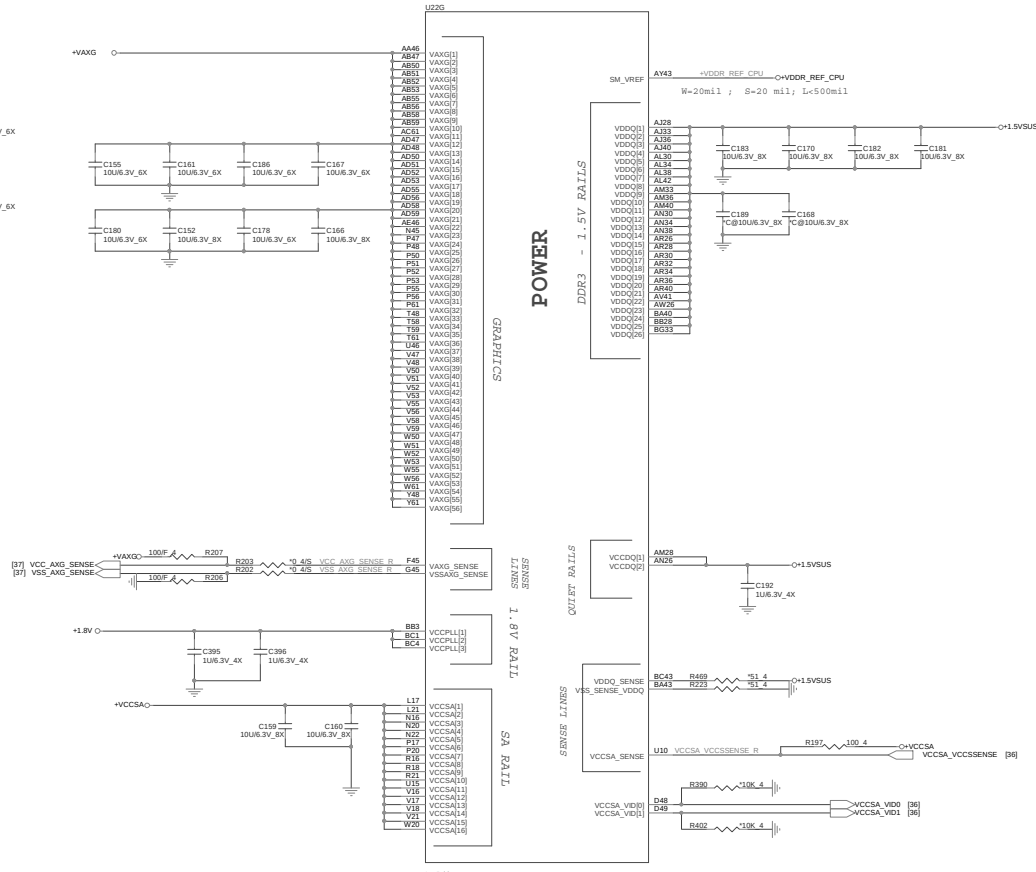
Quanta Computer Inc.		
PROJECT : BY2D		
Size	Document Number: Ivy/Sandy Bridge 2/4	Rev: 3B
Date: Monday, March 26, 2012	Sheet 4 of 42	

<CPU>

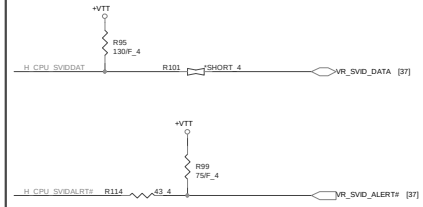
Ivy/Sandy Bridge Processor (POWER)



Ivy/Sandy Bridge Processor (GRAPHIC POWER)



Layout note: need routing together and ALERT need between CLK and DATA

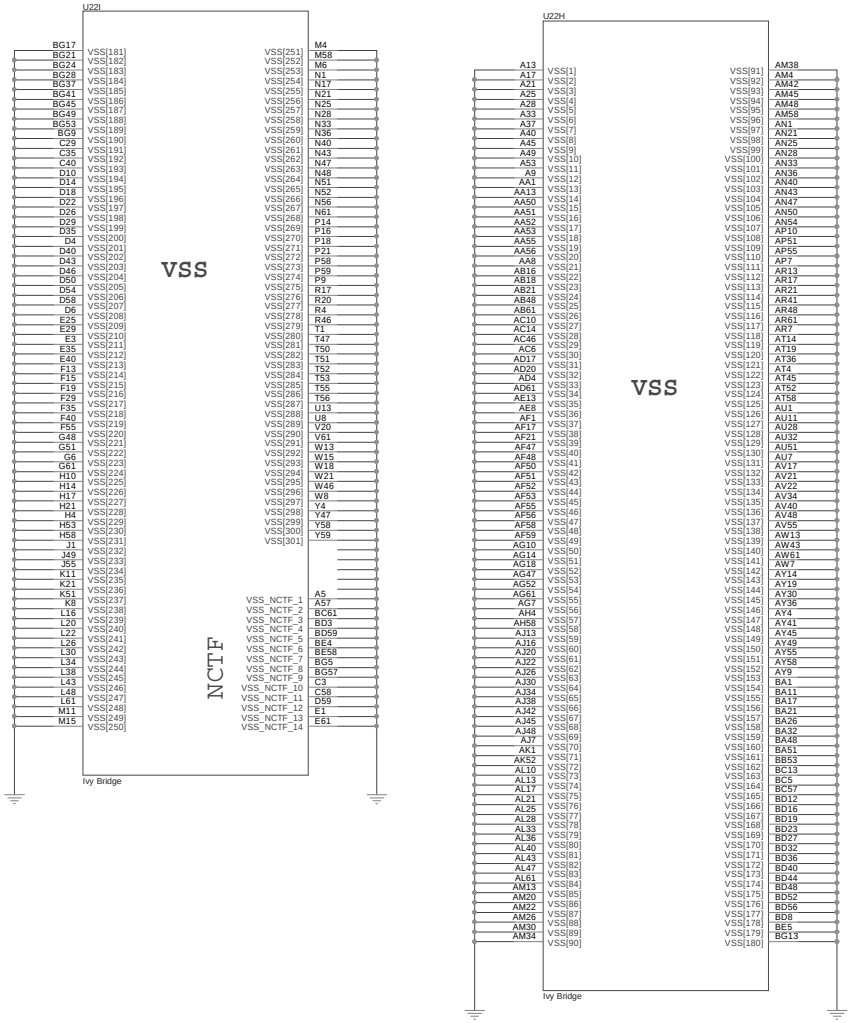


Quanta Computer Inc.			
PROJECT : BY2D			
Size	Document Number: Ivy/Sandy Bridge 3/4		Rev: 3B
Date: Monday, March 26, 2012	Sheet 5 of 42		

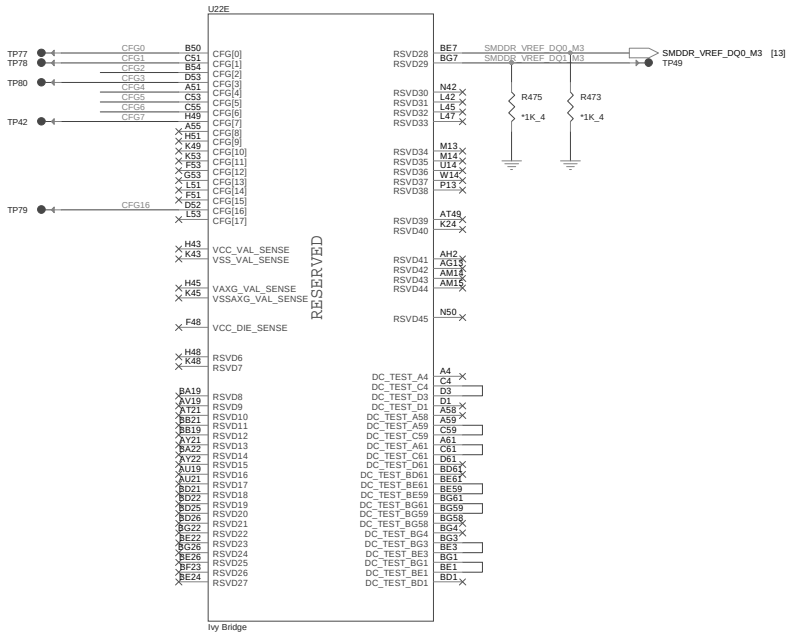
<CPU>

06

Ivy/Sandy Bridge Processor (GND)

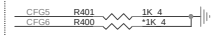


Ivy/Sandy Bridge Processor (RESERVED, CFG)



Processor Strapping

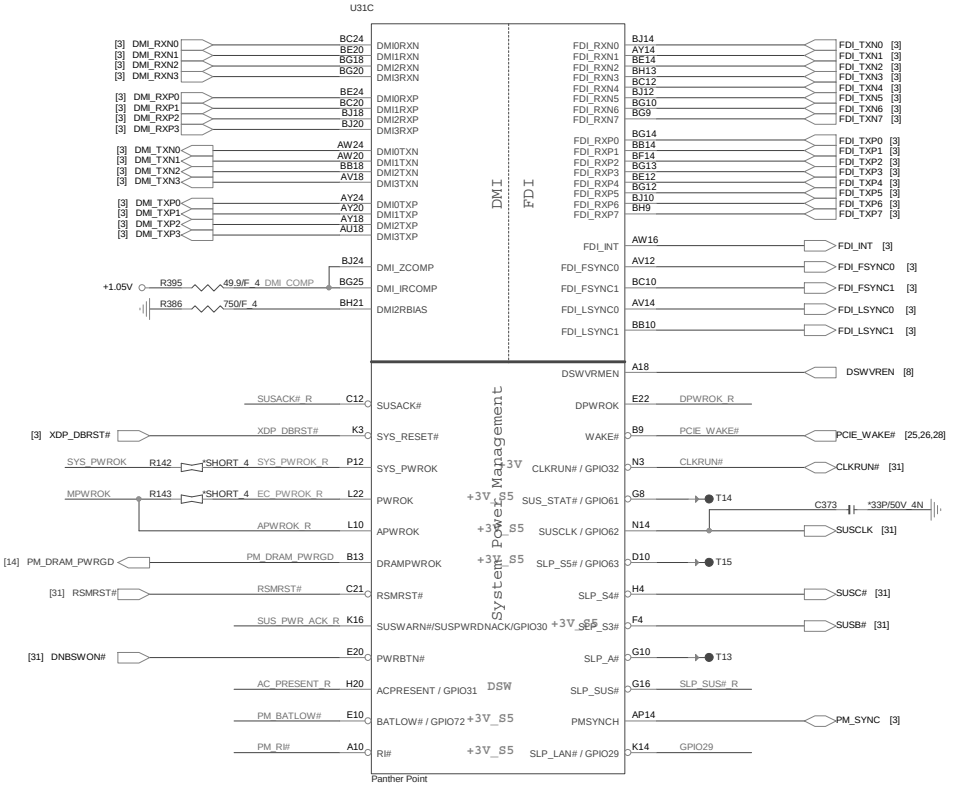
	1	0
CFG2 (PCI-E Static x16 Lane Reversal)	Normal Operation	Lane Reversed
CFG3 (PCI-E Static x4 Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP



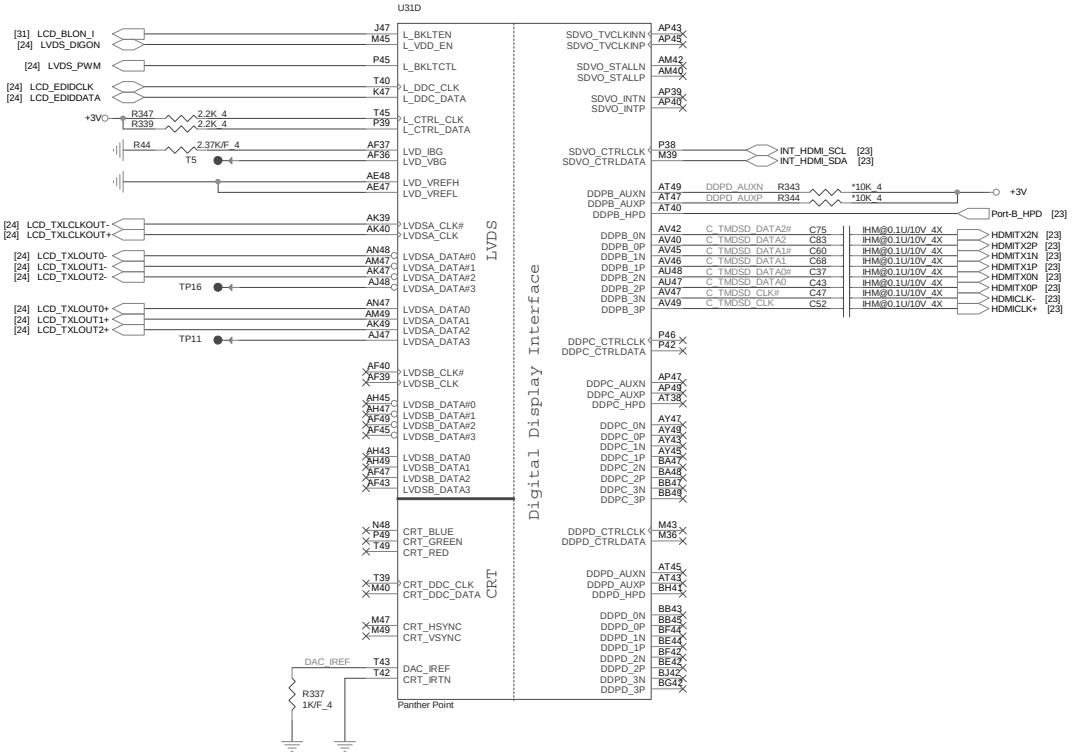
CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

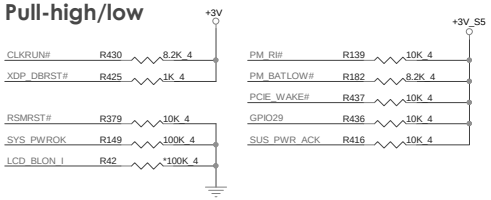
Panther/Cougar Point (DMI,FDI,PM)



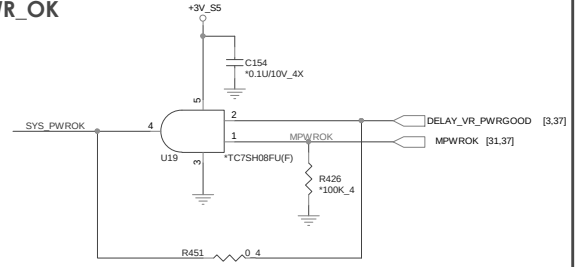
Panther/Cougar Point (LVDS,DDI)



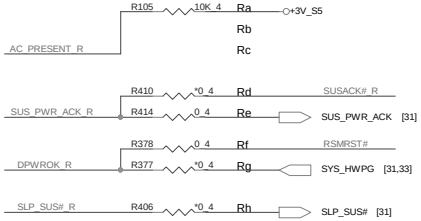
PCH Pull-high/low <CLG>



System PWR_OK <CLG>



Deep Sx <CLG>



Net Name	Deep Sx Support	Deep Sx No Support
AC_PRESENT	Rb,Rc stuff	Ra stuff
SUS_PWR_ACK	Rd stuff	Re stuff
DPWROK	Rg stuff	Rf stuff
SLP_SUS	Rh stuff	Rh No stuff

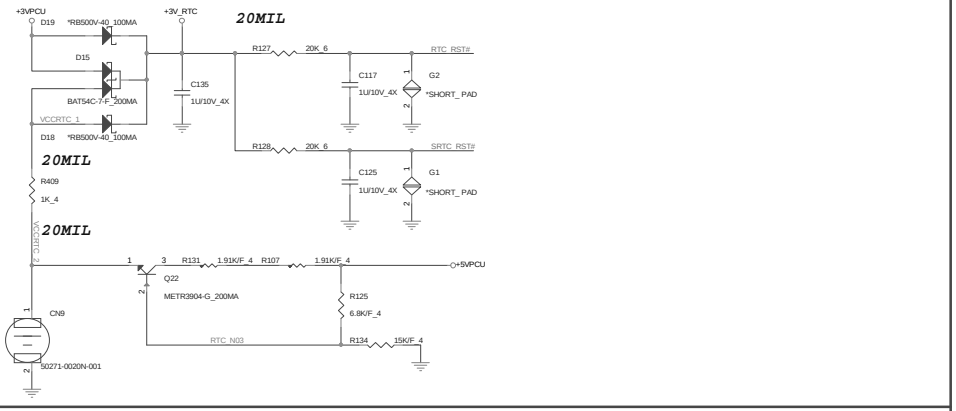
Quanta Computer Inc.

PROJECT : BY2D

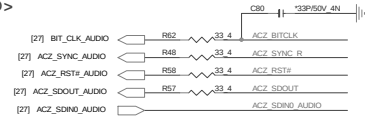
Size	Document Number	Rev
	Panther/Cougar Point 1/6	3B

Date: Monday, March 26, 2012 Sheet 7 of 42

RTC Circuit <RTC>

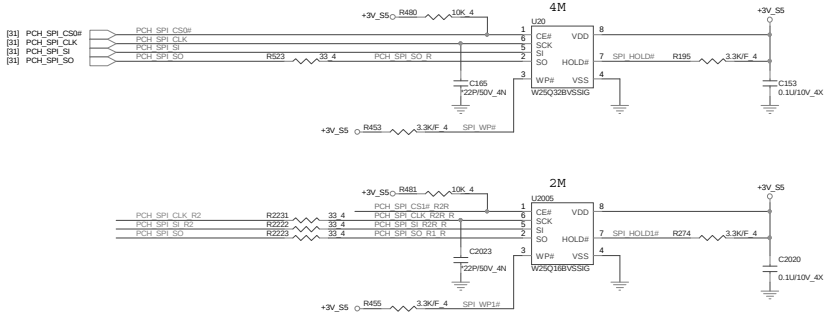


HDA Bus <ADO>



PCH JTAG Debug (CLG)

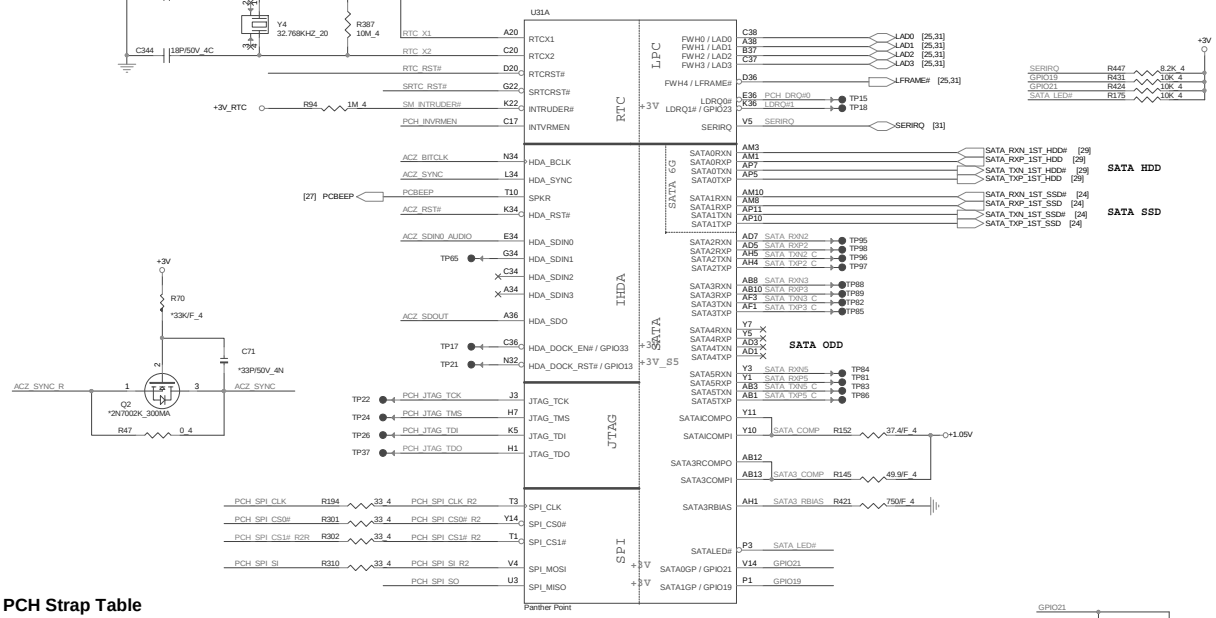
PCH Dual SPI (CLG)



PCH2 <CLG> <ADO> <RTC>

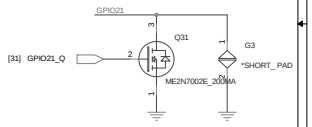
Panther/Cougar Point (HDA,JTAG,SATA)

08



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	R432 *1K_4 PCBEEP
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R352 *1K_4 PCI_GNT3# [9]
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	R84 330K_4 PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GPIO19 / Boot Location: 1 / 1 / SPI *; 0 / 0 / LPC	R49 *1K_4 GNT1# [9]
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		R441 *1K_4 GPIO19
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)	R55 *1K_4 ACZ_SDOUT ACZ_SDOUT [31]
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)	R423 2.2K_4 R427 1K_4 +1.8V DF_TVS [10] H_SNB_IVB# [3]
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R443 *10K_4 R444 *1K_4 PLL_ODVR_EN [10]
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	R50 1K_4 ACZ_SYNC
GPIO15	TLS Confidentiality	RSMRST	0 = Default. TLS no Confidentiality 1 = TLS Confidentiality	R132 1K_4 GPIO15 [10]
DSWVRMEN	Deep S4/S5 Well On -Die Voltage Regulator Enable	ALWAYS	0 = Disable 1 = Enable	DSWVREN [7] R89 330K_4 R90 *330K_4
INIT3_3V#	**Reserved**	PWROK	1 = Default (weak pull-up 20K)	**Should not pull low. leave as No Connect**
GNT2#/ GPIO53	**ESI Strap (Server Only)**	PWROK	1 = Default. Should not be pulled low for desktop and mobile	**Should not pull low for desktop and mobile**
L_DDC_DATA	LVDS Detected	PWROK	0 = Default. Not Detected 1 = Detected	1= PU to 3V
SDVO_CTRLDATA	Port B Detected	PWROK	0 = Default. Not Detected 1 = Detected	1= PU to 3V
DDPC_CTRLDATA	Port C Detected	PWROK	0 = Default. Not Detected 1 = Detected	0=NC
DDPD_CTRLDATA	Port D Detected	PWROK	0 = Default. Not Detected 1 = Detected	0=NC
SATA3GP/ GPIO37	**Reserved**	PWROK	0 = Default	**Should not be pulled high when strap is sampled**
SATA2GP/ GPIO36	**Reserved**	PWROK	0 = Default	**Should not be pulled high when strap is sampled**



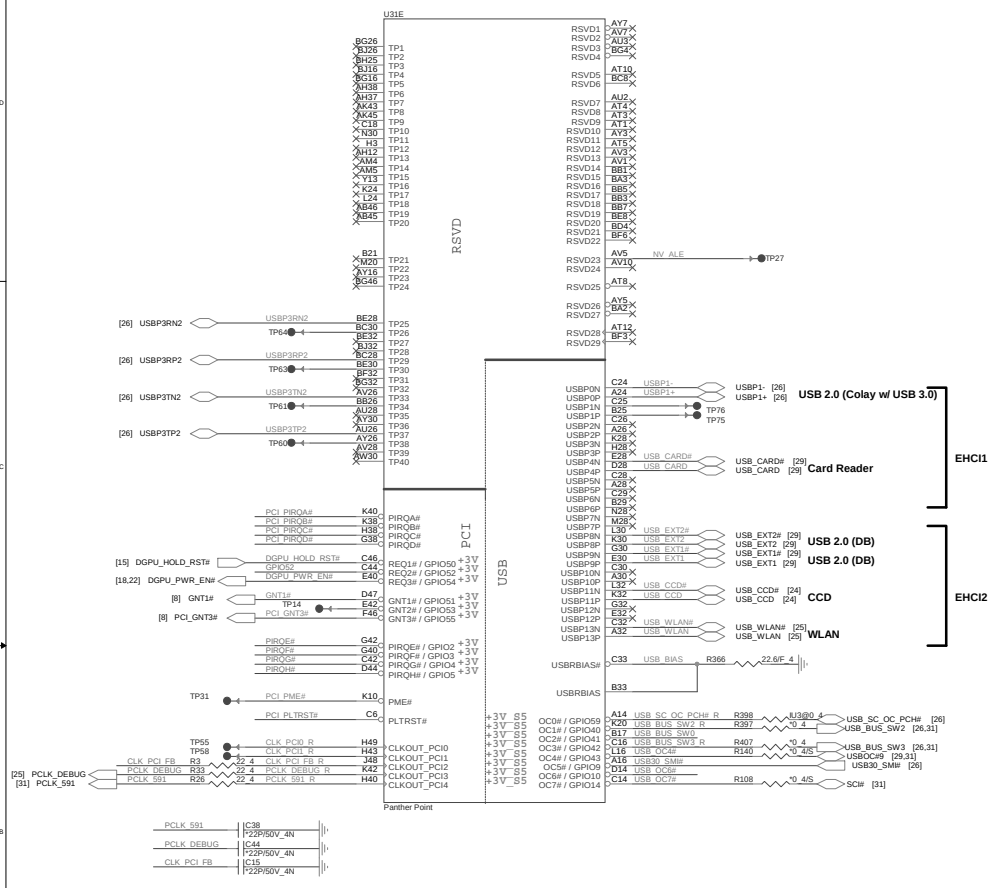
Quanta Computer Inc.

PROJECT : BY2D

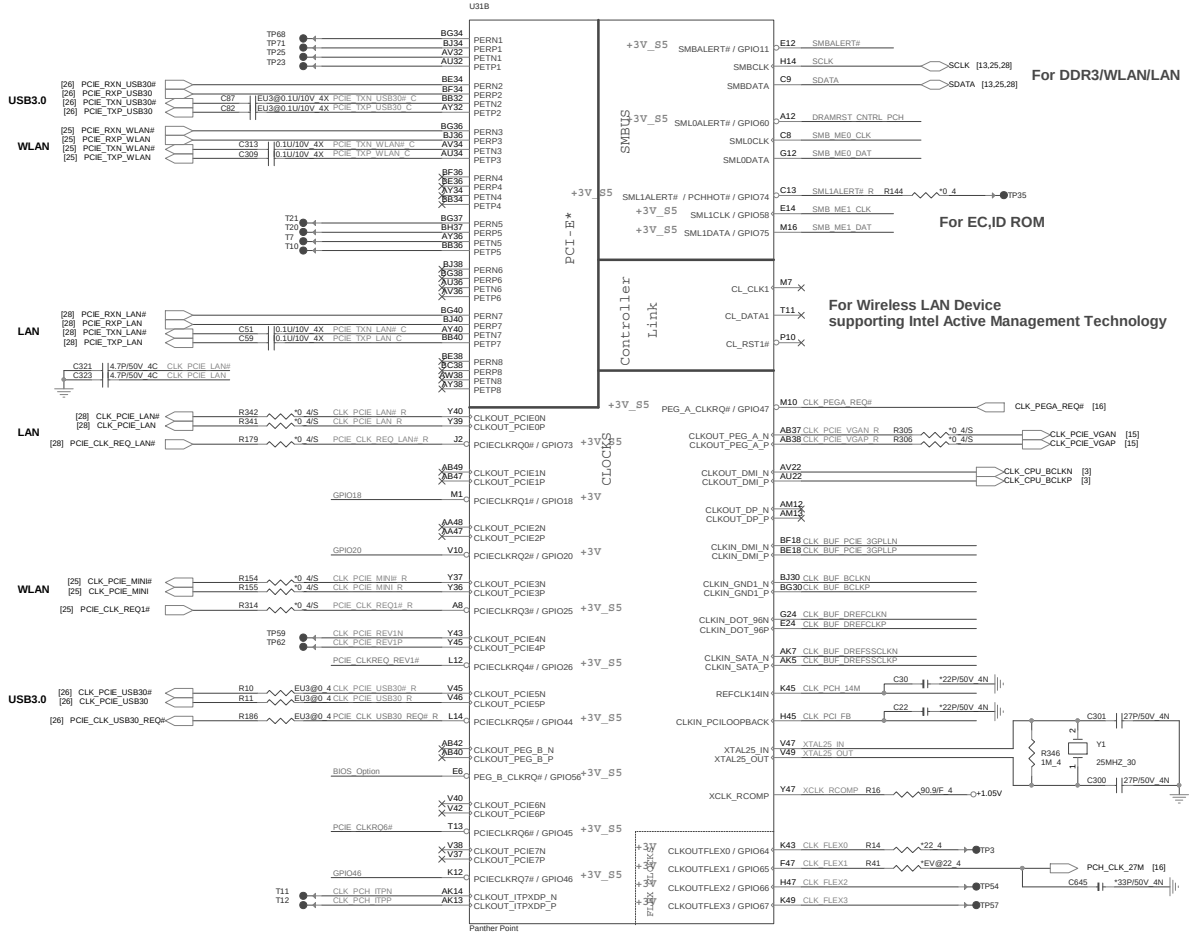
Size	Document Number	Rev
	Panther/Cougar Point 2/6	3B

Date: Monday, March 26, 2012 Sheet 8 of 42

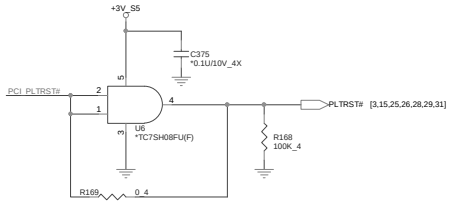
Panther/Cougar Point-M (PCI,USB,NVRAM)



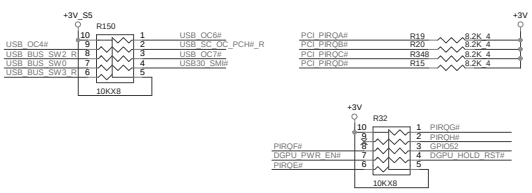
Panther/Cougar Point-M (PCI-E,SMBUS,CLK)



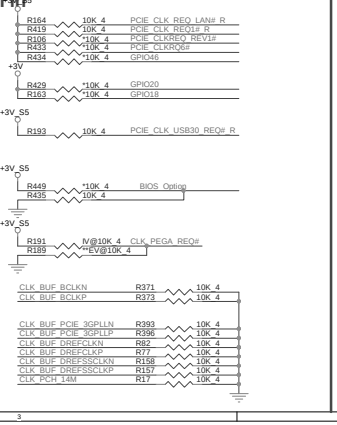
PLTRST# <CLG>



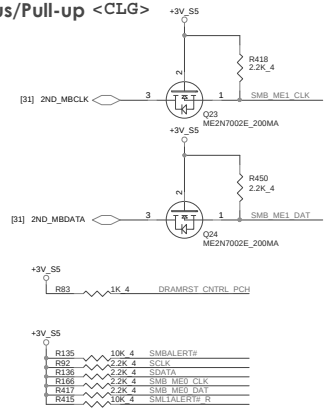
PCI/USBOC# Pull-up <CLG>



CLK_REQ/Strap Pin <CLG>



SMBus/Pull-up <CLG>



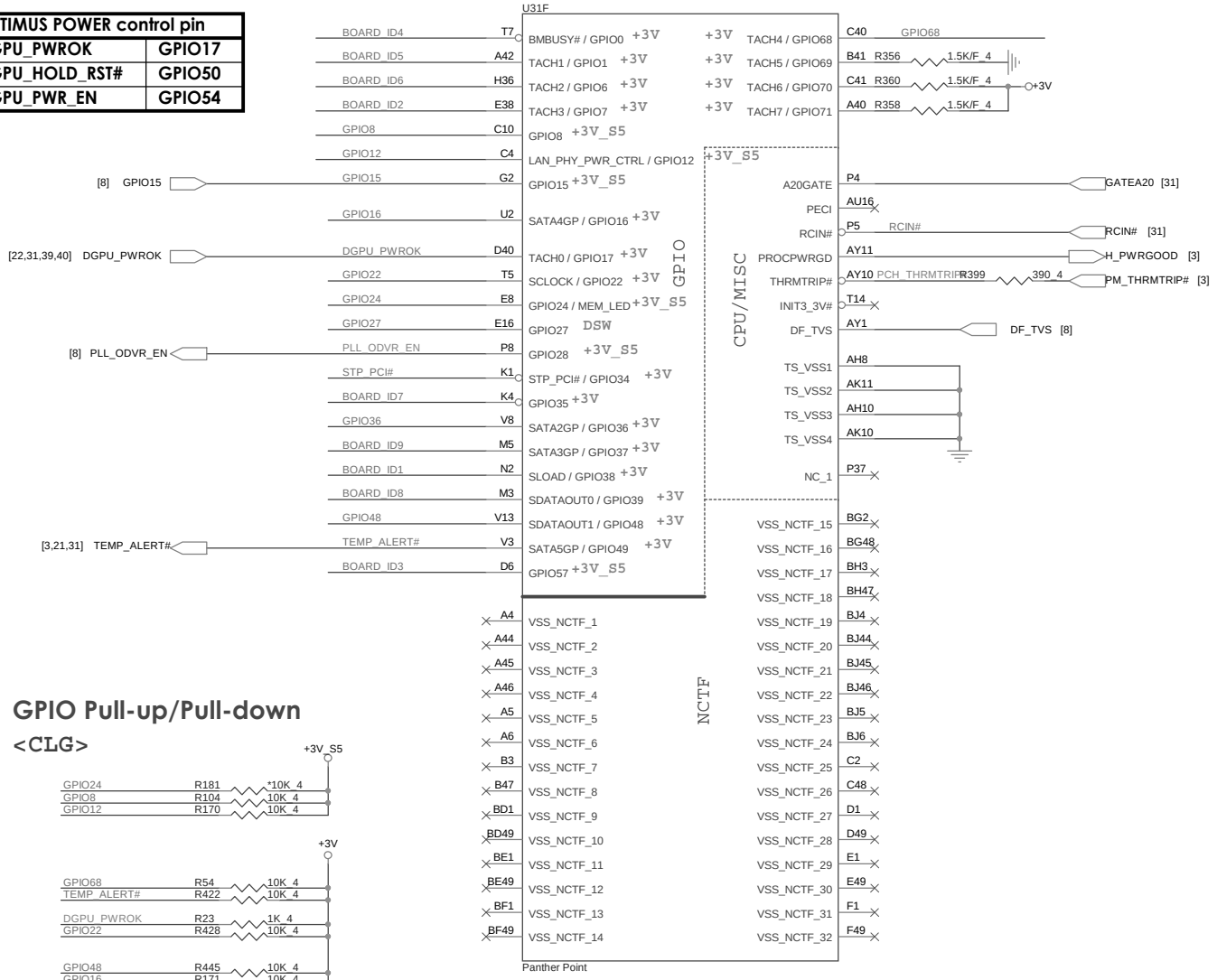
	33MHz	27MHz	48/24MHz	14.318MHz	25MHz
CLK_FLEX0	●	●	●	●	
CLK_FLEX1		●	●	●	
CLK_FLEX2	●	●	●	●	●
CLK_FLEX3		●	●	●	

Quanta Computer Inc.			
PROJECT : BY2D			
Size	Document Number		Rev
	Panther/Cougar Point 3/6		3B
Date: Monday, March 26, 2012	Sheet 9	of 42	

<CLG>

Panther/Cougar Point (GPIO,VSS_NCTF,RSVD)

OPTIMUS POWER control pin	
DGPU_PWROK	GPIO17
DGPU_HOLD_RST#	GPIO50
DGPU_PWR_EN	GPIO54



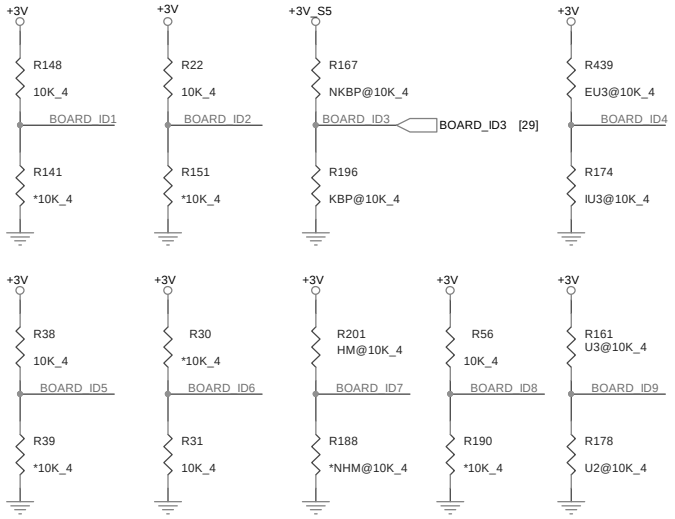
GPIO Pull-up/Pull-down

<CLG>

BOARD ID SETTING <CLG>

10

Board ID	ID1	ID2	ID3	ID4	ID5	ID6	ID7	ID8	ID9
BU6 SKU KZ1 SKU	H L								
BY2D BY2		H L							
W/O LED KB W/ LED KB			H L						
Ext USB3.0 Int USB3.0				H L					
Reserve					H L				
W/O CCD W/ CCD						H L			
W/ HDMI W/O HDMI							H L		
BY1 BU6 or KZ1								H L	
W/ USB3.0 W/O USB3.0									H L

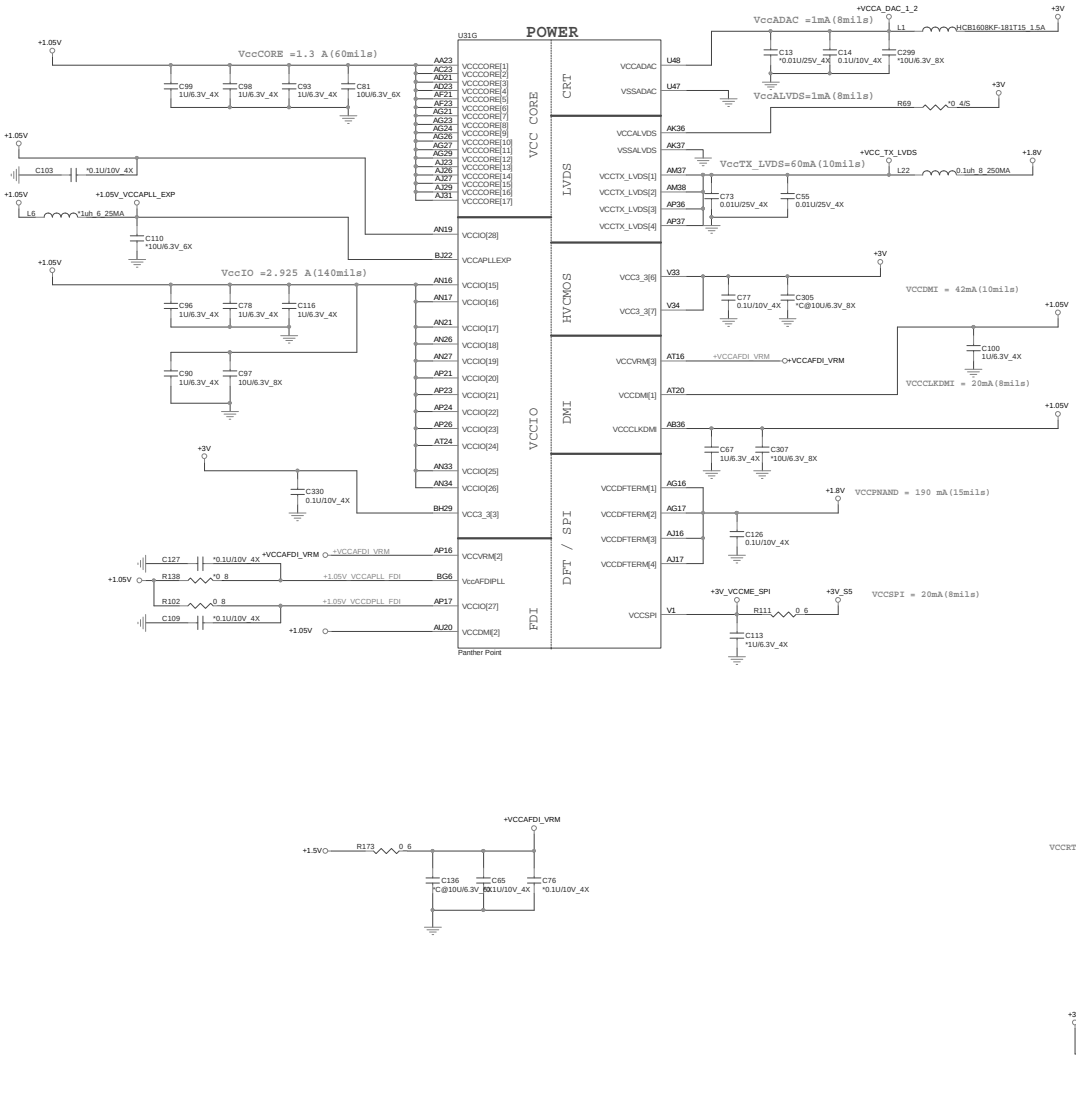


Quanta Computer Inc.

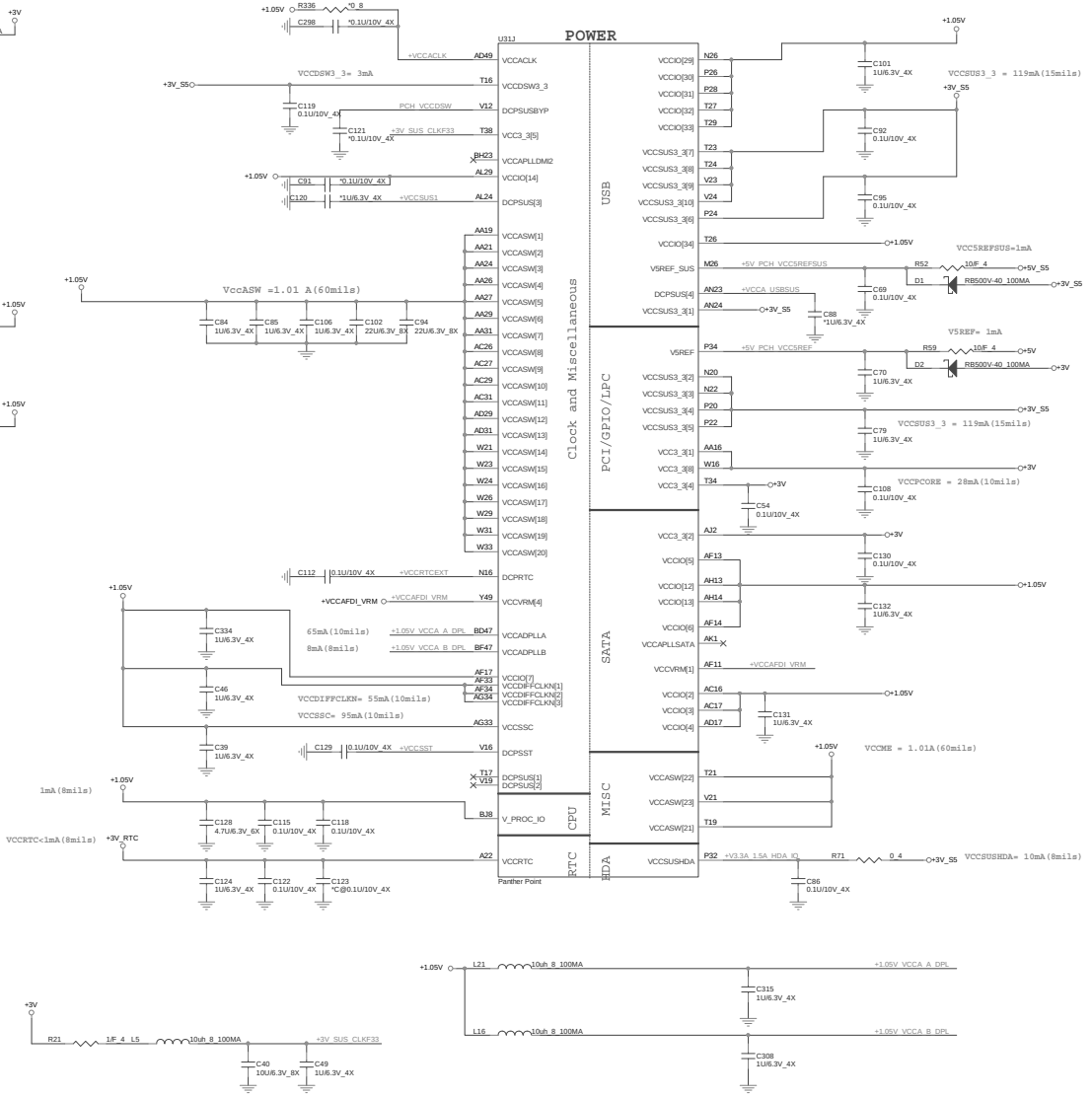
PROJECT : BY2D

Size	Document Number	Rev
	Panther/Cougar Point 4/6	3B
Date: Monday, March 26, 2012	Sheet 10 of 42	

Panther/COUGAR POINT (POWER)

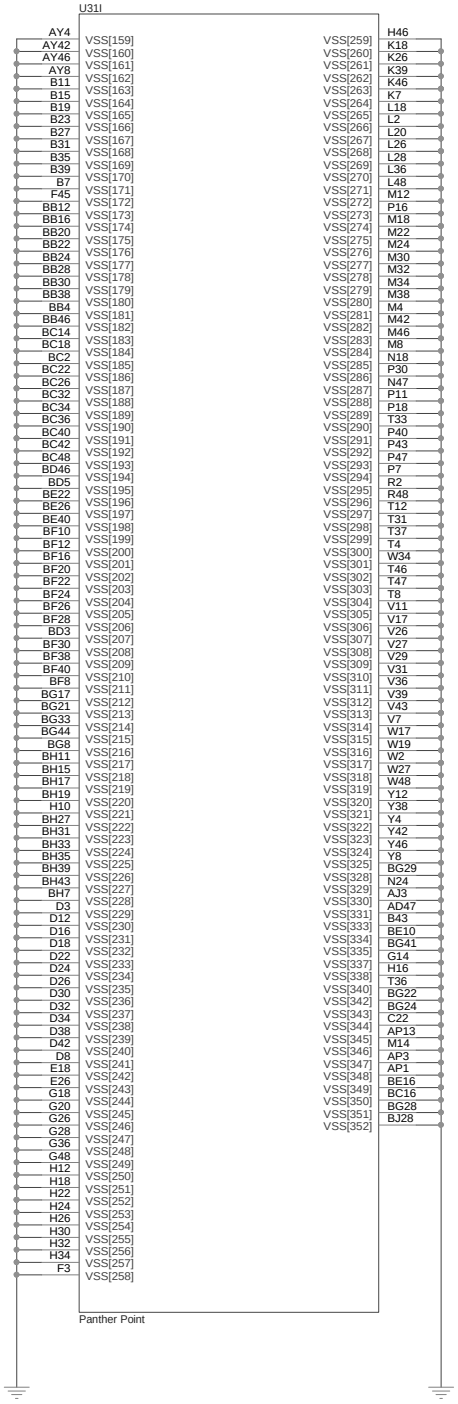


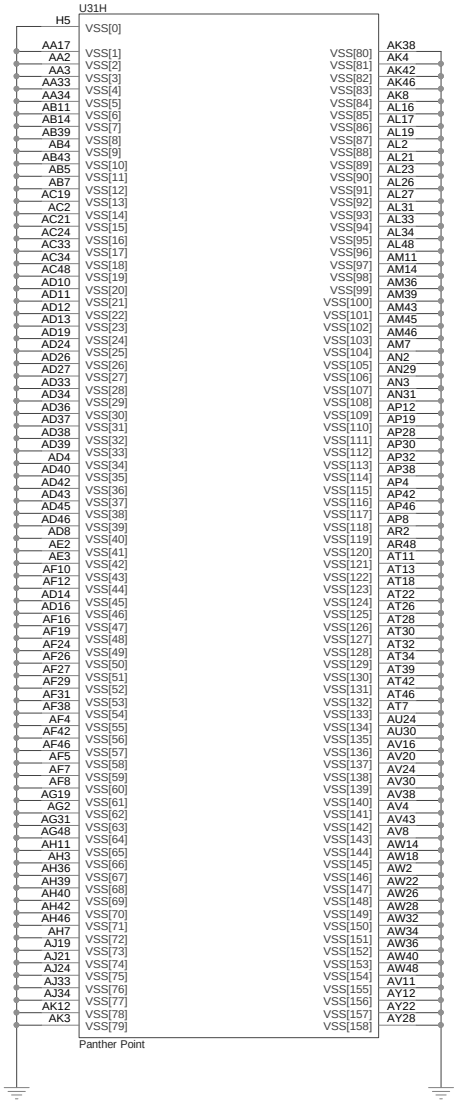
Panther/Cougar Point-M (POWER)



Quanta Computer Inc.			
PROJECT : BY2D			
Size	Document Number		Rev
	Panther/Cougar Point 5/6		3B
Date: Monday, March 26, 2012	Sheet 11	of	42

Panther/Cougar Point -M (GND)

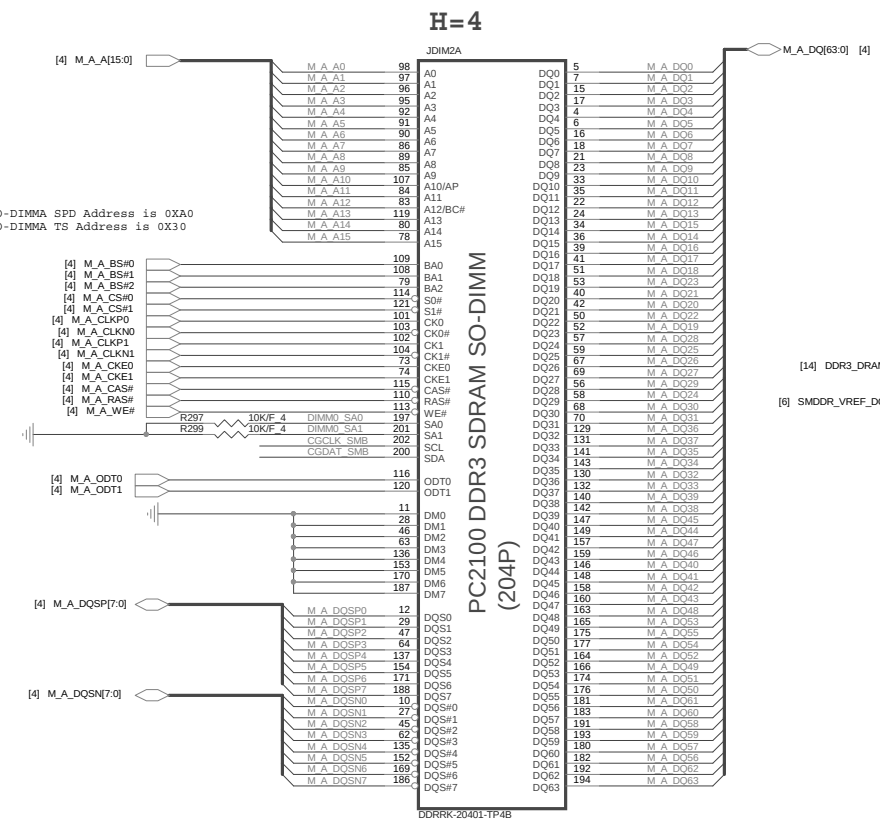


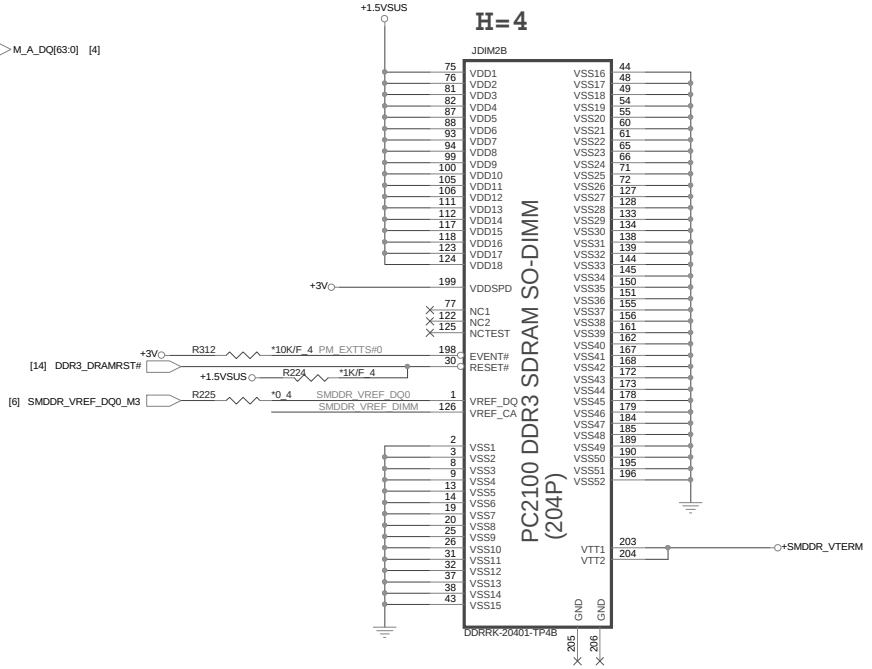


Quanta Computer Inc.

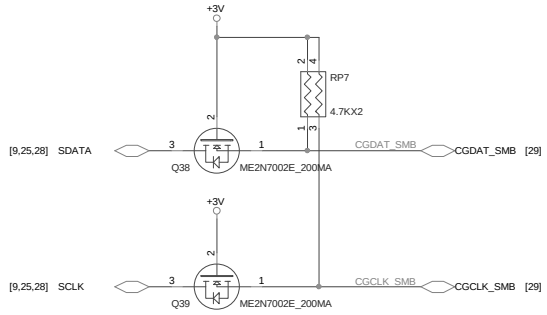
PROJECT :BY2D

Size	Document Number	Rev
	Panther/Cougar Point 6/6	3B
Date: Monday, March 26, 2012	Sheet 12 of 42	

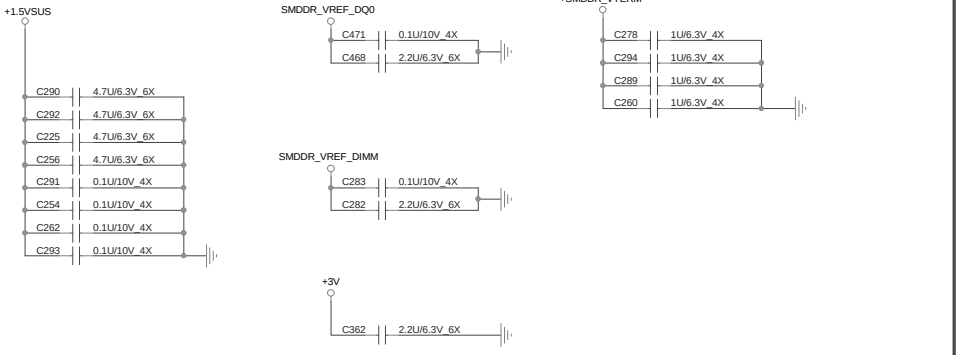


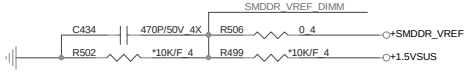


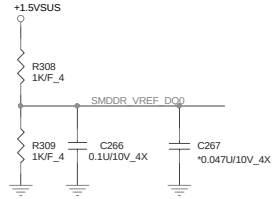
SMBus(DDR3/WLAN/LAN)



Place these Caps near Memory Down-1

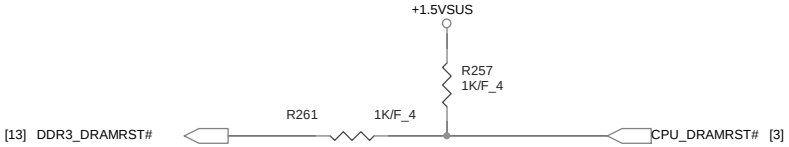




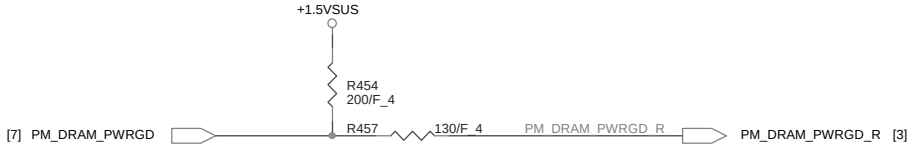


Quanta Computer Inc.		
PROJECT : BY2D		
Size	Document Number	Rev
	DDR3 DIMM-0	3B
Date: Monday, March 26, 2012	Sheet 13 of 42	

S3 power Reduction (SM_DRAMRST#) <S3P> <4>

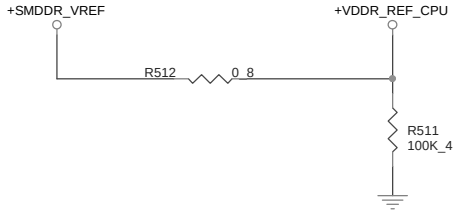


S3 power Reduction (SM_DRAMPWROK) <S3P> <3>



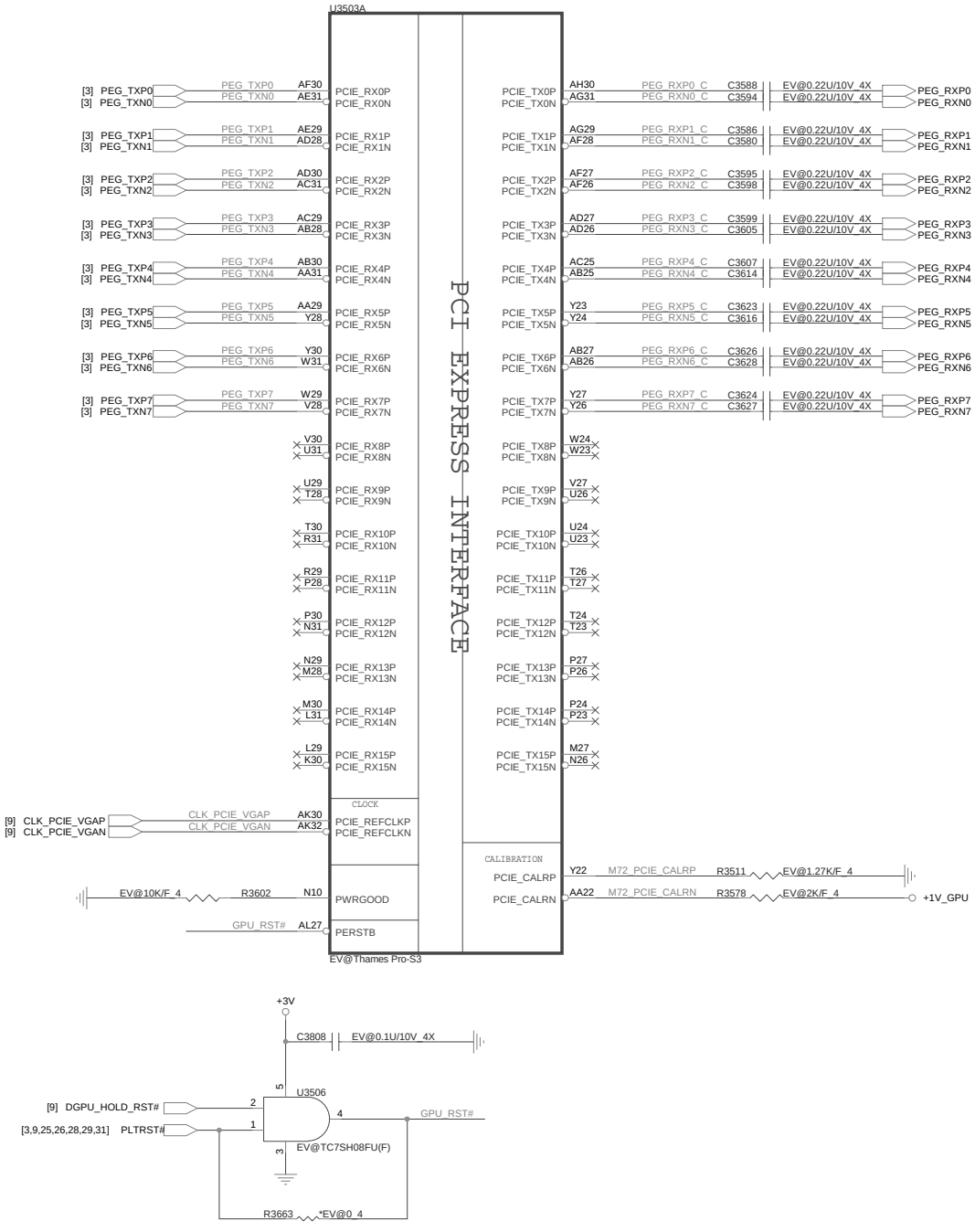
For S3 power Reduction Sequence <S3P> <3>

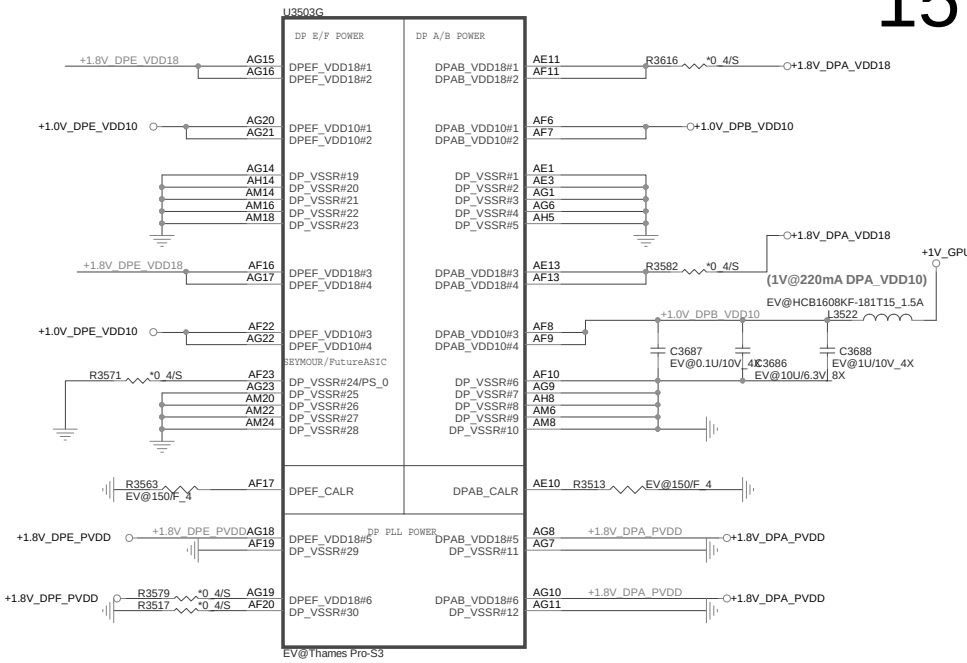
S3 power Reduction (CPU Power) <S3P> <5>

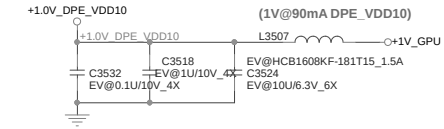


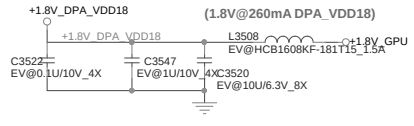
For S3 power Reduction VTT discharge <S3P> <13>

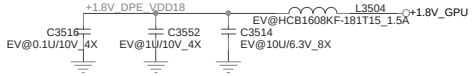
Quanta Computer Inc.		
PROJECT : BY2D		
Size	Document Number: S3 power Reduction	Rev: 3B
Date: Monday, March 26, 2012	Sheet 14 of 42	

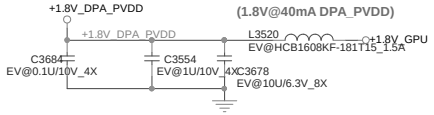


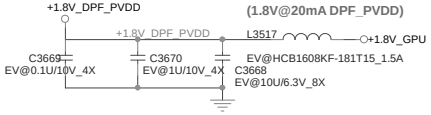


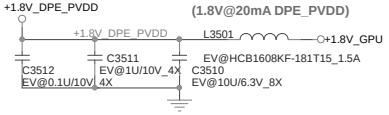










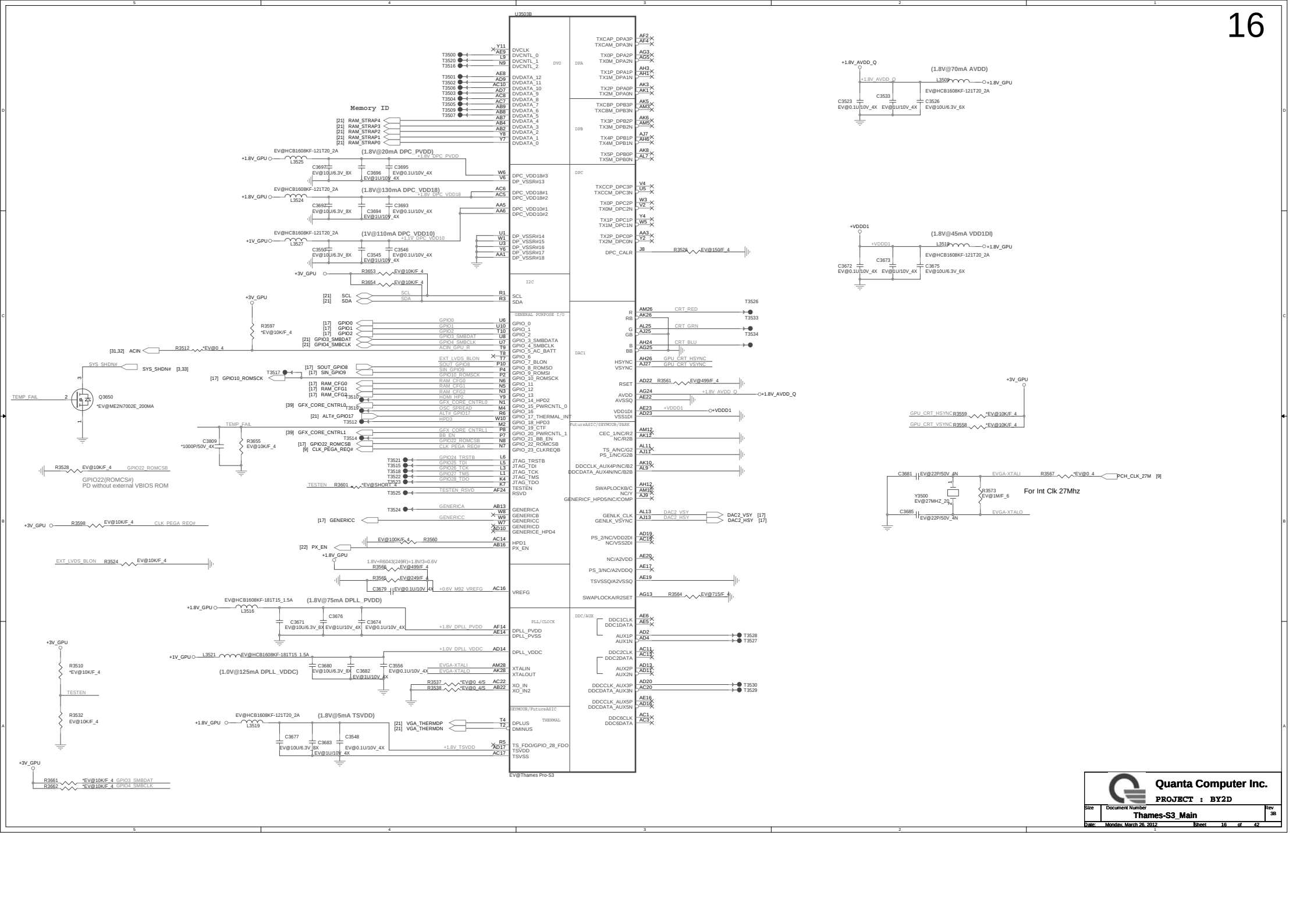


Quanta Computer Inc.

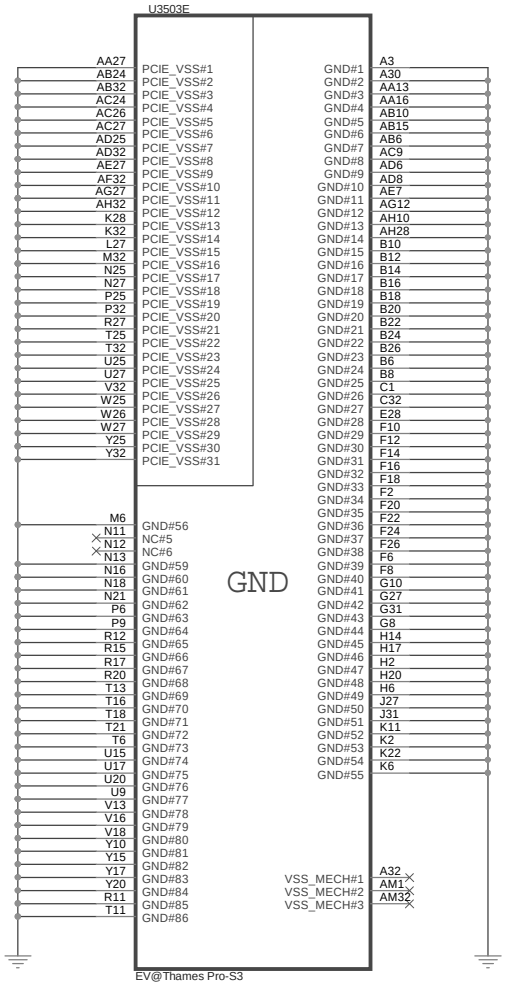
PROJECT : BY2D

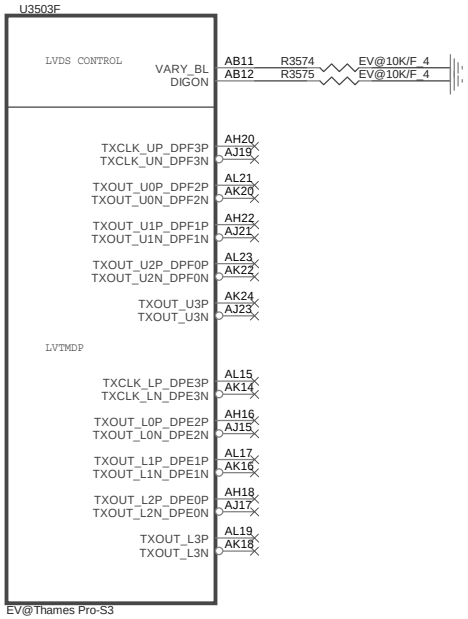
Size	Document Number	Rev
	Thames-S3_PCIE_Interface	3B

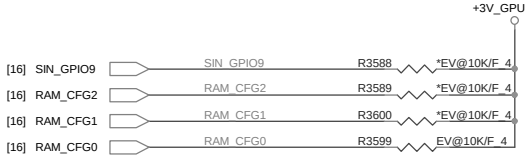
Date: Monday, March 26, 2012 Sheet 15 of 42



Quanta Computer Inc.
PROJECT : BY2D
Size
Document Number
Thames-S3_Main
Rev
3B
Date: Monday, March 26, 2012
Sheet 16 of 42







CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	**Transmitter Power Savings Enable** 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	**PCI Express Transmitter De-emphasis Enable** 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	0
BIF_GEN2_EN_A	GPIO2	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	1
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

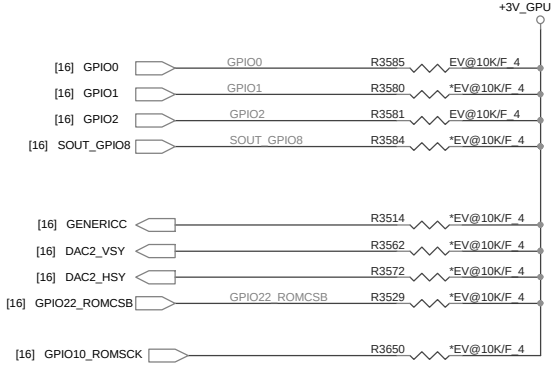
H2SYNC GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO21_BB_EN

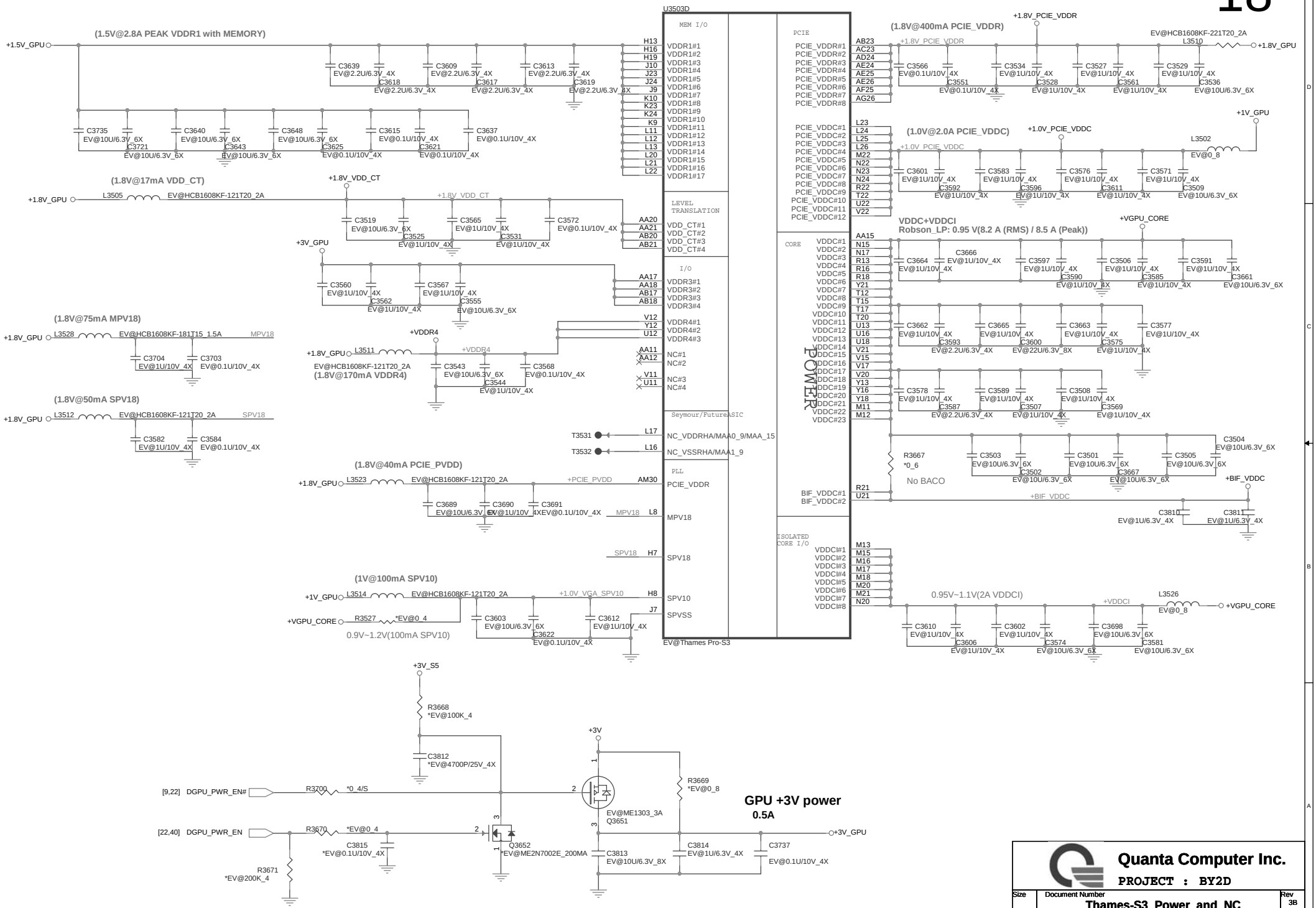
Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

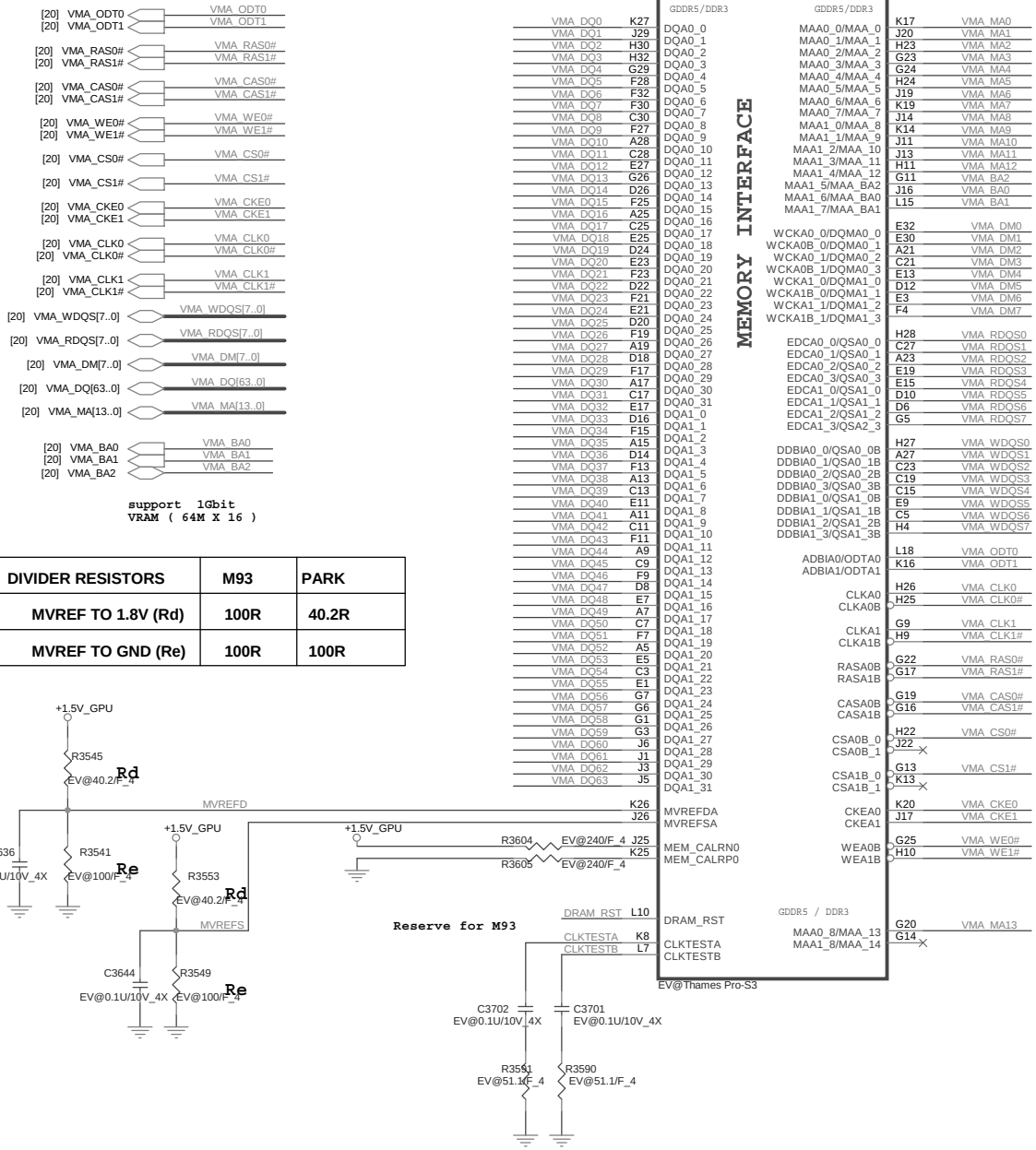


Quanta Computer Inc.
PROJECT : BY2D

Size	Document Number	Rev
	Thames-S3_GND/LVDS/Straps	3B
Date: Monday, March 26, 2012	Sheet 17 of 42	

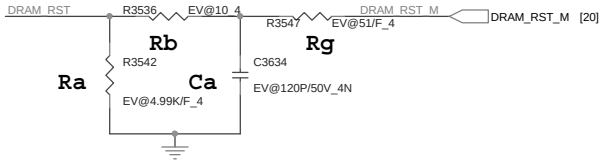


Quanta Computer Inc.			
PROJECT : BY2D			
Size	Document Number: Thames-S3_Power_and_NC		Rev: 3B
Date: Monday, March 26, 2012		Sheet 18 of 42	



DIVIDER RESISTORS	M93	PARK
MVREF TO 1.8V (Rd)	100R	40.2R
MVREF TO GND (Re)	100R	100R

Designator	Robson
Ra	5K
Rb	10R
Ca	120pF
Rg	51R



Quanta Computer Inc.

PROJECT : BY2D

Size	Document Number	Rev
	Thames-S3 MEM_Interface	3B
Date: Monday, March 26, 2012	Sheet 19 of 42	

512MB DDR3

[19] VMA_MA[13..0]
[19] VMA_DM[7..0]
VMA_MA[13..0]
[19] VMA_DQ[63..0]
[19] VMA_WDQS[7..0]
[19] VMA_RDQS[7..0]

U3501 / U3504 / U3500 / U3505 — 100-BALL SDRAM DDR3 — EV@H5TQ2G63BFR-11C

Should be 240 Ohms +-1%

R3552 EV@243/F_4
R3609 EV@243/F_4
R3546 EV@243/F_4
R3606 EV@243/F_4

+1.5V_GPU

R3613 EV@4.99K/F_4 — VREFC_VMA1
R3533 EV@4.99K/F_4 — VREFD_VMA1
R3612 EV@4.99K/F_4 — C3723 EV@0.1U/10V_4X
R3535 EV@4.99K/F_4 — C3638 EV@0.1U/10V_4X

R3611 EV@4.99K/F_4 — VREFC_VMA2
R3534 EV@4.99K/F_4 — VREFD_VMA2
R3614 EV@4.99K/F_4 — C3729 EV@0.1U/10V_4X
R3539 EV@4.99K/F_4 — C3715 EV@0.1U/10V_4X

R3556 EV@4.99K/F_4 — VREFC_VMA3
R3550 EV@4.99K/F_4 — VREFD_VMA3
R3555 EV@4.99K/F_4 — C3649 EV@0.1U/10V_4X
R3554 EV@4.99K/F_4 — C3645 EV@0.1U/10V_4X

R3608 EV@4.99K/F_4 — VREFC_VMA4
R3603 EV@4.99K/F_4 — VREFD_VMA4
R3610 EV@4.99K/F_4 — C3719 EV@0.1U/10V_4X
R3607 EV@4.99K/F_4 — C3714 EV@0.1U/10V_4X

VMA_CLK0
R3543 EV@56/F_4
VMA_CLK0_COMM — C3642 EV@0.01U/25V_4X
R3548 EV@56/F_4
VMA_CLK0#
VMA_CLK1
R3540 EV@56/F_4
VMA_CLK1_COMM — C3635 EV@0.01U/25V_4X
R3544 EV@56/F_4
VMA_CLK1#

+1.5V_GPU
C3632 C3655 C3641 C3630 C3633 C3646 C3631 C3732 EV@1U/6.3V_4X
C3709 C3707 C3730 C3629 C3733 C3724 C3706 C3705 EV@1U/6.3V_4X
C3736 C3726 C3652 C3727 C3734 C3650 C3654 C3731 EV@1U/6.3V_4X
C3712 C3708 C3718 C3647 C3717 C3720 C3651 C3710 EV@1U/6.3V_4X
C3728 C3658 C3657 C3711 C3660 EV@10U/6.3V_6X
C3713 C3725 C3656 C3653 C3722 C3716 C3659 EV@10U/6.3V_6X

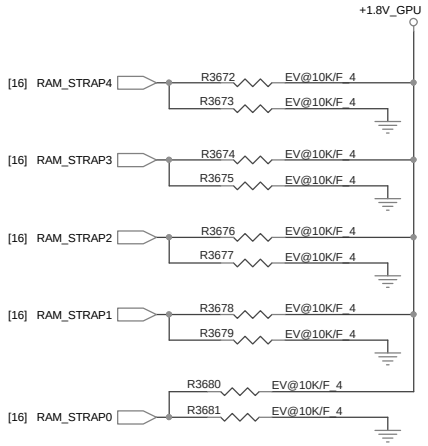
	QCI PN
SAMSUNG	AKD5MGWT500
HYNIX	AKD5MGWTW00

Quanta Computer Inc.
PROJECT : BY2D

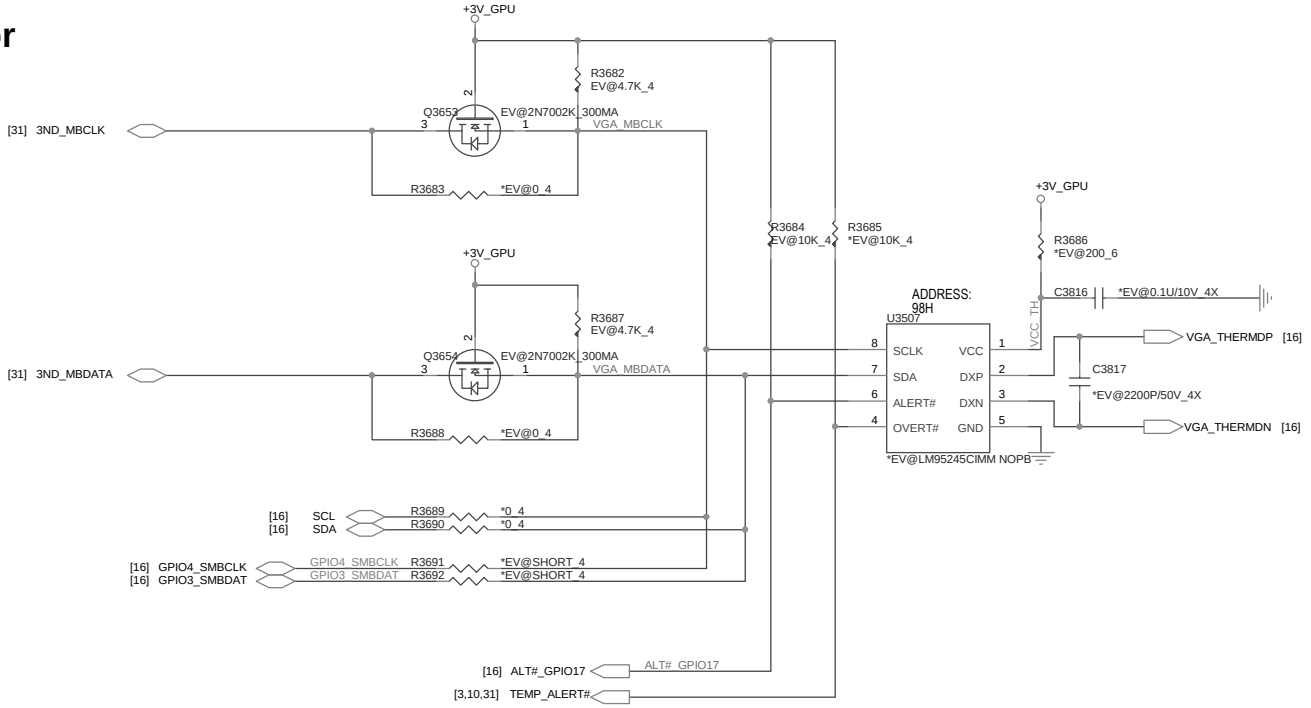
Size	Document Number	Rev
	Thames-S3 VRAM DDR3 BGA96	3B
Date: Monday, March 26, 2012	Sheet 20 of 42	

VRAM Memory TYPE

Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP4 DVPDATA_4	RAM_STRAP3 DVPDATA_3	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
AMD	23EY2387MC11	AKD5EZWT700 *4 (64M*16-1Gb)	512MB	0	0	0	1	0
	23EY4187MA11	AKD5DZWT700 *4 (128M*16-2Gb)	1GB	0	1	0	1	0
Samsung	K4W1G1646G-BC11	AKD5EGGT500 *4 (64M*16-1Gb)	512MB	0	0	0	0	1
	K4W2G1646C-HC11	AKD5MGWT500 *4 (128M*16-2Gb)	1GB	0	1	0	0	1
Hynix	H5TQ1G63DFR-11C	AKD5LZWTW02 *4 (64M*16-1Gb)	512MB	0	0	0	0	0
	H5TQ2G63BFR-11C	AKD5MGWTW00 *4 (128M*16-2Gb)	1GB	0	1	0	0	0



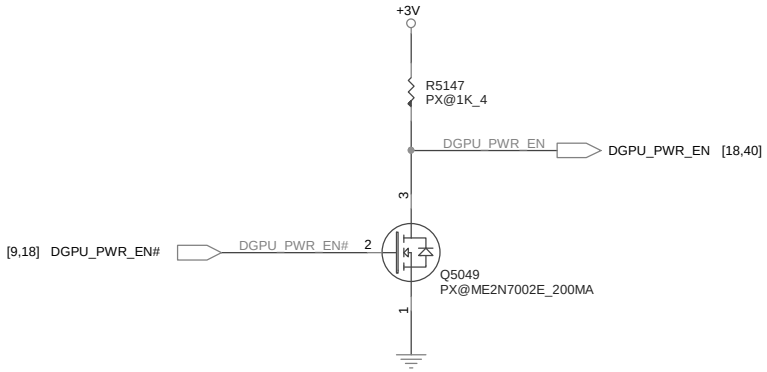
Thermal Sensor



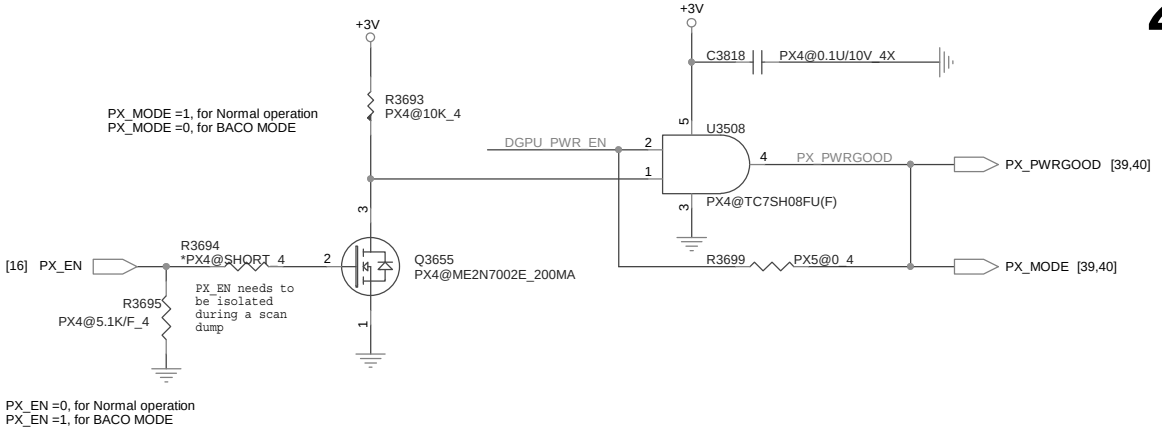
Quanta Computer Inc.
PROJECT : BY2D

Size	Document Number	Rev
	Thames-S3 Strip/Thermal	3B
Date: Monday, March 26, 2012	Sheet 21 of 42	

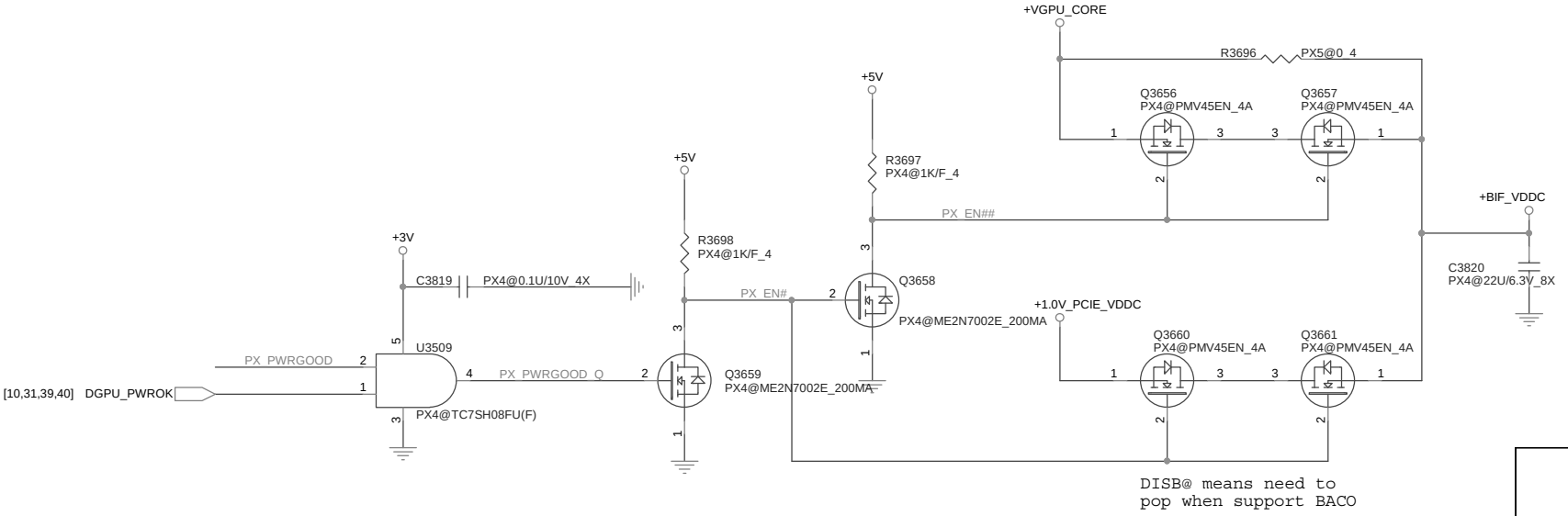
<SWA> VGA Power Enable Reverse (Intel --> Low Active)



PX Mode control signal

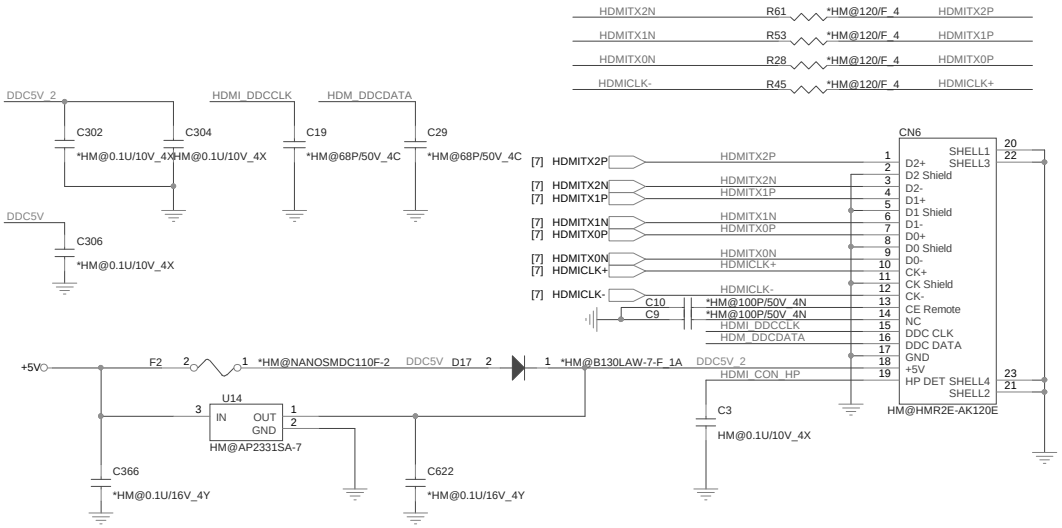


PX Mode Core power for PCIE Logic

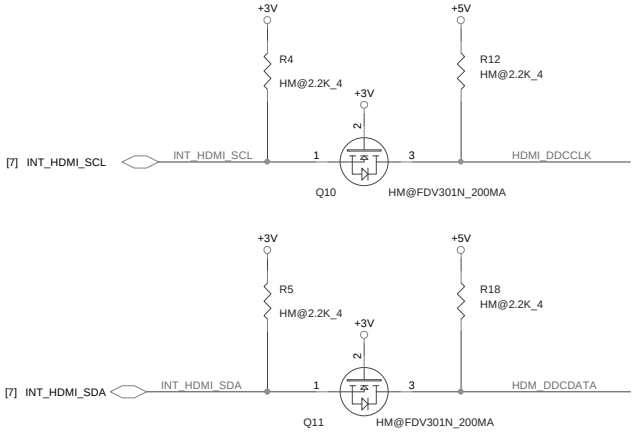


Quanta Computer Inc. PROJECT : BY2D		
Size	Document Number: Thames-S3 RS/SM-S3_Baco	Rev: 3B
Date: Monday, March 26, 2012	Sheet 22 of 42	

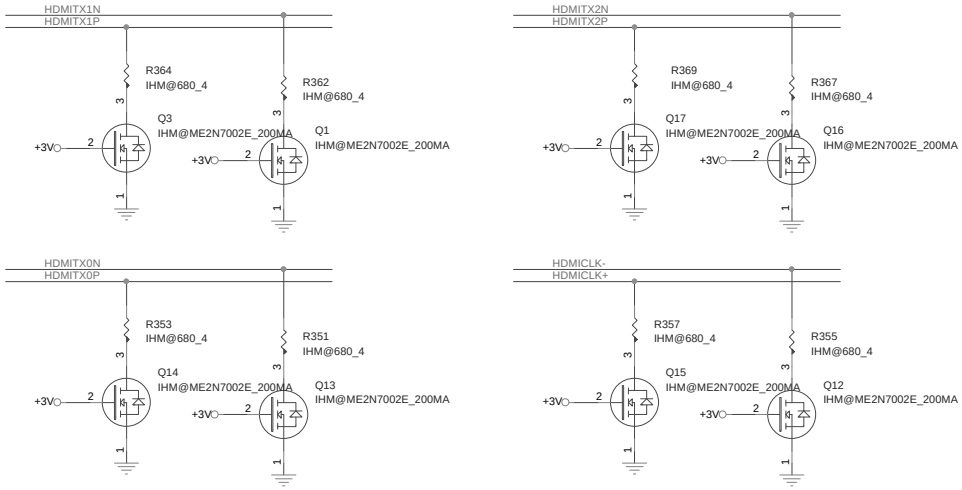
HDMI Conn <HDM>



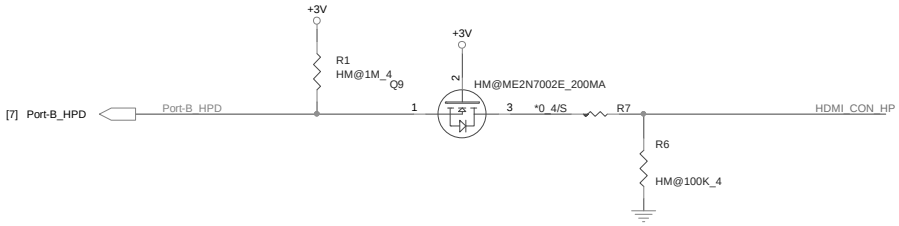
HDMI-SMBus <HDM>



HDMI-passive level shift <HDM>



HDMI-HPD <HDM>



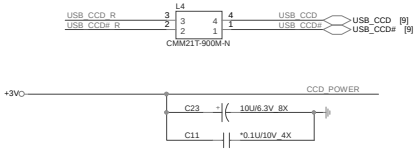
Quanta Computer Inc.

PROJECT : BY2D

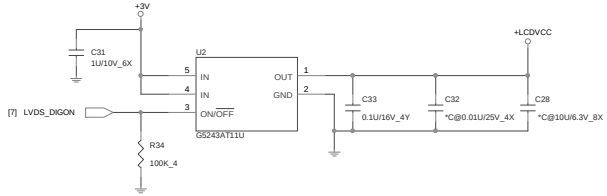
Size	Document Number	Rev
	HDMI CONN	3B

Date: Monday, March 26, 2012 Sheet 23 of 42

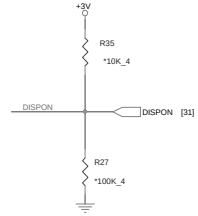
CCD <CCD>



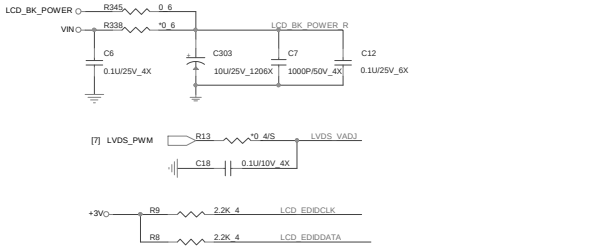
LCD POWER SWITCH <LDS>

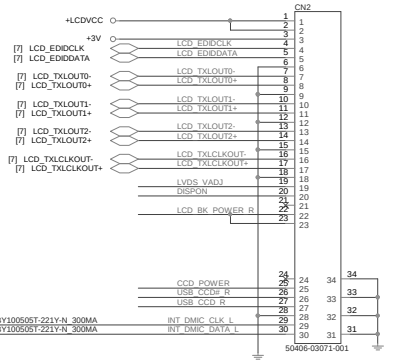


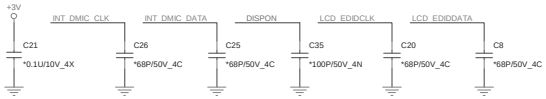
HALL SENSOR&BACK LIGHT SWITCH <HSR>



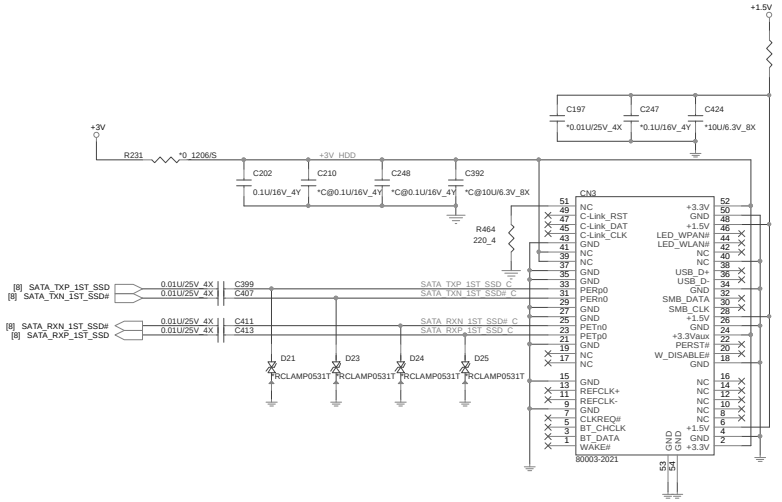
LCD Panel Module <LDS>







mSATA (SATA over mini PCIe) <H1D>



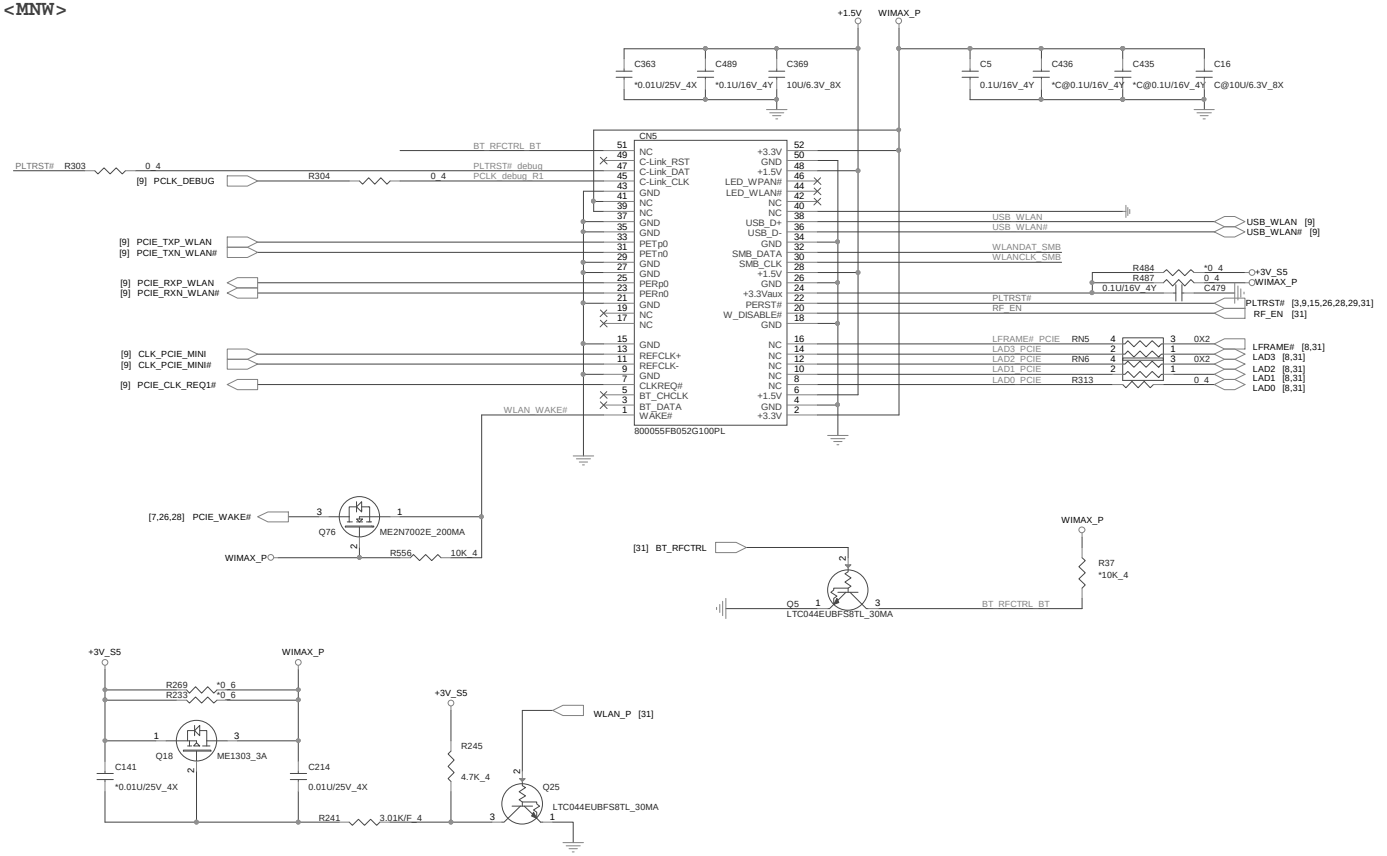
Quanta Computer Inc.

PROJECT : BY2D

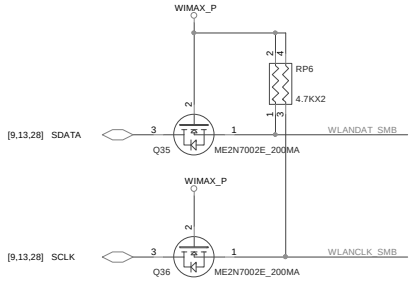
Size	Document Number	Rev
	LCD/CCD/mSATA	3B

Date: Monday, March 26, 2012 Sheet 24 of 42

MINI Card Slot#1 <MNW>
(WiFi)



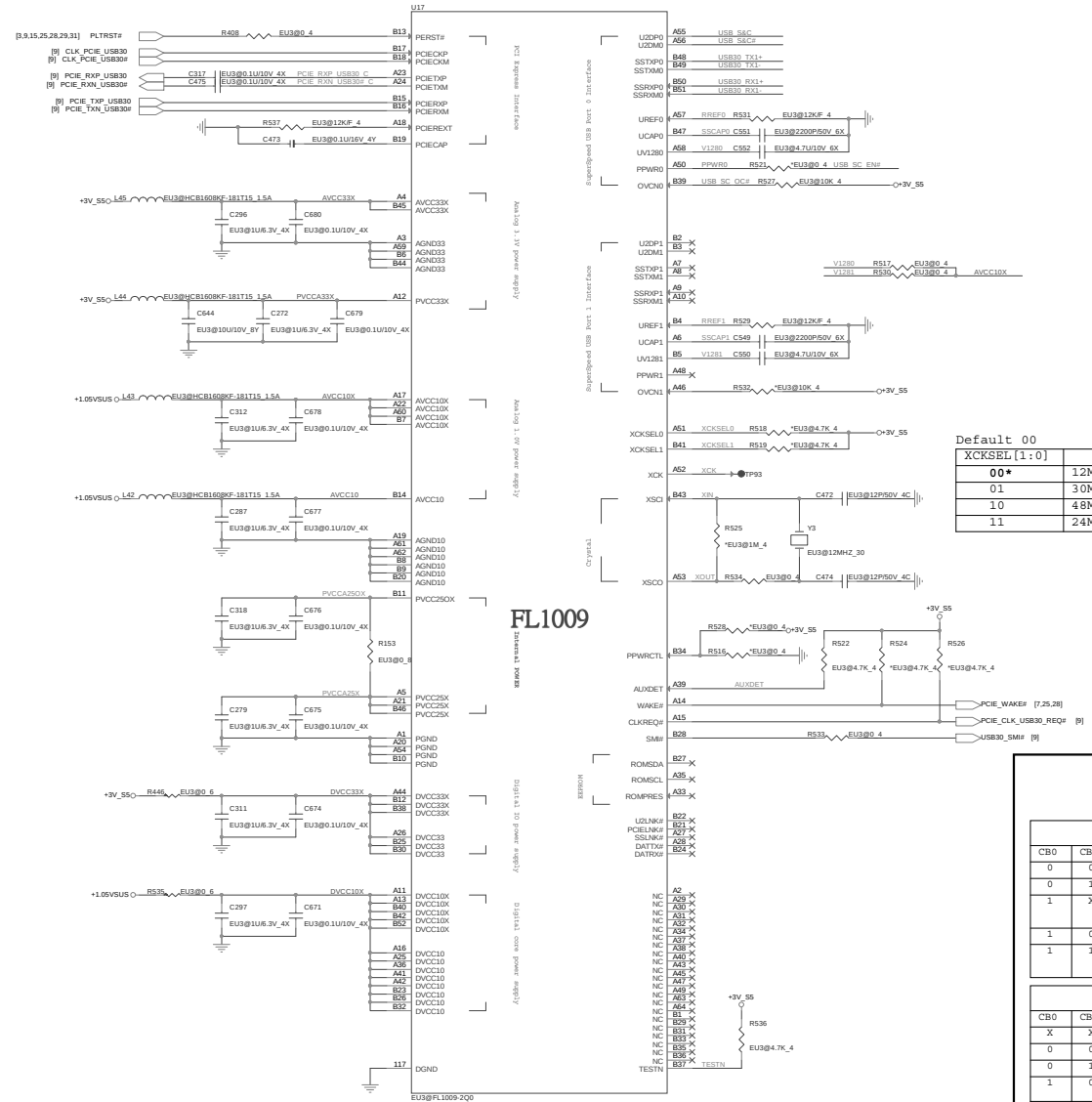
SMBus(DDR3/WLAN/3G)



Quanta Computer Inc.
PROJECT : BY2D

Size	Document Number	Rev
	MINI CARD(WLAN/3G/SIM Card)	3B

Date: Monday, March 26, 2012 Sheet 25 of 42



AVCC33X		
Min	Typ	Max
3.15V	3.30V	3.45V
Current = 93mA		

PVCCA33X		
Min	Typ	Max
3.15V	3.30V	3.45V
Current = 75mA		

AVCC10X		
Min	Typ	Max
1.00V	1.05V	1.05V
Current = 82mA		

AVCC10		
Min	Typ	Max
1.00V	1.05V	1.05V
Current = 36mA		

DVCC33X		
Min	Typ	Max
2.97V	3.30V	3.63V
Current = 0mA		

DVCC33		
Min	Typ	Max
2.97V	3.30V	3.63V
Current = 6mA		

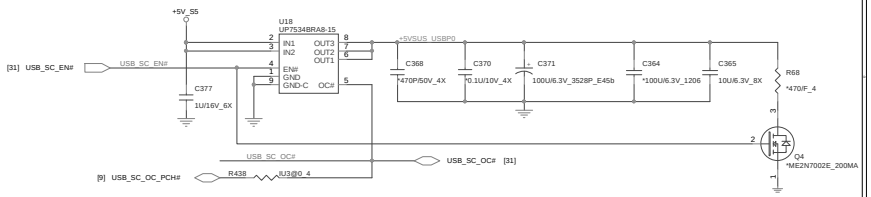
DVCC10X		
Min	Typ	Max
1.00V	1.05V	1.10V
Current = 23mA		

DVCC10		
Min	Typ	Max
1.00V	1.05V	1.10V
Current = 71mA		

Default 00

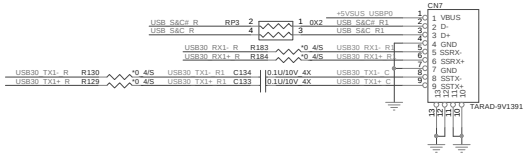
XCKSEL[1:0]	
00*	12MHz crystal oscillator to XSCI/XSCO
01	30MHz crystal oscillator to XSCI/XSCO
10	48MHz reference clock to XCK pin
11	24MHz reference clock to XCK pin

USB 3.0 Power switch <U2B> <USB> <U3B>



<EMI> <U3B> <USB>

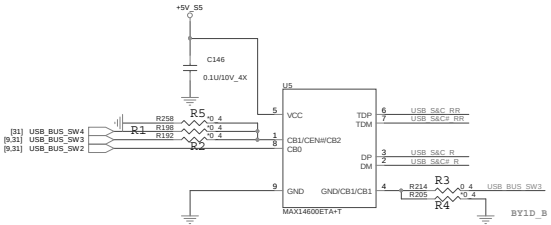
USB 3.0 CONN



USB 3.0 Colay for Chief River and Huron_River

USB 2.0 Colay <U3B> <U2B>

USB w S&C MAXIM solution <SLC>



14566/14600		
CB0	CB1	Status
0	0	Auto mode
0	1	Force dedicated charger mode
1	X	Pass-Through(USB) mode: Connect DP/DM to TDP/TDM for 14566
1	0	Pass-Through(USB) mode for 14600
1	1	pass-through(USB) with CDP Emulation for 14600

14617			
CB0	CB1	CB2	Status
X	X	1	Force Apple 2A Charger Mode
0	0	0	Autodetection charger mode
0	1	0	Force-Dedicated Charger Mode
1	0	0	USB Pass-Through Mode(USB) Connect DP/DM to TDP/TDM
1	1	0	USB Pass-Through Mode with CDP Emulation.Auto connect DP/DM to TDP/TDM depending on CDP status

14566/14600/14617

	R1	R2	R3	R4	R5
14566		V		V	
14600			V		
14617(with CB2)	V		V		
14617(no CB2)			V		V

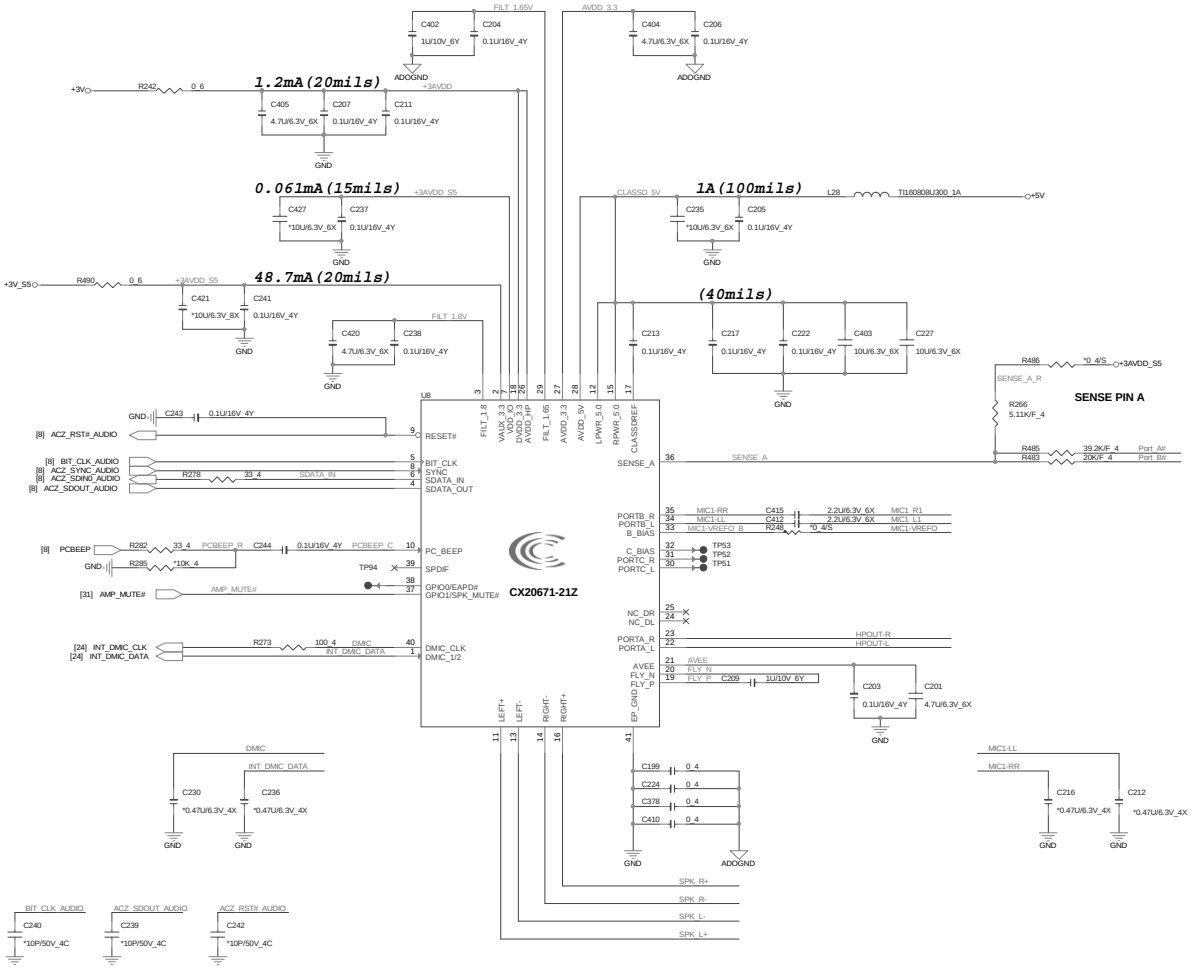
Quanta Computer Inc.

PROJECT : BY2D

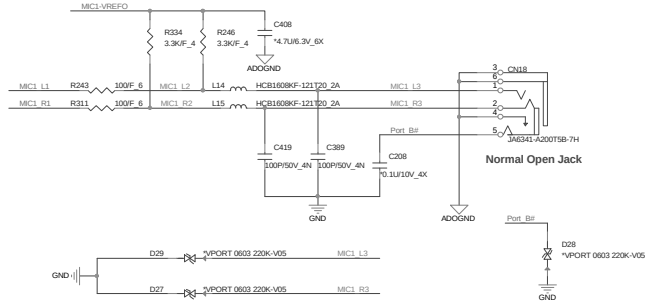
Size	Document Number	Rev
	USB 3.0(UPD720200F1-A)	3B

Date: Monday, March 26, 2012 Sheet 26 of 42

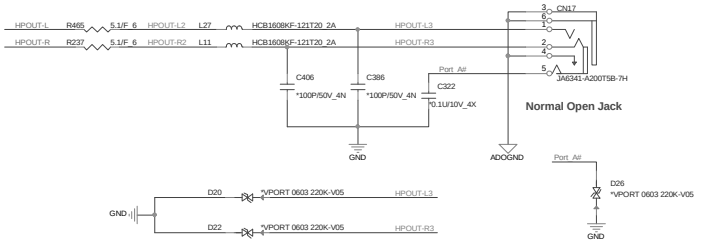
Codec (CX20671-21Z) <ADO> <EMI>



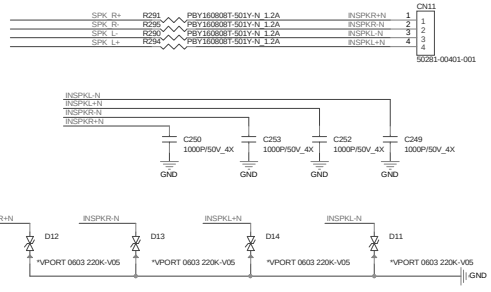
External MIC <ADO> <EMC>



HP <ADO> <EMC>

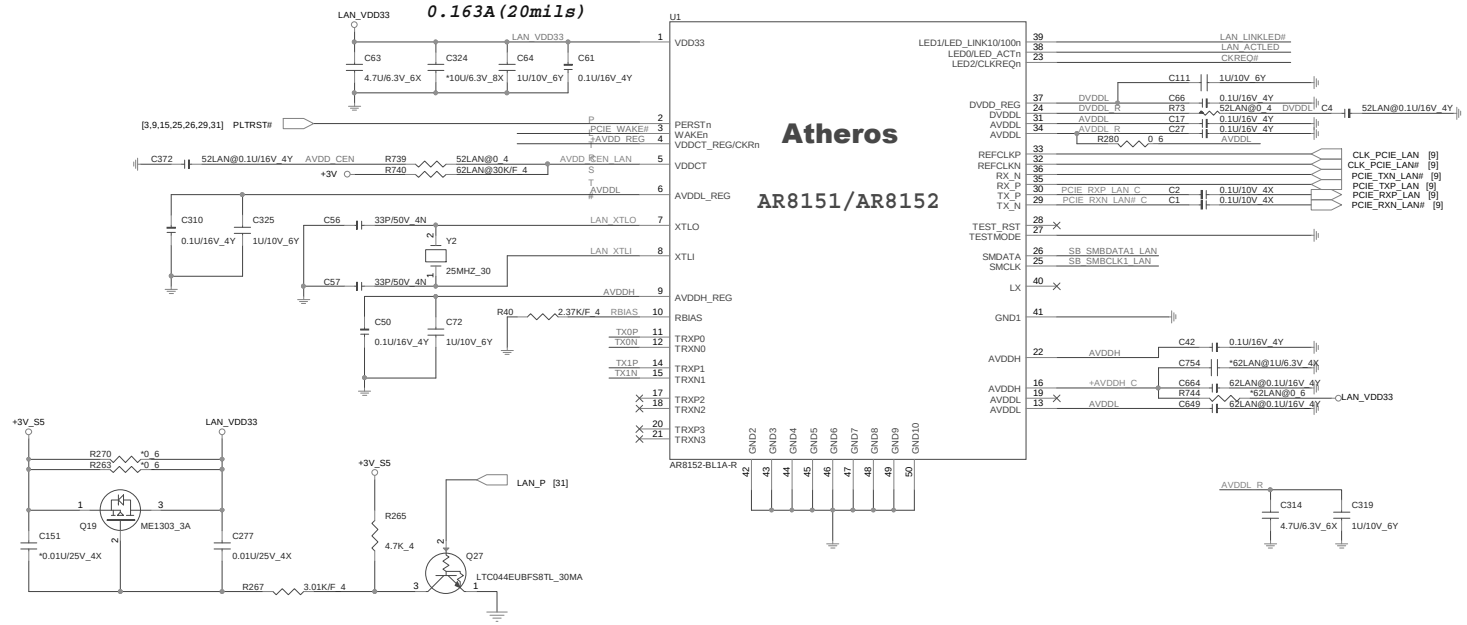


Internal Speaker <ADO> <EMC>

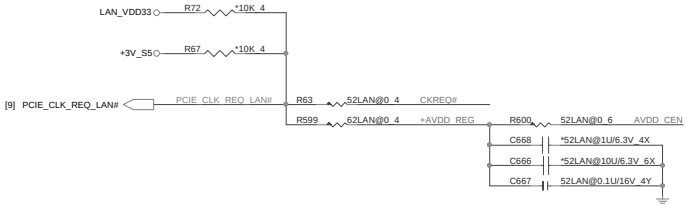


Quanta Computer Inc.			
PROJECT : BY2D			
Size	Document Number		Rev
	Audio Codec(CX20671-21Z)		3B
Date: Monday, March 26, 2012		Sheet 27 of 42	

Atheros Lan <LAN>

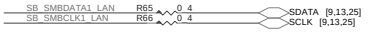


<LAN>



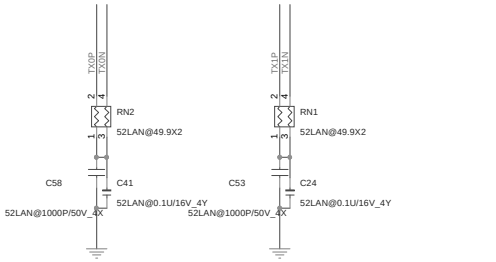
LAN-Wake up function <LAN>

LAN-SM-Bus <LAN>



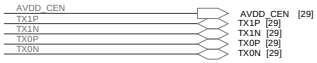
PLACE NEAR LAN IC SIDE

<LAN>

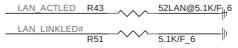


LAN SIGNALS TO CONNECTOR

<LAN>



RJ45<LAN>



LED0 = LAN_ACTLED	1	Over-clocking enable (default = 1)
	0	Over-clocking disable
LED1 = LAN_LINKLED#	1	SWR switch-mode regulator select Giga LAN pull High (default = 1)
	0	LDO linear regulator select 10/100M LAN pull Low
CKREQ# or CKREQ_G#	1	Normal function
	0	ATE test mode

Quanta Computer Inc.

PROJECT : BY2D

Size	Document Number	Rev
	Atheros LAN (AR8151B/52B)	3B

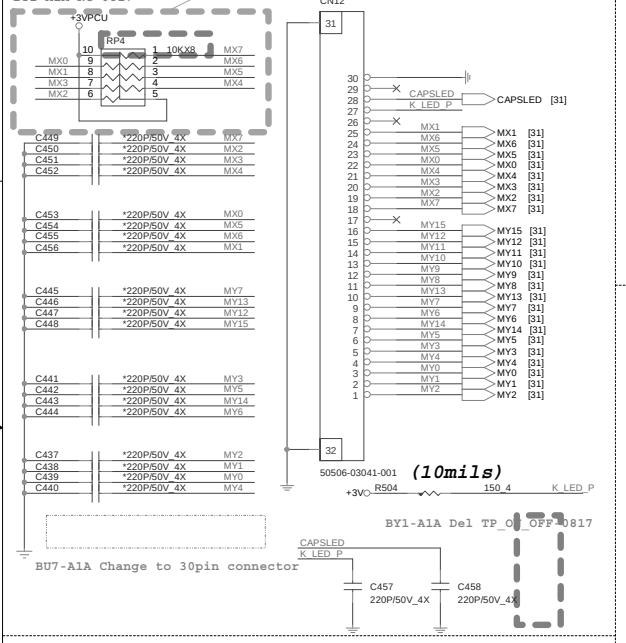
Date: Monday, March 26, 2012 Sheet 28 of 42

INT KeyBoard <KBC> <EMI>

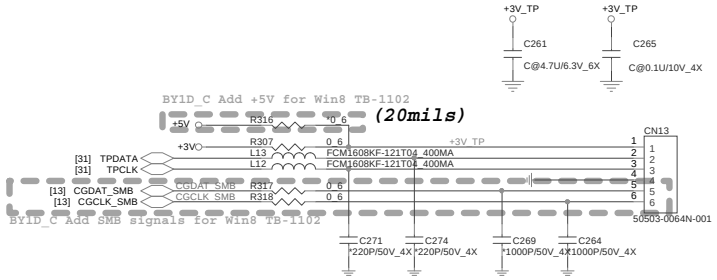
BY1D_C Add PU 10k for KB MX... -1102

BU7-A1A Change to 30pin connector

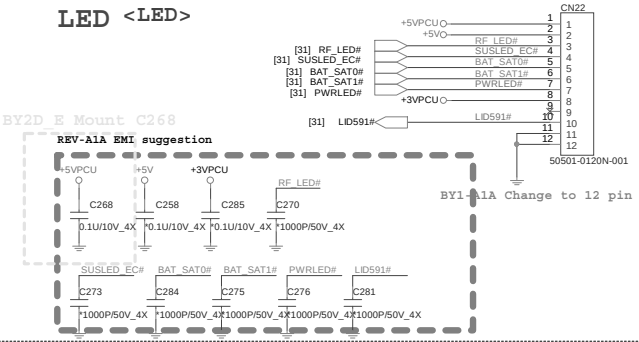
BY1-A1A NC-0817



TP board <TPD> <EMI>



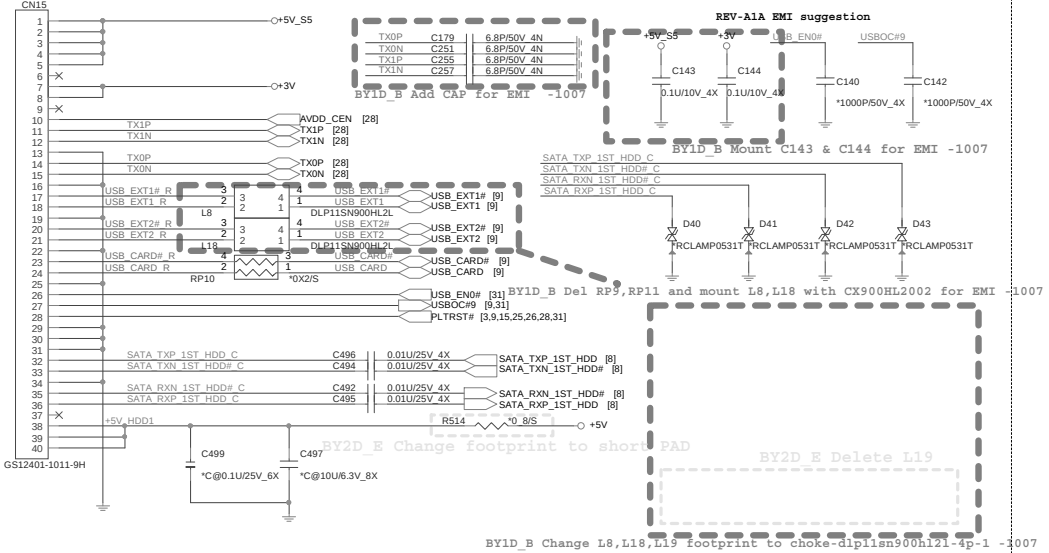
LED <LED>



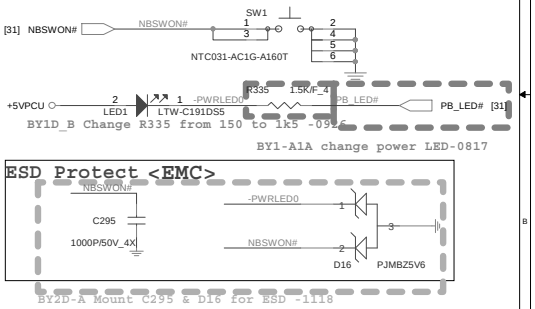
USB3.0 Left 1 & HDD Interface Card Reader Conn

<U3B> <MMC> <EMI> <H1D> <LAN>

BY1-A1A Del USB3.0 0728



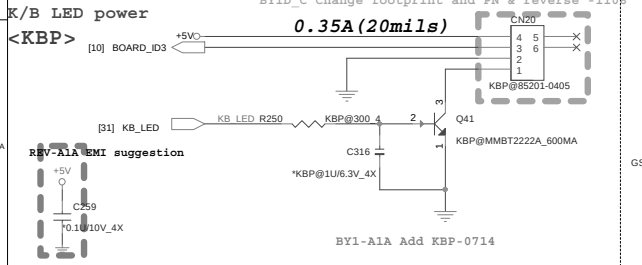
Power Button<PSW>



ESD Protect <EMC>

K/B LED power <KBP>

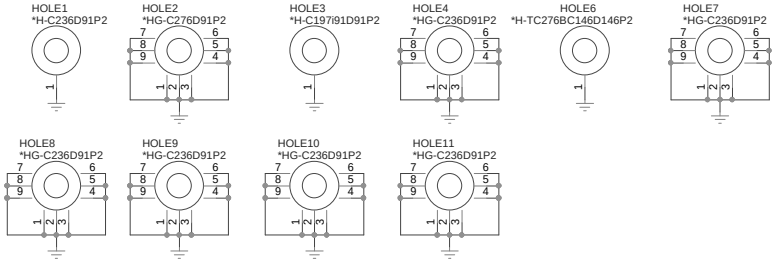
BY1D_C Change footprint and PN & reverse -1103

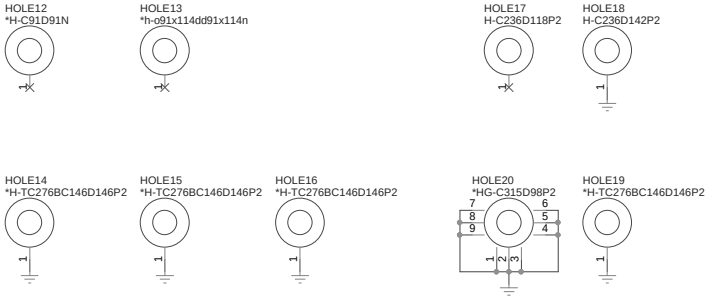


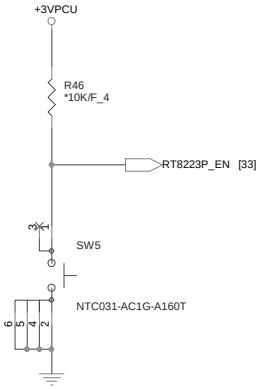
Quanta Computer Inc.
PROJECT : BY2D

Size	Document Number	Rev
	KB/TP&TP/PB/FL/LEB/MMB/B-CAS	3B
Date: Monday, March 26, 2012	Sheet 29 of 42	

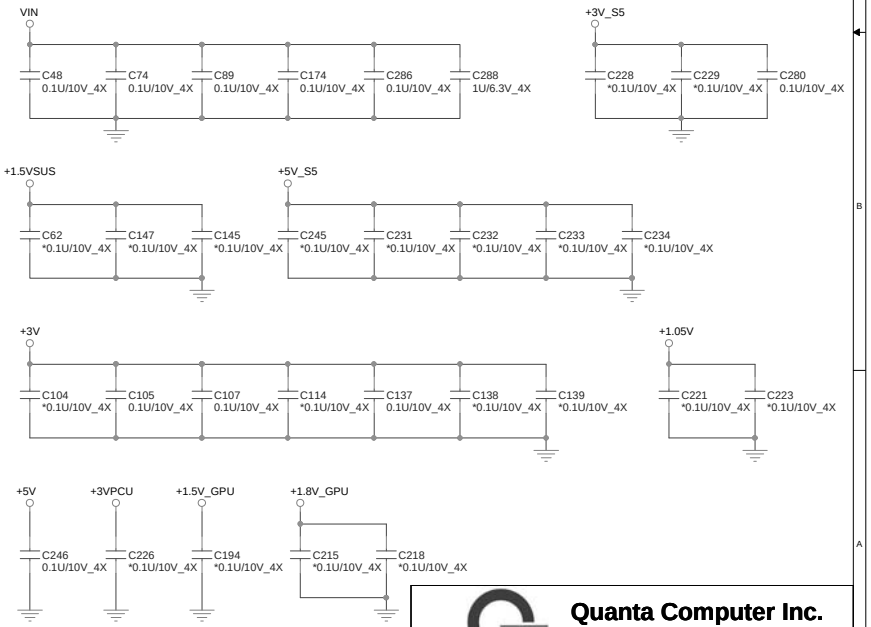
HOLE <OTH>







EMI <EMI>



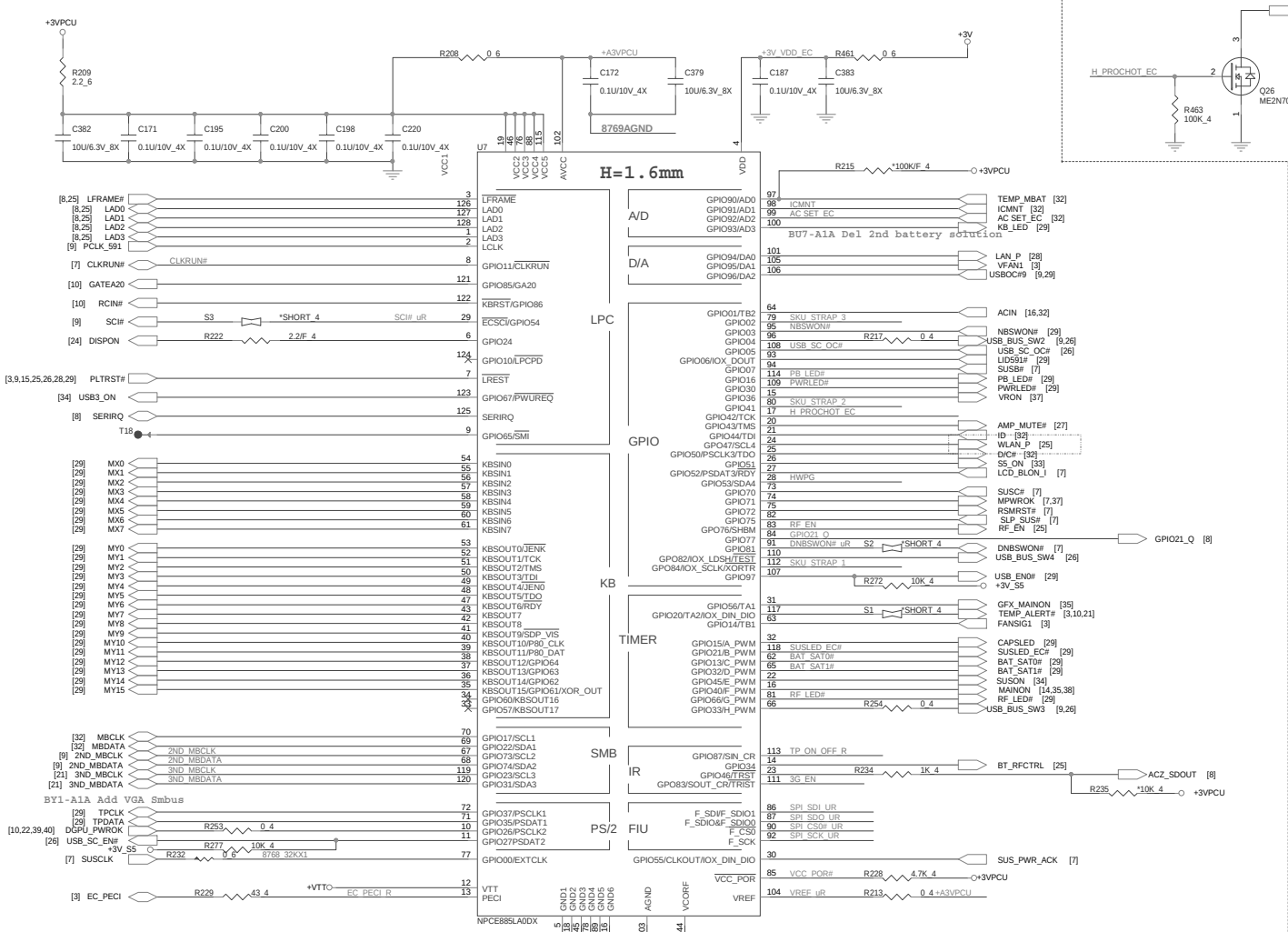
Quanta Computer Inc.

PROJECT : BY2D

Size	Document Number	Rev
	CUT BAT Control/HOLE/EMI	3B

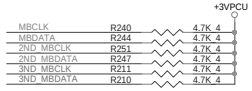
Date: Monday, March 26, 2012 Sheet 30 of 42

EC <KBC>



Intel Turbo mode only <CPU>

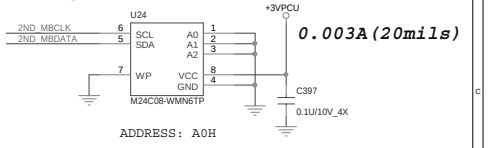
SM BUS PU/Address <KBC>



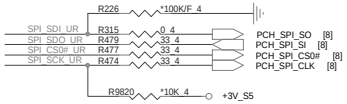
3Cell Battery protect & K/B LED Control<KBC>

Strap <KBC>

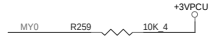
ID EEPROM <KBC>



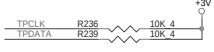
SPI FLASH <KBC>



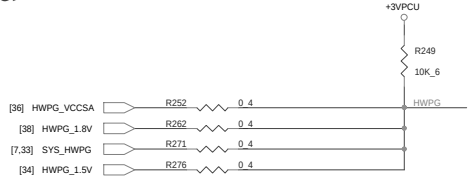
INTERNAL KEYBOARD STRIP SET <KBC>



TP interface PU <KBC>



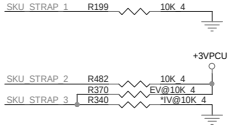
HWPG circuit <KBC>



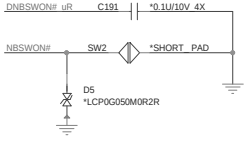
SMBUS Table

SMBUS	Devices	Address
1	Battery	12H
2	CPU Board Thermal Sensor	
	EC EEPROM	A0H
3	VGA Board Thermal Sensor	98H

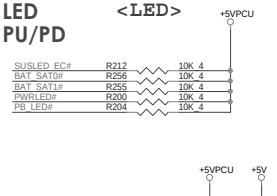
SKU strap pin <KBC>



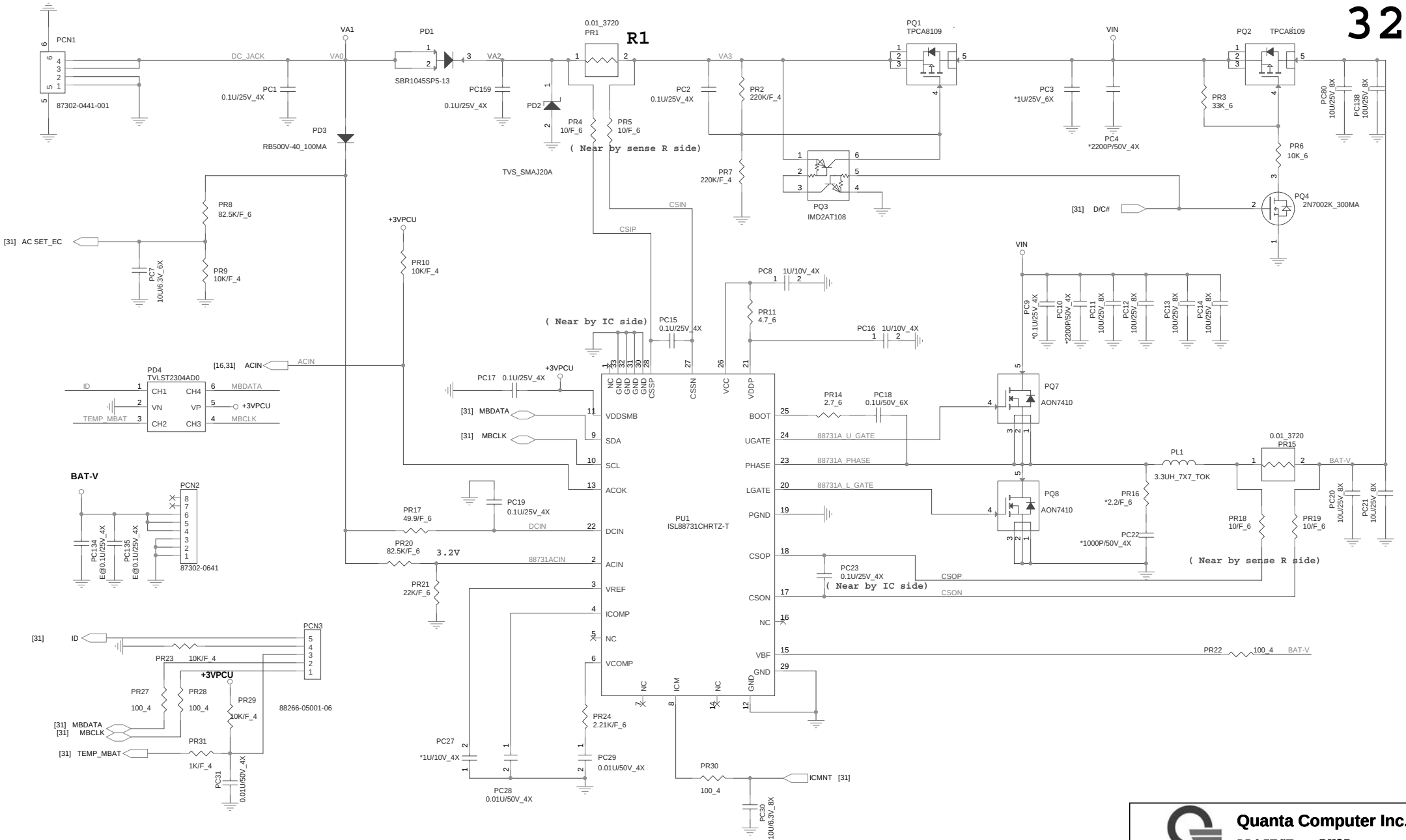
Power Button <KBC>



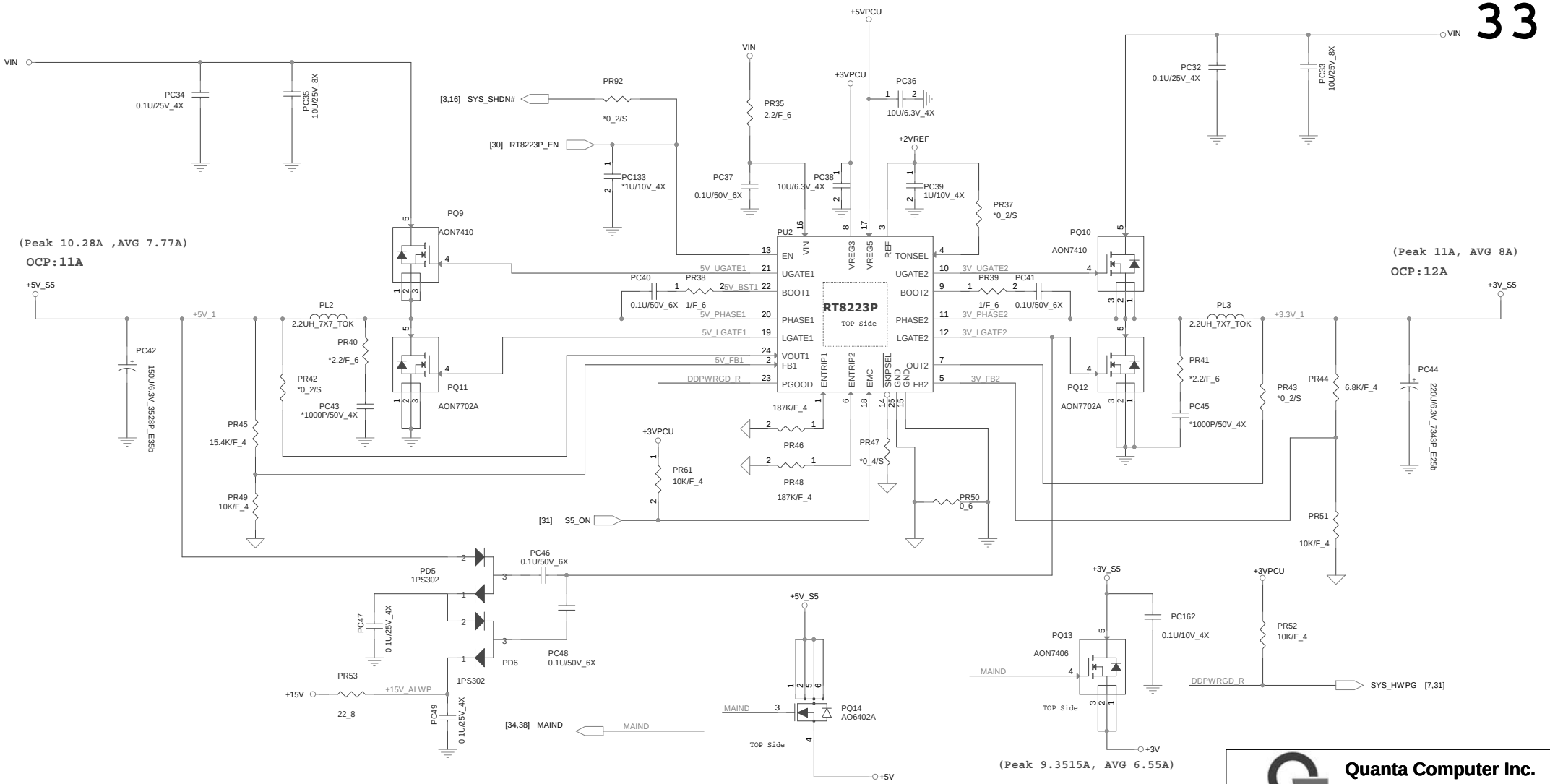
LED PU/PD <LED>



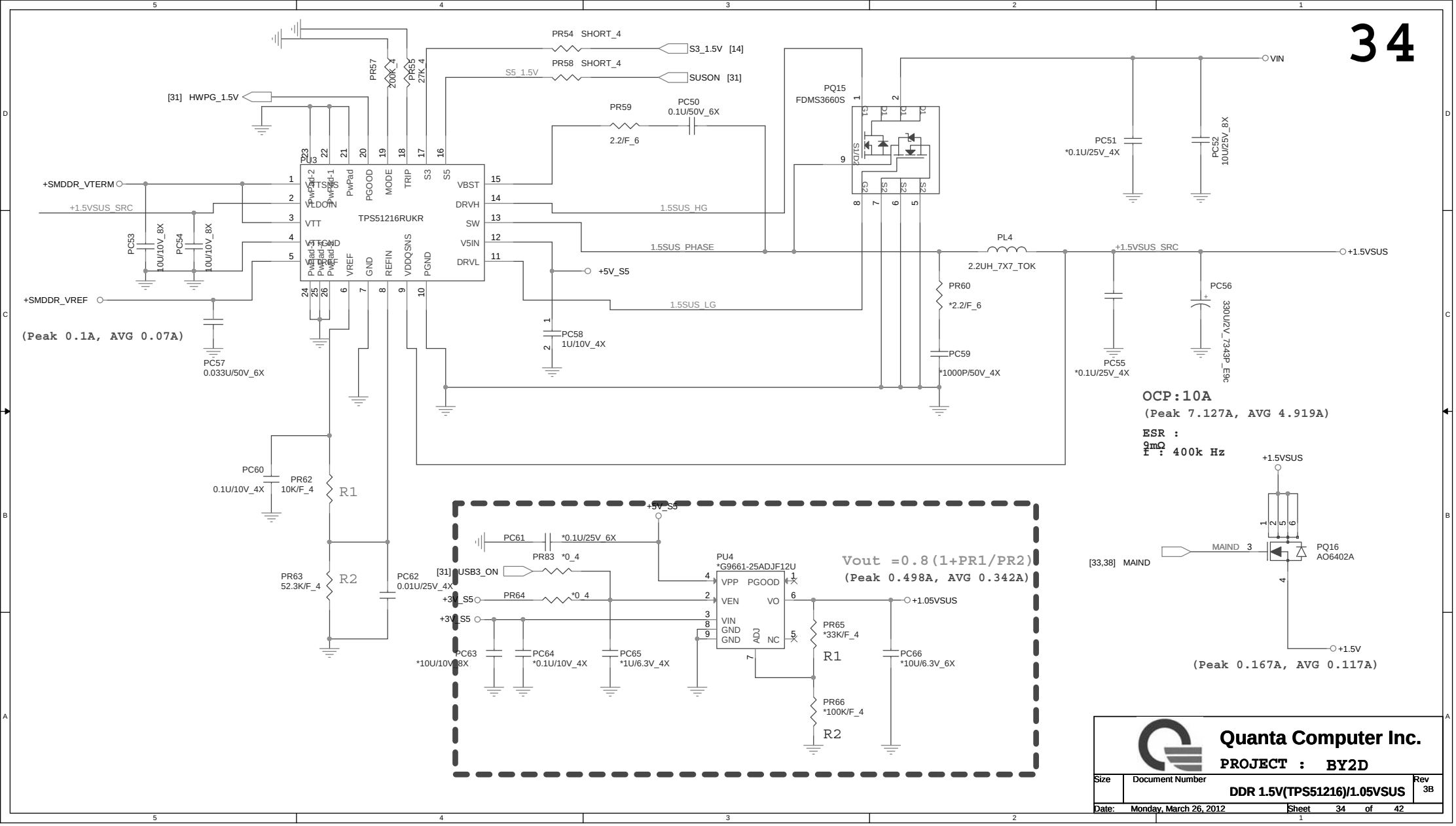
Quanta Computer Inc.
PROJECT : BY2D
Size | Document Number: EC NPCE885LA0DX | Rev 3B
Date: Monday, March 26, 2012 | Sheet 31 of 42



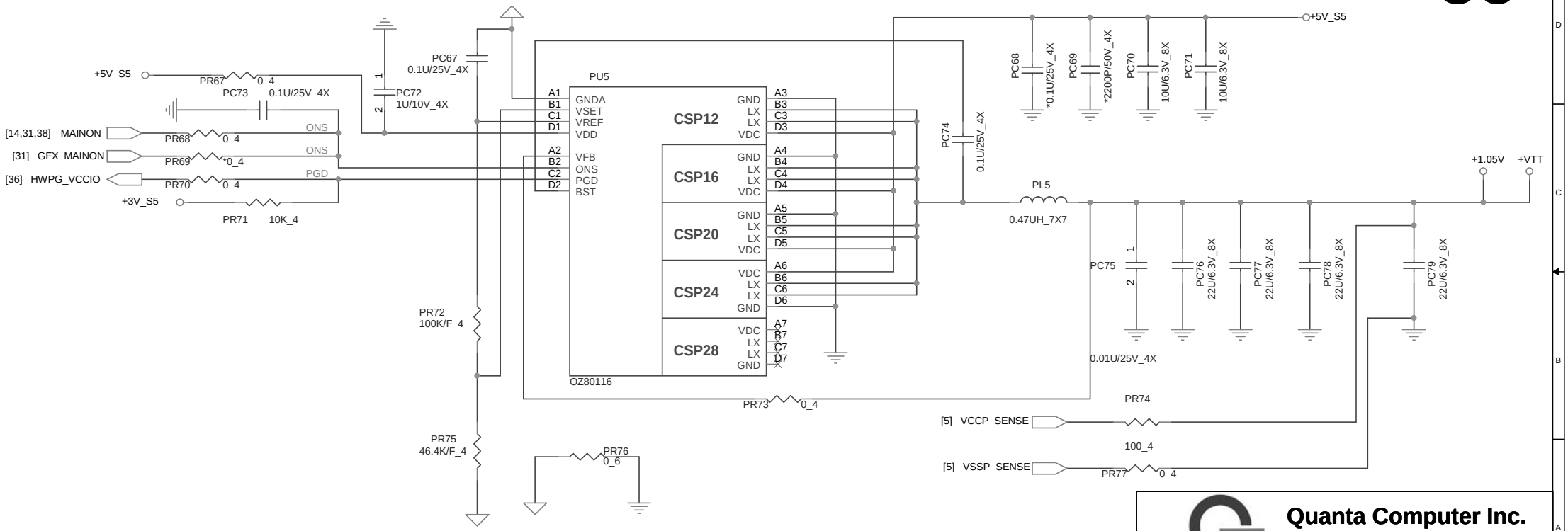
Quanta Computer Inc.		
PROJECT : BY2D		
Size	Document Number	Rev
	CHARGER-ISL88731C	3B
Date: Monday, March 26, 2012	Sheet 32 of 42	



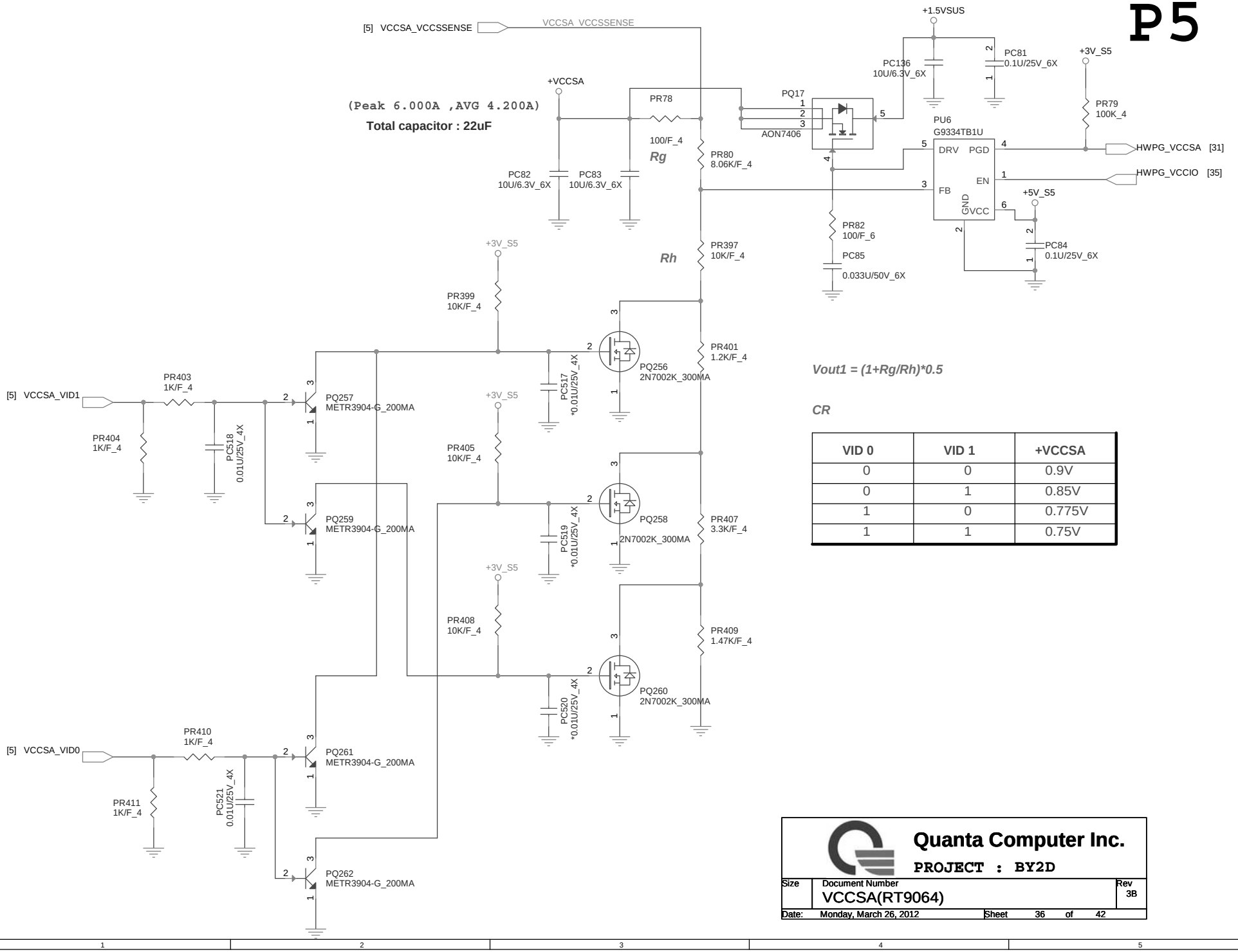
Quanta Computer Inc.		
PROJECT : BY2D		
Size	Document Number: System 3V/5V(RT8210B)	Rev: 3B
Date: Monday, March 26, 2012	Sheet 33 of 42	



Quanta Computer Inc.		
PROJECT : BY2D		
Size	Document Number: DDR 1.5V(TPS51216)/1.05VSUS	Rev: 3B
Date: Monday, March 26, 2012	Sheet 34 of 42	



Quanta Computer Inc.		
PROJECT : BY2D		
Size	Document Number: VTT/1.05V(OZ80116)	Rev: 3B
Date: Monday, March 26, 2012	Sheet 35 of 42	



*Vout1 = (1+Rg/Rh)*0.5*

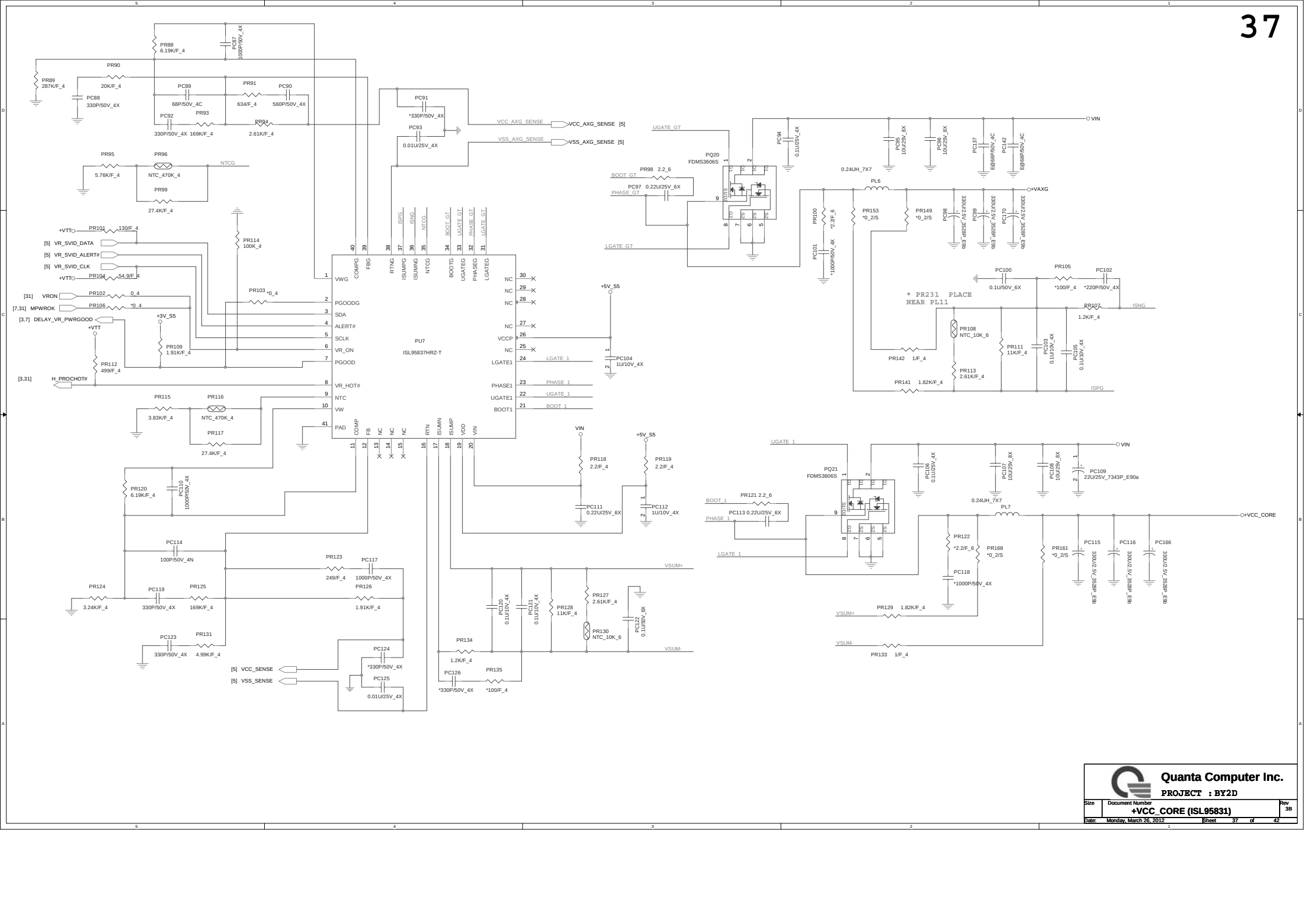
CR

VID 0	VID 1	+VCCSA
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

Quanta Computer Inc.

PROJECT : BY2D

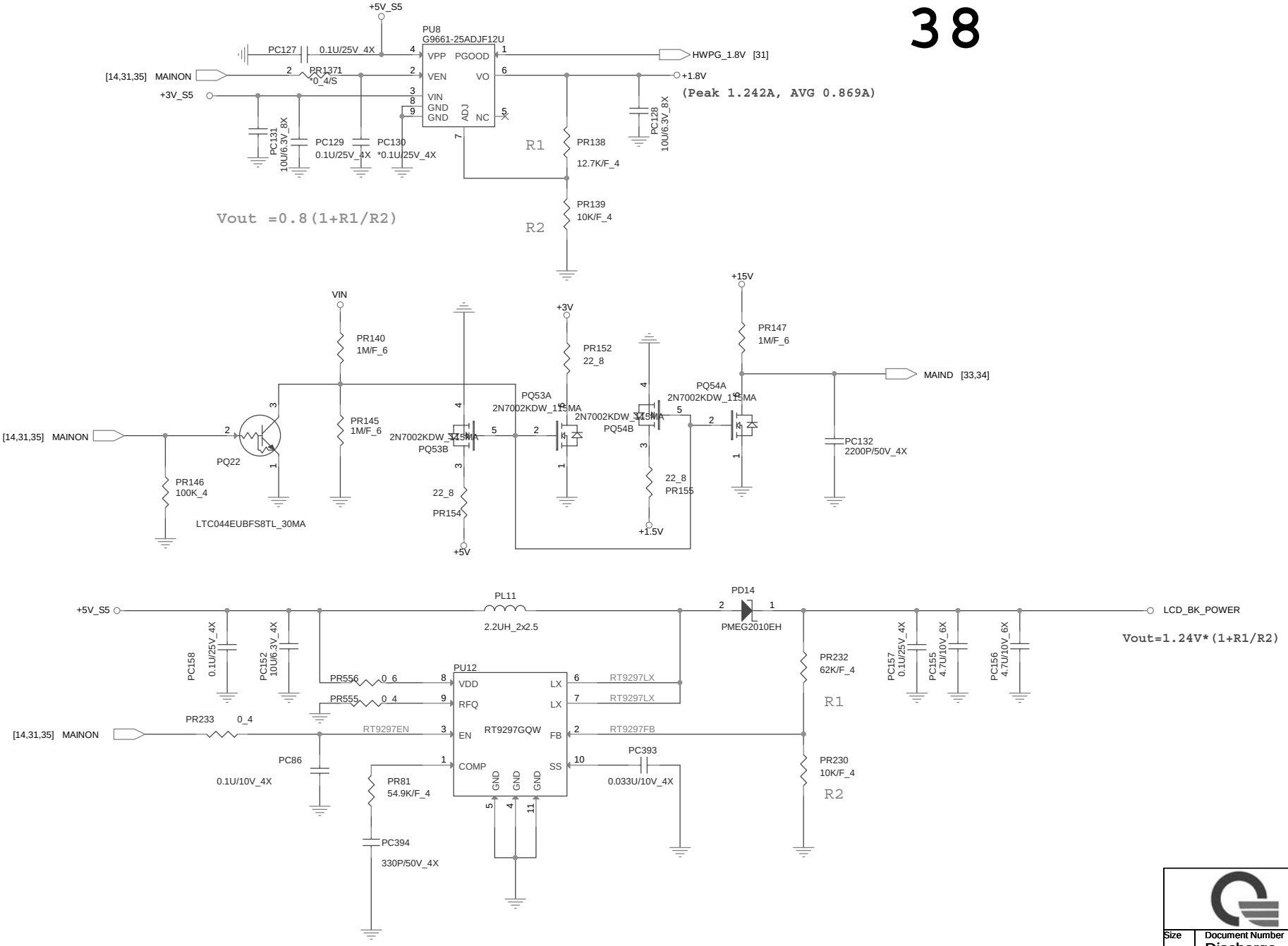
Size	Document Number	Rev
	VCCSA(RT9064)	3B
Date: Monday, March 26, 2012	Sheet 36 of 42	



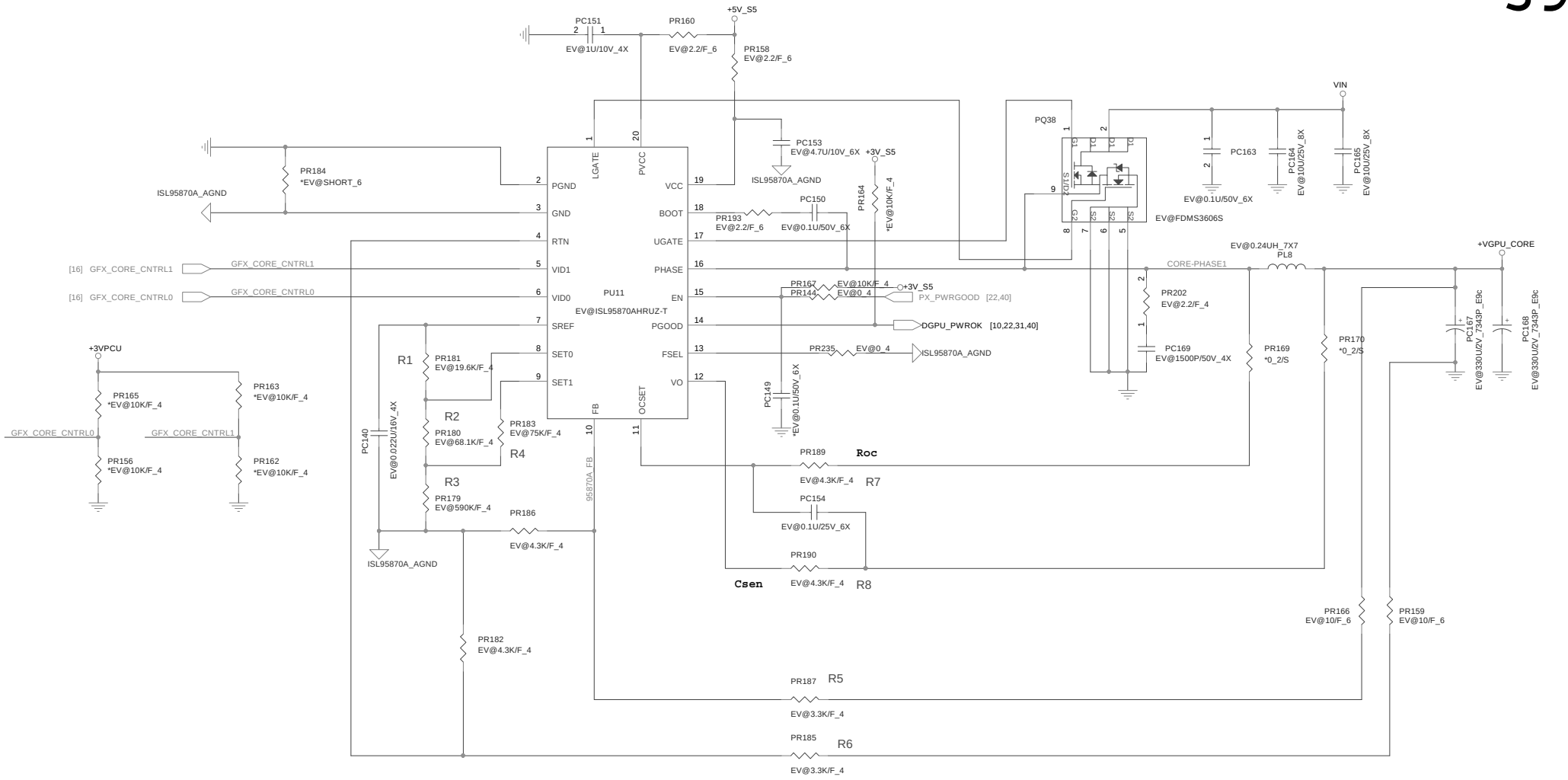
Quanta Computer Inc.

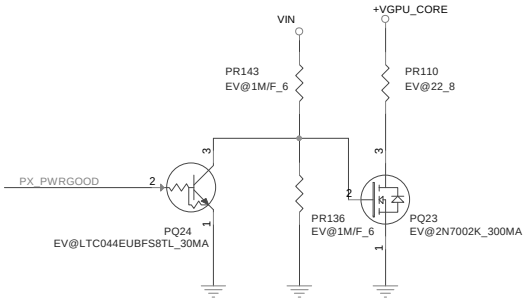
PROJECT : BY2D

Size	Document Number	Rev
	+VCC_CORE (ISL95831)	3B
Date: Monday, March 26, 2012	Sheet 37 of 42	



Quanta Computer Inc.		
PROJECT : BY2D		
Size	Document Number: Discharge	Rev: 3B
Date: Monday, March 26, 2012	Sheet 38 of 42	





R1	19.6K/F_4
R2	68.1K/F_4
R3	590K/F_4
R4	75K/F_4
R5/R6	3.3K/F_4
R7/R8	4.3K/F_4

Thames Pro S3

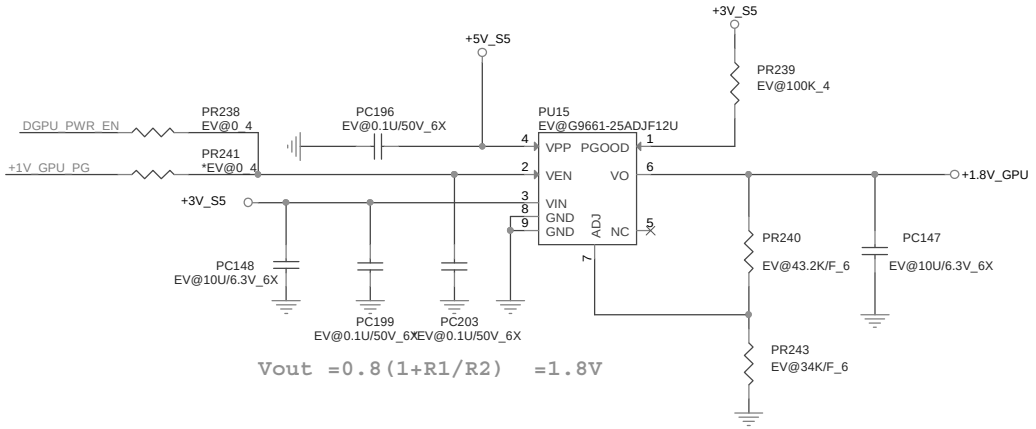
GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	+VGPU_CORE
1	1	0.875V
1	0	0.9V
0	1	1V
0	0	1V

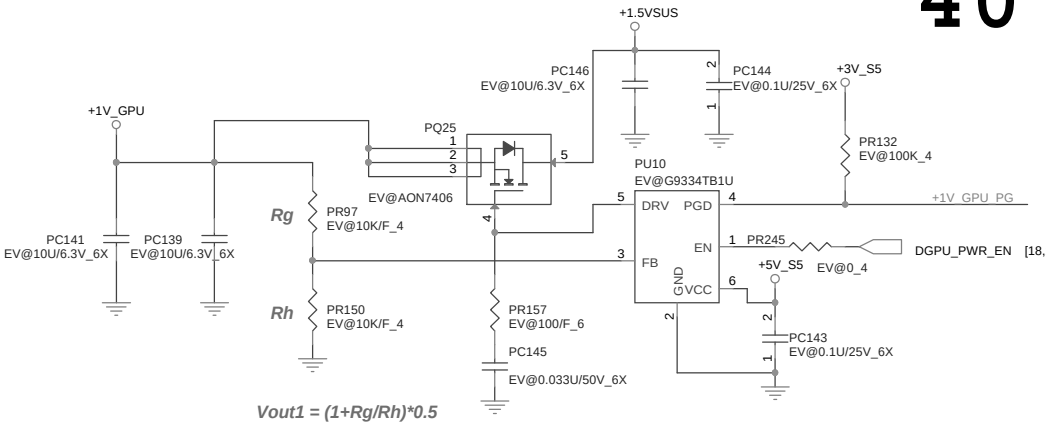
Quanta Computer Inc.

PROJECT : BY2D

Size	Document Number	Rev
	GPU Core (ISL62881C)	3B

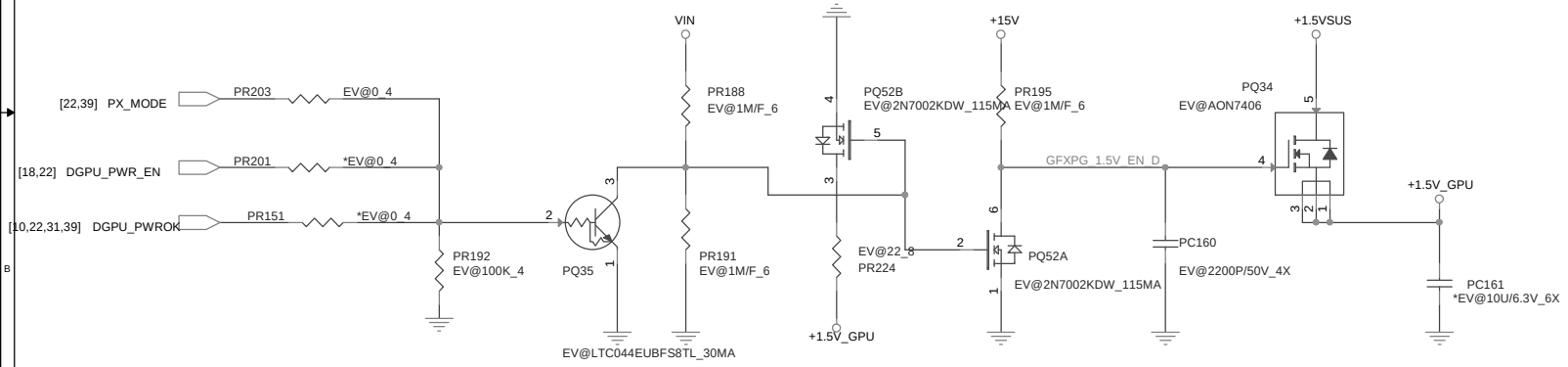
Date: Monday, March 26, 2012 Sheet 39 of 42





(Peak 6.000A ,AVG 4.200A)

Total capacitor : 22uF

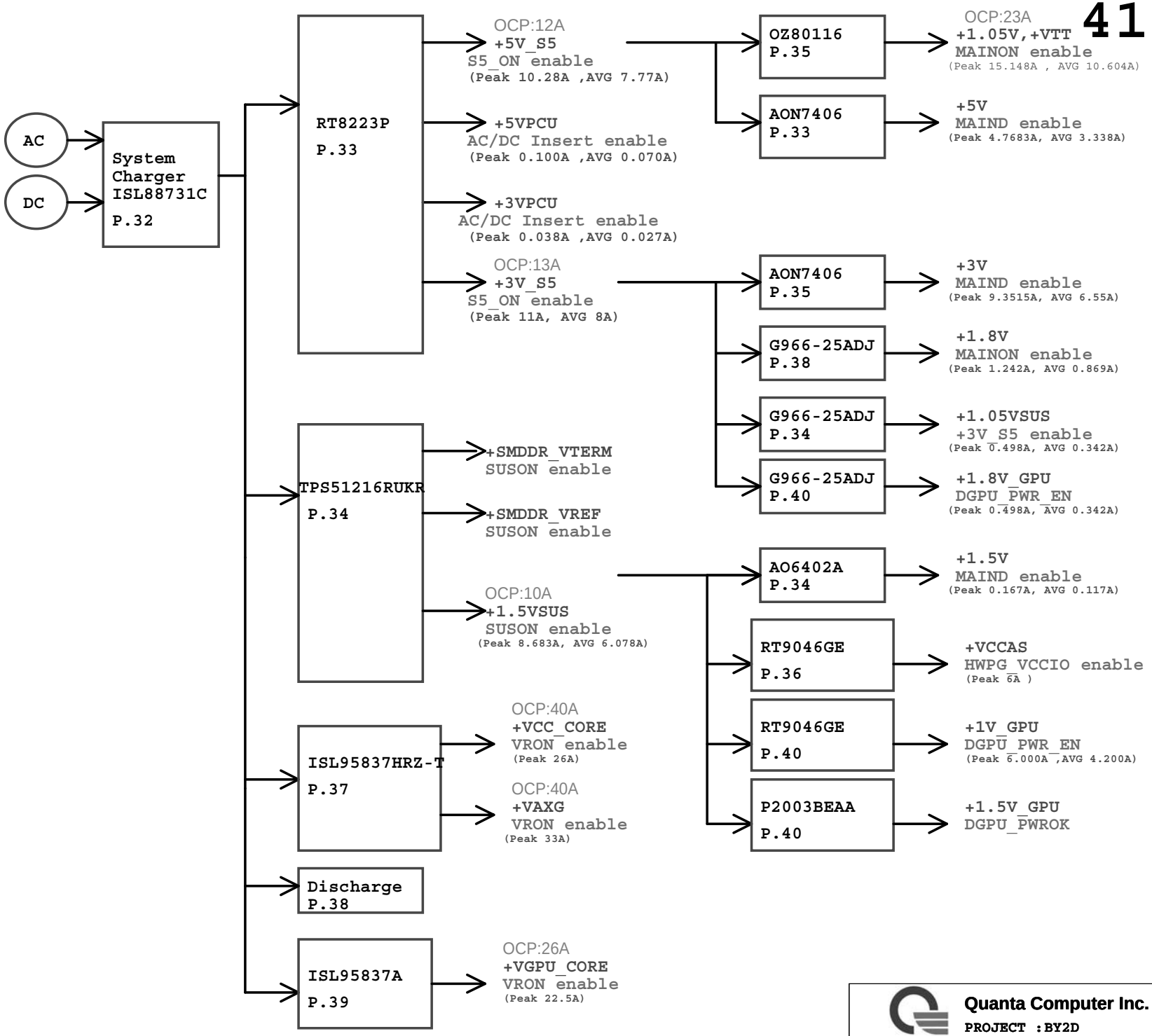


Power On Sequence
1. +3V_GPU connect +3V
2.PX_PWRGOOD Enable +VGPU_CORE
3.DGPU_PWROK Enable(Delay) +1.8V_GFX
4. DGPU_PWR_EN Enable(Delay) +1.5V_GFX
5.DGPU_PWR_EN Enable(Delay) +1V_GFX

Quanta Computer Inc.

PROJECT : BY2D

Size	Document Number	Rev
	+VGACORE	3B
Date: Monday, March 26, 2012	Sheet 40 of 42	



Quanta Computer Inc.		
PROJECT : BY2D		
Size	Document Number: POWER TREE	Rev 3B
Date: Monday, March 26, 2012	Sheet 41 of 42	

Model REV 4A

CHANGE LIST

BY2D MB

PAGE 10: BY2D_B Add BOARD_ID4 to set HI=Int or Low=Ext USB3.0
PAGE 10: BY2D_B Correct BOARD_ID2 Hi=BY2D Low=BY2
PAGE 22: BY2D_B Change R5147 from 10k to 1k for VGA loss issue
PAGE 24: BY2D_B Del R345 but add R338
PAGE 25: BY2D_B Mount C16 for WiMAX power issue
PAGE 26: BY2D_B Mount C371 for USB3.0 power issue
PAGE 31: BY2D_B Add RF_LED# PU 10k to +5VPCU
PAGE 34: BY2D_B Remove +1.05VSUS power rail circuit
PAGE 38: BY2D_B Remove LCD_BK_POWER power rail circuit PU12,PL11,PD14,PC152,PC158,PR555,PR556,PR233,PC86,PR81,PC394,PC393,PR230,PR232,PC155,PC156,PC157
PAGE 08: BY2D_C Add D15 and remove D19 & D18
PAGE 09: BY2D_C Change usb3.0 port from port2 to port1
PAGE 09: BY2D_C Change usb2.0(Colay w/ USB 3.0) port from port1 to port0
PAGE 24: BY2D_C Del R338 but add R345
PAGE 33: BY2D_C Remove PC133
PAGE 37: BY2D_C Change PR124 from 2.37k to 3.24k, PR95 from 3.83K to 5.76K
PAGE 38: BY2D_C Add LCD_BK_POWER power rail circuit PU12,PL11,PD14,PC152,PC158,PR555,PR556,PR233,PC86,PR81,PC394,PC393,PR230,PR232,PC155,PC156,PC157
PAGE 38: BY2D_C Change PR232 from 97.6K to 62K
The BY2D_D schematic is the same as BY2D_C
PAGE 3: BY2D_E R118,R383 Change footprint to short PAD
PAGE 3: BY2D_E Add ESD parts D46,D47,D48
PAGE 5: BY2D_E R112,R113,R208,R209,R218,R220 Change footprint to short PAD
PAGE 8: BY2D_E Add U2005,R2222,R2223,R2231,R481,R455,R274,C2020,R302 second BIOS into BOM
PAGE 9: BY2D_E R108,R140,R154,R155,R179,R305,R306,R314,R341,R342 Change footprint to short PAD
PAGE 11: BY2D_E R69 Change footprint to short PAD
PAGE 15: BY2D_E R3517,R3571,R3579,R3582,R3616 Change footprint to short PAD
PAGE 18: BY2D_E R3700 Change footprint to short PAD
PAGE 18: BY2D_E Change C3600 footprint from 0603 to 0805
PAGE 23: BY2D_E R7 Change footprint to short PAD
PAGE 24: BY2D_E R13,R231 Change footprint to short PAD
PAGE 24: BY2D_E Add C6 for LCD noise.
PAGE 26: BY2D_E R129,R130,R183,R184 Change footprint to short PAD
PAGE 26: BY2D_E Change C364 footprint from 0805 to 1206
PAGE 26: BY2D_E Delete L9
PAGE 27: BY2D_E R248,R486 Change footprint to short PAD
PAGE 29: BY2D_E Delete L19
PAGE 29: BY2D_E R514 Change footprint to short PAD
PAGE 29: BY2D_E Mount C268
PAGE 30: BY2D_E Hole17 disconnect to GND
PAGE 31: BY2D_E Remove R226
PAGE 31: BY2D_E Add ESD parts D49,D50
PAGE 32: BY2D_E Remove R226
PAGE 34: BY2D_E Change PR54,PR58 footprint from RC0402 to SHORT0402
PAGE 35: BY2D_E Change PC76,PC77,PC78,PC79 footprint from 0603 to 0805
PAGE 37: BY2D_E Change PQ20,PQ21 from FDMS3660S to MS3606S
PAGE 37: BY2D_E Change PR107,PR134 from 1.02kOhm to 1.2kOhm
PAGE 37: BY2D_E Change PC114 from 68pF to 100pF
PAGE 37: BY2D_E Add PC166,PC170 330U/2.5V_3528P_E9b
PAGE 37: BY2D_E Change PC89 from 47pF to 68pF
PAGE 37: BY2D_E Change PC92 from 270pF to 330pF
PAGE 37: BY2D_E Change PR93 from 255kOhm to 169kOhm
PAGE 38: BY2D_E PU12.9 connect to GND
PAGE 39: BY2D_E Change PQ38 from FDMS3660S to FDMS3606S

MODEL

PAGE	FROM	To
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		
11		
12		
13		
14		
15		
16		
17		
18		
19		
20		
21		
22		
23		
24		
25		
26		
27		
28		
29		
30		
31		
32		
33		
34		
35		
36		
37		
38		
39		
40		

Quanta Computer Inc.
PROJECT : BY2D
Size | Document Number: EE Change list | Rev: 3B
Date: Monday, March 26, 2012 | Sheet 42 of 42