SJM50-PU Block Diagram

Project code: 91.4FC01.001
PCB P/N : 48.4FC01.0SB
REVISION : 08256-SB

PCB STACKUP

TOP	L1
GND	L2
S	L3
S	L4
GND	L5
BOTTOM	L6

Thermal Sensor
SMSC
EMC2103 31

CLK GEN.
ICS9LPRS480BKLFT 3

AMD Giffin CPU
S1G2 (35W)
638-Pin uFCPGA638 4,5,6,7

OUT / IN 16X16

Video RAM
64Mbx16x4 55,56

PCIex16

GPU ON BOARD
M92-M2
50, 51, 52, 53, 54, 55, 56

DDR2
667/800 MHz 16,17

DDR2
667/800 MHz 16,17

North Bridge
AMD RS780M
CPU I/F LVDS, CRT I/F
INTEGRATED GRAHPICS
8,9,10

HDMI 20
LCD 18
CRT 19

A-Link
PCI-E x 4

PCIe
LAN
Giga LAN
BCM5784 26

TXFM 27
RJ45 27

(include SPDIF)
Line Out
MIC In

Codec
VIA VT1702S

AZALIA

South Bridge
AMD SB700
USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
ATA 66/100
ACPI 1.1
LPC I/F
PCI/PCI BRIDGE
11,12,13,14,15

PCIe
Mini 1 Card
Wire LAN 30

RJ11
MODEM
MDC Card

Daughter Board

LPC BUS

SATA
HDD SATA 21

SATA
ODD SATA 22

SATA
ESATA 23

USB
Mini USB
Blue Tooth 24

USB
1 Port

Usb Board

USB
Camera 18

USB
2 Port 26

Cardreader
RTS5159 29

KBC
Winbond
WPCE773LA0DG
32

SPI
BIOS
25X16 33

MEDIA
KEY 35

Touch
Pad 34

INT.
KB 32

MS/MS Pro/xD
/MMC/SD 29

LPC
DEBUG
CONN.

29
INT.SPKR
1.5W

OP AMP
G1454R41U 28

SYSTEM DC/DC
TPS51125 40

INPUTS	OUTPUTS
DCBATOUT	5V_S5(8A) 3D3V_S5(6A) 5V_AUX_S5 3D3V_AUX_S5

TPS51124 41

INPUTS	OUTPUTS
DCBATOUT	1D1V_S0(9A) 1D2V_S0(5A)

TPS51117 42

INPUTS	OUTPUTS
DCBATOUT	1D8V_S3(10A)

RT9026PFP 43

5V_S5	DDR_VREF_S3 0D9V_S3

RT9166 43

3D3V_S0	2D5V_S0 (300mA)

G957 43

3D3V_S0	1D5V_S0 (1A)

G9161 43

3D3V_S5	1D2V_S5 (400mA)

CHARGER
ISL88731HRZ 46

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A

CPU DC/DC
ISL6265HR 39

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0_0 0~1.55V 18A VCC_CORE_S0_1 0~1.55V 18A VDDNB 0~1.55V 18A

SJM50

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Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM

Size: Custom | Document Number: SJM50-PU | Rev: SB

Date: Wednesday, December 24, 2008 Sheet 1 of 56

SJM50

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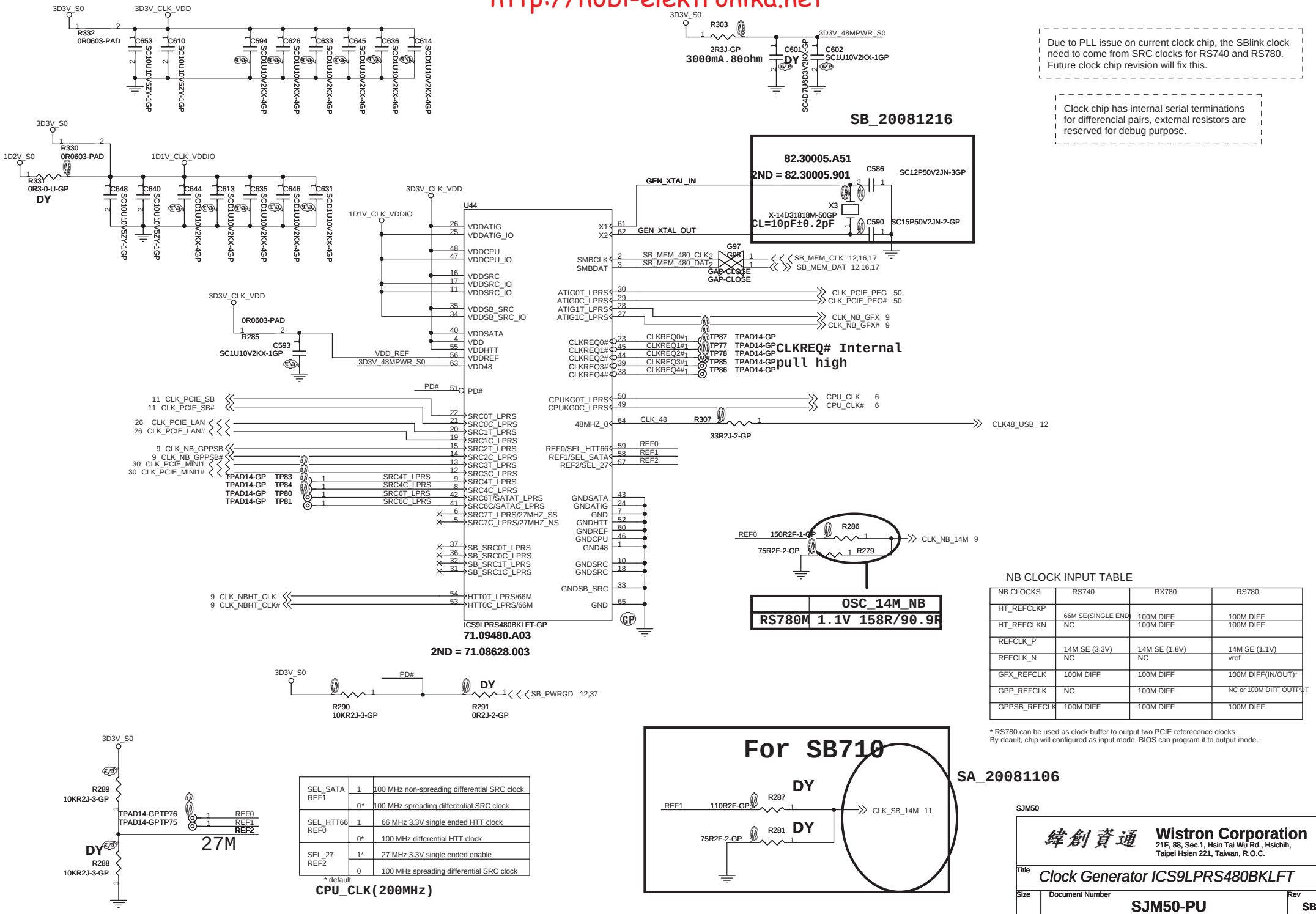
Title: ***Change Lst***

Size	Document Number	Rev
A3	SJM50-PU	SB

Date: Friday, December 05, 2008 Sheet 2 of 56



NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

* RS780 can be used as clock buffer to output two PCIE referecence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.

SJM50

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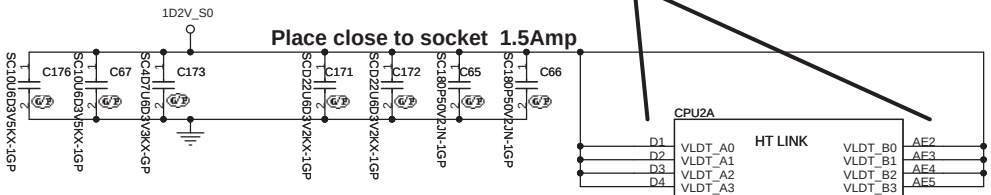
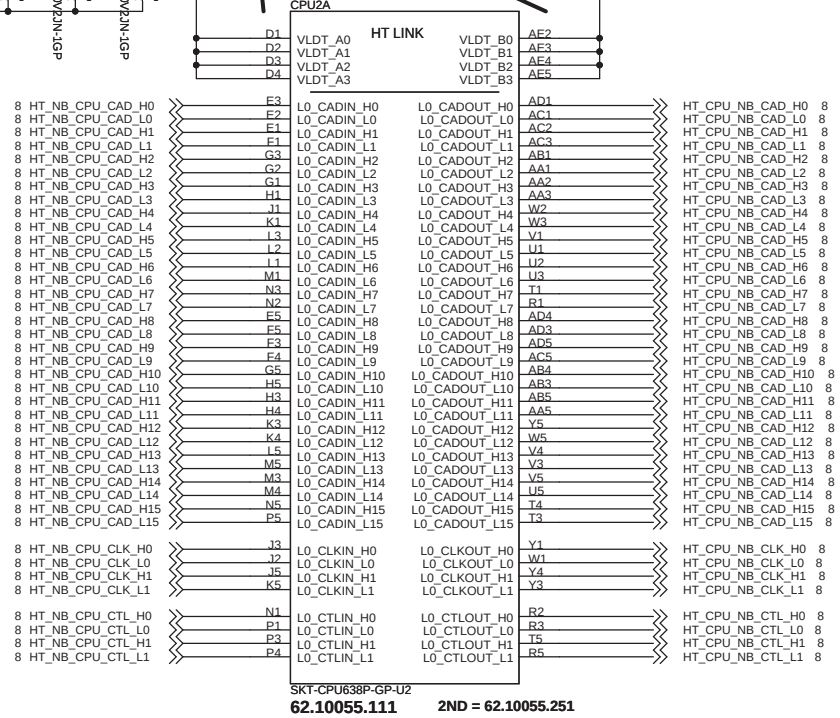
Title: Clock Generator ICS9LPRS480BKLFT

Size	Document Number	Rev
	SJM50-PU	SB

Date: Tuesday, December 23, 2008 Sheet 3 of 56

Placement note:
10ux1,4.7ux1,0.22ux1,180px1 for each group





62.10055.111 **2ND = 62.10055.251**

SKT-BGA638H176

State	Specification	Notes	2M200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P2	CPU COF	1	1500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P3	CPU COF	1	1300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P4	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P6	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P7	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V

SJM50

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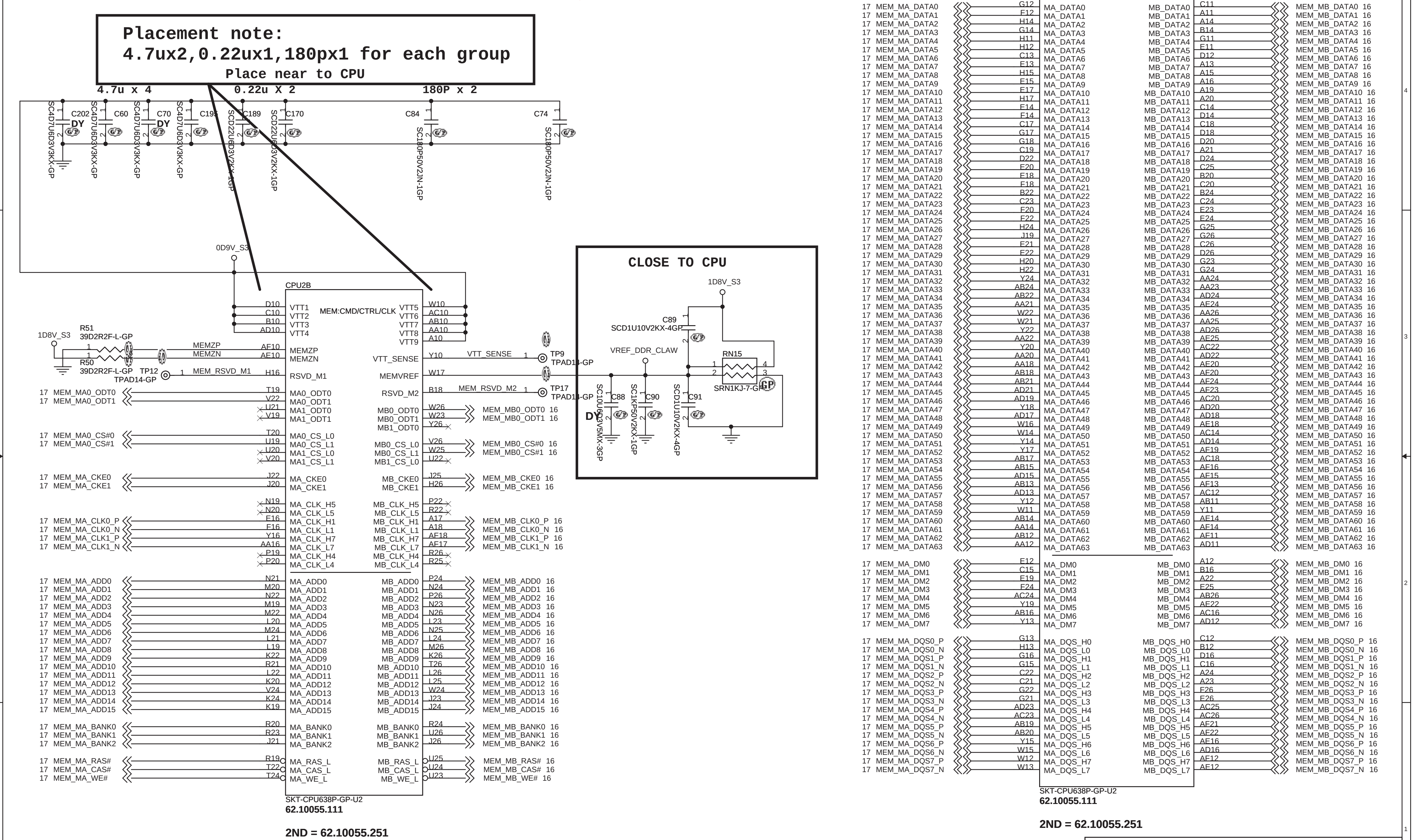
Title: ***CPU (1 of 4)***

Size | Document Number: **SJM50-PU** | Rev: **SB**

Date: Tuesday, December 23, 2008 Sheet 4 of 56


Placement note:
4.7ux2,0.22ux1,180px1 for each group
Place near to CPU
4.7u x 4
0.22u X 2
180P x 2
C202 DY
C60
C70 DY
C195
C189
C170
C84
C74
SC4D7U6D3V3KX-GP
SC4D7U6D3V3KX-GP
SC4D7U6D3V3KX-GP
SC4D7U6D3V3KX-GP
SCD22U6D3V2KX-1GP
SCD22U6D3V2KX-1GP
SC180P50V2JN-1GP
SC180P50V2JN-1GP
0D9V_S3
1D8V_S3
R51
39D2R2F-L-GP
R50
39D2R2F-L-GP
TP12
TPAD14-GP
MEMZP
MEMZN
MEM_RSVD_M1
CPU2B
MEM:CMD/CTRL/CLK
VTT1
VTT2
VTT3
VTT4
VTT5
VTT6
VTT7
VTT8
VTT9
VTT_SENSE
MEMVREF
RSVD_M1
RSVD_M2
TP9
TPAD14-GP
TP17
TPAD14-GP
MEM_RSVD_M2
17 MEM_MA0_ODT0
17 MEM_MA0_ODT1
17 MEM_MA0_CS#0
17 MEM_MA0_CS#1
17 MEM_MA_CKE0
17 MEM_MA_CKE1
17 MEM_MA_CLK0_P
17 MEM_MA_CLK0_N
17 MEM_MA_CLK1_P
17 MEM_MA_CLK1_N
17 MEM_MA_ADD0 … MEM_MA_ADD15
17 MEM_MA_BANK0
17 MEM_MA_BANK1
17 MEM_MA_BANK2
17 MEM_MA_RAS#
17 MEM_MA_CAS#
17 MEM_MA_WE#
MEM_MB0_ODT0 16
MEM_MB0_ODT1 16
MEM_MB0_CS#0 16
MEM_MB0_CS#1 16
MEM_MB_CKE0 16
MEM_MB_CKE1 16
MEM_MB_CLK0_P 16
MEM_MB_CLK0_N 16
MEM_MB_CLK1_P 16
MEM_MB_CLK1_N 16
MEM_MB_ADD0 … MEM_MB_ADD15 16
MEM_MB_BANK0 16
MEM_MB_BANK1 16
MEM_MB_BANK2 16
MEM_MB_RAS# 16
MEM_MB_CAS# 16
MEM_MB_WE# 16
SKT-CPU638P-GP-U2
62.10055.111
2ND = 62.10055.251
CLOSE TO CPU
1D8V_S3
C89
SCD1U10V2KX-4GP
VREF_DDR_CLAW
RN15
SRN1KJ-7-GP
C88
C90
C91
DY
SC10U6D3V5MX-3GP
SC1KP50V2KX-1GP
SCD1U10V2KX-4GP
CPU2C
MEM:DATA
17 MEM_MA_DATA0 … MEM_MA_DATA63
MEM_MB_DATA0 … MEM_MB_DATA63 16
17 MEM_MA_DM0 … MEM_MA_DM7
MEM_MB_DM0 … MEM_MB_DM7 16
17 MEM_MA_DQS0_P … MEM_MA_DQS7_N
MEM_MB_DQS0_P … MEM_MB_DQS7_N 16
SKT-CPU638P-GP-U2
62.10055.111
2ND = 62.10055.251

緯創資通 Wistron Corporation
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Title: **CPU (2 of 4)**

Size	Document Number	Rev
	SJM50-PU	SB

Date: Tuesday, December 23, 2008 — Sheet 5 of 56

The Processor has reached a preset maximum operating temperature. 100℃
I=Active HTC
O=FAN

LYAOUT:ROUTE VDDA TRACE APPROX. 50mils WIDE(USE 2X25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491

Notice: Nerver change to PAD for R1522
(between ALLOW_LDTSTOP and CPU_LED_REQ#_CPU)

SB_20081202

SA_20081113

SA_20081030

CPU exceeds to 125℃

Cloce To CPU

For HDT DBG

internal pull high 300 ohm

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

Near CPU PIN

84.T3904.C11
2ND = 84.03904.L06

SKT-CPU638P-GP-U2
62.10055.111

2ND = 62.10055.251

HDT Connectors

SMC-CONN26A-FP

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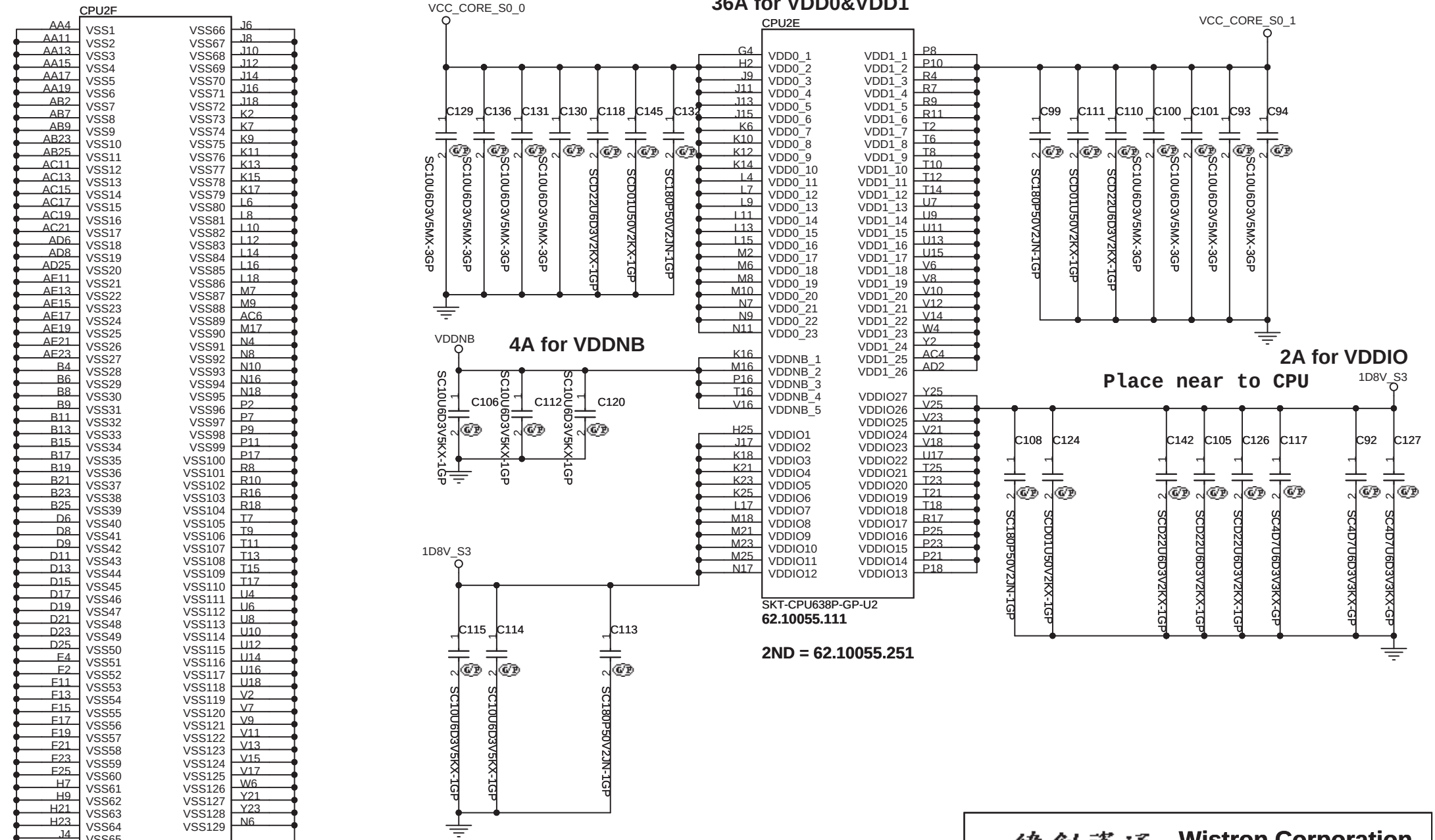
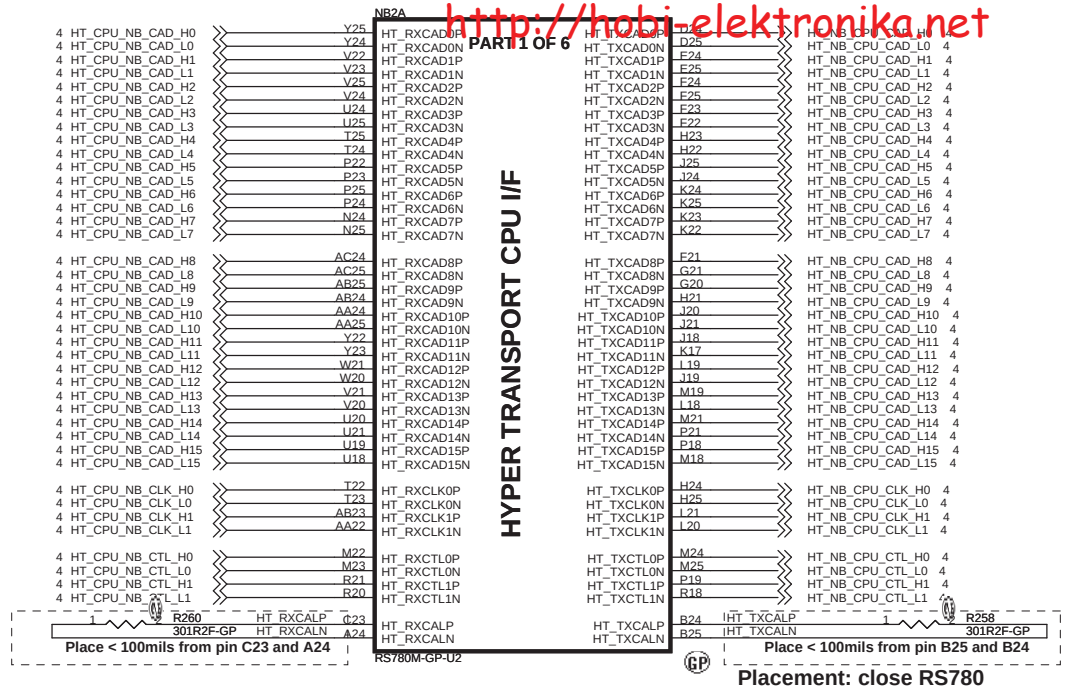
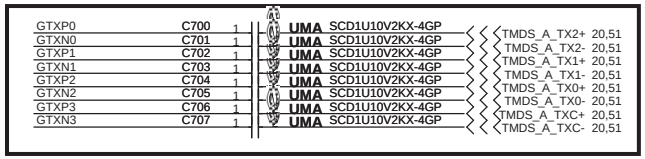
Title: CPU (3 of 4)	
Size	Document Number: SJM50-PU	Rev: SB
Date: Tuesday, December 23, 2008	Sheet 6 of 56	

SJM50



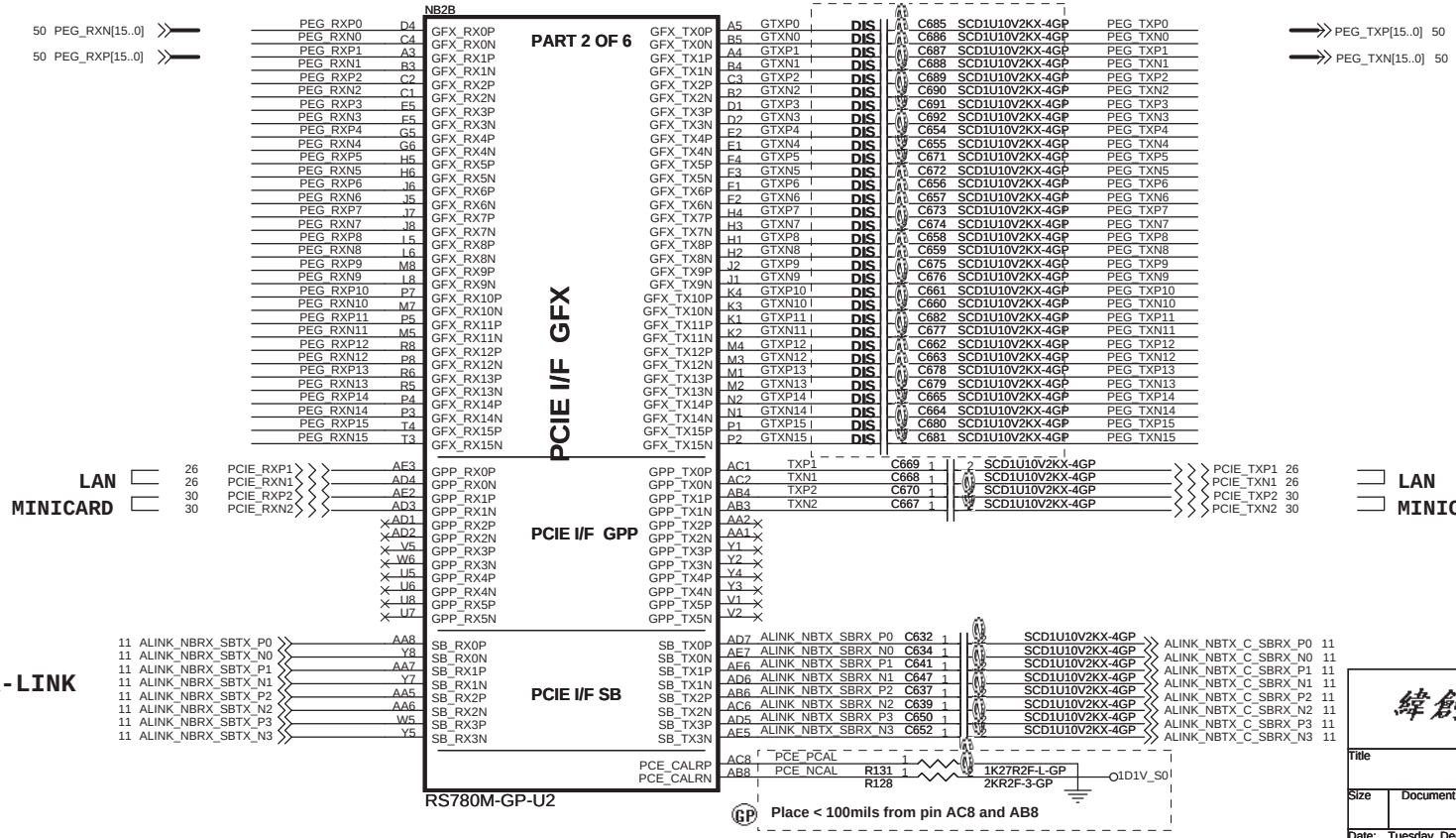
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CPU (4 of 4)***	
Size	Document Number **SJM50-PU**	Rev **SB**
Date: Friday, December 05, 2008	Sheet 7 of 56	





RS780M Display Port Support(muxed on GFX)

DP0	GFX_TX0,TX1,TX2,TX3,AUX0,HPD0
DP1	GFX_TX4,TX5,TX6,TX7,AUX1,HPD1



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Title	RS780 (1 of 3)
Size	Document Number: SJM50-PU
Rev	SB
Date: Tuesday, December 23, 2008	Sheet 8 of 56

STRAP_DEBUG_BUS_GPIO_ENABLEb
Enables the Test Debug Bus using GPIO.(PIN: RS780M--> VSYNC#)
*1 :Disable 0 : Enable

RS780: Enables Side port memory (RS780 use HSYNC#)
*1 :Disable 0 : Enable

SUS_STAT#
Selects Loading of STRAPS From EEPROM
*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected,
or use default values if not connected

NB2C

PART 3 OF 6

CRT/TVOUT
PWR
LVTM
PLL
PM
CLOCKs
MIS.

RS780M-GP-U2

Close to NB ball

SA_20081110

ENABLE External CLK GEN

	GPIO MODE	
STRP_DATA	0	*1
VCC_NB	1.0V	1.1V

Near NB

SB_20081221

68.00206.121
2ND = 68.00216.161

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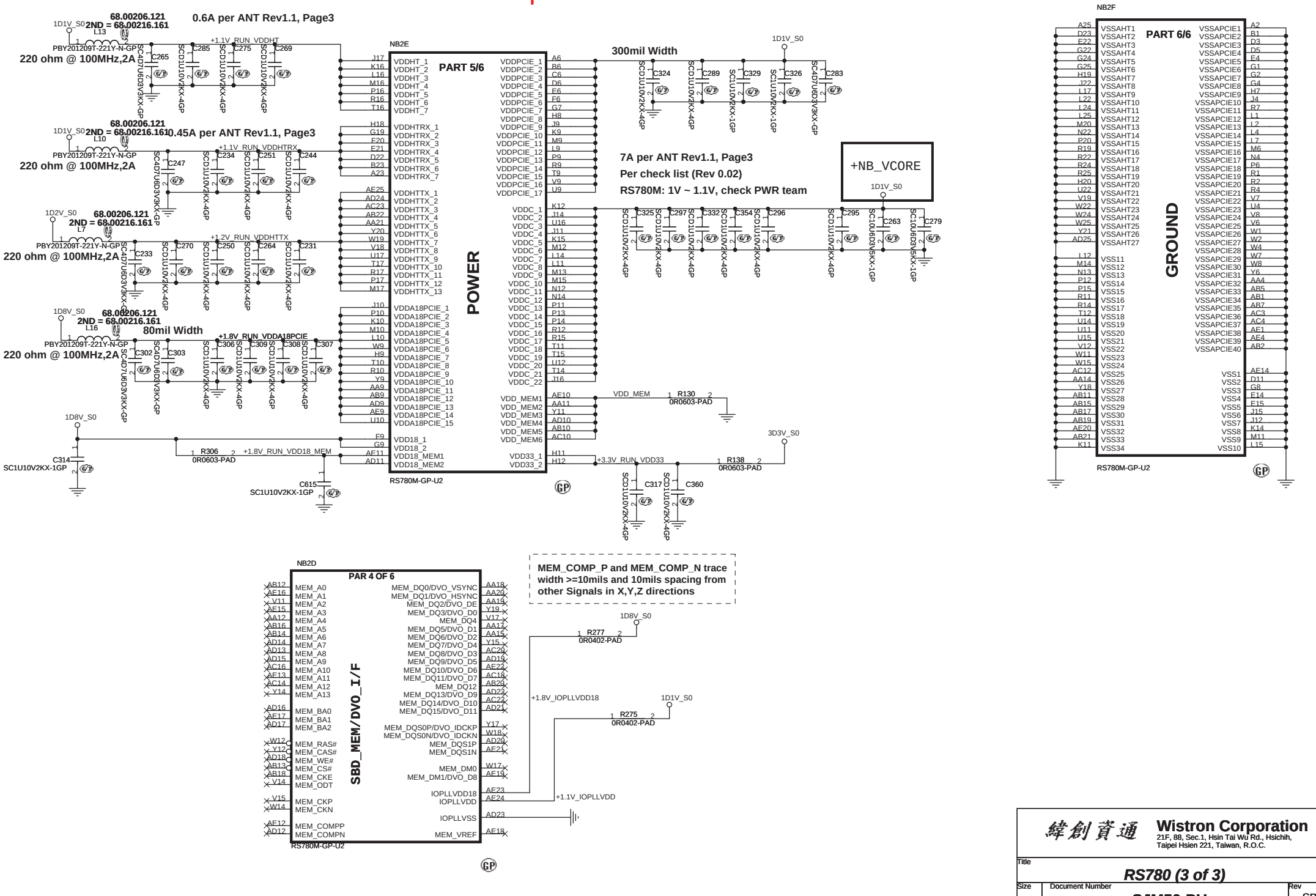
Title: RS780 (2 of 3)	
Size:	Document Number: SJM50-PU
Rev: SB	
Date: Tuesday, December 23, 2008	Sheet 9 of 56



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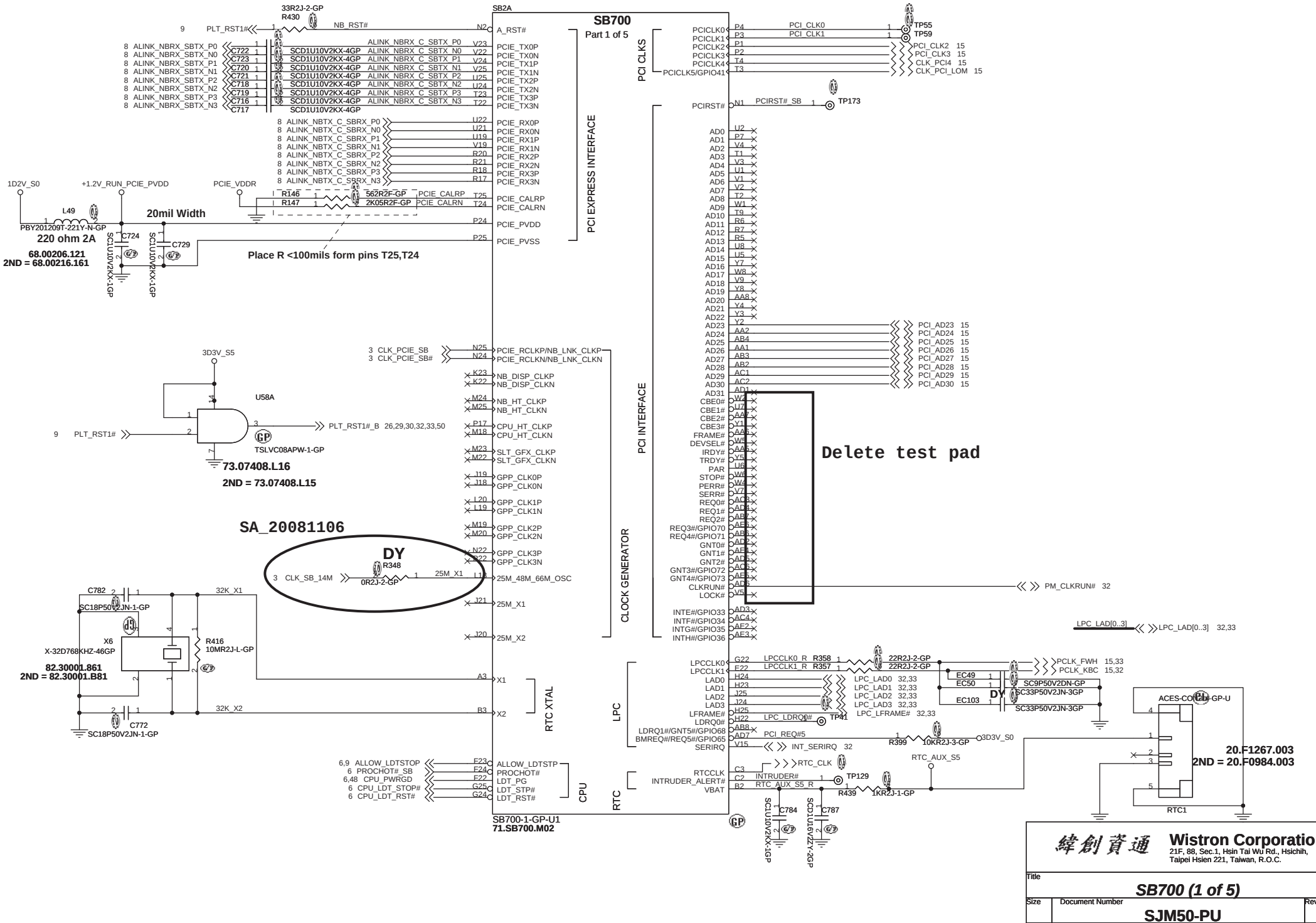
Title	***RS780 (3 of 3)***	
Size	Document Number **SJM50-PU**	Rev SB
Date: Tuesday, December 16, 2008	Sheet 10 of 56	



緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	SB700 (1 of 5)	
Size	Document Number: SJM50-PU	Rev: SB
Date: Tuesday, December 23, 2008	Sheet 11 of 56	

SB700 Part 4 of 5

Place R near pin14. Route it with 10mils Trace width and 25mils spacing to any signals in X, Y, Z directions.

Place these close SB700

USB	
Pair	Device
11	CardReader
10	CCD
9	NC
8	USB4
7	USB3
6	USB2
5	BlueTooth
4	NC
3	NC
2	NC
1	Mini Card1
0	USB1

OCP2#
OCP1#
OCP0#

SA_20081104

Close to SB700

Strap Pin / define to use LPC or SPI ROM

SA_20081107

SB700-1-GP-U1
71.SB700.M02

SJM50

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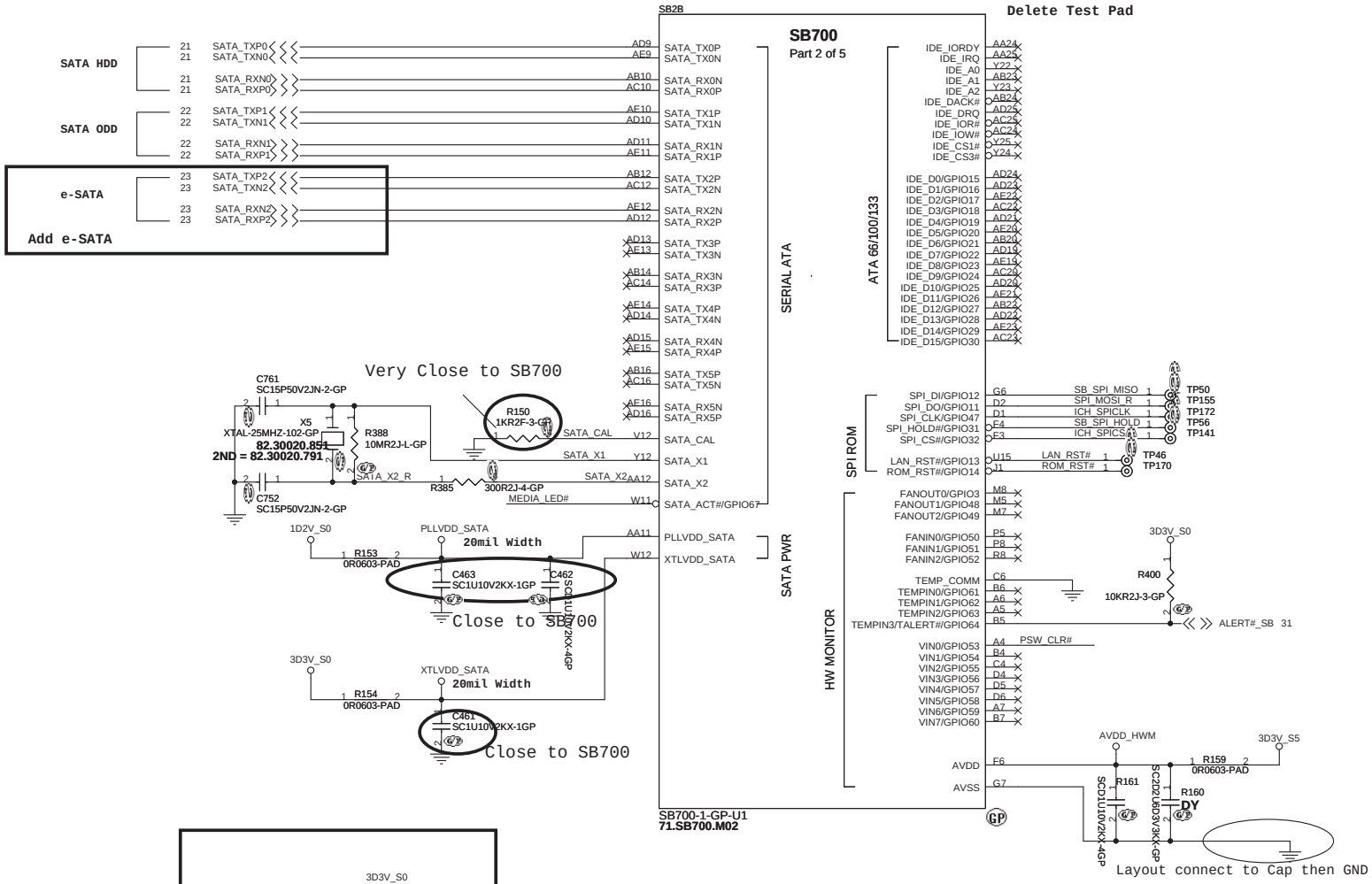
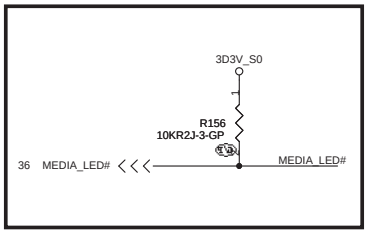
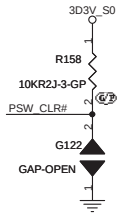
Title: SB700 (2 of 5)
Size: Document Number: SJM50-PU Rev: SB
Date: Tuesday, December 23, 2008 Sheet 12 of 56





SA_20081030



SJM50

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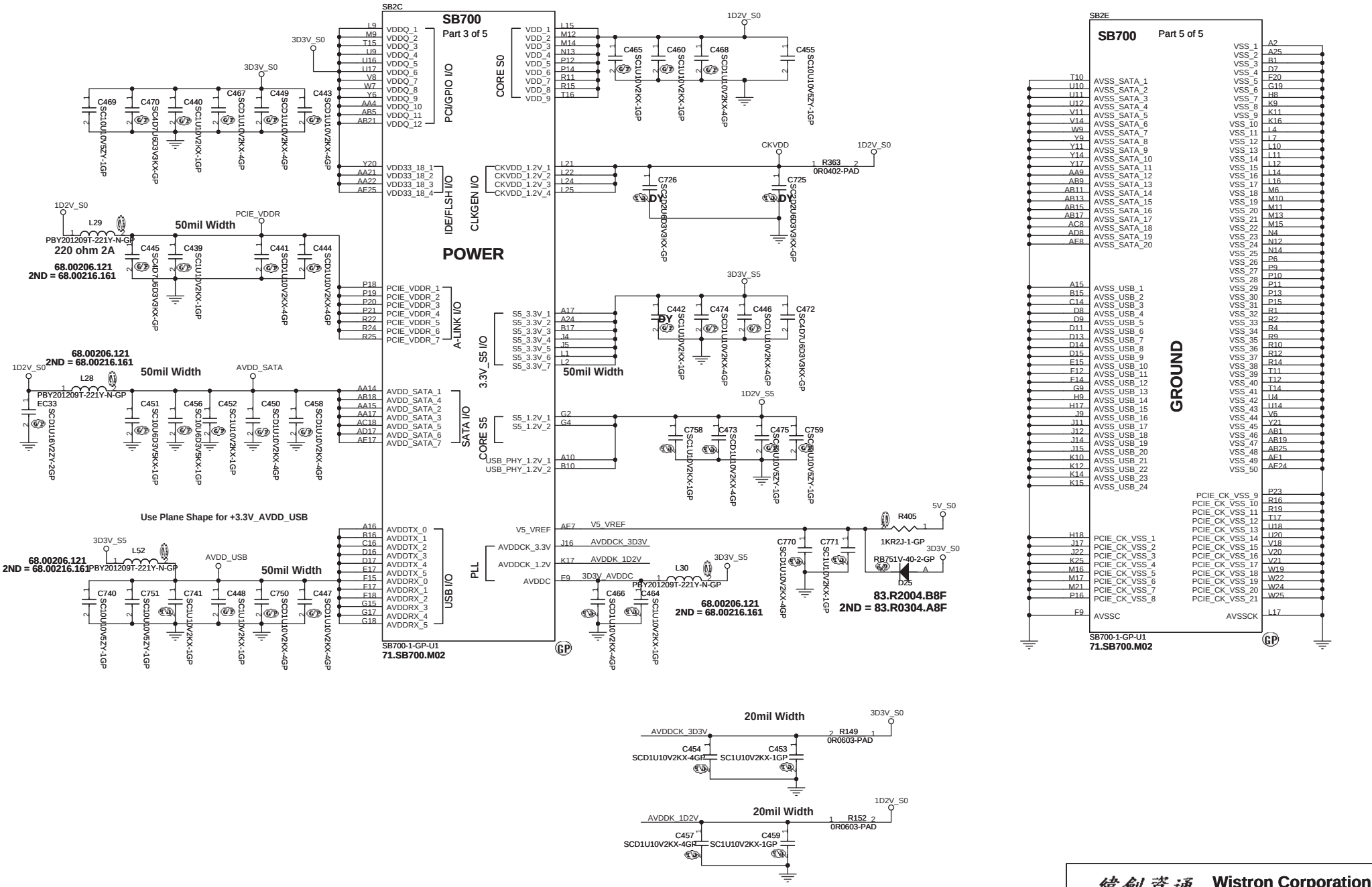
Title: SB700 (3 of 5)		
Size	Document Number: SJM50-PU	Rev: SB
Date: Tuesday, December 23, 2008	Sheet 13 of 56	



緯創資通	**Wistron Corporation**	
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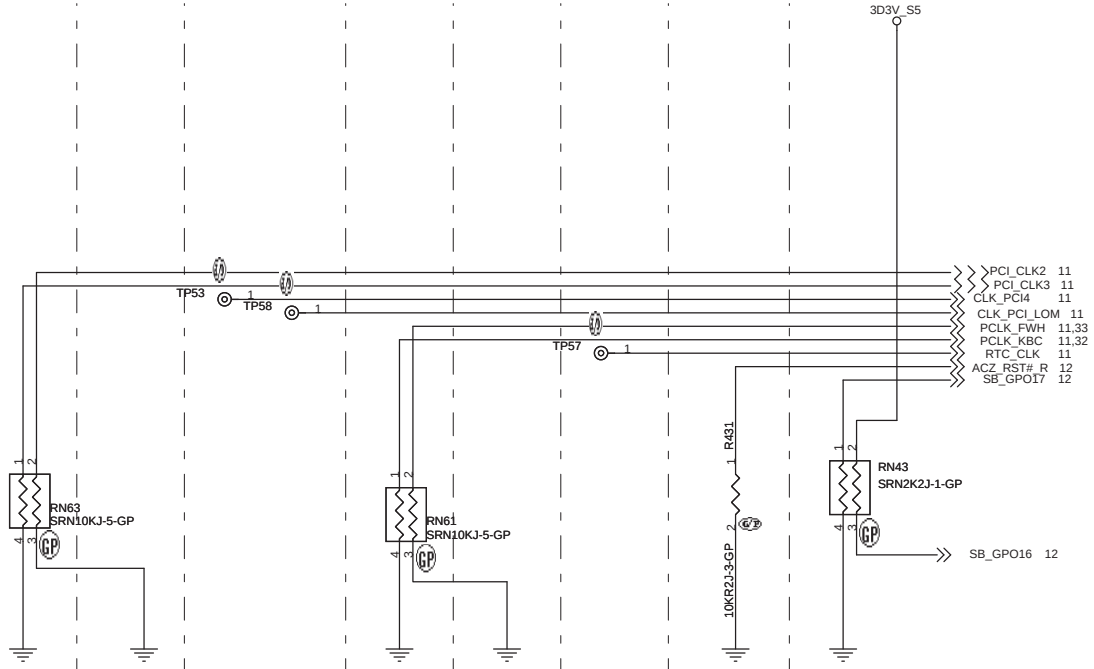
Title	***SB700 (4 of 5)***	
Size	Document Number: **SJM50-PU**	Rev: SB
Date: Tuesday, December 16, 2008	Sheet 14 of 56	

Delete DY Parts

REQUIRED STRAPS

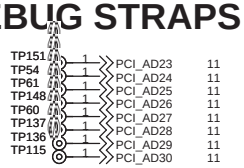
REQUIRED SYSTEM STRAPS



	PCI_CLK2	PCI_CLK3	CLK_PCI_LOM CLK_PCI4	PCLK_FWH	PCLK_KBC	RTCCLK	AZ_RST#	SB_GPO17 , SB_GPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	IMC ENABLED	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT	ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT	L, H = LPC ROM L, L = FWH ROM

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

DEBUG STRAPS



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

緯創資通 Wistron Corporation
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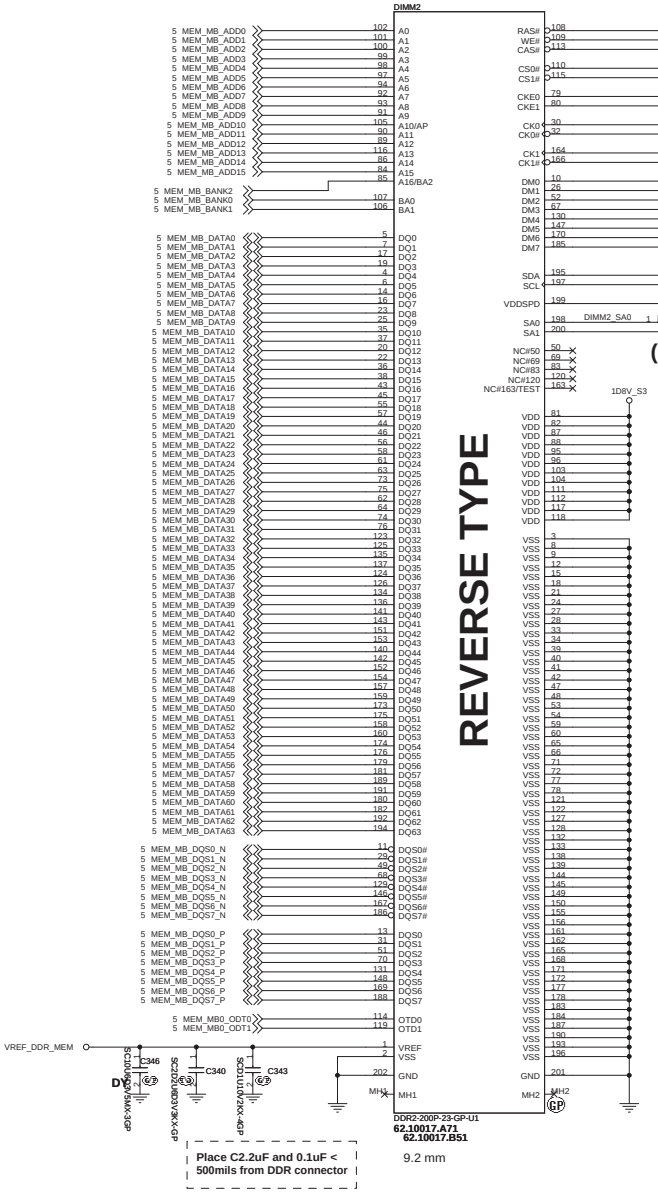
Taipei Hsien 221, Taiwan, R.O.C.

Title: *SB700 (5 of 5)*

Size | Document Number: SJM50-PU | Rev: SB

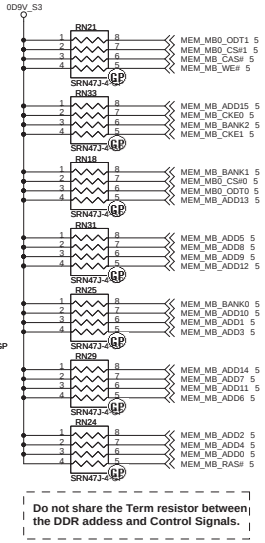
Date: Tuesday, December 23, 2008 | Sheet 15 of 56

DDR2 SOCKET_2



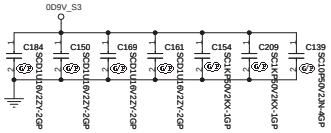
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

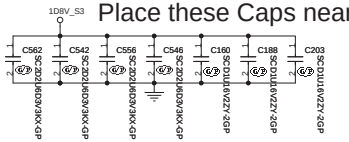


Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

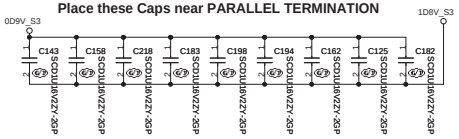


Place these Caps near DM1

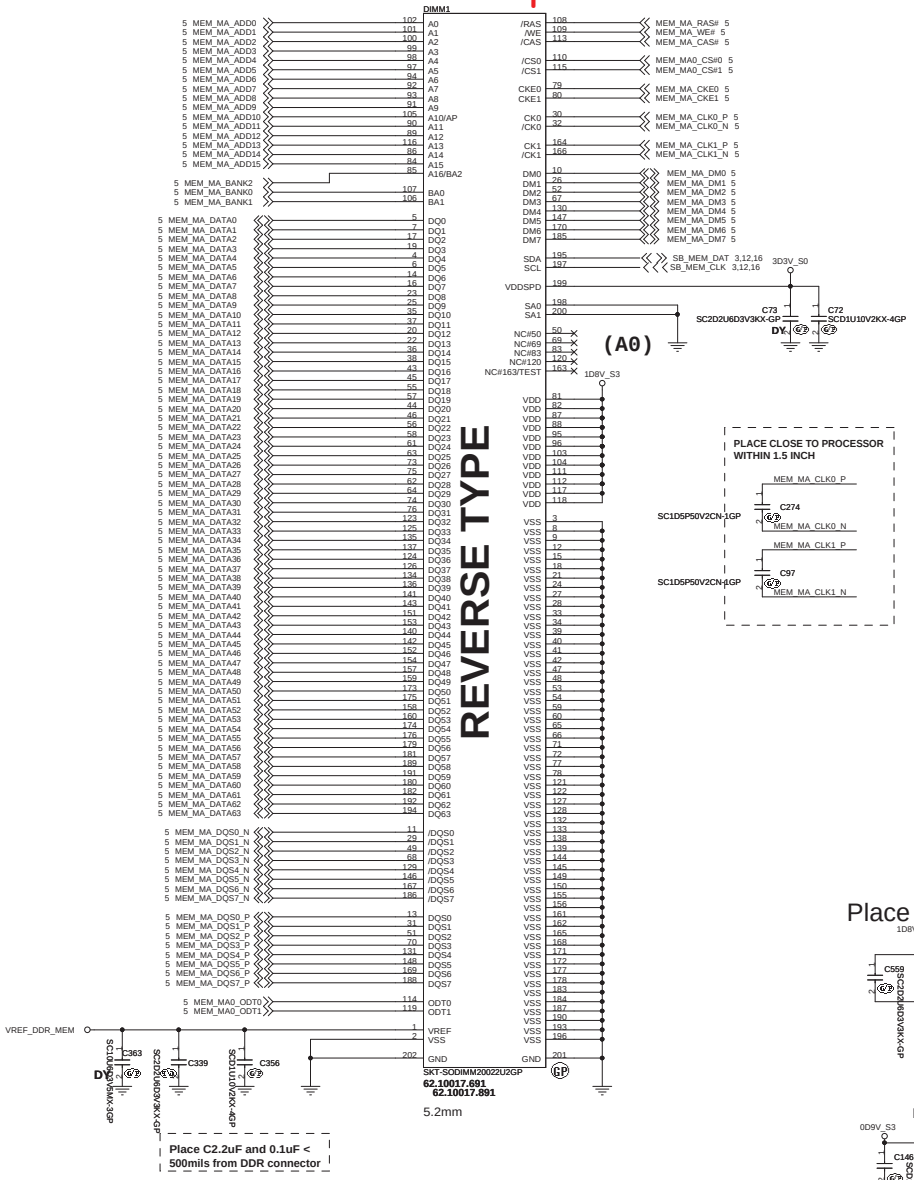


Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near PARALLEL TERMINATION

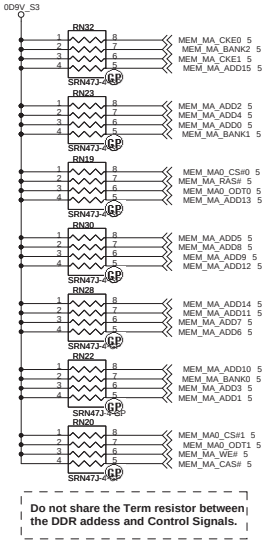


緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: DDR2 Socket_2		
Size	Document Number: SJM50-PU	Rev: SB
Date: Tuesday, December 23, 2008	Sheet 16 of 56	



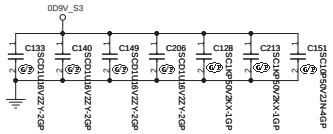
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

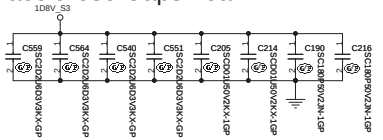


Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

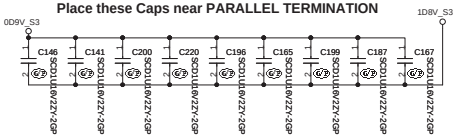


Place these Caps near DM2

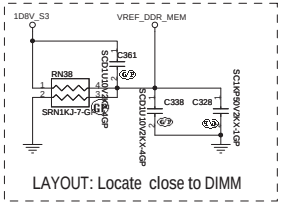


Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near PARALLEL TERMINATION

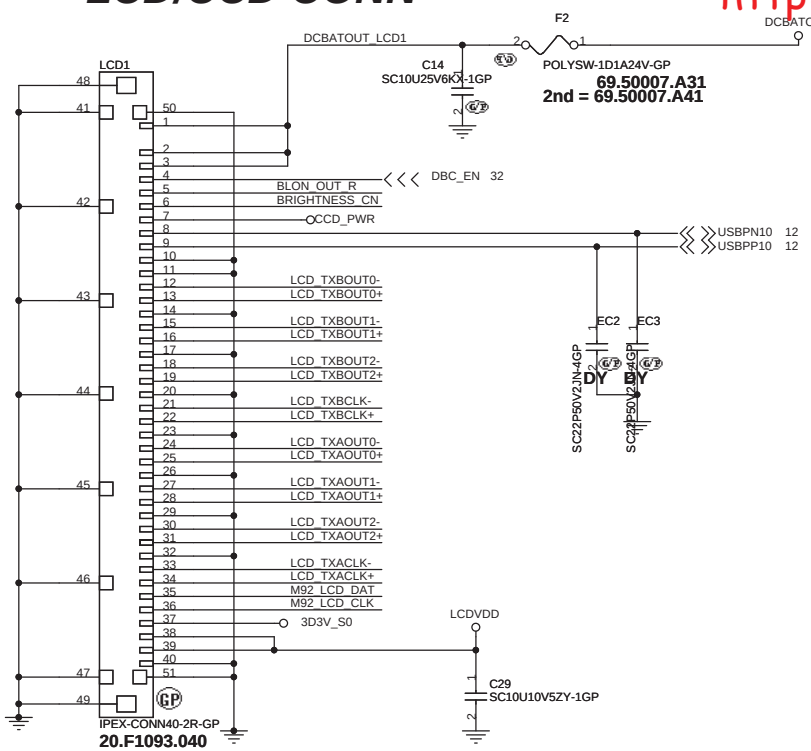


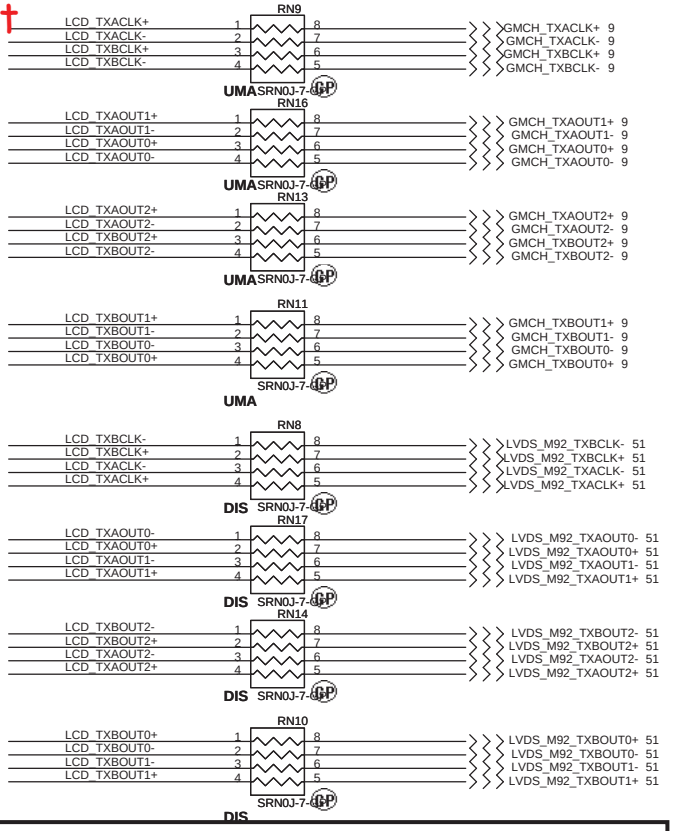
DDR_VREF



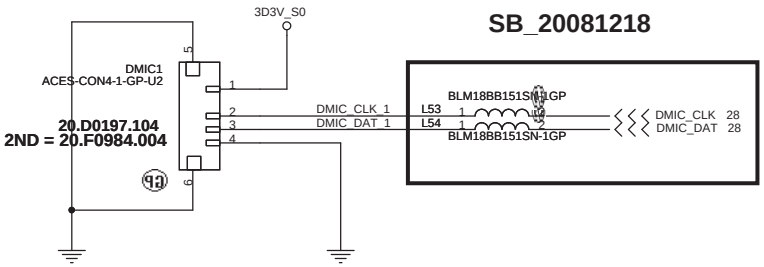
緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: *DDR2 Socket_1*		
Size	Document Number: SJM50-PU	Rev: SB
Date: Tuesday, December 23, 2008	Sheet 17 of 56	

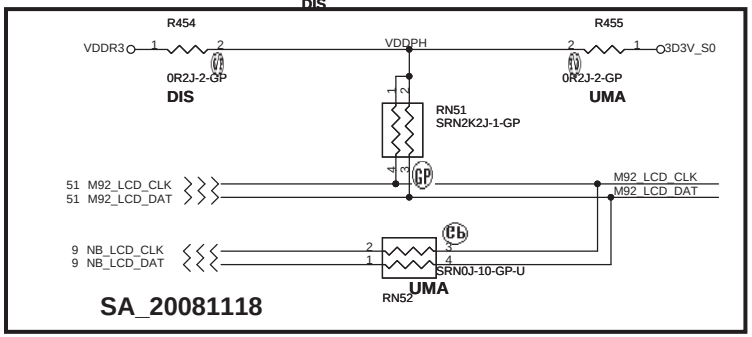
LCD/CCD CONN

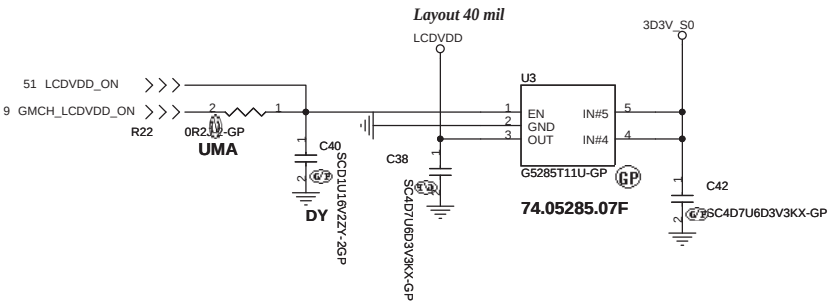


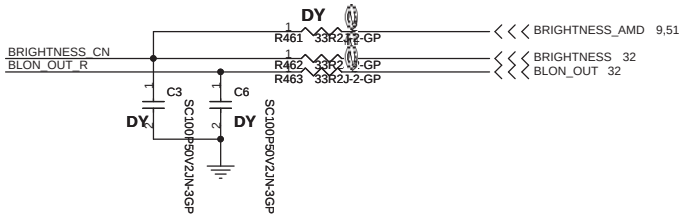


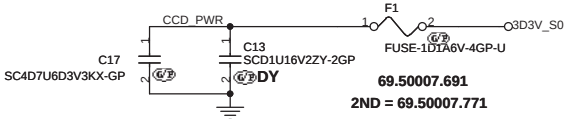
DMIC Pin	
Pin	Symbol
1	3D3V_S0
2	DMIC_CLK
3	DMIC_DAT
4	GND











SJM50

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD CONN

Size	Document Number	Rev
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Date: Tuesday, December 23, 2008 Sheet 18 of 56

Layout Note:
Place these resistors close to the CRT-out connector

UMA RN41 *Close to GPU card*
GMCH_RED 9
GMCH_GREEN 9
GMCH_BLUE 9
SRN0J-7-GP

Ferrite bead impedance: 10 ohm@100MHz

51 CRT_RED — FCB1608CF-GP — CRT_R
68.00230.021 L1 2nd = 68.00119.081
51 CRT_GREEN — FCB1608CF-GP — CRT_G
68.00230.021 L2 2nd = 68.00119.081
51 CRT_BLUE — FCB1608CF-GP — CRT_B
68.00230.021 L3 2nd = 68.00119.081

R39 150R2F-1-GP
R33 150R2F-1-GP
R26 150R2F-1-GP
R25 140R2F-GP
DIS UMA

C44 C47 C52 SC3P50V2CN-1-GP DY
C45 C50 C51 SC5D6P50V2CN-1GP

SA_20081030

Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

5V_S0
CRT_R 3 — D2 DY — BAV99PT-GP-U
CRT_G 3 — D3 DY — BAV99PT-GP-U
CRT_B 3 — D4 DY — BAV99PT-GP-U

Hsync & Vsync level shift

For System CRT

5V_S0
C31 SCD1U16V2ZY-2GP
U2A TSAHCT125PW-GP
2nd = 73.74125.L12
U2B TSAHCT125PW-GP

DIS
51,54 M92_HSYNC
51,54 M92_VSYNC
RN42 SRN0J-10-GP-U
HSYNC_1
VSYNC_1
CRT_HSYNC1_1
CRT_VSYNC1_1
RN3 SRN33J-9-GP-U
CRT_HSYNC1
CRT_VSYNC1

UMA
9 GMCH_VSYNC
9 GMCH_HSYNC
RN40 SRN0J-10-GP-U

DDC_CLK & DATA level shift

2ND = 69.50007.771
69.50007.691
3D3V_S0
5V_CRT_S0
5V_S0
D11 CH551H-30PT-GP
83.R5003.C8F
2ND = 83.R5003.H8H
F3 FUSE-1D1A6V-4GP-U
5V_CRT_DDC
RN2 SRN2K2J-1-GP
RN45 SRN10KJ-6-GP
U32 2N7002EDW-GP
CRT_DEC#
DAT_DDC1_5
CLK_DDC1_5

DIS
51 M92_CRT_DAT
51 M92_CRT_CLK
RN53 SRN0J-10-GP-U
DAT_DDC1_5_Q
9 NB_CRT_CLK
9 NB_CRT_DAT
CLK_DDC1_5_Q
UMA RN54 SRN0J-10-GP-U

84.27002.F3F
2ND = 84.27002.G3F

CRT I/F & CONNECTOR

6 1 7 2 8 3 9 4 10 5

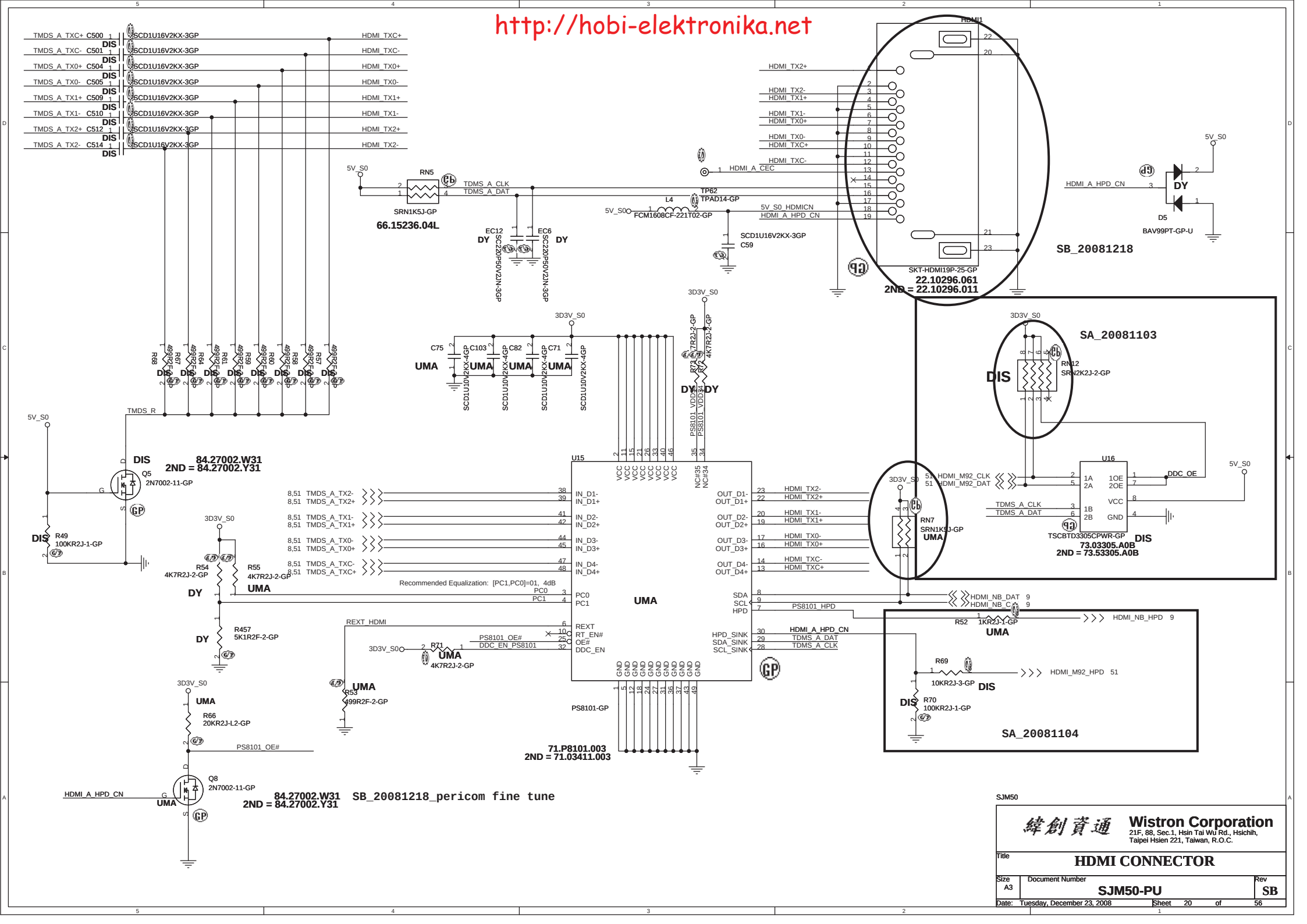
CRT1
NP1 NP2
CRT_R CRT_G CRT_B
DAT_DDC1_5
SC100P50V2JN-3GP C43 DY
CRT_HSYNC1
5V_CRT_S0
CRT_VSYNC1
CLK_DDC1_5
C488 SCD01U50V2KX-1GP
C28 SC100P50V2JN-3GP DY
HEO-15-110-GP
20.20768.015

32 CRT_DEC# — R14 470R2J-2-GP — CRT_IN#_R
C22 SC100P50V2JN-3GP
5V_S0
D1 DY — BAV99PT-GP-U

SJM50

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

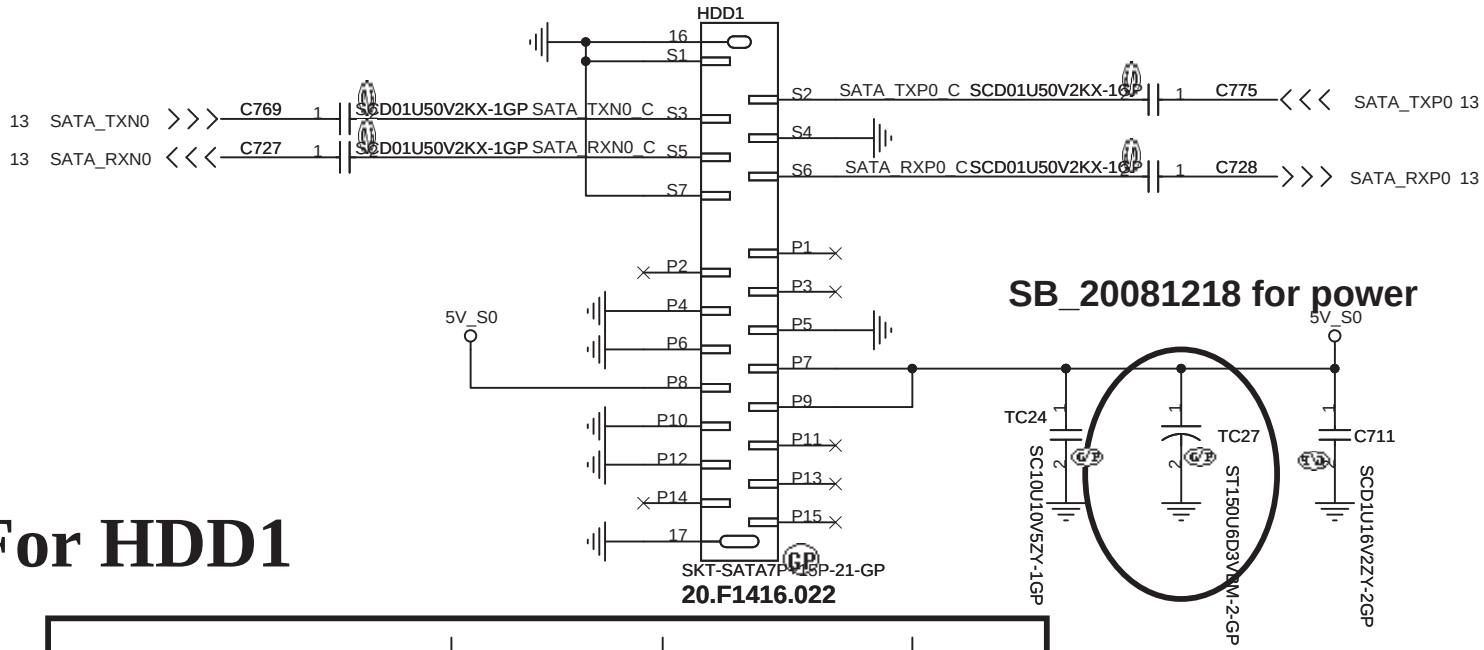
Title: **CRT CONN**
Size | Document Number: **SJM50-PU** | Rev: SB
Date: Tuesday, December 23, 2008 Sheet 19 of 56



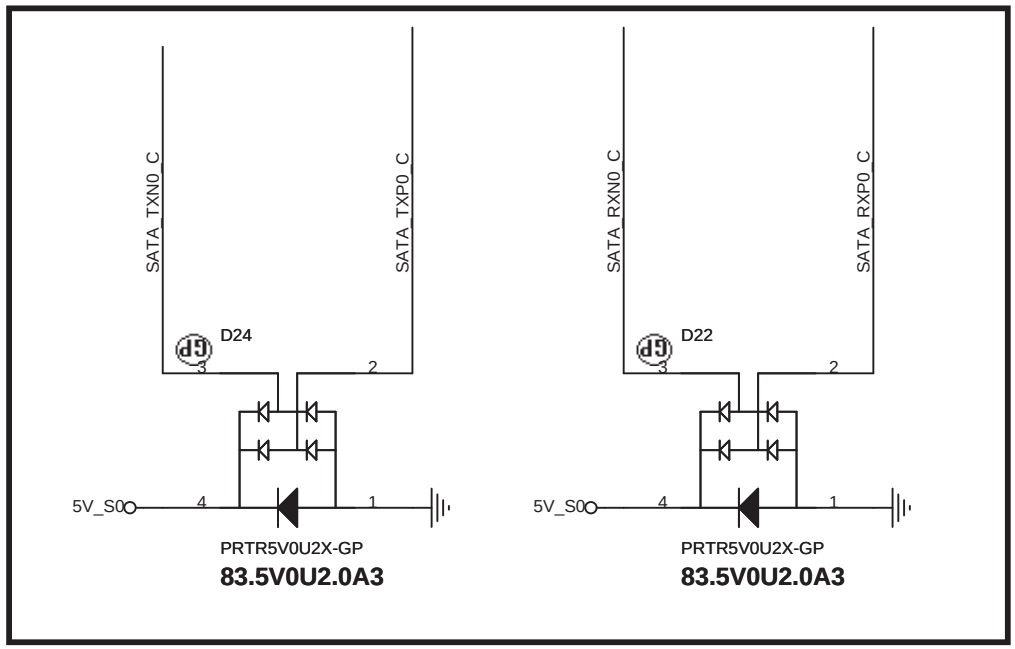
SJM50

Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: HDMI CONNECTOR	
Size: A3	Document Number: SJM50-PU
Rev: SB	
Date: Tuesday, December 23, 2008	Sheet 20 of 56

SATA Connector



For HDD1

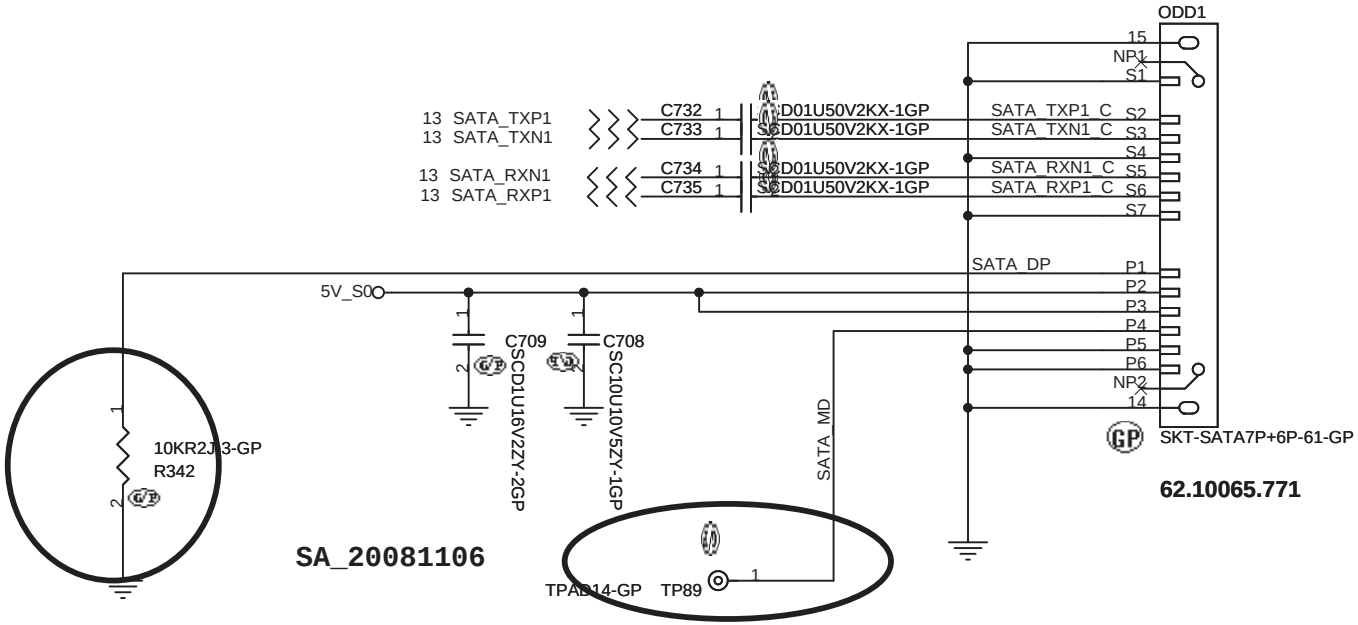


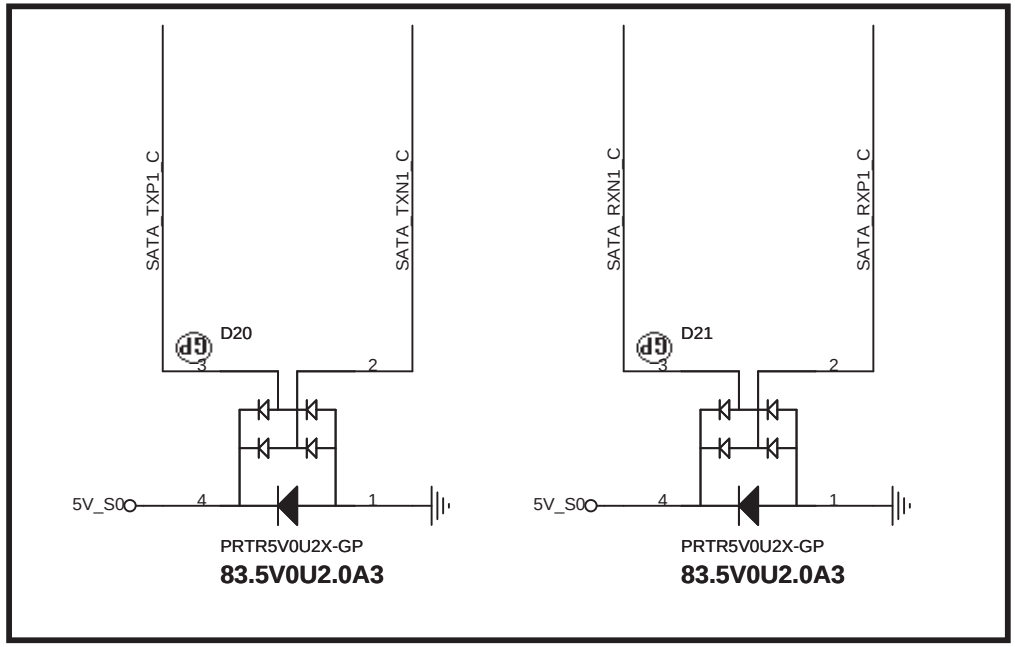
SJM50

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***HDD CONN***	
Size	Document Number **SJM50-PU**	Rev SB
Date: Tuesday, December 23, 2008	Sheet 21 of 56	

ODD Connector





For ODD1

SA_20081112

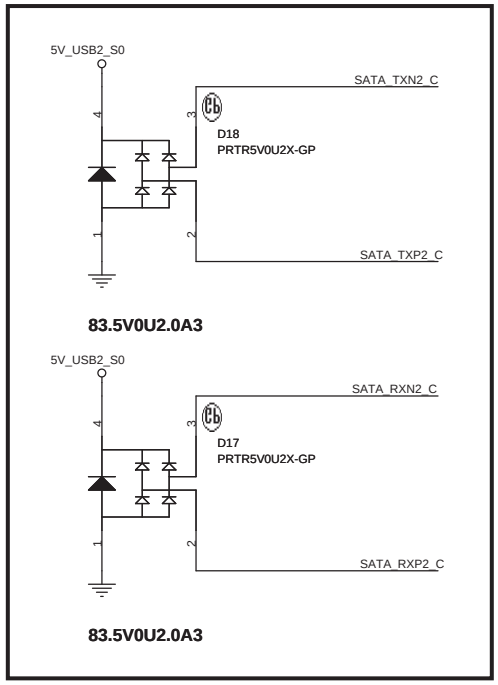
SJM50

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

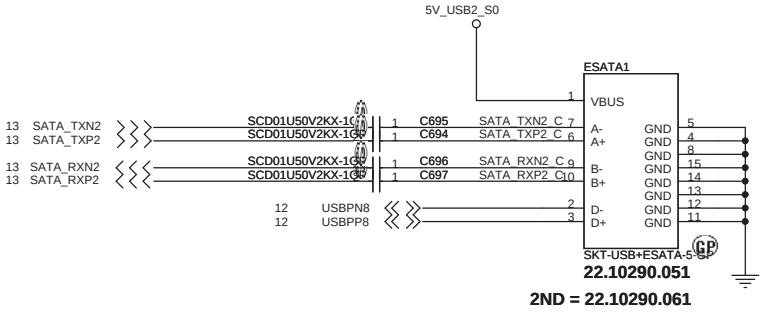
Title: ODD

Size | Document Number: SJM50-PU | Rev: SB

Date: Tuesday, December 23, 2008 | Sheet 22 of 56



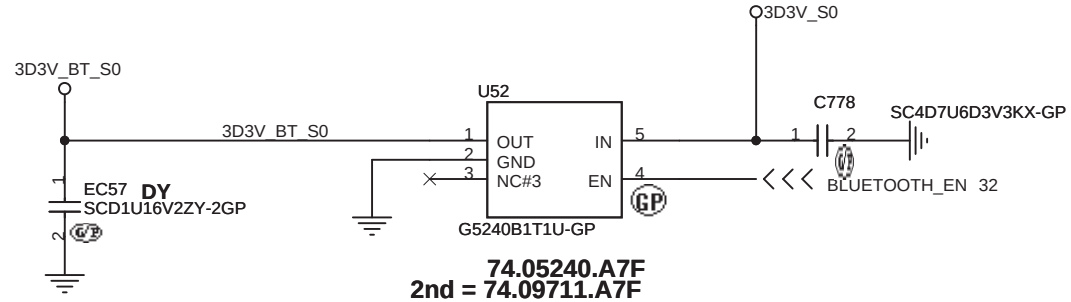
SA_20081111



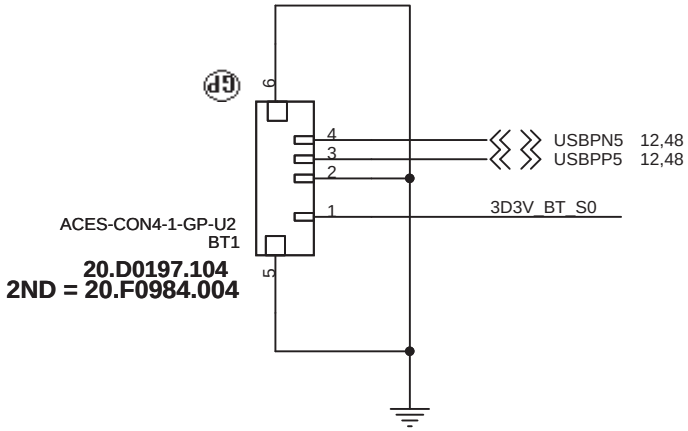
SJM50

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ESATA		
Size: A3	Document Number: SJM50-PU	Rev: SB
Date: Tuesday, December 23, 2008	Sheet 23 of 56	

BLUETOOTH MODULE



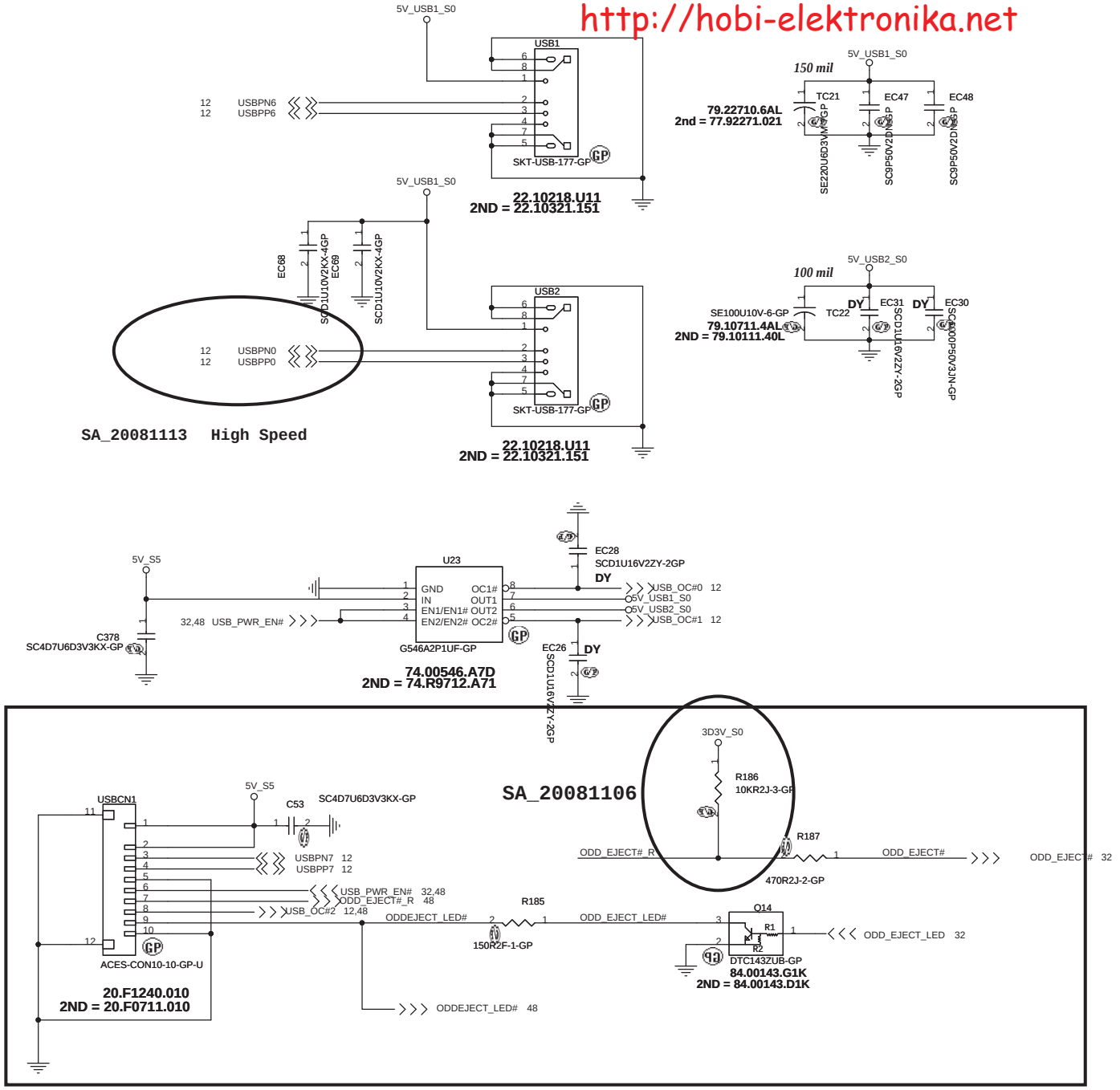
EC20 put near
BLUE1 / all
USB put one
choke near
connector by
EMI request



SJM50

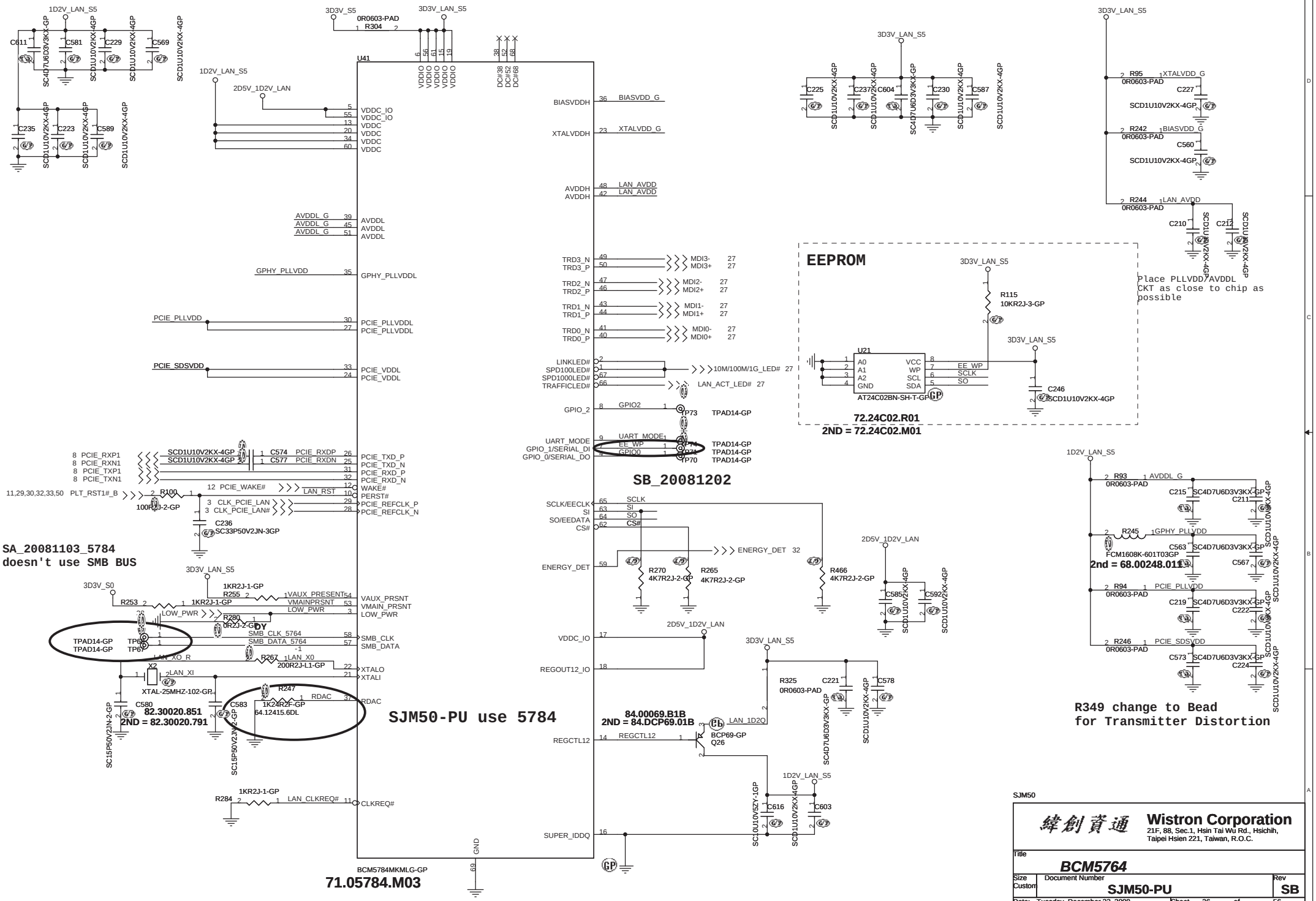
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***BLUETOOTH***		
Size	Document Number: **SJM50-PU**	Rev: SB
Date: Tuesday, December 23, 2008	Sheet 24 of 56	



SJM50

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*USB CONN*
Size	Document Number: SJM50-PU — Rev: SB
Date: Tuesday, December 23, 2008	Sheet 25 of 56



SJM50

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BCM5764

Size	Document Number	Rev
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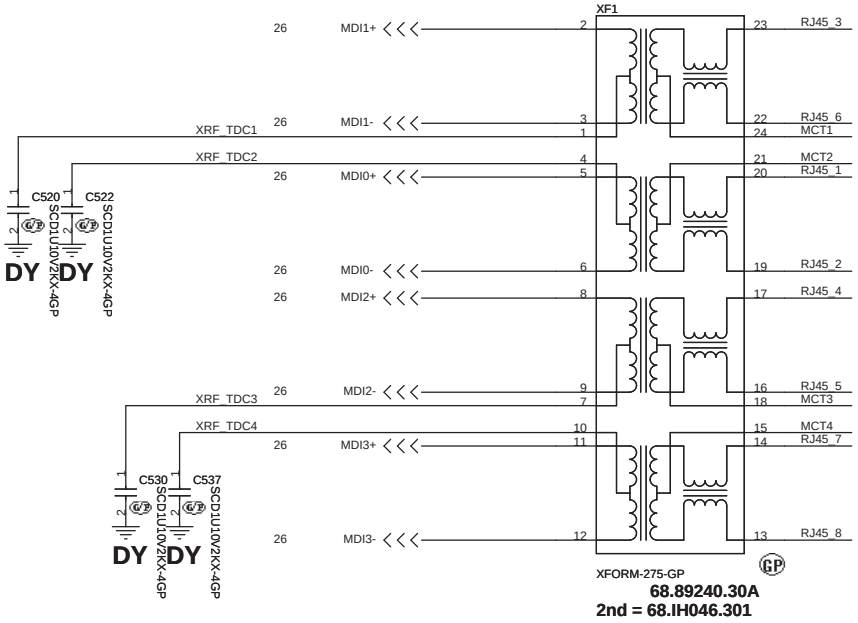
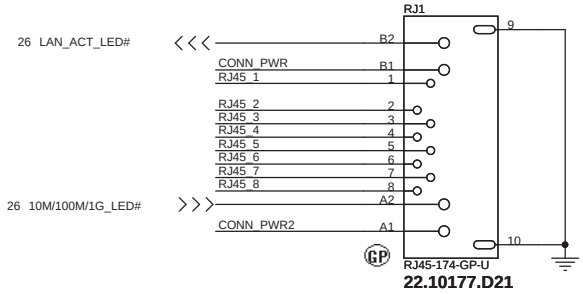
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

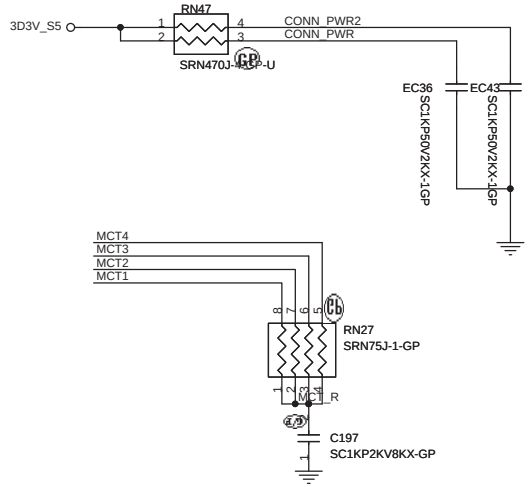
LAN Connector

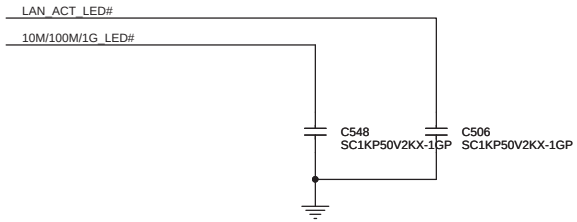
LAN Connector

GIGA Lan Transformer







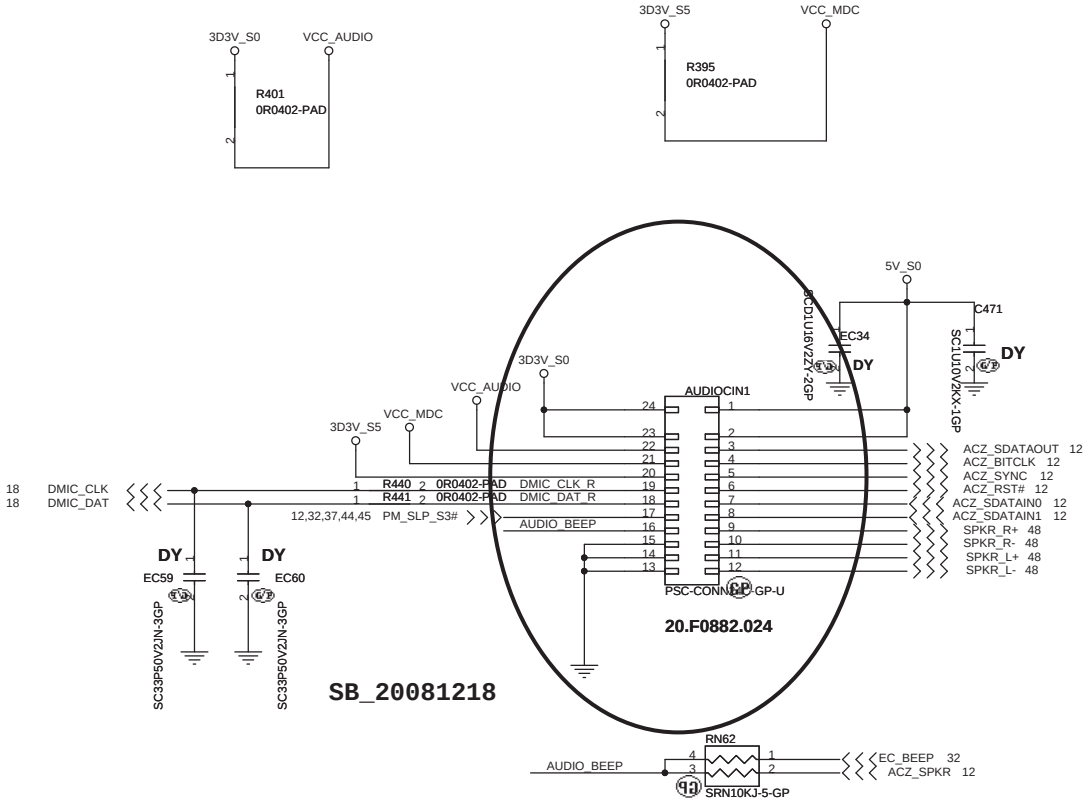


SJM50

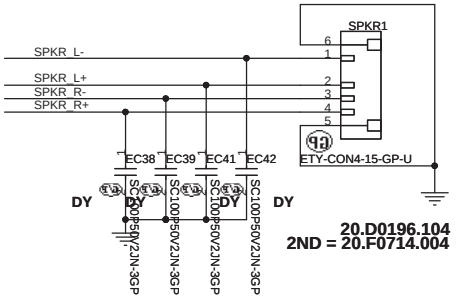
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN CONN		
Size: A3	Document Number: SJM50-PU	Rev: SB
Date: Wednesday, December 24, 2008	Sheet 27 of 56	

AUDIO CONN.

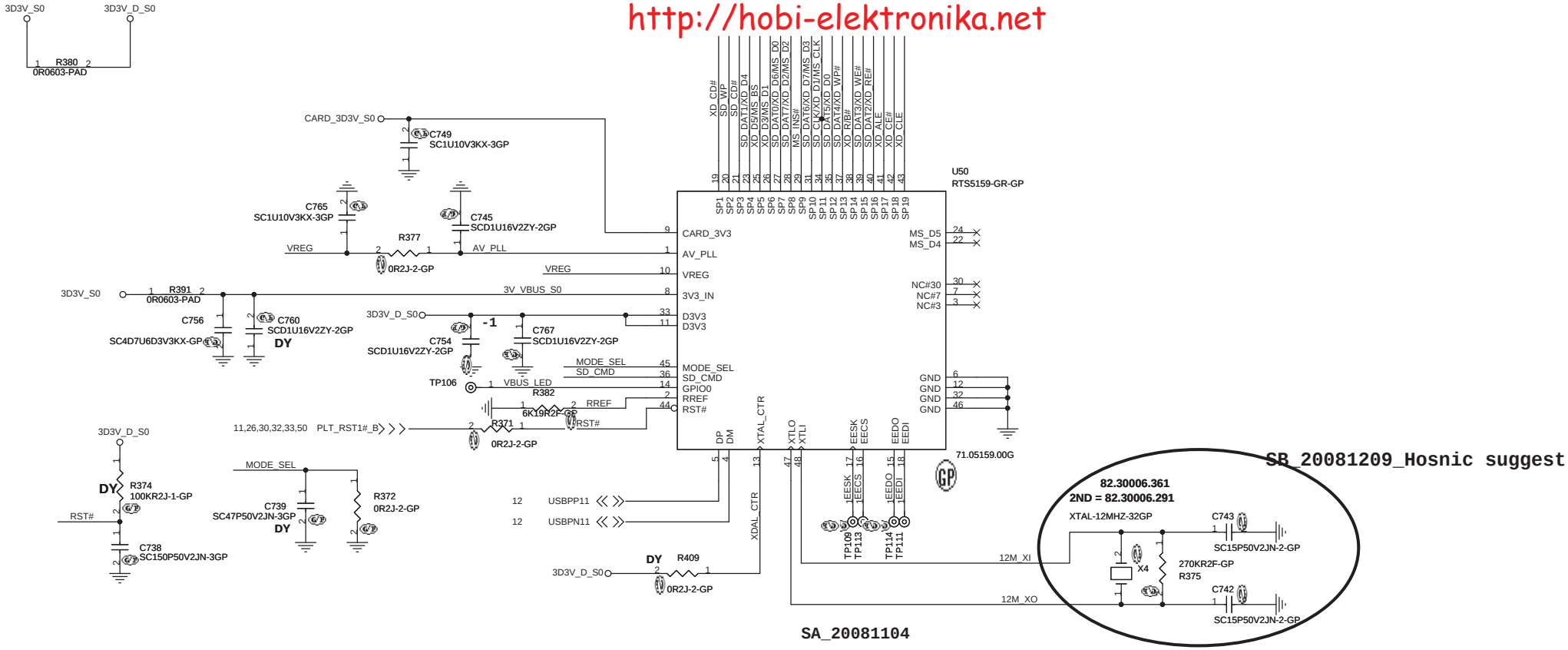


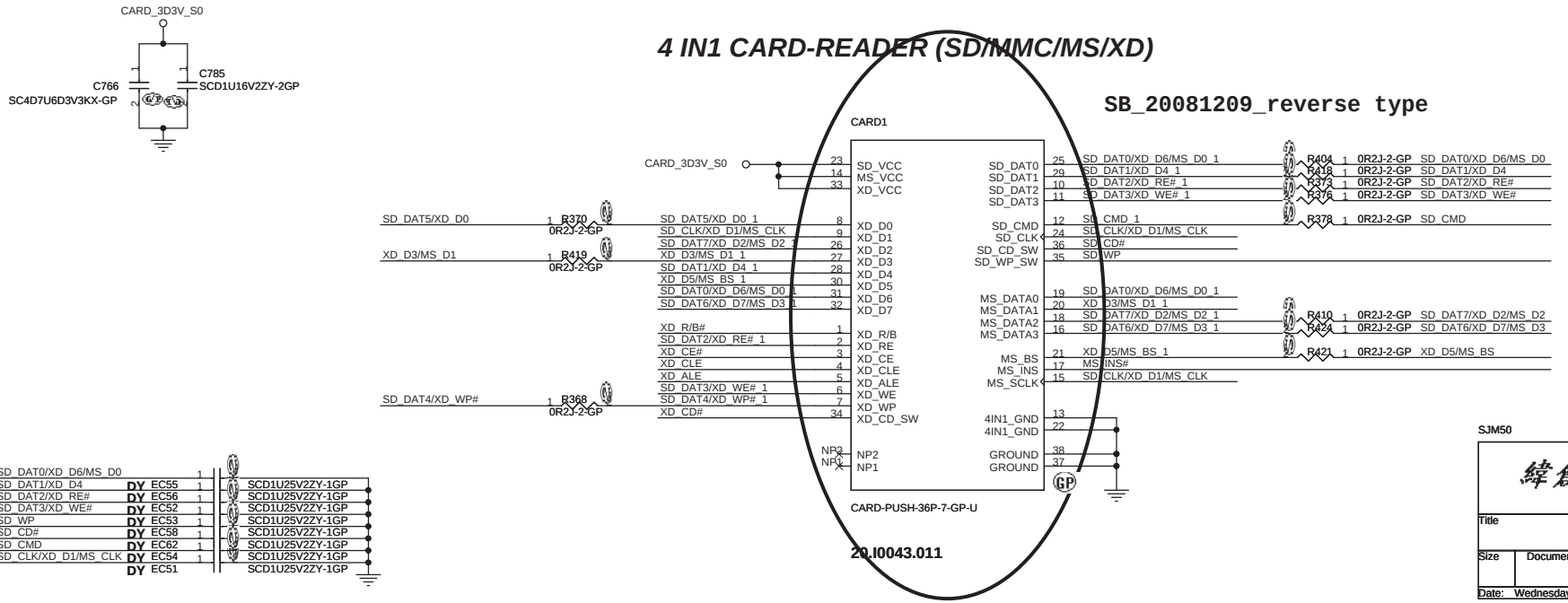
Internal Speaker



SJM50

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*AUDIO AMP AND CONN.*
Size	Document Number: SJM50-PU — Rev: SB
Date: Wednesday, December 24, 2008	Sheet 28 of 56

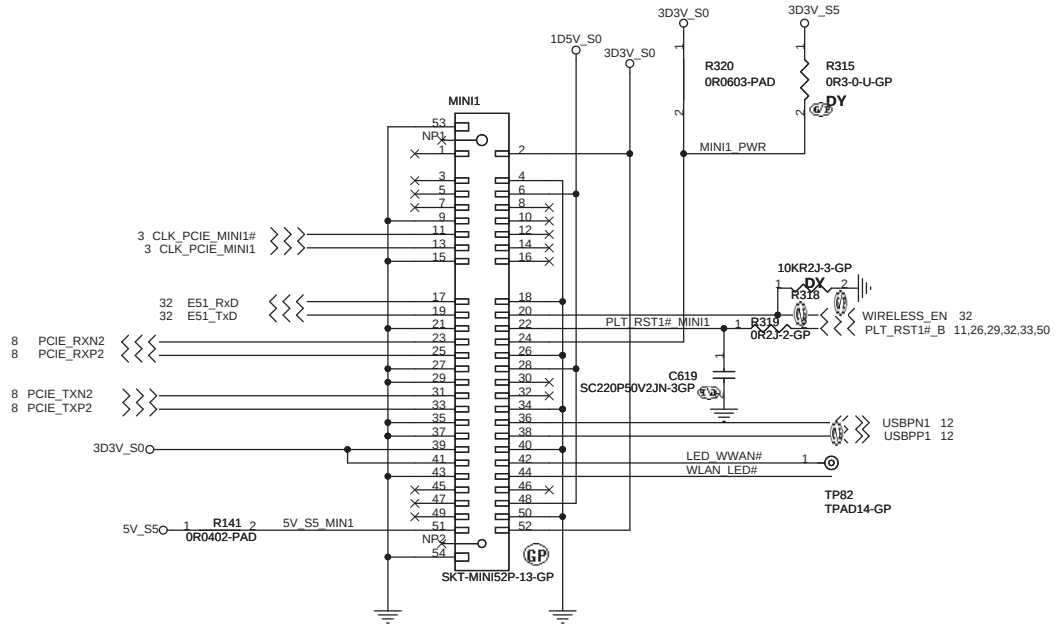




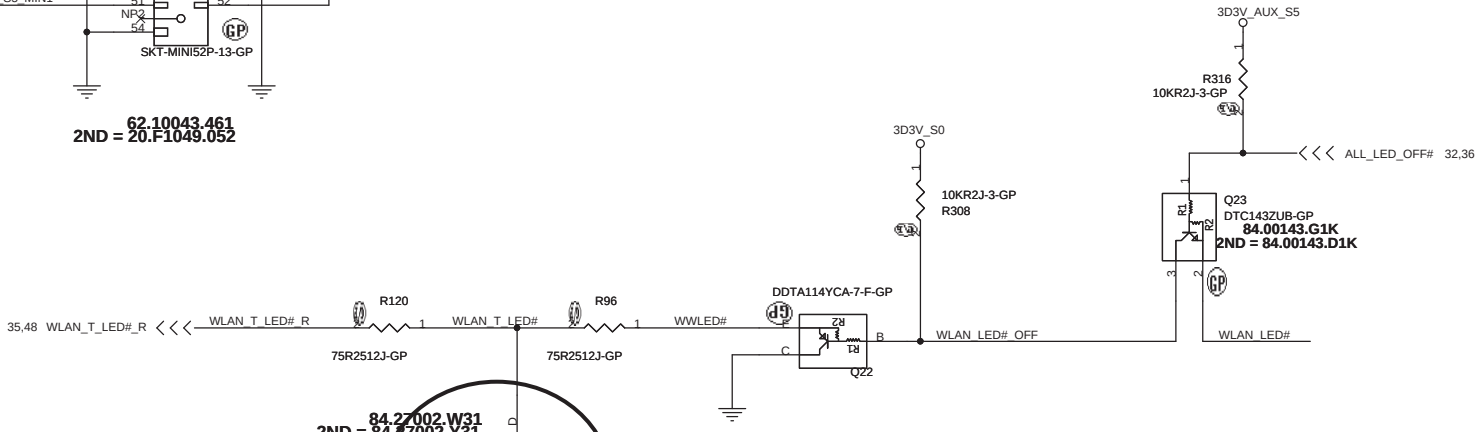
SJM50

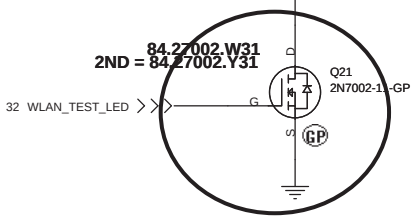
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*Cardreader_RTS5159*	
Size	Document Number: SJM50-PU	Rev: SB
Date: Wednesday, December 24, 2008	Sheet 29 of 56	

Mini Card Connector(WLAN)



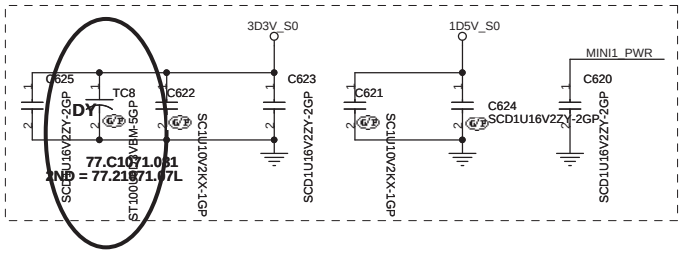
62.10043.461
2ND = 20.F1049.052





SA_20081104

Place near MINI1



SA_20081111

SJM50

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MINI CARD		
Size: A3	Document Number: SJM50-PU	Rev: SB
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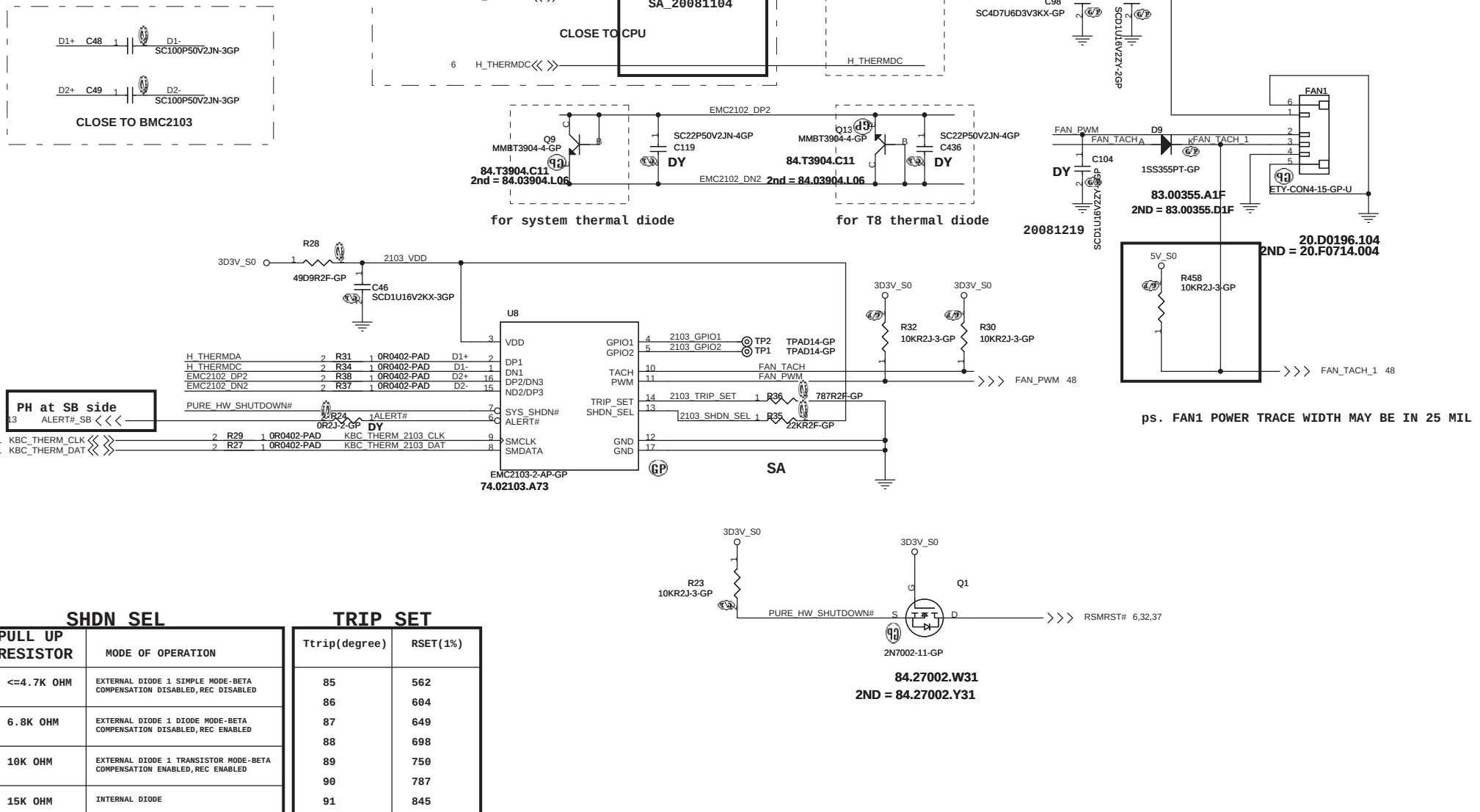
CPU TEMP:

H_THERMDA and H_THERMDC routing 10mil trace width and spacing. Locate Capacity near thermal diode

for CPU thermal diode

C587 for EMI and solve acoustic noise



ps. FAN1 POWER TRACE WIDTH MAY BE IN 25 MIL

SHDN SEL

PULL UP RESISTOR	MODE OF OPERATION
<=4.7K OHM	EXTERNAL DIODE 1 SIMPLE MODE-BETA COMPENSATION DISABLED,REC DISABLED
6.8K OHM	EXTERNAL DIODE 1 DIODE MODE-BETA COMPENSATION DISABLED,REC ENABLED
10K OHM	EXTERNAL DIODE 1 TRANSISTOR MODE-BETA COMPENSATION ENABLED,REC ENABLED
15K OHM	INTERNAL DIODE
22K OHM	EXTERNAL DIODE 2 TRANSISTOR MODE-BETA COMPENSATION ENABLED,REC ENABLED
>=33K OHM	EXTERNAL DIODE 1 TRANSISTOR MODE-BETA COMPENSATION ENABLED,REC ENABLED

TRIP SET

Ttrip(degree)	RSET(1%)
85	562
86	604
87	649
88	698
89	750
90	787
91	845
92	909
93	953
94	1020
95	1100

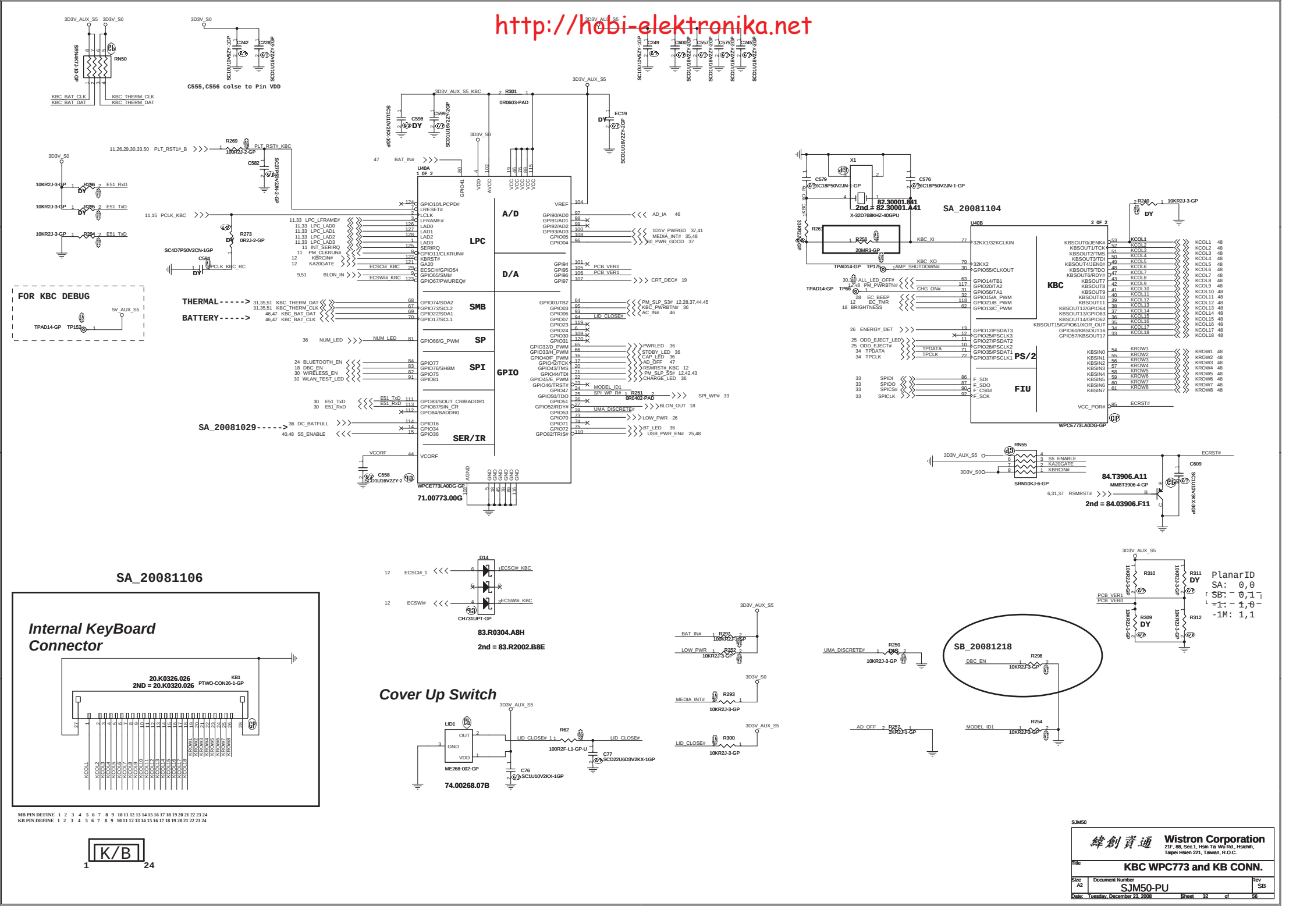
SJM50

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor

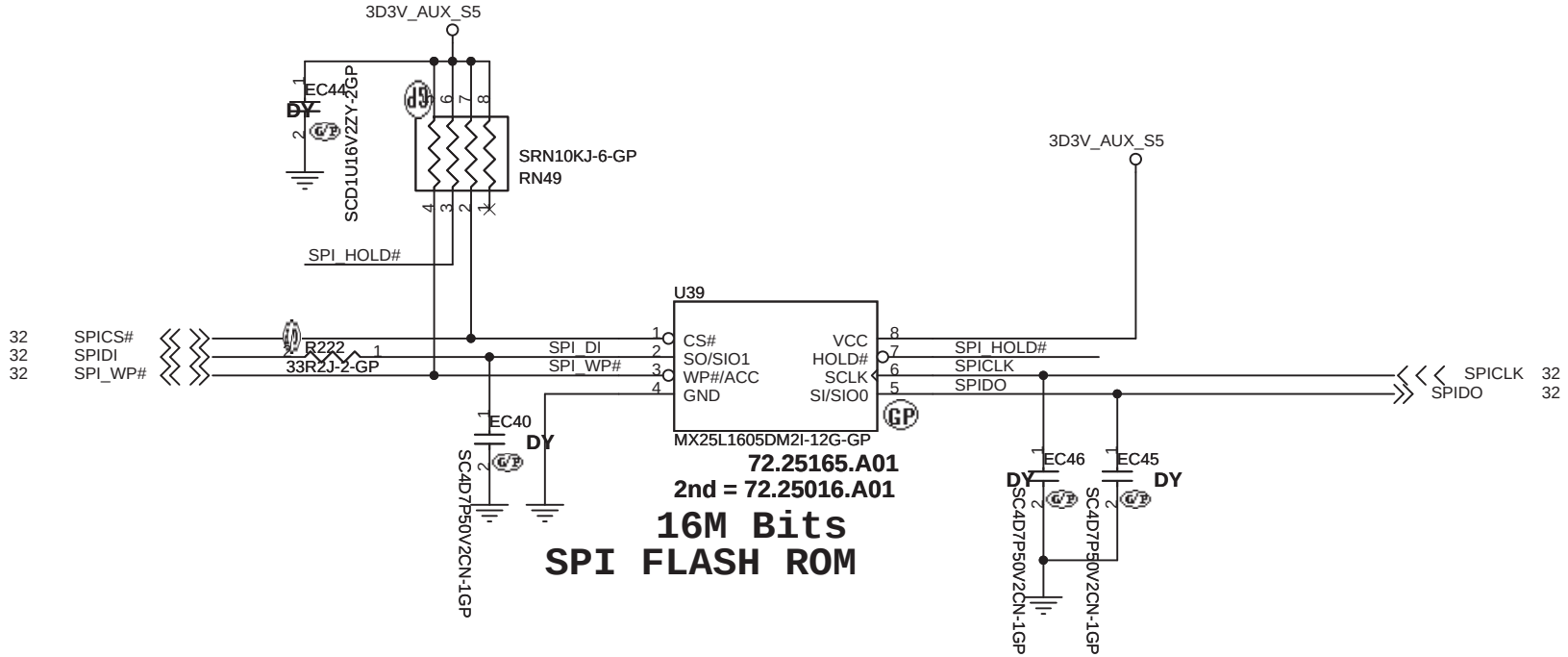
Size | Document Number: SJM50-PU | Rev: SB

Date: Wednesday, December 24, 2008 Sheet 31 of 56

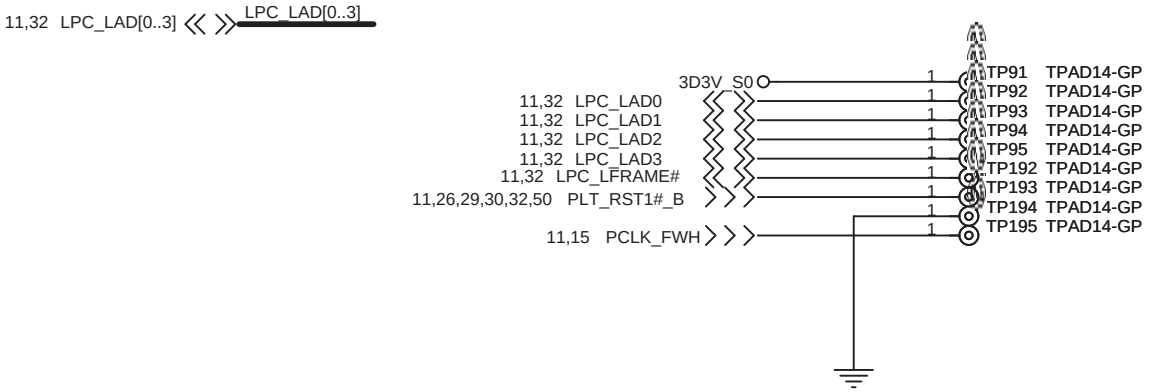


SJM50

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**KBC WPC773 and KB CONN.**	
Size: A2	Document Number: SJM50-PU	Rev: SB
Date: Tuesday, December 23, 2008	Sheet 32 of 56	



GOLDEN FINGER FOR DEBUG BOARD

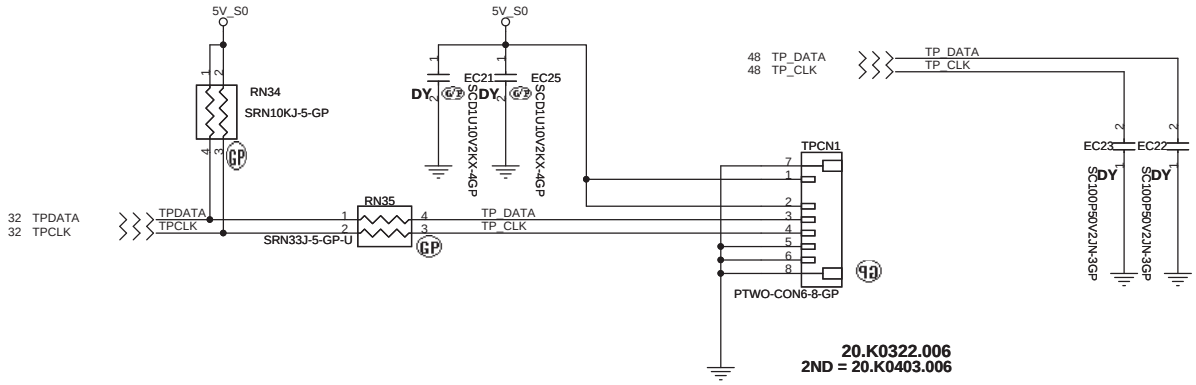


SJM50

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

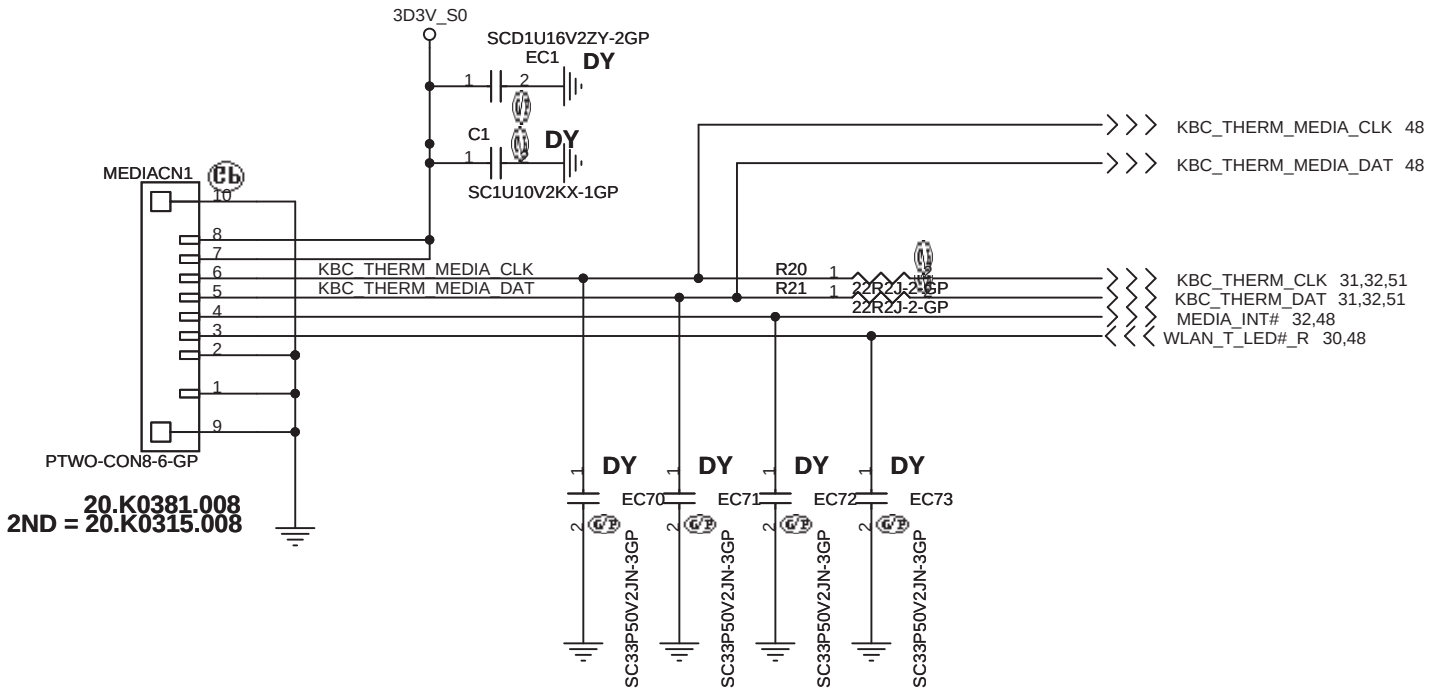
Title	***BIOS***	
Size	Document Number **SJM50-PU**	Rev SB
Date: Tuesday, December 23, 2008	Sheet 33 of 56	

TOUCH PAD



SJM50

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Touch PAD*		
Size	Document Number: SJM50-PU	Rev: SB
Date: Tuesday, December 23, 2008	Sheet 34 of 56	



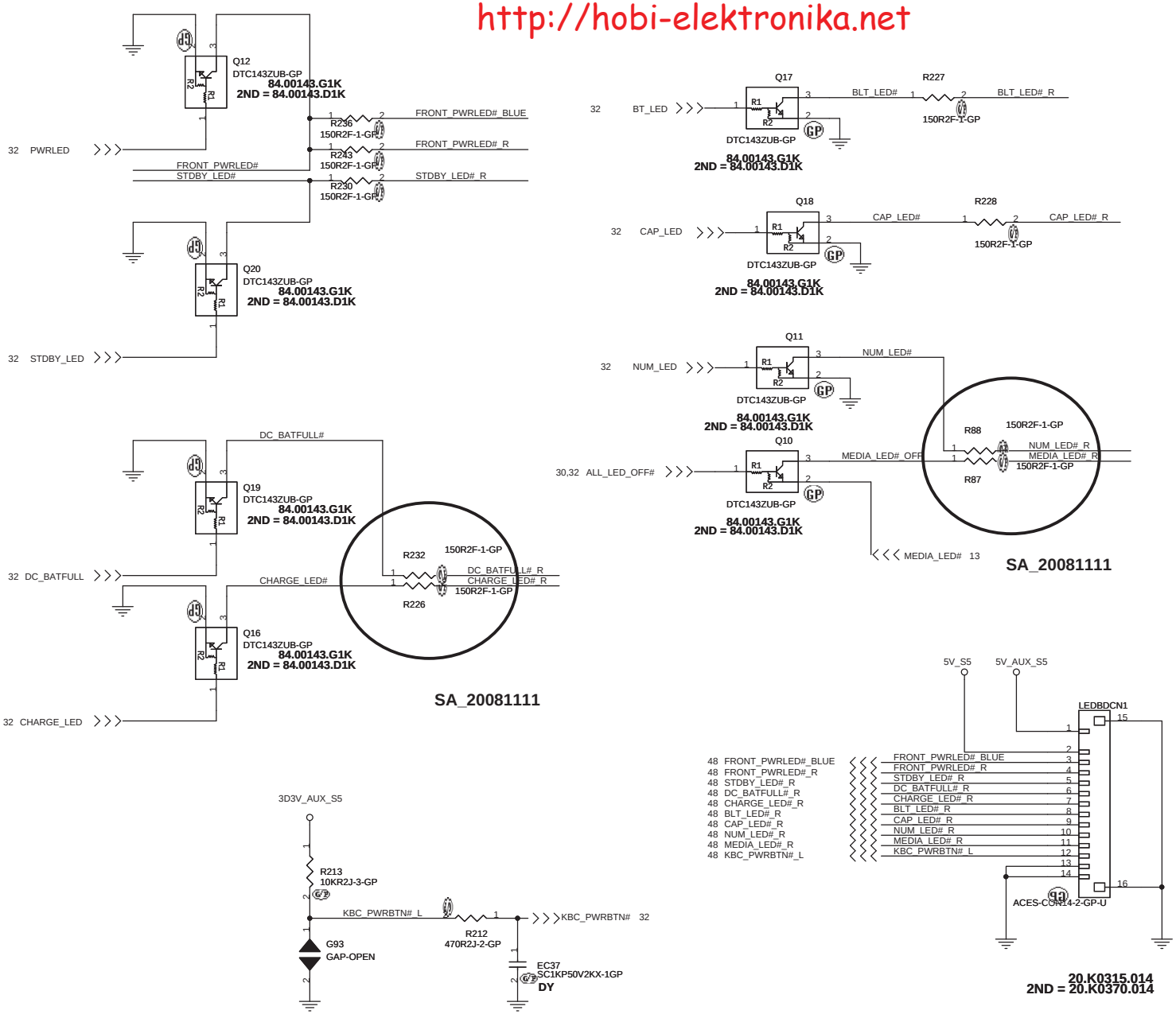
SJM50

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***MEDIA BD CONN***

Size	Document Number	Rev
	SJM50-PU	SB

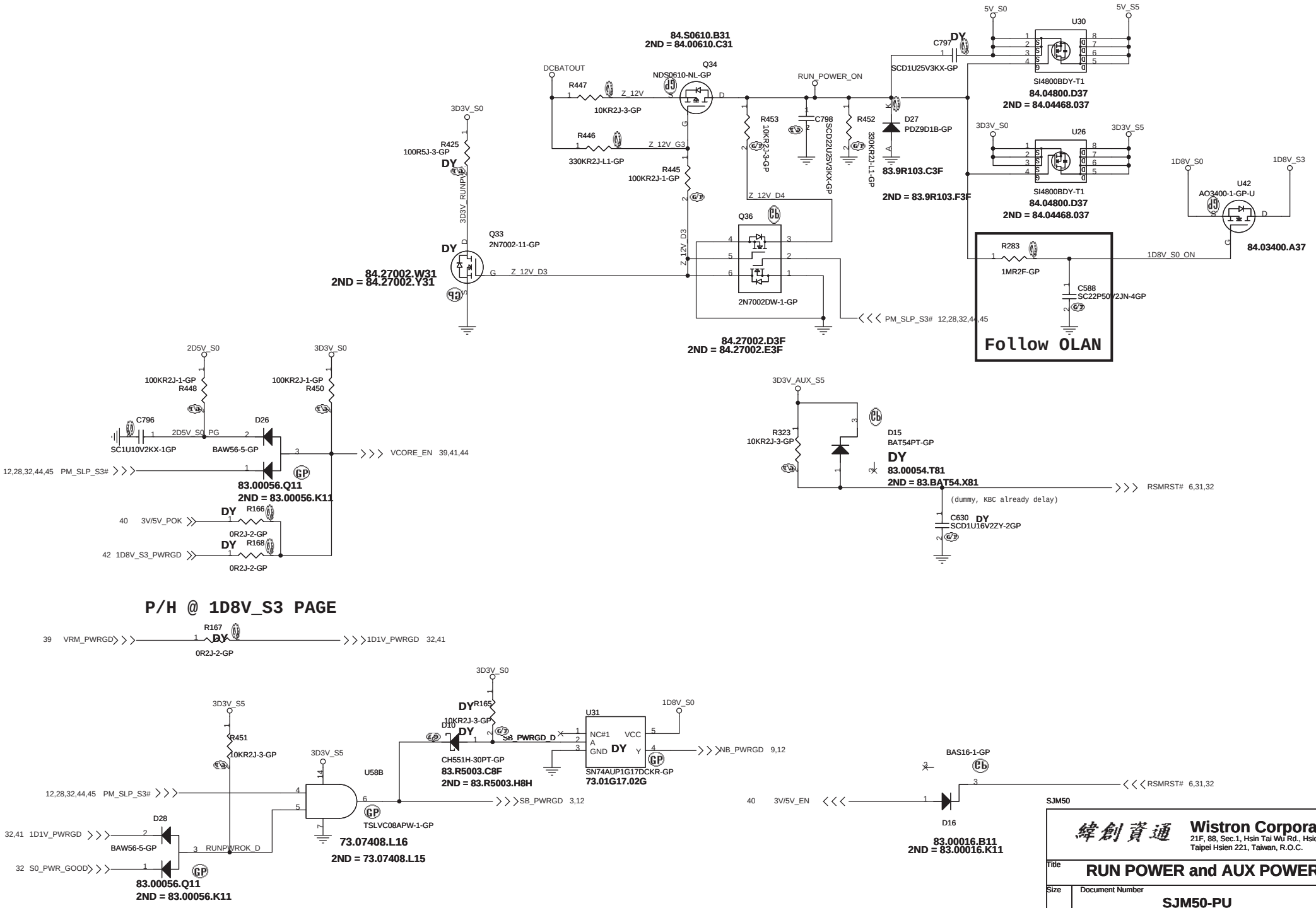
Date: Tuesday, December 23, 2008 Sheet 35 of 56



SJM50

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**LED**
Size	Document Number: **SJM50-PU** — Rev: SB
Date: Wednesday, December 24, 2008	Sheet 36 of 56

Run Power



SJM50

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **RUN POWER and AUX POWER**

Size	Document Number	Rev
	SJM50-PU	SB

Date: Wednesday, December 24, 2008 Sheet 37 of 56

CPU_CORE
ISL6266A

VID0
VID1
VID2
VID3
VID4
VID5
VID6

CPUCORE_ON

VCC_SENSE
VSS_SENSE

DCBATOUT_6266A
5V_S0
3D3V_S0

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)
VID6(I / 3.3V)

Input Signal
EN (I / 3.3V)

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

Input Power
VCC(I)
VCC(I)
VCC(I)

Output Signal
PGOOD

VGATE_PWRGD

Output Power
VCC_CORE_PWR(O)

VCC_CORE(Imax=38A)

TPS51125
5V/3D3V

DCBATOUT_51125

S5_ENABLE

ALW_PWRGD_3V_5V

Input Power
VIN

Input Signal
EN0

Output Signal
PGOOD

Output Power
5V(O)
3D3V(O)
5V(O)
3D3V(O)

5V_S5 (6A)
3D3V_S5 (6A)
5V_AUX_S5
3D3V_AUX_S5

RT9018A
1D5V_S0

1D8V_S3
PM_SLP_S3#

VIN
EN
1D5V(O)
PGOOD

1D5V_S0 (2.5A)
CPUCORE_ON

RT9026
0D9V_S0

5V_S5
1D8V_S3
PM_SLP_S4#

VIN
VLDOIN
S3
S5
VTT
VTTREF

0D9V_S3 (1A)
0D9V_S3_1

GFX_CORE
ISL6263A

VID0
VID1
VID2
VID3
VID4

5V_S0
DCBATOUT

PM_SLP_S3#
GFXVR_EN

VCC_AXG_SENSE
VSS_AXG_SENSE

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)

Input Power
VDD
VIN

Input Signal
VR_ON

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

Output Signal
PGOOD

CPUCORE_ON

Output Power
VGFXCORE (O)

VCC_GFXCORE(5.5A)

TPS51124
1D8V/1D05V

5V_S5
DCBATOUT_51124

PM_SLP_S4#
PM_SLP_S3#

CPUCORE_ON

Input Power
VDD
VCC

Input Signal
EN1
EN2

Output Signal
PGOOD1
PGOOD2

Output Power
1D8V (O)
1D05V(O)

1D8V_S3 (10A)
1D05V_S0 (15A)

Adapter

AD_OFF
AD_JK
5V_AUX_S5

Input Signal
(I)

Input Power
VCC(I)
VCC(I)

Output Signal
(O)

Output Power
VCC(O)

AD_IN#
AD+

Charger BQ24745

CHG_ON#
24750_CELLS

AD+

Input Signal
CHGEN#
CELLS

Input Power
ACN

Output Signal
ACGOOD#
SRSET

Output Power
VOUT (O)
VOUT (O)

AC_IN#
AD_IA

BT+
DCBATOUT

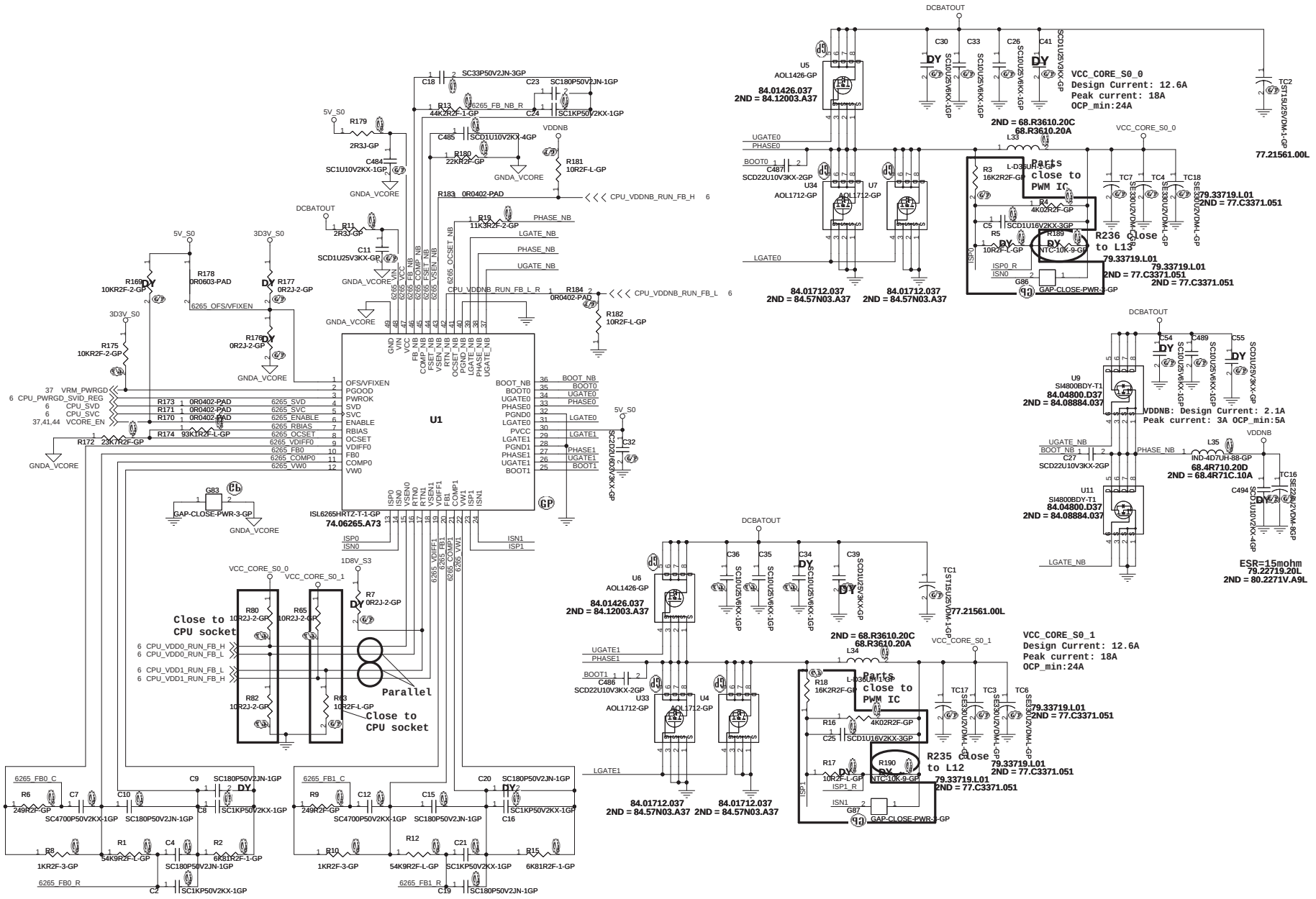
SJM50

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Sequence Logic

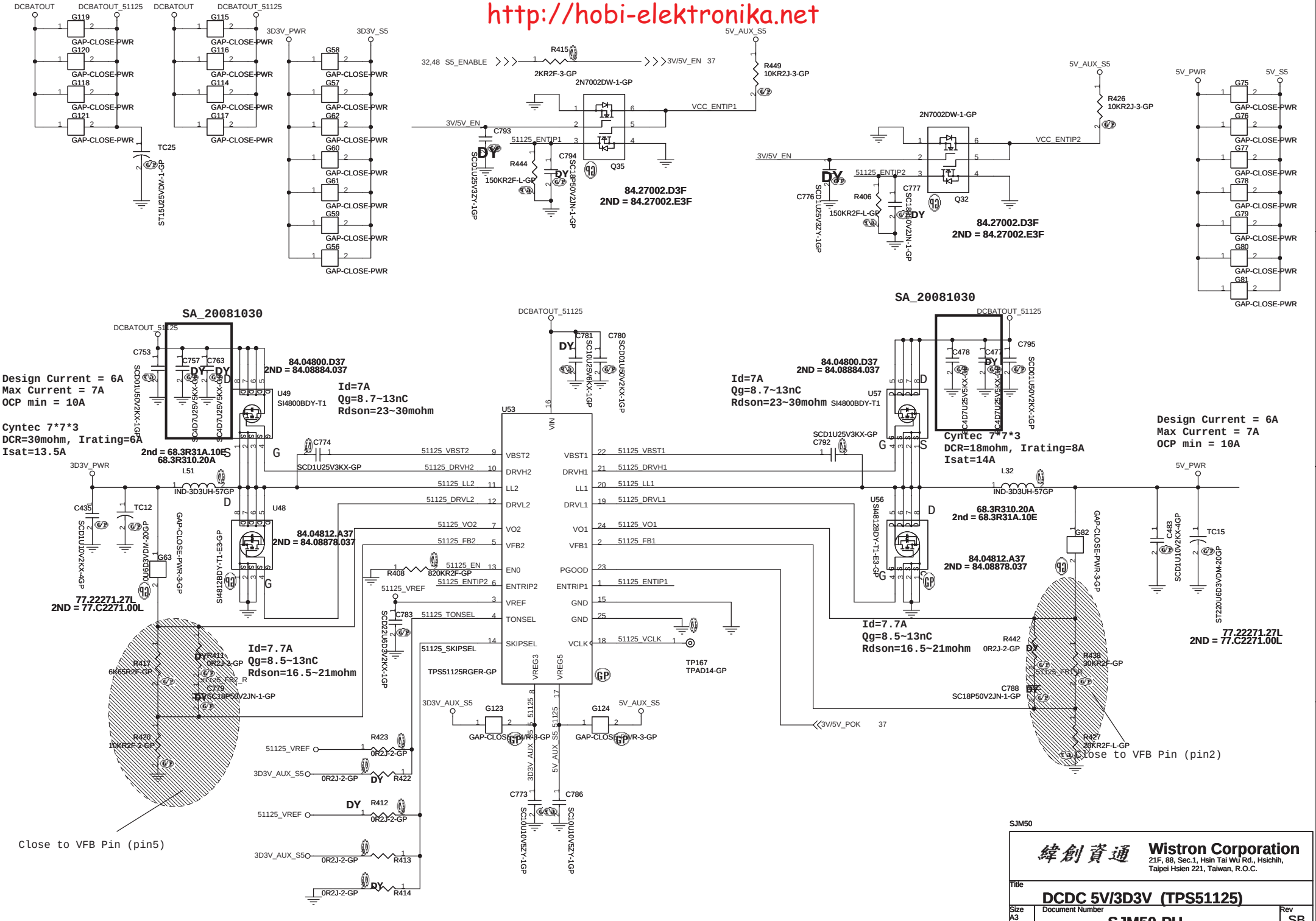
Size: B | Document Number: SJM50-PU | Rev: SB

Date: Friday, December 05, 2008 | Sheet 38 of 56



SJM50

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	CPU Vcore (ISL6265HR)	
Size: Custom	Document Number: SJM50-PU	Rev: SB
Date: Wednesday, December 24, 2008	Sheet 39 of 56	



SA_20081030

SA_20081030

SB_20081216

SA_20081030

Change 4.7u

Change 4.7u

Vtrip(mV)=Rtrip(Kohm)*10(uA)
Iocp=(Vtrip/Rdson)+((1/(2*L*f))*((Vin-Vout)*Vout)/Vin))

Iomax=8A
Vo(cal)=1.1060V

1D2V Iomax=5A
OCP>10A

Close to VFB Pin (pin5)

	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	**300k/CH1** **360k/CH2**	360k/CH1 420k/CH2

Vout=0.758V*(R1+R2)/R2 --> PWM mode
Vout=0.764V*(R1+R2)/R2 --> Skip Mode

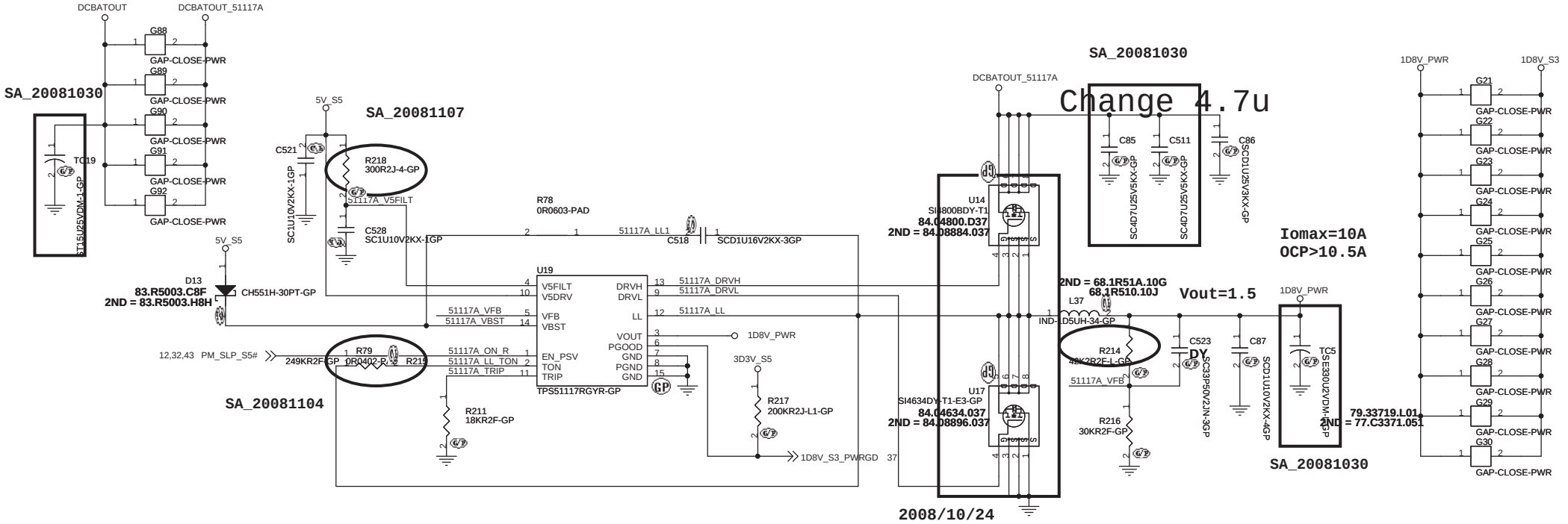
SJM50

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124 1D1V 1D2V

Size: A3 | Document Number: SJM50-PU | Rev: SB

Date: Wednesday, December 24, 2008 | Sheet 41 of 56

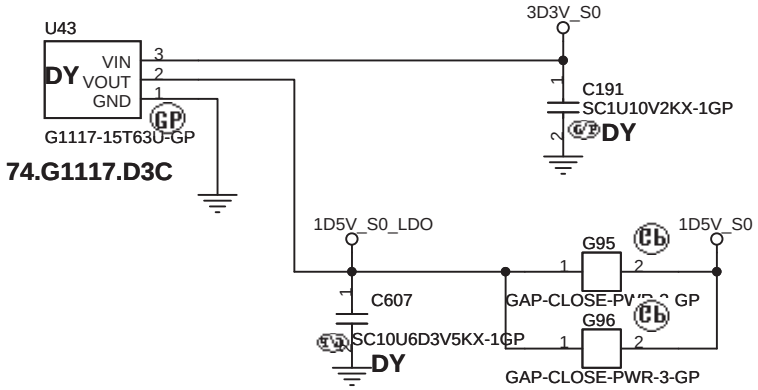


SJM50

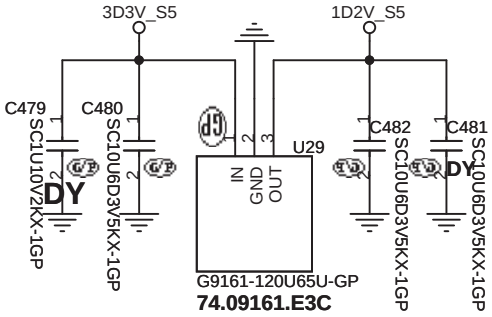
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *TPS51117 1D8V*		
Size: A3	Document Number: SJM50-PU	Rev: SB
Date: Wednesday, December 24, 2008	Sheet 42 of 56	

G1117

1D5V_S0
Iomax=1A

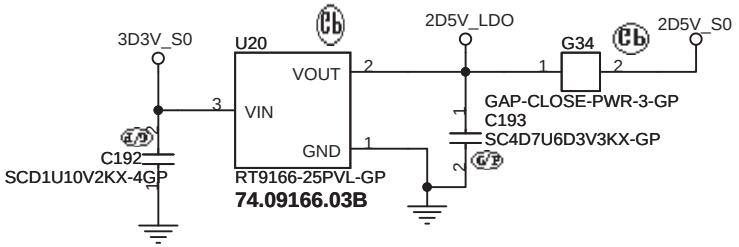


1D2V_S5
Iomax=400mA



Place near to SB700

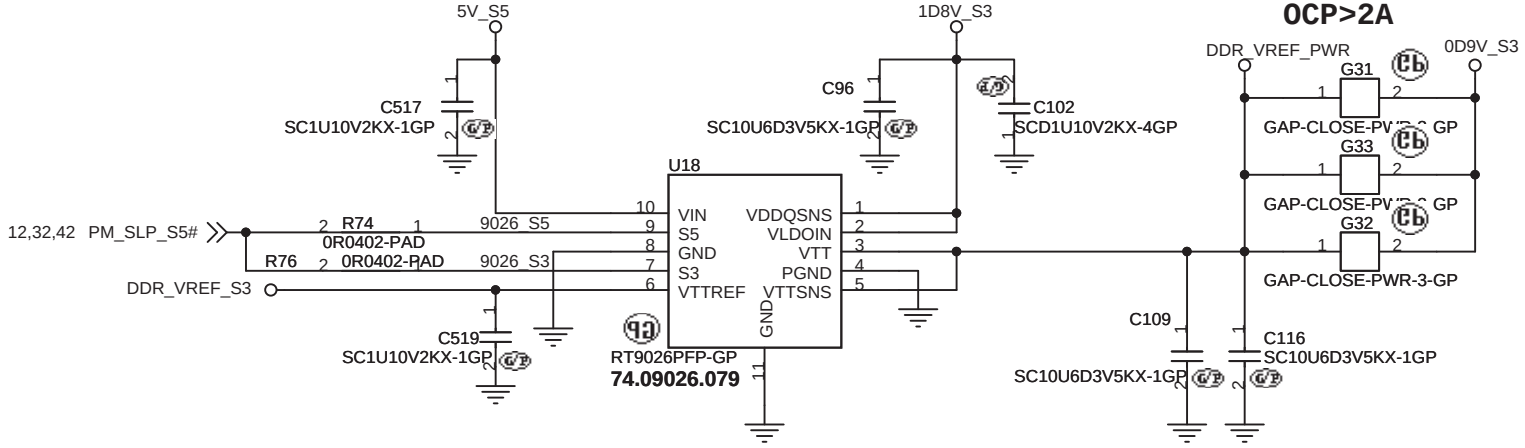
2D5V_S0
Iomax=0.3A 2D5V/300mA



Place near to CPU

Place near to Mini-card

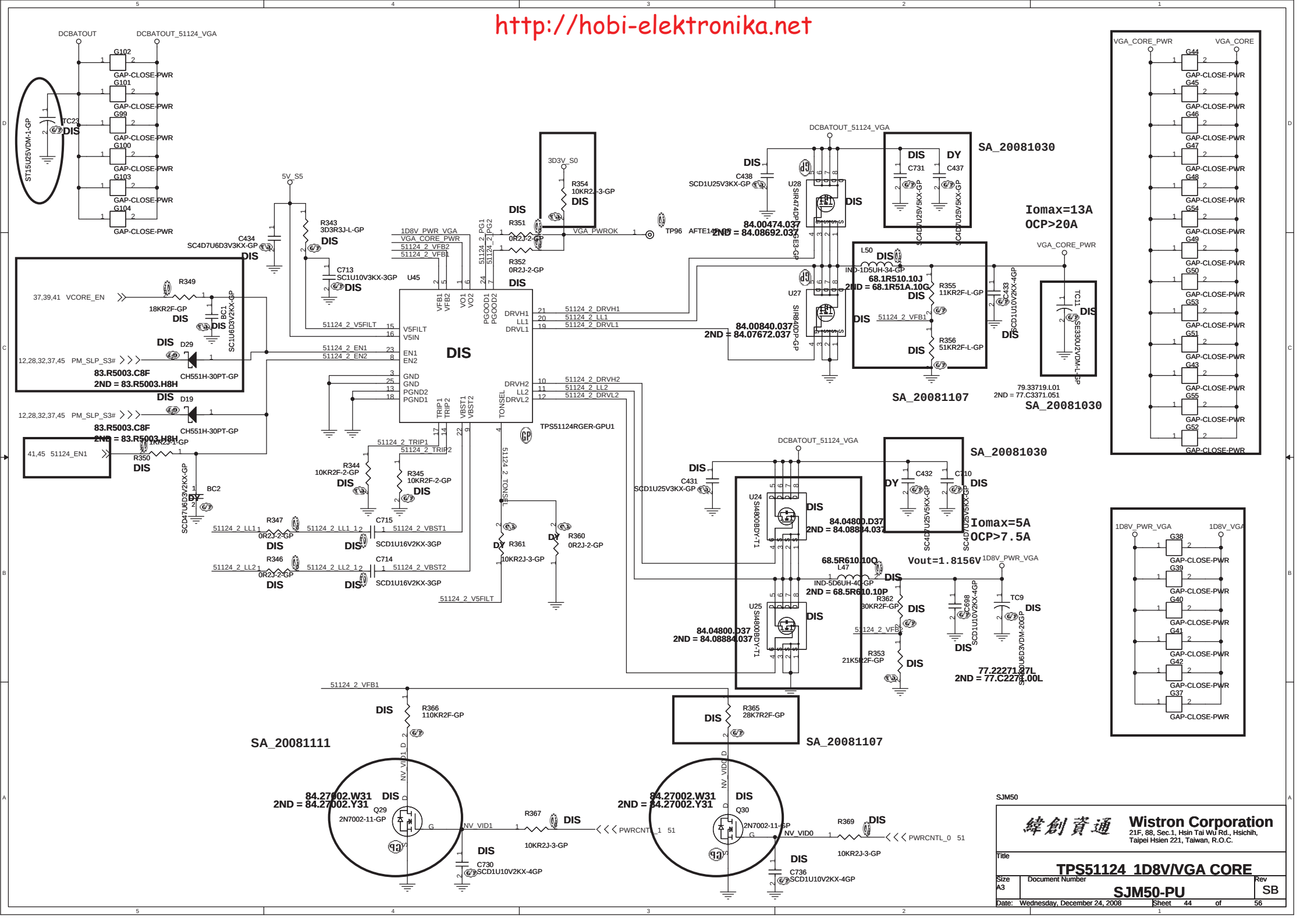
Iomax=1A
OCP>2A



Place near to Dimm

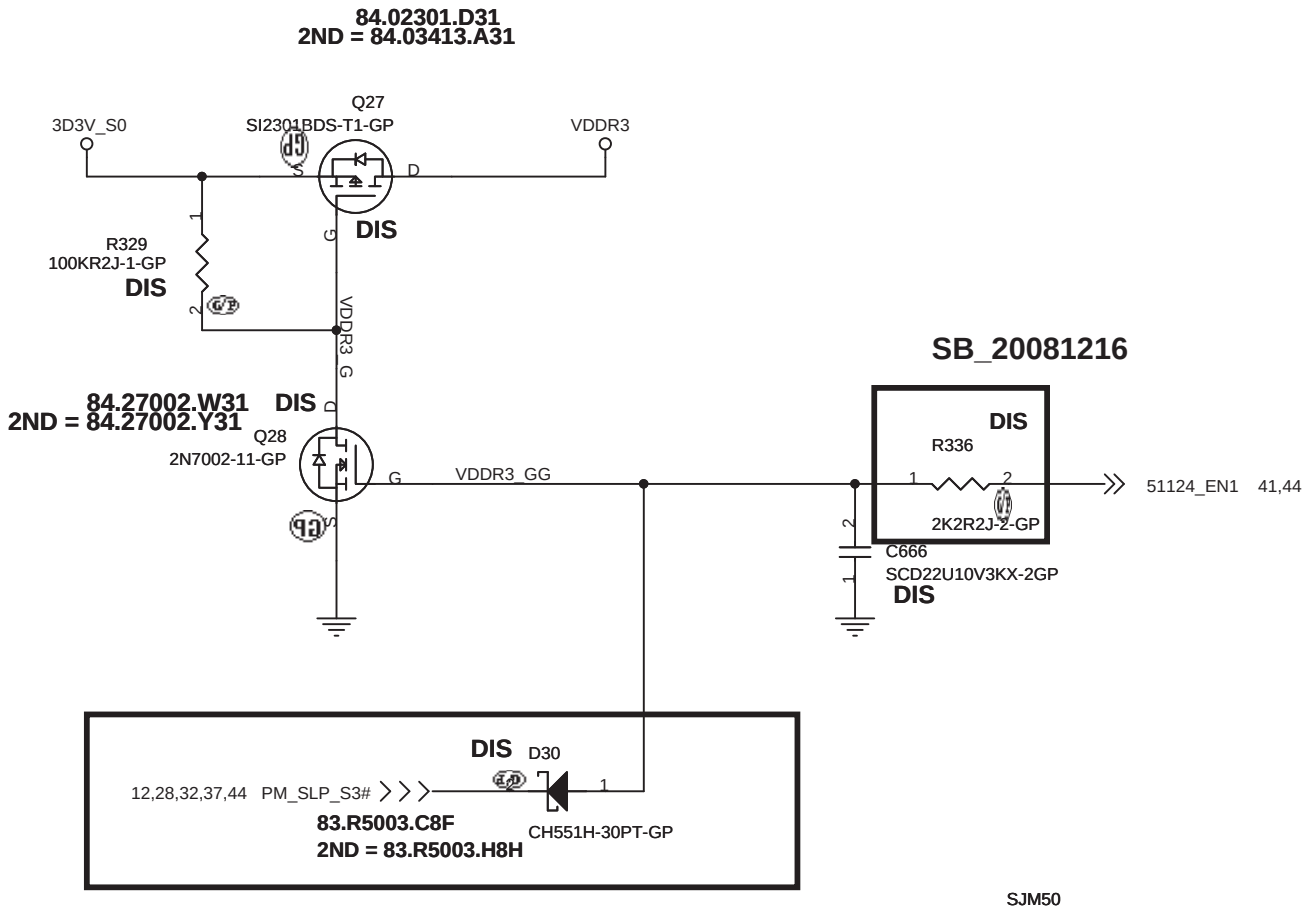
SJM50

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: 0D9V_2D5V_1D25V_1D5V		
Size: A4	Document Number: SJM50-PU	Rev: SB
Date: Tuesday, December 23, 2008	Sheet 43 of 56	



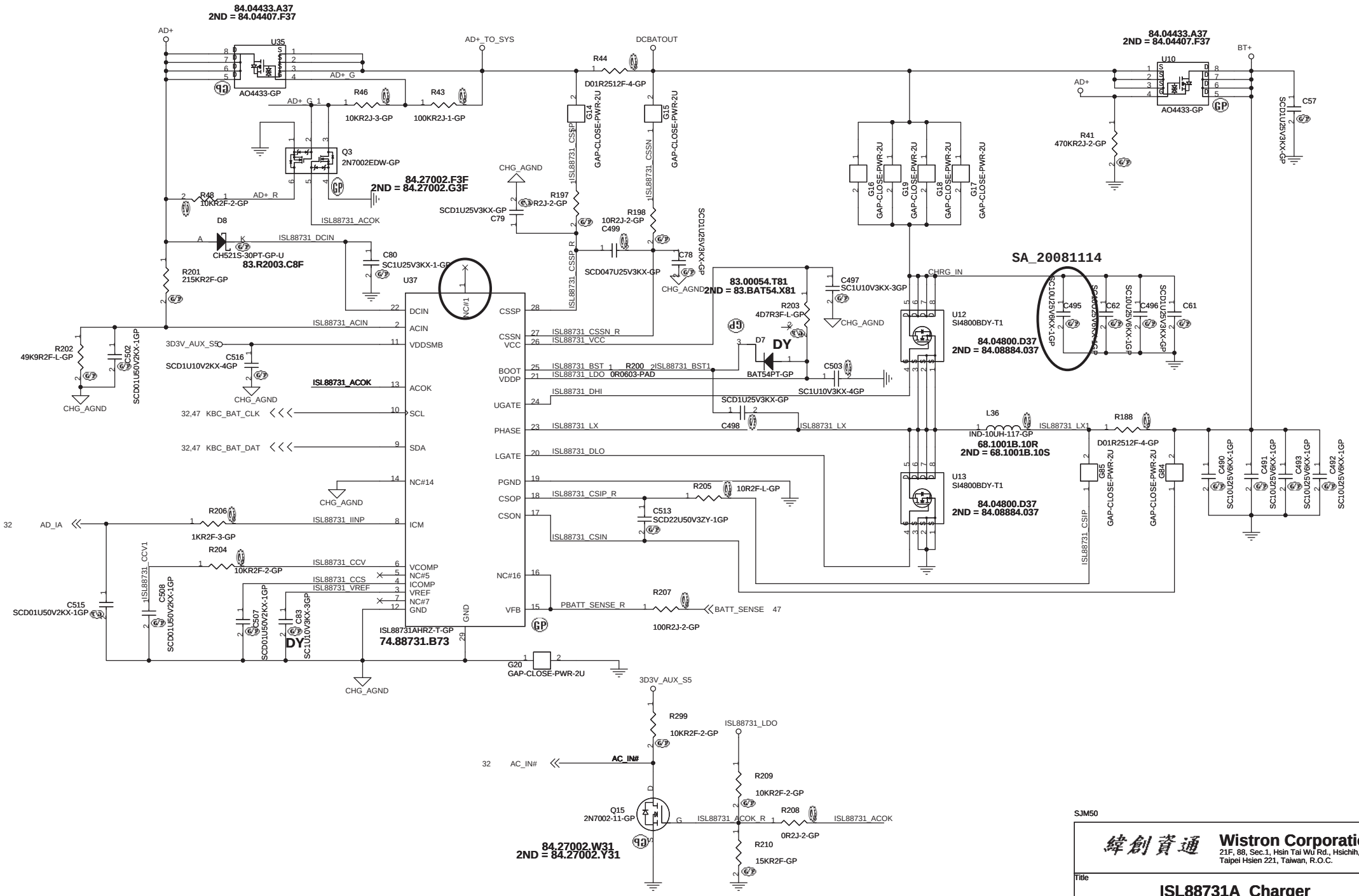
SJM50

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**TPS51124 1D8V/VGA CORE**	
Size: A3	Document Number: **SJM50-PU**	Rev: SB
Date: Wednesday, December 24, 2008	Sheet 44 of 56	



SJM50

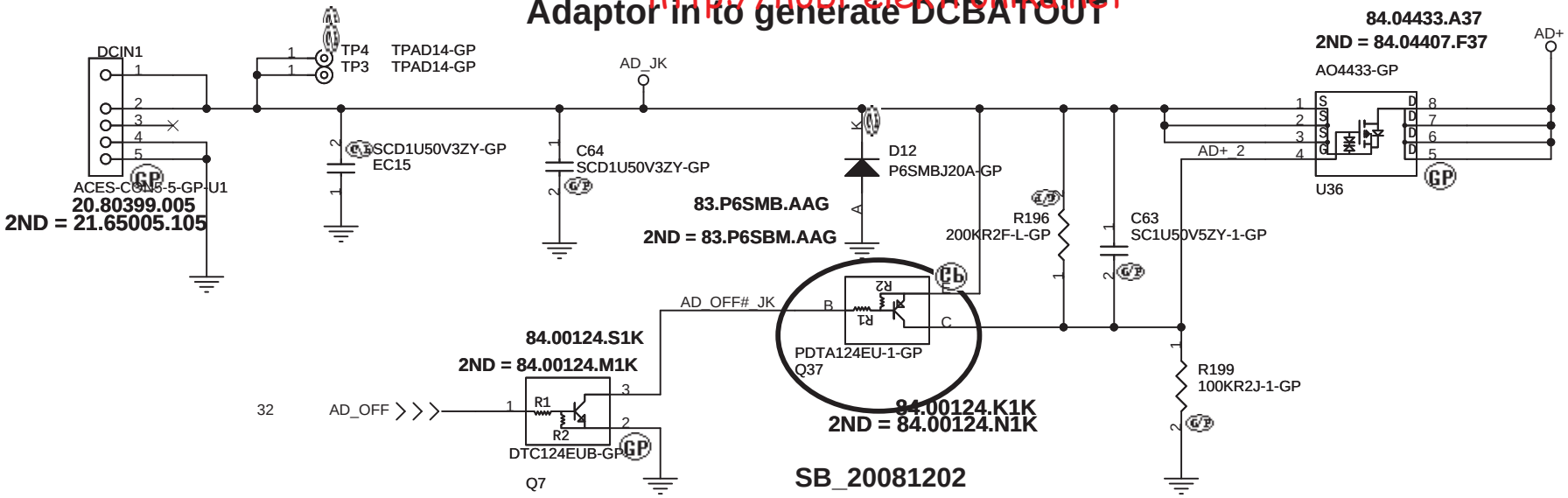
緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*VDDR3*
Size A4 / Document Number	SJM50-PU / Rev SB
Date: Wednesday, December 24, 2008	Sheet 45 of 56



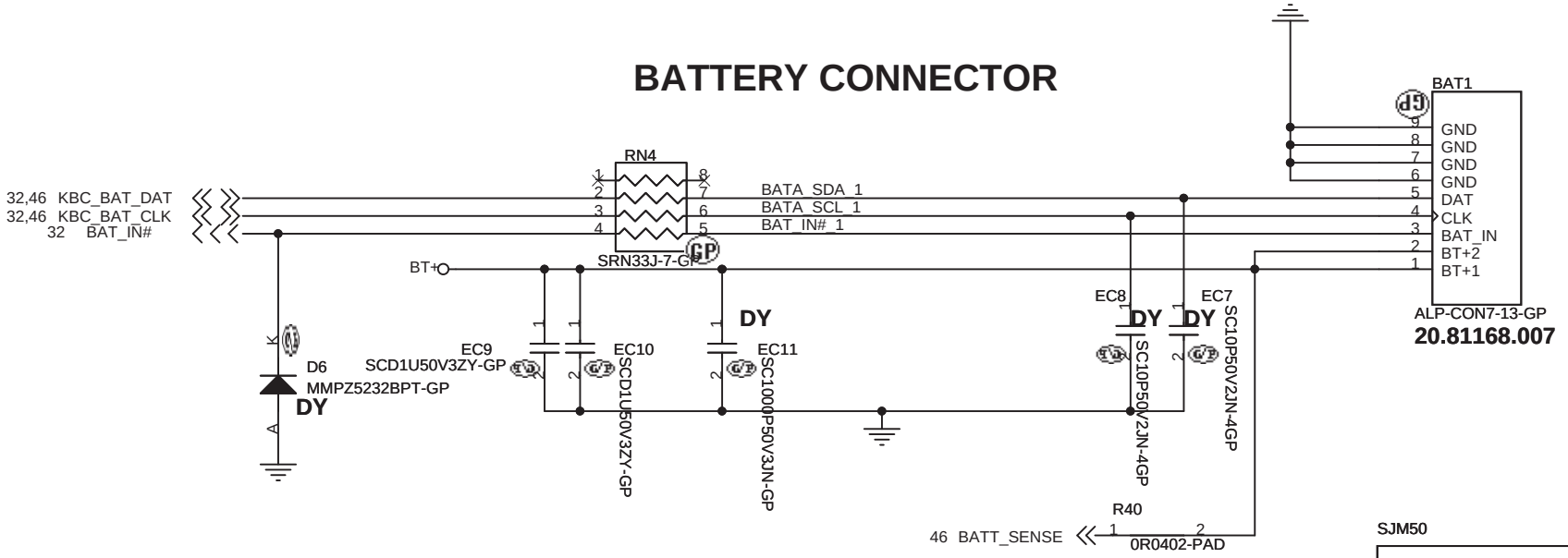
SJM50

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**ISL88731A_Charger**	
Size: A3	Document Number: **SJM50-PU**	Rev: SB
Date: Wednesday, December 24, 2008	Sheet 46 of 56	

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR

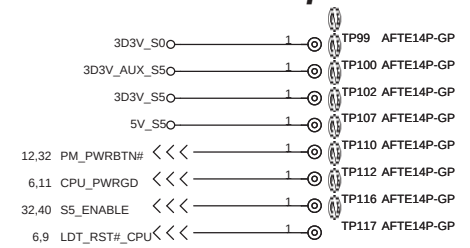


SJM50

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

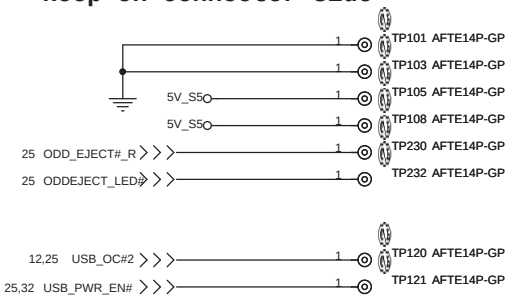
Title	AD/BATT CONN	
Size	Document Number: SJM50-PU	Rev: SB
Date: Tuesday, December 23, 2008	Sheet 47 of 56	

Check test point

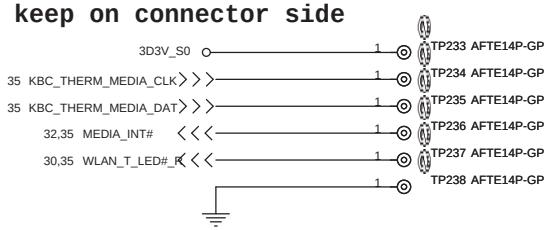


Test Point放在Dimm Door打開可量測處

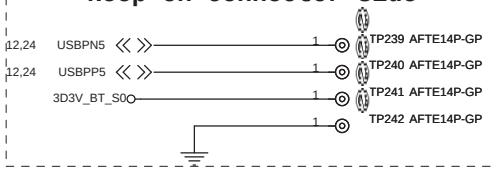
USB Conn. Test Point keep on connector side



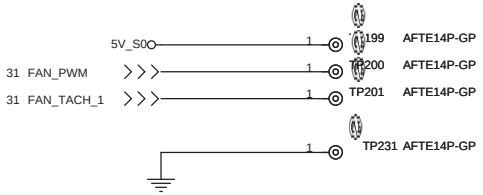
MMBB1 Conn. Test Point keep on connector side



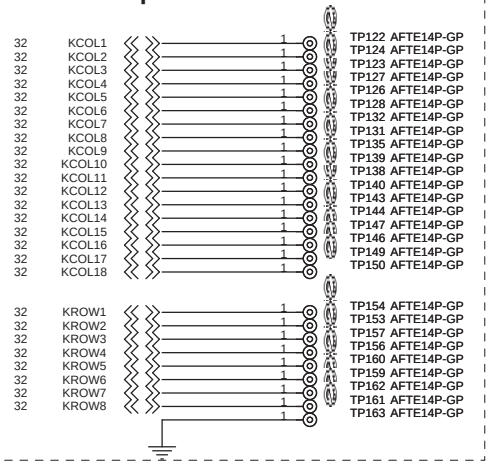
BT Conn. Test Point keep on connector side



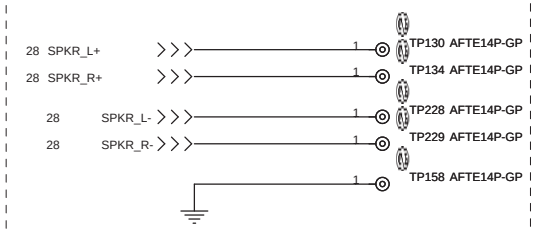
FAN Conn. Test Point keep on connector side



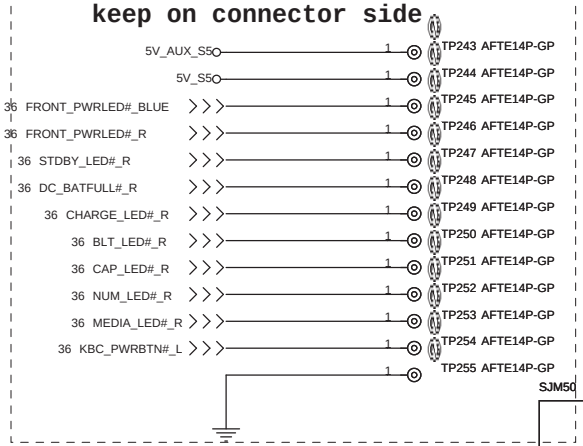
KB1 Conn. Test Point keep on connector side



SPKR1 Conn. Test Point keep on connector side

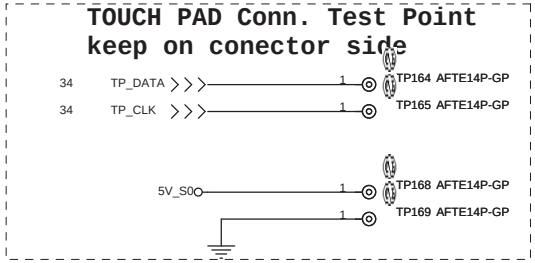


LEDB1 Conn. Test Point keep on connector side



SJM50

TOUCH PAD Conn. Test Point keep on conector side

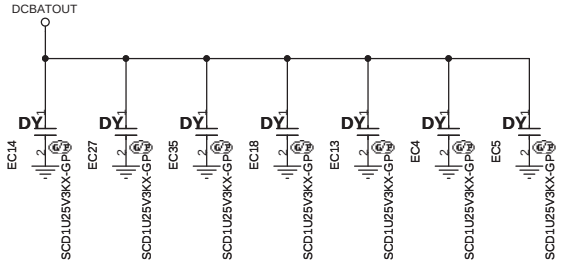


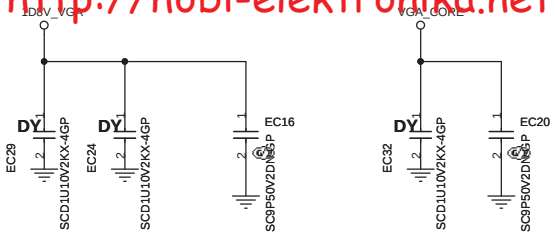
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

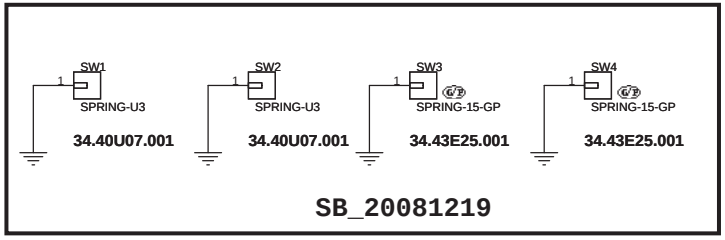
Title: AFTE_TP

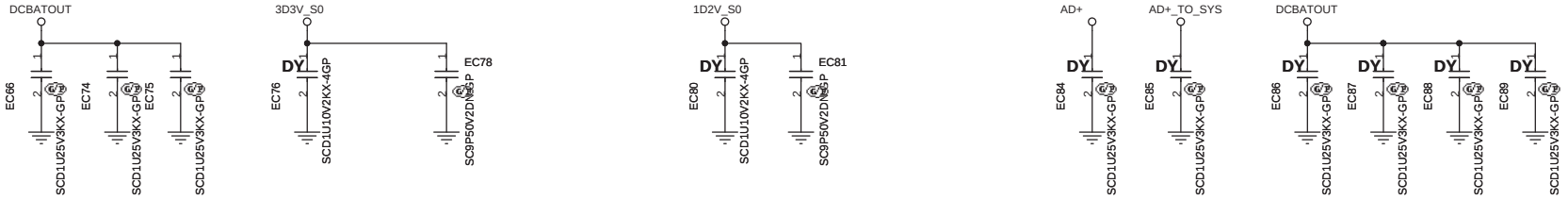
Size	Document Number	Rev
A3	SJM50-PU	SB

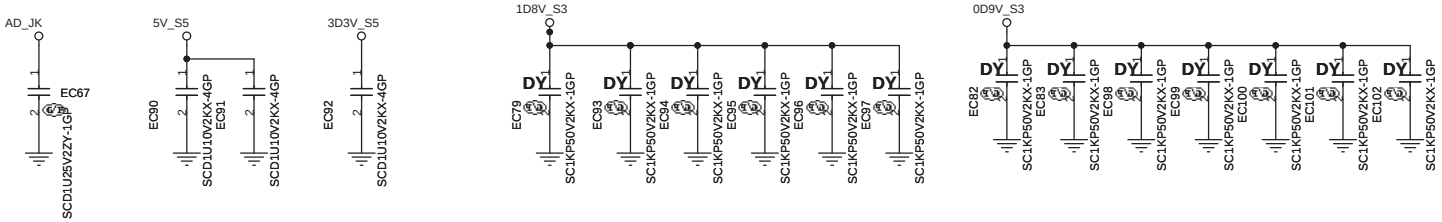
Date: Tuesday, December 23, 2008 Sheet 48 of 56





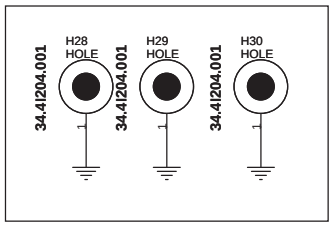




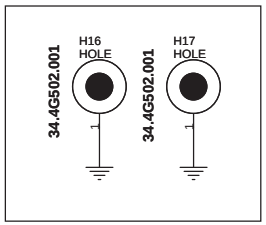


SA_20081117

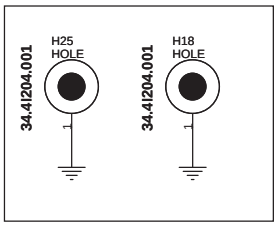
CPU



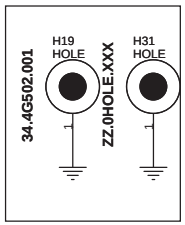
VGA



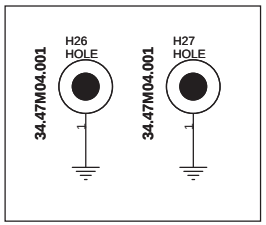
SB

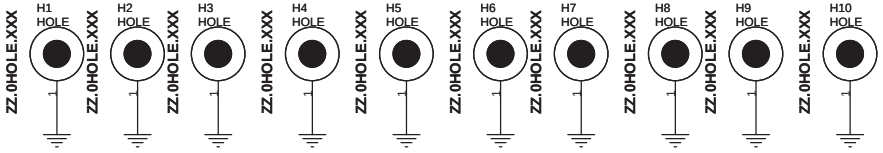


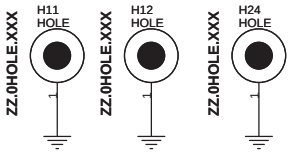
MINICARD

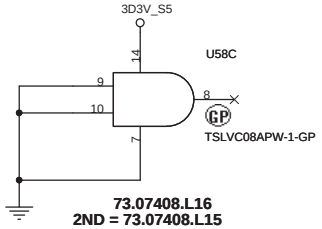


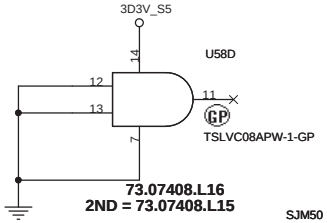
AUDIO Board

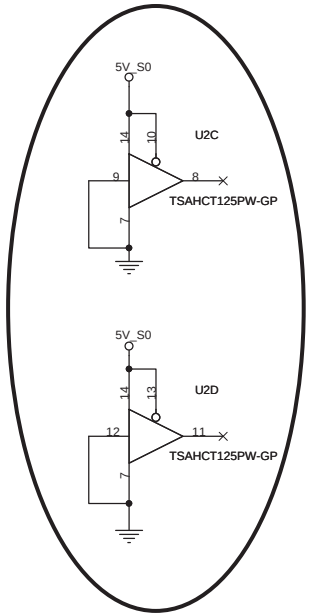












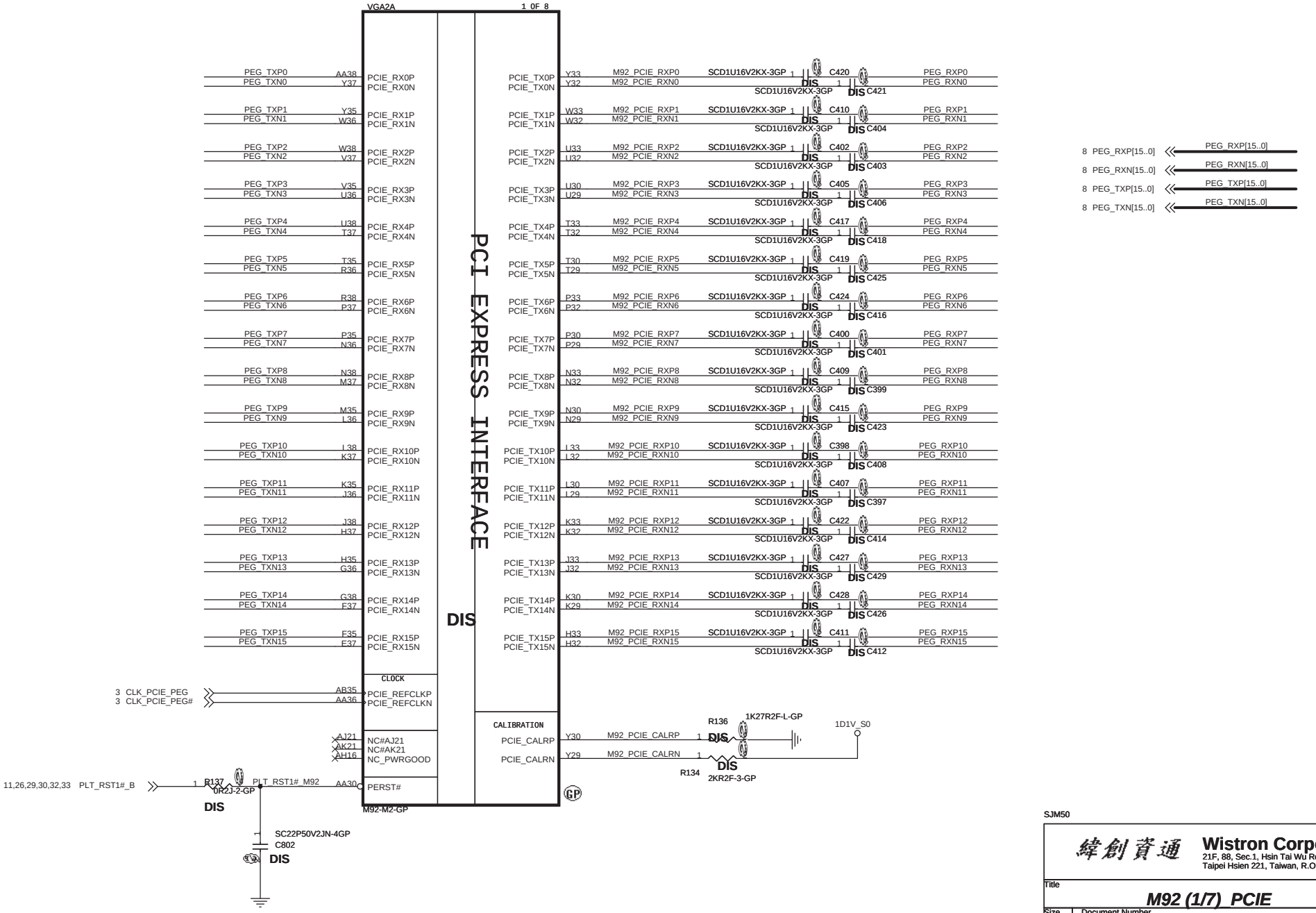
SJM50

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***EMI/Spring/Boss***

Size | Document Number: **SJM50-PU** | Rev: SB

Date: Monday, December 22, 2008 | Sheet 49 of 56



SJM50

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***M92 (1/7) PCIE***	
Size: A3	Document Number: **SJM50-PU**	Rev: SB
Date: Tuesday, December 23, 2008	Sheet 50 of 56	

PLL

SA_20081103

PH at LCD conn.

SA_20081104

Back Bias (body bias) which minimizes power consumption in battery modes.
PD = Disable
PU = Enable

VREFG VOLTAGE DIVIDER IS (VREFG = VDDR4,5(1.8V) / 3 = 0.6V)

Depending on OSC used select voltage divider resist values R25 R70 to ensure XTALIN voltage level of 1.8V

SB_20081218

SA_20081104

SA_20081104

SA_20081111

SA_20081104

SA_20081117

Company	Wistron Corporation, 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	M92 (2/7)_ IO
Size	A2
Document Number	SJM50-PU
Rev	SB
Date	Tuesday, December 23, 2008
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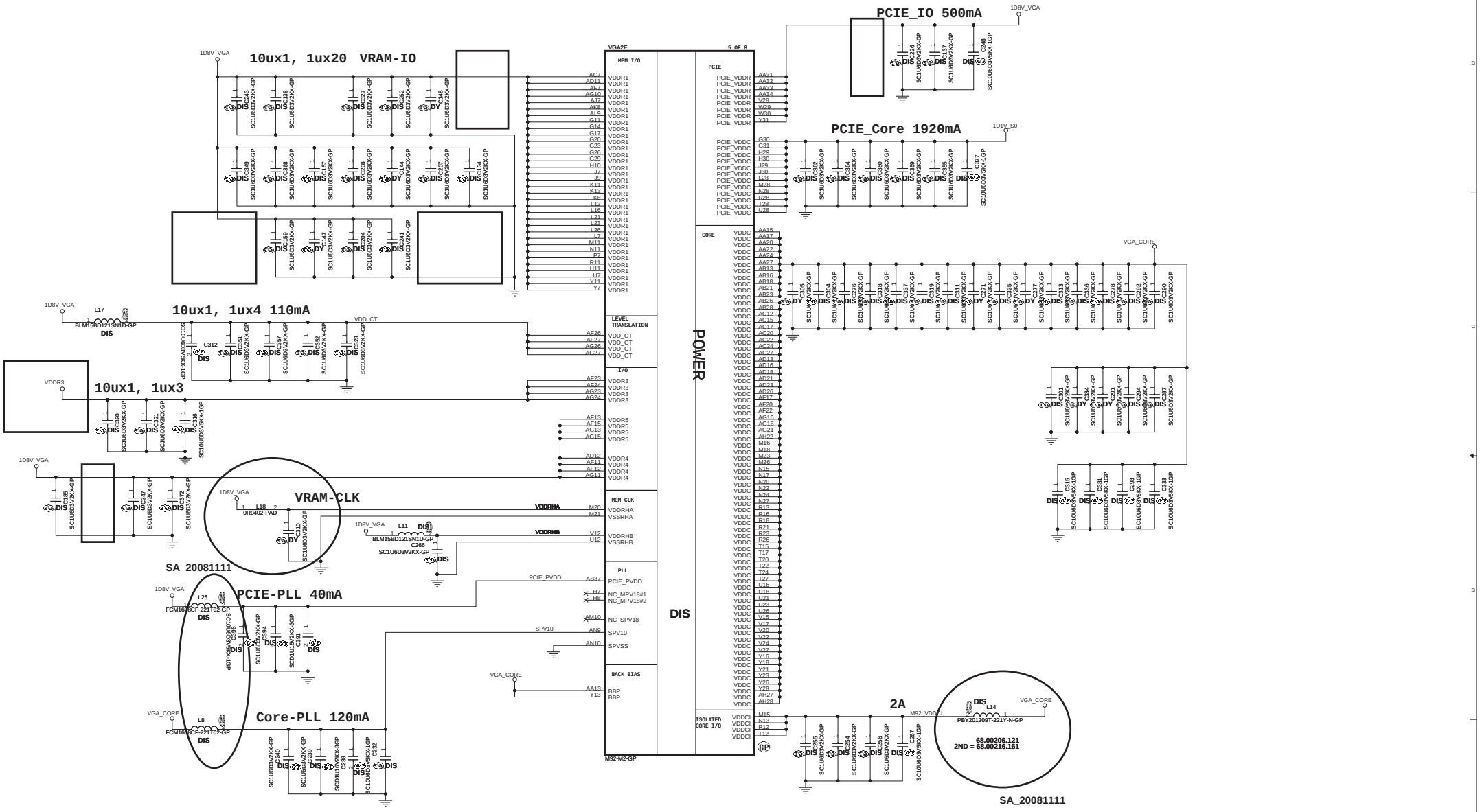
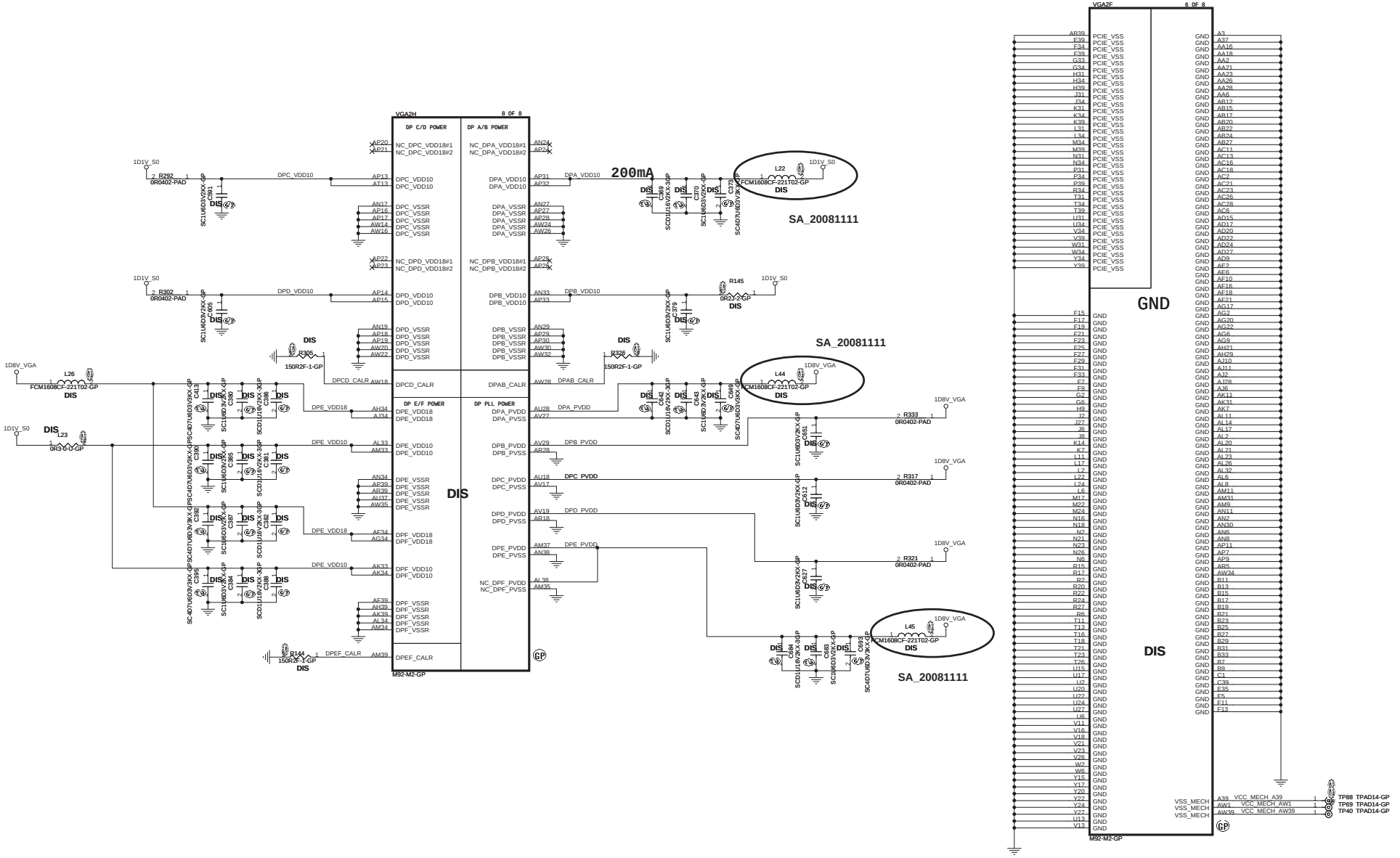


SJM50

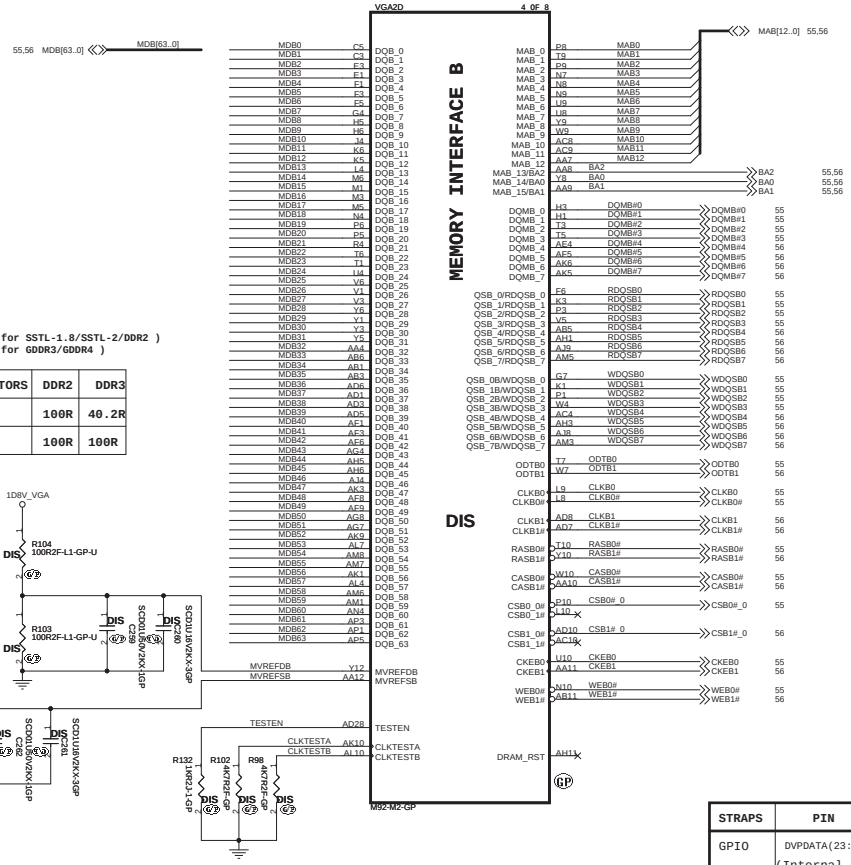
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*M92 (3/7) Power*	
Size A2	Document Number **SJM50-PU**	Rev SB
Date: Monday, December 22, 2008	Sheet 52 of 56	



SJM50

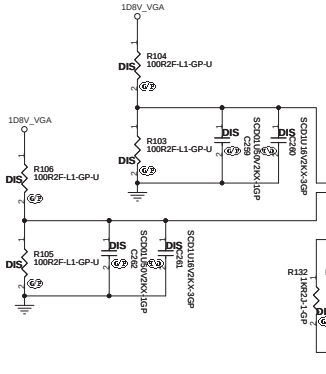
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	M92 (4/7) DP POWER_GND	
Size A2	Document Number SJM50-PU	Rev SB
Date: Monday, December 22, 2008	Sheet 53 of 56	

M92-M2 uses memory group B only

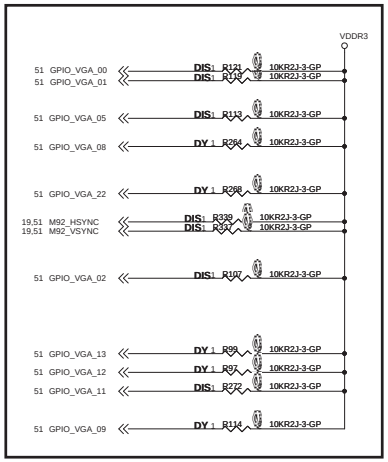


(0.5 * VDDR1) (for SSTL-1.8/SSTL-2/DDR2)
(0.7 * VDDR1) (for GDDR3/GDDR4)

DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R



SA_20081117



HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.

STRAPS	PIN	DESCRIPTION
GPIO	DVPDATA(23:20) (Internal PD)	Initialization Behavior: This signal is input during reset (no reference clock is required). After reset, the default state is output low (0 V). The signals above can be left unconnected if not used.

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC, GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO_28_TDO , GPIO21_BB_EN

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
V 128MB	x000	ST Microelectronics	M25P05A	0100
256MB	x001		M25P10A	0101
64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
2GB	x		Pm25LV010A	0101
4GB	x			

STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
TX_PWRS_ENB (Internal PD)	GPIO0	PCIE FULL TX OUTPUT SWING Tansmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	1
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	1
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED 0 = Advertises the PCI-E device as 2.5GT/s 1 = Advertises the PCI-E device as 5GT/s	1
AC_BATT	GPIO5	AC (Performance mode) = 3.3 V Battery saving mode = 0.0 V	
ROMSO	GPIO8	BIF_CLK_PM_EN Serial ROM Output from ROM	0
ROMSI	GPIO9	VGA ENABLED Serial ROM Input to ROM	0
ROMIDCFG[3:0] (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1, then Config[3:0] defines the ROM type if BIOS_ROM_EN=0, then Config[3:0] defines the primary memory apeture size	X X X
PWRCNTL_[1,0]	GPIO[15,20]	Power control signals to control the core voltage regulator	
BB_EN	GPIO21	Back Bias (body bias) which minimizes power consumption in battery modes. 0V = Disable 3D3V = Enable	0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI	1
CCBYPASS	GENERICC		0

SJM50

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: M92 (5/7) Memory Straps

Size: A2 | Document Number: SJM50-PU | Rev: SB

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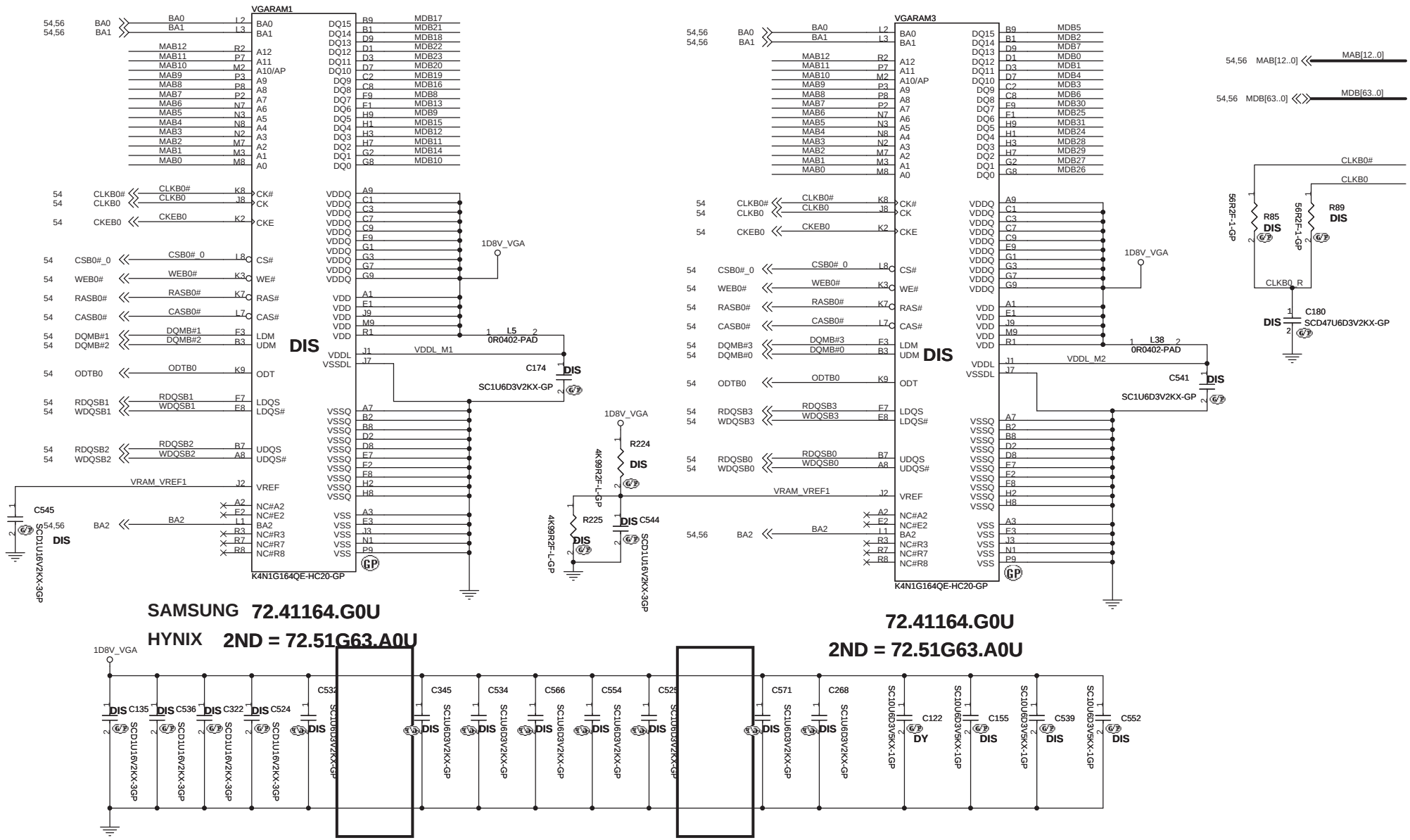

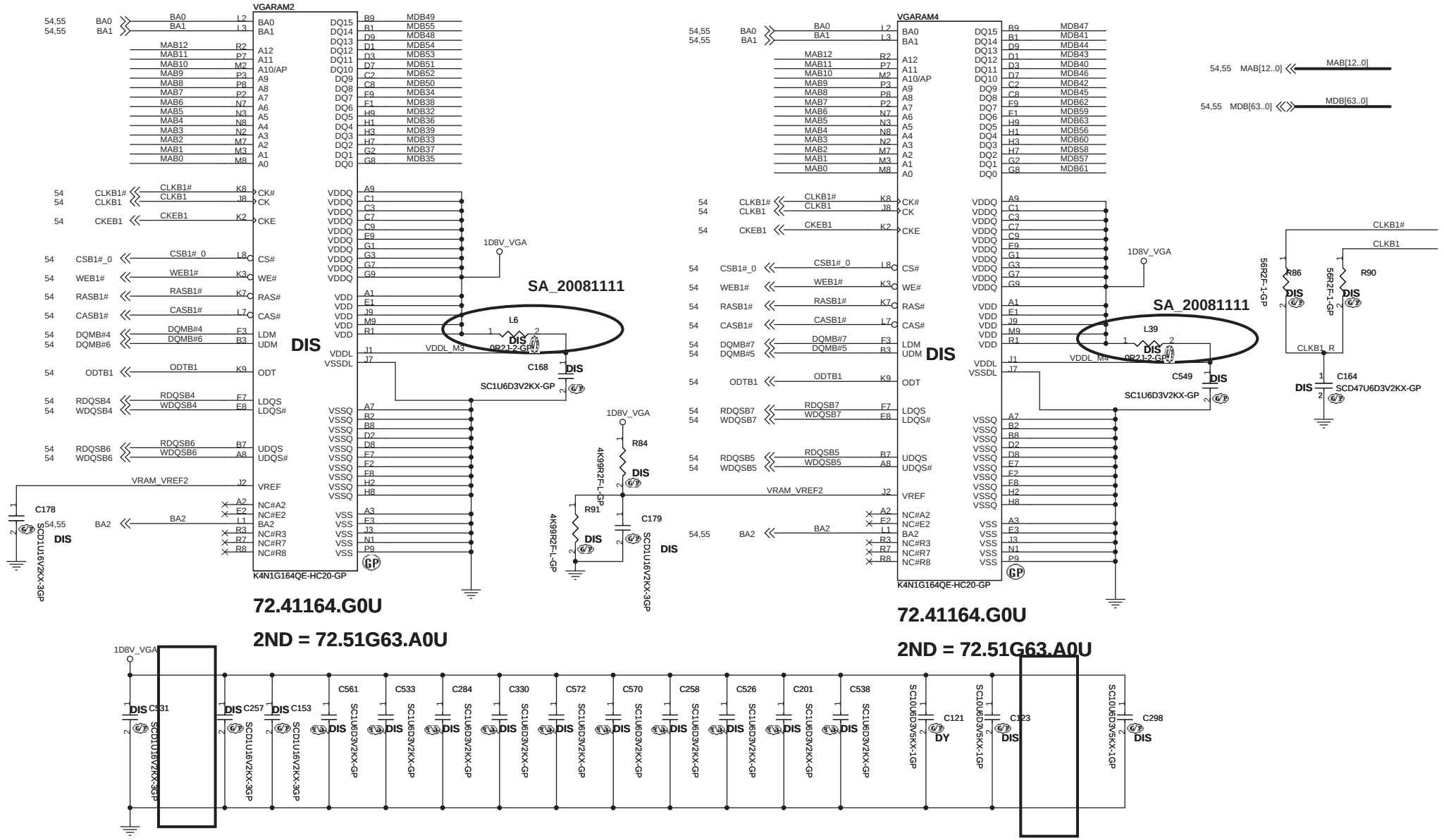

SJM50

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***M92 (7/7) VRAM B1***	
Size: A3	Document Number: **SJM50-PU**	Rev: SB
Date: Tuesday, December 23, 2008	Sheet 56 of 56	