PB5/6 Block Diagram

VCC_CORE

+1.5V

+1.05V

+1.25V

+1.8VSUS
+1.8V

+3VPCU
+3V_S5
+3VSUS
+3V
+5VPCU
+5V_S5
+5V
+SMDDR_VTERM
+SMDDR_VREF

Intel PENRYN uFCPGA
Page 3,4

FSB(667/800MHZ)

CLOCK GENERATOR
CK505
ICS9LPR363
Page 2

CRT
Page 20

INT MIC
Page 19

LCD PANEL
Page 19

CRT

LVDS

NB CANTIGA
Page 5,7,8,9,10,11

PCI-E 16X Lan

VGA CONNECTOR
Page 18

CRT
HDMI
LCD/LED

533/ 667 MHZ DDR II

DDRII-SODIMM1
DDRII-SODIMM2
Page 16, 17

DMI(x2/x4)

SATA - HDD
Page 22

SATA - ODD
Page 22

eSATA
Page 22

SATA

SATA

SATA

MINI CARD-4
ROBSON
(FTB) Page 25

PCIE-4

PCI-Express

PCIE-6

PCIE-3

PCIE-1

PCIE-5

MINI CARD-1
WLAN
Page 25

MINI CARD-2
UMA TV/ROBSON
Page 25

NEW CARD
Page 27

LAN
RTL8102
Page 26

SB ICH9M
Page 12, 13, 14, 15

WLAN
Page 25

Camera
Page 19

Bluetooth
Page 26

New Card
Page 27

M/B USB2
Page 27

M/B USB
Page 27

TV/ROBSON
Page 25

USB-5

USB-3

USB-2

USB-9

USB-7

USB-6

USB-8

USB 2.0

Azalia

PCI Bus

OZ129
Page 24

4 IN 1
Page 24

1394
Page 24

LPC

32.768KHz

ITE8512
Page 28

FAN
Page 3

T/P Board
Page 26

Key Board
Page 26

FLASH ROM
Page 28

CIR
Page 28

HP
Page 30

MIC JACK
Page 30

INT SPK
Page 29

SPK AMP
Page 29

Port-A

Port-B

AUDIO CODEC
ALC268/ALC272
Page 29

VGA Board

USB Board

Touch Pad Board

Function Board

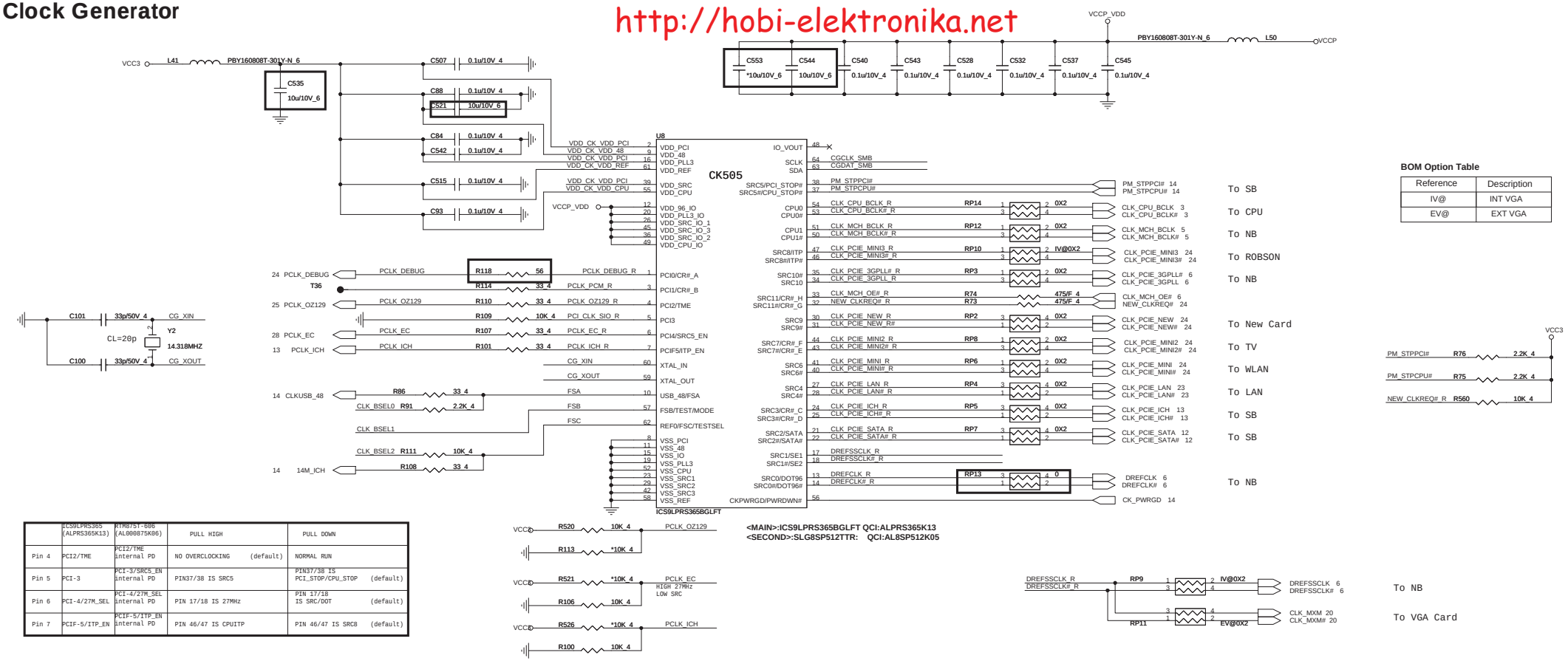
Daughter Board

PROJECT : PB5/6
Quanta Computer Inc.

Size	Document Number	Rev
	Block Diagram	1A

Date: Friday, March 21, 2008 Sheet 1 of 35

Clock Generator



<MAIN>:ICS9LPRS365BGLFT QCI:ALPRS365K13
<SECOND>:SLG8SP512TTR: QCI:AL8SP512K05

	ICS9LPRS365 (ALPRS365K13)	RTM875T-606 (AL000875K06)	PULL HIGH	PULL DOWN
Pin 4	PCI2/TME	PCI2/TME internal PD	NO OVERCLOCKING (default)	NORMAL RUN
Pin 5	PCI-3	PCI-3/SRC5_EN internal PD	PIN37/38 IS SRC5	PIN37/38 IS PCI_STOP/CPU_STOP (default)
Pin 6	PCI-4/27M_SEL	PCI-4/27M_SEL internal PD	PIN 17/18 IS 27MHz	PIN 17/18 IS SRC/DOT (default)
Pin 7	PCIF-5/ITP_EN	PCIF-5/ITP_EN internal PD	PIN 46/47 IS CPUITP	PIN 46/47 IS SRC8 (default)

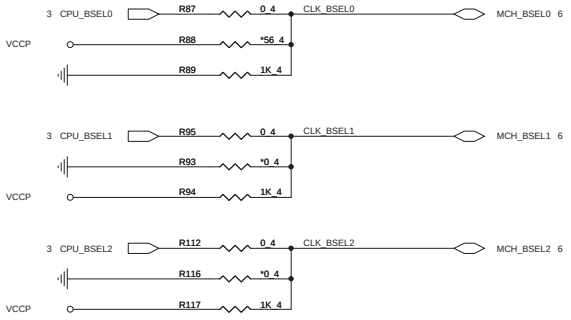
BOM Option Table

Reference	Description
IV@	INT VGA
EV@	EXT VGA

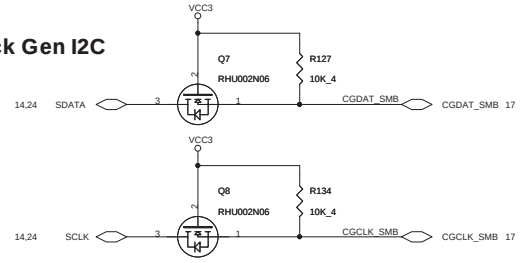
FREQ. SEL TABLE

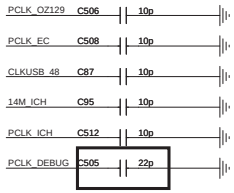
BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz



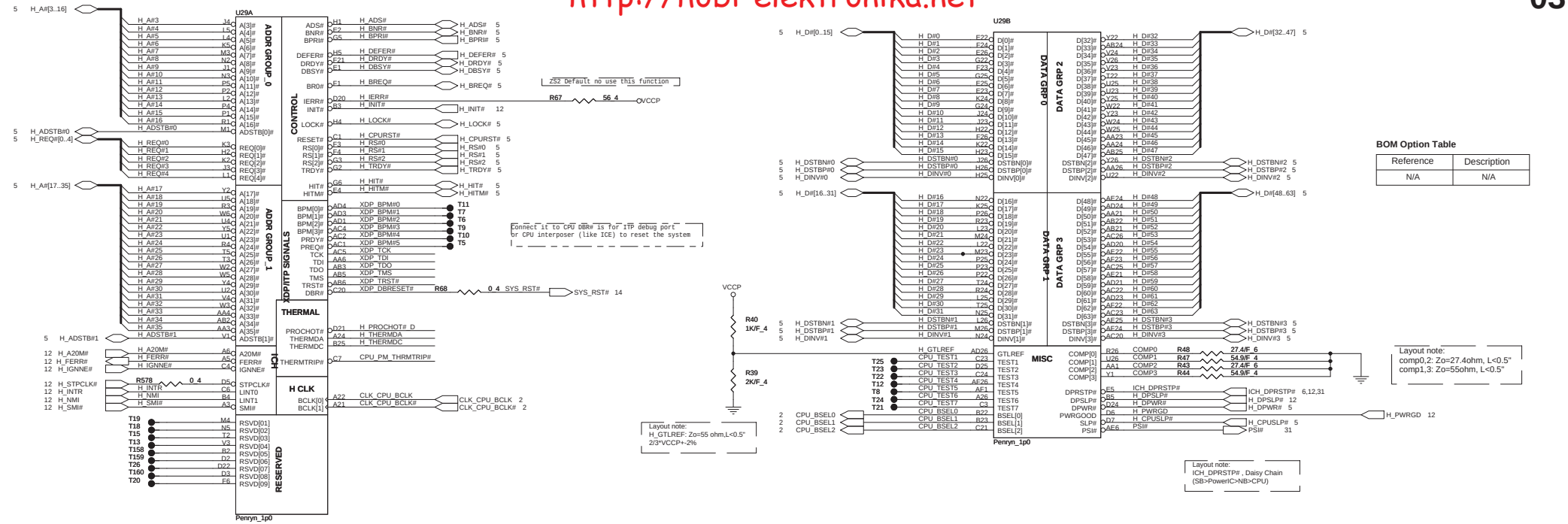
Clock Gen I2C





PROJECT : PB5/6
Quanta Computer Inc.

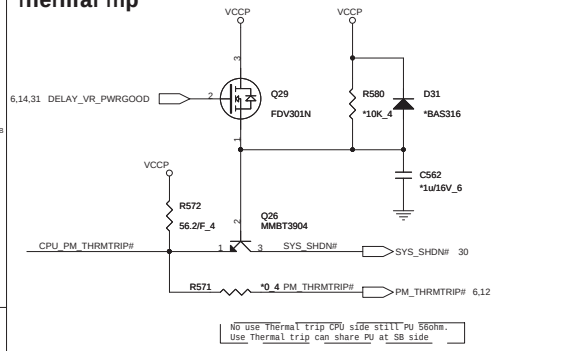
Size	Document Number	Rev
	CLK GEN	1A
Date: Friday, May 30, 2008	Sheet 2 of 35	



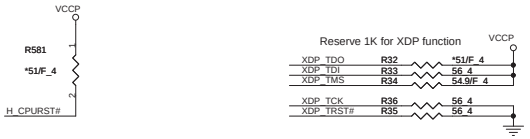
BOM Option Table

Reference	Description
N/A	N/A

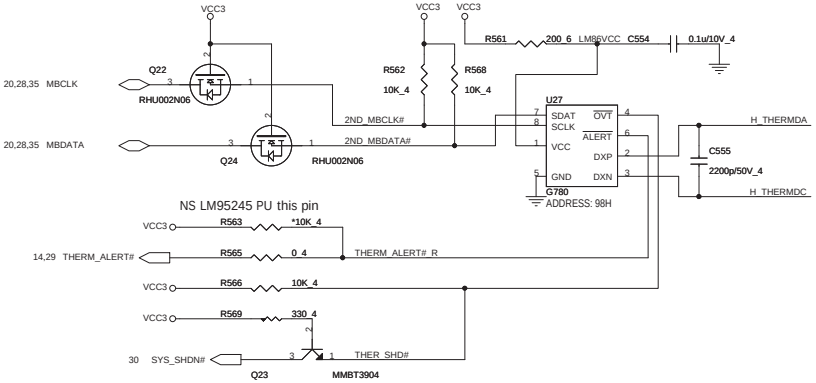
Thermal Trip



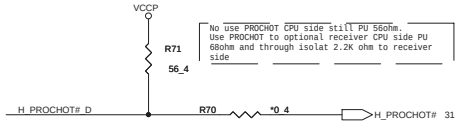
XDP



CPU Thermal monitor



Processor hot



PROJECT : PB5/6

Quanta Computer Inc.

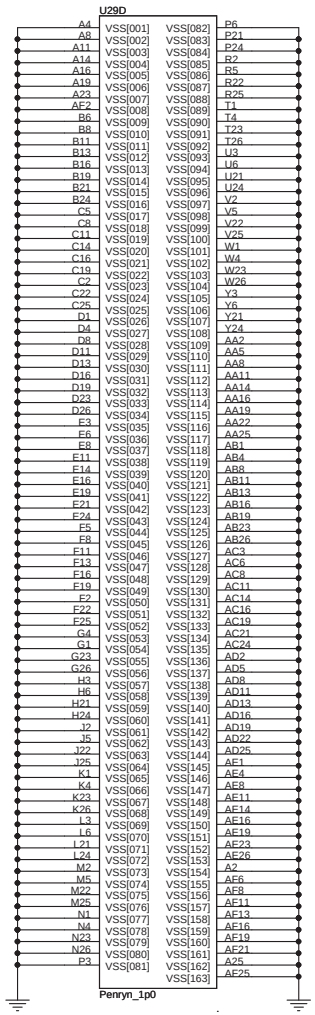
Size	Document Number	Rev
	CPU(1/2) HOST BUS	1A

Date: Friday, May 30, 2008 Sheet 3 of 35

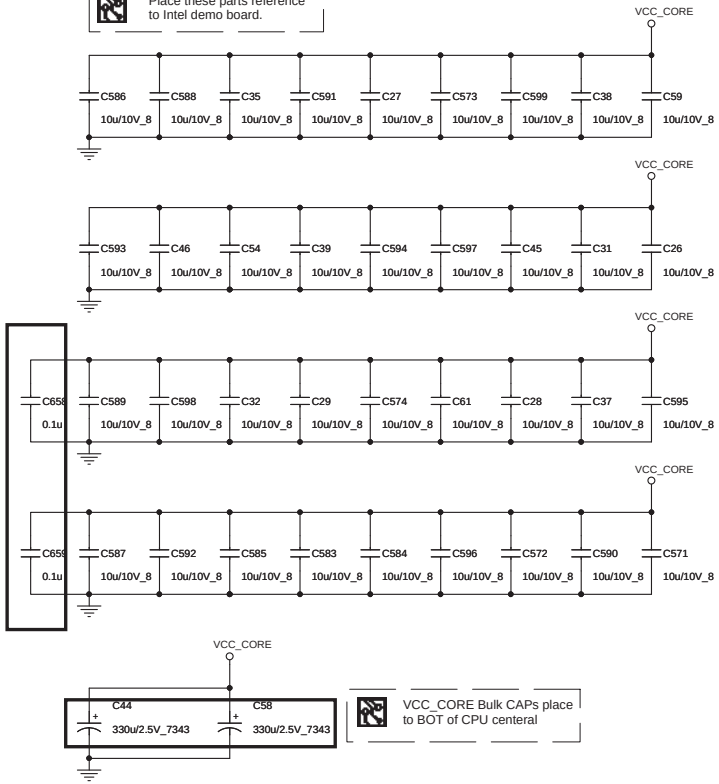
BOM Option Table

Reference	Description
N/A	N/A

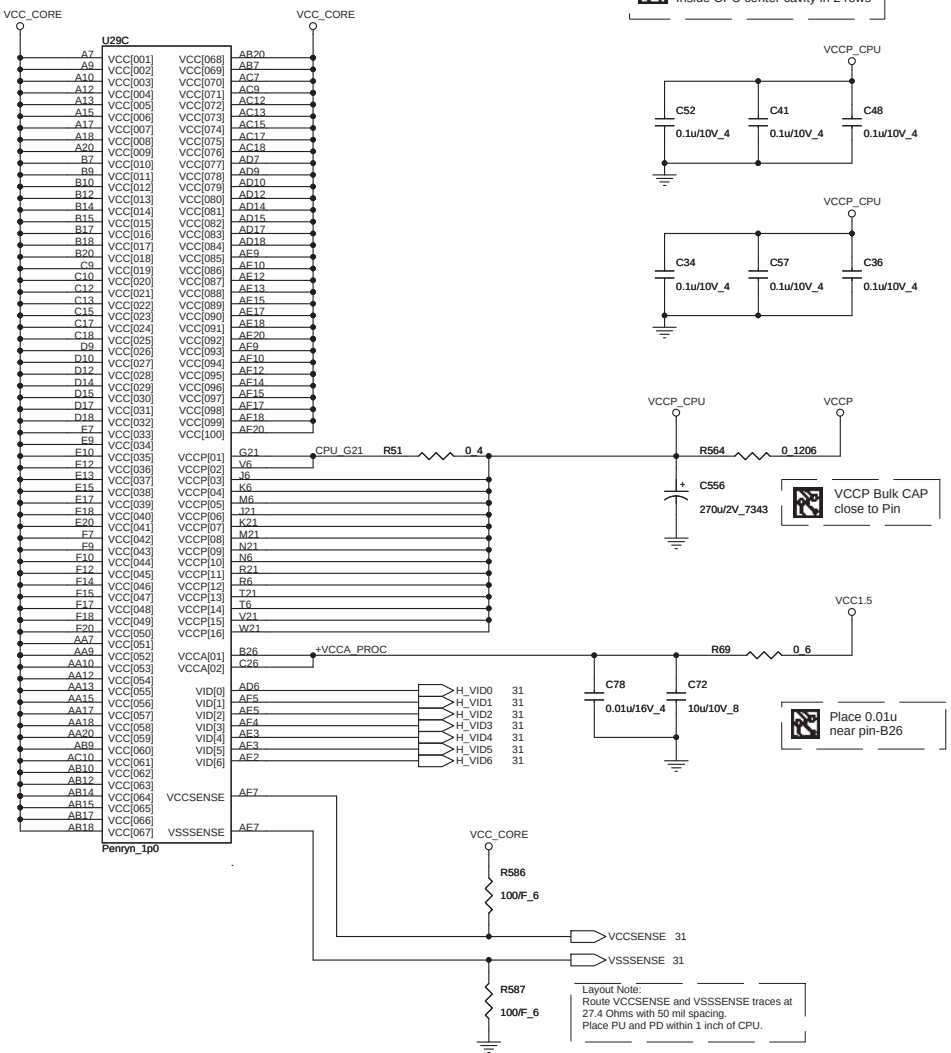
Need NC 20PCS 10u before A1 BOM released(A0 all stuff)



Place these parts reference to Intel demo board.



VCC_CORE Bulk CAPs place to BOT of CPU centeral



Layout Note:
Inside CPU center cavity in 2 rows

VCCP Bulk CAP close to Pin

Place 0.01u near pin-B26

Layout Note:
Route VCCSENSE and VSSSENSE traces at 27.4 Ohms with 50 mil spacing.
Place PU and PD within 1 inch of CPU.

Penryn CPU Power Status and max current table

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCC_CORE	O	X	X	VID	47A	Standard Voltage CPU
VCC_CORE	O	X	X	VID	50A	SV Design Target
VCC_CORE	O	X	X	VID	TBD	Extreme Edition CPU
VCC_CORE	O	X	X	VID	67A	EE Design Target
VCCA	O	X	X	+1.5V	130mA	
VCCP	O	X	X	+1.05V	4.5A	Before VCC Stable
VCCP	O	X	X	+1.05V	2.5A	After VCC Stable

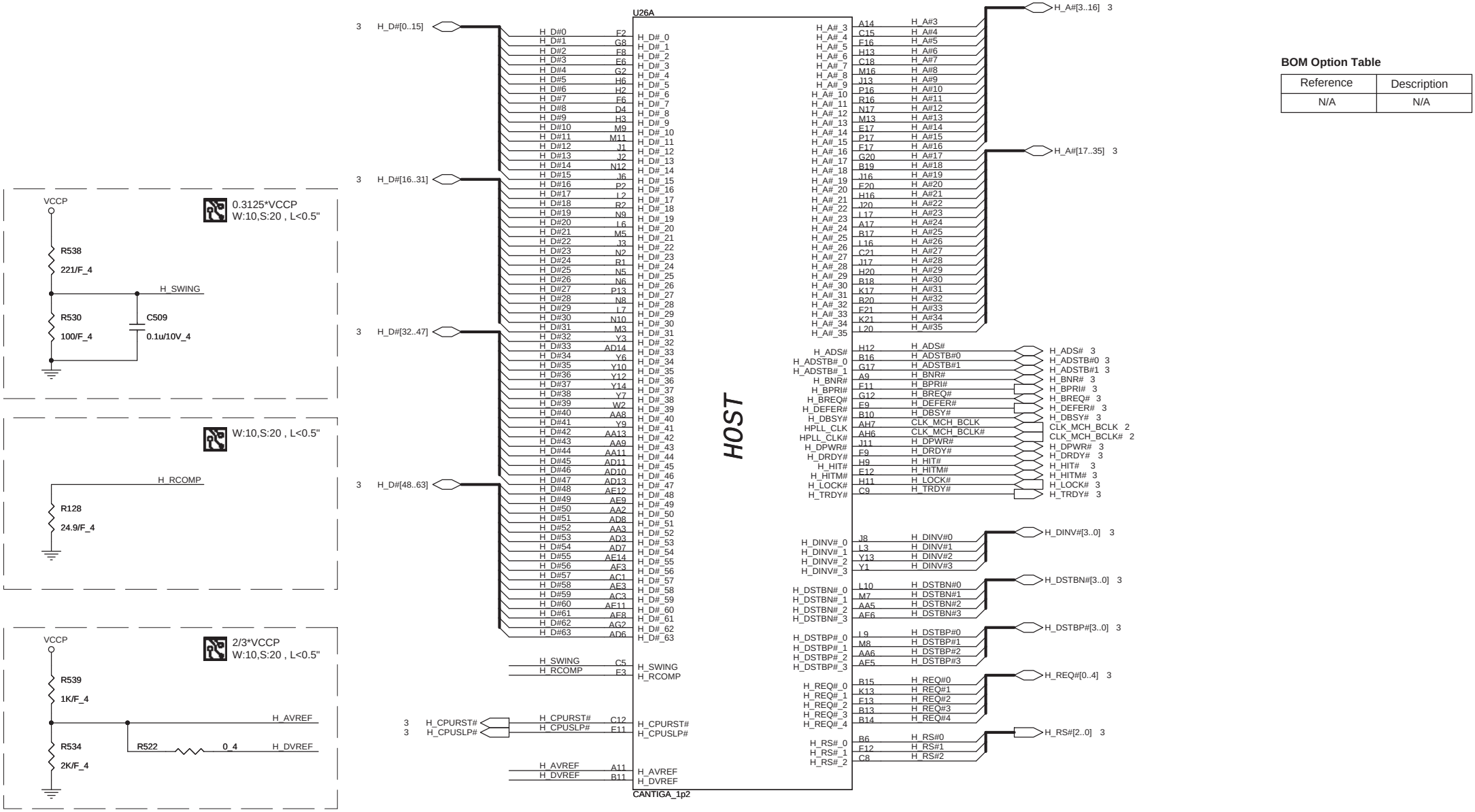
(See Penryn EMTS Rev:1.0 Table7,8 for voltage and current)

(See Penryn EMTS Rev:1.0 Table-3 for VID table)

PROJECT : PB5/6

Quanta Computer Inc.

Size	Document Number	Rev
	CPU(2/2) POWER	1A
Date: Friday, May 30, 2008	Sheet 4 of 35	



BOM Option Table

Reference	Description
N/A	N/A

PROJECT : PB5/6

Quanta Computer Inc.

Size	Document Number	Rev
	NB (1/7) HOST	1A
Date: Friday, May 30, 2008	Sheet 5 of 35	

BOM Option Table

Reference	Description
IV@	INT VGA
EV@	EXT VGA
IHM@	INT HDMI
EV_IV@	EV&IV diff. value

U26B

RSVD / CLK / DDR CLK / CONTROL / COMPENSATION

JTAG

CFG

PM

GRAPHICS VID

DMI

ME

MISC

NC

HDA

CANTIGA_1p2

U26C

LVDS I/F

TV IF (Disable)

CRT I/F

PCI-EXPRESS GRAPHICS

LVDS

VGA

CANTIGA_1p2

Close U3030

NOTE:
If (G)MCH's HD Audio signals are connected to ICH9M for iHDMI, VCCHDA and VCCSUSHDA on ICH9M should be only on 1.5V. These power pins on ICH9M can be supplied with 3.3V if and only if (G)MCH's HDA is not connected to ICH9M. Consequently, only 1.5V audio/modem codecs can be used on the platform.

IV&EV Dis/Enable LVDS setting(See DG 1.0 P190 Table 103)

IV&EV Dis/Enable CRT setting(See DG 1.0 P190 Table 103)

Dis TV/En CRT(See DG1.0 P208 Table 118)

IV&EV Dis/Enable PLL setting(See DG 1.0 P190 Table 103)

SM_PWROK only for DDR3.(DDR2 PD only)

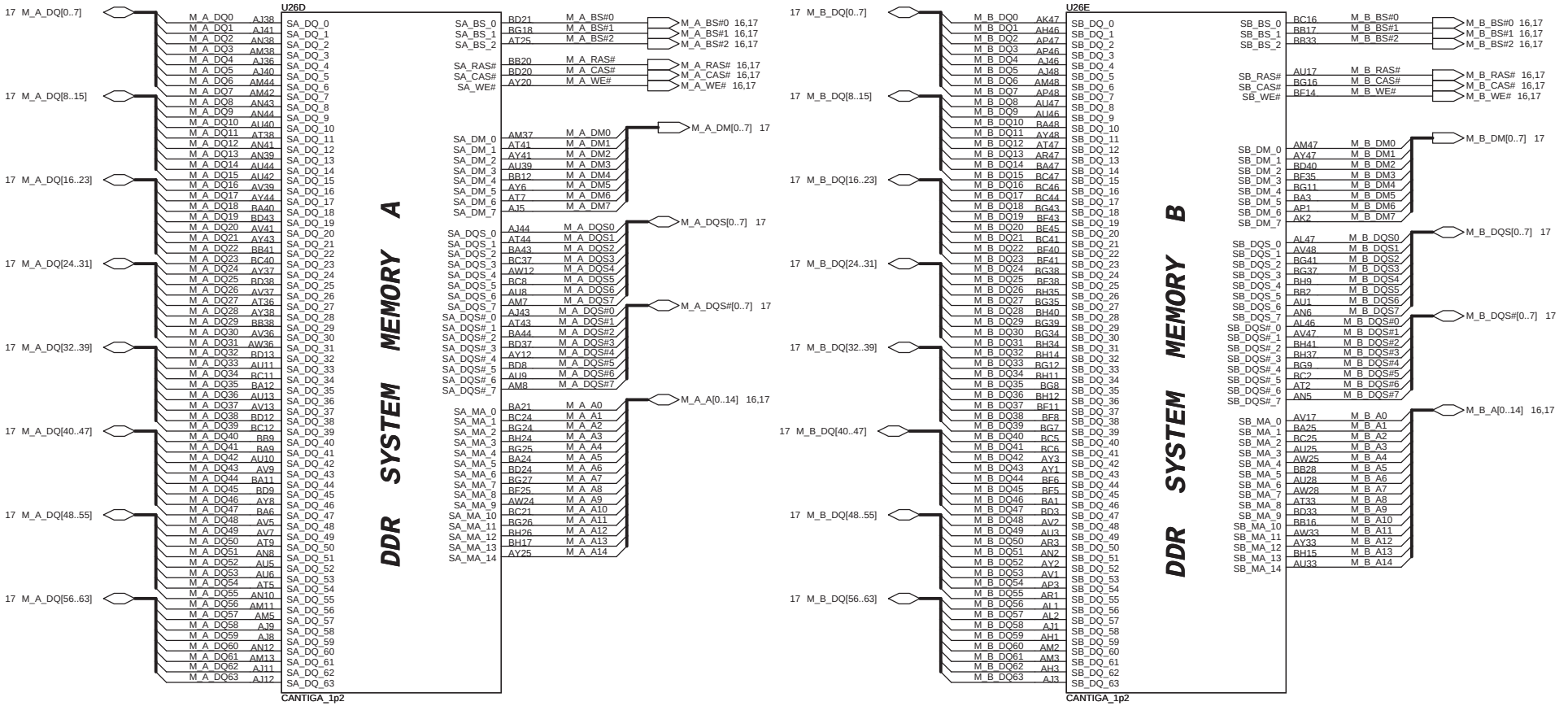
<Checklist ver0.8>
If TSATN# is not used, then it must be terminated with a 56-Ω pull-up resistor to VCCP.

SM_VREF.Default use voltage divider for poor layout cause +SMDDR_VREF not meet spec.And Intel circuit PU/PD is 1K,But Check list PU/PD is 10K.

Check list note : CL_REF=0.35V

BOM Option Table

Reference	Description
N/A	N/A



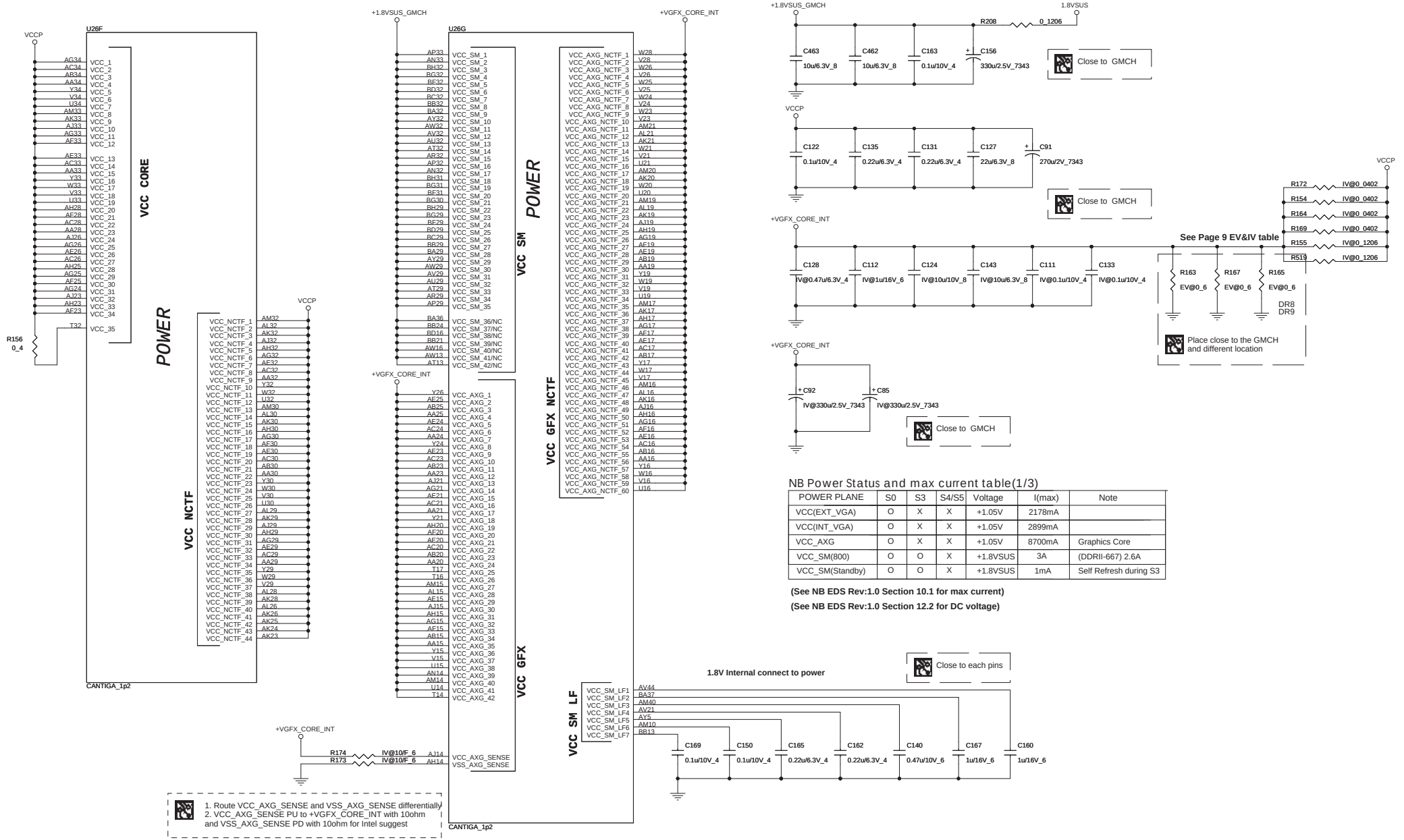
PROJECT : PB5/6

Quanta Computer Inc.

Size	Document Number	Rev
	DDRII	1A
Date: Friday, May 30, 2008	Sheet 7 of 35	

BOM Option Table

Reference	Description
IV@	INT VGA
EV@	EXT VGA



NB Power Status and max current table(1/3)

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCC(EXT_VGA)	O	X	X	+1.05V	2178mA	
VCC(INT_VGA)	O	X	X	+1.05V	2899mA	
VCC_AXG	O	X	X	+1.05V	8700mA	Graphics Core
VCC_SM(800)	O	O	X	+1.8VSUS	3A	(DDRII-667) 2.6A
VCC_SM(Standby)	O	O	X	+1.8VSUS	1mA	Self Refresh during S3

(See NB EDS Rev:1.0 Section 10.1 for max current)

(See NB EDS Rev:1.0 Section 12.2 for DC voltage)

PROJECT : PB5/6

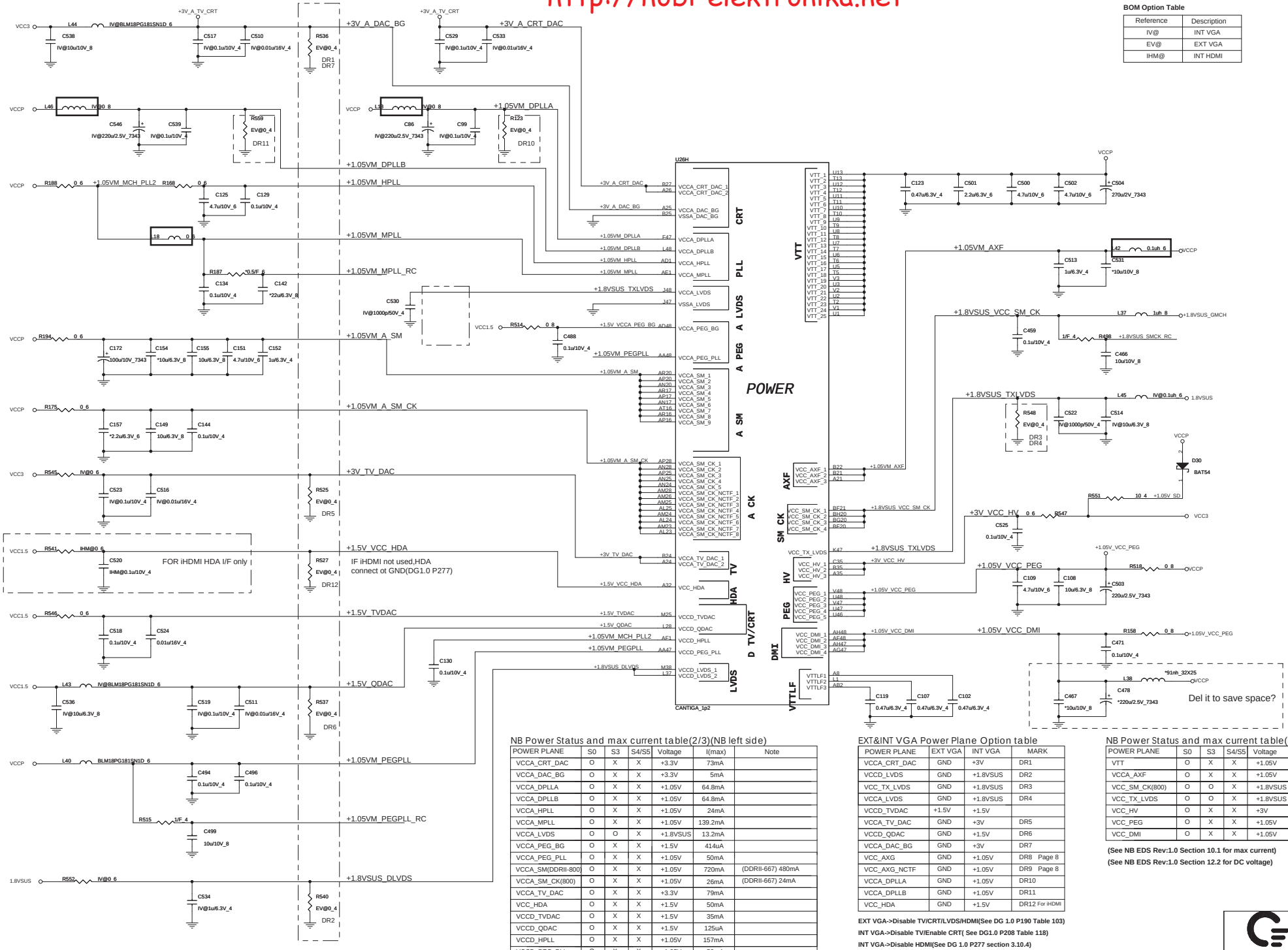
Quanta Computer Inc.

Size	Document Number	Rev
	NB(4/7) VCC ,NCTF	1A

Date: Friday, March 21, 2008 Sheet 8 of 35

BOM Option Table

Reference	Description
IV@	INT VGA
EV@	EXT VGA
IHM@	INT HDMI



NB Power Status and max current table(2/3)(NB left side)

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCCA_CRT_DAC	O	X	X	+3.3V	73mA	
VCCA_DAC_BG	O	X	X	+3.3V	5mA	
VCCA_DPLLA	O	X	X	+1.05V	64.8mA	
VCCA_DPLLB	O	X	X	+1.05V	64.8mA	
VCCA_HPLL	O	X	X	+1.05V	24mA	
VCCA_MPLL	O	X	X	+1.05V	139.2mA	
VCCA_LVDS	O	O	X	+1.8VSUS	13.2mA	
VCCA_PEG_BG	O	X	X	+1.5V	414uA	
VCCA_PEG_PLL	O	X	X	+1.05V	50mA	
VCCA_SM(DDRII-800)	O	X	X	+1.05V	720mA	(DDRII-667) 480mA
VCCA_SM_CK(800)	O	X	X	+1.05V	26mA	(DDRII-667) 24mA
VCCA_TV_DAC	O	X	X	+3.3V	79mA	
VCC_HDA	O	X	X	+1.5V	50mA	
VCCD_TVDAC	O	X	X	+1.5V	35mA	
VCCD_QDAC	O	X	X	+1.5V	125uA	
VCCD_HPLL	O	X	X	+1.05V	157mA	
VCCD_PEG_PLL	O	X	X	+1.05V	50mA	
VCCD_LVDS	O	O	X	+1.8VSUS	60mA	

EXT&INT VGA Power Plane Option table

POWER PLANE	EXT VGA	INT VGA	MARK
VCCA_CRT_DAC	GND	+3V	DR1
VCCD_LVDS	GND	+1.8VSUS	DR2
VCC_TX_LVDS	GND	+1.8VSUS	DR3
VCCA_LVDS	GND	+1.8VSUS	DR4
VCCD_TVDAC	+1.5V	+1.5V	
VCCA_TV_DAC	GND	+3V	DR5
VCCD_QDAC	GND	+1.5V	DR6
VCCA_DAC_BG	GND	+3V	DR7
VCC_AXG	GND	+1.05V	DR8 Page 8
VCC_AXG_NCTF	GND	+1.05V	DR9 Page 8
VCCA_DPLLA	GND	+1.05V	DR10
VCCA_DPLLB	GND	+1.05V	DR11
VCC_HDA	GND	+1.5V	DR12 For iHDMI

EXT VGA->Disable TV/CRT/LVDS/HDMI(See DG 1.0 P190 Table 103)

INT VGA->Disable TV/Enable CRT(See DG1.0 P208 Table 118)

INT VGA->Disable HDMI(See DG 1.0 P277 section 3.10.4)

NB Power Status and max current table(3/3)(NB Right side)

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VTT	O	X	X	+1.05V	852mA	FSB at 1067MHz
VCCA_AXF	O	X	X	+1.05V	322mA	
VCC_SM_CK(800)	O	O	X	+1.8VSUS	124mA	(DDRII-667) 120mA
VCC_TX_LVDS	O	O	X	+1.8VSUS	119mA	
VCC_HV	O	X	X	+3V	106mA	
VCC_PEG	O	X	X	+1.05V	1782mA	
VCC_DMI	O	X	X	+1.05V	456mA	

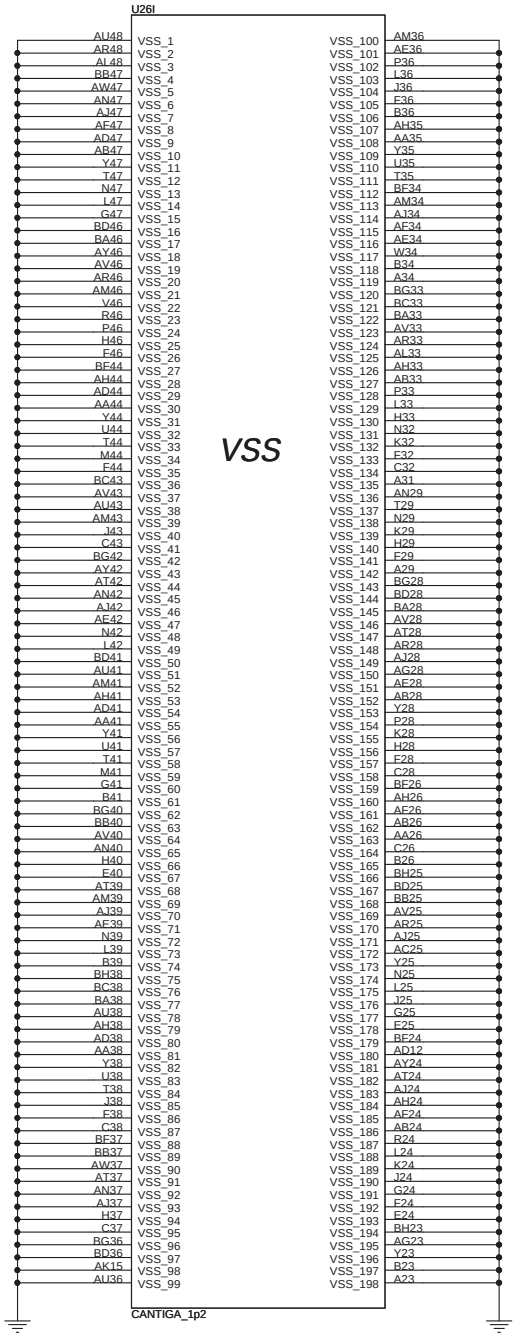
(See NB EDS Rev:1.0 Section 10.1 for max current)

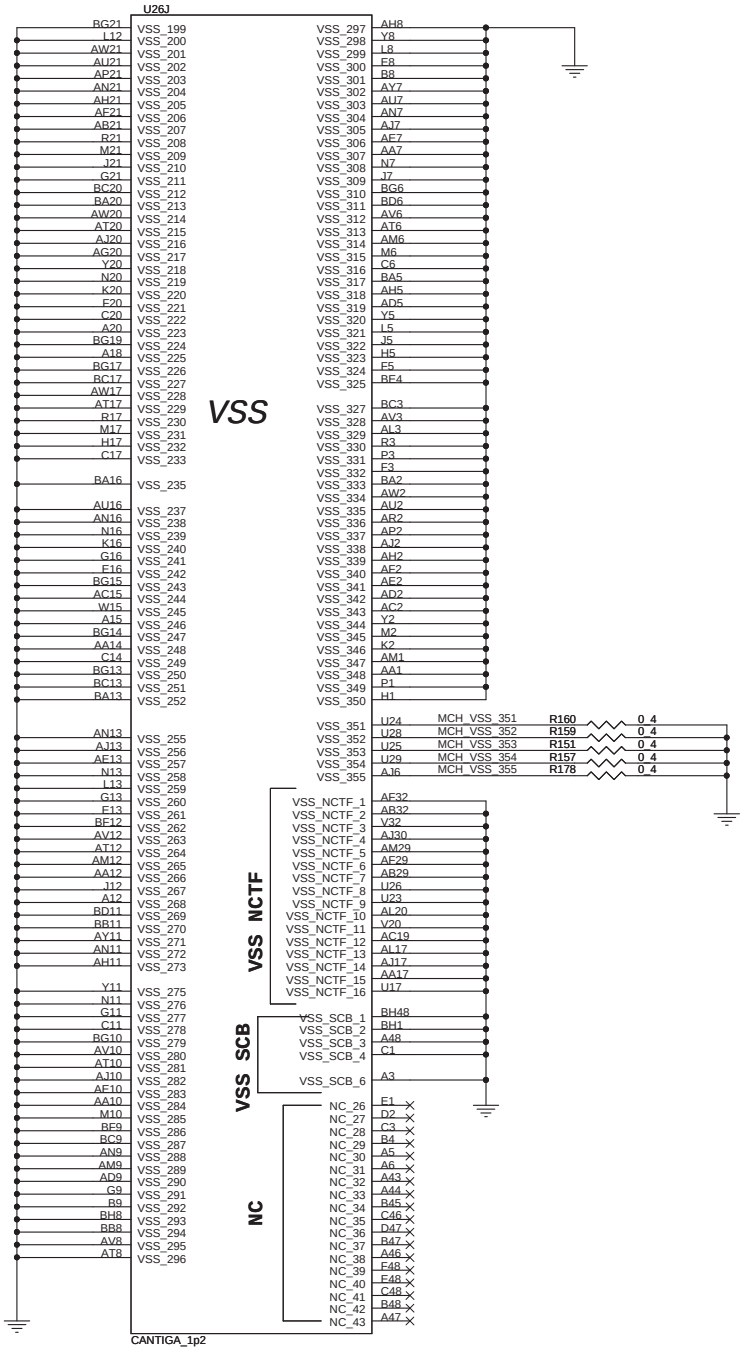
(See NB EDS Rev:1.0 Section 12.2 for DC voltage)

PROJECT : PB5/6

Quanta Computer Inc.

Size	Document Number	Rev
	NB(5/7) POWER	1A
Date: Thursday, April 24, 2008	Sheet 9 of 35	





BOM Option Table

Reference	Description
N/A	N/A

PROJECT : PB5/6

Quanta Computer Inc.

Size	Document Number	Rev
	NB(6/7) VSS	1A
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North Bridge Strap Pin Configuration Table

(See DG 1.0 P295 Table 184)
(See NB EDS 1.0 P187 Table 74)

Pin Name	Strap description	Configuration	PU<4.02K> PD <2.21K>	Note
CFG[2:0]	FSB Frequency Select	[000]= FSB 1066MHz [010] = FSB 800MHz [011] = FSB 667MHz	See Page 2 FSB selection table	
CFG[4:3]	Reserved			
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)	6 MCH_CFG_5 R115 *4.02K/F_4	
CFG6	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)	6 MCH_CFG_6 R146 *10K/F_4	**Enable iTPM**
CFG7	ME TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)	6 MCH_CFG_7 R142 *4.02K/F_4	
CFG8	Reserved			
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)	6 MCH_CFG_9 R549 *4.02K/F_4	
CFG10	PCIE Loopback enable	0 = Enabled 1 = Disabled (Default)	6 MCH_CFG_10 R550 *4.02K/F_4	
CFG11	Reserved			
CFG12	ALLZ	0 = ALLZ mode enable 1 = disable(Default)	6 MCH_CFG_12 R144 *4.02K/F_4	
CFG13	XOR	0 = XOR mode enable 1 = disable(Default)	6 MCH_CFG_13 R150 *4.02K/F_4	
CFG[15:14]	Reserved			
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)	6 MCH_CFG_16 R138 *4.02K/F_4	
CFG[18:17]	Reserved			
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed	6 MCH_CFG_19 R85 *4.02K/F_4 VCC3	
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display port (SDVO/DP/iHDMI) or PCIE is operational (Default) 1 = Digital Display port (SDVO/DP/iHDMI) and PCIE are operating simultaneously via PEG port	6 MCH_CFG_20 R84 *4.02K/F_4 VCC3	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/HDMI/DP Device Present(Default) 1 = SDVO/HDMI/DP Device present	6 SDVO_CTRLDATA R92 *2.2K/F_4 VCC3	
L_DDC_DATA	Local Flat Panel(LFP) Present	0 = LFP Disable(Default) 1 = LFP Card Present;PCIE disable	6,19 INT_LVDS_EDIDDATA R103 *2.2K/F_4 VCC3	
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent(Default) 1 = Digital display(HDMI/DP) device present	6 DDPC_CTRLDATA R90 *2.2K/F_4 VCC3	

BOM Option Table

Reference	Description
N/A	N/A

Enable iTPM Table

PAGE	Net Name	PU & PD	NOTE
11	MCH_CFG_6	PD 10K to GND	NB Strap pin
13	SPI_MOSI	PU 20K to +3V_S5	SB Strap pin
14	CLGPIO5	PU 10K to +3V_S5	SB Strap pin

PROJECT : PB5/6
Quanta Computer Inc.

Size	Document Number	Rev
	NB(7/7) STRAP	1A
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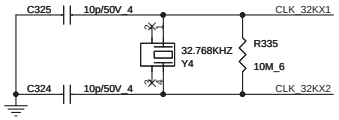
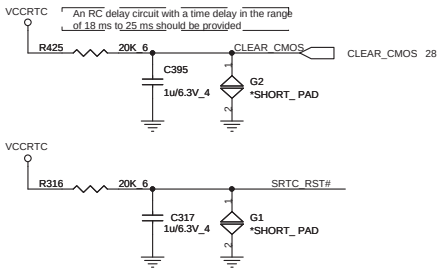
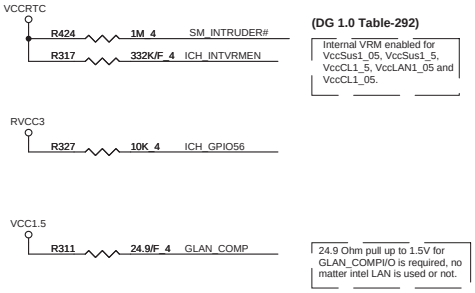
RTC CRYSTAL



RESET JUMP





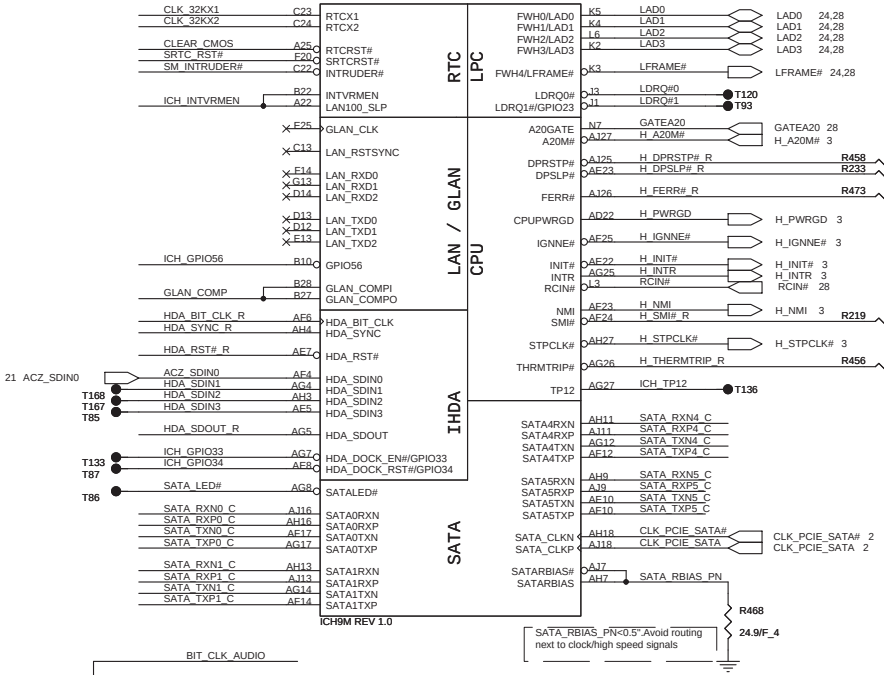
LDRQ0/1# : Internal PU

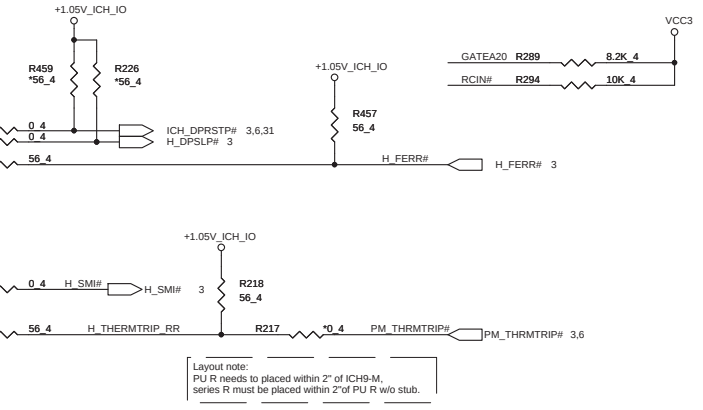
Layout note:
DPRSTP# , Daisy Chain
(SB>Power>NB>CPU)

BOM Option Table

Reference	Description
IHM@	INT HDMI

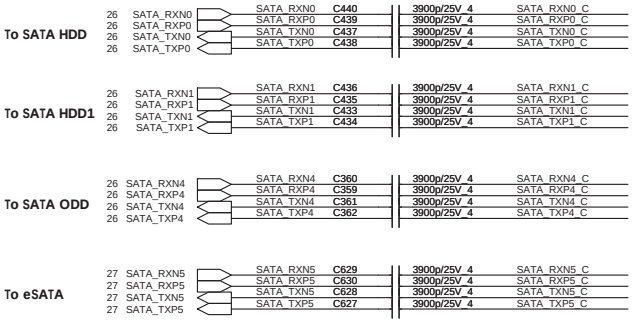
U22A





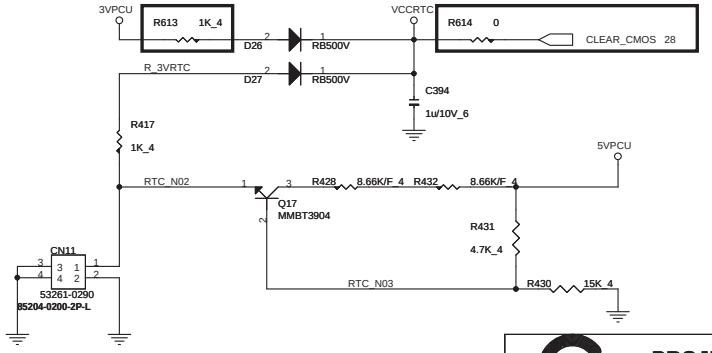
Layout note:
PU R needs to placed within 2" of ICH9-M, series R must be placed within 2"of PU R w/o stub.

SATA I/F



HD Audio I/F(CODEC& iHDMI)

RTC BATTERY



South Bridge Strap Pin (1/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect	This strap should only be enabled in manufacturing environments using an external pull-up resistor.
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU	
TP3	XOR Chain Entrance	PWROK	ICH_TP3 / HDA_SDOUT: 0/0 RSVD; 0/1 Enter XOR Chain; 1/0 Normal opration(Default); 1/1 Set PCIE port config bit 1	14 ICH_TP3 — ICH_TP3 R299 *1K_4
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK		HDA_SDOUT_R R467 *1K_4 +3V_HDA_IO_ICH PU VCC1.5

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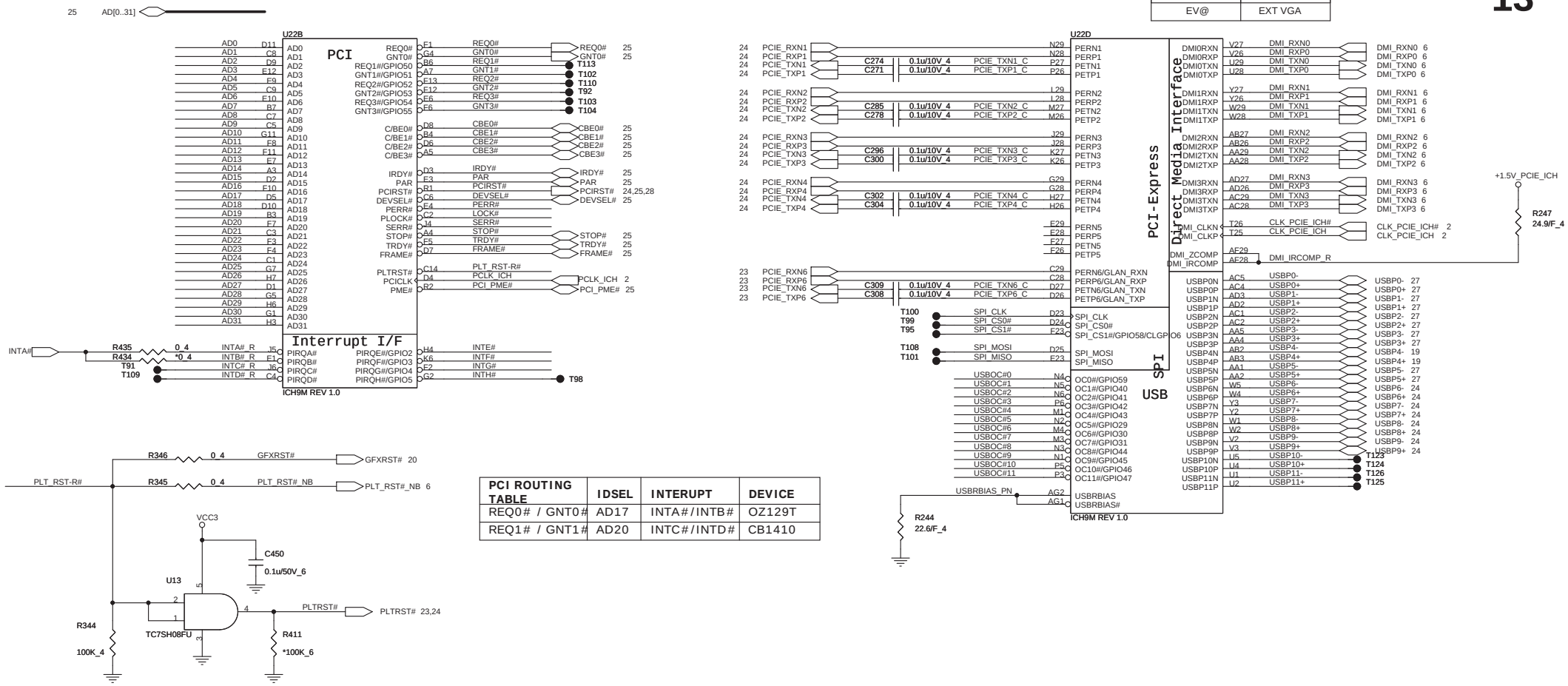
Date: Friday, May 30, 2008	Sheet 12 of 35

BOM Option Table

Reference	Description
IV@	INT VGA
EV@	EXT VGA

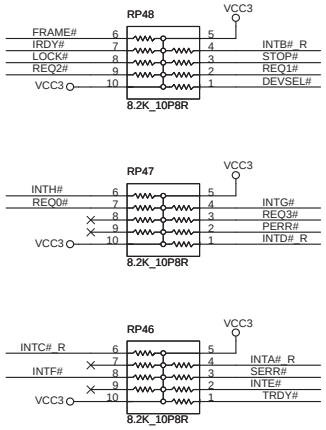


PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD17	INTA#/INTB#	OZ129T
REQ1# / GNT1#	AD20	INTC#/INTD#	CB1410

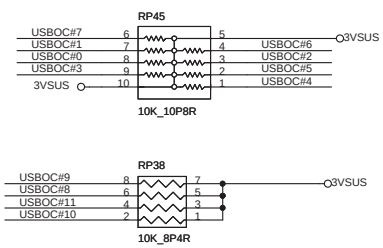
South Bridge Strap Pin (2/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0	
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default	
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default	GNT3# R330 *1K_4
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable	Disable iTPM SPI_MOSI R331 *20K_4 3VSUS
GNT0#	Boot BIOS Selection 0	PWROK	PCI_GNT#0 / SPI_CS#1 / Boot Location 0 / 1 / SPI(Default) 1 / 0 / PCI 1 / 1 / LPC	GNT0# R306 *1K_4
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK		SPI_CS1# R302 *1K_4

PCI PULL-UP



USBOC# PULL-UP



PROJECT : PB5/6

Quanta Computer Inc.

Size	Document Number	Rev
	SB (2/4) PCIE/PCI/USB	1A

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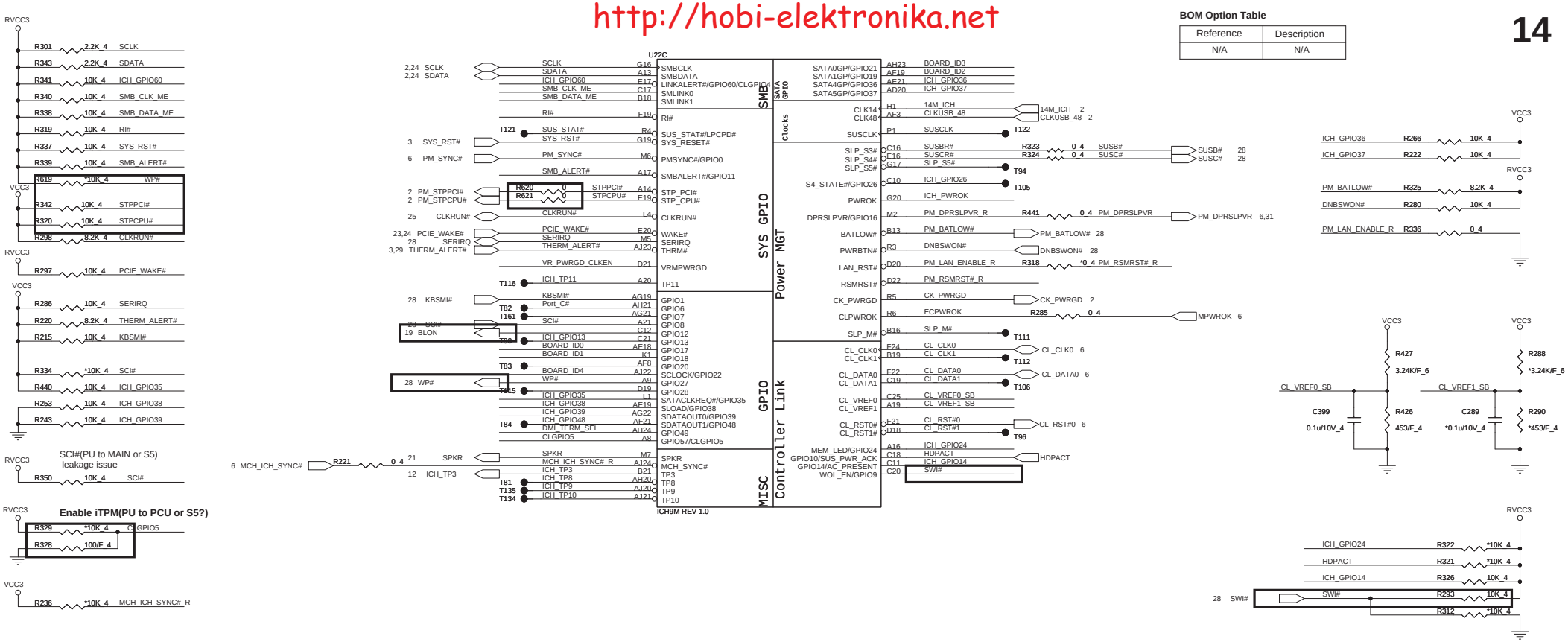
BOM Option Table

Reference	Description
N/A	N/A



South Bridge Strap Pin (3/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
SPKR	No Reboot	PWROK	0 = Default 1 = No Reboot mode	SPKR R291 *1K_4 VCC3
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	DMI_TERM_SEL R241 *1K_4

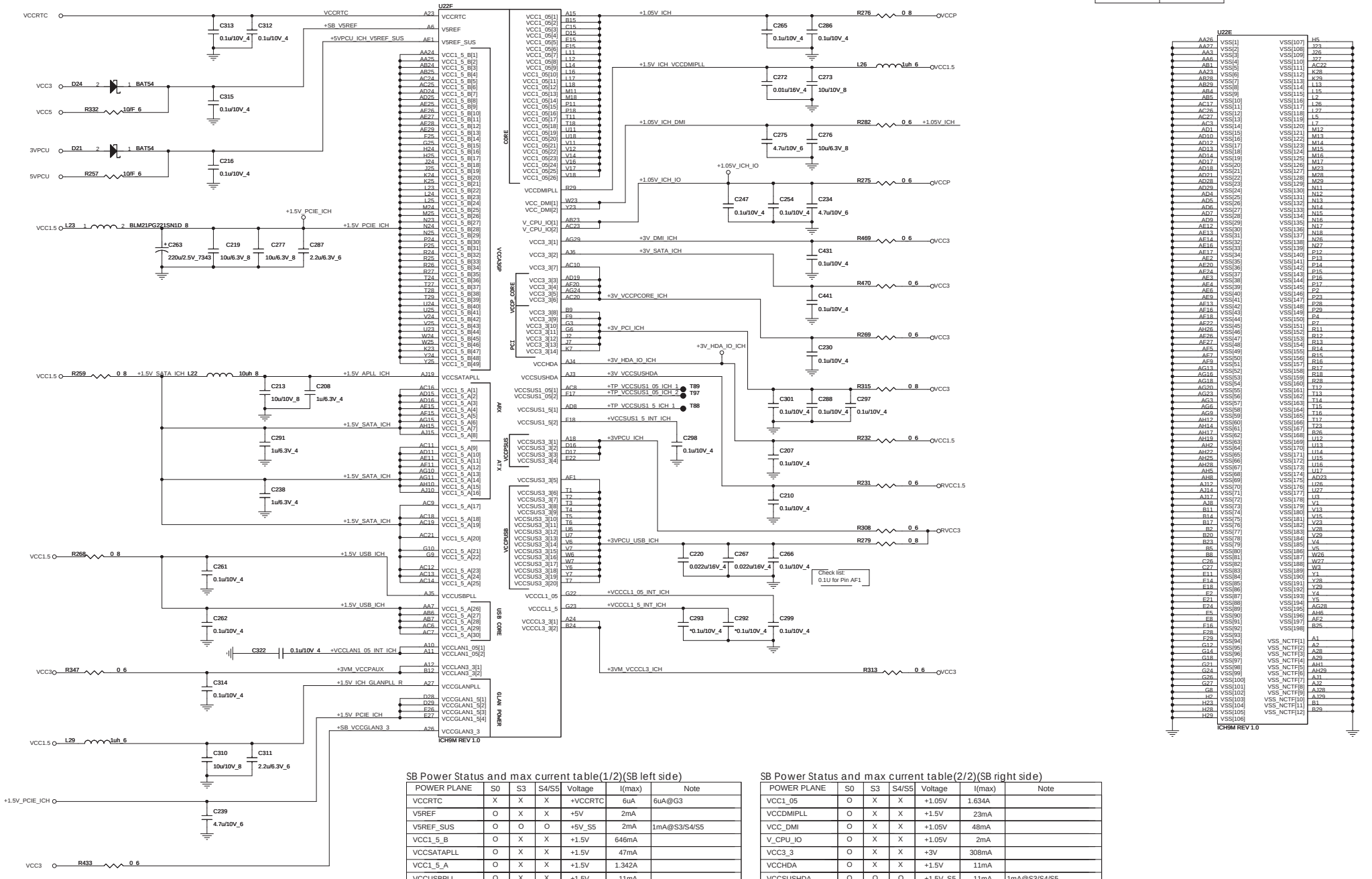
Board ID Table

BOARD_ID3 of TE1M always keep low, TE1 hasn't support TV

Board ID	ID4	ID3	ID2	ID1	ID0
NEW CARD CARD BUS					H L
CCFL Panel LED Panel				H L	
W/ G-SENSOR W/O G-SENSOR			H L		
W/ TV W/O TV		H L			
W/ HDMI W/O HDMI	H L				

BOM Option Table

Reference	Description
N/A	N/A



SB Power Status and max current table(1/2)(SB left side)

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCCRTC	X	X	X	+VCCRTC	6uA	6uA@G3
V5REF	O	X	X	+5V	2mA	
V5REF_SUS	O	O	O	+5V_S5	2mA	1mA@S3/S4/S5
VCC1_5_B	O	X	X	+1.5V	646mA	
VCCSATAPLL	O	X	X	+1.5V	47mA	
VCC1_5_A	O	X	X	+1.5V	1.342A	
VCCUSBPLL	O	X	X	+1.5V	11mA	
VCCLAN1_05	O	X	X	+1.05V	X	Powered by Vcc1_05 in S0
VCCLAN3_3	O	X	X	+3V	19mA	Tied to +3V,not +3VSUS
VCCGLANPLL	O	X	X	+1.5V	23mA	
VCCGLAN1_5	O	X	X	+1.5V	80mA	
VCCGLAN3_3	O	X	X	+3V	1mA	

SB Power Status and max current table(2/2)(SB right side)

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCC1_05	O	X	X	+1.05V	1.634A	
VCCDMIPLL	O	X	X	+1.5V	23mA	
VCC_DMI	O	X	X	+1.05V	48mA	
V_CPU_IO	O	X	X	+1.05V	2mA	
VCC3_3	O	X	X	+3V	308mA	
VCCHDA	O	X	X	+1.5V	11mA	
VCCSUSHDA	O	O	O	+1.5V_S5	11mA	1mA@S3/S4/S5
VCCSUS1_05	O	O	O	+1.05V	X	Powered by Vcc1_05 in S0
VCCSUS1_5	O	O	O	+1.5V	X	Powered by Vcc1_5_A in S0
VCCSUS3_3	O	O	O	+3VSUS	212mA	52mA@S3/S4/S5
VCCCL1_05	O	X	X	+1.05V	X	Powered by Vcc1_05 in S0
VCCCL1_5	O	X	X	+1.5V	X	Powered by Vcc1_5_A in S0
VCCCL3_3	O	X	X	+3V	19mA	Tied to +3V,not +3VSUS

Note:VCCSUS1_05 , VCCSUS1_5 are powered by VccSus3_3 in S3/S4/S5

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Quanta Computer Inc.

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	SB(4/4) POWER	1A

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DDR2 Dual channel A/B PULL UP

BOM Option Table

Reference	Description
N/A	N/A

M_A_A[14..0] → M_A_A[14..0] 7,17

M_B_A[14..0] → M_B_A[14..0] 7,17

DDRII A CHANNEL

SMDDR_VTERM

C225 C197 C201 C202 C259 C198 C280 C257 C284 C282 C199 C226 C256

0.1u/10V_4

DDRII B CHANNEL

SMDDR_VTERM

C227 C223 C224 C221 C283 C250 C260 C258 C222 C196 C281 C200 C279

0.1u/10V_4

Place one cap close to every 2 pull-up resistor terminated to SMDDR_VTERM

M_A_A3	RP21	56X2	M_A_A7	RP25	56X2
M_A_A1			M_A_A6		
M_A_A9	RP22	56X2	6,17 M_CKE3	RP37	56X2
M_A_A5			7,17 M_B_BS#2		
M_A_A2	RP28	56X2	6,17 M_ODT1	RP18	56X2
M_A_A4			6,17 M_CS#1		
M_A_A11	RP26	56X2	6,17 M_ODT3	RP31	56X2
6,17 M_CKE1			7,17 M_B_BS#0		
6,17 M_CKE0	RP23	56X2	M_A_A10	RP20	56X2
M_A_A8			7,17 M_A_BS#0		
M_A_A12	RP24	56X2	7,17 M_A_CAS#	RP19	56X2
7,17 M_A_BS#2			7,17 M_A_WE#		
7,17 M_A_BS#1	RP27	56X2	6,17 M_CS#0	RP30	56X2
M_A_A0			7,17 M_A_RAS#		
M_B_A10	RP33	56X2	7,17 M_B_CAS#	RP32	56X2
7,17 M_B_WE#			6,17 M_CS#3		
M_B_A3	RP34	56X2	M_B_A6	RP43	56X2
M_B_A1			6,17 M_CKE4		
7,17 M_B_BS#1	RP40	56X2	6,17 M_ODT2	RP39	56X2
M_B_A0			7,17 M_B_RAS#		
M_B_A7	RP42	56X2	6,17 M_ODT0	RP29	56X2
M_B_A11			M_A_A13		
M_B_A8	RP35	56X2	M_B_A13	RP44	56X2
M_B_A5			6,17 M_CS#2		
M_B_A2	RP41	56X2			
M_B_A4					
M_B_A9	RP36	56X2			
M_B_A12					

M_A_A14 — R254 — 56_4 — SMDDR_VTERM

M_B_A14 — R287 — 56_4 — SMDDR_VTERM

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Quanta Computer Inc.

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	DDR RES. ARRAV	1A
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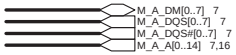
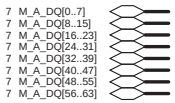
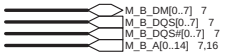
DDR II DIMM Socket

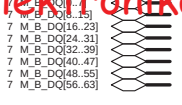
BOM Option Table

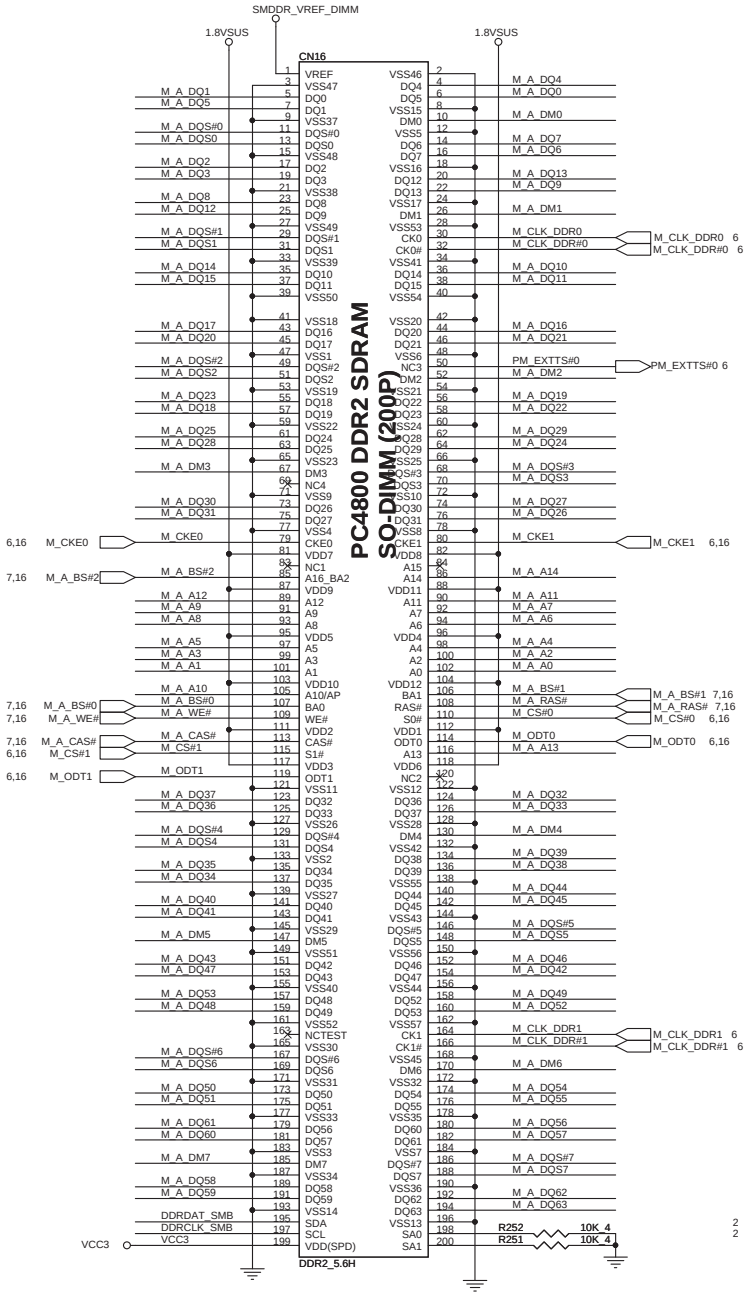
Reference	Description
N/A	N/A

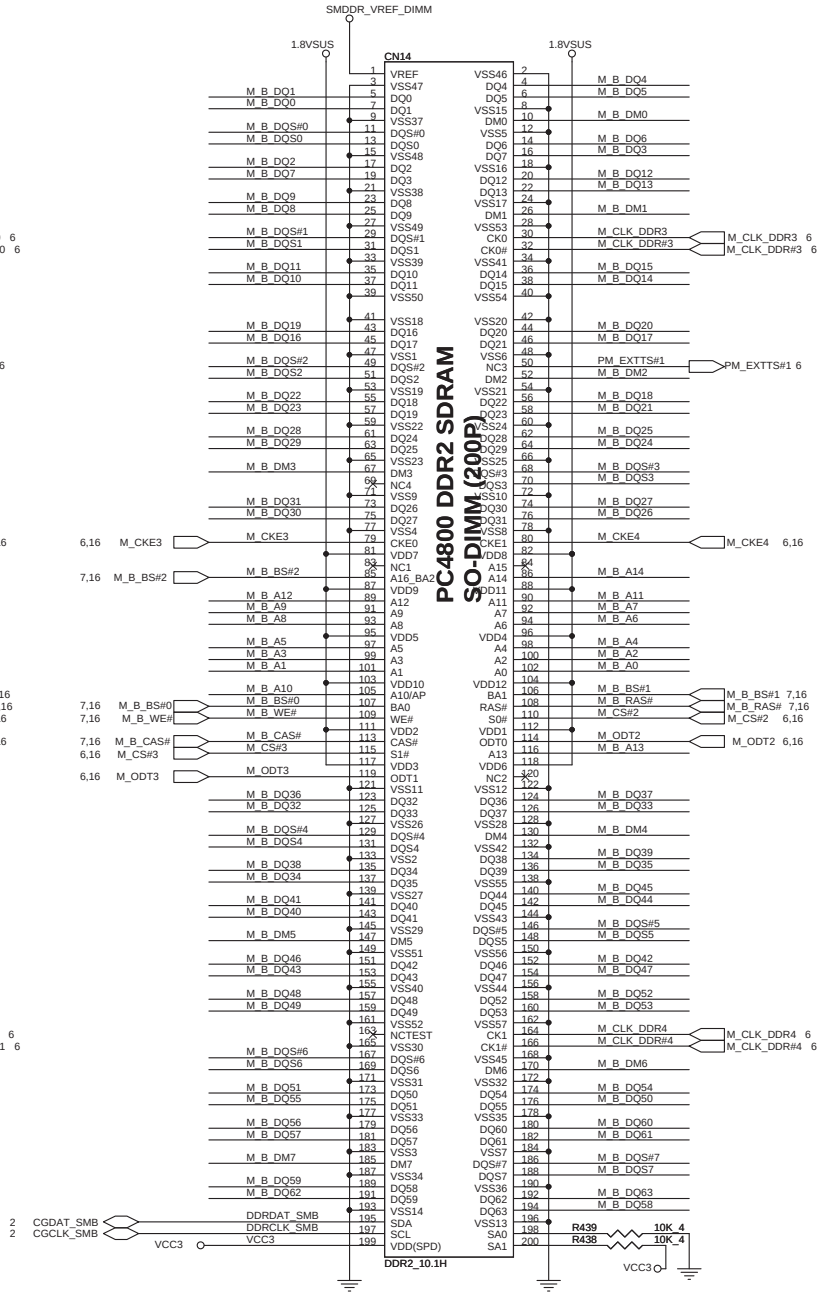


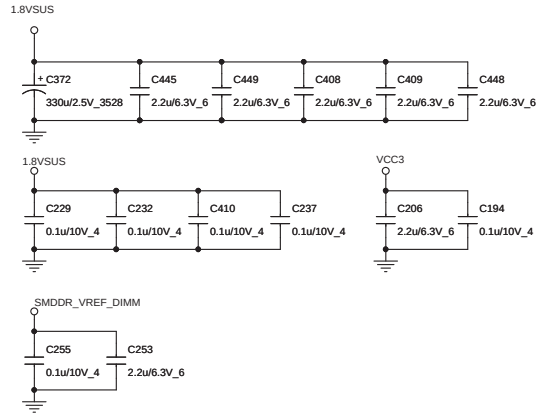


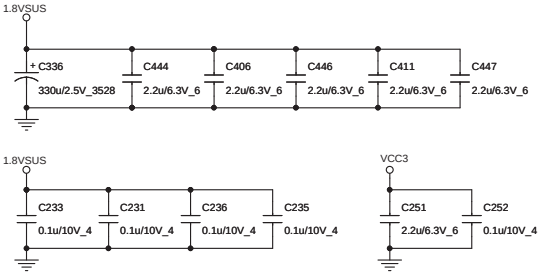


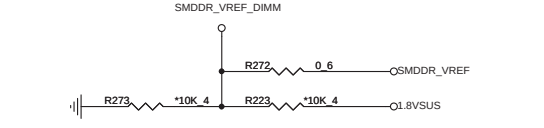












PROJECT : PB5/6

Quanta Computer Inc.

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	DDR SO-DIMM	1A
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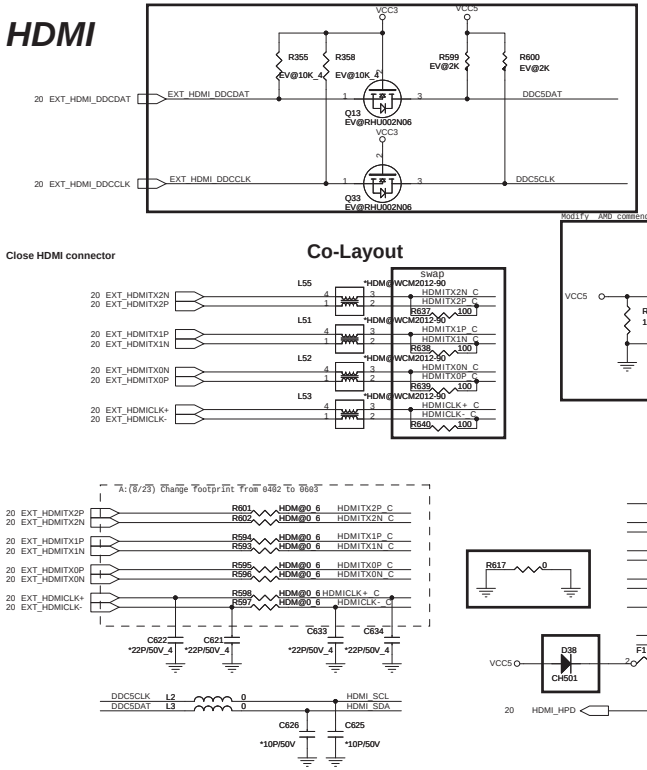
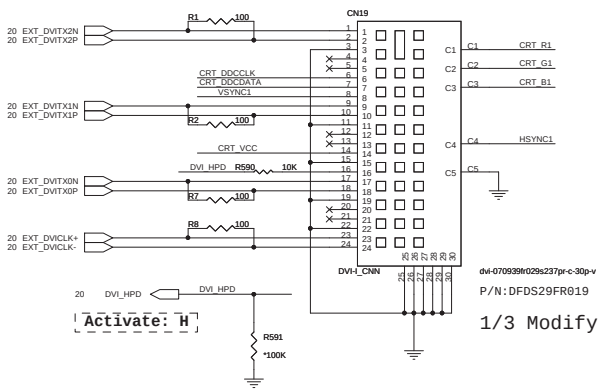
HDMI



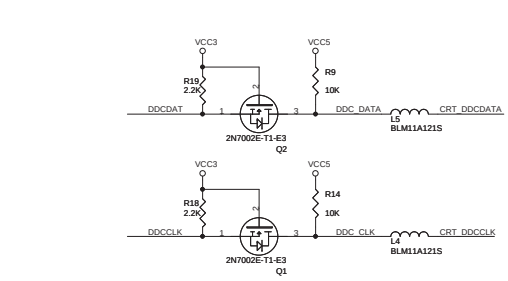
DVI

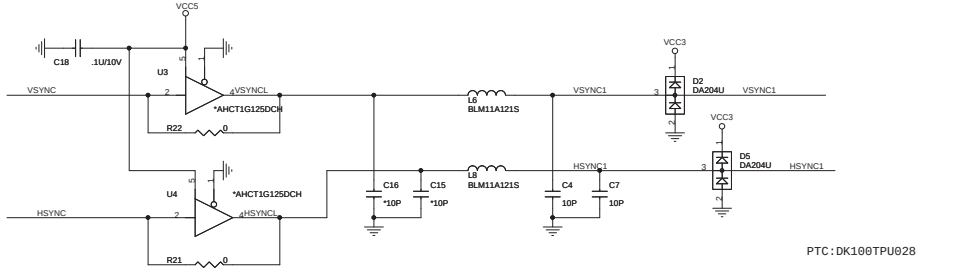
DVI-I

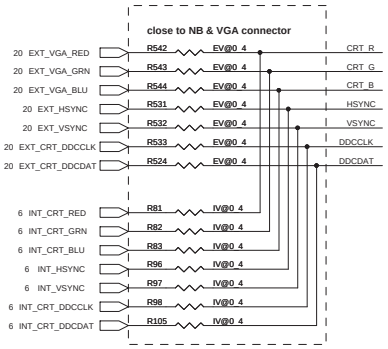
For EMI

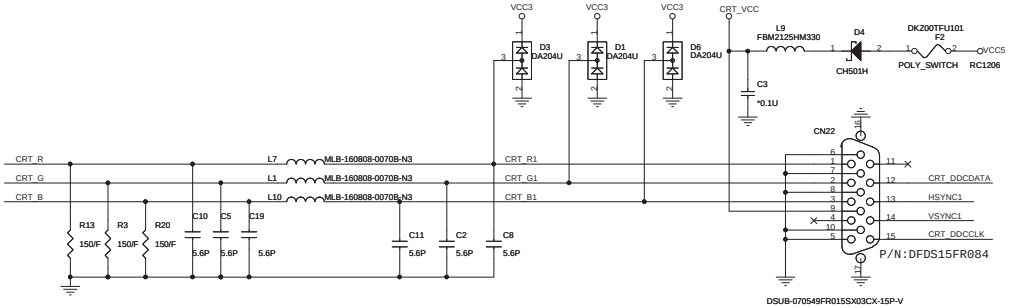


CRT PORT









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Quanta Computer Inc.

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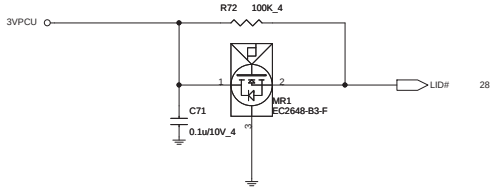
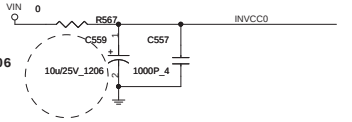
LCD TYPE CONNECTOR

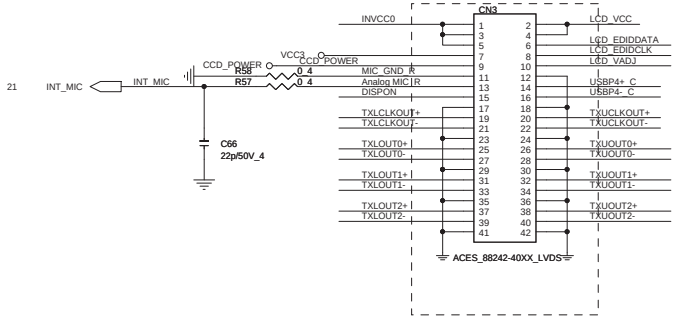
HALL SENSOR



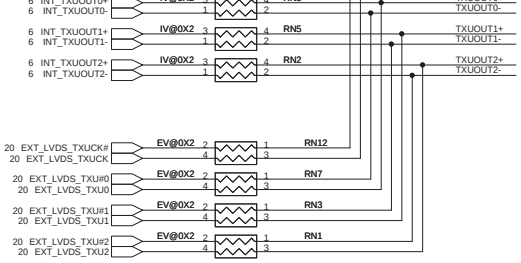
8/13 Change Size To 1206

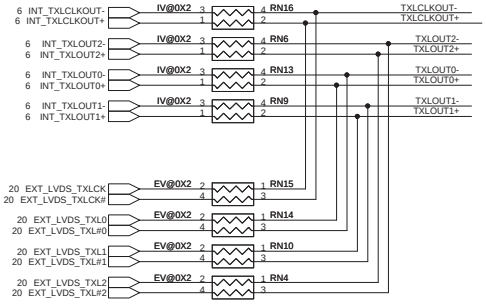


10/22 update p/n From DFHS40FS825 to DFWF40MS000

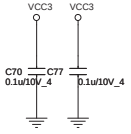


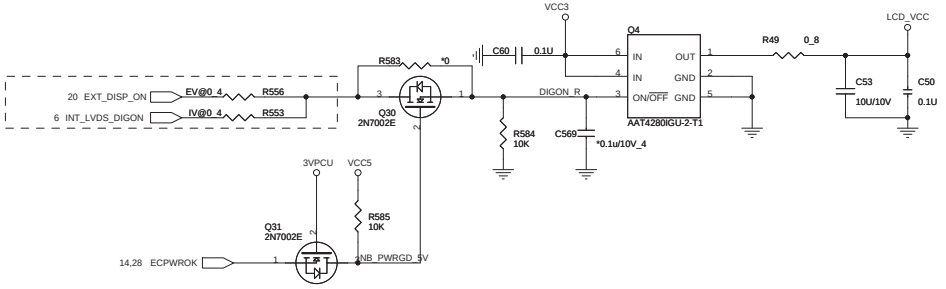
LCD PANEL MODULE

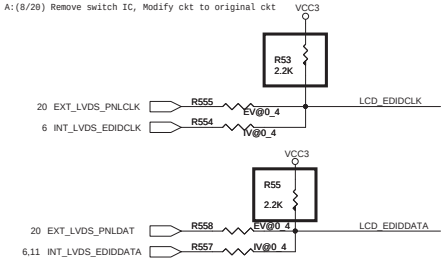




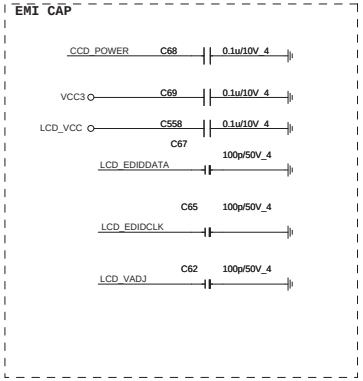
11/01 add stitch cap for LVDS

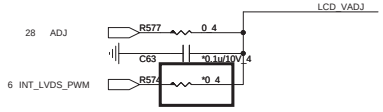






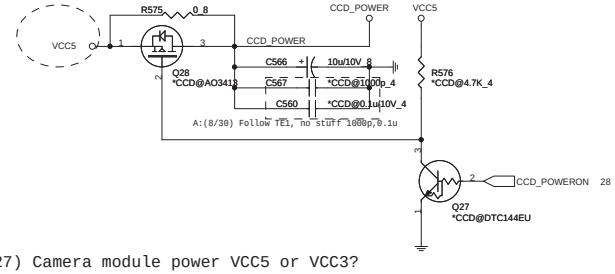
EMI CAP

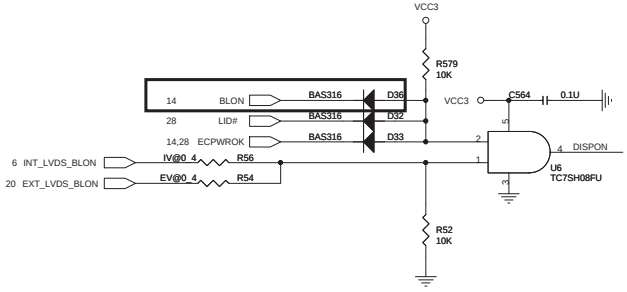


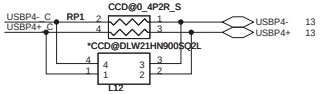


BTO

CAMERA MODULE







A:(11/27) Camera module power VCC5 or VCC3?

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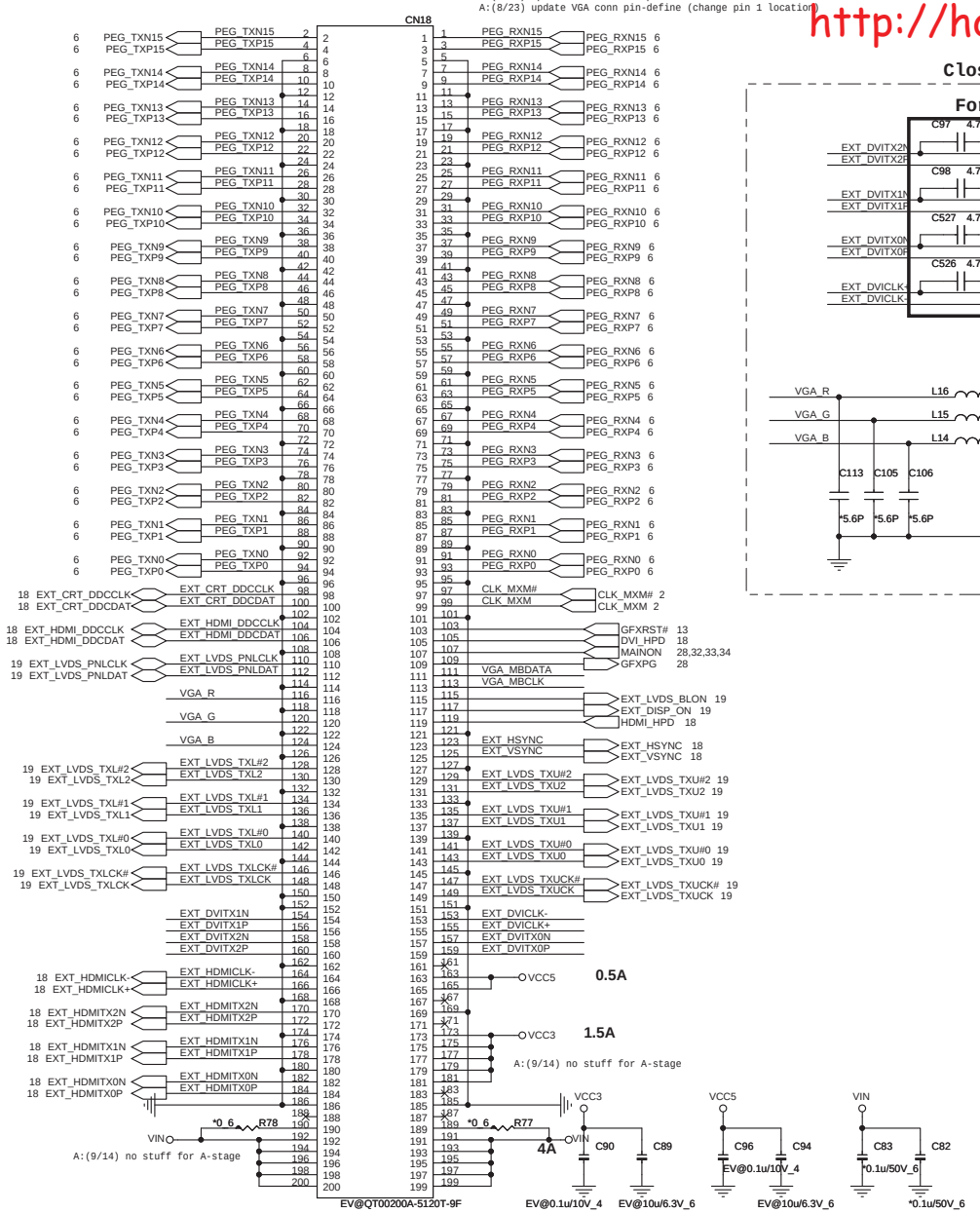
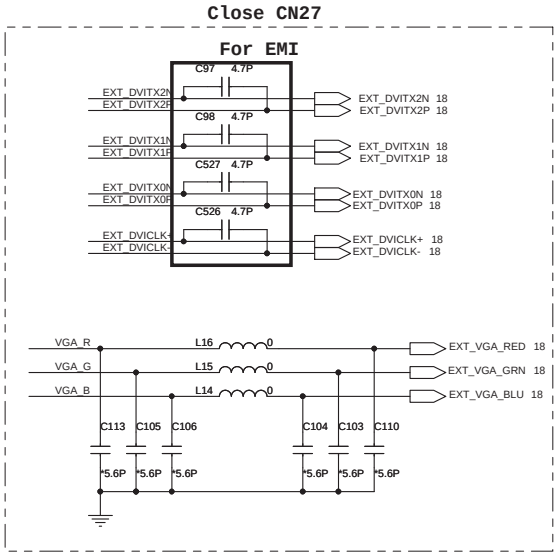
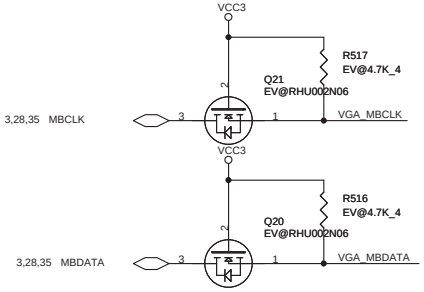
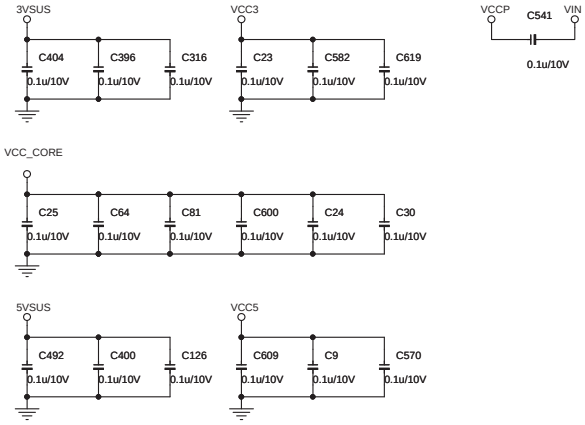
	LCD CONN& CAREMA	1A
Date: Friday, May 30, 2008	Sheet 19 of 35	

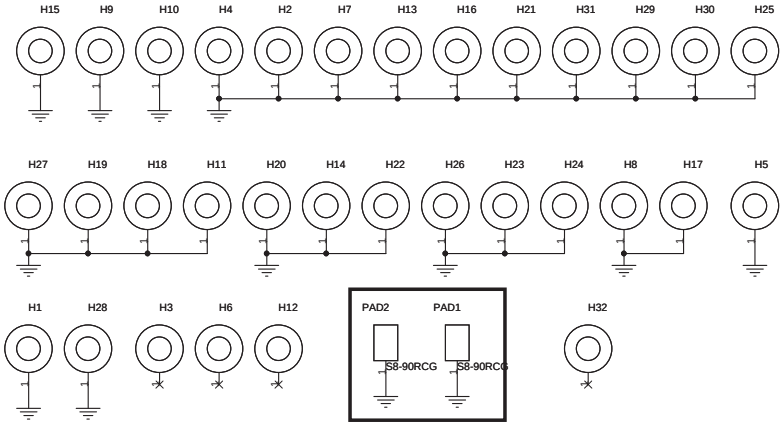
A:(8/18) update VGA conn footprint base on Allan information
A:(8/23) update VGA conn pin-define (change pin 1 location)











PROJECT : PB5/6

Quanta Computer Inc.

Size	Document Number	Rev
	MXM CONNECTOR	1A

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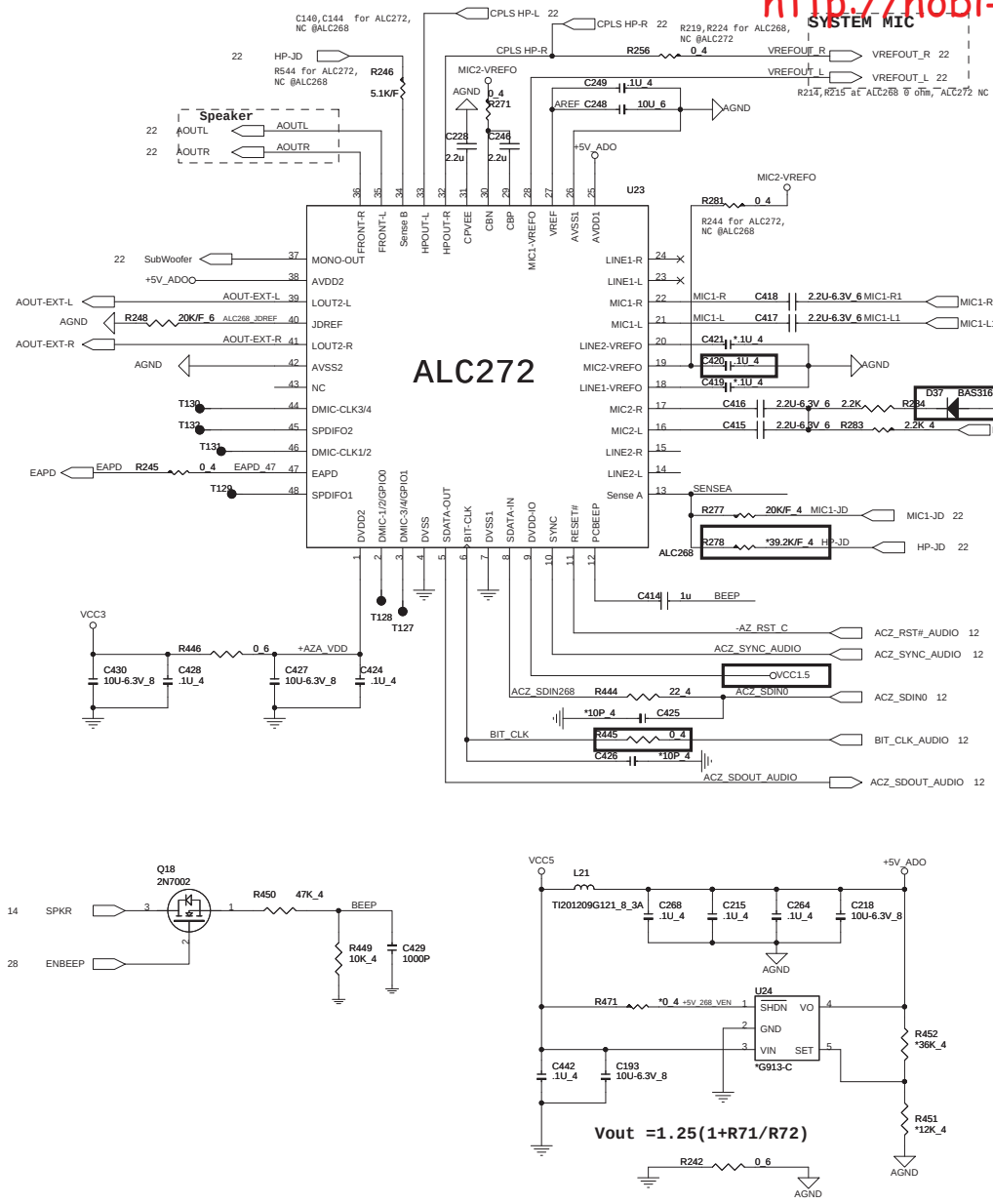
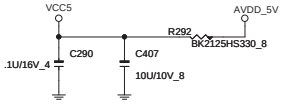
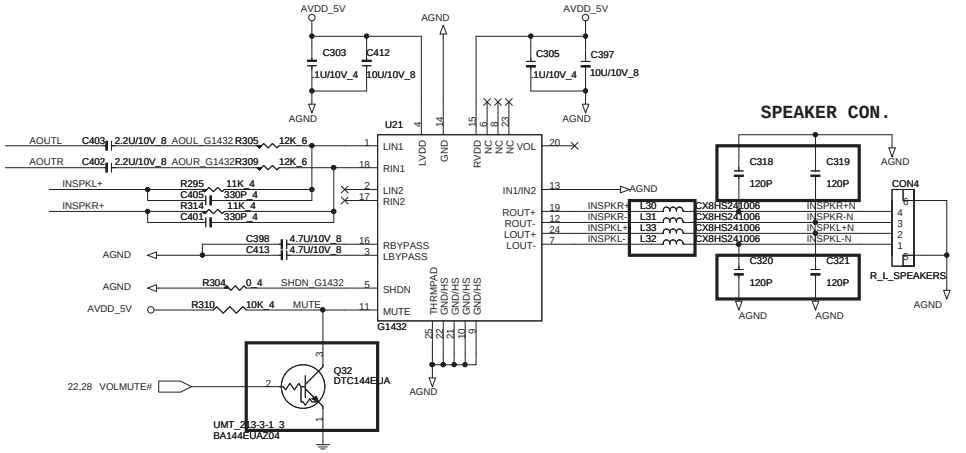
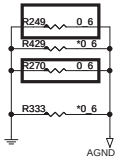








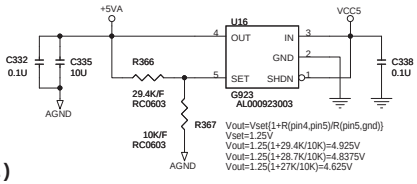
PROJECT : PB5/6

Quanta Computer Inc.

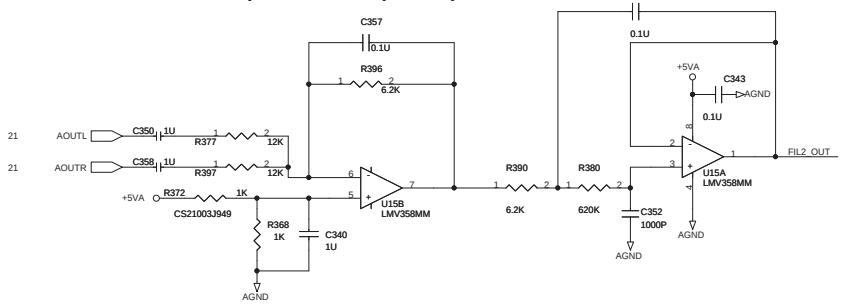
Size	Document Number	Rev
	ALC272/AMP	1A

Date: Friday, May 30, 2008 Sheet 21 of 35

LM358 Power

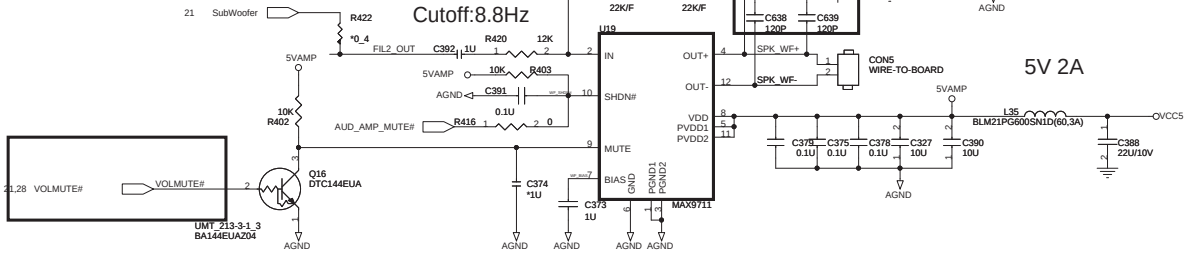


Mixer & 1nd order low pass filter(338HZ)



2nd order low pass filter(338HZ)

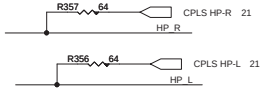
Cutoff:8.8Hz



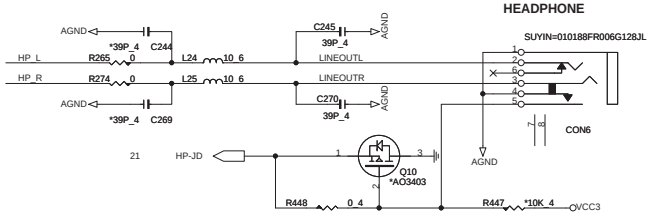
Cutoff:770Hz

5V 2A

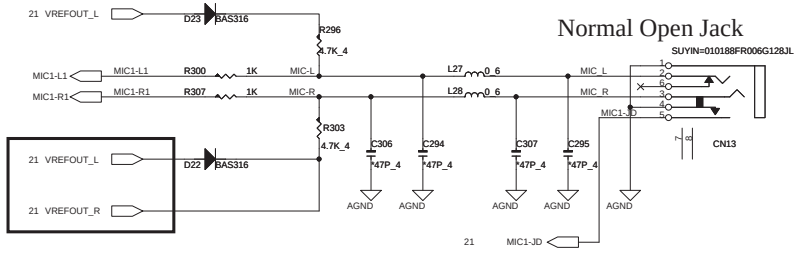
HP



Normal Open Jack



SYSTEM MIC

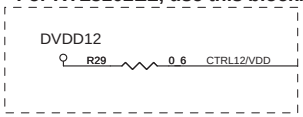


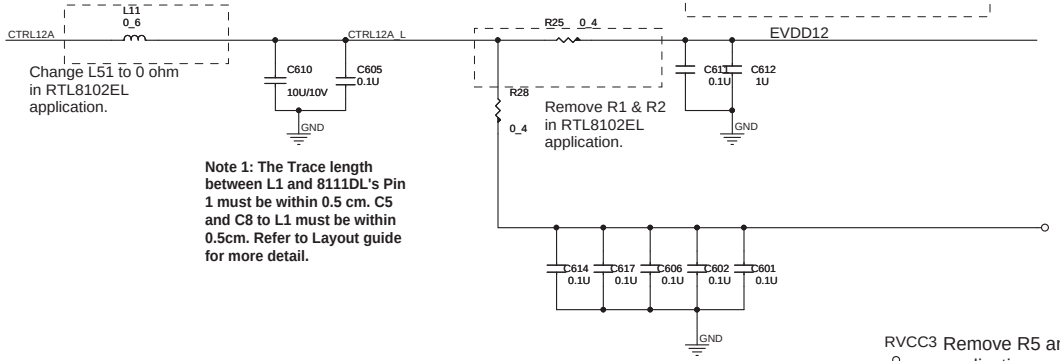
Normal Open Jack

SUYIN=010188FR006G128JL

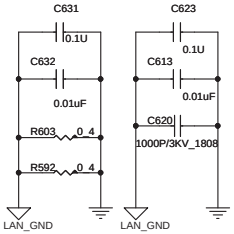
LAN_REALTEK_RTL8102E

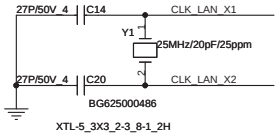
For RTL8102EL, use this block.

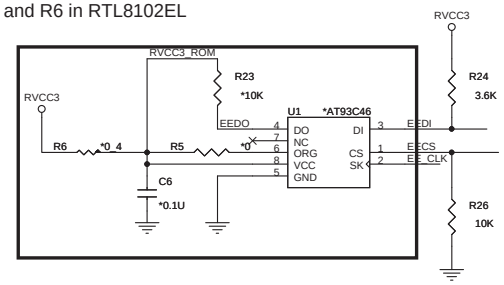


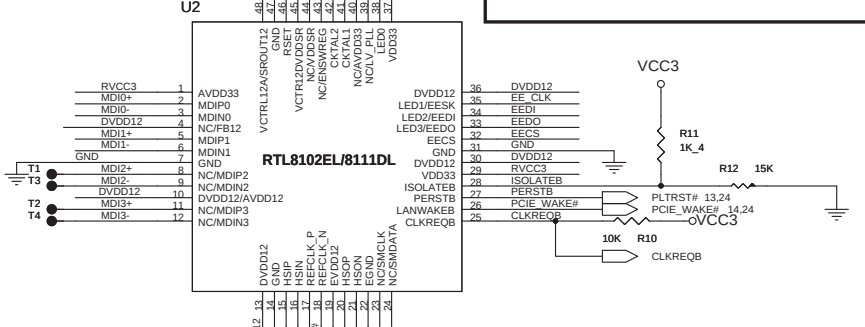


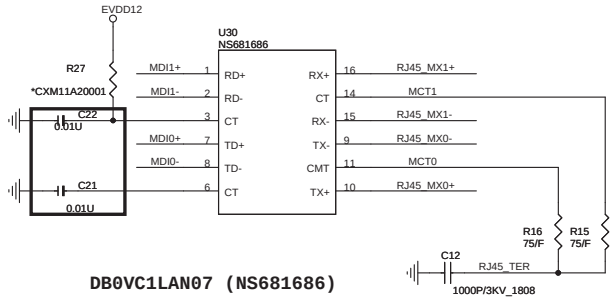
Note 1: The Trace length between L1 and 8111DL's Pin 1 must be within 0.5 cm. C5 and C8 to L1 must be within 0.5cm. Refer to Layout guide for more detail.



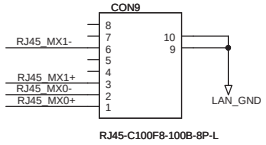


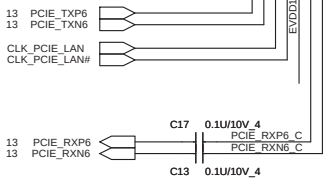






DB0VC1LAN07 (NS681686)





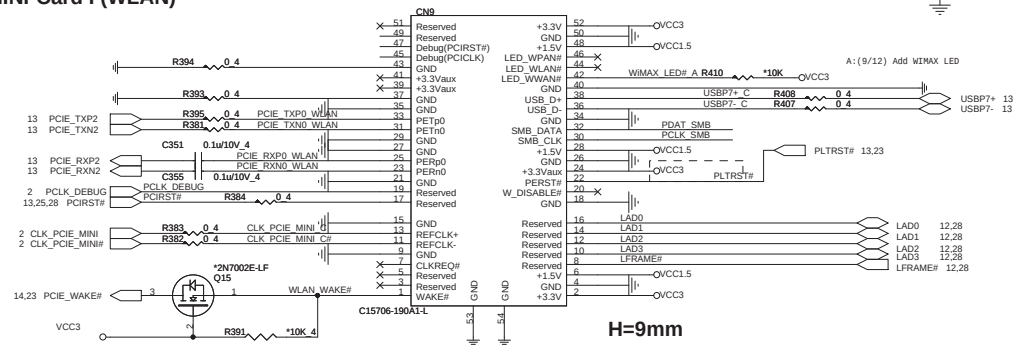
PROJECT : PB5/6

Quanta Computer Inc.

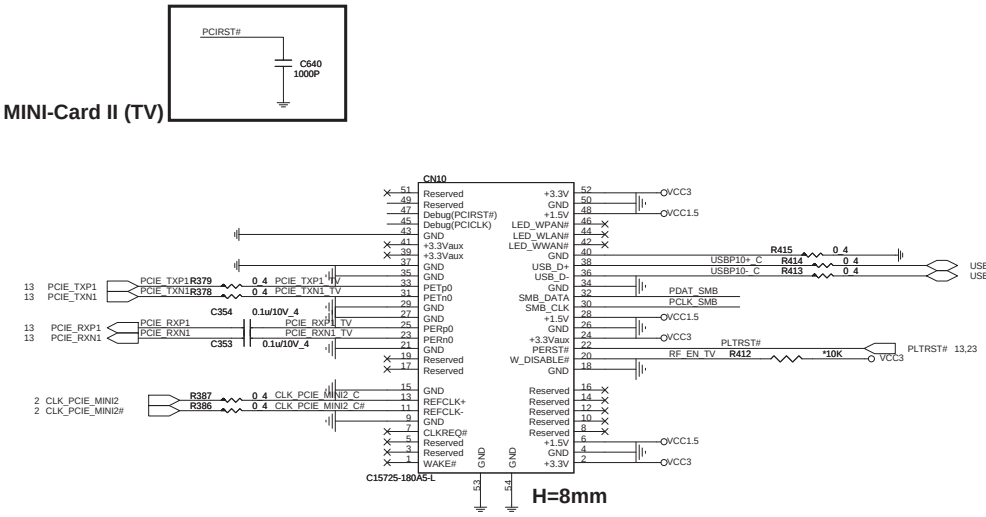
Size	Document Number	Rev
	LAN_REALTEK_RTL8102EL	1A
Date: Friday, May 30, 2008	Sheet 23 of 35	

A:(8/18) Due to EC assign Pin111 to other function
Remove uR_SOUT_CR from EC
A:(8/23) Remove uR_SWD from EC

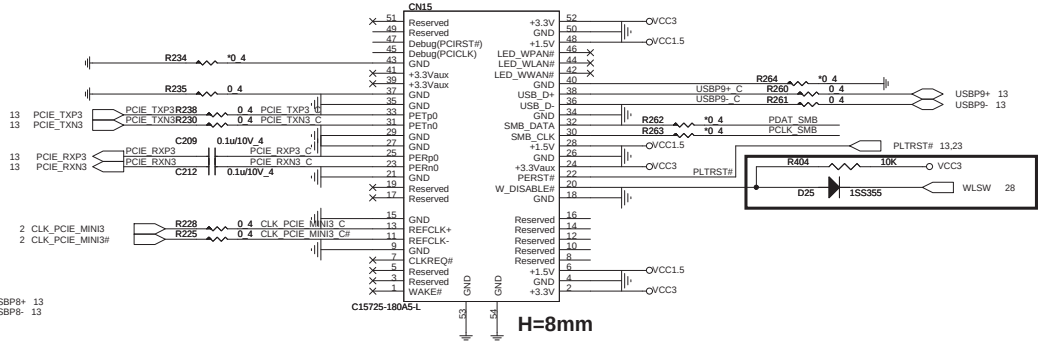
MINI-Card I (WLAN)

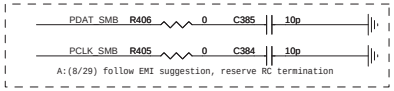


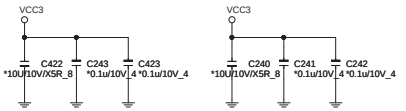
MINI-Card II (TV)

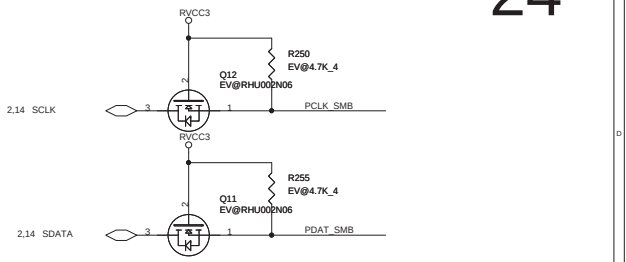


ROBSON









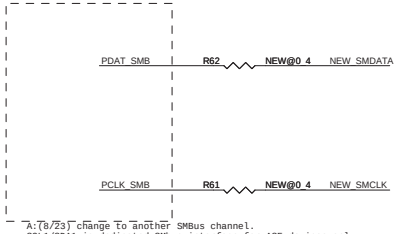
A:(9/7) per TI FAE suggestion:
(1)Please keep all Input and Output capacitor value > 4.8uF (0.1uF +4.7uF)
(2)Please put these caps closed to IC
(3)R4101(pin 19,OC#) value should change to 2k ohm.

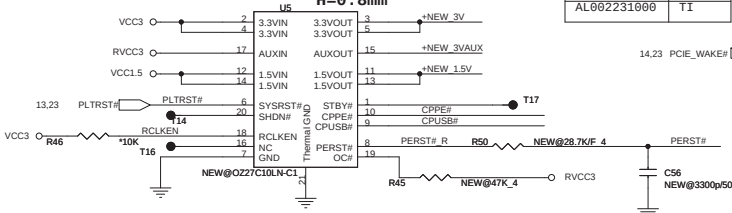
NEW CARD'S POWER SWITCH

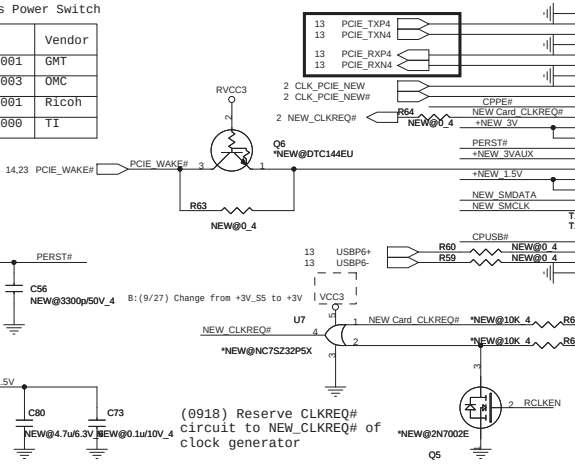
CPPE# : (Internal Pull Up , active low when card support PCIE)
CPUSB# : (Internal Pull Up , active low when card support USB)
SHDN# : (Internal Pull Up)

New Card's Power Switch

QCI PN	Vendor
AL000577001	GMT
AL027C10003	OMC
AL005538001	Ricoh
AL002231000	TI

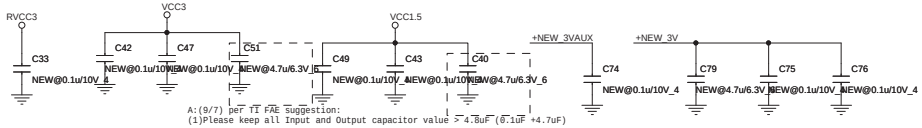






Header 130801-1 DFHD26MR074
Ejector 131851-V FBBL5001010

(0918) Reserve CLKREQ# circuit to NEW_CLKREQ# of clock generator



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Quanta Computer Inc.

Size	Document Number	Rev
	MINI CARD/NEW CARD	1A
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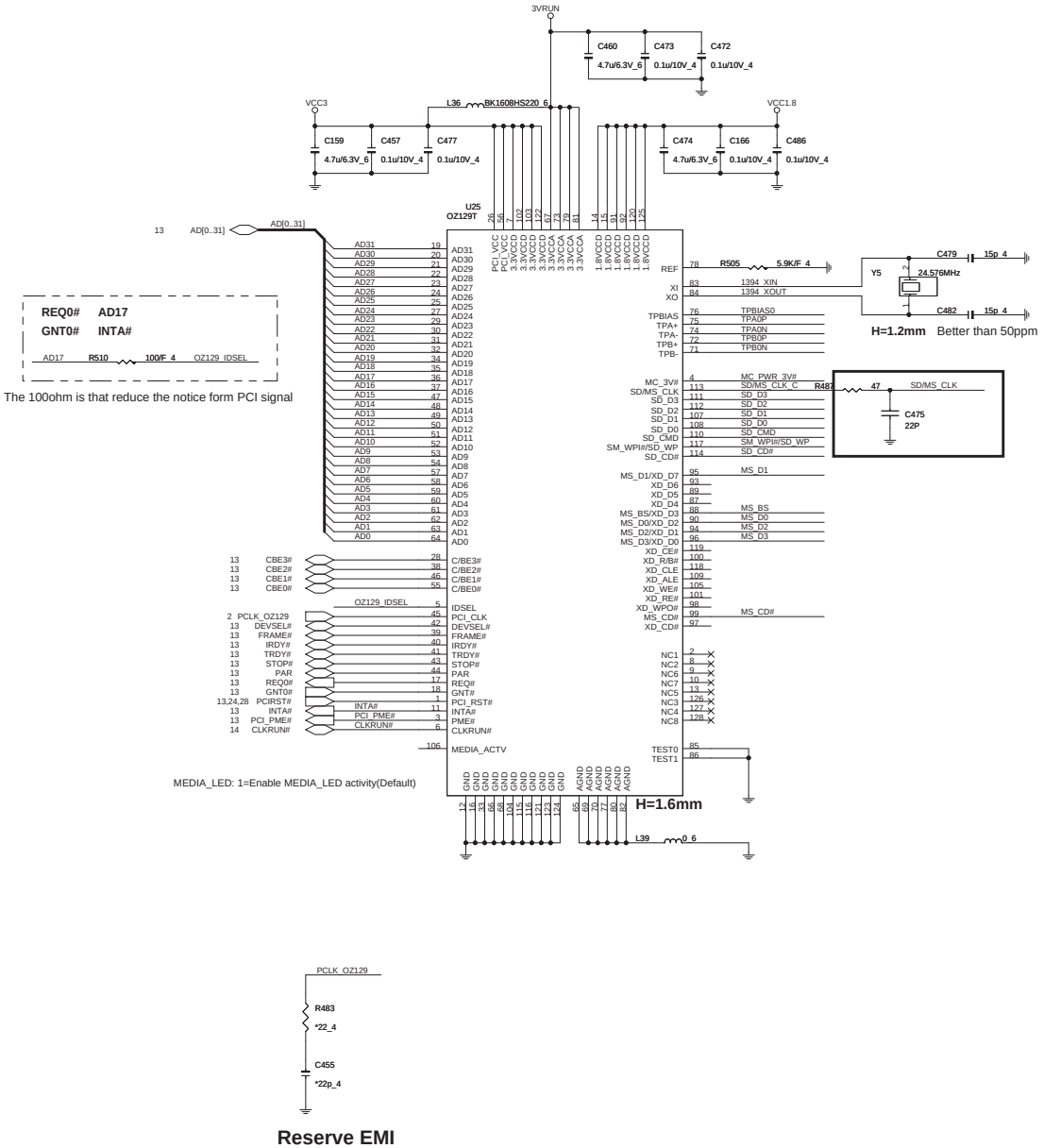
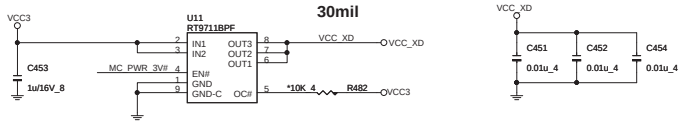
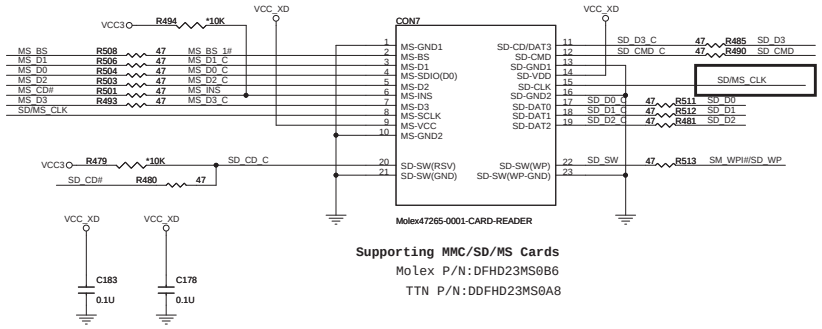
CARD READER



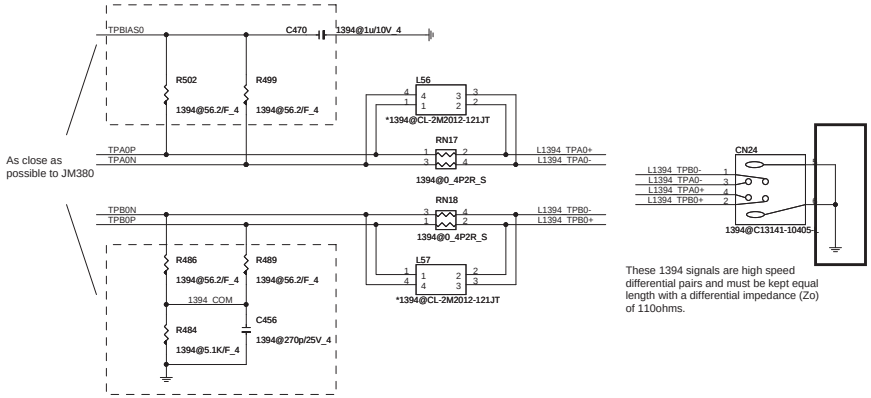
CARD READER POWER



4 IN 1 CONN



1394



PROJECT : PB5/6
Quanta Computer Inc.

Size	Document Number	Rev
	OZ129 (CARD READER / 1394)	1A

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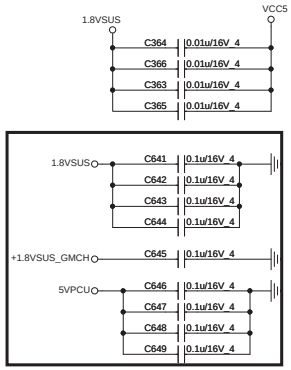
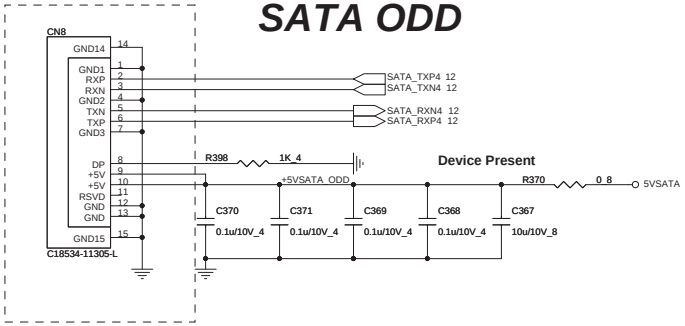
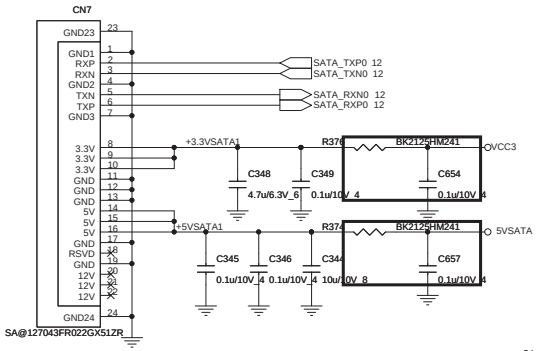


SATA ODD

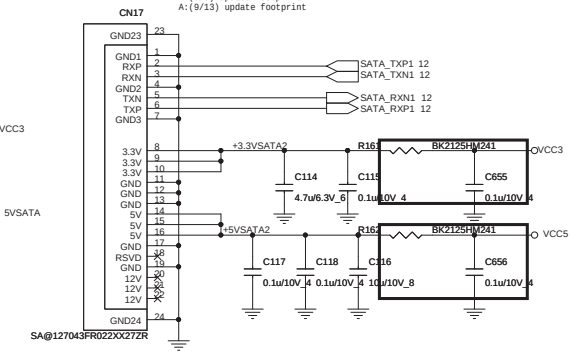


SATA HDD

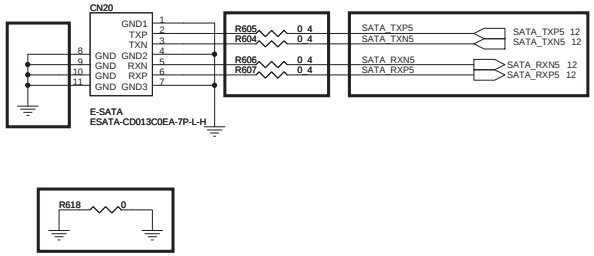


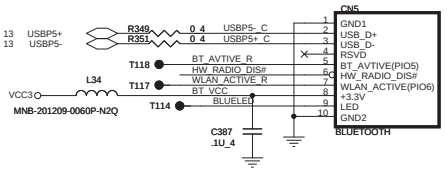
2'nd SATA HDD

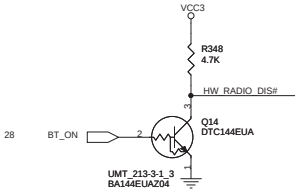
A:(9/5) update footprint
A:(9/13) update footprint

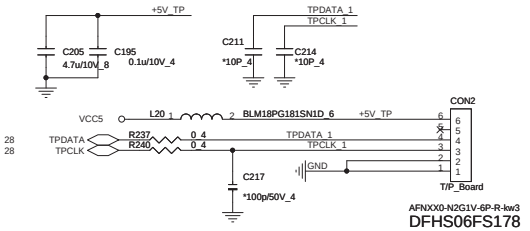


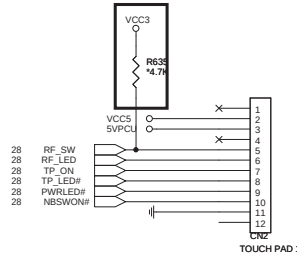
PROJECT : PB5/6		
Quanta Computer Inc.		
Size	Document Number: SATA / HyberFLASH	Rev: 1A
Date: Monday, June 02, 2008	Sheet 26 of 35	

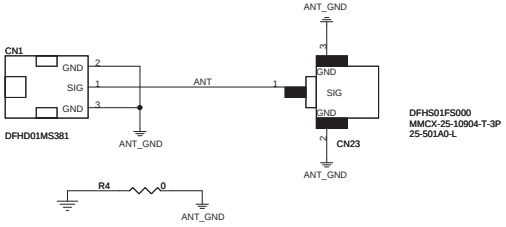


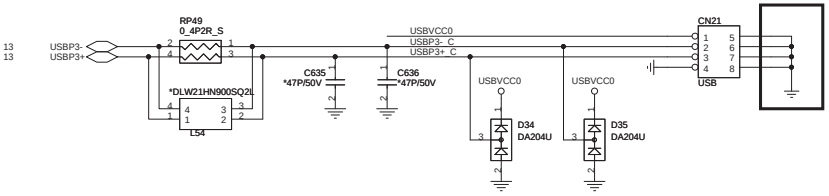


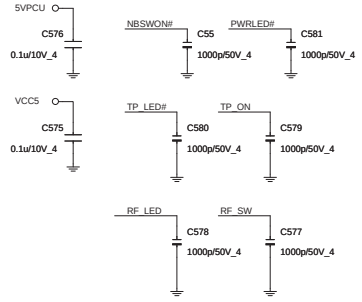


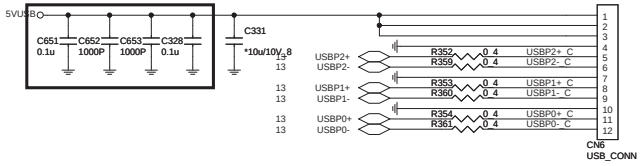






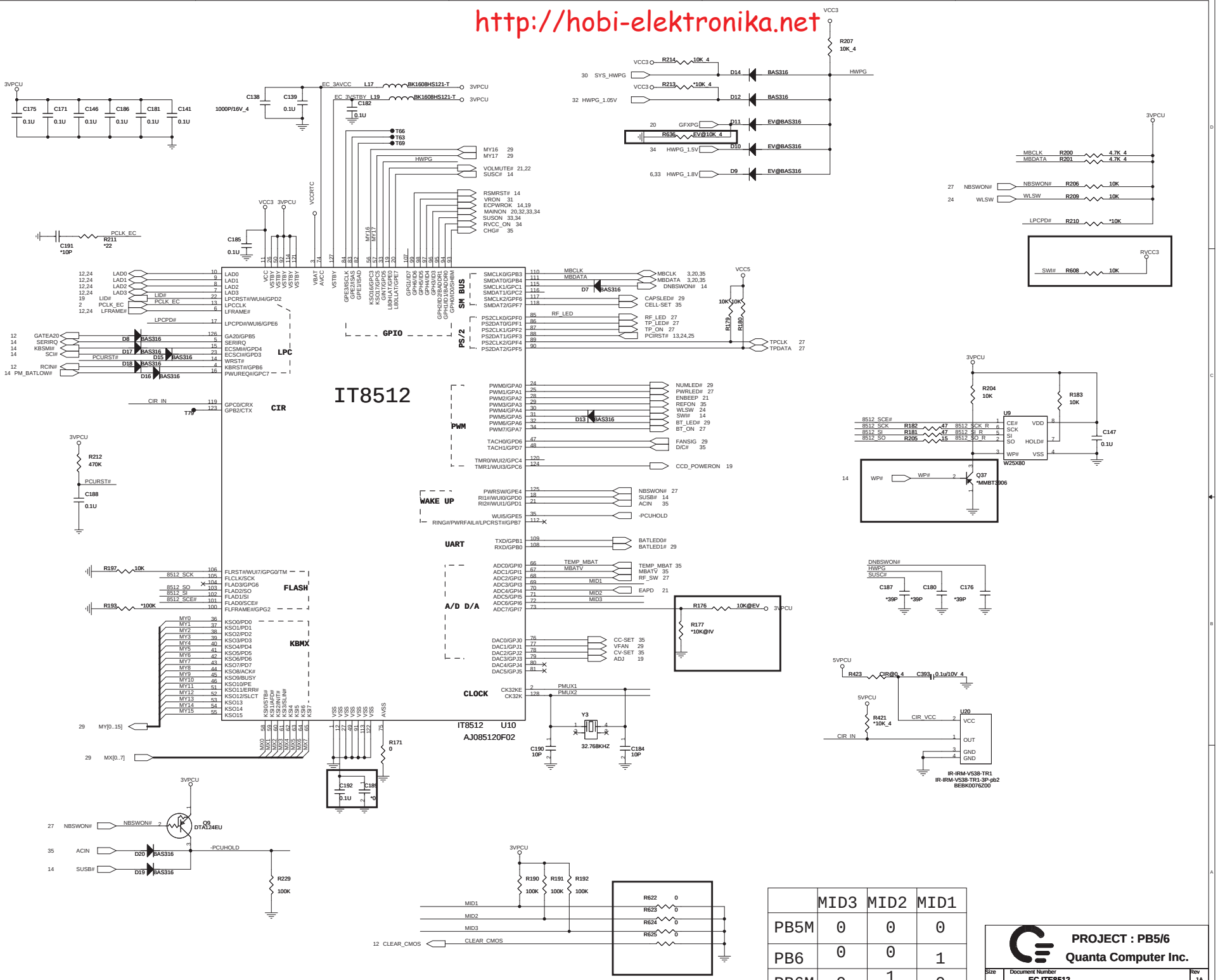






PROJECT : PB5/6
Quanta Computer Inc.

Size	Document Number	Rev
	ESATA/SW/ TP/ USB /BT/TV	1A
Date: Wednesday, June 04, 2008	Sheet 27 of 35	



	MID3	MID2	MID1
PB5M	0	0	0
PB6	0	0	1
PB6M	0	1	0

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Quanta Computer Inc.

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	EC ITE8512	1A

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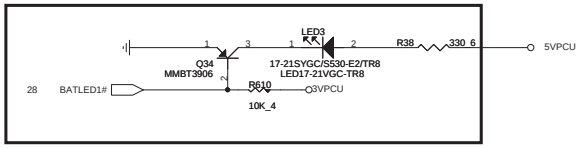
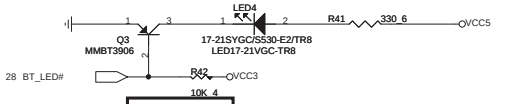
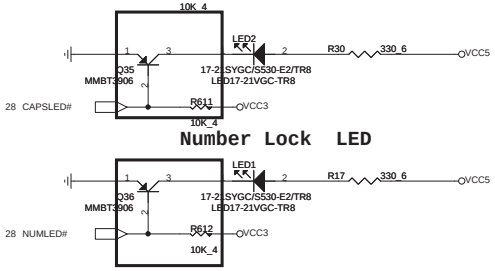
BATTERY CHARGE LED



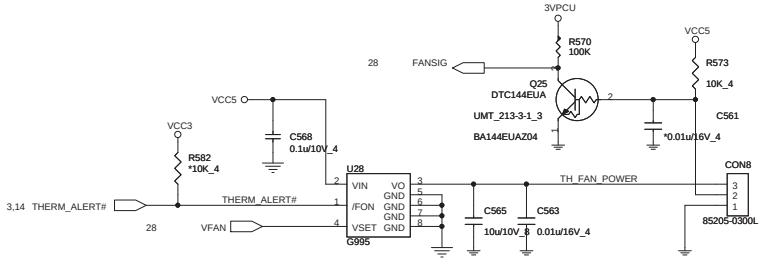
BLUE TOOTH LED



Number Lock LED



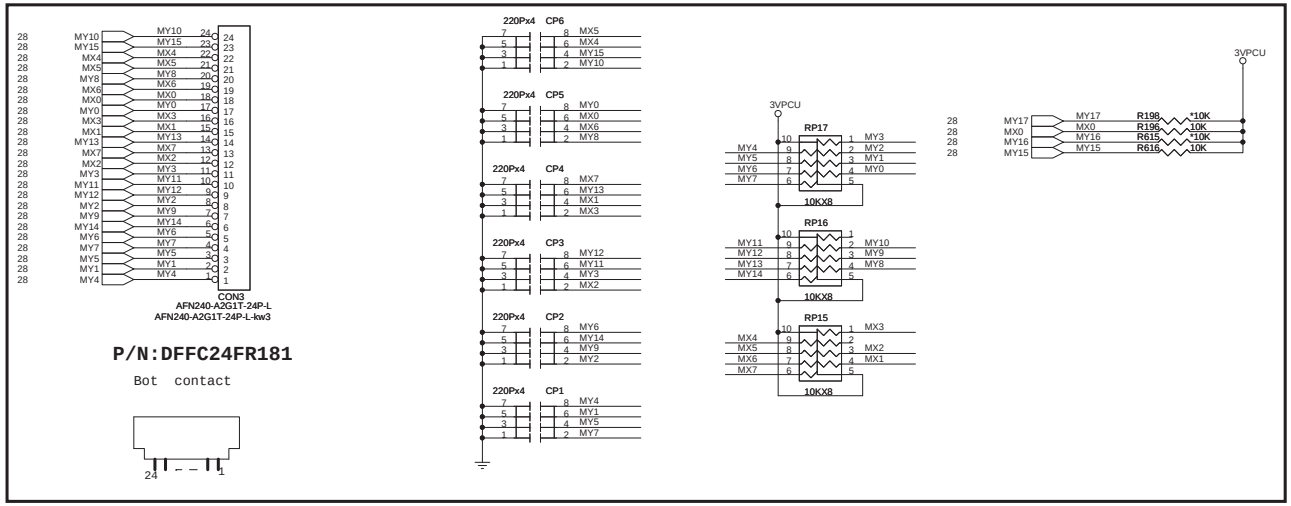
CPU FAN



FANPWR = 1.6*VSET

G995/Pin1- internal pull high (+5V)

Keyboard CONN



P/N:DFFC24FR181

Bot contact

	15"	17"
CAPSLED K_LED_P (Pin 31)	V	V
FN_F10 K_LED_P (Pin 6)	V	
NUMLED K_LED_P (Pin 1)	V	V

PROJECT : PB5/6

Quanta Computer Inc.

Size	Document Number	Rev
	SW/LED/Keyboard	1A

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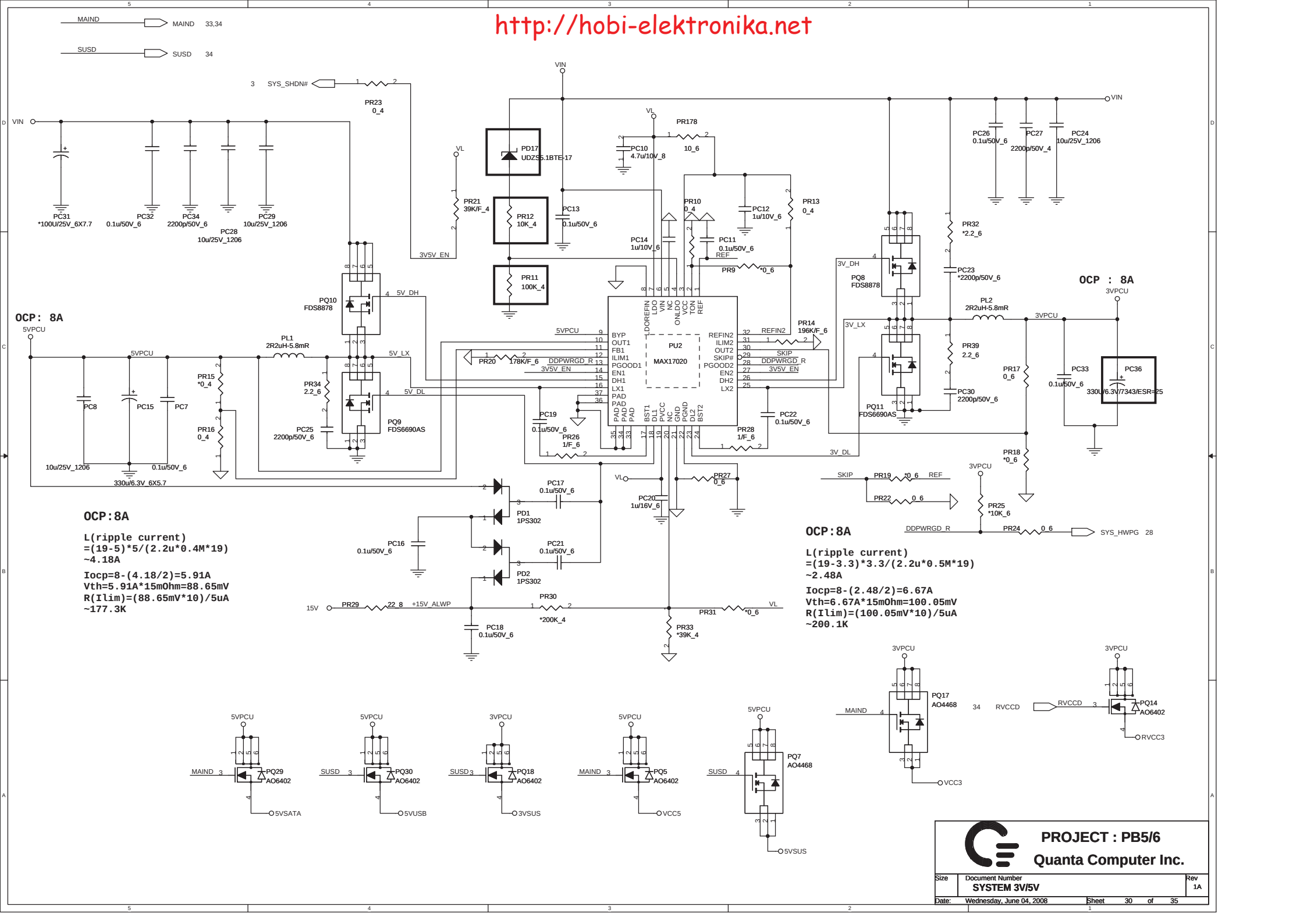
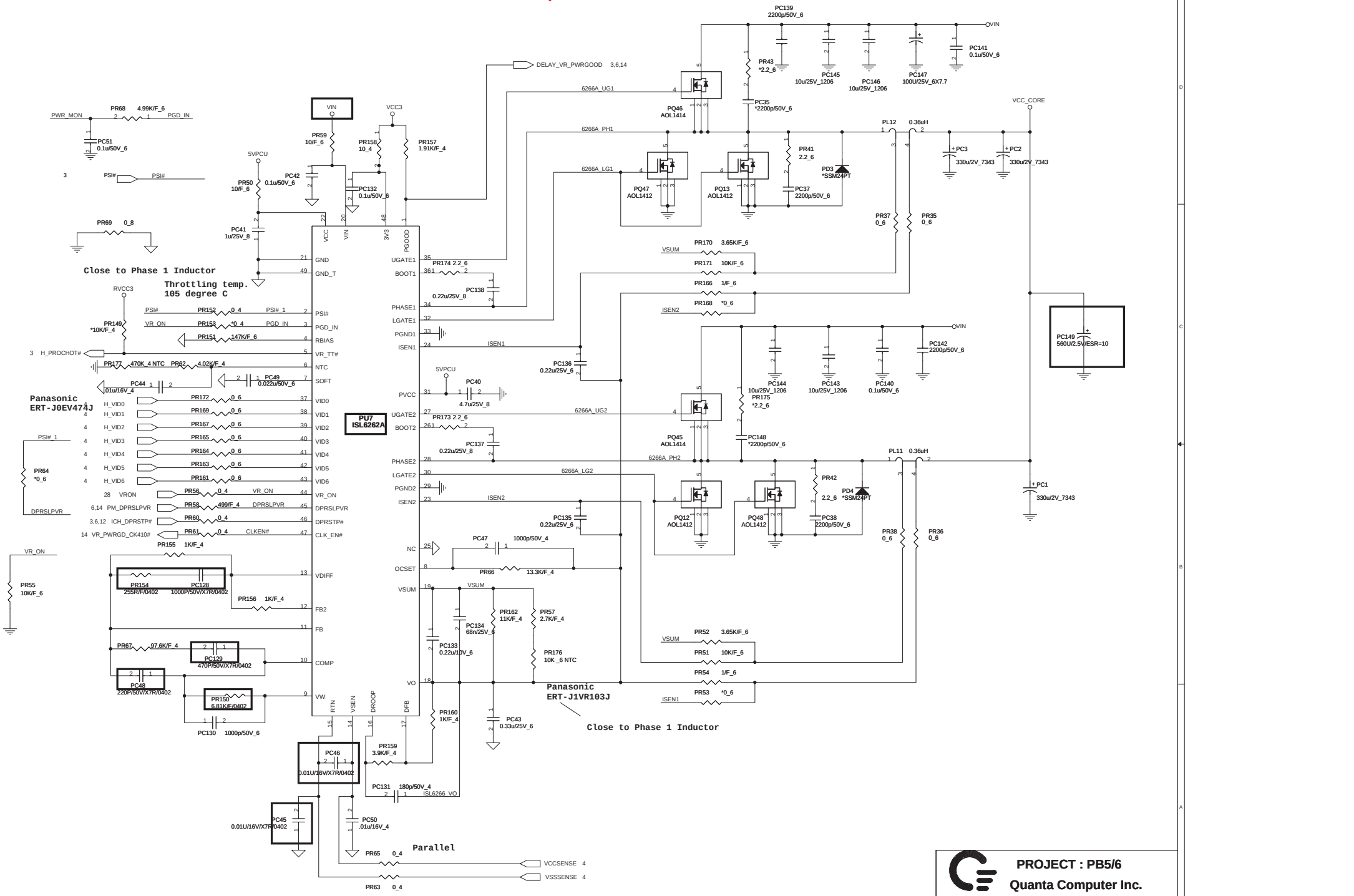
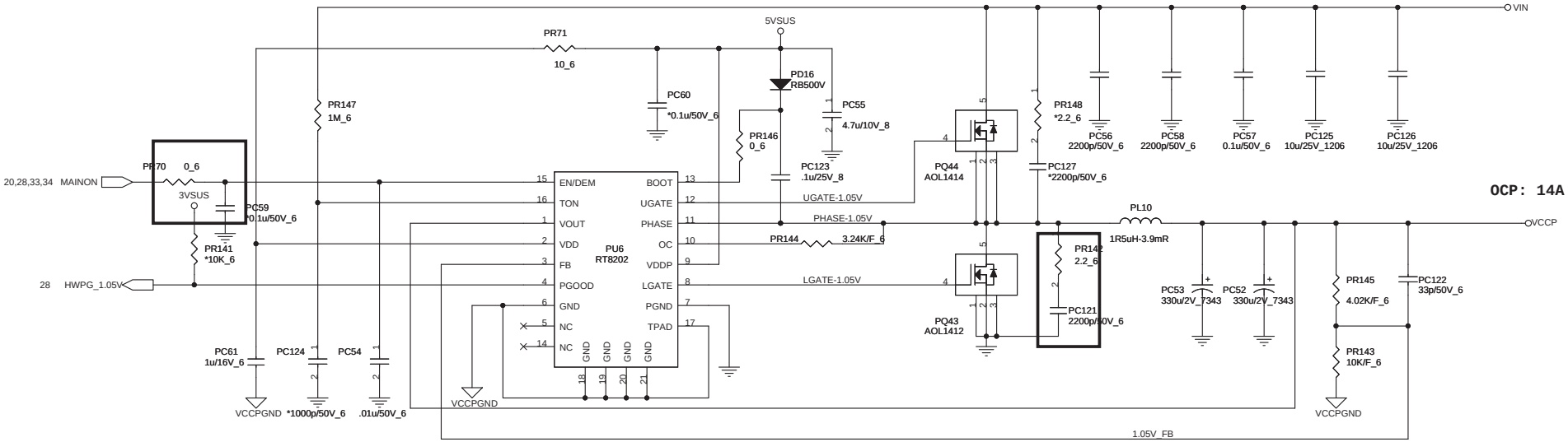


PROJECT : PB5/6		
Quanta Computer Inc.		
Size	Document Number: SYSTEM 3V/5V	Rev: 1A
Date: Wednesday, June 04, 2008	Sheet 30 of 35	



Size	Document Number		Rev
	CPU CORE		1A
Date:	Wednesday, June 04, 2008	Sheet 31 of 35	

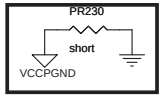
PROJECT : PB5/6
Quanta Computer Inc.



OCP: 14A

TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)



Rds*OCP=RILIM*20uA
AOL1412 Rds=4.6mOhm
14A OCP --- OC=3.22K

VOUT=(1+R2/R3)*0.75

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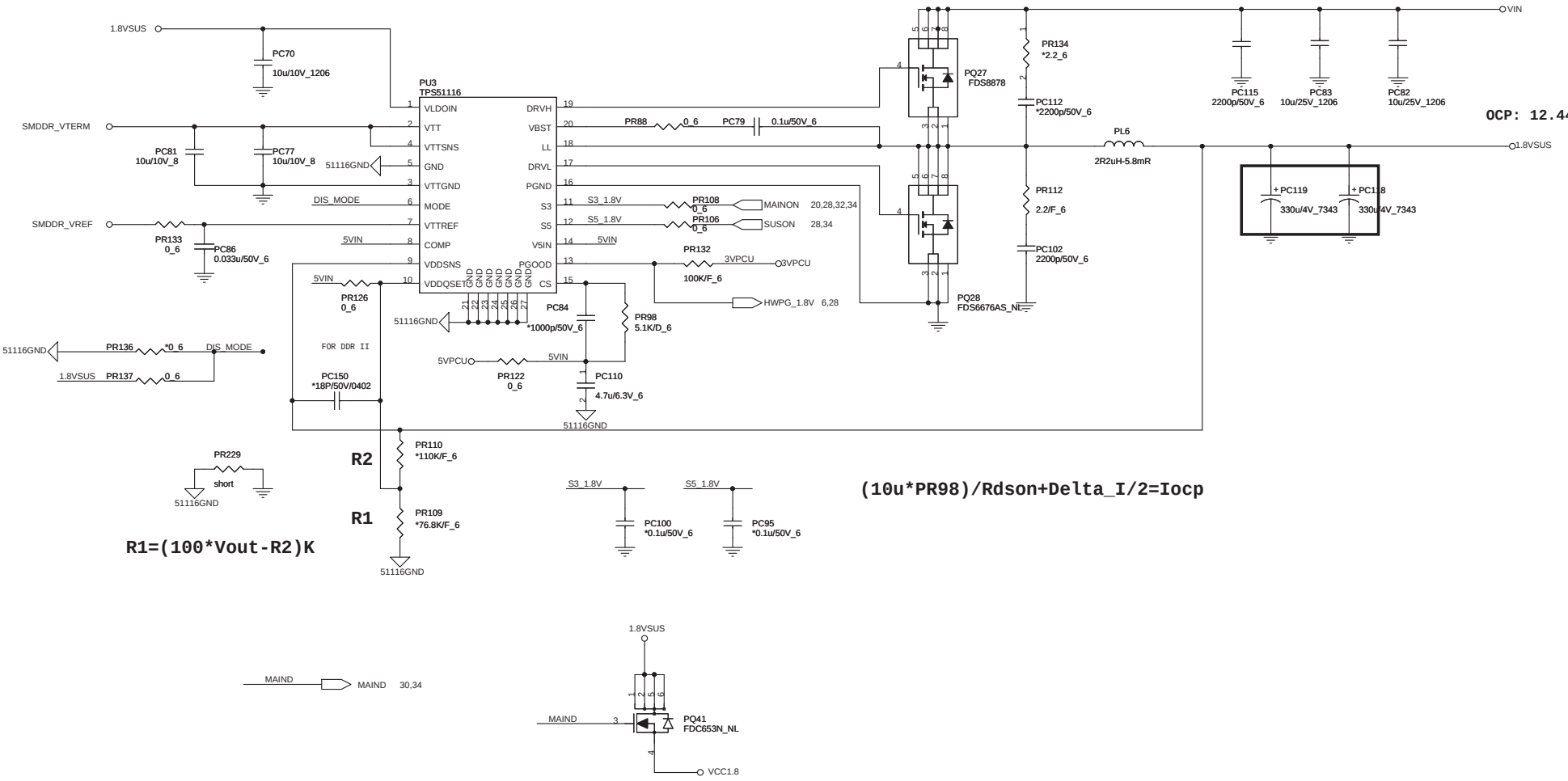
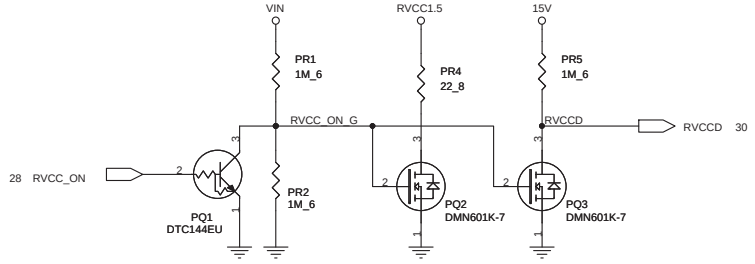
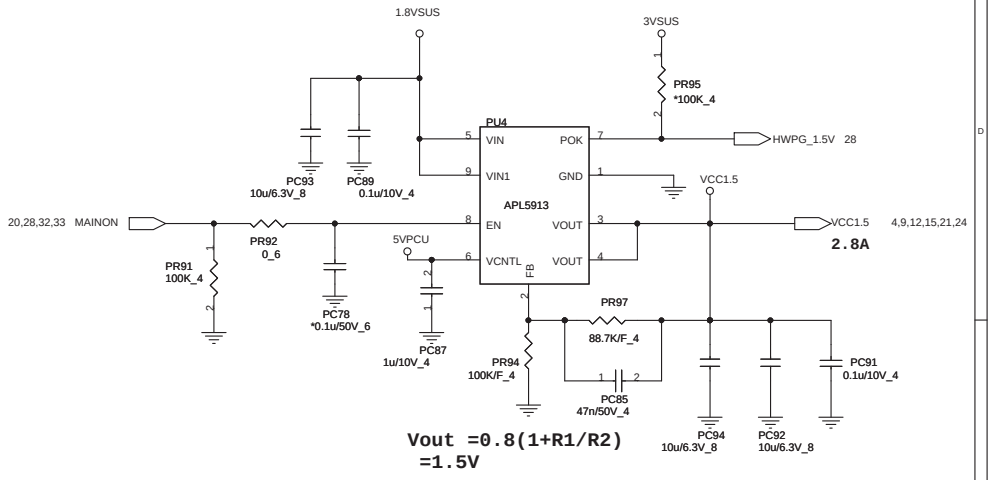
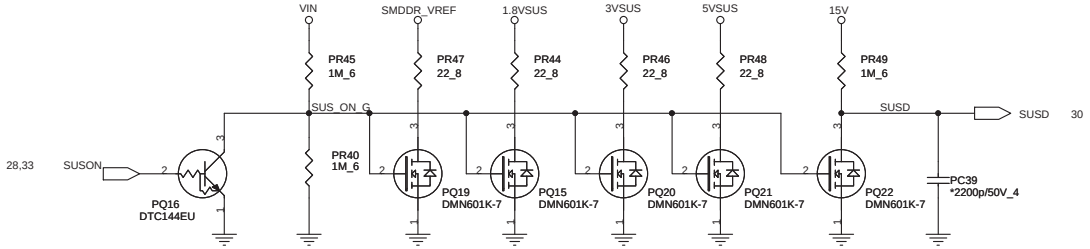
Quanta Computer Inc.		
Size	Document Number: VCCP	Rev: 1A
Date: Wednesday, June 04, 2008	Sheet 32 of 35	

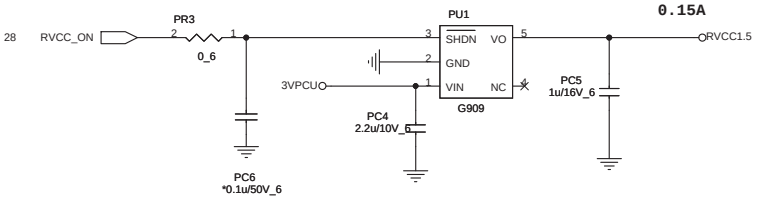


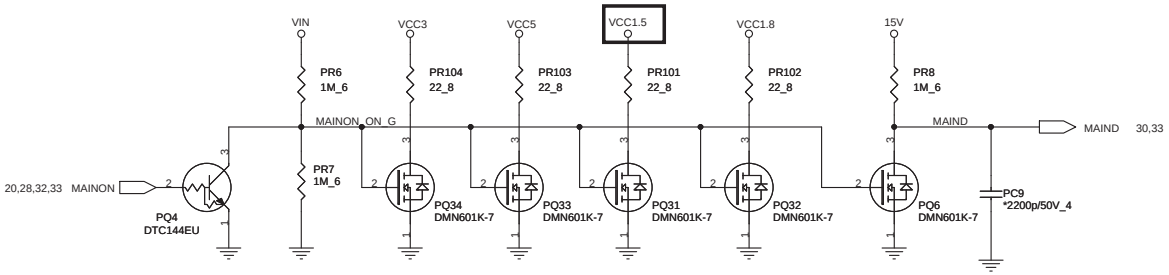
PROJECT : PB5/6		
Quanta Computer Inc.		
Size	Document Number: DDR 1.8V	Rev: 1A
Date: Wednesday, June 04, 2008	Sheet 33 of 35	











PROJECT : PB5/6

Quanta Computer Inc.

Size	Document Number	Rev
	DISCHARGE	1A

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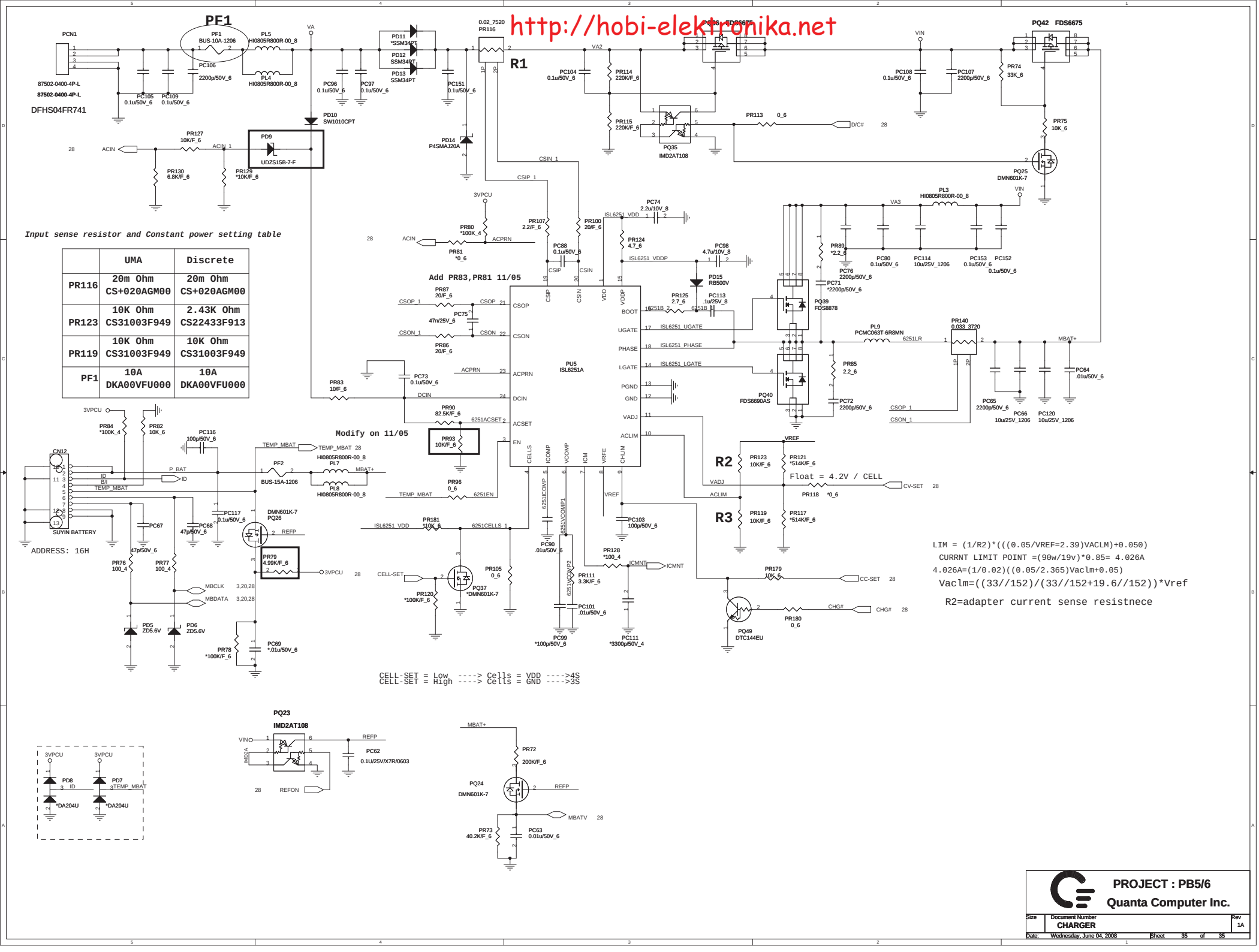

Input sense resistor and Constant power setting table

	UMA	Discrete
PR116	20m Ohm CS+020AGM00	20m Ohm CS+020AGM00
PR123	10K Ohm CS31003F949	2.43K Ohm CS22433F913
PR119	10K Ohm CS31003F949	10K Ohm CS31003F949
PF1	10A DKA00VFU000	10A DKA00VFU000

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Quanta Computer Inc.	
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