ZRH SYSTEM BLOCK DIAGRAM

GPU CORE PWR MAX17007 P44	CHARGER ISL88731 P37
GPU IO PWR P45	3/5V SYS PWR RT8223M P38
DISCHARGER +3V,+ 5V,+1.5V,+1.05V,+1.1V_VTT P46	CPU CORE PWR MAX17511 P39
+1.0V/+1.8V RT9018A + TPS54418 P47	CPU VCCSA TPS51461 P411
CPU VGFX_AXG MAX17511 P40	VTT 1.05V RT8238 P41
THERMAL PROTECTION P47	DDR3 PWR RT8207A P42

BCLK: 133MHz
PEG_CLK: 100MHz
DPLL_REF_SSCLK: 120MHz

Fan Driver (PWM Type) P35

intel <MCH Processor>
Sandy Bridge
rPGA 989 (37.5mm X 37.5mm)
P3.4.5.6
DDR SYSTEM MEMORY
PCI-E X16
FDI
DMI

DDR III P13,14, 15, 16
SO-DIMM 0
SO-DIMM 1
SO-DIMM 2
SO-DIMM 3
Dual Channel
1066/ 1333 MHz
800 MT/s 1066 MT/s

PCIE
2.5GT/s
NVIDIA GPU
N12E-GE / N12P-GS
1GB *(64Mb x 32 IO x 8 pcs)*
P18,19,20,21,22,23,24,25
X'TAL 27.0MHz

FDI interface
X4 DMI interface

intel <PCH>
FDI
DMI
Graphics Interfaces
SATA *6.0 GT/s*
CougarPoint
SATA *3.0 GT/s*
USB
HDA
SPI
LPC
mBGA 989 (27mm X 25mm)
P7.8.9.10.11.12
PCI-E
RTC P9
X'TAL 32.768KHz

INT_CRT → CRT P25
INT_LVDS (2 ch) → USB 12 → 3D panel P25 / LVDS P25
INT_HDMI → HDMI P26

HDD (SATA) P27 — SATA0
ODD (SATA) P27 — SATA1
eSATA Buffer P32 — SATA4

Note:
HM55 does not support USB 6 & 7
HM55 does not support SATA 2 & 3

eSATA Conn. USB 9 P32
USB Port x 3 USB 1, 3, 9 P32 — USB 2.0
Bluetooth USB 4 P35
CCD USB 8 P25
FingerPrint USB 2 P35
USB 12
DT dongle USB 0 P32
DT Touch Pad

Azalia
Audio CODEC ALC669X P29
Rear Audio Amp & Head phone AN12947A P30
Sub-Amplifier (TPA311D1) P30
Int. Speaker P30
SUBWOOFER P30
Line in P30
MIC Jack P30
Int. D-MIC P30
S/PDIF P30

SPI ROM 4MB x1 (Basic ME+Braidwood) P8
EC (WPC791) P36
SPI ROM 128KB x1 P36
K/B COON. P34

PCI-Express *2.5GT/s*
PCIE-2 *CLKOUT_PEG_3* → USB3.0 Chip UPD720200F1 P33 → USB Charger P33 → USB 3.0 Conn P33
PCIE-3 & 6 *CLKOUT_PEG_1&2* → Mini Card WLAN / GPS USB 10 & 13 P28
PCIE-5 *CLKOUT_PCIE5* → IEEE1394 & Media Cardreader JM388A P31 → IEEE1394a connector P31 / Card Reader Connector P31
X'TAL 24.576MHz
PCIE-1 *CLKOUT_PEG_B* → Realtek Giga-LAN RTL8111E P34 & Daughter Board → Transformer Daughter Board → RJ45 Daughter Board
X'TAL 25MHz

SSID:
SVID: 1025
GFX:

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PROJECT : ZRH
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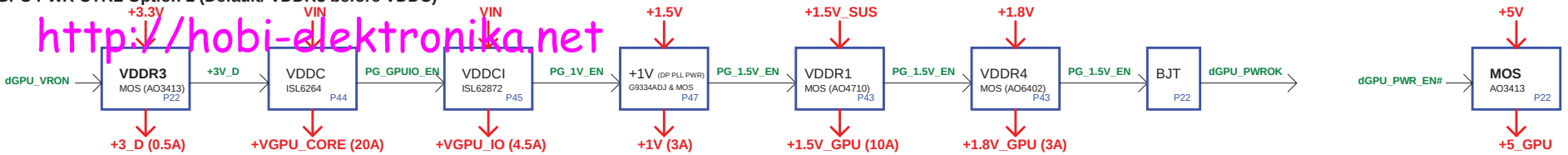
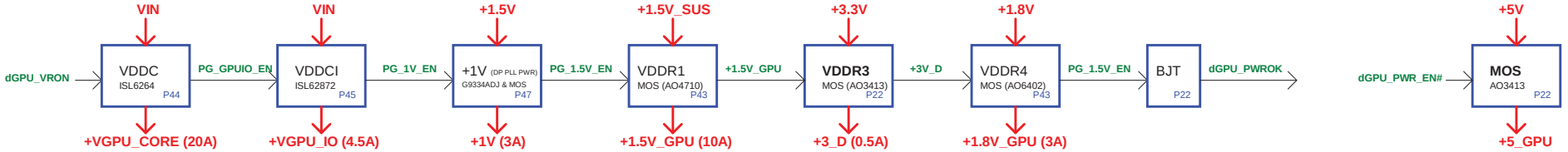
GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



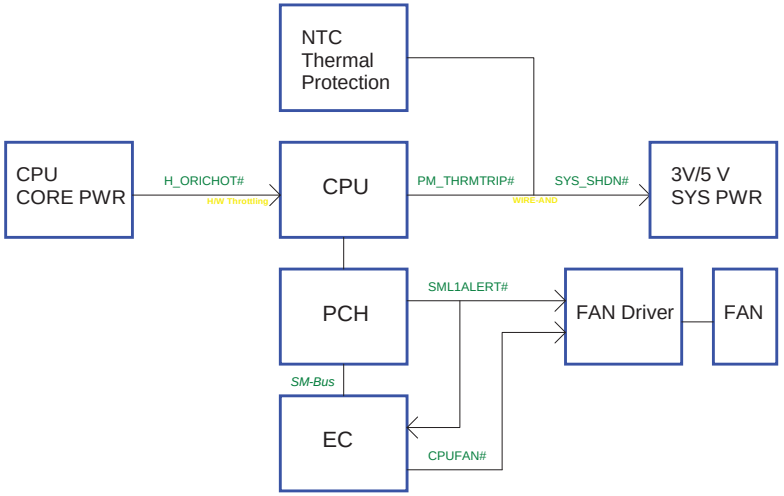
GPU PWR CTRL Option 2 (VDDR3 after VDDR1)



Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+5V_GPU	+5V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN#	Discrete enable
+GPU_CORE	+0.9V~+1.1V	GPU CORE POWER	+3V_D	Discrete enable
+GPU_IO	+0.9V~+1.1V	GPU I/O POWER	PG_GPUIO_EN	Discrete enable
+1.5V_GPU	+1.5V	VRAM CORE POWER	PG_1.5V_EN	Discrete enable
+1.8V_GPU	+1.8V	GPU_CRE/LVDS/PLL POWER	+1.5V_GPU	Discrete enable
+1V	+1V	DP/PEG POWER	PG_1V_EN	Discrete enable

Thermal Follow Chart



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	PWR Status & GPU PWR CRL & THRM	1A

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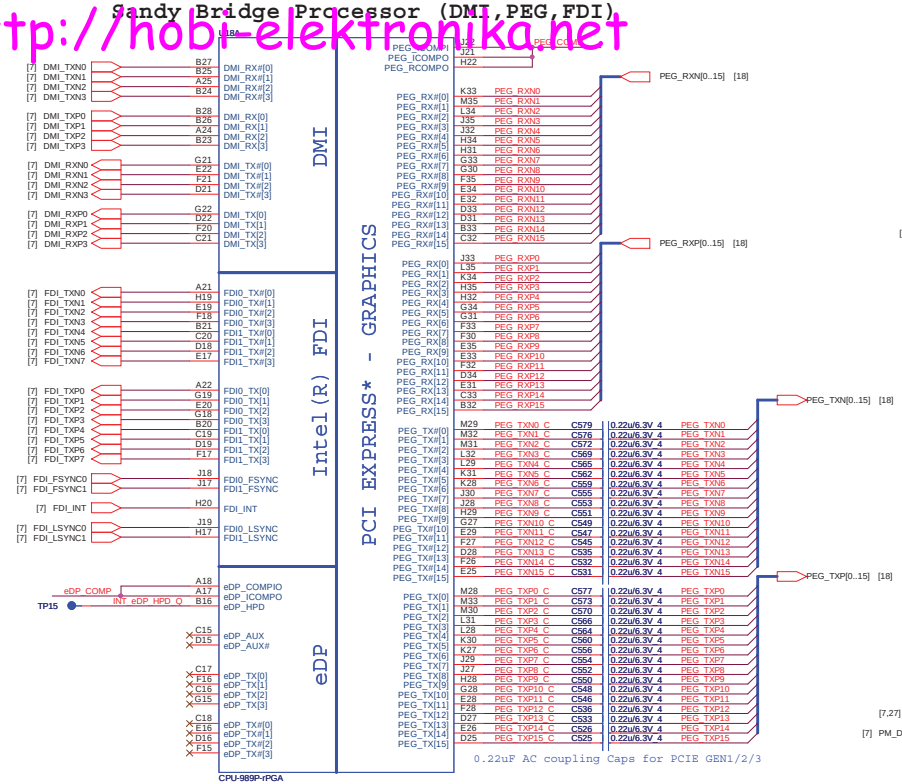
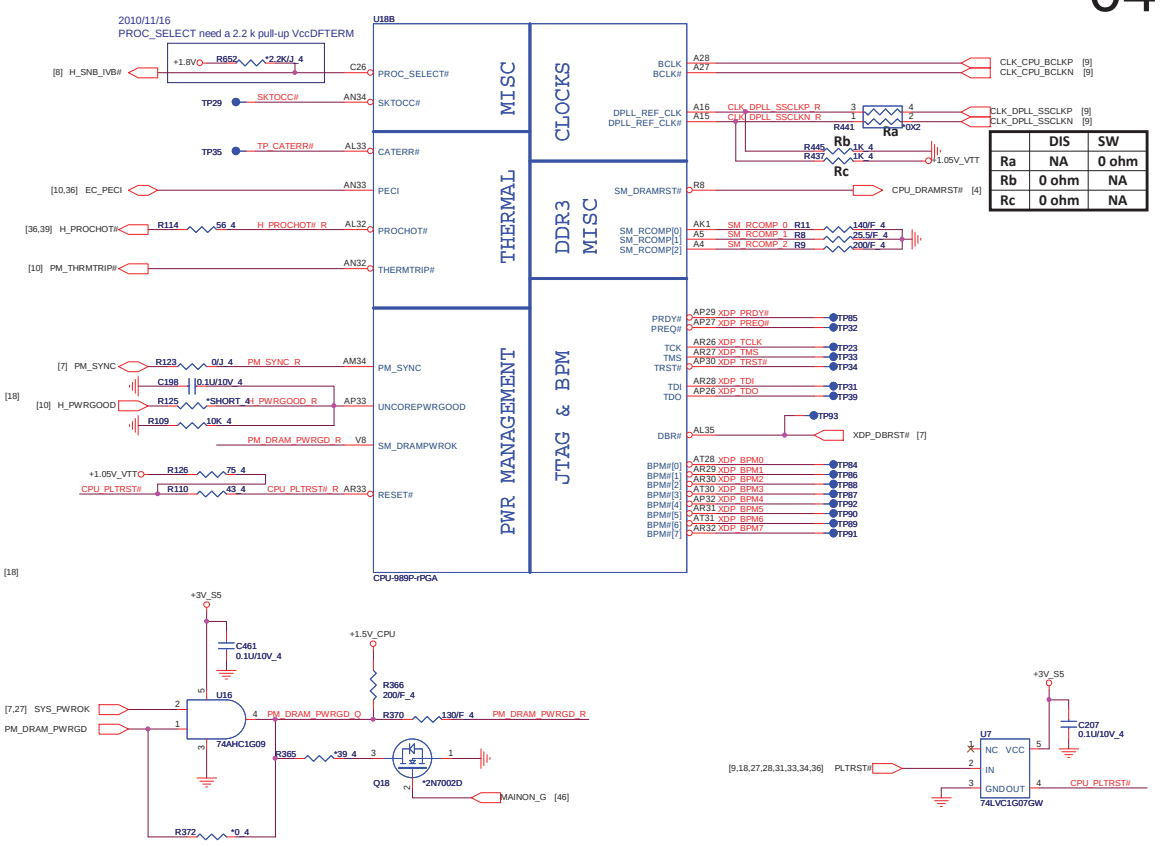
Sandy Bridge Processor (DMI,PEG,FDI)



Sandy Bridge Processor (CLK,MISC,JTAG)

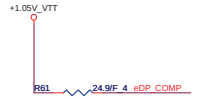
04



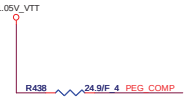
	DIS	SW
Ra	NA	0 ohm
Rb	0 ohm	NA
Rc	0 ohm	NA

FDI Disabling (Discrete Only)

DP & PEG Compensation



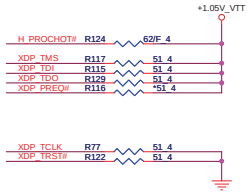
eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

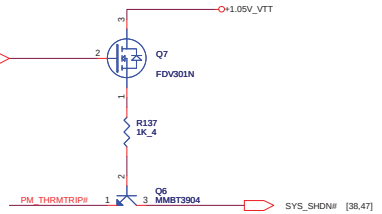


PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms

PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

Processor pull-up(CPU)





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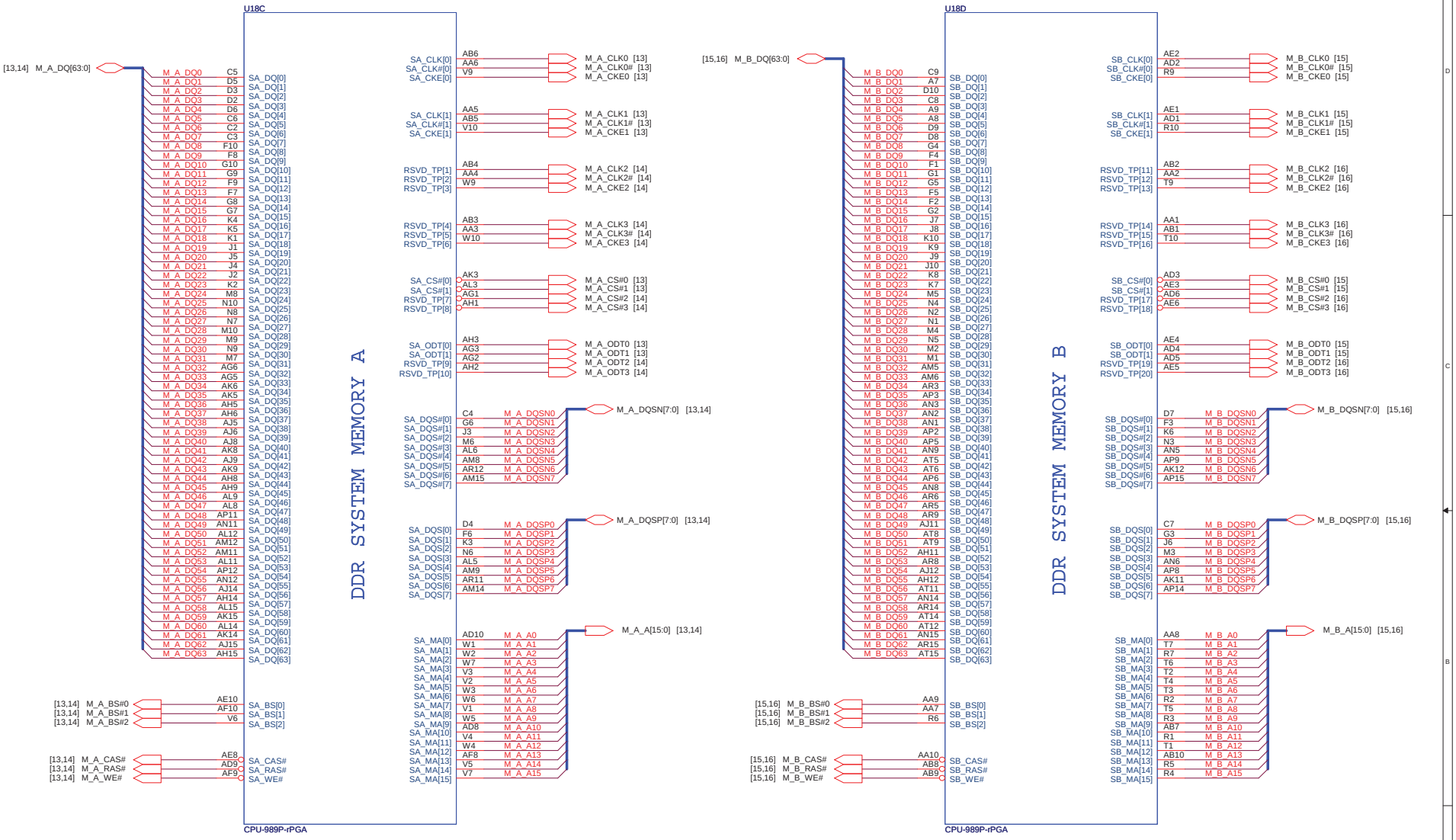
Sandy Bridge Processor (DDR3)



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Sandy Bridge Processor (POWER)

Sandy Bridge Processor (GRAPHIC POWER)

CPU Core Power SNB 45W:52A

Spec	Real
470uF/4mohm x 4	470uF/4mohm x 3
22uF x 16	22uF x 14
10uF x 10	10uF x 9

CPU VTT SNB 45W:8.5A

Spec	Real
330uF/6mohm x 2	390uF/10mohm x 1
22uF x 12	22uF x 10
22uF x 7 (Non-stuff)	10uF x 1

CPU VGT SNB 45W:21.5A

Spec	Real
470uF/4mohm x 2	330uF/10mohm x 1
22uF x 12	22uF x 8
	10uF x 6

CPU VCCPL SNB 45W:1.5A

Spec	Real
330uF/7mohm x 1	10uF x 1
10uF x 1	1uF x 2
1uF x 2	

CPU MCH SNB 45W: 5A

Spec	Real
330uF/6mohm x 1	10uF x 8
10uF x 6	

CPU SA SNB 45W: 6A

Spec	Real
330uF/7mohm x 1	10uF x 3
10uF x 3	

U18F — CPU-989P-rPGA

POWER

CORE SUPPLY

PEG AND DDR

SVID

SENSE LINES

U18G — CPU-989P-rPGA

POWER

GRAPHICS

SENSE LINES

VREF

DDR3 -1.5V RAILS

SA RAIL

1.8V RAIL

MISC

10uF (Reserved)

	DIS	SW
Ra	0 ohm	NA

2010/11/16
add 10K pull high to VCC_CORE, pull low to GND

2010/11/16
change to 10/F_4

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

Layout note: need routing together and ALERT need between CLK and DATA

SVID CLK

SVID DATA

SVID ALERT

Place PU resistor close to CPU

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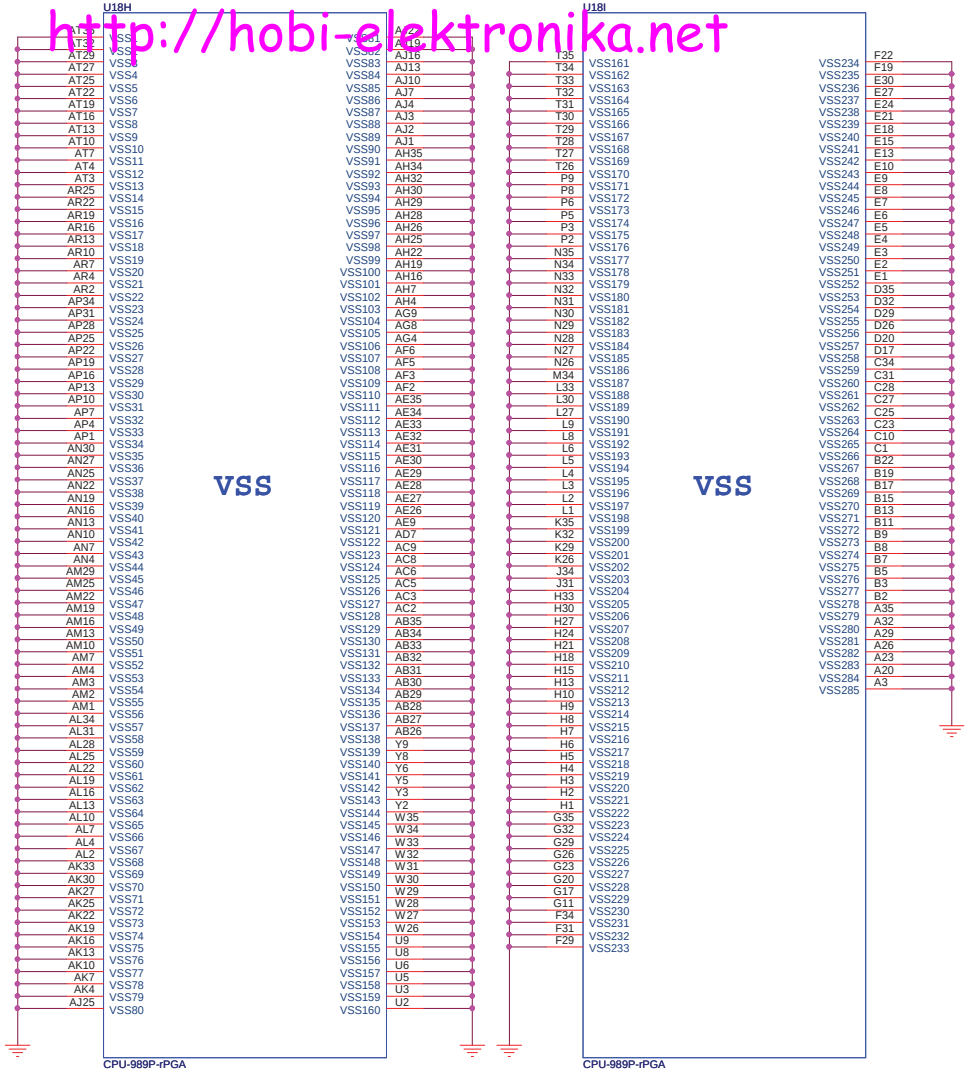
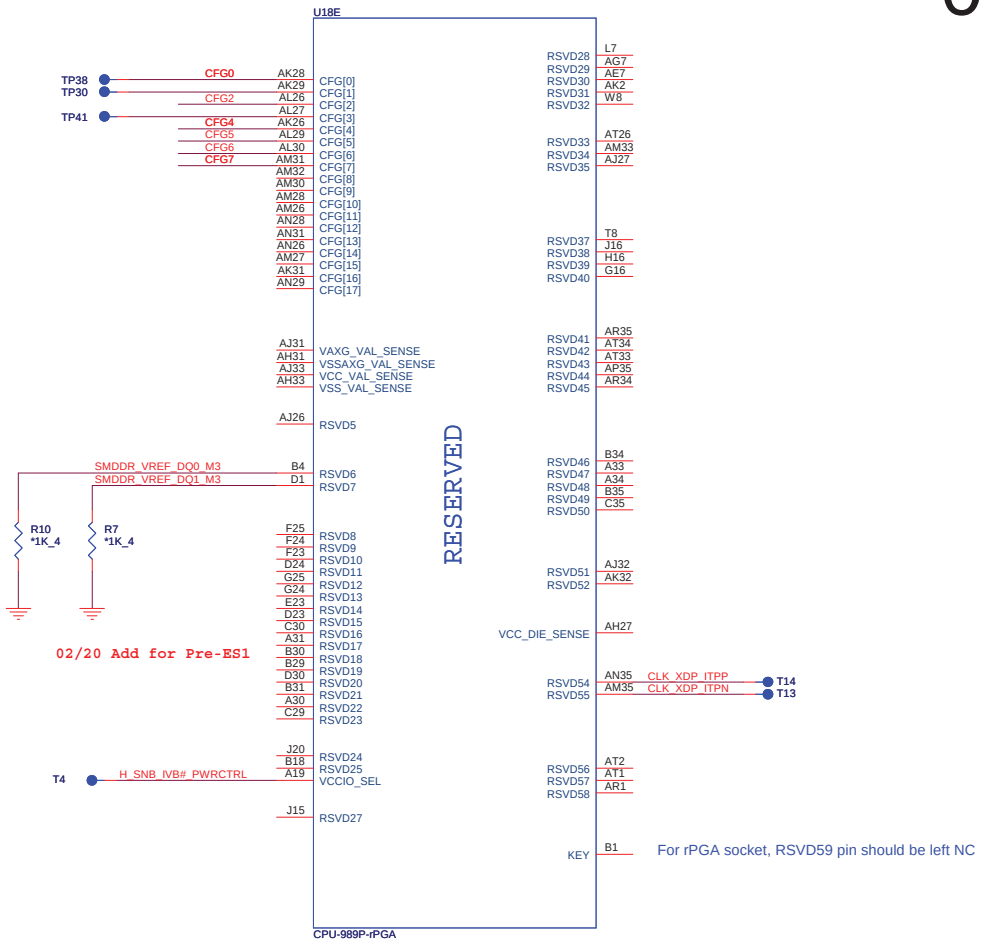
Sandy Bridge Processor (GND)



Sandy Bridge Processor (RESERVED, CFG)

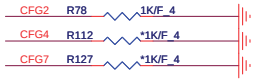


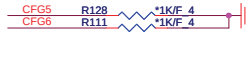
For rPGA socket, RSVD59 pin should be left NC

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training





CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

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	Sandy Bridge 4/4	1A

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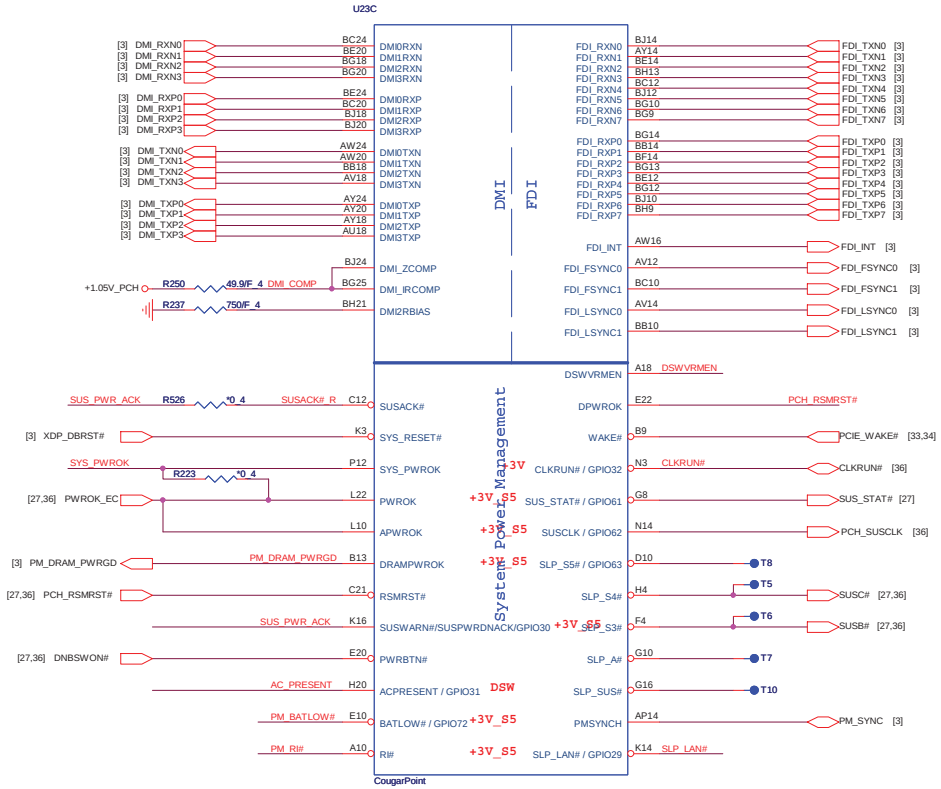
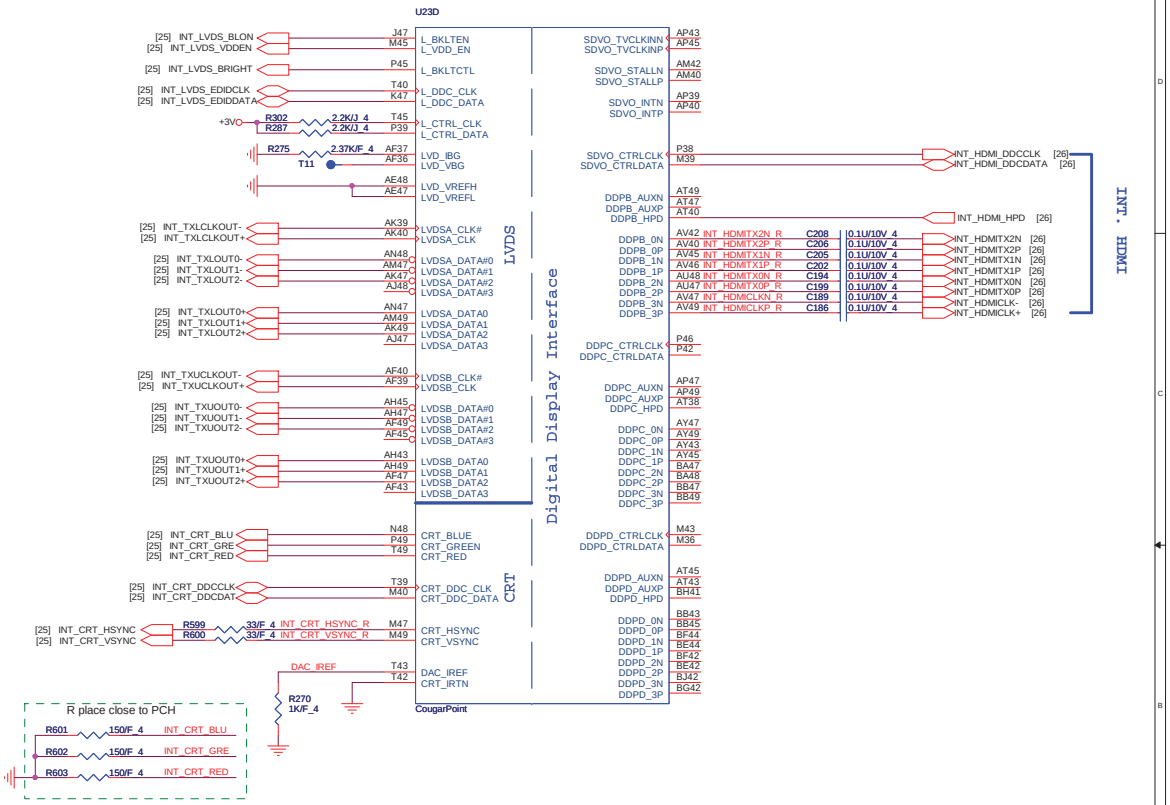
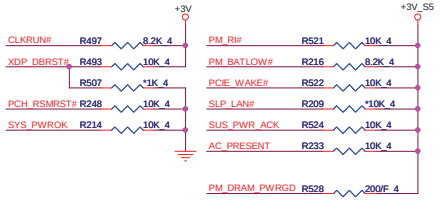
Cougar Point (DMI,FDI,PM)



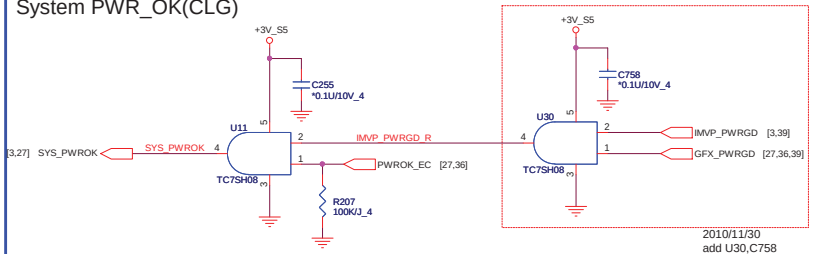
Cougar Point (LVDS,DDI)



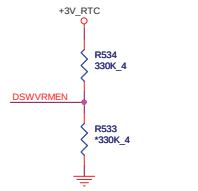
PCH Pull-high/low(CLG)



System PWR_OK(CLG)



2010/11/30
add U30,C758



On Die DSW VR Enable
High = Enable (Default)
Low = Disable

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	Cougar Point 1/6	1A
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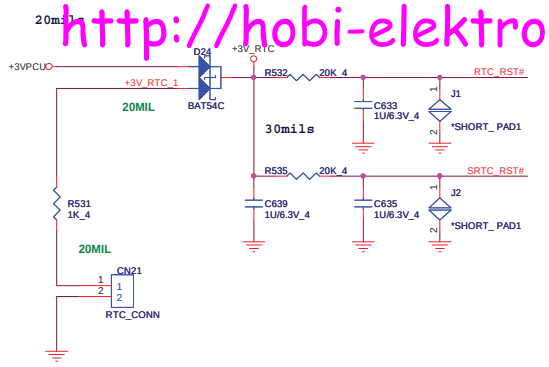
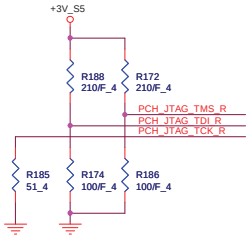
RTC Circuitry(RTC)



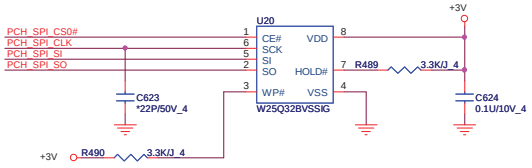
HDA Bus(CLG)

PCH JTAG Debug (CLG)



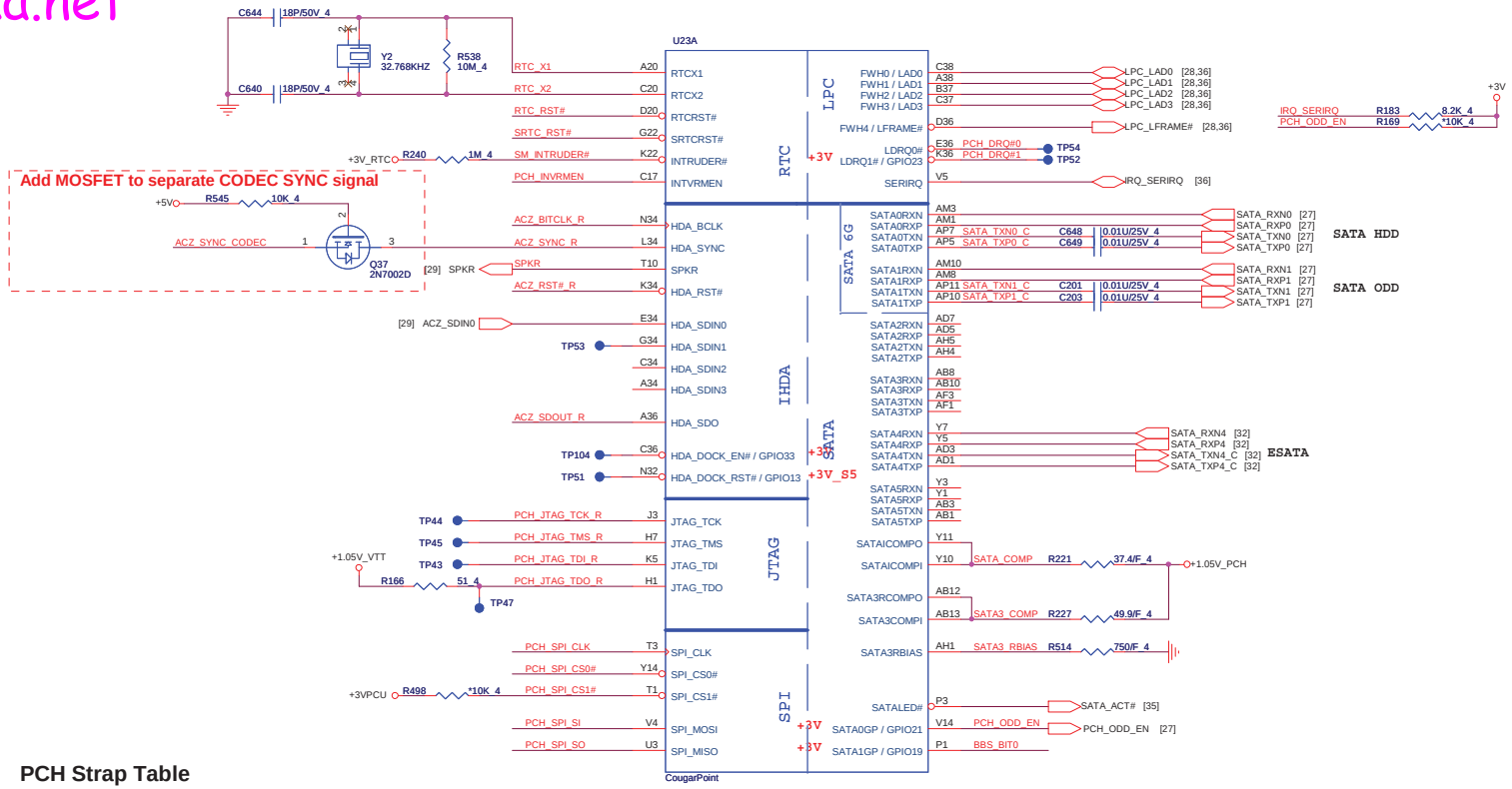
PCH Dual SPI (4M)

Winbond W25Q32BVSSIG AKE391P0N00
MXIC MX25L3205DM2I-12G: AKE39FP0Z00



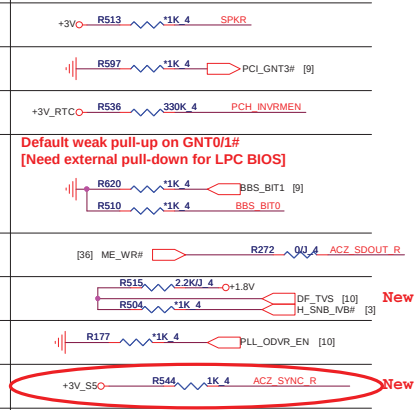
PCH2 (CLG)

Cougar Point (HDA,JTAG,SATA)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location: 1 / 1 / SPI *; 0 / 0 / LPC
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK	
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 20kohm)



New Add in CPT EDS Rev1.0 at 0316

New Add in CPT EDS Rev1.0 at 0316

3/16 Remove based on CPT EDS rev1.0

3/16 Remove based on CPT EDS rev1.0

3/16 Remove based on CPT EDS rev1.0

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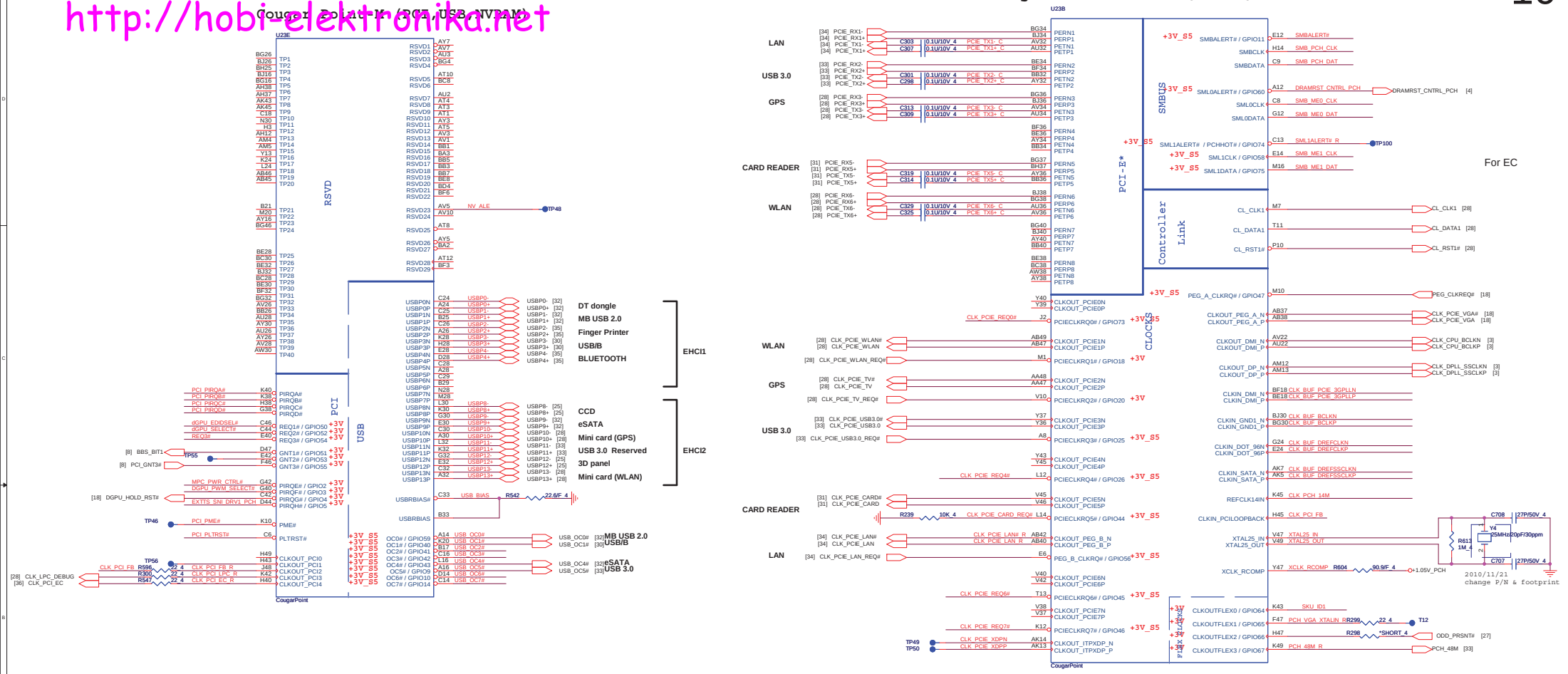
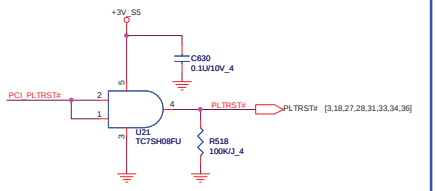
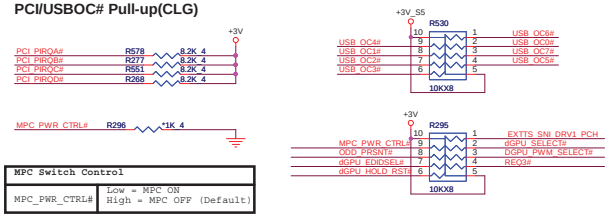
Cougar Point-M (PCI-E,SMBUS,CLK)



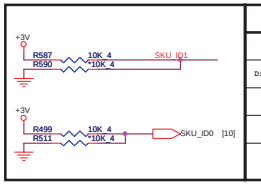
PLTRST#(CLG)



PCI/USBOC# Pull-up(CLG)



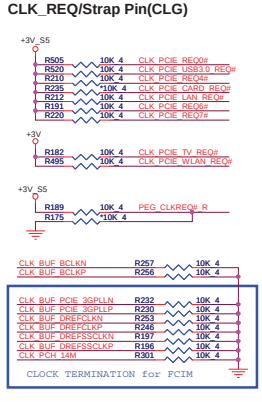
MPC Switch Control	
MPC_PWR_CTRL#	Low = MPC ON High = MPC OFF (Default)



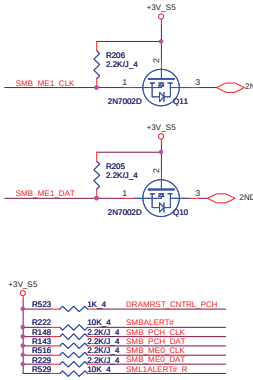
	dGPU_PW_CTRL#	SKU_ID1	SKU_ID0	VGA H/W Signal	Setup Menu	
UMA Only	1	0	0	UMA	Hidden	UMA boot
Discrete Only	0 or 1	0	1	GPU	Hidden	GPU boot
Switchable (Mux)	0	1	0	UMA+dGPU	DIS/SG	UMA boot
Optimize (Muxless)	0	1	1	UMA	UMA/SG	UMA boot

0 = GPU power is control by PCH GPIO (Discrete, SG or Optimize)
1 = GPU power is control by H/W (pure Discrete SKU)

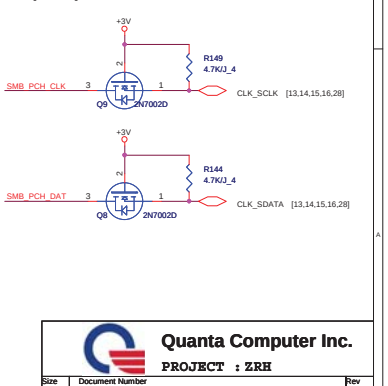
CLK_REQ/Strap Pin(CLG)



SMBus(EC)



SMBus(PCH)



Quanta Computer Inc.
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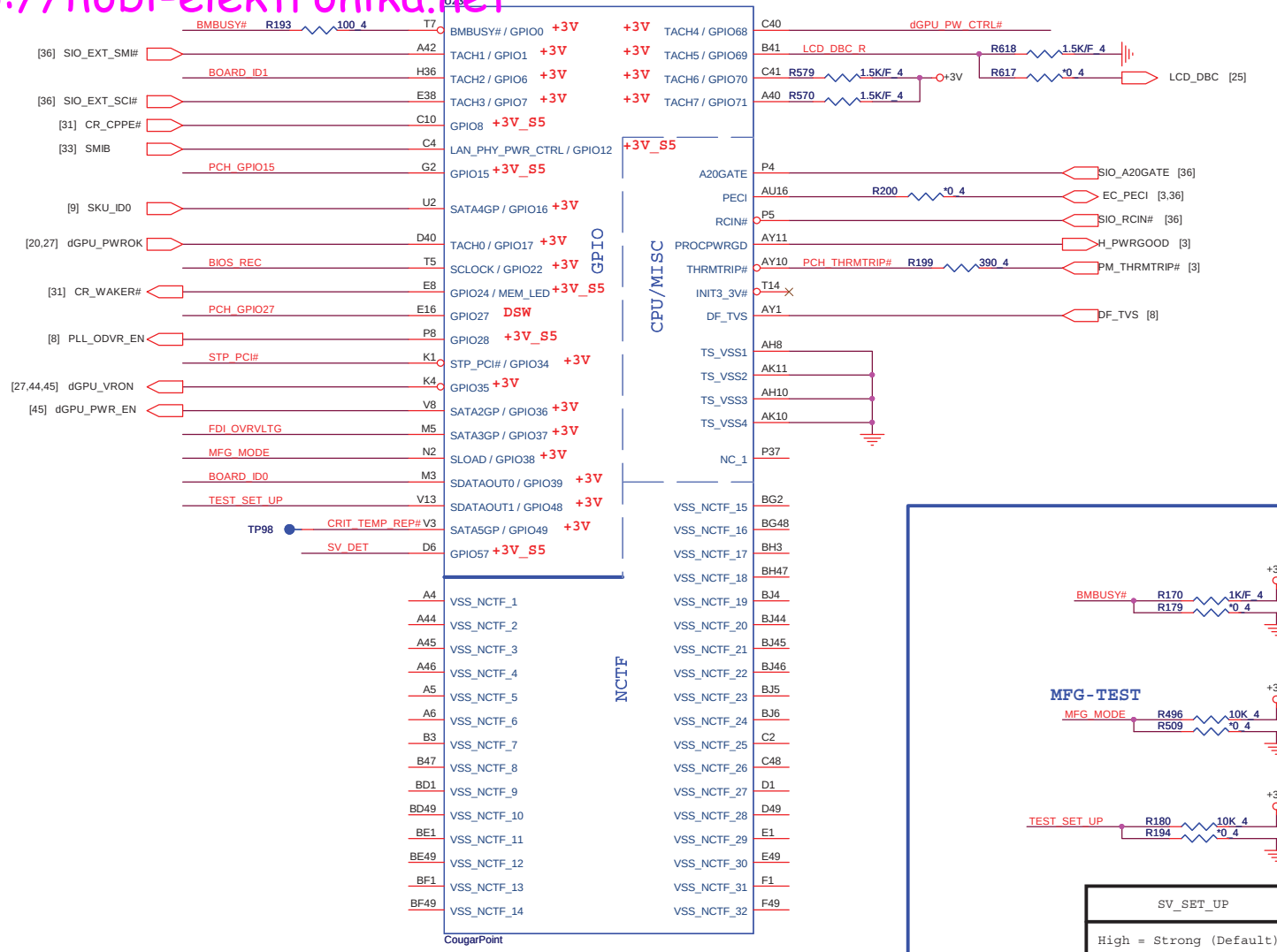
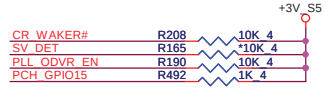
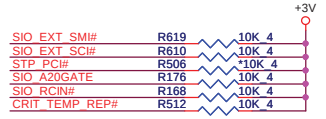
Cougar Point (GPIO,VSS_NCTF,RSVD)

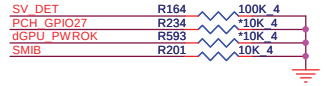


GPIO Pull-up/Pull-down(CLG)



GPIO15
Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

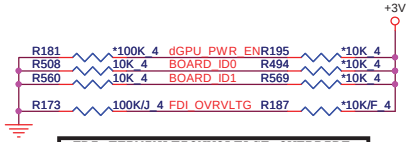




MFG-TEST

SV_SET_UP
High = Strong (Default)

BIOS RECOVERY	High = Disable (Default) Low = Enable



FDI TERMINATIONVOLTAGE OVERRIDE
LOW - Tx, Rx terminated to same voltage

high	GPU power is control by H/W (DIS only, UMA only)
low	GPU power is control by PCH GPIO (Discrete, SG or Optimize)

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COUGAR POINT (POWER)

Cougar Point-M (POWER)

VccADAC Power

	Ra	Rb
DIS	LOW	LOW
SW	HIGH	HIGH

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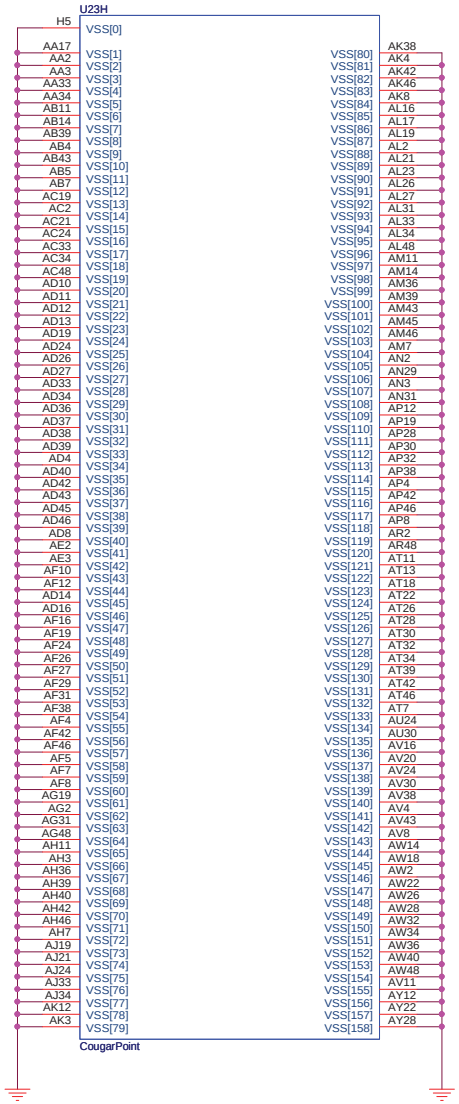
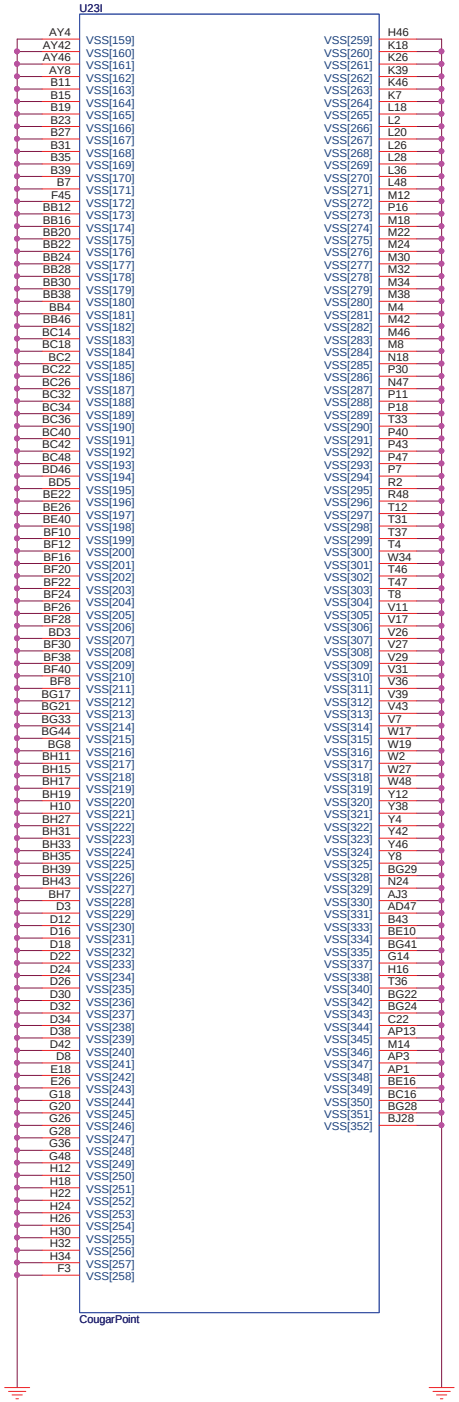
IBEX PEAK-M (GND)





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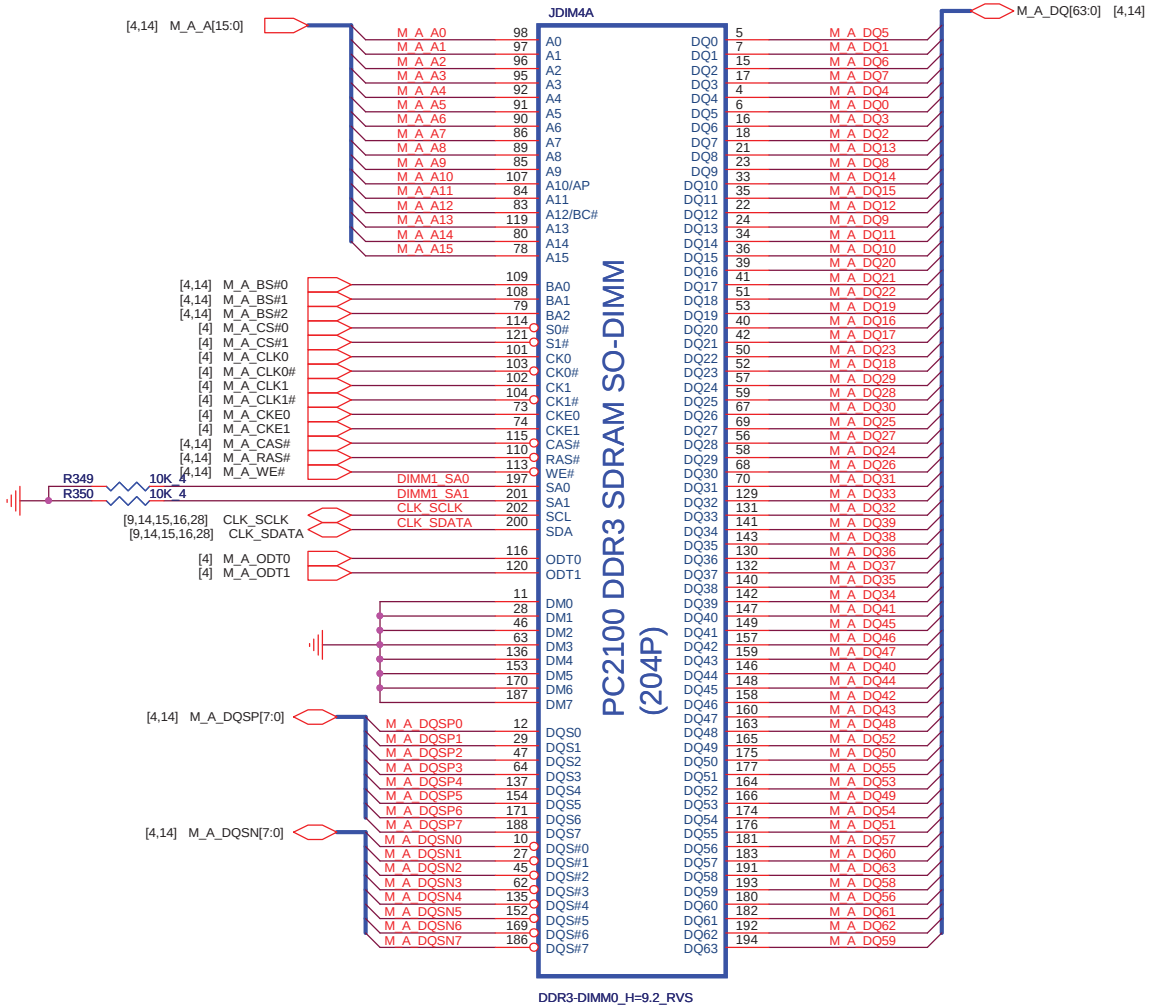
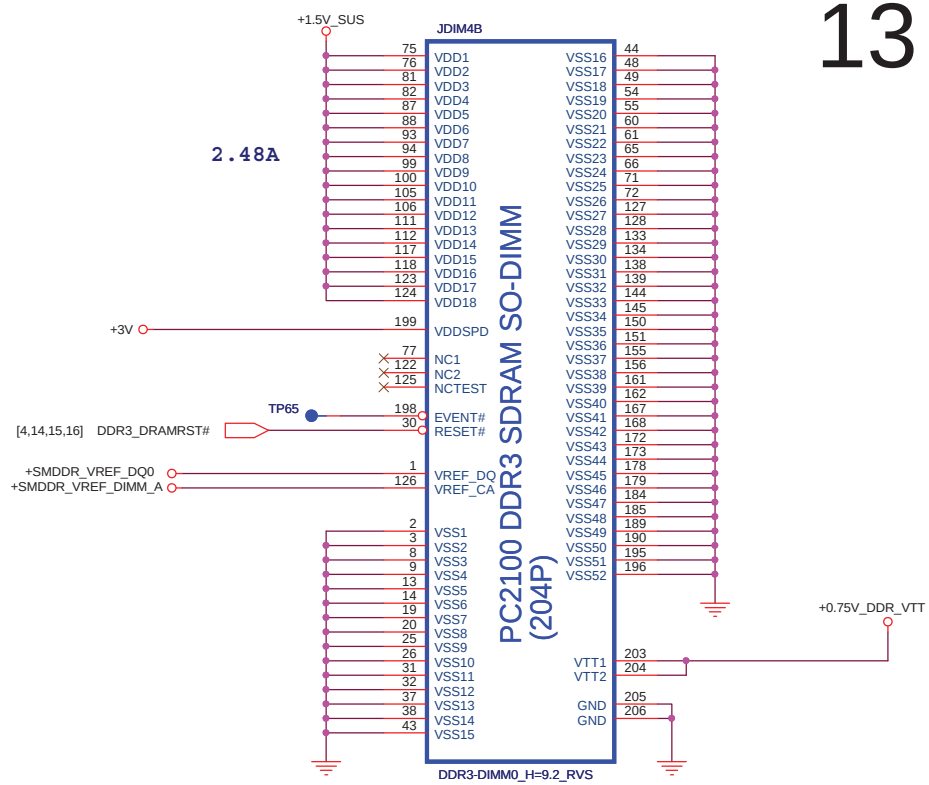
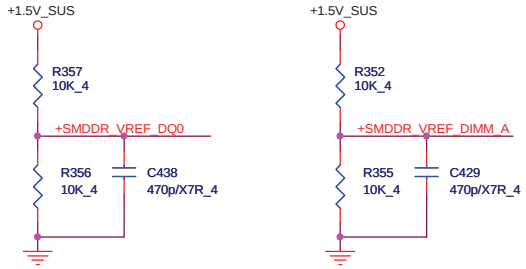
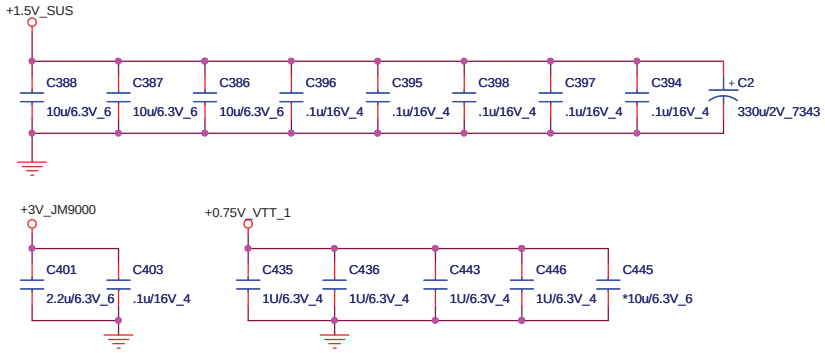
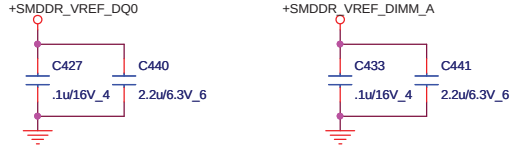






Place these Caps near So-Dimm0.





	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

Quanta Computer Inc.

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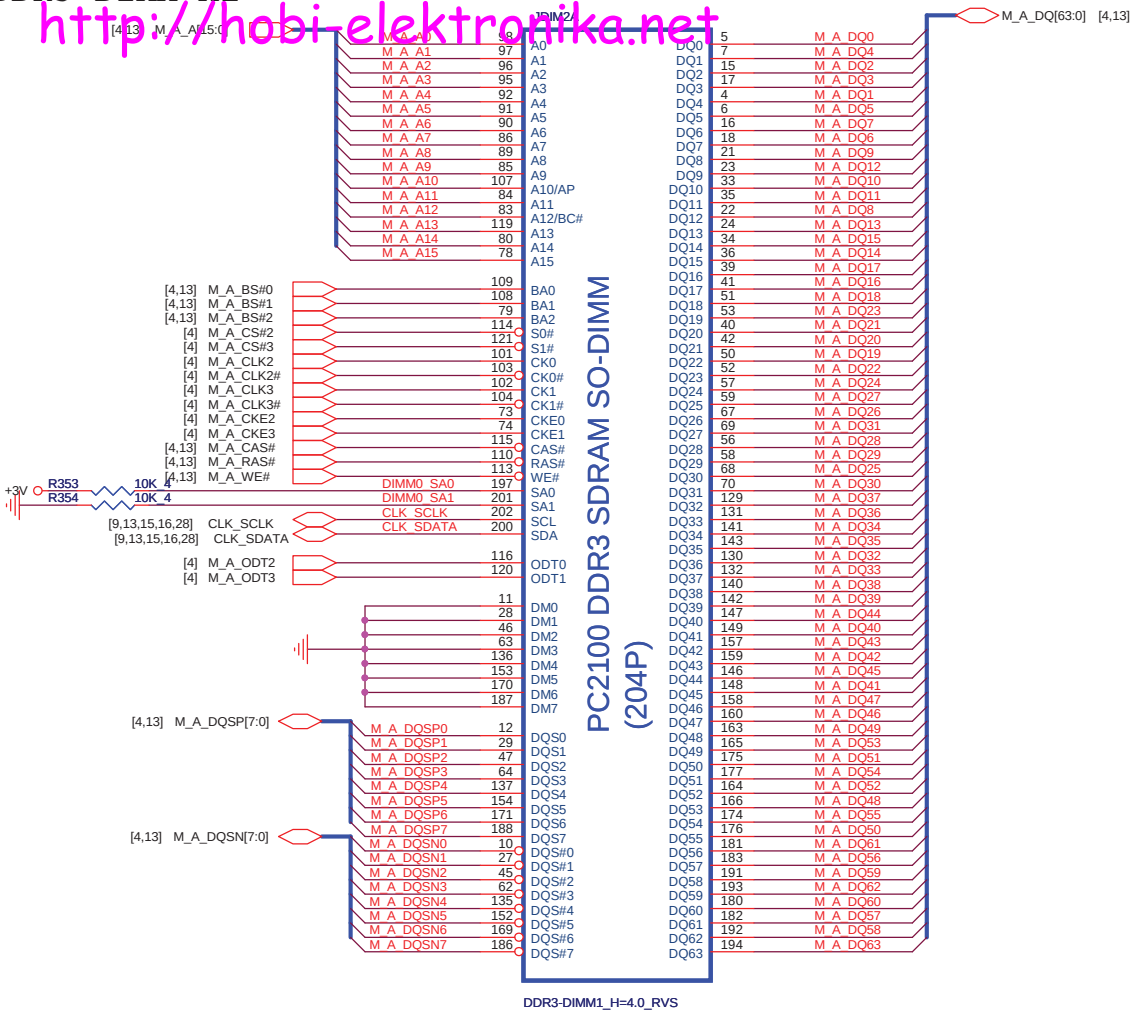
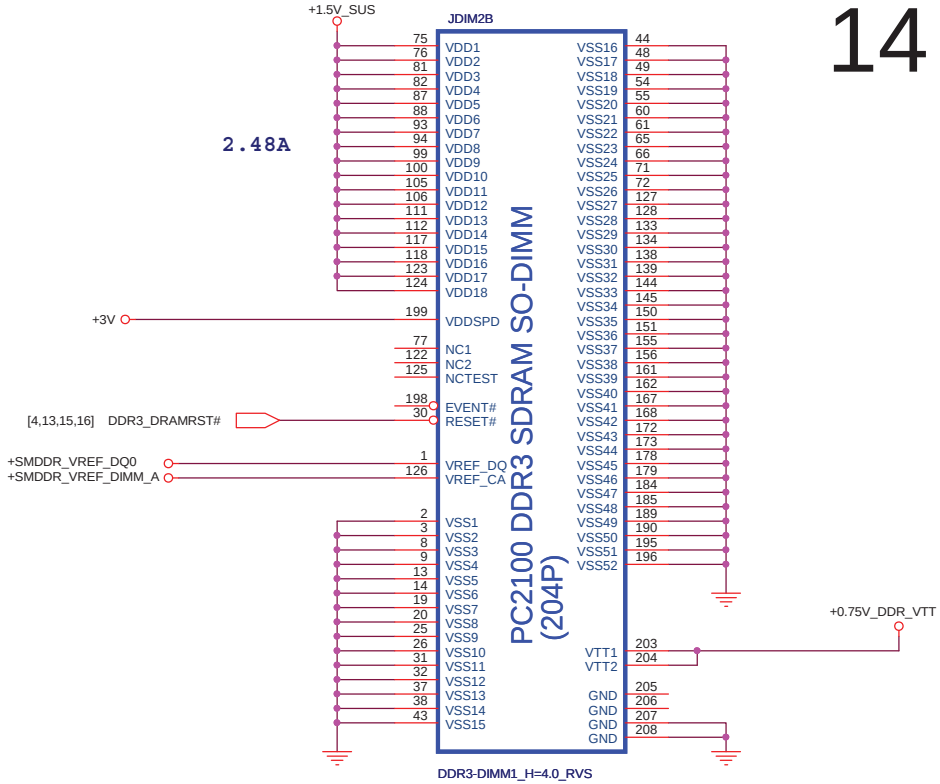
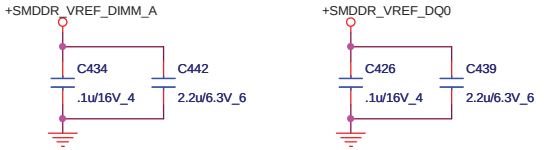
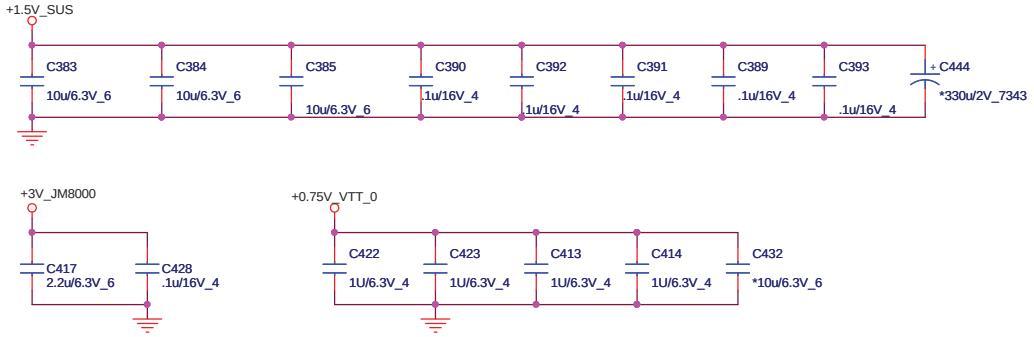
DDR3 DIMM-A1







Place these Caps near So-Dimm0.



	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

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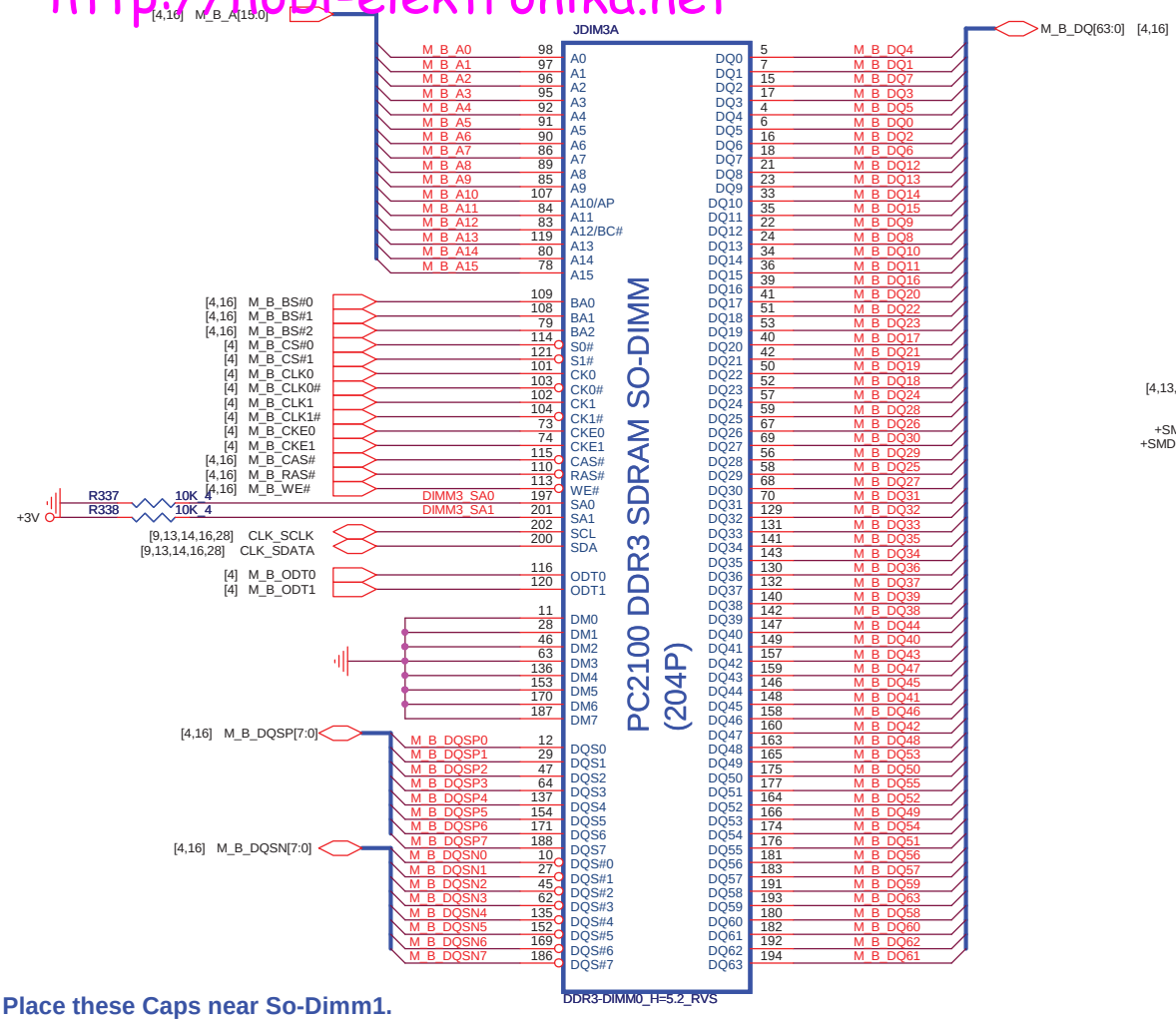
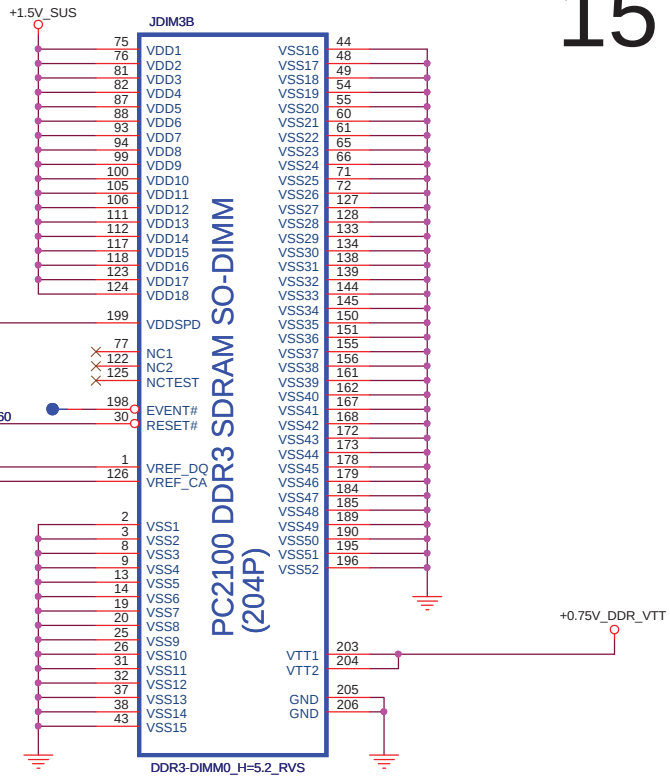
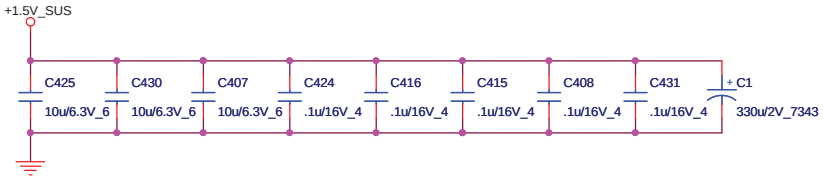
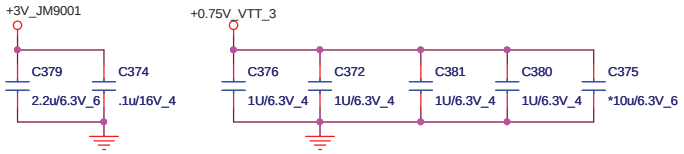


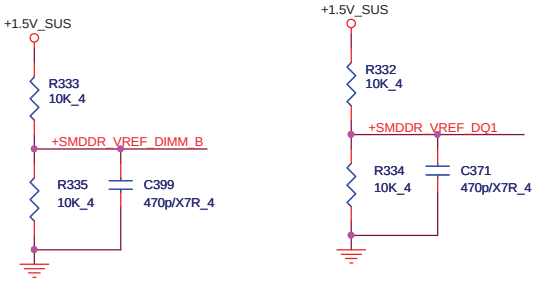


Place these Caps near So-Dimm1.





	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1



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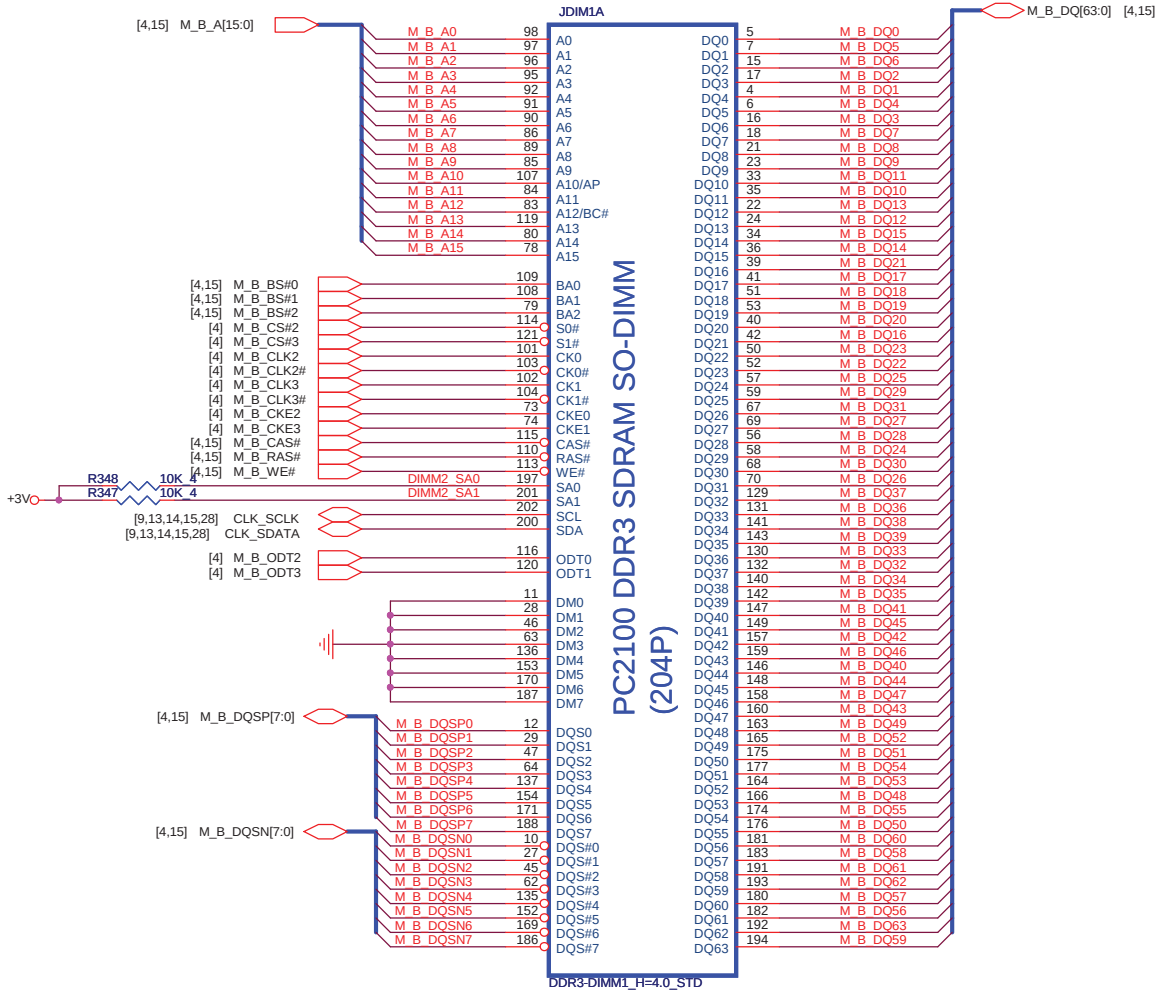
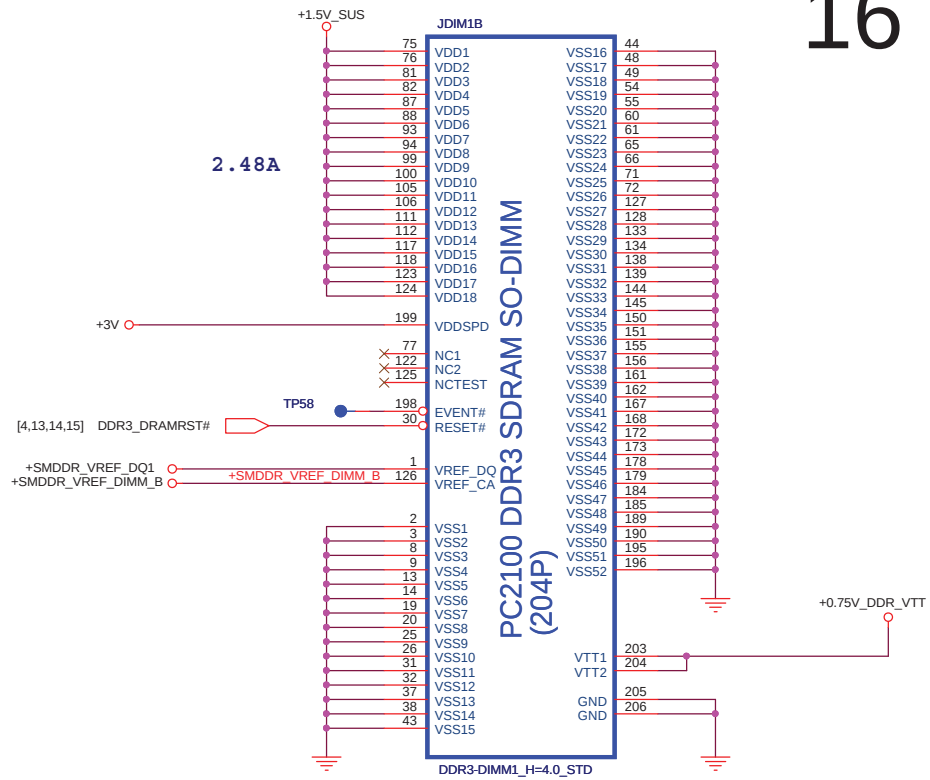
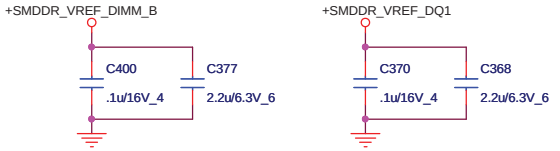
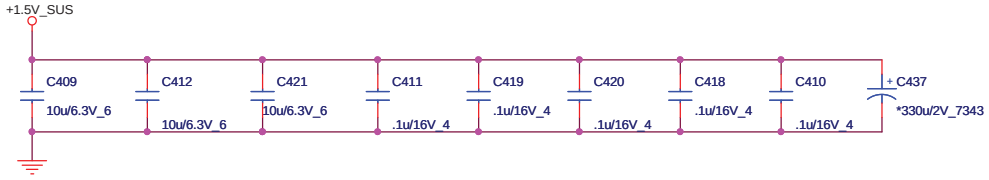
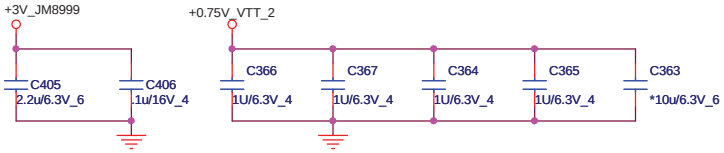






Place these Caps near So-Dimm1.





	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

Quanta Computer Inc.

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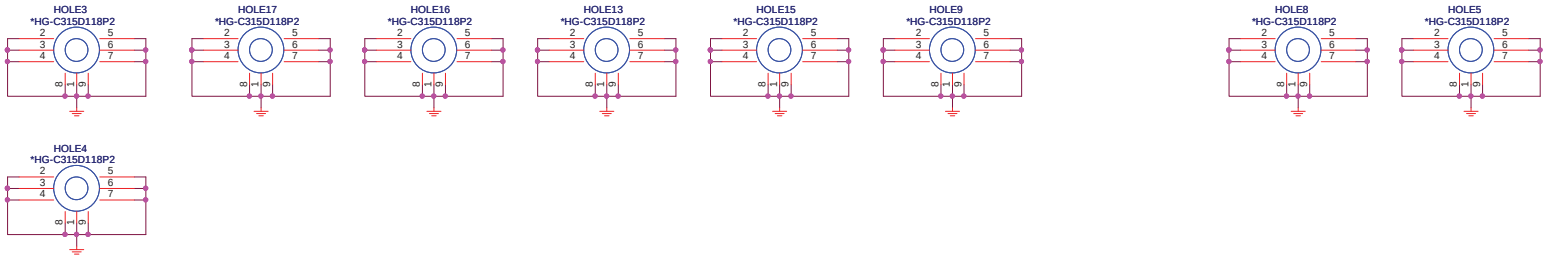
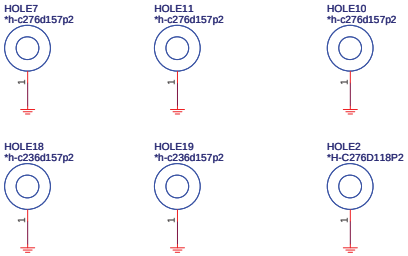
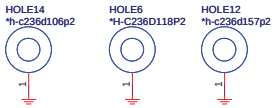
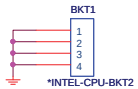
SCREW HOLE









Quanta Computer Inc.

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	XDP/ Hole	1A

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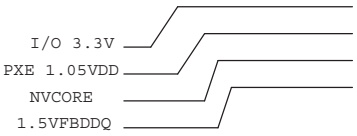
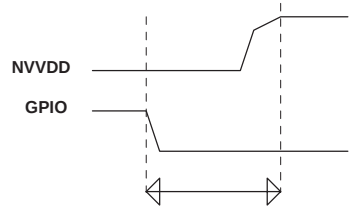
power up sequence



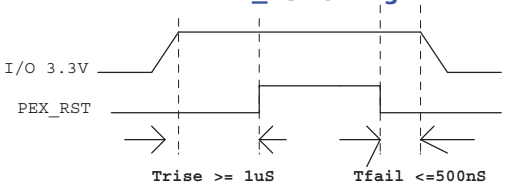
NB9M: VGACORE +0.90V (Normal) , +1.09V

NVVDD Maximum Settling Time

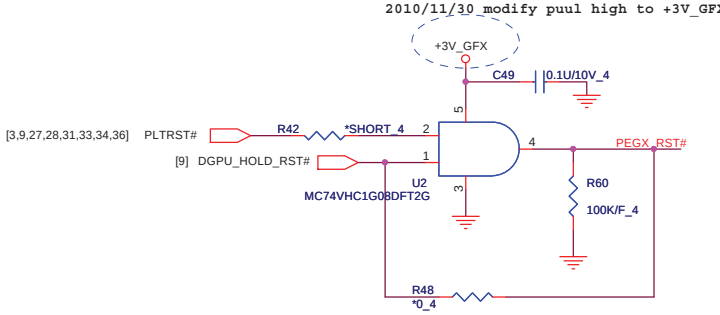


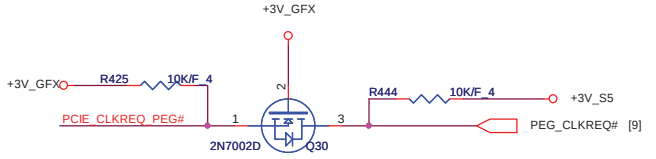
tsNVVDD<= 192us

PEX_RST timing

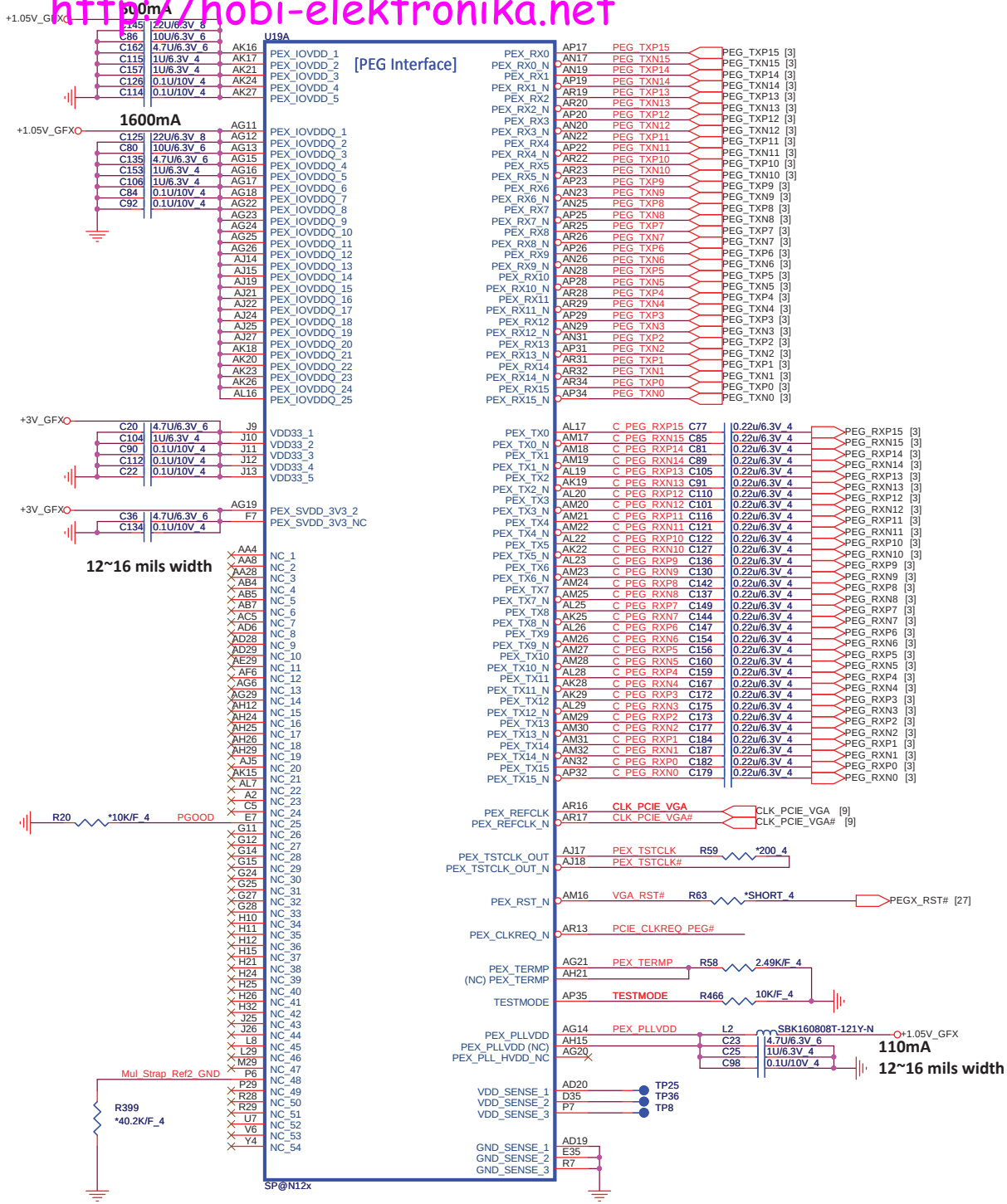


2010/11/30 modify puul high to +3V_GFX





[19,20,45] +1.05V_GFX
[20,21,36,44,45] +3V_GFX



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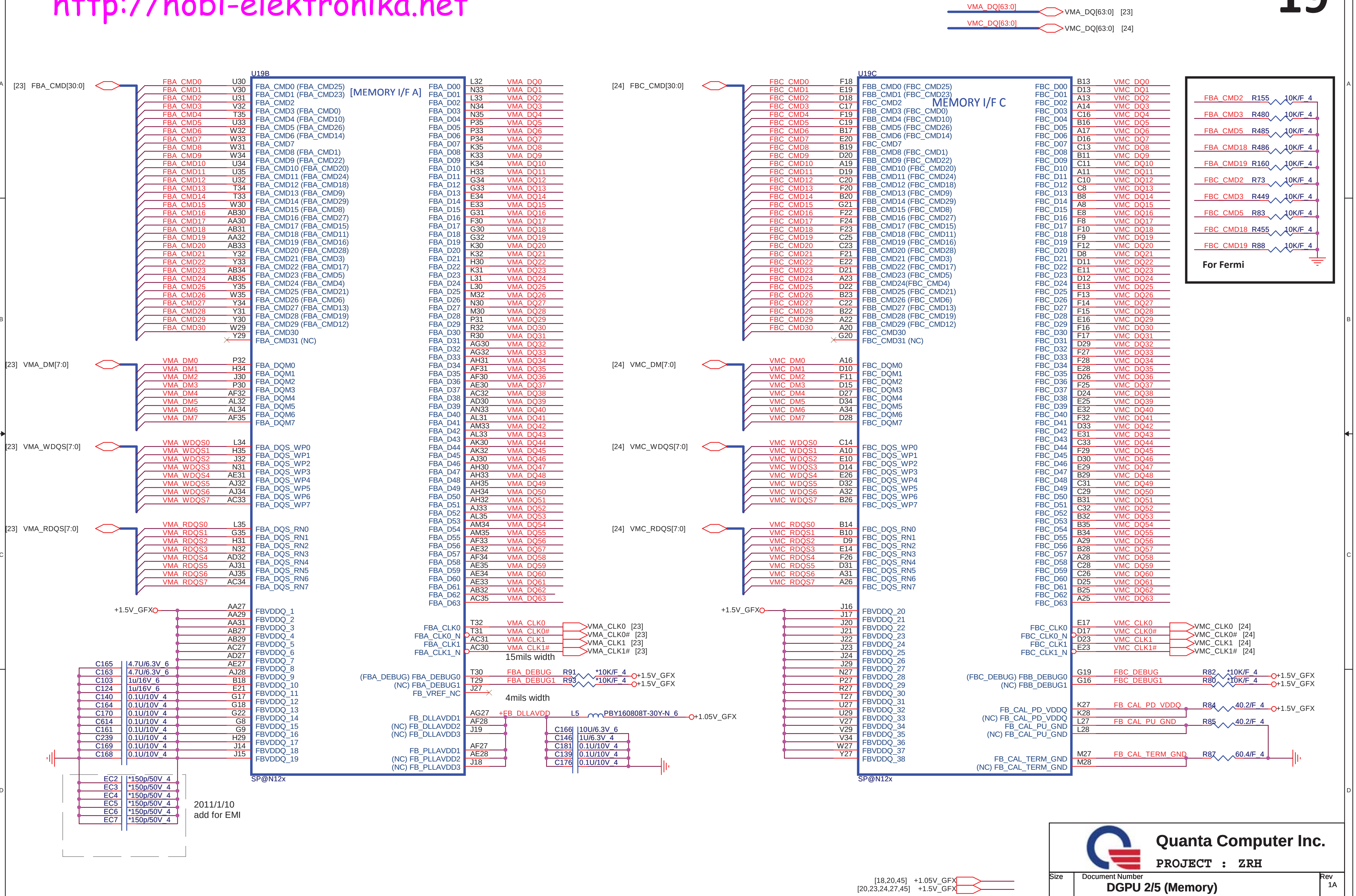
VMA_DQ[63:0] VMA_DQ[63:0] [23]
VMC_DQ[63:0] VMC_DQ[63:0] [24]
U19B
[MEMORY I/F A]
[23] FBA_CMD[30:0]
FBA_CMD0 U30 FBA_CMD0 (FBA_CMD25)
FBA_CMD1 V30 FBA_CMD1 (FBA_CMD23)
FBA_CMD2 U31 FBA_CMD2
FBA_CMD3 V32 FBA_CMD3 (FBA_CMD0)
FBA_CMD4 T35 FBA_CMD4 (FBA_CMD10)
FBA_CMD5 U33 FBA_CMD5 (FBA_CMD26)
FBA_CMD6 W32 FBA_CMD6 (FBA_CMD14)
FBA_CMD7 W33 FBA_CMD7
FBA_CMD8 W31 FBA_CMD8 (FBA_CMD1)
FBA_CMD9 W34 FBA_CMD9 (FBA_CMD22)
FBA_CMD10 U34 FBA_CMD10 (FBA_CMD20)
FBA_CMD11 U35 FBA_CMD11 (FBA_CMD24)
FBA_CMD12 U32 FBA_CMD12 (FBA_CMD18)
FBA_CMD13 T34 FBA_CMD13 (FBA_CMD9)
FBA_CMD14 T33 FBA_CMD14 (FBA_CMD29)
FBA_CMD15 W30 FBA_CMD15 (FBA_CMD8)
FBA_CMD16 AB30 FBA_CMD16 (FBA_CMD27)
FBA_CMD17 AA30 FBA_CMD17 (FBA_CMD15)
FBA_CMD18 AB31 FBA_CMD18 (FBA_CMD11)
FBA_CMD19 AA32 FBA_CMD19 (FBA_CMD16)
FBA_CMD20 AB33 FBA_CMD20 (FBA_CMD28)
FBA_CMD21 Y32 FBA_CMD21 (FBA_CMD3)
FBA_CMD22 Y33 FBA_CMD22 (FBA_CMD17)
FBA_CMD23 AB34 FBA_CMD23 (FBA_CMD5)
FBA_CMD24 AB35 FBA_CMD24 (FBA_CMD4)
FBA_CMD25 Y35 FBA_CMD25 (FBA_CMD21)
FBA_CMD26 W35 FBA_CMD26 (FBA_CMD6)
FBA_CMD27 Y34 FBA_CMD27 (FBA_CMD13)
FBA_CMD28 Y31 FBA_CMD28 (FBA_CMD19)
FBA_CMD29 Y30 FBA_CMD29 (FBA_CMD12)
FBA_CMD30 W29 FBA_CMD30
Y29 FBA_CMD31 (NC)
[23] VMA_DM[7:0]
VMA_DM0 P32 FBA_DQM0
VMA_DM1 H34 FBA_DQM1
VMA_DM2 J30 FBA_DQM2
VMA_DM3 P30 FBA_DQM3
VMA_DM4 AF32 FBA_DQM4
VMA_DM5 AL32 FBA_DQM5
VMA_DM6 AL34 FBA_DQM6
VMA_DM7 AF35 FBA_DQM7
[23] VMA_WDQS[7:0]
VMA_WDQS0 L34 FBA_DQS_WP0
VMA_WDQS1 H35 FBA_DQS_WP1
VMA_WDQS2 J32 FBA_DQS_WP2
VMA_WDQS3 N31 FBA_DQS_WP3
VMA_WDQS4 AE31 FBA_DQS_WP4
VMA_WDQS5 AJ32 FBA_DQS_WP5
VMA_WDQS6 AJ34 FBA_DQS_WP6
VMA_WDQS7 AC33 FBA_DQS_WP7
[23] VMA_RDQS[7:0]
VMA_RDQS0 L35 FBA_DQS_RN0
VMA_RDQS1 G35 FBA_DQS_RN1
VMA_RDQS2 H31 FBA_DQS_RN2
VMA_RDQS3 N32 FBA_DQS_RN3
VMA_RDQS4 AD32 FBA_DQS_RN4
VMA_RDQS5 AJ31 FBA_DQS_RN5
VMA_RDQS6 AJ35 FBA_DQS_RN6
VMA_RDQS7 AC34 FBA_DQS_RN7
+1.5V_GFX
AA27 FBVDDQ_1
AA29 FBVDDQ_2
AA31 FBVDDQ_3
AB27 FBVDDQ_4
AB29 FBVDDQ_5
AC27 FBVDDQ_6
AD27 FBVDDQ_7
AE27 FBVDDQ_8
AJ28 FBVDDQ_9
B18 FBVDDQ_10
E21 FBVDDQ_11
G17 FBVDDQ_12
G18 FBVDDQ_13
G22 FBVDDQ_14
G8 FBVDDQ_15
G9 FBVDDQ_16
H29 FBVDDQ_17
J14 FBVDDQ_18
J15 FBVDDQ_19
C165 4.7U/6.3V_6
C163 4.7U/6.3V_6
C103 1u/16V_6
C124 1u/16V_6
C140 0.1U/10V_4
C164 0.1U/10V_4
C170 0.1U/10V_4
C614 0.1U/10V_4
C161 0.1U/10V_4
C239 0.1U/10V_4
C169 0.1U/10V_4
C168 0.1U/10V_4
EC2 *150p/50V_4
EC3 *150p/50V_4
EC4 *150p/50V_4
EC5 *150p/50V_4
EC6 *150p/50V_4
EC7 *150p/50V_4
2011/1/10
add for EMI
SP@N12x
FBA_D00 L32 VMA_DQ0
FBA_D01 N33 VMA_DQ1
FBA_D02 L33 VMA_DQ2
FBA_D03 N34 VMA_DQ3
FBA_D04 N35 VMA_DQ4
FBA_D05 P35 VMA_DQ5
FBA_D06 P33 VMA_DQ6
FBA_D07 P34 VMA_DQ7
FBA_D08 K35 VMA_DQ8
FBA_D09 K33 VMA_DQ9
FBA_D10 K34 VMA_DQ10
FBA_D11 H33 VMA_DQ11
FBA_D12 G34 VMA_DQ12
FBA_D13 G33 VMA_DQ13
FBA_D14 E34 VMA_DQ14
FBA_D15 E33 VMA_DQ15
FBA_D16 G31 VMA_DQ16
FBA_D17 F30 VMA_DQ17
FBA_D18 G30 VMA_DQ18
FBA_D19 G32 VMA_DQ19
FBA_D20 K30 VMA_DQ20
FBA_D21 K32 VMA_DQ21
FBA_D22 H30 VMA_DQ22
FBA_D23 K31 VMA_DQ23
FBA_D24 L31 VMA_DQ24
FBA_D25 L30 VMA_DQ25
FBA_D26 M32 VMA_DQ26
FBA_D27 N30 VMA_DQ27
FBA_D28 M30 VMA_DQ28
FBA_D29 P31 VMA_DQ29
FBA_D30 R32 VMA_DQ30
FBA_D31 R30 VMA_DQ31
FBA_D32 AG30 VMA_DQ32
FBA_D33 AG32 VMA_DQ33
FBA_D34 AH31 VMA_DQ34
FBA_D35 AF31 VMA_DQ35
FBA_D36 AF30 VMA_DQ36
FBA_D37 AE30 VMA_DQ37
FBA_D38 AC32 VMA_DQ38
FBA_D39 AD30 VMA_DQ39
FBA_D40 AN33 VMA_DQ40
FBA_D41 AL31 VMA_DQ41
FBA_D42 AM33 VMA_DQ42
FBA_D43 AL33 VMA_DQ43
FBA_D44 AK30 VMA_DQ44
FBA_D45 AK32 VMA_DQ45
FBA_D46 AJ30 VMA_DQ46
FBA_D47 AH30 VMA_DQ47
FBA_D48 AH33 VMA_DQ48
FBA_D49 AH35 VMA_DQ49
FBA_D50 AH34 VMA_DQ50
FBA_D51 AH32 VMA_DQ51
FBA_D52 AJ33 VMA_DQ52
FBA_D53 AL35 VMA_DQ53
FBA_D54 AM34 VMA_DQ54
FBA_D55 AM35 VMA_DQ55
FBA_D56 AF33 VMA_DQ56
FBA_D57 AE32 VMA_DQ57
FBA_D58 AF34 VMA_DQ58
FBA_D59 AE35 VMA_DQ59
FBA_D60 AE34 VMA_DQ60
FBA_D61 AE33 VMA_DQ61
FBA_D62 AB32 VMA_DQ62
FBA_D63 AC35 VMA_DQ63
FBA_CLK0 T32 VMA_CLK0 VMA_CLK0 [23]
FBA_CLK0_N T31 VMA_CLK0# VMA_CLK0# [23]
FBA_CLK1 AC31 VMA_CLK1 VMA_CLK1 [23]
FBA_CLK1_N AC30 VMA_CLK1# VMA_CLK1# [23]
15mils width
(FBA_DEBUG) FBA_DEBUG0 T30 FBA_DEBUG R91 *10K/F_4 +1.5V_GFX
(NC) FBA_DEBUG1 T29 FBA_DEBUG1 R93 *10K/F_4 +1.5V_GFX
FB_VREF_NC J27
4mils width
FB_DLLAVDD1 AG27 +FB_DLLAVDD L5 PBY160808T-30Y-N_6 +1.05V_GFX
(NC) FB_DLLAVDD2 AF28
(NC) FB_DLLAVDD3 J19
FB_PLLAVDD1 AF27
(NC) FB_PLLAVDD2 AE28
(NC) FB_PLLAVDD3 J18
C166 10U/6.3V_6
C146 1U/6.3V_4
C181 0.1U/10V_4
C139 0.1U/10V_4
C176 0.1U/10V_4
U19C
MEMORY I/F C
[24] FBC_CMD[30:0]
FBC_CMD0 F18 FBB_CMD0 (FBC_CMD25)
FBC_CMD1 E19 FBB_CMD1 (FBC_CMD23)
FBC_CMD2 D18 FBC_CMD2
FBC_CMD3 C17 FBB_CMD3 (FBC_CMD0)
FBC_CMD4 F19 FBB_CMD4 (FBC_CMD10)
FBC_CMD5 C19 FBB_CMD5 (FBC_CMD26)
FBC_CMD6 B17 FBB_CMD6 (FBC_CMD14)
FBC_CMD7 E20 FBC_CMD7
FBC_CMD8 B19 FBB_CMD8 (FBC_CMD1)
FBC_CMD9 D20 FBB_CMD9 (FBC_CMD22)
FBC_CMD10 A19 FBB_CMD10 (FBC_CMD20)
FBC_CMD11 D19 FBB_CMD11 (FBC_CMD24)
FBC_CMD12 C20 FBB_CMD12 (FBC_CMD18)
FBC_CMD13 F20 FBB_CMD13 (FBC_CMD9)
FBC_CMD14 B20 FBB_CMD14 (FBC_CMD29)
FBC_CMD15 G21 FBB_CMD15 (FBC_CMD8)
FBC_CMD16 F22 FBB_CMD16 (FBC_CMD27)
FBC_CMD17 F24 FBB_CMD17 (FBC_CMD15)
FBC_CMD18 F23 FBB_CMD18 (FBC_CMD11)
FBC_CMD19 C25 FBB_CMD19 (FBC_CMD16)
FBC_CMD20 C23 FBB_CMD20 (FBC_CMD28)
FBC_CMD21 F21 FBB_CMD21 (FBC_CMD3)
FBC_CMD22 E22 FBB_CMD22 (FBC_CMD17)
FBC_CMD23 D21 FBB_CMD23 (FBC_CMD5)
FBC_CMD24 A23 FBB_CMD24(FBC_CMD4)
FBC_CMD25 D22 FBB_CMD25 (FBC_CMD21)
FBC_CMD26 B23 FBB_CMD26 (FBC_CMD6)
FBC_CMD27 C22 FBB_CMD27 (FBC_CMD13)
FBC_CMD28 B22 FBB_CMD28 (FBC_CMD19)
FBC_CMD29 A22 FBB_CMD29 (FBC_CMD12)
FBC_CMD30 A20 FBC_CMD30
G20 FBC_CMD31 (NC)
[24] VMC_DM[7:0]
VMC_DM0 A16 FBC_DQM0
VMC_DM1 D10 FBC_DQM1
VMC_DM2 F11 FBC_DQM2
VMC_DM3 D15 FBC_DQM3
VMC_DM4 D27 FBC_DQM4
VMC_DM5 D34 FBC_DQM5
VMC_DM6 A34 FBC_DQM6
VMC_DM7 D28 FBC_DQM7
[24] VMC_WDQS[7:0]
VMC_WDQS0 C14 FBC_DQS_WP0
VMC_WDQS1 A10 FBC_DQS_WP1
VMC_WDQS2 E10 FBC_DQS_WP2
VMC_WDQS3 D14 FBC_DQS_WP3
VMC_WDQS4 E26 FBC_DQS_WP4
VMC_WDQS5 D32 FBC_DQS_WP5
VMC_WDQS6 A32 FBC_DQS_WP6
VMC_WDQS7 B26 FBC_DQS_WP7
[24] VMC_RDQS[7:0]
VMC_RDQS0 B14 FBC_DQS_RN0
VMC_RDQS1 B10 FBC_DQS_RN1
VMC_RDQS2 D9 FBC_DQS_RN2
VMC_RDQS3 E14 FBC_DQS_RN3
VMC_RDQS4 F26 FBC_DQS_RN4
VMC_RDQS5 D31 FBC_DQS_RN5
VMC_RDQS6 A31 FBC_DQS_RN6
VMC_RDQS7 A26 FBC_DQS_RN7
+1.5V_GFX
J16 FBVDDQ_20
J17 FBVDDQ_21
J20 FBVDDQ_22
J21 FBVDDQ_23
J22 FBVDDQ_24
J23 FBVDDQ_25
J24 FBVDDQ_26
J29 FBVDDQ_27
N27 FBVDDQ_28
P27 FBVDDQ_29
R27 FBVDDQ_30
T27 FBVDDQ_31
U27 FBVDDQ_32
U29 FBVDDQ_33
V27 FBVDDQ_34
V29 FBVDDQ_35
V34 FBVDDQ_36
W27 FBVDDQ_37
Y27 FBVDDQ_38
SP@N12x
FBC_D00 B13 VMC_DQ0
FBC_D01 D13 VMC_DQ1
FBC_D02 A13 VMC_DQ2
FBC_D03 A14 VMC_DQ3
FBC_D04 C16 VMC_DQ4
FBC_D05 B16 VMC_DQ5
FBC_D06 A17 VMC_DQ6
FBC_D07 D16 VMC_DQ7
FBC_D08 C13 VMC_DQ8
FBC_D09 B11 VMC_DQ9
FBC_D10 C11 VMC_DQ10
FBC_D11 A11 VMC_DQ11
FBC_D12 C10 VMC_DQ12
FBC_D13 C8 VMC_DQ13
FBC_D14 B8 VMC_DQ14
FBC_D15 A8 VMC_DQ15
FBC_D16 E8 VMC_DQ16
FBC_D17 F8 VMC_DQ17
FBC_D18 F10 VMC_DQ18
FBC_D19 F9 VMC_DQ19
FBC_D20 F12 VMC_DQ20
FBC_D21 D8 VMC_DQ21
FBC_D22 D11 VMC_DQ22
FBC_D23 E11 VMC_DQ23
FBC_D24 D12 VMC_DQ24
FBC_D25 E13 VMC_DQ25
FBC_D26 F13 VMC_DQ26
FBC_D27 F14 VMC_DQ27
FBC_D28 F15 VMC_DQ28
FBC_D29 E16 VMC_DQ29
FBC_D30 F16 VMC_DQ30
FBC_D31 F17 VMC_DQ31
FBC_D32 D29 VMC_DQ32
FBC_D33 F27 VMC_DQ33
FBC_D34 F28 VMC_DQ34
FBC_D35 E28 VMC_DQ35
FBC_D36 D26 VMC_DQ36
FBC_D37 F25 VMC_DQ37
FBC_D38 D24 VMC_DQ38
FBC_D39 E25 VMC_DQ39
FBC_D40 E32 VMC_DQ40
FBC_D41 F32 VMC_DQ41
FBC_D42 D33 VMC_DQ42
FBC_D43 E31 VMC_DQ43
FBC_D44 C33 VMC_DQ44
FBC_D45 F29 VMC_DQ45
FBC_D46 D30 VMC_DQ46
FBC_D47 E29 VMC_DQ47
FBC_D48 B29 VMC_DQ48
FBC_D49 C31 VMC_DQ49
FBC_D50 C29 VMC_DQ50
FBC_D51 B31 VMC_DQ51
FBC_D52 C32 VMC_DQ52
FBC_D53 B32 VMC_DQ53
FBC_D54 B35 VMC_DQ54
FBC_D55 B34 VMC_DQ55
FBC_D56 A29 VMC_DQ56
FBC_D57 B28 VMC_DQ57
FBC_D58 A28 VMC_DQ58
FBC_D59 C28 VMC_DQ59
FBC_D60 C26 VMC_DQ60
FBC_D61 D25 VMC_DQ61
FBC_D62 B25 VMC_DQ62
FBC_D63 A25 VMC_DQ63
FBC_CLK0 E17 VMC_CLK0 VMC_CLK0 [24]
FBC_CLK0_N D17 VMC_CLK0# VMC_CLK0# [24]
FBC_CLK1 D23 VMC_CLK1 VMC_CLK1 [24]
FBC_CLK1_N E23 VMC_CLK1# VMC_CLK1# [24]
(FBC_DEBUG) FBB_DEBUG0 G19 FBC_DEBUG R82 *10K/F_4 +1.5V_GFX
(NC) FBB_DEBUG1 G16 FBC_DEBUG1 R80 *10K/F_4 +1.5V_GFX
FB_CAL_PD_VDDQ K27 FB_CAL_PD_VDDQ R84 40.2/F_4 +1.5V_GFX
(NC) FB_CAL_PD_VDDQ K28
FB_CAL_PU_GND L27 FB_CAL_PU_GND R85 40.2/F_4
(NC) FB_CAL_PU_GND L28
FB_CAL_TERM_GND M27 FB_CAL_TERM_GND R87 60.4/F_4
(NC) FB_CAL_TERM_GND M28
FBA_CMD2 R155 10K/F_4
FBA_CMD3 R480 10K/F_4
FBA_CMD5 R485 10K/F_4
FBA_CMD18 R486 10K/F_4
FBA_CMD19 R160 10K/F_4
FBC_CMD2 R73 10K/F_4
FBC_CMD3 R449 10K/F_4
FBC_CMD5 R83 10K/F_4
FBC_CMD18 R455 10K/F_4
FBC_CMD19 R88 10K/F_4
For Fermi
[18,20,45] +1.05V_GFX
[20,23,24,27,45] +1.5V_GFX

Quanta Computer Inc.

PROJECT : ZRH

Size	Document Number	Rev
	DGPU 2/5 (Memory)	1A

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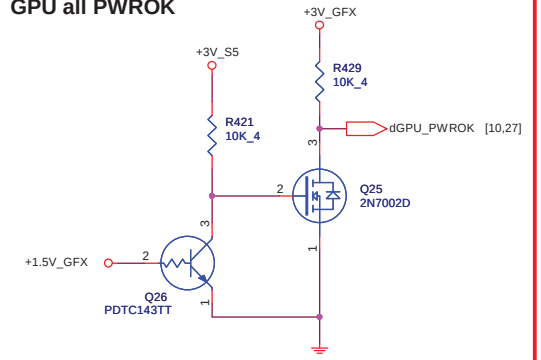
[18,19,45] +1.05V_GFX
[18,21,36,44,45] +3V_GFX

U19D

[IFPA/B_LVDS]
[IFPC/D_TMDS]
[IFPE/F_DP]
[DACA/B_CRT]
[XTAL IN]

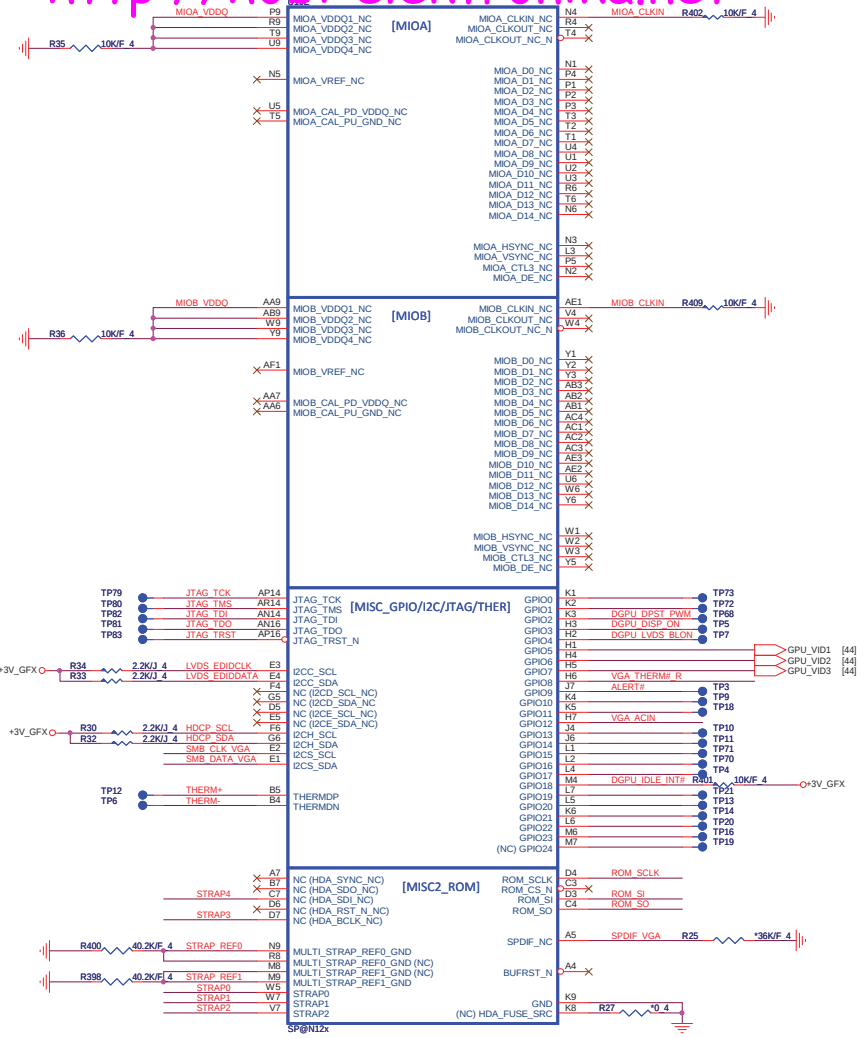
SP@N12x

GPU all PWROK



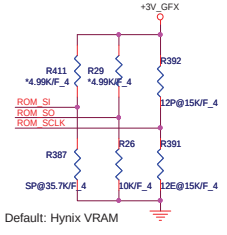
2010/11/25
change to 27P

Quanta Computer Inc.		
PROJECT : ZRH		
Size	Document Number: DGPU 3/5 (Display)	Rev 1A
Date: Friday, January 14, 2011	Sheet 20 of 50	

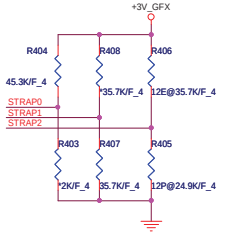


	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	N12P-GS	N12E-GE
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	1010	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	0XXX	0XXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	0100	1110
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110	0110
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111	1111

ROM_SI	DESCRIPTION	Vendor P/N	ROM_SI	Quanta P/N B/S
0010	Hynix DDR3 64Mx16x8, 1GB,900MHz	H5TQ1G63DFR-11C	PD 15K	AKD5LZWTW05
0011	Samsung DDR3 64Mx16x8, 1GB,900MHz	K4W1G1646E-HC11	PD 20K	
0110	Hynix DDR3 128Mx16x8, 2GB,900MHz	H5TQ2G63BFR-11C	PD 35K	
0111	Samsung DDR3 128Mx16x8, 2GB,900MHz	K4W2G1646C-HC11	PD 45K	



Default: Hynix VRAM

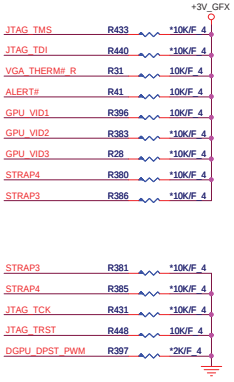


Logical Strap Bit Mapping

	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

CHIP	N12P-GS	N12E-GE
ROM_SCLK	PU 15K	PD 15K
STRAP2	PD 25K	PU 35K

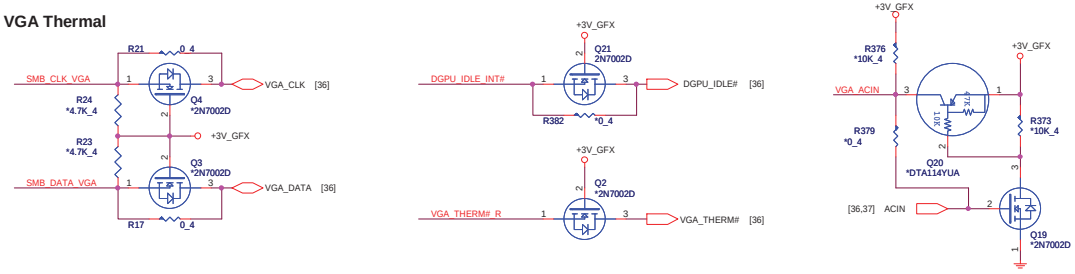
4.99K/F_4: CS24992FB26 [RES CHIP 4.99K 1/16W +1%(0402)]
10K/F_4: CS31002FB26 [RES CHIP 10K 1/16W +1% (0402)]
15K/F_4: CS31502FB24 [RES CHIP 15K 1/16W +1% (0402)]
30.1K/F_4: CS33012FB18 [RES CHIP 30.1K 1/16W +-1%(0402)]
35.7K/F_4: CS33572FB13 [RES CHIP 35.7K 1/16W +-1%(0402)]
45.3K/F_4: CS34532FB18 [RES CHIP 45.3K 1/16W +-1% (0402)]
20K/F_4: CS32002FB29 RES CHIP 20K 1/16W +-1%(0402)



GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID1
6	OUT	N/A	NVVDD VID2
7	OUT	N/A	NVVDD VID3
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

VGA Thermal



Quanta Computer Inc.		
PROJECT : ZRH		
Size	Document Number: DGPU 4/5 (MIO/GPIO)	Rev 1A
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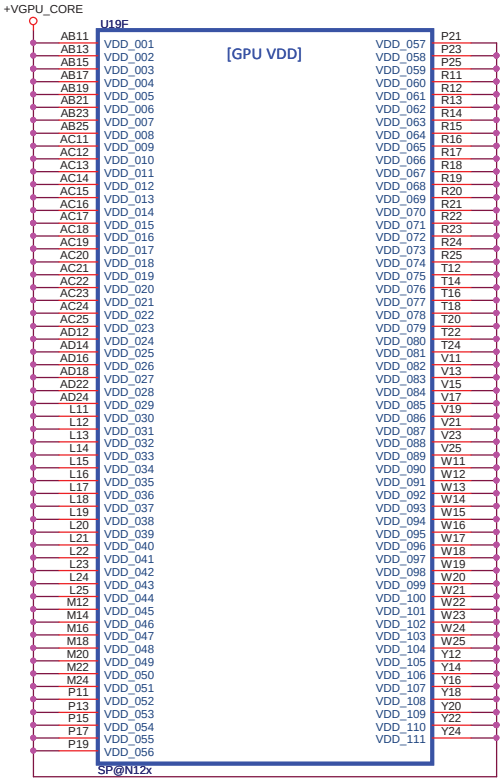

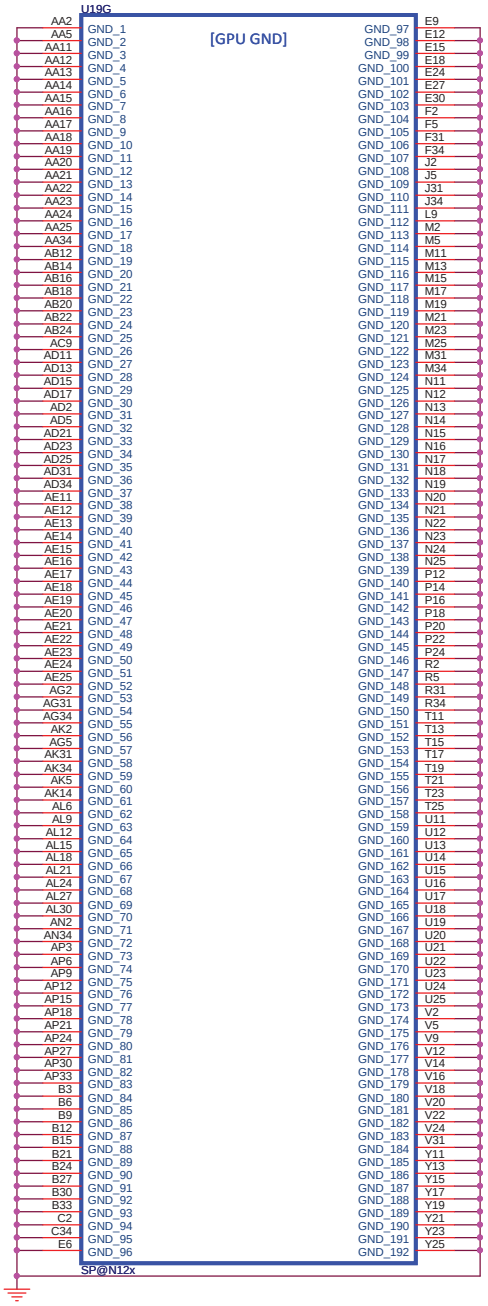

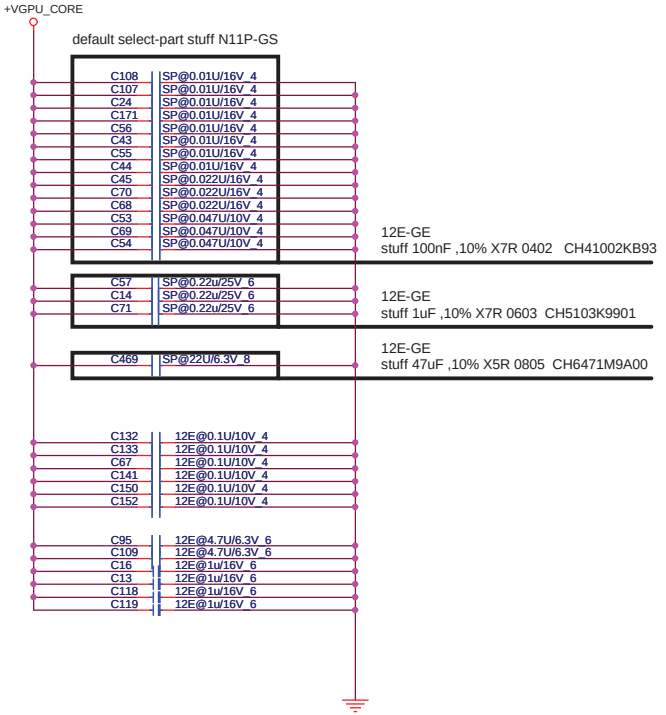

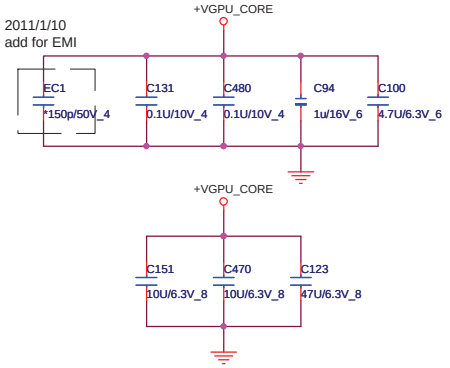

SPEC	GB2-128 12P-GS	GB3-128 12E-GE
10nF ,10% X7R 0402	8	
22nF ,10% X7R 0402	3	
47nF ,10% X7R 0402	3	
100nF ,10% X7R 0402	2	22
220nF ,10% X7R 0603	3	
1uF ,10% X7R 0603	1	8
4.7uF ,10% X5R 0603	1	3
10uF ,10% X5R 0805	2	2
22uF ,10% X5R 0805	1	
47uF ,10% X5R 0805	1	2
470uF	1	

Quanta Computer Inc.

PROJECT : ZRH

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	DGPU 5/5 (Power/Ground)	1A

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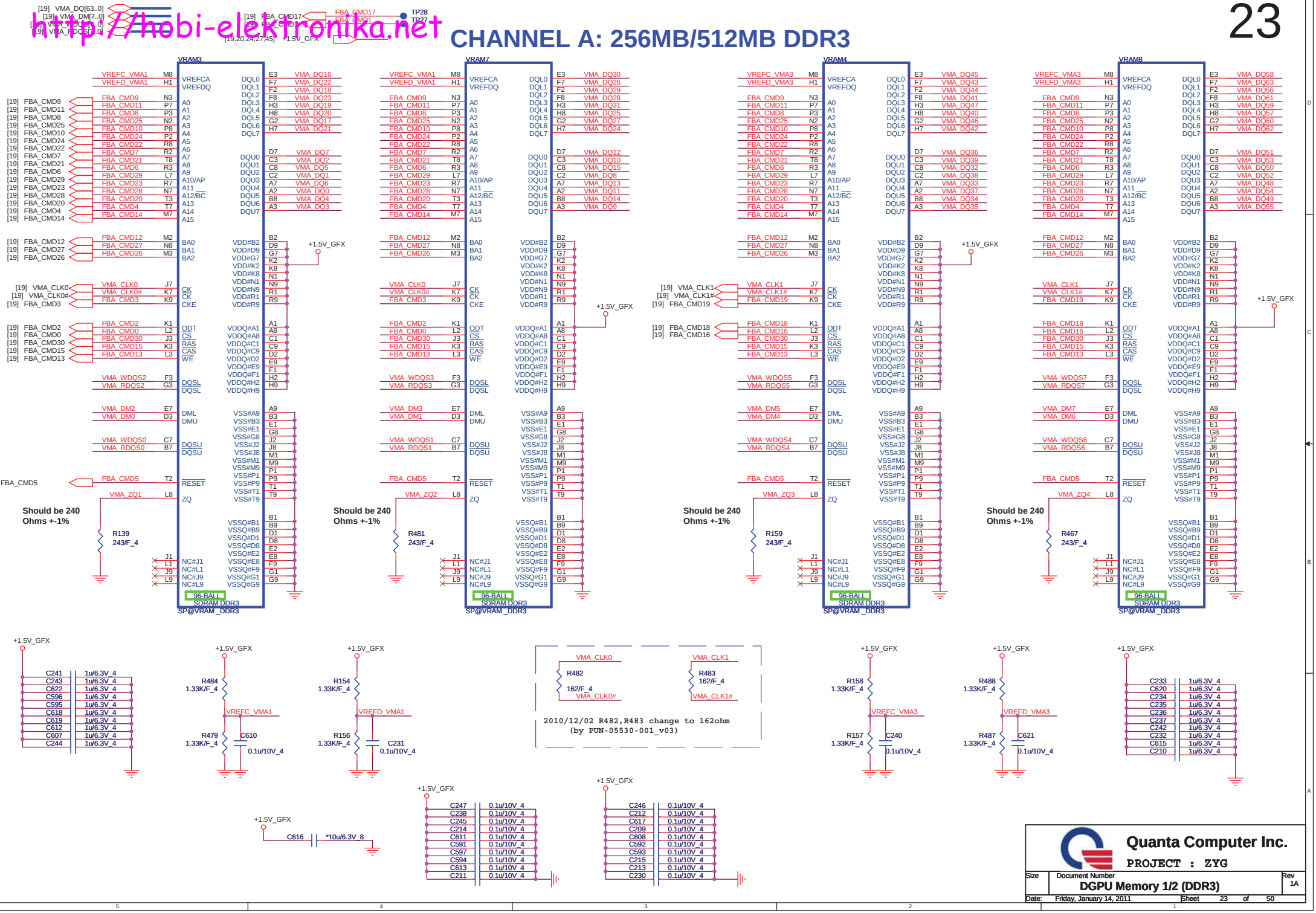
CHANNEL A: 256MB/512MB DDR3



Quanta Computer Inc.		
PROJECT : ZYG		
Size	Document Number	Rev
	DGPU Memory 1/2 (DDR3)	1A
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CHANNEL B: 256MB/512MB DDR3

[19] VMC_DQ[63..0]
[19] VMC_DM[7..0]
[19] VMC_DQS[7..0]
[19] VMC_DQS#[7..0]

[19] FBC_CMD17
[19] FBC_CMD1
FBC_CMD17
FBC_CMD1
TP26
TP24

[19,20,23,24,45] +1.5V_GFX

VRAM5

VREFC_VMC1 M8
VREFD_VMC1 H1
VREFCA
VREFDQ

[19] FBC_CMD9 N3
[19] FBC_CMD11 P7
[19] FBC_CMD8 P3
[19] FBC_CMD25 N2
[19] FBC_CMD10 P8
[19] FBC_CMD24 P2
[19] FBC_CMD22 R8
[19] FBC_CMD7 R2
[19] FBC_CMD21 T8
[19] FBC_CMD6 R3
[19] FBC_CMD29 L7
[19] FBC_CMD23 R7
[19] FBC_CMD28 N7
[19] FBC_CMD20 T3
[19] FBC_CMD4 T7
[19] FBC_CMD14 M7
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12/BC A13 A14 A15

[19] FBC_CMD12 M2
[19] FBC_CMD27 N8
[19] FBC_CMD26 M3
BA0 BA1 BA2

[19] VMC_CLK0
[19] VMC_CLK0#
[19] FBC_CMD3
VMC_CLK0 J7
VMC_CLK0# K7
FBC_CMD3 K9
CK CK CKE

[19] FBC_CMD2
[19] FBC_CMD0
[19] FBC_CMD30
[19] FBC_CMD15
[19] FBC_CMD13
FBC_CMD2 K1
FBC_CMD0 L2
FBC_CMD30 J3
FBC_CMD15 K3
FBC_CMD13 L3
ODT CS RAS CAS WE

VMC_WDQS2 F3
VMC_RDQS2 G3
DQSL DQSL

VMC_DM2 E7
VMC_DM0 D3
DML DMU

VMC_WDQS0 C7
VMC_RDQS0 B7
DQSU DQSU

[19] FBC_CMD5 T2
RESET

VMC_ZQ1 L8
ZQ

VDD#B2 VDD#D9 VDD#G7 VDD#K2 VDD#K8 VDD#N1 VDD#N9 VDD#R1 VDD#R9
VDDQ#A1 VDDQ#A8 VDDQ#C1 VDDQ#C9 VDDQ#D2 VDDQ#E9 VDDQ#F1 VDDQ#H2 VDDQ#H9
VSS#A9 VSS#B3 VSS#E1 VSS#G8 VSS#J2 VSS#J8 VSS#M1 VSS#M9 VSS#P1 VSS#P9 VSS#T1 VSS#T9
VSSQ#B1 VSSQ#B9 VSSQ#D1 VSSQ#D8 VSSQ#E2 VSSQ#E8 VSSQ#F9 VSSQ#G1 VSSQ#G9
NC#J1 NC#L1 NC#J9 NC#L9

DQL0 DQL1 DQL2 DQL3 DQL4 DQL5 DQL6 DQL7
DQU0 DQU1 DQU2 DQU3 DQU4 DQU5 DQU6 DQU7

VMC_DQ21 VMC_DQ16 VMC_DQ18 VMC_DQ17 VMC_DQ23 VMC_DQ19 VMC_DQ20 VMC_DQ22
VMC_DQ0 VMC_DQ4 VMC_DQ2 VMC_DQ7 VMC_DQ1 VMC_DQ6 VMC_DQ3 VMC_DQ5

+1.5V_GFX

96-BALL SDRAM DDR3
SP@VRAM_DDR3

Should be 240 Ohms +-1%
R451 243/F_4

VRAM1

VREFC_VMC1 M8
VREFD_VMC1 H1

FBC_CMD9 N3
FBC_CMD11 P7
FBC_CMD8 P3
FBC_CMD25 N2
FBC_CMD10 P8
FBC_CMD24 P2
FBC_CMD22 R8
FBC_CMD7 R2
FBC_CMD21 T8
FBC_CMD6 R3
FBC_CMD29 L7
FBC_CMD23 R7
FBC_CMD28 N7
FBC_CMD20 T3
FBC_CMD4 T7
FBC_CMD14 M7

FBC_CMD12 M2
FBC_CMD27 N8
FBC_CMD26 M3

VMC_CLK0 J7
VMC_CLK0# K7
FBC_CMD3 K9

FBC_CMD2 K1
FBC_CMD0 L2
FBC_CMD30 J3
FBC_CMD15 K3
FBC_CMD13 L3

VMC_WDQS3 F3
VMC_RDQS3 G3

VMC_DM3 E7
VMC_DM1 D3

VMC_WDQS1 C7
VMC_RDQS1 B7

FBC_CMD5 T2

VMC_ZQ2 L8

VMC_DQ24 VMC_DQ28 VMC_DQ26 VMC_DQ25 VMC_DQ30 VMC_DQ31 VMC_DQ27 VMC_DQ29
VMC_DQ8 VMC_DQ12 VMC_DQ9 VMC_DQ15 VMC_DQ11 VMC_DQ13 VMC_DQ10 VMC_DQ14

+1.5V_GFX

Should be 240 Ohms +-1%
R66 243/F_4

VRAM2

VREFC_VMC3 M8
VREFD_VMC3 H1

FBC_CMD9 N3
FBC_CMD11 P7
FBC_CMD8 P3
FBC_CMD25 N2
FBC_CMD10 P8
FBC_CMD24 P2
FBC_CMD22 R8
FBC_CMD7 R2
FBC_CMD21 T8
FBC_CMD6 R3
FBC_CMD29 L7
FBC_CMD23 R7
FBC_CMD28 N7
FBC_CMD20 T3
FBC_CMD4 T7
FBC_CMD14 M7

FBC_CMD12 M2
FBC_CMD27 N8
FBC_CMD26 M3

[19] VMC_CLK1
[19] VMC_CLK1#
[19] FBC_CMD19
VMC_CLK1 J7
VMC_CLK1# K7
FBC_CMD19 K9

[19] FBC_CMD18
[19] FBC_CMD16
FBC_CMD18 K1
FBC_CMD16 L2
FBC_CMD30 J3
FBC_CMD15 K3
FBC_CMD13 L3

VMC_WDQS4 F3
VMC_RDQS4 G3

VMC_DM4 E7
VMC_DM5 D3

VMC_WDQS5 C7
VMC_RDQS5 B7

FBC_CMD5 T2

VMC_ZQ3 L8

VMC_DQ35 VMC_DQ34 VMC_DQ32 VMC_DQ33 VMC_DQ37 VMC_DQ36 VMC_DQ39 VMC_DQ38
VMC_DQ40 VMC_DQ42 VMC_DQ41 VMC_DQ45 VMC_DQ43 VMC_DQ47 VMC_DQ44 VMC_DQ46

+1.5V_GFX

Should be 240 Ohms +-1%
R86 243/F_4

VRAM6

VREFC_VMC3 M8
VREFD_VMC3 H1

FBC_CMD9 N3
FBC_CMD11 P7
FBC_CMD8 P3
FBC_CMD25 N2
FBC_CMD10 P8
FBC_CMD24 P2
FBC_CMD22 R8
FBC_CMD7 R2
FBC_CMD21 T8
FBC_CMD6 R3
FBC_CMD29 L7
FBC_CMD23 R7
FBC_CMD28 N7
FBC_CMD20 T3
FBC_CMD4 T7
FBC_CMD14 M7

FBC_CMD12 M2
FBC_CMD27 N8
FBC_CMD26 M3

VMC_CLK1 J7
VMC_CLK1# K7
FBC_CMD19 K9

FBC_CMD18 K1
FBC_CMD16 L2
FBC_CMD30 J3
FBC_CMD15 K3
FBC_CMD13 L3

VMC_WDQS6 F3
VMC_RDQS6 G3

VMC_DM6 E7
VMC_DM7 D3

VMC_WDQS7 C7
VMC_RDQS7 B7

FBC_CMD5 T2

VMC_ZQ4 L8

VMC_DQ52 VMC_DQ48 VMC_DQ55 VMC_DQ53 VMC_DQ49 VMC_DQ50 VMC_DQ54 VMC_DQ51
VMC_DQ61 VMC_DQ58 VMC_DQ62 VMC_DQ56 VMC_DQ60 VMC_DQ59 VMC_DQ63 VMC_DQ57

+1.5V_GFX

Should be 240 Ohms +-1%
R461 243/F_4

Decoupling

+1.5V_GFX
C516 C158 C599 C598 C574 C557 C188 C563 C519 C589 1u/6.3V_4

+1.5V_GFX
R434 1.33K/F_4
VREFC_VMC1
R446 1.33K/F_4
C527 0.1u/10V_4

+1.5V_GFX
R53 1.33K/F_4
VREFD_VMC1
R56 1.33K/F_4
C62 0.1u/10V_4

VMC_CLK0
R65 162/F_4
VMC_CLK0#
VMC_CLK1
R92 162/F_4
VMC_CLK1#

2010/12/02 R65,R92 change to 162ohm
(by PUN-05530-001_v03)

+1.5V_GFX
R460 1.33K/F_4
VREFC_VMC3
R458 1.33K/F_4
C561 0.1u/10V_4

+1.5V_GFX
R101 1.33K/F_4
VREFD_VMC3
R98 1.33K/F_4
C178 0.1u/10V_4

+1.5V_GFX
C502 C51 C60 C66 C46 C33 C507 C503 C580 C524 1u/6.3V_4

+1.5V_GFX
C581 *10u/6.3V_8

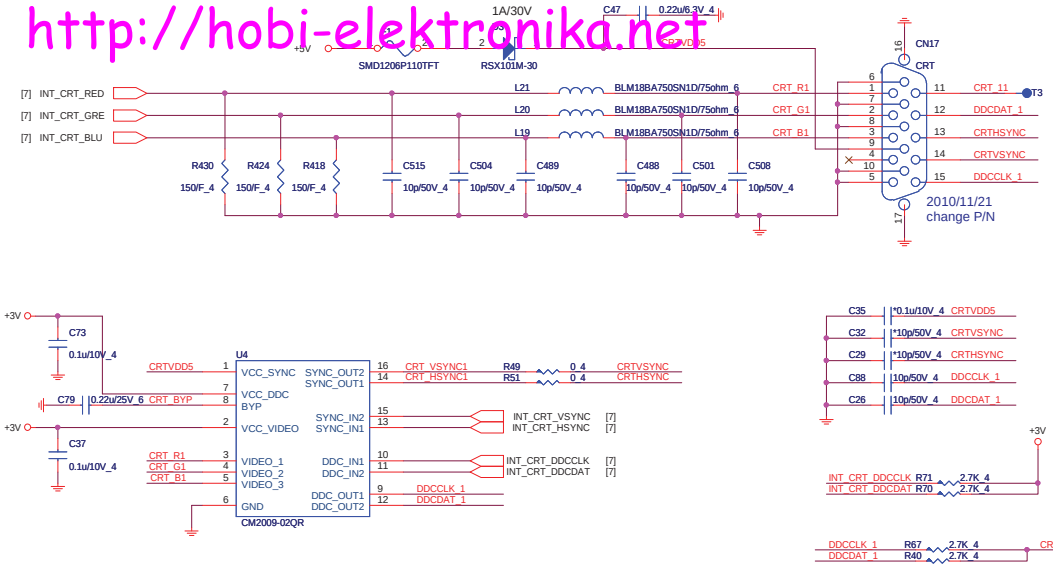
+1.5V_GFX
C476 C475 C600 C590 C87 C509 C578 C588 C517 C479 0.1u/10V_4

+1.5V_GFX
C601 C518 C477 C506 C575 C568 C191 C478 C571 C195 0.1u/10V_4

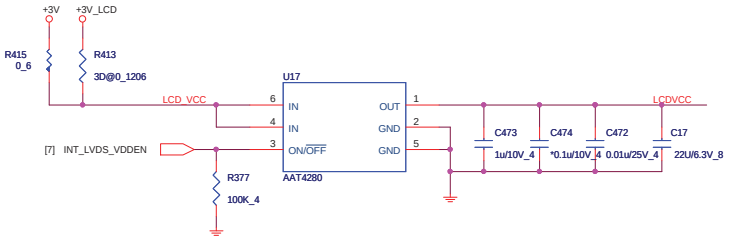
Quanta Computer Inc.
PROJECT : ZYG

Size	Document Number	Rev
	DGPU Memory 2/2 (DDR3)	1A
Date: Friday, January 14, 2011	Sheet 24 of 50	

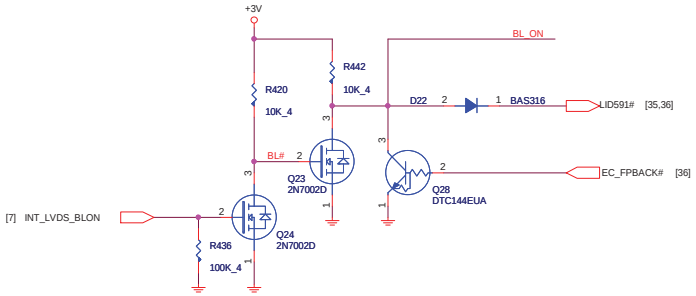
CRT



LCD Power

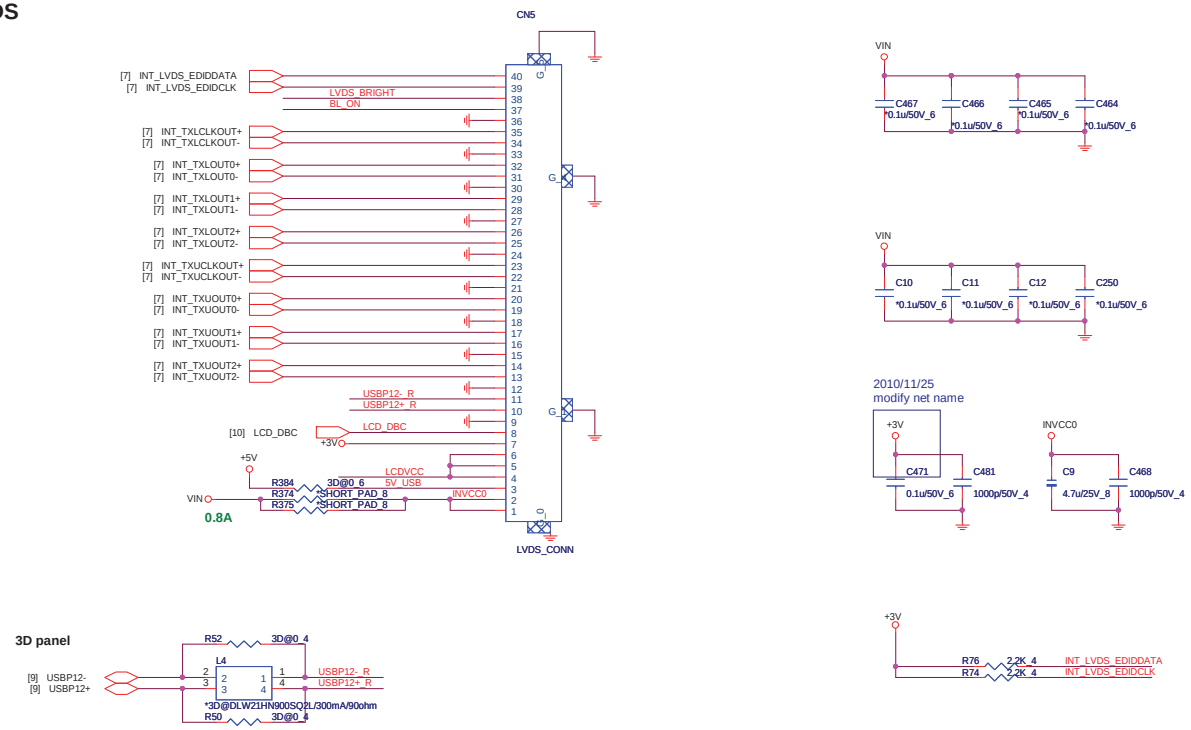


Backlight Control



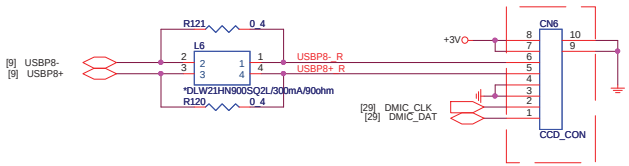
Brightness Control

LVDS



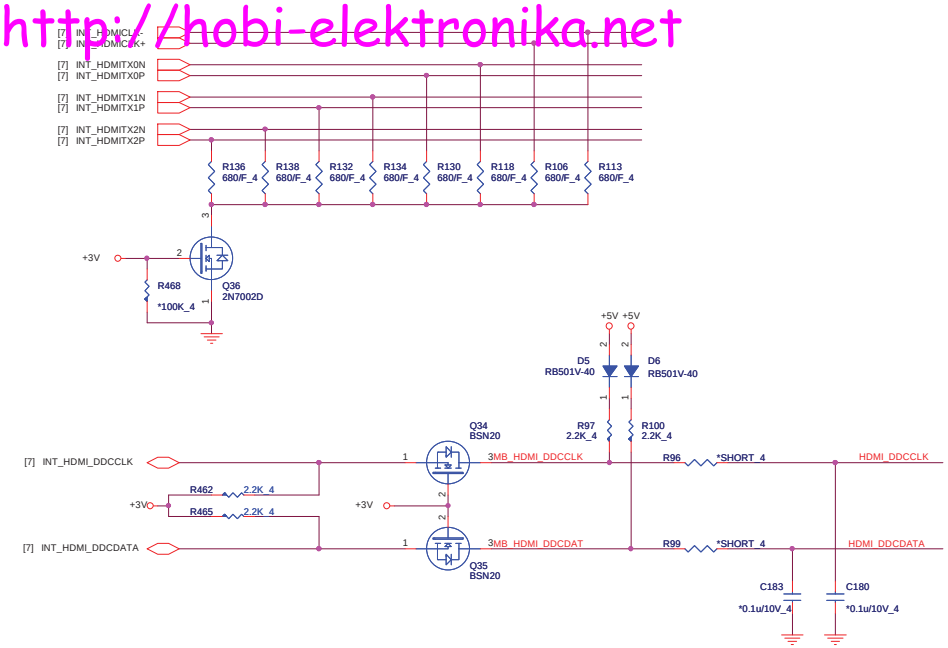
3D panel

CCD & MIC

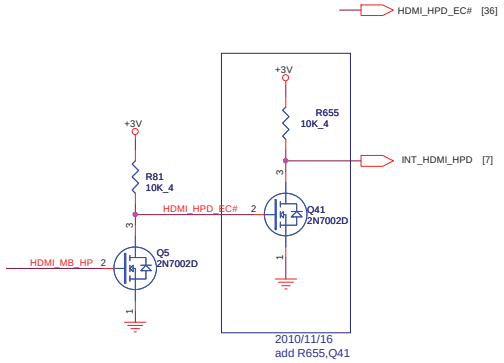


Quanta Computer Inc.			
PROJECT : ZRH			
Size	Document Number		Rev
	CRT/LVDS/LID		1A
Date: Friday, January 14, 2011	Sheet 25 of 50		

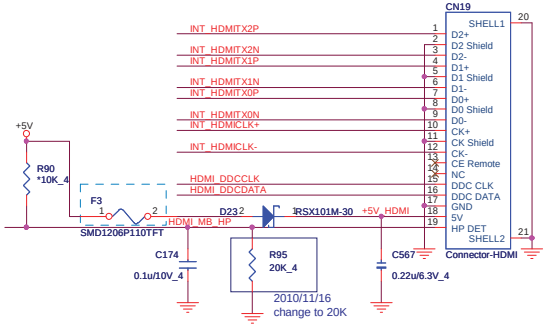
HDMI



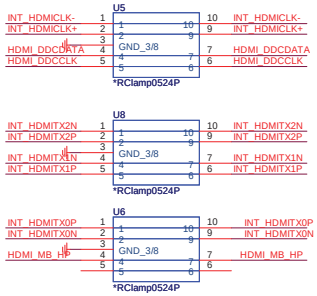
HDMI -detect



HDMI connector



ESD Protect



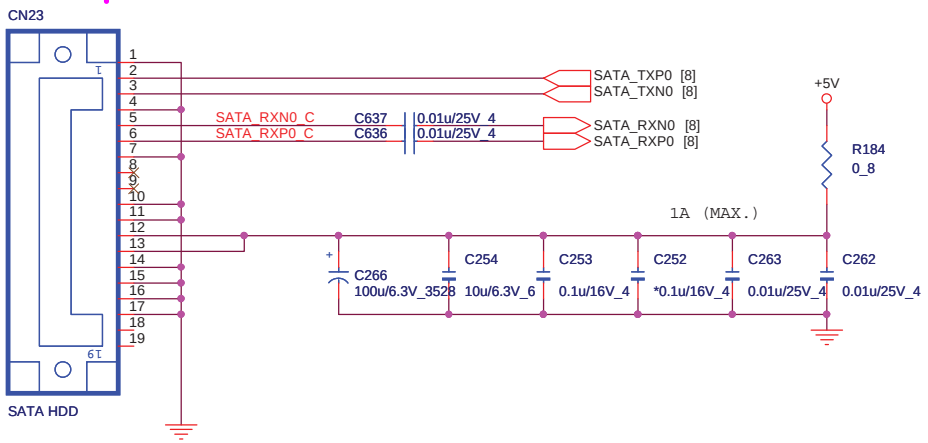
Quanta Computer Inc.

PROJECT : ZRH

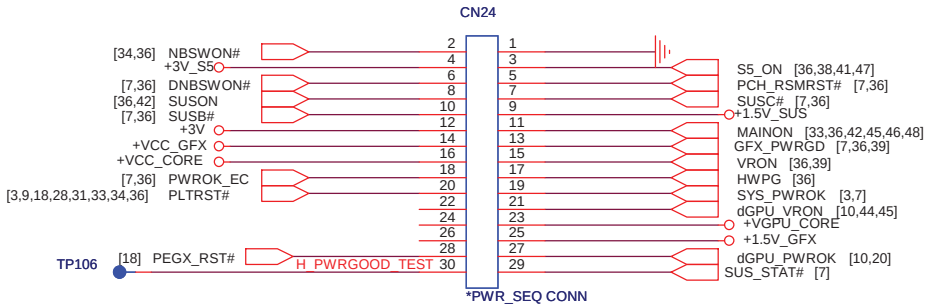
Size	Document Number	Rev
	HDMI/ LEVEL SHIFTER	1A

Date: Friday, January 14, 2011 Sheet 26 of 50

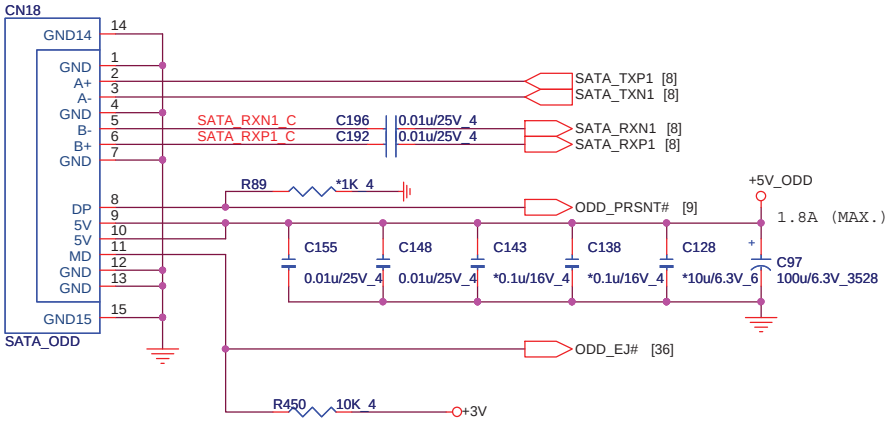
SATA HDD



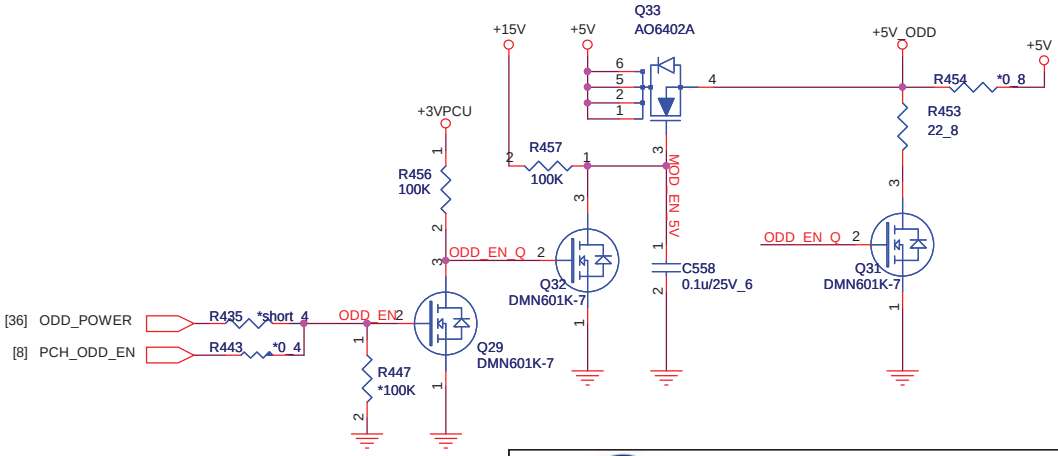
Power sequence



ODD (SATA)



ODD Power (SATA)



Quanta Computer Inc.

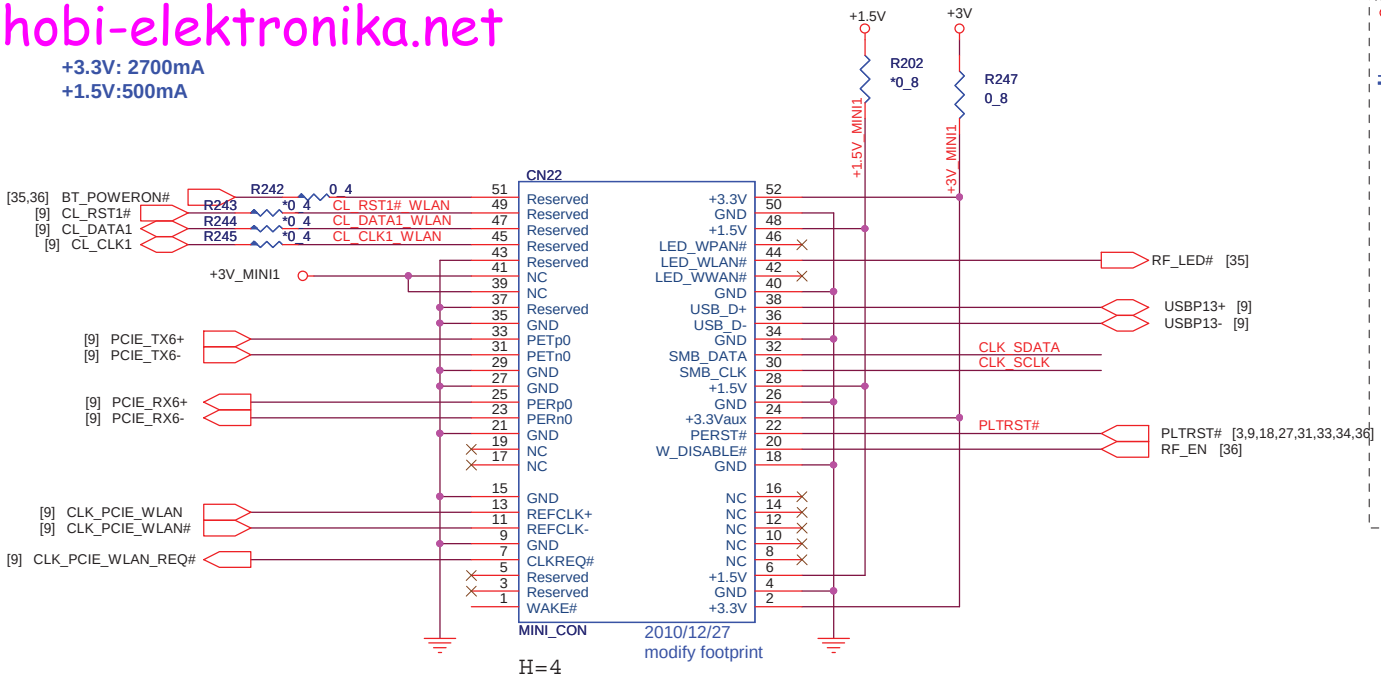
PROJECT : ZRH

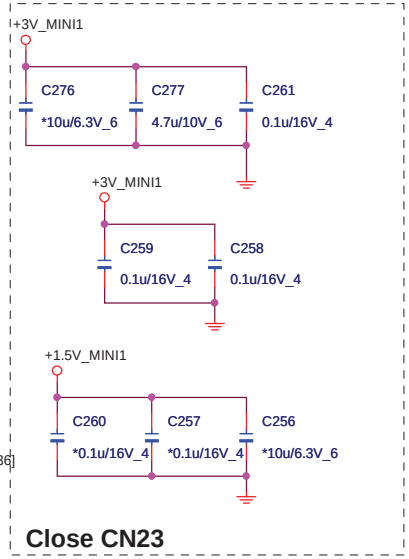
Size	Document Number	Rev
	SATA-HDD/ODD	1A
Date: Friday, January 14, 2011	Sheet 27 of 50	

Wireless

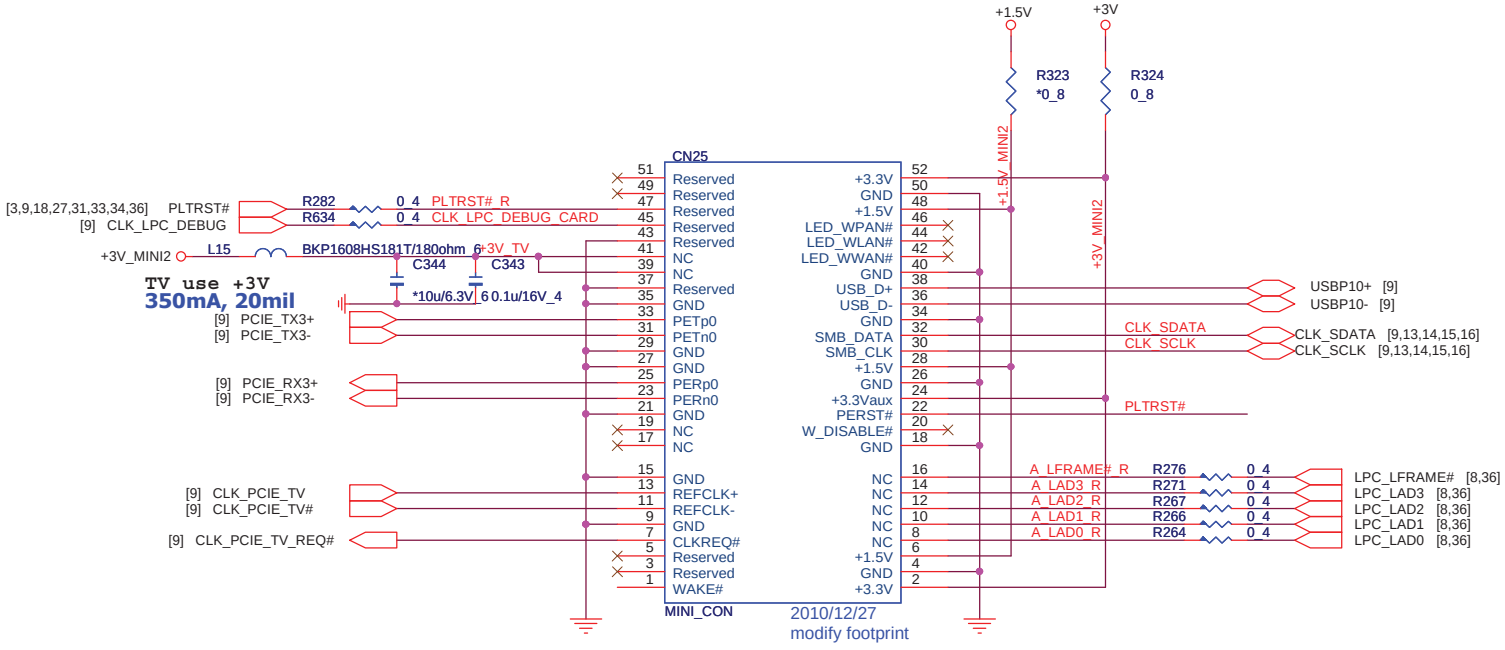
http://hobi-elektronika.net

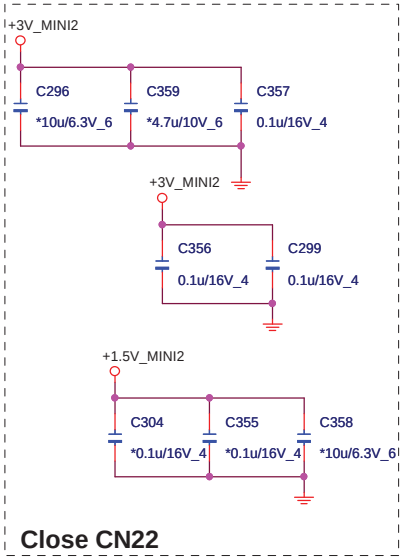
+3.3V: 2700mA
+1.5V:500mA





TV and Debug



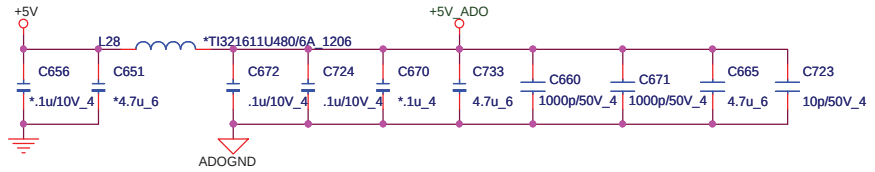


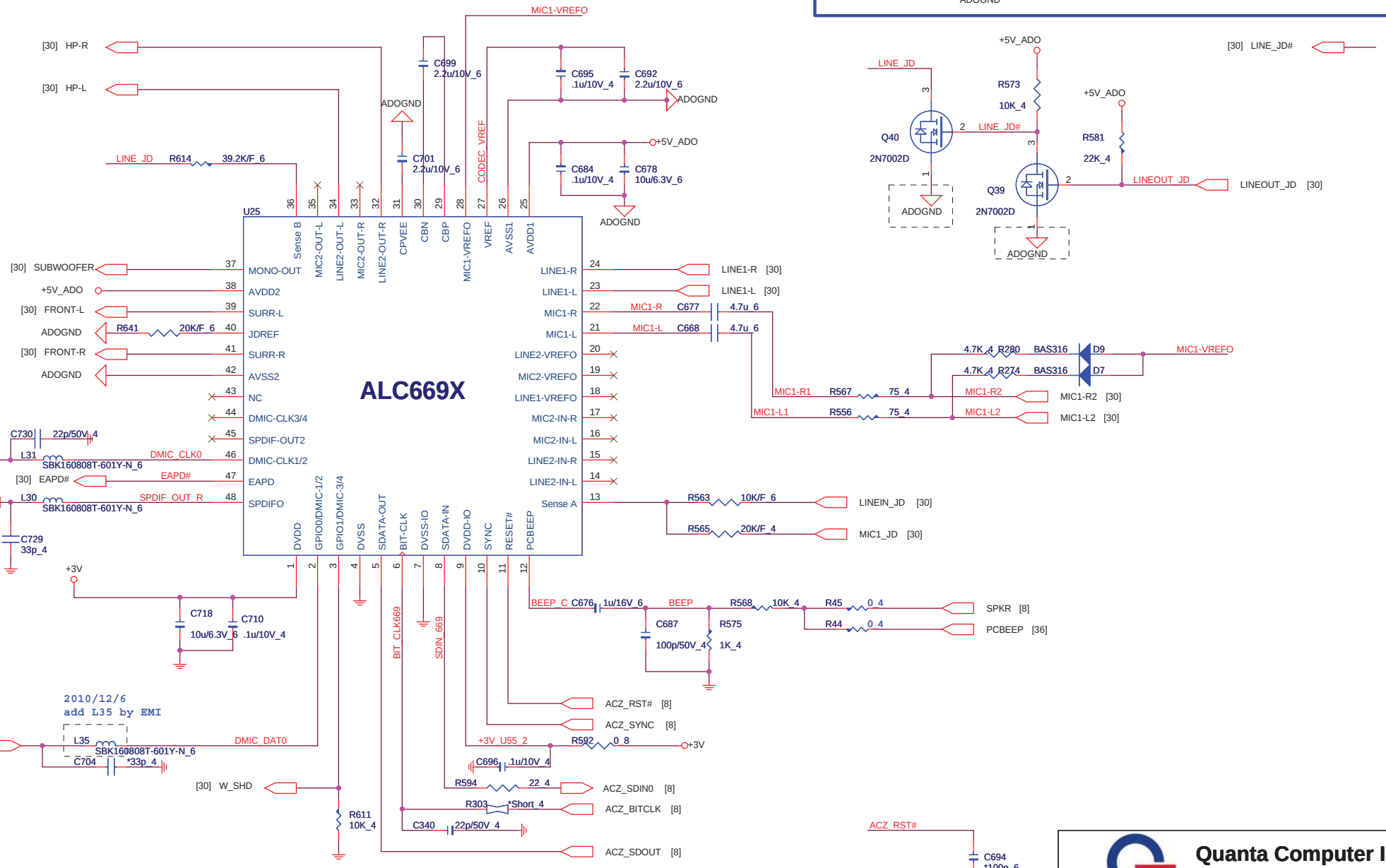
Quanta Computer Inc.
PROJECT : ZRH

Size	Document Number	Rev
	MINI PCI-E card/TV	1A
Date: Friday, January 14, 2011	Sheet 28 of 50	

CODEC(ALC669X)

CODEC/AMP Power





Quanta Computer Inc.		
PROJECT : ZRH		
Size	Document Number: REALTEK ALC889X/MONO-AMP	Rev: 1A
Date: Friday, January 14, 2011	Sheet 29 of 50	

AMP & INT Speaker

AGC ON Level Setting

R595 (AGC_Lv1)	R591 (AGC_Lv2)	Po (RL = 4 Ω)
Low	Low	2.0 W
Low	High	1.8 W
High	Low	1.5 W
High	High	1.0 W

Panasonic AN12947A

SPK

HP

2010/12/6 add AND gate

SUBWOOFER

SUBWOOFER Power(AMP)

SUBWOOFER CONN

AMO GAIN

2010/12/2 change to 0 ohm

LPF for fc(-3dB)=500Hz

SDZ ::shutdown signal for IC<LOW=disable , HIGH=enable>

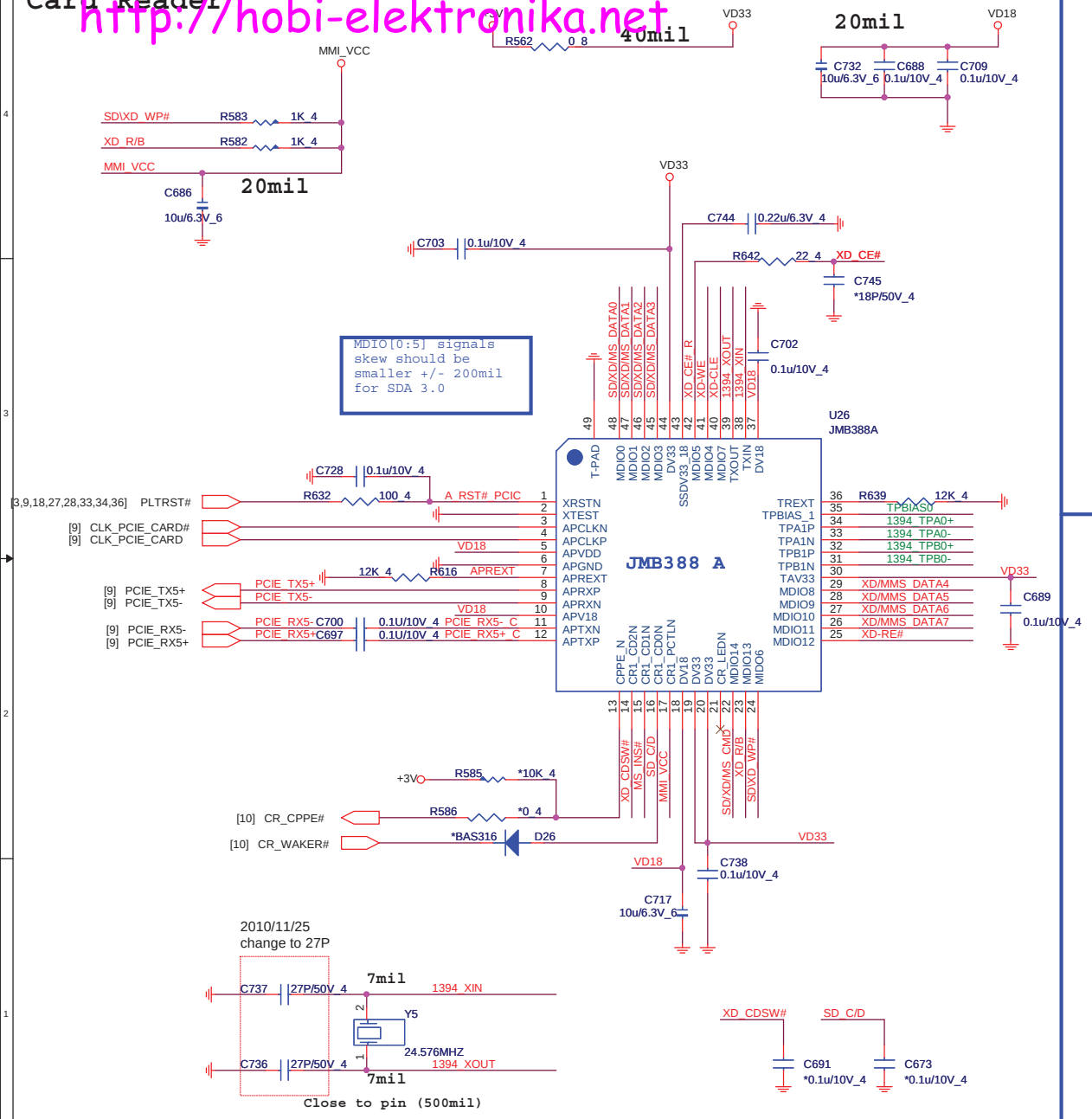
SHUTDOWN	TPA3110D1
L (0V~0.8V)	SHUTDOWN
H (2V ~ VDD)	ACTIVE

To USB AUDIO/B

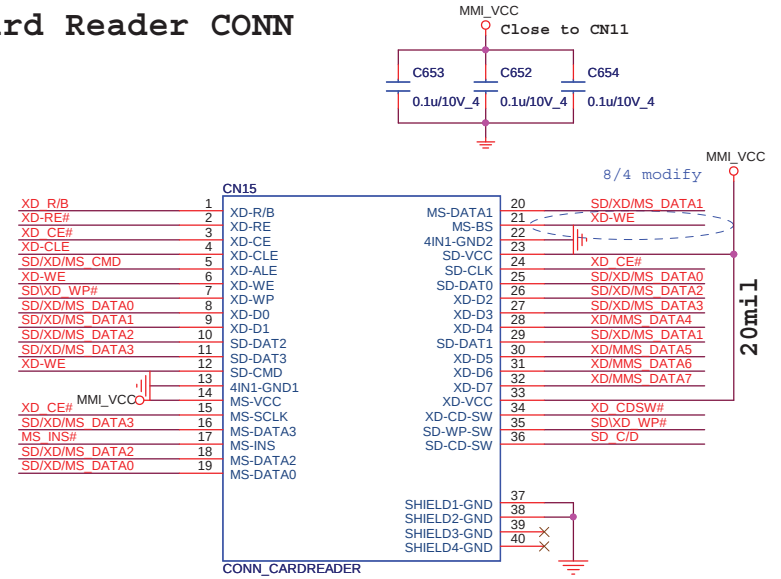
2010/11/30
SWAP CN12 pin define
2010/12/6
pin 7.8 change to +5VPCU
pin 20 change to GND

Quanta Computer Inc.	
PROJECT : ZRH	
Size	Document Number: AMP/AUDIO JACK/WOOFER — Rev 1A
Date: Friday, January 14, 2011	Sheet 30 of 50

Card Reader

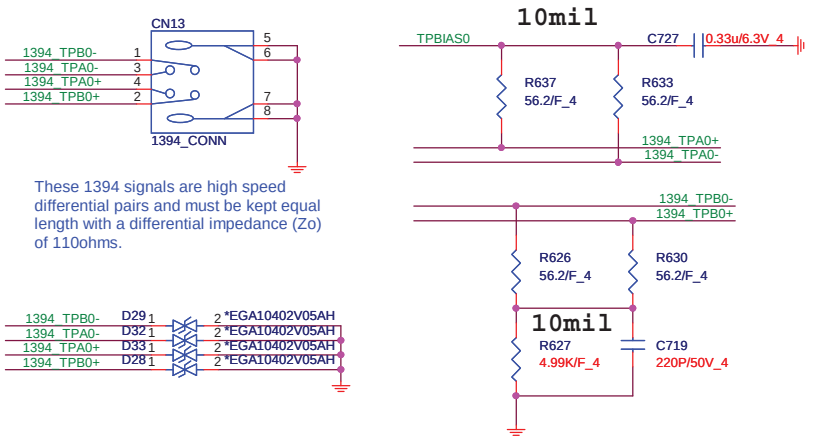


Card Reader CONN



1394

[FIW]



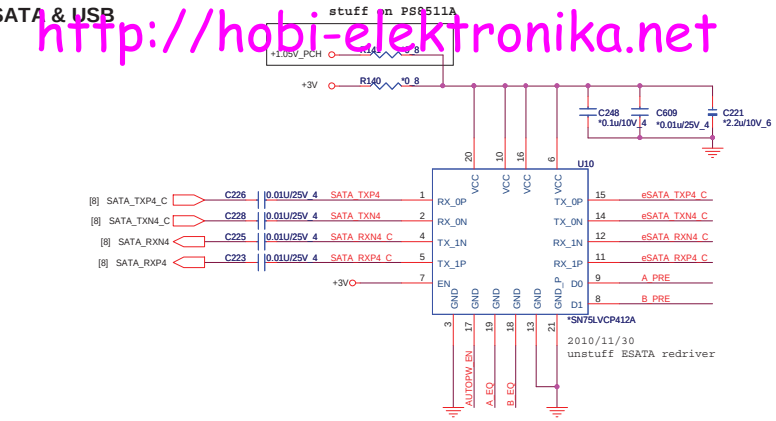
These 1394 signals are high speed differential pairs and must be kept equal length with a differential impedance (Zo) of 110ohms.

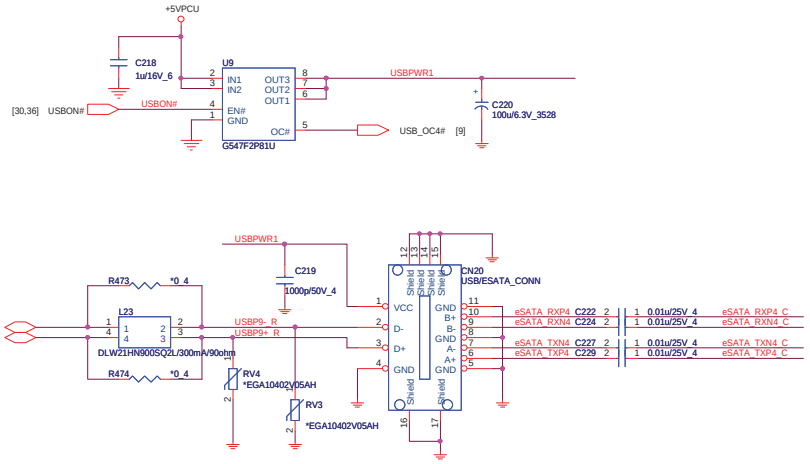
Quanta Computer Inc.

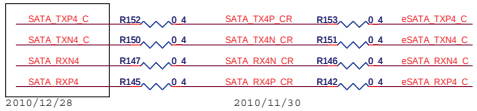
PROJECT : ZRH

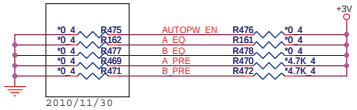
Size	Document Number	Rev
	Card Reader & 1394	1A
Date: Friday, January 14, 2011	Sheet 31 of 50	

ESATA & USB









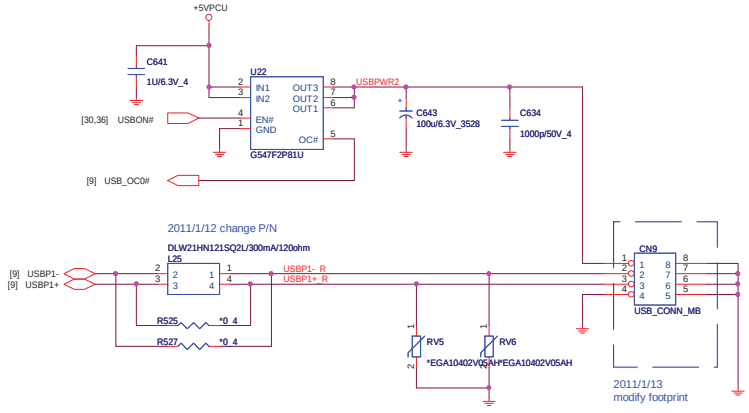
AL008511001

EN	A_PRE	B_PRE	dB
0	X	X	Power down mode
1	0	0	Pre-emphasis disable
1	1	1	Pre-emphasis enable

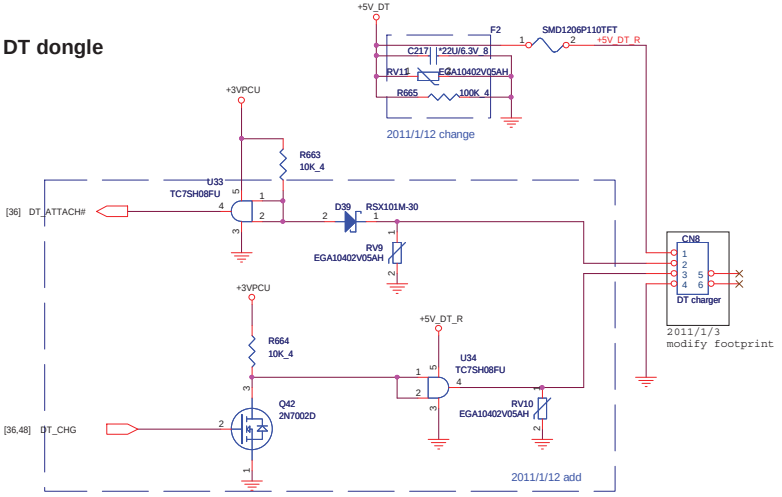
ALLVC412000

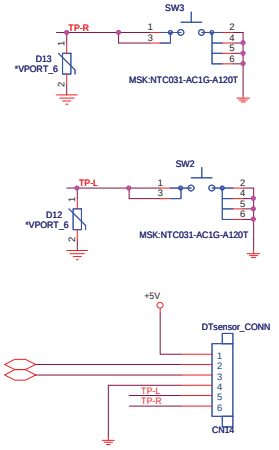
EN	D0	D1	CH-0	CH-1
0	X	X	Standby	Standby
1	0	0	0dB	0dB
1	1	0	Pre-emphasis (5dB)	0dB
1	0	1	0dB	Pre-emphasis (5dB)
1	1	1	Pre-emphasis (5dB)	Pre-emphasis (5dB)

MB USB dual way



DT dongle





	DT IN	DT OUT
DT_PLUG#	LO	HI

Quanta Computer Inc.

PROJECT : ZRH

Size	Document Number	Rev
	USB/eSATA	1A

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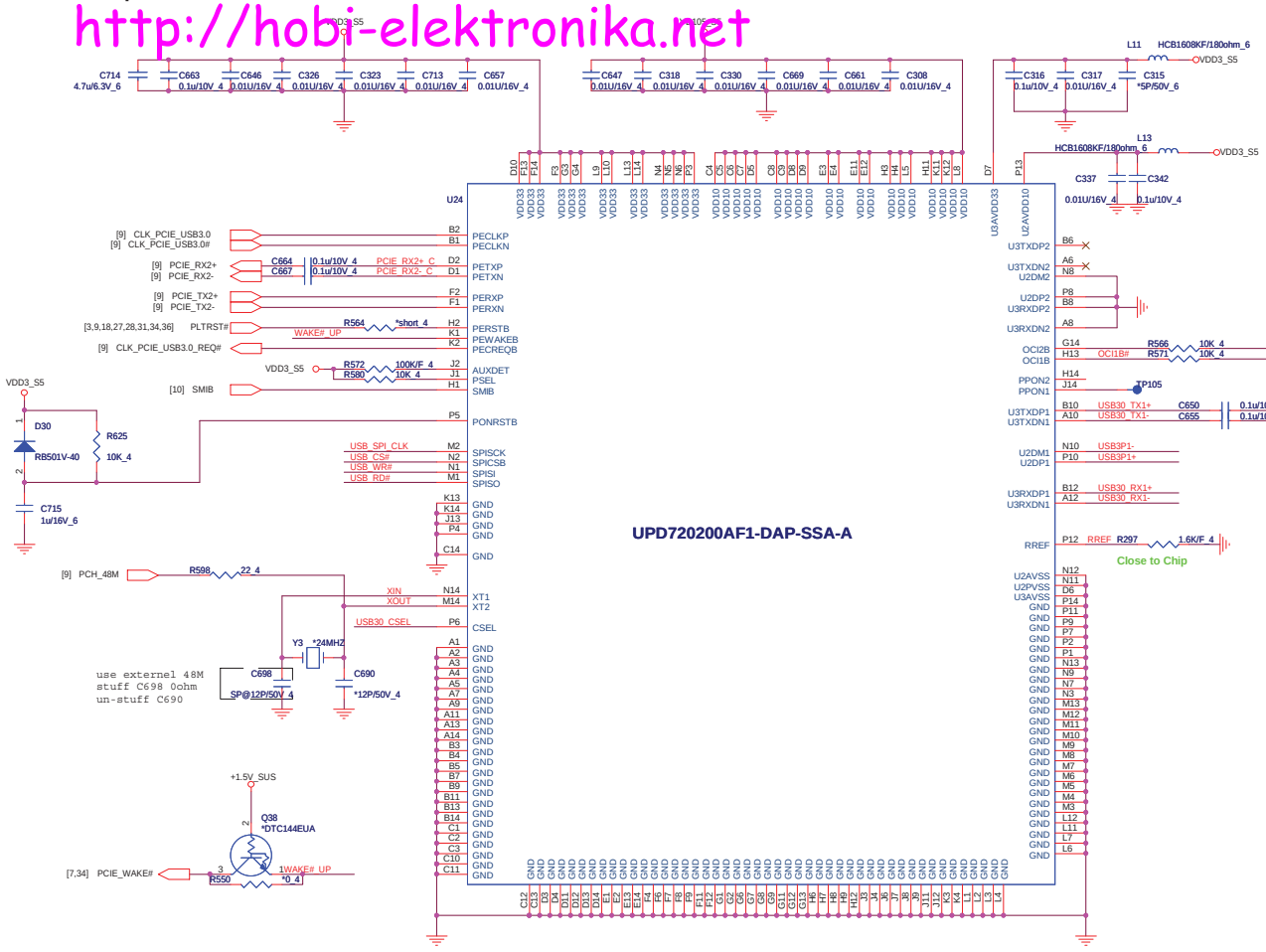
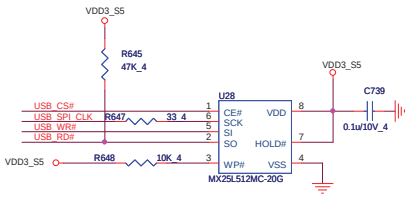
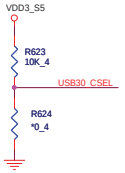
USB3.0 Chip



USB3.0 ROM



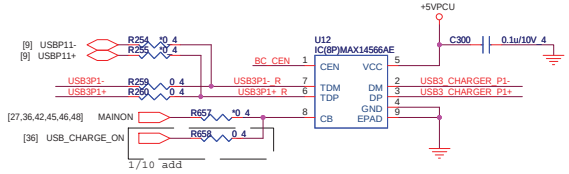


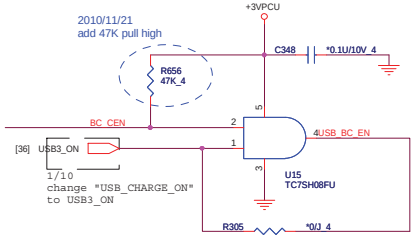
Clock select signal	
USB3.0_CSEL	High = External 48Mhz Low = 24MHz X'tal

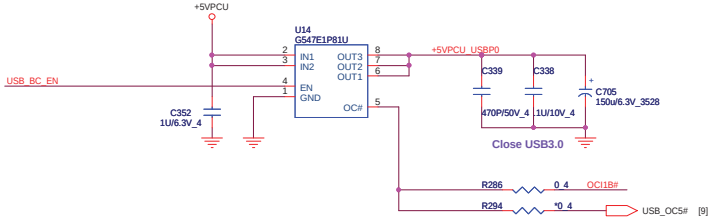
Name	USB data	State	Max Current	Apple Device
SDP	YES	S0~S3	500mA	500mA
CDP	YES	S0~S3	1500mA	500mA
DCP,Auto	NO	S4~S5	1800mA	1800mA

USB charger

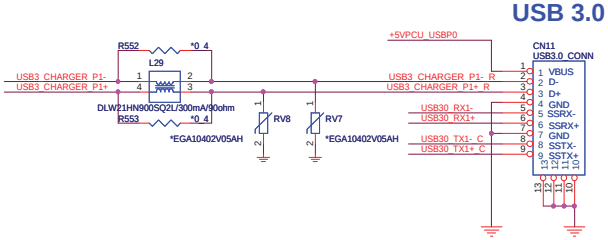
Battery Status, EC GPO control it.
> Hi: S0 and S3~S5 Battery over 30%
> Lo: S3~S5/ Battery under 30%





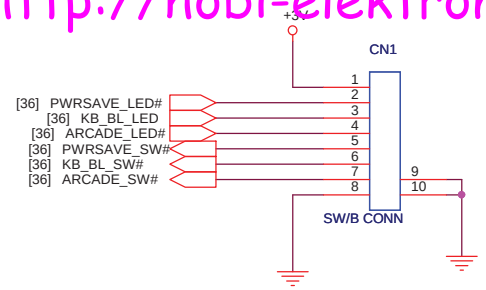


USB3.0 CONN

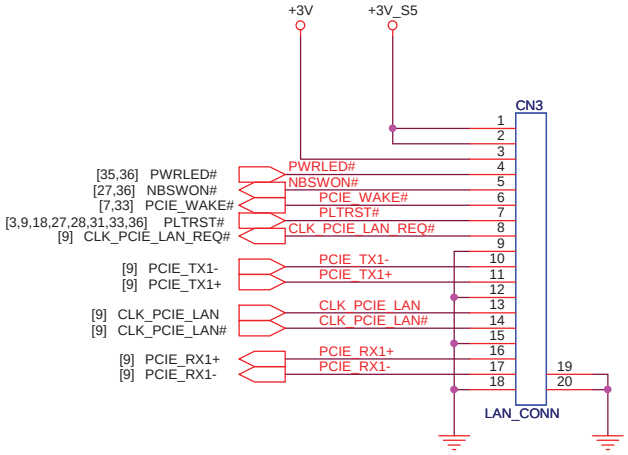


Quanta Computer Inc.			
PROJECT : ZRH			
Size	Document Number		Rev
	USB 3.0		1A
Date: Friday, January 14, 2011		Sheet 33 of 50	

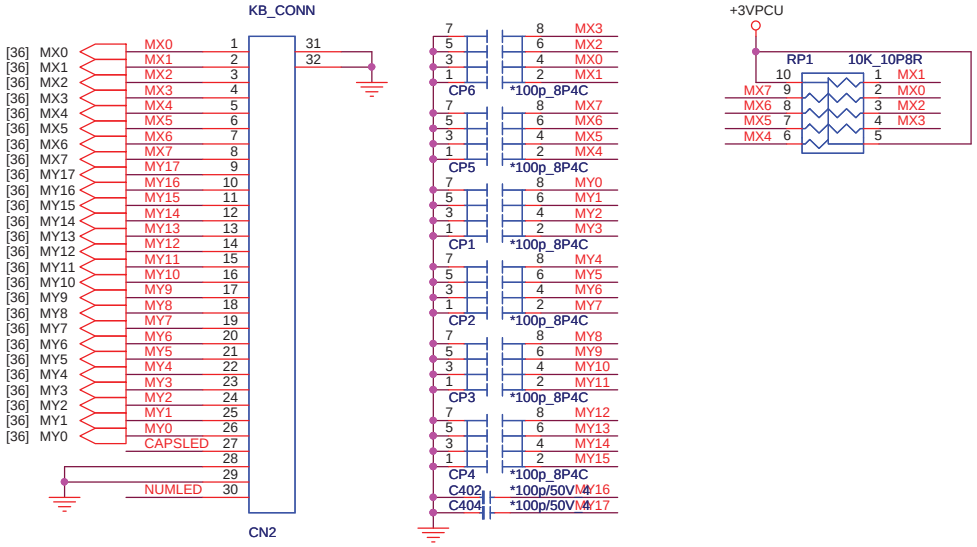
SW BOARD



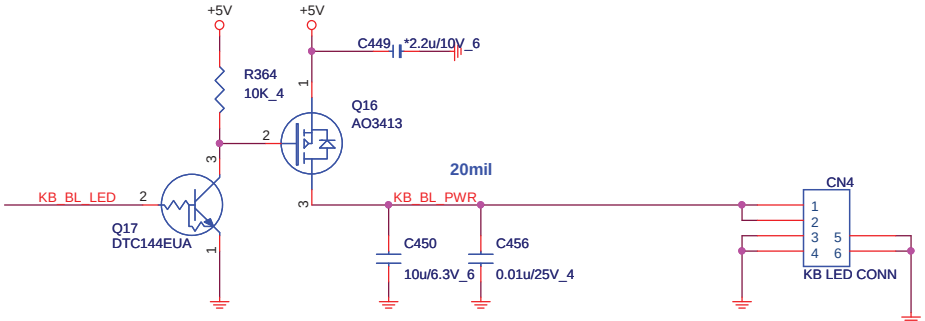
LAN_PWR/B



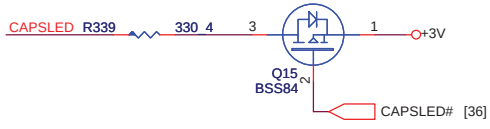
INT K/B



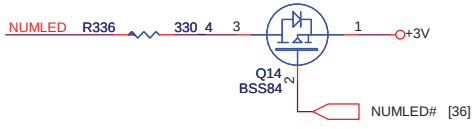
Keyboard LED control



AMBER LED (HKC)

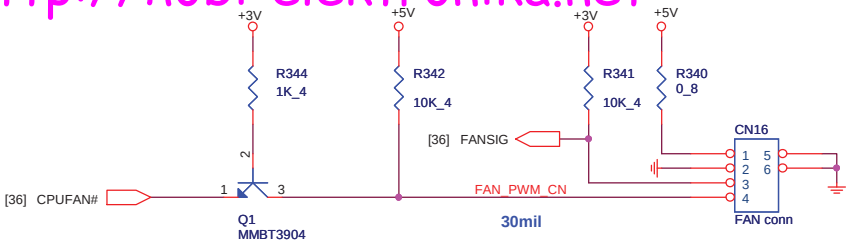


AMBER LED (HKC)

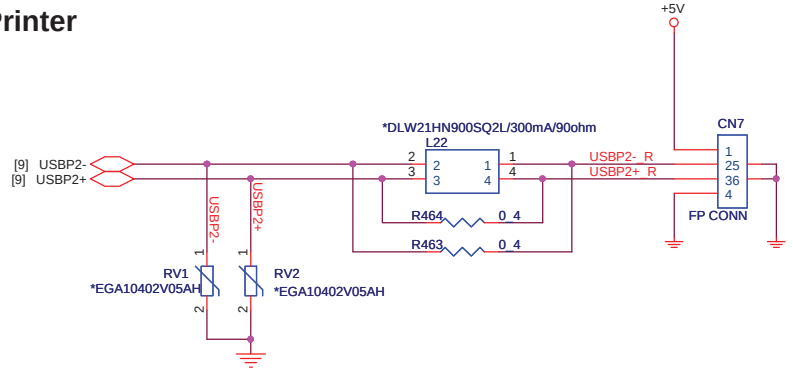


Quanta Computer Inc.		
PROJECT : ZRH		
Size	Document Number: KB/LAN_B/PWR_B	Rev: 1A
Date: Friday, January 14, 2011	Sheet 34 of 50	

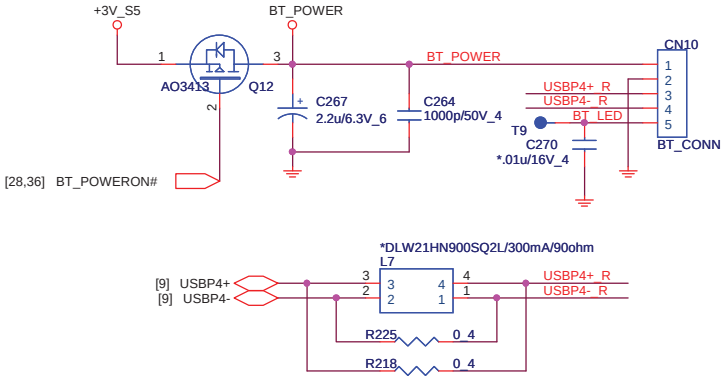
CPU FAN



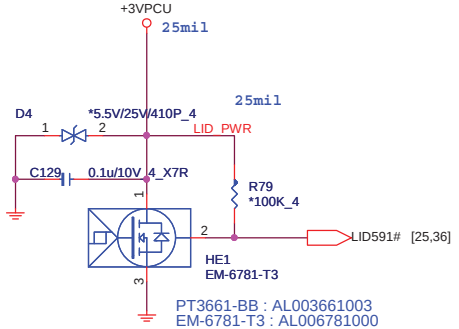
Finger Printer



BT

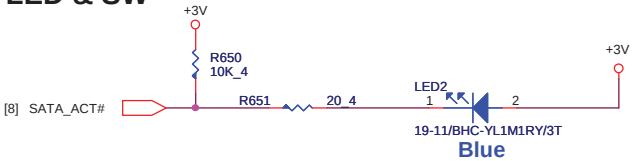


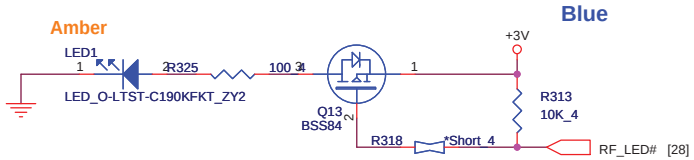
Lid Switch (Hall sensor)

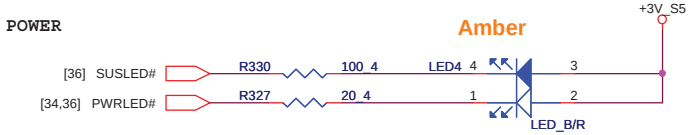


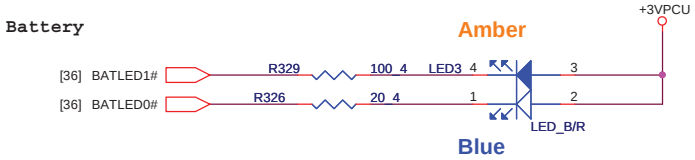
LED & SW

2010/11/21
change LED1,LED2 ,LED3 ,LED4 footprint

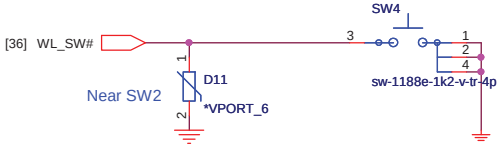








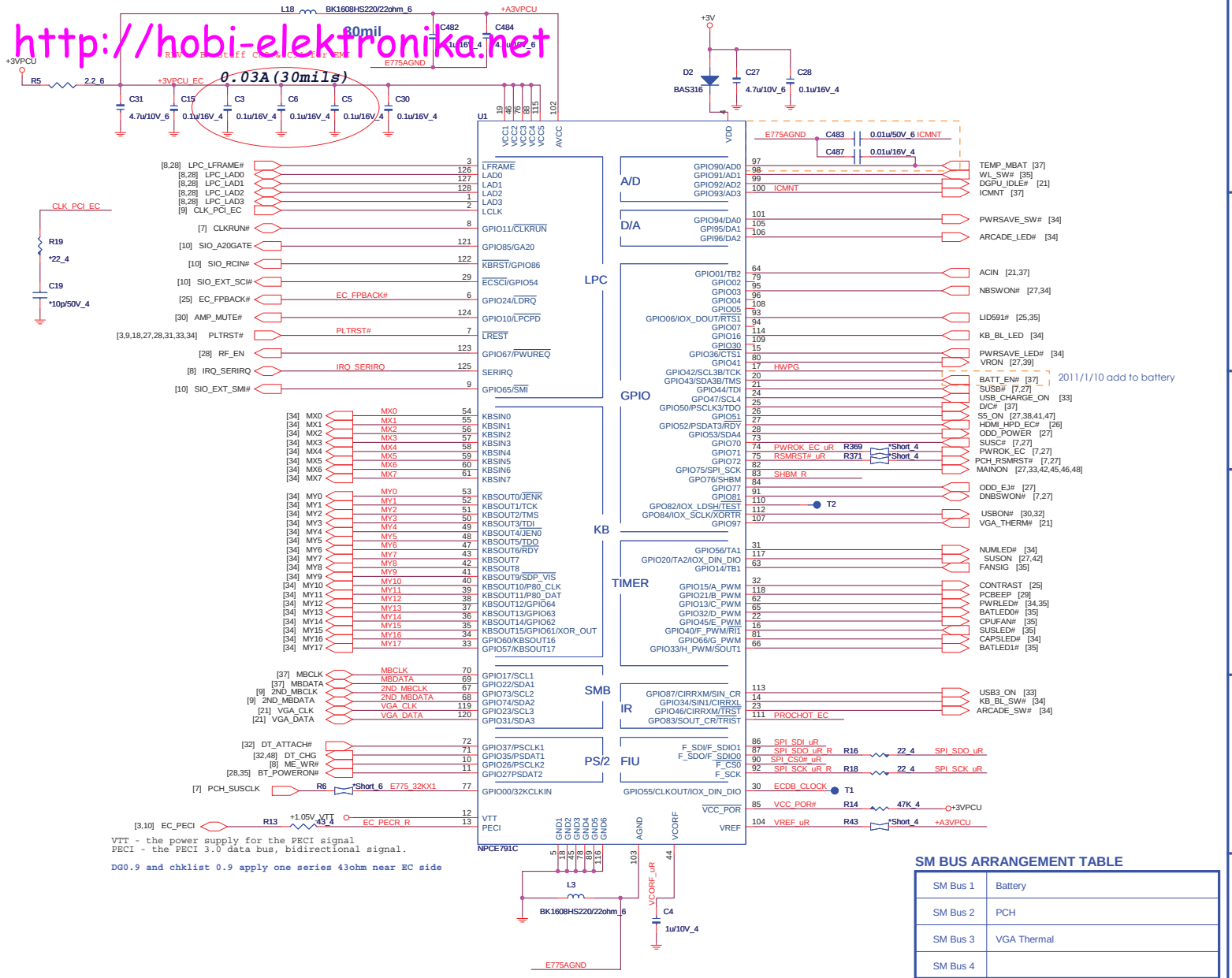
2010/12/3 modify footprint



2010/12/3 modify footprint

Quanta Computer Inc.		
PROJECT : ZRH		
Size	Document Number	Rev
	DT/BT/FP/LED/FAN	1A
Date: Friday, January 14, 2011	Sheet 35 of 50	

EC



VTT - the power supply for the PECI signal
PECI - the PECI 3.0 data bus, bidirectional signal.

DG0.9 and chklist 0.9 apply one series 43ohm near EC side

2011/1/10 add to battery

SM BUS ARRANGEMENT TABLE

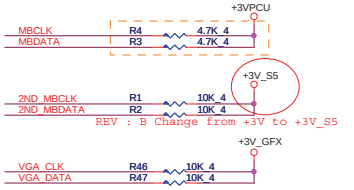
SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	VGA Thermal
SM Bus 4	

I/O ADDRESS SETTING

	I/O Address	
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

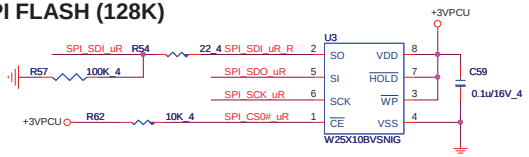
SHBM=0: Enable shared memory with host BIOS

SM BUS PU

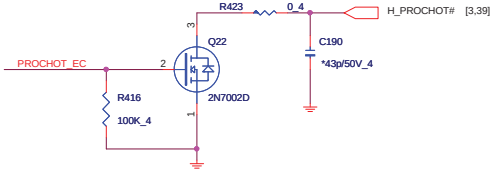


INTERNAL KEYBOARD STRIP SET

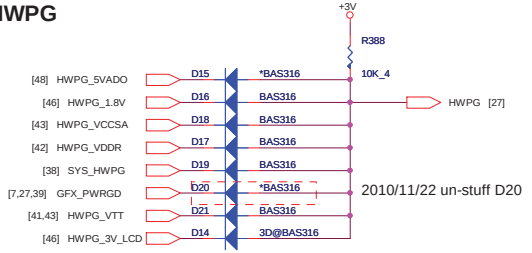
SPI FLASH (128K)



Winbond	W25X10BVSNIG	AKE35FN0N00
EON	EN25F10-100GIP	AKE35FN0Q00
AMIC	A25L010O-F	AKE35ZN0800

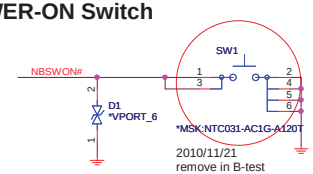


HWPG



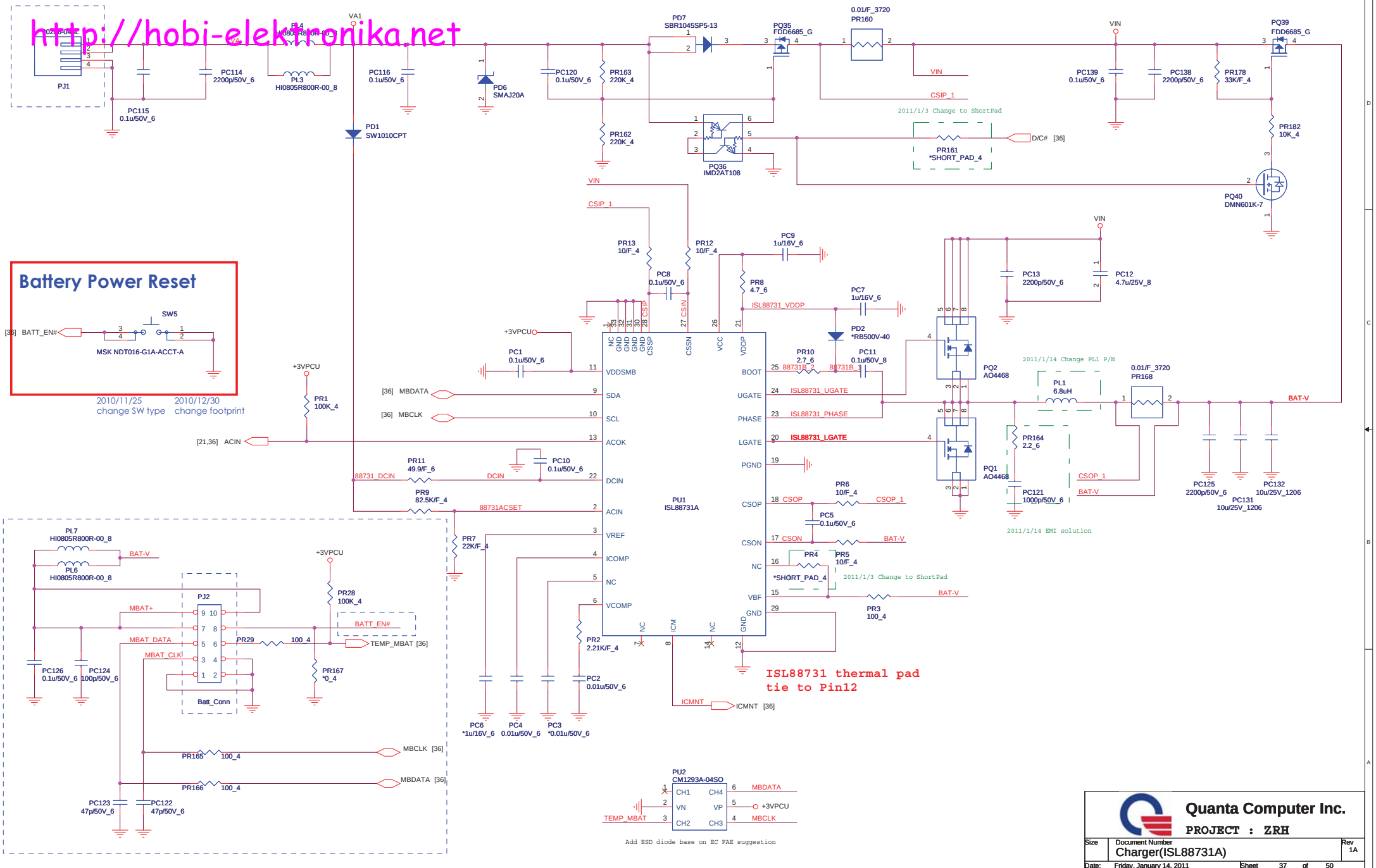
2010/11/22 un-stuff D20

POWER-ON Switch



2010/11/21
remove in B-test

Quanta Computer Inc.			
PROJECT : ZRH			
Size	Document Number		Rev
	WPCE775C_0DG & FLASH		1A
Date: Friday, January 14, 2011		Sheet 36 of 50	



MAIND → MAIND [41,42,43]

SYS_SHDN# → SYS_SHDN# [3,47]

Ven=7.23V

[36] SYS_HWPG

2010/12/2 Remove JP12,TP97,TP94

2010/12/2 Remove JP17,TP102,TP101

2010/12/2 Remove JP11,TP95,TP96

2010/12/2 Remove JP18,TP103,TP99

2011/1/3 Change to ShortPad

2011/1/14 Change PL16 P/N

2011/1/14 EMI solution

2010/12/2 Change to ShortPad

+5VPCU
5 Volt +/- 5%
TDC : 8.9A
PEAK : 11A
OCP : 12A
Width : 360mil

+3VPCU
3.3 Volt +/- 5%
TDC : 5.23A
PEAK : 7A
OCP : 8A
Width : 220mil

PU6 RT8223M

PQ66 AOL1448
PQ68 AOL1718
PQ73 AO4468
PQ71 AO4710

OCP:12A
L(ripple current)
=(9-5)*5/(2.2u*0.4M*9)
=2.525A
Iocp=12-(2.525/2)=10.74A
Vth=10.74A*4.3mOhm=46.17mV
R(Ilim)=(46.17mV*10)/10uA
~46.17K

OCP:8A
L(ripple current)
=(9-3.3)*3.3/(2.2u*0.5M*9)
~1.9A
Iocp=8-(1.9/2)=7.05A
Vth=7.05A*14.2mOhm=100.11mV
R(Ilim)=(100.11mV*10)/10uA
=100.11K

PD4 CHN217
PD3 CHN217

27,36,41,47 S5_ON

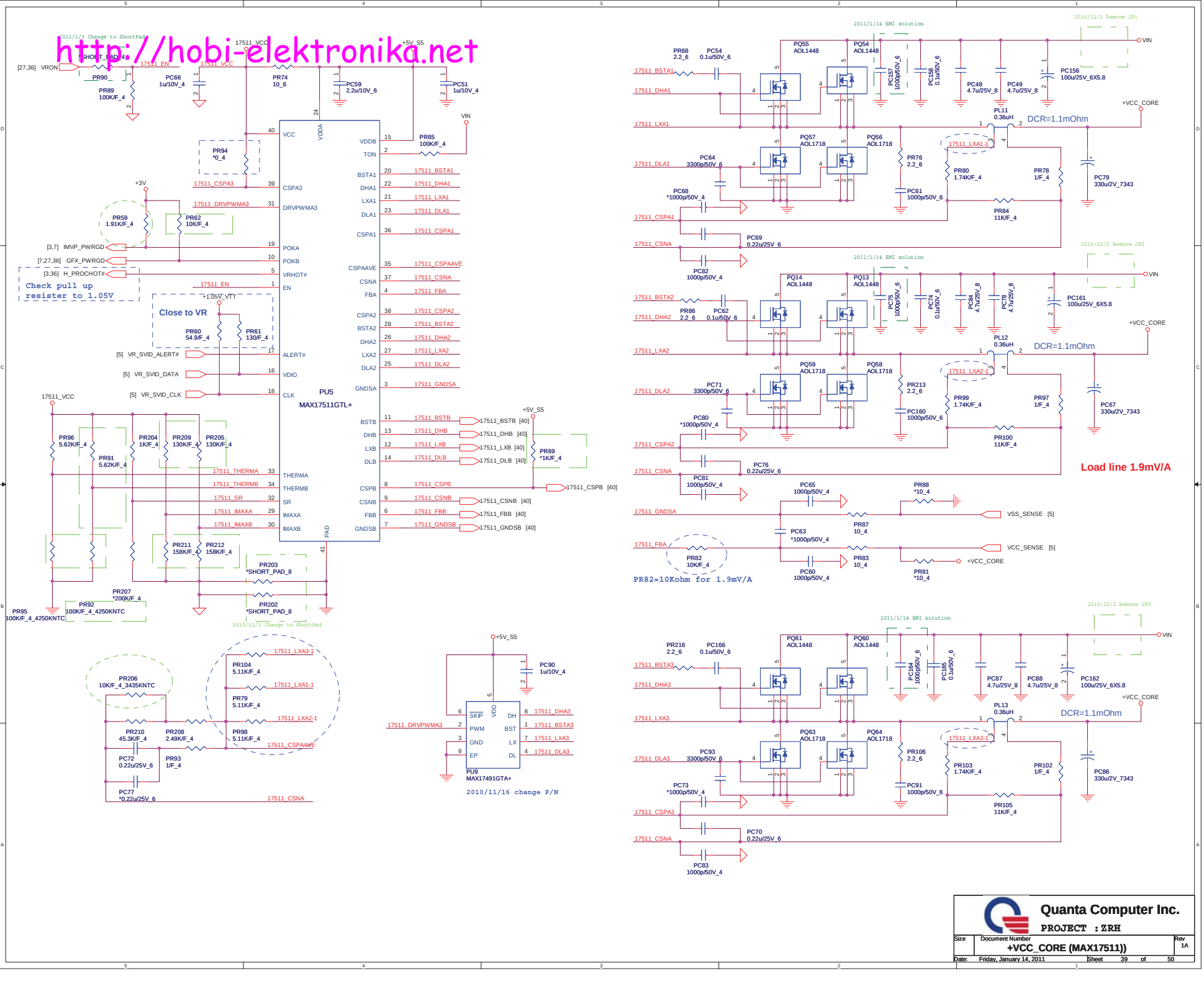
PQ30 DTC144EUA
PQ76 DMN601K-7
PQ26 DMN601K-7
PQ25 DMN601K-7
PQ67 AO4468
PQ69 AO4468
PQ75 AO4468
PQ74 AO3404

4.5A 180mil
2.17A 90mil
3.85A 160mil
0.33A 10mil

Quanta Computer Inc.
PROJECT : ZRH

Size	Document Number	Rev
	SYSTEM 5V/3V (RT8223M)	1A

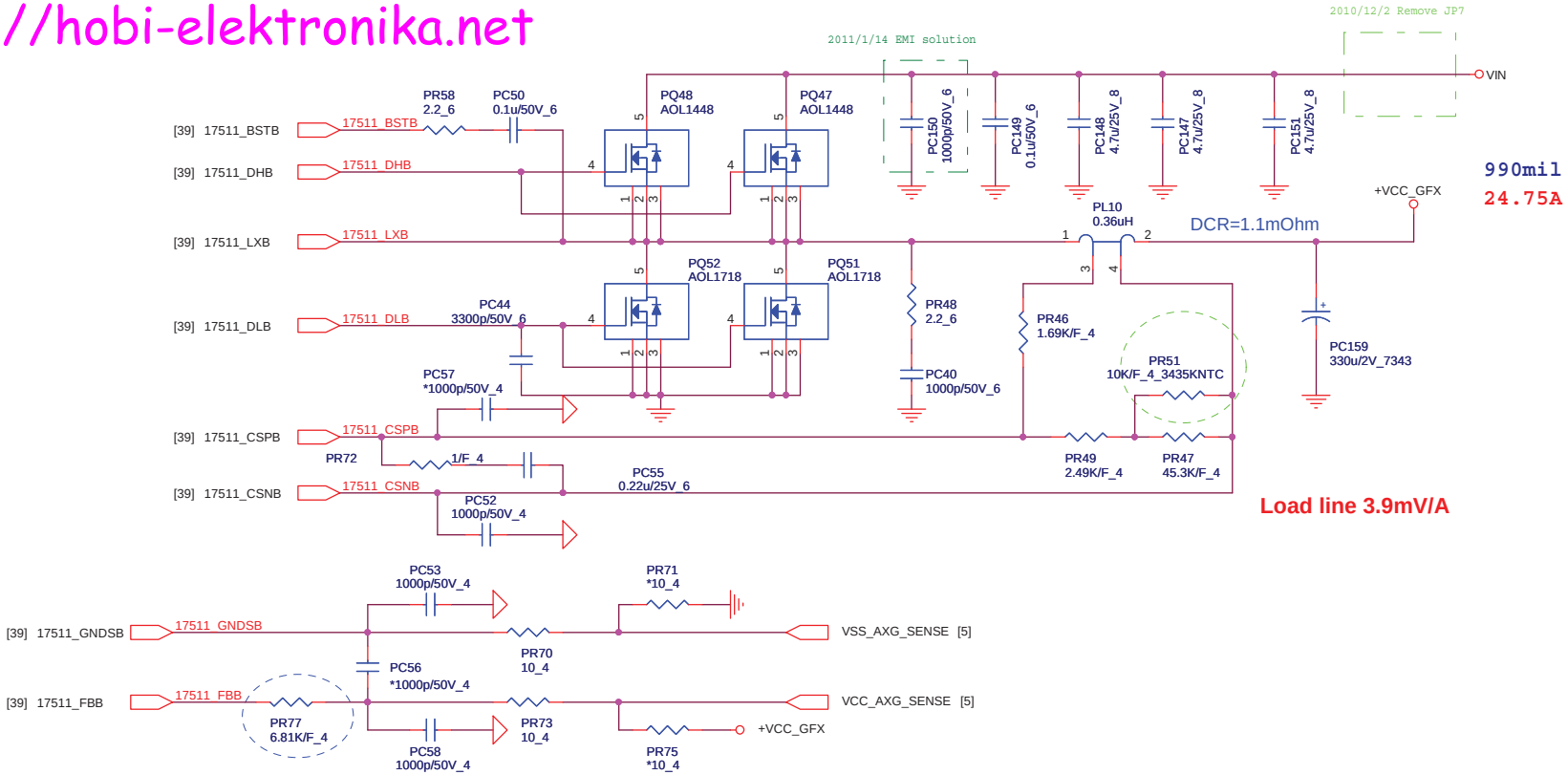
Date: Friday, January 14, 2011 Sheet 38 of 50



Quanta Computer Inc.

PROJECT : ZRH

Size	Document Number	Rev
	+VCC_CORE (MAX17511))	1A
Date: Friday, January 14, 2011	Sheet 39 of 50	

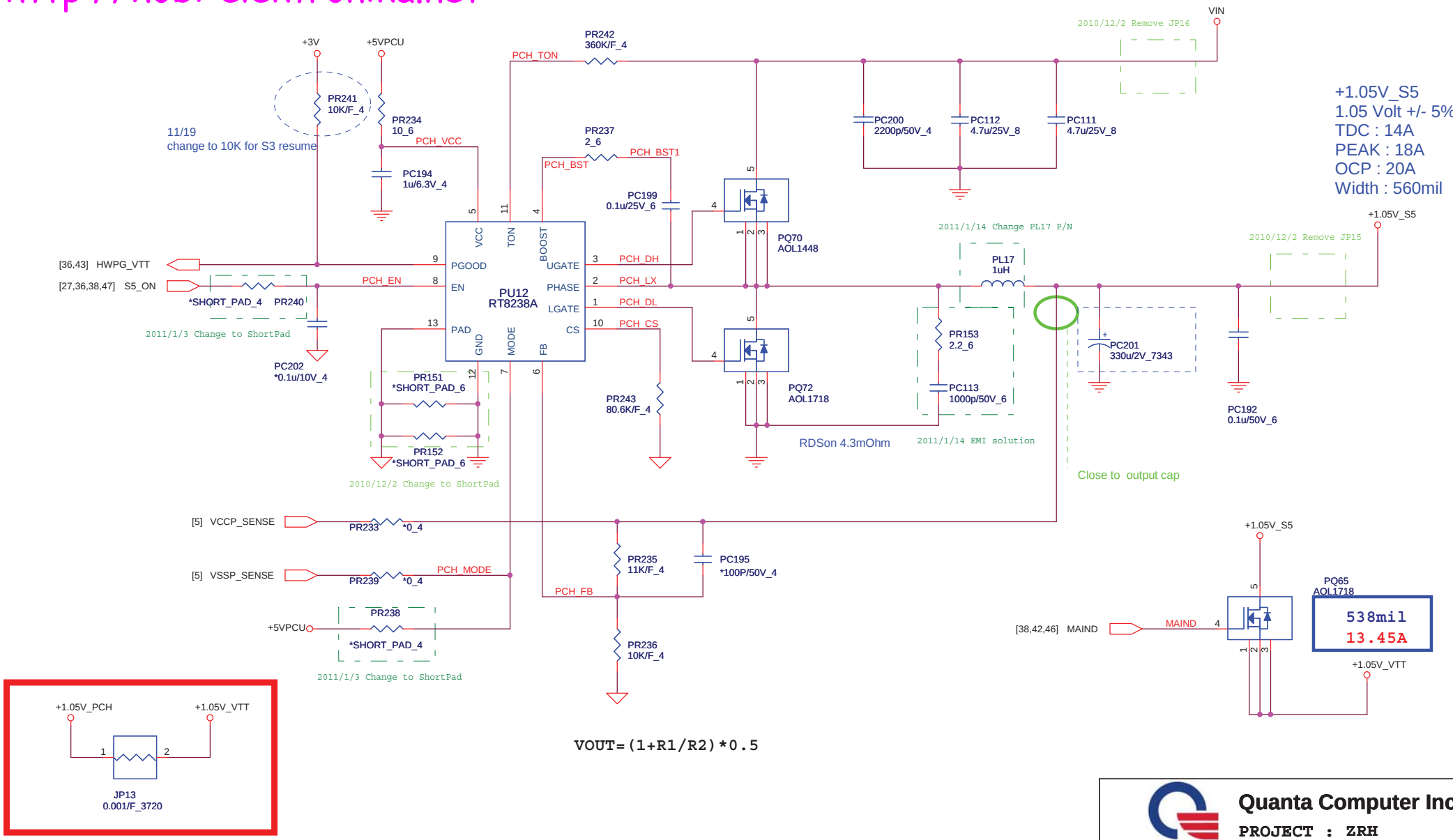


	Dual Core (35W)	Quad Core (45W)
CPU Conver	2-Phase	3-Phase
PR94	Populated	NC
PR209	150K/F_4 (CS41502FB18)	130K/F_4 (CS41302FB00)
PR211	200K/F_4 (CS42002FB12)	158K/F_4 (CS41582FB14)
PR104	NC	5.11K/F_4 (CS25112FB15)
PR79	3.4K/F_4 (CS23402FB08)	5.11K/F_4 (CS25112FB15)
PR98	3.4K/F_4 (CS23402FB08)	5.11K/F_4 (CS25112FB15)

	UMA (IV@) / Muxless (MS@)	External VGA (EV@)
PR69	NC	Populated
PR85	100K/F_4 (CS41002FB28)	200K/F_4 (CS42002FB12)
PR205	130K/F_4 (CS41302FB00)	NC
PR212	158K/F_4 (CS41582FB14)	NC
PR91	5.62K/F_4 (CS25622FB18)	1K/F_4 (CS21002FB24)
PR92	Populated	NC
PR62	Populated	NC

Quanta Computer Inc.
PROJECT : ZRH

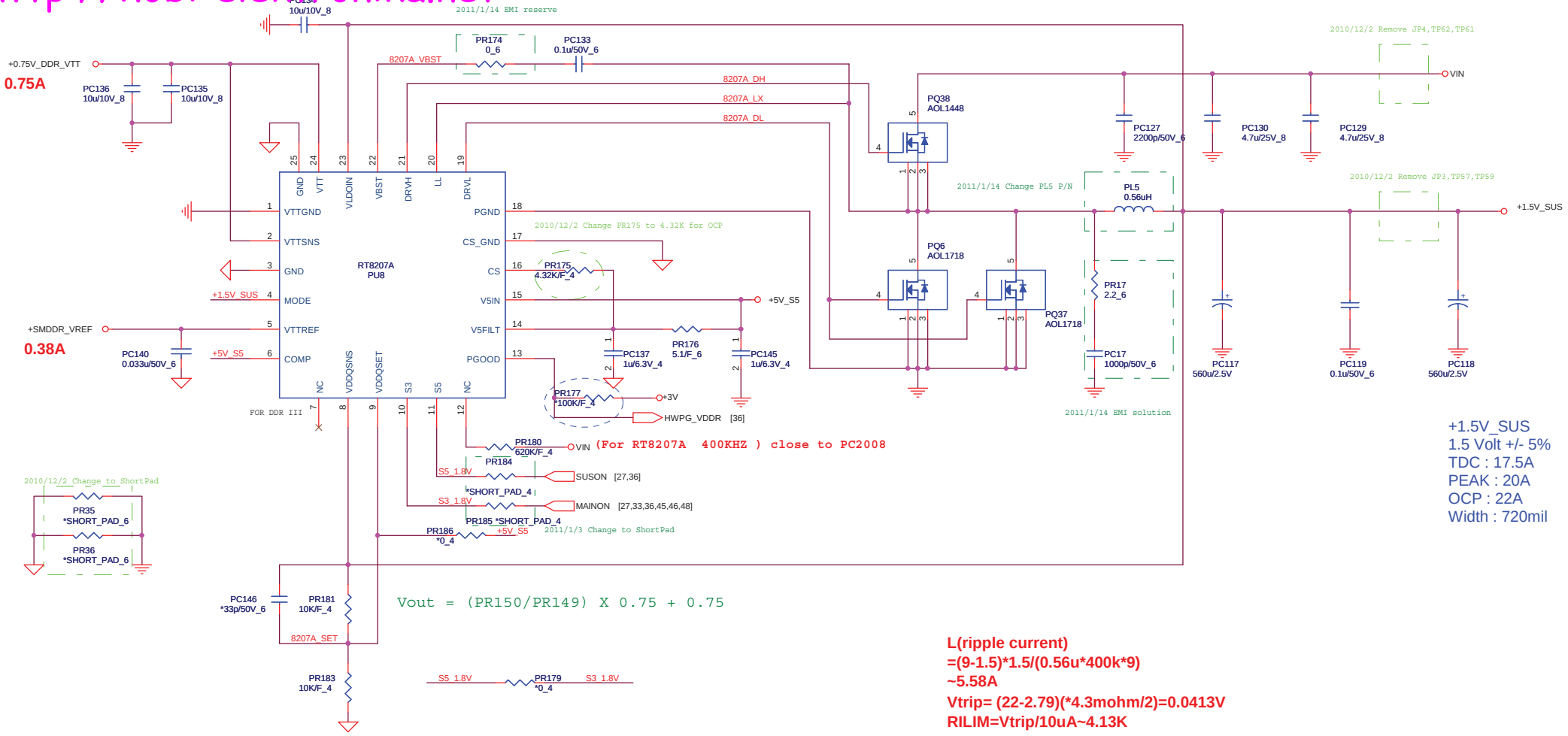
Size	Document Number	Rev
	+VCC_GFX (MAX17511))	1A
Date: Friday, January 14, 2011	Sheet 40 of 50	



Quanta Computer Inc.		
PROJECT : ZRH		
Size	Document Number: +PCH&VTT (RT8238A)	Rev: 1A
Date: Friday, January 14, 2011	Sheet 41 of 50	

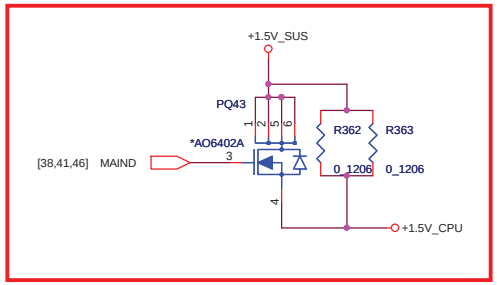
[PWM]

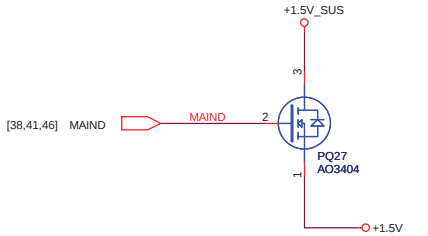
http://hobi-elektronika.net



+1.5V_SUS
1.5 Volt +/- 5%
TDC : 17.5A
PEAK : 20A
OCP : 22A
Width : 720mil

L(ripple current)
=(9-1.5)*1.5/(0.56u*400k*9)
~5.58A
Vtrip= (22-2.79)(*4.3mohm/2)=0.0413V
RILIM=Vtrip/10uA~4.13K





0.38A
20mil

	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

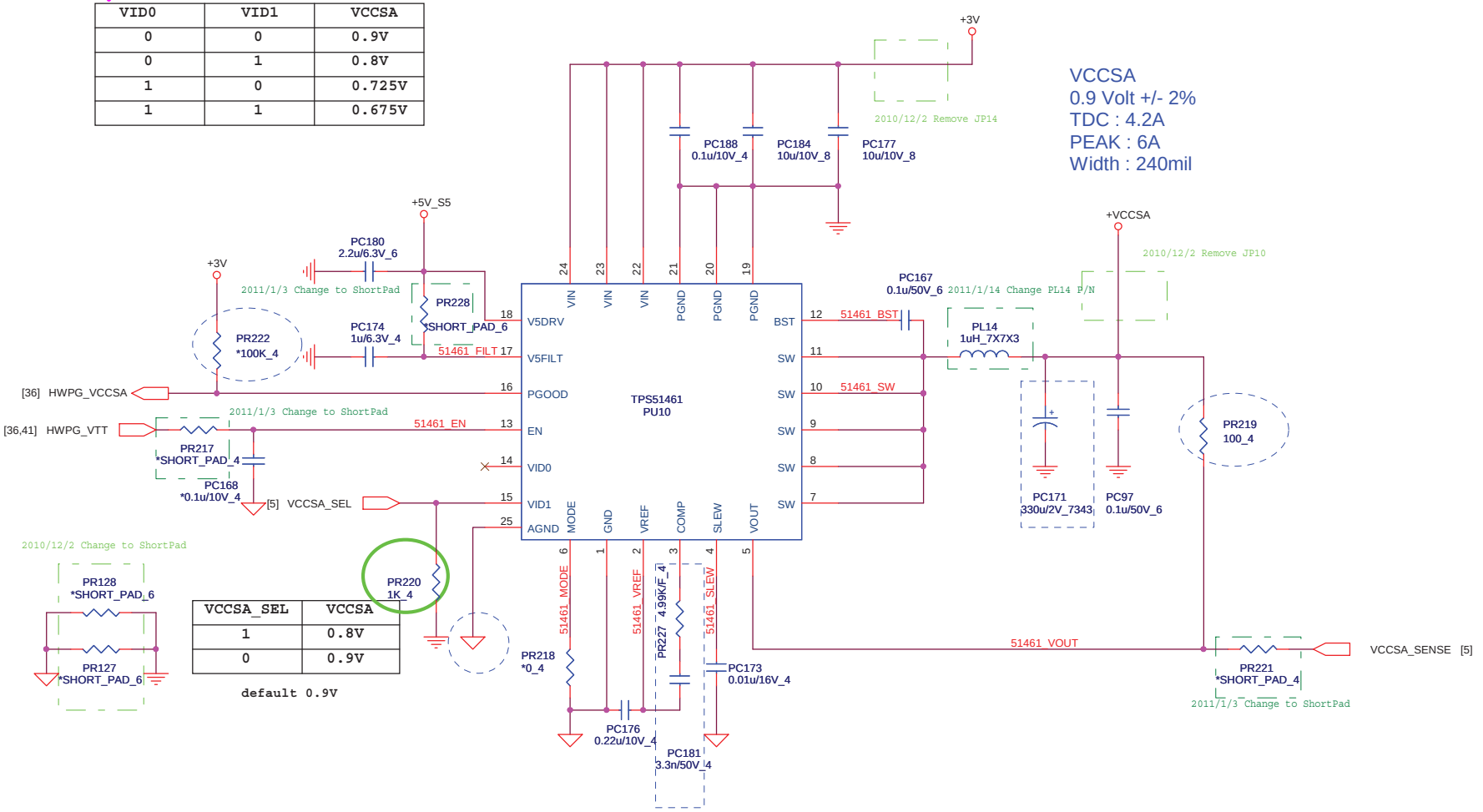
Quanta Computer Inc.
PROJECT : ZRH

Size	Document Number	Rev
	DDR 1.5V(TPS51116)	1A

Date: Friday, January 14, 2011 Sheet 42 of 50

VID0	VID1	VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

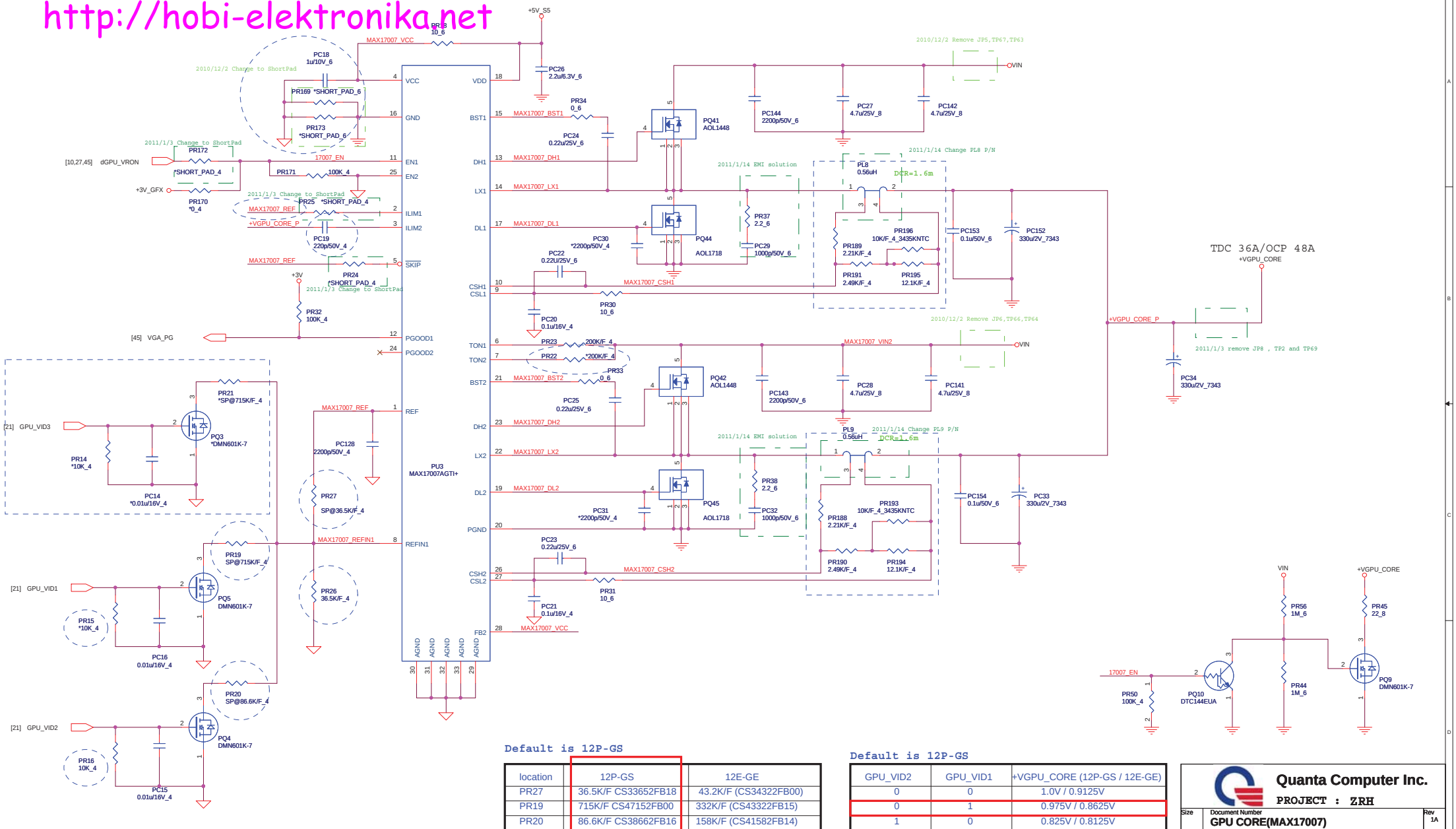
VCCSA
0.9 Volt +/- 2%
TDC : 4.2A
PEAK : 6A
Width : 240mil



VCCSA_SEL	VCCSA
1	0.8V
0	0.9V

default 0.9V

Quanta Computer Inc.		
PROJECT : ZRH		
Size	Document Number: VCCSA(TPS51461)	Rev 1A
Date: Friday, January 14, 2011	Sheet 43 of 50	



Default is 12P-GS

location	12P-GS	12E-GE
PR27	36.5K/F CS33652FB18	43.2K/F (CS34322FB00)
PR19	715K/F CS47152FB00	332K/F (CS43322FB15)
PR20	86.6K/F CS38662FB16	158K/F (CS41582FB14)

Default is 12P-GS

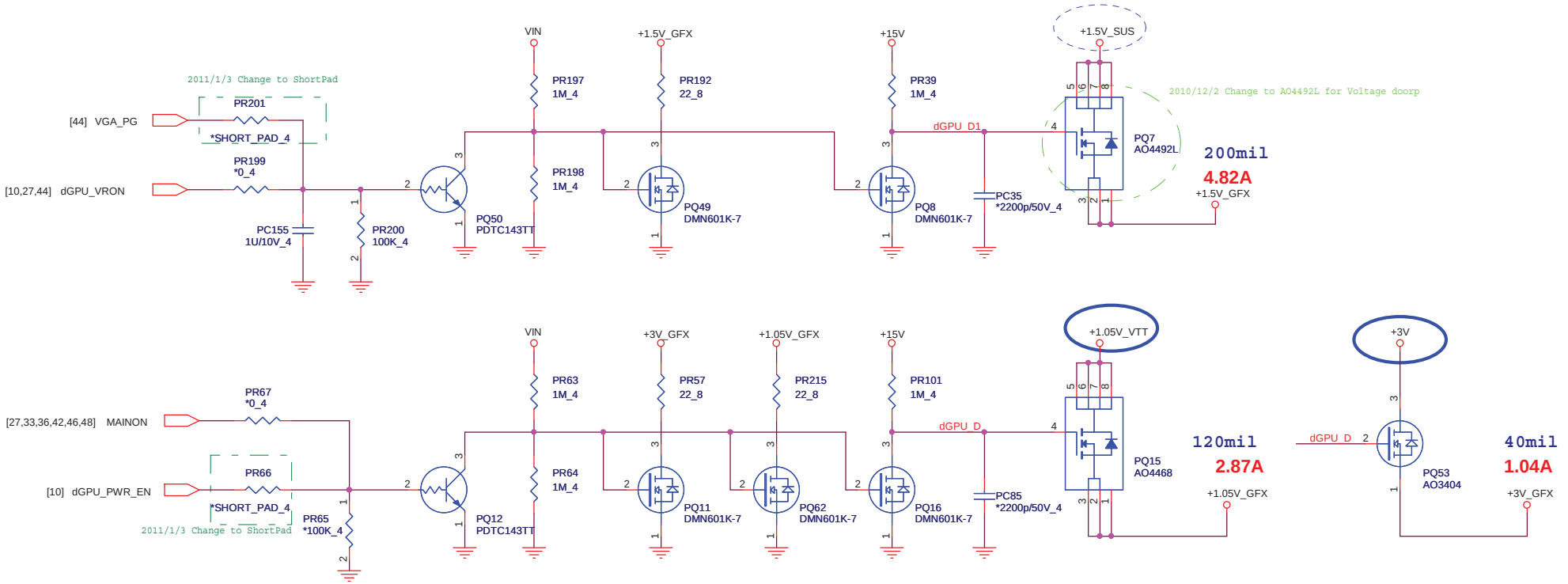
GPU_VID2	GPU_VID1	+VGPU_CORE (12P-GS / 12E-GE)
0	0	1.0V / 0.9125V
0	1	0.975V / 0.8625V
1	0	0.825V / 0.8125V

Quanta Computer Inc.

PROJECT : ZRH

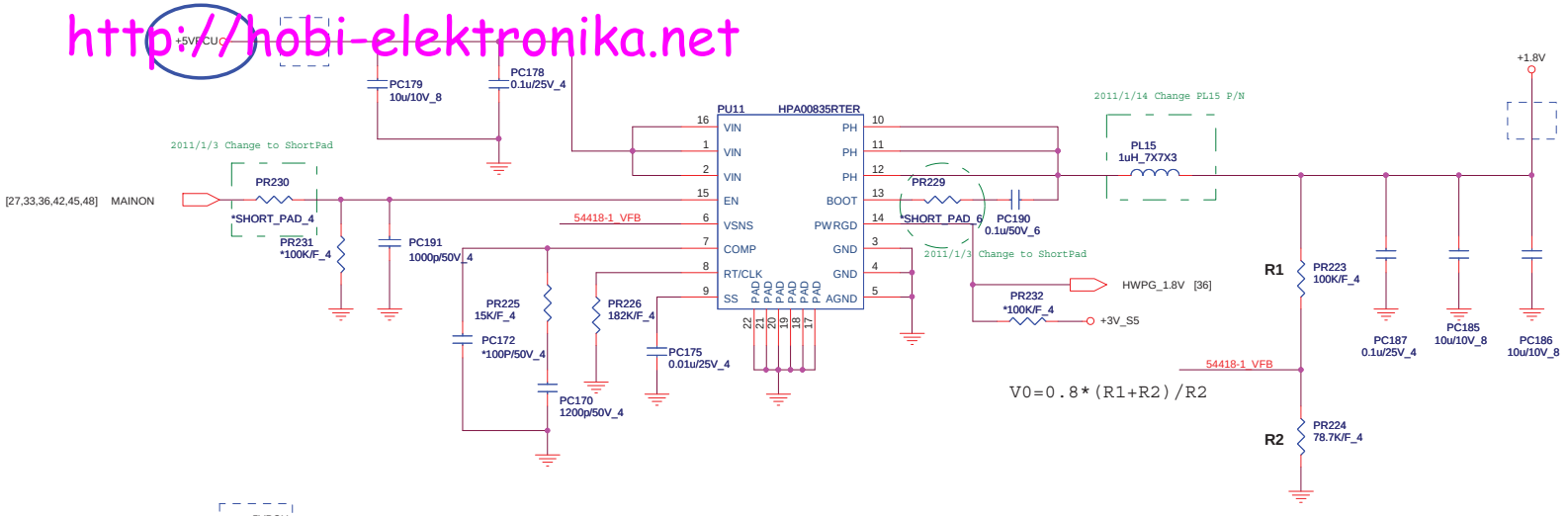
Size	Document Number	Rev
	GPU CORE(MAX17007)	1A

Date: Friday, January 14, 2011 Sheet 44 of 50

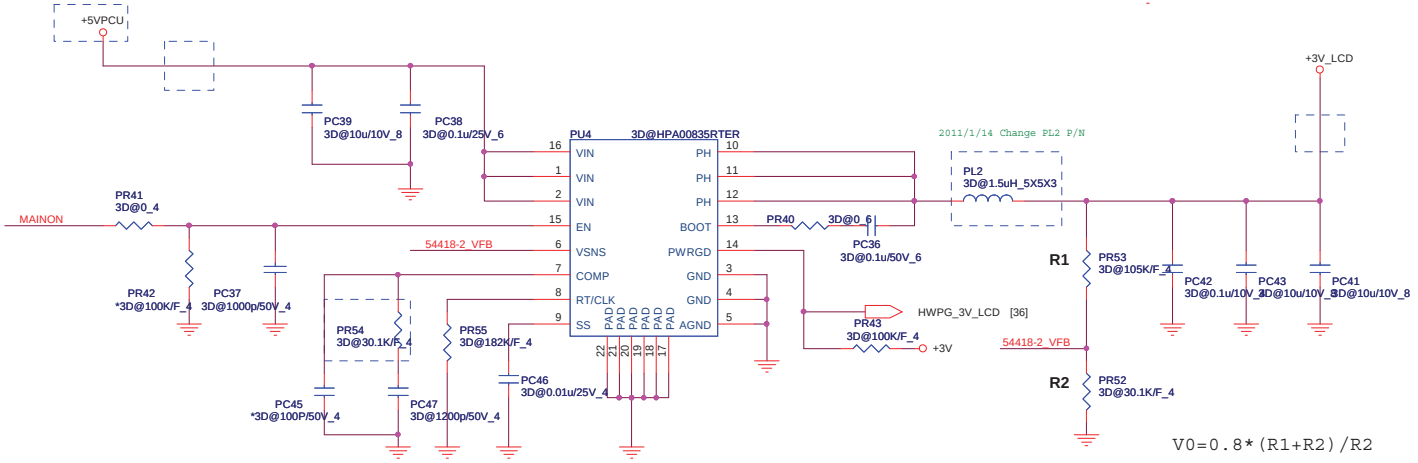


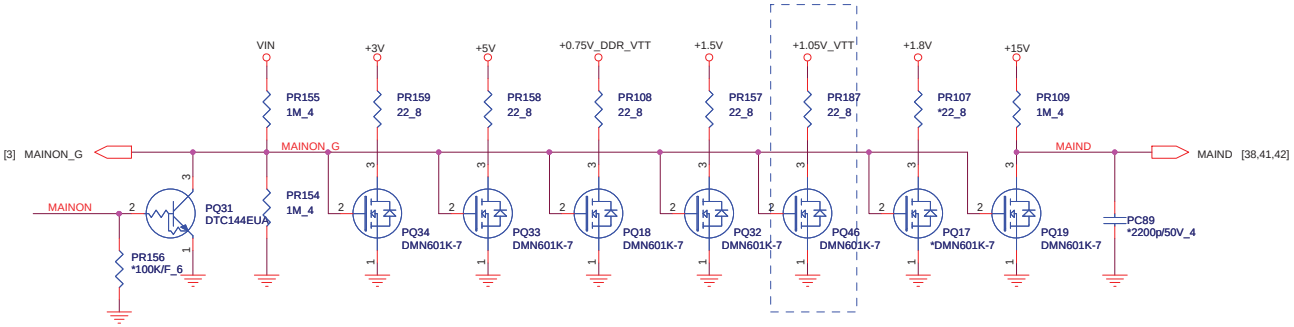
Quanta Computer Inc.		
PROJECT : ZRH		
Size	Document Number: GPU_PWR	Rev: 1A
Date: Friday, January 14, 2011	Sheet 45 of 50	

+1.8V
1.8 Volt +/- 5%
TDC : 1.54A
PEAK : 2A
Width : 60mil



+3V_LCD
3.6 Volt +/- 5%
TDC : 1.5A
PEAK : 2A
Width : 60mil

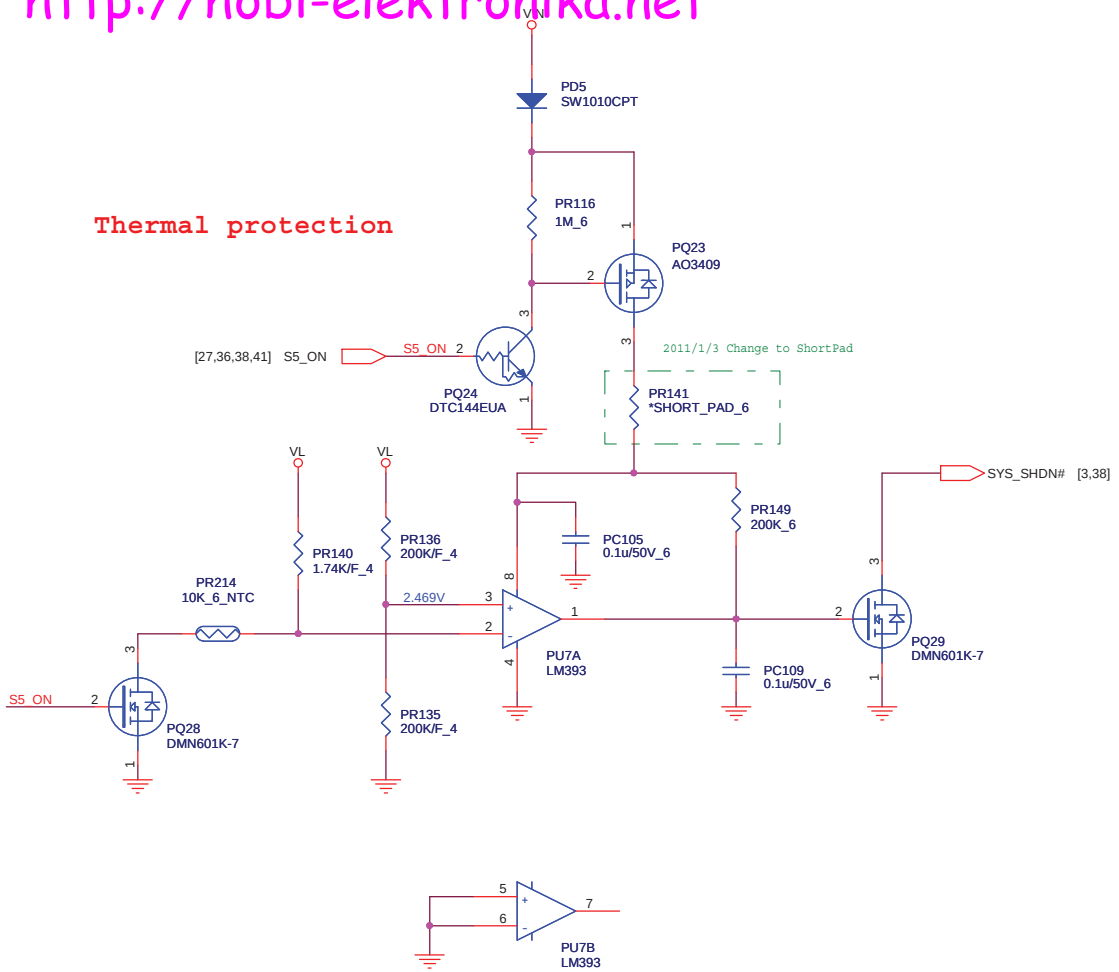




Quanta Computer Inc.
PROJECT : ZRH

Size	Document Number	Rev
	+1V/+1.8V/Discharge	1A
Date: Friday, January 14, 2011	Sheet 46 of 50	

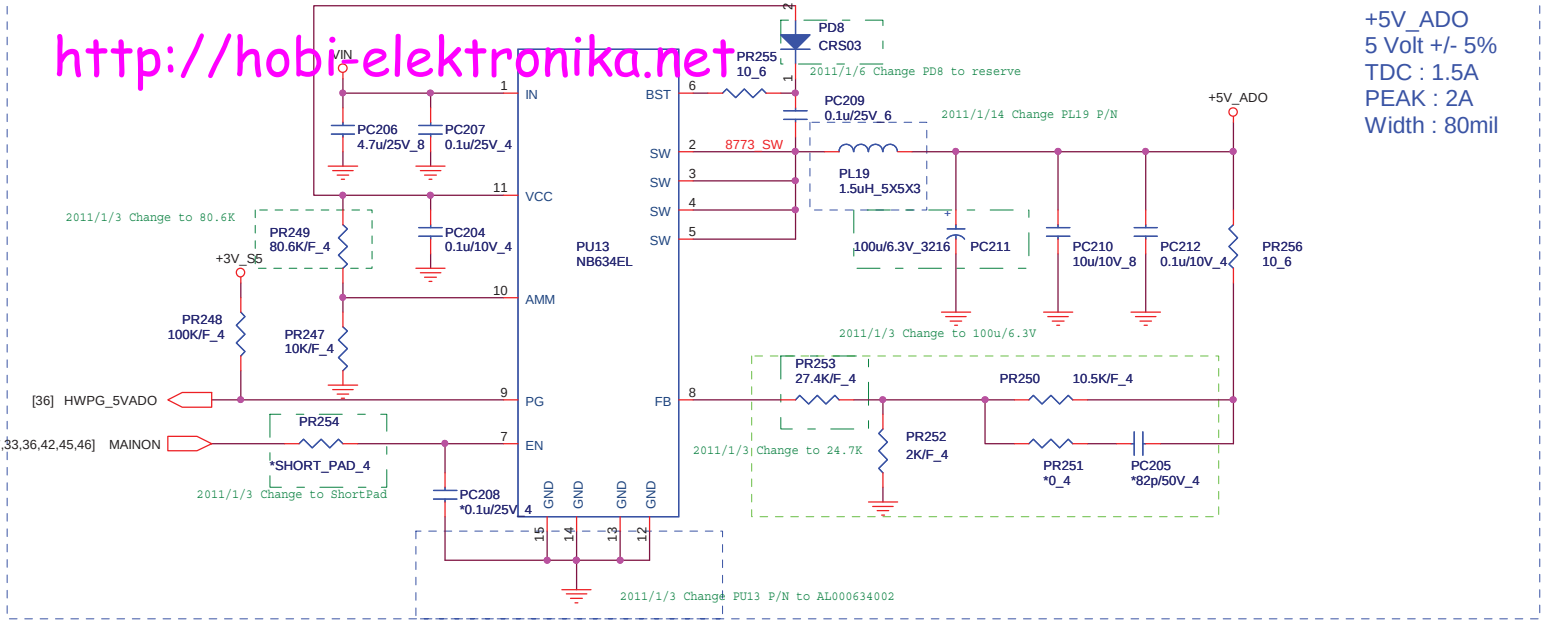
Thermal protection

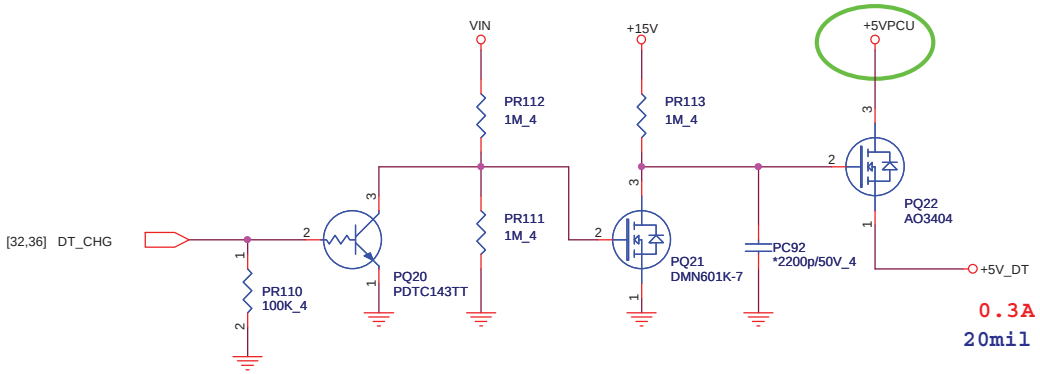


For EC control thermal protection (output 3.3V)

Quanta Computer Inc.		
PROJECT : ZRH		
Size	Document Number: Thermal protect	Rev 1A
Date: Friday, January 14, 2011	Sheet 47 of 50	

+5V_ADO
5 Volt +/- 5%
TDC : 1.5A
PEAK : 2A
Width : 80mil

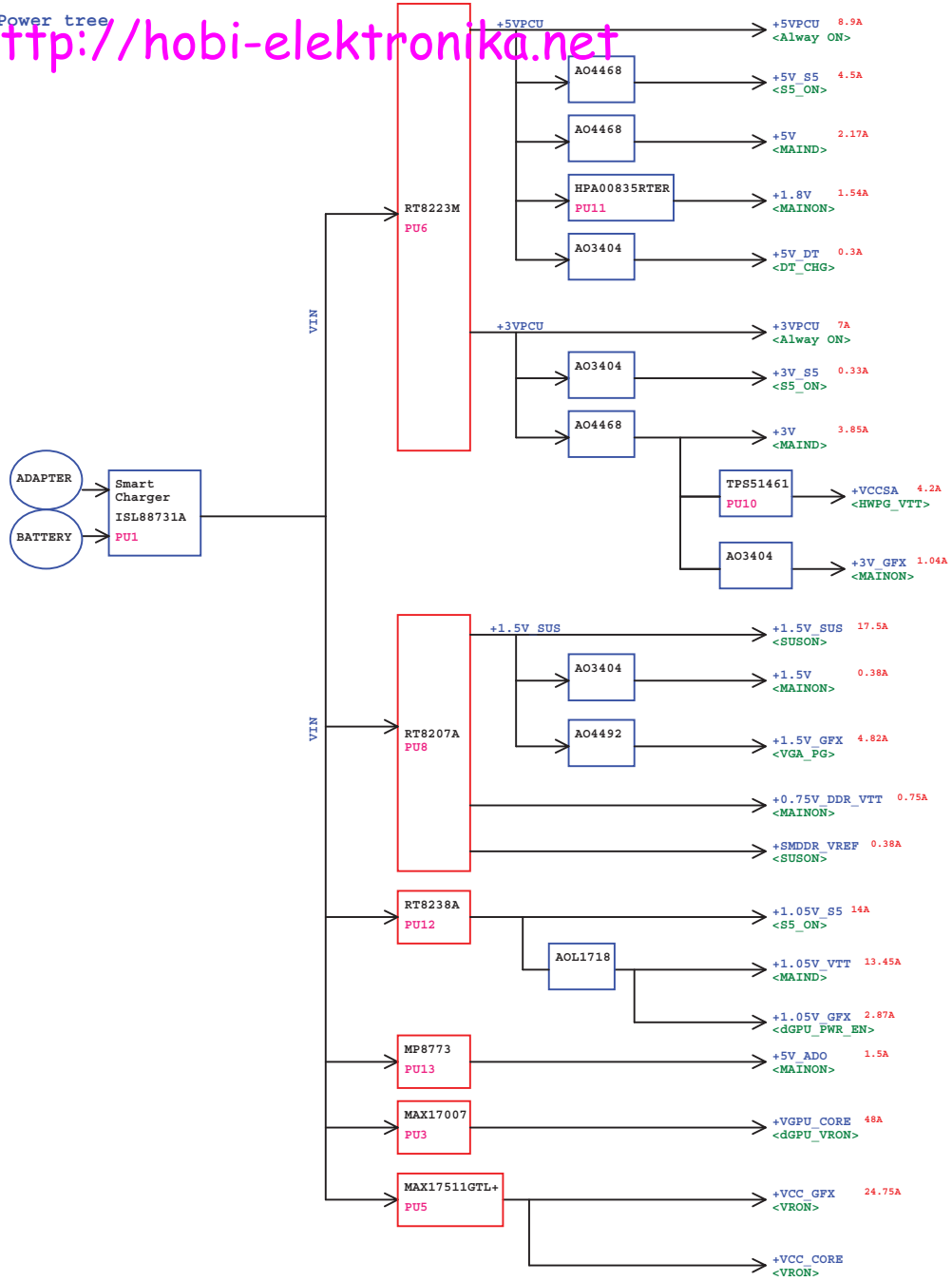




Quanta Computer Inc.
PROJECT : ZRH

Size	Document Number	Rev
	+5V_ADO (MP8773)	1A
Date: Friday, January 14, 2011	Sheet 48 of 50	

ZRH Power tree



PROJECT : ZYB & ZYBA
Quanta Computer Inc.

Size	Document Number	Rev
	ZYA/B Power tree	1A
Date: Friday, January 14, 2011	Sheet 49 of 49	

Model

ZRH MB

CHANGE LIST

REV		
	2010/11/16	page 3 : R692 add for PROC_SELECT need a 2.2 k pull-up VccOPTEMM page 5 : R104,R105 change to 10 Ohm 1% R692 add pull-up to VCC_CORE R693 add pull-down to GND page 16 : Q41,R698 add for new EMI issue R40 change from 10K to 22K ohm 1% page 17 : R698 change to 10K ohm 1% resistance page 31 : change L801,L802 ,L803 ,L804 footprint page 33 : R4656 47K add to pull high charger DC_IN_CHK to +3VPCU page 7 : U4 change P/N & footprint page 32 : CN8 short pin1 & pin4 page 34 : SW1 remove to N-test page 25 : CN37 change P/N
	2010/11/25	page 37 : SW5 change type (P/N,footprint) page 11 : C747 add 120 OHM for fix monitor issue page 20 : C686,C685 change to 27P page 31 : C734,C737 change to 27P page 25 : C671 modify pull high to +3V page 32 : CN8 modify footprint
	2010/11/30	page 7 : U10 add for power sequence page 18 : U2 modify pull high to +3V_SPI page 30 : CN12 SWAP pin define page 32 : U13 must down R6687A re-driver ,should 0 ohm
	2010/12/2	page 23 : R682,R683 change to 1K2 ohm page 24 : R85,R92 change to 1K2 ohm page 37 : Change R71 PN to SMR0368B115 page 38 : Remove JP37,JP38,JP12,JP11 Change PR124,PR114 to ShortPad page 39 : Remove JP6,JP2,JP9 Change PR203,PR202 to ShortPad page 40 : Remove JP7 page 41 : Remove JP16,JP15 Change PR191,PR192 to ShortPad page 42 : Remove JP4,JP3 Change PR19,PR20 to ShortPad Change PR175 to 6.32K/F_4 page 43 : Remove JP14,JP12 Change PR128,PR127 to ShortPad page 44 : Remove JP8,JP9 Change PR169,PR173 to ShortPad page 45 : Change PQ7 to AO4932, PN:SA0A932G000 page 30 : R316,R320 change to 0 ohm
	2010/12/3	page 30 : LED1,LED4 modify footprint page 35 : SW4 modify footprint page 25 : CN5 change footprint
	2010/12/4	page 30 : CN12 pin7,8 change to +5VPCU pin 20 change to GND page 32 : add U11,C759 ,dac 2kΩ,OR,R697 to MUTE_SPK page 29 : add L26 for EMI page 32 : CN8 pin5,6 to dummy
	2010/12/22	page 32 : CN5 modify footprint page 35 : R598 0 ohm remove
	2010/12/27	page 29 : CN22,CN25 modify footprint to standard type. page 32 : R132,R130,R147,R148 connect to PCH.
C	2010/12/28	page : Change to short pad R229,R434,R64,R109,R110,R108,R298,R63,R42,R96,R89 page : Remove 0 ohm R662,R637,R631,R638,R639,R200,R281,R637,R697,R658,R605,R604,R290,R291,R288,R289,R292,R290, R147,R368,R363,R358,R359,R331,R361,R351,R365,R374,R375,R242,R660,R659,R898,R315,R314,R301,R689,R15
	2011/1/3	page 37 : SW5 modify footprint page 32 : CN8 modify footprint page 25 : CN5 modify footprint
	2011/1/6	page 32 : C740,R99 add page 32 : CN8 modify footprint page 37 : SW5 modify footprint page 37 : Change PR140,PR4 to ShortPad page 38 : Change PR120,PR122,PR118,PR112,PR130 to ShortPad page 39 : Change PR90 to ShortPad page 41 : Change PR240,PR238 to ShortPad page 42 : Change PR188,PR189,PR174 to ShortPad page 43 : Change PR217,PR223,PR218 to ShortPad page 44 : Change PR24,PR23,PR172 to ShortPad page 45 : Change PR231,PR66 to ShortPad page 46 : Change PR230,PR229 to ShortPad page 47 : Change PR241 to ShortPad page 48 : Change PR256 to ShortPad page 49 : Change PR249 to 80.6K/F,PR250 to 27.4K,PC211 to 1000/6.3V_3216 page 49 : Change PC11 P/N to A2000044402 page 44 : Remove JP8,UP2 and TP49 page 49 : Change PC8 to remove
	2011/1/10	page 36 : add Y1 pin 23 to EAPY_EMB page 33 : add U12 pin8 to USB_CHARGE_ON page 33 : Change U16 pin1 to EC_USB1_ON page 33 : Change U14 pin6 to EC_CHK page 23 : add R11 for EMI page 29 : add EC2,EC3,EC4,EC5,EC6,EC7 for EMI page 33 : add R699 pull high +3VPCU page 42 : change PR174 to 22ohm 0603 page 35 : change R127,R651 to 2Kohm ,R229 to 150ohm ,R330 to 100ohm page 15 : add U12 LDO circuit fix monitor issue
	2011/1/12	page 32 : add U13,U14,U39,Q42 for ST dongle shut down issue page 32 : remove C216, add R711, change C217 to 22u 0805
	2011/1/13	page 33 : Change U14 pin6 to USB_EC_EN, remove R699 page 32 : Change CN9 footprint (change USB to single way) page 32 : Add R665 pull low 100K from +5V_ST

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