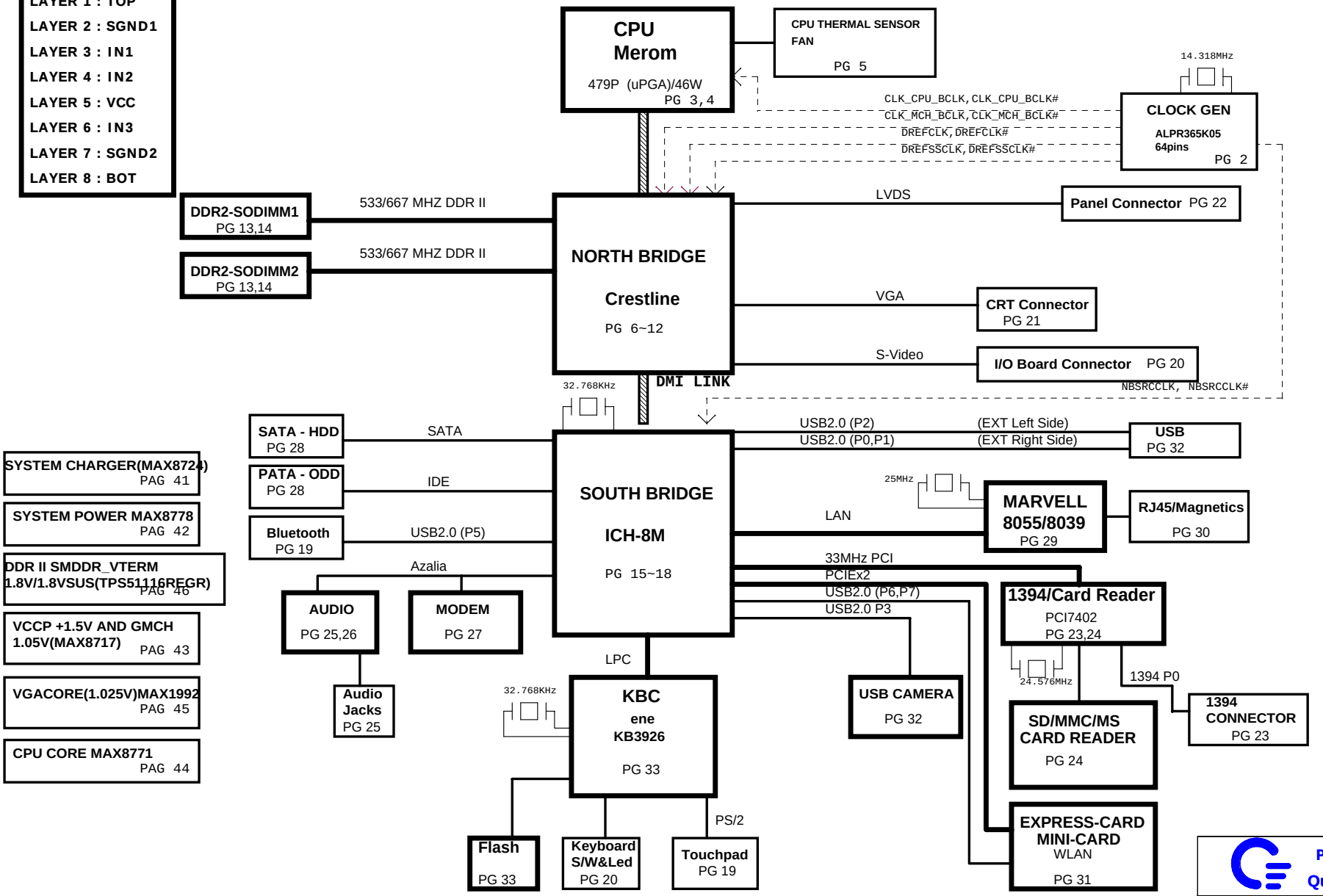
SW7 BLOCK DIAGRAM

01

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND1
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : IN3
- LAYER 7 : SGND2
- LAYER 8 : BOT



PROJECT : SW7

Quanta Computer Inc.

Size	Document Number	Rev
	BLOCK DIAGRAM	1A

Date: Friday, September 28, 2007 Sheet 1 of 44

+3V
L37 BLM21PG600SN1D 120 ohms@100Mhz
C448 4.7uF/6.3V_6
C447 4.7uF/6.3V_6
C483 0.1uF/10V
C482 0.1uF/10V
C451 0.1uF/10V
C466 0.1uF/10V
C485 0.1uF/10V
+CK_VDD_MAIN
L36 BLM21PG600SN1D
VDDCPU
C449 4.7uF/6.3V_6
C450 4.7uF/6.3V_6
C463 0.1uF/10V
L39 BLM21PG600SN1D 120 ohms@100Mhz
C455 4.7uF/6.3V_6
C453 4.7uF/6.3V_6
C245 0.1uF/10V
C486 0.1uF/10V
C484 0.1uF/10V
C464 0.1uF/10V
C465 0.1uF/10V
C467 0.1uF/10V
+CK_VDD_MAIN2

Y9
CLK_XTAL_IN
CLK_XTAL_OUT
14.318MHZ
C474 22pF/50V
C475 22pF/50V
14.318MHz

CLK_3GPLLREQ# R282 10K/F
NEW-CARD_CLK_REQ# R276 10K/F

U24
CK505
ICS9LPRS365AGLFT

+CK_VDD_MAIN
VDDCPU
+CK_VDD_MAIN2
VDDPLL3
VDD48
VDDPCI
VDDREF
VDDSRC
VDDCPU
VDD96I/O
VDDPLL3I/O
VDDSRCI/O
VDDSRCI/O
VDDSRCI/O
VDDCPU_IO
NC
CLK_XTAL_IN
CLK_XTAL_OUT
X1
X2
CK_PWRGD/PD#
FSLB/TEST_MODE
SCLK
SDATA
GND
GND
GND48
GNDCPU
GNDPCI
GNDREF
GNDSRC
GNDSRC
GNDSRC

CPUCLKT0 CLK_CPU_BCLK 3
CPUCLKC0 CLK_CPU_BCLK# 3
CPUCLKT1 CLK_MCH_BCLK 6
CPUCLKC1 CLK_MCH_BCLK# 6
CPUT2_ITP/SRCT8 T18
CPUT2_ITP/SRCC8 T17
DOTT_96/SRCT0 MCH_DREFCLK 7
DOTC_96/SRCC0 MCH_DREFCLK# 7
27MHz_Nonss/SRCCLK1/SE1 DREF_SSCLK 7
27Mhz_ss/SRCCLC1/SE2 DREF_SSCLK# 7
SRCCLKT2/SATACL CLK_PCIE_SATA 15
SRCCLKC2/SATACL CLK_PCIE_SATA# 15
SRCCLKT3/CR#_C
SRCCLKC3/CR#_D
SRCCLKT4 CLK_PCIE_LAN 29
SRCCLKC4 CLK_PCIE_LAN# 29
PCI_STOP# H_STP_PCI# 17
CPU_STOP# H_STP_CPU# 17
SRCCLKT6 CLK_PCIE_ICH 16
SRCCLKC6 CLK_PCIE_ICH# 16
SRCCLKT7/CR#_F CLK_PCIE_MINI 31
SRCCLKC7/CR#_E CLK_PCIE_MINI# 31
SRCCLKT9 CLK_MCH_3GPLL 7
SRCCLKC9 CLK_MCH_3GPLL# 7
SRCCLKT10 CLK_PCIE_EXPCARD 31
SRCCLKC10 CLK_PCIE_EXPCARD# 31
SRCCLKT11/CR#_H NEW-CARD_CLK_REQ# R R281 475/F NEW-CARD_CLK_REQ# NEW-CARD_CLK_REQ# 31
SRCCLKC11/CR#_G CLK_3GPLLREQ# R R283 475/F CLK_3GPLLREQ# CLK_3GPLLREQ# 7
PCICLK0/CR#_A PCI_EC R284 33 CLK_PCI_EC 33
PCICLK1/CR#_B PCI_PCCARD R291 33 CLK_PCI_PCCARD 23
PCICLK2/TME TME
PCICLK3
PCICLK4/27_SELECT PCI_DBP R286 33 CLK_PCI_DBP 31
R287 33 CLK_PCI_ICH 16
PCI_F5/ITP_EN ITP_EN R290 22 R293 22 CLK_7402_48M 24 CLK_ICH_48M 17
USB_48MHZ/FSLA FSA R298 4.7K/F CPU_MCH_BSEL0
FSLC/TST_SL/REF FSC R277 4.7K/F CPU_MCH_BSEL2 R278 33 CLK_ICH_14M 17

+3V
R292 10K/F
TME
R285 *4.7K
0=overclocking of CPU and SRC Allowed
1 = overclocking of CPU and SRC not Allowed

+3V
RP37 4P2R-S-2.2K
Q24 2N7002E
17,31 ICH_SMBDATA
CLK_SDATA
17 CK_PWG
CPU_MCH_BSEL1 R280 4.7K/F FSB
Q25 2N7002E
17,31 ICH_SMBCLK
CLK_SCLK
14,31 CLK_SCLK
14,31 CLK_SDATA

C487 *33pF/50V CLK_PCI_EC
C503 *33pF/50V CLK_PCI_PCCARD
C489 10pF/50V CLK_PCI_ICH
C488 *33pF/50V CLK_PCI_DBP
C459 *33pF/50V CLK_ICH_14M
for EMI

PCI_DBP
R301 10K/F
0=UMA
1 = External VGA

ITP_EN
10K/F R302
Disable ITP

CPU Clock select

3 CPU_MCH_BSEL0 R308 *56 R306 1K/F +1.05V_VCCP R304 0 MCH_BSEL0 7
3 CPU_MCH_BSEL1 R274 *0 R273 1K/F +1.05V_VCCP R279 0 MCH_BSEL1 7
3 CPU_MCH_BSEL2 R271 *0 R270 1K/F +1.05V_VCCP R272 0 MCH_BSEL2 7

<FAE>
1K to NB only when XDP is implement.No XDP can use 0 ohm

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

PROJECT : SW7
Quanta Computer Inc.

Size	Document Number	Rev
	CLOCK GENERATOR	1A
Date: Friday, September 28, 2007	Sheet 2 of 44	

U22A

ADDR GROUP 0 CONTROL

ADDR GROUP 1 XDP/ITP SIGNALS

THERMAL

H CLK

RESERVED

Merom Ball-out Rev 1a

U22B

DATA GRP 2

DATA GRP 1

DATA GRP 3

MISC

Merom Ball-out Rev 1a

Add for ESD

*VZ0603M260APT

Layout Note:
Place voltage divider within 0.5" of GTLREF pin

Note:
H_DPRTSTP need to daisy chain from ICH8 to IMVP6 to CPU.

Reserved for EMI.

C418 0.1uF/10V

Merom CPU Socket PN:
FOX: DGT^000021
TYC: DGT^000012
MLX: DGT^000004

Place C close to the CPU_TEST4 pin. Make sure CPU_TEST4 routing is reference to GND and away from other noisy signal.

For the purpose of testability, route these signals through a ground referenced Z0 = 55ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

Q26 *MMBT3904

Populate ITP700Flex for bringup

Layout Note:
Place R4,R361,R346 & R7 close to CPU.

ITP debug signals

Layout Note:
Place R8 close ITP.

Q13 DTC144EUA

Q16 2N7002E

Comp0,2 connect with Zo=27.4ohm,Comp1,3 connect with Zo=55ohm, make those traces length shorter than 0.5".Trace should be at least 25 mils away from any other toggling signal.

ITP disable guidelines

Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the ITP
TMS	39 ohm +/- 1%	VTT	Within 2.0" of the ITP
TRST#	500-680ohm +/- 5%	GND	Within 2.0" of the ITP
TCK	27 ohm +/- 1%	GND	Within 2.0" of the ITP
TDO	150 ohm +/- 5%	VTT	Within 2.0" of the ITP

Note: Populate R5, R8, C372 & R430 when ITP connector is populated.

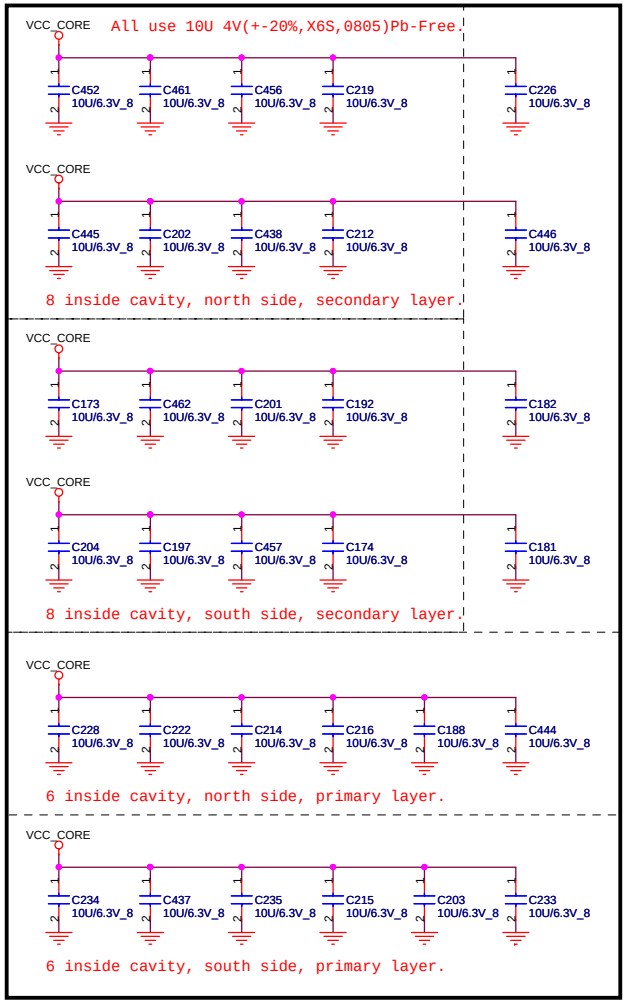
FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0

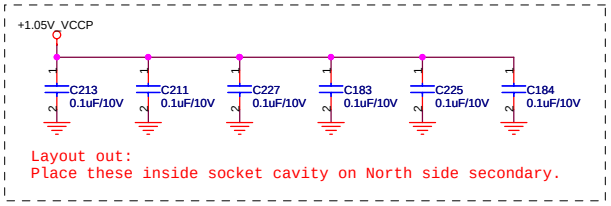
PROJECT : SW7

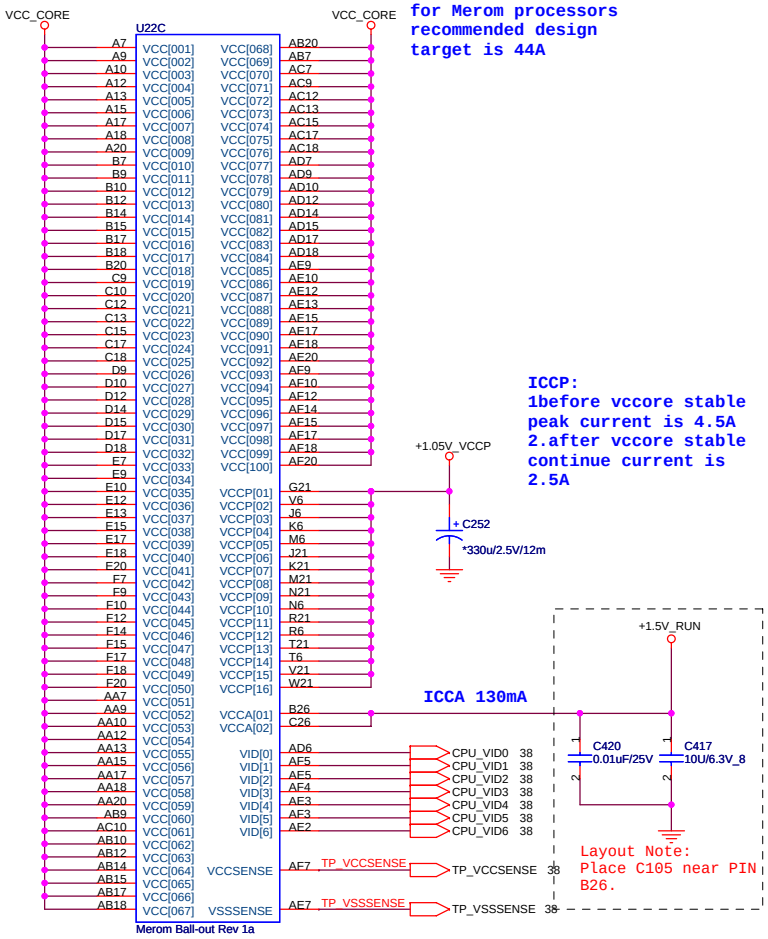
Quanta Computer Inc.

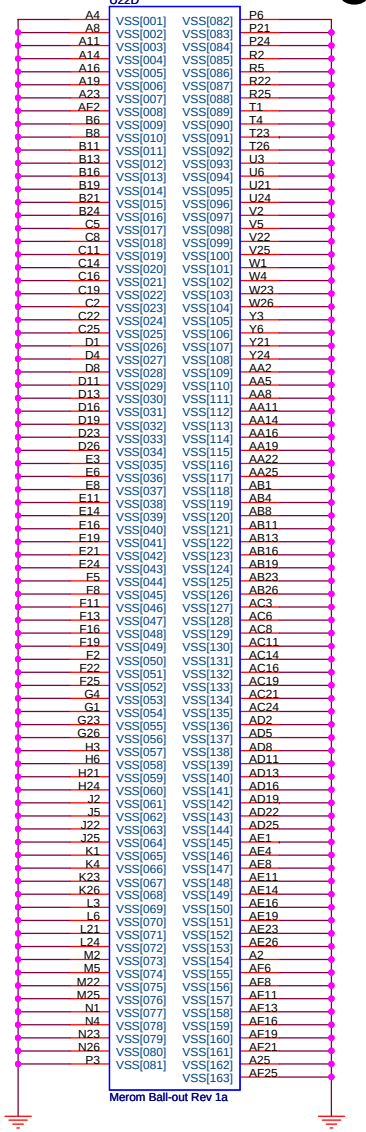
Size	Document Number	Rev
	Merom (HOST BUS)	1A

Date: Friday, September 28, 2007 Sheet 3 of 44

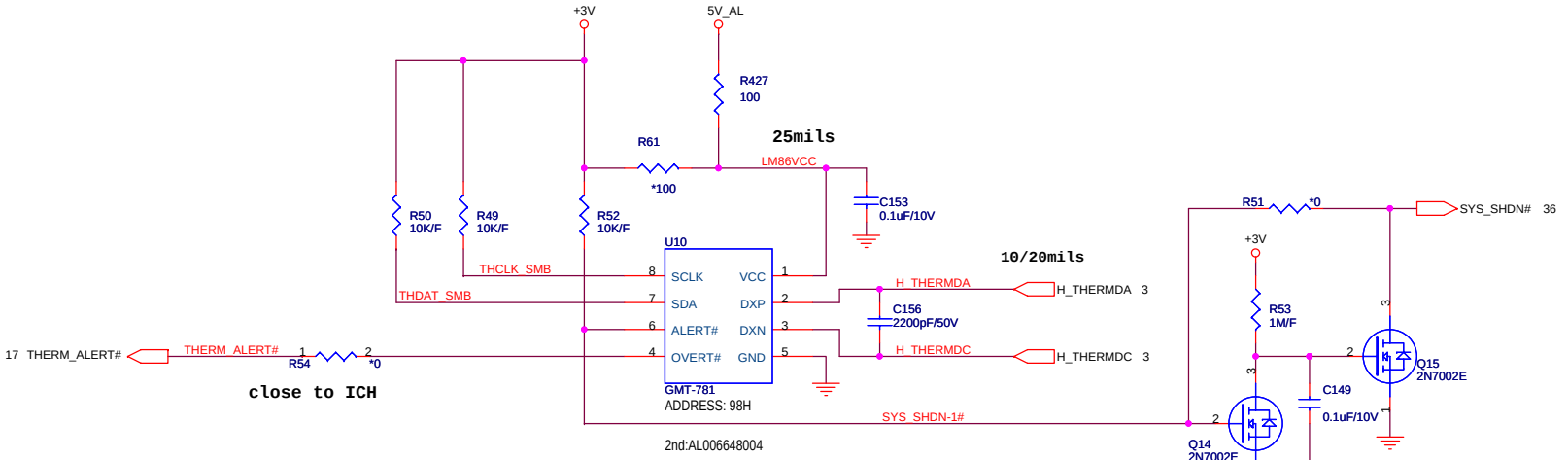


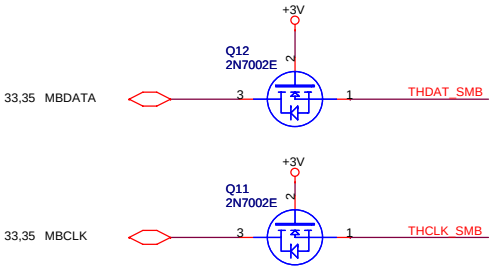




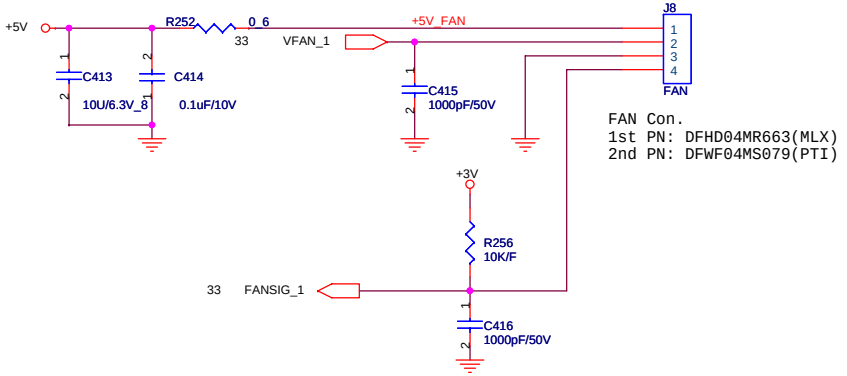


PROJECT : SW7		
Quanta Computer Inc.		
Size	Document Number	Rev
	Merom Processor (POWER)	1A
Date: Friday, September 28, 2007	Sheet 4 of 44	





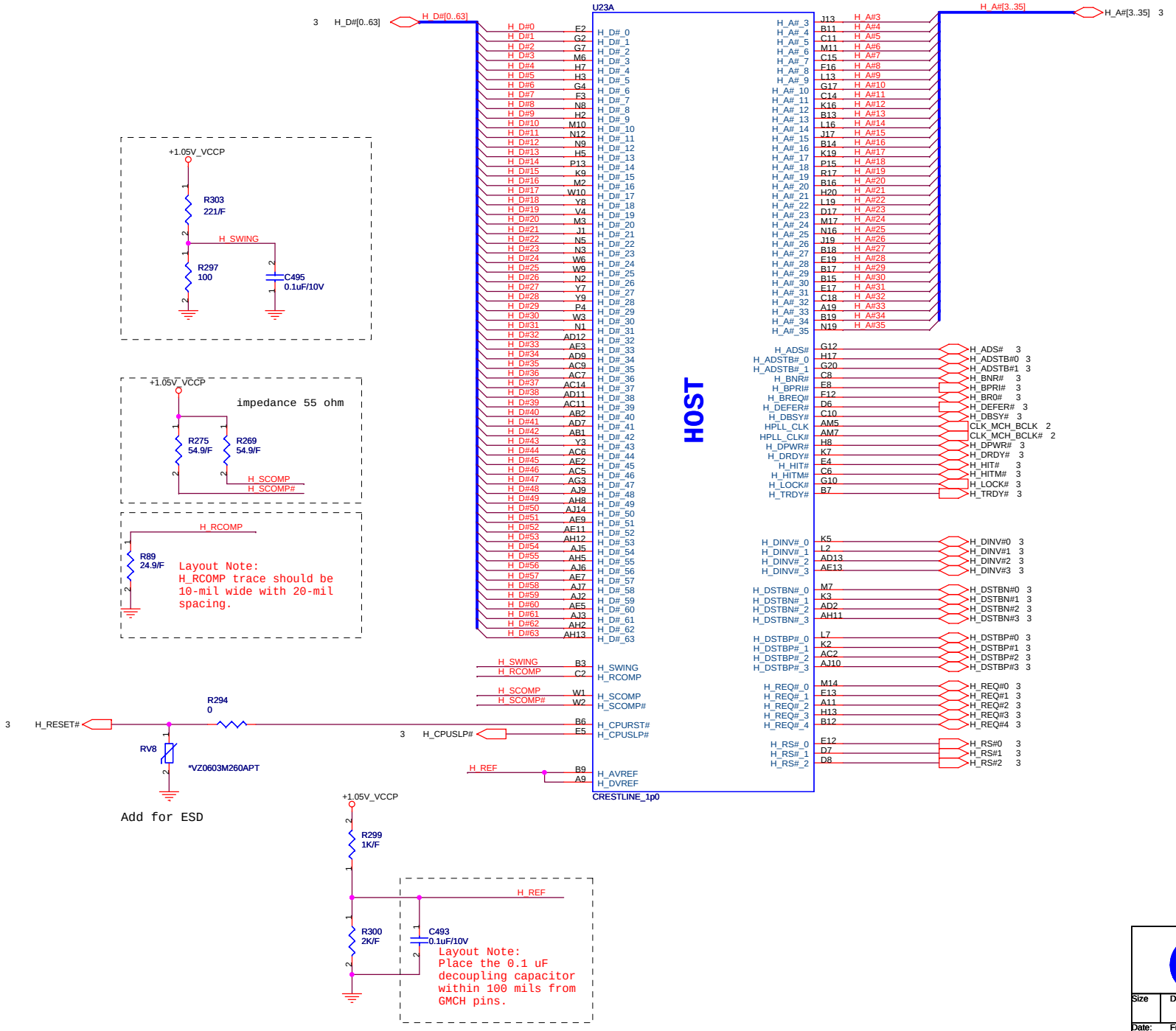
1st FAN OUT CONNECTOR



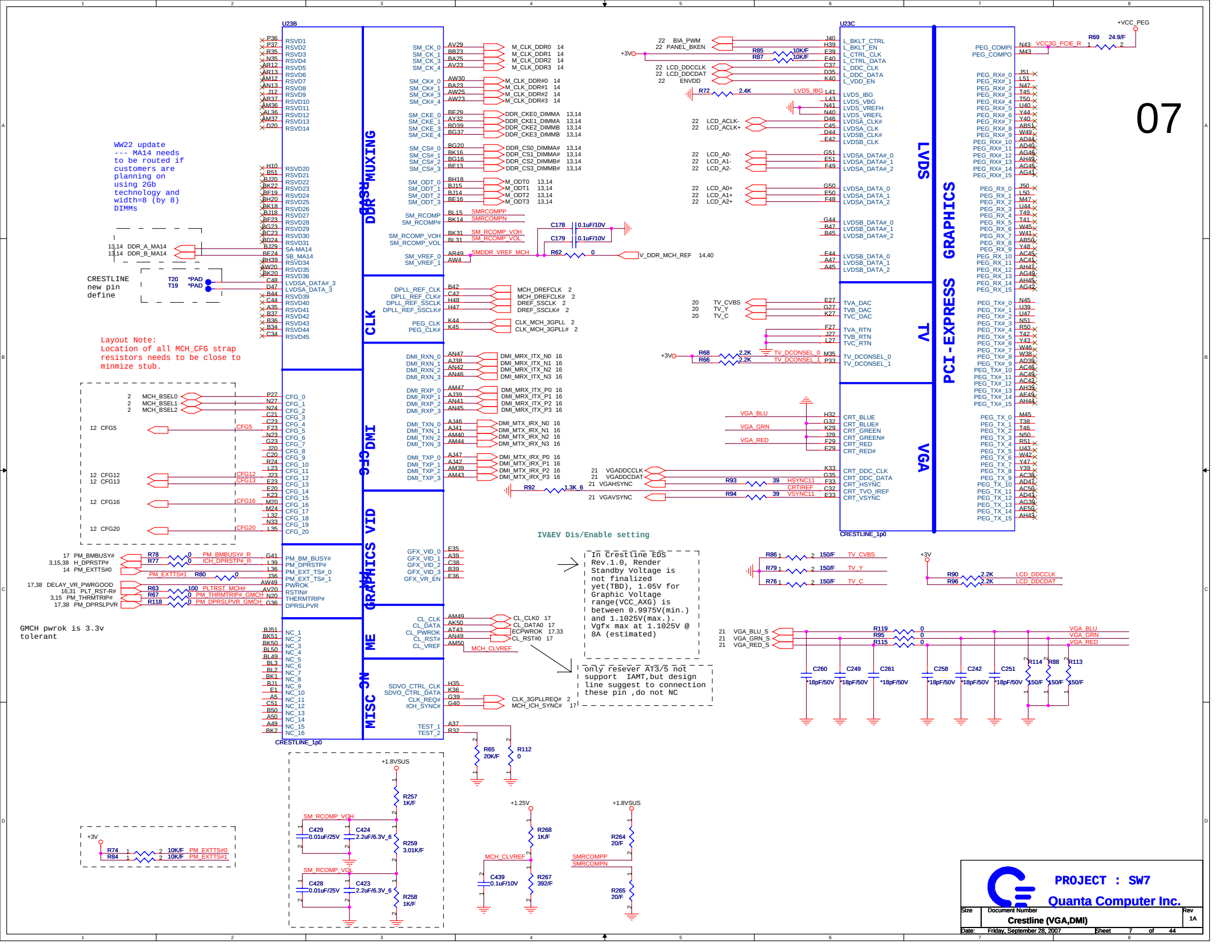
PROJECT : SW7

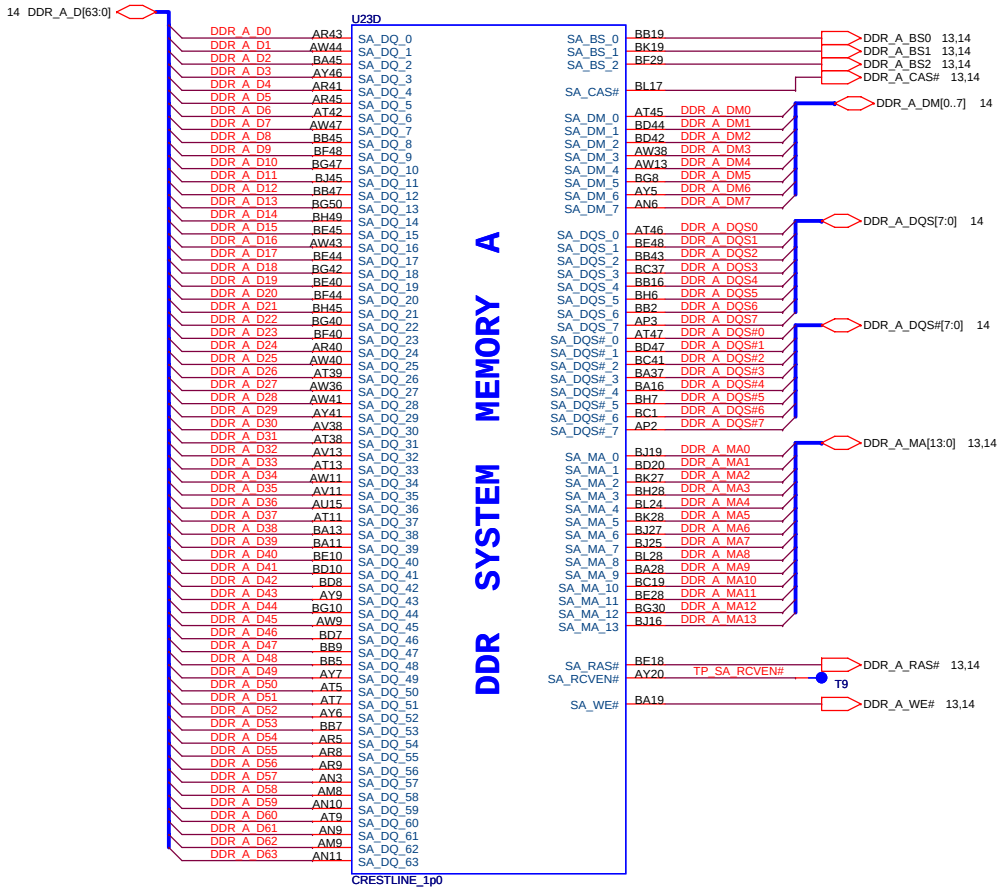
Quanta Computer Inc.

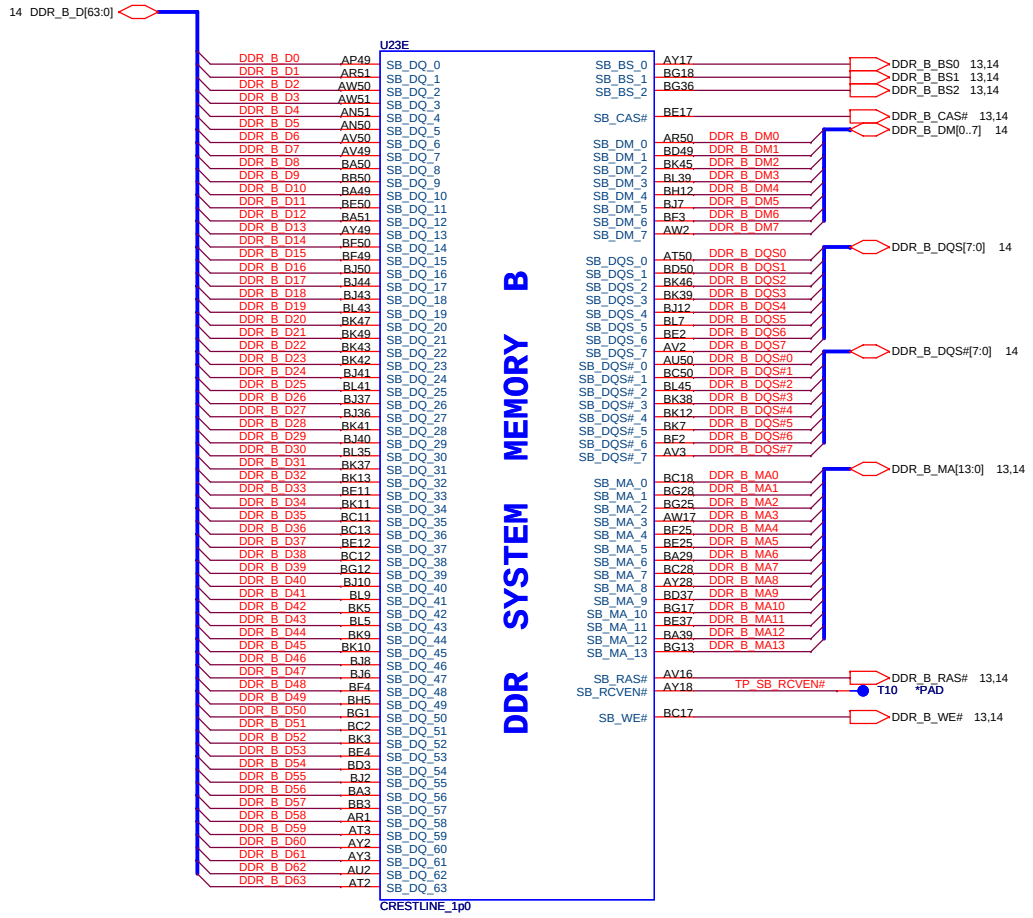
Size	Document Number	Rev
	THERMAL LM86 & FAN	1A
Date: Friday, September 28, 2007	Sheet 5 of 44	



PROJECT : SW7		
Quanta Computer Inc.		
Size	Document Number: Crestline (HOST)	Rev: 1A
Date: Friday, September 28, 2007	Sheet 6 of 44	


07
U23B
U23C
DDR MUXING
CLK
DMI CFG
GRAPHICS VID
MISC NC
LVDS
TV
VGA
PCI-EXPRESS GRAPHICS
CRESTLINE_1p0
WW22 update
--- MA14 needs
to be routed if
customers are
planning on
using 2Gb
technology and
width=8 (by 8)
DIMMs
CRESTLINE
new pin
define
Layout Note:
Location of all MCH_CFG strap
resistors needs to be close to
minmize stub.
GMCH pwrok is 3.3v
tolerant
IV&EV Dis/Enable setting
In Crestline EDS
Rev.1.0, Render
Standby Voltage is
not finalized
yet(TBD), 1.05V for
Graphic Voltage
range(VCC_AXG) is
between 0.9975V(min.)
and 1.1025V(max.).
Vgfx max at 1.1025V @
8A (estimated)
only resever A13/5 not
support IAMT,but design
line suggest to connection
these pin ,do not NC
PROJECT : SW7
Quanta Computer Inc.
Crestline (VGA,DMI)
Friday, September 28, 2007
Sheet 7 of 44
Rev 1A





PROJECT : SW7

Quanta Computer Inc.

Size	Document Number	Rev
	Crestline (DDR)	1A
Date: Friday, September 28, 2007	Sheet 8 of 44	

09

POWER

IVCCSM supply current 1 channel 1.615A 2 channel 3.318A

U23G

VCC CORE

VCC SM

VCC GFX NCTF

VCC GFX

VCC SM LF

CRESTLINE_1p0

U23F

VCC NCTF

VSS NCTF

VCC AXM

VCC AXM NCTF

VSS SCB

POWER

CRESTLINE_1p0

Layout Note:
370 mils from edge.

Ivcc (External GFX 1.310 A, integrate 1.572 A)

Layout Note:
Inside GMCH cavity.

Ivcc_AXG Graphics core supply current 7.7A

Layout Note:
370 mils from edge.

Layout Note:
Inside GMCH cavity for VCC_AXG.

for IAMT power if not support need to connection to S0 power

Ivcc_AXM Controller supply current 540mA

Layout Note:
Inside GMCH cavity.

Layout Note:
Place close to GMCH edge.

Layout Note:
Place C901 where LVDS and DDR2 taps.

Layout Note:
Place on the edge.

GMCH 1.05V	current(A)	Remark
VCC Core	1.573	(1.3A for external GFX)
VCC_AXG	7.7	for integrated Gfx
VCC_AXD	0.2	
VTT	0.85	FSB VCCP
VCC_PEG	1.2	for PCIEG
VCC_AXM	0.54	for IAMT function
VCCR_RX_DMI	0.25	DMI
SUM	**12.313**	

PROJECT : SW7

Quanta Computer Inc.

Size	Document Number	Rev
	Crestline (VCC, NCTF)	1A
Date: Friday, September 28, 2007	Sheet 9 of 44	

CRT/TV Disable/Enable guideline

External VGA with EV@part,Internal VGA with IV@ part

Ball	Enable	Disable	Ball	Enable	Disable
VCCA_CRT	3.3V	GND	VCCA_C_TVO	3.3V	GND
VCCD_CRT	1.5V	GND	VCCD_TVO	1.5V	1.5V
VCCDQ_CRT	1.5V	GND	VCCABG_DAC	3.3V	GND
VCCA_A_TVO	3.3V	GND	VSSABG_DAC	GND	GND
VCCA_B_TVO	3.3V	GND	VCC_SYNC	3.3V	GND

LVDS Disable/Enable guideline

External VGA with EV@part,Internal VGA with IV@ part

Signal	If SDVO Disable LVDS Disable	If SDVO enable LVDS Disable	If SDVO enable LVDS enable
VCCD_LVDS	GND	1.8V	1.8V
VCCA_LVDS	GND	GND	1.8V
VCCTX_LVDS	GND	GND	1.8V

IV&EV Dis/Enable setting

FB_120ohm+-25%_100mHz _200mA_0.2ohm DC

FB_180ohm+-25%_100mHz_1500mA_0.09ohm DC

FB_180ohm+-25%_100mHz_1500mA_0.09ohm DC

FB_180ohm+-25%_ 100mHz_1500mA_ 0.09ohm DC

FB_220ohm+-25%_100MHz _2A_0.1ohm DC

For TV-OUT

22nF & 0.1uF for VCC_TVDACA:C_R should be placed with in 250 mils from Crestline.

0.1Caps should be placed 200 mils with in its pins.

Ivcca_PEG_BG supply current 10mA

Ivcc_VTT FSB supply current 0.85A

Ivcc_DMI supply current 100mA

Ivcc_PEG supply current 1.2A

Ivcc_RX_DMI supply current 250mA

Reserved L81 pad for inductor.

Place caps close to VCC_AXD.

Place caps close to VCC_AXF

Place on the edge.

Place on the edge.

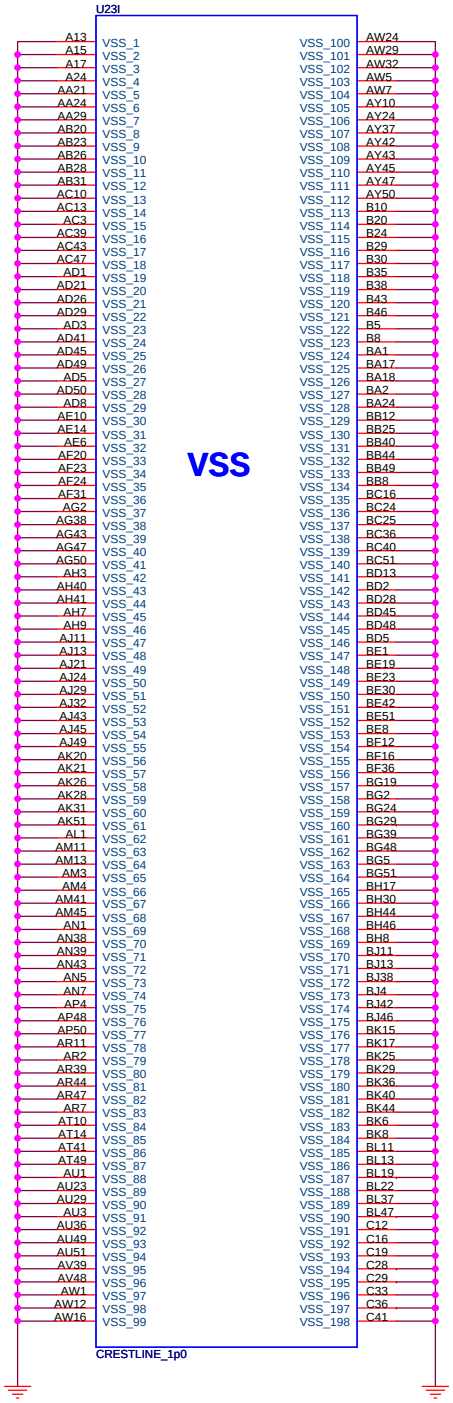
+3V_VCC_HV

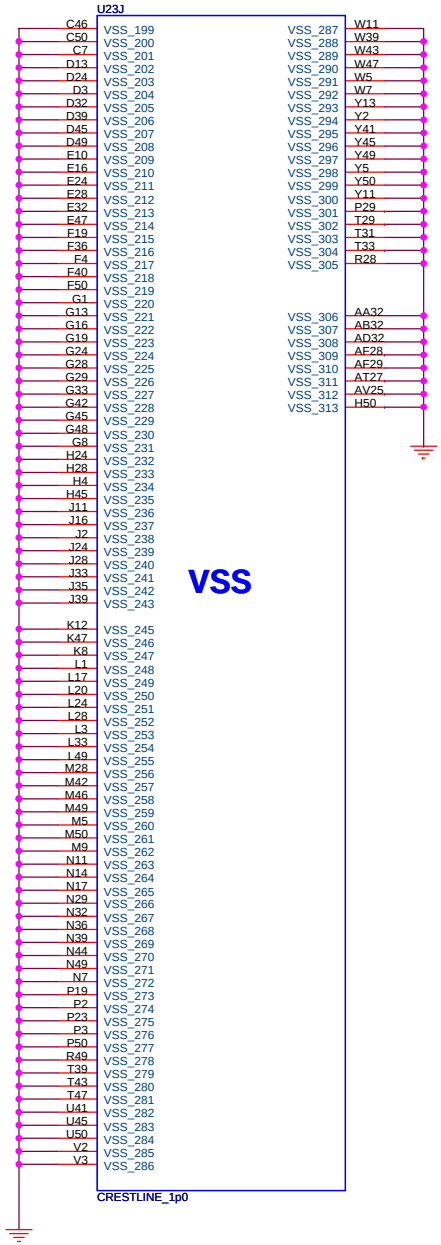
40 mil wide

U23H

CRESTLINE_1p0

Project	PROJECT : SW7
Company	Quanta Computer Inc.
Size	Document Number: Crestline (POWER)
Rev	1A
Date	Friday, September 28, 2007
Sheet	10 of 44





PROJECT : SW7

Quanta Computer Inc.

Size	Document Number	Rev
	Crestline (VSS)	1A
Date: Friday, September 28, 2007	Sheet 11 of 44	

Strap table

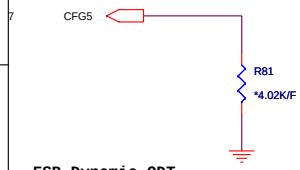
All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal

CFG[17:3] Have internal Pull-up
CFG[18:19] Have internal Pull-down
Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Low power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIe concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

DMI X2 Select

MCH_CFG_5	Low = DMIX2 High = IDMIX4(Default)



DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane

XOR /ALLz /Clock Un-gating

MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)

PCI Express Graphics

MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)

SDVO Present

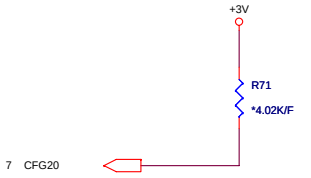
Strap define at External DVI control page

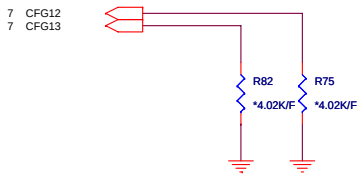
FSB Dynamic ODT

MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)

SDVO/PCIE Concurrent operation

MCH_CFG_20	Low = Only SDVO or PCIE X1 is operational(Default) High = SDVO andPCIE X1 are operating simultaneously via the PEG port



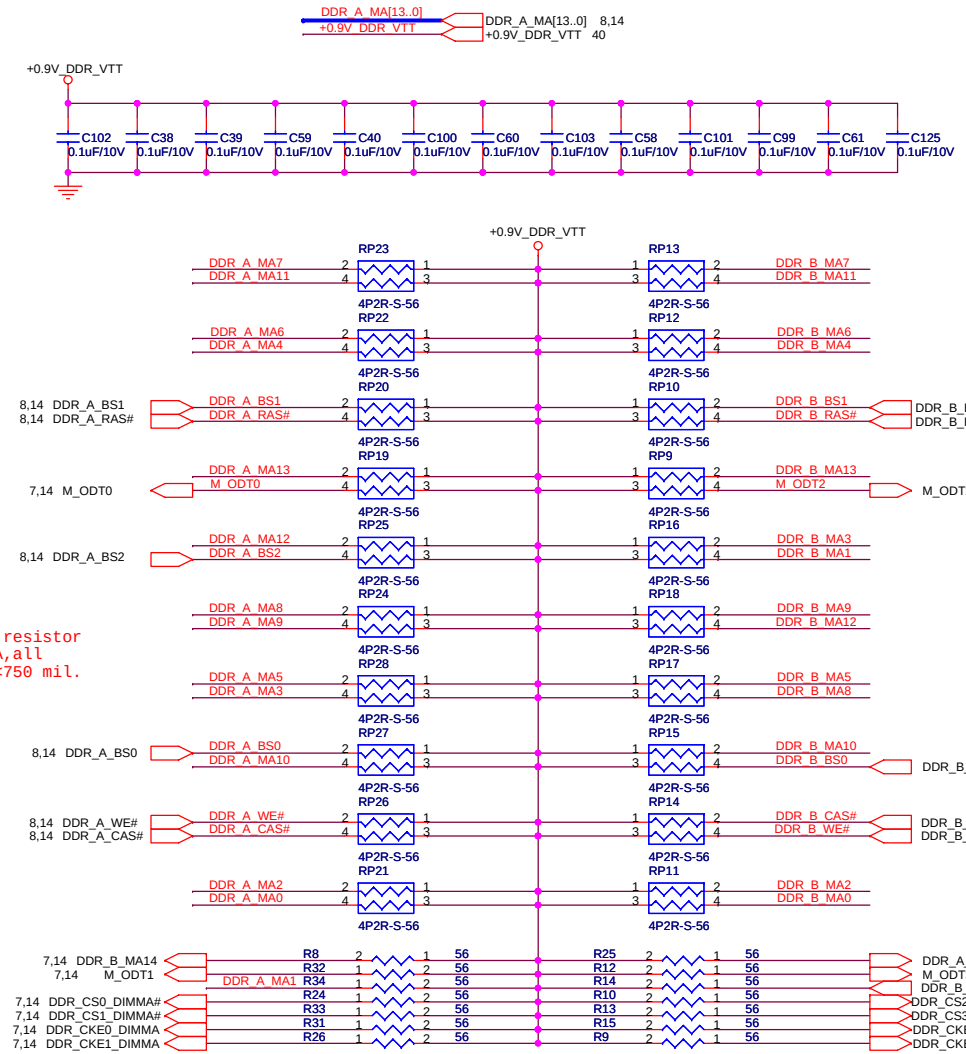


PROJECT : SW7
Quanta Computer Inc.

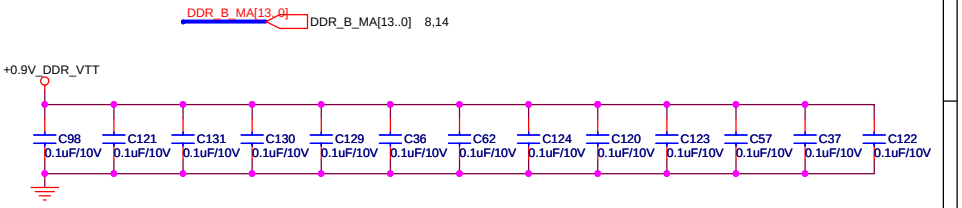
Size	Document Number	Rev
	GMCH STRAP	1A
Date: Friday, September 28, 2007	Sheet 12 of 44	

DDRII DUAL CHANNEL A,B.

DDRII A CHANNEL



DDRII B CHANNEL



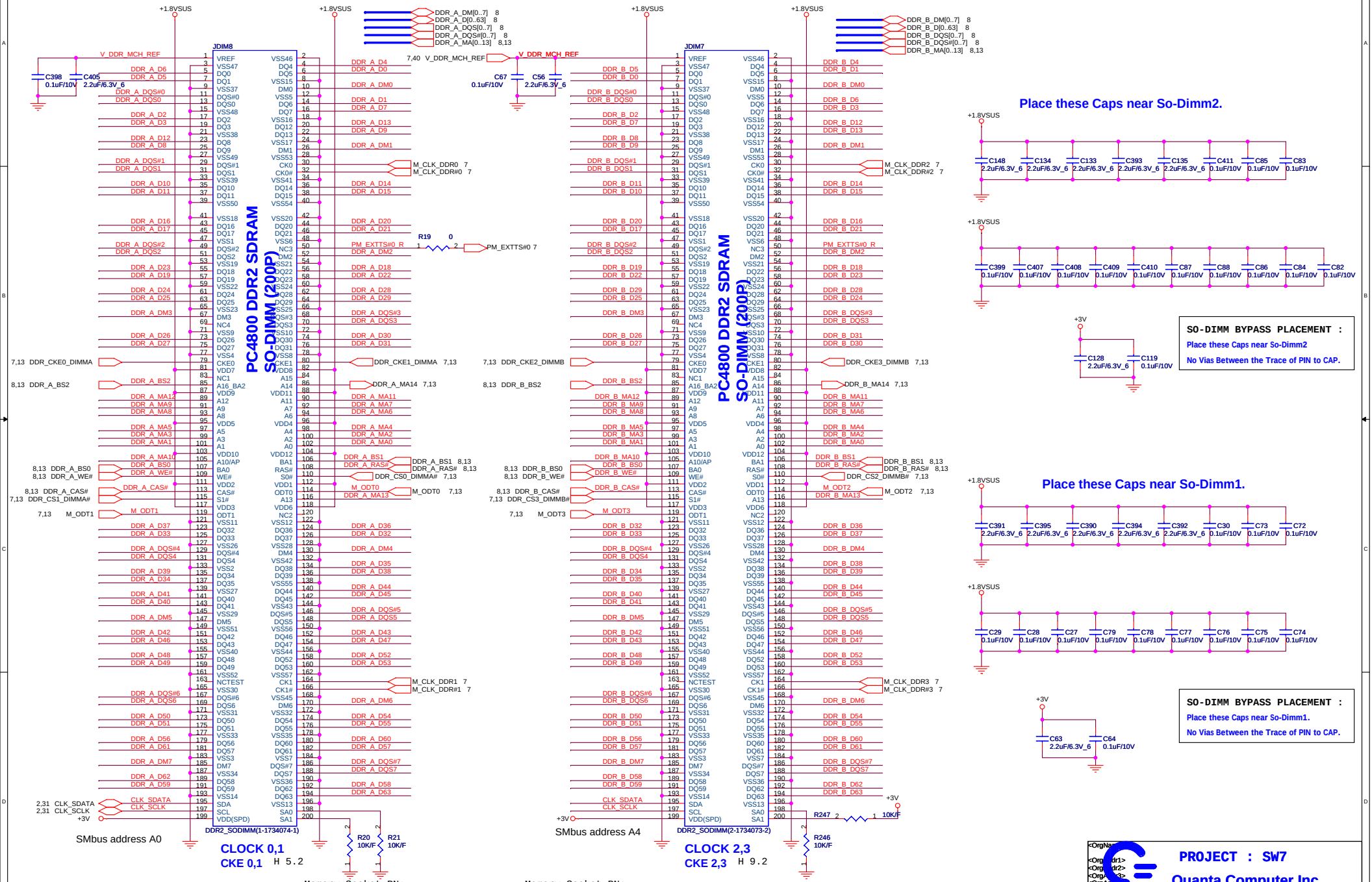
Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM

Please these resistor closely DIMMA,all trace length<750 mil.

Please these resistor closely DIMMB,all trace length<750 mil.

PROJECT : SW7		
Quanta Computer Inc.		
Size	Document Number: DDRII RES.ARRAY	Rev: 1A
Date: Friday, September 28, 2007	Sheet 13 of 44	

PROJECT :
Quanta Com



Place these Caps near So-Dimm2.

SO-DIMM BYPASS PLACEMENT :

Place these Caps near So-Dimm2

No Vias Between the Trace of PIN to CAP.

Place these Caps near So-Dimm1.

SO-DIMM BYPASS PLACEMENT :

Place these Caps near So-Dimm1.

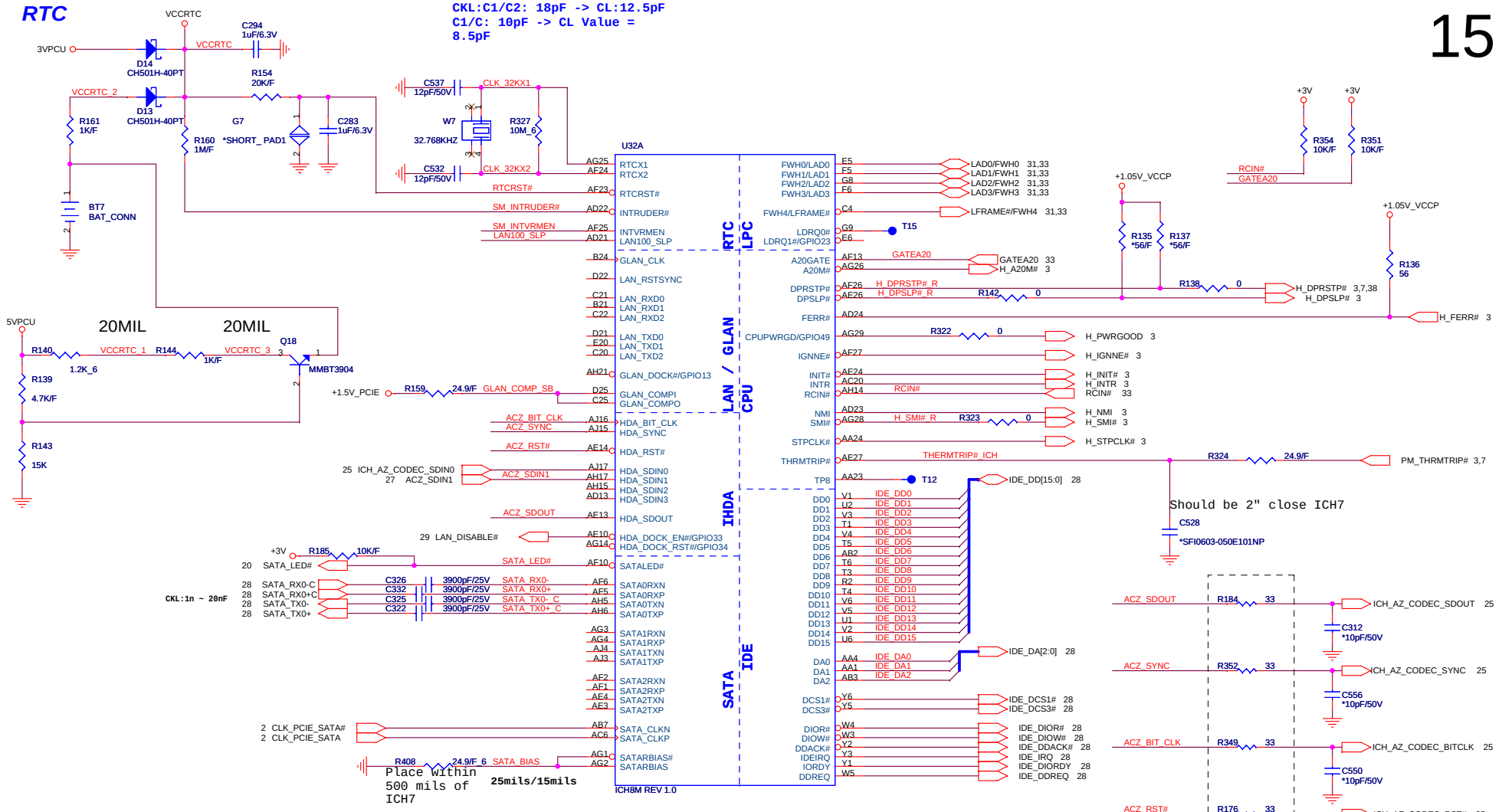
No Vias Between the Trace of PIN to CAP.

<OrgName>
<OrgAddr1>
<OrgAddr2>
<OrgAddr3>
<OrgAddr4>
PROJECT : SW7
Quanta Computer Inc.

Size	Document Number	Rev
	DDRII SO-DIMM(200P)	1A
Date: Friday, September 28, 2007	Sheet 14 of 44	

RTC

CKL:C1/C2: 18pF -> CL:12.5pF
C1/C: 10pF -> CL Value = 8.5pF



SB Strap

ICH8-M Internal VR Enable strap (Internal VR for Vccsus1_05,VccSus1_5 and VccCL1_5)

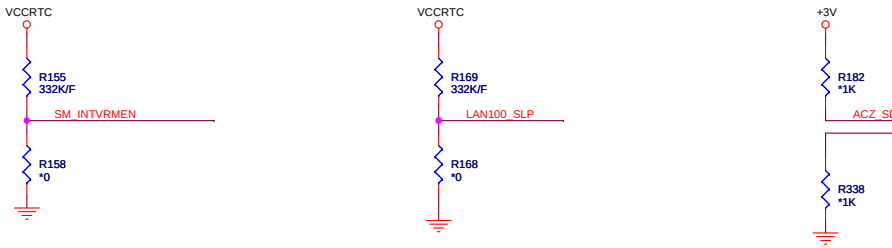
INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)

ICH8-M LAN100_SLP Strap (Internal VR for VccLAN1_05 and VccCL1.05)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)

XOR Chain Entrance Strap

ICH_RSV0	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1



PROJECT : SW7

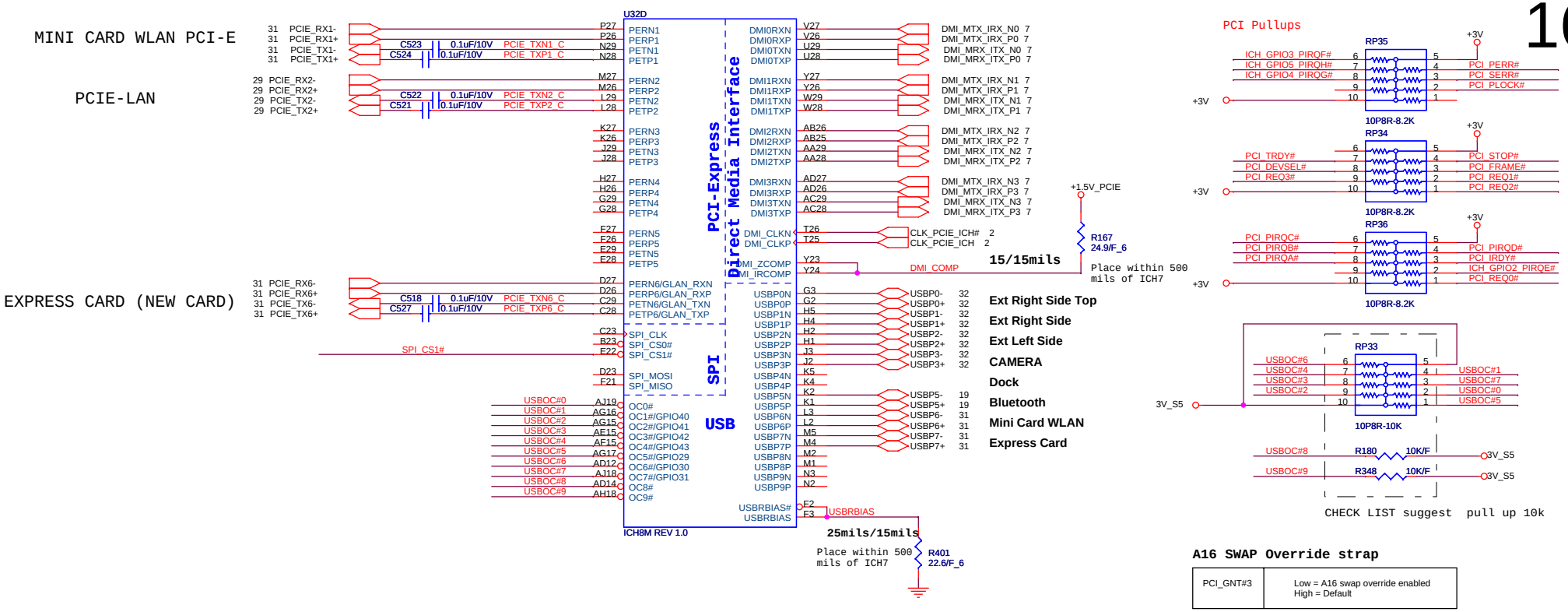
Quanta Computer Inc.

Size	Document Number	Rev
	ICH8-M HOST(1/4)	1A
Date: Friday, September 28, 2007	Sheet 15 of 44	

MINI CARD WLAN PCI-E

PCIE-LAN

EXPRESS CARD (NEW CARD)



PCI Pullups

CHECK LIST suggest pull up 10k

A16 SWAP Override strap

PCI_GNT#3	Low = A16 swap override enabled High = Default

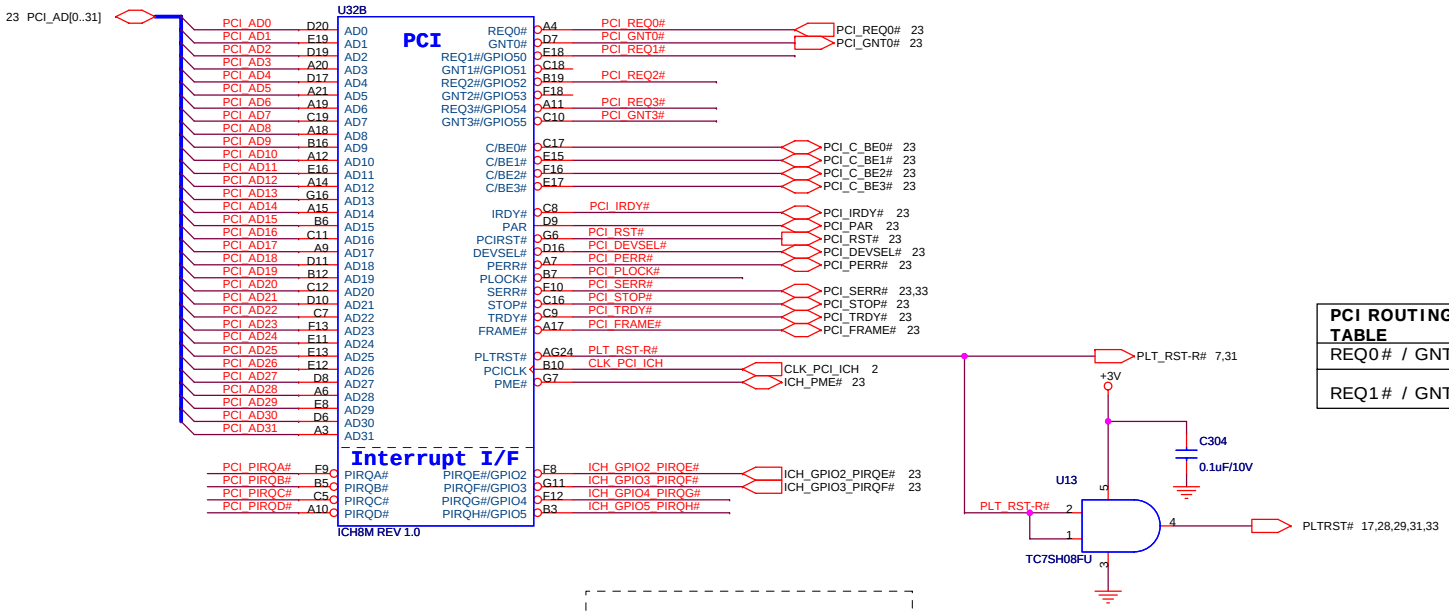
PCI_GNT3# R190 *1K

ICH8 Boot BIOS select

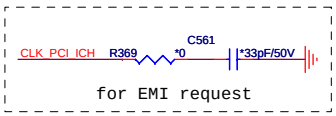
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC

SPI_CS1# R166 *1K

PCI_GNT0# R200 *1K



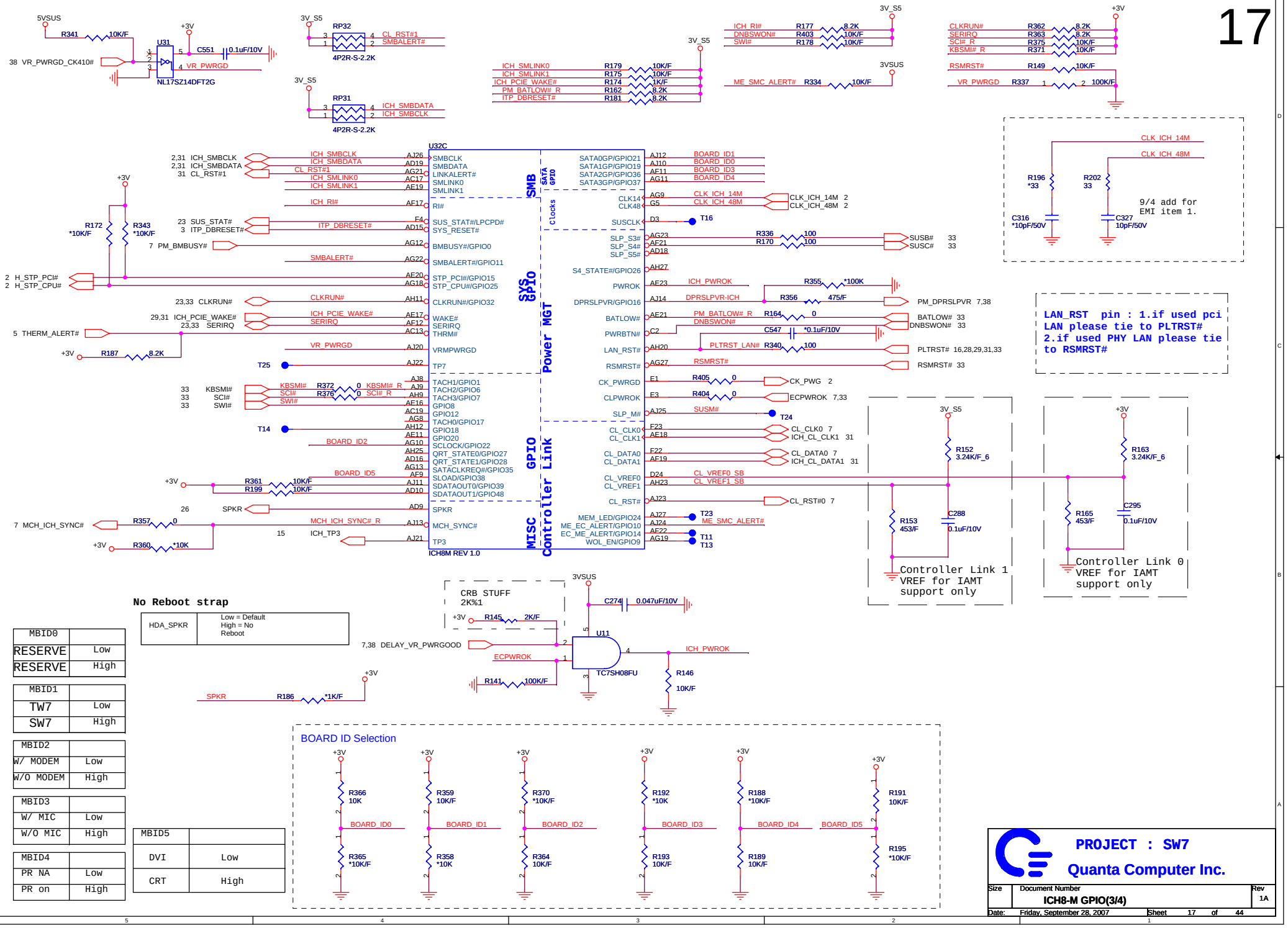
PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD25	INTE#,INTF#	PCI7402
REQ1# / GNT1#	AD22	INTC#,INTD#	MINI PCI for debug



PROJECT : SW7

Quanta Computer Inc.

Size	Document Number	Rev
	ICH8-M M PCI E(2/4)	1A
Date: Friday, September 28, 2007	Sheet 16 of 44	



MBID0	
RESERVE	Low
RESERVE	High

MBID1	
TW7	Low
SW7	High

MBID2	
W/ MODEM	Low
W/O MODEM	High

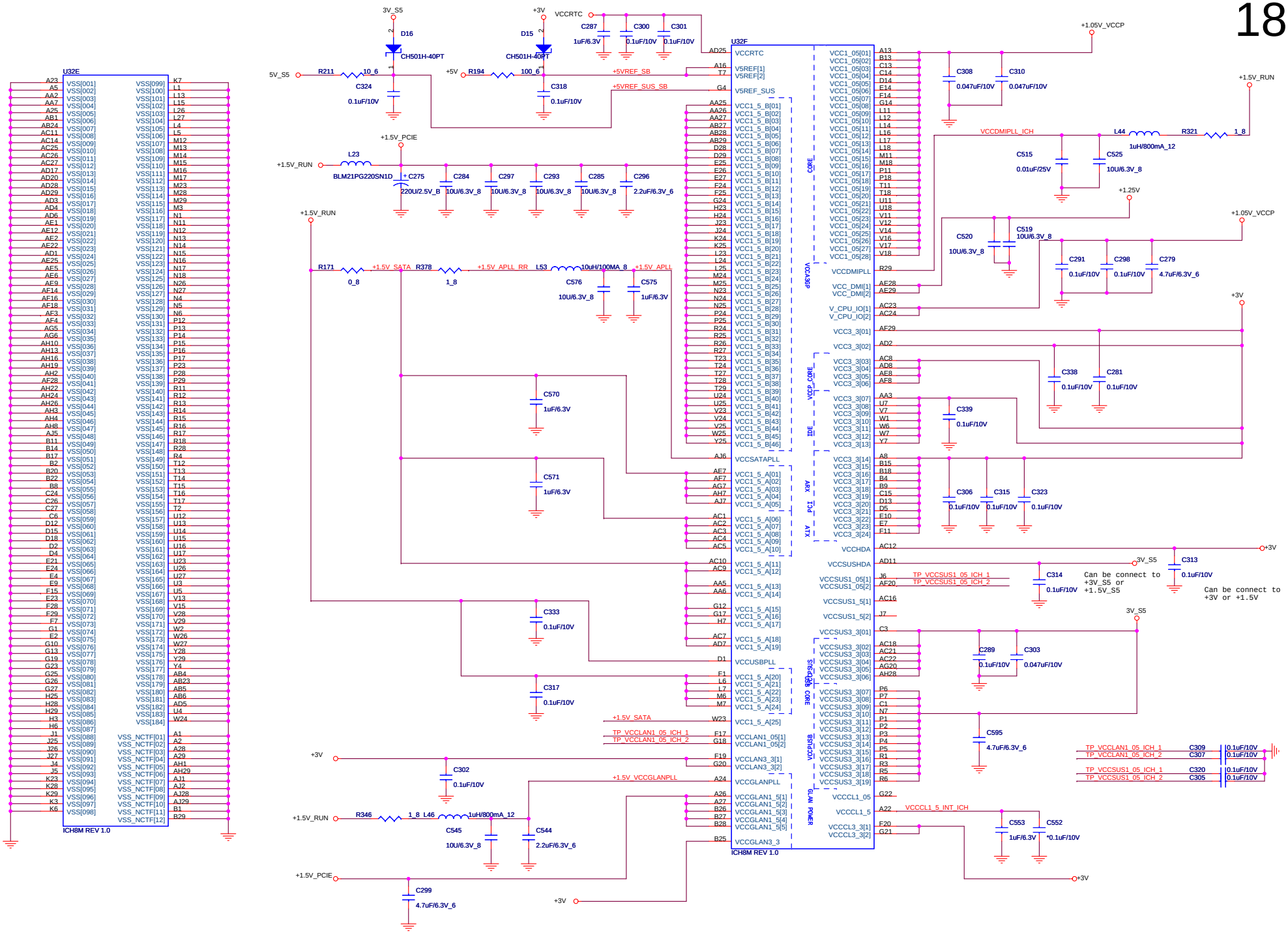
MBID3	
W/ MIC	Low
W/O MIC	High

MBID4	
PR NA	Low
PR on	High

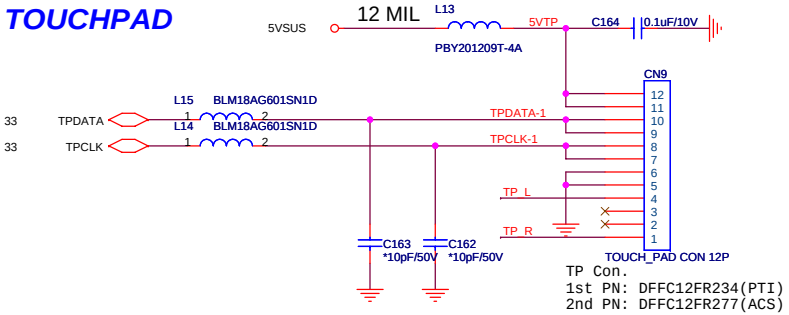
HDA_SPKR	Low = Default High = No Reboot

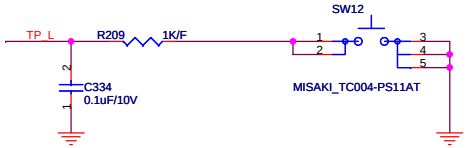
MBID5	
DVI	Low
CRT	High

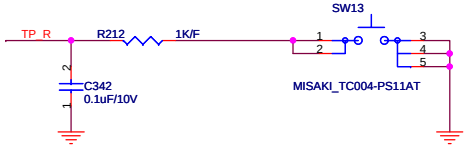
Size	Document Number	Rev
	ICH8-M GPIO(3/4)	1A
Date: Friday, September 28, 2007	Sheet 17 of 44	


U32E
ICH8M REV 1.0
U32F
ICH8M REV 1.0
D16
CH501H-40PT
D15
CH501H-40PT
3V_S5
+3V
VCCRTC
C287
1uF/6.3V
C300
0.1uF/10V
C301
0.1uF/10V
R211
10_6
C324
0.1uF/10V
R194
100_6
C318
0.1uF/10V
+5VREF_SB
+5VREF_SUS_SB
+1.5V_PCIE
+1.5V_RUN
L23
BLM21PG220SN1D
C275
220U/2.5V_B
C284
10U/6.3V_8
C297
10U/6.3V_8
C293
10U/6.3V_8
C285
10U/6.3V_8
C296
2.2uF/6.3V_6
R171
0_8
+1.5V_SATA
R378
1_8
+1.5V_APLL_RR
L53
10uH/100MA_8
+1.5V_APLL
C576
10U/6.3V_8
C575
1uF/6.3V
C570
1uF/6.3V
C571
1uF/6.3V
C333
0.1uF/10V
C317
0.1uF/10V
+1.5V_SATA
TP_VCCLAN1_05_ICH_1
TP_VCCLAN1_05_ICH_2
+3V
C302
0.1uF/10V
+1.5V_VCCGLANPLL
+1.5V_RUN
R346
1_8
L46
1uH/800mA_12
C545
10U/6.3V_8
C544
2.2uF/6.3V_6
+1.5V_PCIE
C299
4.7uF/6.3V_6
+3V
+1.05V_VCCP
C308
0.047uF/10V
C310
0.047uF/10V
+1.5V_RUN
VCCDMIPLL_ICH
L44
1uH/800mA_12
R321
1_8
C515
0.01uF/25V
C525
10U/6.3V_8
+1.25V
+1.05V_VCCP
C520
10U/6.3V_8
C519
10U/6.3V_8
C291
0.1uF/10V
C298
0.1uF/10V
C279
4.7uF/6.3V_6
+3V
C338
0.1uF/10V
C281
0.1uF/10V
C339
0.1uF/10V
C306
0.1uF/10V
C315
0.1uF/10V
C323
0.1uF/10V
+3V
3V_S5
C313
0.1uF/10V
TP_VCCSUS1_05_ICH_1
TP_VCCSUS1_05_ICH_2
C314
0.1uF/10V
Can be connect to
+3V_S5 or
+1.5V_S5
Can be connect to
+3V or +1.5V
3V_S5
C289
0.1uF/10V
C303
0.047uF/10V
C595
4.7uF/6.3V_6
TP_VCCLAN1_05_ICH_1
TP_VCCLAN1_05_ICH_2
C309
0.1uF/10V
C307
0.1uF/10V
TP_VCCSUS1_05_ICH_1
TP_VCCSUS1_05_ICH_2
C320
0.1uF/10V
C305
0.1uF/10V
VCCCL1_5_INT_ICH
C553
1uF/6.3V
C552
*0.1uF/10V
+3V
PROJECT : SW7
Quanta Computer Inc.
Size
Document Number
ICH8-M POWER(4/4)
Rev
1A
Date: Friday, September 28, 2007
Sheet 18 of 44

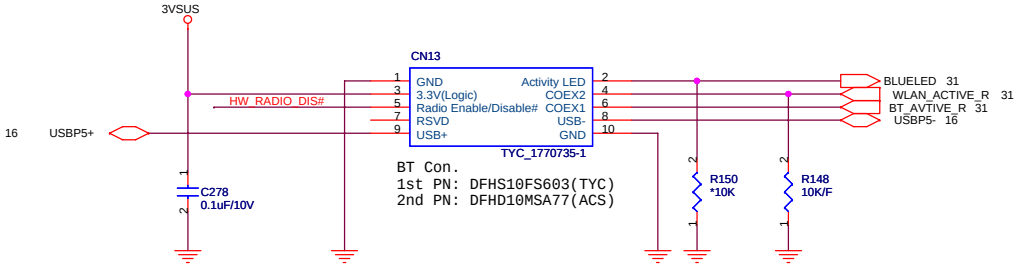
TOUCHPAD

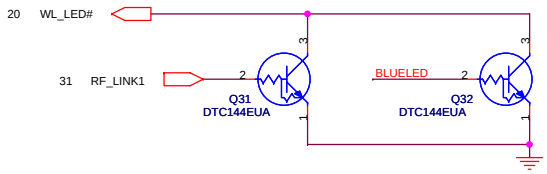


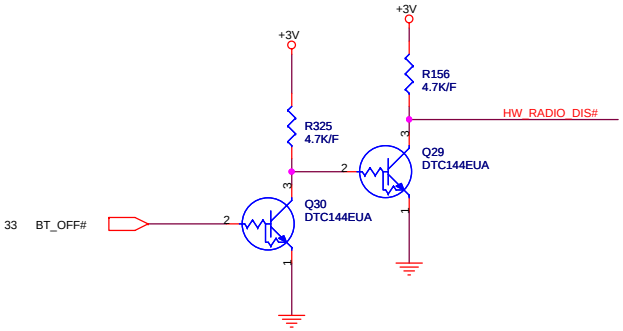




Bluetooth





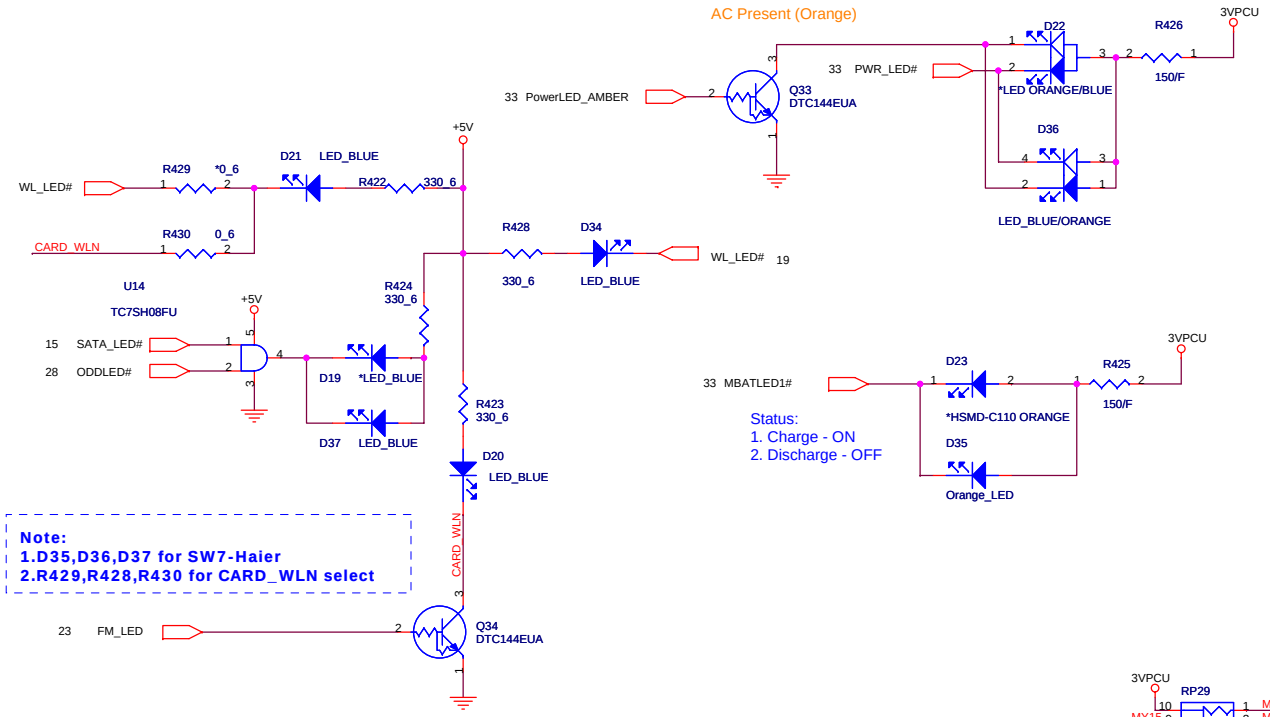


PROJECT : SW7

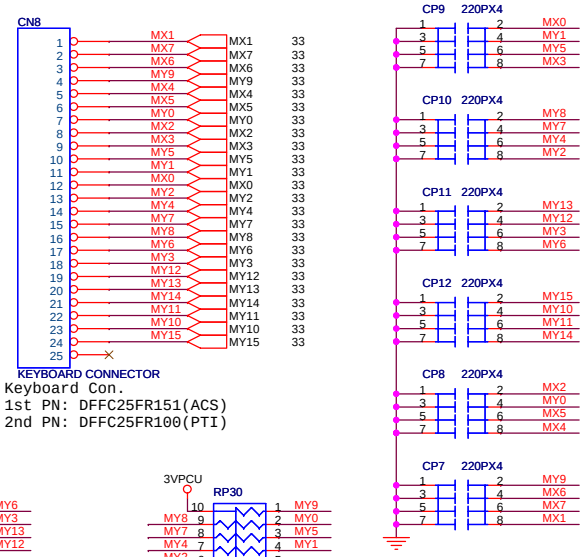
Quanta Computer Inc.

Size	Document Number	Rev
	TOUCH PAD & BULE TOOTH	1A
Date: Friday, September 28, 2007	Sheet 19 of 44	

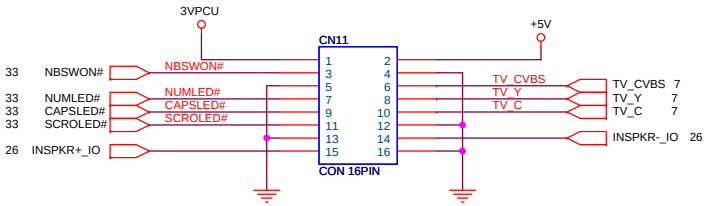
LED



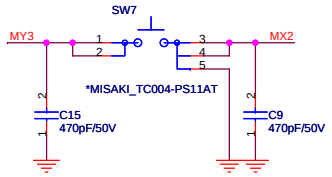
KEYBOARD



I/O Board CONN

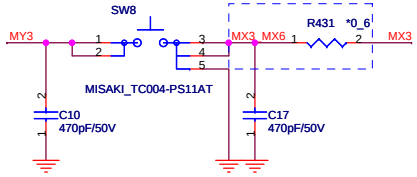


IE

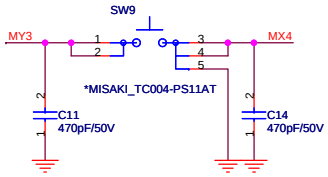


E-Mail

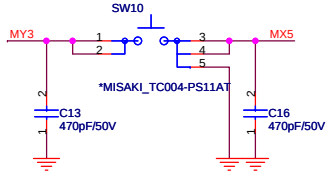
MODIFY FOR SWITCH WLAN FUNCTION



FAN

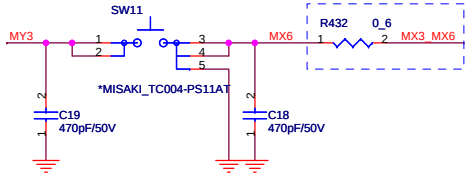


MUTE

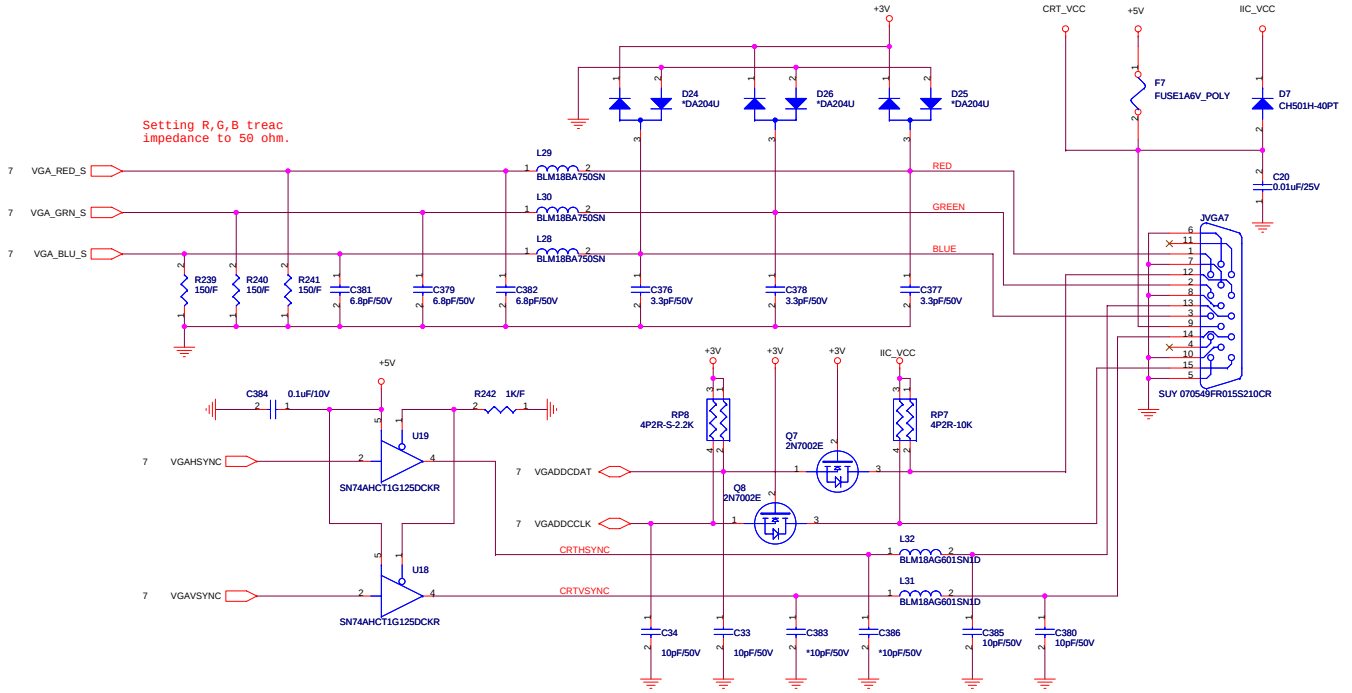


WLAN

MODIFY FOR SWITCH WLAN FUNCTION



PROJECT : SW7		
Quanta Computer Inc.		
Size	Document Number: SWITCH, KEYBOARD & LED	Rev: 1A
Date: Friday, September 28, 2007	Sheet 20 of 44	

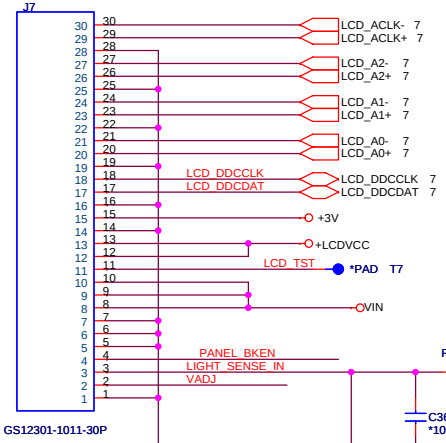


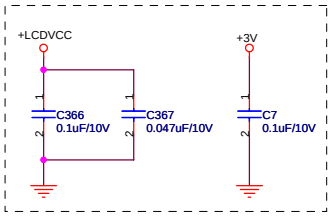
PROJECT : SW7

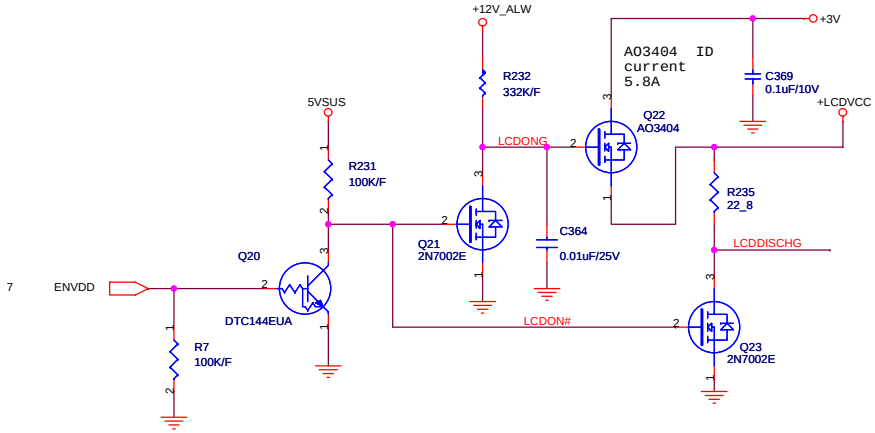
Quanta Computer Inc.

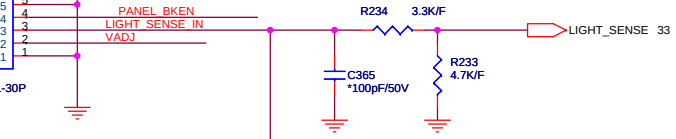
Size	Document Number	Rev
	CRT	1A
Date: Friday, September 28, 2007	Sheet 21 of 44	

LCD CONNECTOR

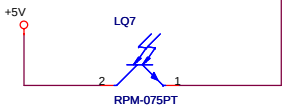






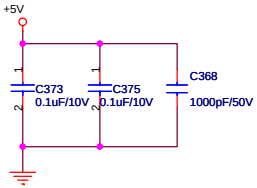


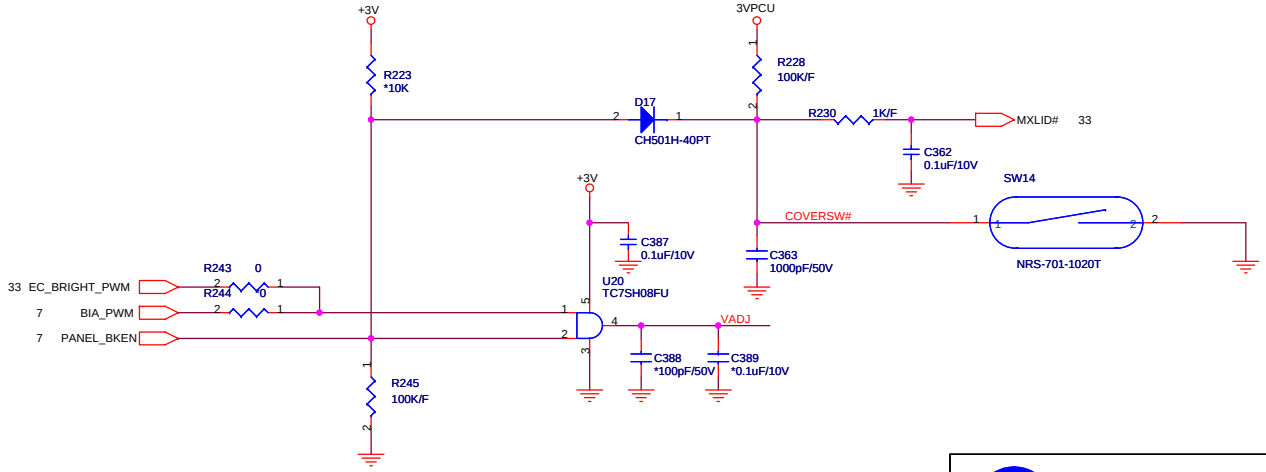
Light sensor



Pin 1:Emitter

Pin 2:Collector

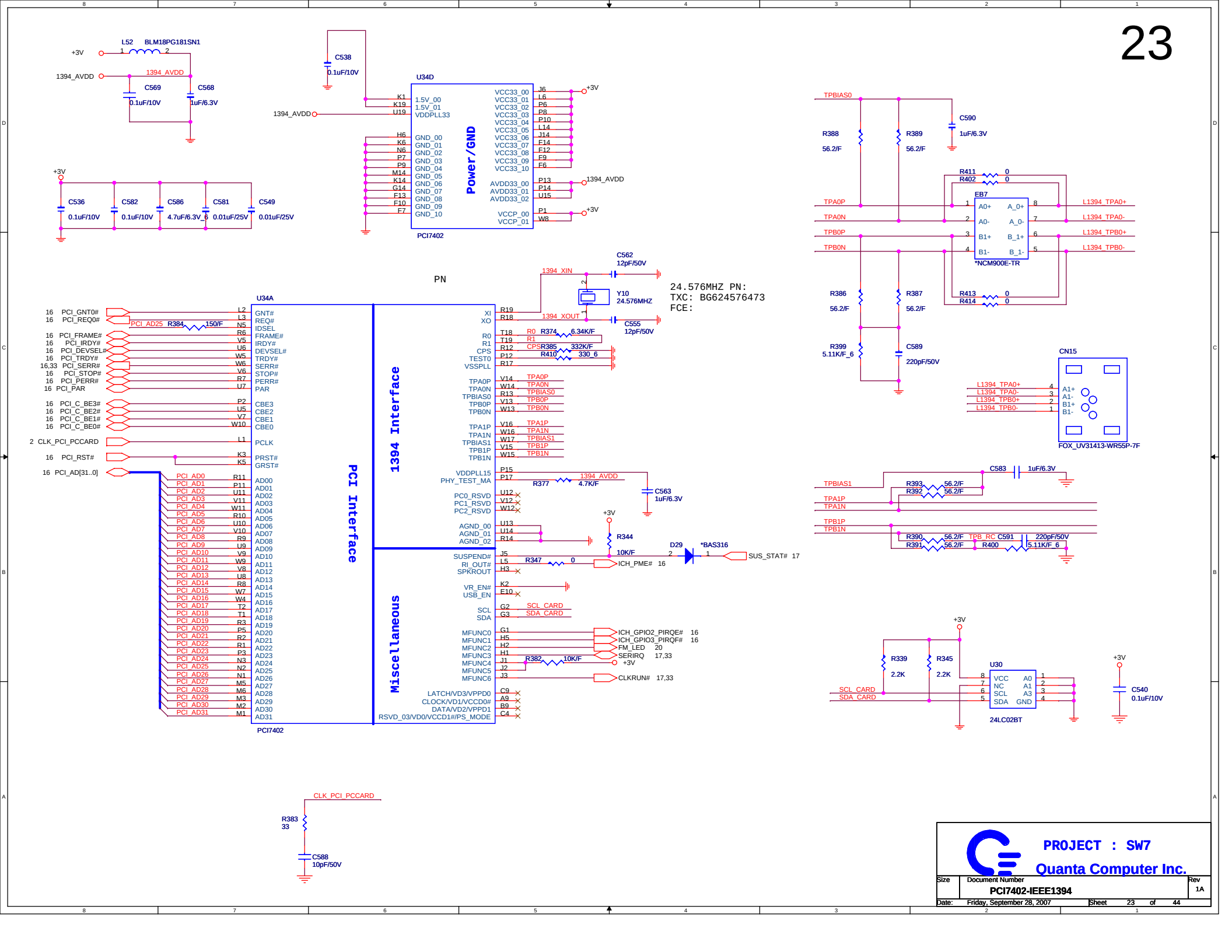




PROJECT : SW7

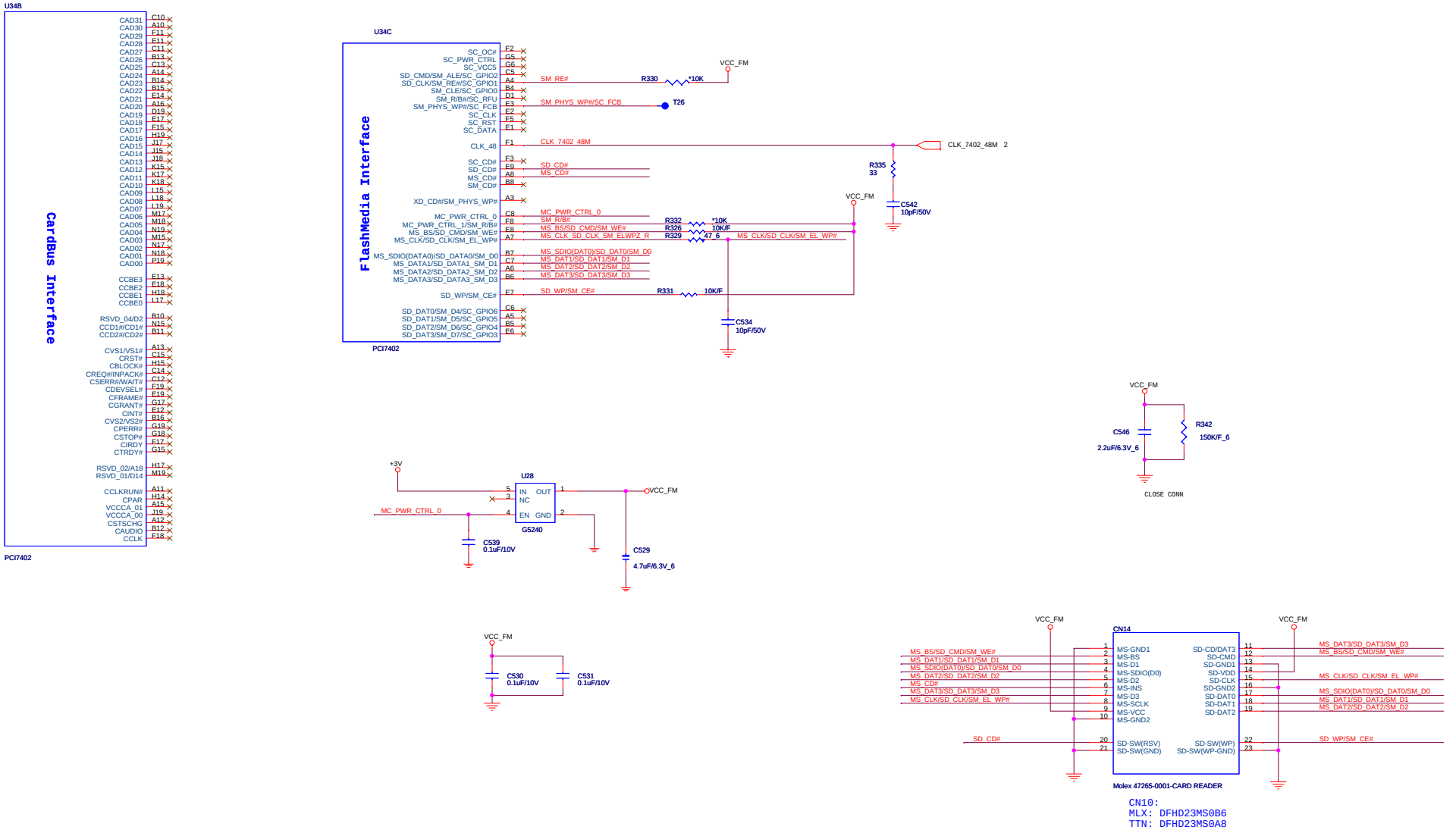
Quanta Computer Inc.

Size	Document Number	Rev
	LCD CONN	1A
Date: Friday, September 28, 2007	Sheet 22 of 44	



Quanta Computer Inc.	PROJECT : SW7	
Size	Document Number: PCI7402-IEEE1394	Rev: 1A
Date: Friday, September 28, 2007	Sheet 23 of 44	

DO NOT INSERT SD/MMC, MEMORYSTICK AND XD SIMULTANEOUSLY.

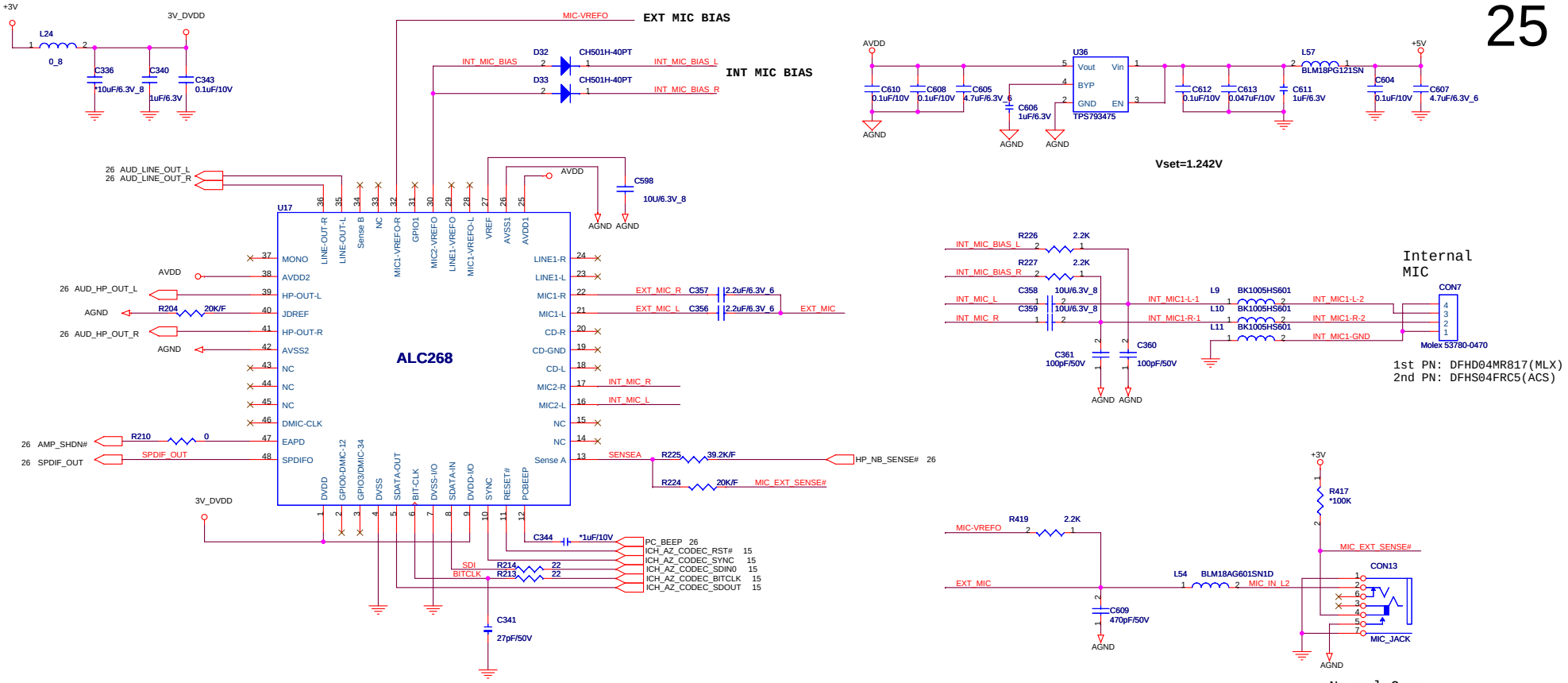


PROJECT : SW7

Quanta Computer Inc.

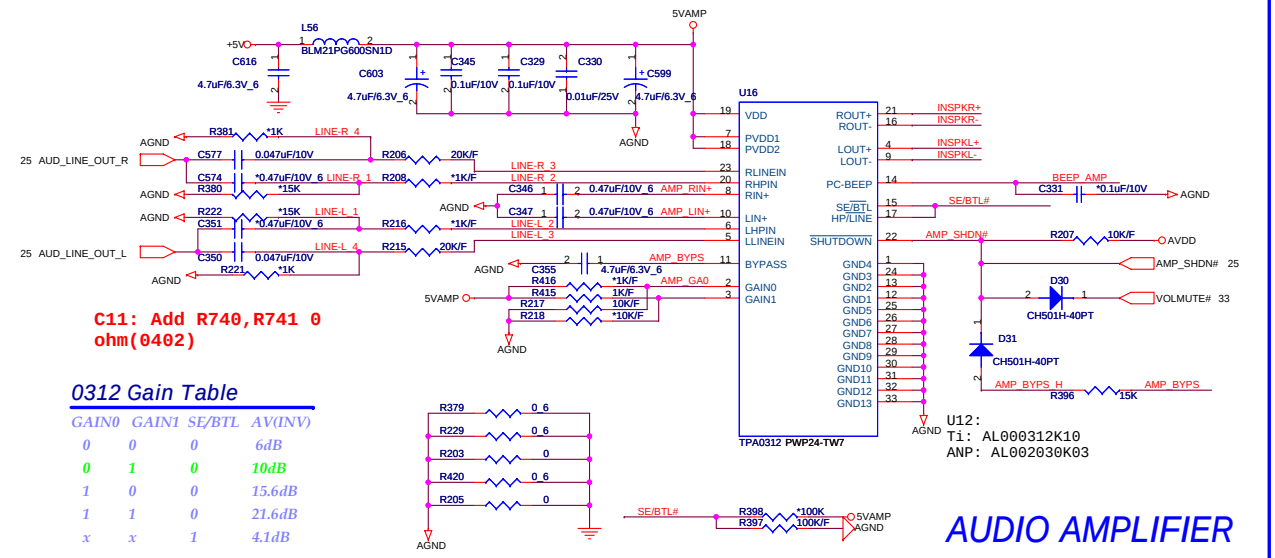
Size	Document Number	Rev
	PCI7402-CARD READER	1A

Date: Friday, September 28, 2007 Sheet 24 of 44



PROJECT : SW7		
Quanta Computer Inc.		
Size	Document Number	Rev
	Azalia ALC268	1A
Date: Friday, September 28, 2007	Sheet 25 of 44	

PROJECT : SW7
Quanta Computer Inc.

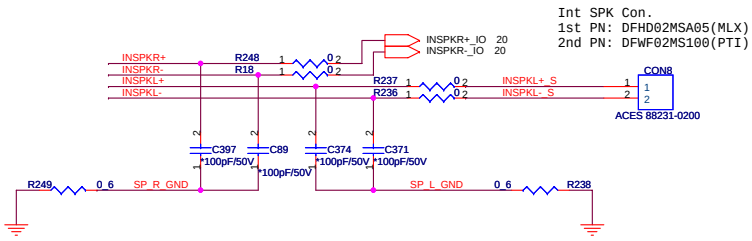


0312 Gain Table

GAIN0	GAIN1	SE/BTL	AV(INV)
0	0	0	6dB
0	1	0	10dB
1	0	0	15.6dB
1	1	0	21.6dB
x	x	1	4.1dB

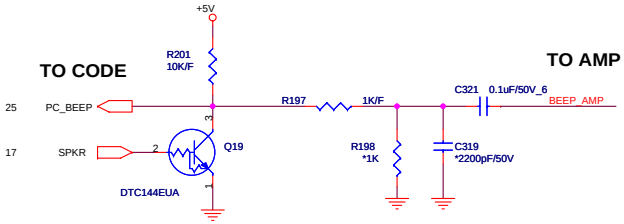
AUDIO AMPLIFIER

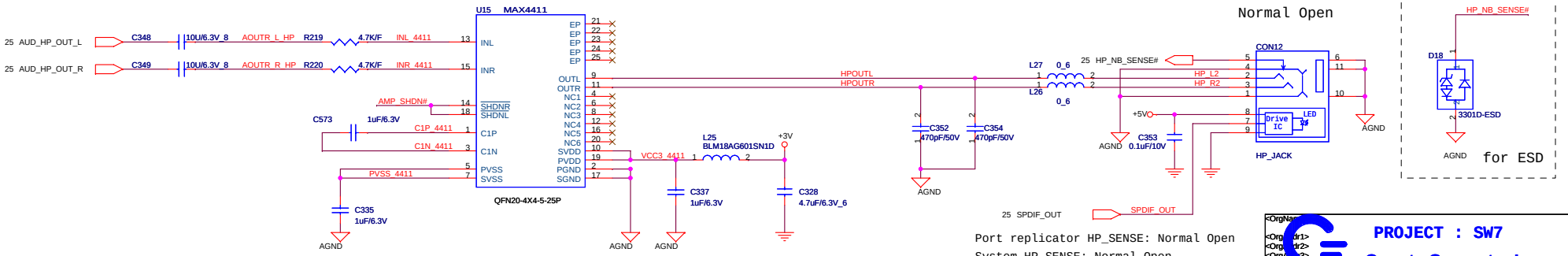
INT. SPEAKER



Int SPK Con.
1st PN: DFHD02MSA05(MLX)
2nd PN: DFWF02MS100(PTI)

PCSPK BEEP





Normal Open

Port replicator HP_SENSE: Normal Open
System HP_SENSE: Normal Open

<OrgName>	PROJECT : SW7	
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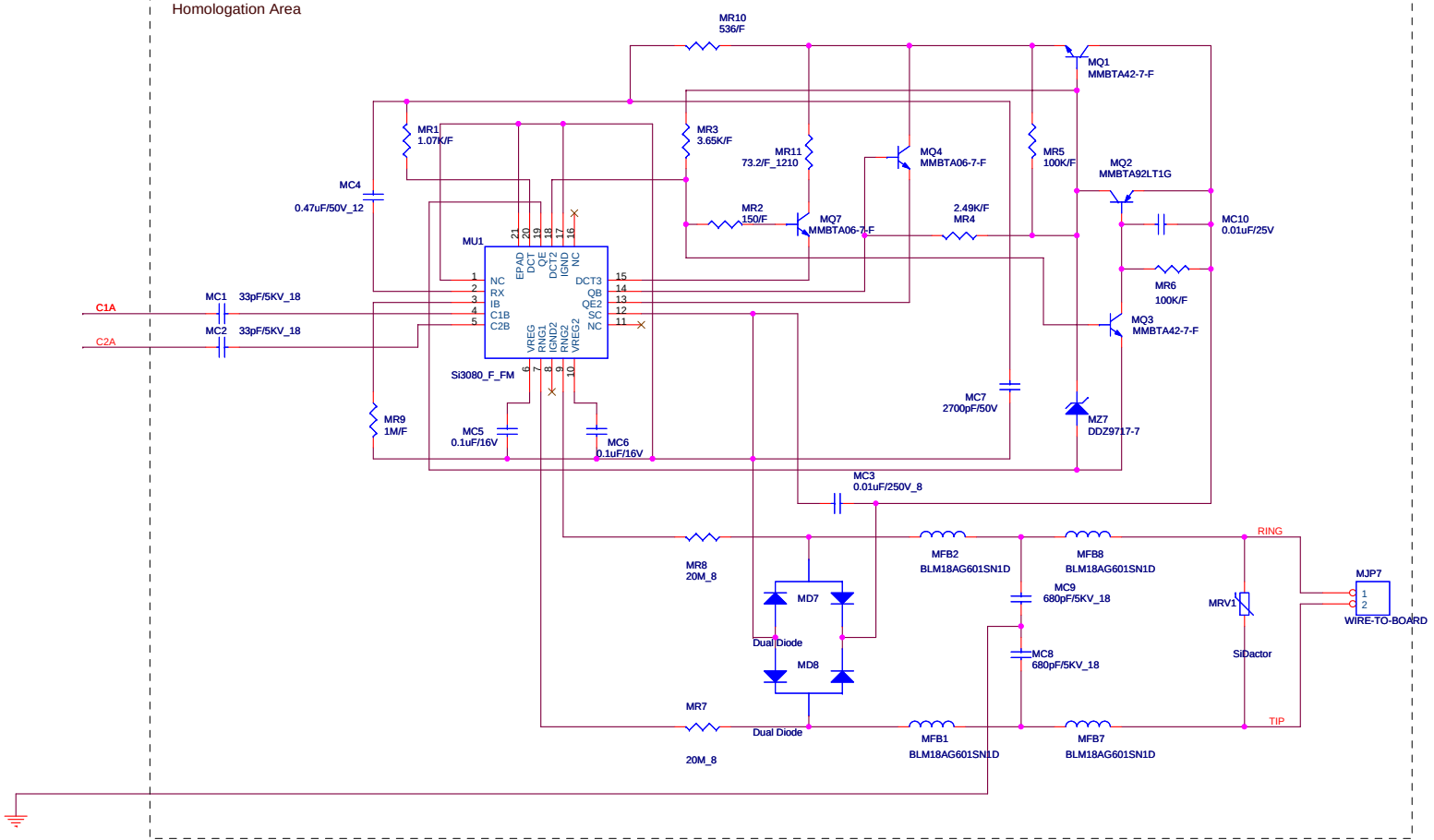
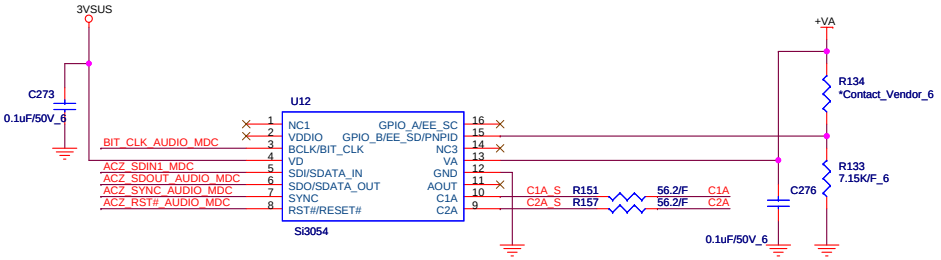
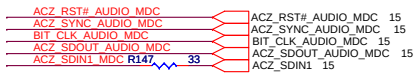
<OrgAdr2>		
<OrgAdr3>		
Size	Document Number	Rev
	JACK/AMP_TAP0312	1A
Date: Friday, September 28, 2007	Sheet 26 of 44	

No Ground Plane In DAA Section

Homologation Area







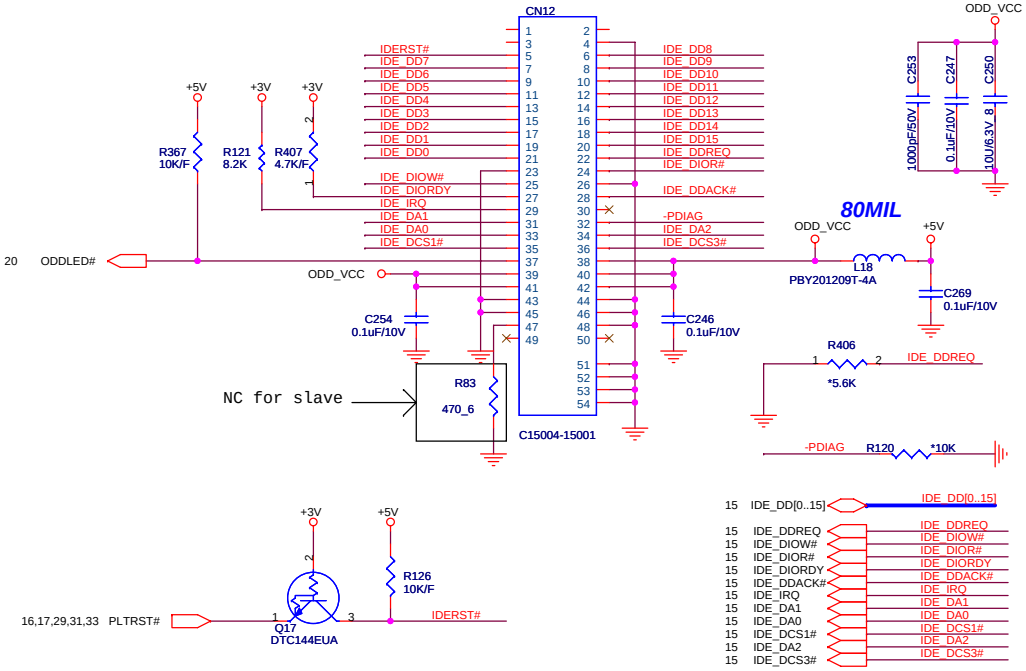
SILICON LABORATORIES CONFIDENTIAL

PROJECT : SW7

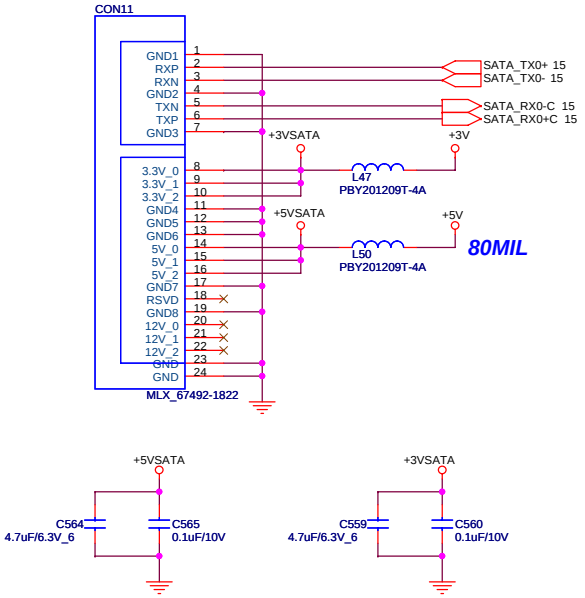
Quanta Computer Inc.

Size	Document Number	Rev
	MODEM(DAA)	1A
Date: Friday, September 28, 2007	Sheet 27 of 44	

ODD CONNECTOR



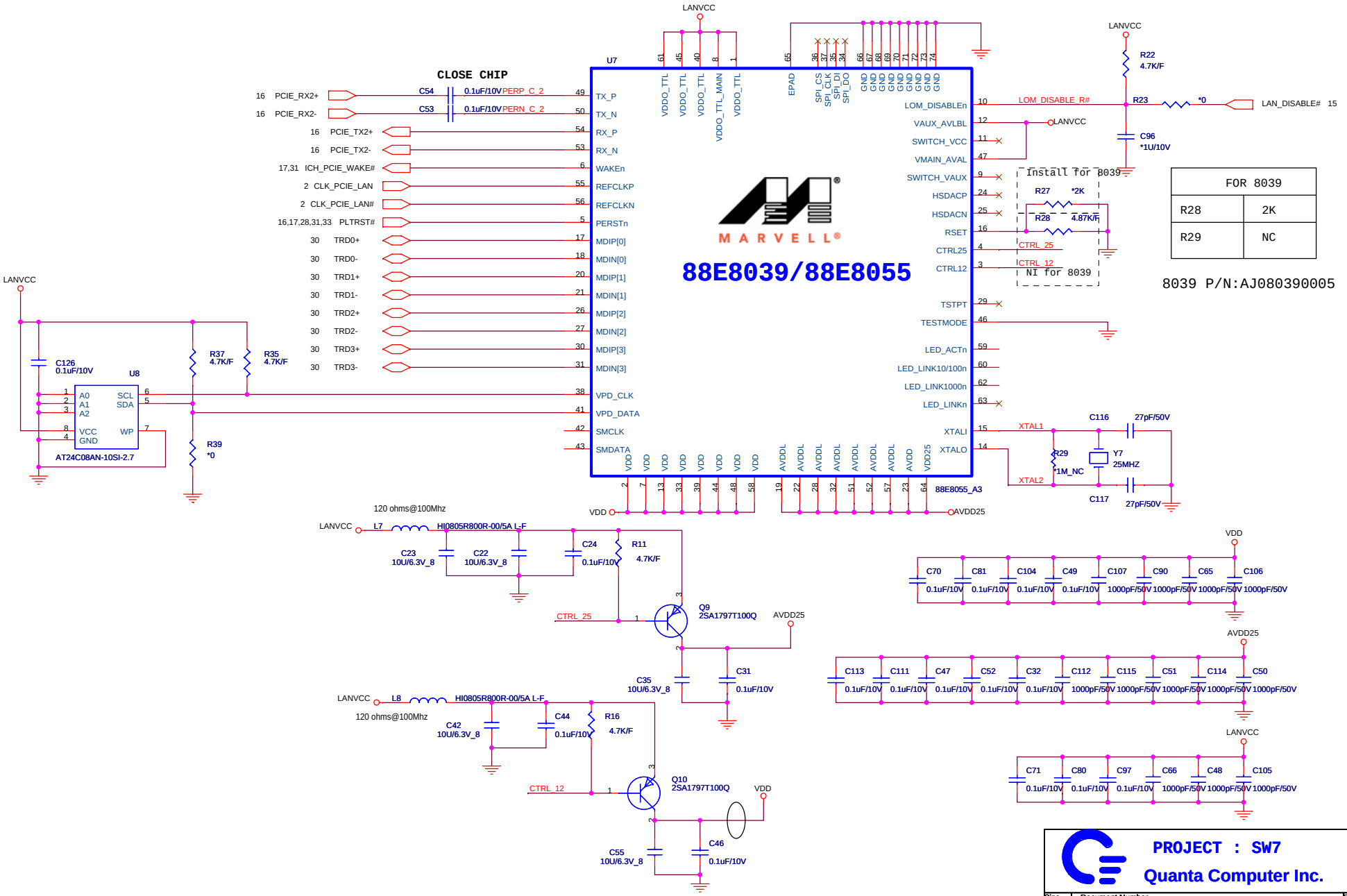
SATA Connector.



PROJECT : SW7

Quanta Computer Inc.

Size	Document Number	Rev
	SATA HDD/CD-ROM	1A
Date: Friday, September 28, 2007	Sheet 28 of 44	



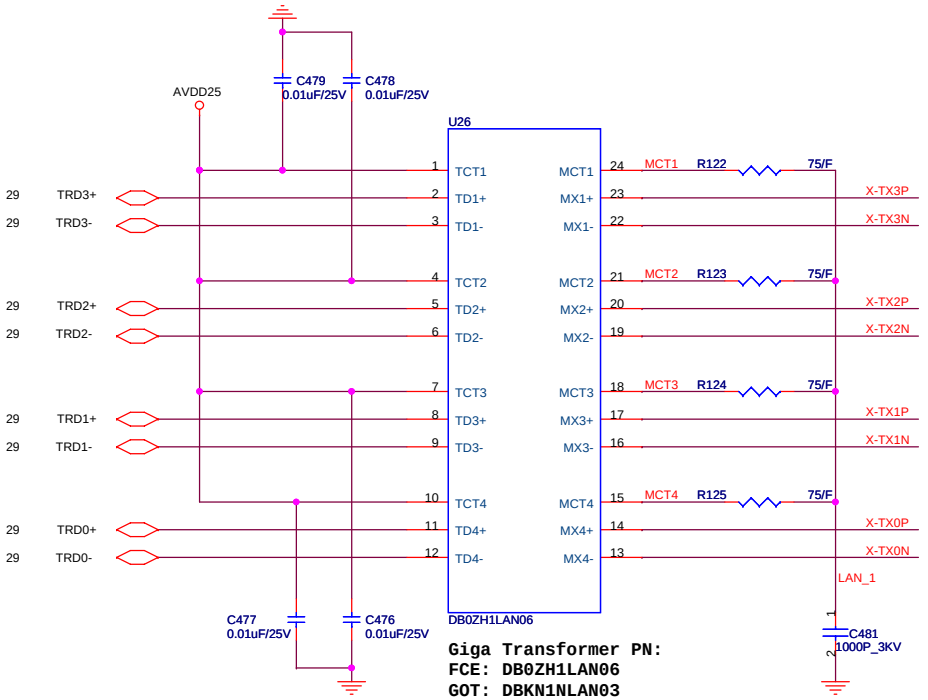
FOR 8039	
R28	2K
R29	NC

8039 P/N:AJ080390005

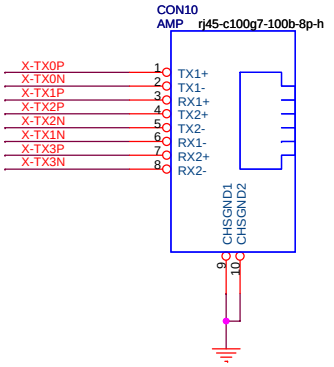
PROJECT : SW7

Quanta Computer Inc.

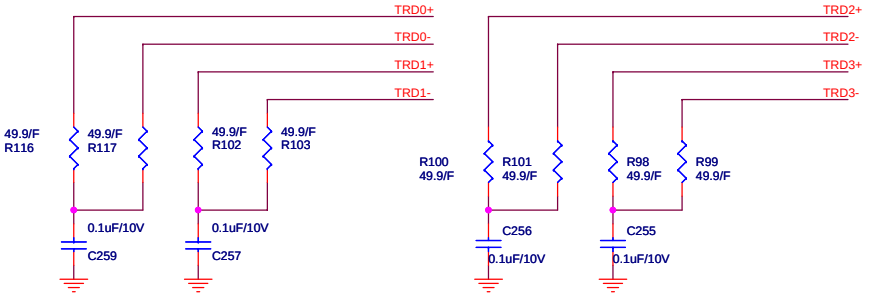
Size	Document Number	Rev
	MARVELL 8039/8055	1A
Date: Friday, September 28, 2007	Sheet 29 of 44	



Giga Transformer PN:
FCE: DB0ZH1LAN06
GOT: DBKN1NLAN03
HYT: DB0MW1LAN17



10/100 Transformer PN:
FCE: DBED2LLAN05
BOT: DB0TW3LAN12

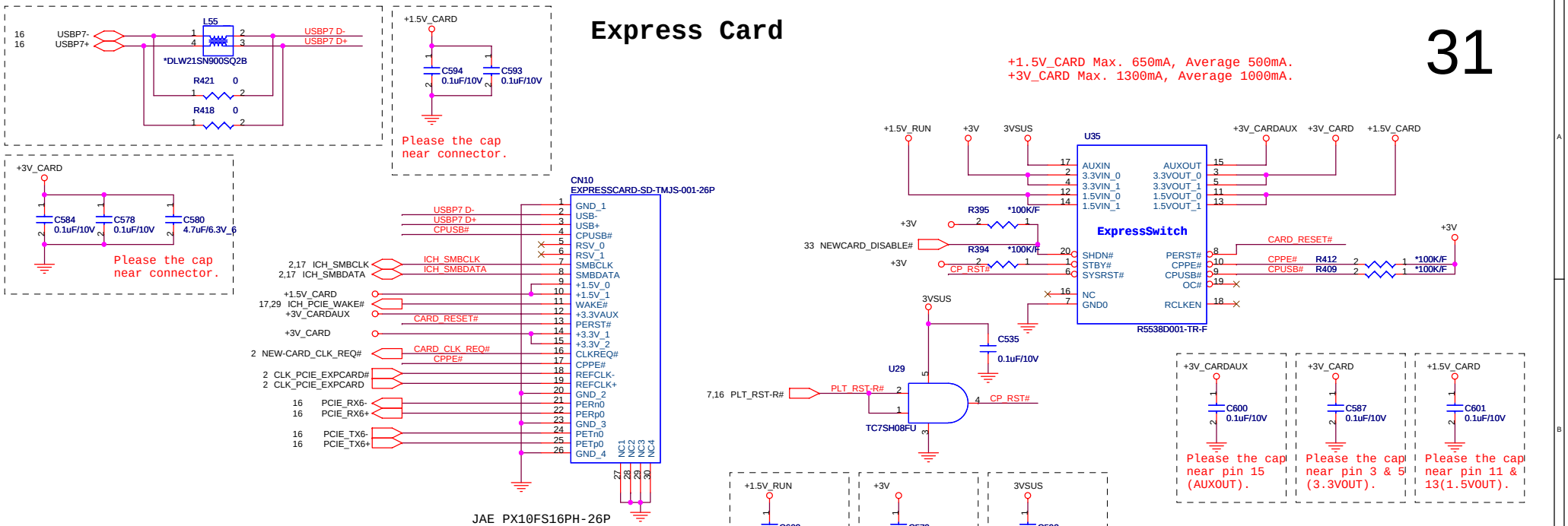


PROJECT : SW7
Quanta Computer Inc.

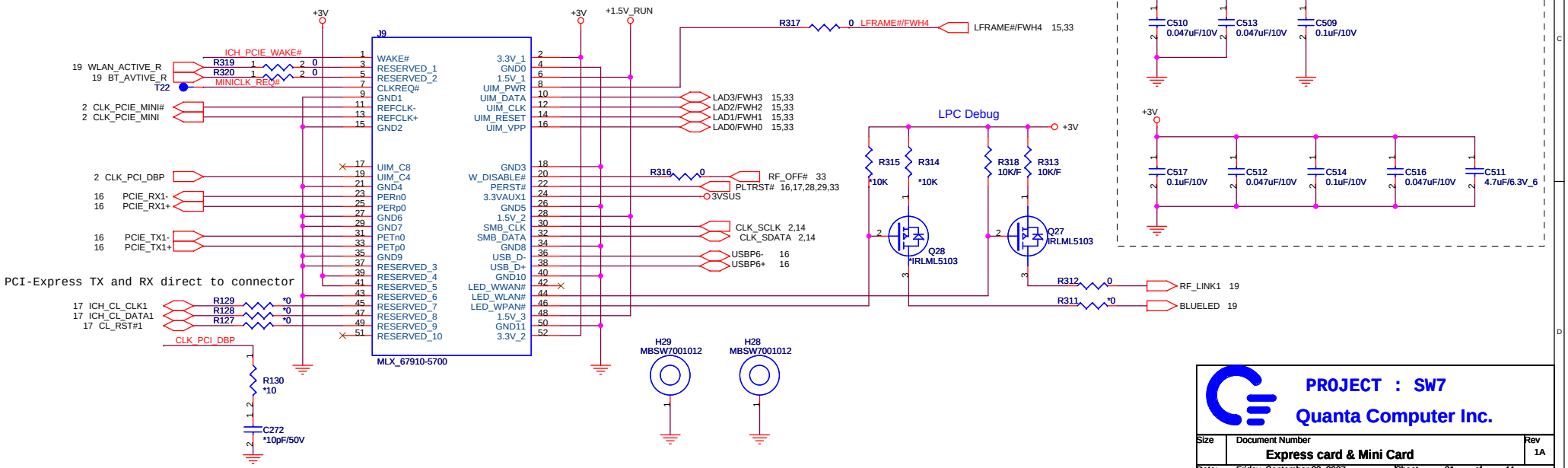
Size	Document Number	Rev
	LAN Transformer & Conn.	1A
Date: Friday, September 28, 2007	Sheet 30 of 44	

Express Card

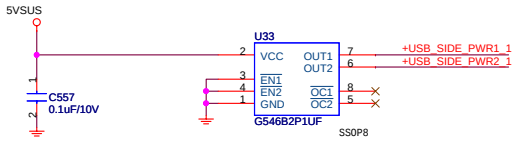
+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.



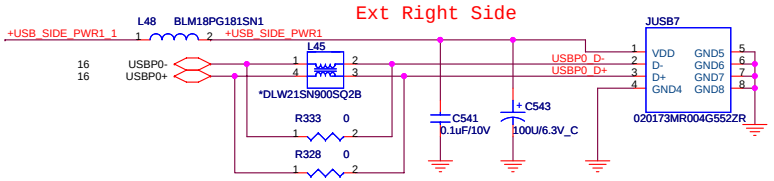
MiniCard WLAN connector

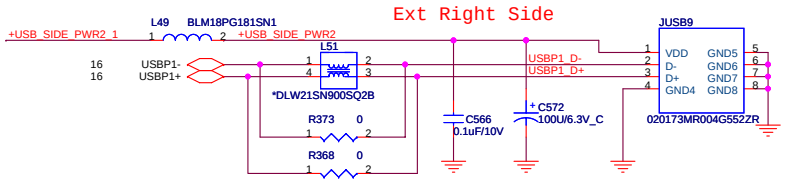


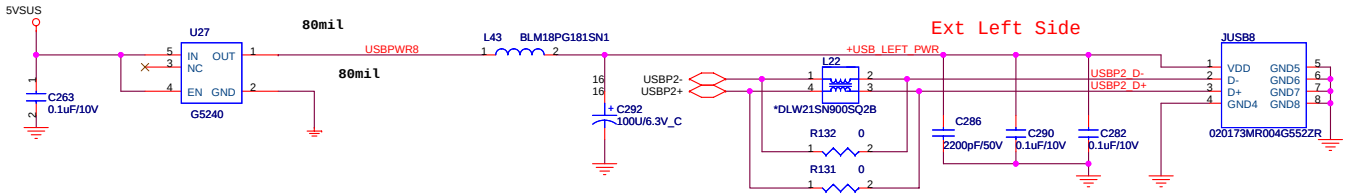
PROJECT : SW7		
Quanta Computer Inc.		
Size	Document Number: Express card & Mini Card	Rev: 1A
Date: Friday, September 28, 2007	Sheet 31 of 44	



2nd source AL002062005.

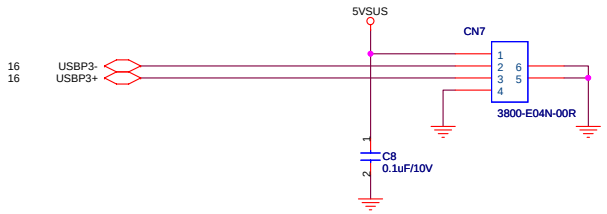






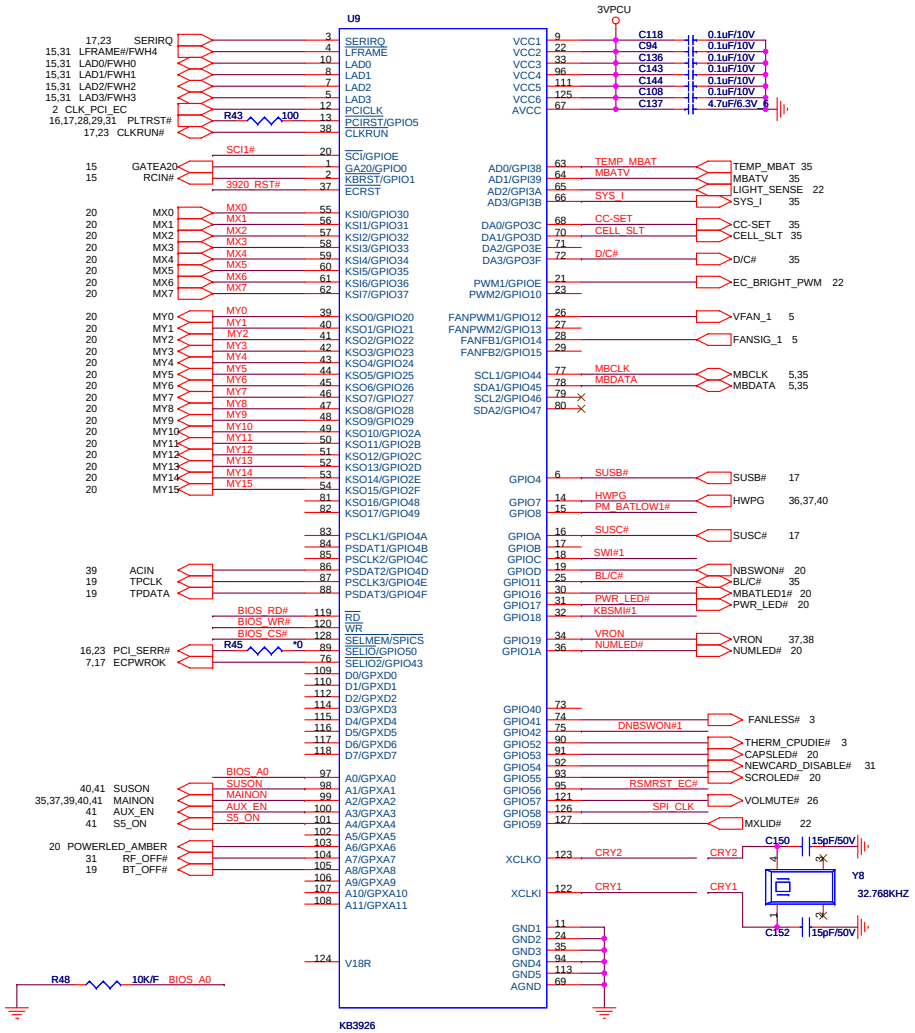
USB Con.
1st PN: DFHS04FR920(SUY)
2nd PN: DFHS04FRB11(AOP)

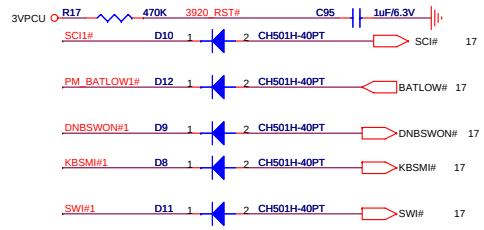
Int USB Con.
1st PN: DFHD04MR876(EIC)
2nd PN: DFHD04MR981(PTI)

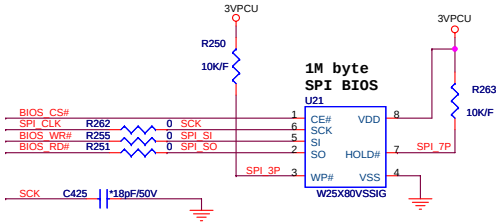


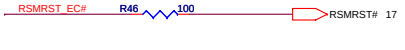
PROJECT : SW7
Quanta Computer Inc.

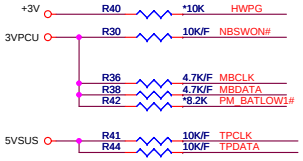
Size	Document Number	Rev
	USB PORTS	1A
Date: Friday, September 28, 2007	Sheet 32 of 44	











PROJECT : SW7		
Quanta Computer Inc.		
Size	Document Number	Rev
	KB3926/ROM	1A
Date: Friday, September 28, 2007	Sheet 33 of 44	

H18 *H-TE335X276BC316D236P2
H23 *HOLE-h-c276d118p2
H13 *HOLE-h-c315d118p2
H17 *h-te332x365bc330d118p2
H22 *H-h-te335x276bc276d118p2
AGND

H12 *H-C294D191X163P2-8
H11 *H-C296D163P2-8
H14 *h-tc294bc185d185p2-8
H15 *H-C296D185P2-8
H10 *HOLE-h-c315d118p2
H20 *H-TC138BC177D87P2

H21 *HOLE-h-tc217bc276d118p2
H7 *HOLE-h-c197d110p2
H19 *HOLE-h-c315d118p2
H16 *h-tc291bc315d236p2-8
H9 *HOLE-h-te331be236x181d118x181p2
H30 MBSW7001012
MTH7
H24 *h-c165d165n
GND
H25 *h-c315d118p2
H8 MBSW7002010

MCH

FAN

H26 MBSW1002017
H27 MBSW1002017

3VSUS
C533 4700P/25V

+3V
C585 4700P/25V
C567 4700P/25V

+3V
C526 4700P/25V
C548 4700P/25V
C596 4700P/25V

VIN
C12 0.1uF/50V_6
C141 0.1uF/50V_6
C43 0.1uF/50V_6
C21 0.1uF/50V_6
C370 0.1uF/50V_6
C45 0.1uF/50V_6
C25 0.1uF/50V_6
C93 0.1uF/50V_6
C145 0.1uF/50V_6
C206 0.1uF/50V_6

Place along VIN power plane for EMI.

PV20 EMI_SU_27G
PV18 EMI_SU_27G
PV19 EMI_SU_27G
PV17 EMI_SU_27G
GND

瞨紮

PV16 *PAD197X98_NC
PV15 *PAD197X98_NC
PV21 *PAD197X98_NC
PV7 EMI_504025-N7
GND

PV8 *EMI_2520-N1_NC
PV9 *EMI_2520-N1_NC
PV13 FDSW1003015
GND

PV12 FDSW1003015
PV14 FDSW1003015
PV11 FDSW1003015
PV10 EMI_2520-N1
GND

EMI

5VPCU
C91 0.1uF/10V
C139 0.1uF/10V
C614 0.1uF/10V
C92 1000pF/50V
C140 1000pF/50V
C615 1000pF/50V
C271 0.1uF/10V
C270 1000pF/50V

+3V
C127 0.1uF/10V
C109 0.1uF/10V
C68 0.1uF/10V
C69 1000pF/50V
C372 1000pF/50V
C110 1000pF/50V
C41 0.1uF/10V

3VPCU
C396 0.1uF/10V
C412 0.1uF/10V
C142 0.1uF/10V
C138 1000pF/50V
C597 1000pF/50V

5VSUS
C277 0.1uF/10V
C268 0.1uF/10V
C280 1000pF/50V
C264 1000pF/50V
C267 1000pF/50V

EMI for DDR DIMM.

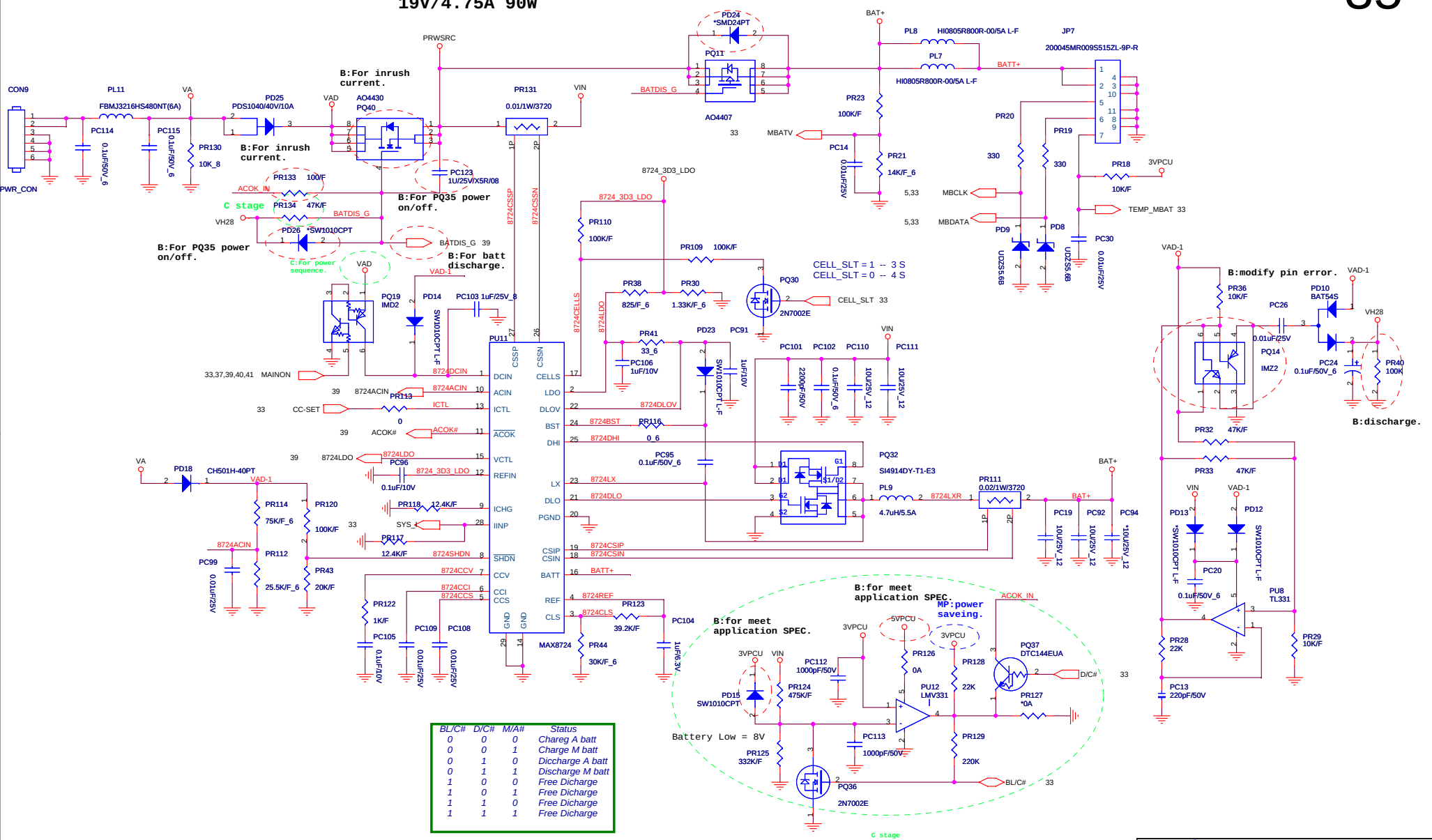
+1.8VSUS
C403 4700P/25V
C146 4700P/25V
C404 4700P/25V
C402 4700P/25V
C147 4700P/25V
C159 4700P/25V
C401 4700P/25V
C158 4700P/25V
C406 4700P/25V
C400 4700P/25V

+1.8VSUS
C185 4700P/25V
C26 4700P/25V

PROJECT : SW7
Quanta Computer Inc.

Size	Document Number	Rev
	Screw Holes & EMI	1A
Date: Friday, September 28, 2007	Sheet 34 of 44	

Adapter:19V/3.45A 65W
19V/3.95A 75W
19V/4.75A 90W



BL/C#	D/C#	M/A#	Status
0	0	0	Chareg A batt
0	0	1	Charge M batt
0	1	0	Diccharge A batt
0	1	1	Discharge M batt
1	0	0	Free Dicharge
1	0	1	Free Dicharge
1	1	0	Free Dicharge
1	1	1	Free Dicharge

PROJECT : SW7

Quanta Computer Inc.

Size	Document Number	Rev
	SYSTEM CHARGER (MAX8724)	1A

Date: Friday, September 28, 2007 Sheet 35 of 44

DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+12V_ALW

I_lim*MOSFET(RDSON)=V_ILIM(mV)/10

V_ILIM(mV)=5uA*R_ILIM

5VPCU
0.02A
OCP=12A

Vout=0.7(Ra+Rb)/Rb

Rb around 49.9k

3VPCU
0.06A
OCP=12A

TOPN: OUT1/OUT2
GND=400KHz/500KHz
REF = 400KHz /300KHz
VCC5=200KHz/300KHz

B:for OCP.

Rds(on) 16m ohm

B:for cost down.

B:for timing.

5V_S5
0.01A
S0-S5

SECFB -2V

LANVCC
0.7A
S0-S5

3V_S5
0.07A
S0-S5

+5V
6.14A
S0-S1

5VSUS
1.74A
S0-S3

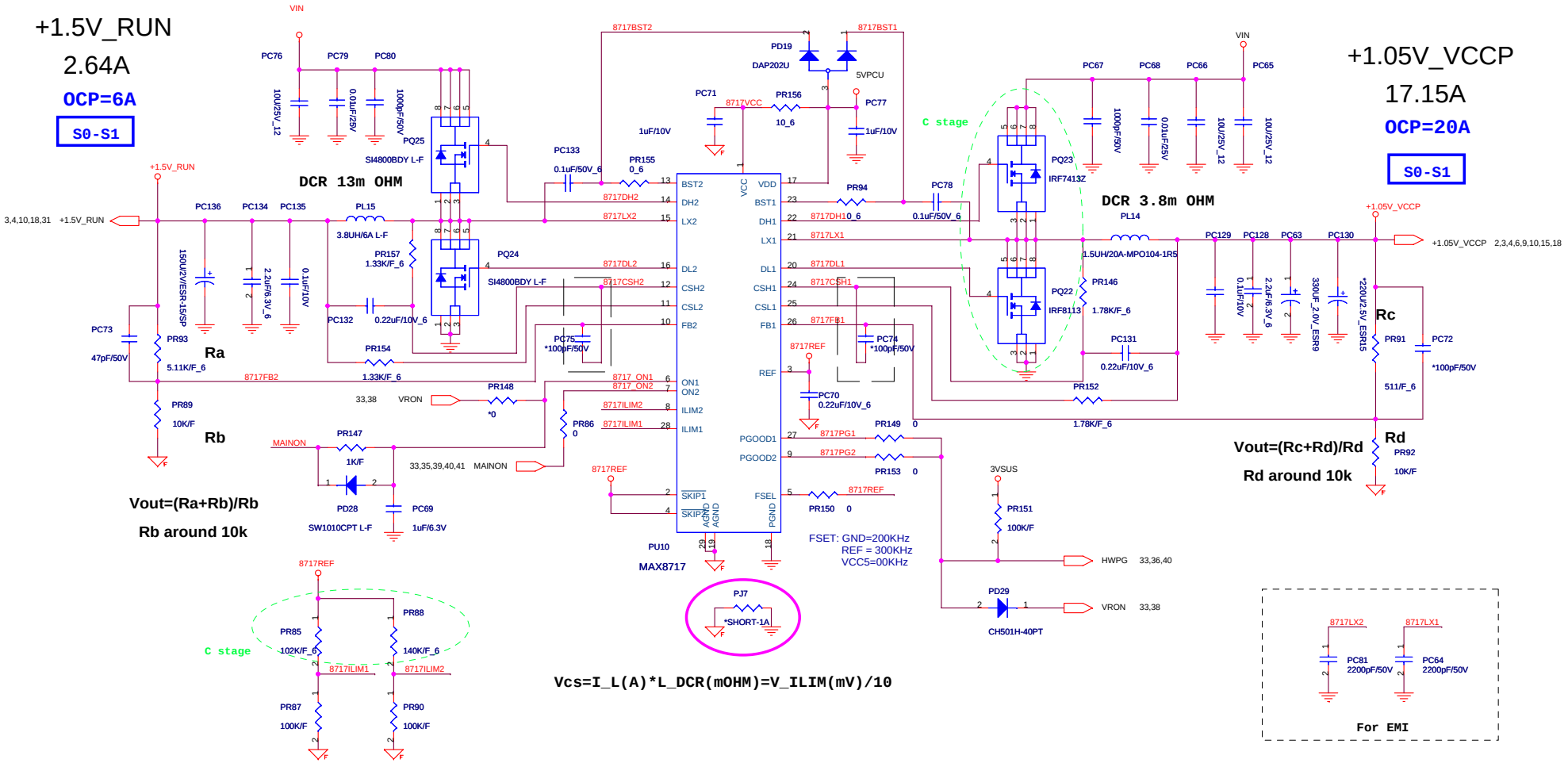
+3V
6.57A
S0-S1

3VSUS
0.48A
S0-S3

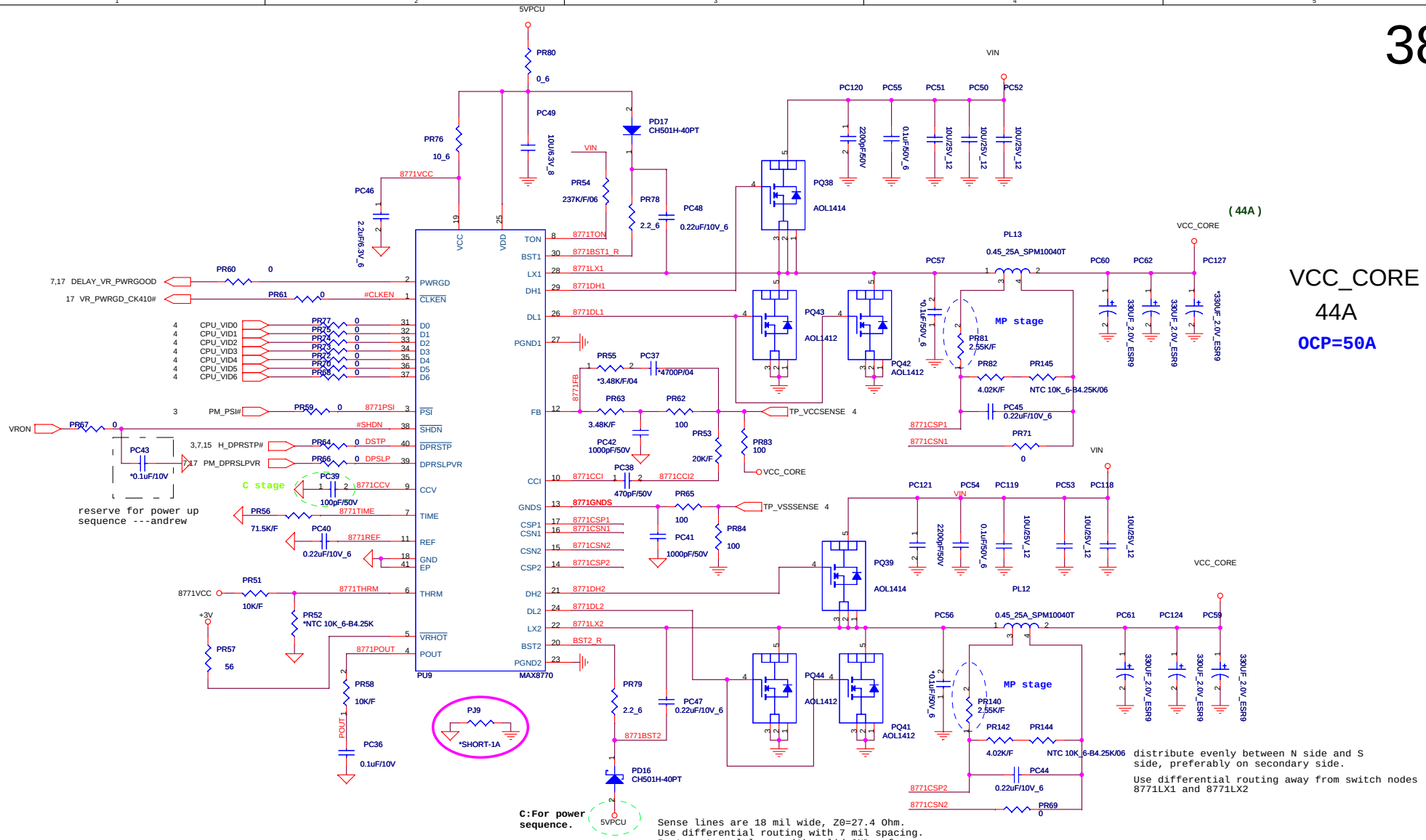
PROJECT : SW7			
Quanta Computer Inc.			
Size	Document Number		Rev
	5V/3V/+12V_ALW(MAX8778)		1A
Date: Friday, September 28, 2007		Sheet 36 of 44	

+1.5V_RUN
2.64A
OCP=6A
S0-S1

+1.05V_VCCP
17.15A
OCP=20A
S0-S1



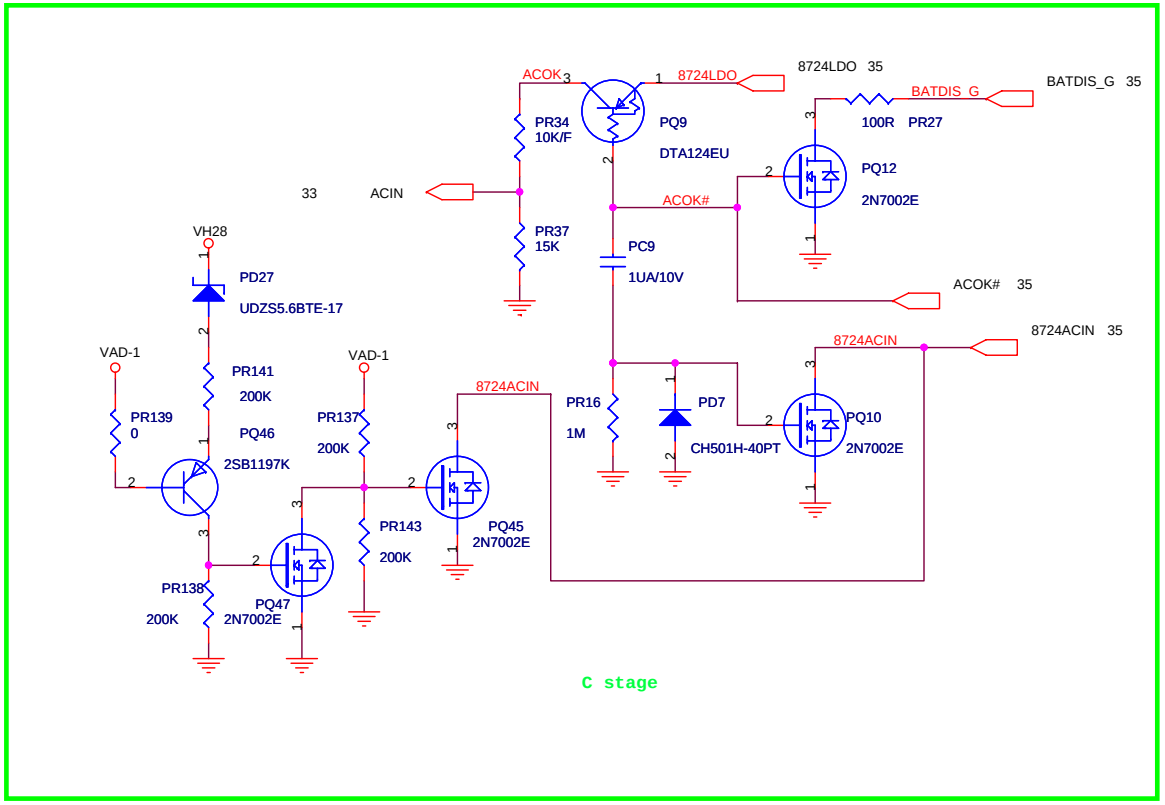
PROJECT : SW7		
Quanta Computer Inc.		
Size	Document Number	Rev
	+1.5V_RUN/+1.05V_VCCP (MAX8717)	1A
Date: Friday, September 28, 2007	Sheet 37 of 44	

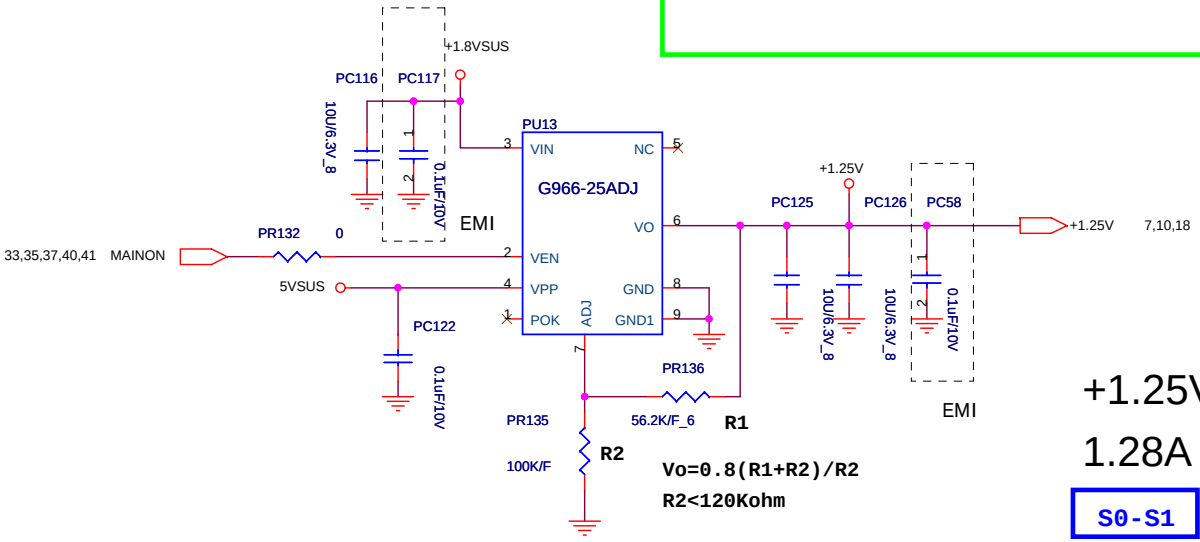


VCC_CORE
44A
OCP=50A

PROJECT : SW7
Quanta Computer Inc.

Size	Document Number	Rev
	VCC_CORE(MAX8770)	1A
Date: Friday, September 28, 2007	Sheet 38 of 44	





+1.25V

1.28A

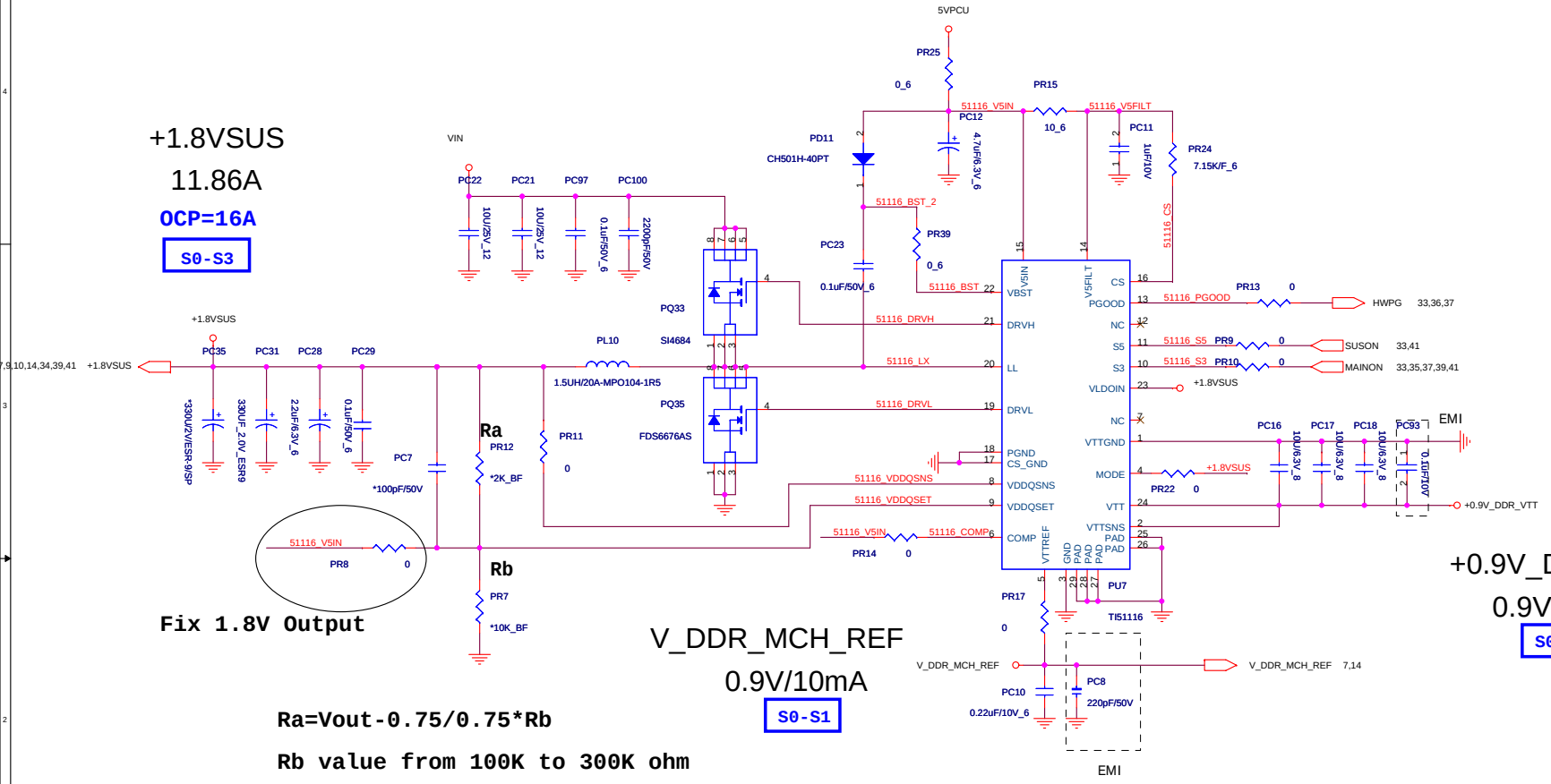
S0-S1

PROJECT : SW7

Quanta Computer Inc.

Size	Document Number	Rev
	+1.25V&+2.5V	1A
Date: Friday, September 28, 2007	Sheet 39 of 44	

+1.8VSUS
11.86A
OCP=16A
S0-S3



Fix 1.8V Output

V_DDR_MCH_REF
0.9V/10mA
S0-S1

+0.9V_DDR_VTT
0.9V/10mA
S0-S1

Ra=Vout-0.75/0.75*Rb

Rb value from 100K to 300K ohm

Mode	Discharge Mode
V5IN	No discharge
VDDQ	Tracking discharge
Gnd	Non-tracking discharge

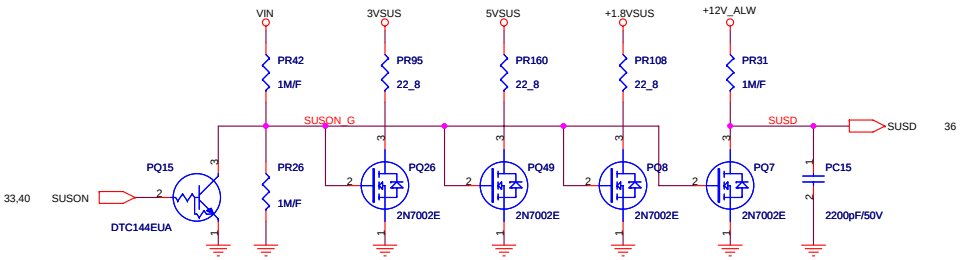
V_TRIP(mV)=R_TRIP(Kohm)*10(uA)
I_OCP=V_trip/Rds_on+I_Ripple/2

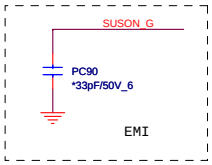
VDDQSET	VDDQ(V)	VTTREF and Vtt	Note
GND	2.5	V_ vddqsns/2	DDR
V5IN	1.8	V _vddqsns/2	DDR2
FB	adjustable	V_VDDQSNS/2	1.5V<VDDQ<3V

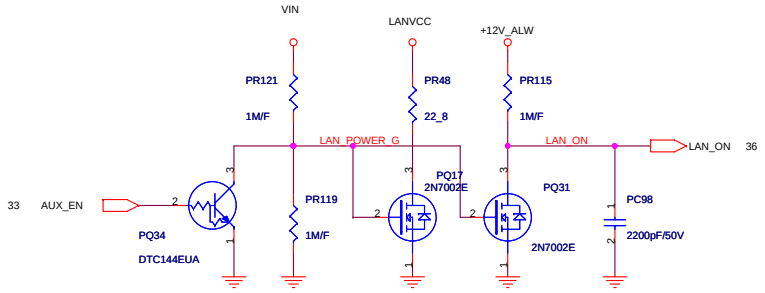
PROJECT : SW7
Quanta Computer Inc.

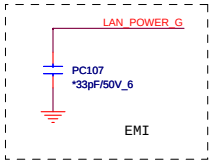
Size	Document Number	Rev
	DDRII +1.8VSUS/+0.9V_DDR_VTT	1A

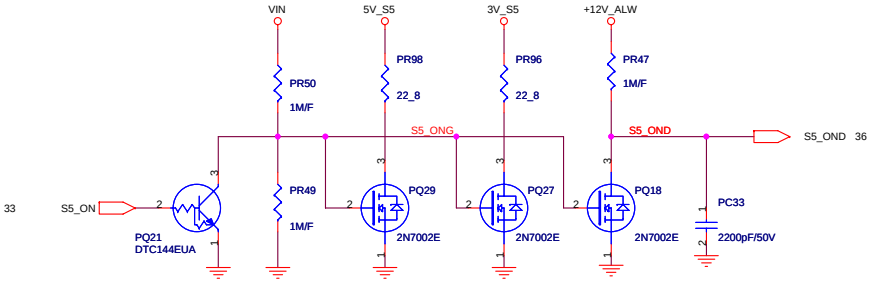
Date: Friday, September 28, 2007 Sheet 40 of 44

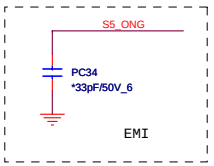


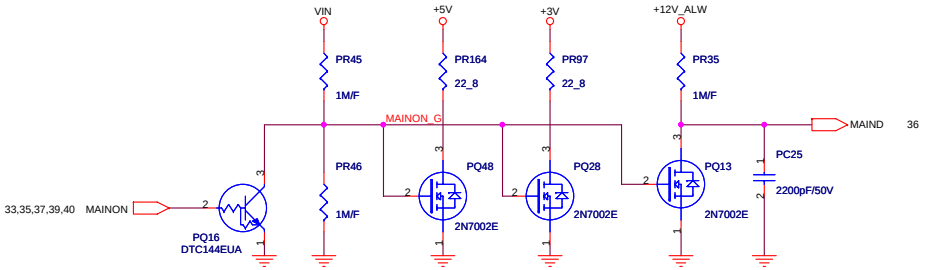


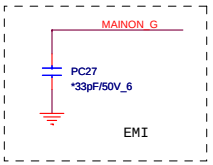












PROJECT : SW7

Quanta Computer Inc.

Size	Document Number	Rev
	DISCHARGE	1A

Date: Friday, September 28, 2007 Sheet 41 of 44