

Schematics Page Index (Title / Revision / Change Date)

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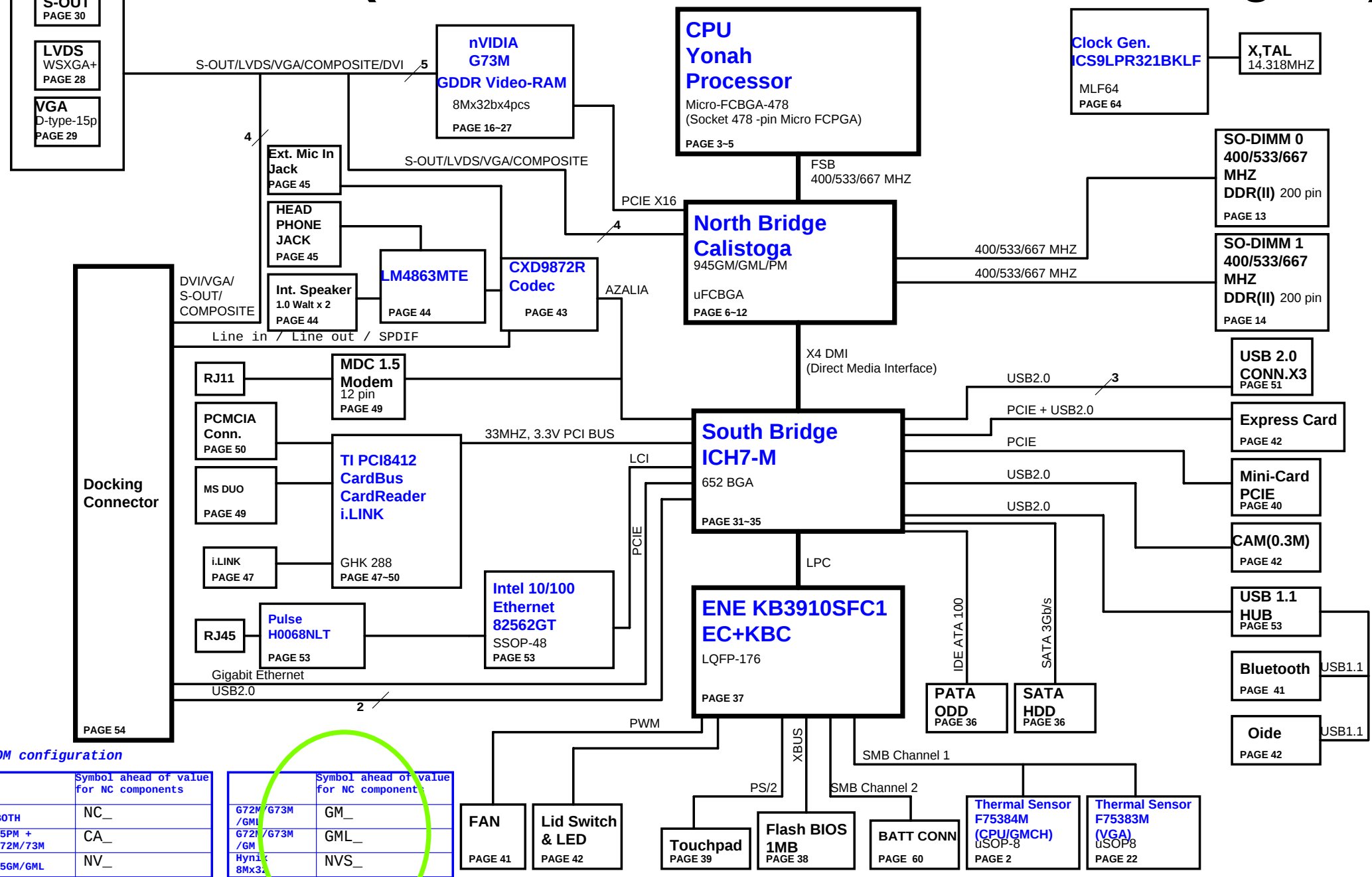
P. Leader	Check by	Design by

Project Code & Schematics Subject: MS13 Main Board

PCB P/N:	1P-0067100-8M11(FUBAI)
	1P-0067200-8M11(NAN YA)
	1P-0067500-8M11(HANSTAR)

FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title Index Page			
Size A3	Document Number MS13-1-01 (MBX-149)	Rev 1.0	
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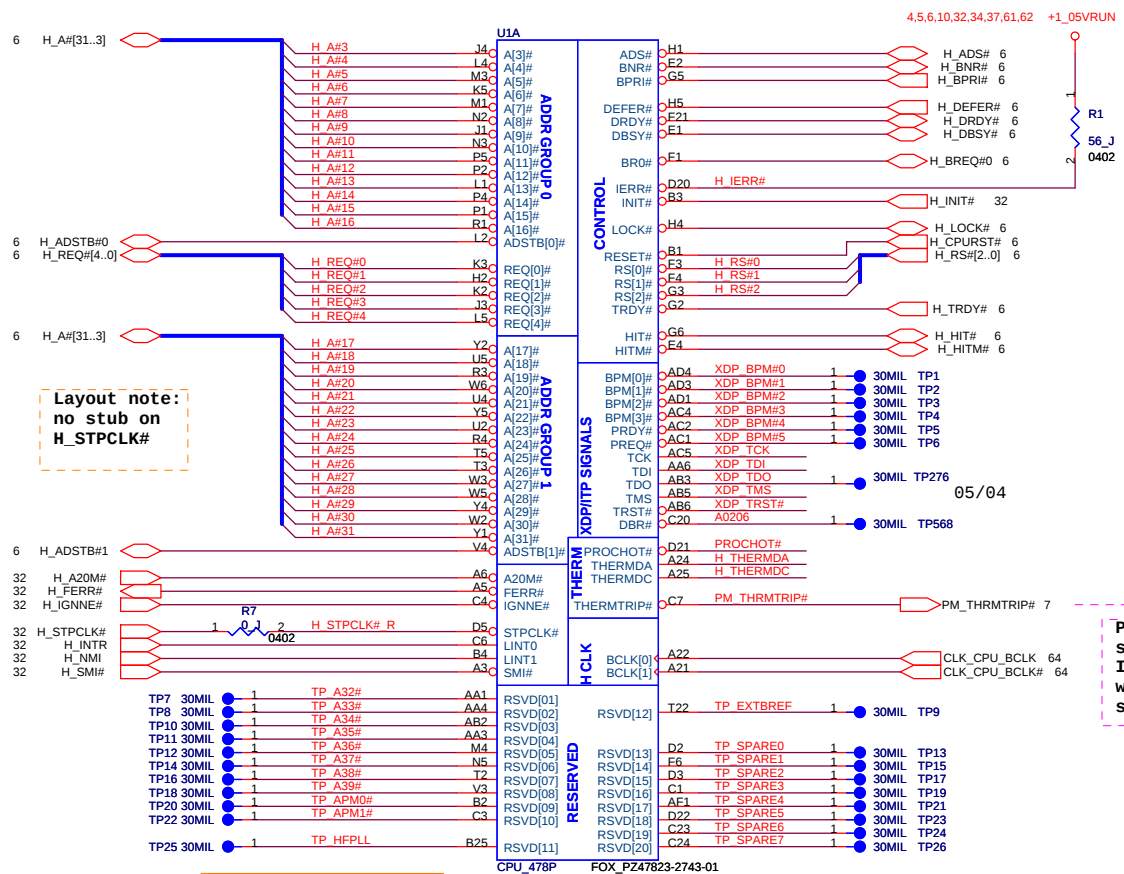
MBX-149(CALISTOGA PM/GM+Gfx Block Diagram)



BOM configuration

	Symbol ahead of value for NC components		Symbol ahead of value for NC components
BOTH	NC_	G72M/G73M /GML	GM_
G45PM + NV72M/73M	CA_	G72M/G73M /GML	GML_
G45GM/GML	NV_	Hynix 8Mx32	NVS_
G45PM+G72M or GM/GML	NV73_	G72M and Hynix 8Mx32	NV73S_
G45PM+G73M_A2 /G73M_B01 or GM/GML	NV72_		

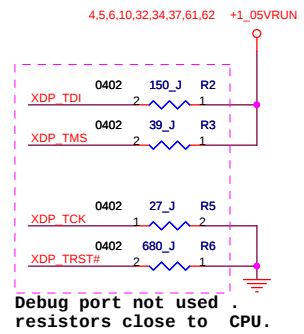
MS13 DVT Modify



Layout note:
no stub on
H_STPCLK#

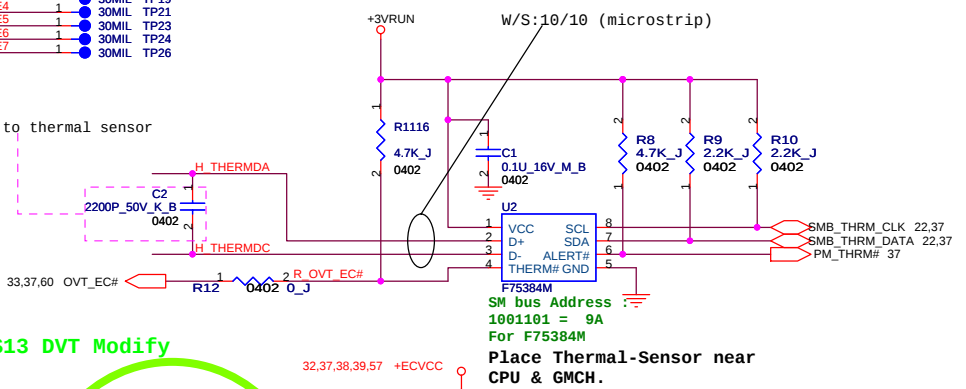
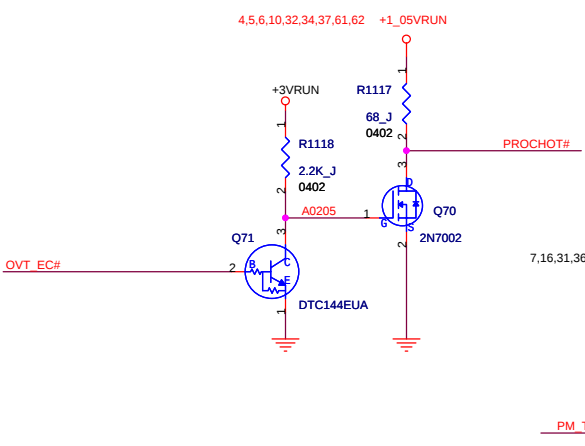
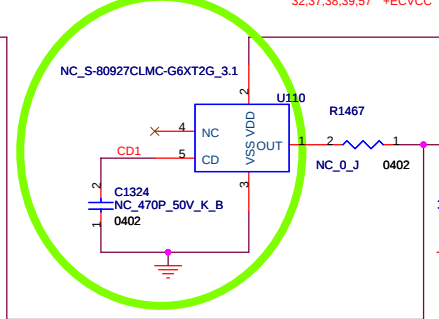
A#[32-39], APM#[0-1]:
Leave escape routing
on for future
functionality

ICH7M's GPIO12: VIL----> -0.5V ~ -0.8V
VIH----> 2.0V ~ 3.3+0.5V
YONAH's PROCHOT#: VIL----> -0.1V ~ -0.3*VCCP
VIH----> 0.7*VCCP ~ VCCP+0.1

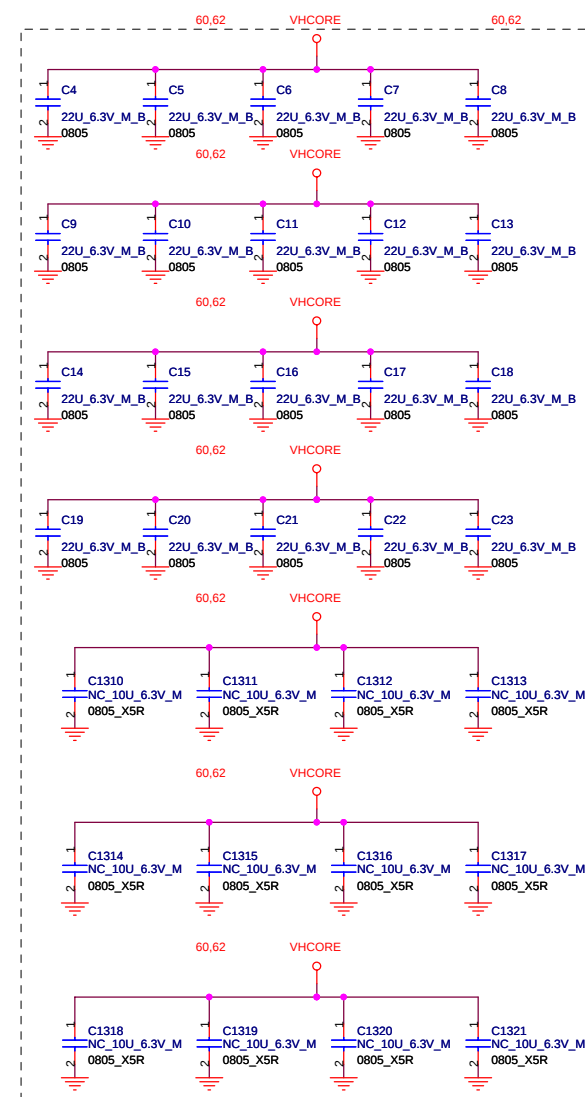


PM_THRMTRIP#
should connect to
ICH7-M and GMCH
without T-ing (No
stub)

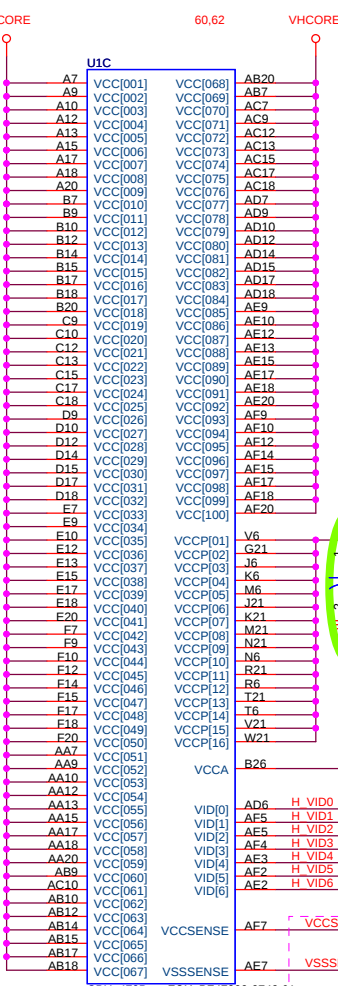
MS13 DVT Modify



When use U110, R15 and C3
need change to NC.

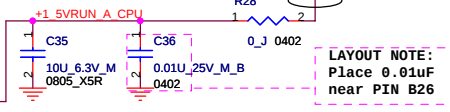
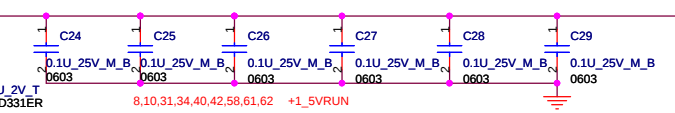
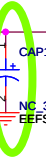


10uF *32 instead of 22uF*20 for 22uF 6.3V_0805 shortage



CPU_VCCA---->120mA
CPU_VCCP----->2.5A
CPU_VCC----->44A

MS13 DVT Modify

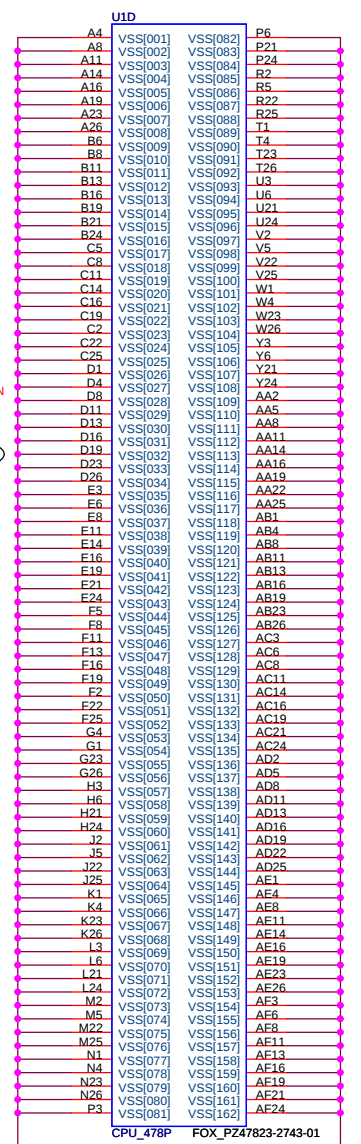


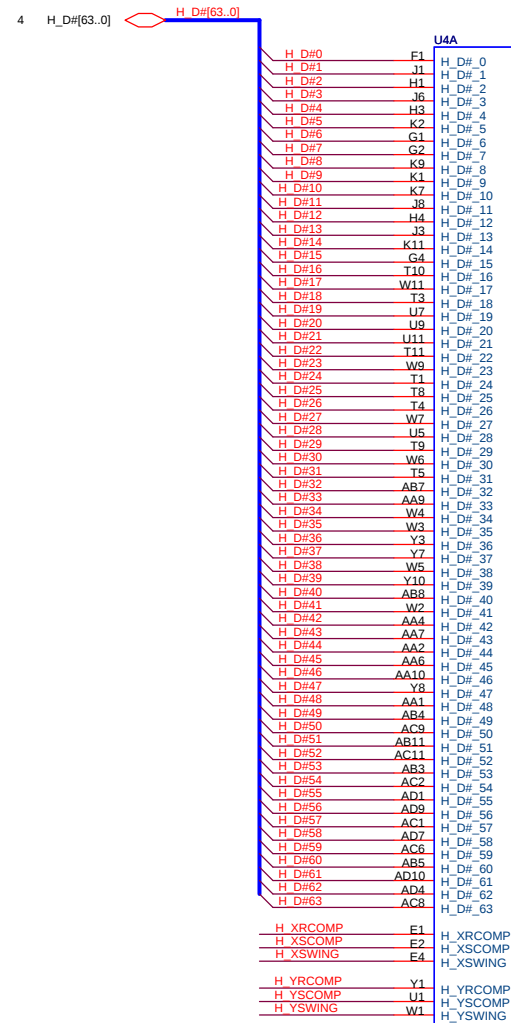
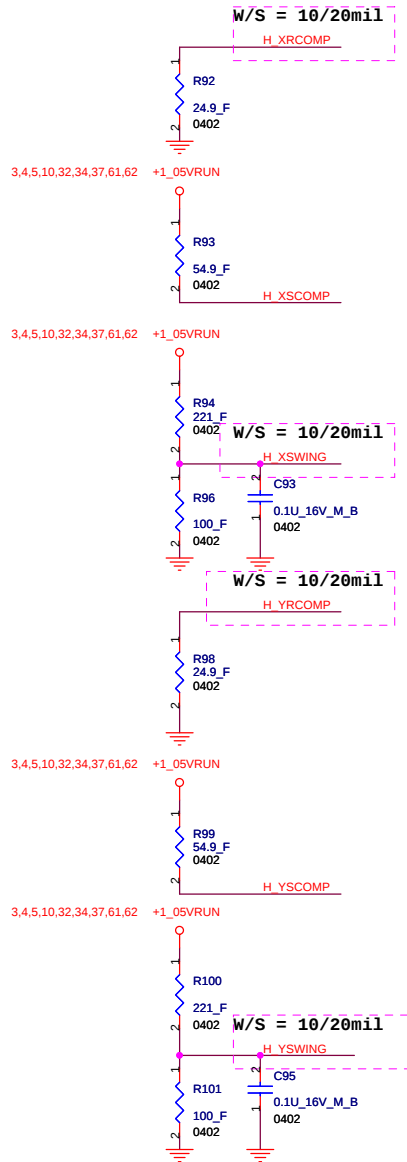
LAYOUT NOTE:
Place 0.01uF
near PIN B26

Same Length

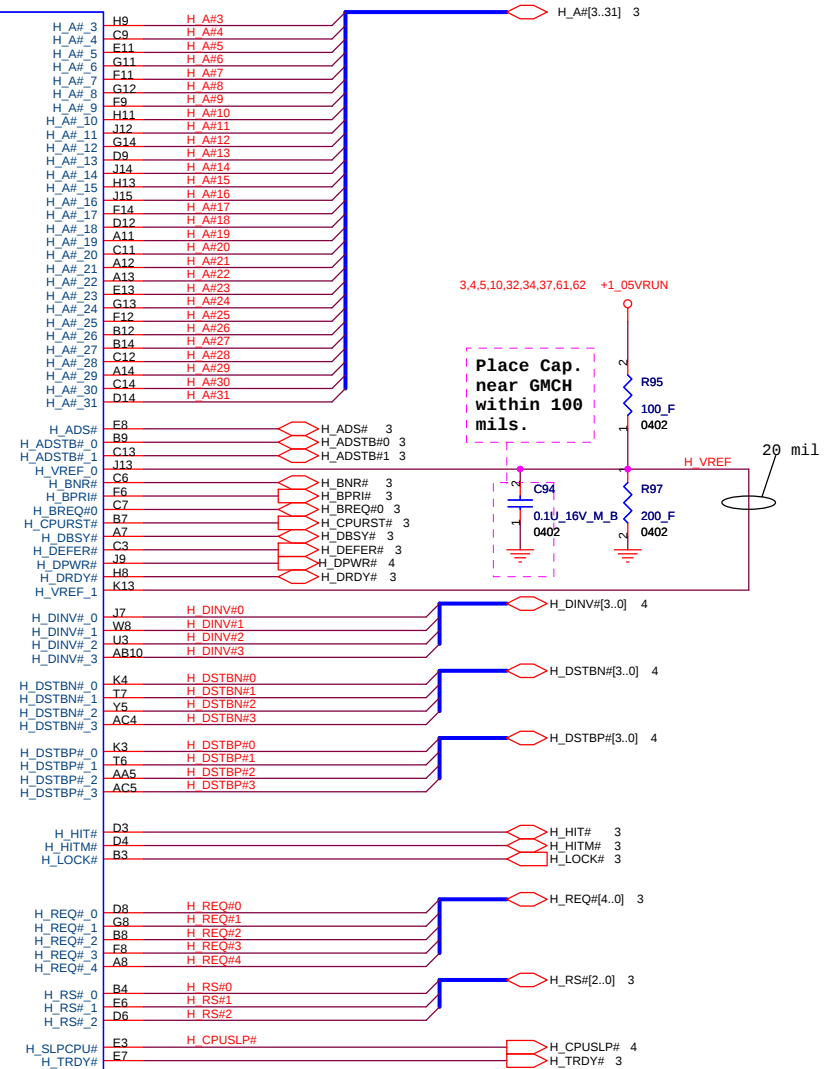
Layout Note: Route
VCCSENSE traces at 27.4
Ohms with 50 mil spacing.
Place PU and PD within 1
inch of cpu.

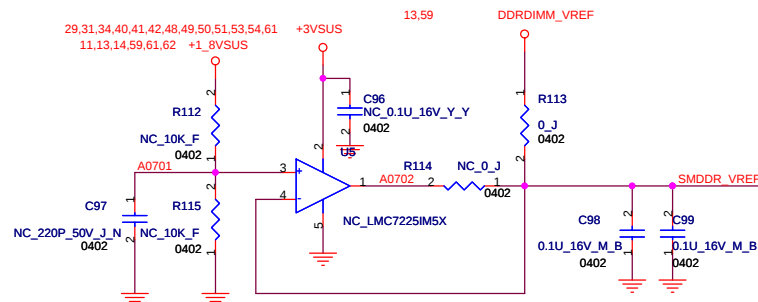
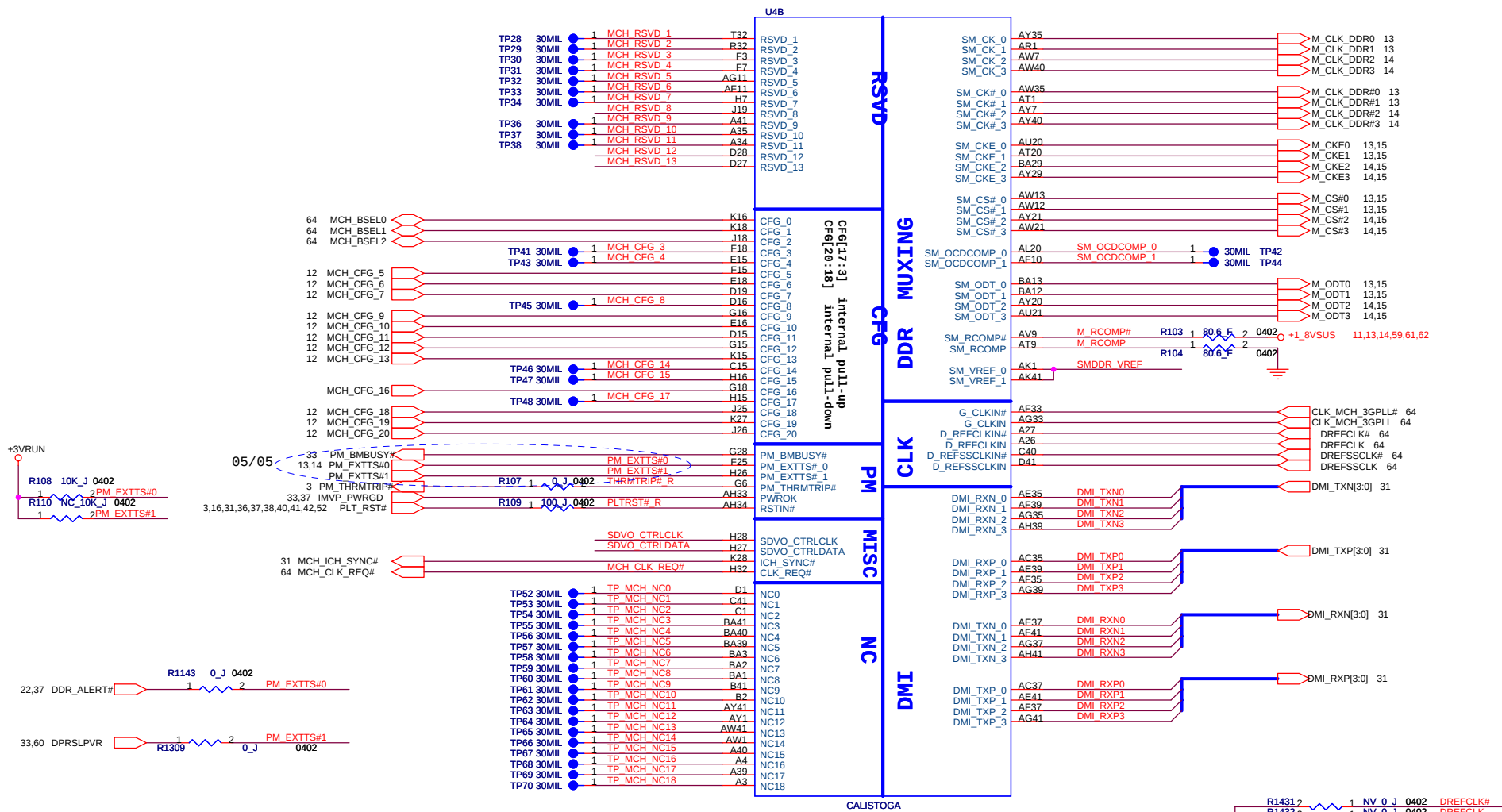
width=18 mil
spacing=7 mil

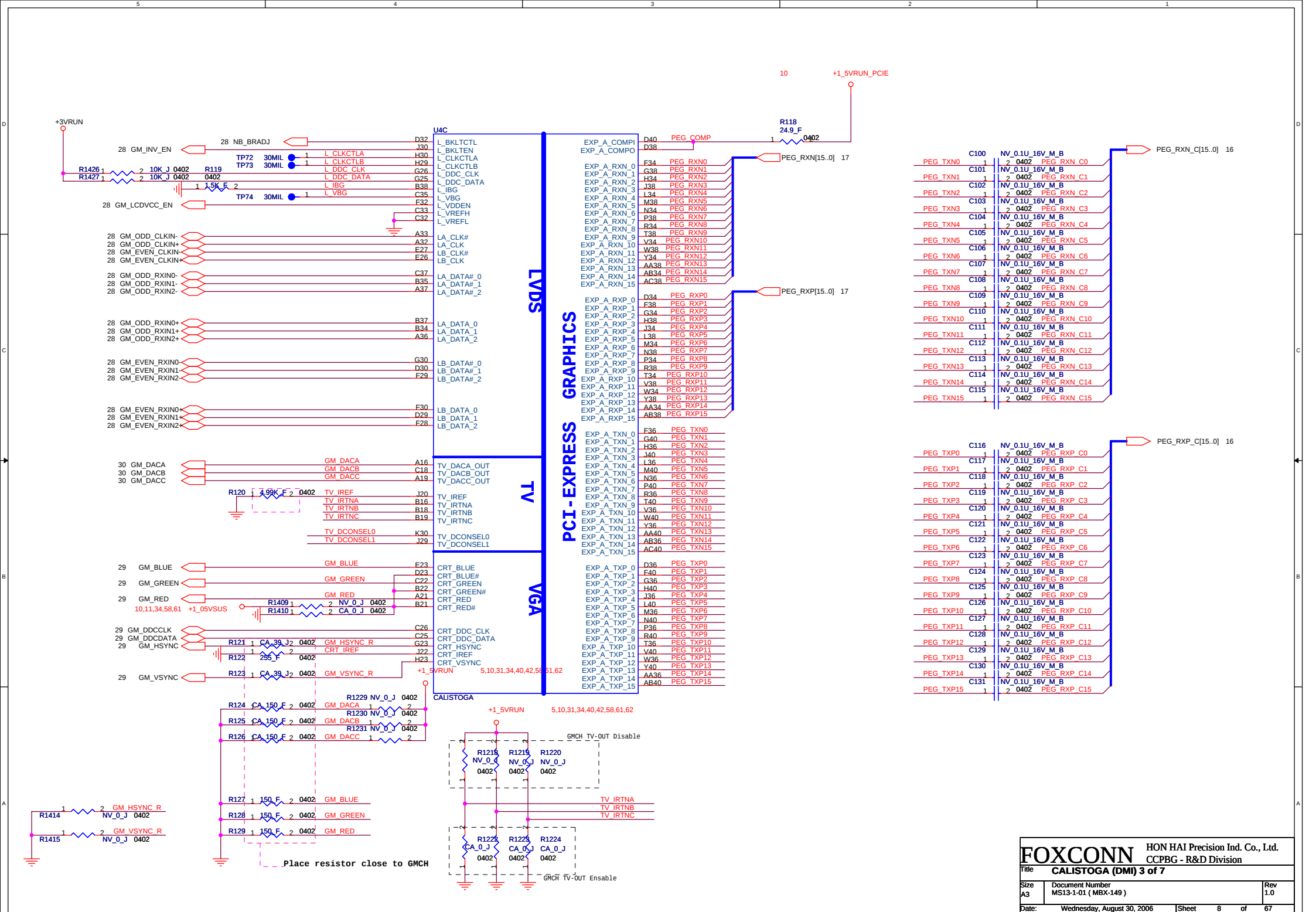


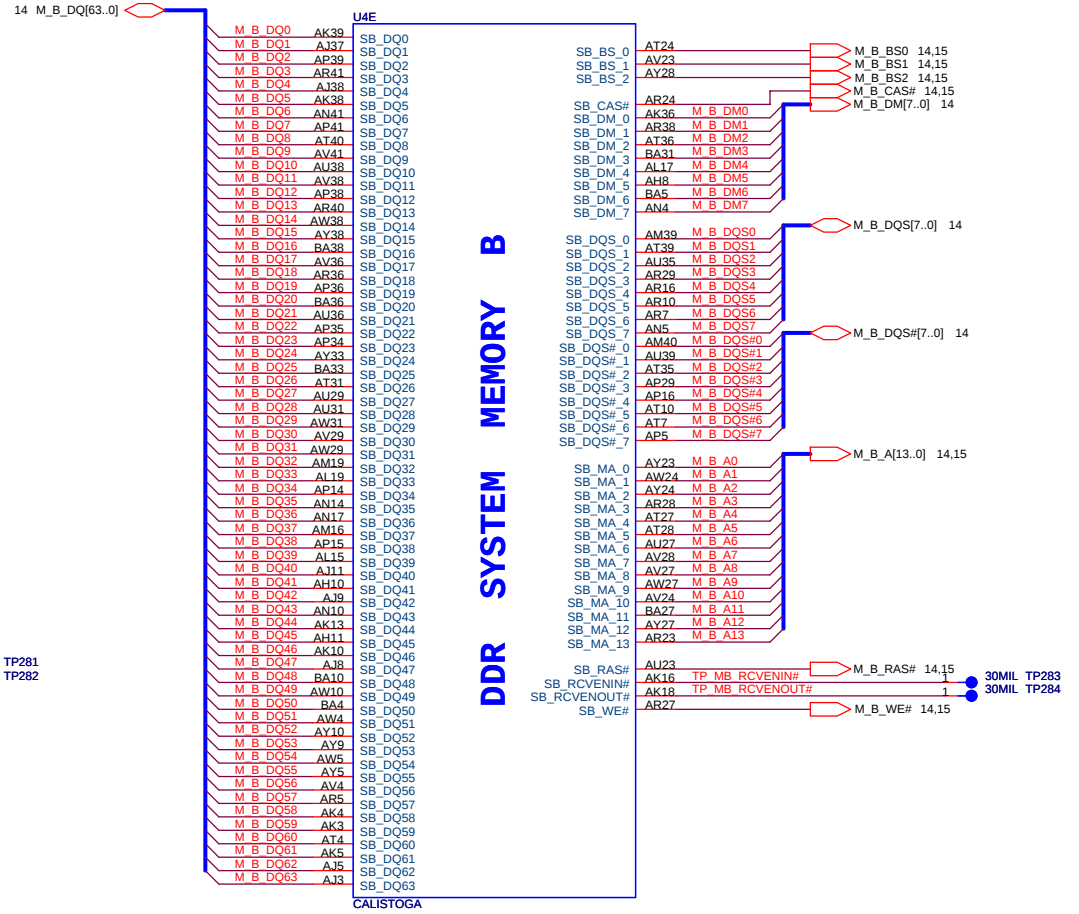
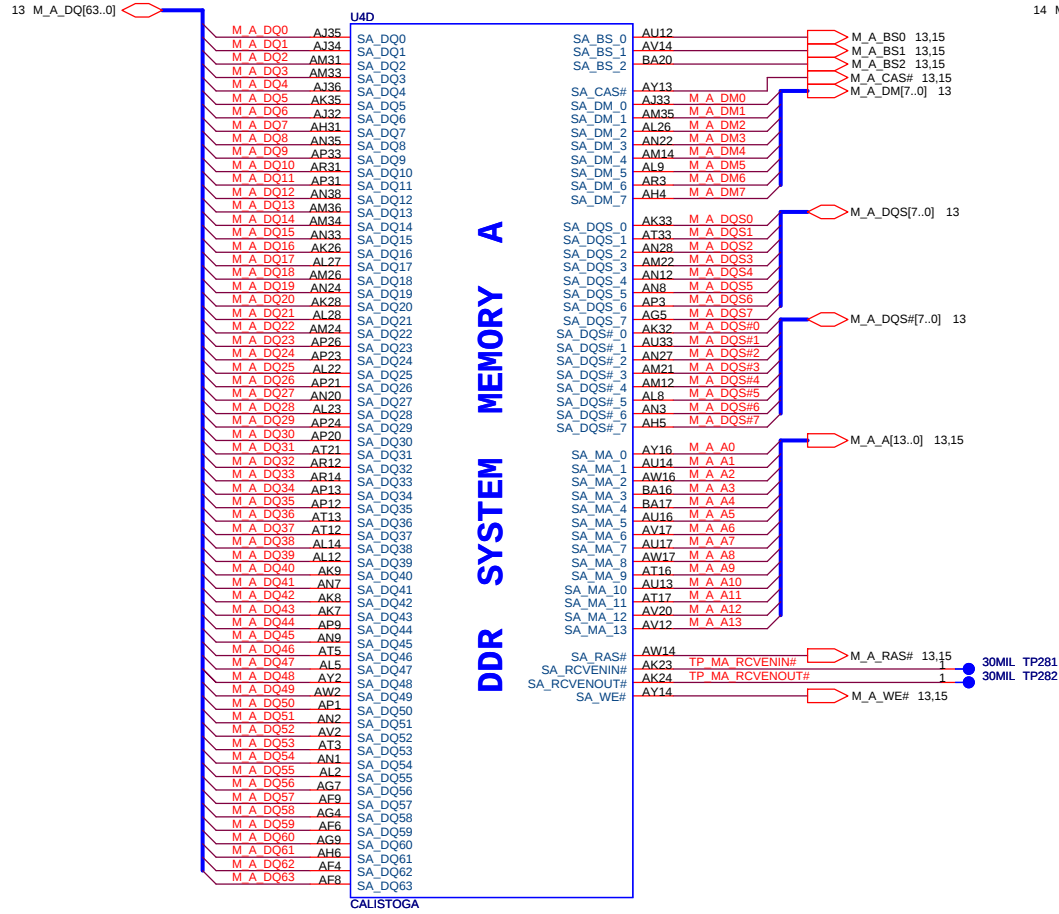


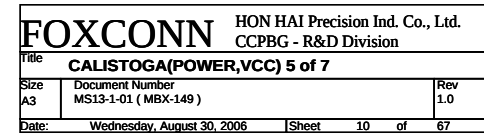
HOST











7 MCH_CFG_5 30MIL TP554

MCH_CFG_5
Low = DMIX2
High = DMIX4

MCH_CFG_18
(VCC_CORE Select)
Low = 1.05V(default)
High = 1.5V

7 MCH_CFG_18 30MIL TP555

7 MCH_CFG_6 30MIL TP556

MCH_CFG_6
Low = Moby Dick
High = Calistoga
DDR2 select (default high)

MCH_CFG_19
(DMI LANE REVERSAL)
Low = Normal(default)
High = LANES REVERSED

7 MCH_CFG_19 30MIL TP558

7 MCH_CFG_7 30MIL TP557

MCH_CFG_7
(CPU Strap)
Low = RSVD
High = Mobile Yonah processor

MCH_CFG_20
(PCIe Backward Interpoerability mode)
Low = Only SDVO or PCIE x1 is operational (defaults)
High = SDVO and PCIE x1 are operating simultaneously via the PEG port

7 MCH_CFG_20 30MIL TP561

7 MCH_CFG_9 30MIL TP559

MCH_CFG_9
(PCIe Graphics Lane)
Low = Reverse Lane
High = Normal operation

For layout convenience

7 MCH_CFG_10 30MIL TP560

MCH_CFG_10
(HOST PLL VCC SELECT)
Low = RESERVED
High = MOBILITY

Layout Noe:
Location of all MCH_CFG strap resistors needs to be close to trace to minimize stub

7 MCH_CFG_11 30MIL TP562

MCH_CFG_11
(PSB 4x CLK ENABLE)
Low = Calistoga
High = Reserved

R162
NC_2.2K_J
0402

7 MCH_CFG_12 30MIL TP562

7 MCH_CFG_13 30MIL TP563

MCH_CFG [13:12]
(XOR/ALLZ)
00=Partial Clock Gating Disable
01=XOR Mode Enable
10=All-Z Mode Enable
11=Normal Operation(Default)

7 MCH_CFG_16 30MIL TP563

MCH_CFG_16
(FSB Dynamic ODT)
Low = Dynamic ODT Disabled
High = Dynamic ODT Enable

U4I
AC41 VSS_0
AA41 VSS_1
WA1 VSS_2
TA1 VSS_3
PA1 VSS_4
MA1 VSS_5
JA1 VSS_6
FA1 VSS_7
AV40 VSS_8
AP40 VSS_9
AN40 VSS_10
AK40 VSS_11
AH40 VSS_12
AG40 VSS_13
AF40 VSS_14
AE40 VSS_15
AD40 VSS_16
AC40 VSS_17
AB40 VSS_18
AA40 VSS_19
WA39 VSS_20
TA39 VSS_21
PA39 VSS_22
MA39 VSS_23
JA39 VSS_24
FA39 VSS_25
Y39 VSS_26
W39 VSS_27
V39 VSS_28
T39 VSS_29
R39 VSS_30
P39 VSS_31
N39 VSS_32
M39 VSS_33
L39 VSS_34
J39 VSS_35
H39 VSS_36
G39 VSS_37
F39 VSS_38
D39 VSS_39
C39 VSS_40
AT38 VSS_41
AM38 VSS_42
AH38 VSS_43
AG38 VSS_44
AF38 VSS_45
AE38 VSS_46
AD38 VSS_47
AK37 VSS_48
AH37 VSS_49
AB37 VSS_50
Y37 VSS_51
W37 VSS_52
V37 VSS_53
T37 VSS_54
R37 VSS_55
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J37 VSS_60
H37 VSS_61
G37 VSS_62
F37 VSS_63
D37 VSS_64
C37 VSS_65
AY36 VSS_66
AW36 VSS_67
AN36 VSS_68
AH36 VSS_69
AG36 VSS_70
AF36 VSS_71
AD36 VSS_72
AC36 VSS_73
C36 VSS_74
B36 VSS_75
BA35 VSS_76
AV35 VSS_77
AR35 VSS_78
AQ35 VSS_79
AB35 VSS_80
AA35 VSS_81
Y35 VSS_82
W35 VSS_83
V35 VSS_84
T35 VSS_85
R35 VSS_86
P35 VSS_87
N35 VSS_88
M35 VSS_89
L35 VSS_90
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F35 VSS_94
D35 VSS_95
C35 VSS_96
AN34

VSS

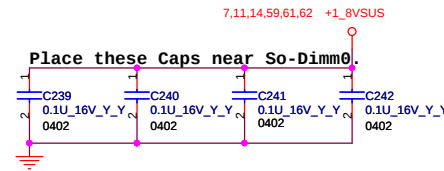
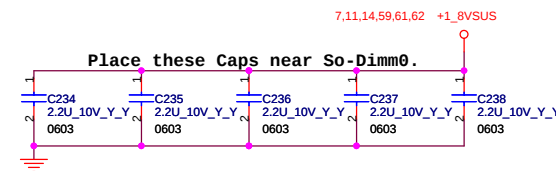
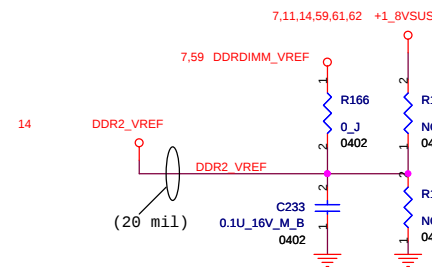
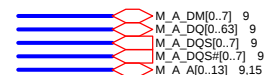
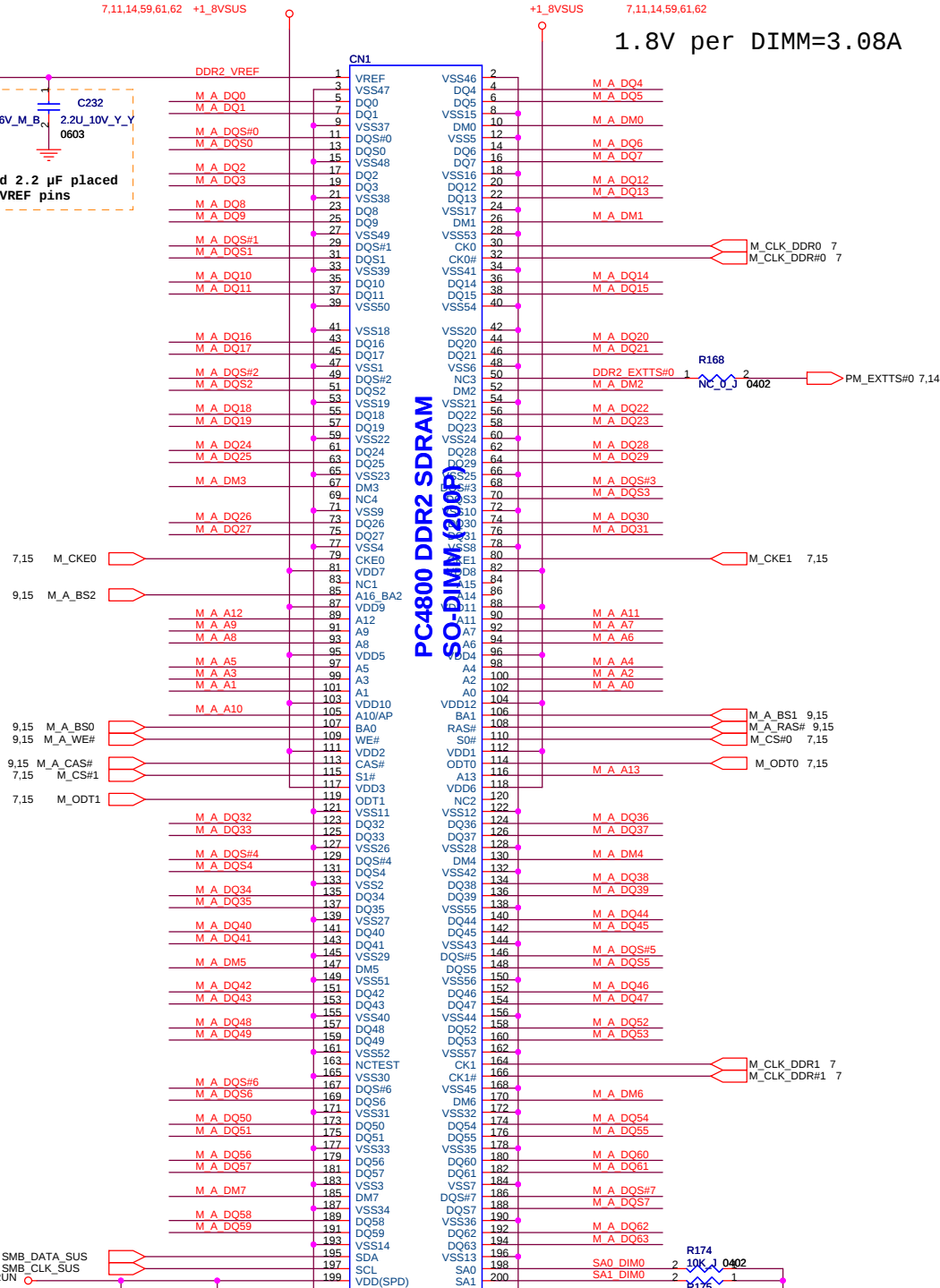
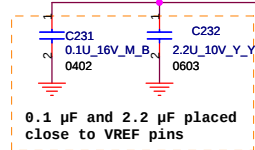
VSS_97 AK34
VSS_98 AG34
VSS_99 AF34
VSS_100 AE34
VSS_101 AC34
VSS_102 AW33
VSS_103 AV33
VSS_104 AR33
VSS_105 AE33
VSS_106 AC33
VSS_107 AB33
VSS_108 Y33
VSS_109 V33
VSS_110 T33
VSS_111 R33
VSS_112 M33
VSS_113 H33
VSS_114 B33
VSS_115 D33
VSS_116 BA21
VSS_117 B33
VSS_118 AH32
VSS_119 AG32
VSS_120 AF32
VSS_121 AE32
VSS_122 AC32
VSS_123 AB32
VSS_124 G32
VSS_125 B32
VSS_126 AY31
VSS_127 AV31
VSS_128 AN31
VSS_129 AJ31
VSS_130 AG31
VSS_131 AB31
VSS_132 Y31
VSS_133 AB30
VSS_134 E30
VSS_135 AT29
VSS_136 AN29
VSS_137 AB29
VSS_138 T29
VSS_139 N29
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VSS_144 B29
VSS_145 A29
VSS_146 BA28
VSS_147 AM28
VSS_148 AP28
VSS_149 AV28
VSS_150 AM28
VSS_151 AD28
VSS_152 AC28
VSS_153 W28
VSS_154 J28
VSS_155 E28
VSS_156 AP27
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VSS_159 J27
VSS_160 G27
VSS_161 F27
VSS_162 C27
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VSS_166 K26
VSS_167 F26
VSS_168 D26
VSS_169 AK25
VSS_170 P25
VSS_171 K25
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VSS_173 E25
VSS_174 D25
VSS_175 A25
VSS_176 BA24
VSS_177 AU24
VSS_178 AL24
VSS_179 AW23

U4J
AT23 VSS_180
AN23 VSS_181
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AW20 VSS_209
AR20 VSS_210
AM20 VSS_211
AA20 VSS_212
K20 VSS_213
B20 VSS_214
A20 VSS_215
AN19 VSS_216
AC19 E30
W19 VSS_217
K19 VSS_218
G19 VSS_219
C19 VSS_220
AH18 VSS_221
K29 VSS_222
H18 VSS_223
D18 VSS_224
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AY17 VSS_226
AR17 VSS_227
AP17 VSS_228
AM17 VSS_229
AK17 VSS_230
AV16 VSS_231
AN16 VSS_232
AL16 VSS_233
J16 VSS_234
W16 VSS_235
U16 VSS_236
R16 VSS_237
N15 VSS_238
M15 VSS_239
L15 VSS_240
B15 VSS_241
A15 VSS_242
BA14 VSS_243
AT14 VSS_244
M26 VSS_245
AD14 VSS_246
AA14 VSS_247
U14 VSS_248
K14 VSS_249
H14 VSS_250
P25 VSS_251
E14 VSS_252
AV13 VSS_253
E25 VSS_254
AM13 VSS_255
A25 VSS_256
BA24 VSS_257
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AL24 VSS_259
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P13 VSS_261
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AC12 VSS_266
K12 VSS_267
H12 VSS_268
E12 VSS_269
AD11 VSS_270
AA11 VSS_271
Y11 VSS_272

VSS

VSS_273 J11
VSS_274 D11
VSS_275 B11
VSS_276 AV10
VSS_277 AP10
VSS_278 AL10
VSS_279 AJ10
VSS_280 AG10
VSS_281 AC10
VSS_282 W10
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VSS_288 AB9
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VSS_352 U2
VSS_353 T2
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VSS_358 C2
VSS_359 AL1
VSS_360

CALISTOGA



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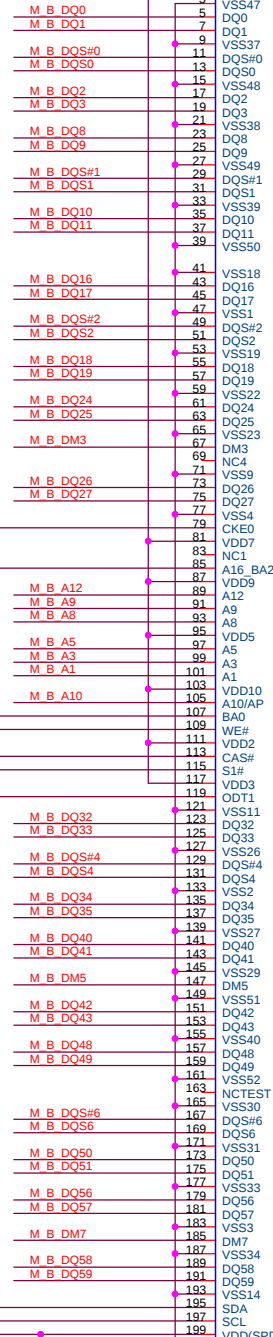
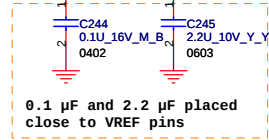
DDR2_VREF

7,11,13,59,61,62 +1_8VSUS

+1_8VSUS

7,11,13,59,61,62

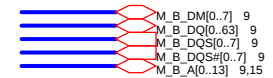
1.8V per DIMM=3.08A

PC4800 DDR2 SDRAM
SO-DIMM (200P)

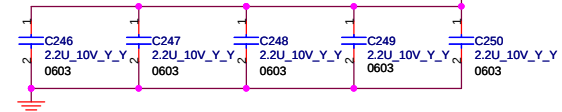
DIMM_1

SMBus Address: A4(W)/A5(R)

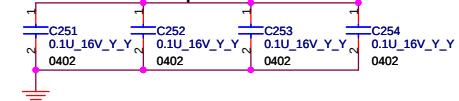
DIMM_1 is placed farther from the GMCH than DIMM_0



Place these Caps near So-Dimm1.



Place these Caps near So-Dimm1.



FOXCONN			HON HAI Precision Ind. Co., Ltd.	
File			CCPBG - R&D Division	
Size			Document Number	
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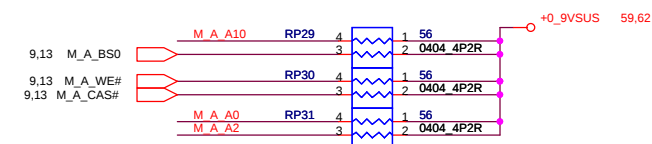
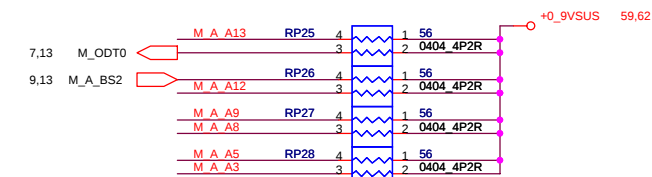
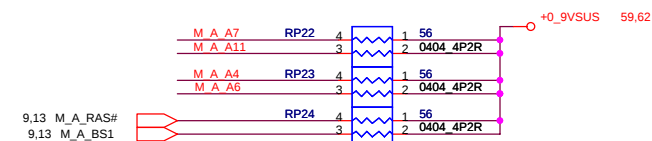
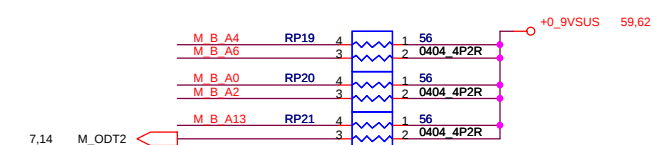
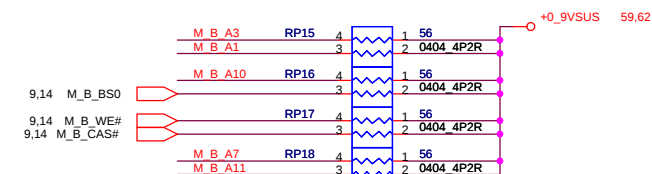
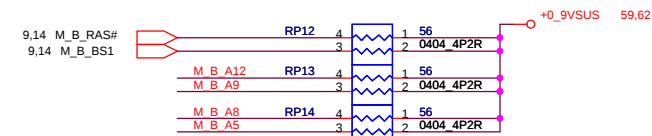
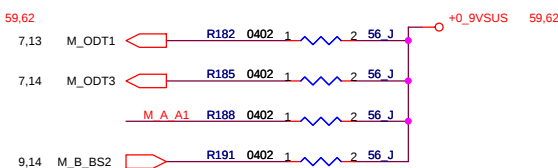
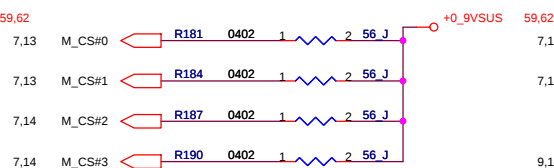
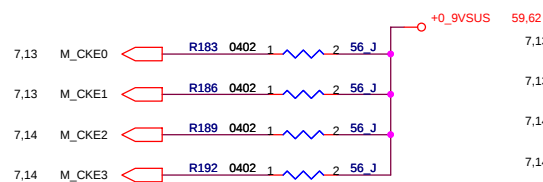
+0_9VSUS

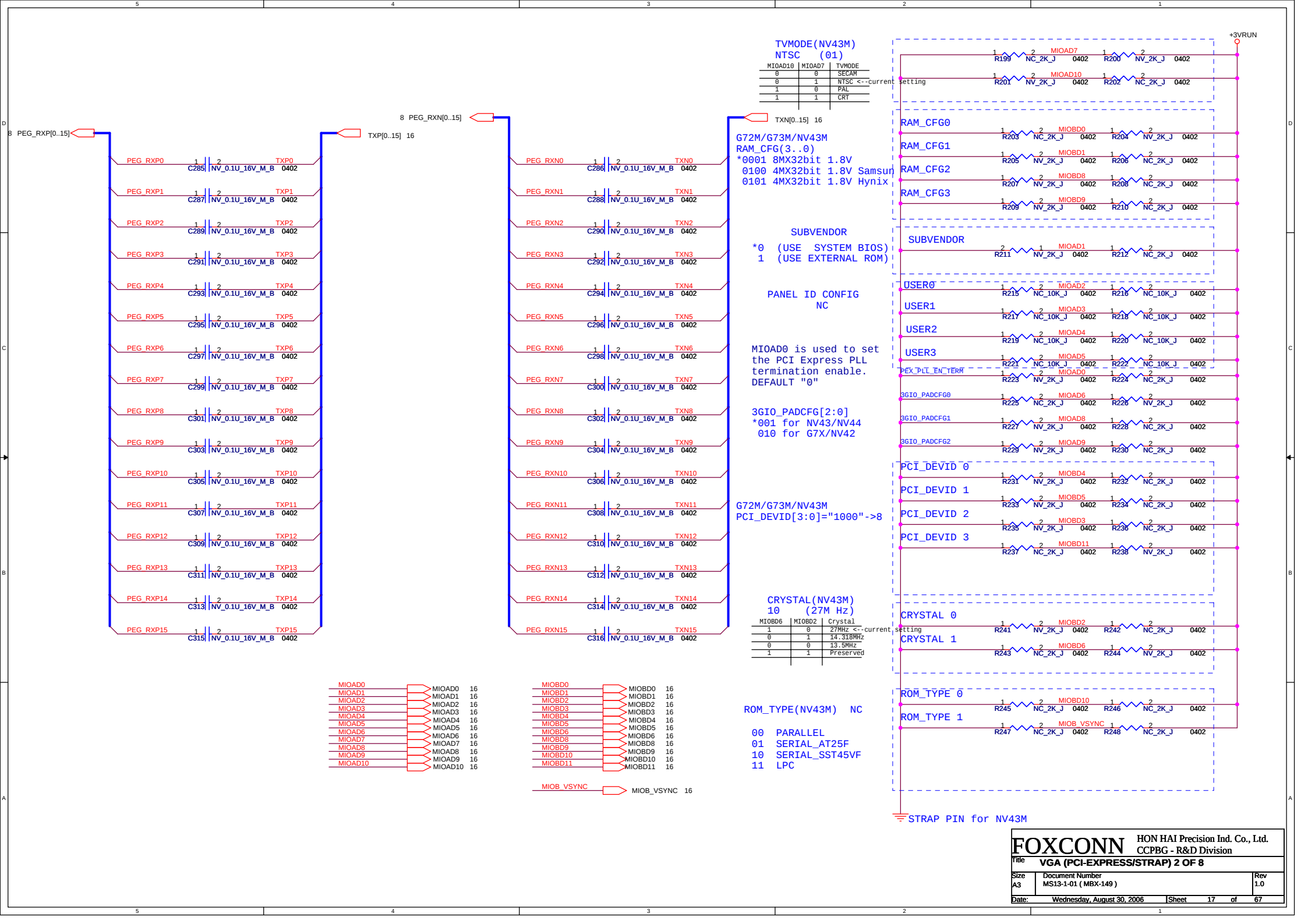
59,62

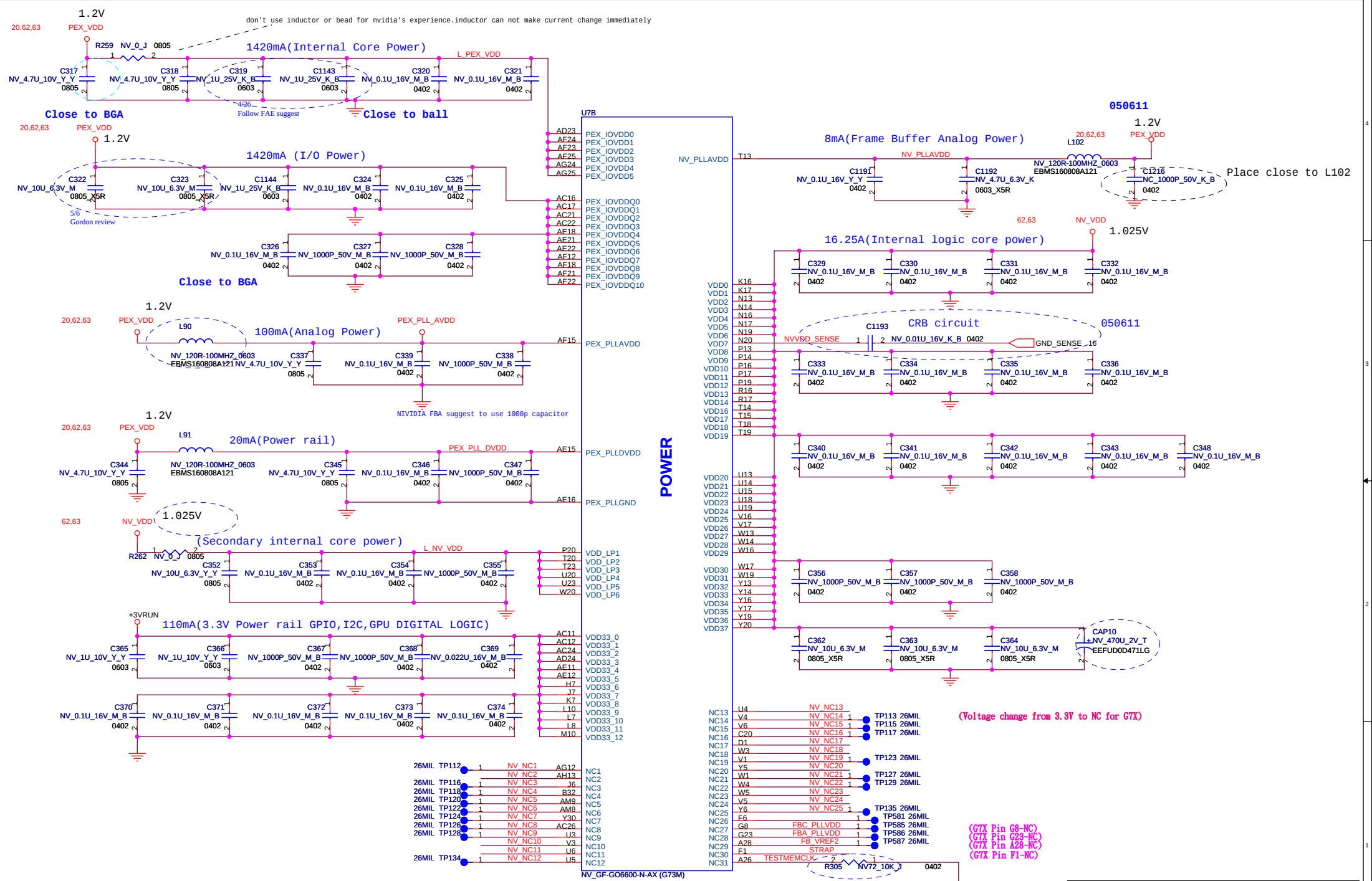
+0_9VSUS

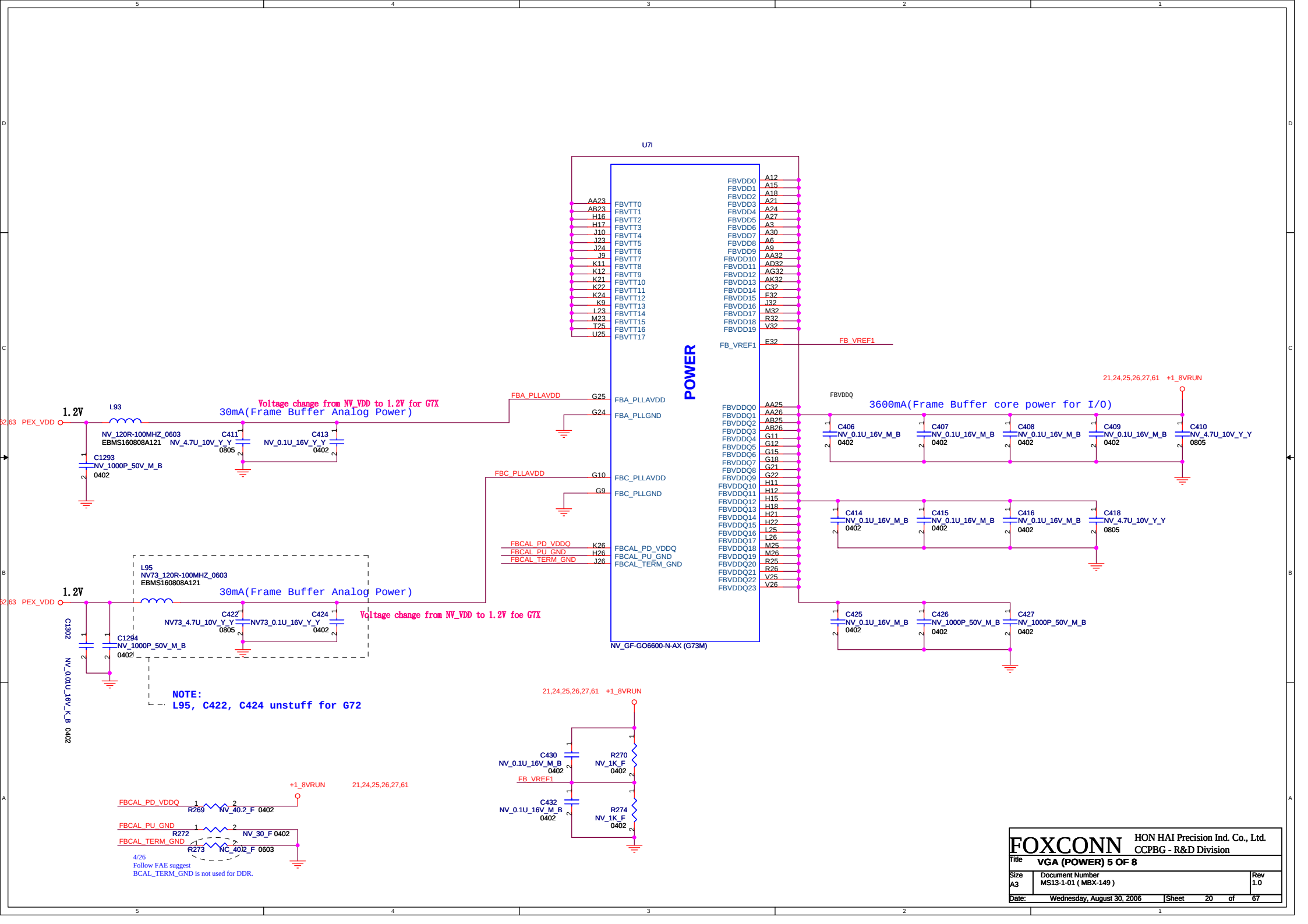
Layout note: Place 1 cap close to every 1 R-pack terminated to +0_9VSUS

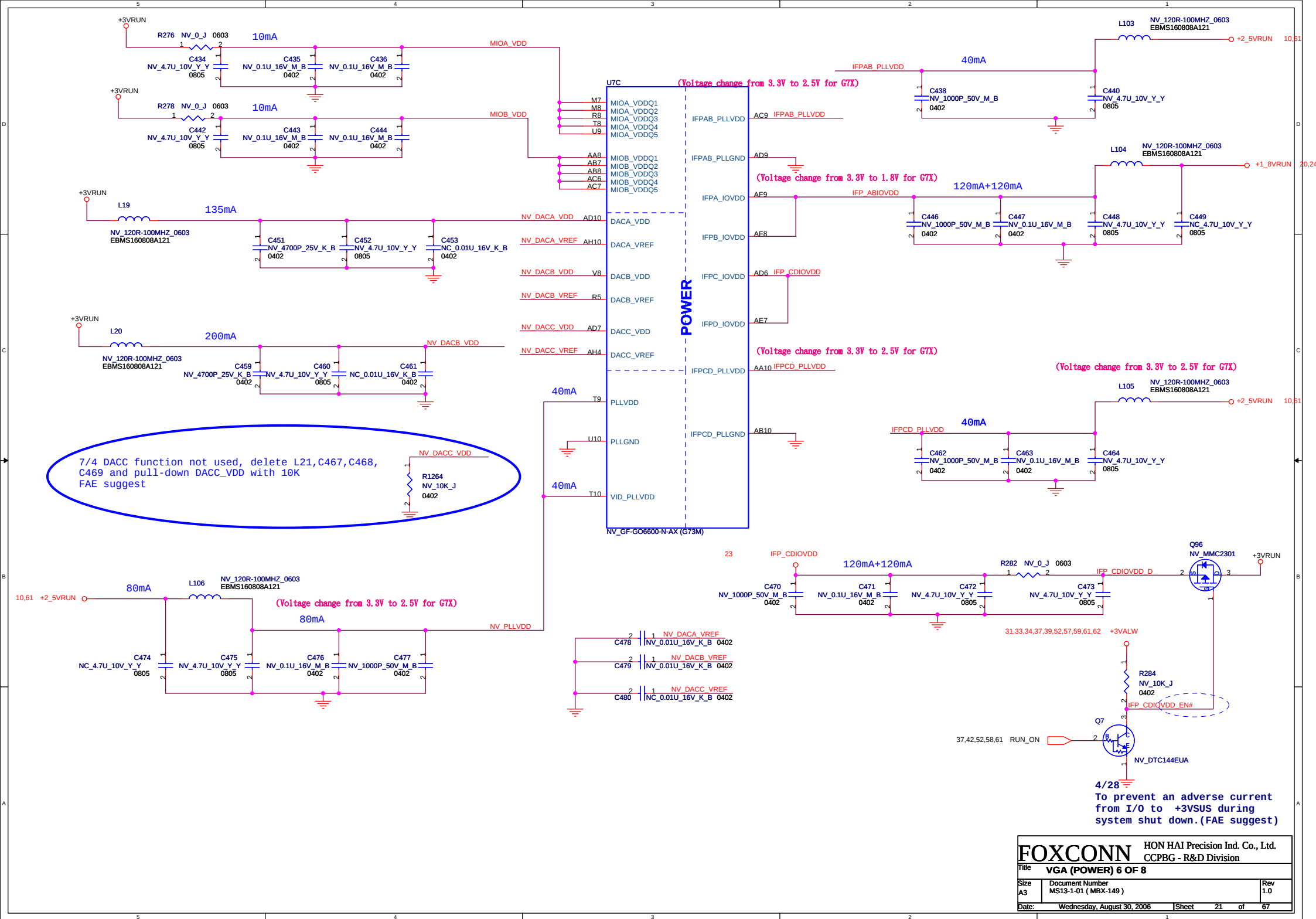
Layout note: Place 1 cap close to every 1 R-pack terminated to +0_9VSUS

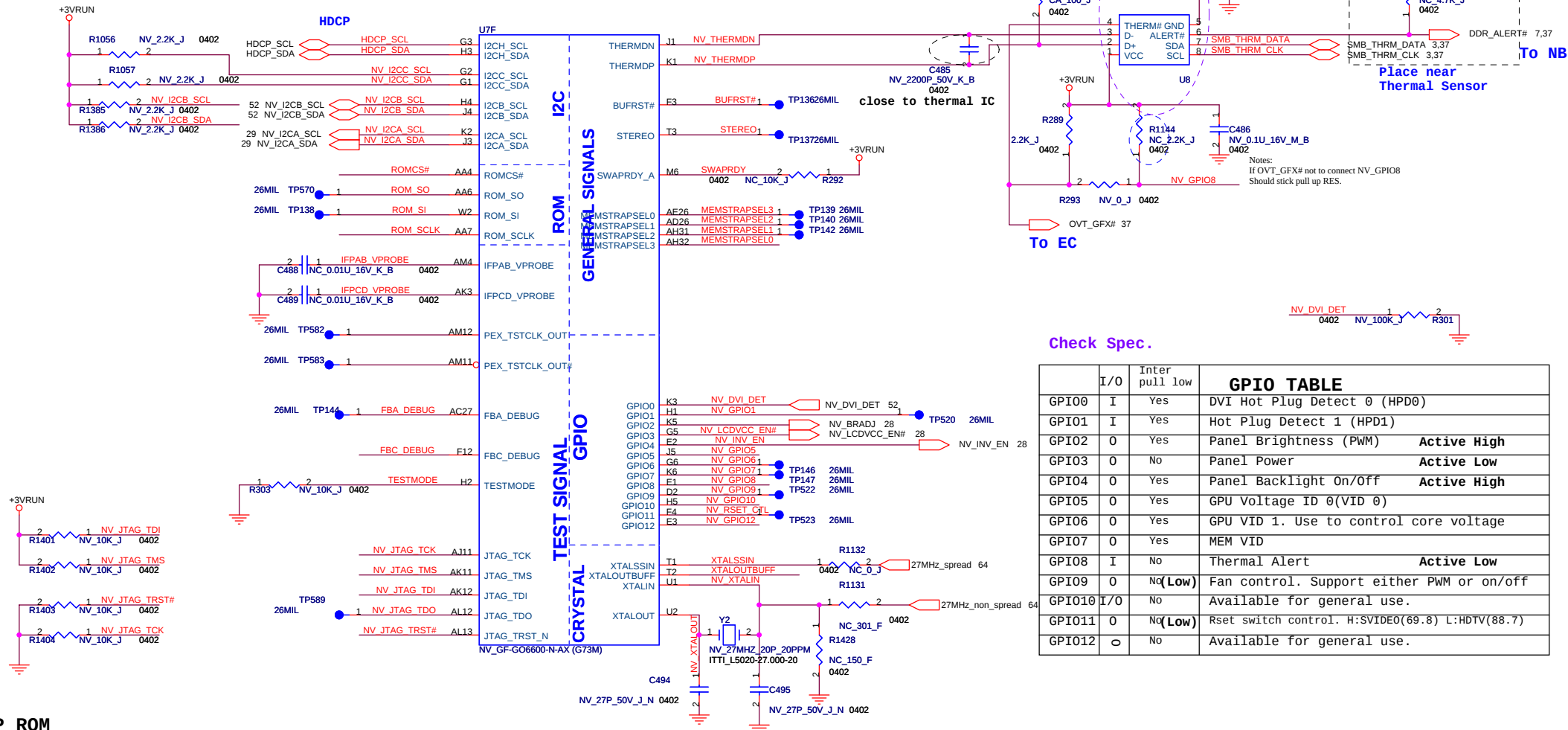




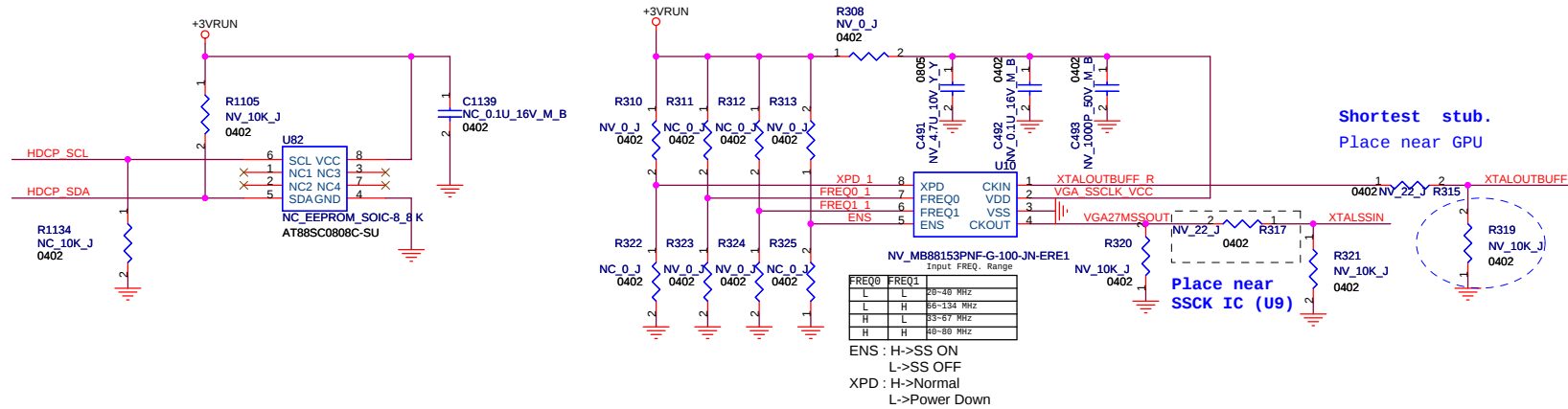


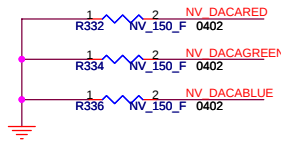




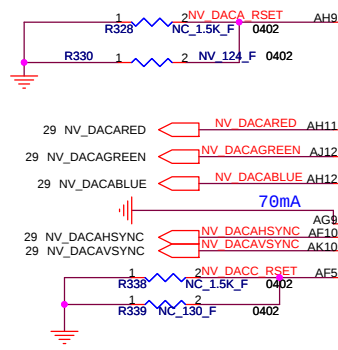


HDCP ROM



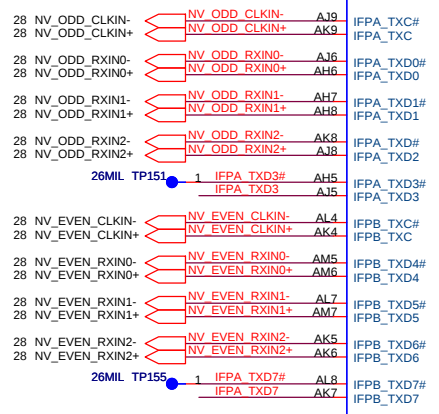
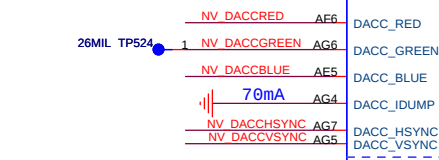


CLOSE TO GPU

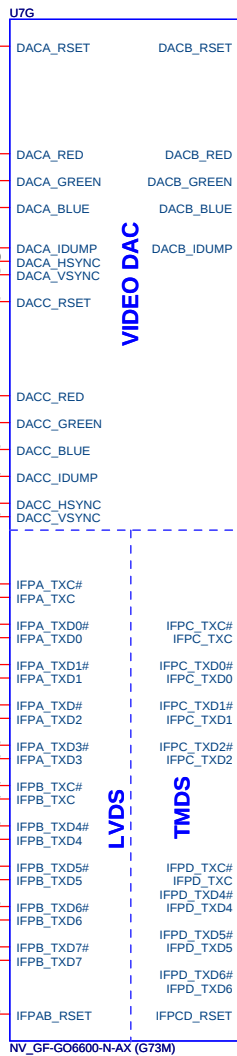


CLOSE TO GPU

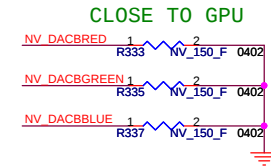
DACA	VGA-CRT			I2CA
DACA-RED	R			
DACA-GREEN	G			
DACA-BLUE	B			
DACA-HSYNC	HSYNC			
DACA-VSYNC	VSYNC			
	VGA-DBCLK			SCL
	VGA-DBDATA			SDA
DACB	S-VIDEO	COMPOSITE	D-CONNECTOR	I2CC
DACB-RED	C		PR	
DACB-GREEN	Y		Y	
DACB-BLUE		COMPOSITE		
			LINE1	SCL
			LINE2	SDA
			LINE3	
DACC	DVI-I			I2CB
DACC-RED	R			
DACC-GREEN	G			
DACC-BLUE	B			
DACC-HSYNC	HSYNC			
DACC-VSYNC	VSYNC			
	DVI-DBCLK			SCL
	DVI-DBDATA			SDA



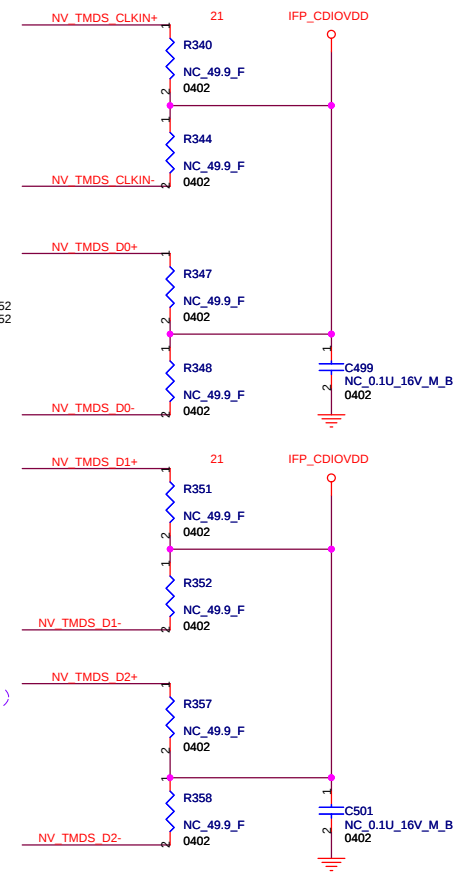
for G7X Unstuff (NC)

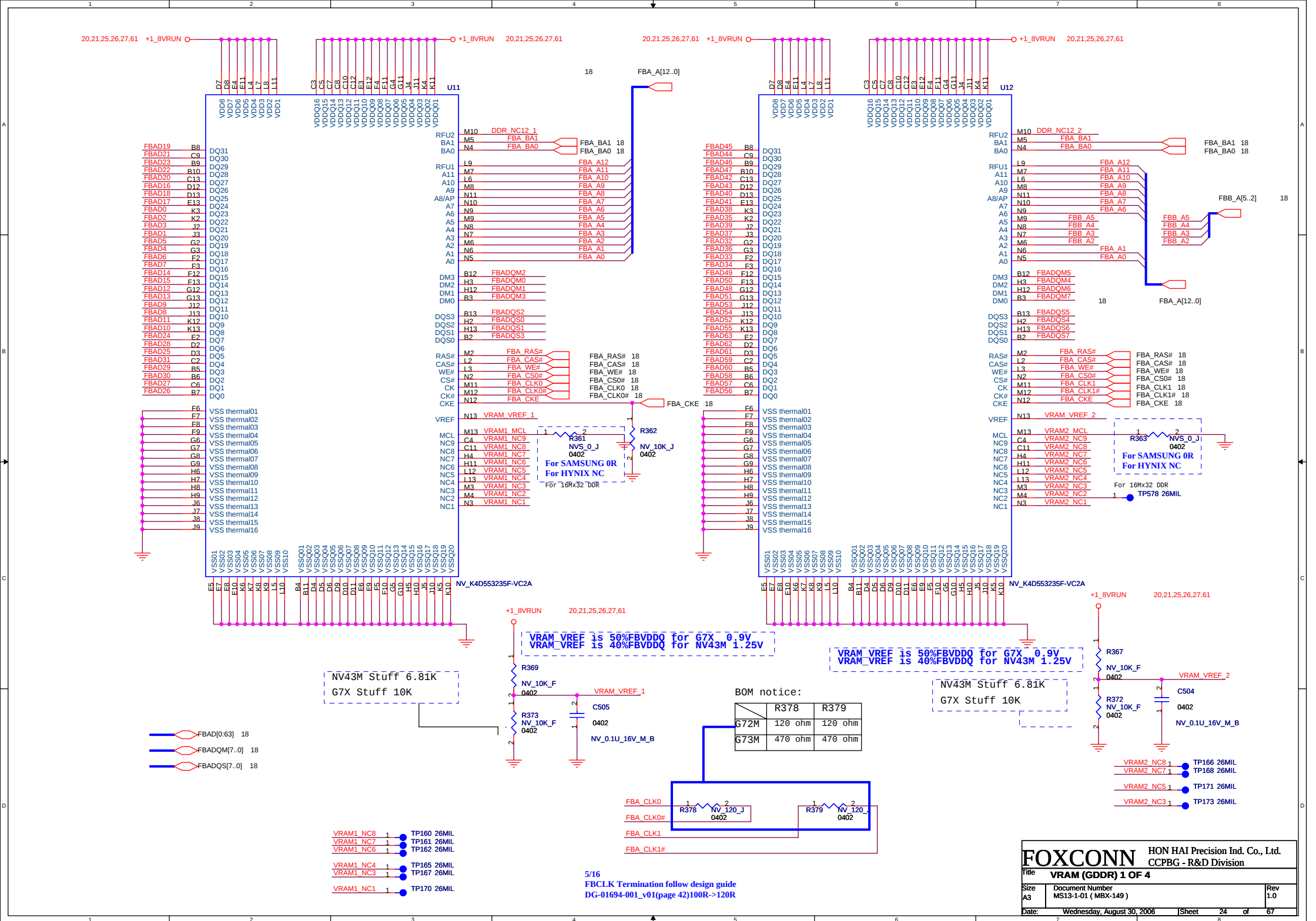


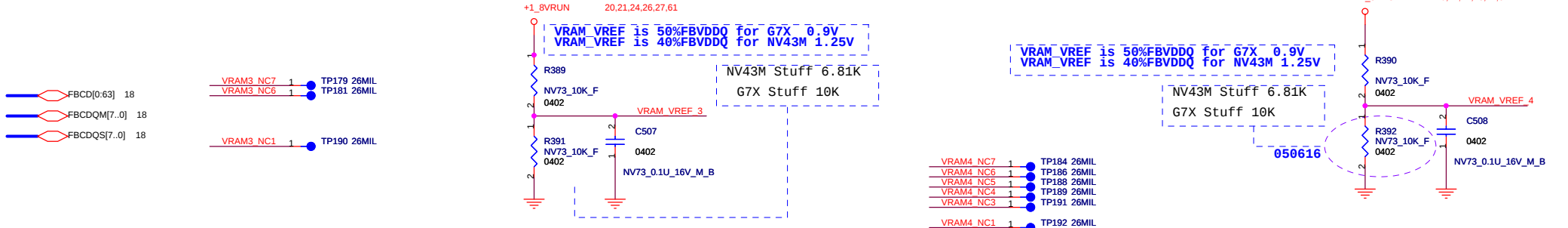
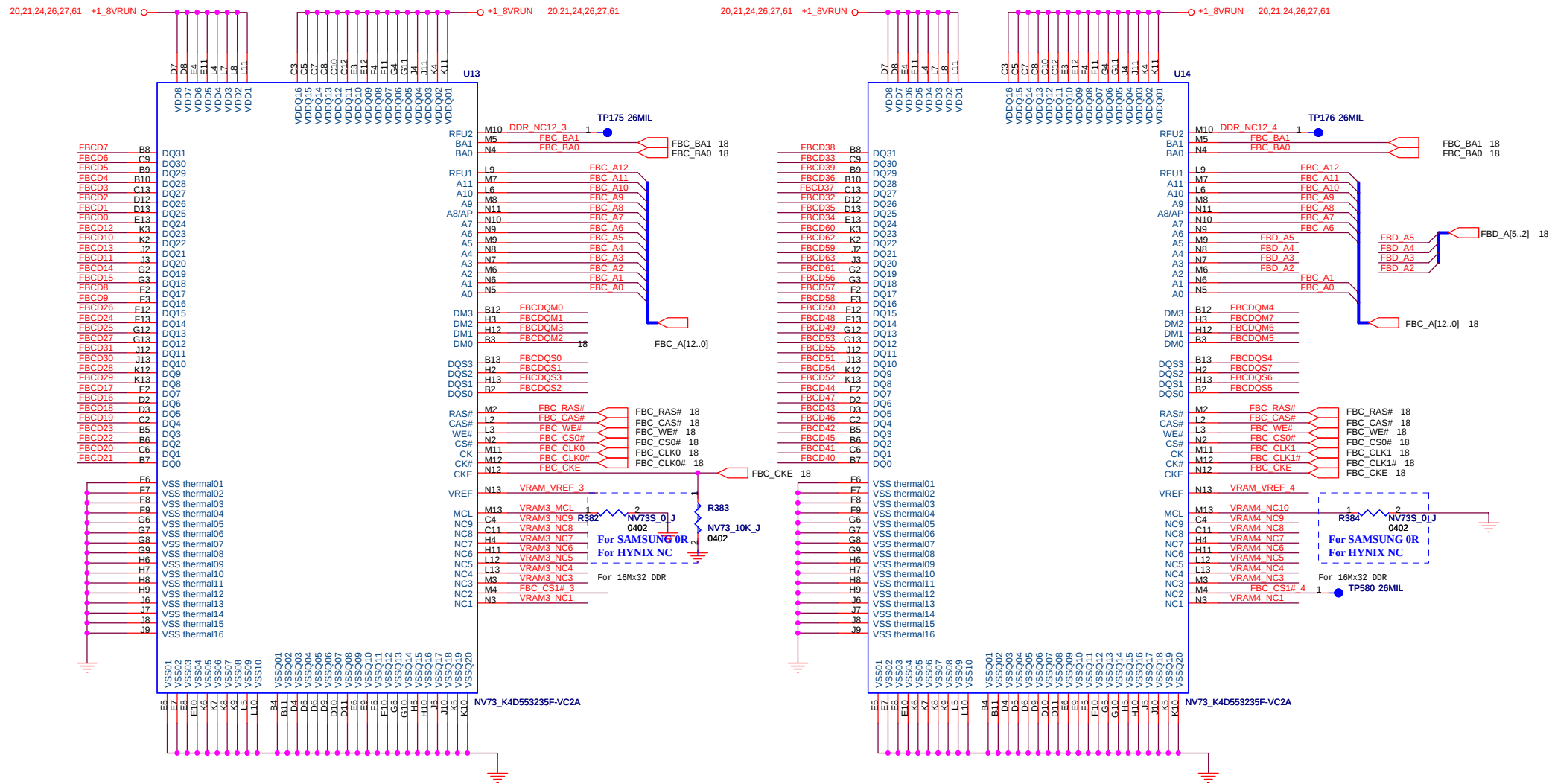
Place close to chipset



CLOSE TO GPU



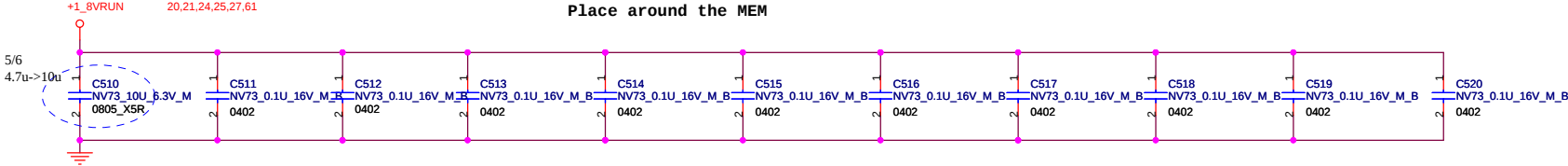




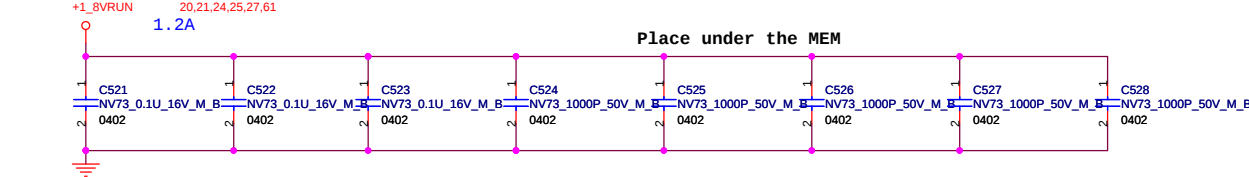
If use G72M, please unstuff U13, U14 and their related circuit

Decoupling for right MEMORY

Place around the MEM

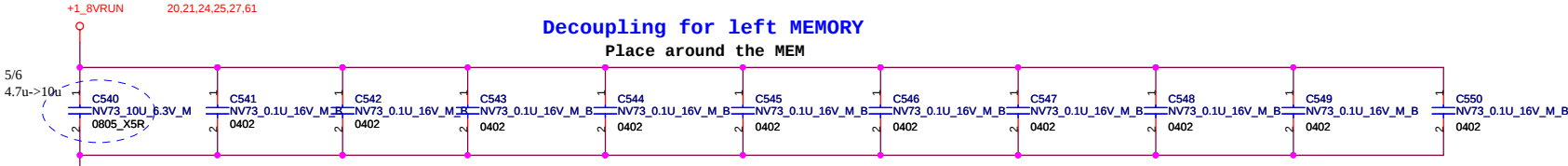


Place under the MEM

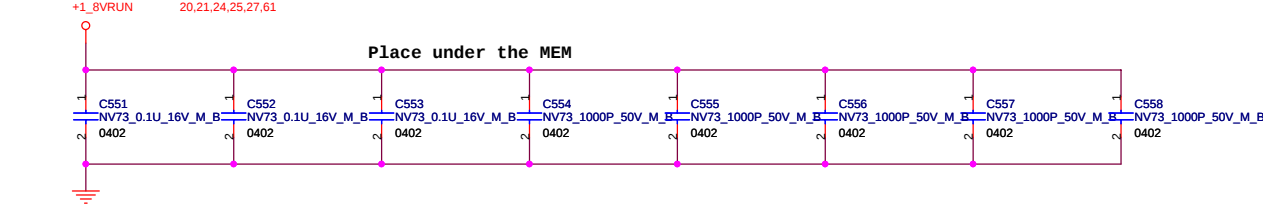


Decoupling for left MEMORY

Place around the MEM

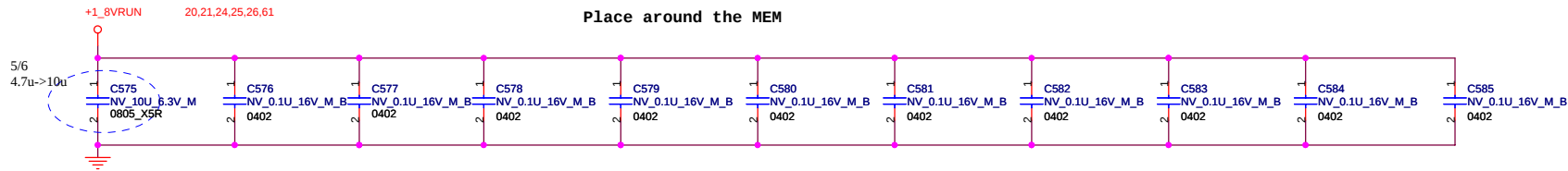


Place under the MEM

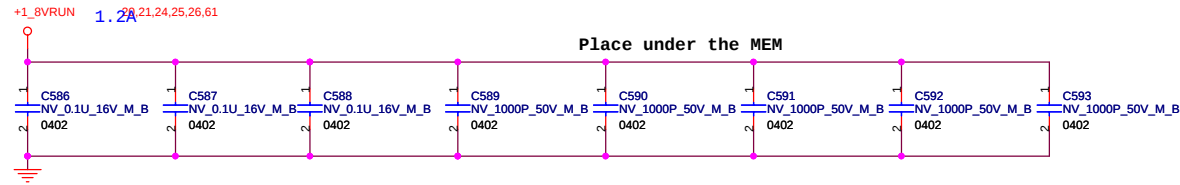


Decoupling for right MEMORY

Place around the MEM



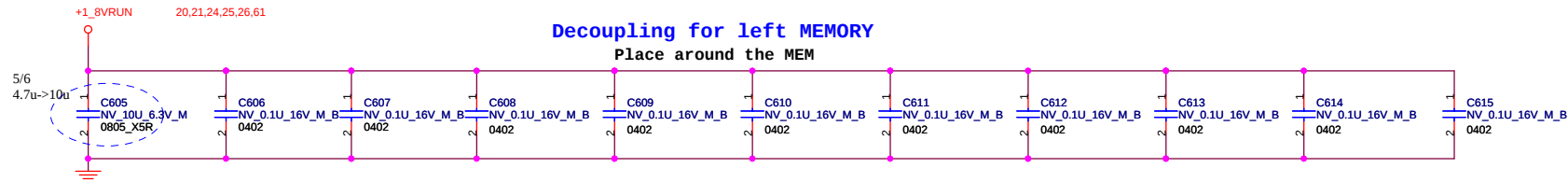
Place under the MEM



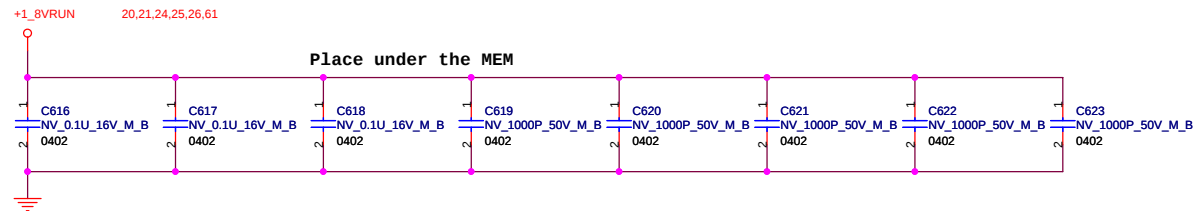
NO USE

Decoupling for left MEMORY

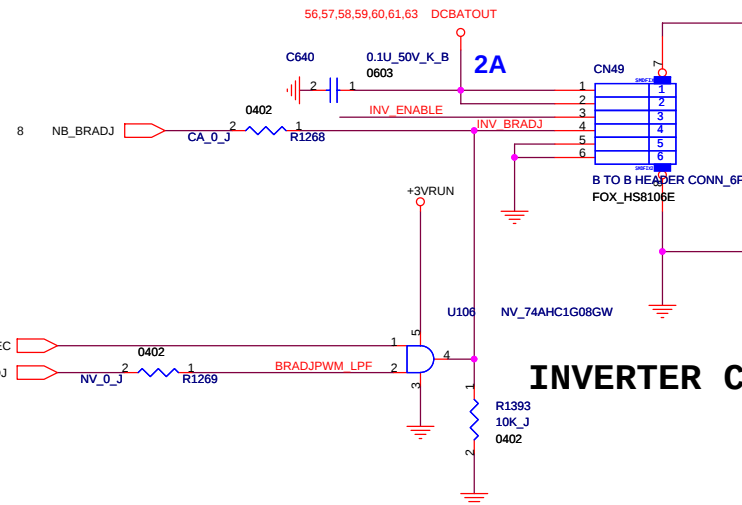
Place around the MEM



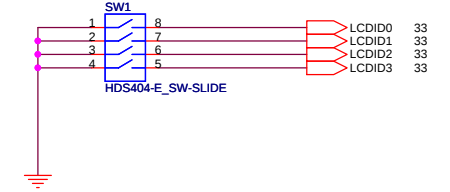
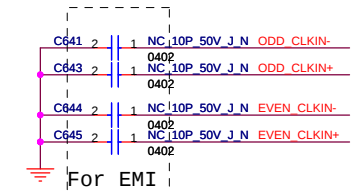
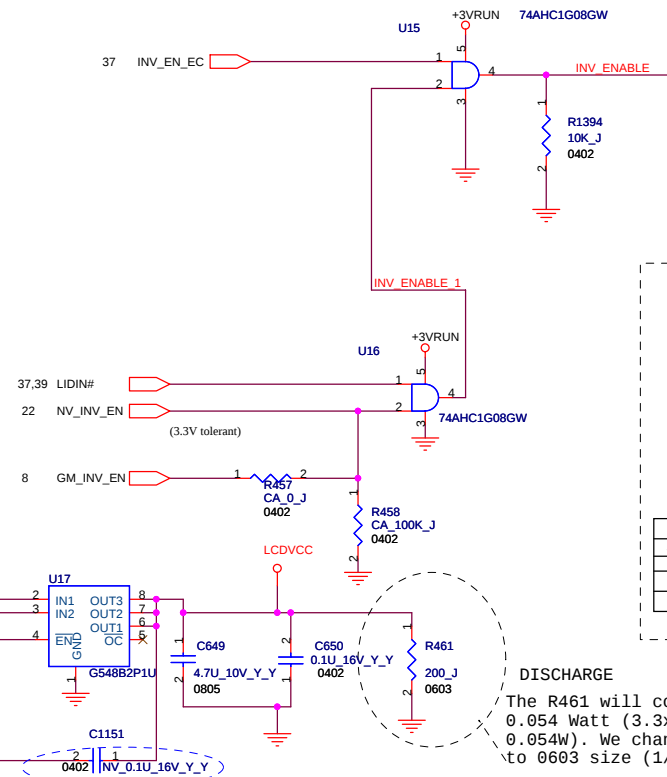
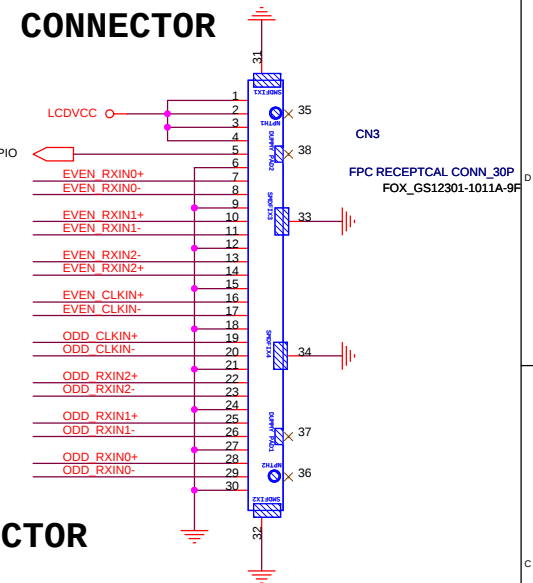
Place under the MEM



Group1,Group1 should be close



LVDS CONNECTOR



Type	WXGA	WXGA-HC	WSXGA+
Size	15.4" wide	15.4" wide	15.4" wide
Vendor	Hitach	Hitachi	Hitachi
Device Name	TX39D81VC1AAA	TX39D80VC1GAA	TX39D90VC1GAA
Panel ID Check[3...0]	1000	1000	1100

ON=0

DISCHARGE

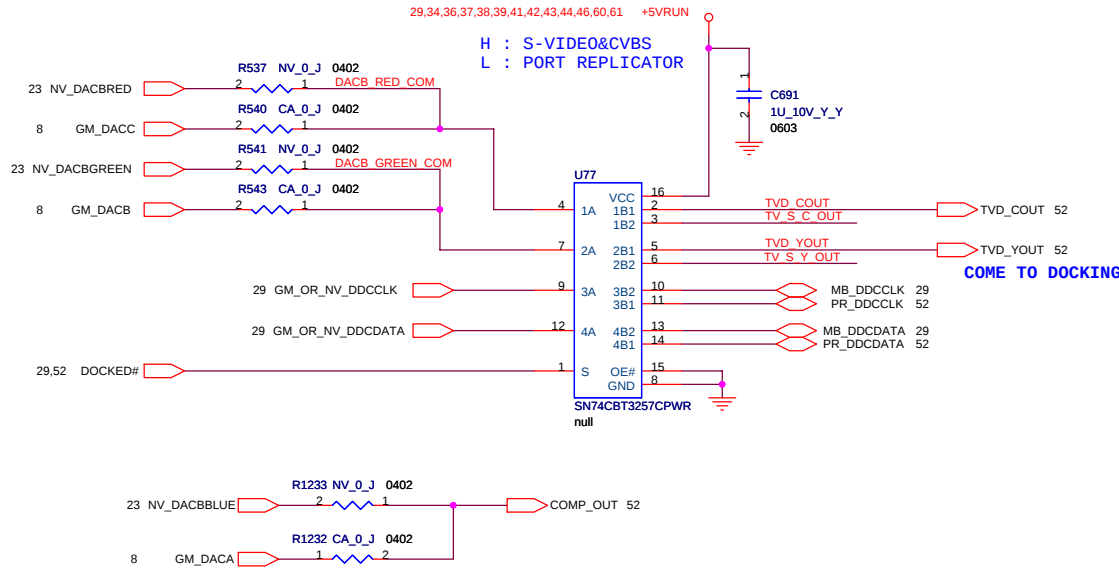
```

/ The R461 will consume about
/ 0.054 Watt ( $3.3 \times 3.3 / 200 =$ 
\ 0.054W). We changed resistor
\ to 0603 size (1/8 Watt)

```

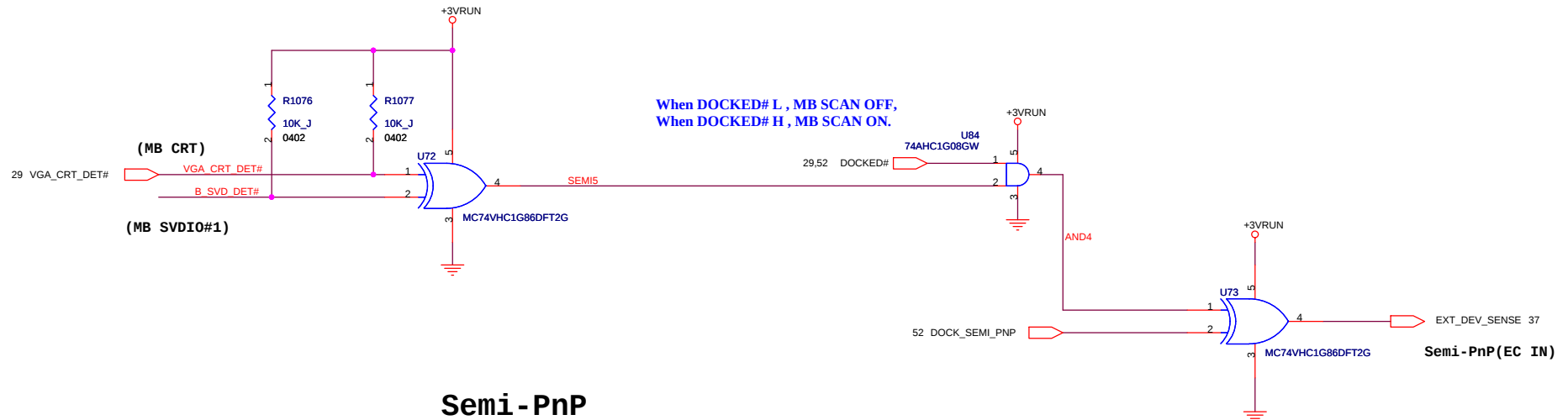
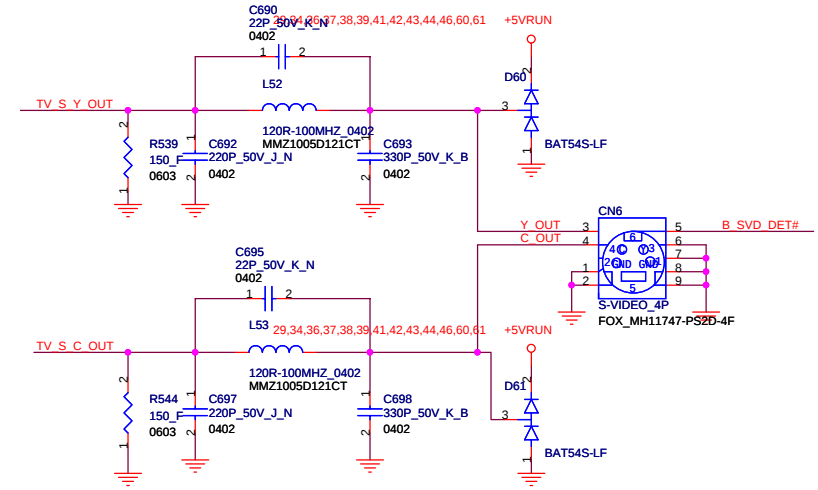
FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title LVDS		CCPBG - R&D Division	
Size A3	Document Number MS13-1-01 (MBX-149)	Rev 1.0	
Date:	Wednesday, August 30, 2006	Sheet	28 of 67

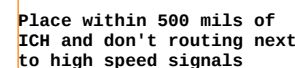
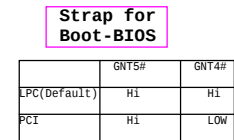
S-VIDEO ANALOG SWITCH

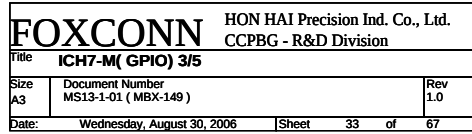


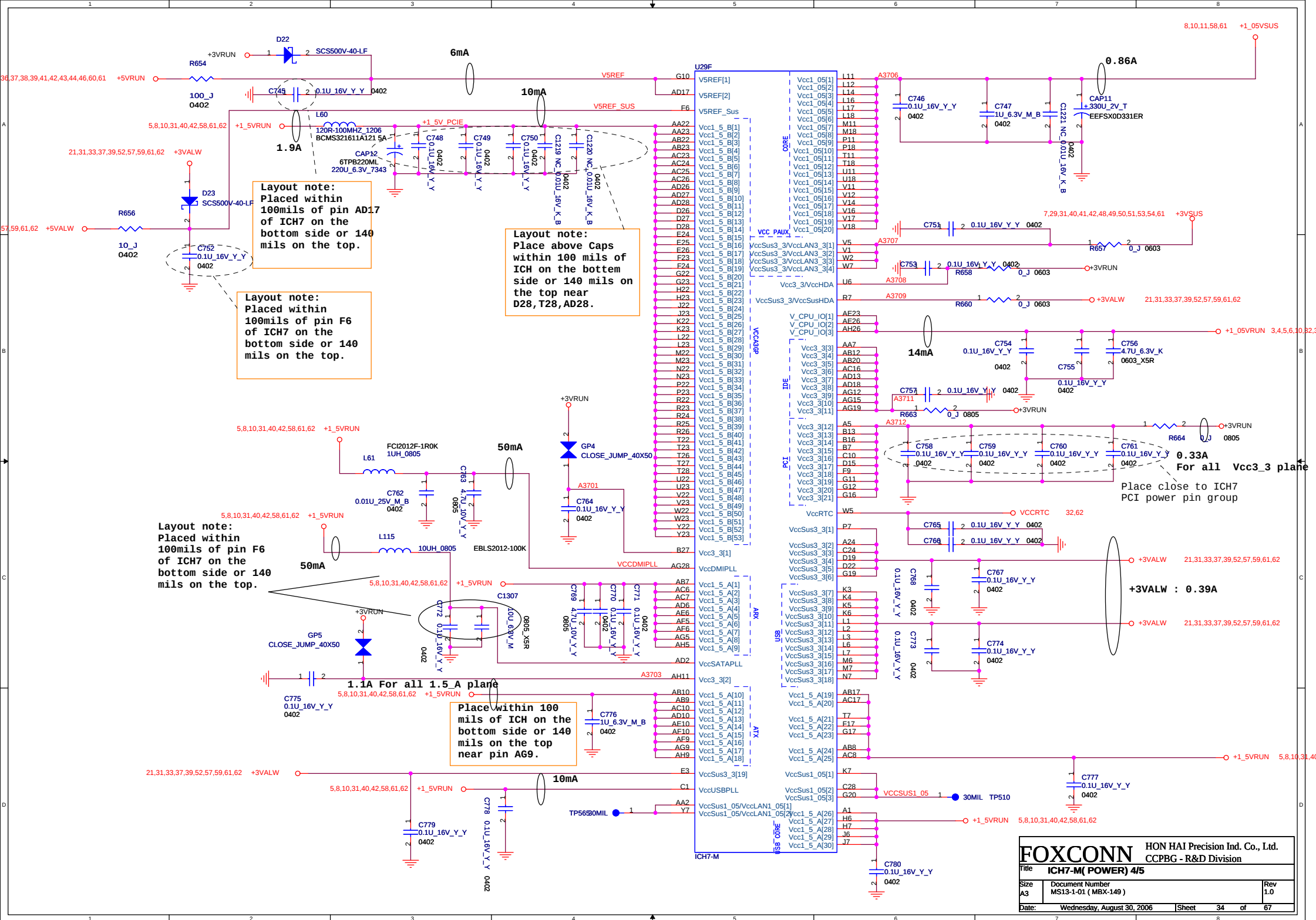
S-VIDEO

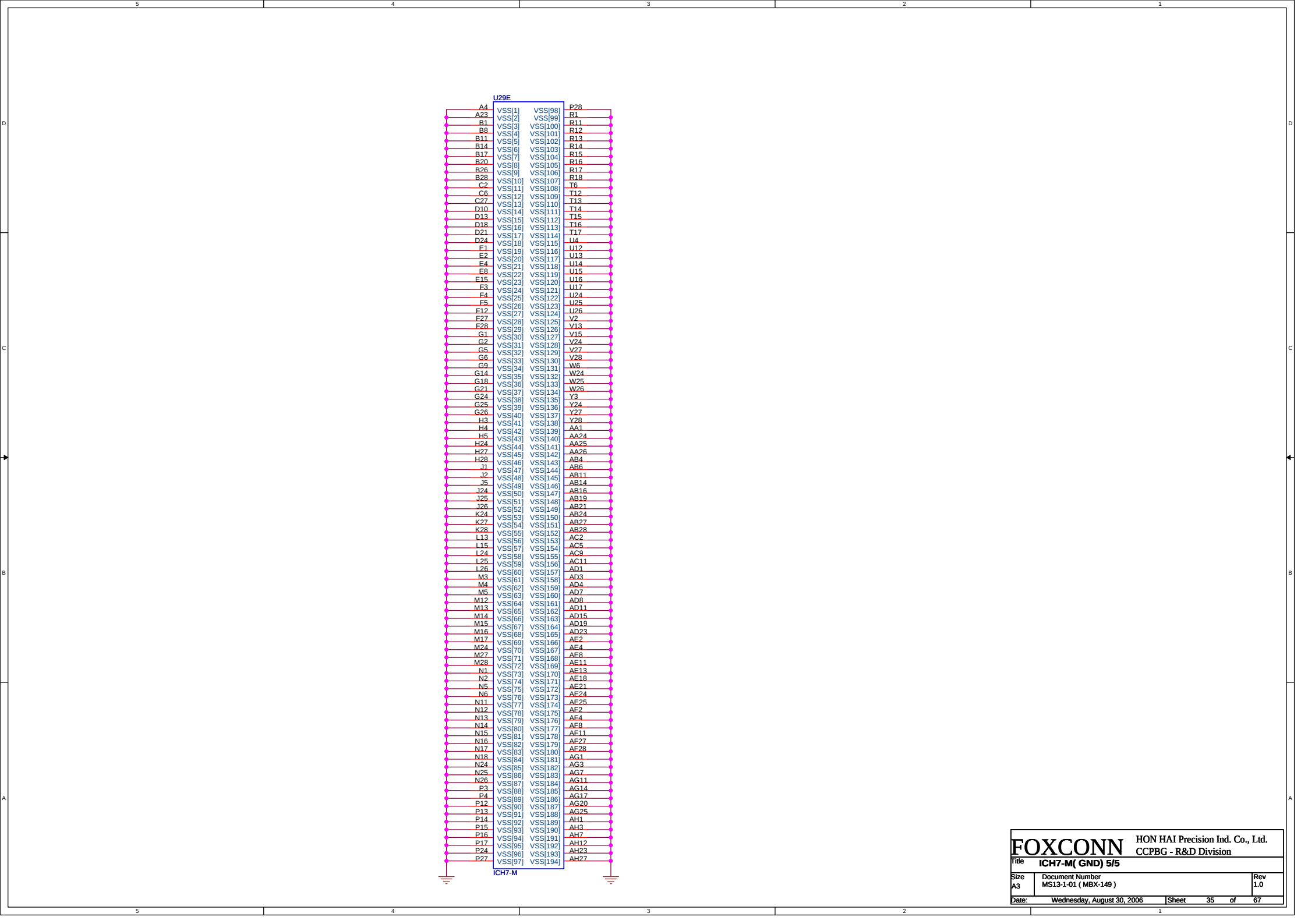
These compoent close to S-Video connector within 700 mil

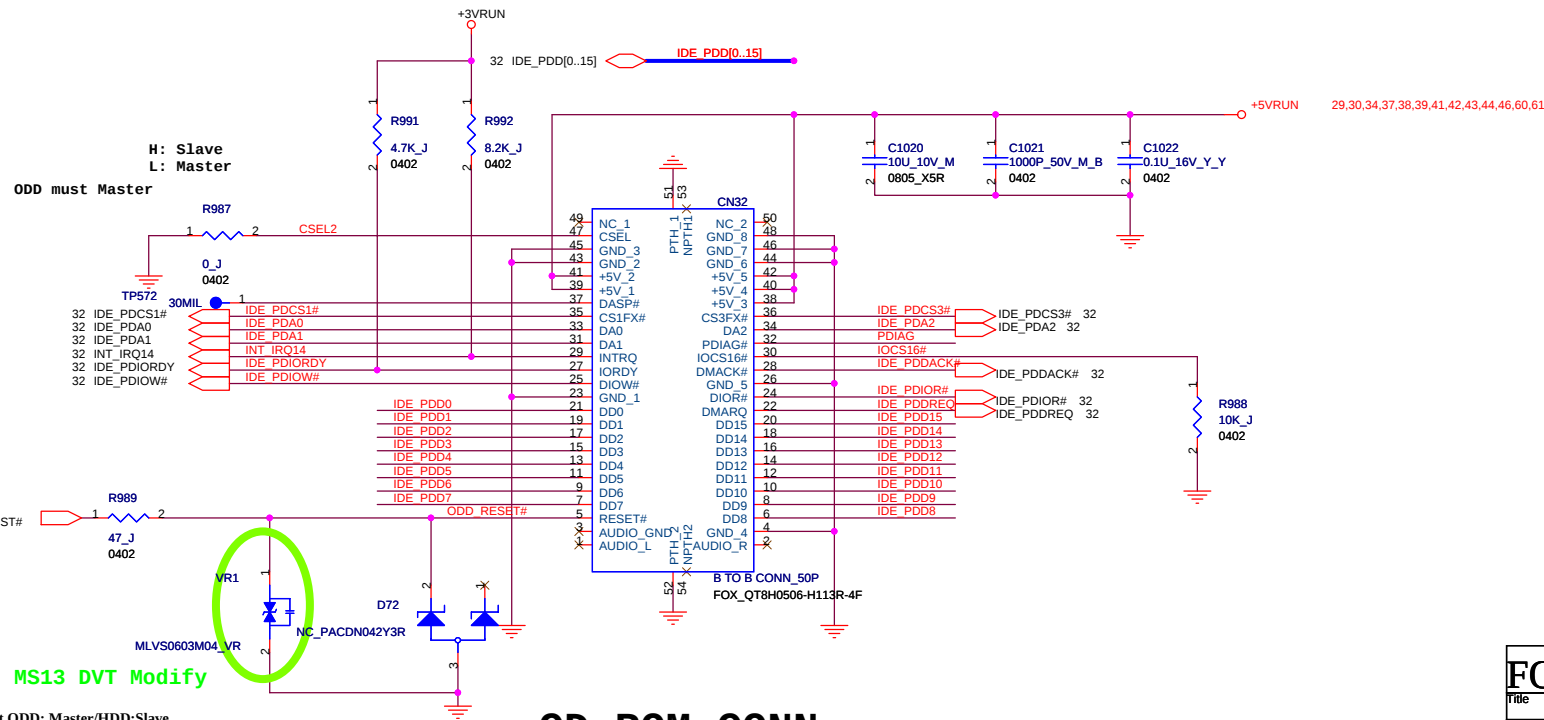
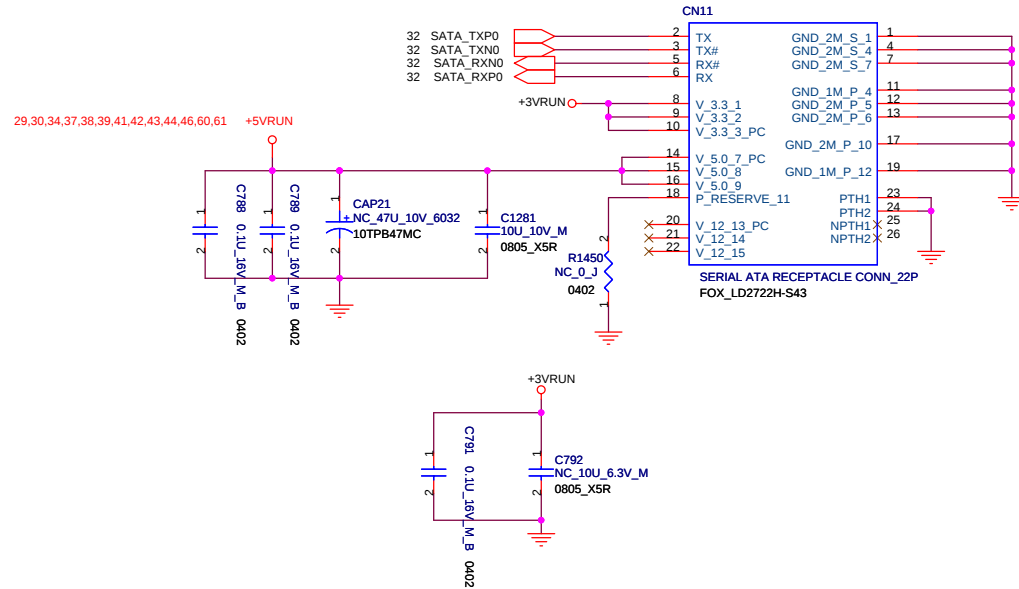






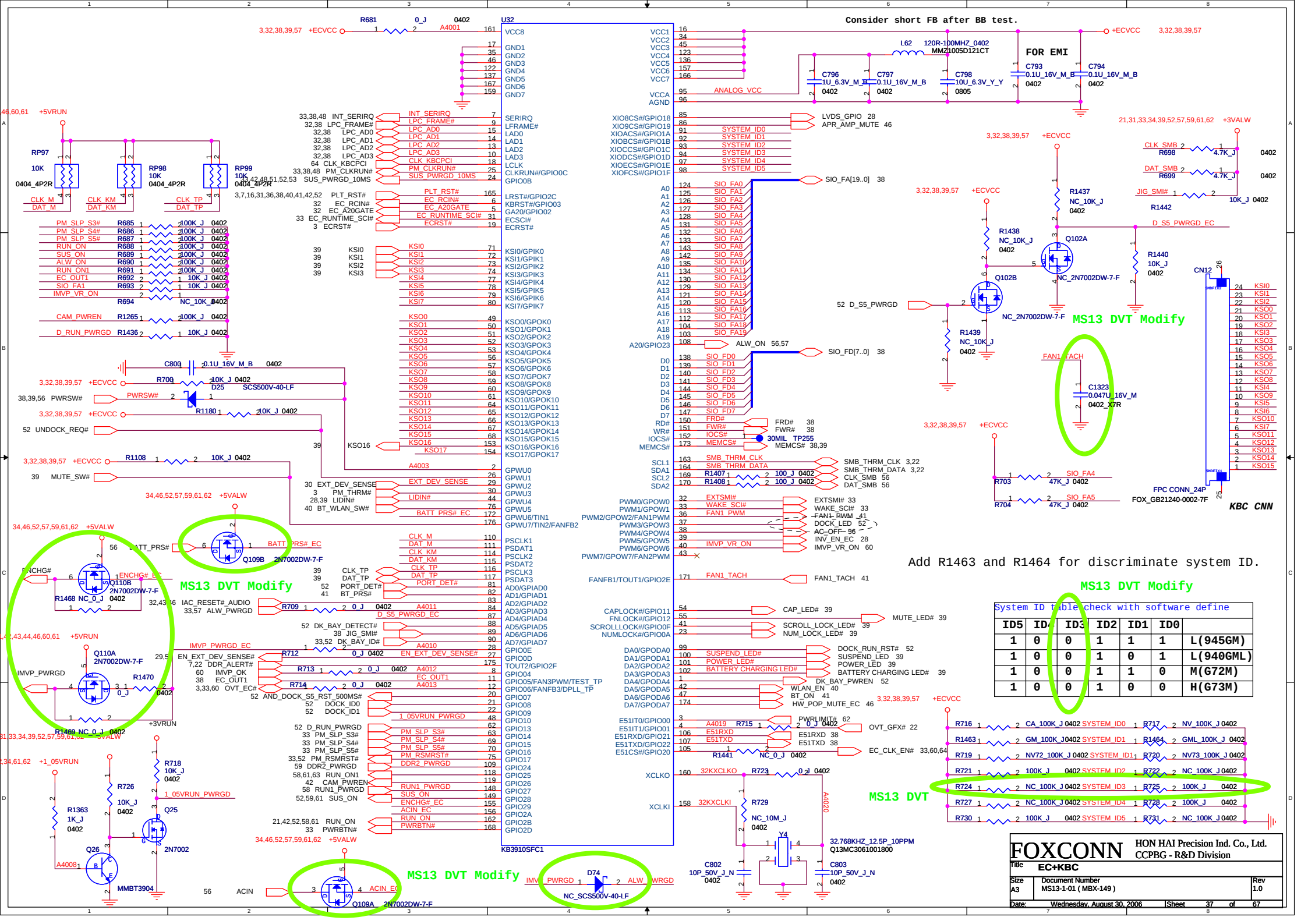






CD-ROM CONN

FOXCONN			HON HAI Precision Ind. Co., Ltd.
Title			CCPBG - R&D Division
Size			Rev
A3	Document Number	MS13-1-01 (MBX-149)	1.0
Date:	Wednesday, August 30, 2006	Sheet	36 of 67



Consider short FB after BB test.

FOR EMI

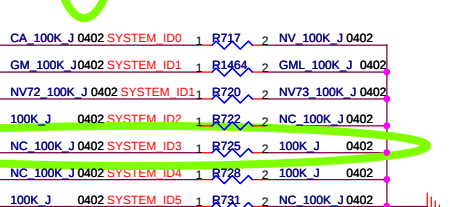
MS13 DVT Modify

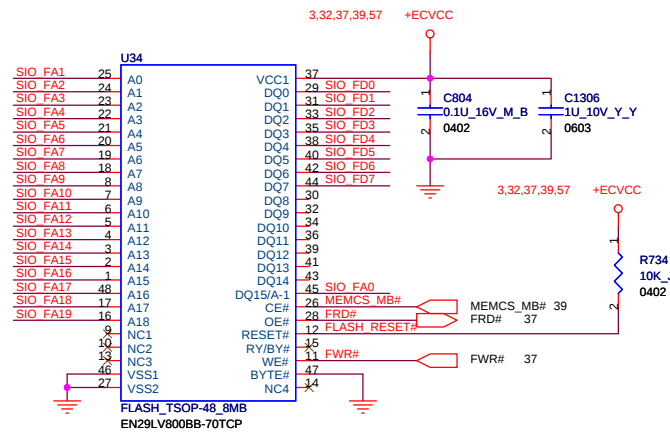
Add R1463 and R1464 for discriminate system ID.

MS13 DVT Modify

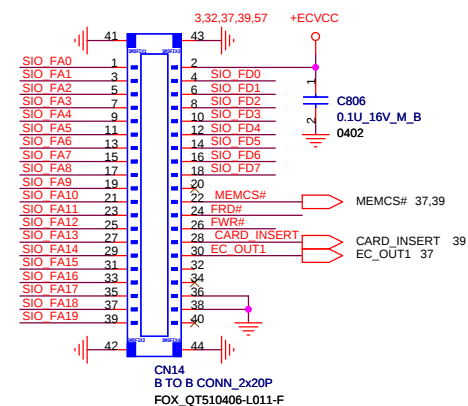
System ID table check with software define

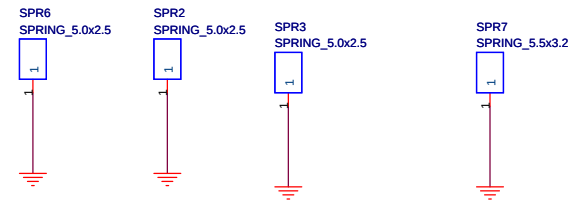
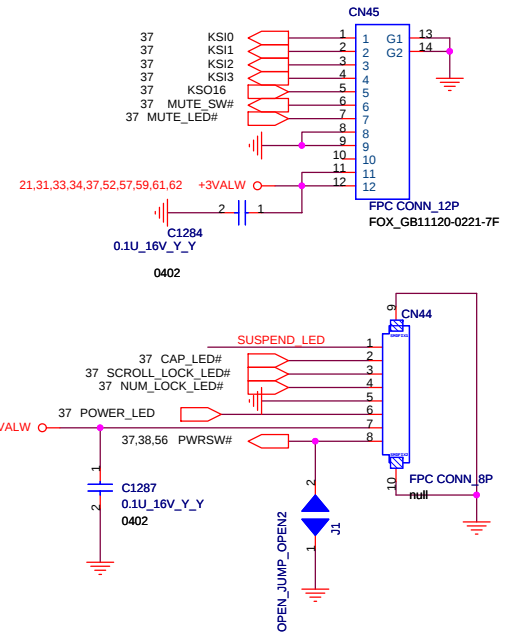
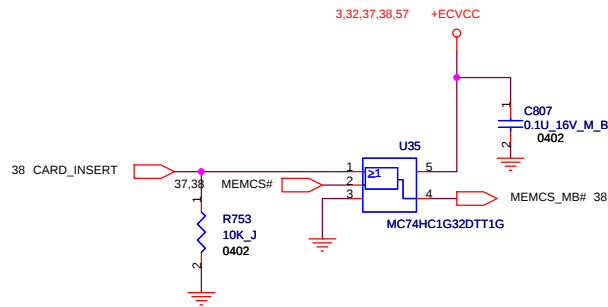
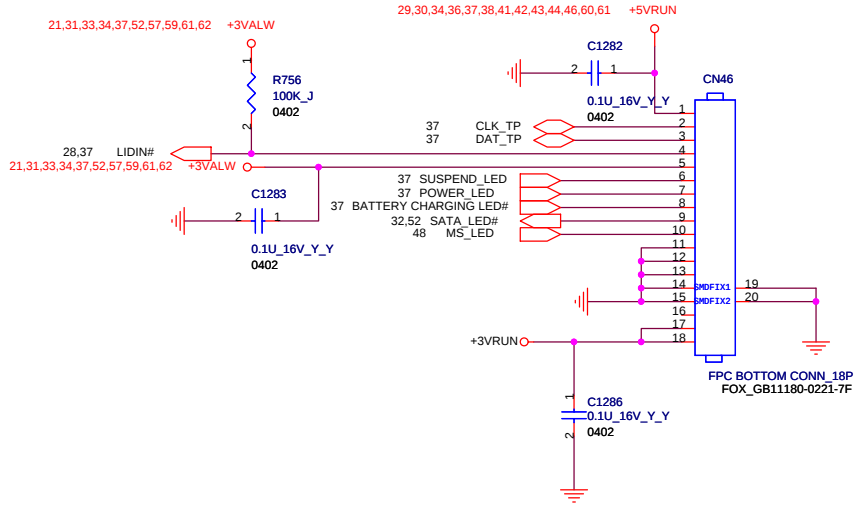
ID5	ID4	ID3	ID2	ID1	ID0	
1	0	0	1	1	1	L(945GM)
1	0	0	1	0	1	L(940GML)
1	0	0	1	1	0	M(672M)
1	0	0	1	0	0	H(673M)

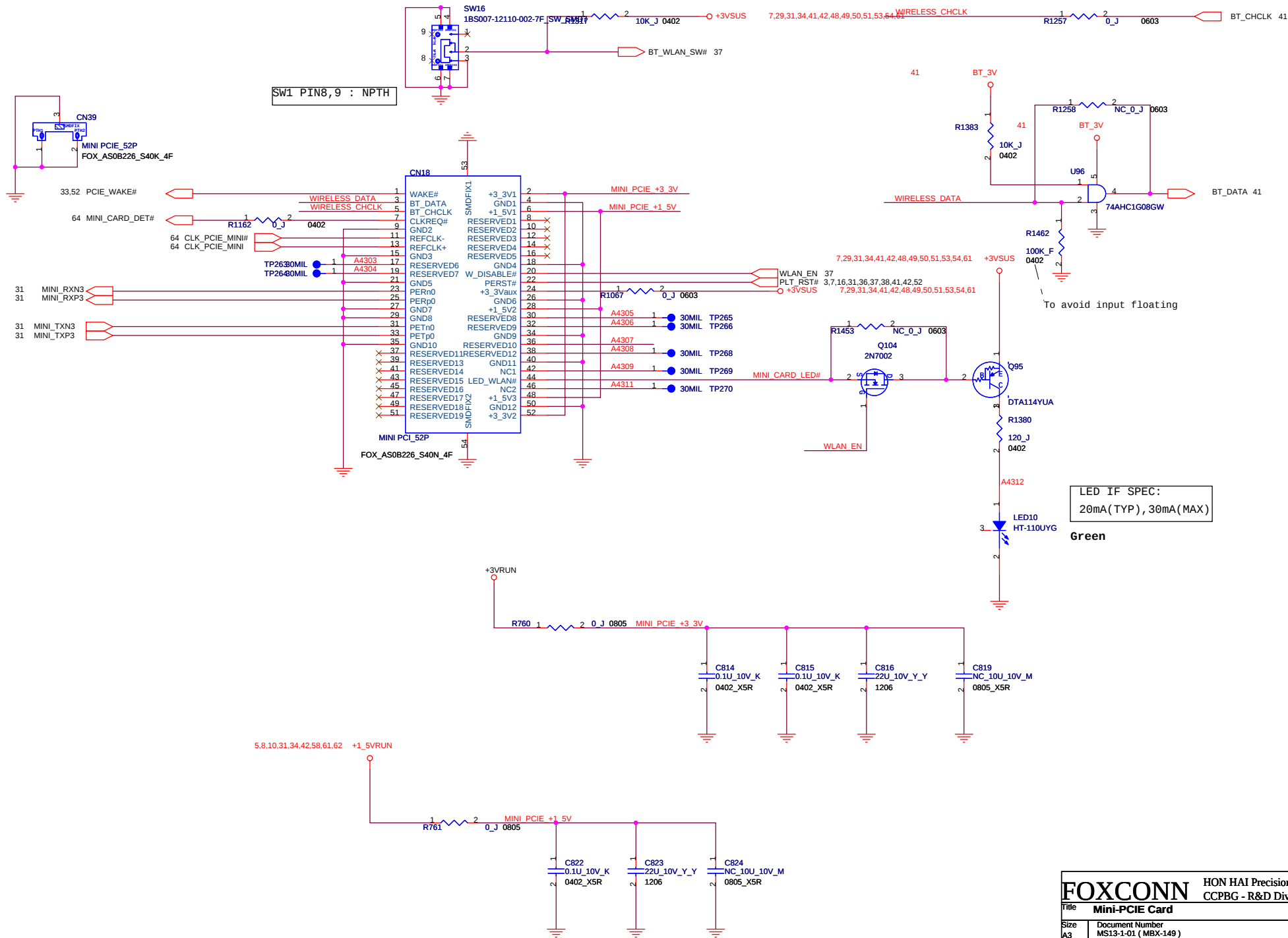


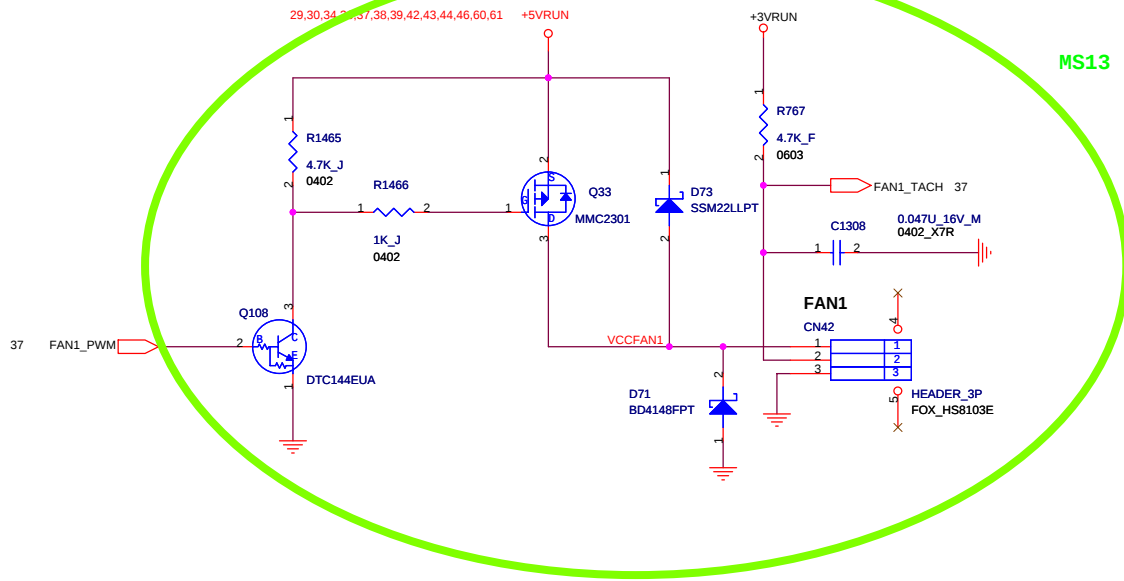


JIG-120

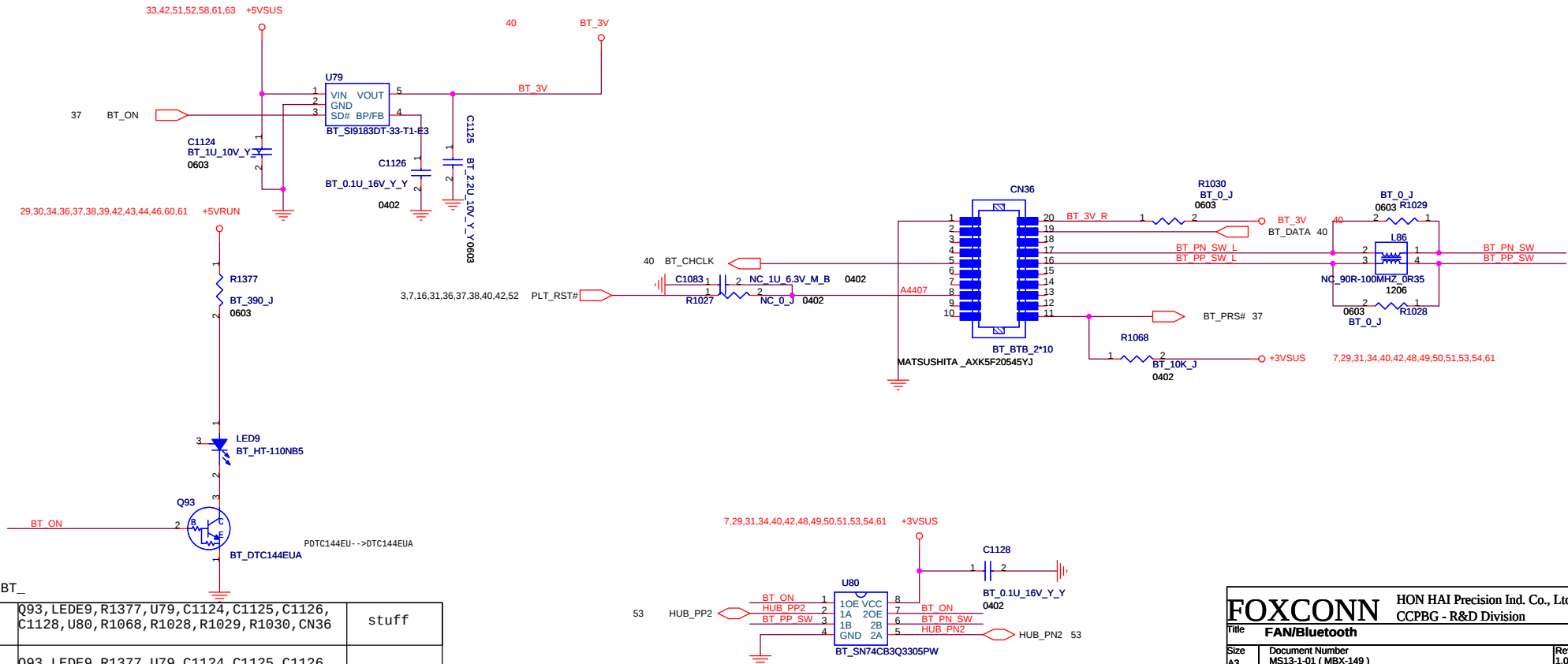








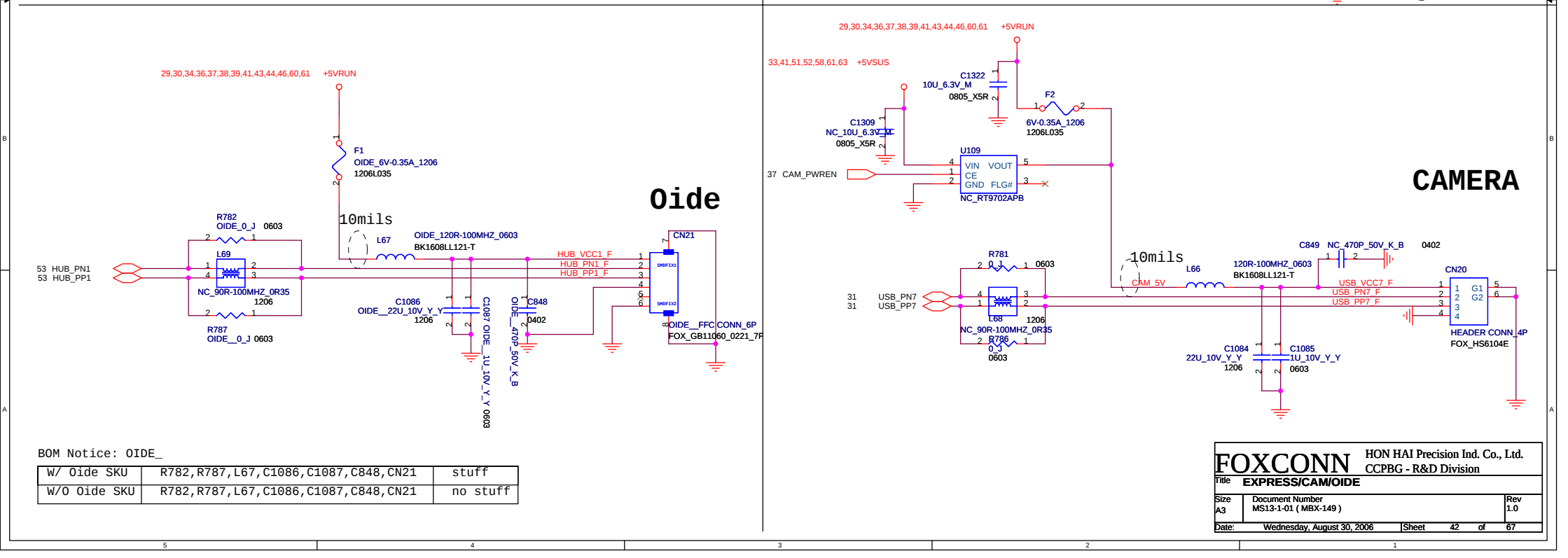
MS13 DVT Modify

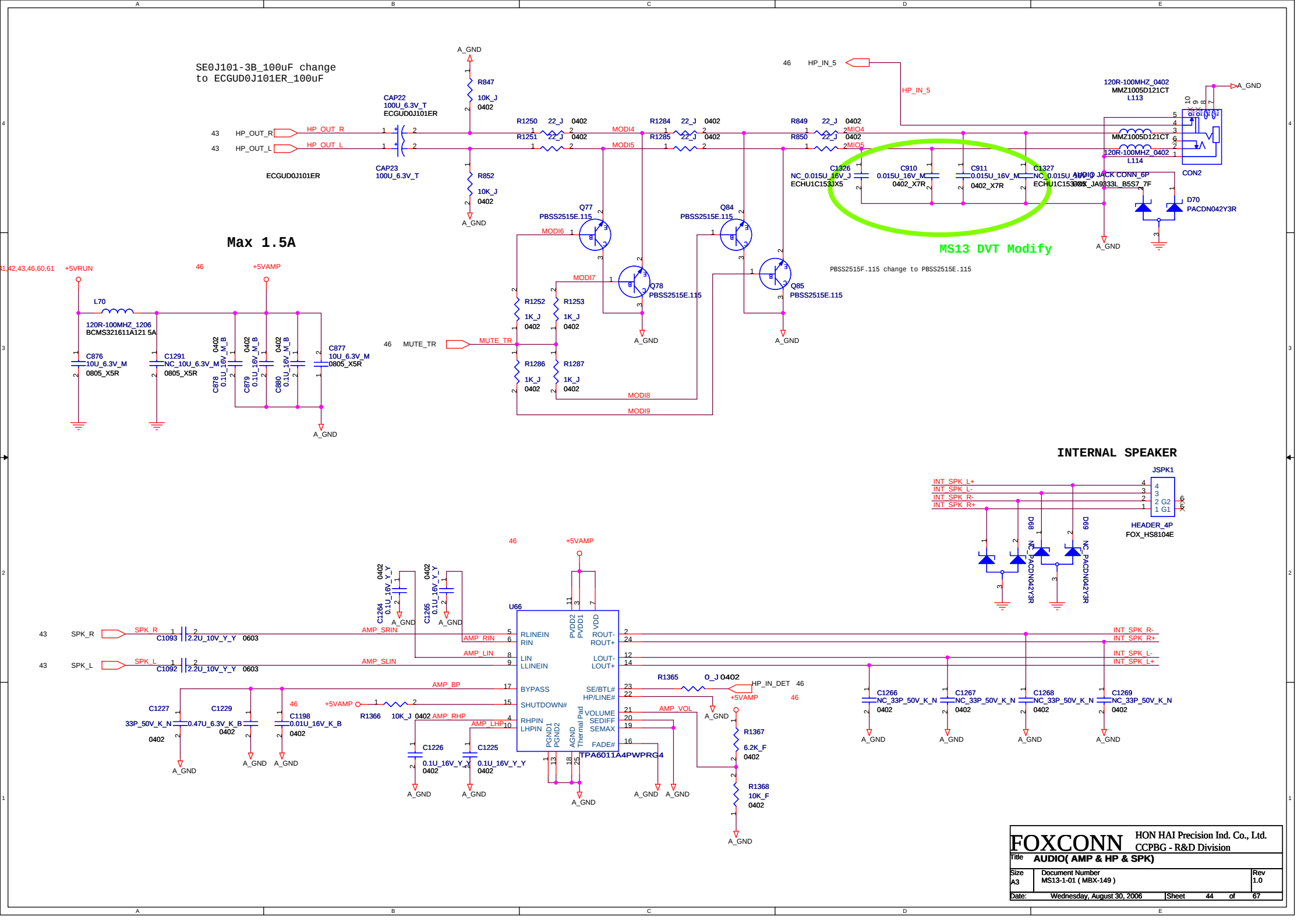


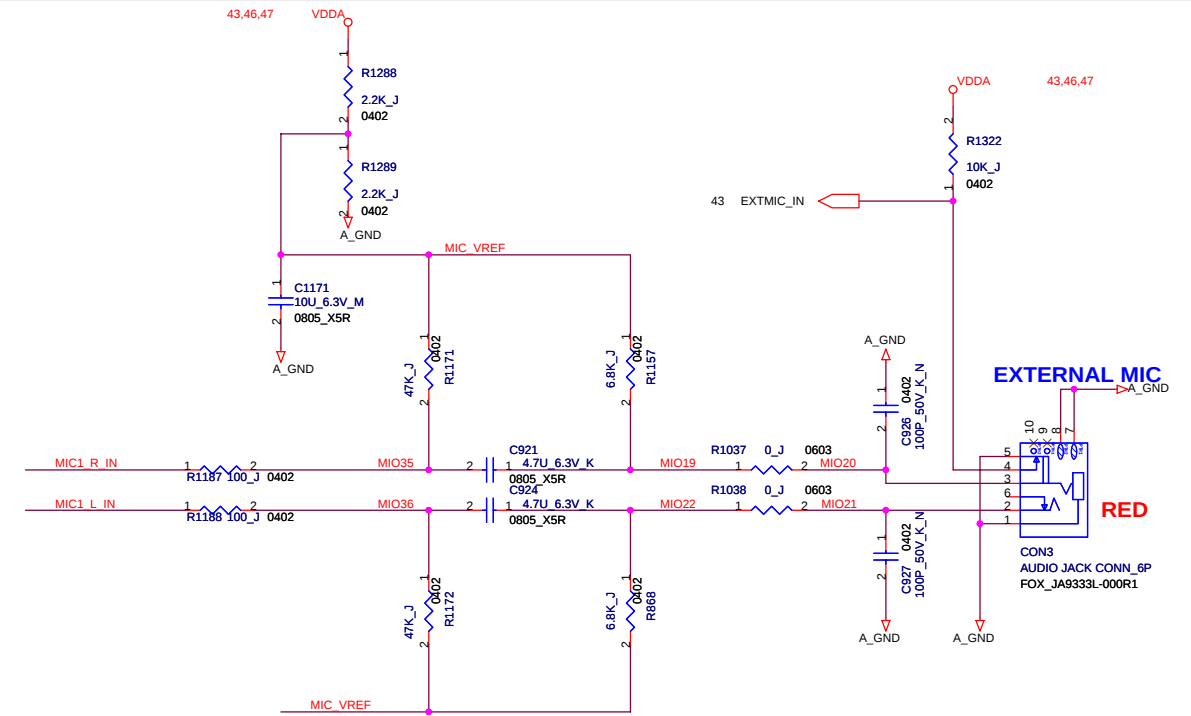
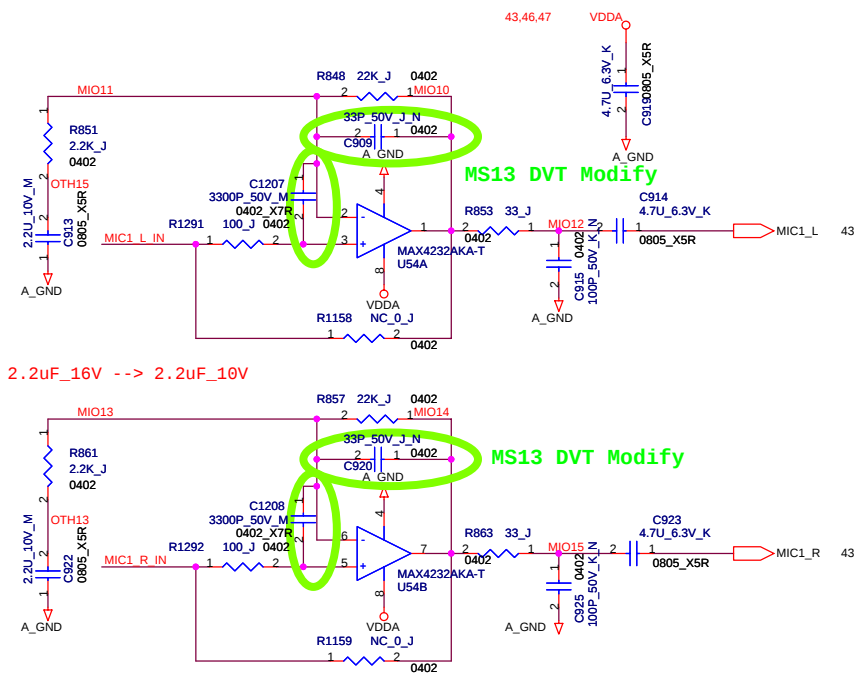
BOM Notice: BT_

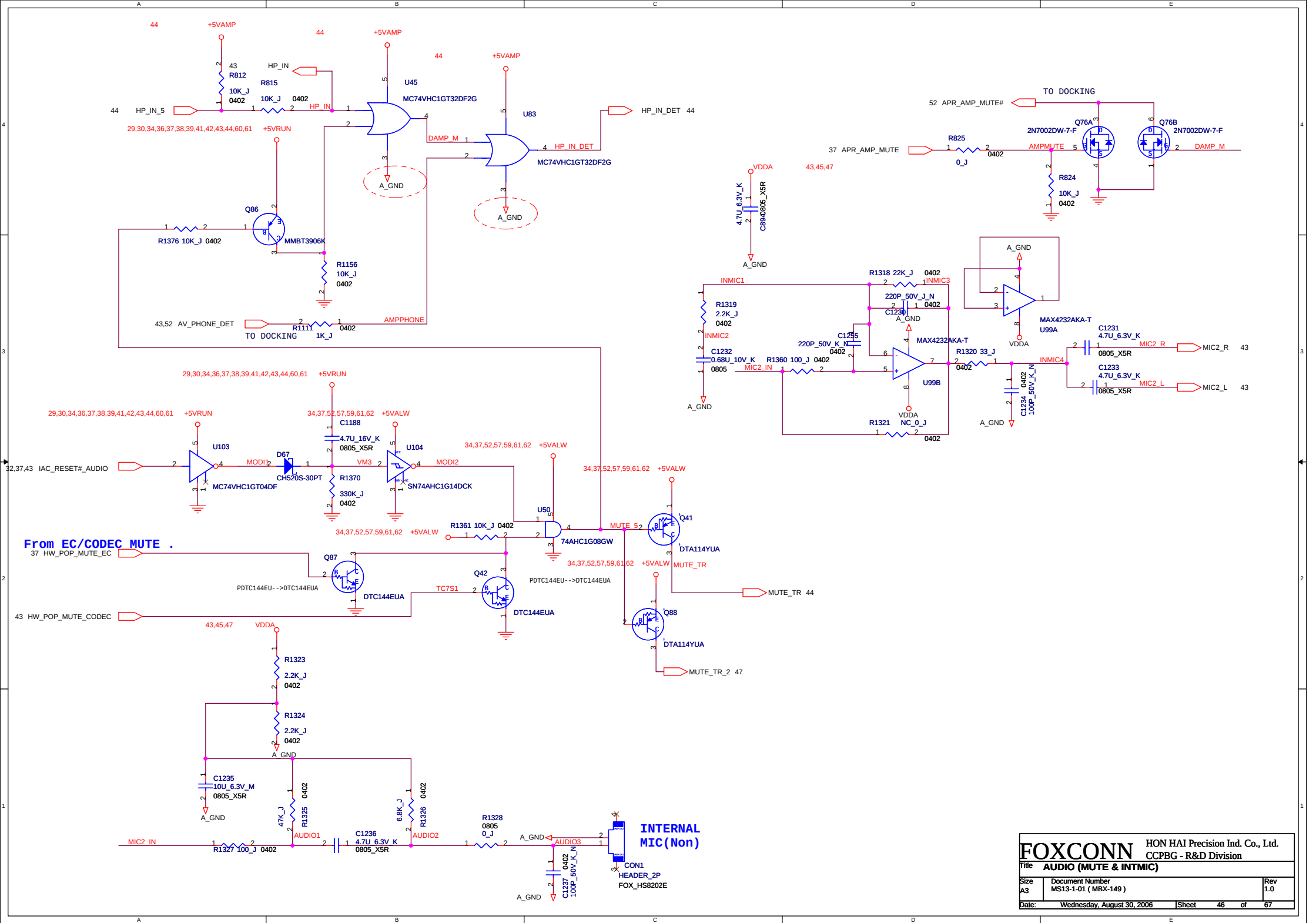
W/ BT SKU	Q93, LEDE9, R1377, U79, C1124, C1125, C1126, C1128, U80, R1068, R1028, R1029, R1030, CN36	stuff
W/O BT SKU	Q93, LEDE9, R1377, U79, C1124, C1125, C1126, C1128, U80, R1068, R1028, R1029, R1030, CN36	no stuff

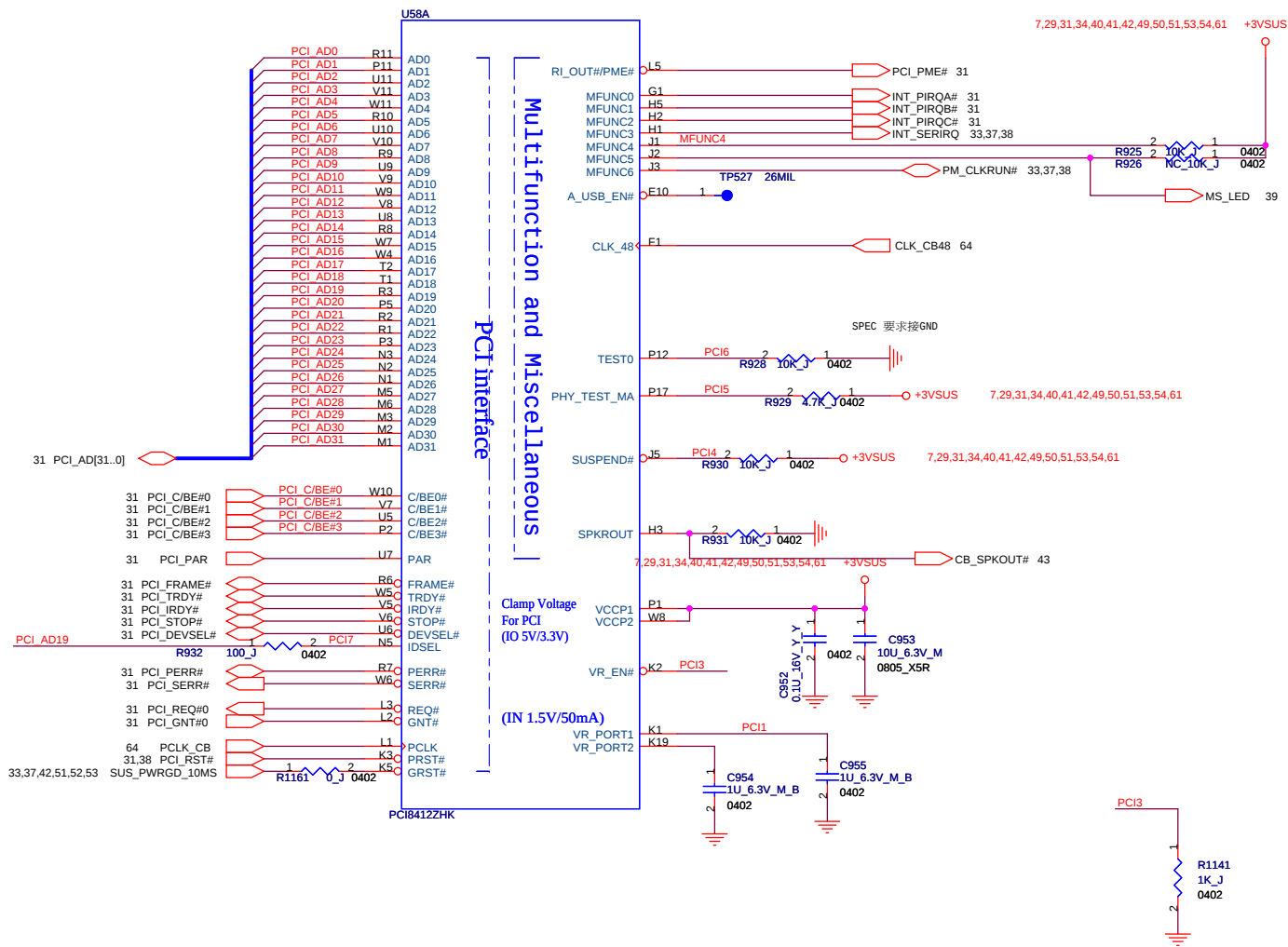
FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title FAN/Bluetooth		CCPBG - R&D Division	
Size A3	Document Number MS13-1-01 (MBX-149)	Rev 1.0	
Date: Wednesday, August 30, 2006	Sheet 41	of 67	











This array must be placed close to VDPLL (Pin U19)
They must be tied to a low-impedance GND.

This array must be placed close to AVDD (Pin P13,P14,U15)
They must be tied to a low-impedance GND.

This capacitor should be placed between Pin P15 and Pin R17 .

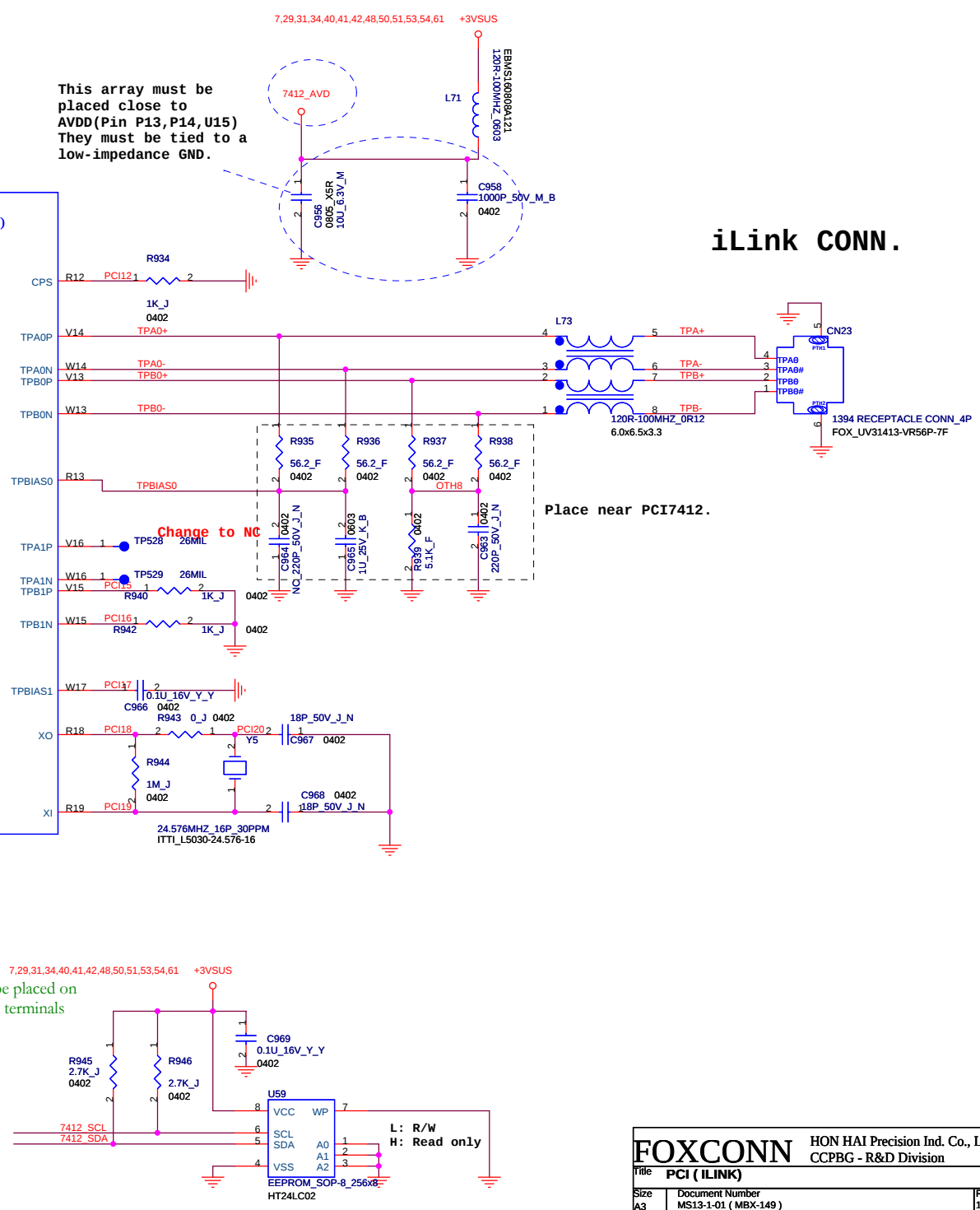
This capacitor must be placed to IC pin

VSSPLL must be tied to a low-impedance GND.

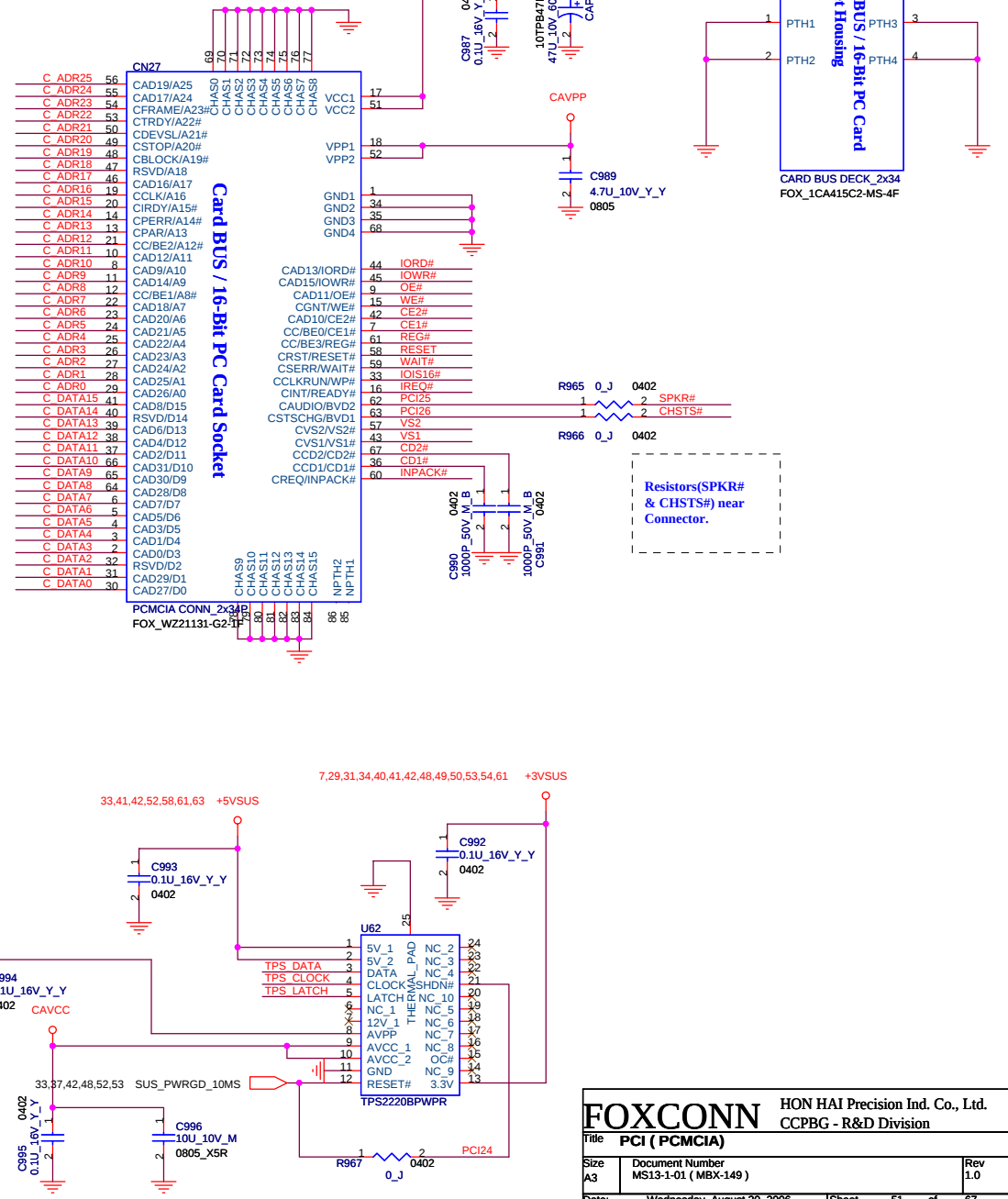
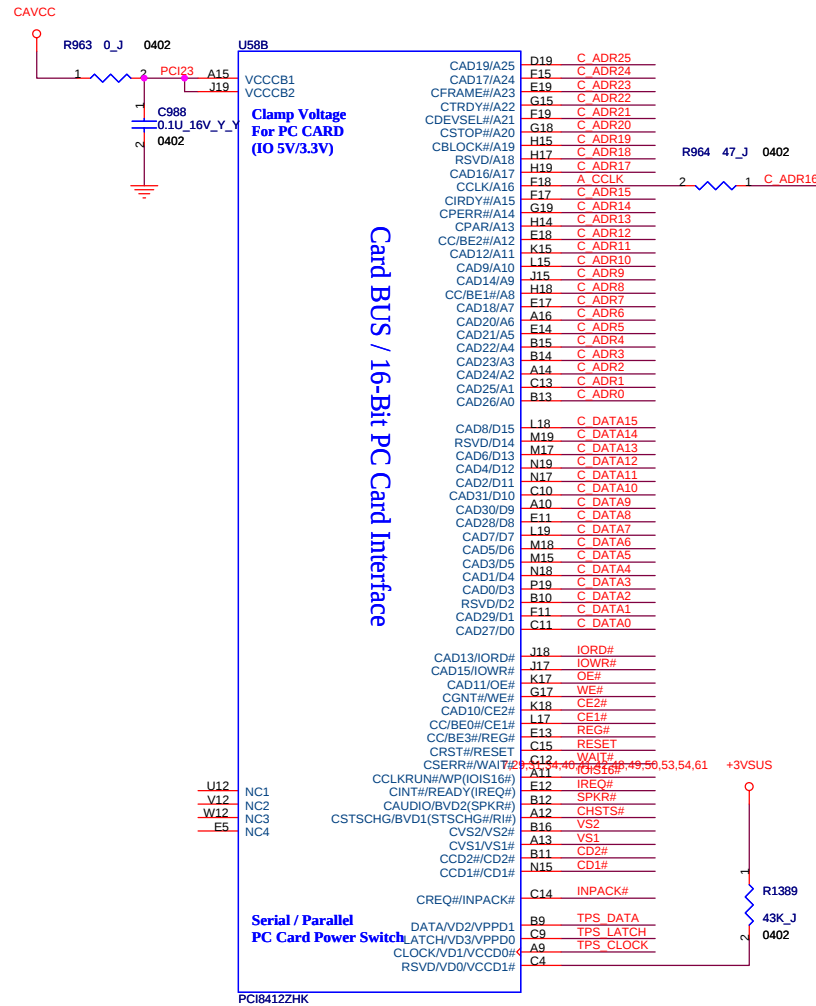
iLink CONN.

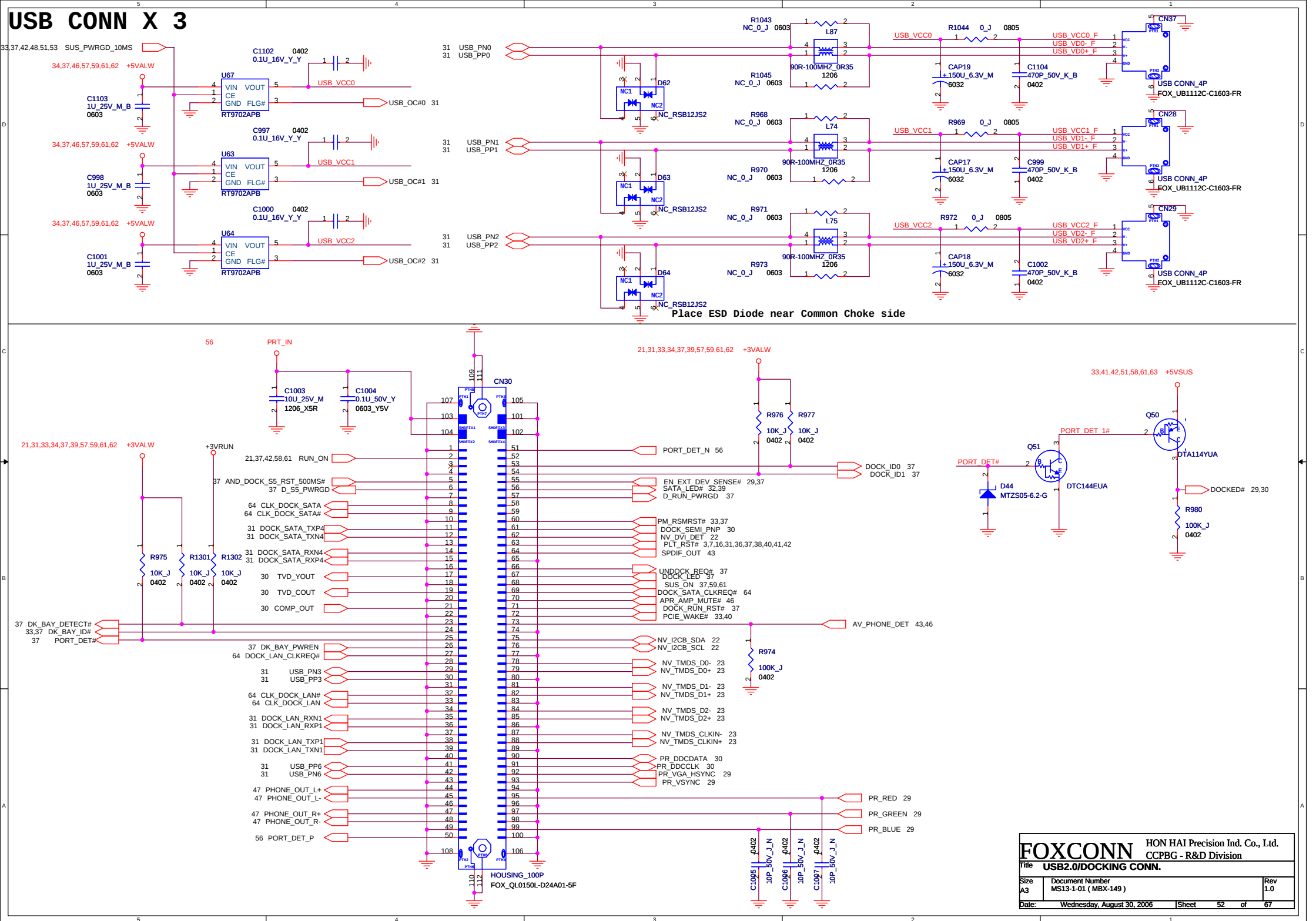
Place near PCI7412.

Resistors should be placed on the SCL and SDA terminals



PCMCIA CONN.





BOM notice:

	R1194	R1195
BT + OIDE SKU	30 ohm	30 ohm
BT SKU	0 ohm	0 ohm
OIDE SKU	0 ohm	0 ohm

BOM notice:

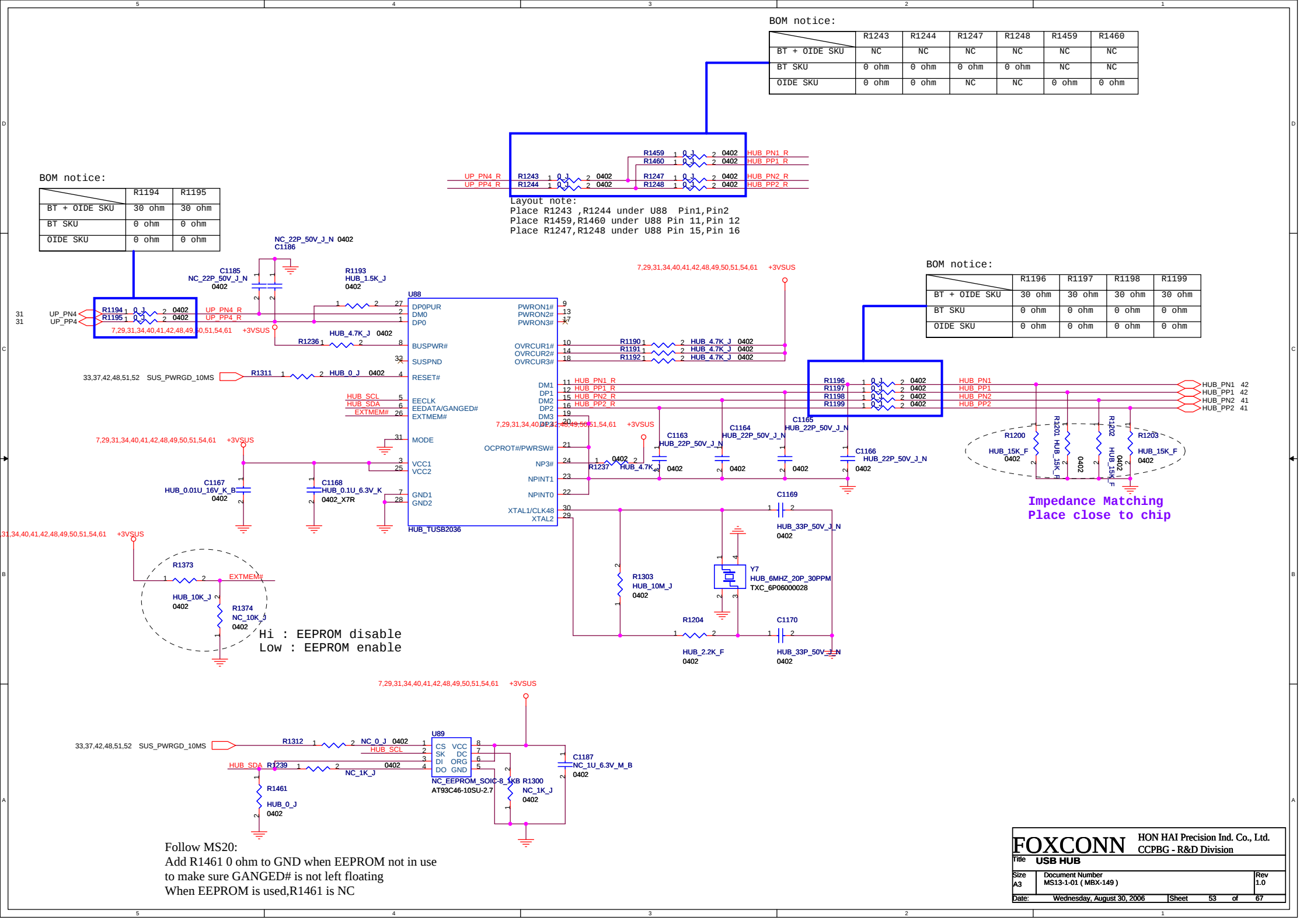
	R1243	R1244	R1247	R1248	R1459	R1460
BT + OIDE SKU	NC	NC	NC	NC	NC	NC
BT SKU	0 ohm	0 ohm	0 ohm	0 ohm	NC	NC
OIDE SKU	0 ohm	0 ohm	NC	NC	0 ohm	0 ohm

Layout note:

Place R1243 ,R1244 under U88 Pin1,Pin2
Place R1459,R1460 under U88 Pin 11,Pin 12
Place R1247,R1248 under U88 Pin 15,Pin 16

BOM notice:

	R1196	R1197	R1198	R1199
BT + OIDE SKU	30 ohm	30 ohm	30 ohm	30 ohm
BT SKU	0 ohm	0 ohm	0 ohm	0 ohm
OIDE SKU	0 ohm	0 ohm	0 ohm	0 ohm

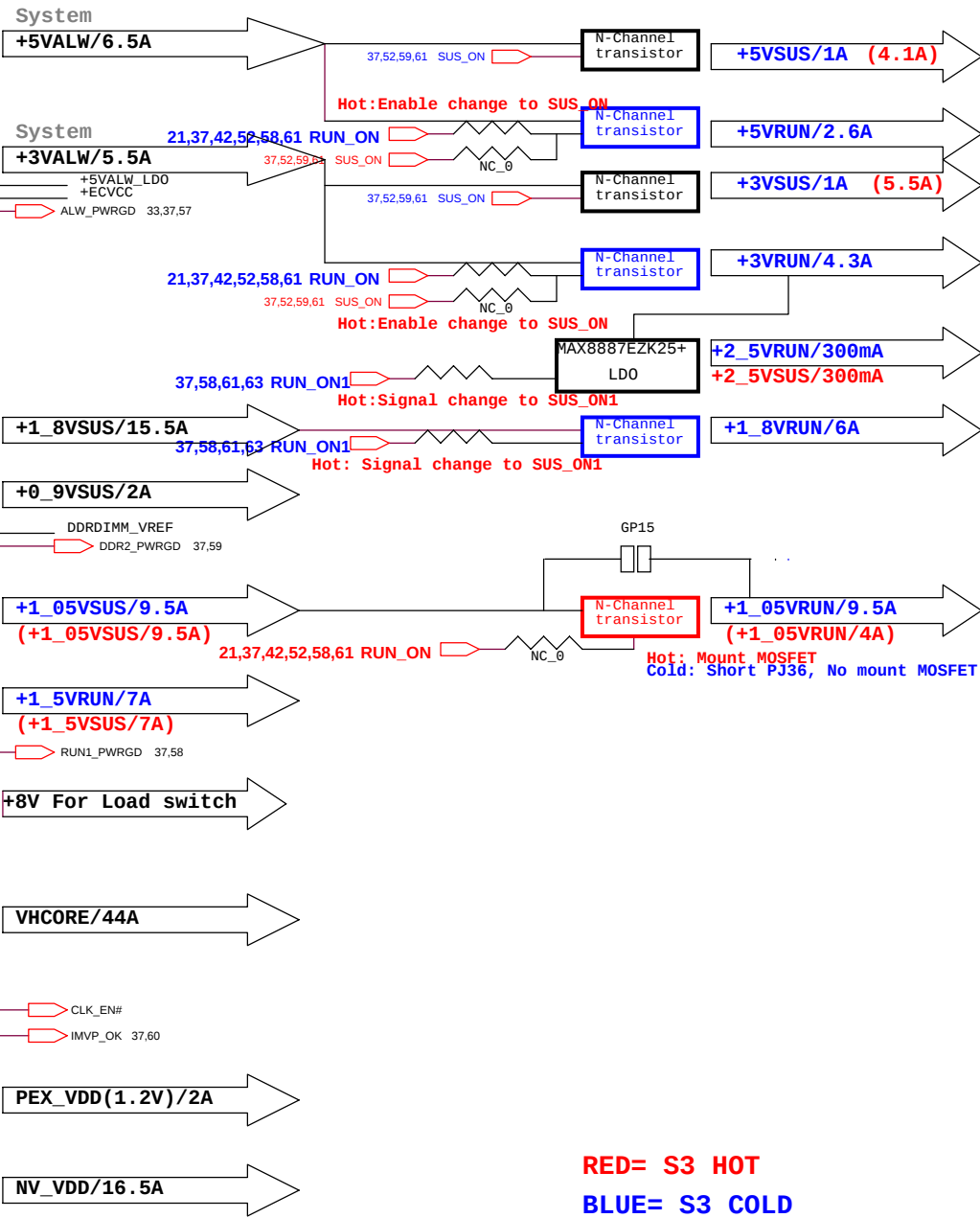
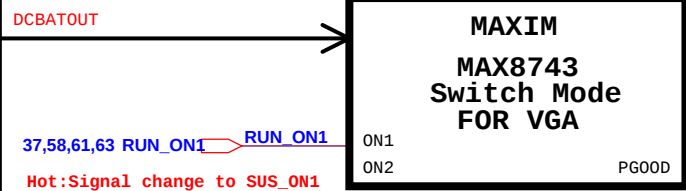
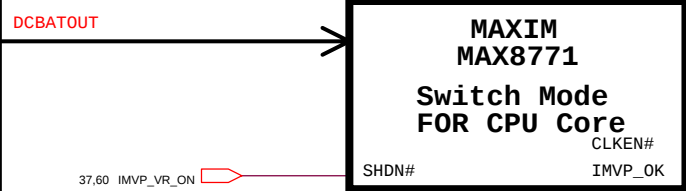
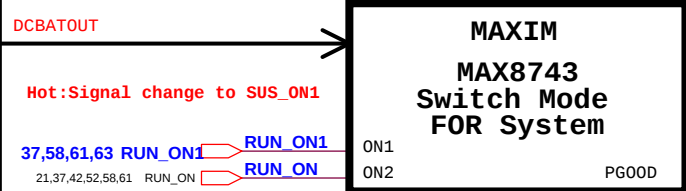
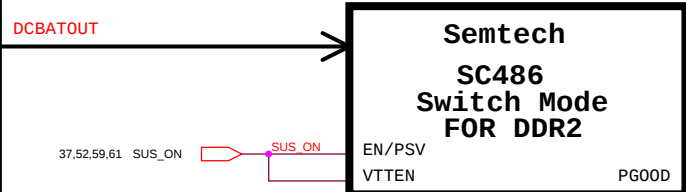
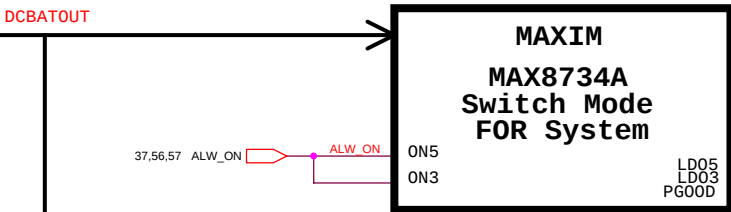
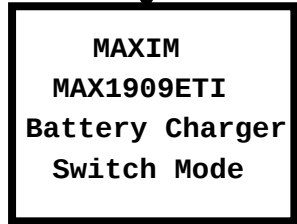
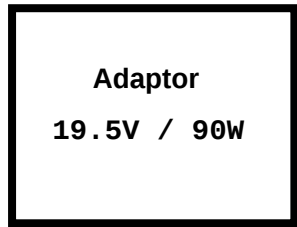


Follow MS20:

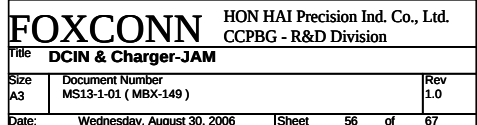
Add R1461 0 ohm to GND when EEPROM not in use
to make sure GANGED# is not left floating

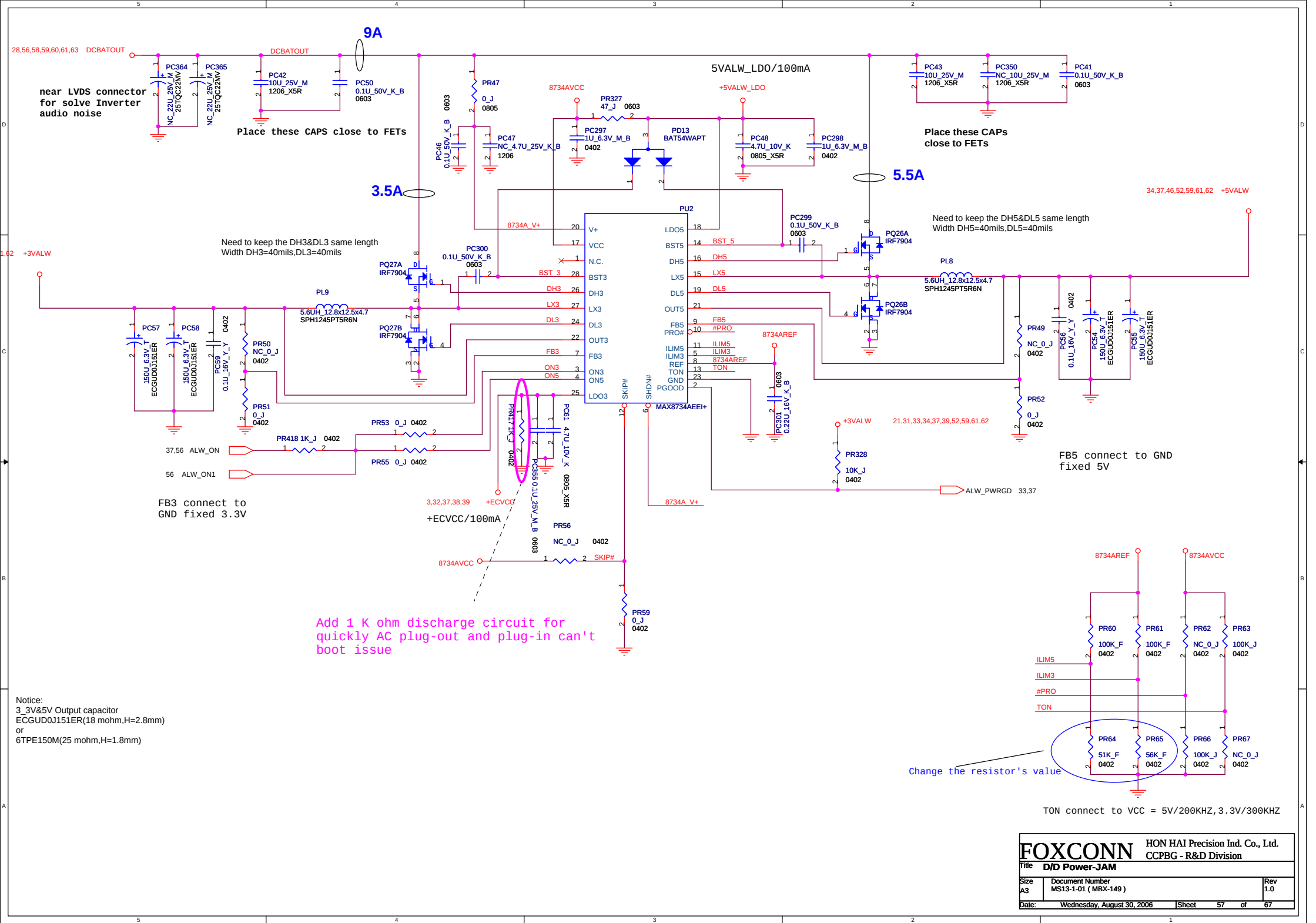
When EEPROM is used,R1461 is NC

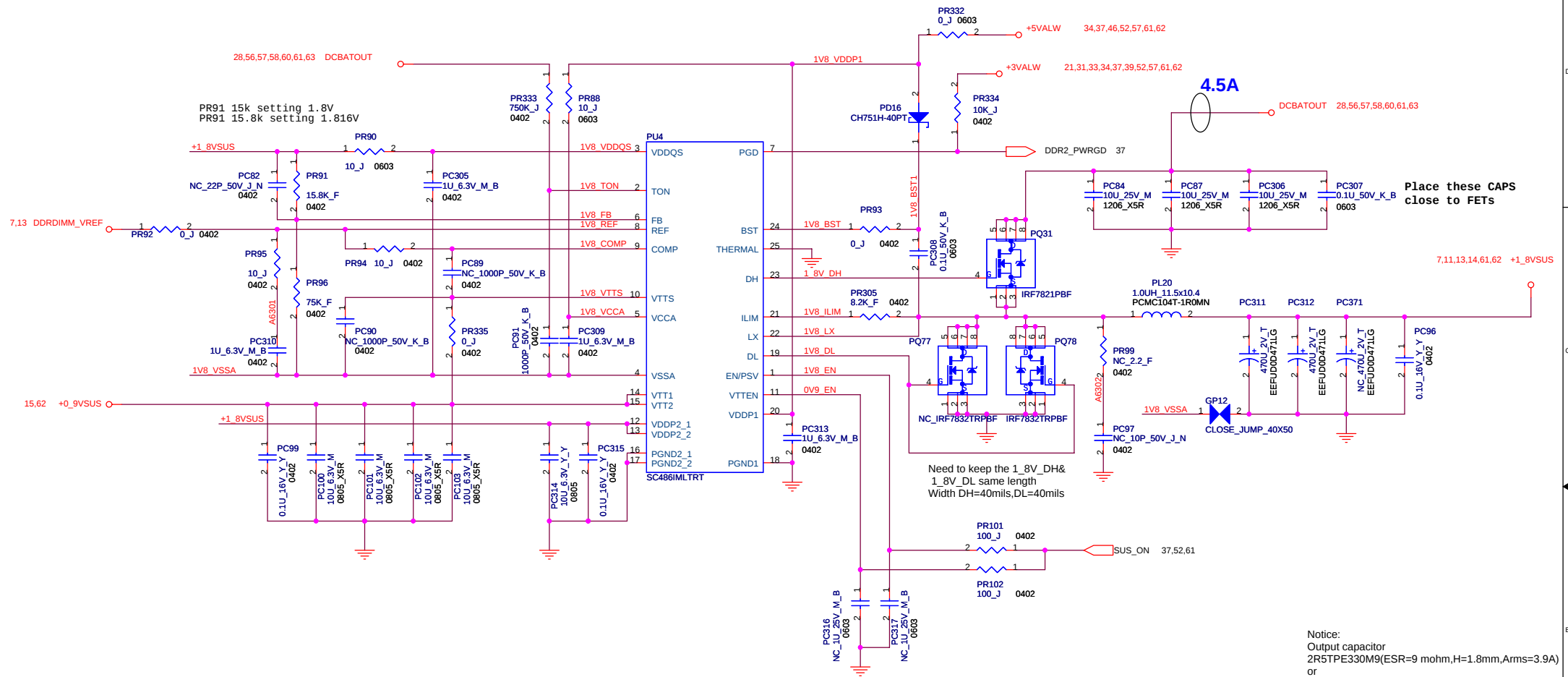
FOXCONN			HON HAI Precision Ind. Co., Ltd.	
Title			CCPBG - R&D Division	
Size			Document Number	
A3			MS13-1-01 (MBX-149)	
Date:			Rev	
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RED= S3 HOT
BLUE= S3 COLD

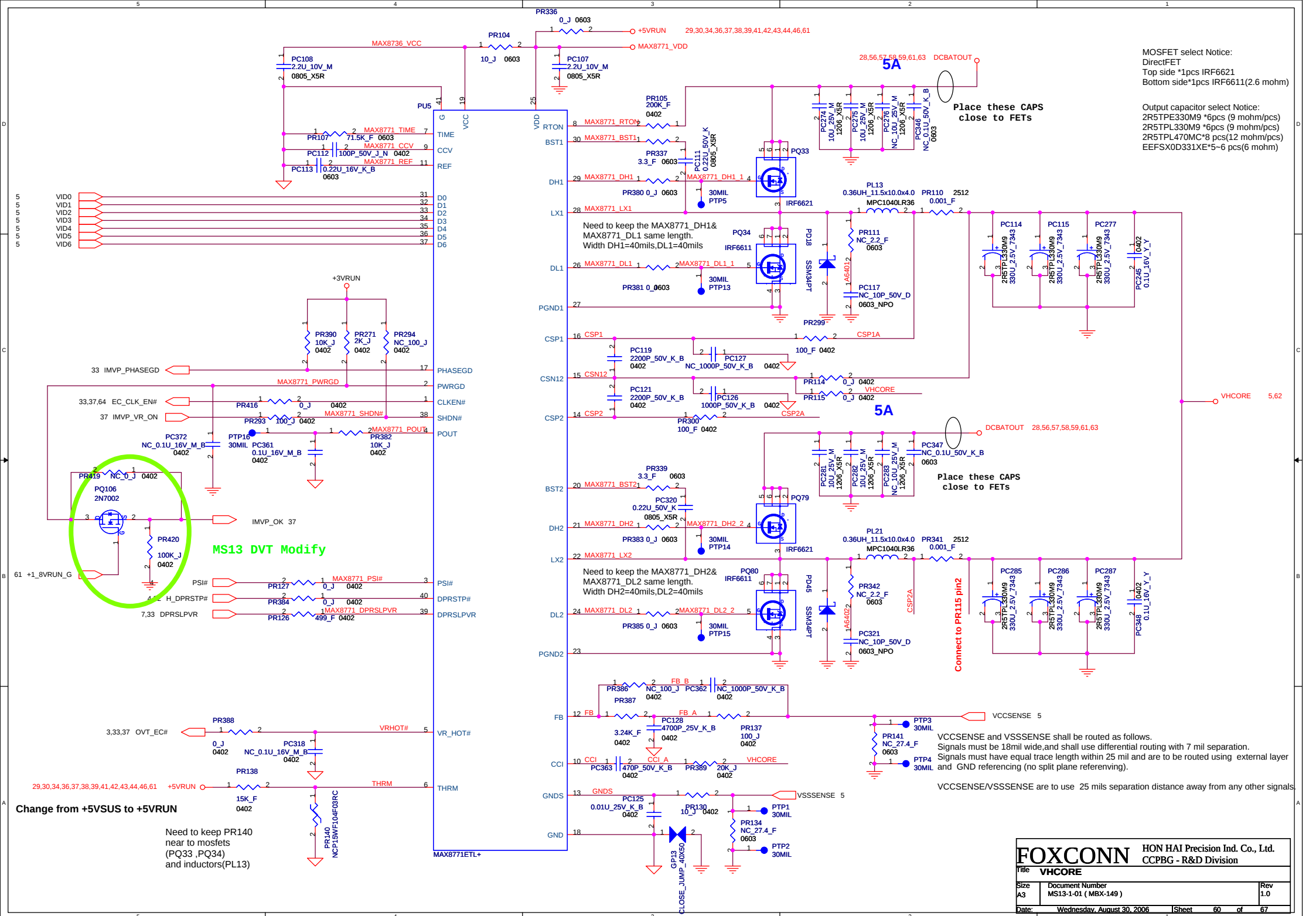






Notice:
Output capacitor
2R5TPE330M9(ESR=9 mohm,H=1.8mm,Arms=3.9A)
or
EEFSX0D331ER(ESR=9mohm,H=1.9mm,Arms=3.0A)

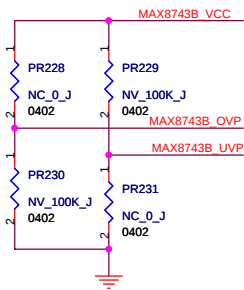
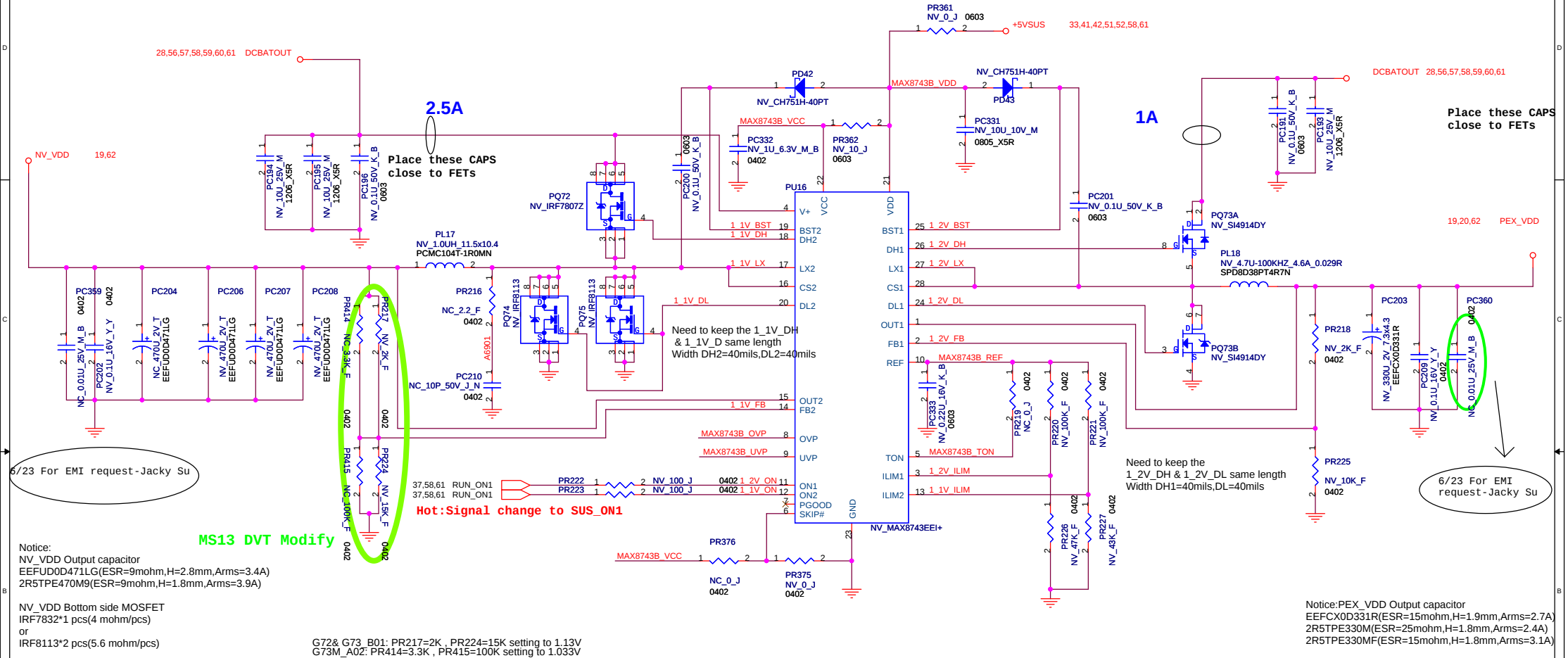
Bottom side MOSFET
IRF7832*1 pcs(4 mohm/pcs)
or
IRF7811*2 pcs(14 mohm/pcs)



Control ACIN OCP protect

LMC7225IM5X change to NCS2202SN1T1G

5/16 Change +5VRUN to +5VSUS



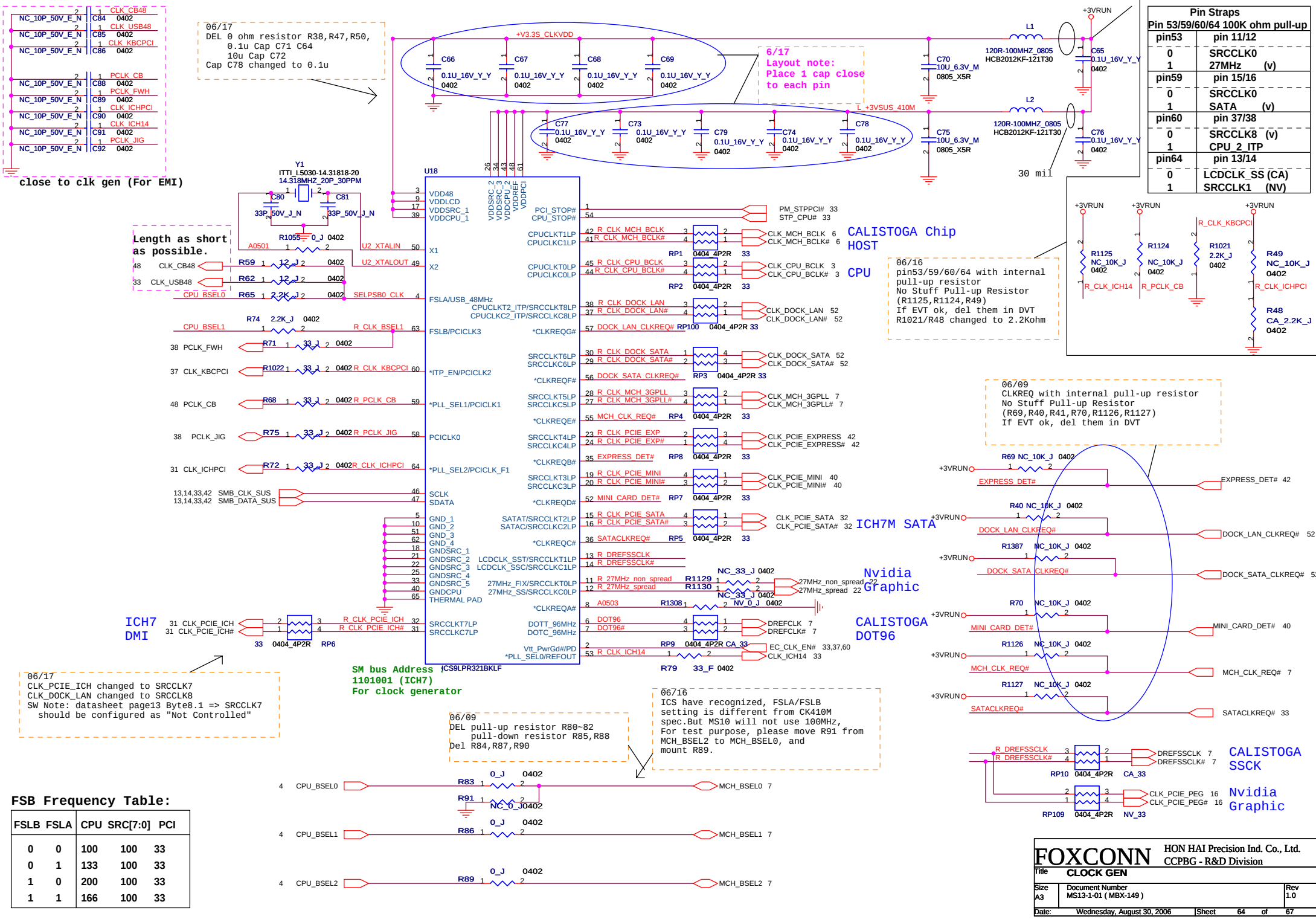
NV_VDD=Vfb * (1+R1/R2)
Vfb=1V
R1=PR217 or PR414
R2=PR224 or PR415

NC_10P_50V_E_N	2	1	CLK_CB48
NC_10P_50V_E_N	2	1	CLK_USB48
NC_10P_50V_E_N	2	1	CLK_KBCPCI
NC_10P_50V_E_N	2	1	PCLK_CB
NC_10P_50V_E_N	2	1	PCLK_FWH
NC_10P_50V_E_N	2	1	CLK_ICHPCI
NC_10P_50V_E_N	2	1	CLK_ICH14
NC_10P_50V_E_N	2	1	PCLK_JIG
NC_10P_50V_E_N	2	1	C92

06/17
DEL 0 ohm resistor R38, R47, R50,
0.1u Cap C71 C64
10u Cap C72
Cap C78 changed to 0.1u

close to clk gen (For EMI)

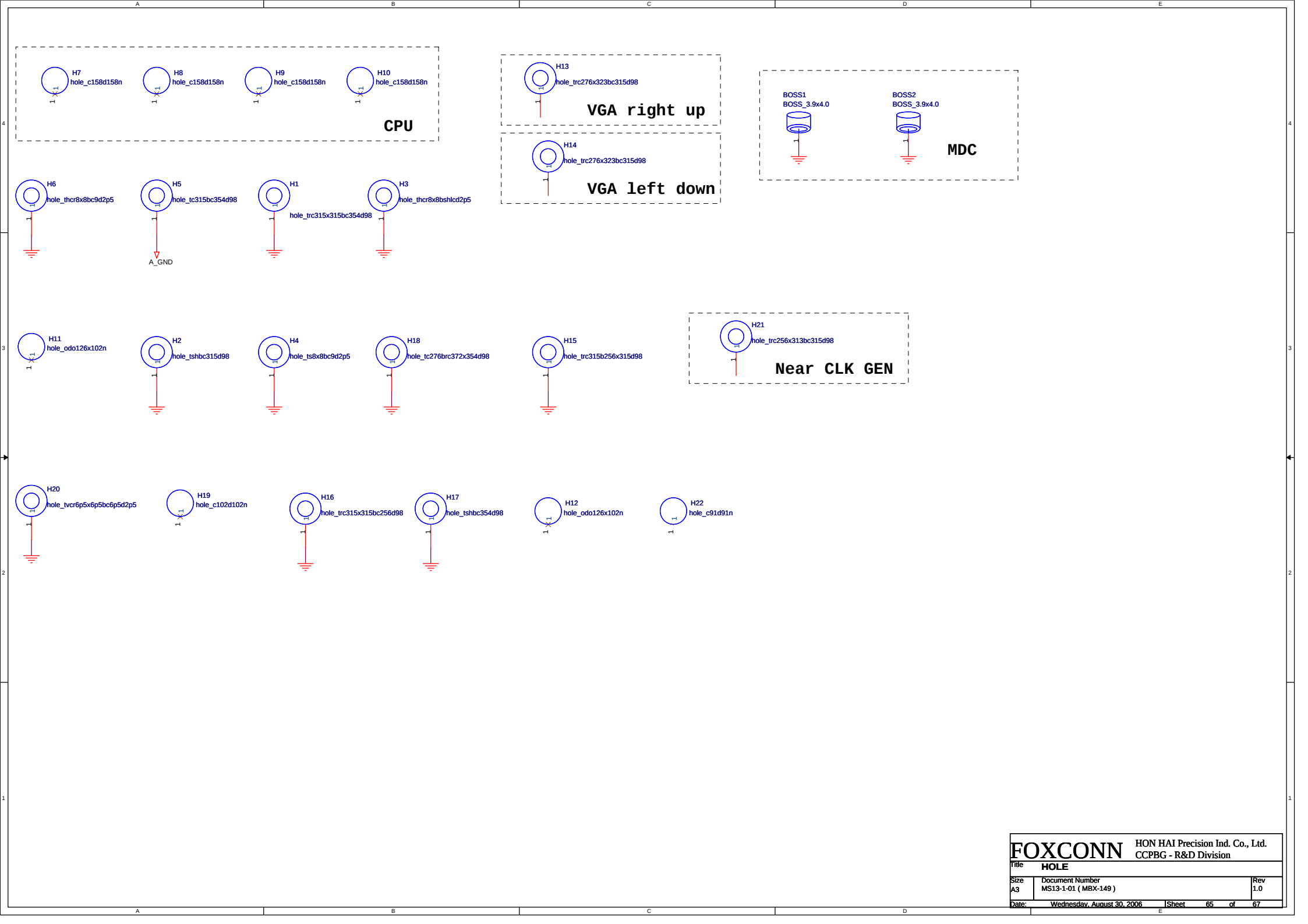
Length as short as possible.



Pin Straps			
Pin 53/59/60/64 100K ohm pull-up		pin 11/12	
pin53	pin 11/12	pin 15/16	
0	SRCCLK0	SRCCLK0	(v)
1	27MHz	SATA	(v)
pin59	pin 37/38	CPU 2 ITP	
0	SRCCLK8	CPU 2 ITP	(v)
1	SATA	CPU 2 ITP	(v)
pin60	pin 13/14	LCDCLK_SS (CA)	
0	SRCCLK8	LCDCLK_SS (CA)	(v)
1	SATA	LCDCLK_SS (CA)	(v)

FSB Frequency Table:

FSLB	FSLA	CPU SRC[7:0]	PCI
0	0	100	100
0	1	133	100
1	0	200	100
1	1	166	100



HISTORY

(2006/08/16 Initail REV 1.0)

P.02 Because MS13 only use G73B01 version, since we delete head value of NV7273B01_ and NV73A02_.

P.63 Change head value as below: PR217(NV7273B01_2K_F-->NV_2K_F) PR224(NV7273B01_15K_F-->NV_15K_F) PR414(NV73A02_3_3K_F-->NC_3_3K_F) PR415(NV73A02_100K_F-->NC_100K_F)

P.45 Change C909,C920 from 220P_50V_J_N to 100P_50V_K_N. The change will make Frequency Response pass VISTA requirement.

P.43 Change U39 from CXD9872KXXNBEB2XR to CXD9872AKDNBEC3XR(4th+).

P.56 Change PR377 from 1K_F to 15K_F to avoid resistor damage when OVP occur.

P.60 Add PQ106, PR420 to prevent glitch occur on the IMVP_OK signal.

P.41 Change fan control circuit as same as MS20.

P.03 Reserve U110, R1467, C1324 for RTC stop issue.

P.37 Add Q110 for RTC stop issue.

P.37 Reserve D74 for RTC stop issue.

P.44 Change C910, C911 from 0.033uF to 0.015uF and modify the size from 1206 to 0402 for co-layout. And we also add C1326, C1327 to keep 1206 size.

P.47 Change R1330, R1339 from 10K to 9.1K and Change C1238, C1242 from 270pf to 150pf then the phone out D/A will pass.

P.37 Add Q109, Q110 to prevent ACIN, BATT_PR# and ENCHG# is faster than ECVCC.

(2006/08/18)

P.33 Change R633 from 100_J to 1K_J and add D75 for PM_RSMRST# falling timing fail issue.

P.56 Change PR369 from NC_0_J to 15K_J to make BATT_PR# signal high level from 5V to 3.3V.

P.10 Correct +1_5VRUN maximum current description from 1885mA to 1900mA.

P.11 Correct +1_05VSUS maximum current description from 4.6A to 3.5A.

P.11 Correct +1_8VSUS maximum current description from 3.1A to 3.2A.

(2006/08/22)

P.33 Correct D75 from NC_CA_SCS500V-40-LF to SCS500V-40-LF.

P.41 Correct C1308 from NC_0.01U_25V_K_B to 0.047U_16V_M.

(2006/08/23)

P.45 Change C909,C920 from 100pF to 33pF and change C1207, C1208 from 220pF to 3300pF.
The Magnitude Response of Microphone(A-D) will be pass.

P.37 Correct D74 from NC_CA_SCS500V-40-LF to NC_SCS500V-40-LF.

(2006/08/24)

P.43 Change U39 from CXD9872AKDNBEC3XR(4th+ with dolby) to CXD9872AKXNBEC3XR(4th+ without dolby).

P.05 Change Cap1 from 330U_2V_T to NC_330U_2V_T.

P.11 Change Cap9 from 330U_2V_T to NC_330U_2V_T.

(2006/08/28)

P.36 Add VR1 for PACDN042Y3R shortage issue.

(2006/08/29)

P.37 For system ID change, since change R724 from 100K_J to NC_100K_J and change R725 from NC_100K_J to 100K_J.

(2006/08/30)

P.36 Change VR1 from NC_MS06A05T1V1_VR to MLVS0603M04_VR. And change D72 from PACDN042Y3R to NC_PACDN042Y3R.

P.37 Add R1470 for MS13 DVT combine list.

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

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