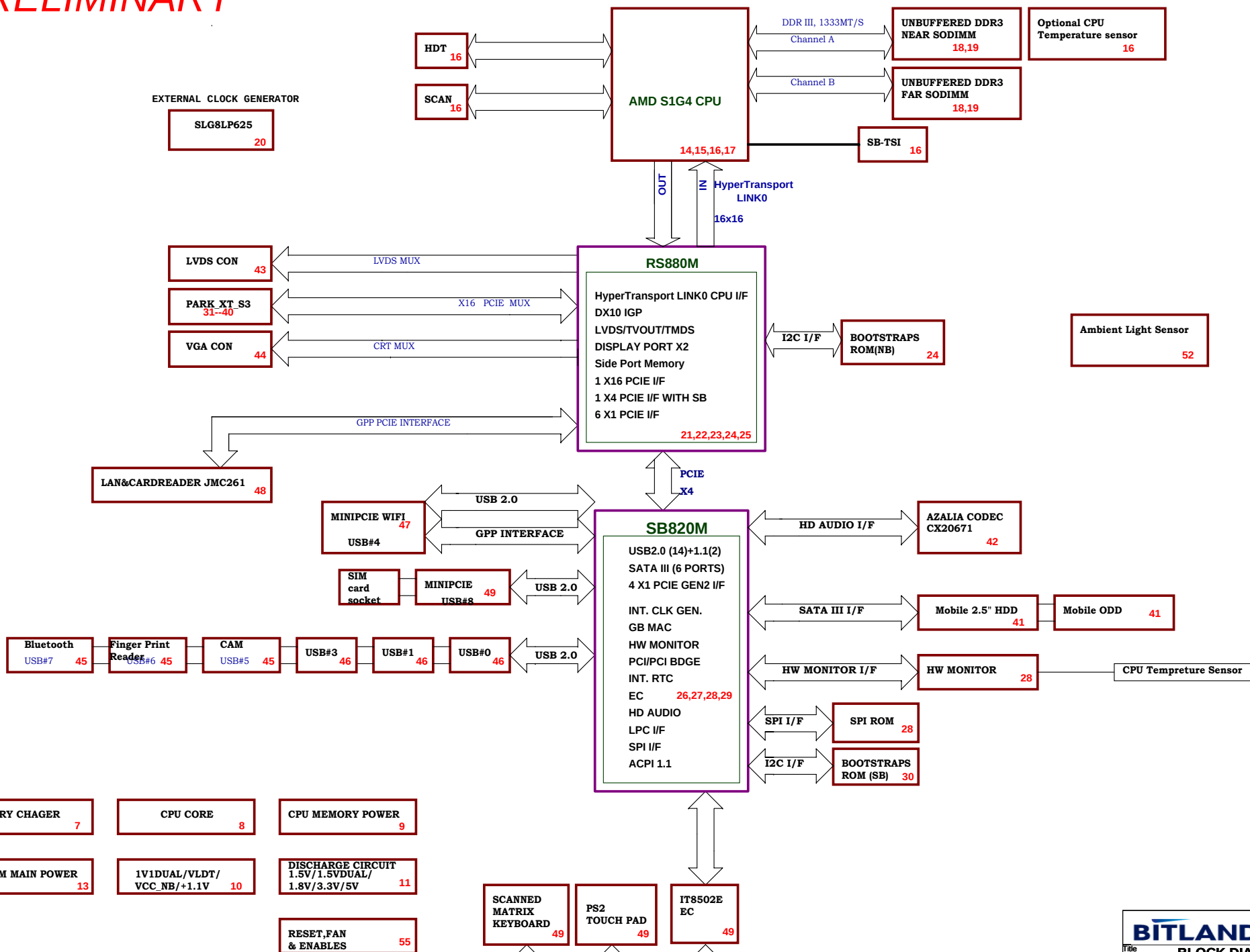


PRELIMINARY

GUAM S1G4 SCHEMATIC DESIGN

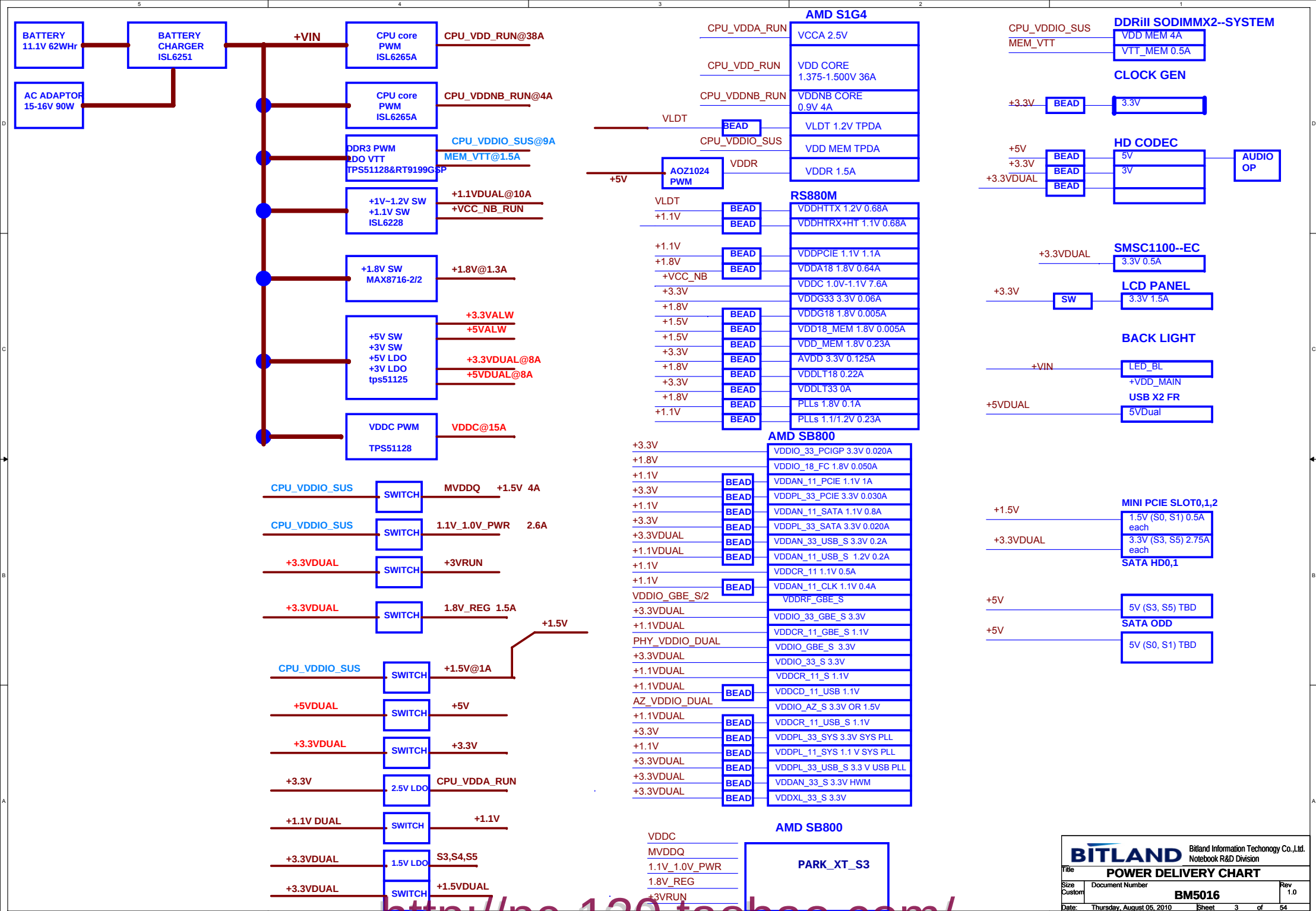


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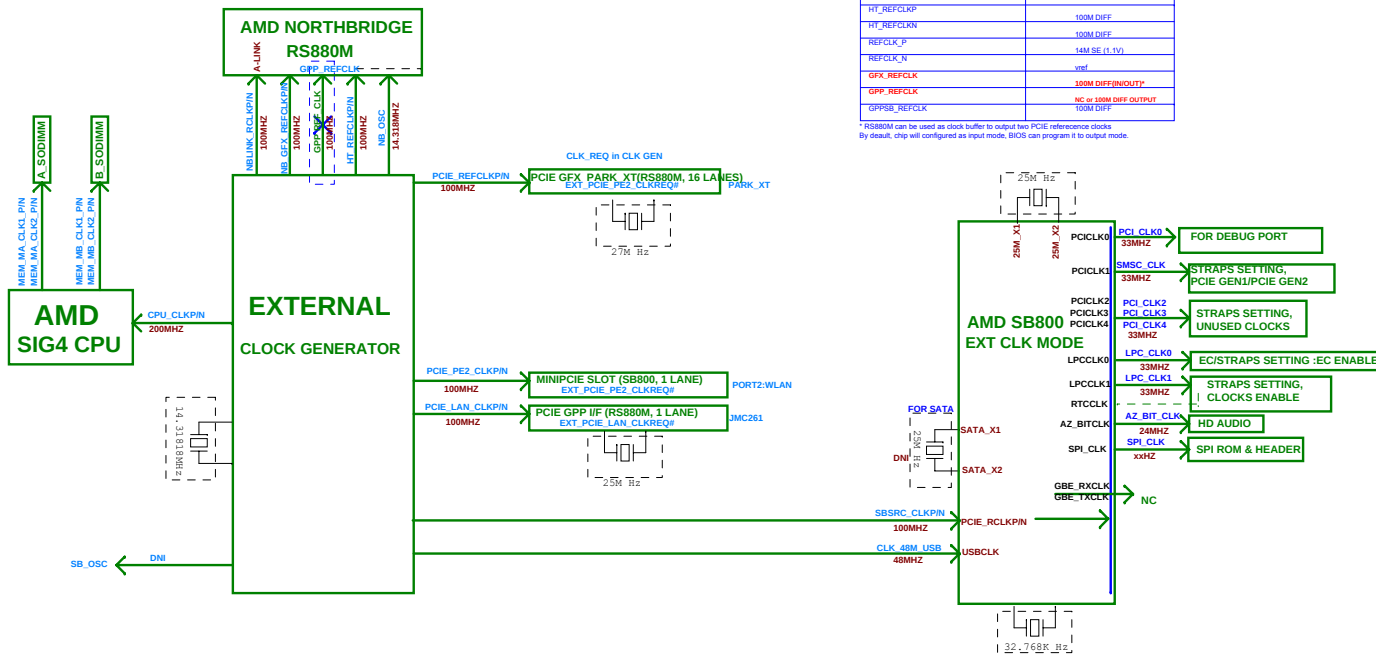
BITLAND		Bitland Information Techonogy Co.,Ltd. Notebook R&D Division	
TABLE OF CONTENTS			
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<http://pc-120.taobao.com/>

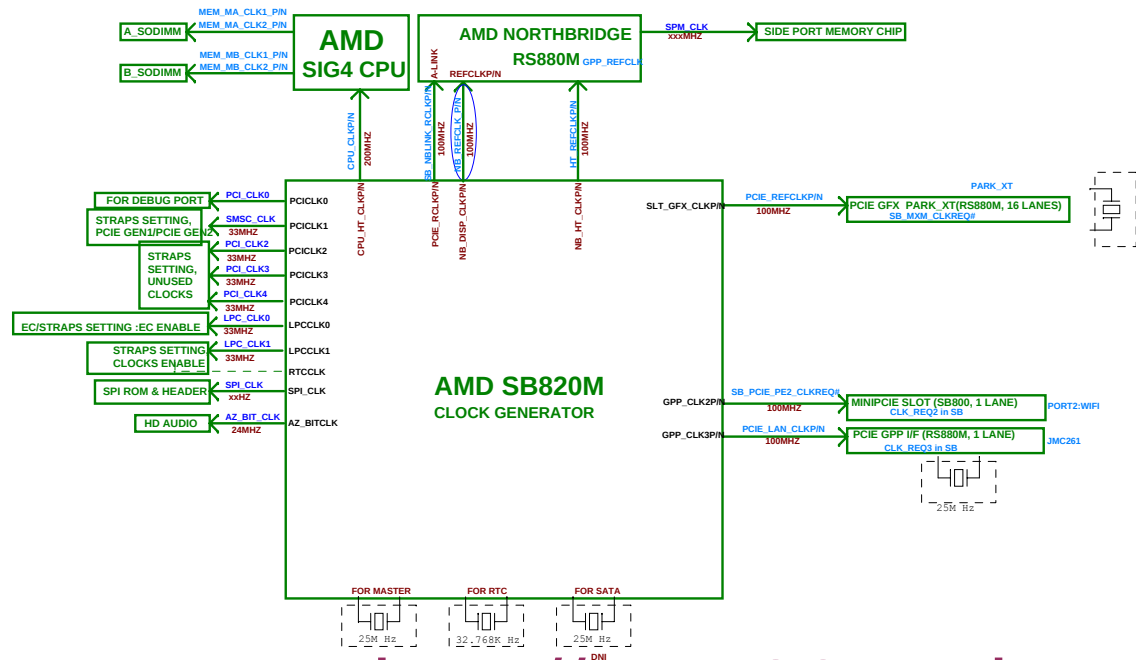


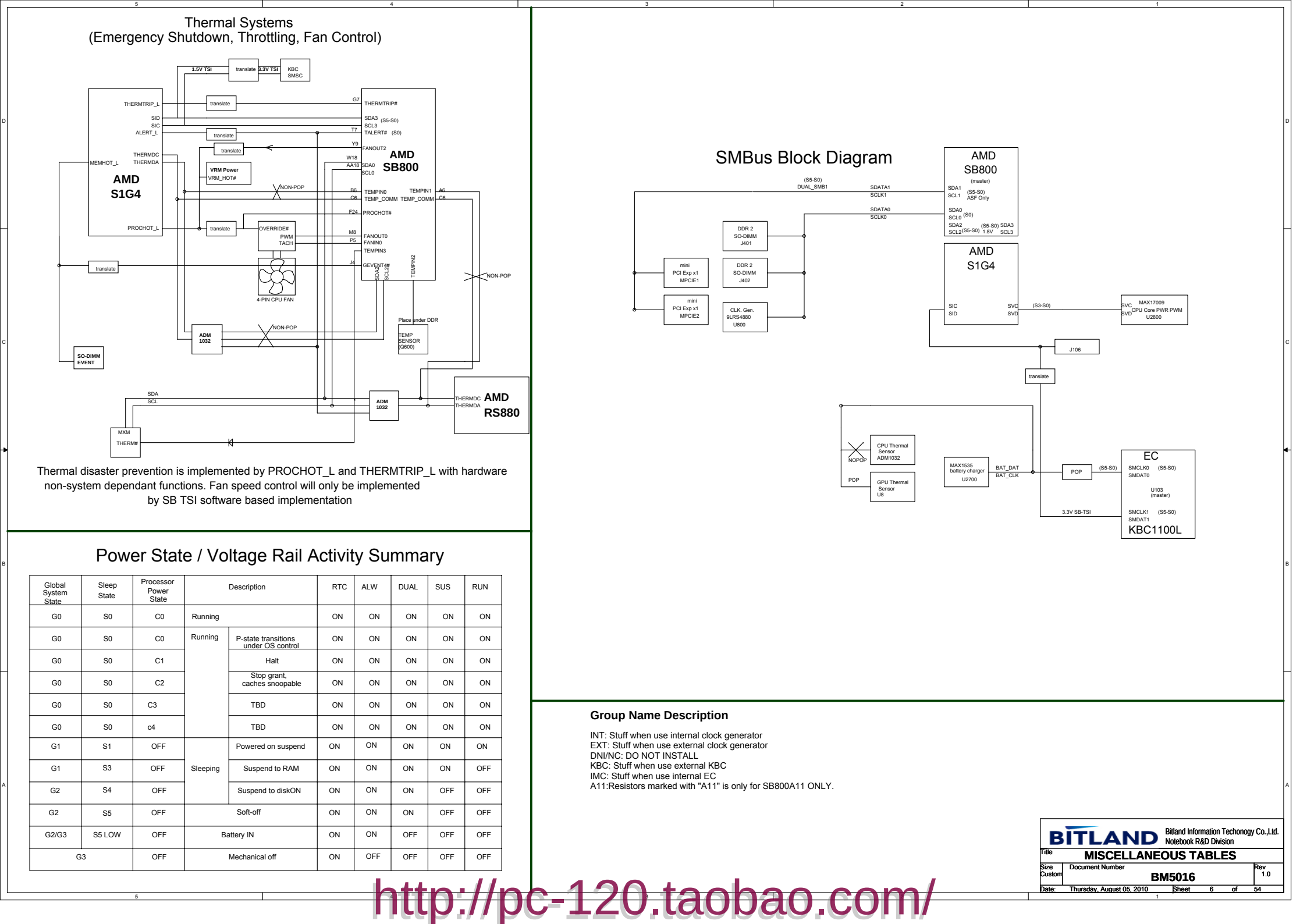
<http://pc-120.taobao.com/>

EXTERNAL CLOCK MODE



INTERNAL CLOCK MODE



[illegible][illegible]

D

C

B

A

Thermal Systems
(Emergency Shutdown, Throttling, Fan Control)

Thermal disaster prevention is implemented by PROCOT_L and THERMTrip_L with hardware non-system dependant functions. Fan speed control will only be implemented by SB TSI software based implementation

Power State / Voltage Rail Activity Summary

Global System State	Sleep State	Processor Power State	Description	RTC	ALW	DUAL	SUS	RUN
G0	S0	C0	Running	ON	ON	ON	ON	ON
G0	S0	C0	P-state transitions under OS control	ON	ON	ON	ON	ON
G0	S0	C1	Halt	ON	ON	ON	ON	ON
G0	S0	C2	Stop grant, caches snooperable	ON	ON	ON	ON	ON
G0	S0	C3	TBD	ON	ON	ON	ON	ON
G0	S0	c4	TBD	ON	ON	ON	ON	ON
G1	S1	OFF	Powered on suspend	ON	ON	ON	ON	ON
G1	S3	OFF	Suspend to RAM	ON	ON	ON	ON	OFF
G2	S4	OFF	Suspend to disk ON	ON	ON	ON	OFF	OFF
G2	S5	OFF	Soft-off	ON	ON	ON	OFF	OFF
G2/G3	S5 LOW	OFF	Battery IN	ON	ON	OFF	OFF	OFF
G3		OFF	Mechanical off	ON	OFF	OFF	OFF	OFF

SMBus Block Diagram

Group Name Description

INT: Stuff when use internal clock generator
EXT: Stuff when use external clock generator
DNI/NC: DO NOT INSTALL
KBC: Stuff when use external KBC
IMC: Stuff when use internal EC
A11:Resistors marked with "A11" is only for SB800A11 ONLY.

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Bitland Information Technology Co.,Ltd.
Notebook R&D Division

Title MISCELLANEOUS TABLES

Size Custom Document Number BM5016 Rev 1.0

Date Thursday, August 05, 2010 Sheet 6 of 54

http://pc-120.taobao.com/

[illegible][illegible]

Thermal Systems
(Emergency Shutdown, Throttling, Fan Control)

Thermal disaster prevention is implemented by PROCHOT_L and THERMTRIP_L with hardware non-system dependant functions. Fan speed control will only be implemented by SB TSI software based implementation

SMBus Block Diagram

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G1	S3	OFF	Suspend to RAM	ON	ON	ON	ON	OFF
G2	S4	OFF	Suspend to disk ON	ON	ON	ON	OFF	OFF
G2	S5	OFF	Soft-off	ON	ON	ON	OFF	OFF
G2/G3	S5 LOW	OFF	Battery IN	ON	ON	OFF	OFF	OFF
G3	OFF	OFF	Mechanical off	ON	OFF	OFF	OFF	OFF

Group Name Description

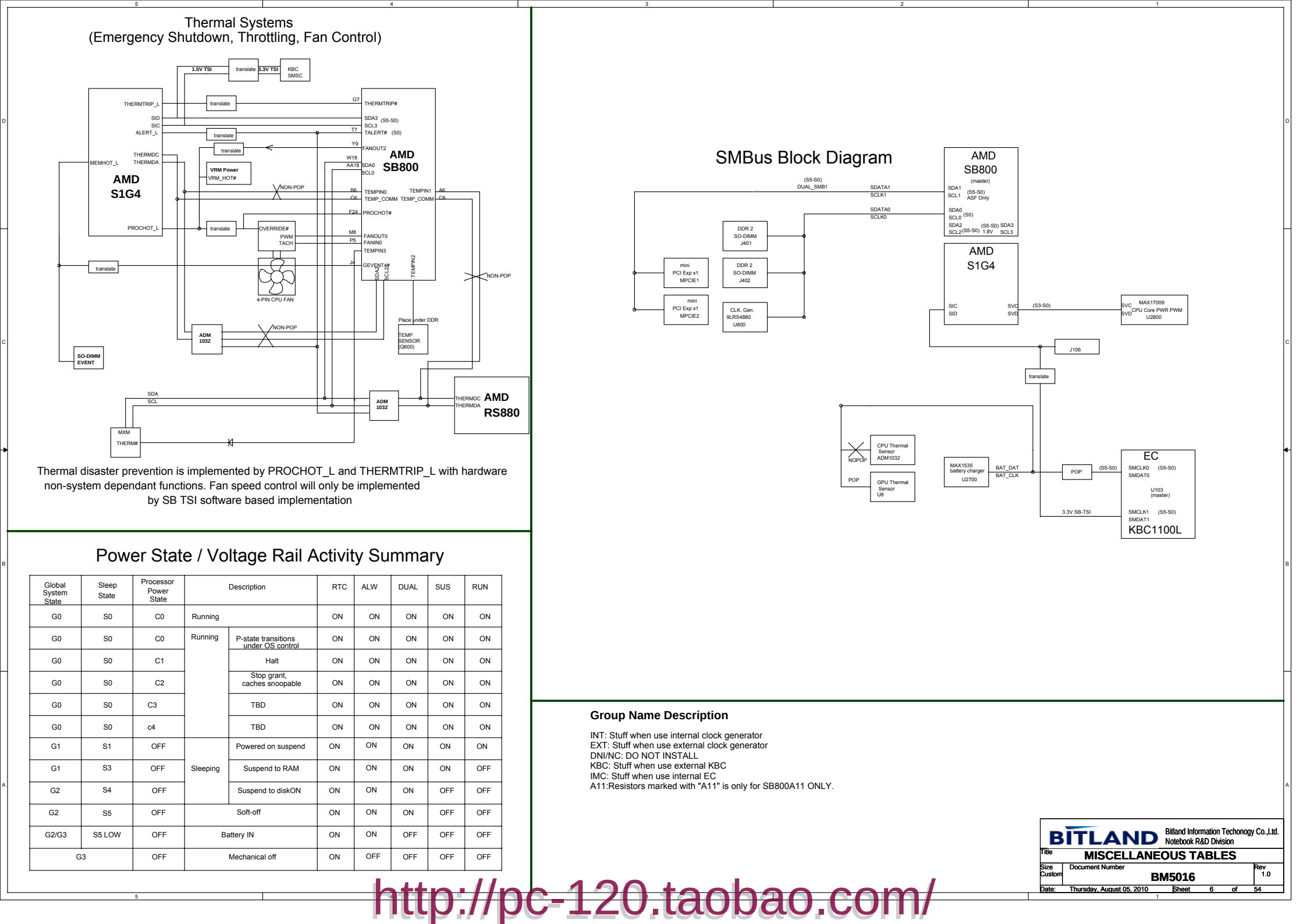
INT: Stuff when use internal clock generator
EXT: Stuff when use external clock generator
DNI/NC: DO NOT INSTALL
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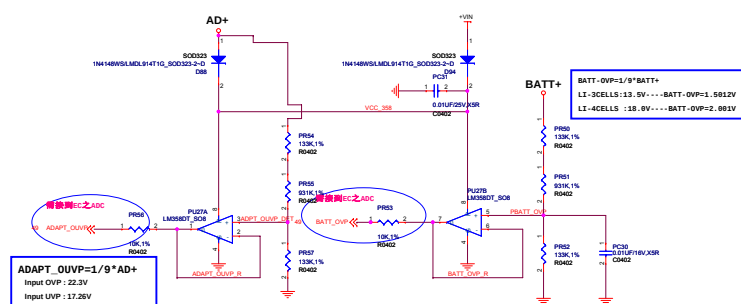
BITLAND Bitland Information Technology Co., Ltd.
Notebook R&D Division

Title: MISCELLANEOUS TABLES

Size Custom Document Number: BM5016 Rev 1.0

Date: Thursday, August 05, 2010 Sheet 6 of 54

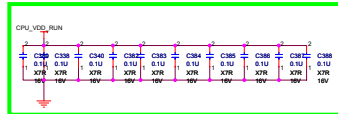




 Bitland Information Technology Co., Ltd. Notebook R&D Division	
Title ADP IN/BATTERY CHARGER	
Size D	Document Number BM5016
Date Thursday, April 05, 2012	Rev 1.0

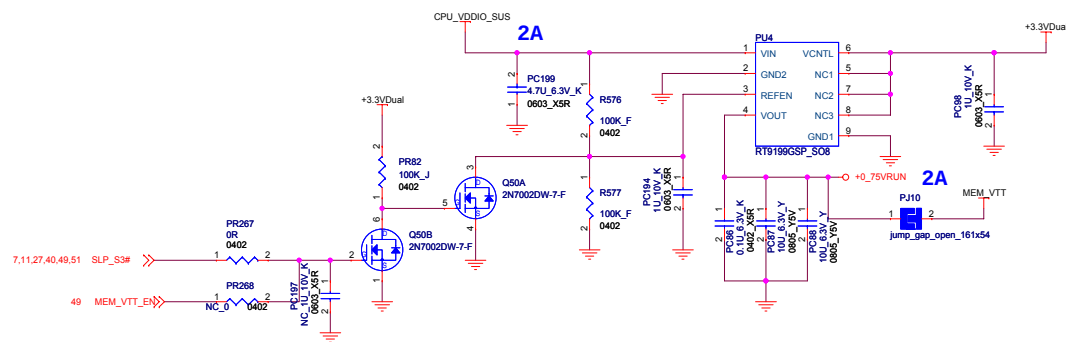
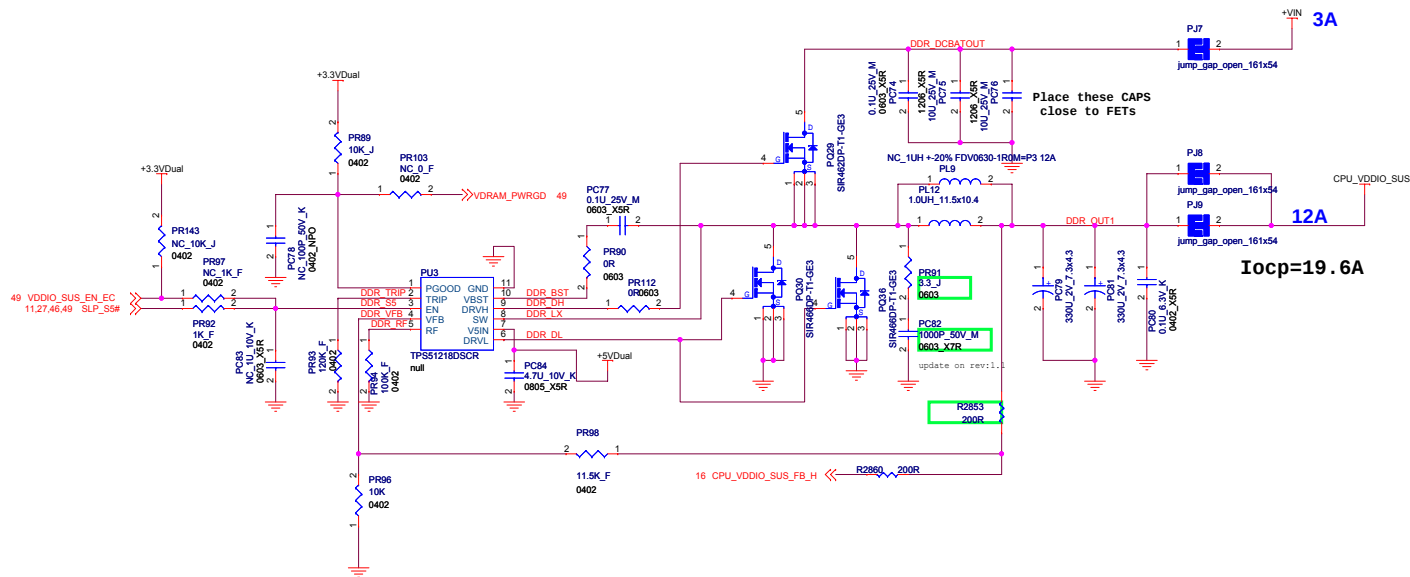
<http://pc-120.taobao.com/>

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8



0.7 - 1.3 V 36A

Fou Uni-plane:
G16,G17,R39:Assembly
R38:Not Assembly



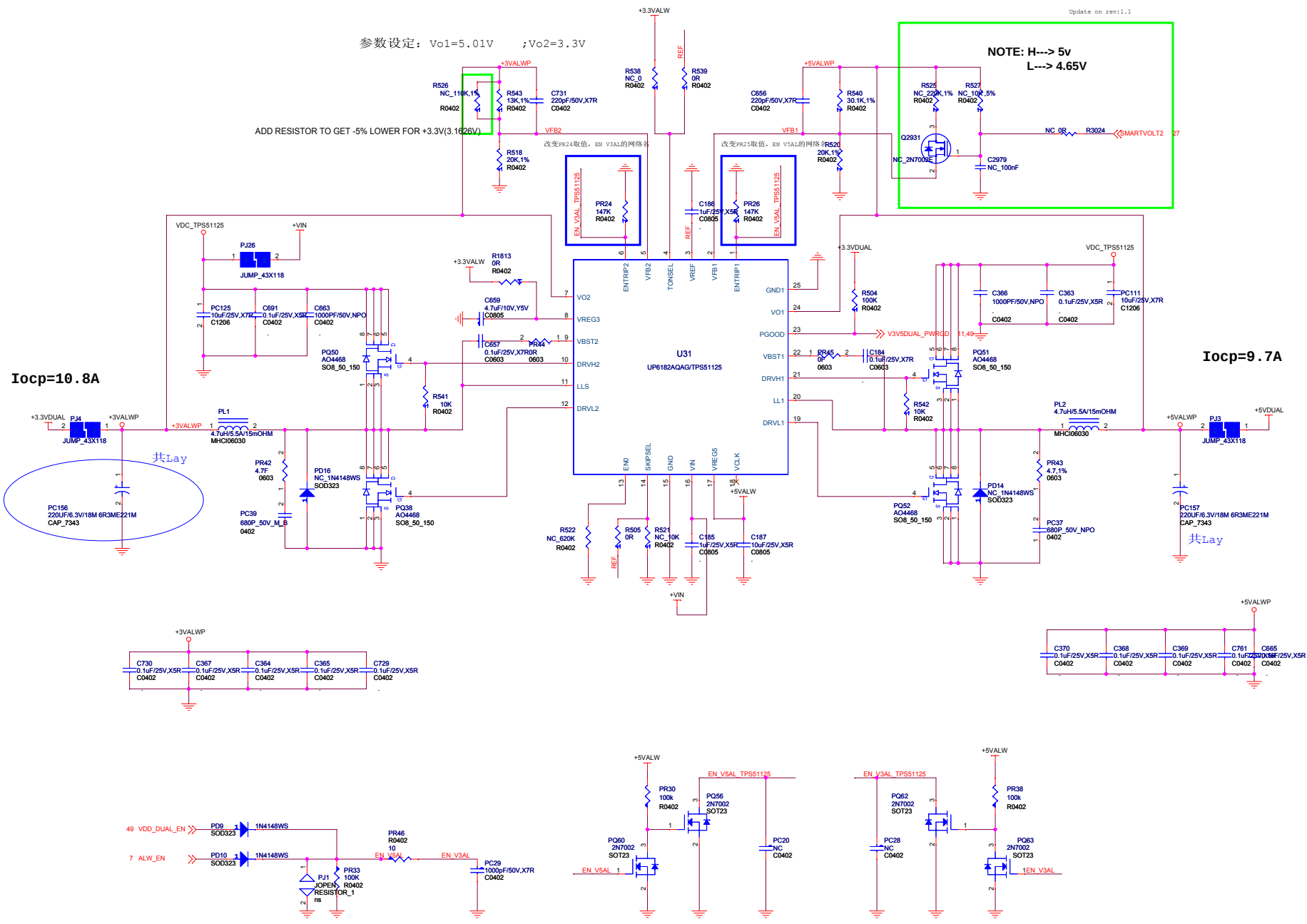
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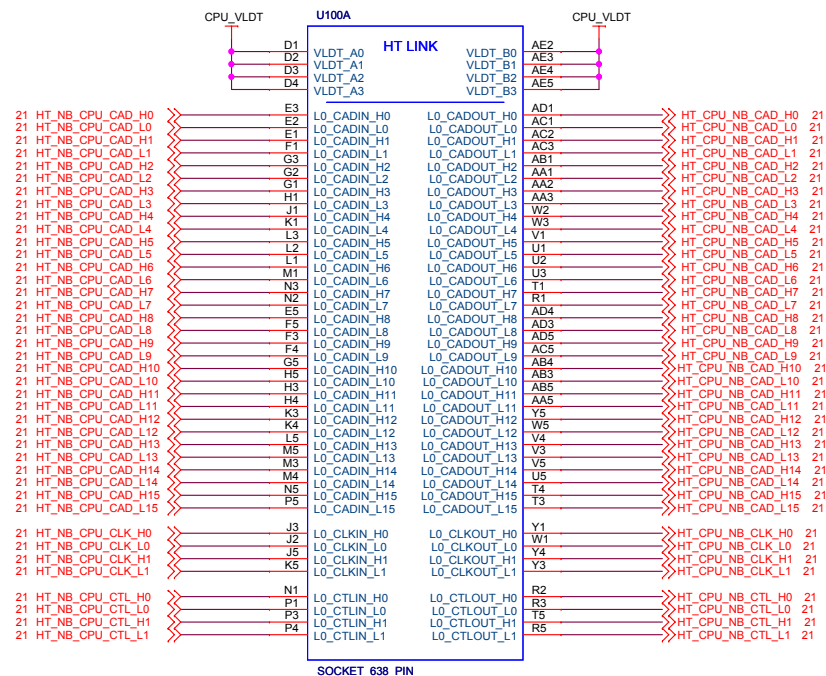
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BITLAND		Bitland Information Technology Co., Ltd. Notebook R&D Division	
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Size C	Document Number BM5016		Rev 1.0
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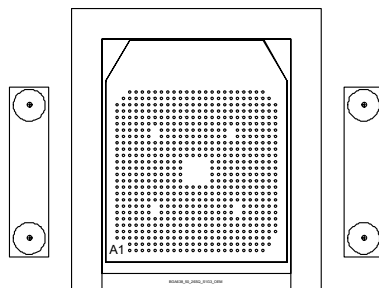
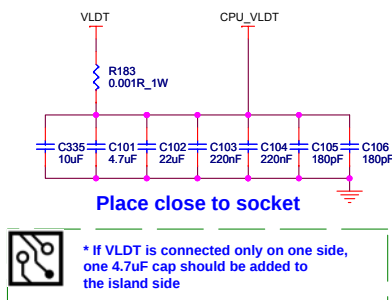


<http://pc-120.taobao.com/>

CPU_VLDT 1.1V 1.5A

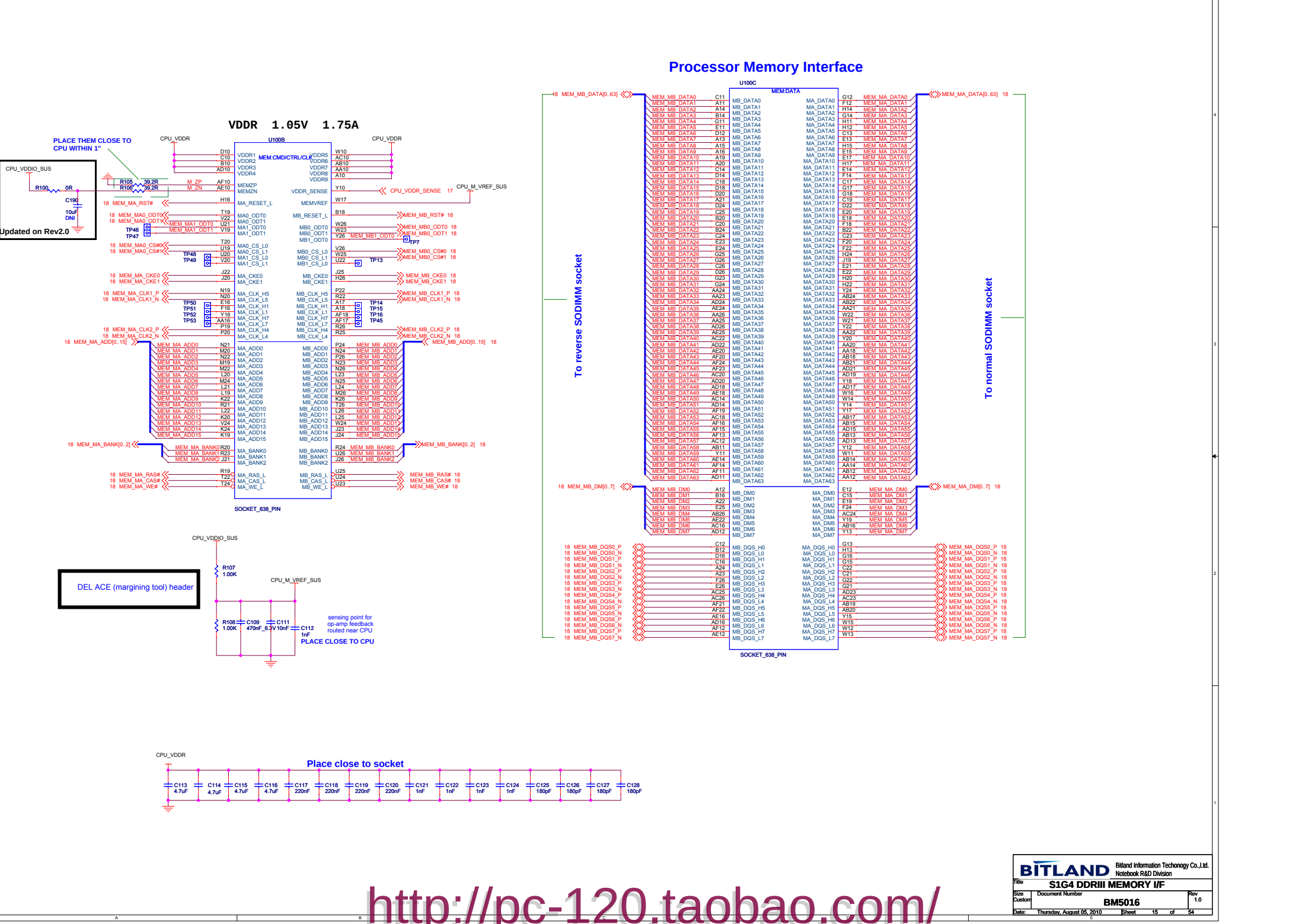


DEL HTPA Soft-Touch Duo Connectors



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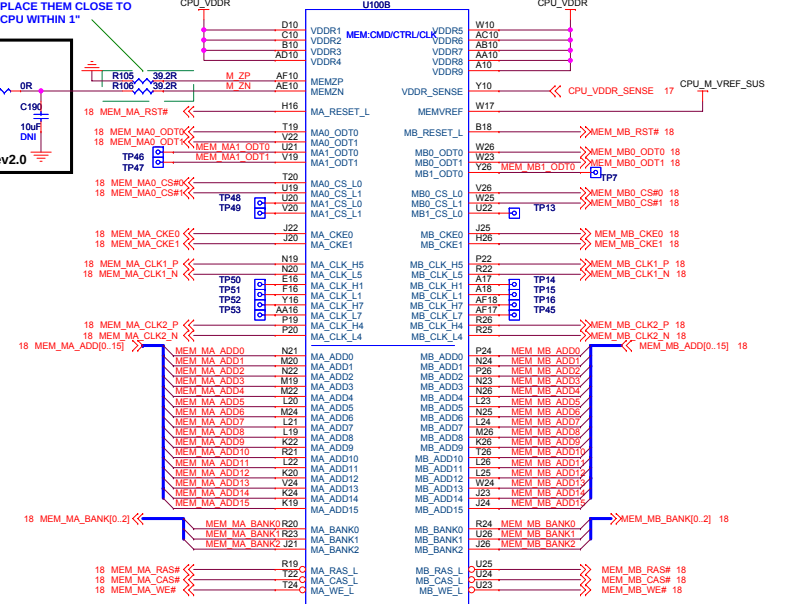
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		Notebook R&D Division	
Title	S1G4 HT I/F		
Size	Document Number	BM5016	
Custom			Rev 1.0
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Processor Memory Interface

VDD 1.05V 1.75A

Updated on Rev2.0



To reverse SODIMM socket

To normal SODIMM socket

18 MEM_MB_DM0[0..7]

18 MEM_MA_DM0[0..7]

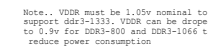
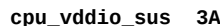
SOCKET_638_PIN

SOCKET_638_PIN

CPU_VDDQ

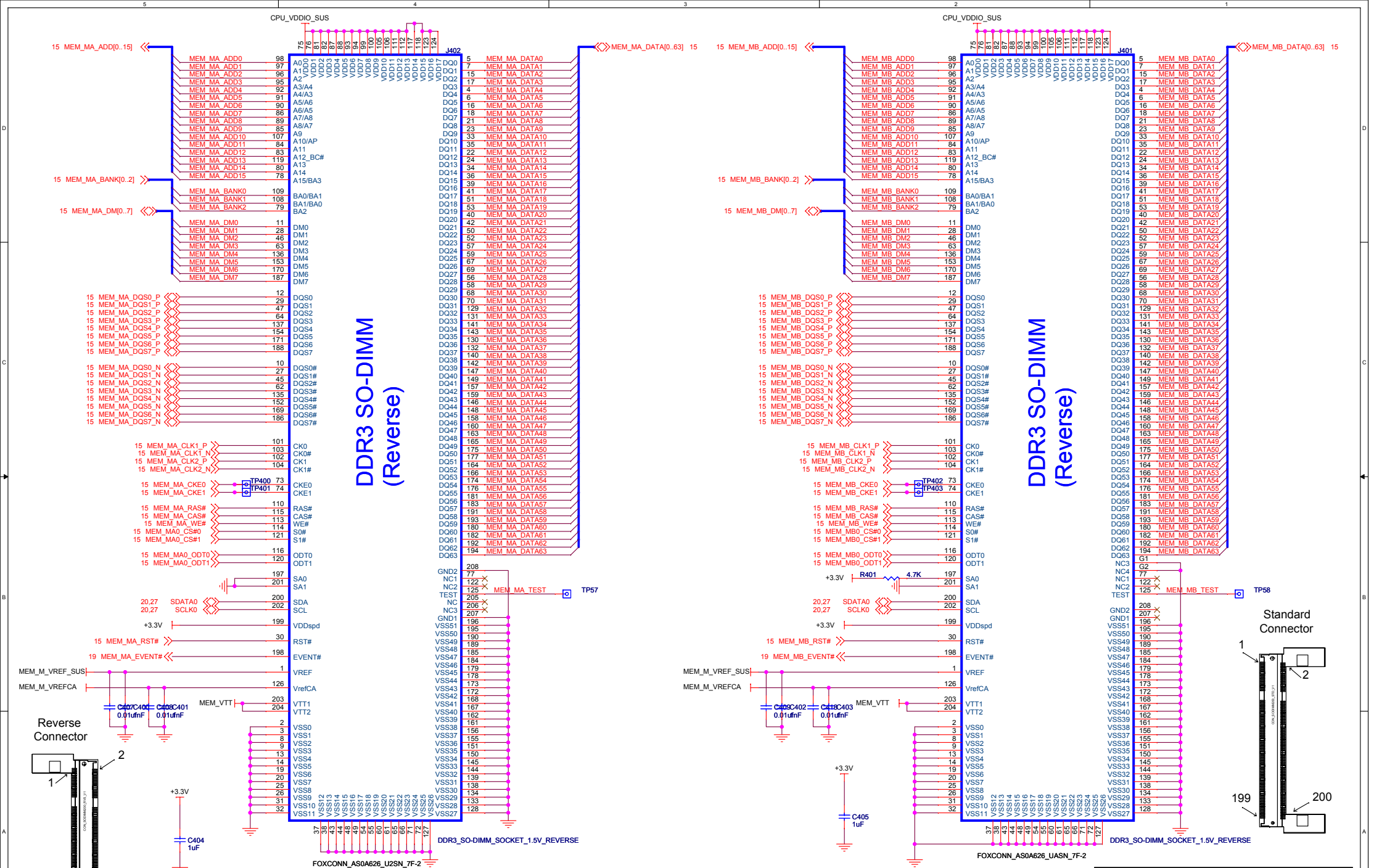
Place close to socket



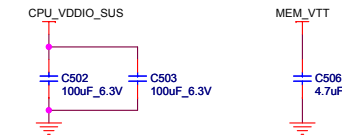
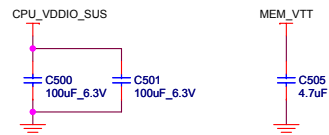
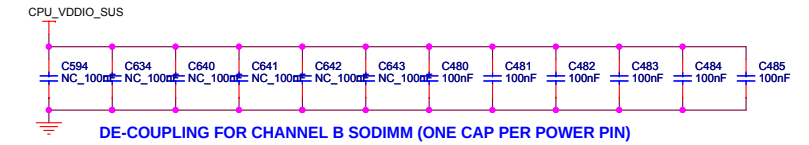
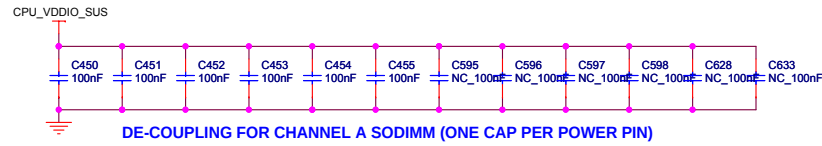
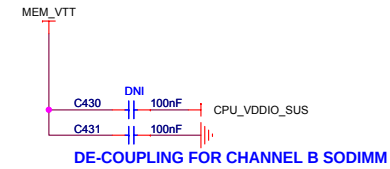
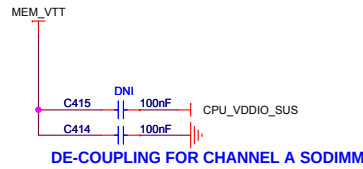


VDDR_1.2_EN:
1 : VDDR = 1.05V 1.75A
0: VDDR = 0.9V 1.25 A (Default)

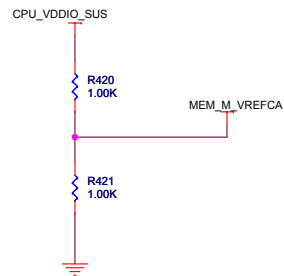
Update on rev:1.



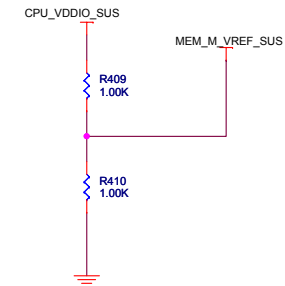
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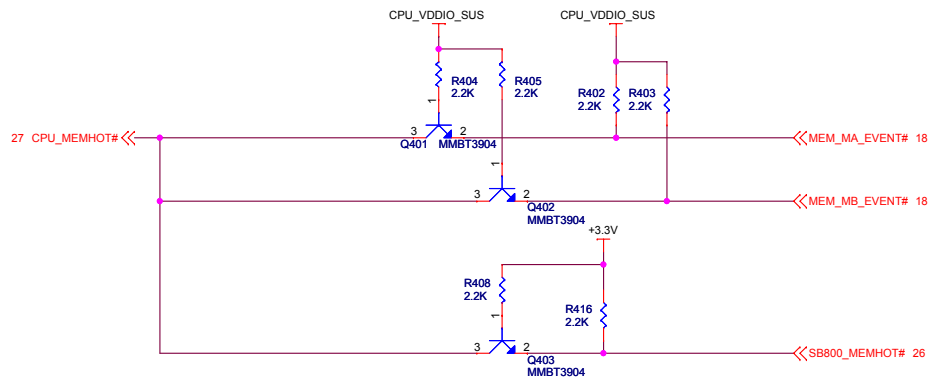
LAYOUT: PLACE CLOSE TO DIMMS

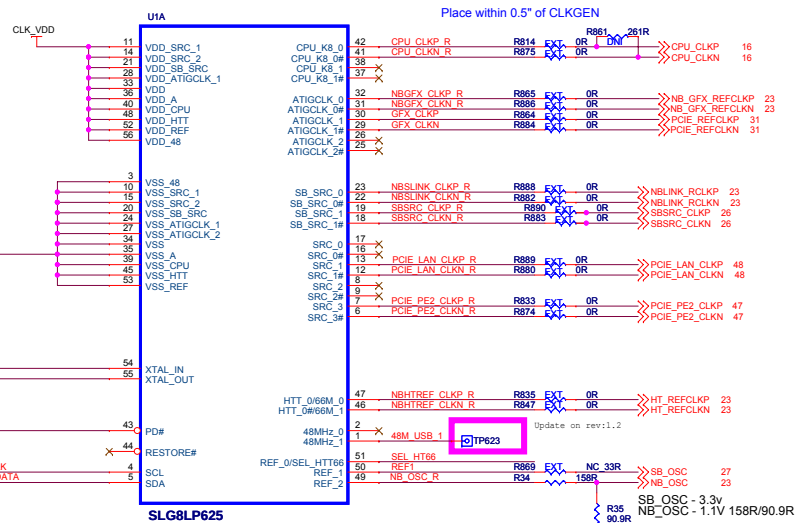
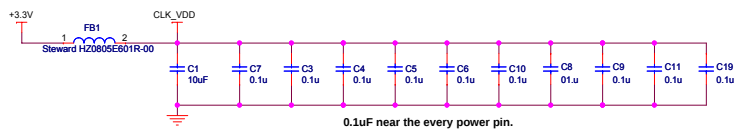


MEM_VREF_SUS



LAYOUT: PLACE CLOSE TO DIMMS





Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	6M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

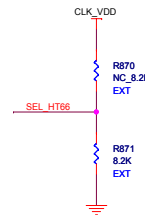
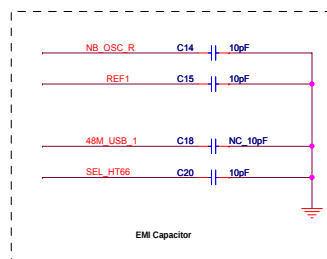
* RS780 can be used as clock buffer to output two PCIe reference clocks. By default, chip will configured as input mode, BIOS can program it to output mode.

R34/R35 (value may change)

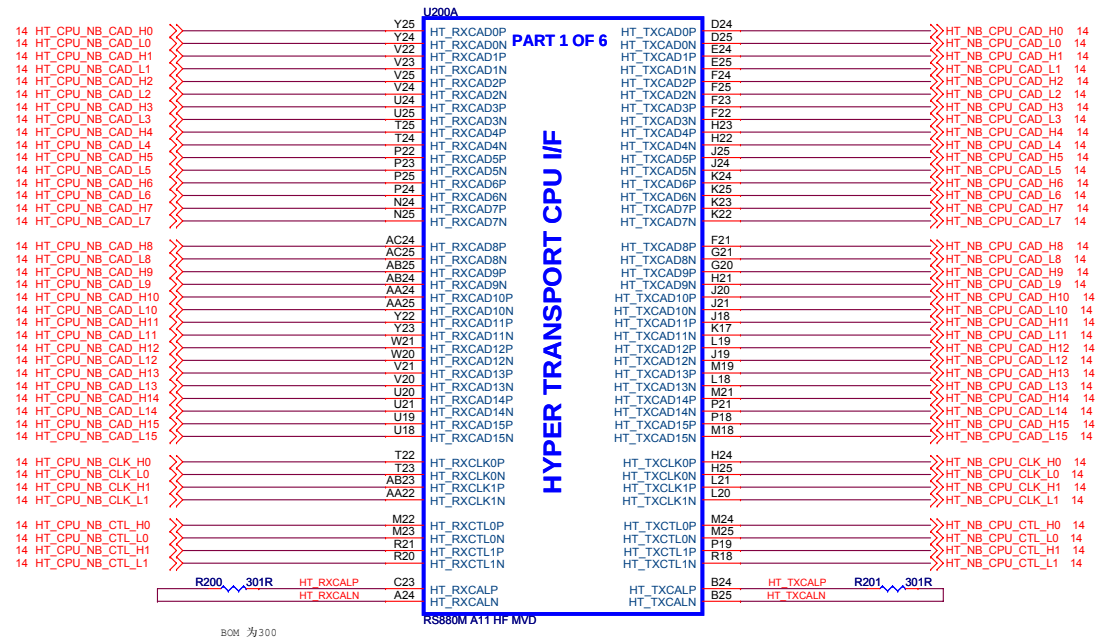
	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 33R/43R
RS780	1.1V 200R/100R

SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1*	100 MHz non-spreading differential SRC clock
	0	100 MHz spreading differential SRC clock

* default



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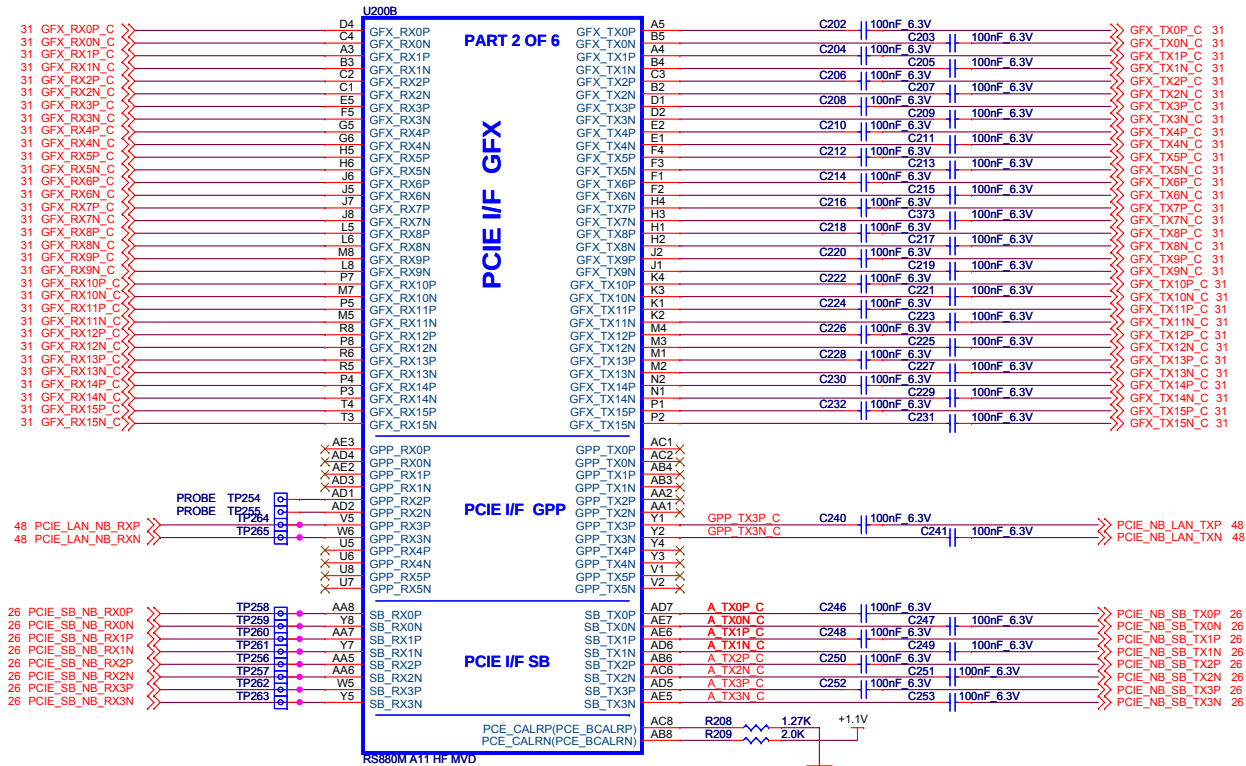
DEL HTPA PROBE CONNECTOR FOR DEBUG(NB SIDE)



MXM3.0 need put the CAP on the motherboard.
Close to the MXM Slot



MXM3.0 need put the CAP on the motherboard.
Close to the MXM Slot



Keep the impedance of PCIE lane to 85ohm +/-15%
Including the A-link



All PCie lane shou route 8" max for Gen2 connector and max 12" for Gen2 on board devices
Guam has the Lasso lane over 8" due to the large board, should use shorter lasso calbe for Guam.
Customer need to follow the MBDG.

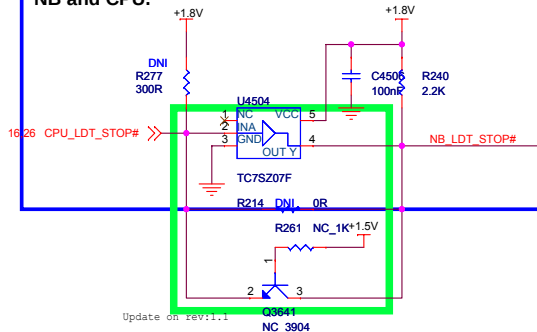
DEL PCIE MIDDLE BUS PROBE FOR DEBUG

RS880M Display Port Support (muxed on GFX)

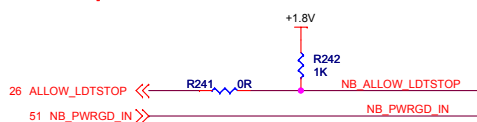
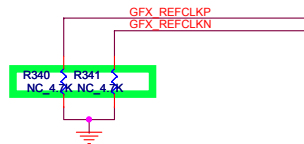
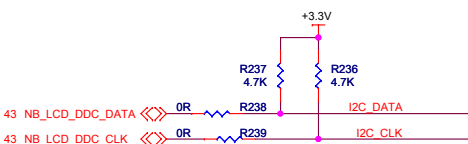
DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

24,26,31,49 A_RST# >>> R210 0R NB_RST# IN

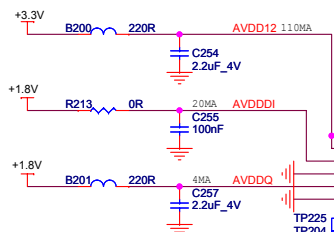
Note:Regarding LDT_STOP# signal,It's required within 40ns skew for both assertion and de-assertion between NB and CPU.



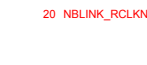
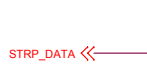
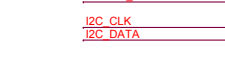
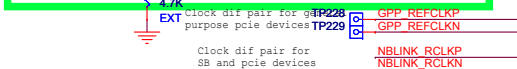
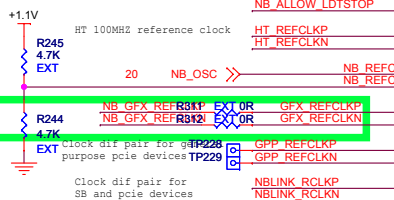
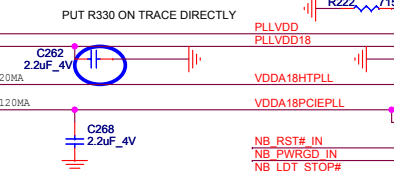
Change B204 to Resistor 3.9R(315003R900G)



DEL
RS880M UVD DEBUG HEAD
RS880M JTAG
8BIT DEBUG HEADER



Termination resistors < 1 inch trace



PLACE R291, R292 CLOSE TO NB(R291, R292 IS FOR A11 SB800 ONLY)

PART 3 OF 6

CRT/TVOUT

PLL PWR

LVTM

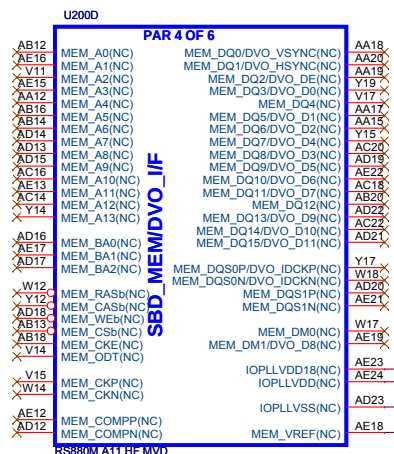
PM

CLOCKS

MIS.

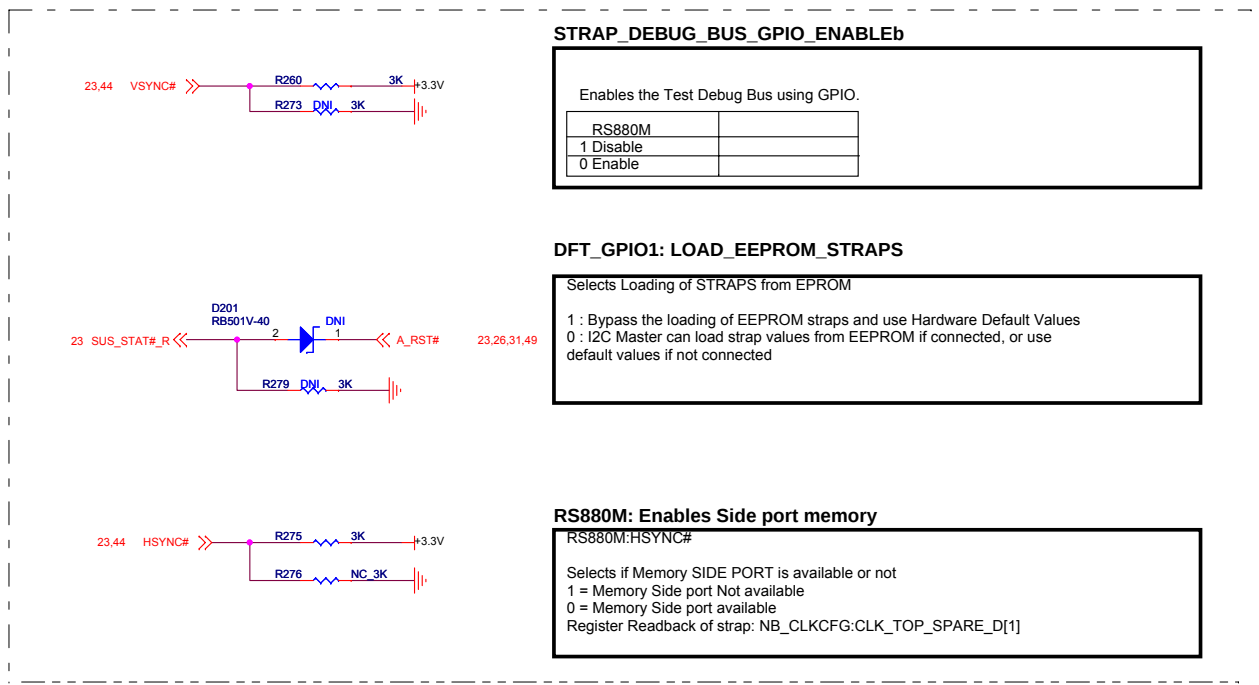


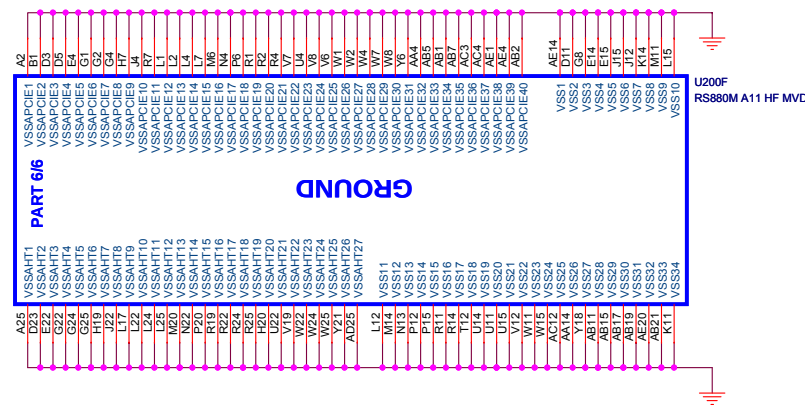
DEL THERMAL SENSOR



DEL U202

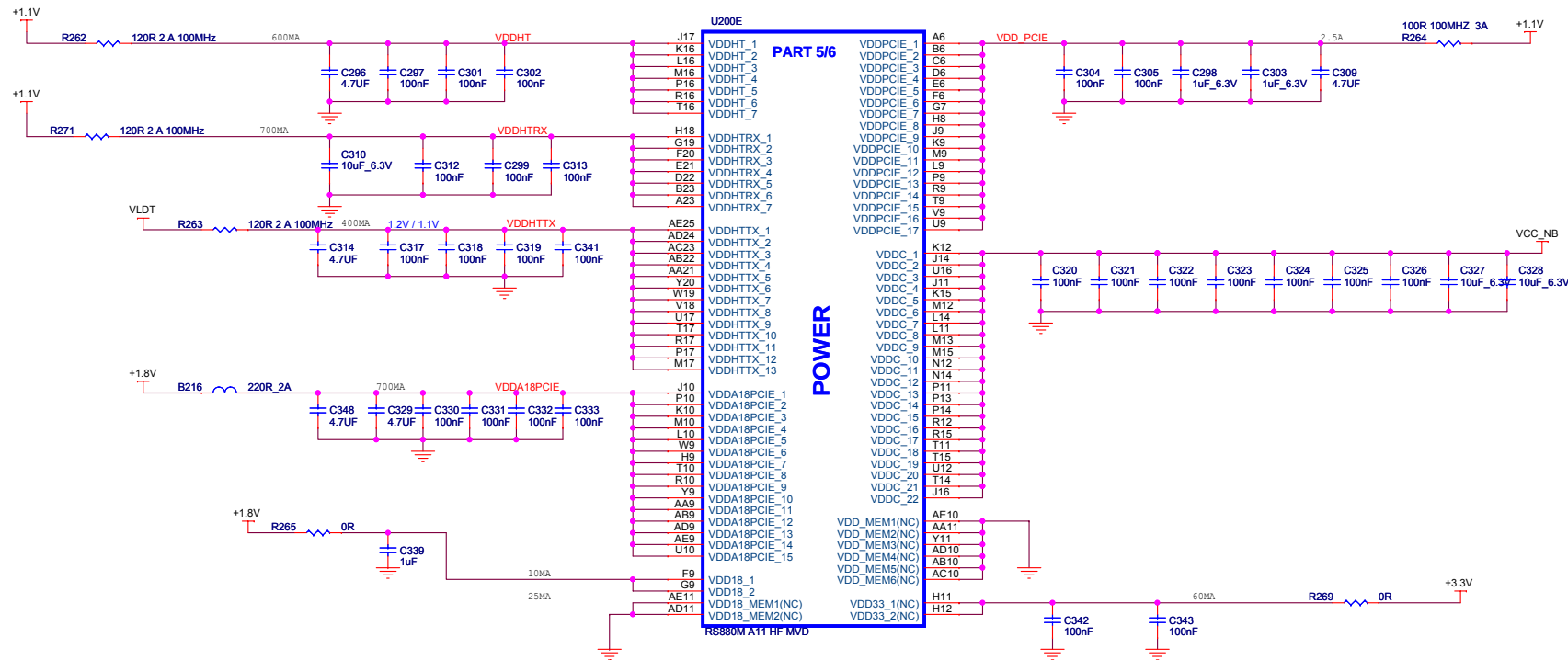
DEL SDRAM DDR3





RS880M POWER TABLE

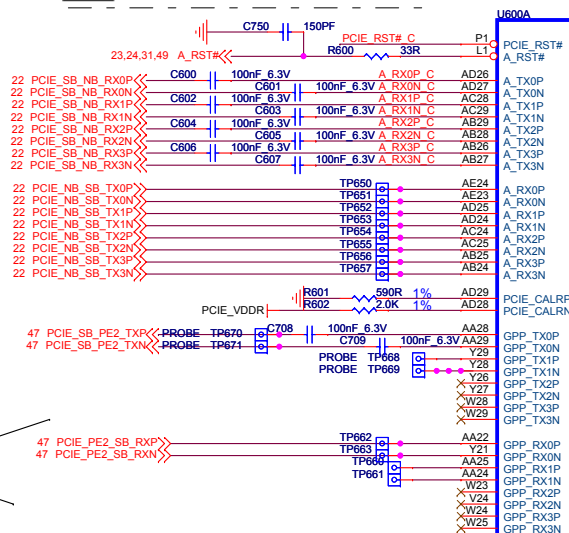
PIN NAME	RS880M	PIN NAME	RS880M
VDDHT	+1.1V	IOPLLVD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVD	+1.1V
VDD18_MEM	+1.8V	PLLVD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDLT18	+1.8V
IOPLLVD18	+1.8V	VDDLT33	NC



DEL FAN CIRCUIT



PLACE THESE PCIE AC
COUPLING CAPS CLOSE TO U600



J613 CLOSE TO U600

NOTE: SB8XX ONLY SUPPORTS 2 GPP
PORT 2 AND 3 IS NOT SUPPORTED.



NOTE: The 0R serial resistor on SB CLK pair
must share Pin Pad with the serial resistor close to U800

FOR EXT GRAPHICS

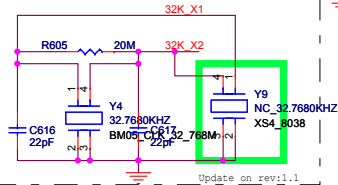
FOR WIFI

FOR LAN

Updated on Rev2.0



PLACE THESE COMPONENTS CLOSE TO U600, AND
USE GROUND GUARD FOR 32K_X1 AND 32K_X2



PCIE EXPRESS INTERFACES

PCI INTERFACE

CLOCK GENERATOR

LPC

CPU

RTC

SB800 Part 1 of 5

PCICLK0

PCICLK1/GPIO38

PCICLK2/GPIO37

PCICLK3/GPIO38

PCICLK4/14M_OSC/GPIO39

PCIRST#

AD0/GPIO0

AD1/GPIO1

AD2/GPIO2

AD3/GPIO3

AD4/GPIO4

AD5/GPIO5

AD6/GPIO6

AD7/GPIO7

AD8/GPIO8

AD9/GPIO9

AD10/GPIO10

AD11/GPIO11

AD12/GPIO12

AD13/GPIO13

AD14/GPIO14

AD15/GPIO15

AD16/GPIO16

AD17/GPIO17

AD18/GPIO18

AD19/GPIO19

AD20/GPIO20

AD21/GPIO21

AD22/GPIO22

AD23/GPIO23

AD24/GPIO24

AD25/GPIO25

AD26/GPIO26

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AD30/GPIO30

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AD42/GPIO42

AD43/GPIO43

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AD65/GPIO65

AD66/GPIO66

AD67/GPIO67

AD68/GPIO68

AD69/GPIO69

AD70/GPIO70

AD71/GPIO71

AD72/GPIO72

AD73/GPIO73

AD74/GPIO74

AD75/GPIO75

AD76/GPIO76

AD77/GPIO77

AD78/GPIO78

AD79/GPIO79

AD80/GPIO80

AD81/GPIO81

AD82/GPIO82

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AD246/GPIO246

AD247/GPIO247

AD248/GPIO248

AD249/GPIO249

AD250/GPIO250

AD251/GPIO251

AD252/GPIO252

AD253/GPIO253

AD254/GPIO254

AD255/GPIO255

AD256/GPIO256

AD257/GPIO257

AD258/GPIO258

DEL WIRELESS RADIO SWIT



TEST2	TEST1	TEST0	TEST MODE	DESCRIPTION
0	0	0	None	Normal operation
0	0	1	Reserved	Reserved for ASIC de
0	1	X	Test mode	Enable Test Mode
1	X	X	Reserved	Reserved for ASIC de

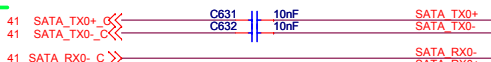
| SB800 SB TEST0.SB TEST1.SB TEST2 has internal 10K PD

<http://pc-120.taobao.com/>

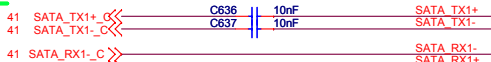


SATA trace should use only 1via on the trace. customers can use 2vias with GND via within 150mils of signal via as long as they can ensure that their platform meets SATA logo requirements. Return loss is expected to get affected with 2 vias. AMD platforms are validated with one via only

FOR SATA HD



FOR SATA ODD



SATA PORTS DISTRIBUTION:

- 0, - 2.5 INCH DISK DRIVER
- 1, SATA, ODD
- 2, NOT USED
- 3, NOT USED
- 4 & 5, NOT USED

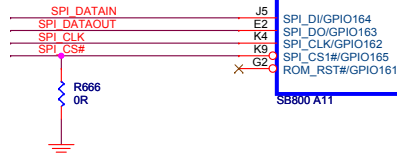
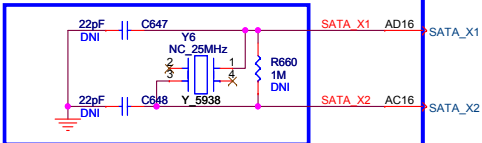


PLACE SATA_CAL RES VERY CLOSE TO BALL OF U600



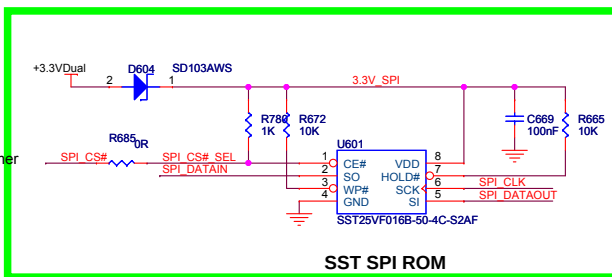
51 SATA_ACT# to AD11, SATA_ACT#/GPIO67

To meet SB800 SCL1.02: DNI SATA XTAL circuit's parts



R685: Normal

R666: EXT Programmer



change to SPI mode

SB800 Part 2 of 5

FLASH

SERIAL ATA

HW MONITOR

SPI ROM

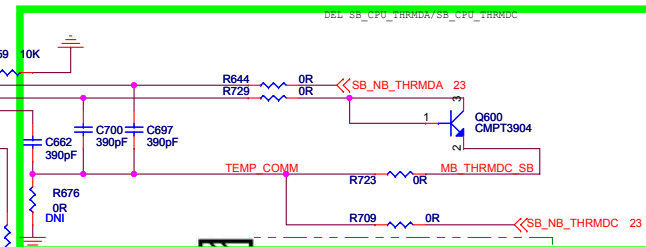
U600B

FC_CLK# AH28, FC_FBCLKOUT# AG28, FC_FBCLKIN# AF28, FC_OE#/GPIO145 AF28, FC_AVD#/GPIO146 AG28, FC_WE#/GPIO148 AF27, FC_CE1#/GPIO149 AE28, FC_CE2#/GPIO150 AF28, FC_INT1#/GPIO144 AF28, FC_INT2#/GPIO147 AH27, FC_ADQ0#/GPIO128 AJ27, FC_ADQ1#/GPIO129 AJ26, FC_ADQ2#/GPIO130 AH25, FC_ADQ3#/GPIO131 AG23, FC_ADQ4#/GPIO132 AH23, FC_ADQ5#/GPIO133 AJ22, FC_ADQ6#/GPIO134 AG23, FC_ADQ7#/GPIO135 AF21, FC_ADQ8#/GPIO136 AH22, FC_ADQ9#/GPIO137 AJ23, FC_ADQ10#/GPIO138 AF23, FC_ADQ11#/GPIO139 AJ24, FC_ADQ12#/GPIO140 AJ25, FC_ADQ13#/GPIO141 AG25, FC_ADQ14#/GPIO142 AH26, FC_ADQ15#/GPIO143 AH26

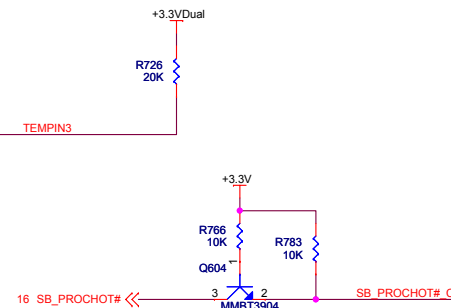
FANOUT0/GPIO52 W5, FANOUT1/GPIO53 W6, FANOUT2/GPIO54 Y9, FANIN0/GPIO56 W7, FANIN1/GPIO57 V9, FANIN2/GPIO58 W8, TEMPIN0/GPIO171 B6, TEMPIN1/GPIO172 A8, TEMPIN2/GPIO173 A5, TEMPIN3/TALERT#/GPIO174 B5, TEMP_COMM C7, VINO/GPIO175 B6, VIN1/GPIO176 A4, VIN2/GPIO177 A4, VIN3/GPIO178 C5, VIN4/GPIO179 A7, VIN5/GPIO180 B7, VIN6/GBE_STAT3/GPIO181 B8, VIN7/GBE_LED3/GPIO182 A8, NC1 G27, NC2 Y2

W5, W6, Y9, W7, V9, W8, B6, A8, A5, B5, C7, B6, A4, A4, C5, A7, B7, B8, A8, G27, Y2

Connect C7 and D8, then go to GND directly.



NOTE: ROUTE TEMP_COMM AS A 10MIL TRACE

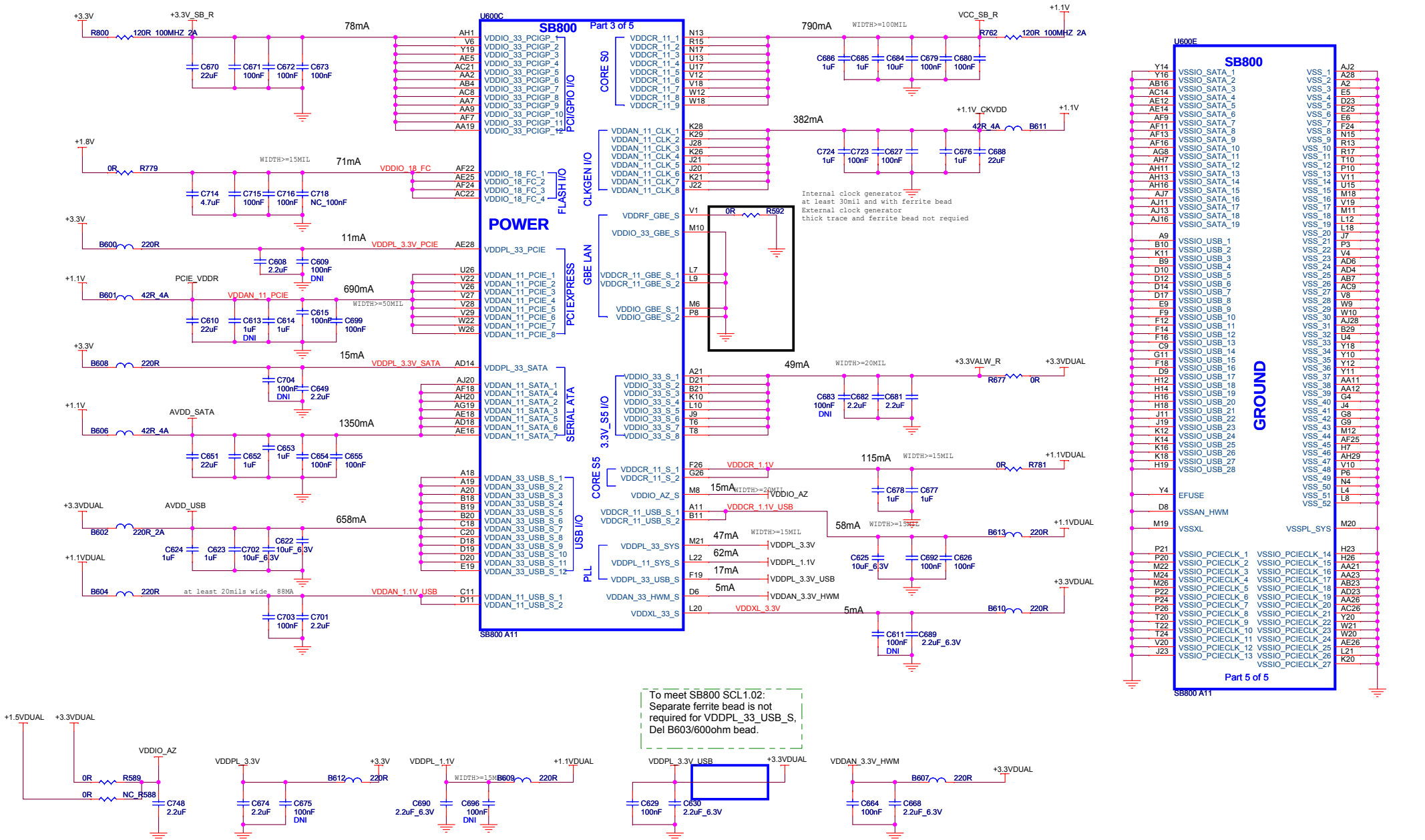


		Bitland Information Technology Co., Ltd. Notebook R&D Division	
Title SB8X0-SATA/IDE/HWM/SPI			
Size Custom	Document Number BM5016		Rev 1.0
Date:	Thursday, August 05, 2010	Sheet 28 of 54	

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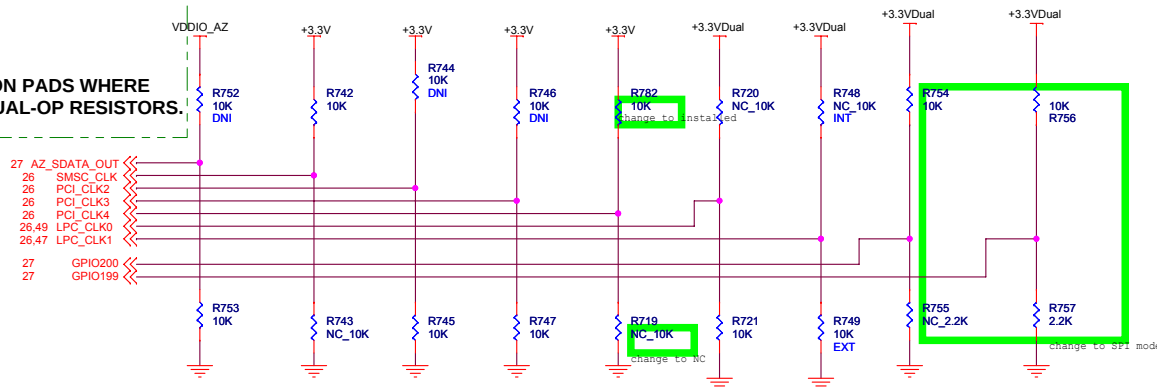
PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.



To meet SB800 SCL1.02:
Separate ferrite bead is not
required for VDDPL_33_USB_S,
Del B603/600ohm bead.



OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



DEL JTAG HEADER

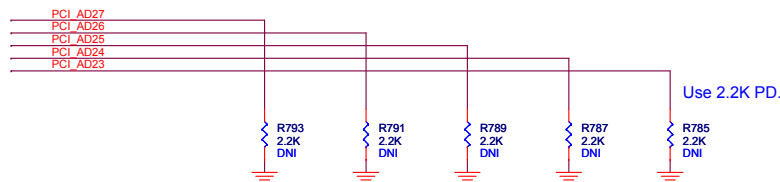
REQUIRED STRAPS

	AZ_SDOUT	SSMSC_CLK	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM (Default) L,L = FWH ROM	

DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

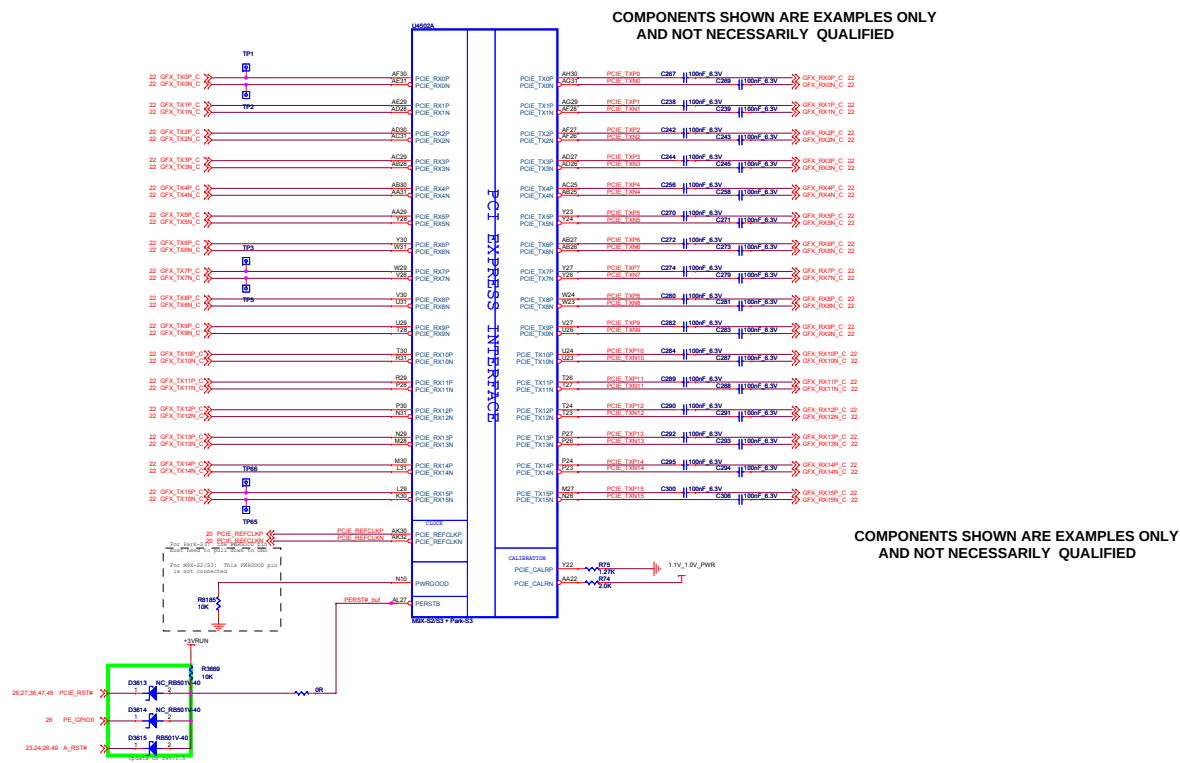
26 PCI_AD[27..23] <<>

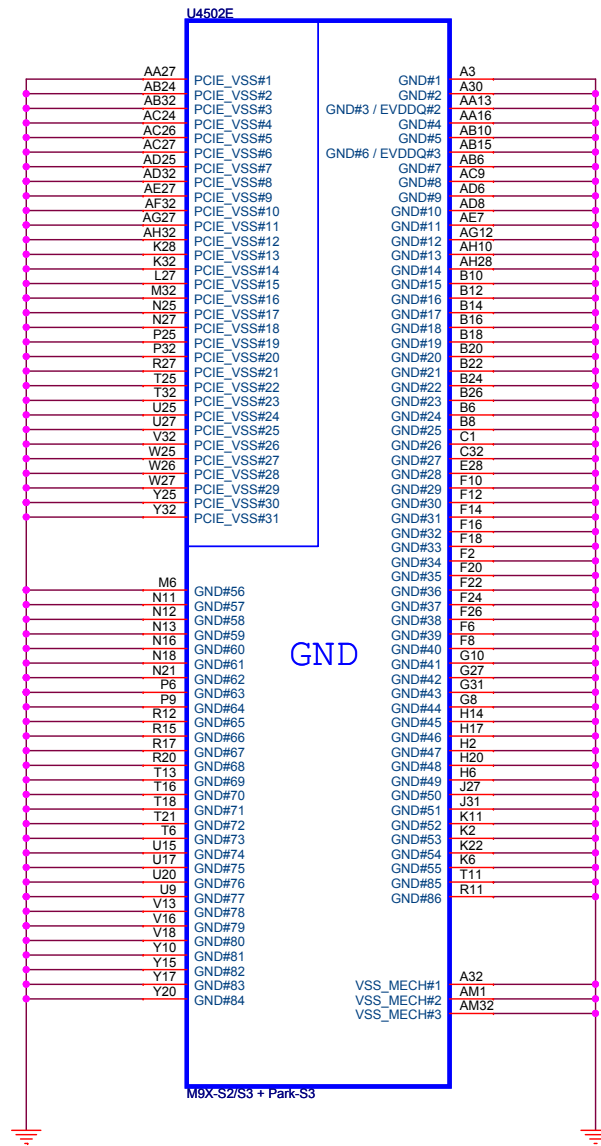


	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

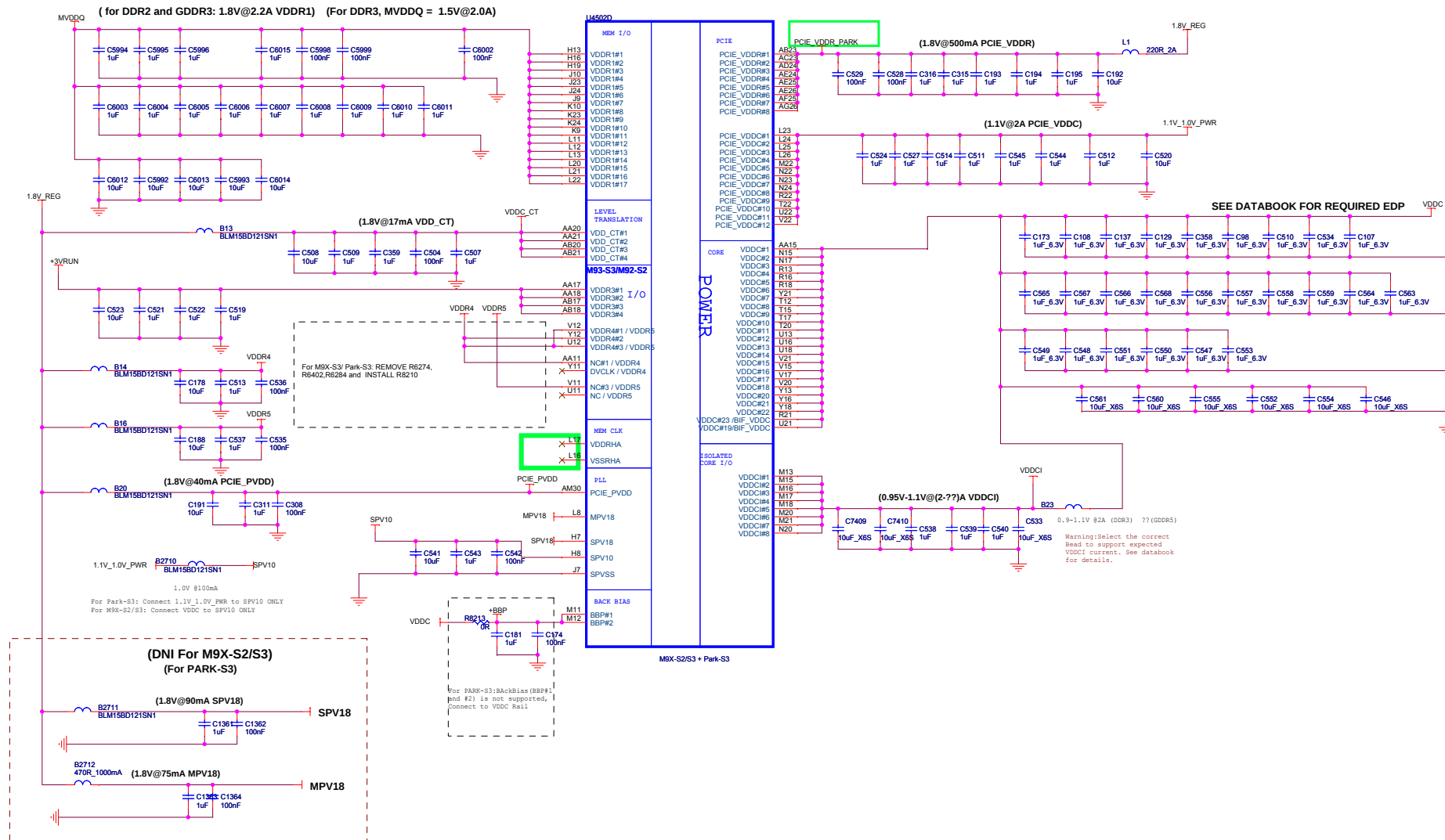
BITLAND Bitland Information Technology Co., Ltd. Notebook R&D Division	
Title SB8X0-STRAPS	
Size Custom	Document Number BM5016
Date: Thursday, August 05, 2010	Sheet 30 of 54

<http://pc-120.taobao.com/>

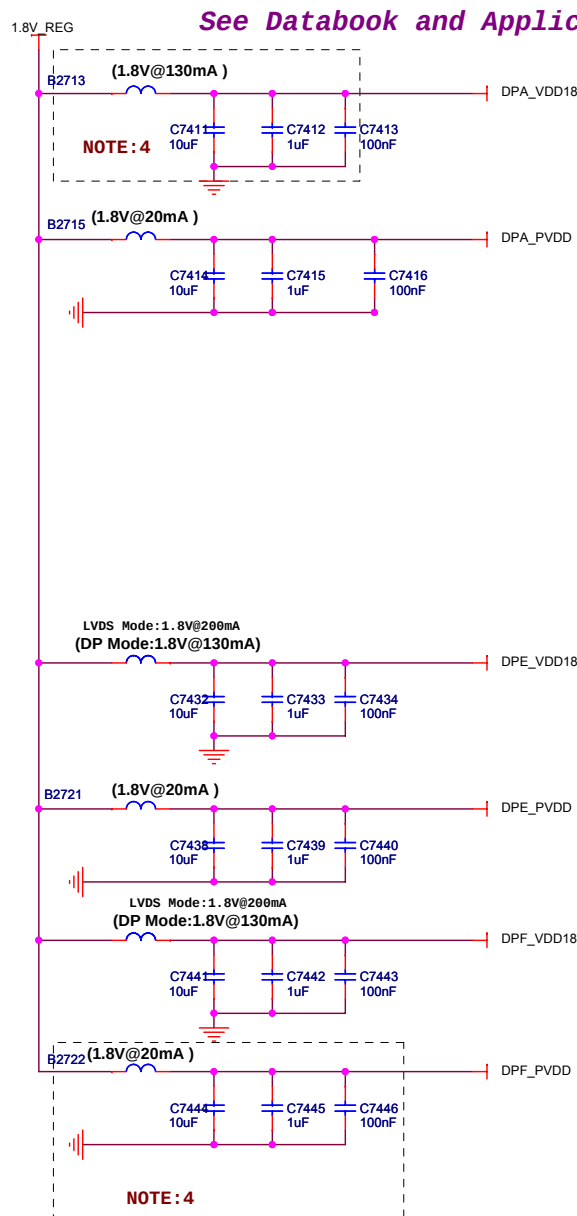




		Bitland Information Technology Co., Ltd. Notebook R&D Division	
Title PARK-XT(Core_GND)			
Size B	Document Number BM5016		Rev 1.0
Date:	Thursday, August 05, 2010	Sheet 33 of 54	



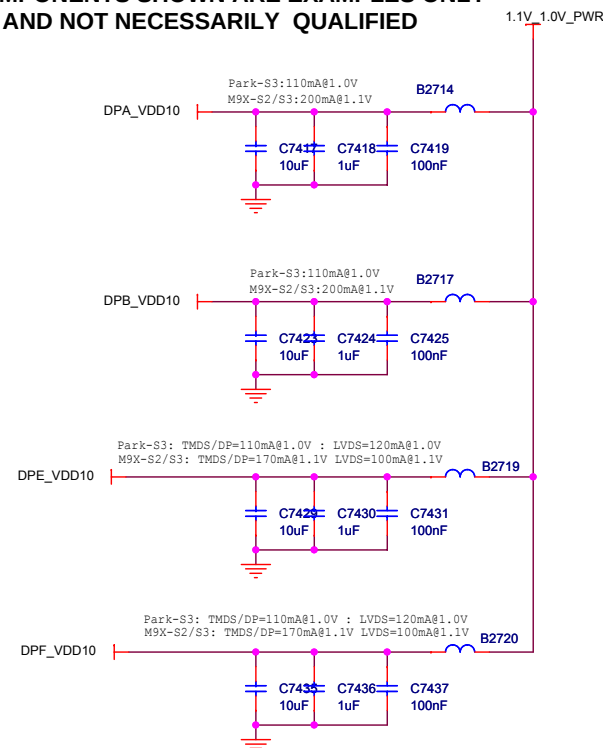
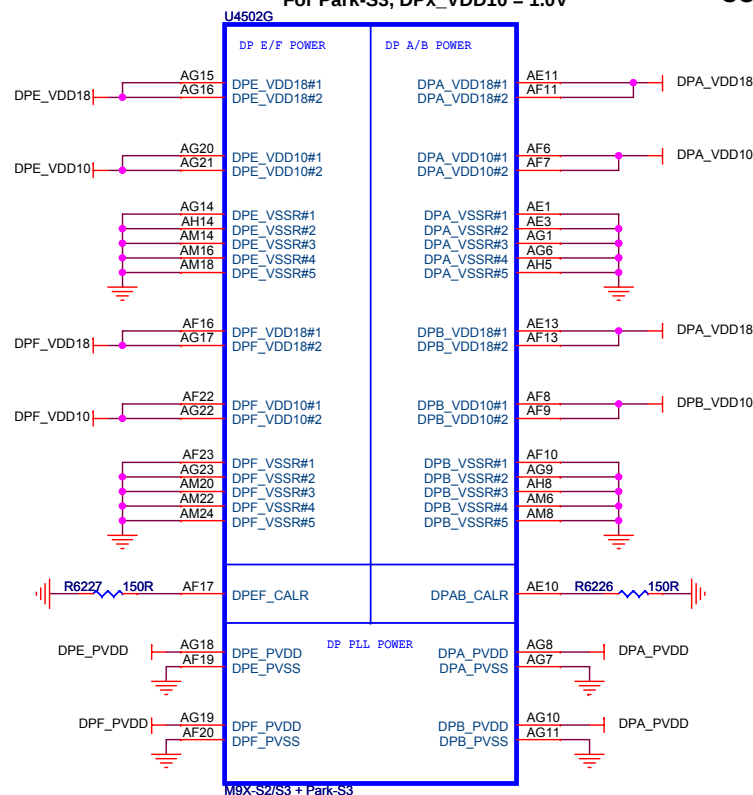
<http://pc-120.taobao.com/>



See Databook and Application note table for Voltage and Current requirements for each individual rail.

For M9X-S2/S3, DPx_VDD10 = 1.1V
For Park-S3, DPx_VDD10 = 1.0V

COMPONENTS SHOWN ARE EXAMPLES ONLY
AND NOT NECESSARILY QUALIFIED



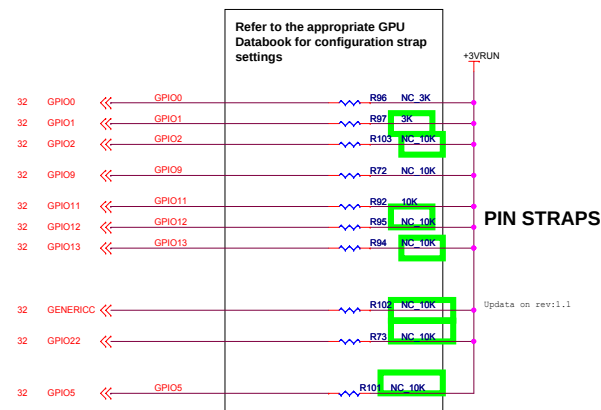
NOTE:1: DPx_VDD18 and DPx_PVDD Rails can be join together and remove Decoupling Capacitors and BEAD for DPx_PVDD if signal integrity for DP lanes are OK.

NOTE:2: DPA_VDD10 / DPB_VDD10 and DPE_VDD10 / DPF_VDD10 Rails can be join together and remove Decoupling Capacitors and BEAD for one rail of each pair if signal integrity for DP lanes are OK. We also need to Change BEAD to minimum 400mA rating.

NOTE:3: DPx_VDD18 Rails can be join together as shown in schematic for Dual -Link DVI or LVDS setting and remove Decoupling Capacitors and BEAD of any one rail of the pair if signal integrity for DP lanes are OK. We need atleast 500mA Bead to support join rails.

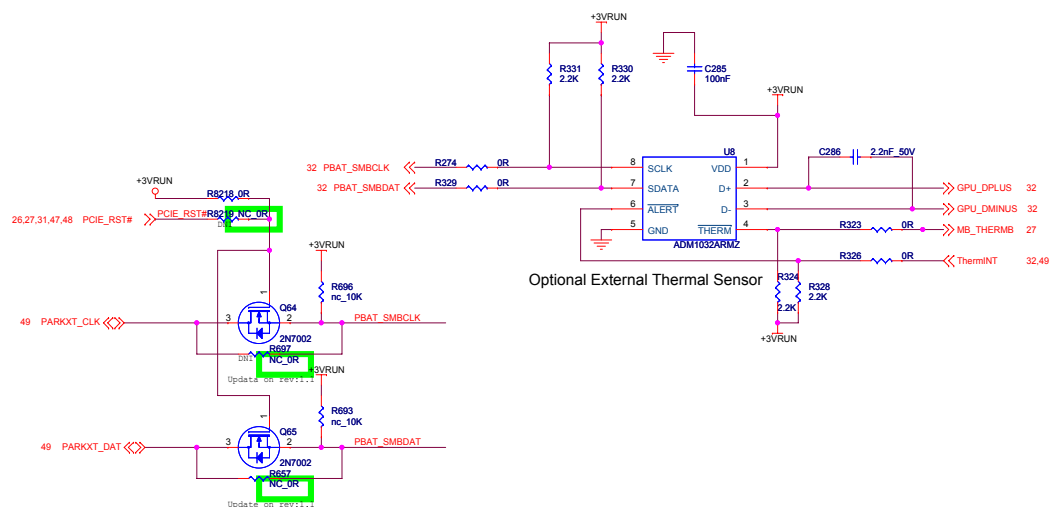
NOTE:4: Do not Install for M9X-S2/S3. INSTALL ONLY for PARK-S3. Other Notes can be apply as well.

		Bitland Information Technology Co., Ltd.	
		Notebook R&D Division	
Title Park-XT(DP Power)			
Size B	Document Number BM5016		Rev 1.0
Date:	Thursday, August 05, 2010	Sheet 35 of 54	



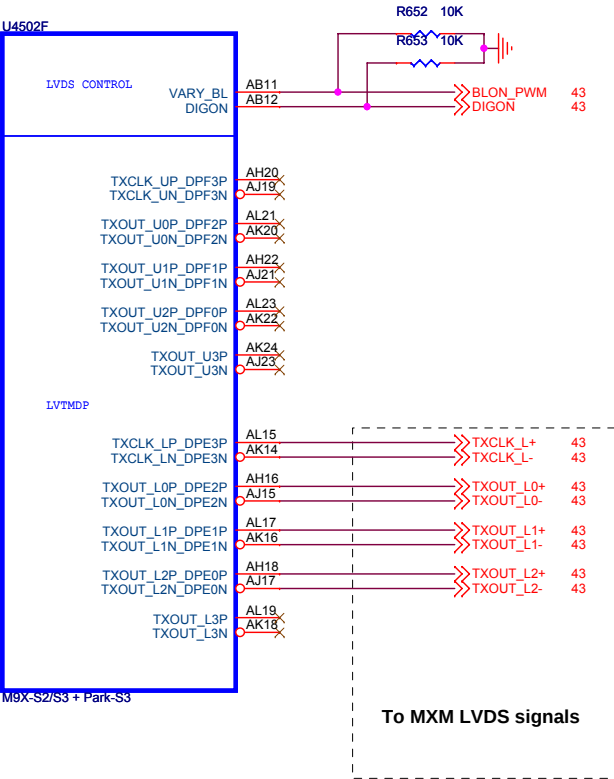
CONFIGURATION STRAPS			RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1= INSTALL 10K RESISTOR X= DESIGN DEPENDANT NA= NOT APPLICABLE
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET			
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
BIF_GEN2_EN_A	GPIO2	PCIE GEN2 ENABLED	X
RSVD	GPIO8	VGA ENABLED	0
BIF_VGA_DIS	GPIO9		0
RSVD	GPIO21		0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	X
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	X X X
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	X
RSVD	GENERICC	AUD[1] AUD[0]	0
AUD[1]	HSYNC	0 0 No audio function	0
AUD[0]	VSNC	0 1 Audio for DisplayPort and HDMI if dongle is detected	X X
		1 0 Audio for DisplayPort only	
		1 1 Audio for both DisplayPort and HDMI	

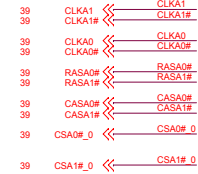
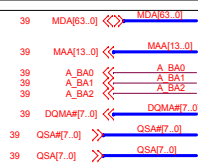
AMD RESERVED CONFIGURATION STRAPS	
Provide pull-up pads for these straps - but do not populate. GPIOs functions on these signals must not conflict with the pin strap at Reset	
H2SYNC	GENERICC
Provide pull-up pads for these straps - but do not populate. GPIOs functions on these signals must not conflict with the pin strap at Reset	
GPIO21_BB_EN	



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LVDS Interface





**MVDDQ = 1.5V FOR
DDR3 Memory**

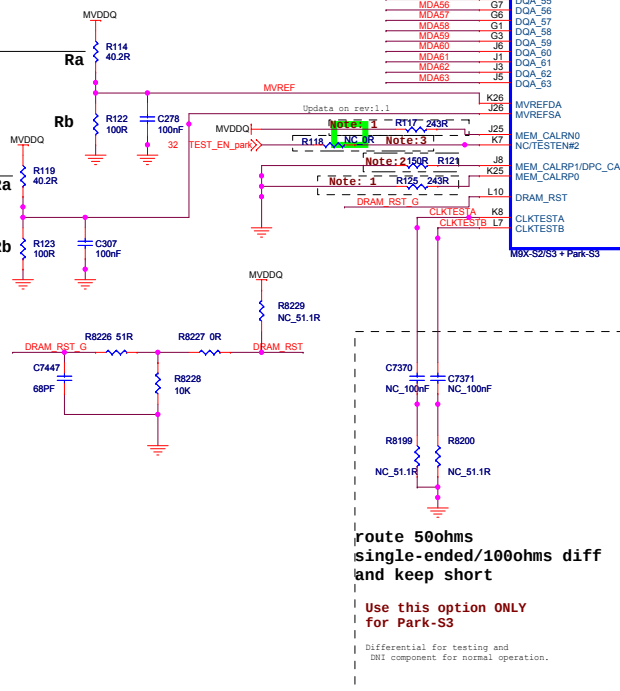
**PLACE MVREF DIVIDERS
AND CAPS CLOSE TO ASIC**

For M9X-S2/S3

DIVIDER RESISTORS	DDR2/DDR3	GDDR3
MVREF TO 1.8V (Ra)	100R	40.2R
MVREF TO GND (Rb)	100R	100R

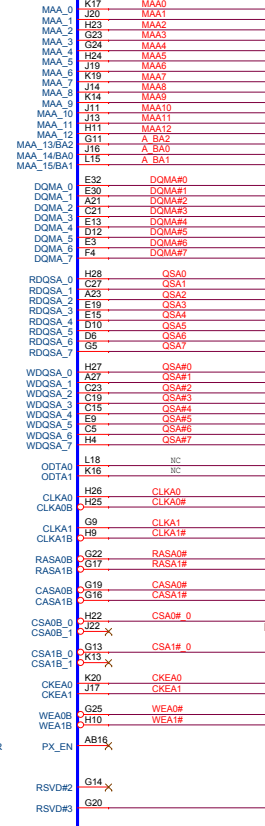
For Park-S3

DIVIDER RESISTORS	DDR2/DDR3	GDDR3
MVREF TO 1.8V (Ra)	40.2R	40.2R
MVREF TO GND (Rb)	100R	100R



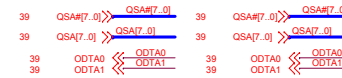
DDR3 Memory Interface

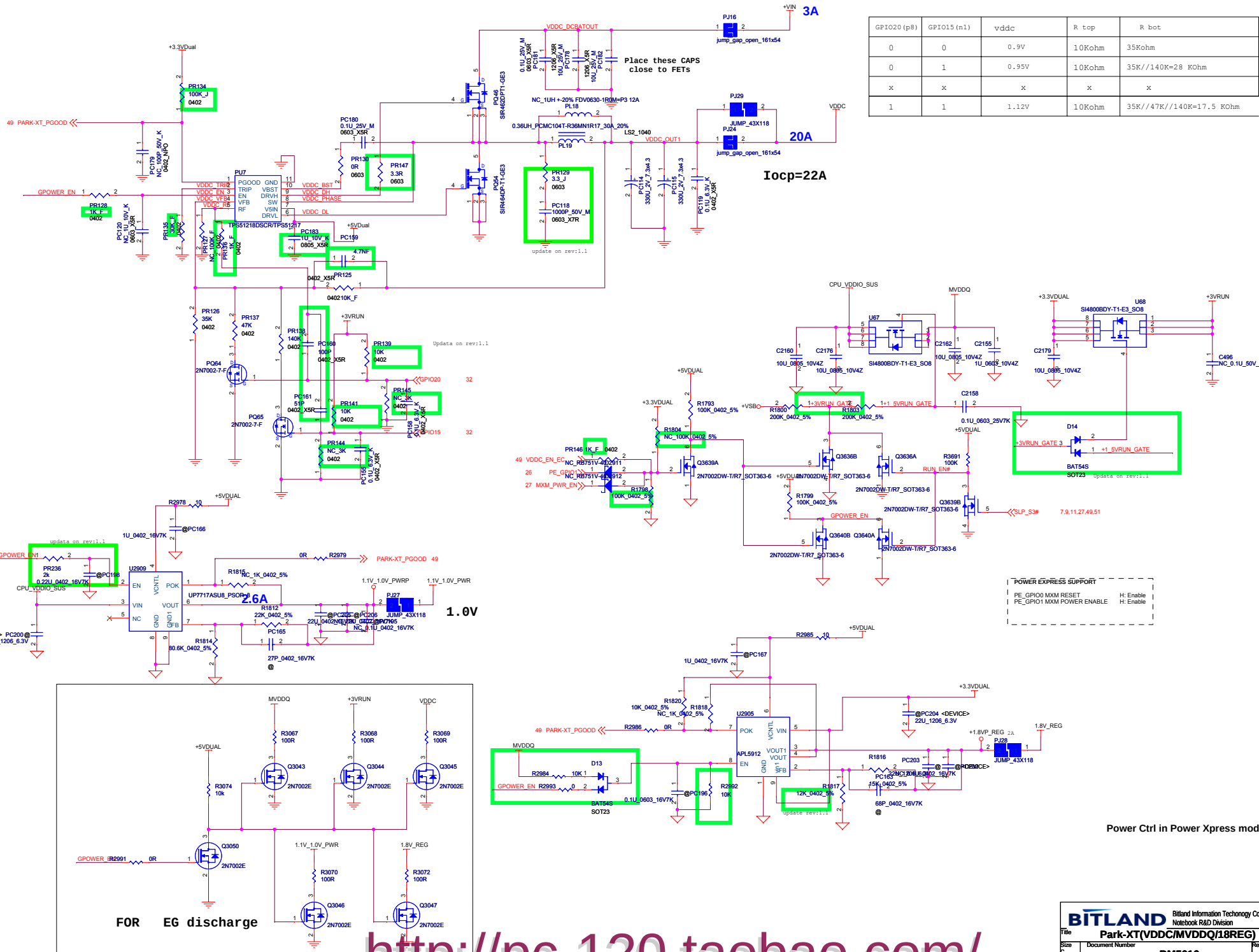
MEMORY INTERFACE



Note 1 : Do not Install for M9X-S2/S3, Install 240 Ohms 0.5% Resistor for PARK-S3.

Note 2 :For M9X-S2/S3, 38 Pin Connect to VSS through 240 ohms(0.5%) resistor.
For Park-S3, 38 Pin Connect to VSS through 150 ohms(1%) resistor for DPC_CALR
Note 3 :For M9X-92/93, K7 Pin (NC_MEM_CALRP1) is Not connected.
For PARK-S3, K7 Pin (TESTEN#2) connect to TEST_EN Signal At AF24





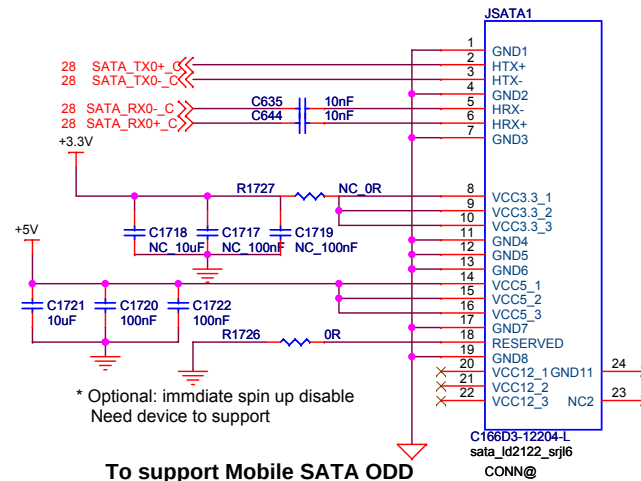
GPI020 (p8)	GPI015 (n1)	vddc	R top	R bot
0	0	0.9V	10Kohm	35Kohm
0	1	0.95V	10Kohm	35K//140K=28 KOhm
x	x	x	x	x
1	1	1.12V	10Kohm	35K//47K//140K=17.5 KOhm

POWER EXPRESS SUPPORT
H: Enable
PE_GPIO0 MXM RESET H: Enable
PE_GPIO1 MXM POWER ENABLE H: Enable

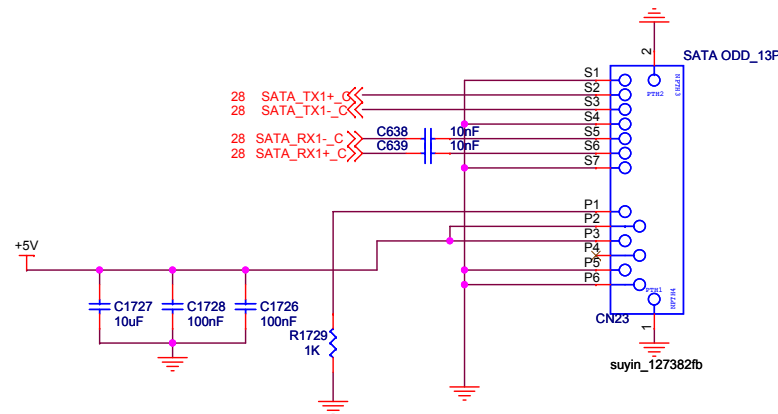
Power Ctrl in Power Xpress mode

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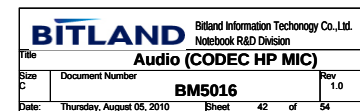
SATA HDD Conn.



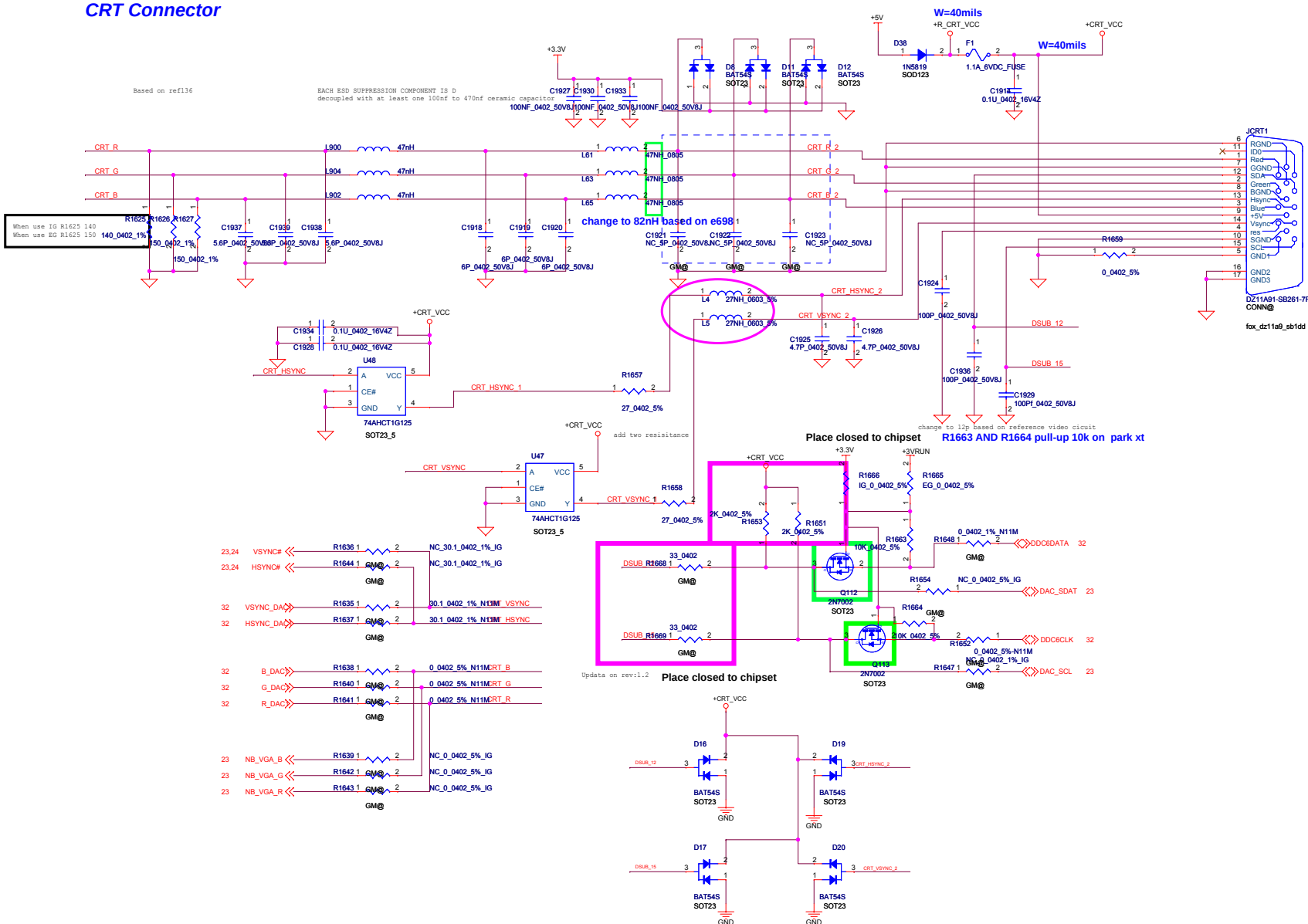
To support Mobile SATA ODD
through cable

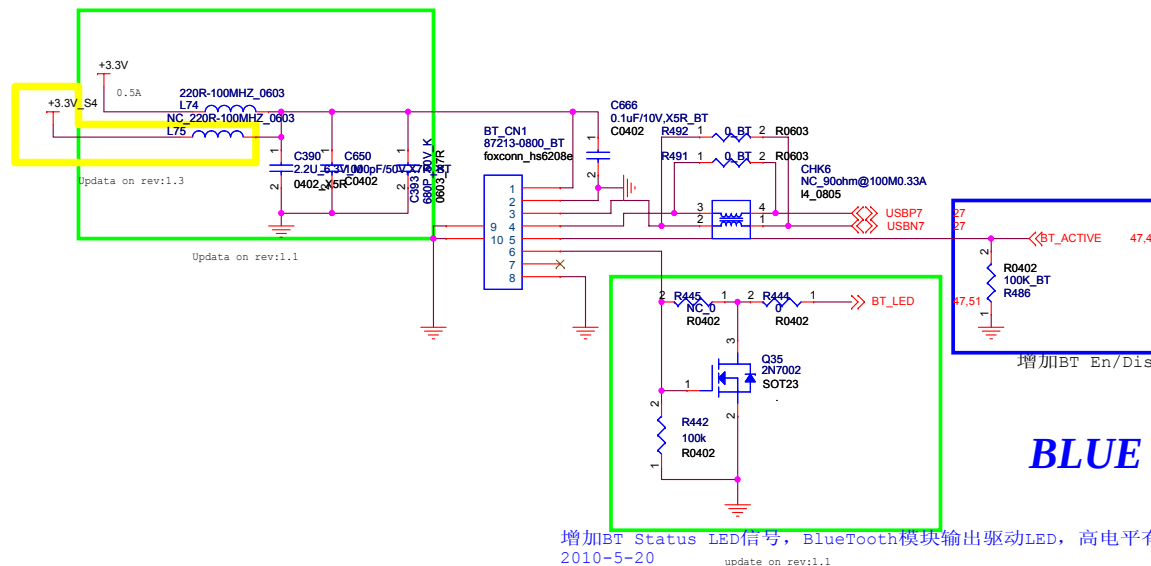


		Bitland Information Technology Co., Ltd. Notebook R&D Division	
Title SATA HDD /ODD			
Size B	Document Number BM5016		Rev 1.0
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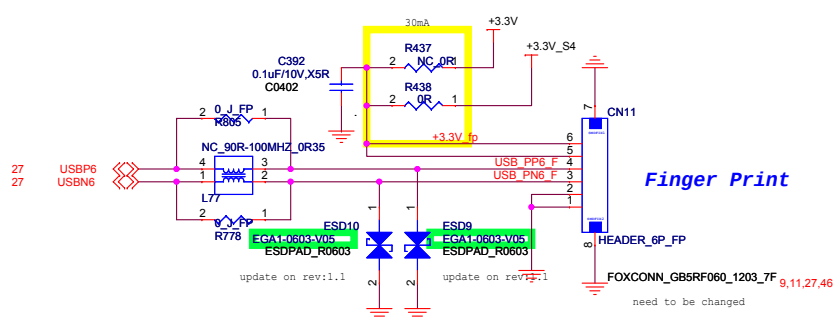


CRT Connector

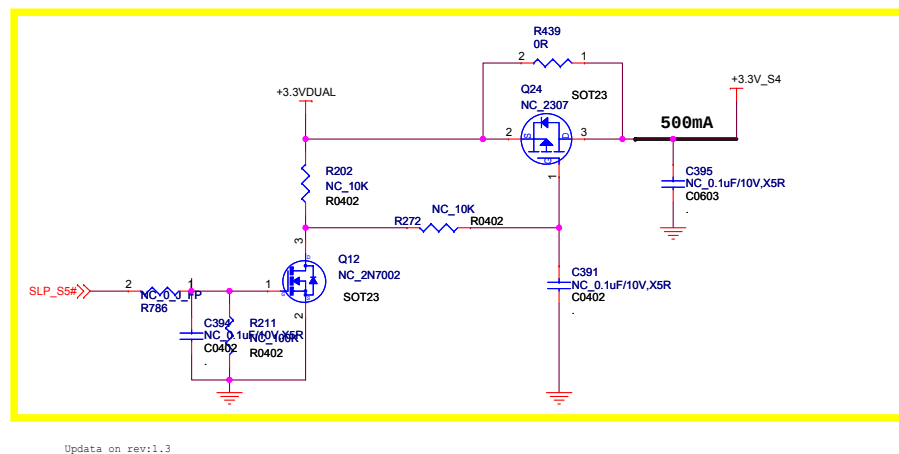




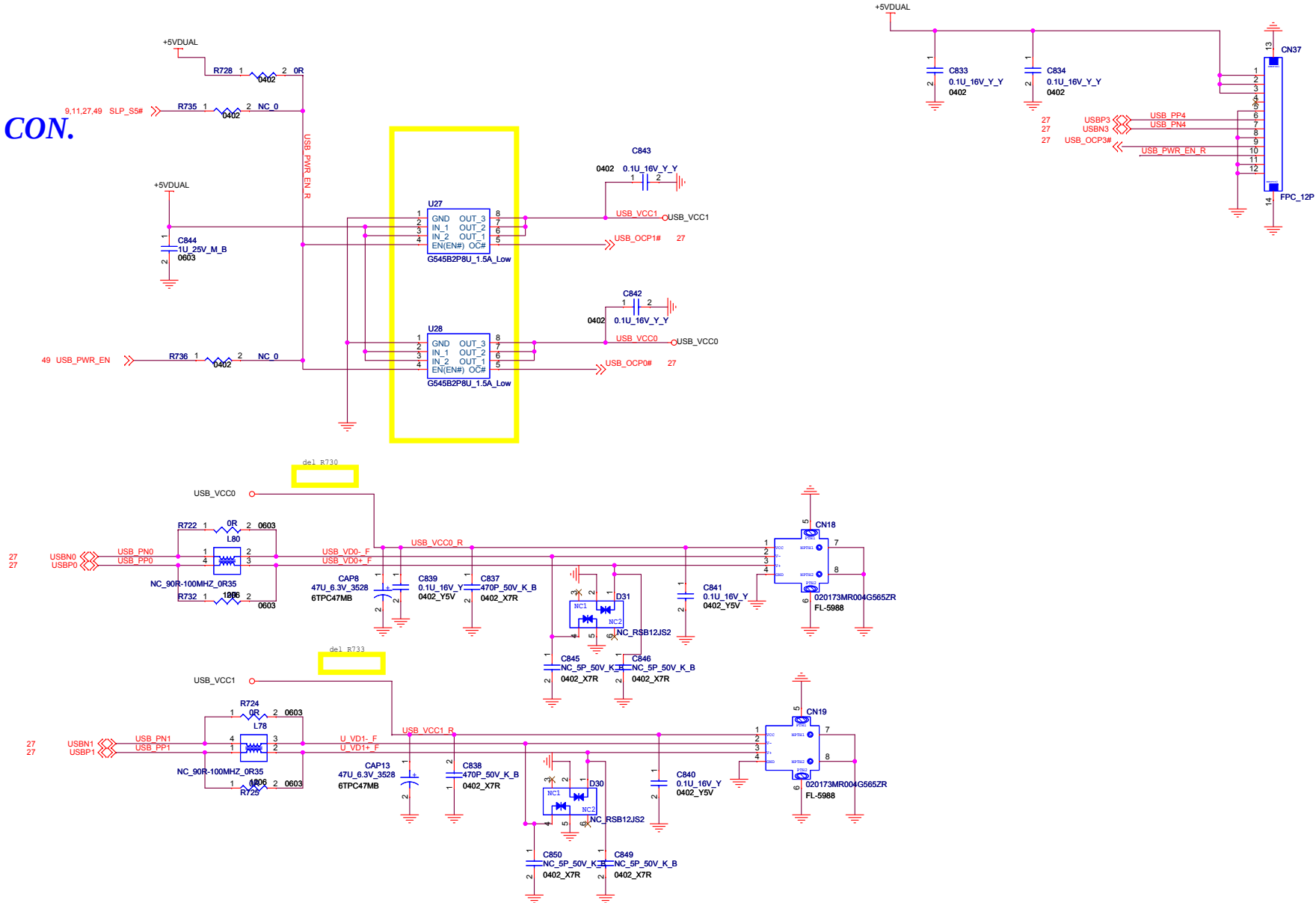
BLUE TOOTH

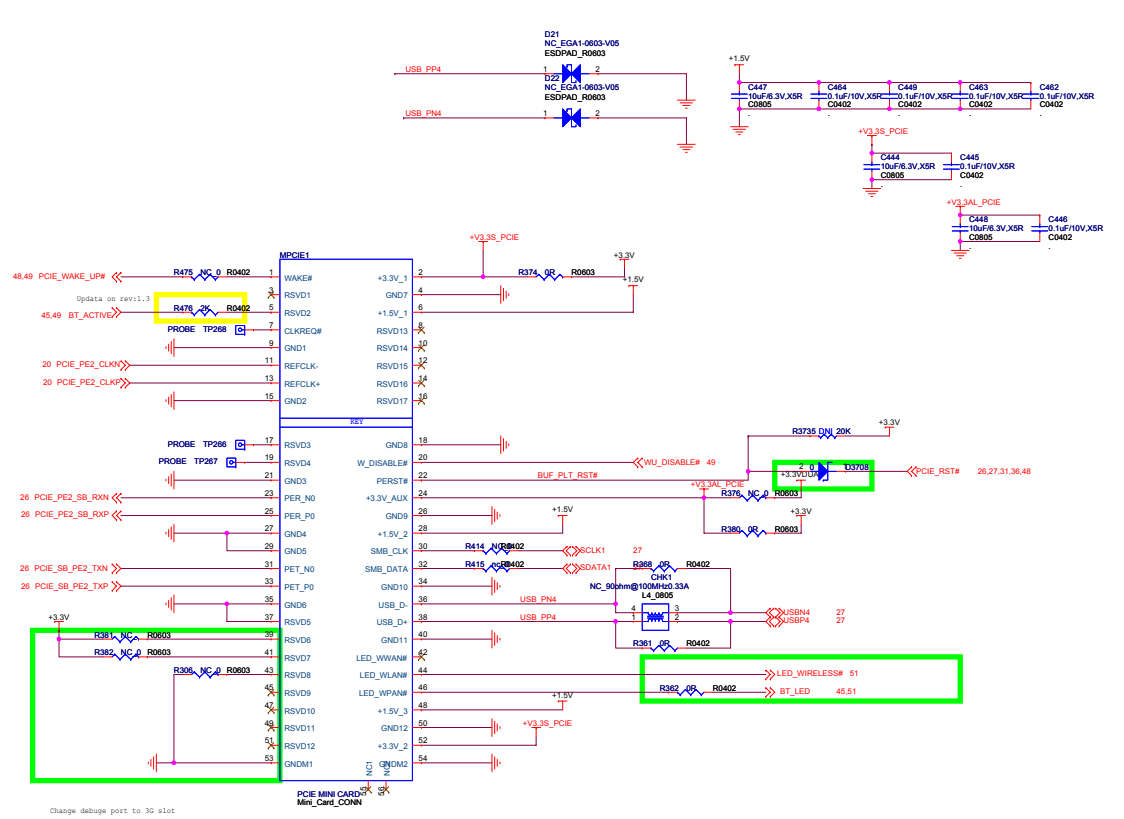


Finger Print



USB CON.

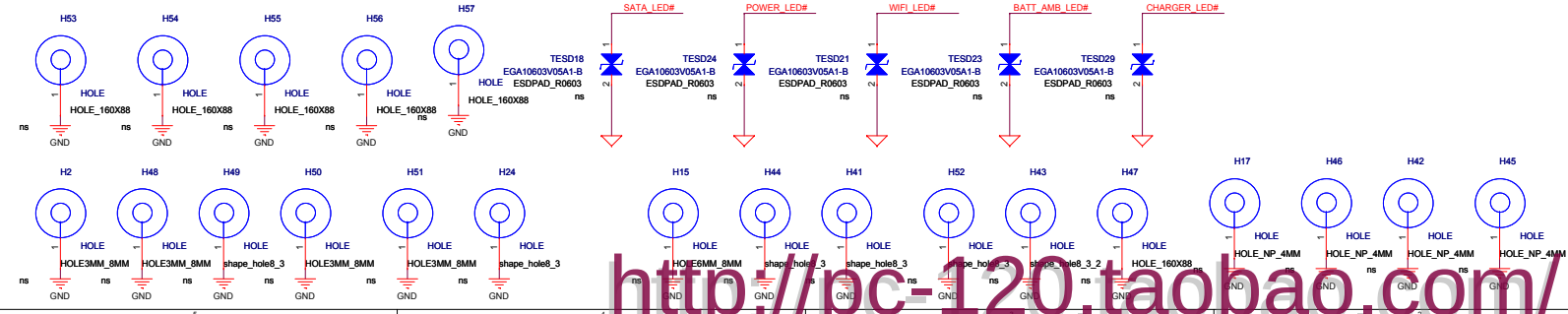
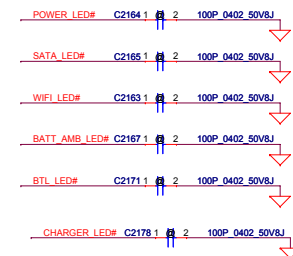






		Bitland Information Technology Co., Ltd. Notebook R&D Division	
Title		//	
Size	Document Number	Rev	
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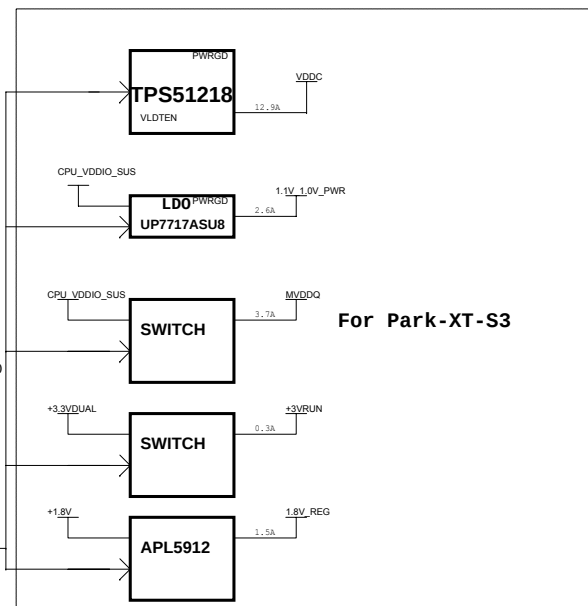
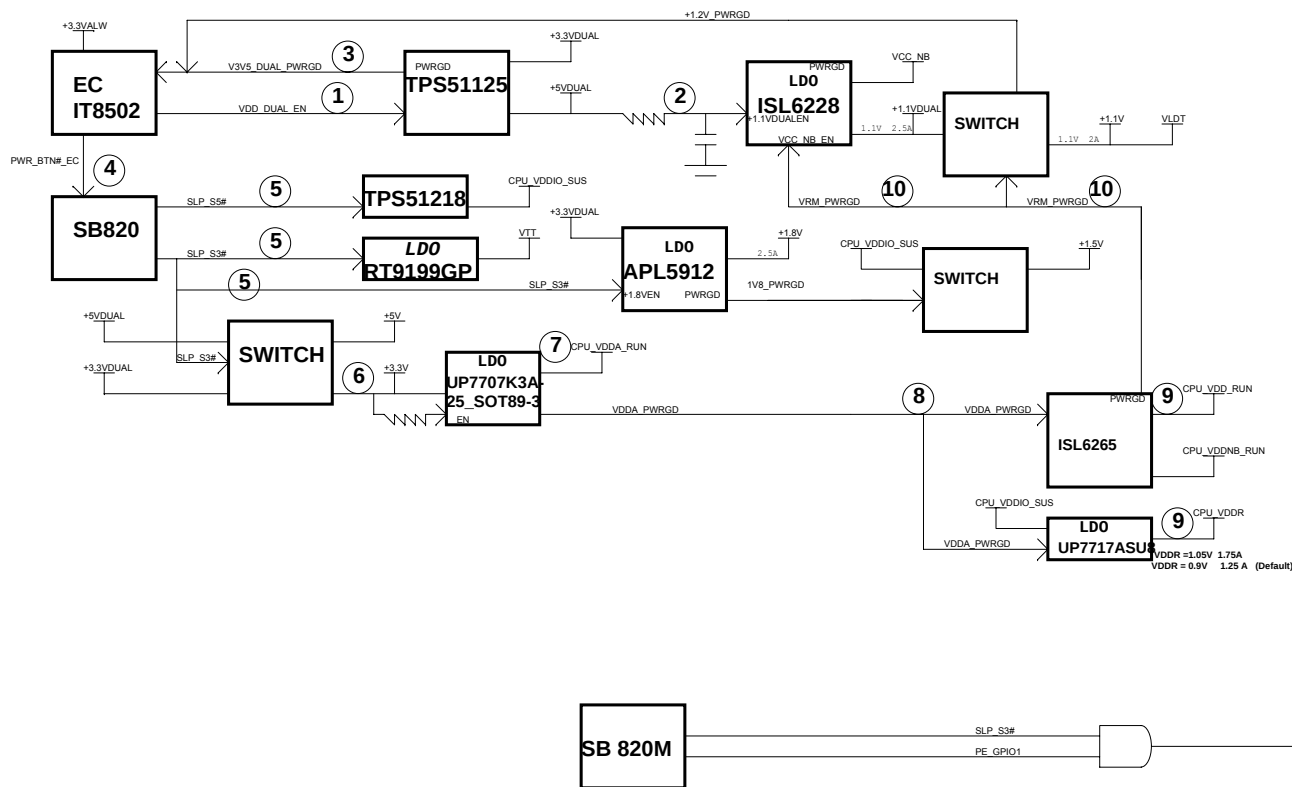


BITLAND		Bitland Information Techonogy Co.,Ltd. Notebook R&D Division	
Title		pull up resistor	
Size	Document Number	Rev	
Custom	BM5016	1.0	
Date:	Thursday, August 05, 2010	Sheet	52 of 54

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The figure is a large empty rectangular area, likely a drawing or data grid. It is bounded by a grid of letters A, B, C, and D on the left side, and numbers 1, 2, 3, 4, and 5 on the top side. The grid lines are thin and black. The area is mostly white, with a small black rectangle in the bottom right corner containing text and a logo.

Size	Document Number	Rev
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Power on Sequence required:

SB800:

- 1, +3.3VDUAL ramp before +1.1VDUAL
- 2, +3.3V ramp before +1.8v
- 3, +1.8V ramp before +1.1v
- 4, +3.3v ramp before +1.1v
- 5, +3.3VALW_R ramping down time > 300us
- 6, 50uS <= All power rails except +3.3VALW_R <= 40ms
- 7, 100uS <= +3.3VALW_R <= 40ms

RS880:

- 1, 0 < (+3.3V) - (+1.8v) < 2.1
- 2, +1.8V ramp before +1.1v
3. +1.1V ramp before VCC_NB

各电源PWM/L/MOS选型

POWER	PWM	L	H_GATE	L_GATE
+3.3VDUAL (+3.3V 8A)	TI/TPS51125RGER	HB90479MA0LFE 4.7uH±20% 5.5A 40mD SMD-E 8946 47x3.0mm	30V 11.6A MOS (ON) C22mD (VDS=4.5V)	A04468
+5VDUAL (+5V 8A)	VQFN24	HB90479MA0LFE 4.7uH±20% 5.5A 40mD SMD-E 8946 47x3.0mm	30V 11.6A MOS (ON) C22mD (VDS=4.5V)	A04468
VCC_NB (+1.1V 12A)	ISL6228HRTZ-T	HB90109M00LFE 1.0uH ±20% 12A 10mD SMD-E 8946 47x3.0mm	VISHAY/SI4172DY-T1-GE3 30V 11.6A MOS (ON) C22mD (VDS=4.5V)	VISHAY/SI4168DY-T1-GE3
VLDY (+1.1V 4A)	TOFN28	HB90479MA0LFE 4.7uH±20% 5.5A 40mD SMD-E 8946 47x3.0mm	L/H integrated (待定)	
VDDIO_SUS (+1.5V 31A)	TPS51218 D8C	HB90109M00LFE 1.0uH ±20% 12A 10mD SMD-E 8946 47x3.0mm	VISHAY/SI4172DY-T1-GE3 30V 11.6A MOS (ON) C22mD (VDS=4.5V)	VISHAY/SI4168DY-T1-GE3
CPU_VDD_RUN (+1.375V -1.5V 36A)	ISL6265 QFN48	HB90479MA0LFE 4.7uH±20% 5.5A 40mD SMD-E 8946 47x3.0mm	PHASE1 VISHAY/SIR462DP-T1-GE3 30A 17.20V 0.1008 2V Power MOS 20-140	VISHAY/SIR468DY-T1-E3/GE3(two)
		HB90479MA0LFE 4.7uH±20% 5.5A 40mD SMD-E 8946 47x3.0mm	PHASE2 VISHAY/SIR462DP-T1-GE3 30A 17.20V 0.1008 2V Power MOS 20-140	VISHAY/SIR468DY-T1-E3/GE3(two)
CPU_VDDNB_RUN (0.3V 4A)	ISL6265 QFN48	HB90479MA0LFE 4.7uH±20% 5.5A 40mD SMD-E 8946 47x3.0mm	L/H integrated (待定)	
		HB90109M00LFE 1.0uH ±20% 12A 10mD SMD-E 8946 47x3.0mm	L/H integrated (待定)	
charger	ISL6251HAZ SSOP24 25 150	HB90109M00LFE 10uH±20% 10A 40mD 71.2mD SMD E 8946 47x3.0mm	AOS/AON7408 30V 11.6A MOS (ON) C22mD (VDS=4.5V) DFN-8	AOS/AON7702 20A MOS (ON) C1.4mD (VDS=4.5V) DFN-8

LDO

VTT	RT9199GP	(+1.5V...+0.75 1.5A)
CPU_VDDA_RUN	APL5508 25DC TRL SOT89-3	(+3.3V...+2.5V 500mA)
+1.8V	APL5930	(+3.3V...+2.5 1.5A)
CPU_VDDR	APL5912	(+1.5V...+1.05V 4A)
+1.1VDUAL	APL5930	(+3.3V...+1.1V 500mA)

SWITCH

INPUT(V)	OUTPUT(V)	MOS
+5VDUAL	+5V	A04468 (8A)
+3.3VDUAL	+3.3V	A04468 (8A)
VLDY	+1.1V	JUMPER (4A)
CPU_VDDIO_SUS	+1.5V	A04468 (5A)