AG1 Block Diagram

Project code: 91.4A901.001
PCB P/N : 55.4A903.XXX
REVISION : 05225-1
(Hannstar, GCE)

PCB STACKUP

TOP
VCC
S
S
GND
BUTTOM

CLK GEN.
ICS954305D
(IDT CV155) 3

Mobile CPU
Yonah 478
Celeron M 4, 5

G792 19

HOST BUS 400/533/667MHz

DDR2 533/667 MHz 11,12
533/667MHz

DDR2 533/667 MHz 11,12
533/667MHz

Calistoga 6,7,8,9,10

TVO 14

LVDS 14"WSXGA+ LCD 13

RGB CRT CRT 14

DMI I/F 100MHz

ICH7-M 15,16,17,18

Line In 29
MIC In 29
Codec ALC883 28
AZALIA

Line Out (SPDIF) 29
OP AMP G1421B 29

INT.SPKR 29

RJ11
MODEM MDC Card 21

PCI Express
New card 30

SATA
PATA

USB 3 PORT 21

PWR SW TPS2231 30
HDD 20
CDROM 18
MINI USB 21 Blue-tooth

PCI BUS

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CARDBUS 1394 CardReader 24,25

PCMCIA I/F
PWR SW TSP2220A 27
PCMCIA SLOT Support TypeII 27

1394 CONN 26

MS/MS Pro/xD/ MMC/SD/SDIO 6 in 1 26

Mini-PCI TV Tuner 30

LAN 10/100 BCM4401-E 22
TXFM 23
RJ45 23

PCIEx1
Mini Card*2 802.11A/B/G 26
Giga LAN 22 BCM5798

SPI I/F
SPI Flash

LPC BUS
SIO NS 87392 32
KBC HD64F2111BVC 31
LPC DEBUG CONN. 34

FIR 32
Touch Pad 33
INT. KB 33

SYSTEM DC/DC
TPS51120 41

INPUTS	OUTPUTS
DCBATOUT	5V_S5 3V_S5

SYSTEM DC/DC
MAX8743EE 42

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3

TPS51100 44

1D8V_S3	DDR_VREF

APL5332KAC 44

3D3V_S5	2D5V_S0

APL5912-U 44

3D3V_S5	1D5V_S0

MAXIM CHARGER
MAX8725+Max1773 43

INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 4.0A UP+5V 5V 100mA

CPU DC/DC
ISL6262 39,40

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0~1.3V 48A

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM
Size: A3
Document Number: AG1
Rev: -1
Date: Monday, January 09, 2006
Sheet 1 of 45

ICH7M Integrated Pull-up and Pull-down Resistors

ICH7-M EDS 17837 1.5V1

EE_DIN, EE_DOUT, GNT[3:0], GPIO[25], GNT[4]#/GPIO48, GNT[5]#/GPO17, PME#, LAD[3:0]#/FHW[3:0]#, LAN_RXD[2:0] LDRQ[0], LDRQ[1]/GPIO[41], PWRBTN#, TP[3]	ICH7 internal 20K pull-ups
DD[7], DDREQ	ICH7 internal 11.5K pull-downs
ACZ_BIT_CLK, ACZ_RST#, ACZ_SDIN[2:0], ACZ_SDOUT, ACZ_SYNC, DPRSLPVR/GPIO16, EE_CS, SPI_ARB, SPI_CLK, SPKR,	ICH7 internal 20K pull-downs
USB[7:0][P,N]	ICH7 internal 15K pull-downs
SATALED#	ICH7 internal 15K pull-up
LAN_CLK	ICH7 internal 100K pull-down

ICH7M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

ICH7M Functional Strap Definitions

page 16

Signal	Usage/When Sampled	Comment
ACZ_SDOUT	XOR Chain Entrance/ PCIE Port Config bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)
ACZ_SYNC	PCIE bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
EE_CS	Reserved	This signal should not be pull high.
EE_DOUT	Reserved	This signal should not be pull low.
GNT2#	Reserved	This signal should not be pull low.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT5#/ GPIO17#, GNT4#/ GPIO48	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT5# is MSB, 01-SPI, 10-PCI, 11-LPC.
DPRSLPVR	Reserved	This signal should not be pull high.
GPIO25	Reserved. Rising Edge of RSMRST#.	This signal should not be pull low.
INTVRMEN	Integrated VccSus1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05 VRM when sampled high
LINKALERT#	Reserved	Requires an external pull-up resistor.
REQ[4:1]#	XOR Chain Selection. Rising Edge of PWROK.	TBD, Chapter 6
SATALED#	Reserved	This signal should not be pull low.
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH7 will disable the TCO Timer system reboot feature). The status is readable via the NO_REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.

954305D 27Mhz/LCDCLK Spread and Frequency Selection Table

page 3

SS3 Byte9 bit 7	SS2 bit6	SS1 bit5	SS0 bit4	Spread Amount%
0	0	0	0	-0.50 Down
0	0	0	1	-1.00 Down
0	0	1	0	-1.50 Down
0	0	1	1	-2.00 Down
0	1	0	0	-0.75 Down
0	1	0	1	-1.25 Down
0	1	1	0	-1.75 Down
0	1	1	1	-2.25 Down
1	0	0	0	+-0.25 Center
1	0	0	1	+-0.5 Center
1	0	1	0	+-0.75 Center
1	0	1	1	+-1.0 Center
1	1	0	0	+-0.25 Center
1	1	0	1	+-0.5 Center
1	1	1	0	+-0.75 Center
1	1	1	1	+-1.0 Center

PCI Routing

page 16

	IDSEL	INT -> PIRQ	REQ/GNT
7412	22	A->G, B->B, C->F, D->G	0
MiniPCI	21	A/C -> E B/D -> E	1
LAN	23	A -> H	2
1410	25	A->G, B->B,	0

Calistoga Strapping Signals and Configuration

EDS 17050 0.71

page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 =Mobile CPU(Default)
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG17	Global R-comp Disable (All R-comps)	0 = All R-comp Disable 1 = Normal Operation (Default)
CFG18	VCC Select	0 = 1.05V (Default) 1 = 1.5V
CFG19	DMI Lane Reversal	0 = Normal operation (Default):lane Numbered in order 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	0 = Only SDVO or PCIE x1 is operational (Default) 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL_DATA	SDVO Present	0 = No SDVO Card present (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading edge of the Calistoga GMCH PWORK in signal.

History

6/6 drawing SA
7/11 Rename for placement

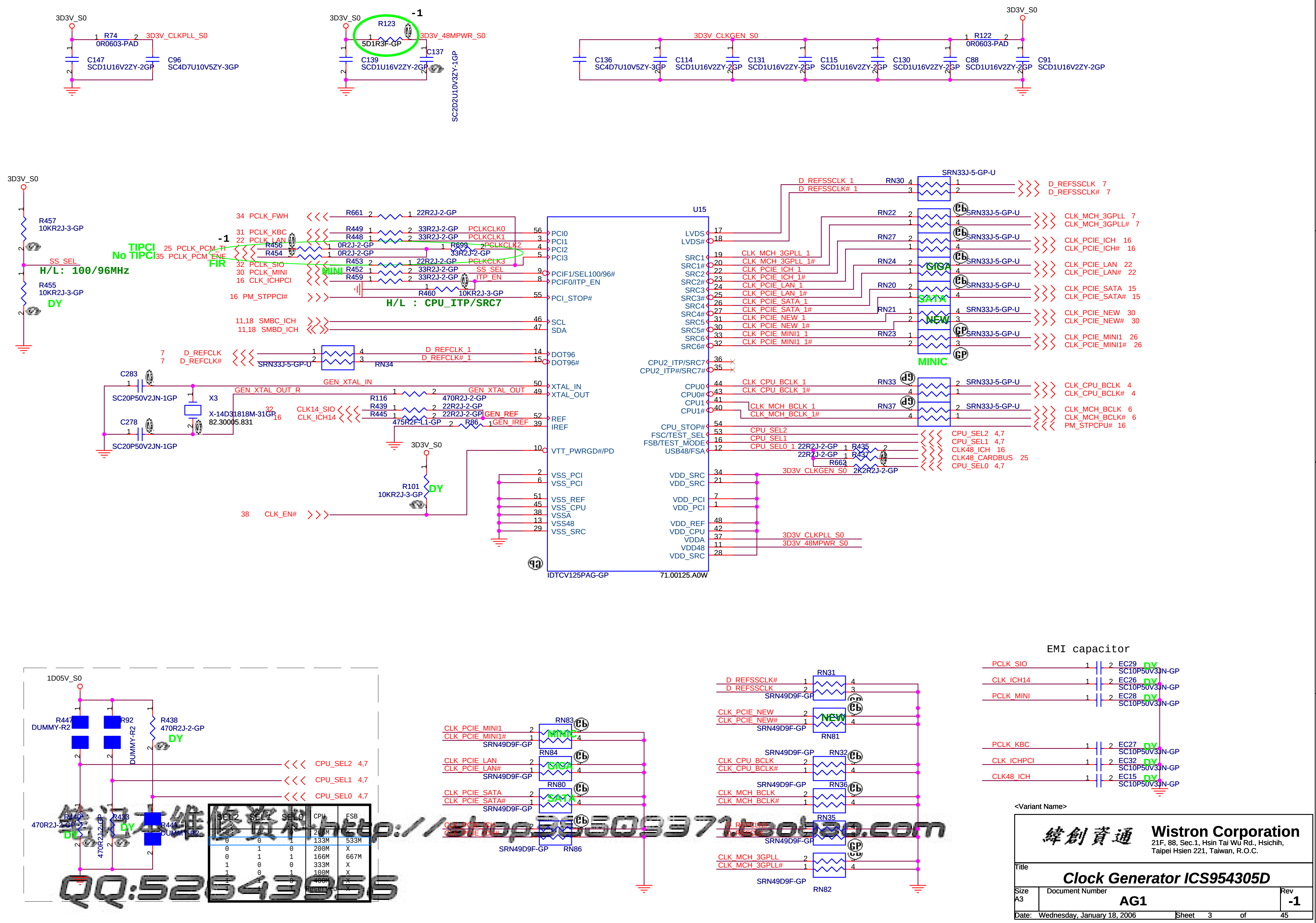
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Reference

Size: A3 | Document Number: AG1 | Rev: -1

Date: Monday, January 09, 2006 | Sheet 2 of 45



SEL2	SEL1	SEL0	CPU	FSB
0	0	0	266M	X
0	0	1	133M	533M
0	1	0	200M	X
0	1	1	166M	667M
1	0	0	333M	X
1	0	1	100M	X
1	1	0	400M	X
1	1	1	Reserved	X

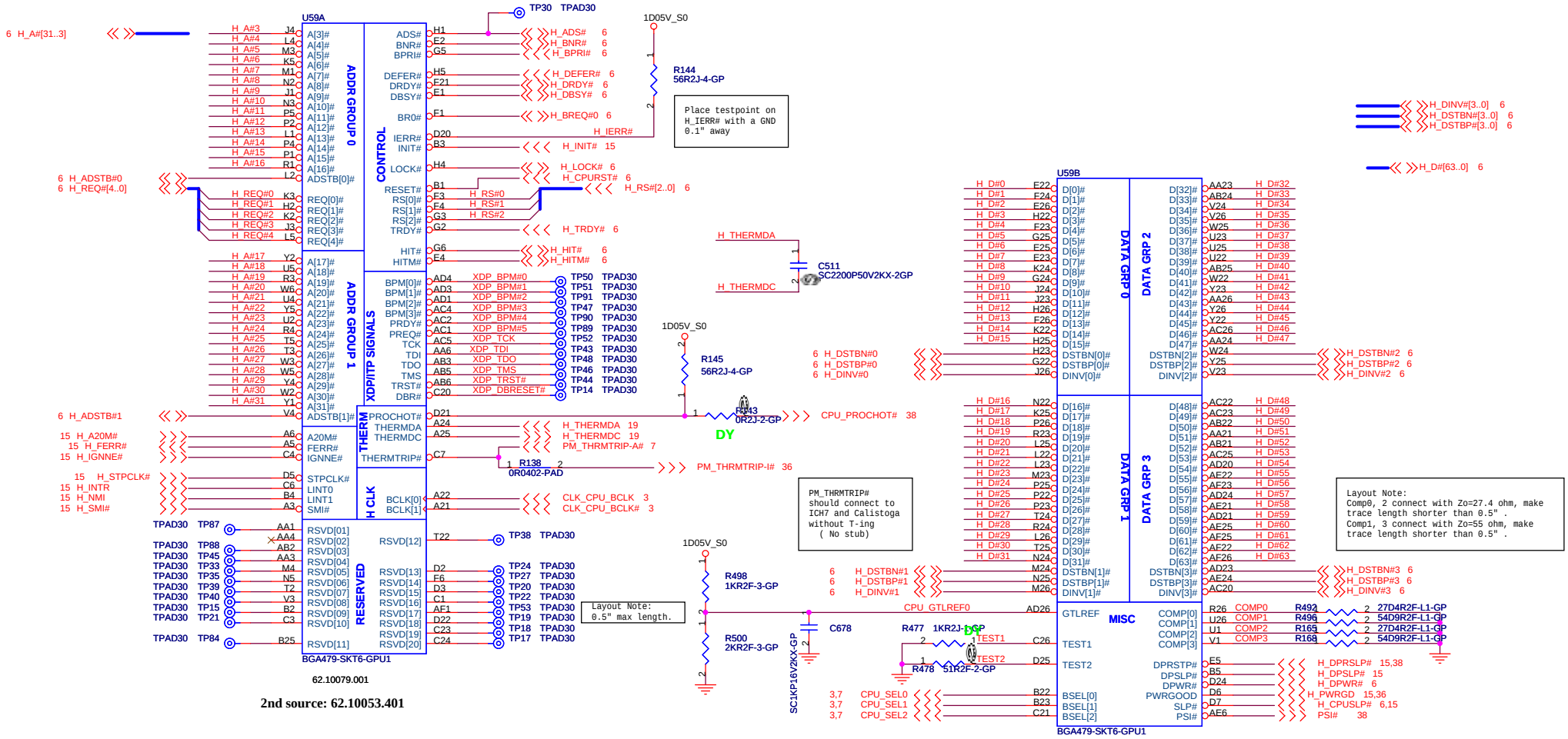
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Clock Generator ICS954305D**

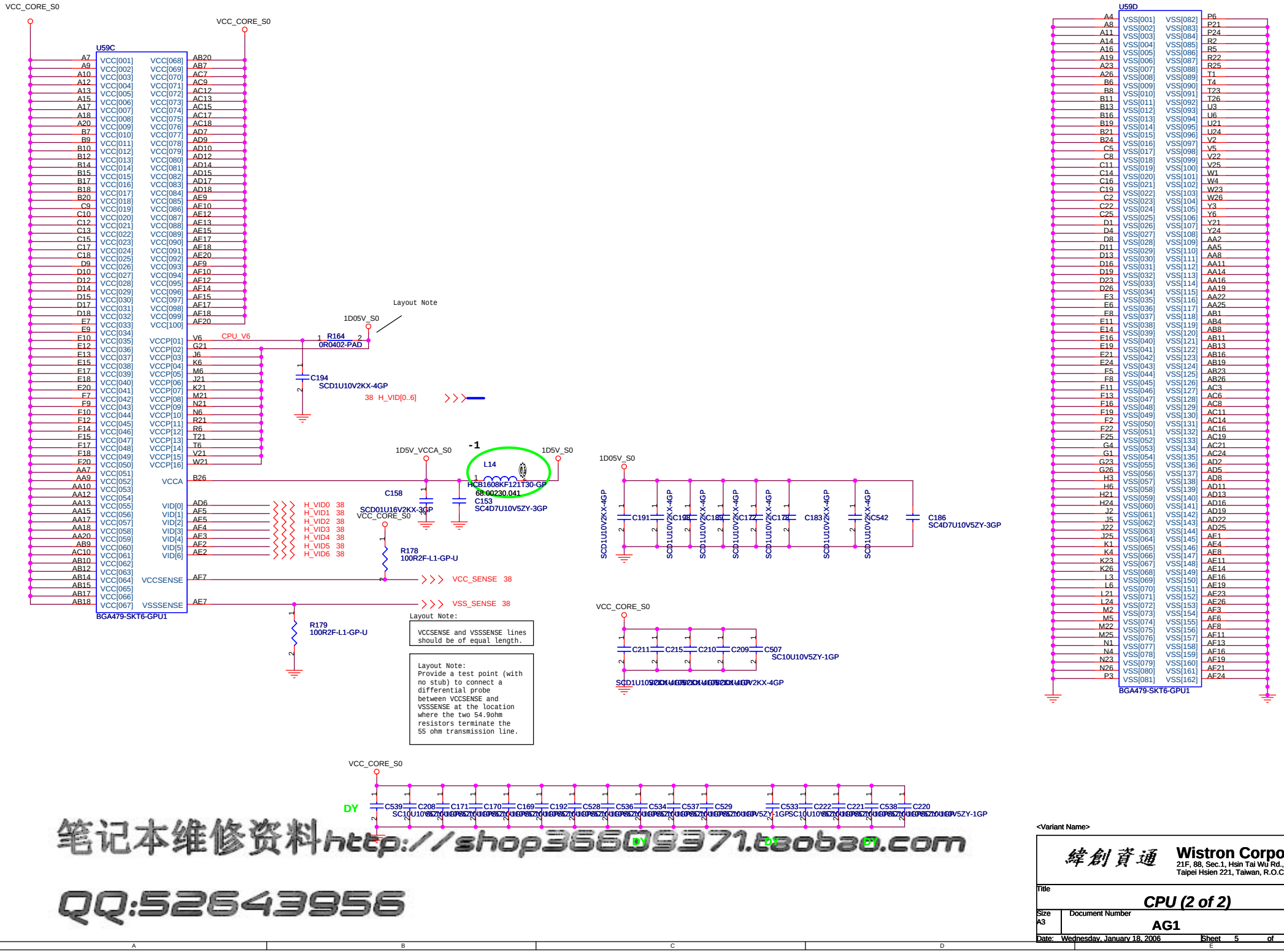
Size: A3 | Document Number: AG1 | Rev: -1

Date: Wednesday, January 18, 2006 | Sheet 3 of 45



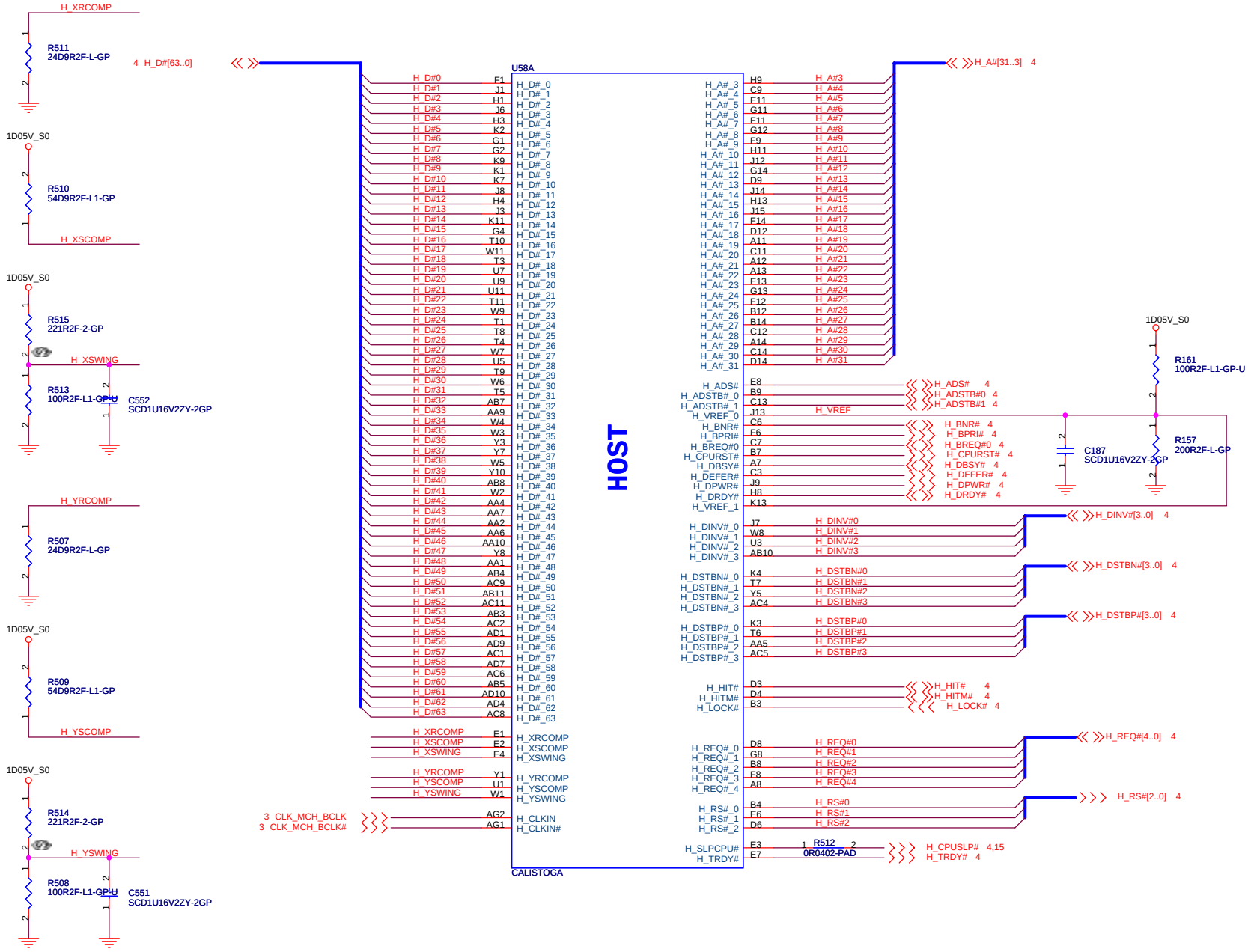
<Variant Name>

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	CPU (1 of 2)
Size A3	Document Number AG1 Rev -1
Date: Wednesday, January 18, 2006	Sheet 4 of 45



<Variant Name>

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	CPU (2 of 2)
Size: A3	Document Number: AG1
Rev	-1
Date: Wednesday, January 18, 2006	Sheet 5 of 45



Place them near to the chip (< 0.5")

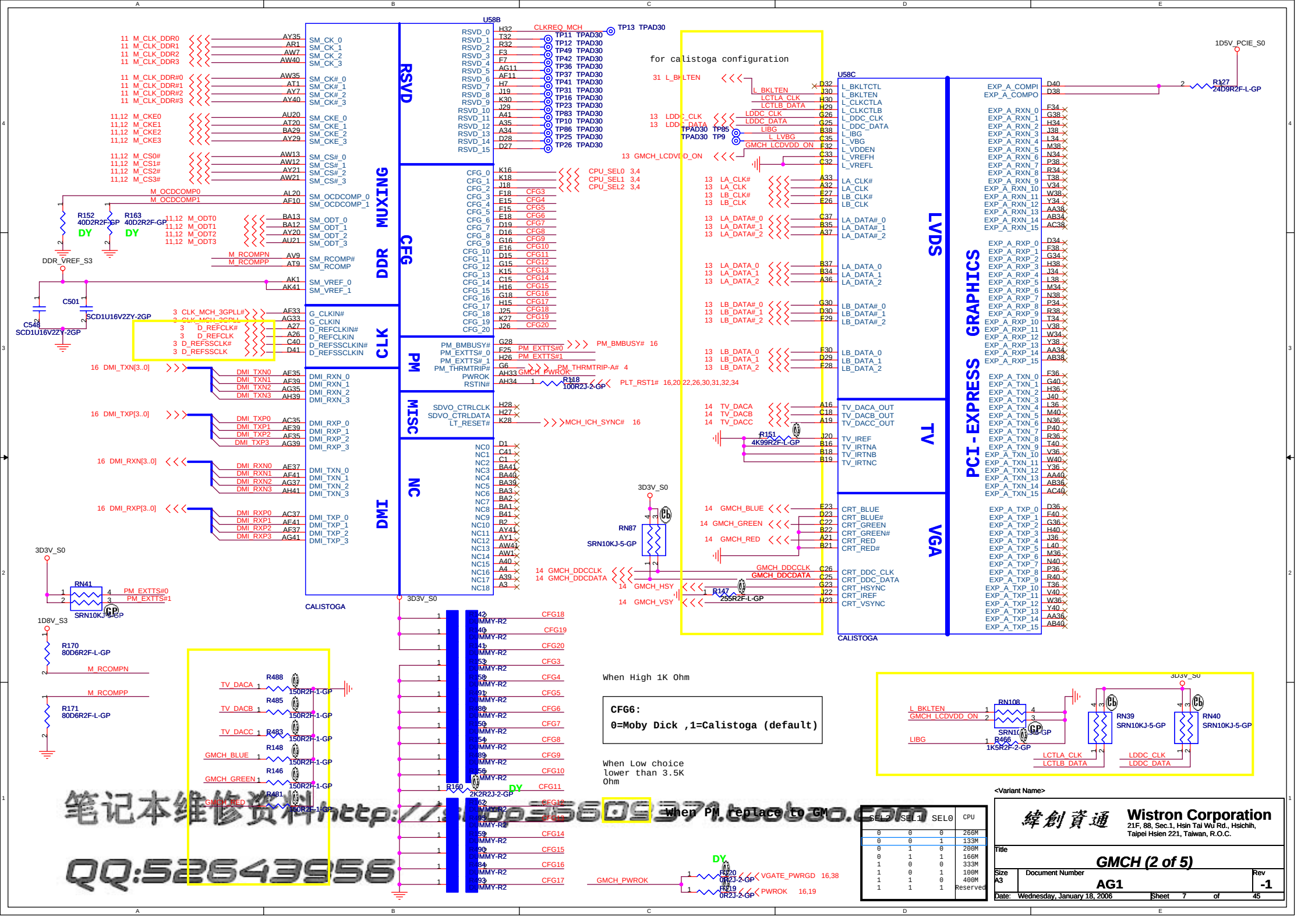
<Variant Name>

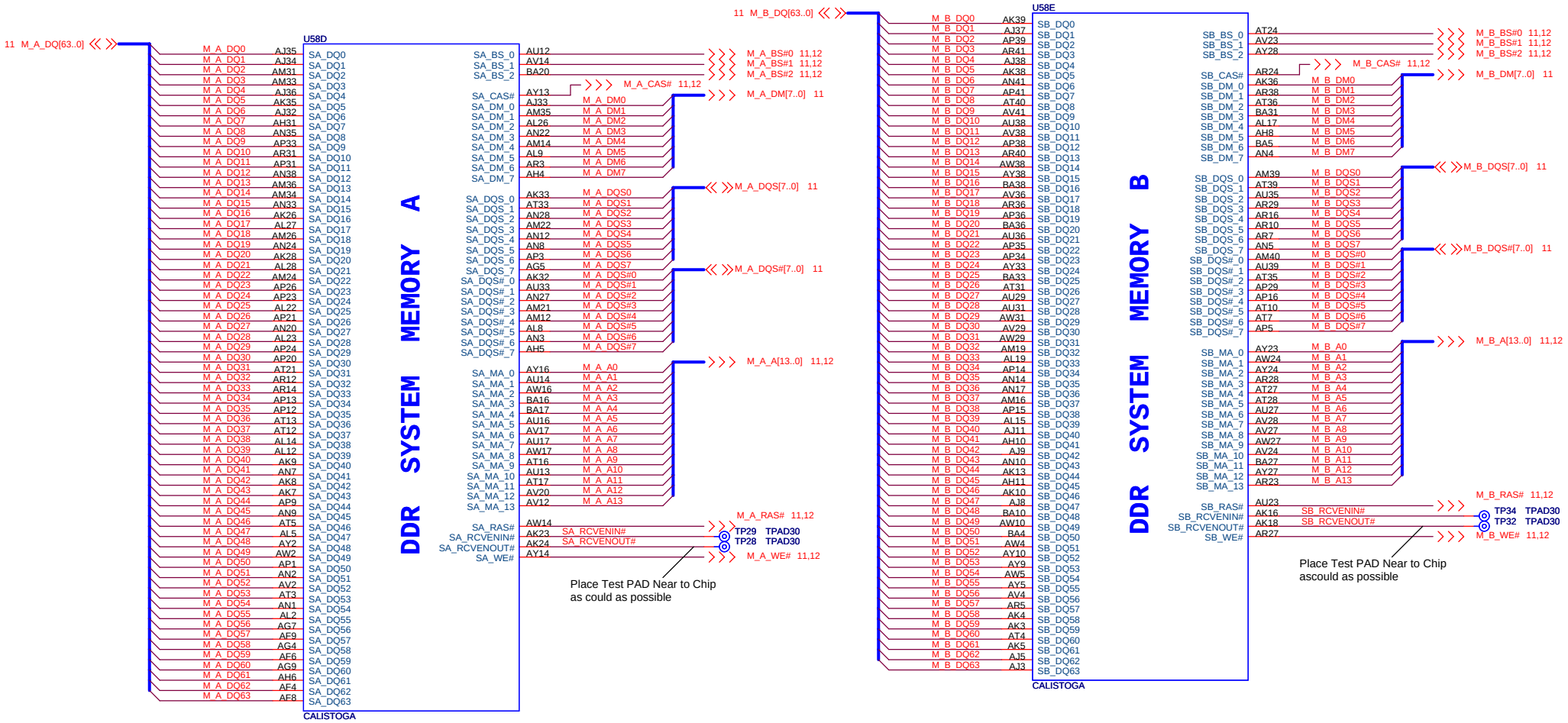
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GMCH (1 of 5)

Size: A3 | Document Number: AG1 | Rev: -1

Date: Wednesday, January 18, 2006 | Sheet 6 of 45





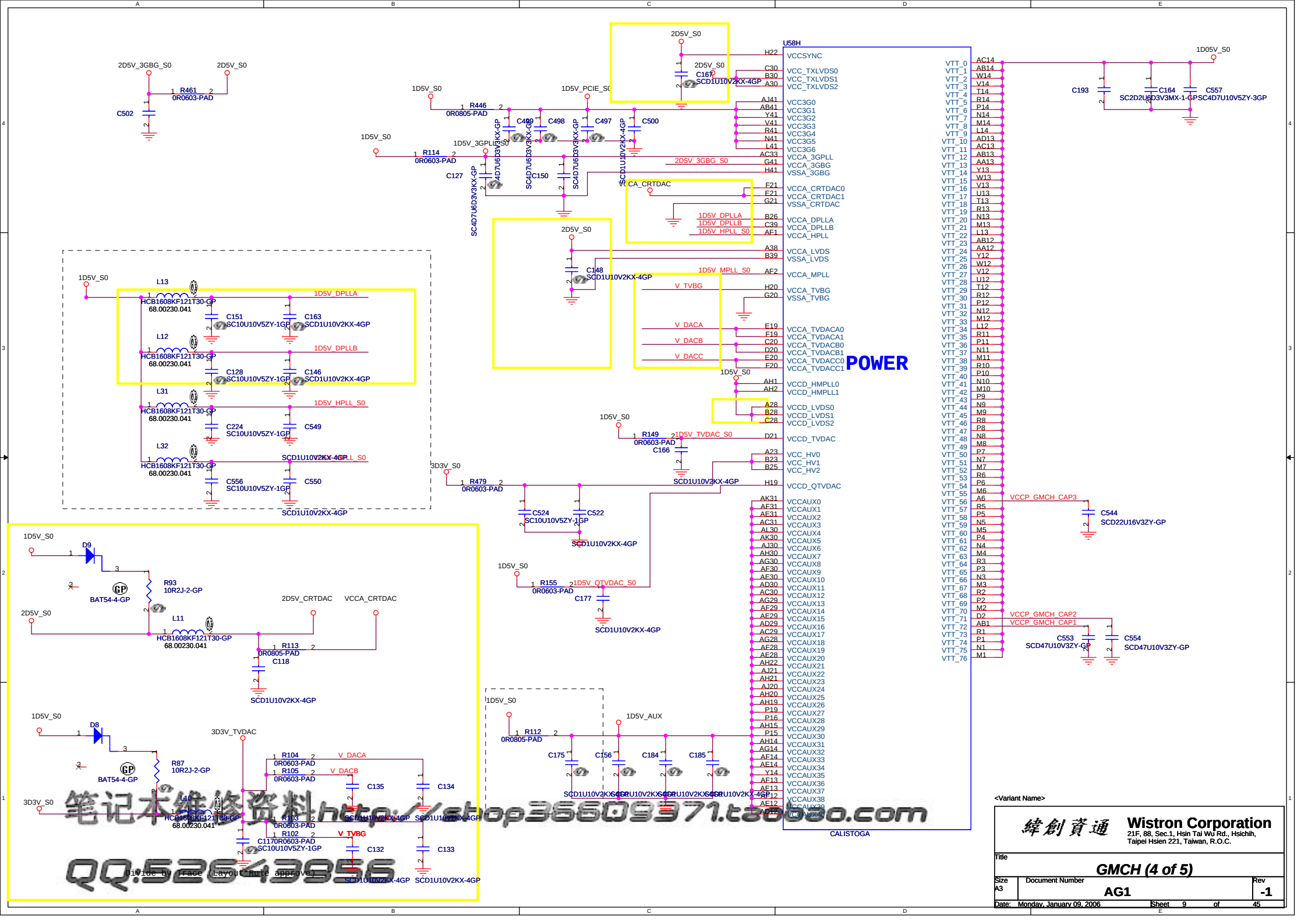
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GMCH (3 of 5)

Size: A3 | Document Number: AG1 | Rev: -1

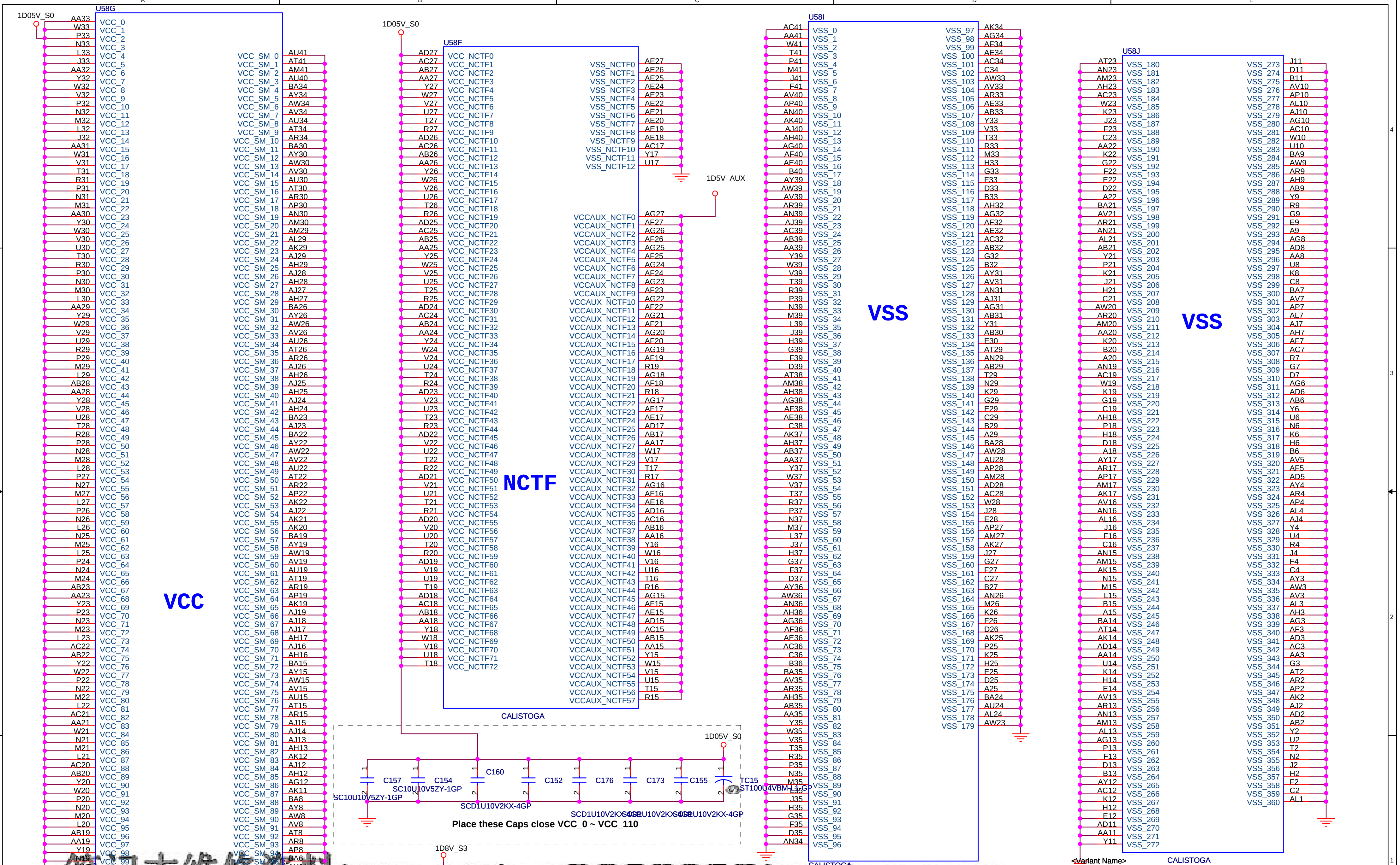
Date: Wednesday, January 18, 2006 | Sheet 8 of 45



Title: GMCH (4 of 5)

Size: A3 | Document Number: AG1 | Rev: -1

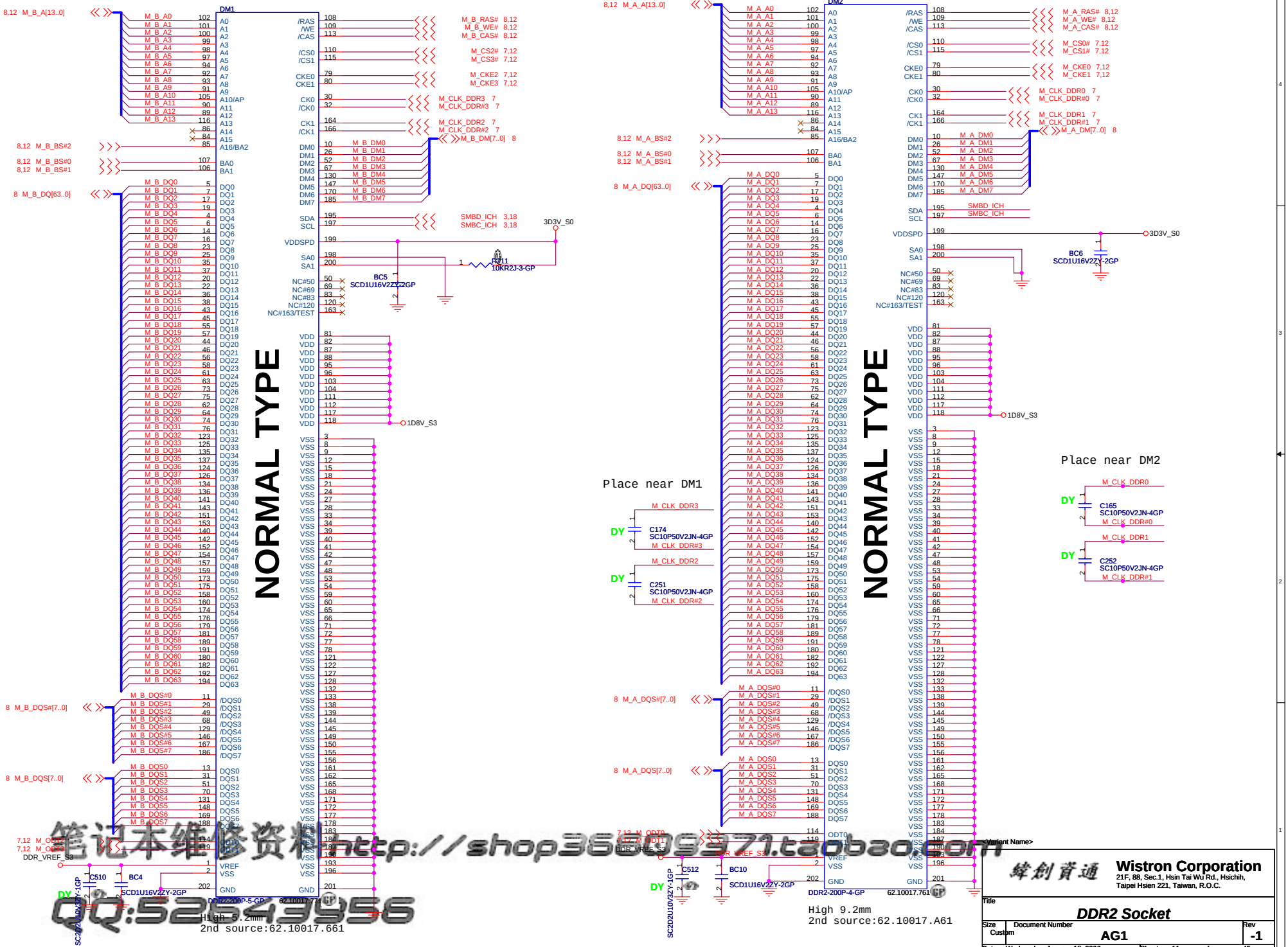
Date: Monday, January 09, 2006 | Sheet 9 of 45



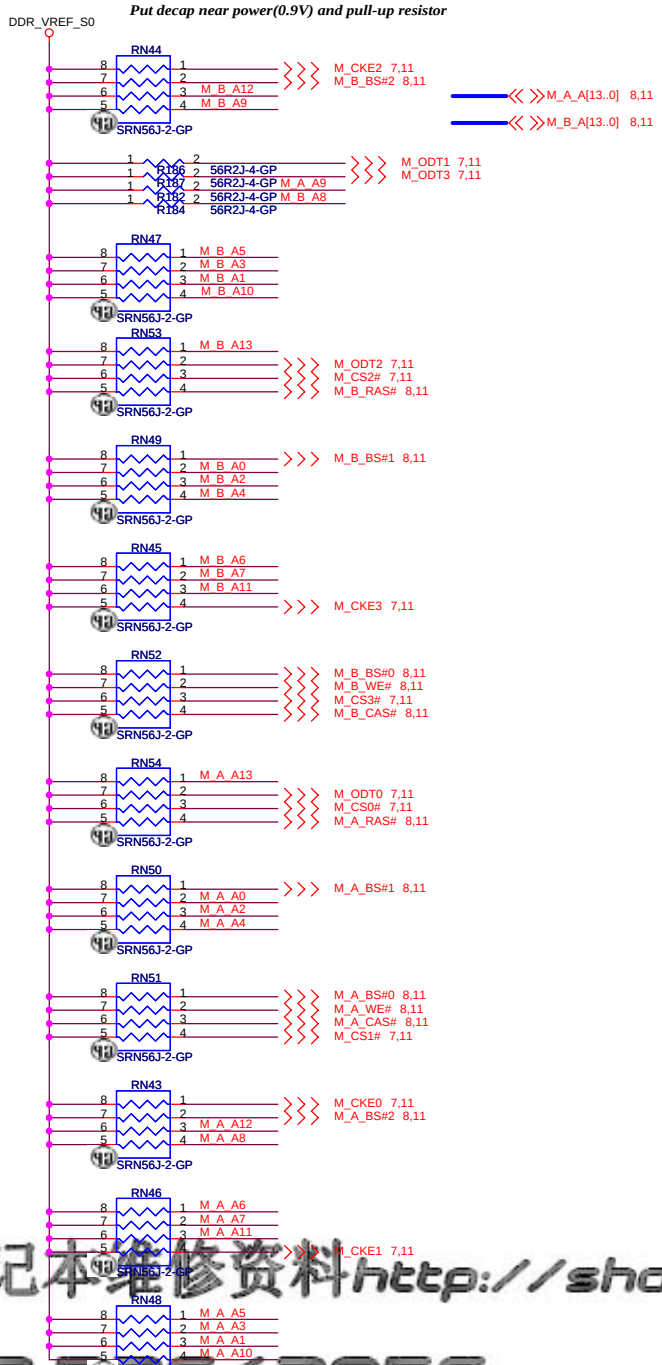
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

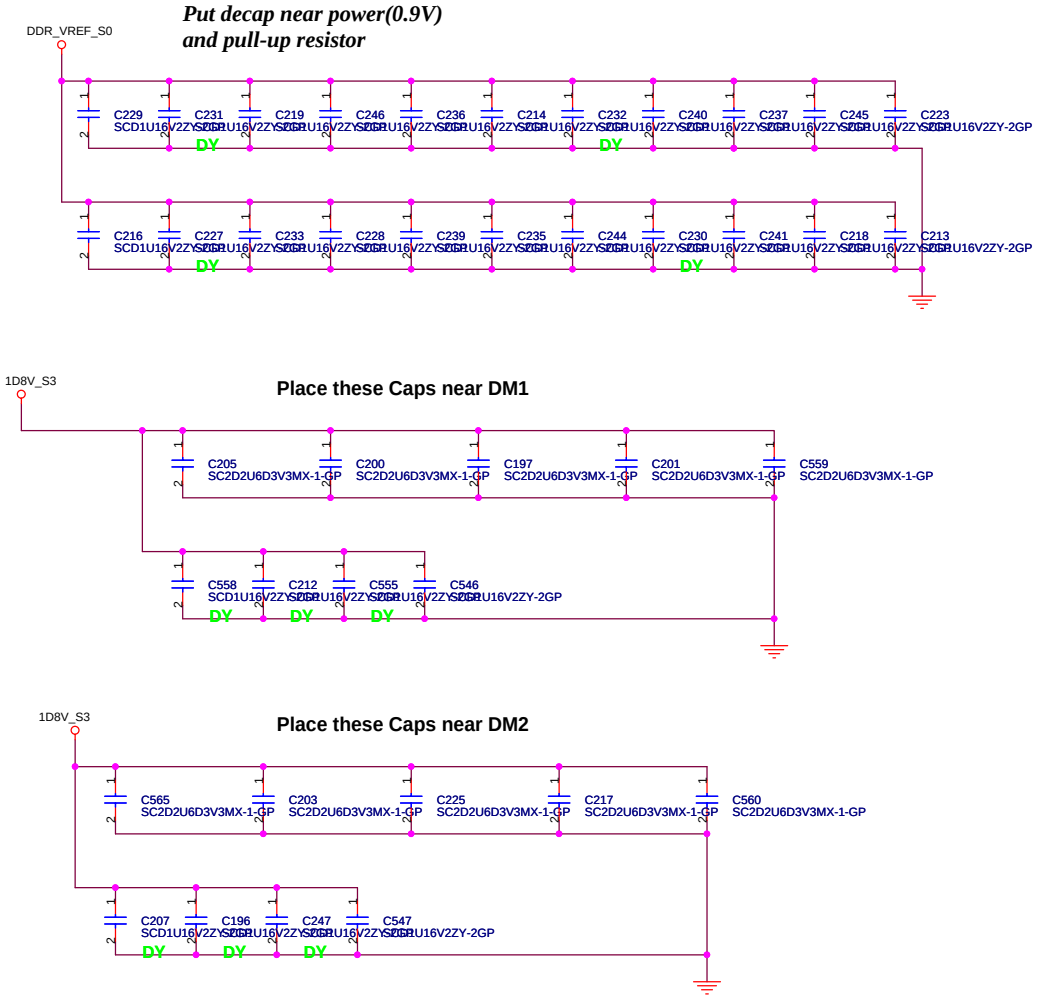
Title		
GMCH (5 of 5)		
Size: A3	Document Number: AG1	Rev: -1
Date: Monday, January 09, 2006	Sheet 10 of 45	



PARALLEL TERMINATION



Decoupling Capacitor



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR2 Termination Resistor***

Size	Document Number	Rev
A3	AG1	-1

Date: Wednesday, January 18, 2006 Sheet 12 of 45

LAUNCH BD CONN

Launch
12 1

LAUNCH1
ACES-CON12-GP
20.K0174.012

2nd source: 20.K0185.012

CCD Pin	
Pin	Symbol
1	5V
2	USB-
3	USB+
4	GND
5	GND

Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	PWM
4	BLON
5	GND
6	GND

Launch BD	
Pin	Symbol
1	3V_S0
2	PWRBTN#
3	PROGRAM#
4	EBUTTON#
5	INTERNET#
6	MAIL#
7	NC
8	MAIL_LED#
9	PWR_B_LED#
10	NC
11	INT_MICP
12	INT_MICN

Layout 40 mil
Layout 40 mil
Layout 60 mil

on Front Panel
on Front Panel
on Front Panel
on Front Panel
on Front Panel

Charger:
OFF : Battery or DC only
Orange : Charging
Orange Blink : Battery low

Power:
Green : S0
Orange : S3
Orange Blinking : Enter S4

2nd source: 20.K0228.008

Edge Trigger

LCD/INVERTER/CCD CONN

LCD1
IPEX-CON40-2-GP
20.F0763.040

EVEN CHANNEL
ODD CHANNEL

TOP VIEW
LCD
1 40

LED BD CONN

LEDB1
MLX-CON8-7-GP-U
CONNECTOR
20.K0185.008

Front panel

LED	V	V	V	V
Button	V	V		

BlutTooth Wireless Charger Power2

<Variant Name>

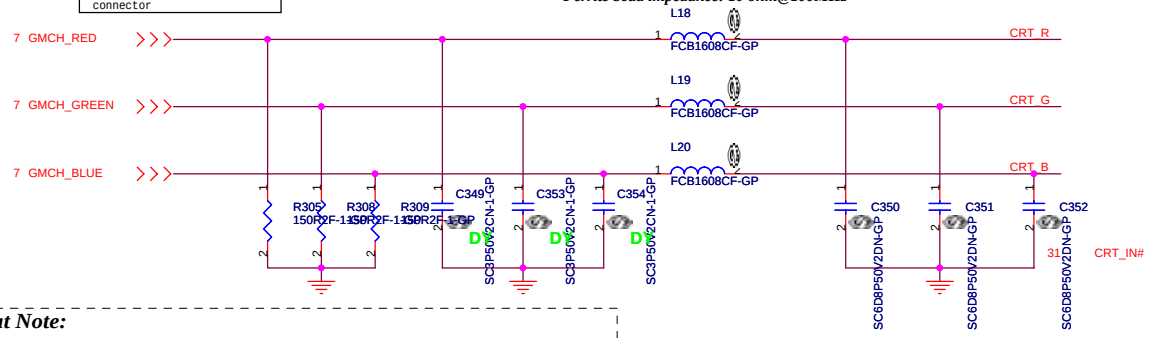
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD / LAUNCH / LEDs
Size: Custom | Document Number: AG1 | Rev: -1
Date: Wednesday, January 18, 2006 | Sheet 13 of 45

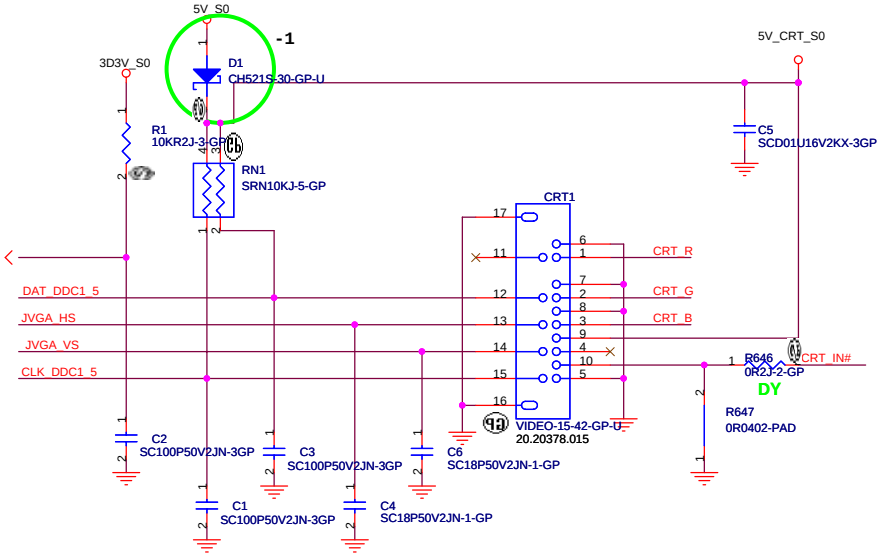
CRT I/F & CONNECTOR

Layout Note:
Place these resistors close to the CRT-out connector

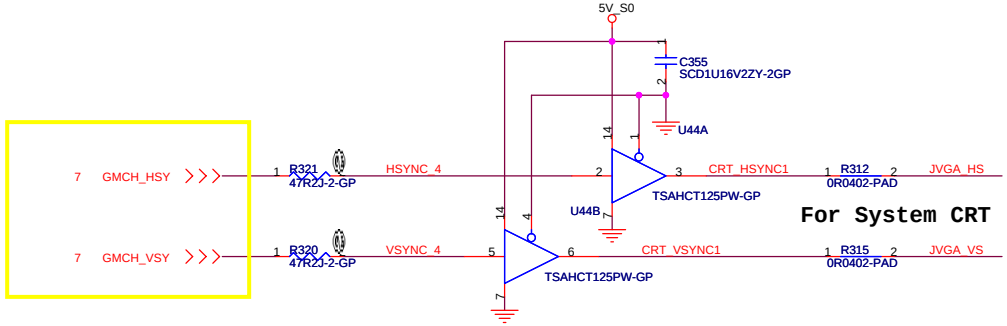
Ferrite bead impedance: 10 ohm@100MHz



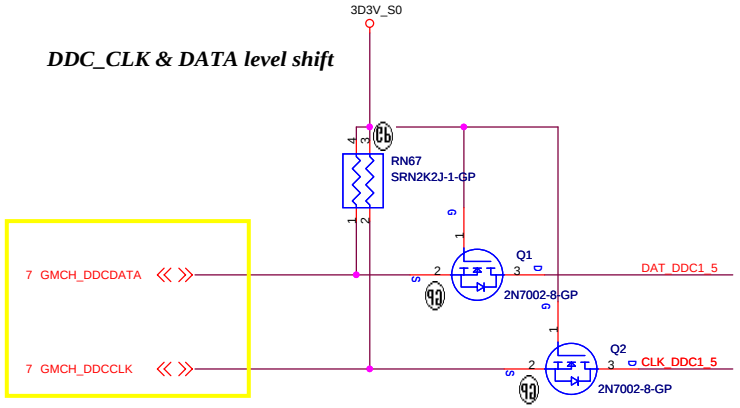
Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



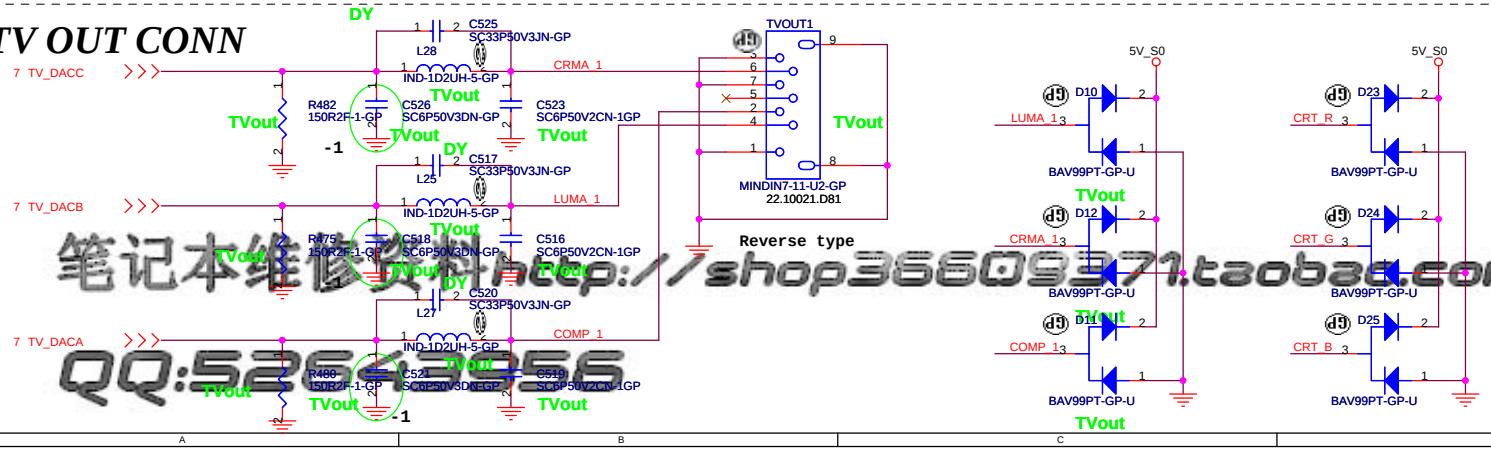
Hsync & Vsync level shift



DDC_CLK & DATA level shift



TV OUT CONN



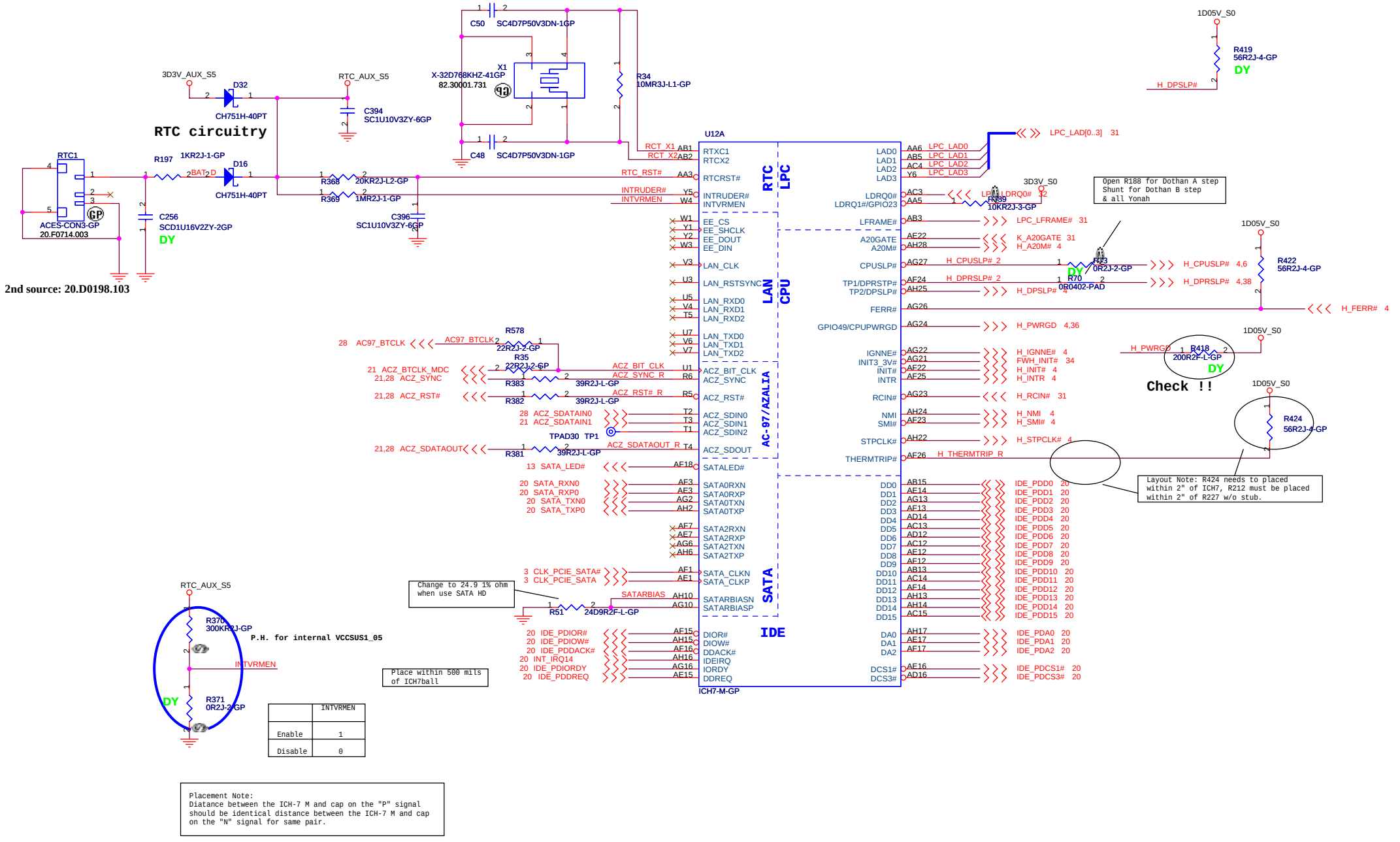
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT/TV Connector

Size	Document Number	Rev
A3	AG1	-1

Date: Friday, February 24, 2006 Sheet 14 of 45



	INTVRMEN
Enable	1
Disable	0

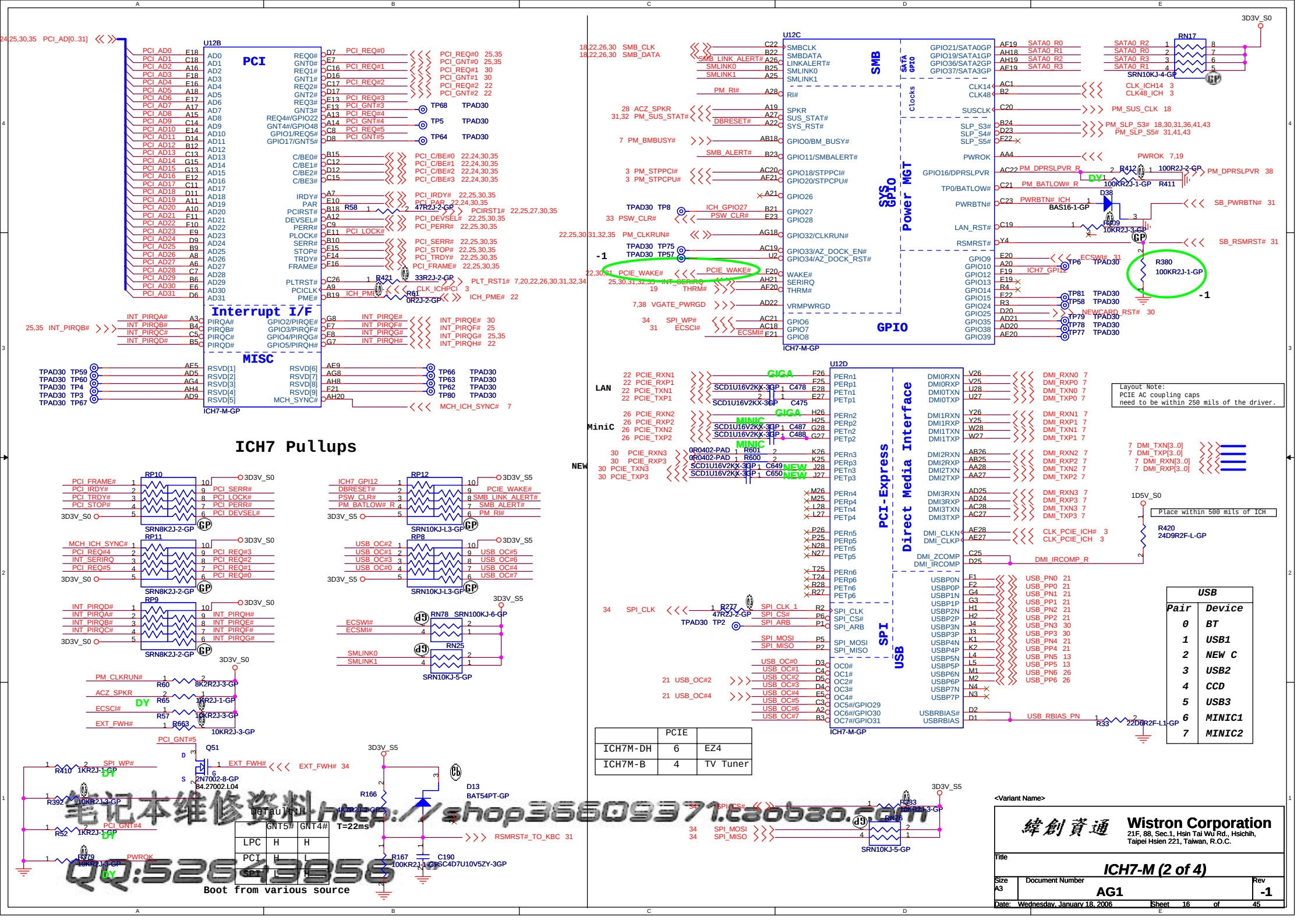
<Variant Name>

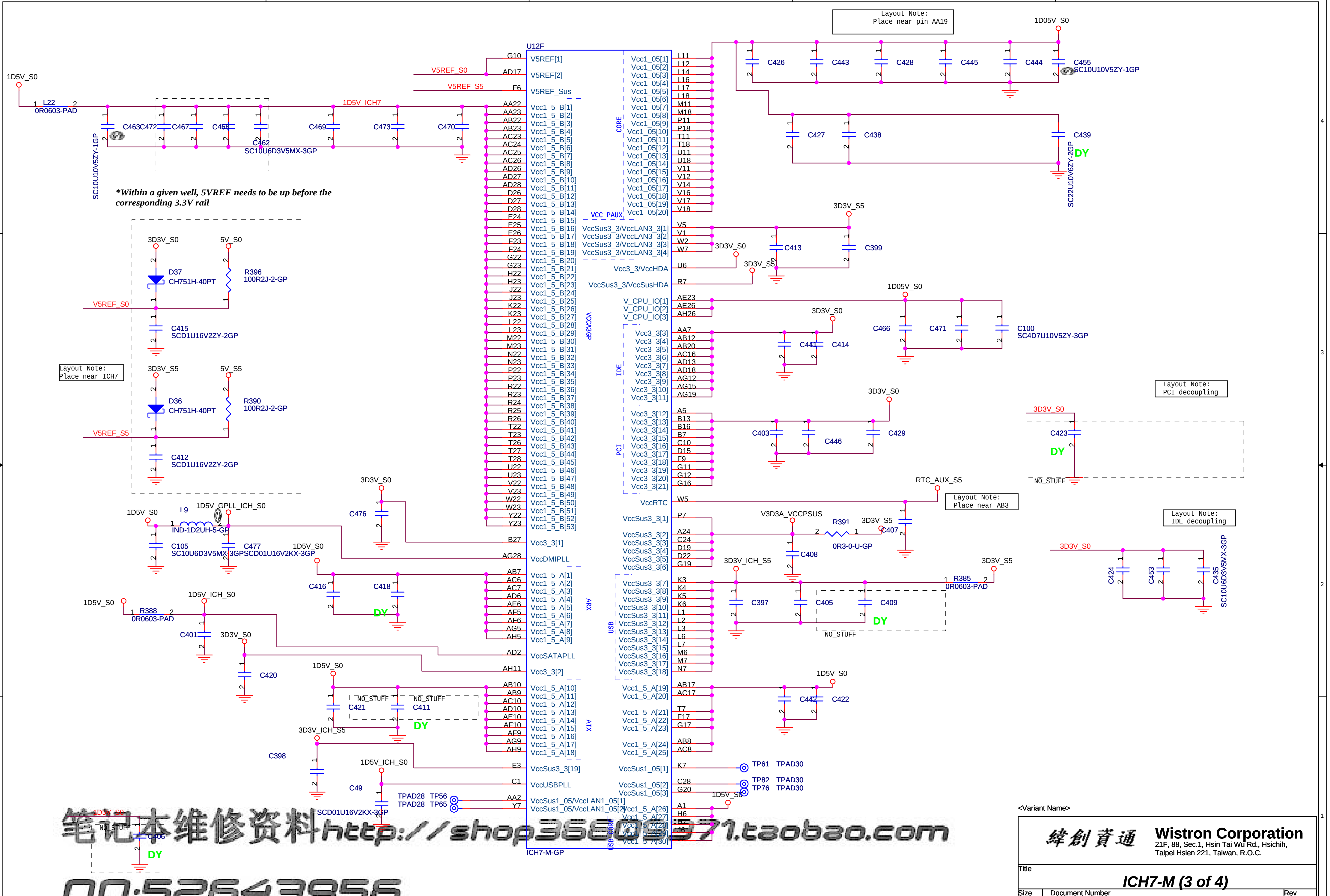
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***ICH7-M (1 of 4)***

Size	Document Number	Rev
A3	AG1	-1

Date: Wednesday, January 18, 2006 Sheet 15 of 45



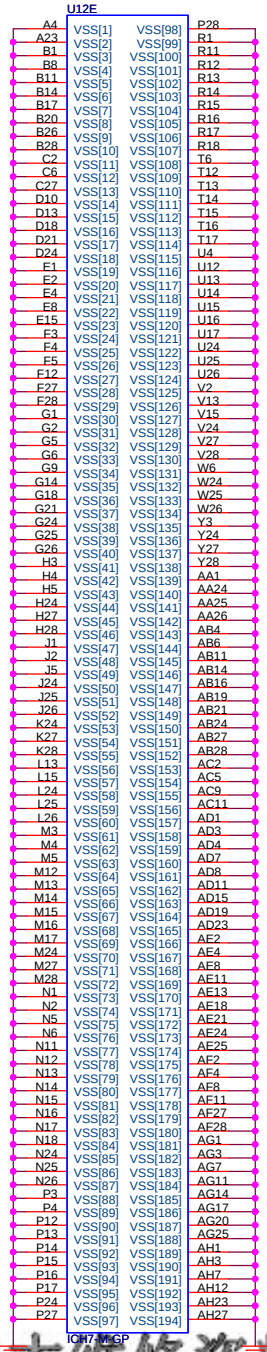


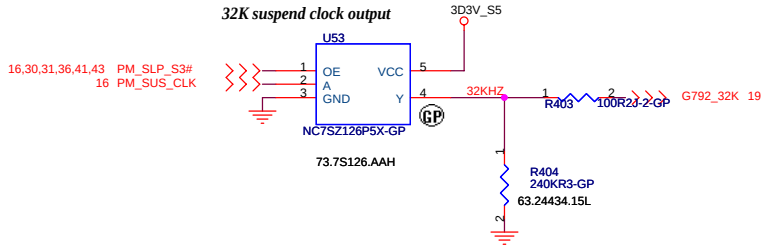
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

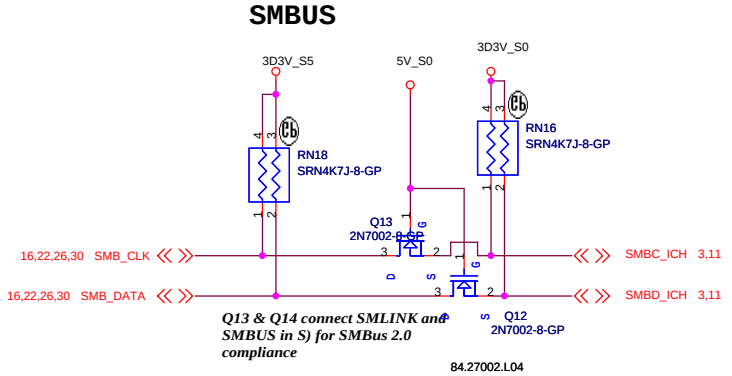
Title: **ICH7-M (3 of 4)**

Size	Document Number	Rev
A3	AG1	-1

Date: Monday, January 09, 2006 Sheet 17 of 45







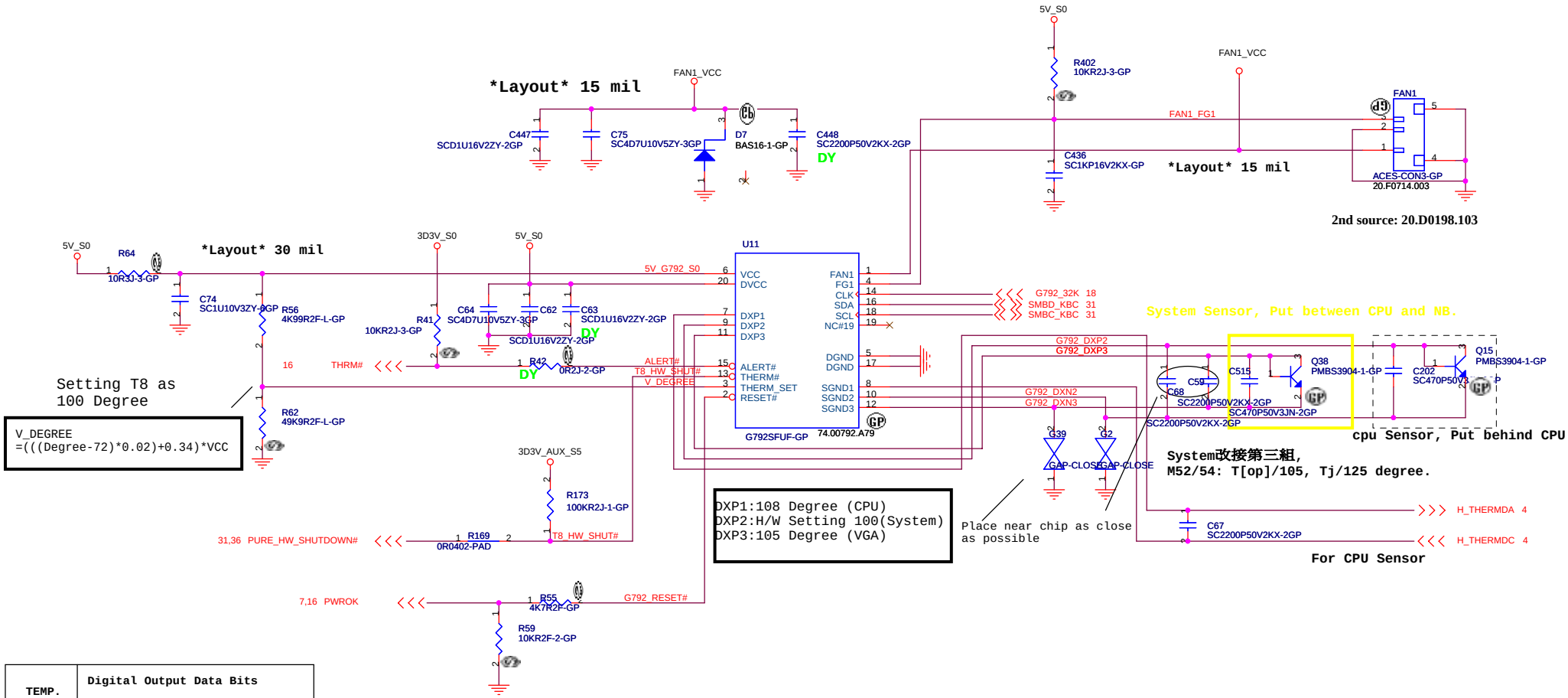
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH7-M (4 of 4)/ODD

Size: A3 | Document Number: AG1 | Rev: -1

Date: Wednesday, January 18, 2006 | Sheet 18 of 45



TEMP.	Digital Output Data Bits			
	Sign	MSB	LSB	EXT
+127.875	0	111	1111	111
+126.375	0	111	1110	011
+25.5	0	001	1001	100
+1.75	0	000	0001	110
+0.5	0	000	0000	100
+0.125	0	000	0000	001
-0.125	1	111	1111	111
-1.125	1	111	1110	111
-25.5	1	110	0110	100
-55.25	1	100	1000	110
-65.000	1	011	1111	000

<Variant Name>

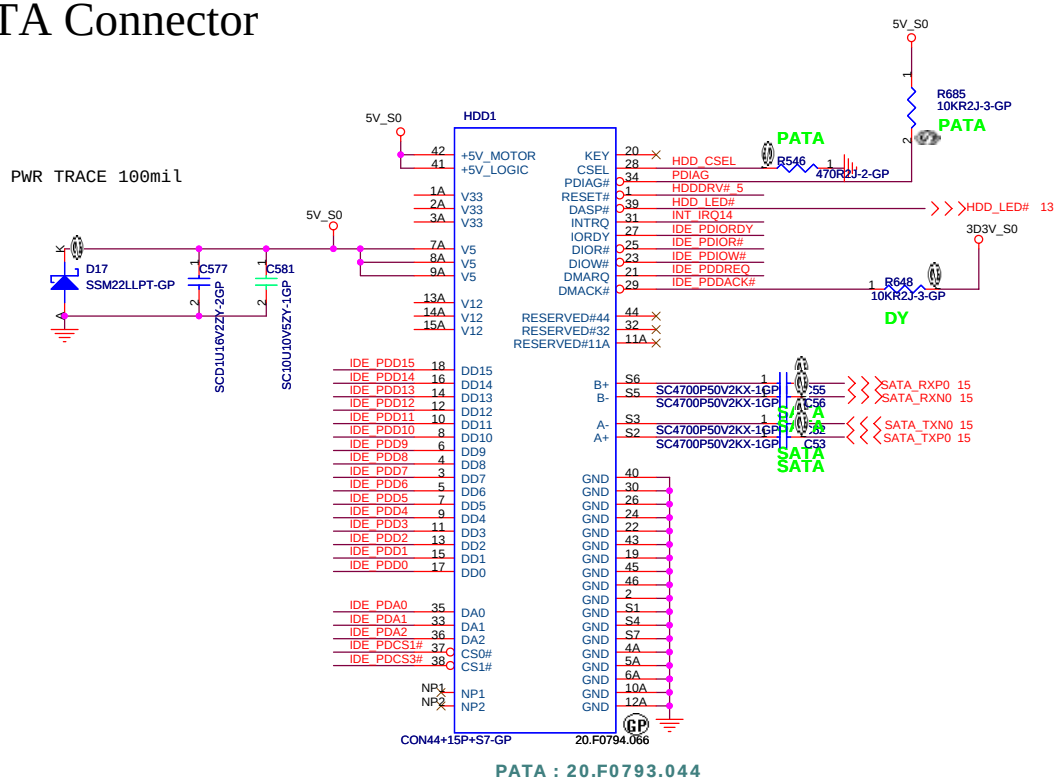
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor G792

Size: Custom | Document Number: AG1 | Rev: -1

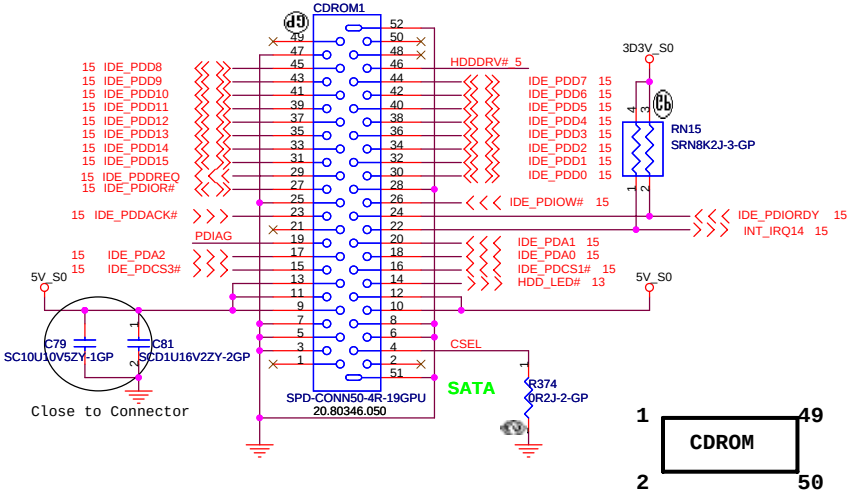
Date: Wednesday, January 18, 2006 | Sheet 19 of 45

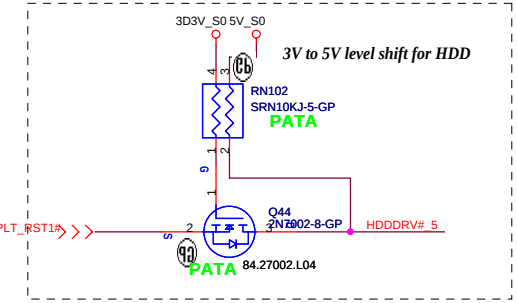
SATA Connector



PATA : 20.F0793.044

CDROM Connector





<Variant Name>

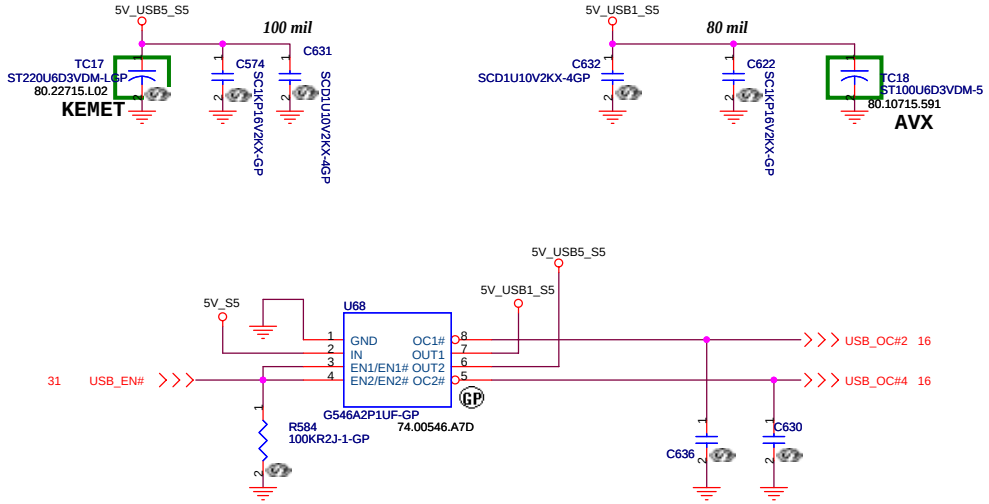
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

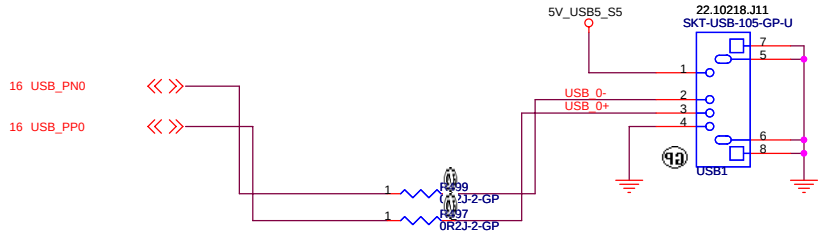
Title: **SATA/PATA HDD ULi-M5285**

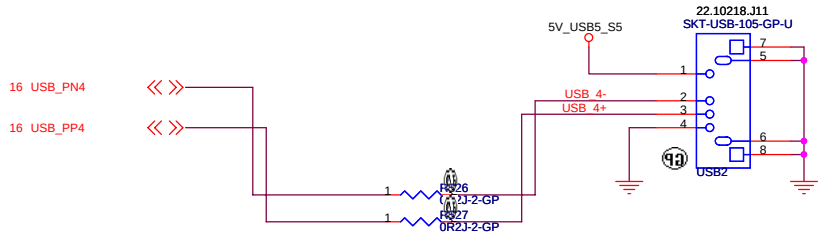
Size	Document Number	Rev
A3	AG1	-1

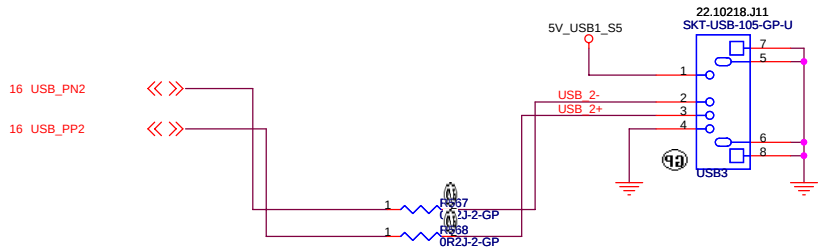
Date: Wednesday, January 18, 2006 Sheet 20 of 45

USB PORT

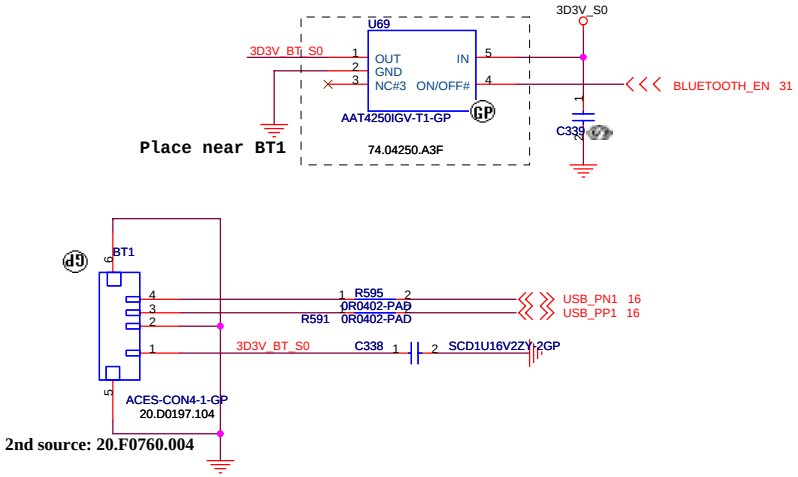




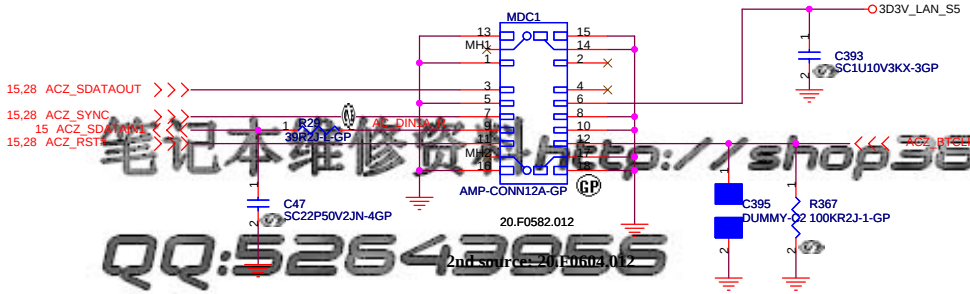




BLUETOOTH MODULE CONNECTOR



MDC 1.5 CONN



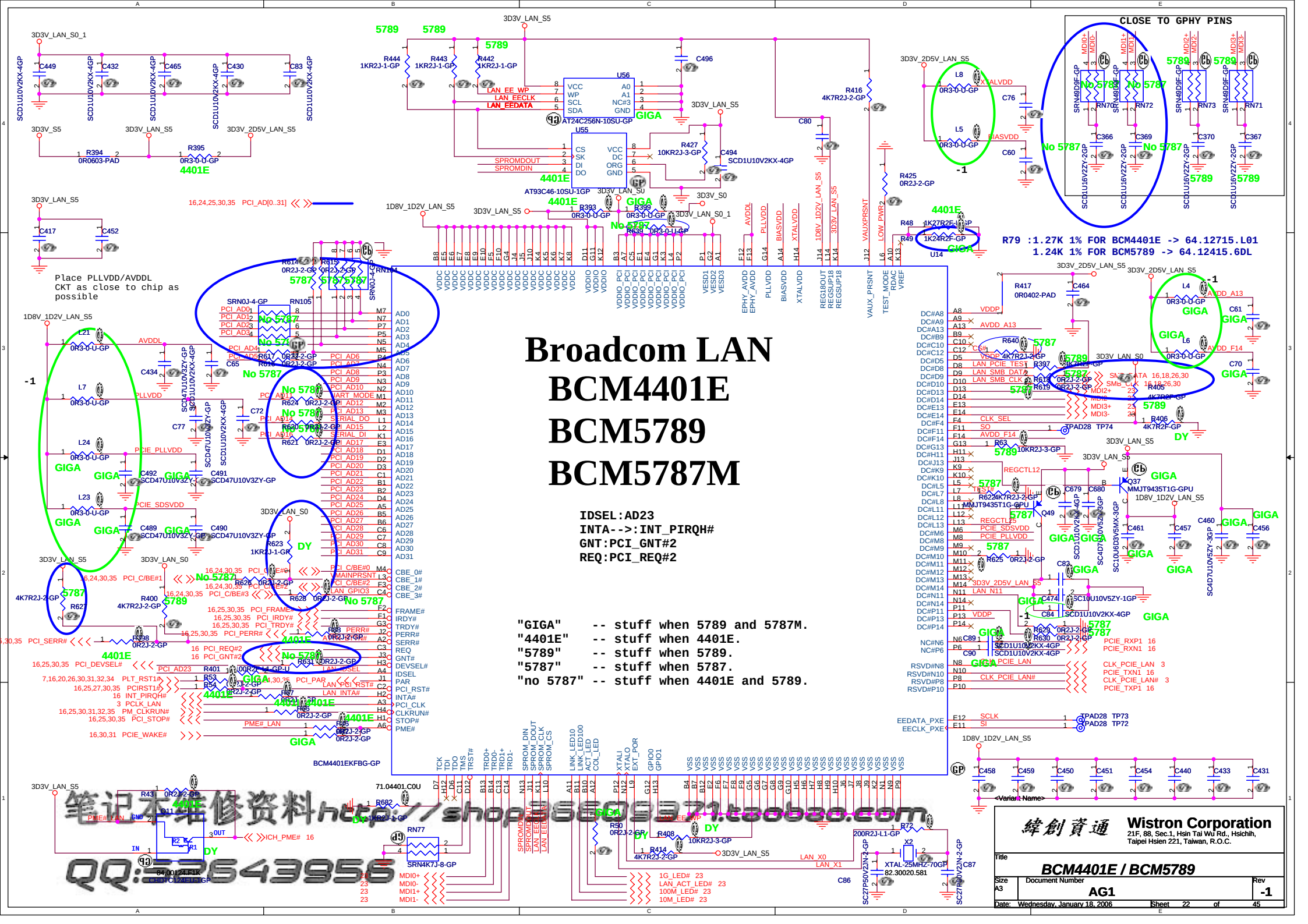
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB and MDC I/F

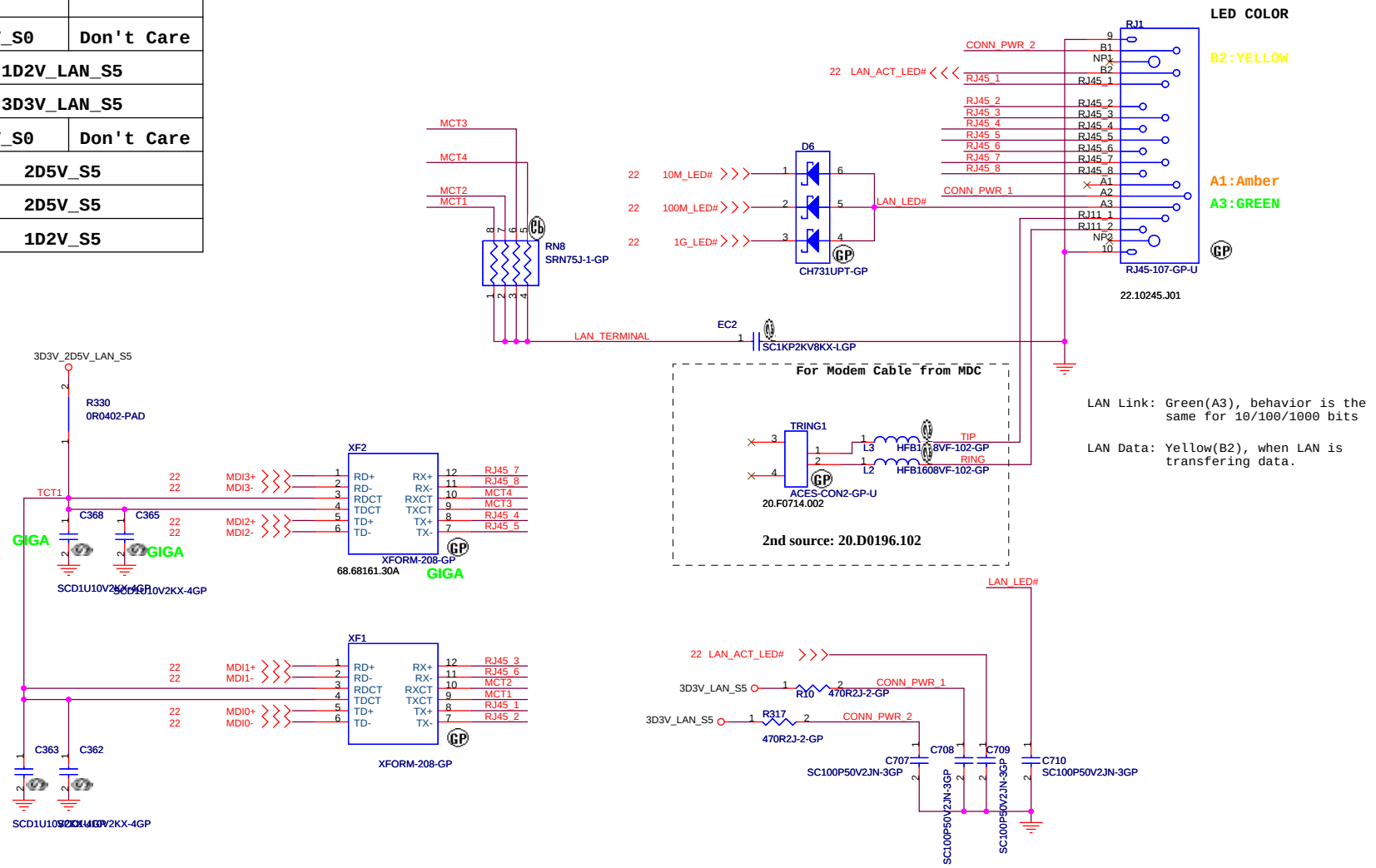
Size	Document Number	Rev
A3	AG1	-1

Date: Friday, February 24, 2006 Sheet 21 of 45



LAN Connector

Voltage Rail	4401E	5789	5787
VDDIO_PCI	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDC	1D8V_LAN_S5	1D2V_LAN_S5	
VDDIO	3D3V_LAN_S5	3D3V_LAN_S5	
VESD	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDP	Don't Care	2D5V_S5	
3D3V_2D5V_S5	3D3V_S5	2D5V_S5	
1D8V_1D2V_S5	1D8V_LAN_S5	1D2V_S5	



1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

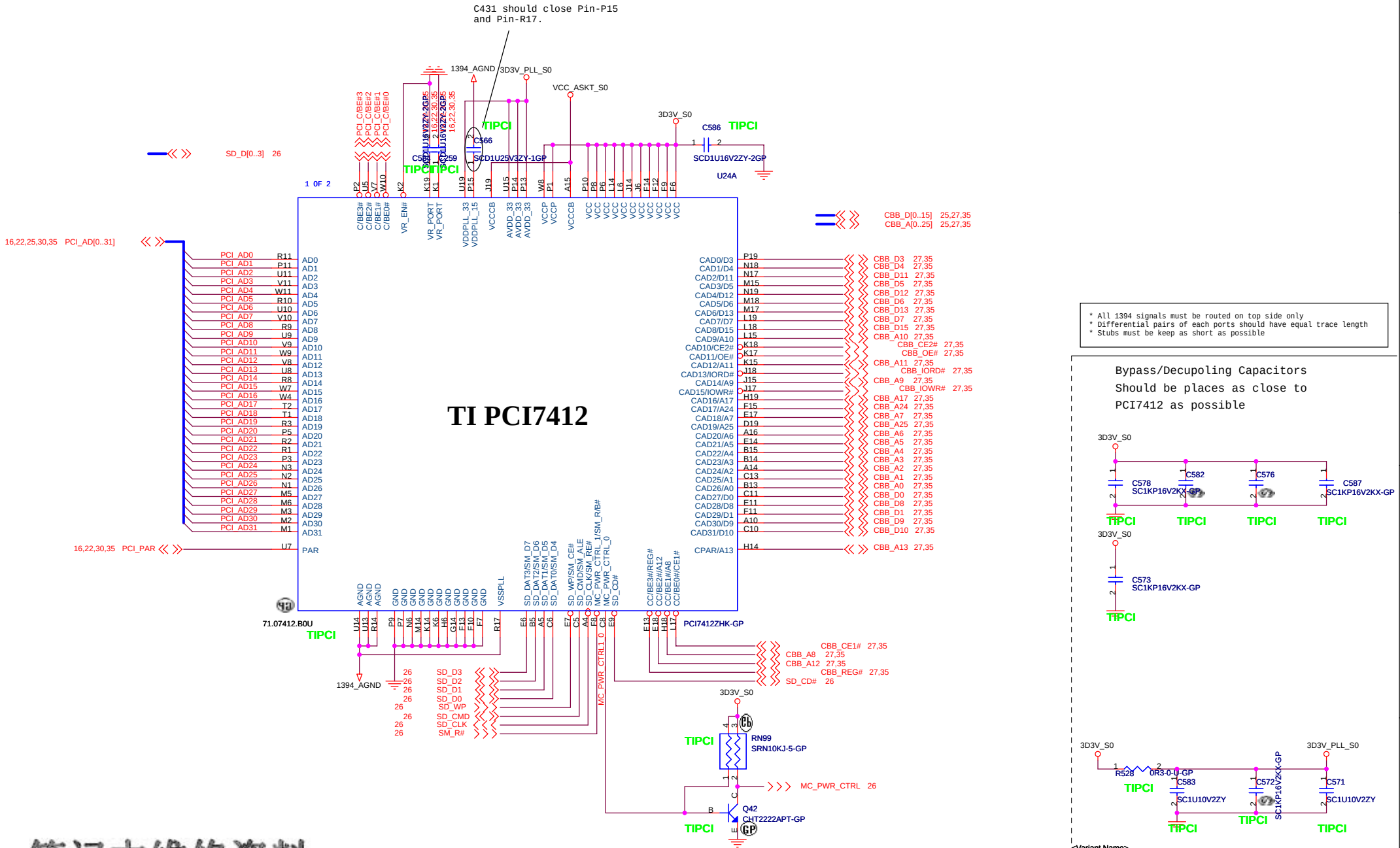
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN Connector**

Size	Document Number	Rev
A3	AG1	-1

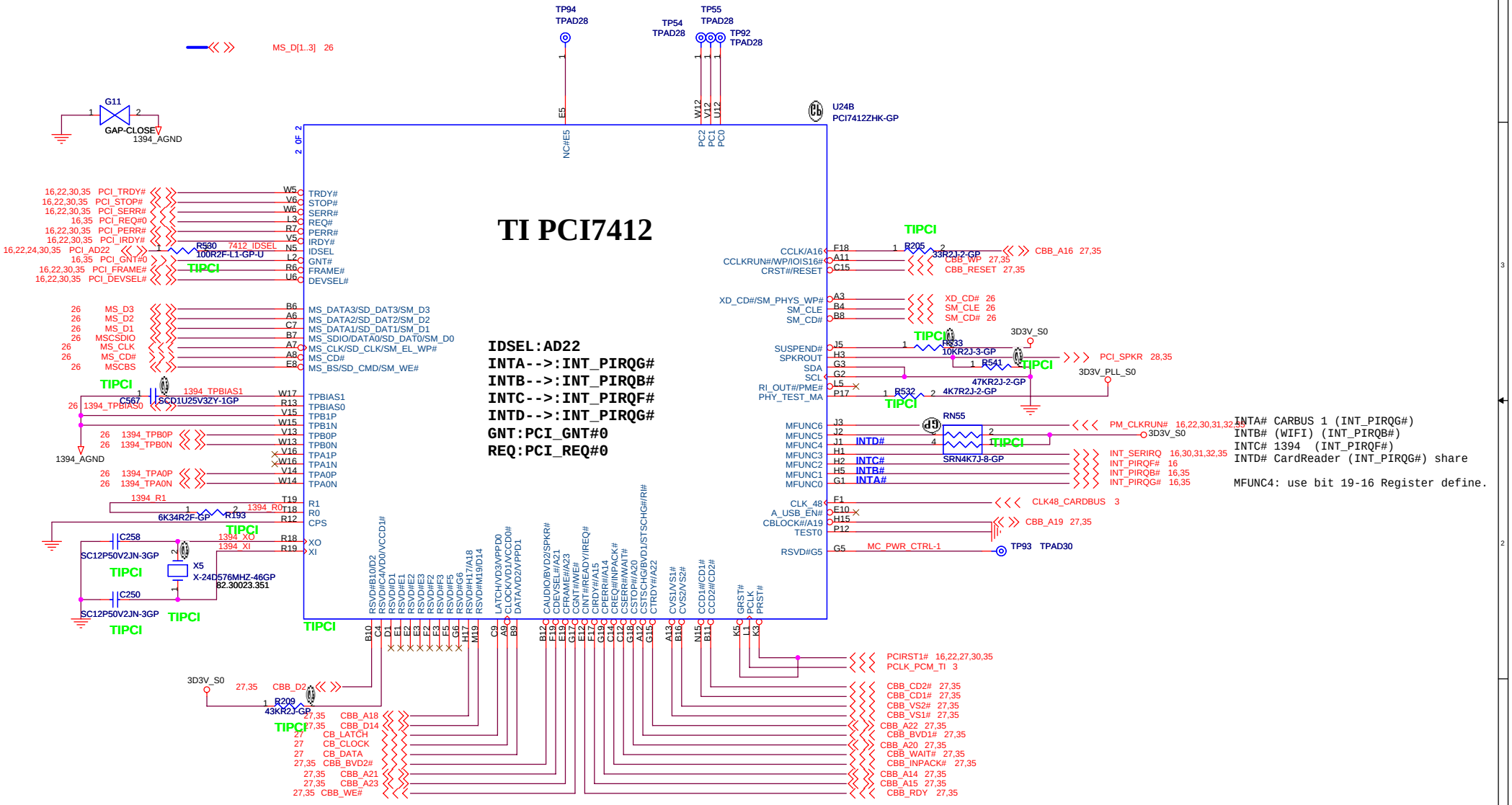
Date: Wednesday, January 18, 2006 Sheet 23 of 45



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

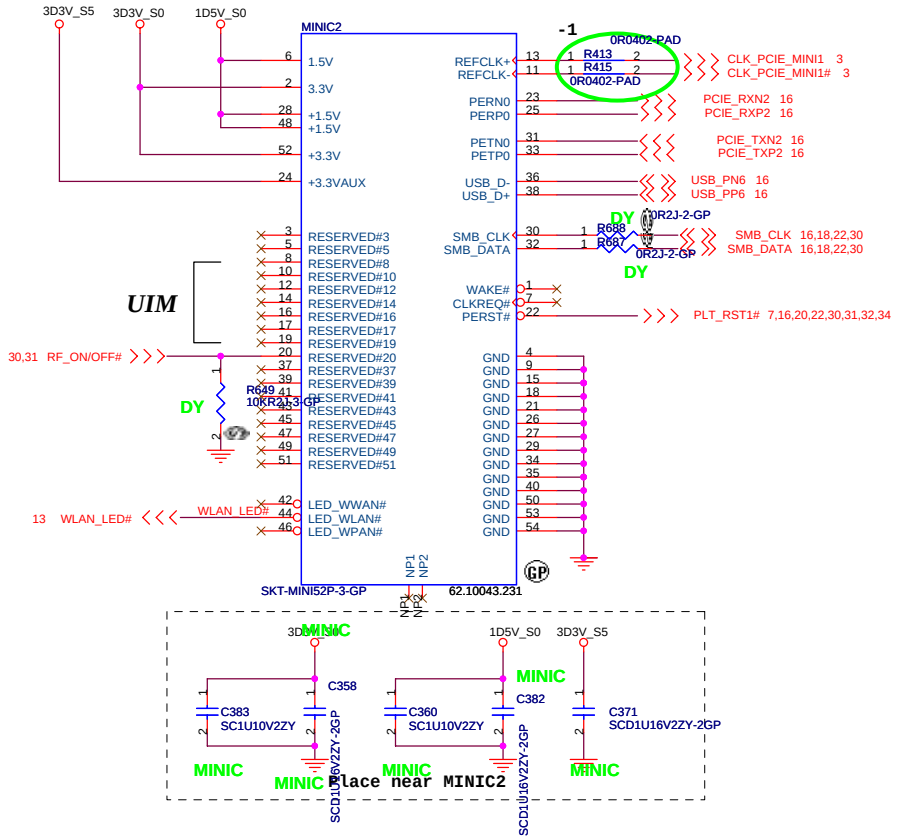
Title	TI PCI7412 (1 of 2)	
Size A3	Document Number AG1	Rev -1
Date: Wednesday, January 18, 2006	Sheet 24 of 45	



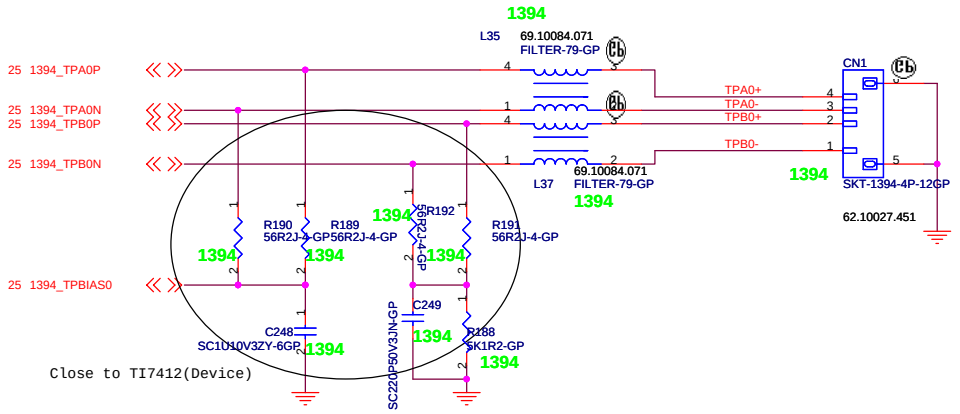
<Variant Name>

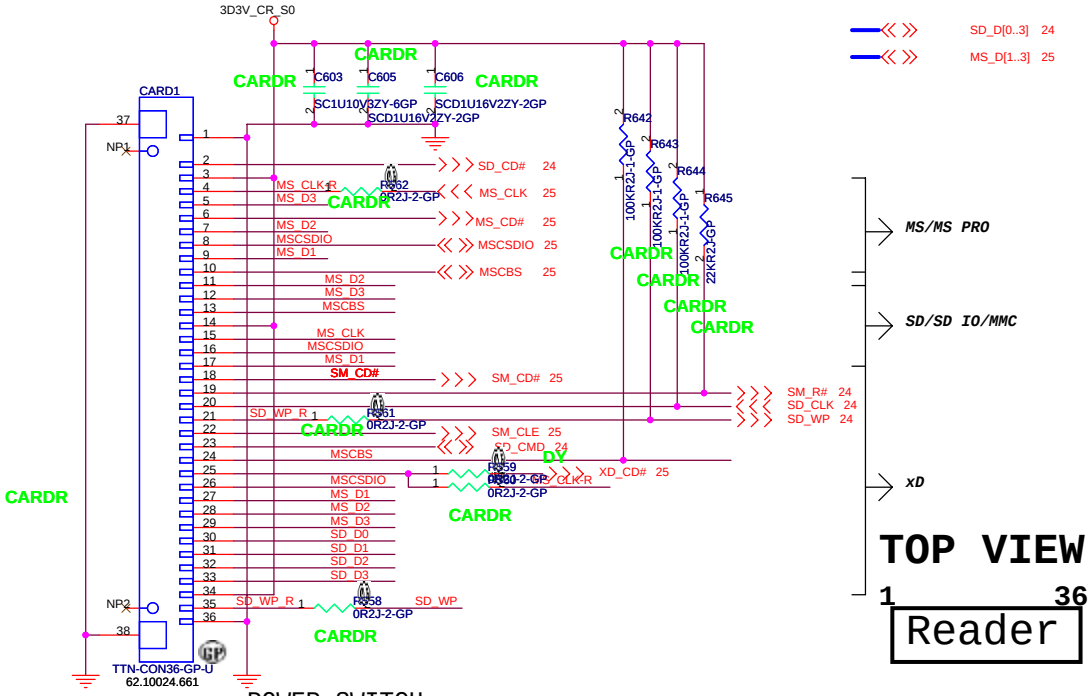
Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	TI PCI7412 (2 of 2)
Size A3	Document Number AG1
Rev	-1
Date: Wednesday, January 18, 2006	Sheet 25 of 45

Mini Card Connector



1394 Connector





<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **MINI CARD / 1394**

Size	Document Number	Rev
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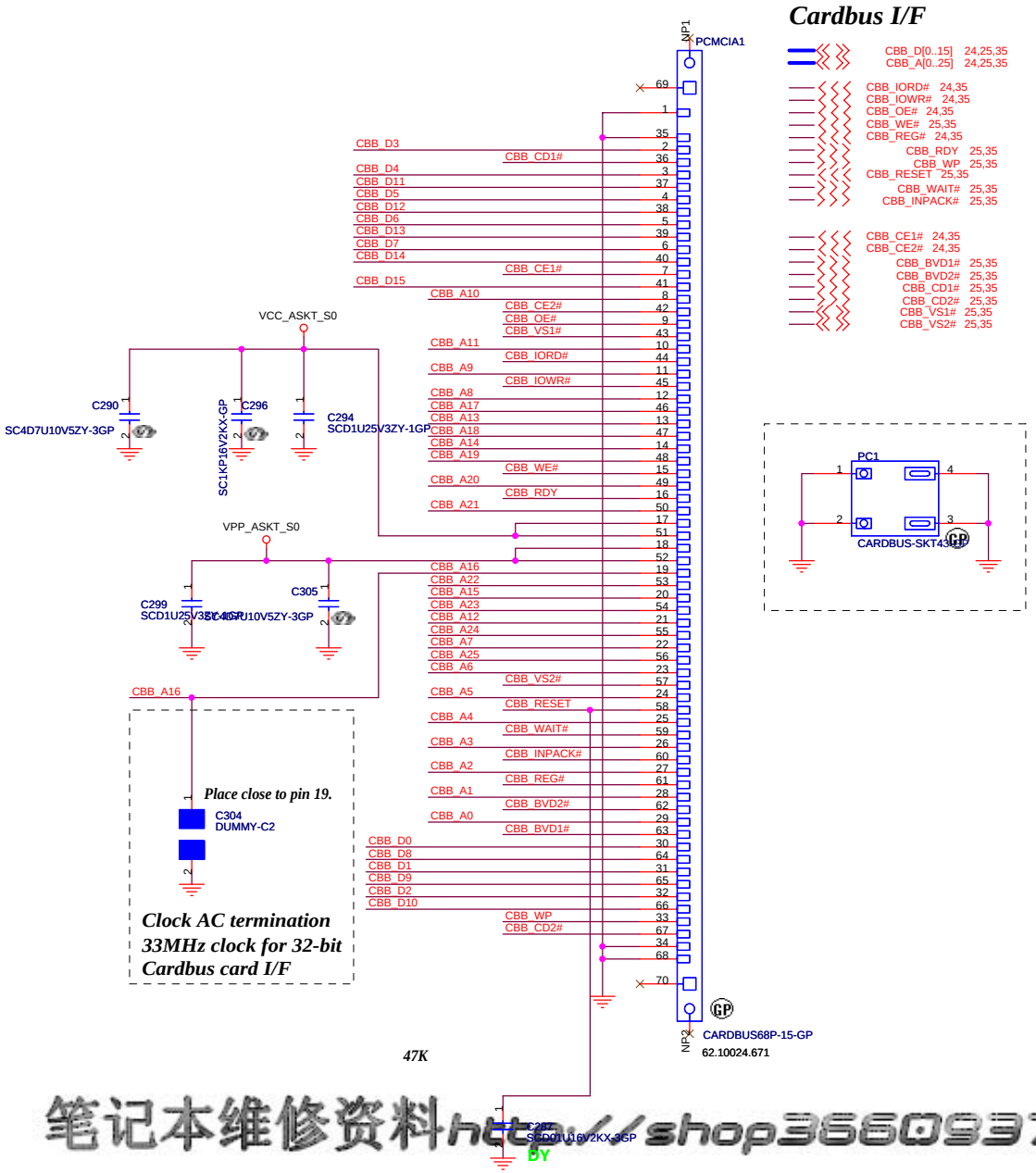
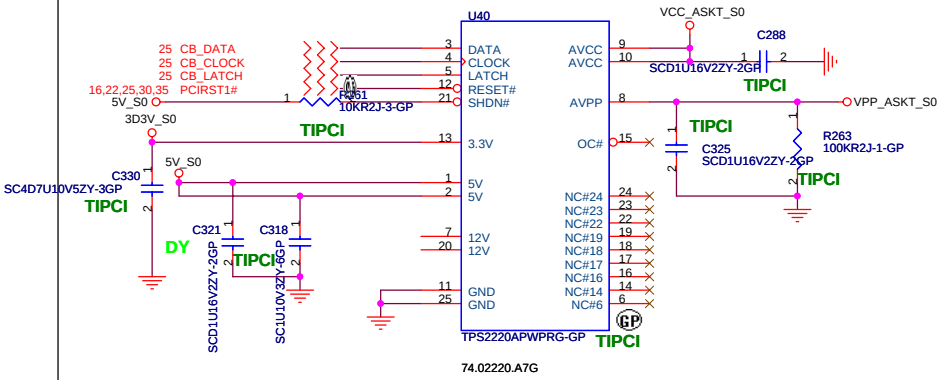
Date: Wednesday, March 01, 2006 Sheet 26 of 45

PCMCIA Socket

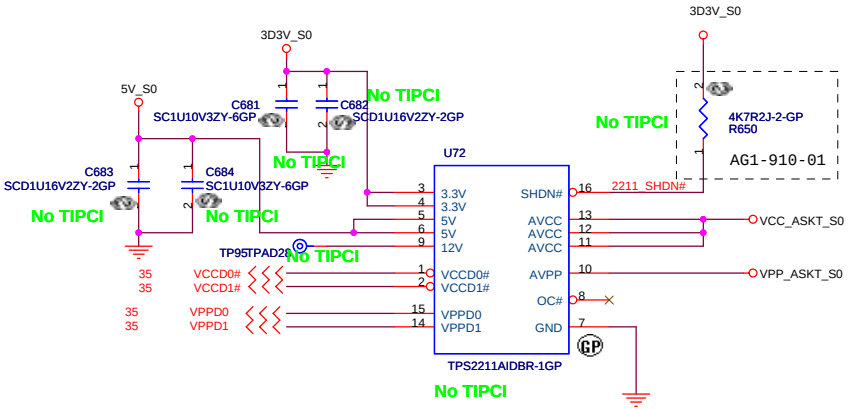


Cardbus I/F

TI Power switch



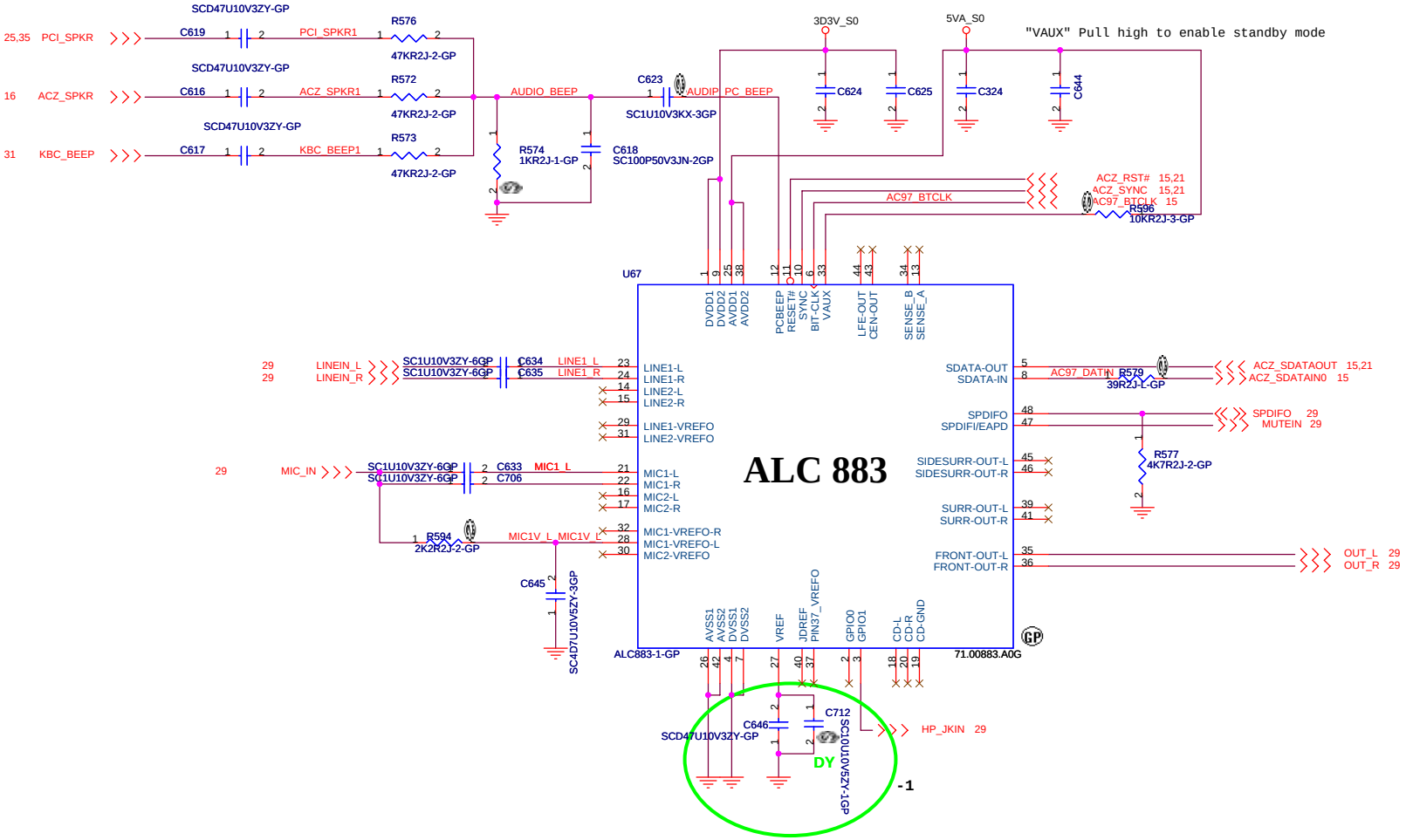
ENE Power switch



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

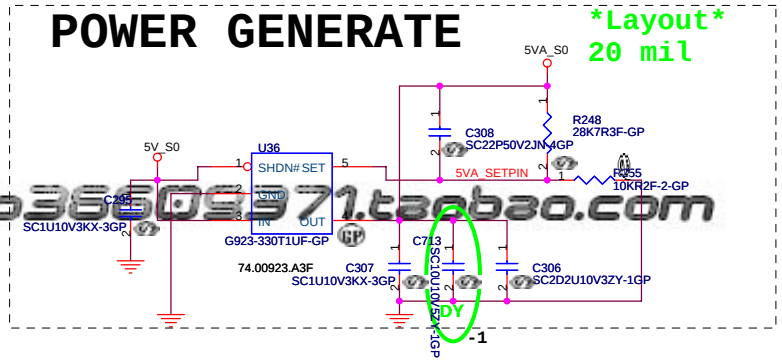
Title	PCMCIA	
Size A3	Document Number AG1	Rev -1
Date: Friday, February 24, 2006	Sheet 27 of 45	



1) When GPIO0 is assered, AMP should be muted.
2) SPDIFO should be turned off when not used.

Configuation:
(3 External Jacks, 1 internal Mic, 1 stereo output Speaker Amp.

Pin	Symbol	Location	Re-tasking
35/36	FRONT	AMP,Jack1	AMP output, line input
39/41	SURR	X	X
43/44	CEN/LEFT	X	SURR-VREFO-L/R
45/46	SIDESURR	X	SIDESURR-L is MIC2-VREFO-R, SIDESURR-R is LINE2-VREFO-R
23/24	LINE1	Jack 2	Line input, line output
21/22	MIC1	Jack 3	Mic input, line output
14/15	LINE2	X	X
16/17	MIC2	Int. Mic	Mic input



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Azalia codec ALC883**

Size	Document Number	Rev
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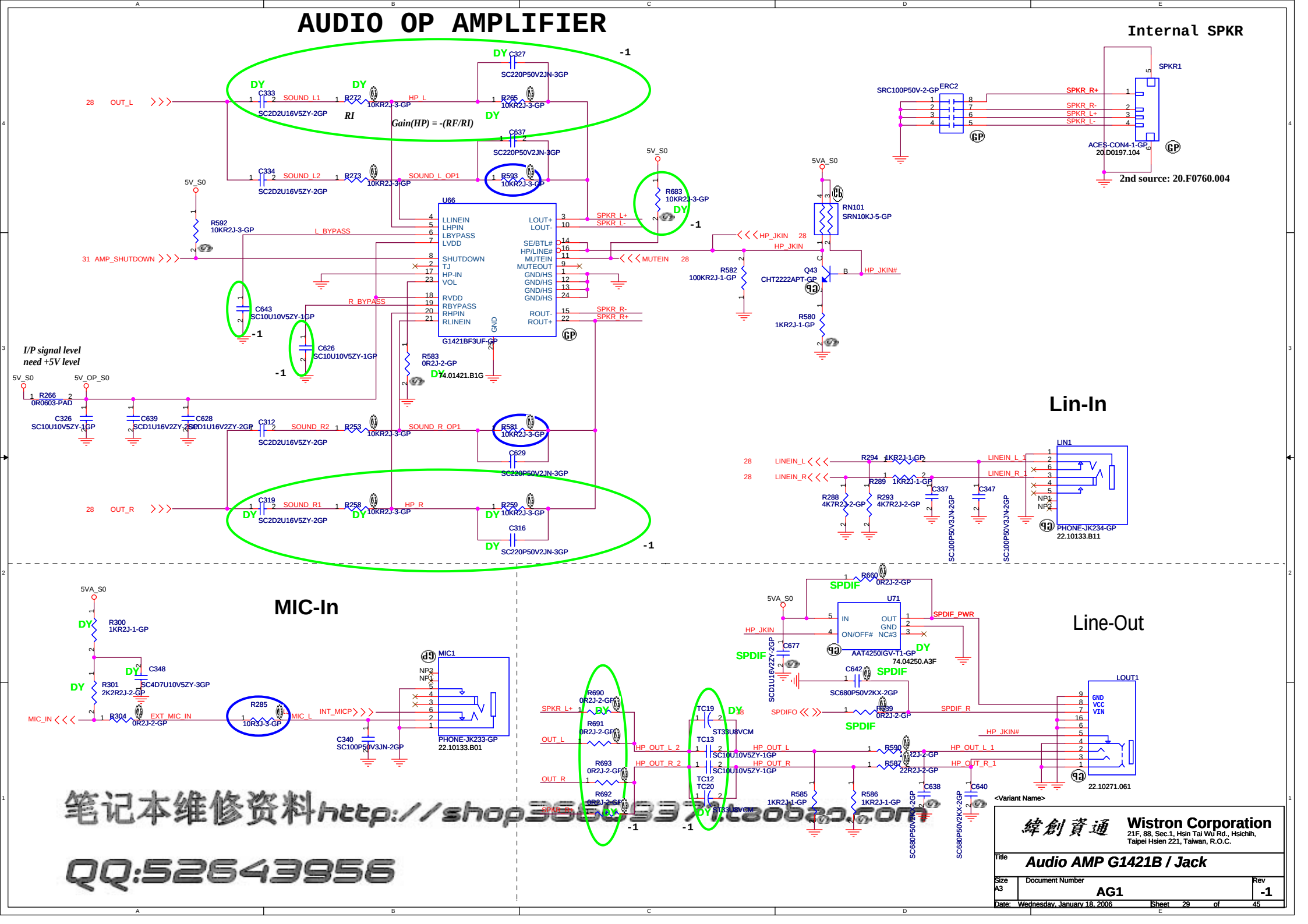
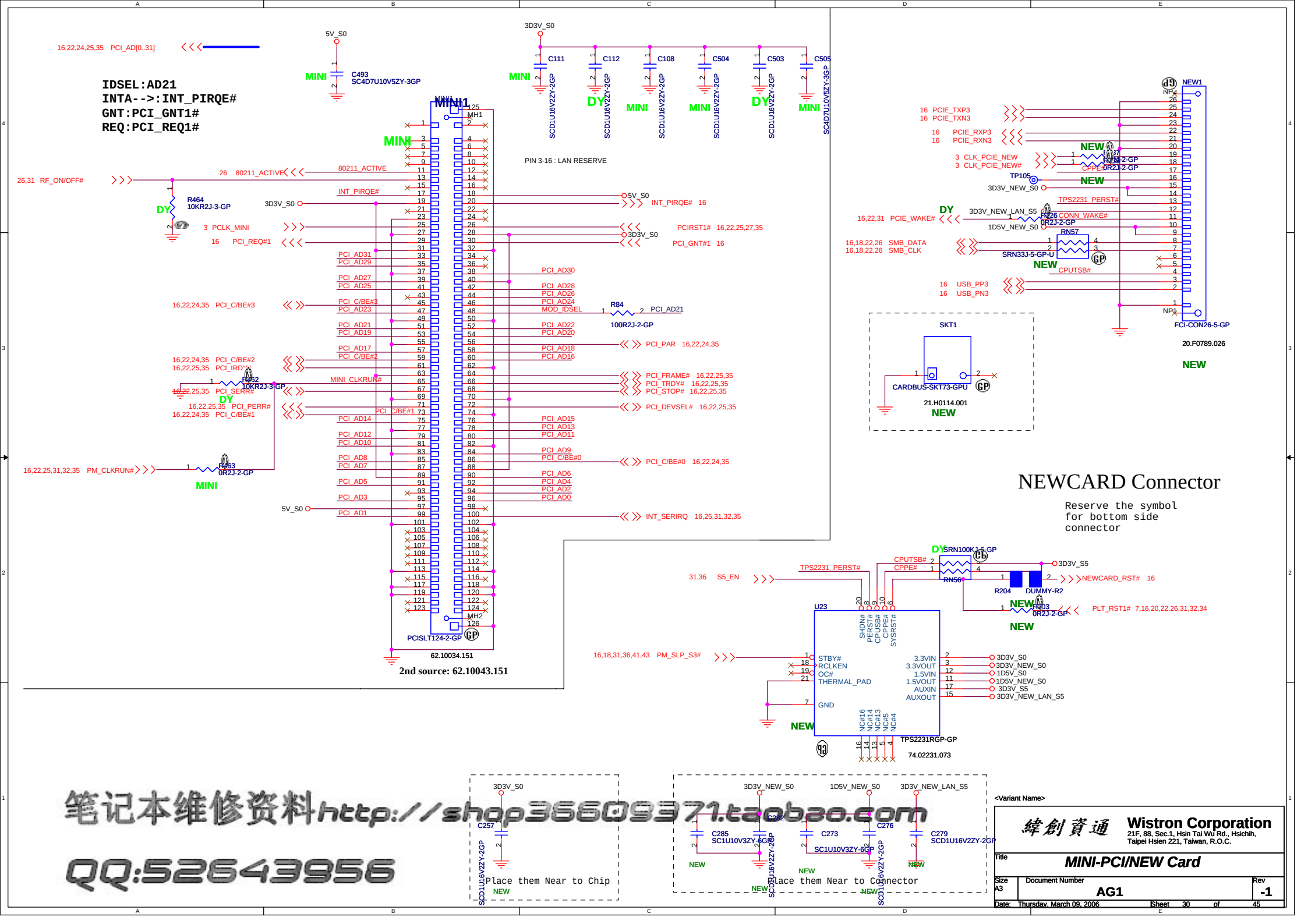
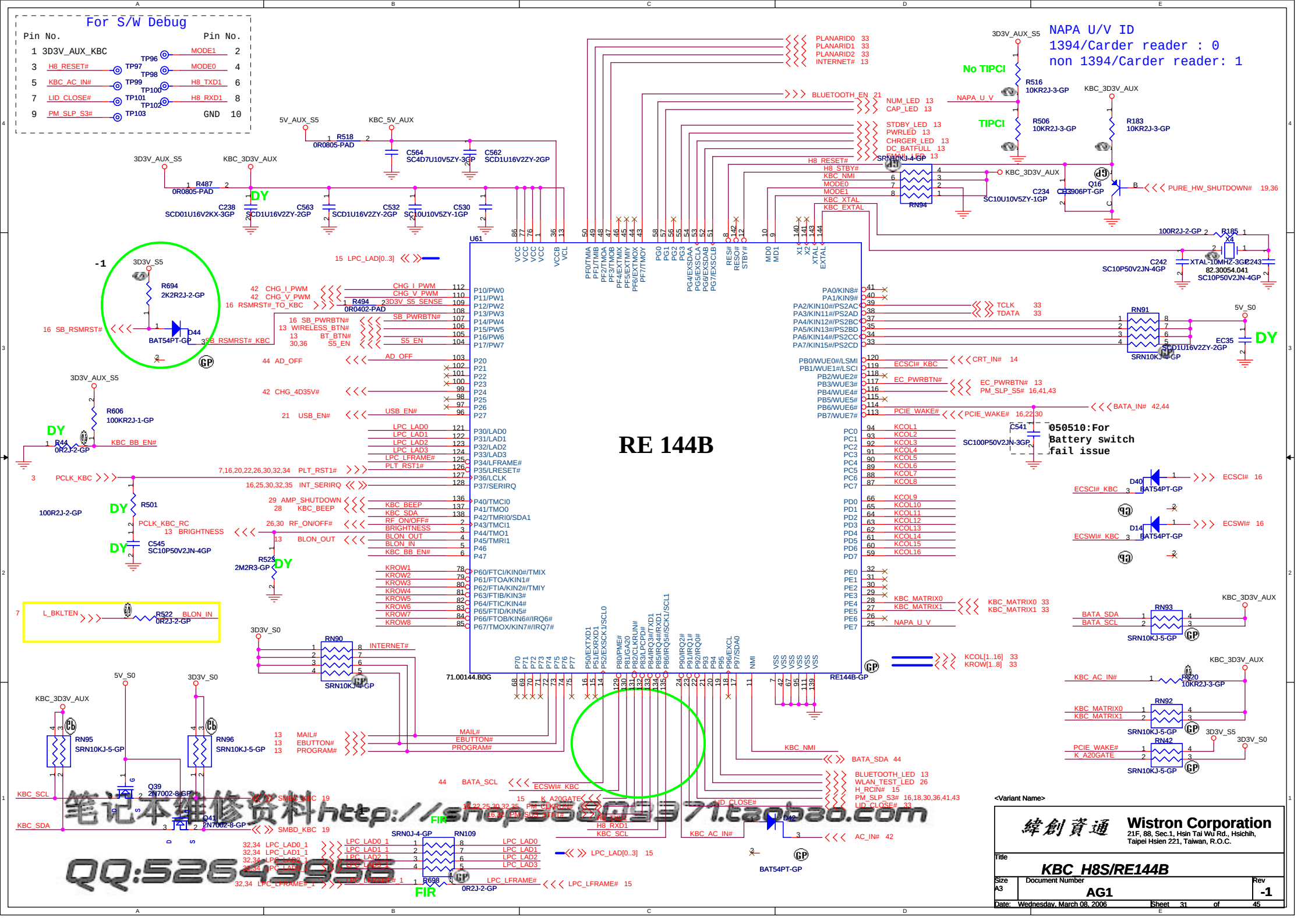
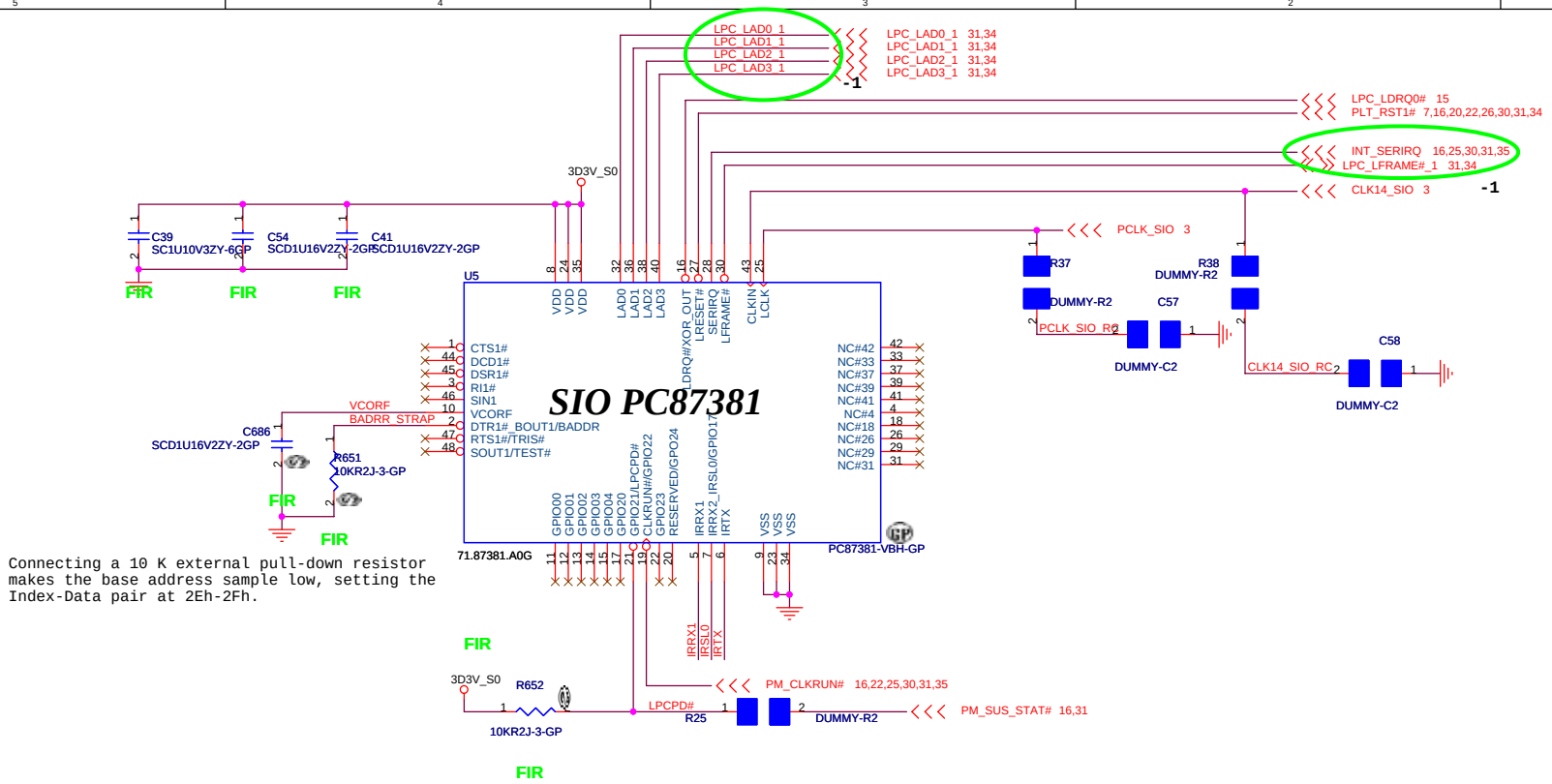
AUDIO OP AMPLIFIER



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Audio AMP G1421B / Jack***	
Size A3	Document Number **AG1**	Rev **-1**
Date: Wednesday, January 18, 2006	Sheet 29 of 45	



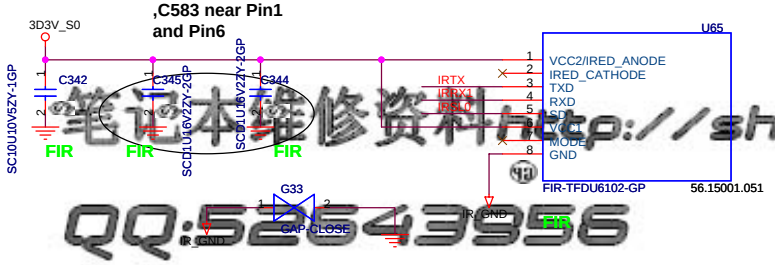

For S/W Debug
Pin No. Pin No.
1 3D3V_AUX_KBC MODE1 2
3 H8_RESET# MODE0 4
5 KBC_AC_IN# H8_TXD1 6
7 LID_CLOSE# H8_RXD1 8
9 PM_SLP_S3# GND 10
TP96 TP97 TP98 TP99 TP100 TP101 TP102 TP103
NAPA U/V ID
1394/Carder reader : 0
non 1394/Carder reader: 1
No TIPCI
TIPCI
RE 144B
71.00144.B0G
RE144B-GP
U61
050510:For
Battery switch
fail issue
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC_H8S/RE144B
AG1
-1
Wednesday, March 08, 2006
31
45
笔记本维修资料http://shop58095371.taobao.com
QQ:526499958



VISHAY FIR/CIR Module

Layout Guide:
(1) FIR_3D3V : 30 mils,
(2) C583, C581 close to U32

Place C581 ,C583 near Pin1 and Pin6



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***SIO 87392 / FIR***

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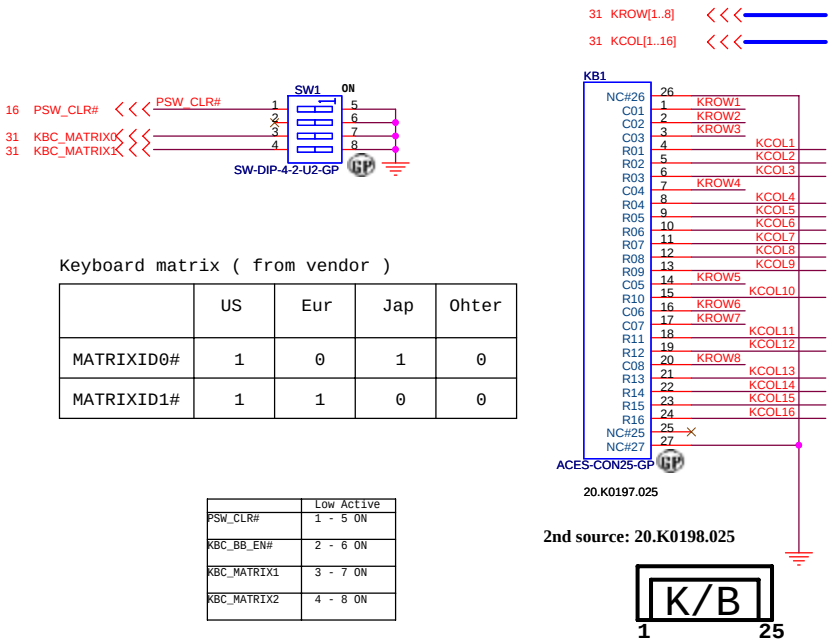
Internal KeyBoard Connector

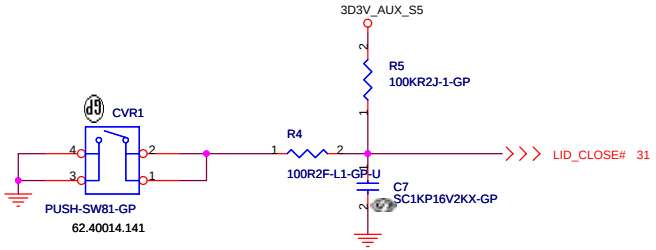


Keyboard matrix (from vendor)

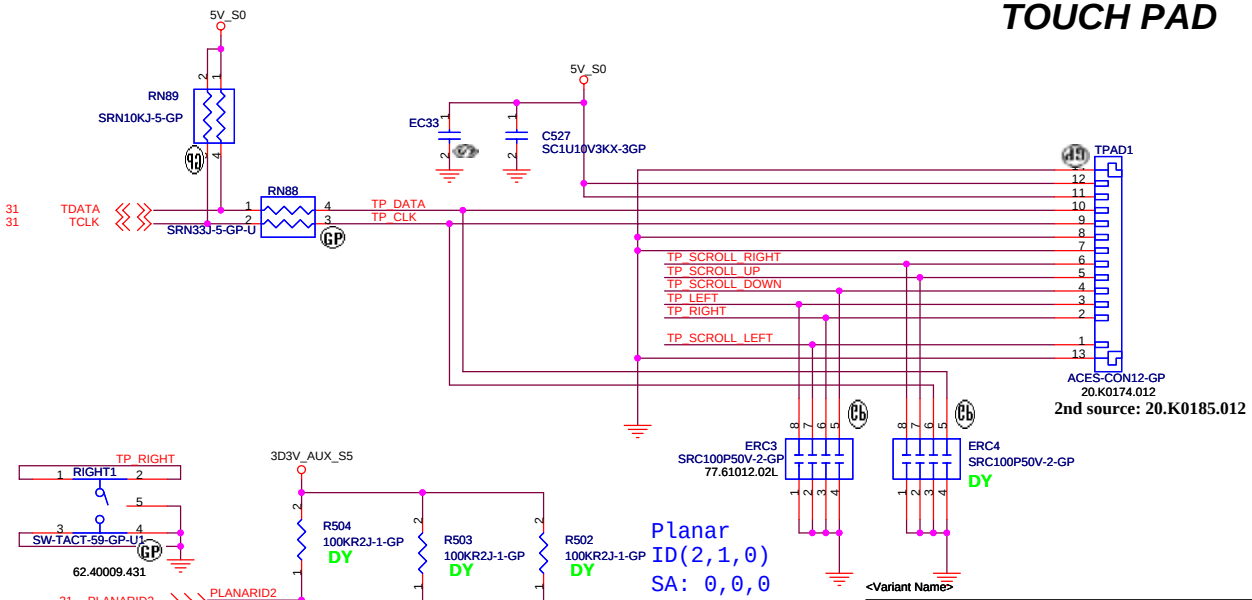
	US	Eur	Jap	Ohter
MATRIXID0#	1	0	1	0
MATRIXID1#	1	1	0	0

	Low Active
PSW_CLR#	1 - 5 ON
KBC_BB_EN#	2 - 6 ON
KBC_MATRIX1	3 - 7 ON
KBC_MATRIX2	4 - 8 ON

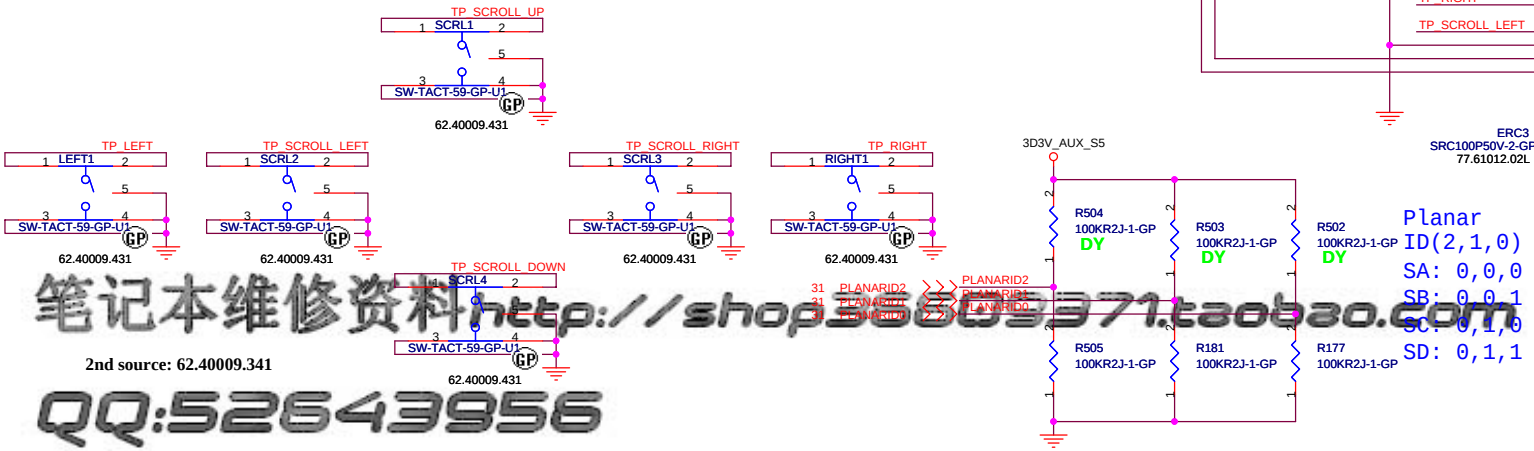
COVER SWITCH



TOUCH PAD



SCROLL KEY



<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: KEYBOARD/TOUCHPAD		
Size: A3	Document Number: AG1	Rev: -1
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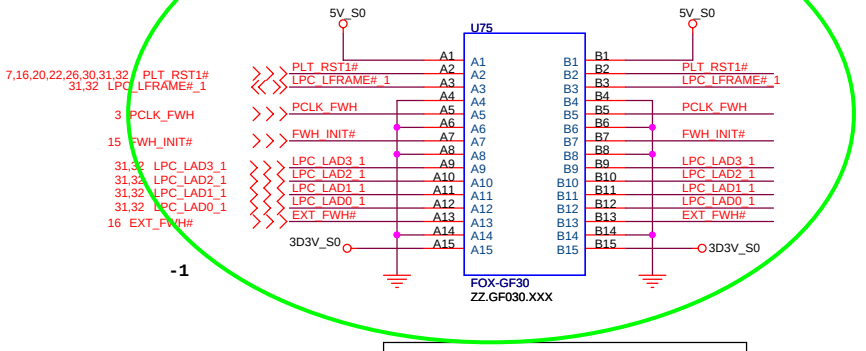
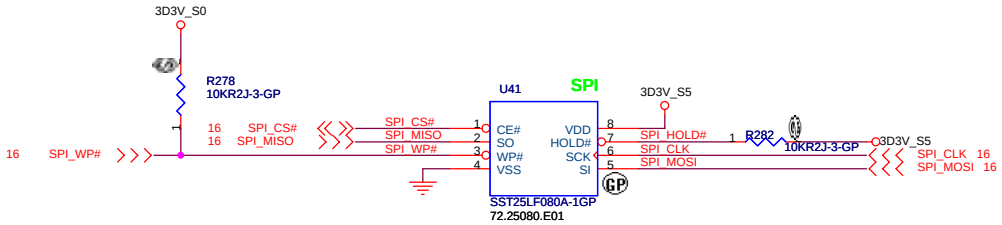
GOLDEN FINGER FOR DEBUG BOARD



Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46

SPI FLASH ROM

8M Bits



SOIC 200 Socket P/N:
Wieson: 62.10076.001
SPI ROM:
SST25LF080A: 72.25080.E01
SST25VF080B : 72.25080.G01
ST M25P80: 72.25P80.001

TOP VIEW

A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

(BOTTOM VIEW)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***BIOS : SPI***

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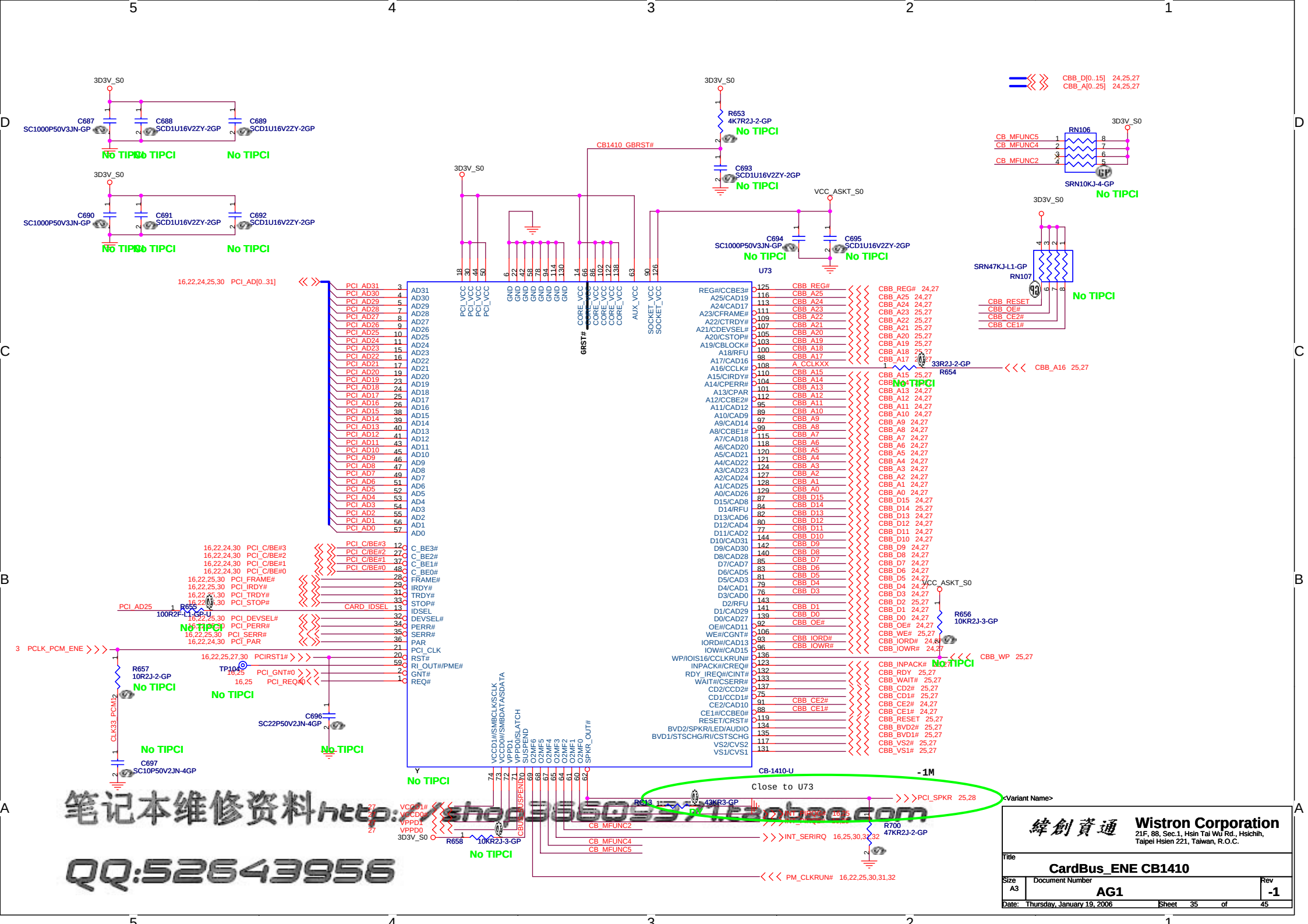
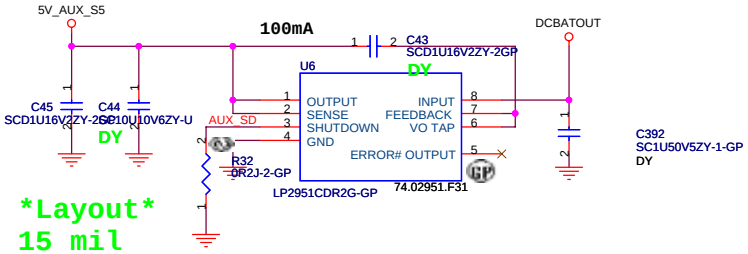
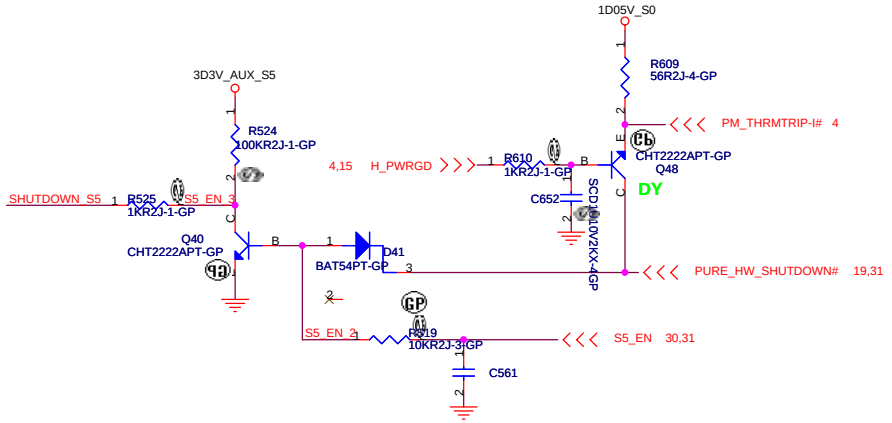
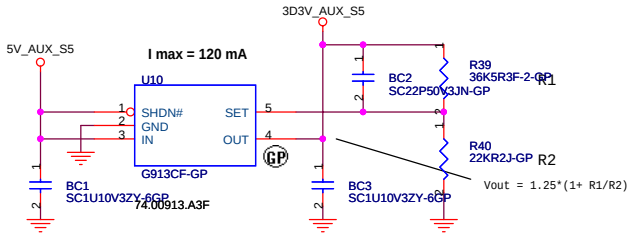
Date: Wednesday, January 18, 2006 Sheet 34 of 45

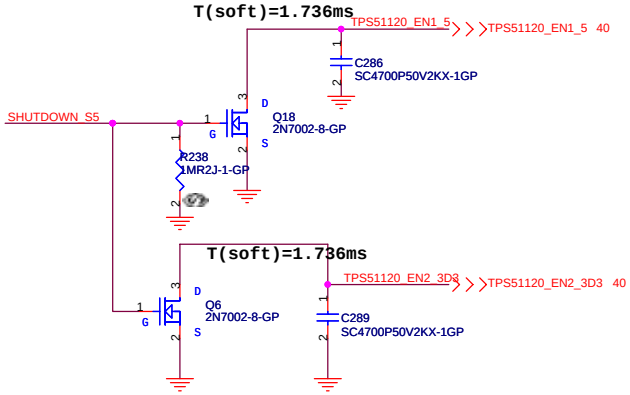


Aux Power

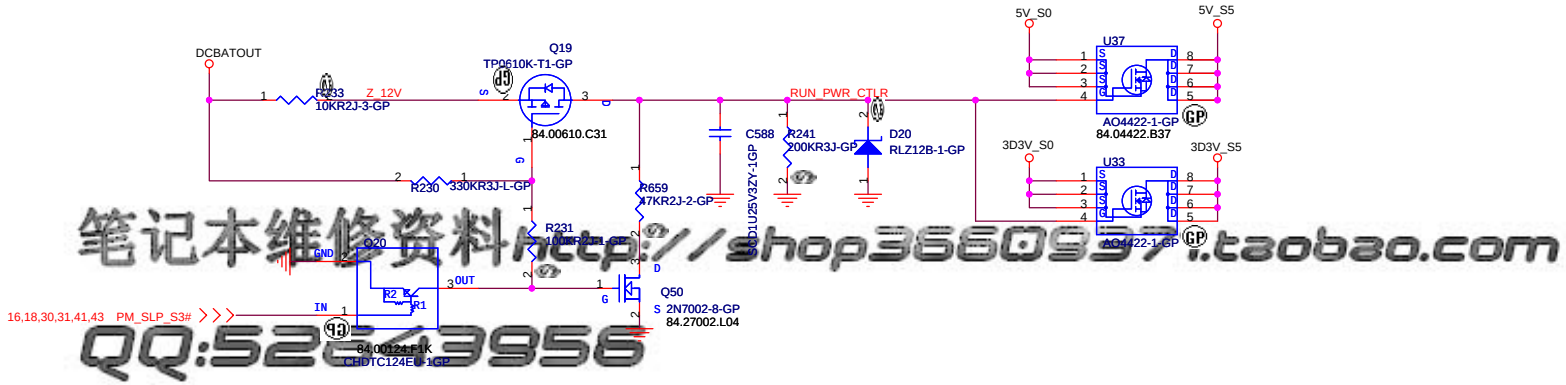








Run Power



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RUN and AUX POWER

Size	Document Number	Rev
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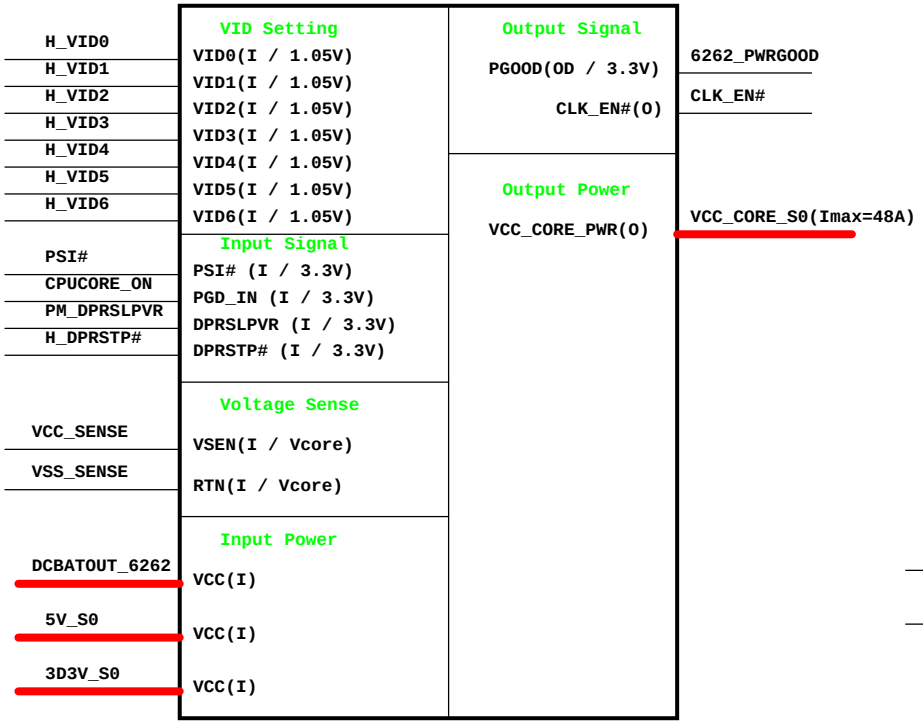
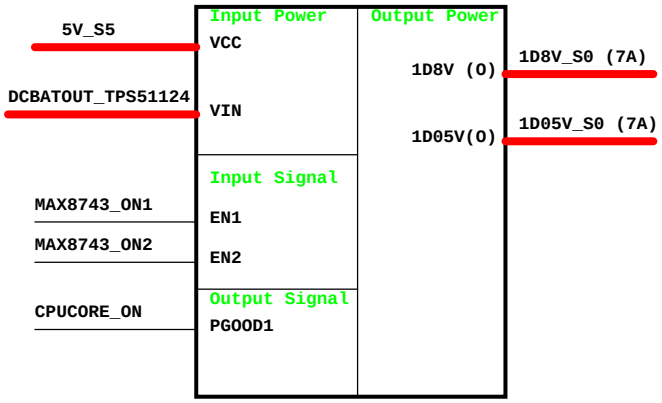
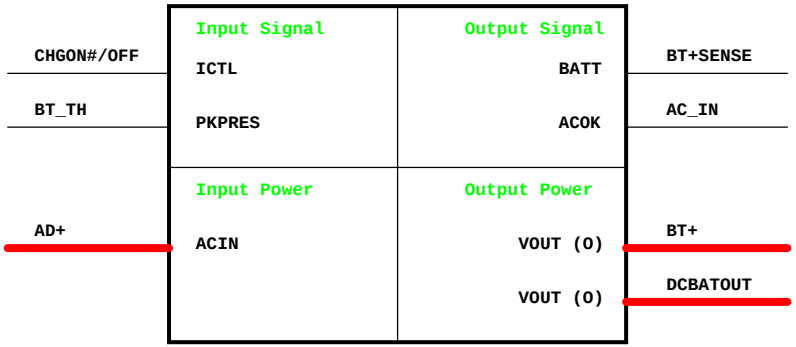
CPU_CORE
Intersil ISL6262



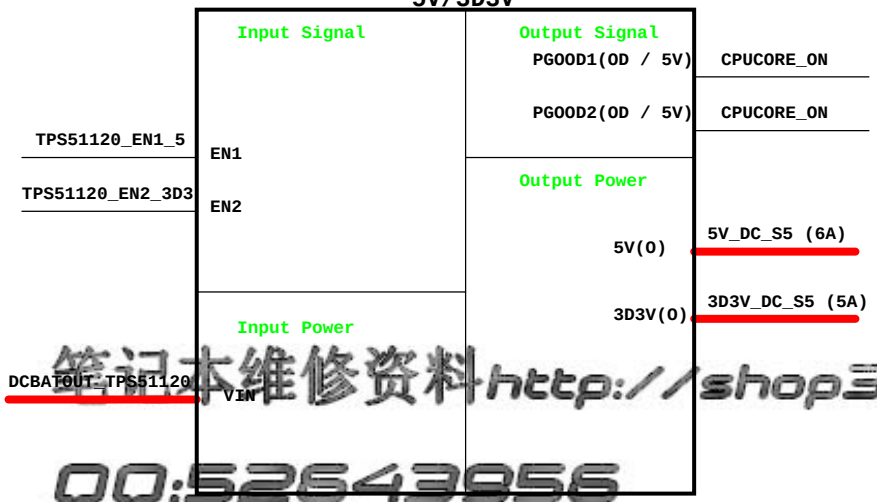
MAX8743
1D8V/1D05V



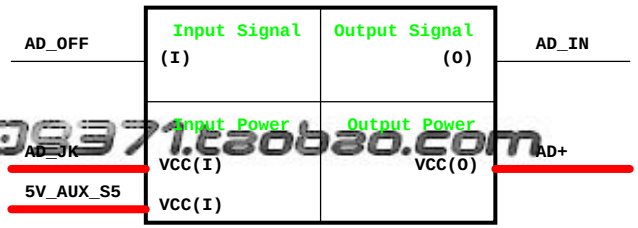
Charger Max8725



TPS51120
5V/3D3V



Adapter



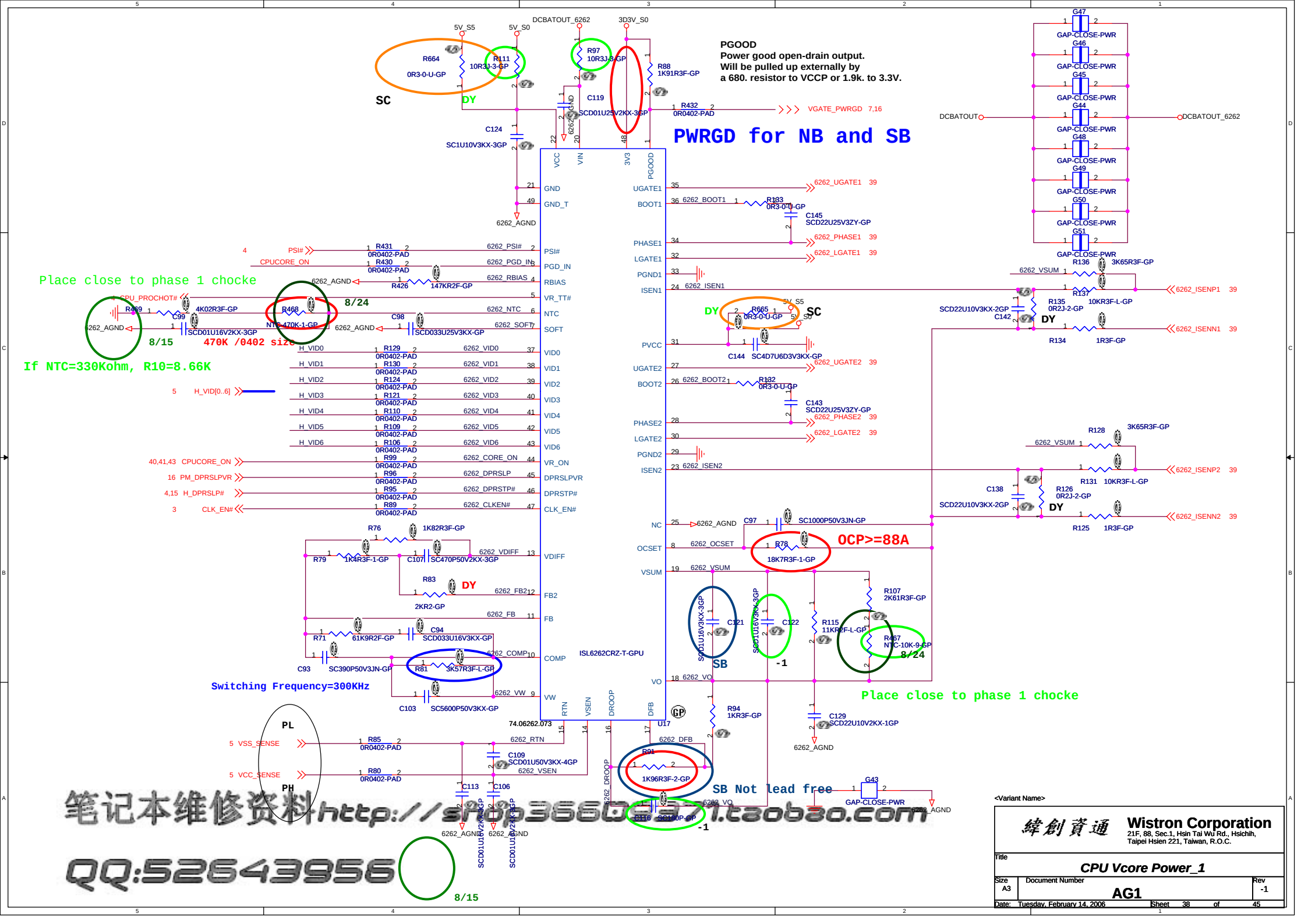
<Variant Name>

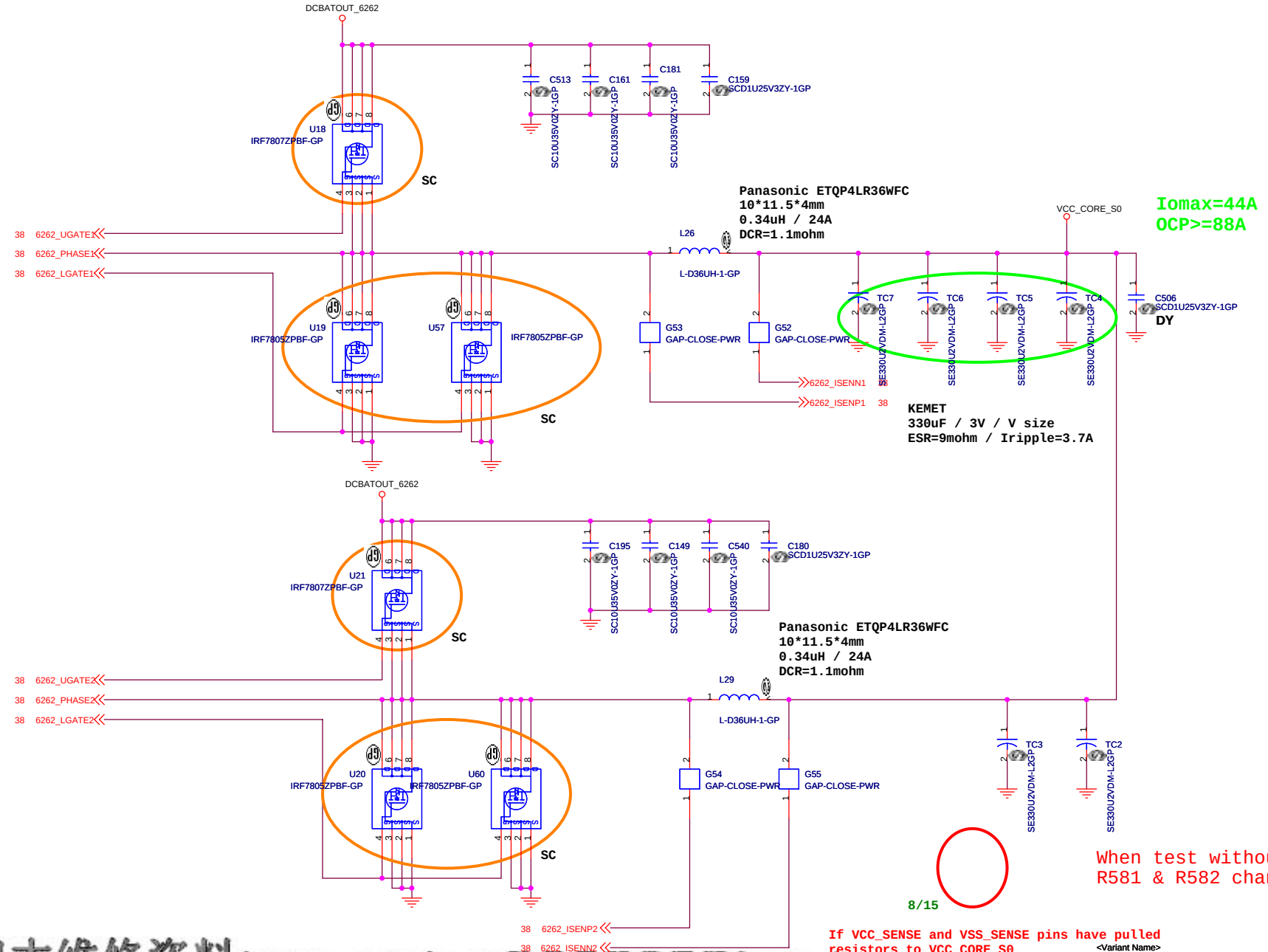
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power Block Diagram***

Size	Document Number	Rev
A3	AG1	-1

Date: Monday, January 09, 2006 Sheet 37 of 45


PGOOD
Power good open-drain output.
Will be pulled up externally by
a 680. resistor to VCCP or 1.9k. to 3.3V.
PWRGD for NB and SB
SC
DY
SB
-1
8/24
8/15
Place close to phase 1 chocke
If NTC=330Kohm, R10=8.66K
470K /0402 size
Switching Frequency=300KHz
OCP>=88A
SB Not lead free
ISL6262CRZ-T-GPU
74.06262.073
PL
PH
VCC
VIN
3V3
PGOOD
GND
GND_T
UGATE1
BOOT1
PHASE1
LGATE1
PGND1
ISEN1
PVCC
UGATE2
BOOT2
PHASE2
LGATE2
PGND2
ISEN2
NC
OCSET
VSUM
VO
PSI#
PGD_IN
RBIAS
VR_TT#
NTC
SOFT
VID0
VID1
VID2
VID3
VID4
VID5
VID6
VR_ON
DPRSLPVR
DPRSTP#
CLK_EN#
VDIFF
FB2
FB
COMP
VW
RTN
VSEN
DROOP
DFB
DCBATOUT_6262
3D3V_S0
5V_S5
5V_S0
6262_AGND
6262_UGATE1
6262_BOOT1
6262_PHASE1
6262_LGATE1
6262_ISEN1
6262_UGATE2
6262_BOOT2
6262_PHASE2
6262_LGATE2
6262_VSUM
6262_ISENP1
6262_ISENN1
6262_ISENP2
6262_ISENN2
6262_OCSET
6262_VO
6262_DFB
6262_VSEN
6262_RTN
6262_VW
6262_COMP
6262_FB
6262_FB2
6262_VDIFF
6262_CLKEN#
6262_DPRSTP#
6262_DPRSLP
6262_CORE_ON
6262_VID0
6262_VID1
6262_VID2
6262_VID3
6262_VID4
6262_VID5
6262_VID6
6262_NTC
6262_SOFT
6262_RBIAS
6262_PGD_IN
6262_PSI#
VGATE_PWRGD 7,16
CPUCORE_ON
CPU_PROCHOT#
H_VID[0..6]
PM_DPRSLPVR
H_DPRSLP#
CLK_EN#
VSS_SENSE
VCC_SENSE
R664 0R3-0-U-GP
R111 10R3J-3-GP
R97 10R3J-3-GP
R88 1K91R3F-GP
R432 0R0402-PAD
C119 SCD01U25V2KX-3GP
C124 SC1U10V3KX-3GP
R133 0R3-0-U-GP
C145 SCD22U25V3ZY-GP
R665 0R3-0-U-GP
C144 SC4D7U6D3V3KX-GP
R132 0R3-0-U-GP
C143 SCD22U25V3ZY-GP
R431 0R0402-PAD
R430 0R0402-PAD
R426 147KR2F-GP
R469 4K02R3F-GP
C99 SCD01U16V2KX-3GP
R468 NTC-470K-1-GP
C98 SCD033U25V3KX-GP
R129 0R0402-PAD
R130 0R0402-PAD
R124 0R0402-PAD
R121 0R0402-PAD
R110 0R0402-PAD
R109 0R0402-PAD
R106 0R0402-PAD
R99 0R0402-PAD
R96 0R0402-PAD
R95 0R0402-PAD
R89 0R0402-PAD
R76 1K82R3F-GP
R79 1K4R3F-1-GP
C107 SC470P50V2KX-3GP
R83 2KR2-GP
R71 61K9R2F-GP
C94 SCD033U16V3KX-GP
C93 SC390P50V3JN-GP
R81 3K57R3F-L-GP
C103 SC5600P50V3KX-GP
R85 0R0402-PAD
R80 0R0402-PAD
C109 SCD01U50V3KX-4GP
C113 SCD01U16V2KX-3GP
C106 SCD01U16V2KX-3GP
C97 SC1000P50V3JN-GP
R78 18K7R3F-1-GP
C121 SCD01U16V3KX-3GP
C122 SCD01U16V3KX-3GP
R115 11KR2F-L-GP
R107 2K61R3F-GP
R467 NTC-10K-9-GP
R94 1KR3F-GP
C129 SCD22U10V2KX-1GP
R91 1K96R3F-2-GP
C116 SC100P-GP
G43 GAP-CLOSE-PWR
G47 GAP-CLOSE-PWR
G46 GAP-CLOSE-PWR
G45 GAP-CLOSE-PWR
G44 GAP-CLOSE-PWR
G48 GAP-CLOSE-PWR
G49 GAP-CLOSE-PWR
G50 GAP-CLOSE-PWR
G51 GAP-CLOSE-PWR
R136 3K65R3F-GP
R137 10KR3F-L-GP
R135 0R2J-2-GP
C142 SCD22U10V3KX-2GP
R134 1R3F-GP
R128 3K65R3F-GP
R131 10KR3F-L-GP
R126 0R2J-2-GP
C138 SCD22U10V3KX-2GP
R125 1R3F-GP
笔记本维修资料http://shop36602a71.taobao.com
QQ:52643956
8/15
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU Vcore Power_1
Size A3
Document Number AG1
Rev -1
Date: Tuesday, February 14, 2006
Sheet 38 of 45



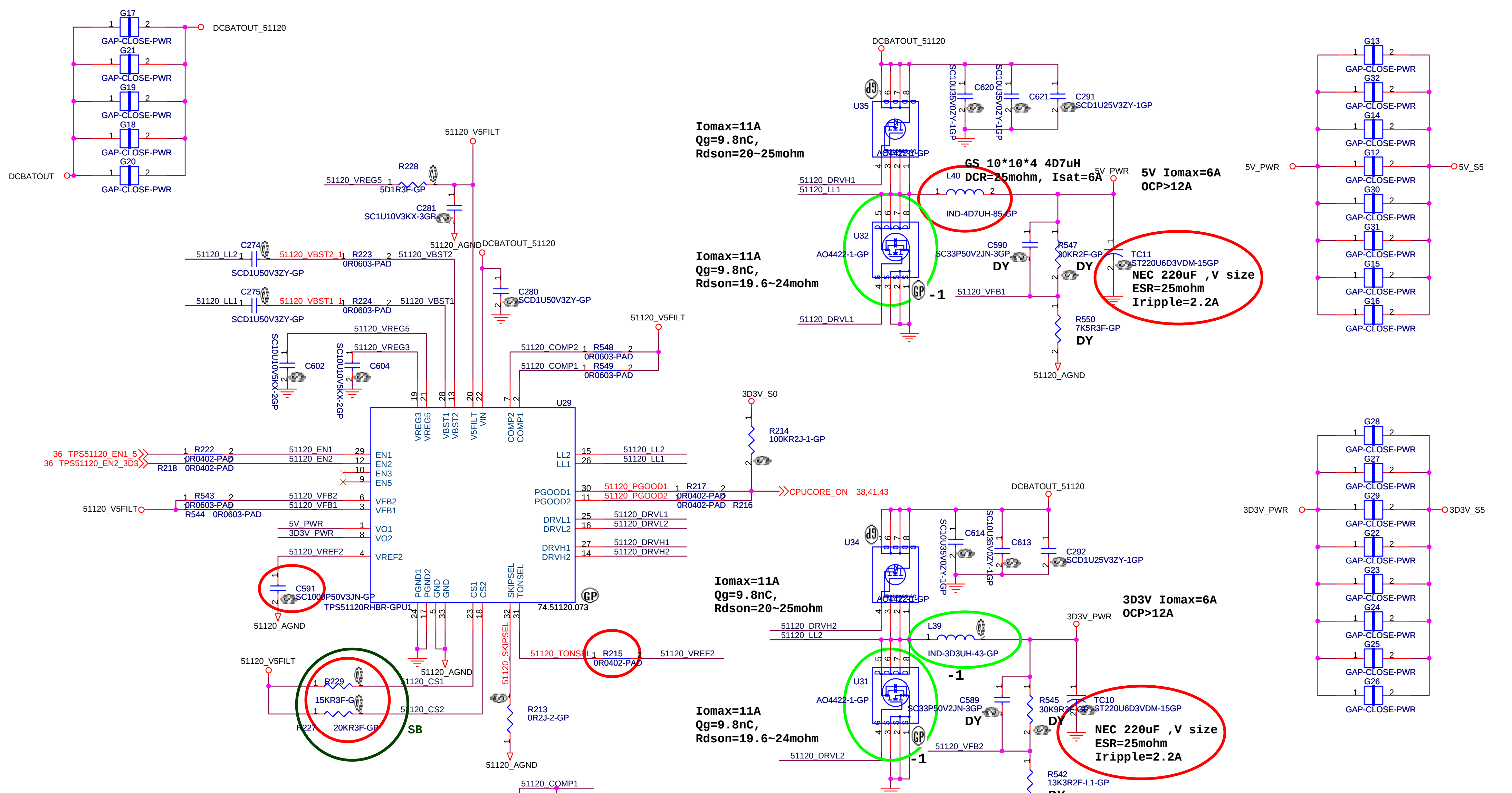
<Variant Name>

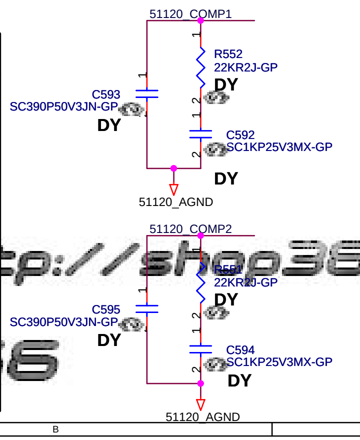
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU Vcore Power_2

Size	Document Number	Rev
A3	AG1	-1

Date: Wednesday, January 18, 2006 Sheet 39 of 45





	GND	VREF2	FLOAT	V5FILT
SKIPSEL	**AUTOSKIP**	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	**D-Cap MODE**
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	**220k/CH1 330k/CH2**	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	**5V Fixed Output**
VFB2	N/A	not use	ADJ.	**3.3V Fixed Output**
EN1,EN2	Switcher OFF	not use	Swithchr ON	Switcher ON
EN3,EN5	LDO OFF	not use	**LDO ON**	VREG3 on

Vout=1V*(R1+R2)/R2

For TPS51120,
Vout=5V
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.

Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
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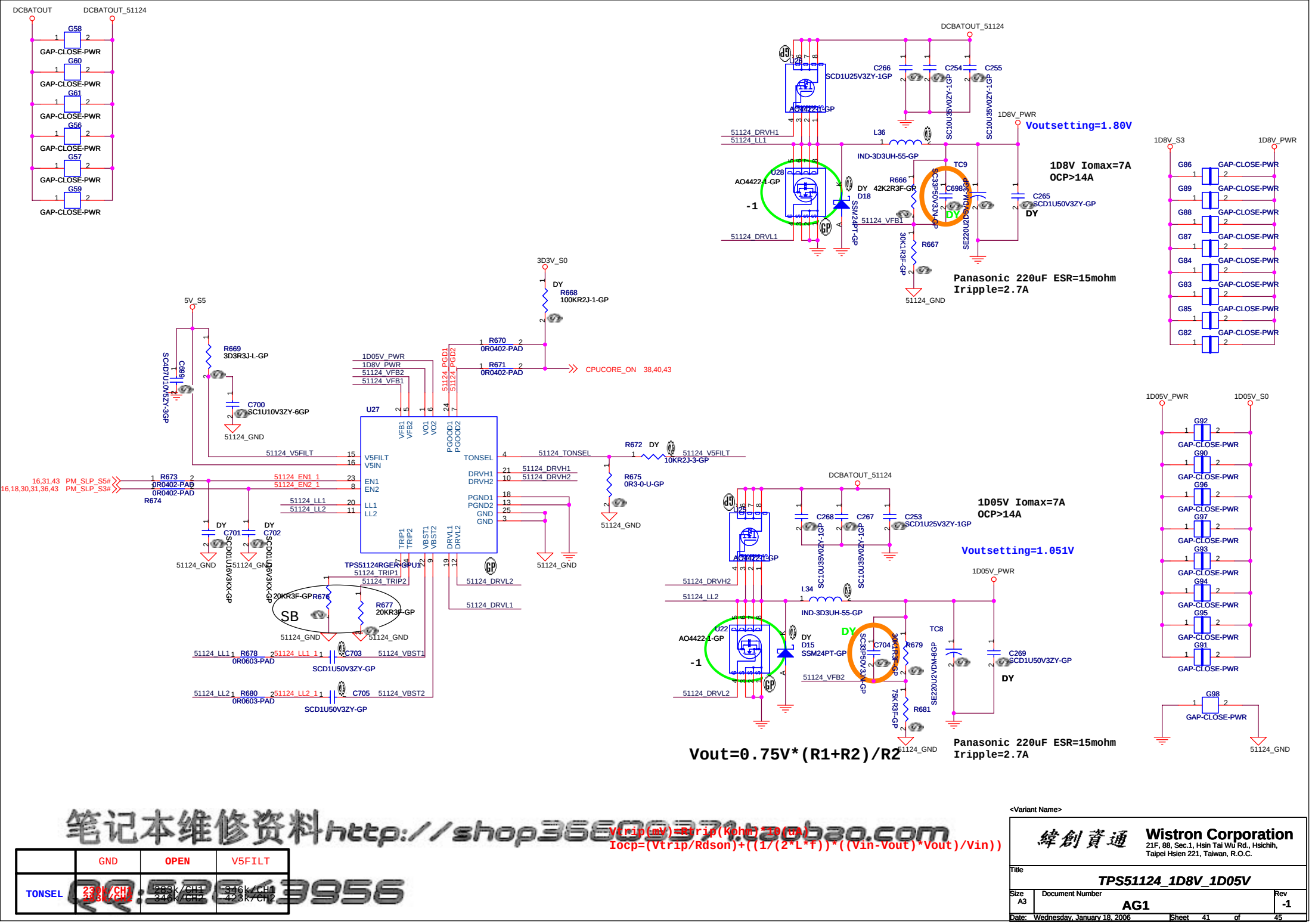
Size A3	Document Number AG1	Rev -1
Date: Wednesday, January 18, 2006	Sheet 40 of 45	


DCBATOUT
DCBATOUT_51124
GAP-CLOSE-PWR
DCBATOUT_51124
SCD1U25V3ZY-1GP
AO4422-1-GP
SC10U35V0ZY-1GP
1D8V_PWR
Voutsetting=1.80V
51124_DRVH1
51124_LL1
L36
IND-3D3UH-55-GP
TC9
U28
R666
42K2R3F-GP
C698
C265
SCD1U50V3ZY-GP
DY
D18
SSM24PT-GP
51124_VFB1
51124_DRVL1
30K1R3F-GP
R667
51124_GND
1D8V Iomax=7A
OCP>14A
Panasonic 220uF ESR=15mohm
Iripple=2.7A
1D8V_S3
G86
G89
G88
G87
G84
G83
G85
G82
3D3V_S0
R668
100KR2J-1-GP
CPUCORE_ON 38,40,43
5V_S5
R669
3D3R3J-L-GP
C700
SC1U10V3ZY-6GP
C691
SC4D7U10V5ZY-3GP
R670
0R0402-PAD
R671
0R0402-PAD
1D05V_PWR
1D8V_PWR
51124_VFB2
51124_VFB1
51124_PGD1
51124_PGD2
U27
VFB1
VFB2
VO1
VO2
PGOOD1
PGOOD2
V5FILT
V5IN
EN1
EN2
LL1
LL2
TONSEL
DRVH1
DRVH2
PGND1
PGND2
GND
TRIP1
TRIP2
VBST1
VBST2
DRVL1
DRVL2
TPS51124RGERGPU1
51124_V5FILT
51124_TONSEL
R672
10KR2J-3-GP
R675
0R3-0-U-GP
16,31,43 PM_SLP_S5#
16,18,30,31,36,43 PM_SLP_S3#
R673
0R0402-PAD
R674
51124_EN1_1
51124_EN2_1
51124_LL1
51124_LL2
C701
C702
SCD01U16V3KX-GP
51124_TRIP1
51124_TRIP2
SB
R676
20KR3F-GP
R677
20KR3F-GP
R678
0R0603-PAD
R680
0R0603-PAD
C703
C705
SCD1U50V3ZY-GP
51124_VBST1
51124_VBST2
51124_DRVL2
51124_DRVL1
DCBATOUT_51124
1D05V Iomax=7A
OCP>14A
Voutsetting=1.051V
C268
C267
C253
SCD1U25V3ZY-1GP
SC10U35V0ZY-1GP
51124_DRVH2
51124_LL2
L34
IND-3D3UH-55-GP
U22
AO4422-1-GP
D15
SSM24PT-GP
C704
R679
TC8
C269
SCD1U50V3ZY-GP
51124_VFB2
75K2R3F-GP
R681
SE220U2VDM-8GP
Vout=0.75V*(R1+R2)/R2
Panasonic 220uF ESR=15mohm
Iripple=2.7A
1D05V_PWR
1D05V_S0
G92
G90
G96
G97
G93
G94
G95
G91
G98
Vtrip(mV)=Rtrip(Kohm)*Io(uA)
Iocp=(Vtrip/Rdson)+((1/(2*L*f))*((Vin-Vout)*Vout)/Vin))
GND
OPEN
V5FILT
TONSEL
230K/CH1
318K/CH2
283K/CH1
316K/CH2
316K/CH1
423K/CH2
笔记本维修资料http://shop36809374.taobao.com
QQ:526413956
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
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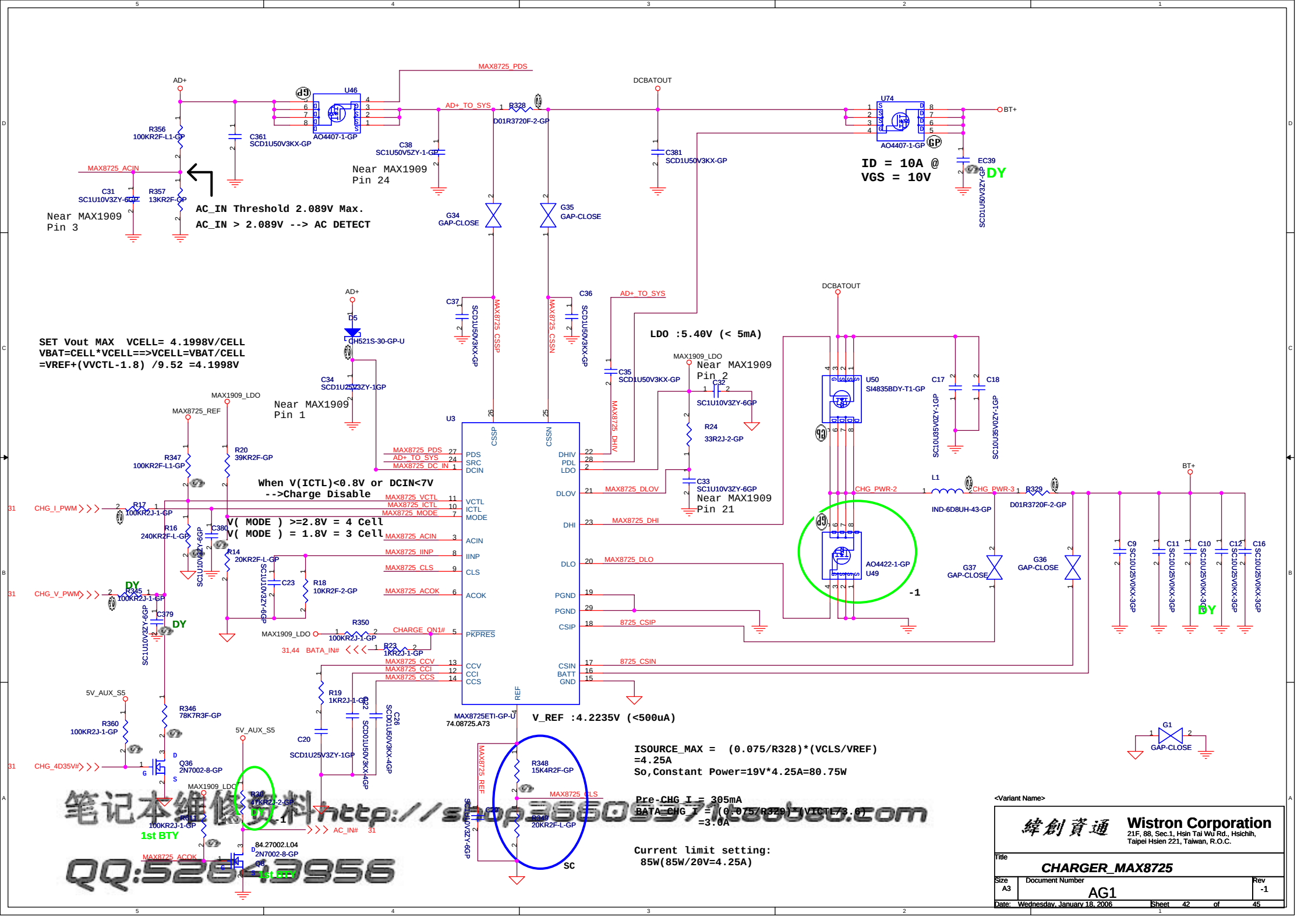
Size
A3
Document Number
AG1
Rev
-1
Date: Wednesday, January 18, 2006
Sheet 41 of 45



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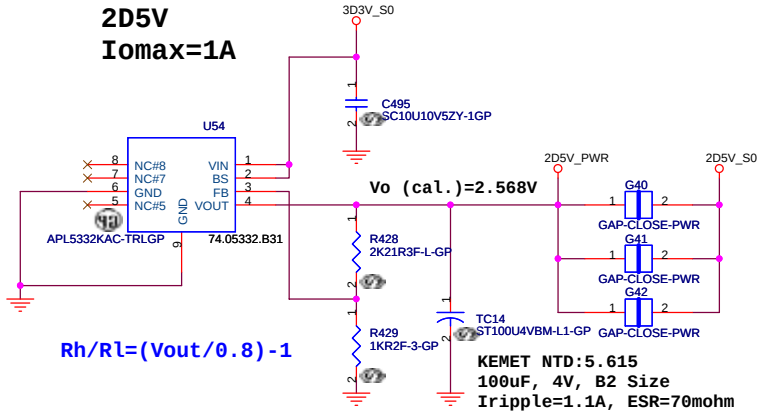
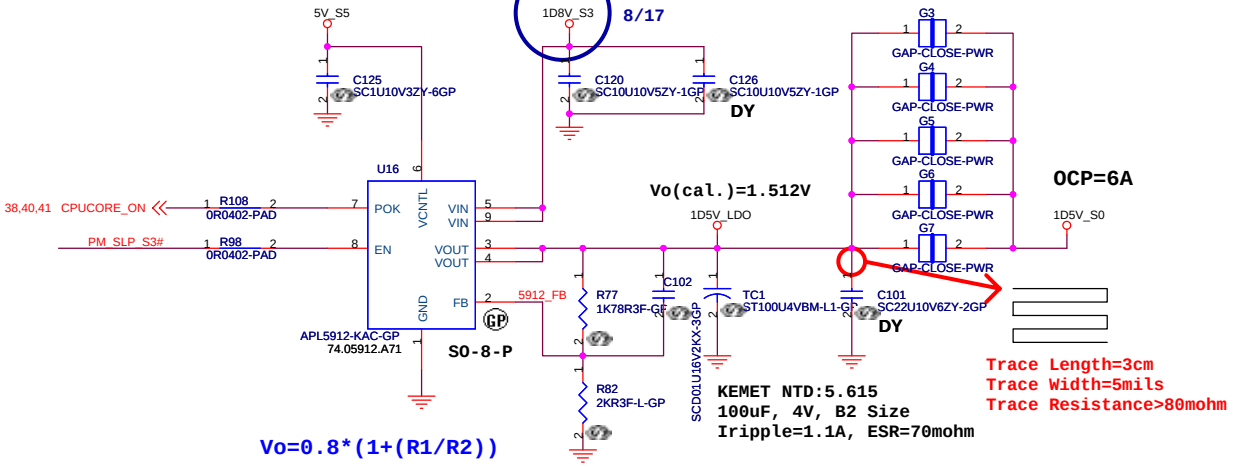


1D5V_S0
Iomax=4.0A



0D9V
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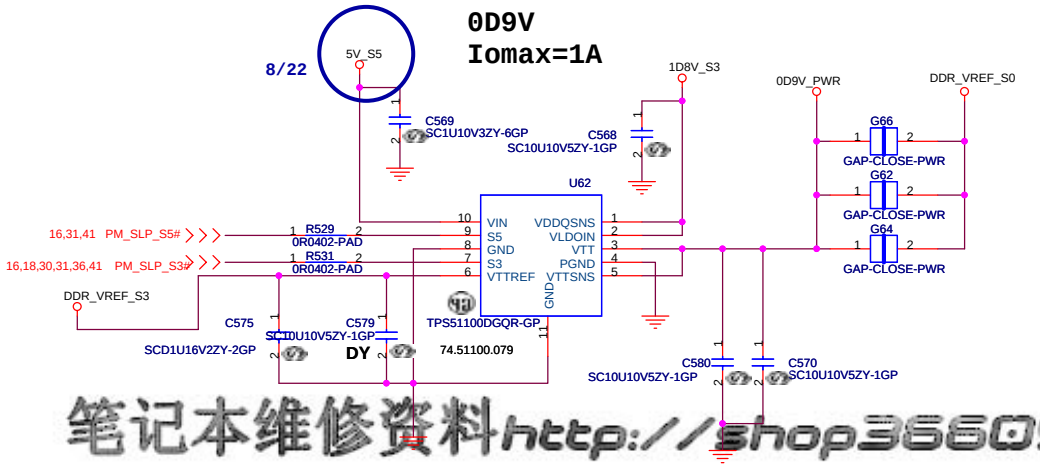

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G2997F6U

<Variant Name>

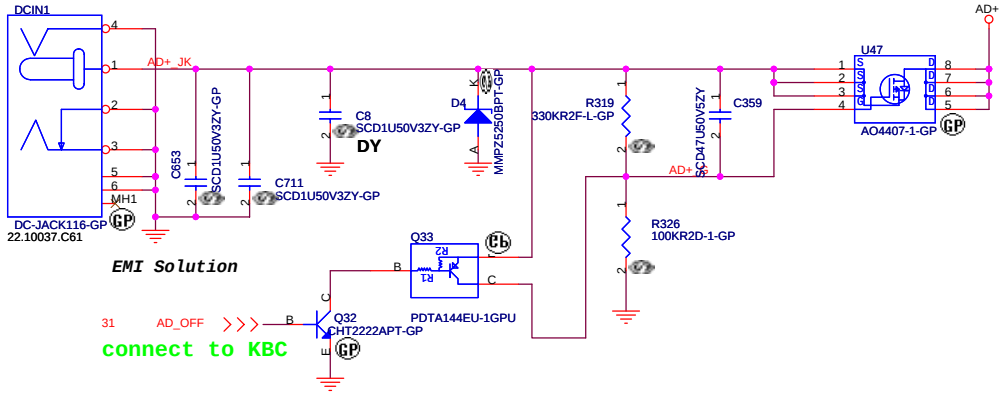
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *0D9V/1D5V/2D5V*

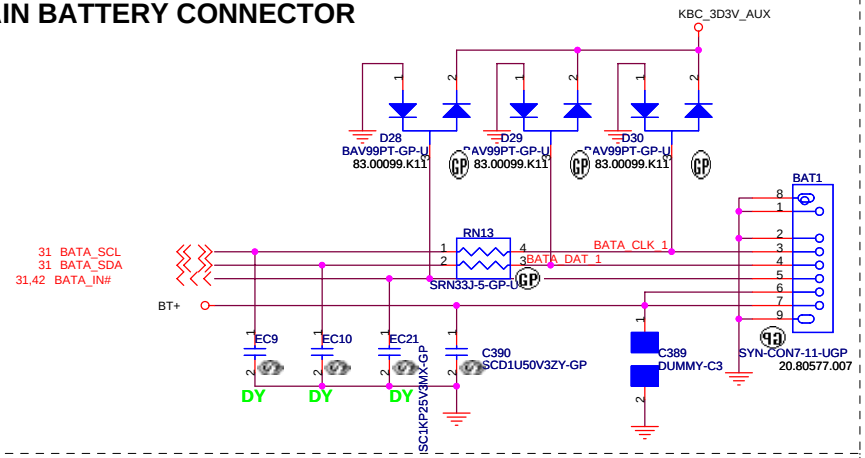
Size	Document Number	Rev
A3	AG1	-1

Date: Wednesday, January 18, 2006 Sheet 43 of 45

ADAPTER IN CIRCUIT

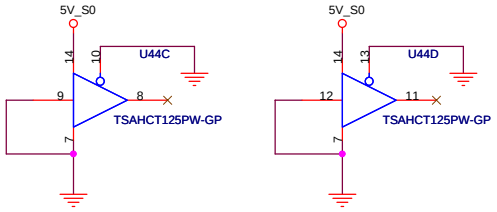


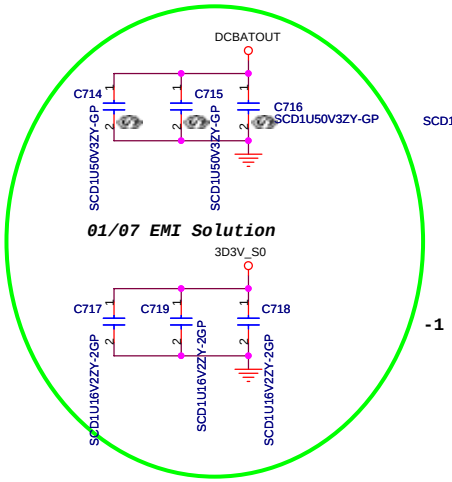
MAIN BATTERY CONNECTOR



<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***AD/BATT CONN***
Size: A3	Document Number: AG1
Rev: -1	
Date: Wednesday, January 18, 2006	Sheet 44 of 45





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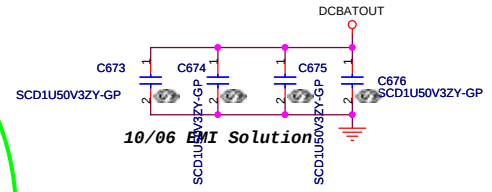
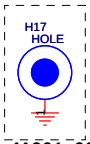


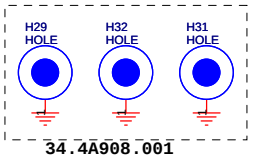
TOP SIDE:

New Card



34.4A901.001

CPU Thermal Module



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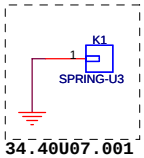

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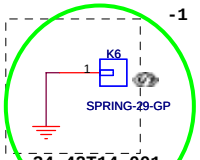

34.42T14.001

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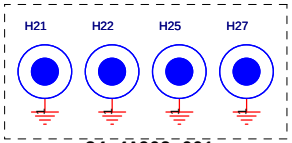
BOTTOM SIDE:

IO Bracket FOR MDC



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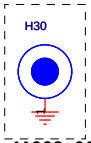

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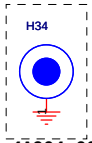

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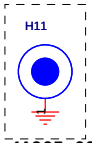

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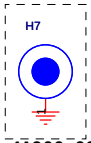

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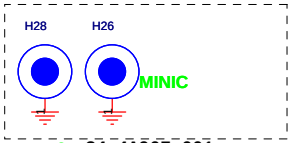

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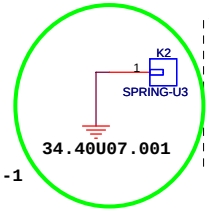

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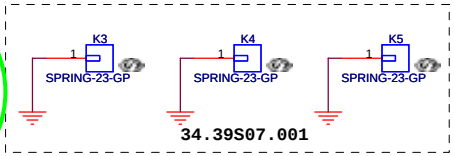

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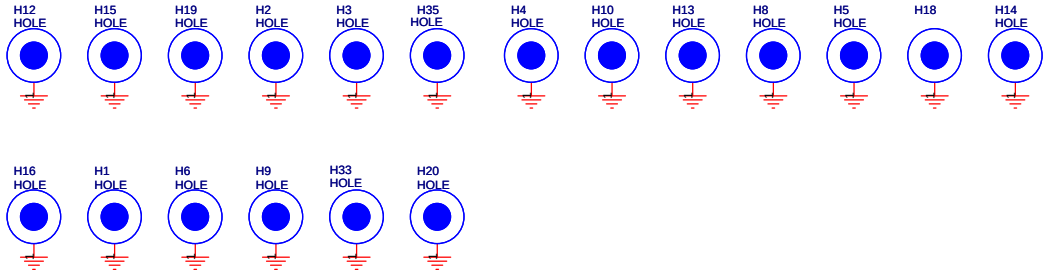

<Variant Name>

緯創資通 Wistron Corporation
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