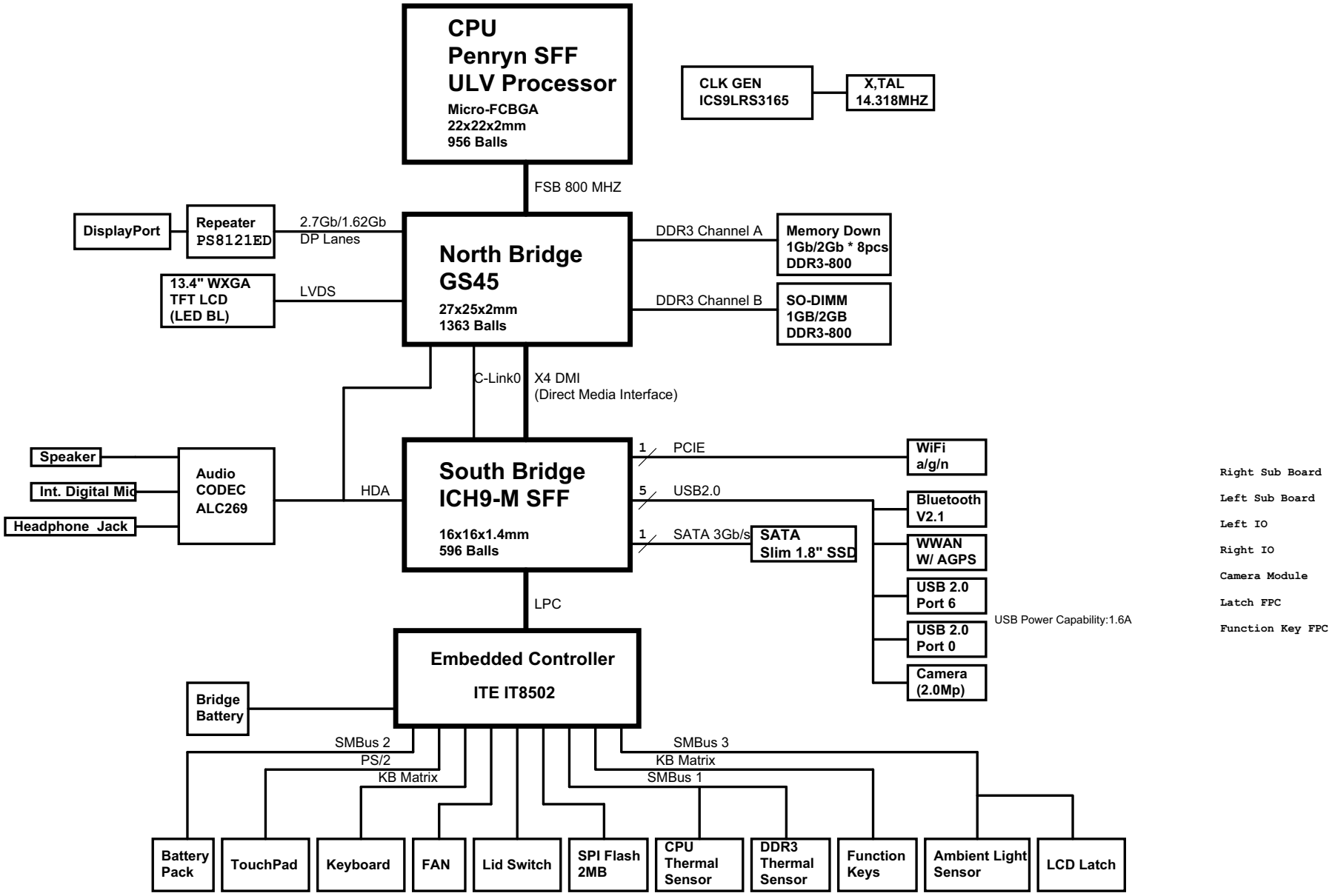
Schematics Page Index (Title / Revision / Change Date)

Project Code & Schematics Subject:	**H800 Main Board**	**1P-0099L00-A000 (COMPEQ)** **1P-0099J00-A000 (IRIS)**

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	**INDEX PAGE**	
Size: Custom	Document Number: H800 MB	Rev: X-Build
Date: Wednesday, October 07, 2009	Sheet 1 of 50	

H800 BLOCK DIAGRAM



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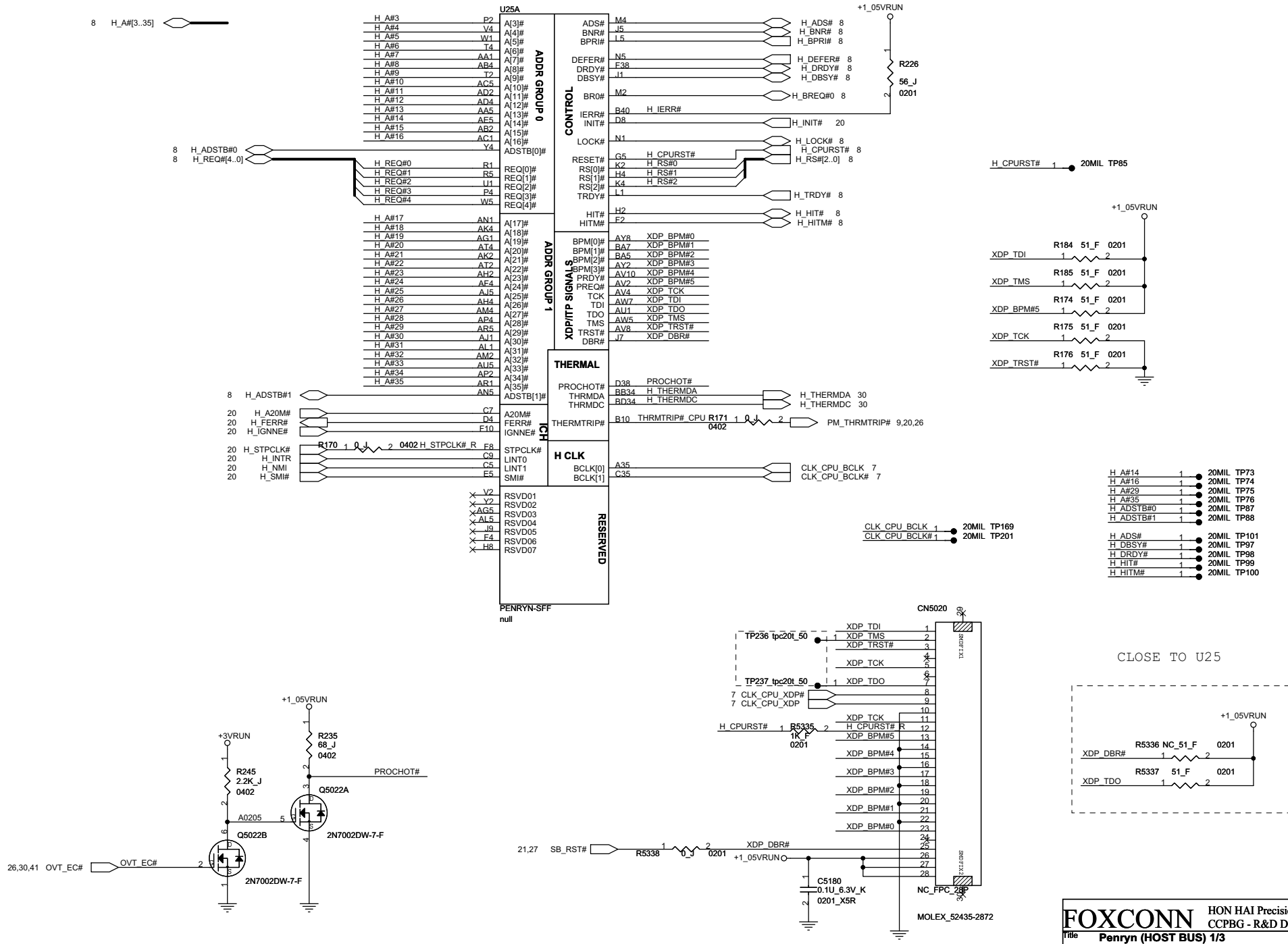
Title: BLOCK DIAGRAM		
Size: Custom	Document Number: H800 MB	Rev: X-Build
Date: Wednesday, October 07, 2009	Sheet 2 of 50	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R184 51_F 0201
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R176 51_F 0201
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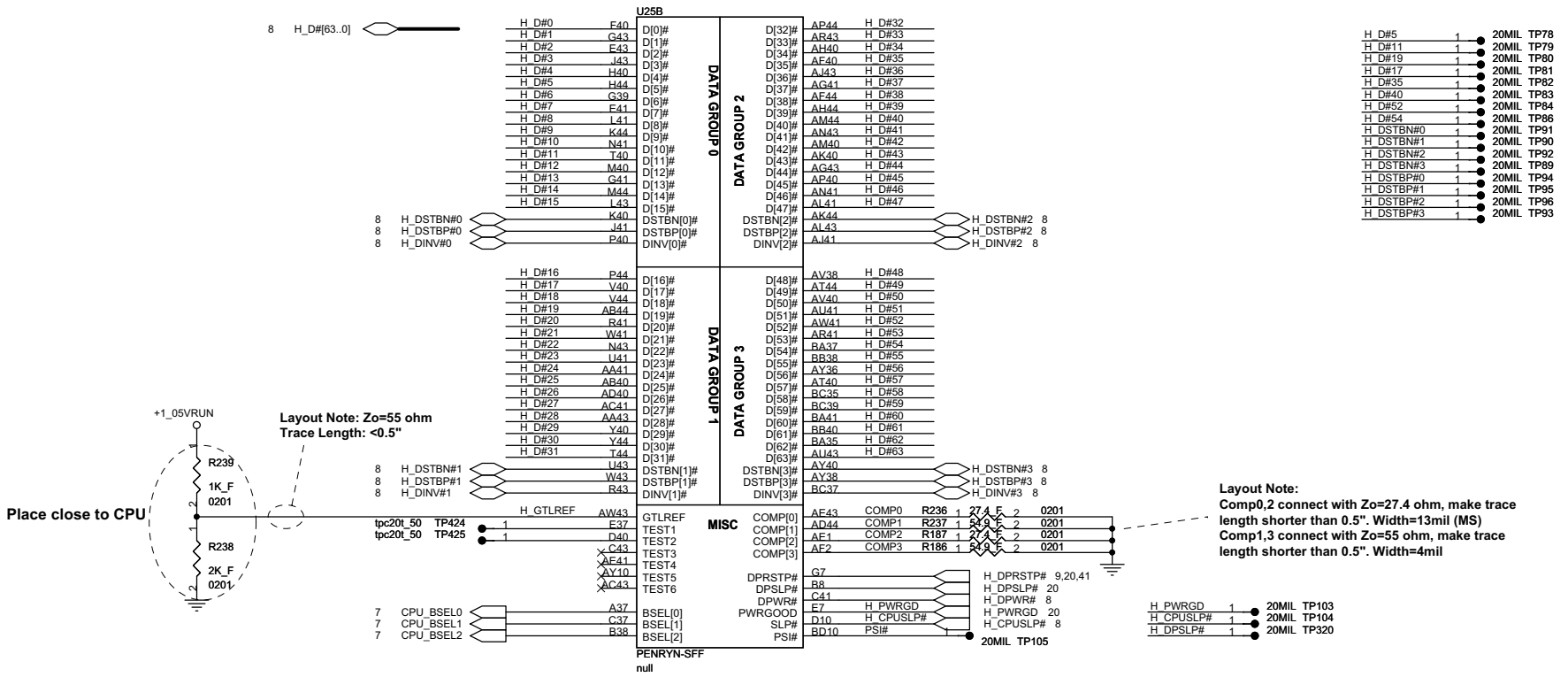
2N7002DW-7-F
CLOSE TO U25
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Penryn (HOST BUS) 1/3
Size A3
Document Number H800 MB
Rev X-Build
Date: Monday, October 12, 2009
Sheet 3 of 50



FOXCONN HON HAI Precision Ind. Co., Ltd.
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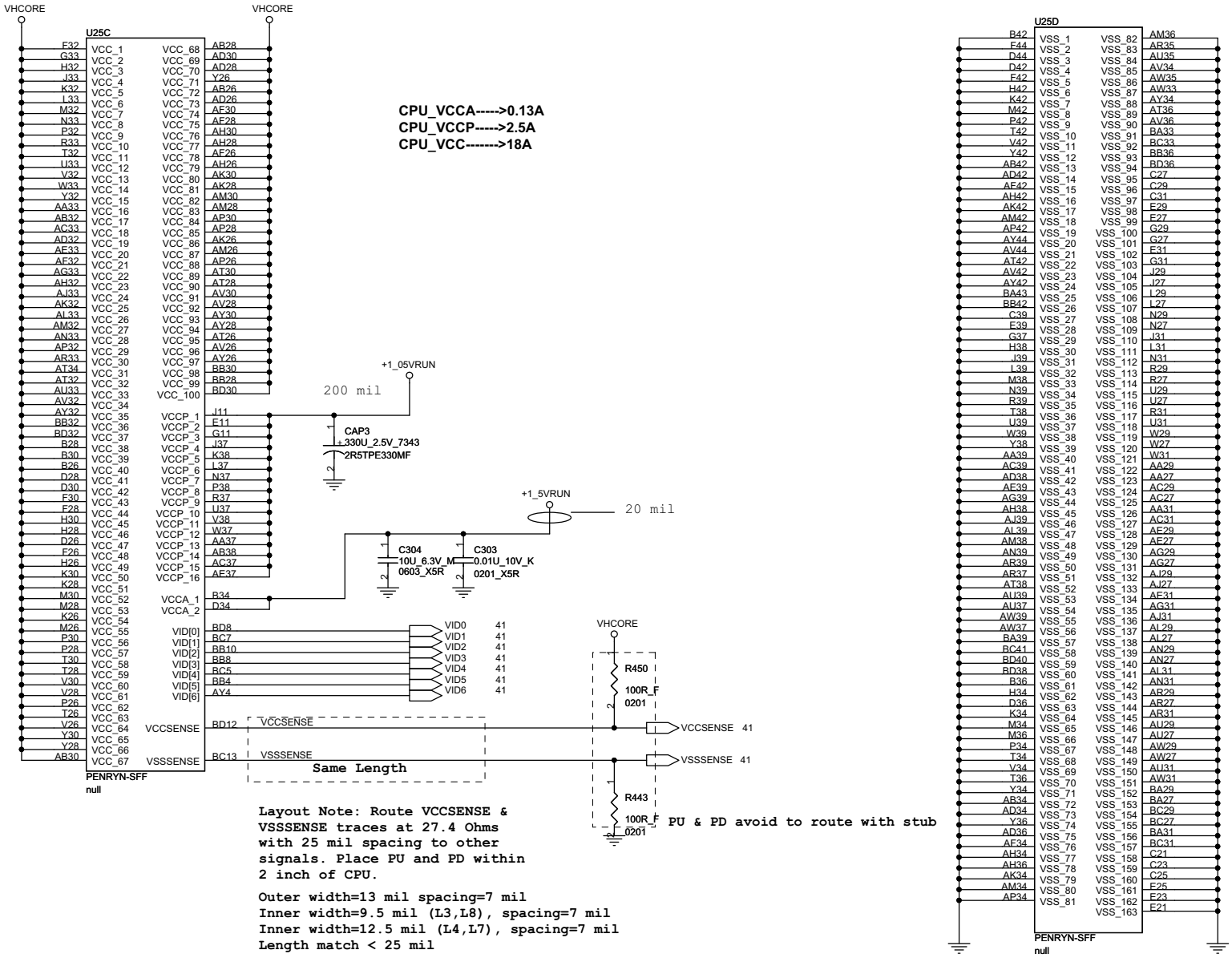
Title: Penryn (HOST BUS) 2/3

Size	Document Number	Rev
A3	H800 MB	X-Build

Date: Monday, October 12, 2009 Sheet 4 of 50



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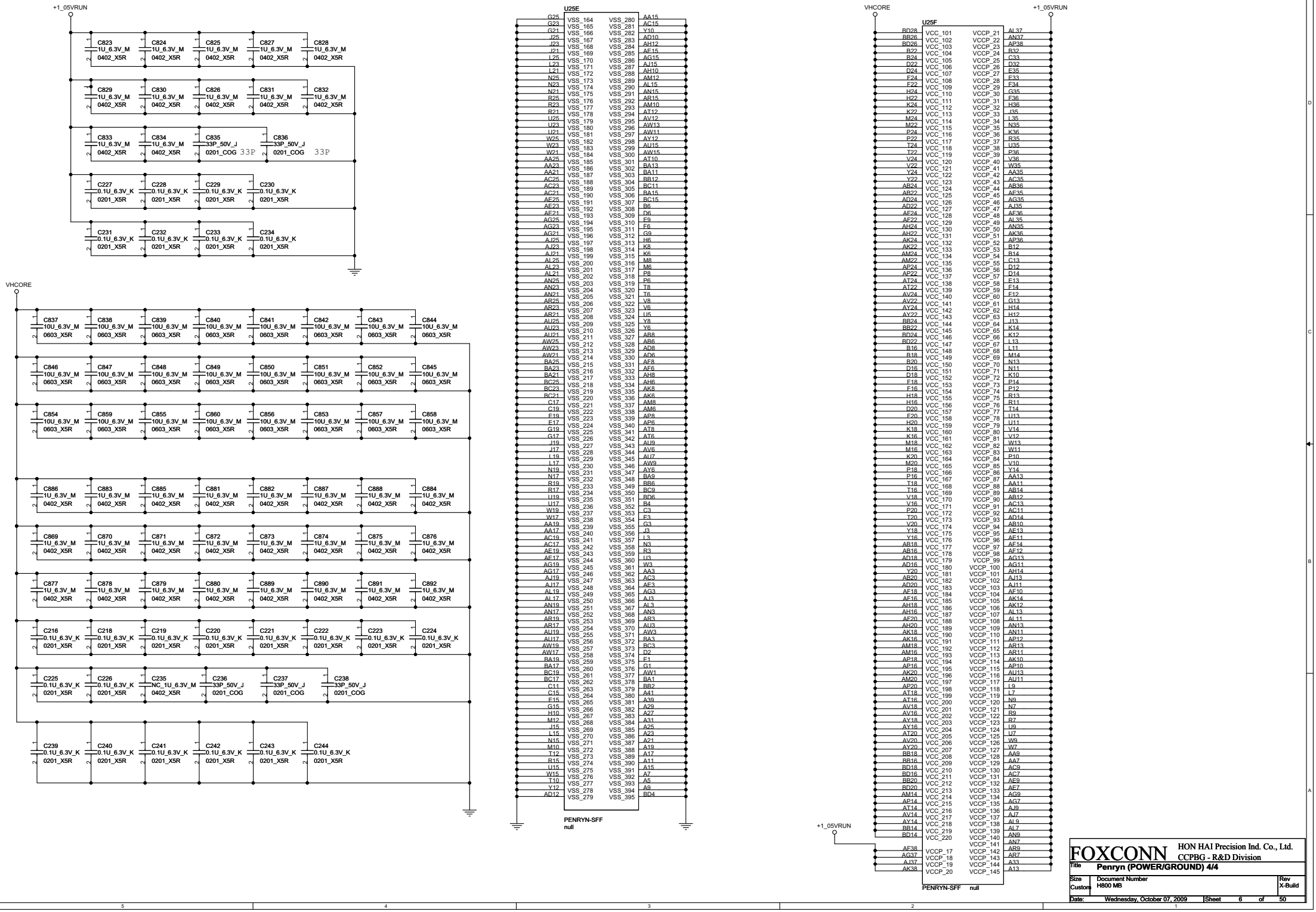
Size A3	Document Number H800 MB	Rev X-Build
Date: Monday, October 12, 2009	Sheet 5 of 50	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C827 1U_6.3V_M 0402_X5R
C828 1U_6.3V_M 0402_X5R
C829 1U_6.3V_M 0402_X5R
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C826 1U_6.3V_M 0402_X5R
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C832 1U_6.3V_M 0402_X5R
C833 1U_6.3V_M 0402_X5R
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VCCP_79 U11
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VCCP_81 V12
VCCP_82 W13
VCCP_83 W11
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VCCP_117 AU11
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VCCP_119 L7
VCCP_120 N9
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VCCP_122 R9
VCCP_123 R7
VCCP_124 U9
VCCP_125 U7
VCCP_126 W9
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HON HAI Precision Ind. Co., Ltd.
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Title
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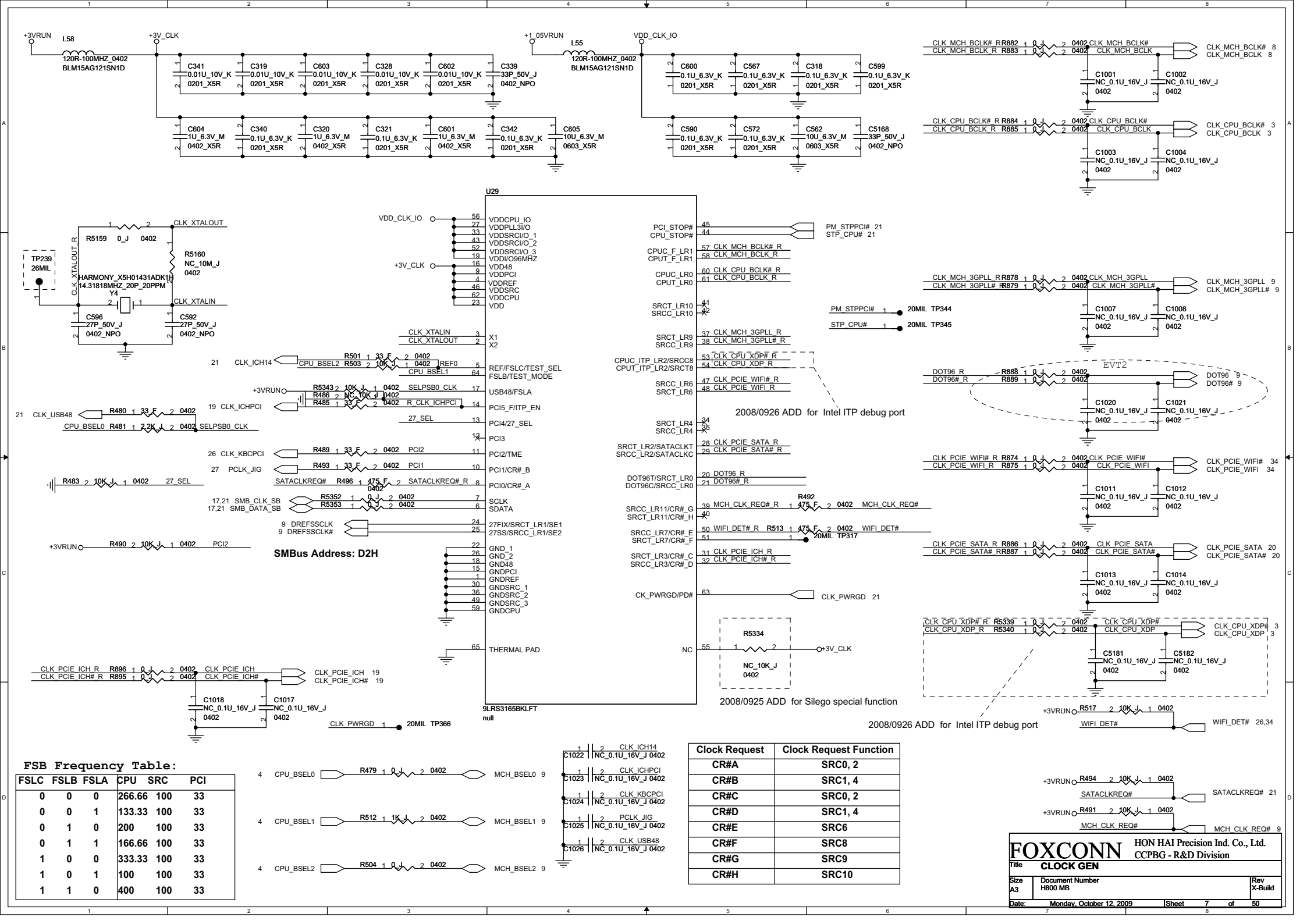
Size
Custom
Document Number
H800 MB
Rev
X-Build
Date:
Wednesday, October 07, 2009
Sheet
6
of
50



FSB Frequency Table:

FSLC	FSLB	FSLA	CPU	SRC	PCI
0	0	0	266.66	100	33
0	0	1	133.33	100	33
0	1	0	200	100	33
0	1	1	166.66	100	33
1	0	0	333.33	100	33
1	0	1	100	100	33
1	1	0	400	100	33

Clock Request	Clock Request Function
CR#A	SRC0, 2
CR#B	SRC1, 4
CR#C	SRC0, 2
CR#D	SRC1, 4
CR#E	SRC6
CR#F	SRC8
CR#G	SRC9
CR#H	SRC10

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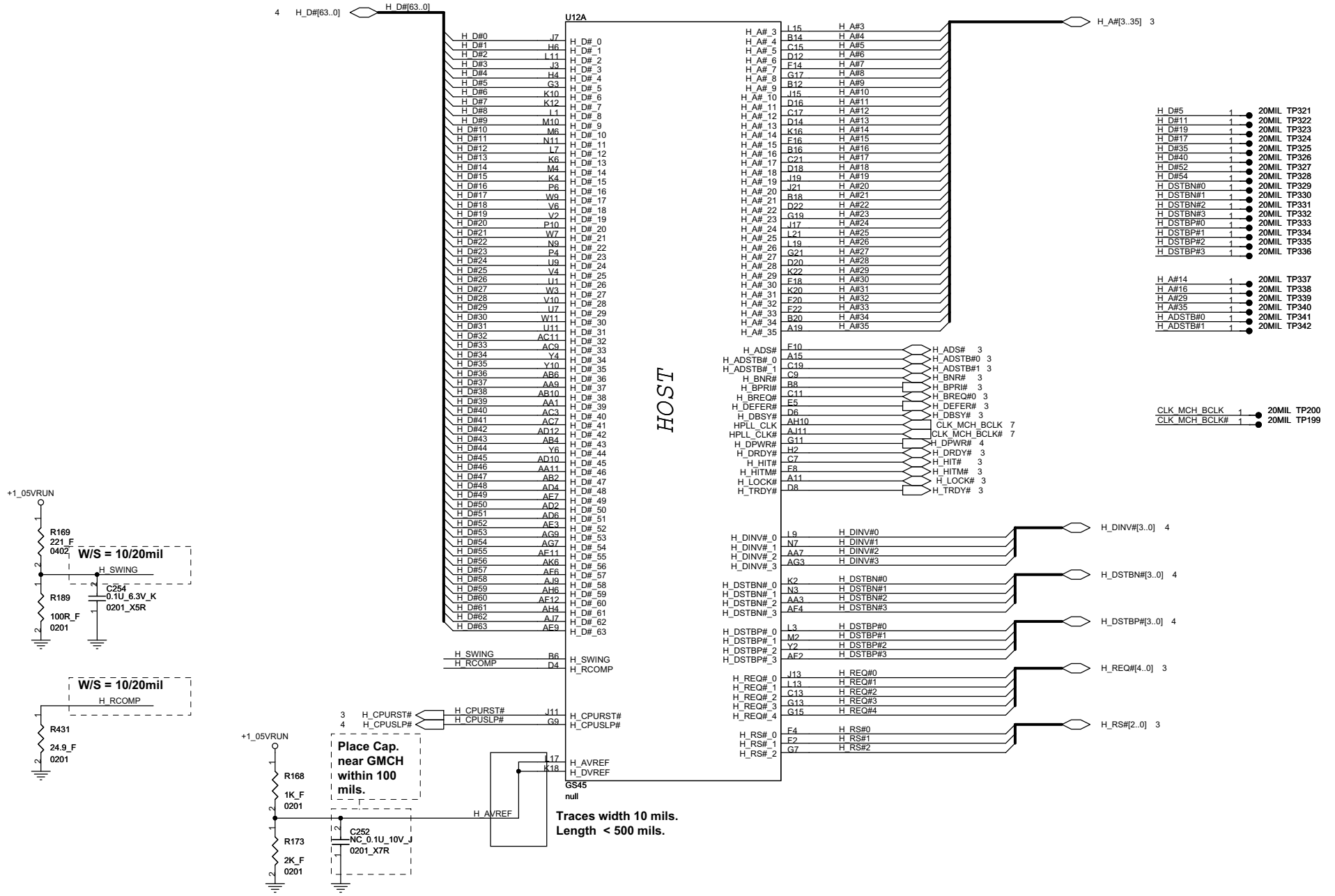
Title: CLOCK GEN		
Size: A3	Document Number: H800 MB	Rev: X-Build
Date: Monday, October 12, 2009	Sheet 7 of 50	



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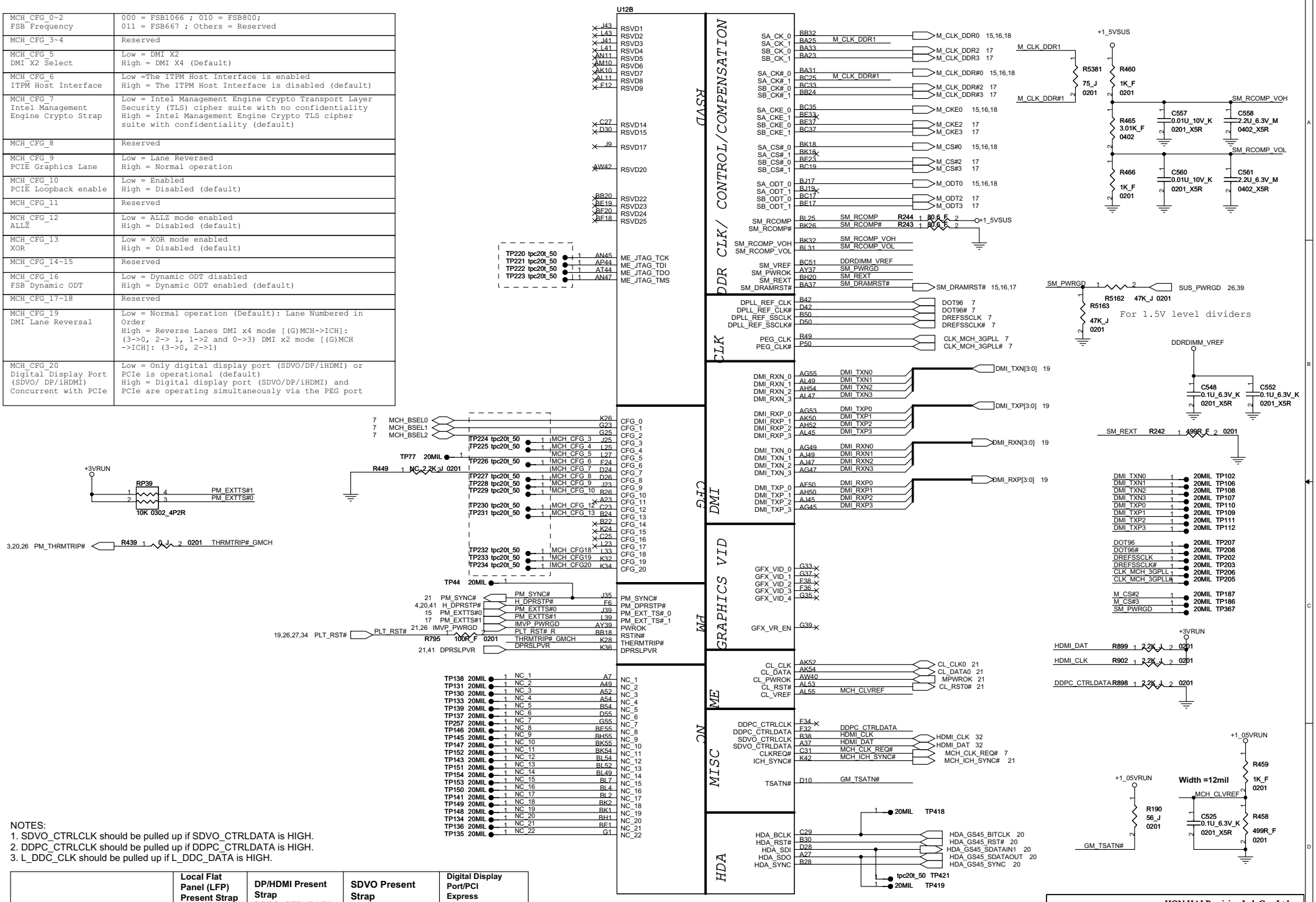
Title: Cantiga (HOST) 1/7		
Size: A3	Document Number: H800 MB	Rev: X-Build
Date: Monday, October 12, 2009	Sheet 8 of 50	

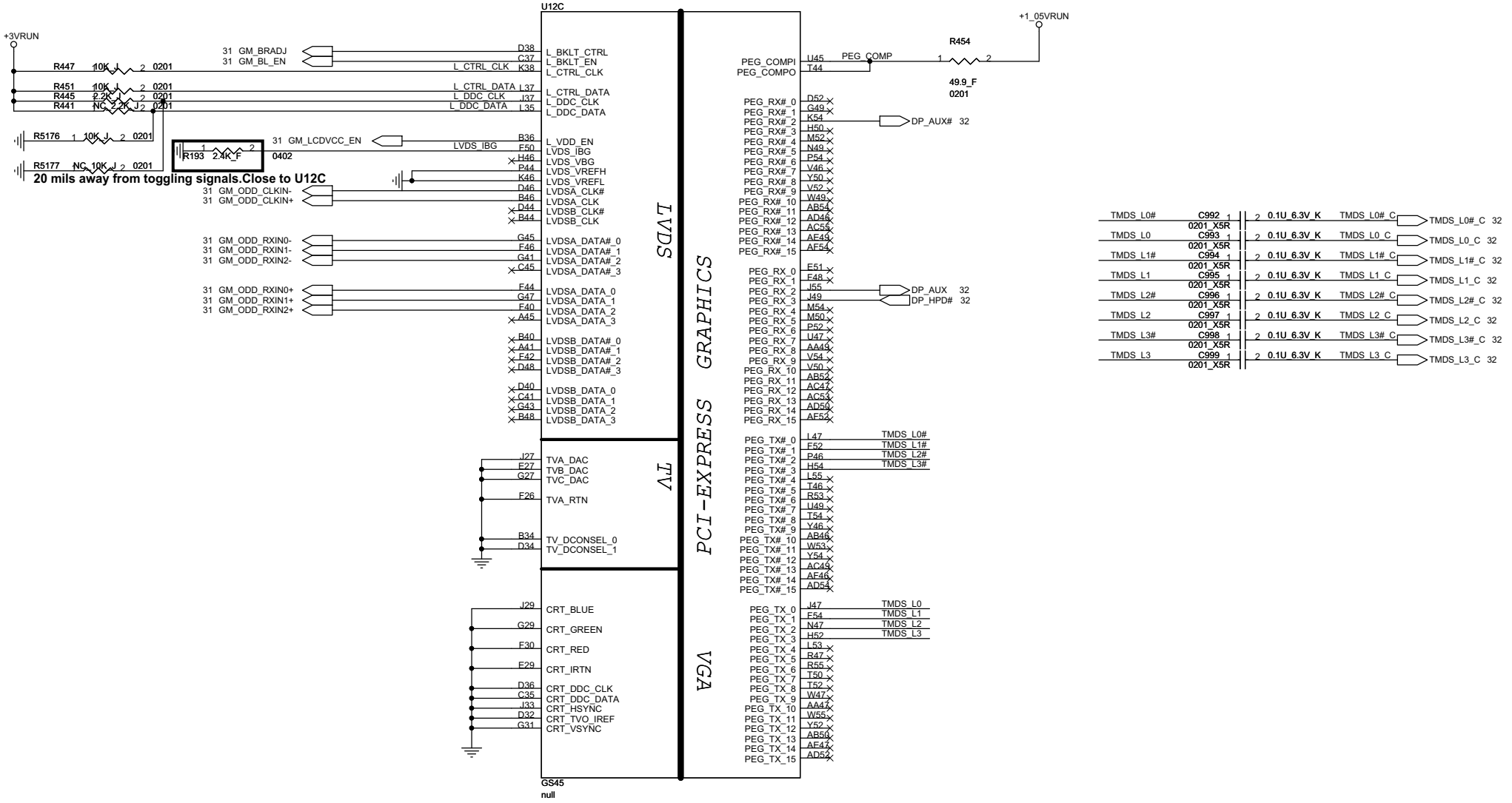
MCH_CFG_0~2 FSB Frequency	000 = FSB1066 ; 010 = FSB800; 011 = FSB667 ; Others = Reserved
MCH_CFG_3~4	Reserved
MCH_CFG_5 DMI X2 Select	Low = DMI X2 High = DMI X4 (Default)
MCH_CFG_6 ITPM Host Interface	Low =The ITPM Host Interface is enabled High = The ITPM Host Interface is disabled (default)
MCH_CFG_7 Intel Management Engine Crypto Strap	Low = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel Management Engine Crypto TLS cipher suite with confidentiality (default)
MCH_CFG_8	Reserved
MCH_CFG_9 PCIE Graphics Lane	Low = Lane Reversed High = Normal operation
MCH_CFG_10 PCIE Loopback enable	Low = Enabled High = Disabled (default)
MCH_CFG_11	Reserved
MCH_CFG_12 ALLZ	Low = ALLZ mode enabled High = Disabled (default)
MCH_CFG_13 XOR	Low = XOR mode enabled High = Disabled (default)
MCH_CFG_14~15	Reserved
MCH_CFG_16 FSB Dynamic ODT	Low = Dynamic ODT disabled High = Dynamic ODT enabled (default)
MCH_CFG_17~18	Reserved
MCH_CFG_19 DMI Lane Reversal	Low = Normal operation (Default): Lane Numbered in Order High = Reverse Lanes DMI x4 mode [(G)MCH->ICH]: (3->0, 2-> 1, 1->2 and 0->3) DMI x2 mode [(G)MCH ->ICH]: (3->0, 2->1)
MCH_CFG_20 Digital Display Port (SDVO/ DP/iHDMI) Concurrent with PCIe	Low = Only digital display port (SDVO/DP/iHDMI) or PCIe is operational (default) High = Digital display port (SDVO/DP/iHDMI) and PCIe are operating simultaneously via the PEG port



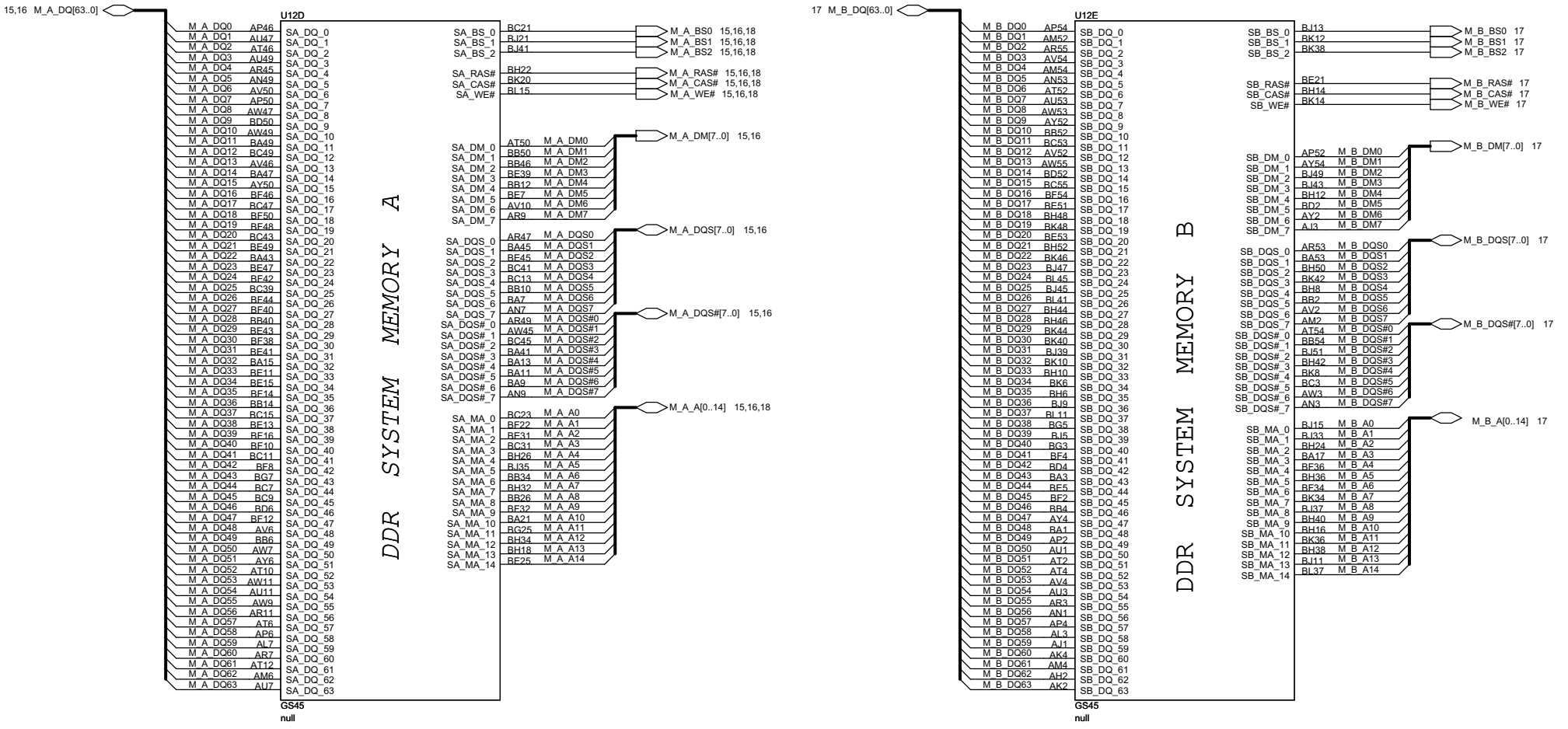
NOTES:
1. SDVO_CTRLCLK should be pulled up if SDVO_CTRLDATA is HIGH.
2. DDPC_CTRLCLK should be pulled up if DDPC_CTRLDATA is HIGH.
3. L_DDC_CLK should be pulled up if L_DDC_DATA is HIGH.

SDVO/HDMI/DP Configuration	Local Flat Panel (LFP) Present Strap L_DDC_DATA	DP/HDMI Present Strap DDPC_CTRLDATA	SDVO Present Strap SDVO_CTRLDATA	Digital Display Port/PCI Express Concurrent Strap CFG20
HDMI/DP Port B Enabled	Low	Low	High	Low

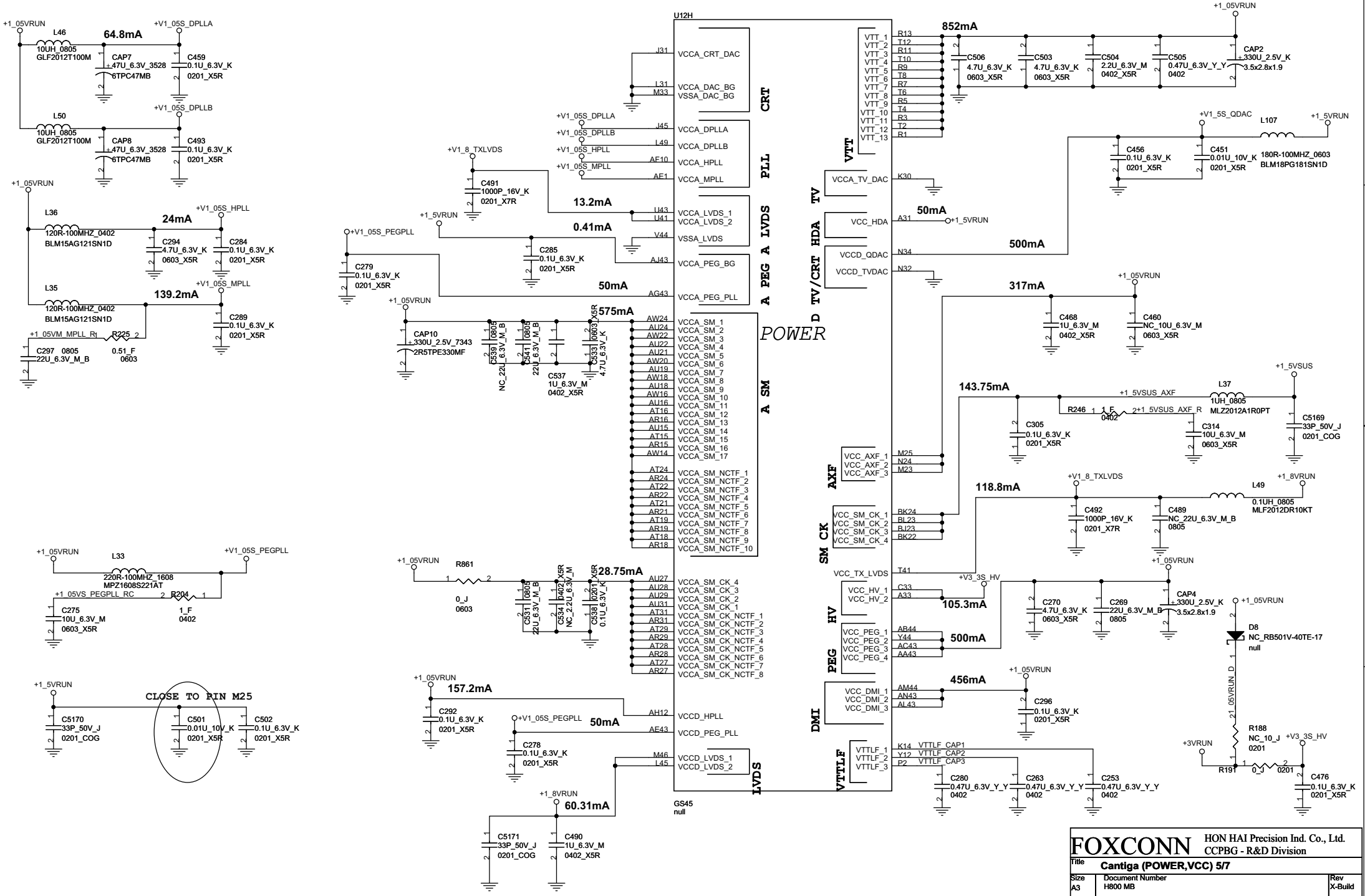
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title: Cantiga (DMI) 2/7			
Size: Custom	Document Number: H800 MB		Rev: X-Build
Date: Monday, October 12, 2009	Sheet 9 of 50		

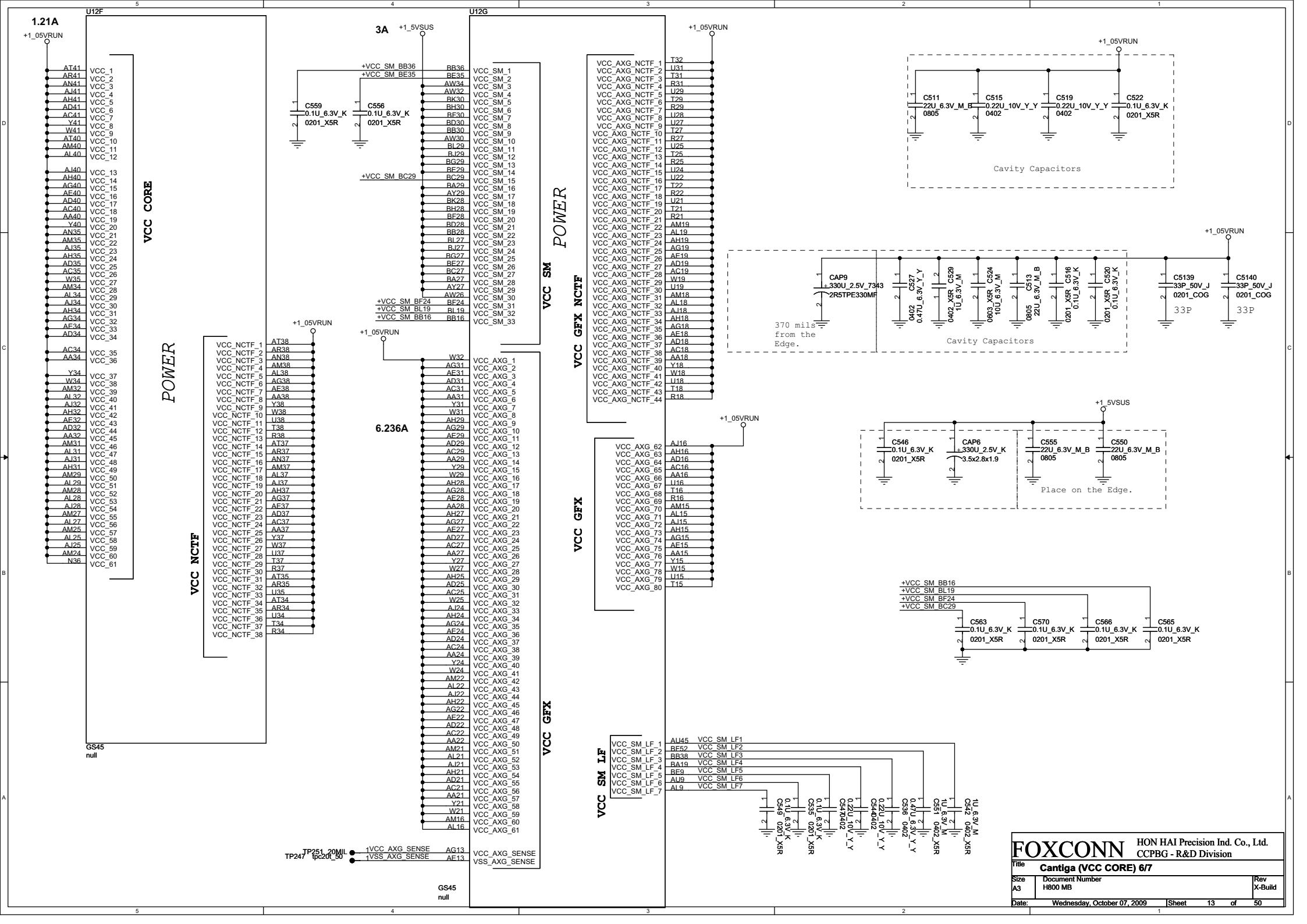


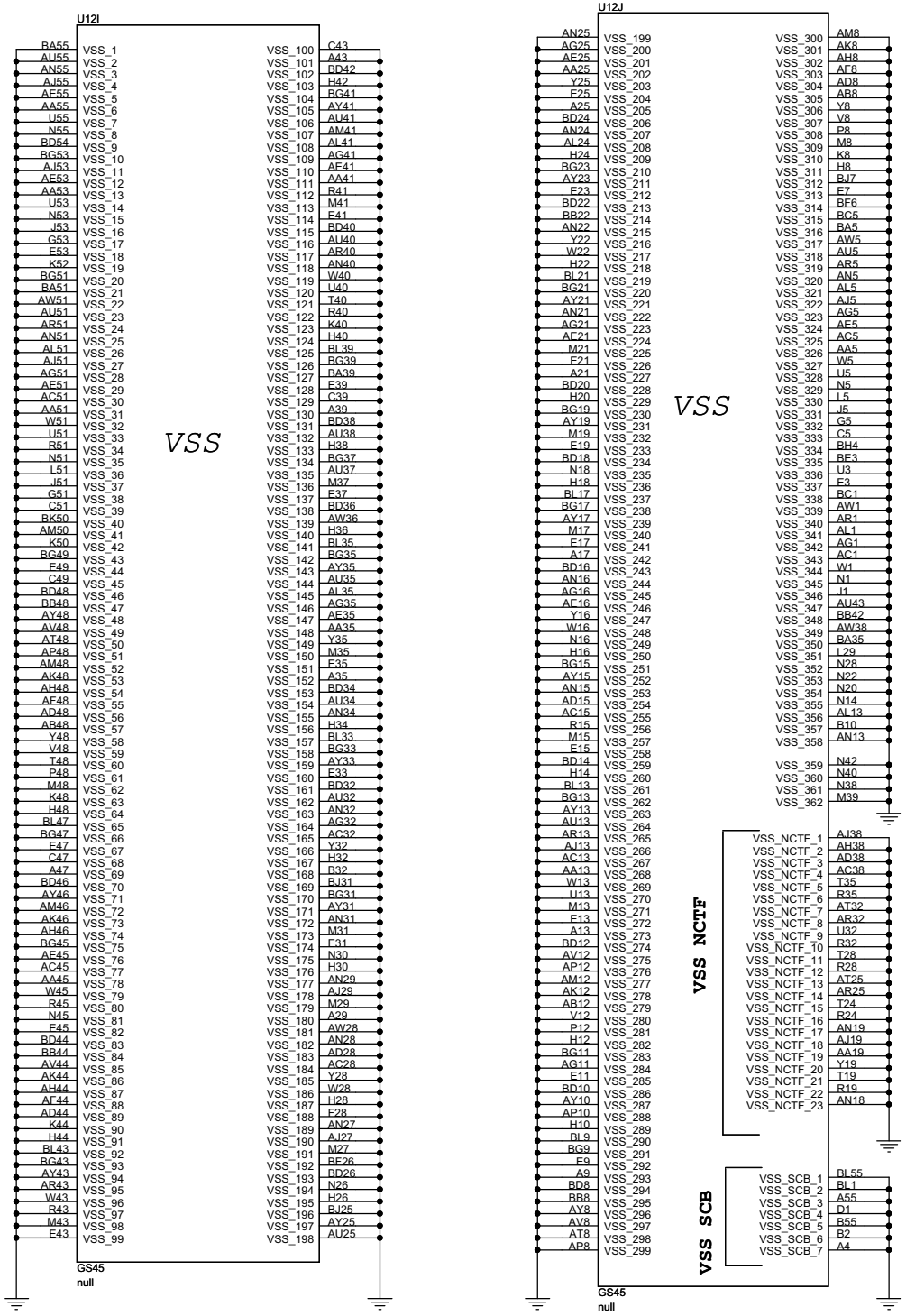
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Cantiga (GRAPHIC) 3/7	
Size A3	Document Number H800 MB	Rev X-Build
Date: Monday, October 12, 2009	Sheet 10 of 50	



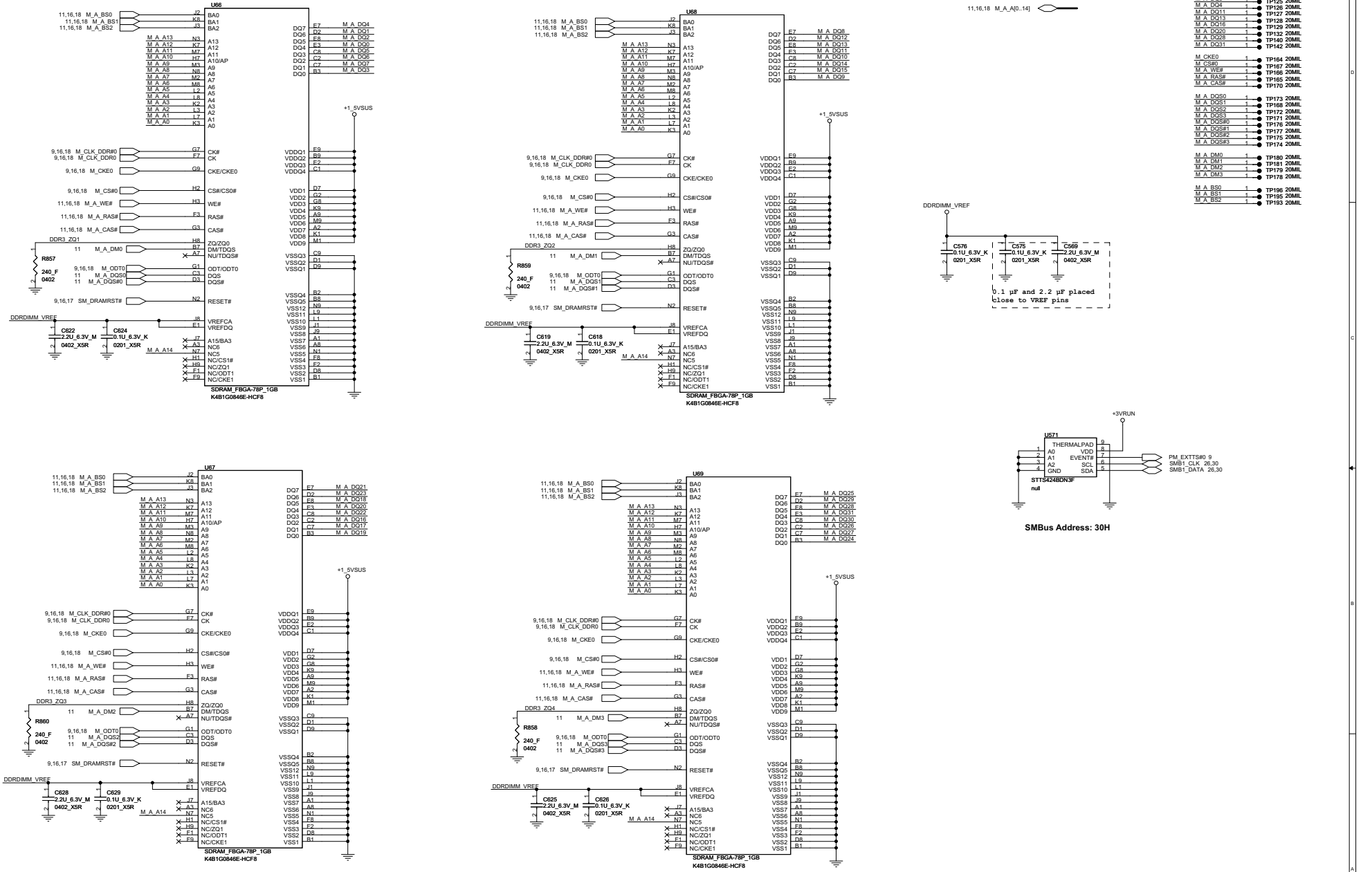
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Cantiga (DDRIII) 4/7	
Size A3	Document Number H800 MB	Rev X-Build
Date: Monday, October 12, 2009	Sheet 11 of 50	


U12H
POWER
CRT
PLL
A LVDS
A PEG
TV/CRT HDA
A SM
VTT
TV
HDA
AXF
SM CK
HV
PEG
DMI
VTTLF
LVDS
GS45
null
64.8mA
13.2mA
0.41mA
24mA
139.2mA
50mA
575mA
28.75mA
157.2mA
60.31mA
852mA
500mA
317mA
143.75mA
118.8mA
105.3mA
456mA
CLOSE TO PIN M25
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Cantiga (POWER,VCC) 5/7
Document Number
H800 MB
Rev
X-Build
Wednesday, October 07, 2009
Sheet 12 of 50

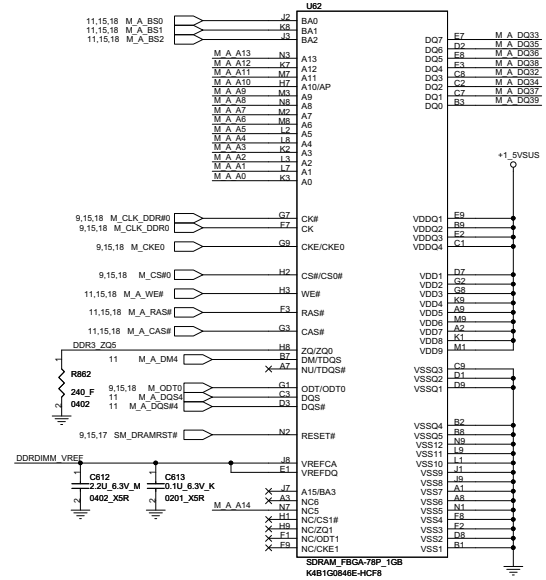

1.21A
U12F
+1_05VRUN
VCC CORE
POWER
VCC NCTF
GS45
null
3A
+1_5VSUS
+VCC_SM_BB36
+VCC_SM_BE35
+VCC_SM_BC29
+VCC_SM_BF24
+VCC_SM_BL19
+VCC_SM_BB16
C559 0.1U_6.3V_K 0201_X5R
C556 0.1U_6.3V_K 0201_X5R
U12G
VCC SM
POWER
6.236A
VCC GFX
TP251 20MIL
TP247 tpc20t_50
+VCC_AXG_SENSE
+VSS_AXG_SENSE
VCC_AXG_SENSE
VSS_AXG_SENSE
GS45
null
VCC GFX NCTF
VCC GFX
VCC SM LF
Cavity Capacitors
370 mils from the Edge.
Place on the Edge.
C511 22U_6.3V_M_B 0805
C515 0.22U_10V_Y_Y 0402
C519 0.22U_10V_Y_Y 0402
C522 0.1U_6.3V_K 0201_X5R
CAP9 +330U_2.5V_7343 2R5TPE330MF
C527 0402 0.47U_6.3V_Y_Y
C529 0402_X5R 1U_6.3V_M
C524 0603_X5R 10U_6.3V_M
C513 0805 22U_6.3V_M_B
C516 0201_X5R 0.1U_6.3V_K
C520 0201_X5R 0.1U_6.3V_K
C5139 33P_50V_J 0201_COG
C5140 33P_50V_J 0201_COG
33P
33P
CAP6 +330U_2.5V_K 3.5x2.8x1.9
C546 0.1U_6.3V_K 0201_X5R
C555 22U_6.3V_M_B 0805
C550 22U_6.3V_M_B 0805
C563 0.1U_6.3V_K 0201_X5R
C570 0.1U_6.3V_K 0201_X5R
C566 0.1U_6.3V_K 0201_X5R
C565 0.1U_6.3V_K 0201_X5R
C549 0.1U_6.3V_K 0201_X5R
C535 0.1U_6.3V_K 0201_X5R
C547 0.22U_10V_Y_Y 0402
C544 0.22U_10V_Y_Y 0402
C536 0.47U_6.3V_Y_Y 0402
C551 1U_6.3V_M 0402_X5R
C542 1U_6.3V_M 0402_X5R
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title: Cantiga (VCC CORE) 6/7
Size: A3
Document Number: H800 MB
Rev: X-Build
Date: Wednesday, October 07, 2009
Sheet 13 of 50

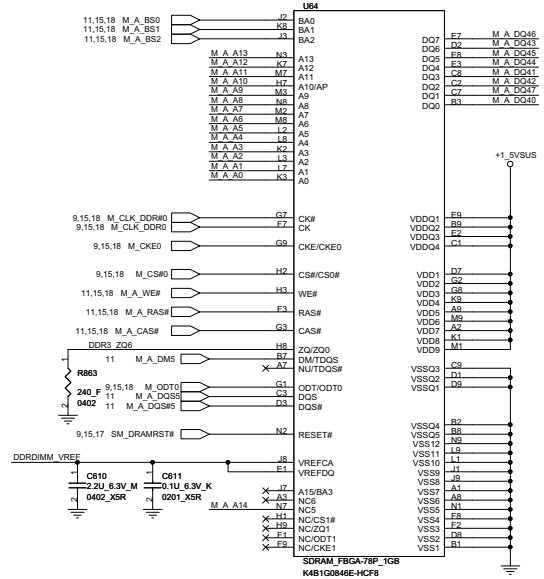


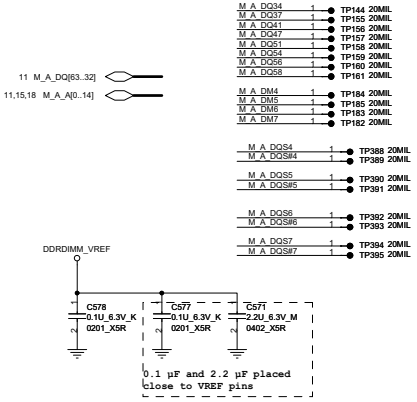
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Cantiga (VSS) 7/7	
Size A3	Document Number H800 MB	Rev X-Build
Date: Wednesday, October 07, 2009	Sheet 14 of 50	

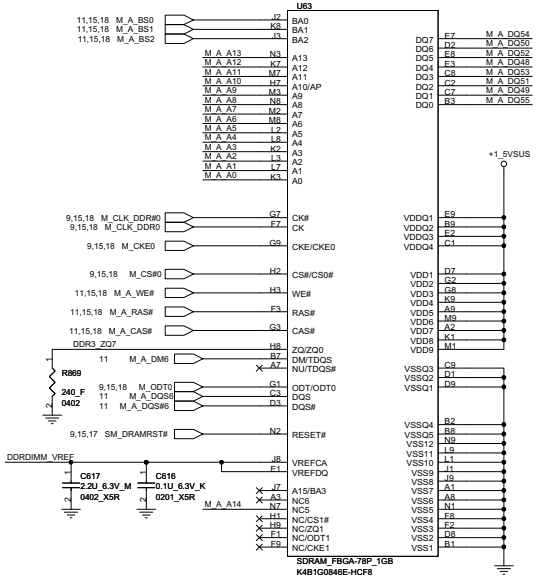


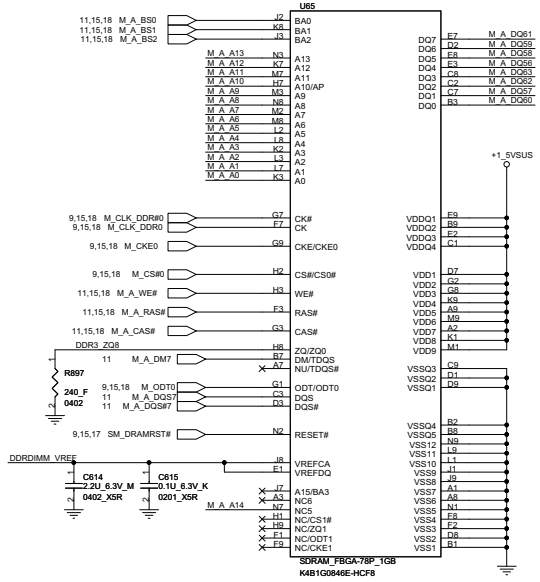
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	DDRIII MD 1/4		
Size A2	Document Number H800 MB		Rev X-Build
Date: Monday, October 12, 2009	Sheet 15 of 50		



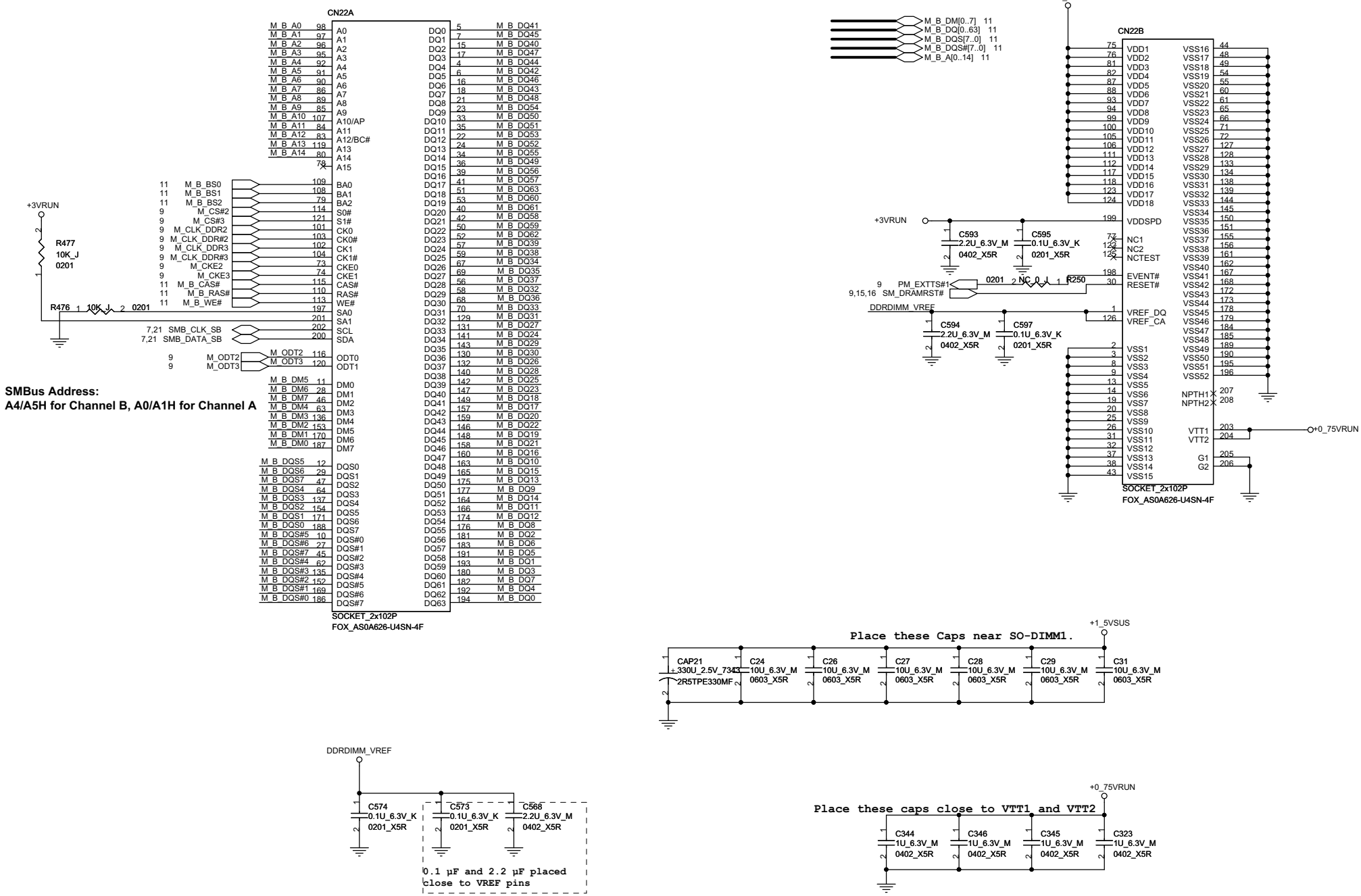








FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: DDRII MD 2/4		
Size: A2	Document Number: H800 MB	Rev: X-Build
Date: Monday, October 12, 2009	Sheet 16 of 50	



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	DDRIII (SO-DIMM) 3/4	
Size A3	Document Number H800 MB	Rev X-Build
Date: Monday, October 12, 2009	Sheet 17 of 50	

Place these caps close to MD

+1_5VSUS

CAP24 +330U_2.5V_K 3.5x2.8x1.9
C35 10U_6.3V_M 0603_X5R
C36 10U_6.3V_M 0603_X5R
C37 10U_6.3V_M 0603_X5R
C38 10U_6.3V_M 0603_X5R
C40 10U_6.3V_M 0603_X5R
C41 10U_6.3V_M 0603_X5R
C200 0.1U_6.3V_K 0201_X5R
C201 0.1U_6.3V_K 0201_X5R
C202 0.1U_6.3V_K 0201_X5R
C203 0.1U_6.3V_K 0201_X5R
C208 0.1U_6.3V_K 0201_X5R
C209 0.1U_6.3V_K 0201_X5R
C210 0.1U_6.3V_K 0201_X5R
C211 0.1U_6.3V_K 0201_X5R
C5141 33P_50V_J 0201_COG
C5142 33P_50V_J 0201_COG

+1_5VSUS

C351 1U_6.3V_M 0402_X5R
C352 1U_6.3V_M 0402_X5R
C350 1U_6.3V_M 0402_X5R
C325 1U_6.3V_M 0402_X5R
C348 1U_6.3V_M 0402_X5R
C349 1U_6.3V_M 0402_X5R
C347 1U_6.3V_M 0402_X5R
C324 1U_6.3V_M 0402_X5R
C204 0.1U_6.3V_K 0201_X5R
C205 0.1U_6.3V_K 0201_X5R
C206 0.1U_6.3V_K 0201_X5R
C207 0.1U_6.3V_K 0201_X5R
C212 0.1U_6.3V_K 0201_X5R
C213 0.1U_6.3V_K 0201_X5R
C214 0.1U_6.3V_K 0201_X5R
C215 0.1U_6.3V_K 0201_X5R
C5143 33P_50V_J 0201_COG
C5144 33P_50V_J 0201_COG

+0_75VRUN

C354 1U_6.3V_M 0402_X5R
C355 1U_6.3V_M 0402_X5R
C353 1U_6.3V_M 0402_X5R
C326 1U_6.3V_M 0402_X5R

M_A_A[0..14] 11,15,16

9,15,16 M_CLK_DDR0
R872 30.1_F 0402
C356 3.3P_50V_C 0402_NPO
M_CLK_DDR0_TERM
R873 30.1_F 0402
C255 0.1U_6.3V_K 0201_X5R
9,15,16 M_CLK_DDR#0

+0_75VRUN

RP43
11,15,16 M_A_BS0
M_A_A0
M_A_BS0
M_A_A7
M_A_A3
36
0201_8P4R

RP45
9,15,16 M_CS#0
9,15,16 M_ODT0
11,15,16 M_A_WE#
M_CS#0
M_ODT0
M_A_WE#
M_A_A13
36
0201_8P4R

RP46
11,15,16 M_A_CAS#
11,15,16 M_A_RAS#
M_A_A5
M_A_A9
M_A_CAS#
M_A_RAS#
36
0201_8P4R

+0_75VRUN

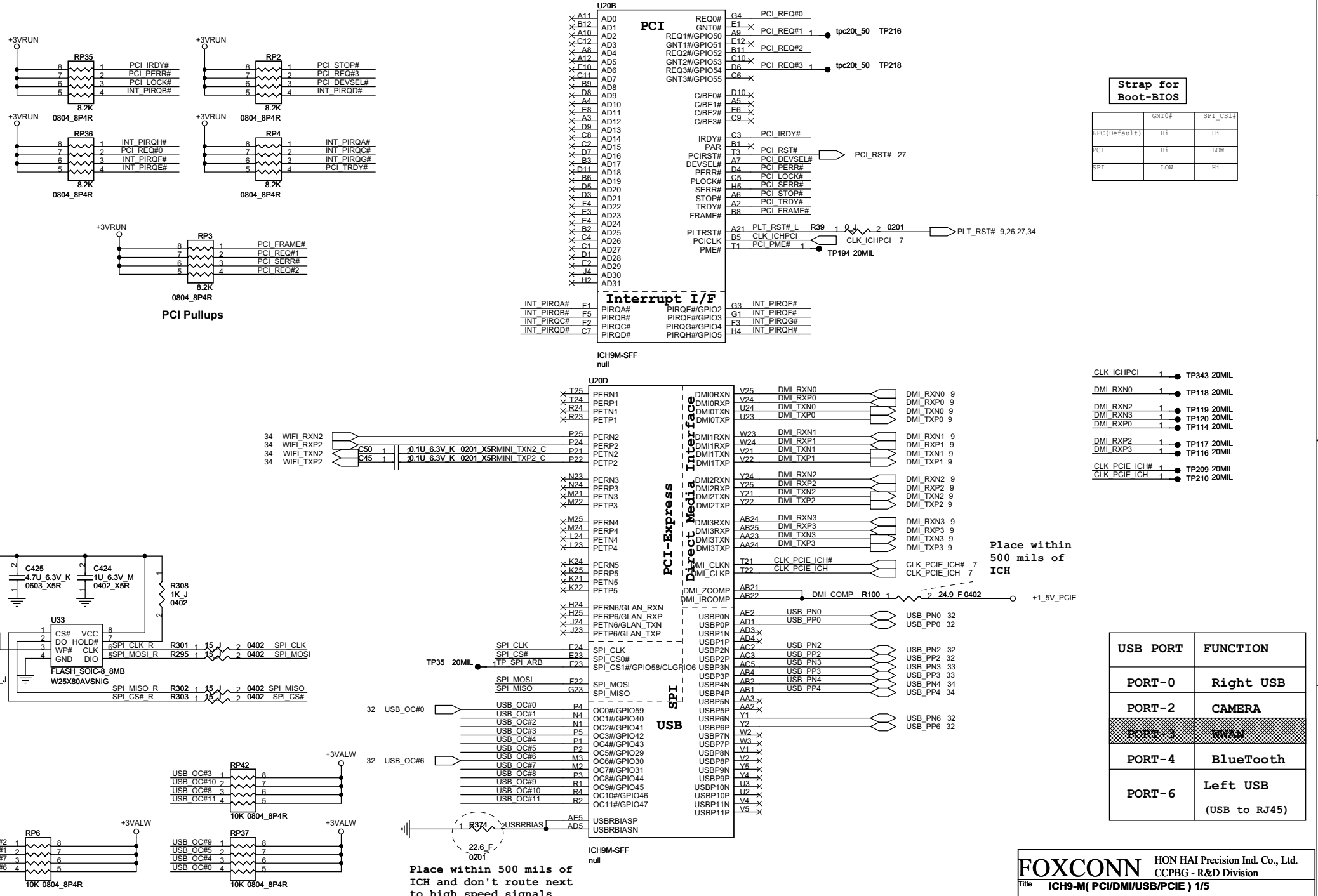
RP47
11,15,16 M_A_BS1
M_A_A11
M_A_BS1
M_A_A14
M_A_A8
36
0201_8P4R

RP48
9,15,16 M_CKE0
M_A_A4
M_A_A10
M_CKE0
M_A_A6
36
0201_8P4R

RP49
11,15,16 M_A_BS2
M_A_BS2
M_A_A2
M_A_A12
M_A_A1
36
0201_8P4R

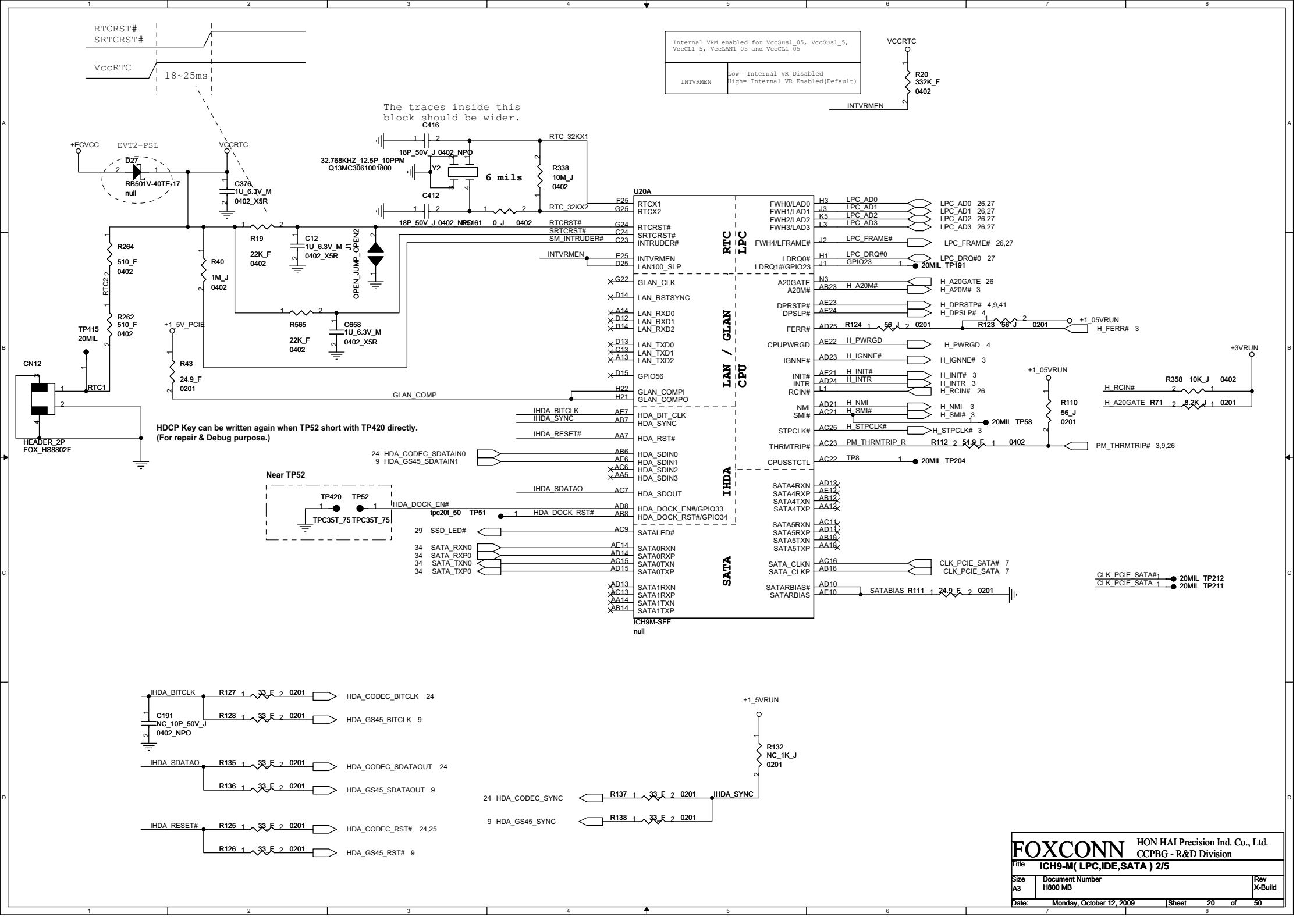
FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	DDR(III)Termination 4/4	
Size A3	Document Number H800 MB	Rev X-Build
Date: Monday, October 12, 2009	Sheet 18 of 50	

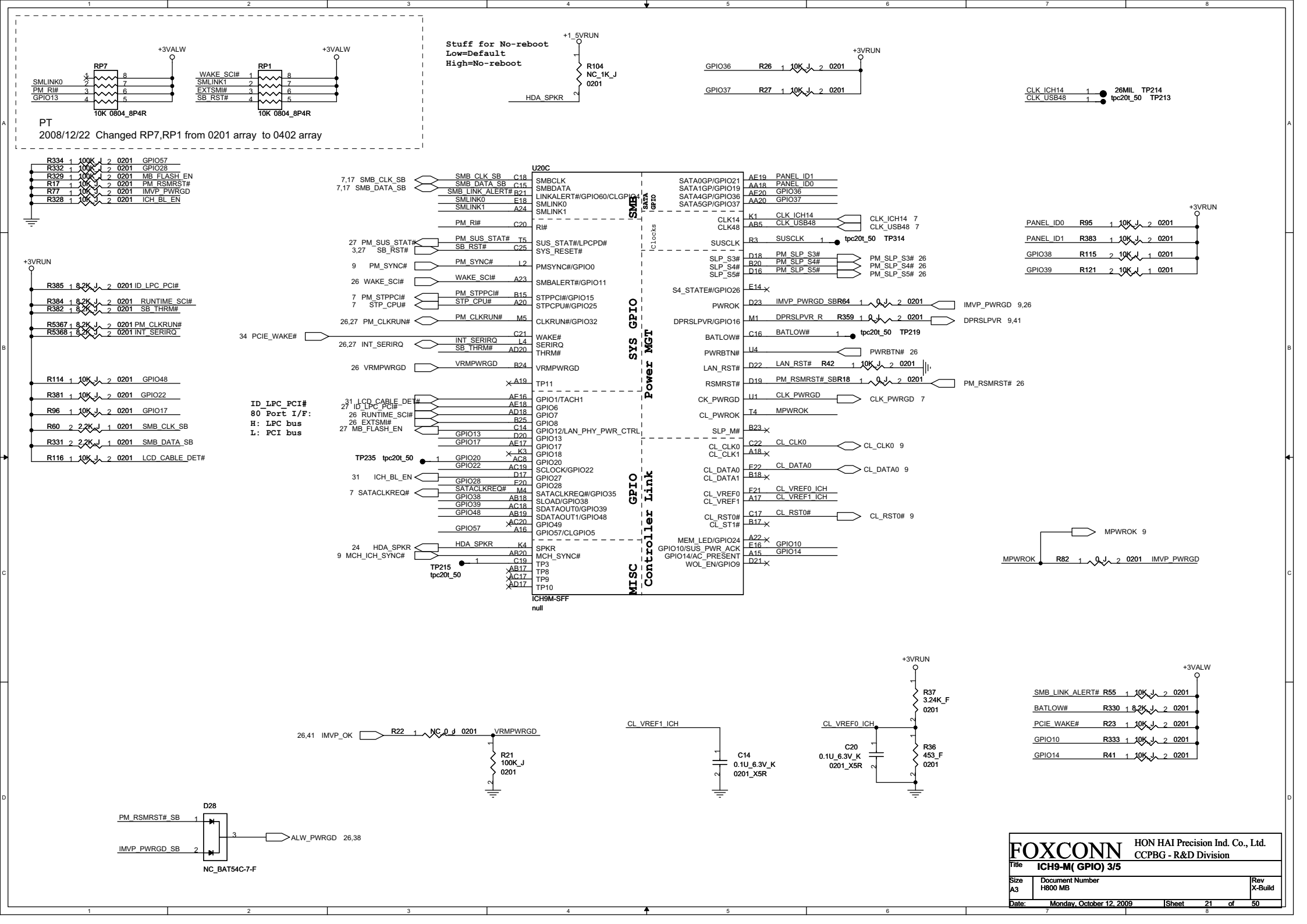


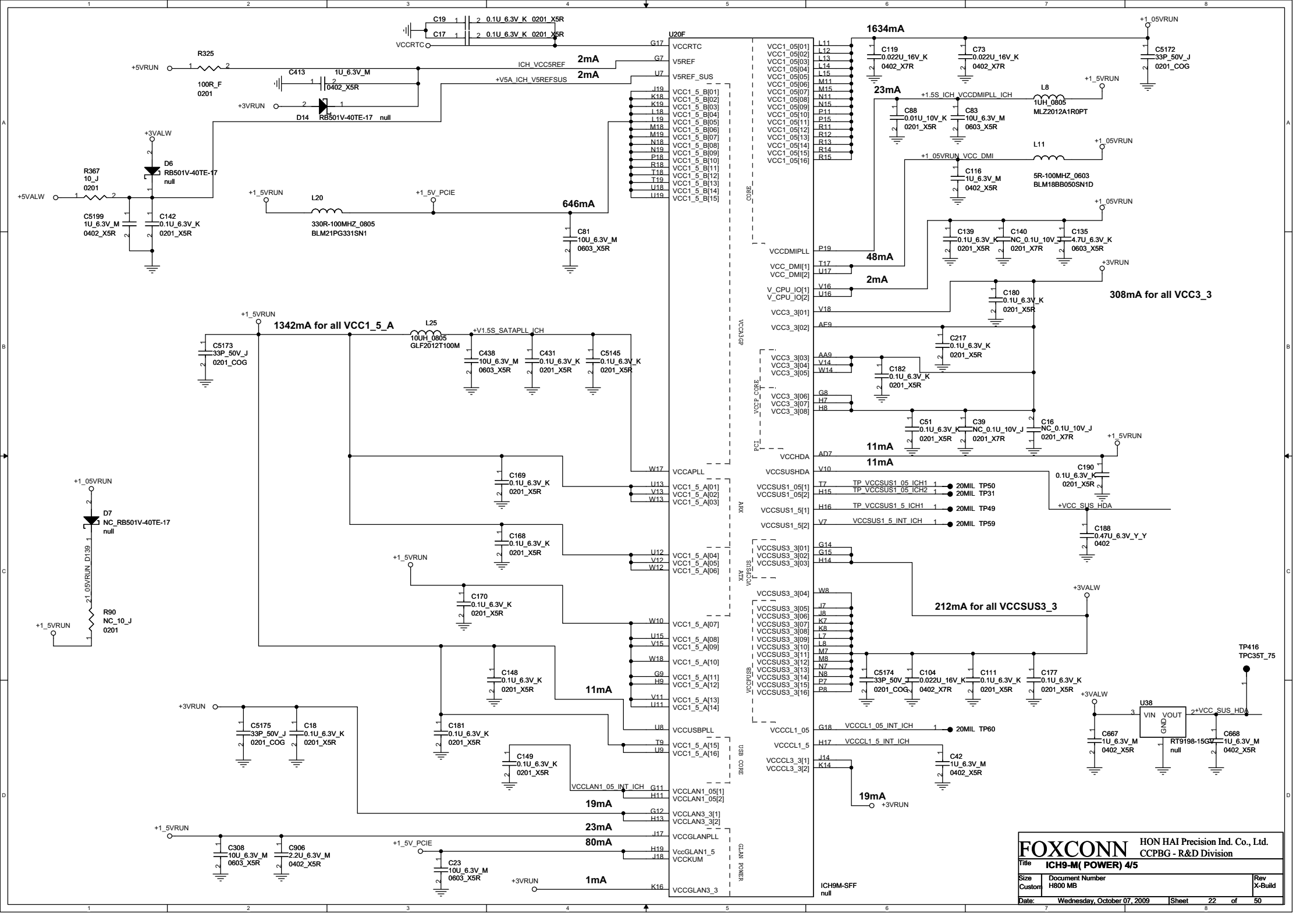
Title	ICH9-M(PCI/DMI/USB/PCIE) 1/5
Size	A3
Document Number	H800 MB
Rev	X-Build
Date:	Monday, October 12, 2009
Sheet	19 of 50

FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division



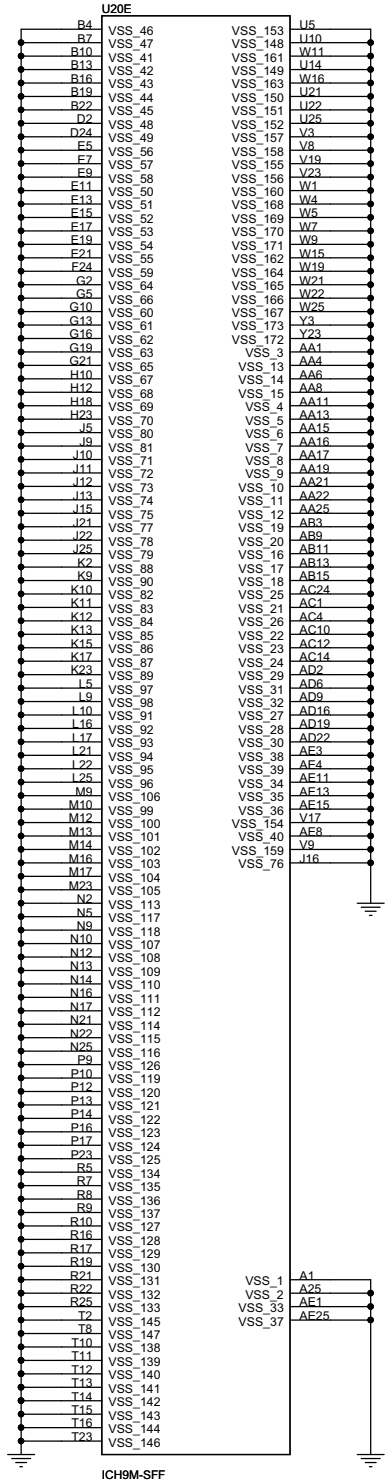
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	ICH9-M(LPC,IDE,SATA) 2/5	
Size A3	Document Number H800 MB	Rev X-Build
Date: Monday, October 12, 2009	Sheet 20 of 50	


RP7
+3VALW
SMLINK0
PM_RI#
GPIO13
10K 0804_8P4R
RP1
WAKE_SCI#
SMLINK1
EXTSMI#
SB_RST#
PT
2008/12/22 Changed RP7,RP1 from 0201 array to 0402 array
Stuff for No-reboot
Low=Default
High=No-reboot
+1_5VRUN
R104
NC_1K_J
0201
HDA_SPKR
+3VRUN
GPIO36
GPIO37
R26
R27
CLK_ICH14
CLK_USB48
26MIL TP214
tpc20t_50 TP213
R334 100K_J 0201 GPIO57
R332 100K_J 0201 GPIO28
R329 100K_J 0201 MB_FLASH_EN
R17 10K_J 0201 PM_RSMRST#
R77 10K_J 0201 IMVP_PWRGD
R328 10K_J 0201 ICH_BL_EN
R385 8.2K_J 0201 ID_LPC_PCI#
R384 8.2K_J 0201 RUNTIME_SCI#
R382 8.2K_J 0201 SB_THRM#
R5367 8.2K_J 0201 PM_CLKRUN#
R5368 8.2K_J 0201 INT_SERIRQ
R114 10K_J 0201 GPIO48
R381 10K_J 0201 GPIO22
R96 10K_J 0201 GPIO17
R60 2.2K_J 0201 SMB_CLK_SB
R331 2.2K_J 0201 SMB_DATA_SB
R116 10K_J 0201 LCD_CABLE_DET#
ID_LPC_PCI#
80 Port I/F:
H: LPC bus
L: PCI bus
U20C
SMBCLK
SMBDATA
LINKALERT#/GPIO60/CLGPIO4
SMLINK0
SMLINK1
RI#
SUS_STAT#/LPCPD#
SYS_RESET#
PMSYNC#/GPIO0
SMBALERT#/GPIO11
STPPCI#/GPIO15
STPCPU#/GPIO25
CLKRUN#/GPIO32
WAKE#
SERIRQ
THRM#
VRMPWRGD
TP11
GPIO1/TACH1
GPIO6
GPIO7
GPIO8
GPIO12/LAN_PHY_PWR_CTRL
GPIO13
GPIO17
GPIO18
GPIO20
SCLOCK/GPIO22
GPIO27
GPIO28
SATACLKREQ#/GPIO35
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
GPIO49
GPIO57/CLGPIO5
SPKR
MCH_SYNC#
TP3
TP8
TP9
TP10
SMB
SATA GPIO
Clocks
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
ICH9M-SFF
null
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA4GP/GPIO36
SATA5GP/GPIO37
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
S4_STATE#/GPIO26
PWROK
DPRSLPVR/GPIO16
BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
CK_PWRGD
CL_PWROK
SLP_M#
CL_CLK0
CL_CLK1
CL_DATA0
CL_DATA1
CL_VREF0
CL_VREF1
CL_RST0#
CL_ST1#
MEM_LED/GPIO24
GPIO10/SUS_PWR_ACK
GPIO14/AC_PRESENT
WOL_EN/GPIO9
PANEL_ID1
PANEL_ID0
GPIO36
GPIO37
CLK_ICH14
CLK_USB48
TP314
PM_SLP_S3#
PM_SLP_S4#
PM_SLP_S5#
IMVP_PWRGD_SB
R64
IMVP_PWRGD 9,26
DPRSLPVR_R
R359
DPRSLPVR 9,41
TP219
PWRBTN# 26
R42
PM_RSMRST#_SB
R18
PM_RSMRST# 26
CLK_PWRGD 7
MPWROK
CL_CLK0
CL_CLK0 9
CL_DATA0
CL_DATA0 9
CL_VREF0_ICH
CL_VREF1_ICH
CL_RST0#
CL_RST0# 9
GPIO10
GPIO14
TP235 tpc20t_50
TP215 tpc20t_50
ICH_BL_EN
SATACLKREQ#
HDA_SPKR
MCH_ICH_SYNC#
PCIE_WAKE#
INT_SERIRQ
SB_THRM#
VRMPWRGD
PM_CLKRUN#
PM_SYNC#
WAKE_SCI#
PM_STPPCI#
STP_CPU#
PM_SUS_STAT#
SB_RST#
LCD_CABLE_DET#
RUNTIME_SCI#
EXTSMI#
MB_FLASH_EN
+3VRUN
PANEL_ID0 R95 10K_J 0201
PANEL_ID1 R383 10K_J 0201
GPIO38 R115 10K_J 0201
GPIO39 R121 10K_J 0201
MPWROK 9
MPWROK R82 0_J 0201 IMVP_PWRGD
+3VALW
SMB_LINK_ALERT# R55 10K_J 0201
BATLOW# R330 8.2K_J 0201
PCIE_WAKE# R23 10K_J 0201
GPIO10 R333 10K_J 0201
GPIO14 R41 10K_J 0201
26,41 IMVP_OK
R22 NC_0_J 0201
VRMPWRGD
R21 100K_J 0201
CL_VREF1_ICH
C14 0.1U_6.3V_K 0201_X5R
CL_VREF0_ICH
C20 0.1U_6.3V_K 0201_X5R
R37 3.24K_F 0201
R36 453_F 0201
D28
PM_RSMRST#_SB
IMVP_PWRGD_SB
ALW_PWRGD 26,38
NC_BAT54C-7-F
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title ICH9-M(GPIO) 3/5
Size A3
Document Number H800 MB
Rev X-Build
Date: Monday, October 12, 2009
Sheet 21 of 50

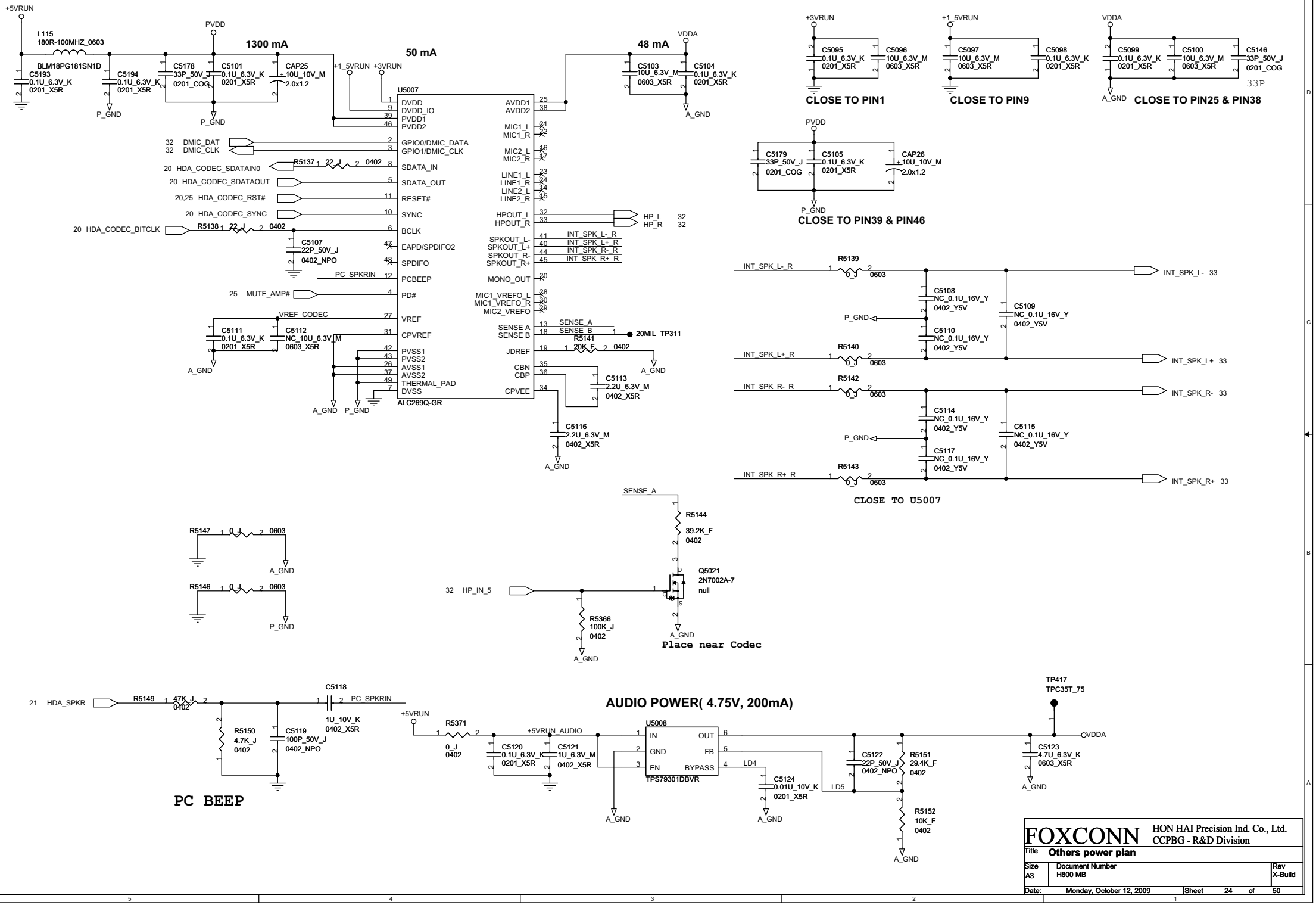


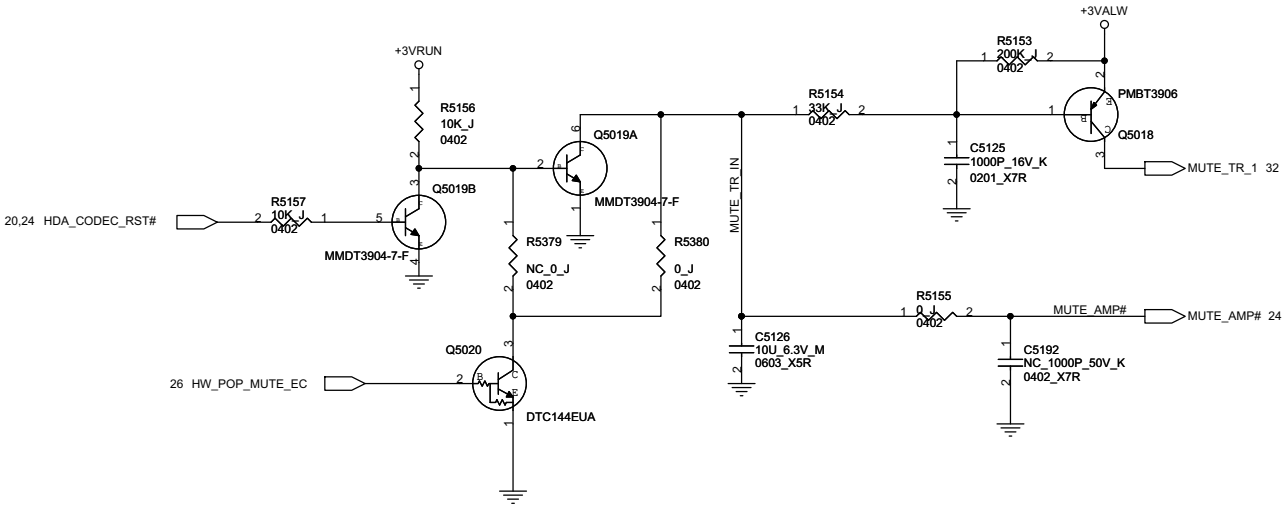
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	ICH9-M(POWER) 4/5	
Size: Custom	Document Number: H800 MB	Rev: X-Build
Date: Wednesday, October 07, 2009	Sheet 22 of 50	

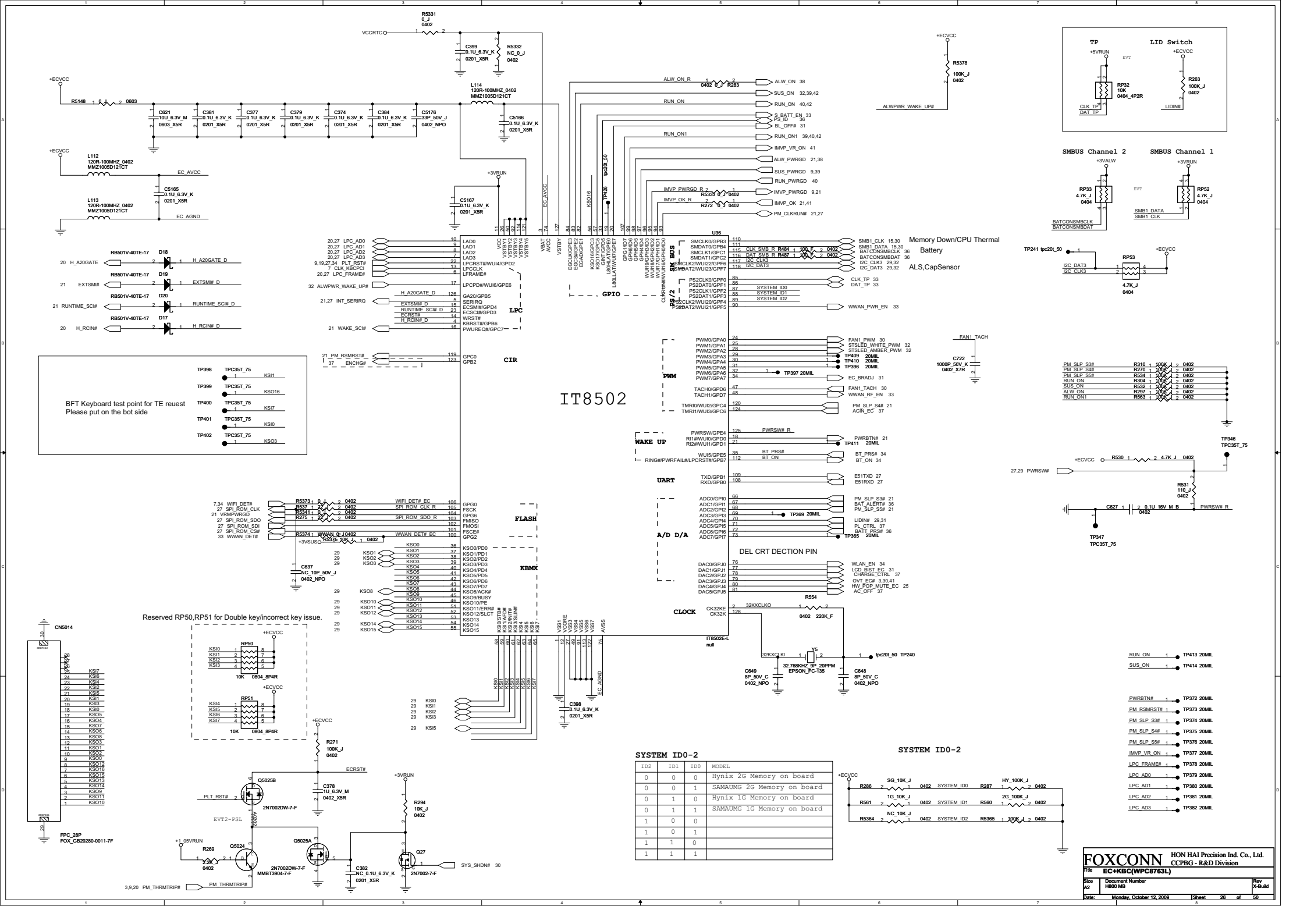


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	ICH9-M(GND) 5/5	
Size A3	Document Number H800 MB	Rev X-Build
Date: Wednesday, October 07, 2009	Sheet 23 of 50	

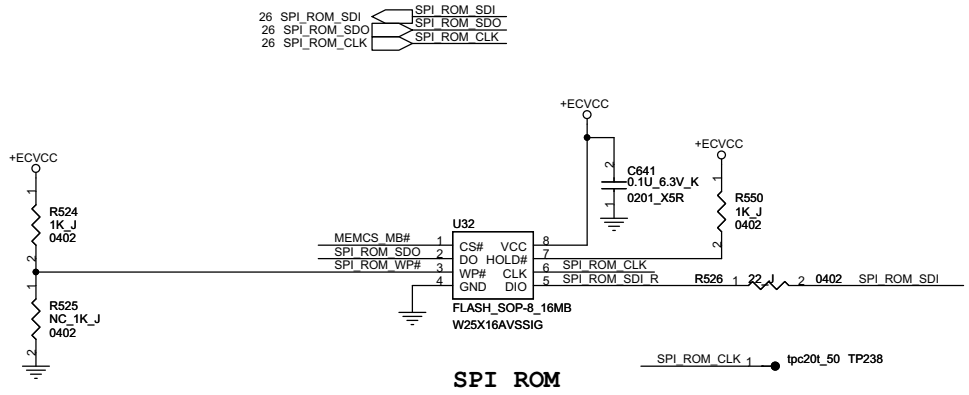

+5VRUN
L115
180R-100MHZ_0603
BLM18PG181SN1D
C5193 0.1U_6.3V_K 0201_X5R
C5194 0.1U_6.3V_K 0201_X5R
P_GND
PVDD
1300 mA
C5178 33P_50V_J 0201_COG
C5101 0.1U_6.3V_K 0201_X5R
CAP25 +10U_10V_M 2.0x1.2
P_GND
+1_5VRUN +3VRUN
50 mA
U5007
DVDD
DVDD_IO
PVDD1
PVDD2
GPIO0/DMIC_DATA
GPIO1/DMIC_CLK
SDATA_IN
SDATA_OUT
RESET#
SYNC
BCLK
EAPD/SPDIFO2
SPDIFO
PCBEEP
PD#
VREF
CPVREF
PVSS1
PVSS2
AVSS1
AVSS2
THERMAL_PAD
DVSS
ALC269Q-GR
32 DMIC_DAT
32 DMIC_CLK
20 HDA_CODEC_SDATAIN0
R5137 22_J 0402
20 HDA_CODEC_SDATAOUT
20,25 HDA_CODEC_RST#
20 HDA_CODEC_SYNC
20 HDA_CODEC_BITCLK
R5138 22_J 0402
C5107 22P_50V_J 0402_NPO
PC_SPKRIN
25 MUTE_AMP#
VREF_CODEC
C5111 0.1U_6.3V_K 0201_X5R
C5112 NC_10U_6.3V_M 0603_X5R
A_GND
P_GND
48 mA
VDDA
C5103 10U_6.3V_M 0603_X5R
C5104 0.1U_6.3V_K 0201_X5R
A_GND
AVDD1
AVDD2
MIC1_L
MIC1_R
MIC2_L
MIC2_R
LINE1_L
LINE1_R
LINE2_L
LINE2_R
HPOUT_L
HPOUT_R
HP_L 32
HP_R 32
SPKOUT_L-
SPKOUT_L+
SPKOUT_R-
SPKOUT_R+
INT_SPK_L- R
INT_SPK_L+ R
INT_SPK_R- R
INT_SPK_R+ R
MONO_OUT
MIC1_VREFO_L
MIC1_VREFO_R
MIC2_VREFO
SENSE A
SENSE B
20MIL TP311
R5141 20K_F 0402
JDREF
CBN
CBP
CPVEE
C5113 2.2U_6.3V_M 0402_X5R
C5116 2.2U_6.3V_M 0402_X5R
A_GND
+3VRUN
C5095 0.1U_6.3V_K 0201_X5R
C5096 10U_6.3V_M 0603_X5R
CLOSE TO PIN1
+1_5VRUN
C5097 10U_6.3V_M 0603_X5R
C5098 0.1U_6.3V_K 0201_X5R
CLOSE TO PIN9
VDDA
C5099 0.1U_6.3V_K 0201_X5R
C5100 10U_6.3V_M 0603_X5R
C5146 33P_50V_J 0201_COG
33P
A_GND
CLOSE TO PIN25 & PIN38
PVDD
C5179 33P_50V_J 0201_COG
C5105 0.1U_6.3V_K 0201_X5R
CAP26 +10U_10V_M 2.0x1.2
P_GND
CLOSE TO PIN39 & PIN46
INT_SPK_L- R
R5139 0_J 0603
INT_SPK_L- 33
C5108 NC_0.1U_16V_Y 0402_Y5V
C5109 NC_0.1U_16V_Y 0402_Y5V
C5110 NC_0.1U_16V_Y 0402_Y5V
P_GND
INT_SPK_L+ R
R5140 0_J 0603
INT_SPK_L+ 33
INT_SPK_R- R
R5142 0_J 0603
INT_SPK_R- 33
C5114 NC_0.1U_16V_Y 0402_Y5V
C5115 NC_0.1U_16V_Y 0402_Y5V
C5117 NC_0.1U_16V_Y 0402_Y5V
P_GND
INT_SPK_R+ R
R5143 0_J 0603
INT_SPK_R+ 33
CLOSE TO U5007
R5147 0_J 0603
A_GND
R5146 0_J 0603
P_GND
SENSE_A
R5144 39.2K_F 0402
32 HP_IN_5
Q5021 2N7002A-7 null
R5366 100K_J 0402
A_GND
Place near Codec
21 HDA_SPKR
R5149 47K_J 0402
C5118 1U_10V_K 0402_X5R
PC_SPKRIN
R5150 4.7K_J 0402
C5119 100P_50V_J 0402_NPO
PC BEEP
AUDIO POWER(4.75V, 200mA)
+5VRUN
R5371 0_J 0402
+5VRUN_AUDIO
C5120 0.1U_6.3V_K 0201_X5R
C5121 1U_6.3V_M 0402_X5R
U5008
IN
GND
EN
OUT
FB
BYPASS
TPS79301DBVR
LD4
LD5
C5124 0.01U_10V_K 0201_X5R
C5122 22P_50V_J 0402_NPO
R5151 29.4K_F 0402
R5152 10K_F 0402
TP417 TPC35T_75
OVDDA
C5123 4.7U_6.3V_K 0603_X5R
A_GND
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title Others power plan
Size A3
Document Number H800 MB
Rev X-Build
Date: Monday, October 12, 2009
Sheet 24 of 50



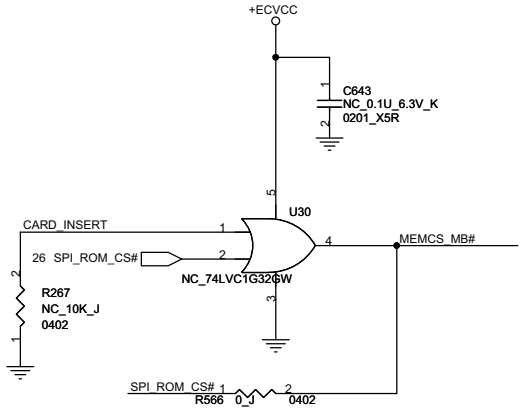
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	**Others power plan**	
Size A3	Document Number H800 MB	Rev X-Build
Date: Monday, October 12, 2009	Sheet 25 of 50	



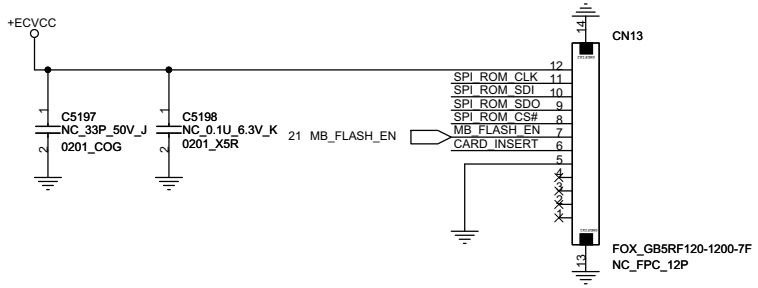
ID2	ID1	ID0	MODEL
0	0	0	Hynix 2G Memory on board
0	0	1	SAMAUMG 2G Memory on board
0	1	0	Hynix 1G Memory on board
0	1	1	SAMAUMG 1G Memory on board
1	0	0	
1	0	1	
1	1	0	
1	1	1	



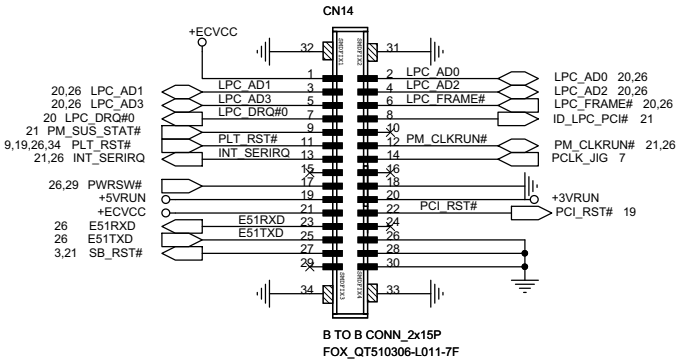
SPI ROM



X-Build 2009.10.12
Disabled external SPI ROM boot function and changed part value as below.
From Mount to NC : U30,C643,R267,CN13
From NC to Mount : R566



EXTERNAL SPI ROM INTERFACE



JIG-120

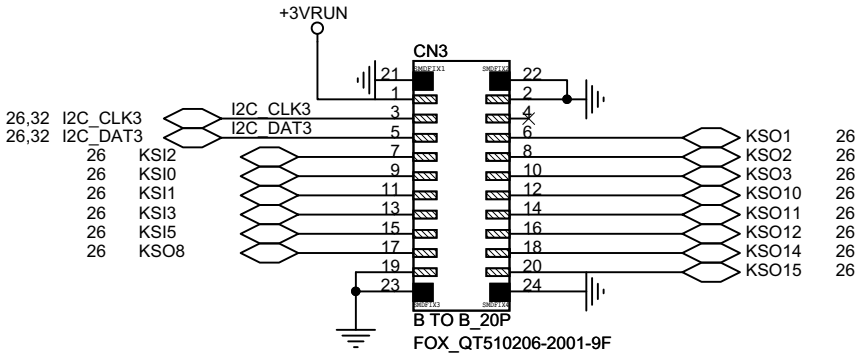
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	SPI ROM/DEBUG PORT	
Size A3	Document Number H800 MB	Rev X-Build
Date: Monday, October 12, 2009	Sheet 27 of 50	

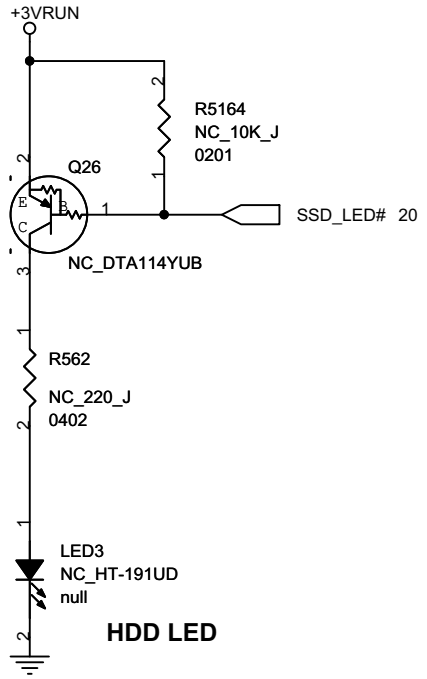
PT

Removed on board key pad design

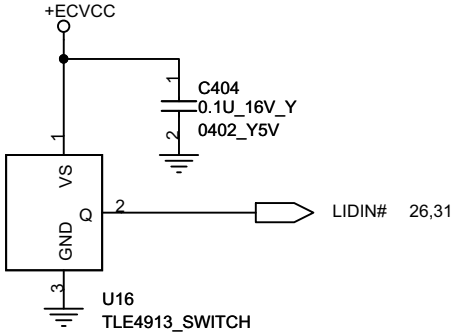
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: KB MATRIS(DELETED)		
Size: A2	Document Number: H800 MB	Rev: X-Build
Date: Wednesday, October 07, 2009	Sheet 28 of 50	

FUNCTION KEY CONN

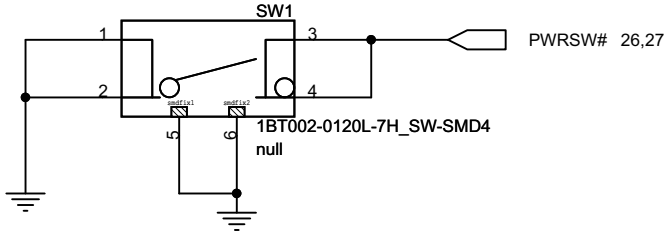




HDD LED

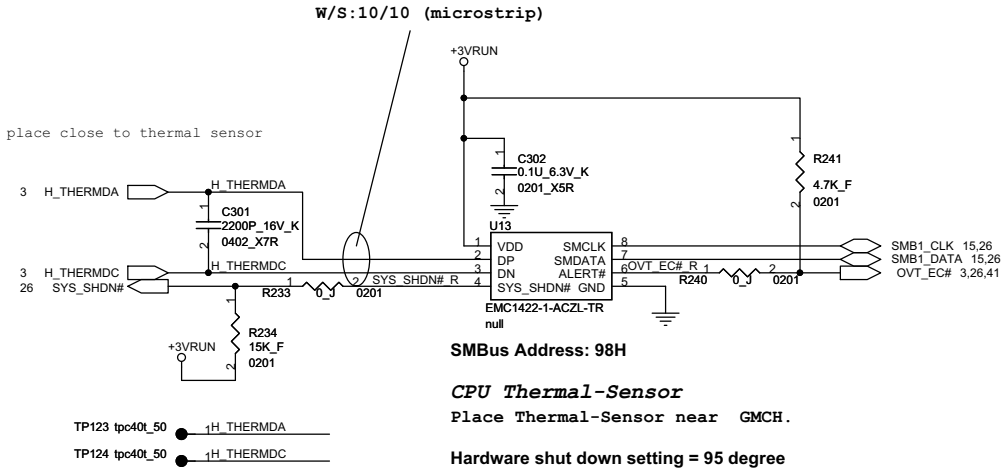


LID SWITCH



POWER BOTTON

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PWR BTN/FK/ALS/LID SW	
Size A4	Document Number H800 MB	Rev X-Build
Date: Monday, October 12, 2009	Sheet 29 of 50	

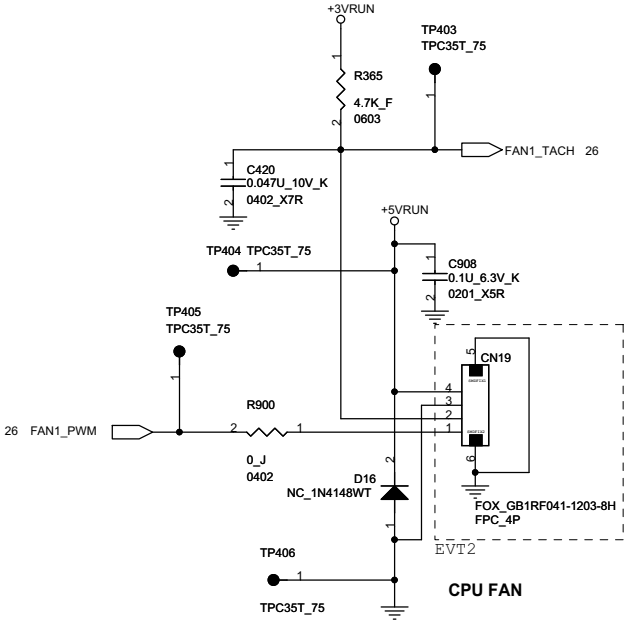


SMBus Address: 98H

CPU Thermal-Sensor

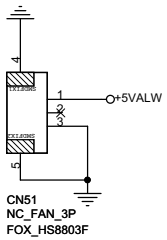
Place Thermal-Sensor near GMCH.

Hardware shut down setting = 95 degree



TP403~TP406 BFT FAN test point for TE request
Please put on the bot side

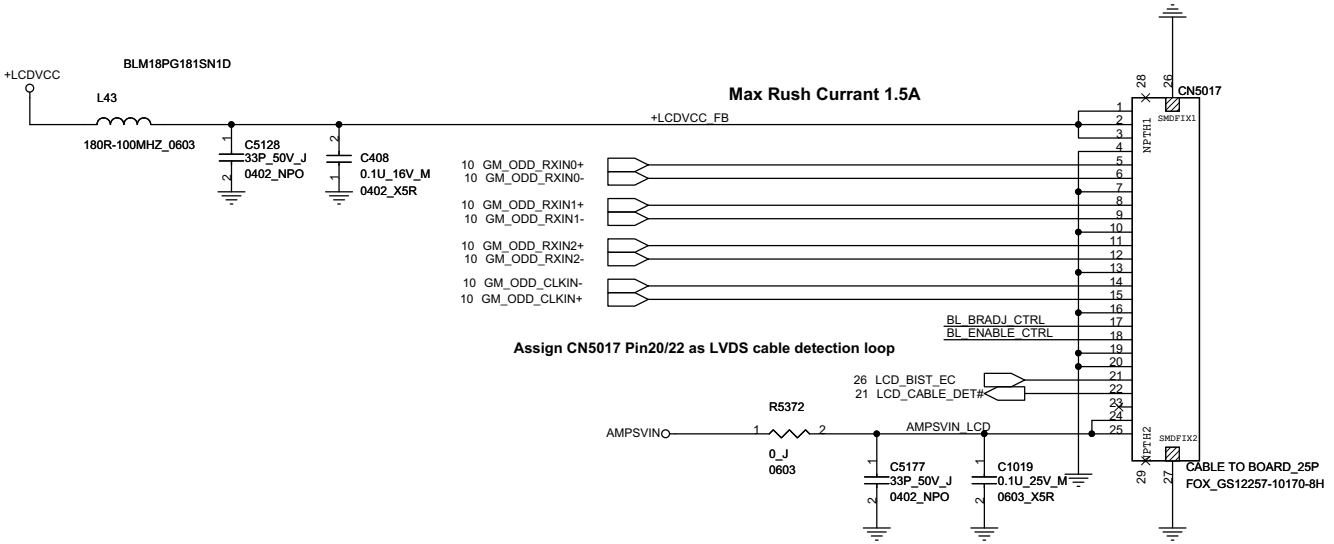
CN51 for test FAN power



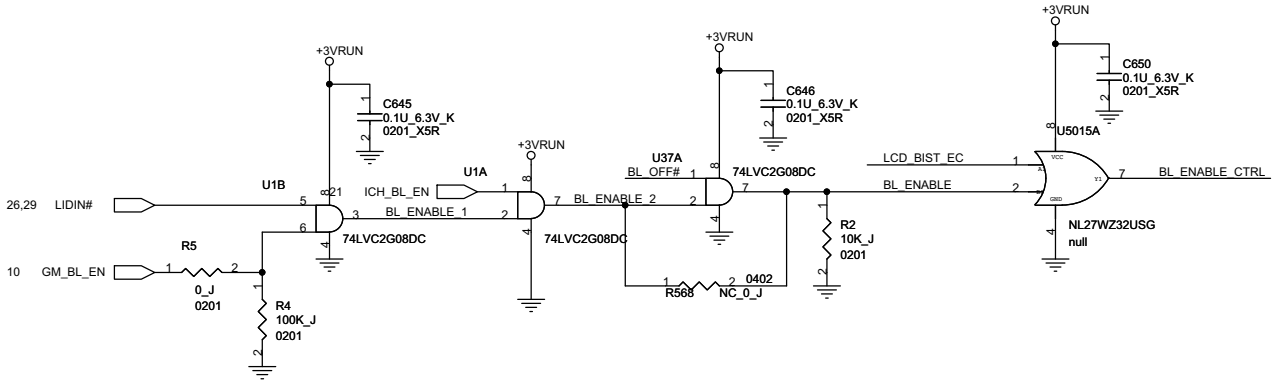
X-Build 2009.10.12
Disabled test fan function and changed part value for CN51 from Mount to NC.

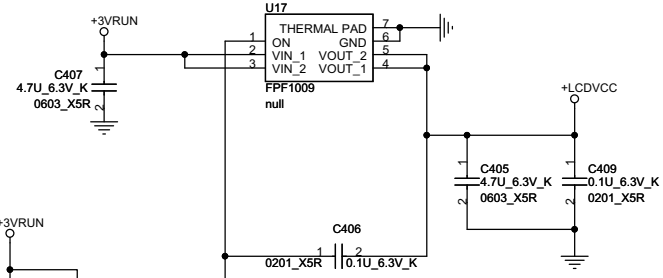
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: FAN/Thermal Sensor		
Size: A3	Document Number: H800 MB	Rev: X-Build
Date: Monday, October 12, 2009	Sheet 30 of 50	

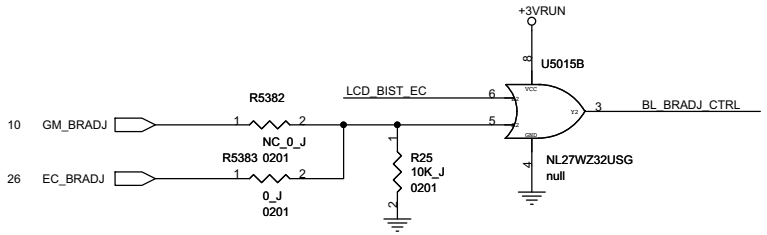
LVDS CONNECTOR

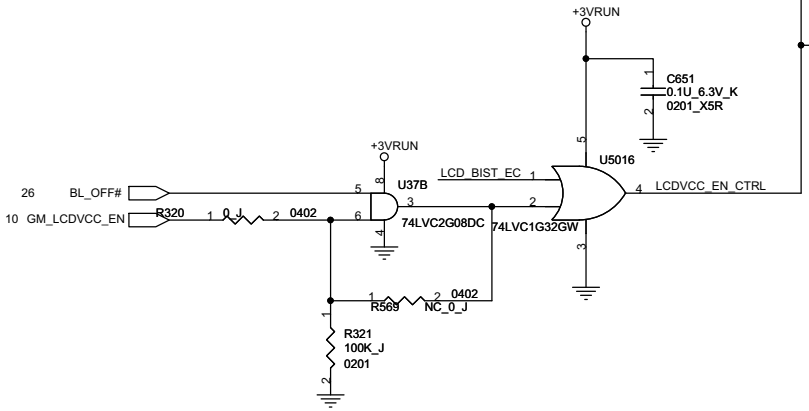


Irms = 20mA per string
Total 6 strings



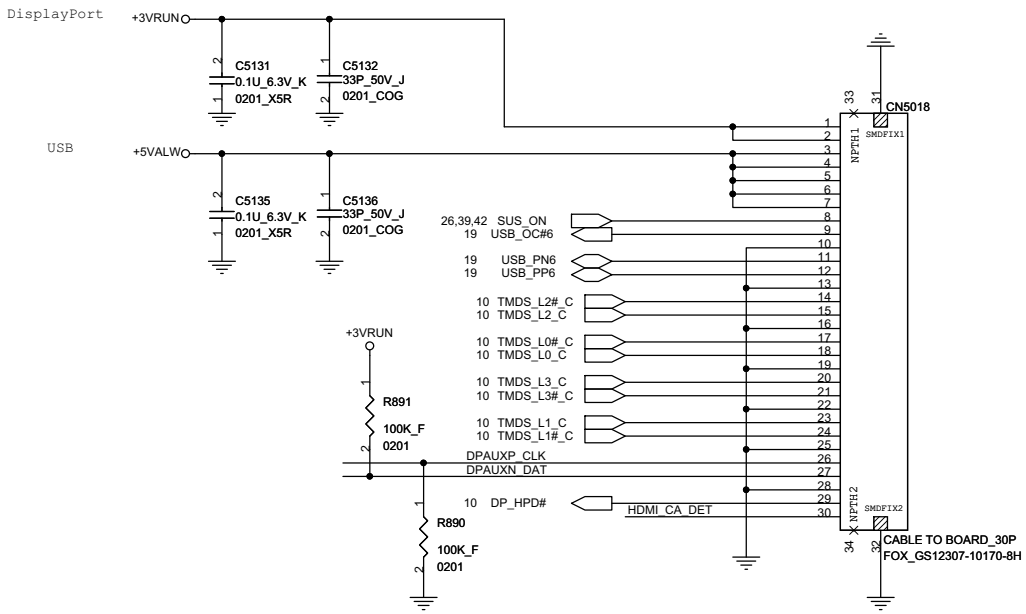




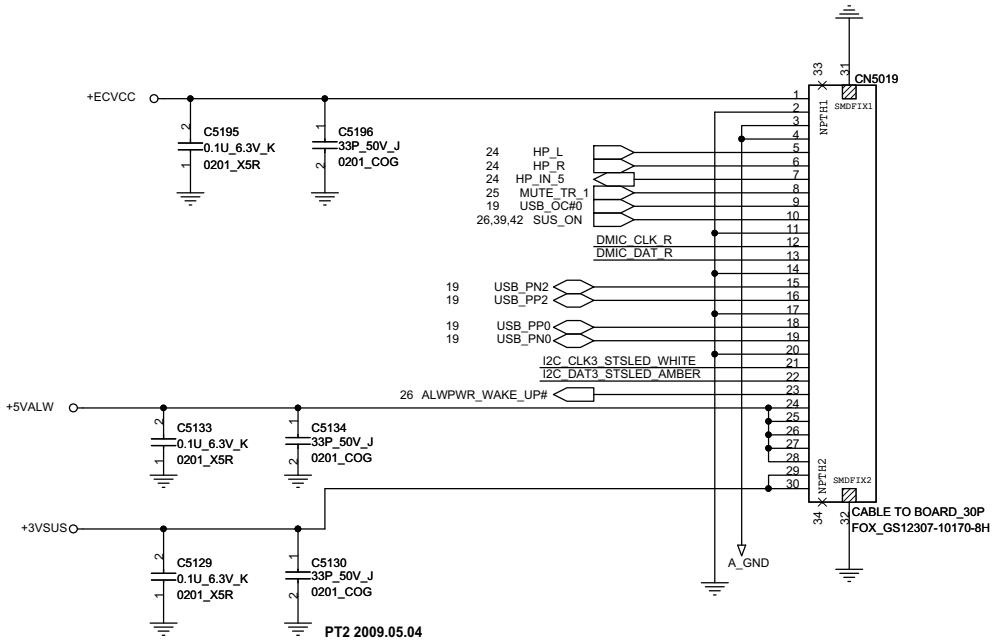


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: LVDS		
Size: A3	Document Number: H800 MB	Rev: X-Build
Date: Monday, October 12, 2009	Sheet 31 of 50	

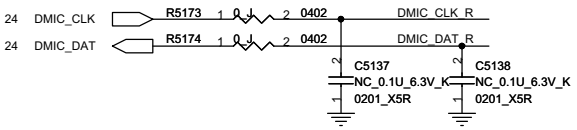
LEFT SIDE I/O CONNECTOR

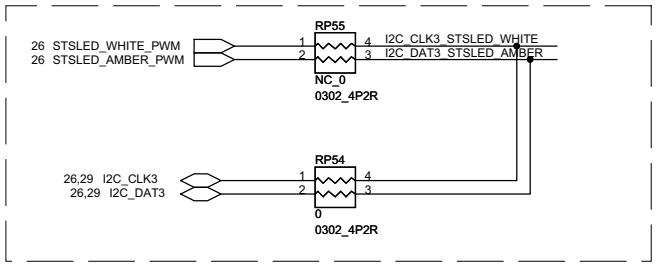


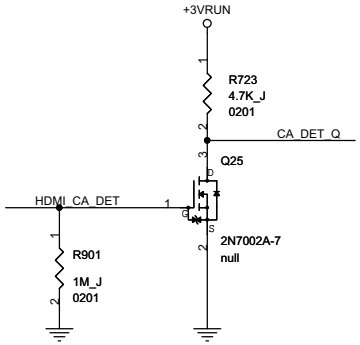
RIGHT SIDE I/O CONNECTOR

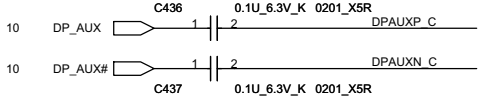


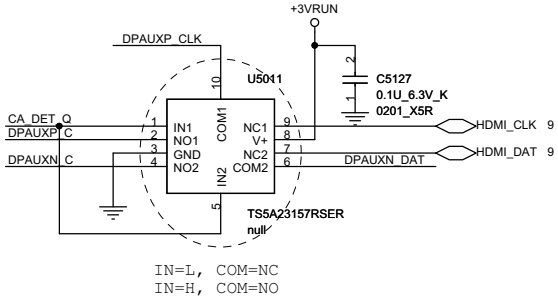
PT2 2009.05.04
Added RP55 & RP54 for the path select function.
If RP55 Mount / RP54 NC : PWM control function by EC.
If RP55 NC / RP54 Mount : I2C Bus connection between Cypress uC(Latch FPC) & EC.





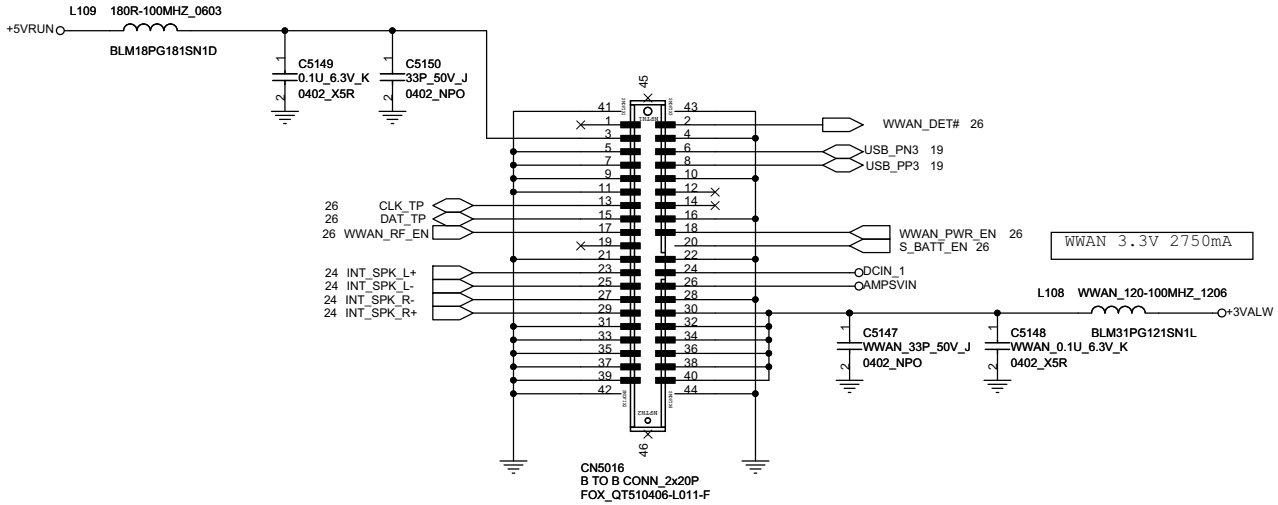




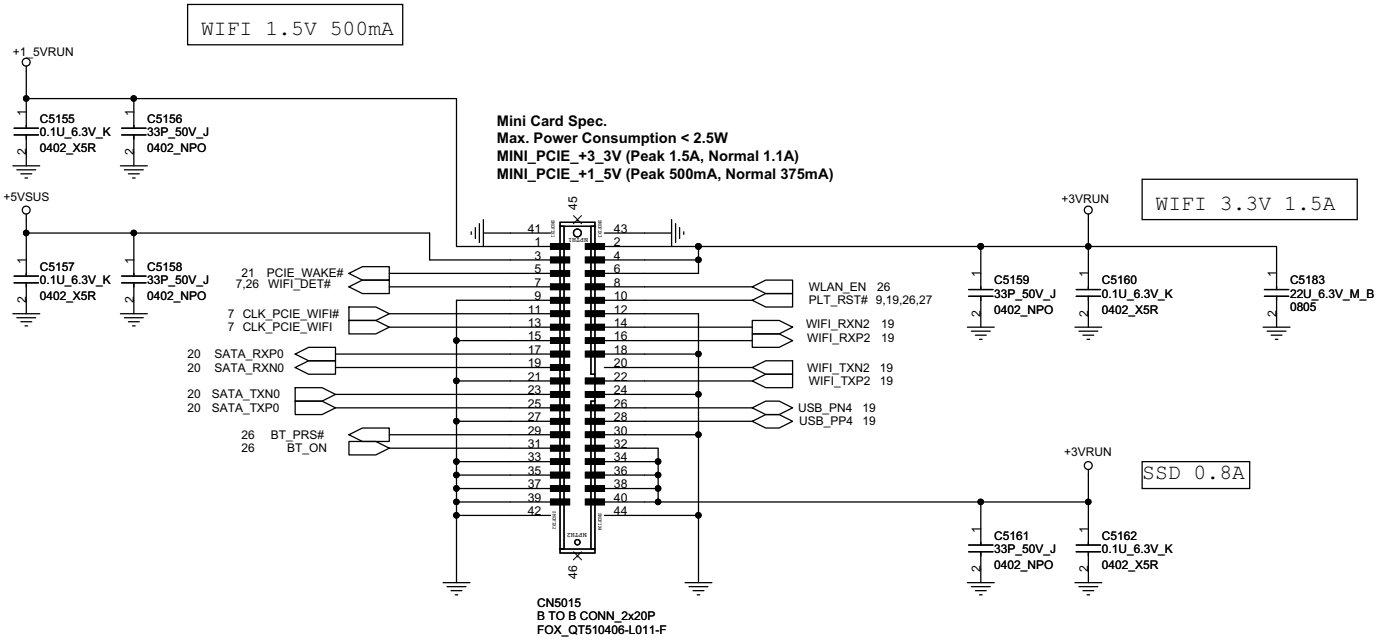


IN=L, COM=NC
IN=H, COM=NO

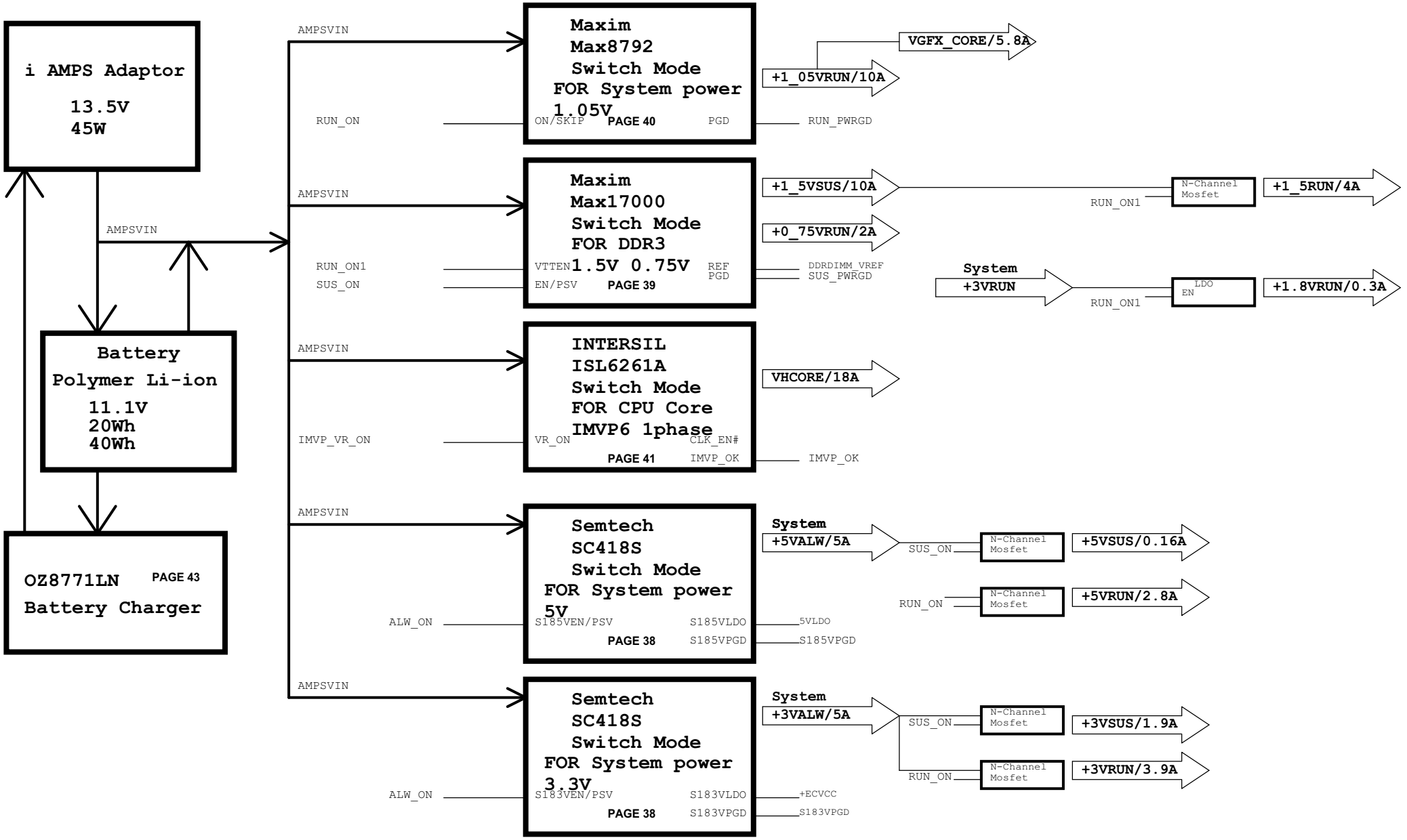
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	IO CONN	
Size A3	Document Number H800 MB	Rev X-Build
Date: Monday, October 12, 2009	Sheet 32 of 50	



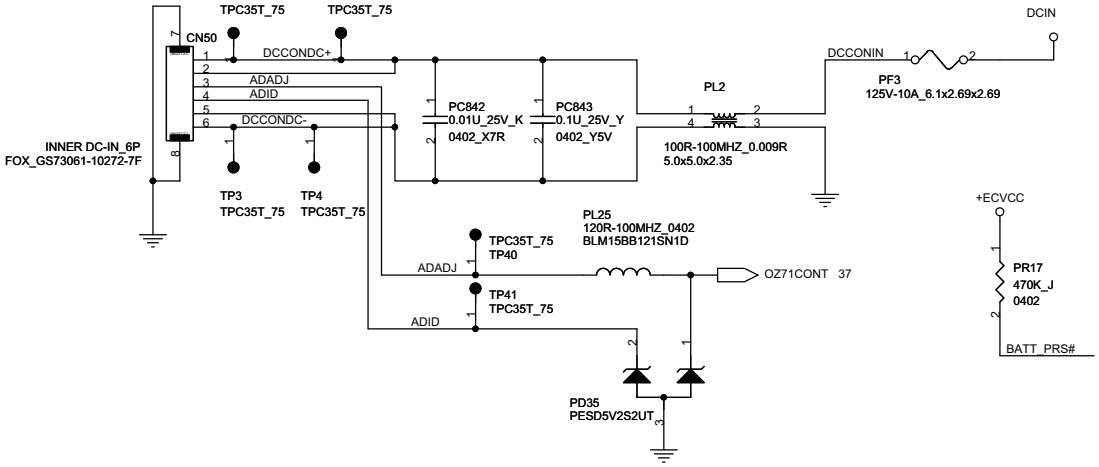
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	WWAN/USB/SPK/TP	
Size A3	Document Number H800 MB	Rev X-Build
Date: Monday, October 12, 2009	Sheet 33 of 50	

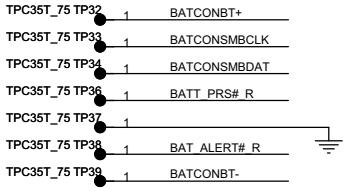


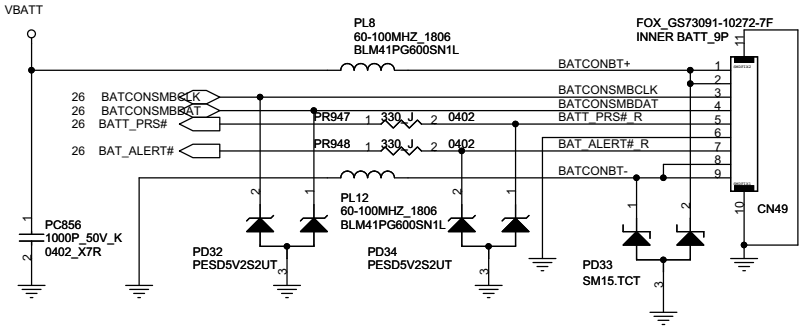
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	WIFI/BT/SSD	
Size A3	Document Number H800 MB	Rev X-Build
Date: Monday, October 12, 2009	Sheet 34 of 50	

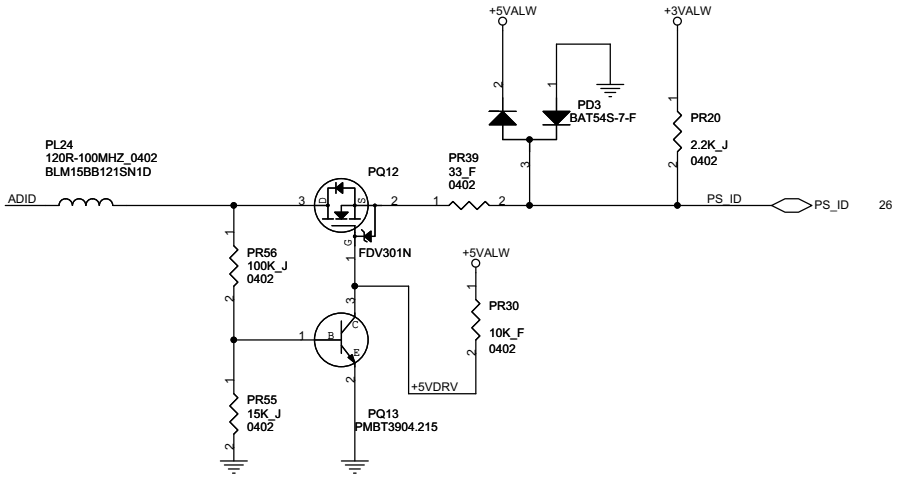


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Power Design Diagram	
Size A3	Document Number H800 MB	Rev X-Build
Date: Wednesday, October 07, 2009	Sheet 35 of 50	

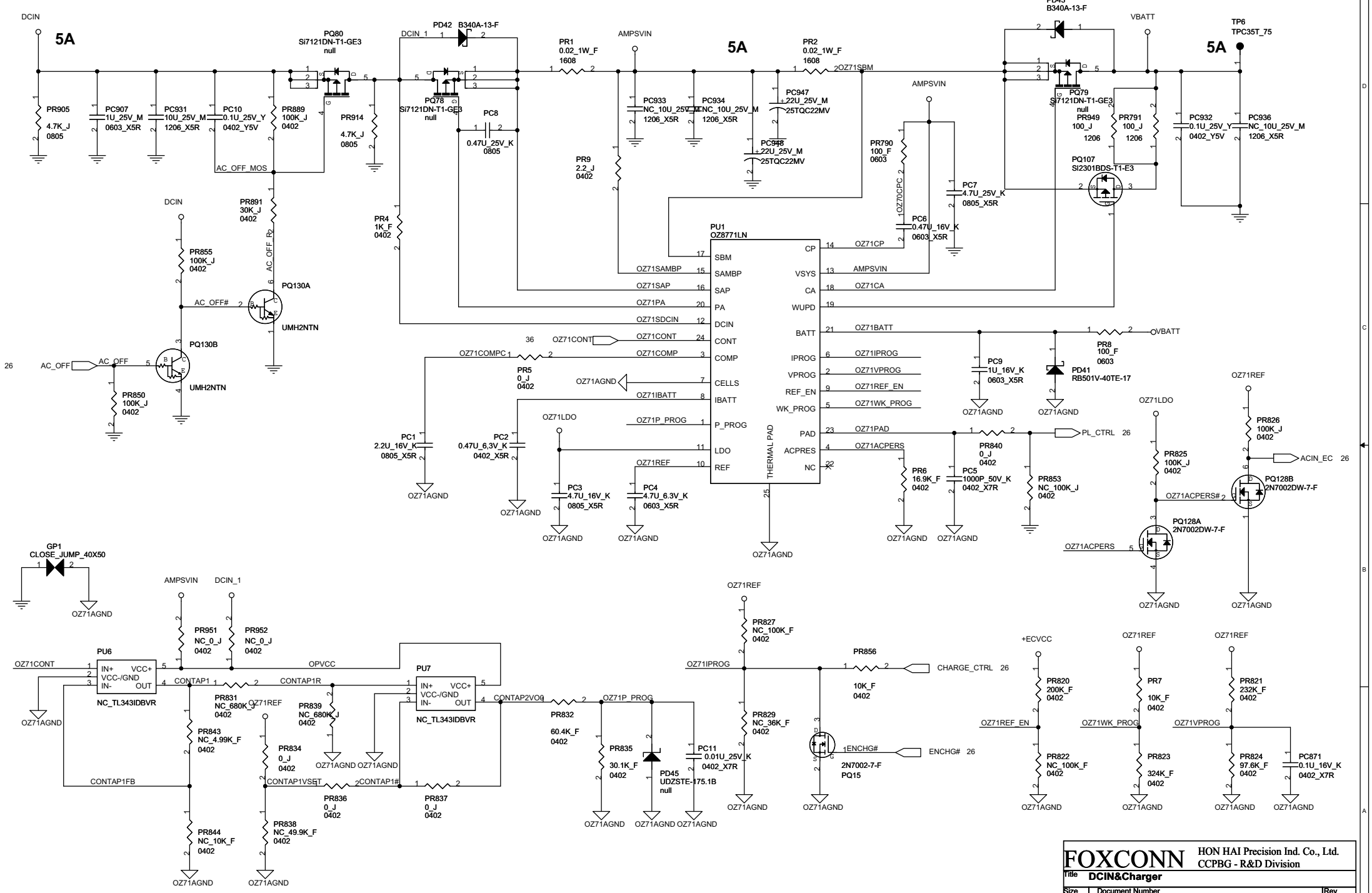




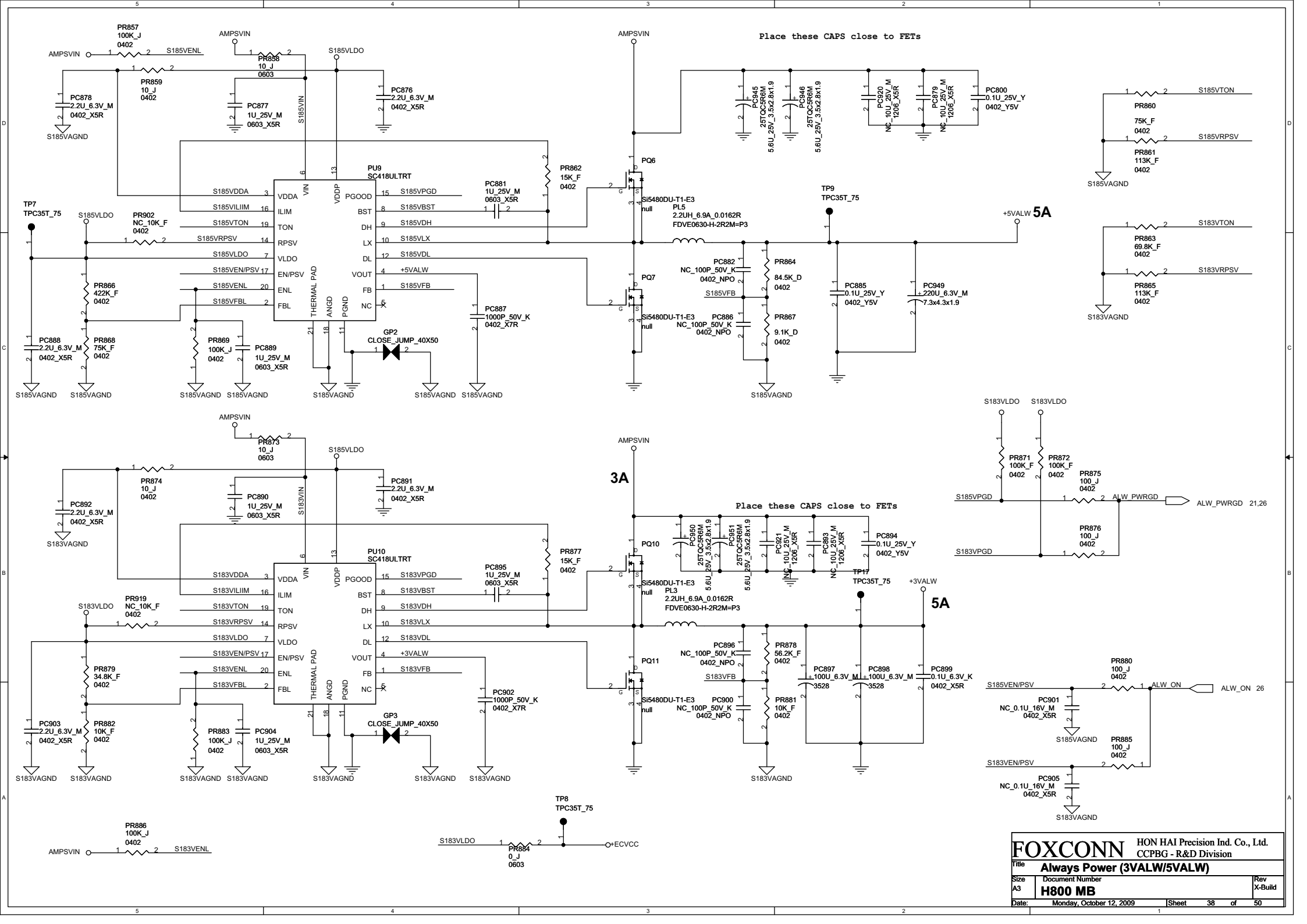




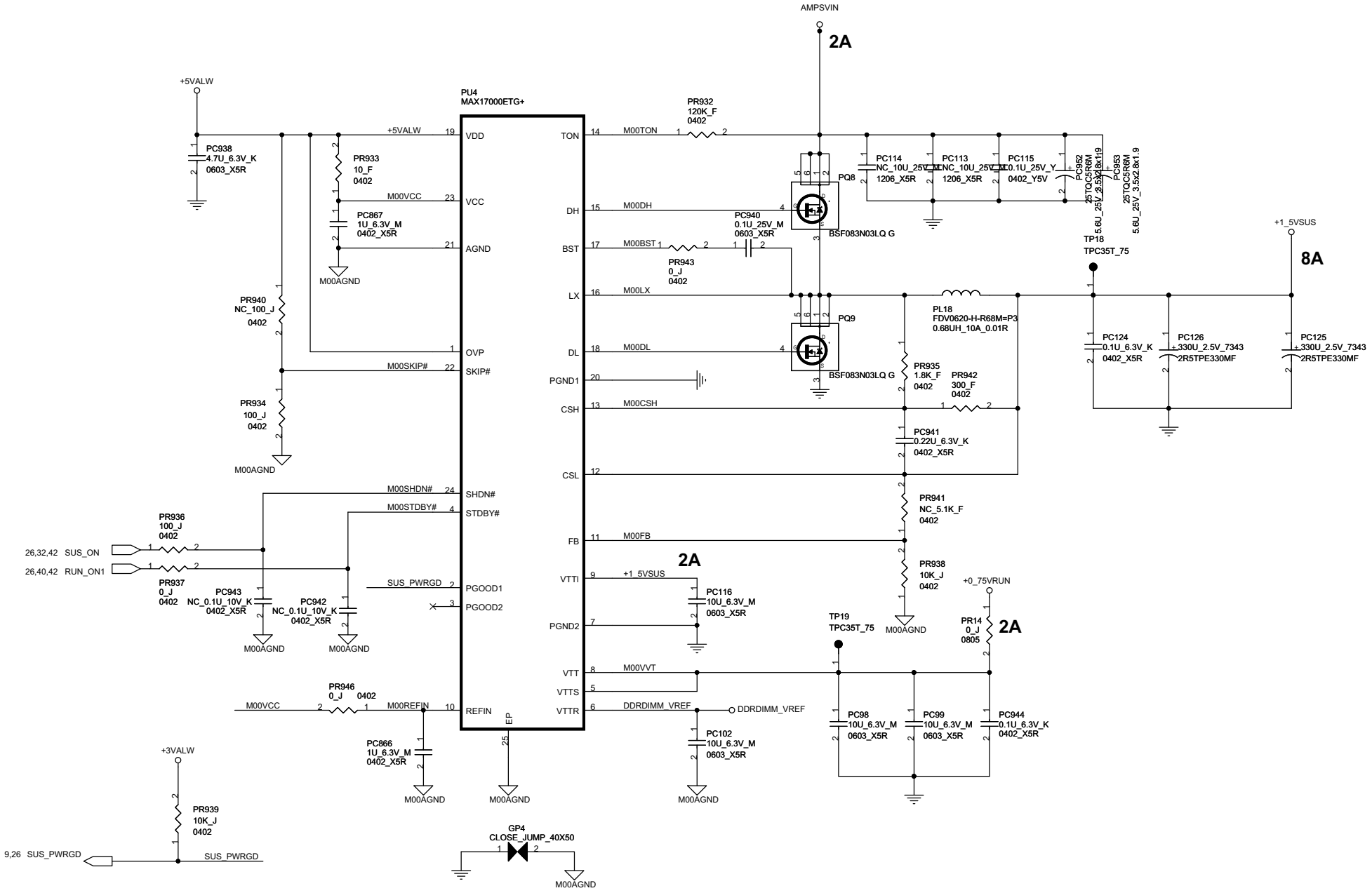
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	DCIN&Charger	
Size A3	Document Number H800 MB	Rev X-Build
Date: Monday, October 12, 2009	Sheet 36 of 50	



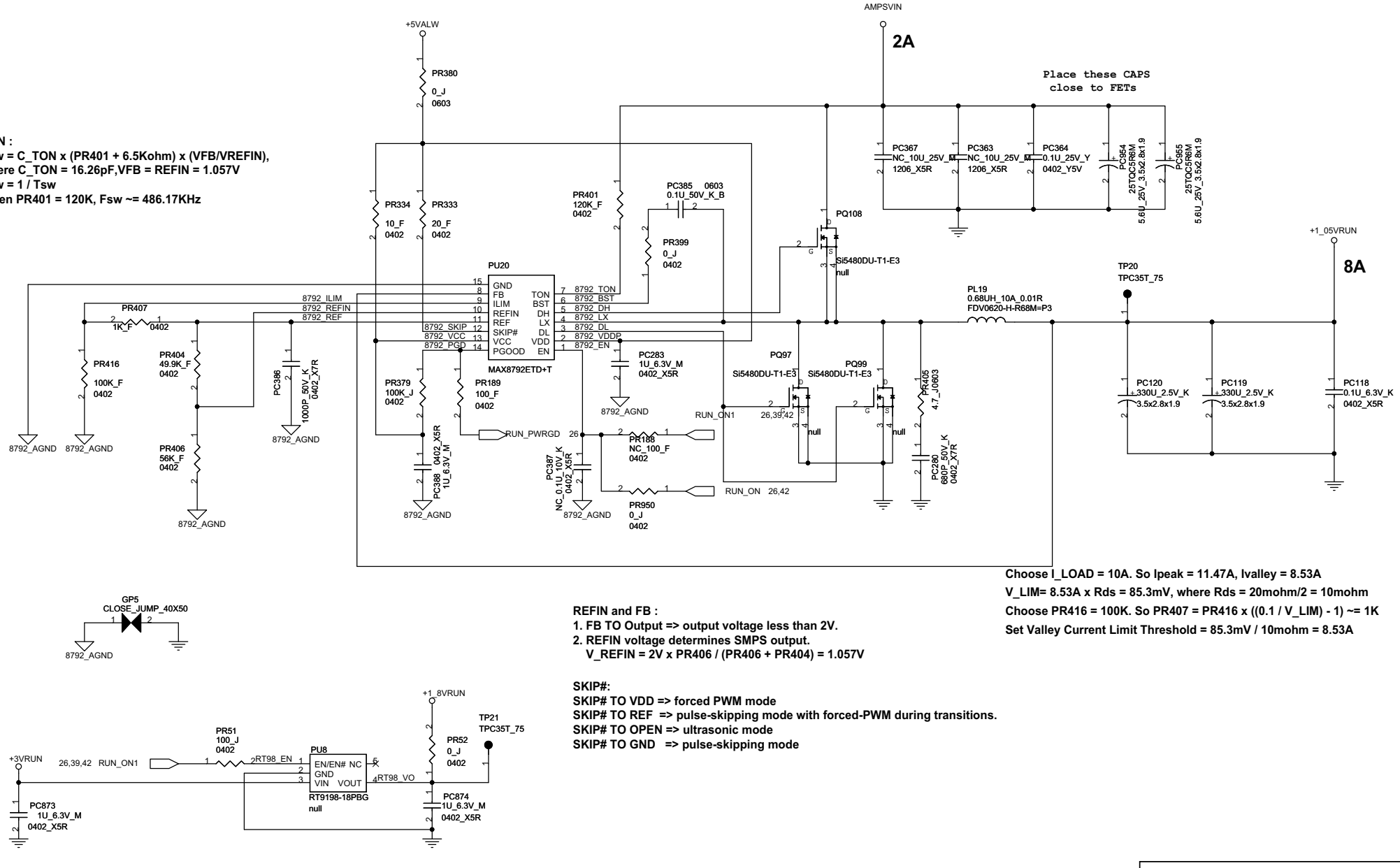
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	DCIN&Charger		
Size A3	Document Number H800 MB		Rev X-Build
Date: Monday, October 12, 2009		Sheet 37 of 50	



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
Title	Always Power (3VALW/5VALW)
Size: A3	Document Number: H800 MB
Rev	X-Build
Date: Monday, October 12, 2009	Sheet 38 of 50



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	DDR3 (+1_5V/+0_75V)	
Size A3	Document Number H800 MB	Rev X-Build
Date: Monday, October 12, 2009	Sheet 39 of 50	

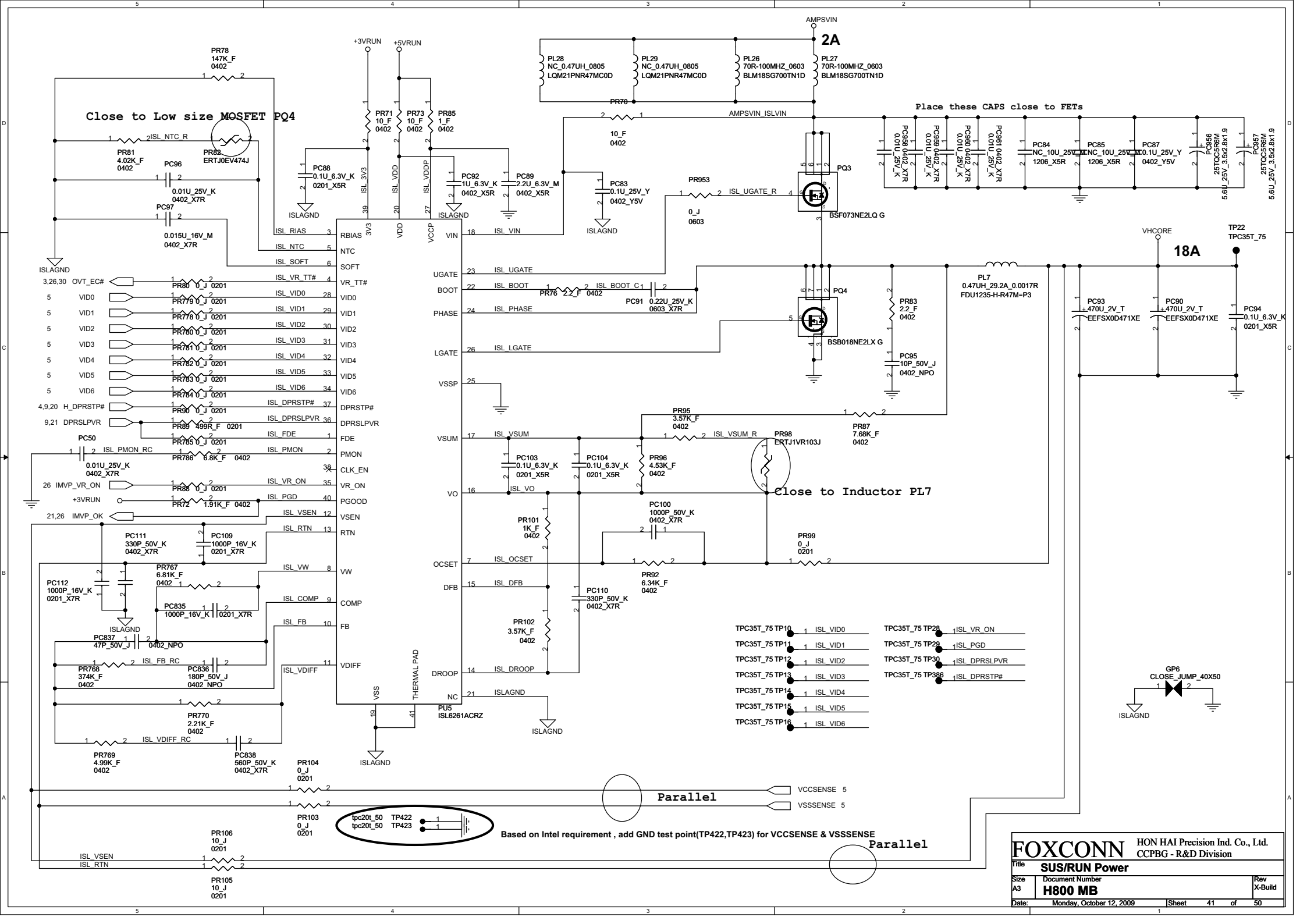


Choose I_LOAD = 10A. So Ipeak = 11.47A, Ivalley = 8.53A
V_LIM= 8.53A x Rds = 85.3mV, where Rds = 20mohm/2 = 10mohm
Choose PR416 = 100K. So PR407 = PR416 x ((0.1 / V_LIM) - 1) ~= 1K
Set Valley Current Limit Threshold = 85.3mV / 10mohm = 8.53A

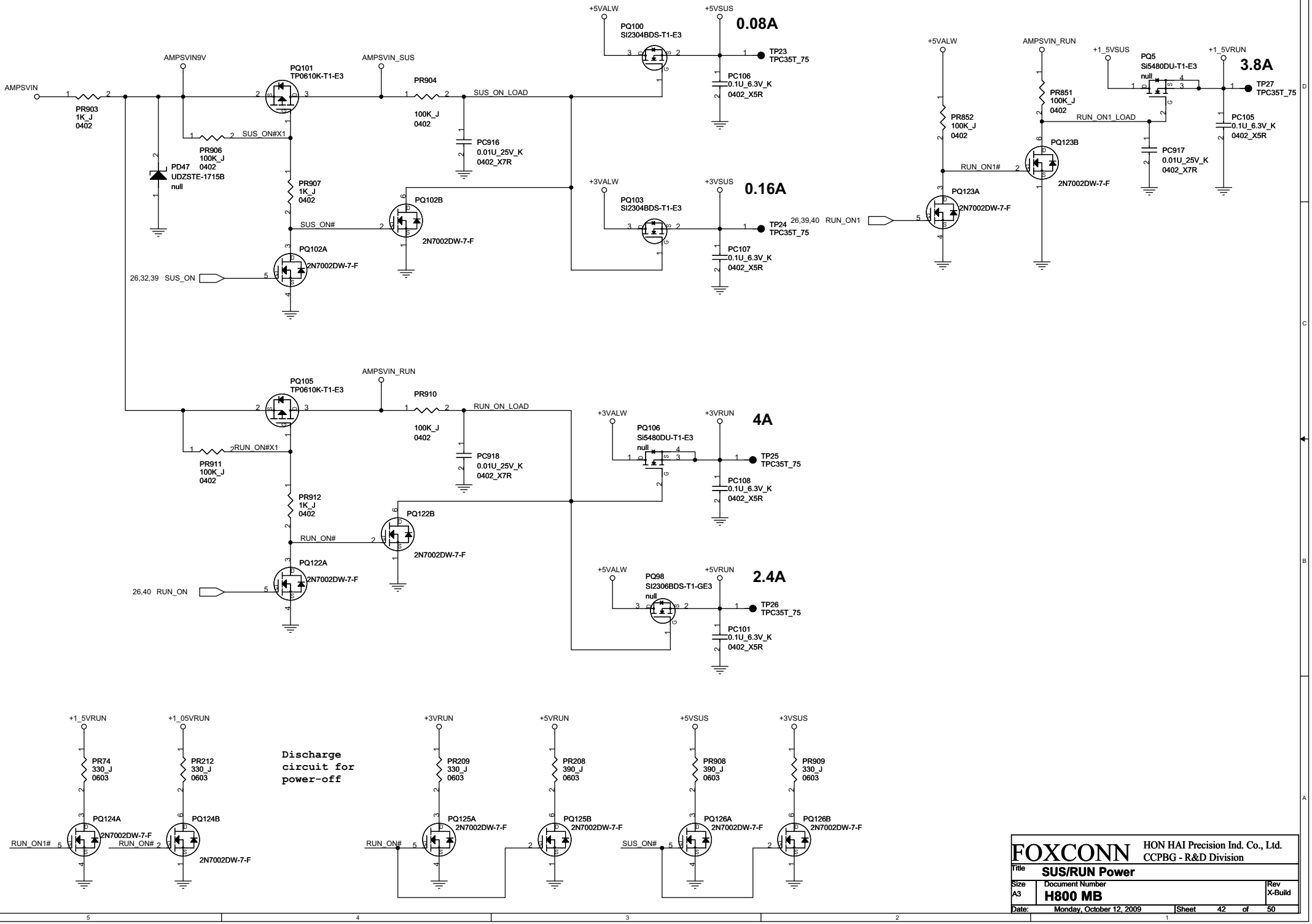
REFIN and FB :
1. FB TO Output => output voltage less than 2V.
2. REFIN voltage determines SMPS output.
   V_REFIN = 2V x PR406 / (PR406 + PR404) = 1.057V

SKIP#:
SKIP# TO VDD => forced PWM mode
SKIP# TO REF => pulse-skipping mode with forced-PWM during transitions.
SKIP# TO OPEN => ultrasonic mode
SKIP# TO GND => pulse-skipping mode

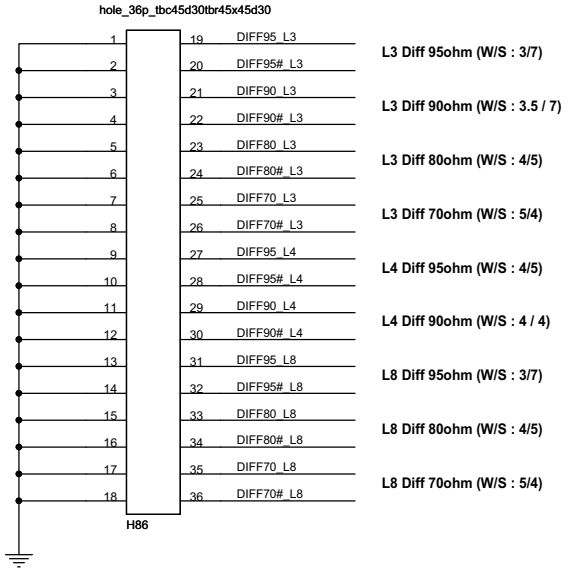
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	SYS Power(+1_05V/+1_8V)	
Size A3	Document Number H800 MB	Rev X-Build
Date: Monday, October 12, 2009	Sheet 40 of 50	



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
Title	SUS/RUN Power
Size A3	Document Number H800 MB
Rev	X-Build
Date: Monday, October 12, 2009	Sheet 41 of 50



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	SUS/RUN Power	
Size A3	Document Number H800 MB	Rev X-Build
Date: Monday, October 12, 2009	Sheet 42 of 50	



L3 Diff 95ohm (W/S : 3/7)

L3 Diff 90ohm (W/S : 3.5 / 7)

L3 Diff 80ohm (W/S : 4/5)

L3 Diff 70ohm (W/S : 5/4)

L4 Diff 95ohm (W/S : 4/5)

L4 Diff 90ohm (W/S : 4 / 4)

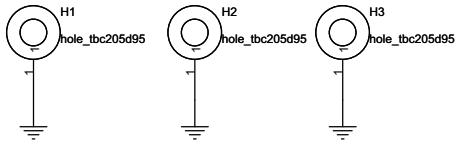
L8 Diff 95ohm (W/S : 3/7)

L8 Diff 80ohm (W/S : 4/5)

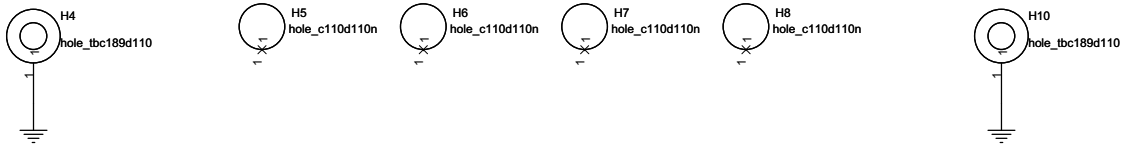
L8 Diff 70ohm (W/S : 5/4)

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: Others power plan		
Size: A3	Document Number: H800 MB	Rev: X-Build
Date: Wednesday, October 07, 2009	Sheet 43 of 50	

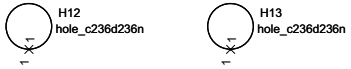
Type A*3PCS

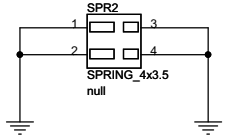


Type B*6PCS



Type C*2PCS





FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	**Others power plan**	
Size A3	Document Number H800 MB	Rev X-Build
Date: Wednesday, October 07, 2009	Sheet 44 of 50	

Page 7. Add R5159,R5160 for crystal accuracy test.
         Delete clocks for LAN chip
Page 9. Pull down DDPC CTRLDATA for DisplayPort strapping
         Add R5162,R5163 for 1.5V CMOS SM_PWRGD signal.
Page 20. Delete SATA1 signals.
Page 26. Change R292 from 10k to 470k.
Page 29. Add R5164 10k PU on SATA_LED#.
Page 30. Add CN19 connector for CPU fan.
Page 32. Add U5011 for dual mode DP Aux/HDMI DDC switch.

2008/0905
1.Update Power schematic

2008/0908

Page9,15,16 addition ODT1,CS#1,CKE1,ZQ1A~ZQ8A and R5165~R5172 for 2 RANK
Page 18 Addition RP54 for 2 RANK
Page 31 Addition C5128,RP50~RP53 For RF team request
Page 32 Addition C5129,C5130,C5131,C5132,C5134,C5135,C5136,C5137,C5138,C5138,R5173,R5174 for RF team request

2008/0909

Page 34 .Move C5055,C5053,C5052,C5050 To right sub board
Page 33   addition pcie_wake# for UWB

2008/0910

Page 18 . DDR3 termal resistance Swap for layout
RP49.4 M_CKE1
RP49.3 M_A_A1
RP49.2 M_A_A12
RP49.1 M_A_A2
RP46.4 M_A_BS2
RP46.3 M_A_RAS#
RP46.2 M_A_CAS#
RP46.1 M_A_A9
RP43.4 M_A_A5
RP43.3M_A_A3
RP43.2 M_A_A7
RP43.1 M_A_BS0
RP45.4 M_ODT1
RP45.3M_A_A0
RP45.2M_A_A13
RP45.1M_A_WE#
RP54.4   M_ODT0
RP54.3   M_CS#1
RP54.2   M_CS#0

For RF suggestion
Page 6 C835,C836,C236,C237,C238 change to 0201 SIZE
Page 13 ADD C5139,C5140
Page 18 ADD C5141~C5144
Page 22 ADD C5145
Page 24 ADD C5146
Page 33 ADD C5147~C5154 ,ADD L109~L111
Page 34 ADD C5155~C5164

2008/0911
Page 33 CN5016 PIN 31 ,PIN33 SWAP for layout route
Page 13 DEL CAP5 for layout space
Page 32 CN5019 power pin 1 from +5VSUS to +3VSUS
         Pin2 from +5VALWS to +5VALW
Page 15,16 U62~U69 Change SDRAM from Qimonda(78ball) to Sumaung 1G (82 Ball)
Page 18 Addition C5165,C5166,R5175,R5176 for 2 rank

2008/0911A 1600
Page 15, Change U68,U69 CLK from M_CLK_DDR#1,M_CLK_DDR1 to M_CLK_DDR#0,M_CLK_DDR0
Page 16, Change U62,U63 CLK from M_CLK_DDR#0,M_CLK_DDR0 to M_CLK_DDR#1,M_CLK_DDR1

2008/0911B-1700
Page 33 CN5016 change to FOX_QT510406-L011-F
Page 34 CN5015 change to FOX_QT510406-L011-F

2008/0912
Page 3 Change test point for FSB each group long and short trace length
        TP73 H_A#4 --->H_A#14
        TP74 H_A#10 --->H_A#16
        TP75 H_A#17 --->H_A#29
        TP76 H_A#20 --->H_A#35
Page 4 TP79 H_D#8 --->H_D#11
        TP81 H_D#29 --->H_D#17
Page 31 ADD LVDS TEST POINT TP320~TP327

2008/0912A
Page9,15,16 DEL ODT1,CS#1,CKE1,ZQ1A~ZQ8A and R5165~R5172 for 1RANK
Page 18 1.DEL RP54 for 1 RANK
        DEL C5165,C5166,R5175,R5176 for 1 rank
        2.. DDR3 termal resistance Swap back for layout
Page 15, Change U68,U69 CLK from M_CLK_DDR#1,M_CLK_DDR1 to M_CLK_DDR#0,M_CLK_DDR0
Page 16, Change U62,U63 CLK from M_CLK_DDR#0,M_CLK_DDR1 to M_CLK_DDR#1,M_CLK_DDR0
Page 44 Addition H1~H23 HOLE

2008/0915
Page 24 DEL R5135,R5136
Page 28 (1)Add 4 keyboard Pad KB5077~KB5080(Page UP,Page Down,Delete,Insert)
        (2) "R-CTRL"KB5061 Pin1 from KSI6 change to KSI1
            Pin2 from KSO7 change to KSO9

        (3)"WIN.APP" KB5072 Pin1 from KSI1 change to KSI6
            Pin2 from KSO9 change to KSO7
        (4)"WIN.APP" KB5071 Pin1 from KSI1 change to KSI6
            Pin2 from KSO9 change to KSO7

Page31 (1) Del LVDS TEST POINT TP320~TP321
       (2) Change RP50~RP53 Form TAI to Cyntec(0404-->0302)

2008/0916
Page 4 ADD TEST POINT TP320 forH_DPSLP#
Page 8 ADD TEST POINT TP321~ ~TP342
Page 11 DEL TEST POINT TP188~TP192
Page 19 (1)ADD TEST POINT TP343 for CLK_ICHPCI
         (2)U33 change package to 13-W25X80A-7000

2008/0916A
        Update Power schematic page 35~43

2008/0916B
        (1)Page 7 Add test point TP344~ TP345
        (2)Change All test point from 26 mil to 20 mil
        (3)Page 10 Add R5176~R5177

2008/0917
        (1)Page 22 Change U38 from G9131-15T73Uf to RT9170-15PV

2008/0917A
Page 29 (1)CN3 change to
        (2)Move U5010 R280,R5158 to Function key FPC
Page 26 Change EC schematic
Page 15 DEL TP 318,TP319

2008/0917B
        Update Power Schematic Page 35~43
        Page 24 DEL R5175

2008/0918
        Page 10 R5176,R5177 Change to 10k
        Page 32 CN5016 Pin6 change to GND
        Page 24 Q5021 Change to 17-2N7002A-7000
        Page 29 LED3 chagne to small size (HT-191UD)
        ADD LED
        DEL R323,R219
        Page 26 DEL R300,R277,R299,R282

2008/0918A
        Page 34 Change C5156,C5158,C5164,C5159,C5161 to 0402 10p

2008/0919
1.Page 26 ADD TEST POINT TP372~TP382
2.Page 7 ADD TEST POINT TP366
3.Page 9 ADD TEST POINT TP367

2008/0919A
1.Page 35~43 Update Power schematic

2008/0919B
1.Page 21 DEL U3,C21

2008/0922
1.Page 32 CN5019 pin11,pin12 swap for layout route
2.Page 32 CN5018 pin11,pin12 swap and pin 17,18 for layout route
3.Page 31 Change U17 to PSL part (TI TPS 2033)
        Rail time 8.6 ms
        Fail time 3.4ms
4.Page 9 Add test point TP384
5.Page 15 U71 Change to STTS42E02BDN3F for PSL

2008/0922B
1.Update Power schematic page35~43

2008/0923
1.Page 7 C339 from 0.1uf change to 33pf for RF suggestion
2.Page 7 ADD C5168 for RF suggestion

2008/0923A
1.Page 24 DEL MIC_L,MIC_R net,MIC1_VREFO_L,MIC1_VREFO_R

2008/0924
1.Page 26 update ec schematic,Del R273,R274,ADD C5176
2.Page 9 DEL TP384
3.Page 31 ADD C5177 33pf
4.Page 12 ADD C5169~C5170 33pf
5.Page 22 ADD C5172~C5175 33 pf
6.Page 6 C835,C836,C236,C237,C238 from 0.1u change to 33pf
7.Page 18 C5141~C5144 from 0.1u change to 33pf
8.Page 24 C5146 from 0.1u change to 33pf
9.Page 33 C5147,C5151,C5153,C5150 from 0.1u change to 33pf
10.Page 31 SWAP CN5017 pin 5 ,6
pin 8,9 ,Pin 11,12 for layout route
11.Page 29 LED1 from HT-170NB5 change to LTW-C191DS5
LED5021 form HT-191UD change to LTW-C194TS5
12.Page 32 Change CN5019 pin for layout route

2008/0925
1.Page7 ADD R for Silego special function
2.Page 24 ADD C5178,C5179
3.Page 34 Change C5156,C5158,C5164,C5159,C5161 form 10PF(0402) to 33PF (0201)
4.Page 26 update EC schematic
5.Page 15 Change U71 STTS424E02BDN3F to STTS424CDA3F
Page 31 DEL U71,ADD R5336,R5337,R5335 ,Q5023,Q5024

2008/0926
1.Update Power schematic page 35~43
2.Page 31 change to TI solution

2008/0926A
1.DEL RP50,RP51,RP52,RP53

2008/0926B
1.Page 1 ADD CN5020 ,R5336,R5337 ,C5180 INTEL ITP DEBUG PORT
2.Page 7 ADD R5339,R5340, C5181,C5182 for INTEL ITP DEBUG PORT

2008/0930
1.Page26 Change CN5014 Pin define
2.Page15~16 Change test point for SI(Short and long)
TP125 Form M_ADQ1 change to M_ADQ3
TP126 Form M_ADQ6 change to M_ADQ4
TP127 Form M_ADQ10 change to M_ADQ11
TP128 Form M_ADQ14 change to M_ADQ13
TP132 Form M_ADQ21 change to M_ADQ20
TP140 Form M_ADQ26 change to M_ADQ28
TP142 Form M_ADQ30 change to M_ADQ31
TP155 Form M_ADQ38 change to M_ADQ37
TP156 Form M_ADQ40 change to M_ADQ41
TP157 Form M_ADQ43 change to M_ADQ47
TP158 Form M_ADQ49 change to M_ADQ51
TP159 Form M_ADQ52 change to M_ADQ54
TP160 Form M_ADQ57 change to M_ADQ56
TP161 Form M_ADQ59 change to M_ADQ58
TP121 Form M_A_A7 change to M_A_A8
TP122 Form M_A_A10 change to M_A_A13

3.Page 30 NC all keyboard back light LED

2008/0930A
1.Update Power schematic
2.Page 24 U5007 ADD SPK_DMA_R,SPK_DMA_L
3.Page 32 Change CN5019 pin define

2008/1001
1.Update Power schematic
2.Page 26 SWAP RP33,R867,R868

2008/1002
Page 34 ADD C5183 for RF suggestion
Page 13 Change C5139 and C5140 from 0.1u to 33PF for RF suggestion

2008/1002A
Page 3 1.ADD SB_RST# to R5338
        2.R5338 from 1k change to 0 ohm
        3.R703.1 From 5V always change to 3V always
        4.ADD R5341 for VRMPWRGD,ADD R5432 for UWB_EN

2008/1003
Page 26 change BAT_ALERT# from 100 to 67 pin

2008/1003B
Page 3 R5337
Page 34~43 Update power schematic

2008/1003C
Page 16 ADD TEST POINT TP388~TP395
Page7 R486 NC,R5334 NC,ADD R for ITP EN

2008/1004
Page 31 RP50~RP53 for RF suggestion ADD

2008/1004A
Page 29 NC LED2 ,ADD CAP_LED net to keyboard CN CN5014.25

DEL R314,R313 ,R707 From 100 change to 680 ohm,R315 From 150 change to 680 ohm

Page 30 NC ,R5036,R5001,R5063,R5094,R5002,
R5003,R5033,R5032,R5006,R5104,
R5004,R5000,R5108,R5109,R5050,
R5105,R5110,R5083,R5034,R5107

Page 30 NC ,R5036,R5001,R5063,R5094,R5002,
R5003,R5033,R5032,R5006,R5104,
R5004,R5000,R5108,R5109,R5050,
R5105,R5110,R5083,R5034,R5107

Page 31 DEL RP50~RP53 ,ADD R5344~R5351,C5184~C5191

CAP3,9,11,21 From 3528 size chang to 7343,DEL CAP10 for Hieght limit <2.0mm

Page 25 ADD C5192 for Codec FAE suggestion

Page 24 ADD C5193,C5194,R5134 change to L115 for Codec FAE suggestion

2008/1006A

1.Chagne Y5 from 4 pin to 2pin for heilght limit<2mm
2. DEL R866,R865,R864
3. Chagne R234 form 33k to 15k for hardware shut seeting 95 degree
4.Chagne R241 form 15k to 4.7k for hardware shut seeting 95 degree

2008/1006B
1.Page 6 ADD R5552,R5553
2.Page 31 Change U17 to PSL part (FPF1009)
3.Page 22 Change U38 from RT9170-15PV to RT9198-15GV
4.Page 19 Change U33 from W25X80AVSSIG to W25X80AVSNIG for helight limit<2mm
5.Change CN5016 ,CN5015 pin define for layout route

2008/1006D
1.Modify HOLE SIZE

2008/10/07
1.Change USB port 5 to Port6 for USB to RJ45 special command application

2008/10/07A
1.C302,C5136,C5132 change to 0201 size

2008/10/07B
1.ADD R5354,R5355,R5356 for LCD_BIST

2008/10/07C
1.Change LCD_BIST_EC form U36.17 toU36. 77

2008/10/07D
1.Update Power schematic

2008/10/07E
1.Change CN3 to FOX_QT510206-2001-9F

2008/10/08
1.ADD KSO8 to CN3.17
2.ADD CAP25,CAP26 (T-CAP),DEL C5102,C5106 for FAE suggestion

2008/10/08B
1. Change CN5020 to MOLEX_52435-2872
2.R703,R705,R317,R318,R322,R319,R324,R5164 change to 0201 size for save layout space
3.ADD Q5024,Q5023,R5358,R5360 for dual color power LED
4.Change C301 to 0402 size for material issue
5.ADD R5357
6.Change CN5019 to 30pin for support latch button
7.Change R5173,R5174 to 0201 size

2008/10/08C
1. Change C301 for 0201 size
2.ADD POWER_LED1 to U36.28

2008/10/08D
1. Change CN5014 connector

2008/10/09
1. ADD U5013,C195 ,ADD R5361

2008/10/09A
1. ADD L116,R5362,,R5363 for EMI suggestion

2008/10/09B
1. Chagne L116 SIZE

2008/10/09C
1. ADD +5VALW to CN5016.2

2008/10/13
1. DelU5013 and C5195

2008/10/13A
1. Change to PU8 part to Green part

2008/10/13B
1. Change CN12 from FOX_HS8802V-S4 to FOX_HS8802F

2008/10/13C
1. Update power schematic
2.Change CN51 to HS8803F

2008/10/14
1.Change CN5017 from GS12257-10170-8F to FOX_GS12257-10170-8H
2.Change CN19 from FOX_GB1RF041-1203-8F to FOX_GB1RF041-1203-8H
2.

2008/10/14A (Ryan-For material preparation concern)
1.Change part for PC938 from 1C-2X30475-K000 to 1C-2B30475-K100
2.Change part from 1C-2B10103-J200 to 1C-2B10103-K200.
C88,C303,C319,C328,C341,C451,C501,C557,C560,C602,C603,C5124

2008/10/14B
1.DEL KB5068,NB5067,KB5070,KB5043,KB5013,KB5047,KB5075,R5068,R5072

2008/10/15
1.Change R5360,R707,R315 to 1K,Change power source R5358,R703,R317,R322 to +5

2008/10/15A
1 DEL H9

2008/10/15B
1 ADD GND to Connector

2008/10/15C1
1 Update HOLE

2008/10/15C2
1 Update KB5060 PCB FOOT PRINT

2008/10/15C3
1 DEL KEYBOARD back light LED and Cap lock LED circuit

2008/10/15D
1 DEL H14

2008/10/15D
1 DEL H14

2008/10/15E
1 ADD Keyboard PAD KB5070,KB5067,KB5068,KB5043,KB5013,KB5047

2008/10/15F
1 ADD R5364,R5365

2008/10/16
1 ADD CN5014 GND PIN

2008/10/16A
1 . Update Key PAD

2008/10/16b
1 . ADD KSI2

2008/10/16C
1 . POP R5365,DEL KB5044

2008/10/17D
1.SWAP U36 pin 32 and pin21
2.Chagne CN5019.1 form AGND to +ECVCC
3.Change R279,R284 pull up power source form +3valway to +ECVCC

2008/10/17E

2008/10/17F
Modify head value for PR847 from FU_NC_ to NC_
Add head value for PC851,PU2 as FU_
Modify head value for PR827,PR829 from OZ_NC_ to NC_
Modify head value for PR856 from OZ_NC_ to OZ_

20081020
Change part for SW1 from 19-1BT0020-1000 to 19-1BT0020-1002
for PSL requirement.

20081021
Change the head value for CN5020 to NC_.

20081028
1.R5360,R315 from 1K change to 499_F (1R-0004990-F200)
2.R707 from 1K change to 680 (1R-0000681-J200)
3.R562 from 150 change to 220 (1R-0000221-J200)

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: SSI Changelist		
Size: D	Document Number: H800 MB	Rev: X-Build
Date: Wednesday, October 07, 2009	Sheet 45 of 59	

2008/11/21
Page 36
1.Change SPI_ROM_SDI from U36 pin 102 to pin 103 to fix EVT2 wrong connection
2.Change SPI_ROM_SDO from U36 pin 103 to pin 102 to fix EVT2 wrong connection
3.Change
R310,R270,R534,R304,R532,R297,R563,R286,R561,R5364,R287,R560,R5365,R867,R868,R279,R284,R294 from 0201 to 0402 for product yield
4.DEL R5361 , R5357 and remove FN_INT#
Page35~43 Update Power schematic
Change PQ4 from 17-1RF6631-TR00 to 17-BSB018N-E200
Change PQ3 from 17-1RF6638-PB00 to 17-BSF073N-E200
Change PQ8,PQ9 from 17-1RF6638-PB00 to 17-BSF083N-0300
Change PR905 from 1R-0000512-F200 to 1R-0001271-F200
Change PR407 from 1R-0000183-F200 to 1R-0000153-F200
Add part PD42 (From NC to 16-B340A13-F000)
Change PR6 from 1R-0001652-F200 to 1R-0001692-F200
Change net name from M00OVP to +5VALW
Change net name from M001D8VVOUT to + +1_5VSUS_1.
Change PR846 From 1R-0000104-F300 to 1R-0000303-F200
Add PD34 16-PESD5V2-S200 for EC ESD

2008/11/24
Page 36
1.ADD L117 for ECVCC

2008/12/1
1.Change EC and audio part
R5324,R537,R5341,R275,R526,R524,R525,R550,R267,R566,R283,R5157,R5156,R5149,R5144,
R5150,R5174,R5152,R5173,R5147,R5141,R5137,R5138,R5155,R5153,R5154 from 0201 to 0402 for product yield

2008/12/1A
1.ADD TEST POINT TP398~TP406 for BFT test point
2.Change
R481,R480,R486,R485,R483,R490,R489,R493,R512,R513,R517,R5343,R496,R494,R503,R501,R5352,R5353,
R491,R492,R495,R502,R19,R565,R308,R309,R306 from 0201 to 0402 for product yeild

2008/12/1B
1.Change C5161,C5162,C5163,C5164,C5159,C5160,C5155,C5156,C5158,C5157,C5148,C5147,C5151,C5152,
C5153,C5154,C5149,C5150 from 0201 to 0402 for product yield

2008/12/07
1.SWAP U36 pin2 and pin5
2.SWAP U32 pin102 and pin103

2008/12/08
1.Update block diagram
2.DEL on board Key pad

2008/12/22
Page 22
1.ADD RP50,RP51 for EC keyboard pull up
Page19
2.Change RP35,RP2,RP36,RP4,RP4,RP3,RP6,RP42,RP37 from 0201_8P4R to 0804_8P4R
3.DEL PWR LED and Status LED circuit
DEL Q5024,R5358,R5359,Q5023,Q54,R703,R705,Q52,R707,LED1,R5360,Q15,R317,R318,Q16,Q18,R322,R319,Q17,Q20,R324,R315
4.Remove UWB circuit
DEL R5342,C52,C46
5.Change R5356 from 0201 to 0402 for product yield
6.Change L117 from 0402 to 0603 for +ECVCC

2008/12/22A
Page 21
Change RP7,RP1 from 0201_8P4R to 0804_8P4R
Page 12
ADD CAP8

2008/12/23
1.ADD Port to EC keyboard to FN key signel
2.DEL USB Port5
3.DEL Fujst Power solution

2008/12/24
1.Change H4,H5,H6,H7,H8,H9,H10,H11 to 2.5mm(1X-HOLE000-0835)

2008/12/25
1.Change CN5018 TMDS and power Pin define for layout route

Pin	NET
14	TMDS_L2#_C
15	TMDS_L2_C
17	TMDS_L0#_C
18	TMDS_L0_C
20	TMDS_L3_C
21	TMDS_L3#_C
23	TMDS_L1_C
24	TMDS_L1#_C

2. Remove DMA speaker function ,Del SPK_DMA_L,SPK_DMA_R signal

3.Change CN5019 pin define for layout route
4.ADD R5366 100k pull down RES for fix HP detect floating issue
5. ADD C5195,C5196 for +ECVCC

2008/12/25
1.ADD SUS_ON and RUN_ON test point for SI

2008/12/29
1.Change C301 from 0201 to 0402 for material prepare issue

2009/01/05
Update Power schematic,
1.Change CN50 from FOX_GS73091-10272-7F to FOX_GS73061-10272-7F,
2. Add PL25.
3. Add power test Pad TP32,TP33,TP34,TP36,TP37,TP38,TP39.
4. CHANGE From 1C-2B60106-M300 to 1C-2B60106-M001 for Derating issue.
5. Add PR18,PR19,PR21,PR23,PR24 for Derating issue

DVT 20090105A
Change Power source for CN5019 Pin29&30 from +3VALW to +3VSUS

DVT 20090106
(1)Follow ME request to change B type Hole from 1X-HOLE000-0835 to 1X-HOLE000-0974
(H4,H5,H6,H7,H8,H9,H10,H11)
(2)For EMI concern , add L118 & L119 for LIO power source and add L120 & L121 for RIO power source

20090109
Update Power schematic (Waiting for PWR change list)

20090109
Change Net name from SMB2_CLK/SMB2_DATA to BATCONSMBCLK/BATCONSMBDAT

20090112
(1)The EMI test result is PASS after SS enable , cancel L118/L119/L120/L121
(2)Add TP415 for RTC Power
(3)Change part for U571 from 15-STTS424-0001 to 15-STTS424-NA00
(4)Assign CN5017 Pin20/22 as LCD cable detection loop
Implement LVDS cable detection function , delete TP365 and add LCD_cable_Det# input for U36-Pin73(GPI7)
(Add R5367 to pull up for LCD_Cable_Det#)

2008/01/13
1.Delete Control ACIN OCP protect, EC Include
2.Delete PSID Circuit, follow H830 [Phelps]
3.Change 1.05VRUN/1.5VSUS power budget 10A to 8A

DVT2009.01.14
Follow SW suggestion to change LCD_Cable_Det# from U36-Pin73(GPI7) to SB GPIO1 and delete R5367 pull up resistor.

DVT 2009.01.16
(1)For L6 DFM concern , change RP5 from 1R-1010822-JX00 to 2pcs 1R-0000822-J100(R5367&R5368).
(2)Based on the Crystal test result , change R554 from 1R-0000000-J200(0 ohm) to 1R-0000224-F200(220K ohm)
(3)Chaned CN5018&CN5019 from 1N-0030007-FKG0 to 1N-0030009-FKG0 for Halogen Free purpose.

DVT 20090116-1
Follow ME request to delete H9

DVT 20090119
(1)For TE test request , add TP416 for +VCC_SUS_HDA
(2)For TE test request , add TP417 for VDDA
(3)To fix BIOS timer issue , change part for C412&C416 from 1C-2N20100-J000 to 1C-2N20180-J000.

DVT 20090120
Due to change WWAN LDO solution , cancel unnecessary +5VALW power source for CN5016

DVT 20090121
Follow ME Connector list to change CN22 from 1N-1204002-0000 to 1N-1204009-0000

DVT 20090121A
To fix OS timer accuracy issue change part solution as below.
(1)Y4 from 1F-X14M318-3001 to 1F-X14M318-2001.
(2)C592&C596 from 1C-2N20330-J000 to 1C-2N20270-J000

DVT 2009/01/22
Change signal from A_GND to GND for CN5019 Pin4&7

DVT2009.02.02
To fix Pure ShutDown(SYS_SHDN#) accuracy issue.
-- Implement Q5023(2N7002-7-F) to instead to Q23B(MMDT3904-7-F)
-- Implement Q5024(MMBT3904-7-F) to instead to Q23A(MMDT3904-7-F)

DVT 2009.02.05
Follow Samsung PM800 SSD SPEC to enhance +3VRUN power and cancel +5VRUN power
-- Changed CN5015 Pin36 from GND to +3VRUN
-- Changed CN5015 Pin39 from +5VRUN to GND
-- Due to cancel +5VRUN power , deleted C5163,C5164

DVT 2009.02.09
Corect signal name for CN49 Pin3&4 from SMB2_CLK/SMB2_DATA to BATCONSMBCLK/BATCONSMBDAT

DVT 2009.02.12
For ICT coverage request , change TP213,TP353,TP314,TP247 to 1X-TESTPT0-0032

DVT 2009.02.12A
(1) Deleted PJ1,PJ3,PC846,PC847 for EMI
(2) Change PQ107 from 17-TP610KT-1E00 to 17-S12301B-DS00
(3) Change PR791 from 0603 to 1206
(4) Change PR7 from 1R-0002323-F200 to 1R-0000363-F200 Wake-up seting 9.4V
(5)Added PR949 for DVT Derating
(6)Deleted R880,R881,C1005,C1006 and canceled CLK_PCIE_UWB/CLK_PCIE_UWB#

PT 2009/02/18
(1)To guarantee Power/Status LED can work normally
when EC in Deep Sleep mode(ALW power will be off) ,
change the power source from +5VALW to S185VLDO for CN5019 Pin28
-- Added R5370 for S185VLDO path
-- Reserved R5369 for +5VALW path
(2)To improve the Power sequency issue for +3VRUN/+1_05VRUN , chnaged the EN signal from RUN_ON1 to RUN_ON for +1_05VRUN.
-- Changed PR188,PC387 from mount to NC.
-- Added PR950 for RUN_ON control path.

2009.02.19
(1)To fix battery low charge issue , changed PR2 from 1R-200500L-FB00(0.05ohm) to 1R-200200L-FB00(0.02ohm)
(2)To reduce power consumption on battery mode , reserved DCIN_1 power source for OPVCC
-- Added PR951 for AMPSVIN power source select
-- Reserved PR952 for DCIN_1 power source select.

PT 2009.02.23
(1)To save more layout spacing , cancelled below parts after confirm with RF team.
(R5344~R5351 & C5184~C5191)
(2)Reserved C5197 & C5198 for RF request.
(3)Added R5371&R5372 for power consumption measurement

PT 2009.02.24
(1)Correct the pull high power source for PS_ID from +3VALW to +ECVCC.
To guarantee it can work well on S5.(battery only mode.)
(2)Added TP418 & TP419 for SI request.

PT 2009.02.25
(1)Added PC947,PC948 for acoustic issue
(2)Due to UWB is dropped , change PQ103 from 17-S12312B-DS00 to 17-S12304B-DS00.
(Cost down)

PT 2009.02.27
(1)Due to USB port for RJ45 dongle has to be assigned to 2nd EHCI (port 6), and defined on left IO.
Changed USB port on LIO from USB_1 to USB_6
(2)Deleted the unnecessary R5354.(R5356 can cover the same function for path select.)
(Rename Net name for R5356 Pin2 as LCD_BIST_EC Pin1 as LCD_BIST and modify head value from Mount to NC_)
(3)Added TP420(GND TP) for TP52. (SI request)
(4)To meet Net name rule , changed name from LCD_Cable_Det# to LCD_CABLE_DET#.
(5)Deleted unnecessary R5147.
(There is 10k pull up to 3.3V on HP jack side.)
(6)Changed head value for RP50,RP51 from Mount to NC_.
(Just reserved for debuging.)

(7)Implement RP52,RP53(Res Array to instead for R867,R868,R279,R284)
(8)Changed part for R524,R525 from 0201 to 0402
(9)Deleted R5369,R5370 to cancel LED power source option.
(Just recover to original +5VLAW power source for LED.)
(EC should turn on always power to drive LED and latch actuators when slider is activated under battery mode)
(10)Merged U5012B to U37B
(11)Deleted unnecessary +1_5VRUN , +3VRUN power source for CN5016.(UWB is dropped.)
-- Deleted L110,L111,C5151,C5152,C5153,C5154
(12)Deleted RC for DREFSSCLK/DREFSSCLK# to optimize layout routing in inner layers.
-- R893,R894,C1015,C1016
(13)Deleted TP412,TP361 and assign GPG0 as WIFI detection pin & GPG2 as WWAN detection pin.
-- Added R5373,R5374,R5375
(14)Changed power source for WIFI +3V from +3VSUS to +3VRUN.(CN5015 Pin2,4,6)
(15)Corected the connection for PD33-Pin1 from BAT_ALERT#_R to BATCONBT-
(16)Corrected head value for PR951,PR952 as below.
PR951 ==> from Mount to NC_
PR952 ==> from NC_ to Mount
(17)Del unnecessary signal - DDPC_CTRLCLK
(18)Implement LCD BIST control finction from SB/EC control.
(19)Reserved PC945 & PC946 &PC949 &PC950 & PC951 &PC952&PC953 &PC954& PC955&PC956& PC957 for acoustic issue
(20)Changed PR825 from 1R-0000103-J200 to 1R-0000104-J200 for power consumption improvement.

PT 2009.03.01
(1)Correct signal connection for CN13 Pin9&10(SWAP)
(2)Follow Realtek design guide to change C5100 from 4.7uF to 10uF.
(3)Follow Code design guide to swap location between R5150&C5119
(4)Changed PGP1 form close jump(1X-JUMP000-0007)to 0ohm(1R-0000000-J300)
(5)Merge single 2N7002 Q22&Q5023(17-2N70027-F000) to Dual 2N7002 Q5025A,Q5025B(17-2N7002D-W000)
(6)Changed L117(1L-BBLM06P-G101) to R5148 0ohm(1R-0000000-J300)
(7)Changed U5012 from 14-74LVC1G-3200 to 14-NC7S32M-5X00
(8)Added Decouping Cap for logic ic power.
-- C644 ~ C450
(9)Added test point for H_A#25 & H_A#17
(10)Changed PO78,PQ79,PQ80 from Si7121DN-T1-E3 to Si7121DN-T1-GE3(Halogen free)
(11)Adjust pin assignment for CN5015 to add two +3VRUN power pin.
(12)To enhance connector SMT reliability , implement additional GND pin for CN5016
(13)Implement ALWPWR_WAKE_UP function on CN5019-Pin23 & U36-Pin

PT2009.03.02
(1)Changed Pull up power source for WWAN_DET# from +3VRUN to +3VSUS
(2)To improve power consumption , changed PD47 from Mount to NC_.
(3)Changed power source for OZ71REF_EN from AMPSVIN9V to +ECVCC and changed PR822 from Mount to NC_
(4)For layout spacing concern changed U5012 from 14-NC7S32M-5X00 to 14-74LVC1G-3200
(5)For part consistence , changed U30 from 14-NC7S32M-5X00 to 14-74LVC1G-3200.(Same as U5012)
(6)Merged U5013,U5014(single OR gate) to U5015(Dual OR gate)
(7)Followed Intel suggestion to add 6pcs 0.1uF Decap for VHCORE power. (C239~C244)
(8)To setting the suitable wake up voltage , changed PR7 from 36Kohm to 10Kohm and PR823 from 97.6Kohm to 324Kohm

PT 2009.03.02B
To meet +3VRUN power budget , changed PQ106 from 17-S12312B-DS00 to 17-S15480D-UT00
PT 2009.03.03_C
Changed pin assignment for CN5019 to separate D/A
PT 2009.03.04
Follow ME request to change H4~8,H10,H11 from 1X-HOLE000-0974 to 1X-HOLE000-1062
PT 2009.03.04_B
Corrected signal name for ALWPWR_WAKE_UP ==>ALWPWR_WAKE_UP#
PT 2009.03.04_C
(1)Changed C5162 from 33pF to 0.1uF.
(2)Deleted C651.

PT 2009.03.05
Changed GND for C5193 from P_GND to GND.
PT 2009.03.06
(1)Due to material preparation L/T issue , changed PU8 from 15-RT91981-0001 to 15-RT91981-0000.
(2)Follow ME request to change H11 from 1X-HOLE000-1063 to 1X-HOLE000-0974
(3)Deleted TP113,TP115 for DMI_RXN1/DMI_RXP1.
(4)Deleted BIST control function from SB

PT 2009.03.09
(1)Due to material purchase concern , changed U5015 from 14-SN74LVC-2G02 to 14-NL27W23-2U00
(2)Backward PS_ID Pull Up power source to +3VALW

PT 2009.03.09_C
(1)For layout spacing concern , c hanged R241 from 0402 to 0201
(2)Follow ME request to add NUT1 & RING1 & RING2

PT 2009.03.11
Add TP235(ICH9-GPIO20) for ICT request.
PT 2009.03.12
Changed R241 from 4.7K 5% to 4.7K 1%
PT 2009.03.16
(1)Changed D8 & R188 from Mount to NC_.(No sequence concern.)
(2)Changed D28 from Mount to NC_
(3)Changed R18 & R64 from 2.2Kohm to 0ohm.
(4)Changed R283 from 2.2Kohm to 0ohm

2009/03/30
For Exponent test purpose , changed
PQ107&PR791&PR949 from NC_ to Mount

Title	PT Changelist	
Size A2	Document Number H800 MB	Rev X-Build
Date: Wednesday, October 07, 2009	Sheet 46 of 50	

PT2 2009.04.20
To fix GPIO function limitation(GPE0 is no function when system in S5) ,
changed ALWPWR_WAKE_UP# from GPE0 to GPE6.
(Deleted TP353 for GPE6 & Added TP426 for GPE0)

PT2 2009.04.27
To improve SMT reliiability issue , implemented new part footprint for
PQ5,PQ6,PQ7,PQ10,PQ11,PQ97,PQ99,PQ106,PQ108

PT2 2009.04.30
To support Bridge Battery function , implement S_BATT_EN for EC GPIO GPC5(Pin57)
(Deleted TP348)
(2)To support Bridge Battery function , implement necessary Power/control signal for CN5016
S_BATT_EN
DCIN_1
AMPSVIN

PT2 2009.05.04
(1)Follow ME DXF to deleted H11
(2)Implement PWRLED & STSLED PWM control for EC to support Power LED & Status LED control in Mech. Latch case.
(3)Added RP55 & RP54 for the path select function.
If RP55 Mount / RP54 NC : PWM control function by EC.
If RP55 NC / RP54 Mount : I2C Bus connection between Cypress uC(Latch FPC) & EC.

PT2 2009.05.05
(1)To improve the HP Crosstalk issue , changed CN5019-Pin3 from GND to A_GND
(2)To fix the timing issue for VCCRTC to RTCRST# , changed part value for R19 from 13Kohm to 17.8Kohm.
(3)To reduce leakage , changed part value for PR857, PR869, PR883, PR886 from 10Kohm to 100Kohm.
(4)Change part for PL3&PL5 from Lead free to Halogen free.
(FDVE0630-2R2M=P3 to FDVE0630-H-2R2M=P3.)
(5)Change part for PL7 from Lead free to Halogen free.
(FDU1235-R47M=P3 to FDU1235-H-R47M=P3.)

PT2 2009.05.06
(1)Added TP241 for I2C_DAT3
(2)For USB 5V power drop concern ,
changed part value for PR864&PR867 to rise +5VALW power level.
PR864 : 91Kohm to 84.5Kohm
PR867 : 10Kohm to 9.1Kohm

PT2 2009.05.07
To fix ghost key issue , mount RP50/RP51 as external pull high.

Title	PT2 Changelist	
Size A2	Document Number H800 MB	Rev X-Build
Date: Wednesday, October 07, 2009	Sheet 47 of 50	

ST 2009.05.22
To fix sense issue for system shudown of SMSC1422 , added Q27 to change the connection of SYS_SHDN# from Source to Gate of MOS.

ST 2009.05.22
To meet Dell requirement , added WWAN_PWR_EN control to separate the WWAN device/power control.

ST 2009.05.25
(1)To fix power noise issue , added C5199(1uF Cap) for +5VALW .
(2)Changed part for PD35 from 15V rating to 5V rating and follow EMI suggestion to connect PD35-1 from ADADJ to OZ71CONT.
(3)Follow Dell requirement to implement PS_ID circuit.
(4)To guarantee the suitable power level output when air adapter condition(14V~19V) , added PC11,PD45.

ST 2009.5.27
(1)Deleted close Gap PJ4,PR10,PR18,PR19 and changed net name form AMPSVINS185V to AMPSVIN
(2)Deleted Close Gap PJ15 and change net name form S185VOUT to +5VALW.
(3)Deleted Close Gap PJ16,PR11,PR21 and changed net name form AMPSVINS183V to AMPSVIN
(4)Deleted Close Gap PJ7 and changed net name form S183VOUT to +3VALW.
(5)Deleted close Gap PJ10,PR12,PR23 and change net name form AMPSVINM00 to AMPSVIN
(6)Deleted Close Gap PJ11,PJ12 and changed net name form +1_5VSUS_1 to +1_5VSUS
(7)Deleted Close Gap PJ18,PR13,PR24 and changed net name form AMPSVINM8792 to AMPSVIN.
(8)Deleted Close Gap PJ19,PJ20 and changed net name form 8792_FB to +1_05VRUN.
(9)Deleted Close Gap PJ14,PR15,PR16 and changed net name form AMPSVIN_ISLVIN to AMPSVIN.
(10)To fix hang up issue(Post code:0x86) ,added R5379 as termination Res.

ST 2009.06.01
Follow the suggestion from SMSC FAE to reserve C382(0.1uF) for RC delay reuqest.

ST 2009.06.02
Removed 75ohm termination Res.--R5379

ST 2009.06.02B
To fix the RTCRST# timing issue ,
changed part value for R19 from 17.8Kohm to 22Kohm and R565 from 13Kohm to 22Kohm.

ST 2009.06.02B
To fix the Ripple /Noise issue for +5V power ,
changed part for PC949 from TEPSLD1A227M(25)12R to TLPSLV0J227M(15)12RE.
(Lower ESR)

ST 2009.06.02B
To fix the Ripple /Noise issue for +5V power ,
changed part value for PR860 from 100K to 75K

ST 2009.06.02B
Corrected signal name as below.
I2C_DAT3_STSLED ==> I2C_DAT3_STSLED_AMBER
I2C_CLK3_PWRLED ==> I2C_CLK3_STSLED_WHITE
PWRLED_PWM ==> STSLED_WHITE_PWM
STSLED_PWM ==> STSLED_AMBER_PWM

ST 2009.06.03
To fix timing accuracy issue , changed part value for C648&C649 from 10pF to 8pF.

ST 2009.06.09
Follow adapter ground linear resistance to adjust part value for PR832,PR835
PR832 : 4.87Kohm to 118Kohm
PR835 : 31.6Kohm to 768Kohm

ST 2009.06.09B
(1)To fix noise issue when Codec initial , changed C5112 from mounted to NC_.
(2)Corrected signal name from WWAN_EN to WWAN_RF_EN
(3)To drop HDD LED function from ST , reserved below parts from mount to NC_
R5164,Q26,R562,LED3
(4)Correcded signal name from HW_POP_MUTE_EC# to HW_POP_MUTE_EC

ST 2009.06.24
(1)To fix derating concern for air adapter condition(14V~19V) , changed part value for PR905,PR914 from 2.2Kohm to 4.7Kohm.
(2)To fix derating concern for air adapter condition(14V~19V) , changed part value for PC932 from 0.1uF_16V to 0.1uF_25V.
(3)To improve ripple noise for +3VALW/+5VALW , NC PC882&PC896
(4)To fix derating concern , changed part value for PC885 from 0.1uF_6.3V to 0.1uF_25V
(5)To control Impedance accurately , implement Impedance coupon on MB.
(6)To fix USB 5V power drop issue , changed part value for PR864.PR867
PR864 : from 84.5Kohm to 110Kohm
PR867 : from 9.1Kohm to 12Kohm

ST 2009.06.29
(1)Update Block Diagram
(2)To fix Slew issue for DREFSSCLK/DREFSSCLK# , changed Clock Gen.(U29) from SL28541BQCJ to 9LRS3165BKLFT.
(3)Reserved R5379/R5380 as path select for HW_POP_MUTE_EC control function.

ST 2009.06.29B
Due to Die-transfer from D to E , changed Part for U62~U69 from K4B1G0846D-HCF8 to K4B1G0846E-HCF8

ST 2009.06.30
(1)Follow JEDEC Standard to implement 75ohm terminator(R5381) for unused M_CLK_DDR1/M_CLK_DDR#1
(2)To fix the DP source detection issue when system in S5 , changed power source for DPAUXN_C pull up & U5011 switch power from +3VRUN to +ECVCC

ST 2009.07.01
(1)Implement special footprint(qfn_65p_20_354x354_th118_H800) that set thermal pad as 3mmx3mm for U29
(2)Implement suitable Symbol/Footprint(H86) for Impedance coupon on MB.

ST 2009.07.02
(1)For BFT test request , changed TP size from tpc20t_50 to TPC35T_75 for TP52/TP420
(2)For height limitation concern , changed part size from 0402 to 0201 for R5381

ST 2009.07.02B
To fix the DP source detection issue when system in S5 , changed power source for CA_DET_Q pull up power from +3VRUN to +ECVCC

ST 2009.07.03
For DFM concern , implemented special footprint to improve SMT quality.
PQ5,PQ6,PQ7,PQ10,PQ11,PQ97,PQ99,PQ106,PQ108

ST 2009.07.07
For ESD concern , changed part for Q25 from 2N7002-7-F to 2N7002A-7(with ESD diode)

ST 2009.07.07B
(1)Deleted unnecessary PJ2(Open GAP for GND)
(2)For fix EMI issue , added SPR1 & SPR2

ST 2009.07.09
For height limitation concern , deleted SPR1

ST 2009.07.13
To prevent the abnormal short between LCD_CABLE_DET#(Pin22) & AMPSVIN_LCD(Pin23) when cable assy ,
changed pin define for CN5017-pin23 from AMPSVIN_LCD to NC.

ST 2009.07.21
To fix the DP source detection issue completely when system in S5 , backward pull high power source for CA_DET_Q/DPAUXN_C/U5011 VDD to +3VRUN.
And move Pull high/Pull down Res(R891/R890) connection from switch input to switch output.

ST 2009.07.22
To fix ESD issue , changed H5~H8 from PTH Hole to NPTH Hole.
(Cut off the path from Keyboard to system GND.)

ST 2009.07.23
To fix the derating issue(Vgs) , changed part for PQ98 from Si2312BDS(8V) to Si2306(20V)

ST 2009.07.27
To fix the derating issue(Vgs) , changed part for PD47 from UDZSTE-179.1B to UDZSTE-1715B.
(Fix AMPSVIN9V level is 15V when air adapter input.)

ST 2009.07.30
To control BOM for option WWAN function , changed the head value for related parts from Mount to WWAN_
Page33 : C5147,C5148,L108
Page26 : R5375

ST 2009.08.03
Follow adapter ground linear resistance to adjust part value for PR832,PR835
PR832 : 118Kohm to 143Kohm
PR835 : 768Kohm to 931Kohm

ST 2009.08.06
Follow adapter ground linear resistance to adjust part value for fixed adapter watt.
NC PR952,PR831,PR843,PR844,PR838,PR839,PU6,PU7
PR834,PR836,PR837 Change part value to 0 ohm.

ST 2009.08.28
(1)
To fix USB 5V power drop issue ,
backward part value for PR864.PR867 to enhance +5VALW level
PR864 : from 110Kohm to 84.5Kohm

(2)(ECN:CDNRDS0908009)
To fix maximum power limitation function , changed part value for PR832,PR835
PR832 : from 143Kohm to 60.4Kohm
PR835 : from 931Kohm to 30.1Kohm
PR867 : from 12Kohm to 9.1Kohm

(3)
To fix the rise time SI issue for Batt SMBus , changed part value for RP33.
From 10Kohm(1R-1010103-JP00) to 4.7Kohm(1R-1010472-JP00)

ST 2009.09.10
To support complete vendor P/N & part description , changed part for PD45 from 16-UD2S51B-0001 to 16-UD2S51B-0000

Title: ST Changelist		
Size: A2	Document Number: H800 MB	Rev: X-Build
Date: Wednesday, October 07, 2009	Sheet 48 of 50	

ST2 2009.09.16
To fix hang up issue , implement below solution for VR design.
(1)Reserved PR953 for H side MOS(PQ3) rise timing adjustment.
(2)To reduce Spike for AMPSVIN_ISLVIN , added PL26,PL27 for PQ3(VR H side MOS) VIN.
(3)To reduce Spike for AMPSVIN_ISLVIN , follow Intel CRB(Rev1.01) to add 4pcs 0.01uF cap(PC958~PC961)

ST2 2009.09.17
Co-layout PL28,PL29 for Inductor solution.

ST2 2009.09.17B
To get better brightness linearity , added EC control signal(EC_BRADJ) and reserved R5382,R5383 for path selection.

ST2 2009.09.18B
Follow the suggestion from PWR team , corrected part for PL28,PL29 from BLM21PG331SN1 to LQM21PNR47MC0D

ST2 2009.09.28
To support blacklight control function by EC side , changed control circuit path from GMCH to EC.
R5382 : From Mount to NC.
R5383 : From NC to Mount.

Title: ST2 Changelist		
Size: A2	Document Number: H800 MB	Rev: X-Build
Date: Wednesday, October 07, 2009	Sheet 49 of 50	

X-Build 2009.10.12
Disabled external SPI ROM boot function and changed part value as below.
From Mount to NC : U30,C643,R267,CN13
From NC to Mount : R566

X-Build 2009.10.12
Disabled test fan function and changed part value for CN51 from Mount to NC.

Title	X-Build Changelist		
Size A2	Document Number H800 MB		Rev X-Build
Date: Monday, October 12, 2009	Sheet 50 of 50		