Acer Flamingo

01200_SD

Project code:
PCB P/N:
REVISION:

PCB LAYER

- L1: Signal 1(X)
- L2: GND
- L3: Signal 2 (Y)
- L4: Signal 3 (X/Y)
- L5: GND
- L6: POWER
- L7: Signal 4(weak)
- L8: Signal 5 (X)
- L9: GND
- L10:Signal 6 (Y)

CLK GEN.
ICS
PAGE:03

Mobile CPU
Tualatin
verson :
PAGE:4~5

HOST BUS (133M)

RAM BUFFER (2*32bit)*2

SO-DIMM*2
PAGE:10

(133M) MEM BUS

Almador-M
GMCH
Version : A4
PAGE:7~9

(66M) AGP 4X

VGA
ATI Mobility M6S
version:
PAGE:11~12

CRT
PAGE:13

LCD
PAGE:13

HUB I/F (66M)

ATA100

PRIMARY EIDE
HDD
PAGE:18

HOT PLUG

SECONDARY EIDE
CDROM
PAGE:18

USB 1.0X2
PAGE:19

ICH3-M
Version :
PAGE:15~17

LAN
82562EM
PAGE:20

DOCK V

TV OUT

PCI BUS (33M)

POWER SW
MIC2564A
PAGE:22

DOCK V

QSW

CARDBUS
OZ6933T
PAGE:21

CARDBUS
SLOT A,B
PAGE:22

AC-Link

LPC BUS (33M)

LINE IN

INT.SPKR

LINE OUT

OP AMP
APA2020
PAGE:25

VR

MIC

AC'97 CODEC
ALC200
PAGE:23

MODEM Daughter Card
PAGE:19

SMsC SIO
LPC47N267
PAGE:27

KBC
M38859
PAGE:26

FWH
82802AB
PAGE:29

LPC DEBUG CONN.
PAGE:29

CMOS BAT

FIR
PAGE:27

FLOPPY
PAGE:18

PRINTER
PAGE:28

SERIAL
PAGE:28

FINGER PRINTER
PAGE:27

TOUCH PAD
PAGE:28

INT. KB
PAGE:26

PS/2 CONN
PAGE:26

DC/DC&CHARGER
Switching Power
MAX1632/MAX1772

INPUTS	OUTPUTS
DCBATOUT	+6V
AD+	+5VSB
	+3.3V
	+5V
	+12V
	CD+5V
	PAGE:32

CPU DC/DC
Switching Power
MAX1718/MAX1714

INPUTS	OUTPUTS
DCBATOUT	+VCC_CORE
	+VCCT
	PAGE:30/31

OTHER DC/DC
MAX1644/MAX1792
MAX8863

INPUTS	OUTPUTS
+5V	+1.8V
+3.3V	+1.5V
LAN_+3.3V	+3VSB
+5VSB	+1.8VSB
	+3.3V
	PAGE:31/32

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Taiwan, R.O.C.

Title: Block Diagram
Size: A3
Document Number: Acer Flamingo
Rev: SB
Date: Thursday, July 05, 2001
Sheet 1 of 38

Acer Flmanigo History

Rev. 0.1 : Jun. /1 / 2001 for PCB team placement

Acer Incorporated
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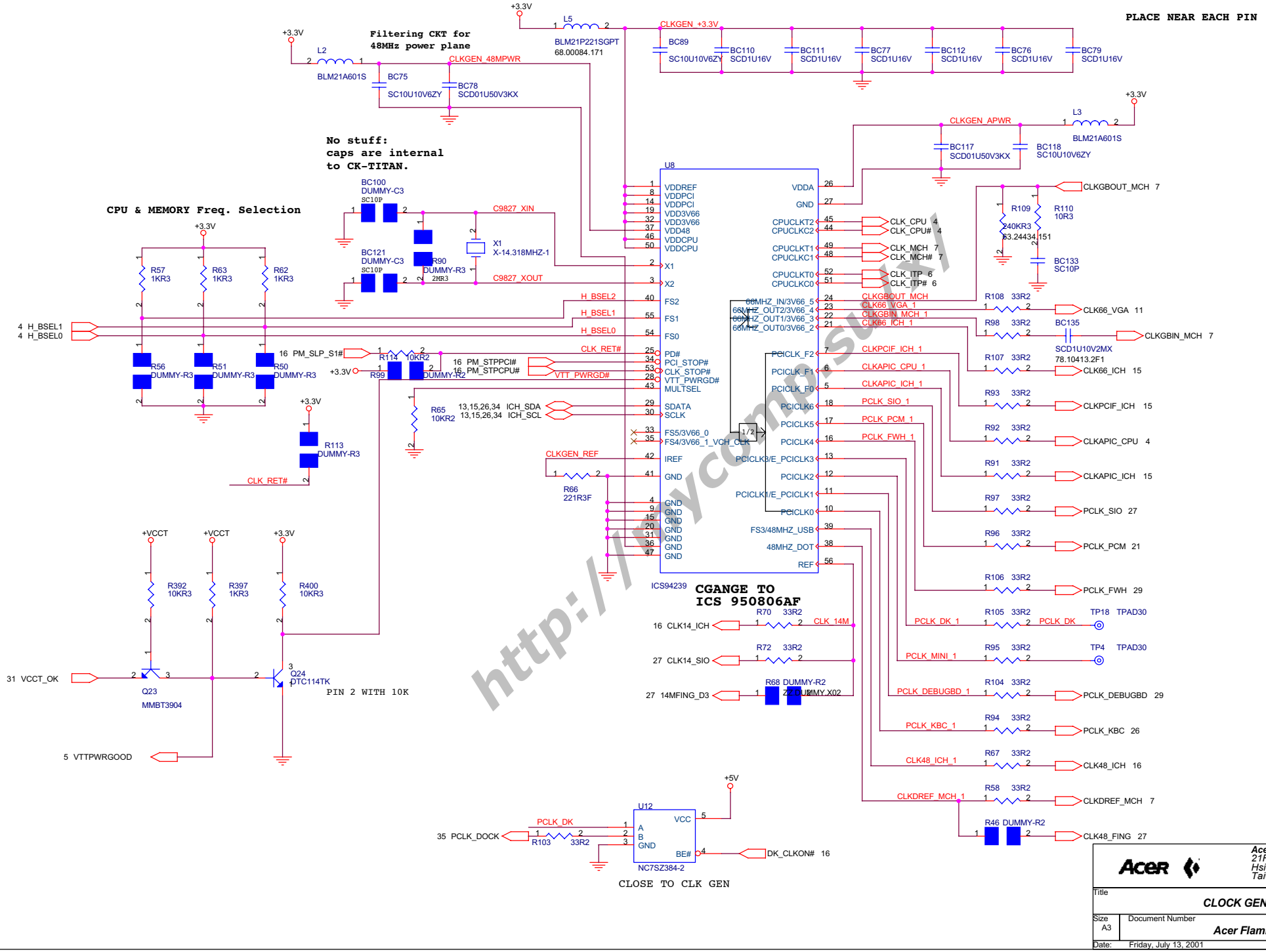
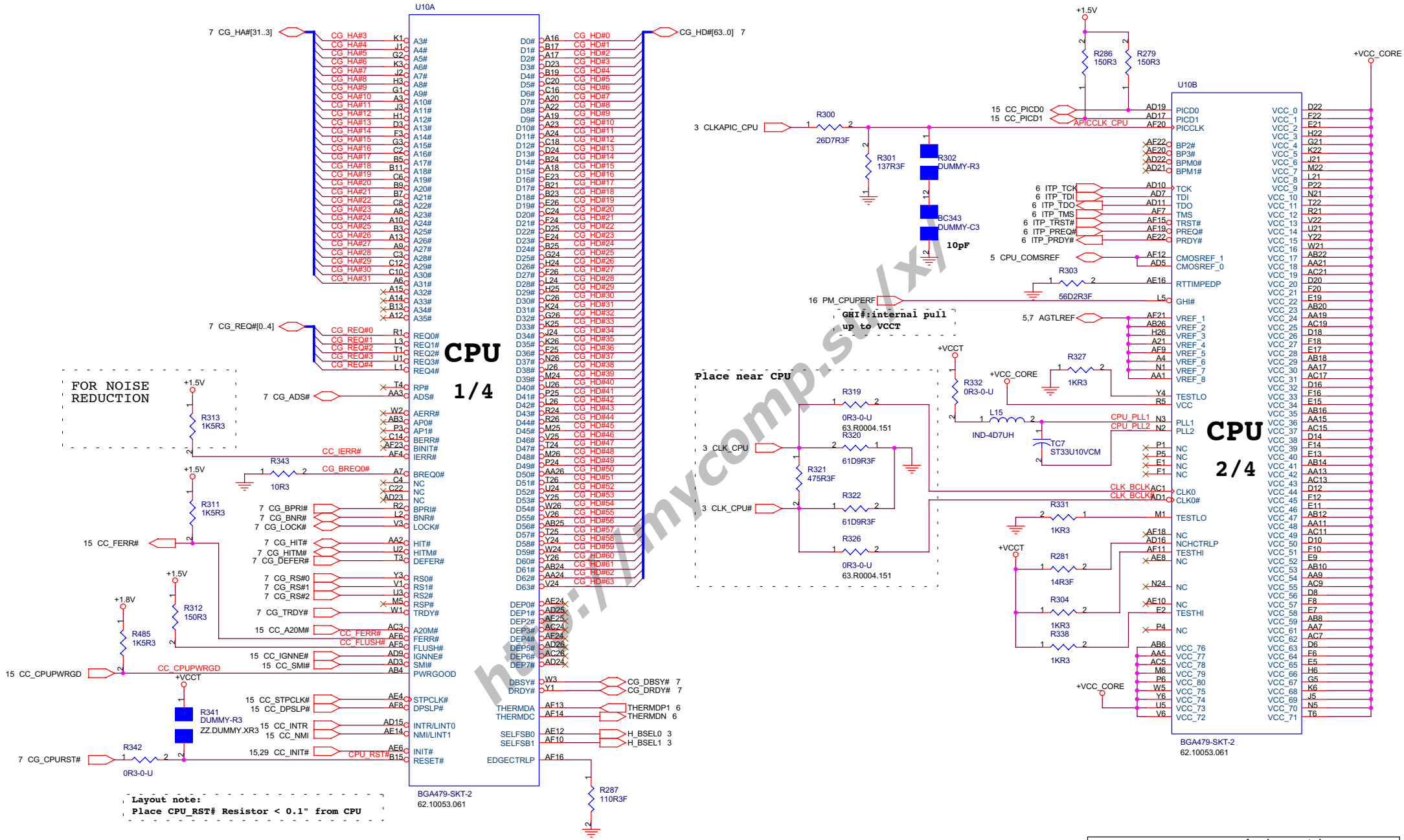
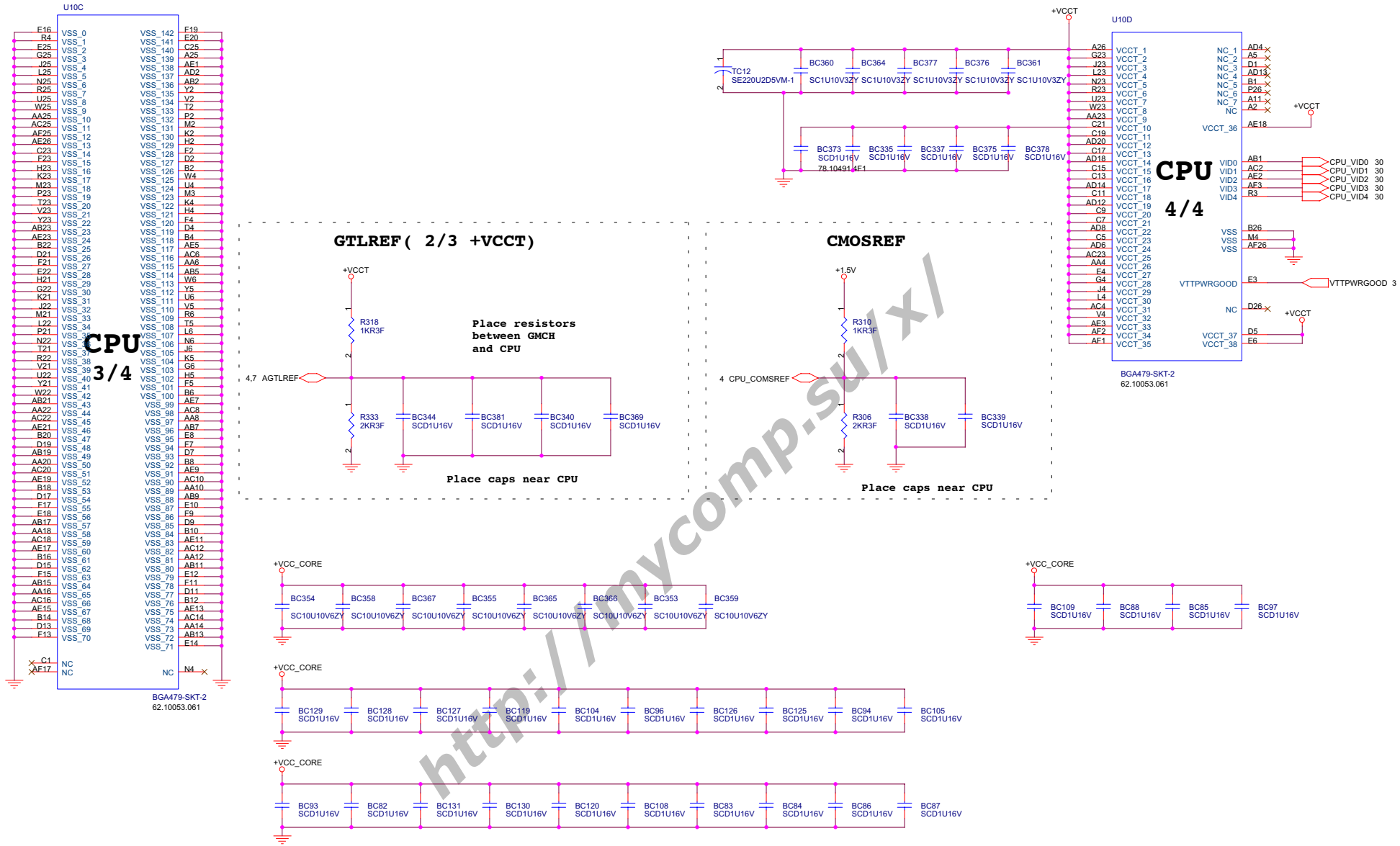
Taiwan, R.O.C.

Title	REVISION HISTORY	
Size: A3	Document Number: Acer Flamingo	Rev: SB
Date: Monday, May 14, 2001	Sheet 2 of 38	



Acer Incorporated	21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	CLOCK GENERATOR
Size	A3
Document Number	Acer Flamingo
Rev	0.1
Date:	Friday, July 13, 2001
Sheet	3 of 38





Decouping Recommendation

				Freeza	Kodiak Ver. 0.5
VCC_CORE	Underneath balls on solder side	0.47uF * 24	Use 2-3 vias per pad for reduced inductance during layout	0.1uF * 24	10uF / 6.3V * 12
	On the peripheral near balls	10uF / 6.3V * 10	Placement should be near processor for all	10uF / 10V * 10	10uF / 6.3V * 10 + 6 * NS
	Bulk Caps			220uF / 2.5V * 8	150uF / 4V * 12 + 2 * NS
VCCT	Place close to processor for all	1uF * 10	Use 2 vias per pad for reduced inductance during layout	1uF * 10	1uF * 10 + 2 * NS
	Bulk Caps			220uF / 2.5V * 2	150uF / 4V * 5 + 1 * NS

Almador-M Checklist Ver. 0.5 8/28

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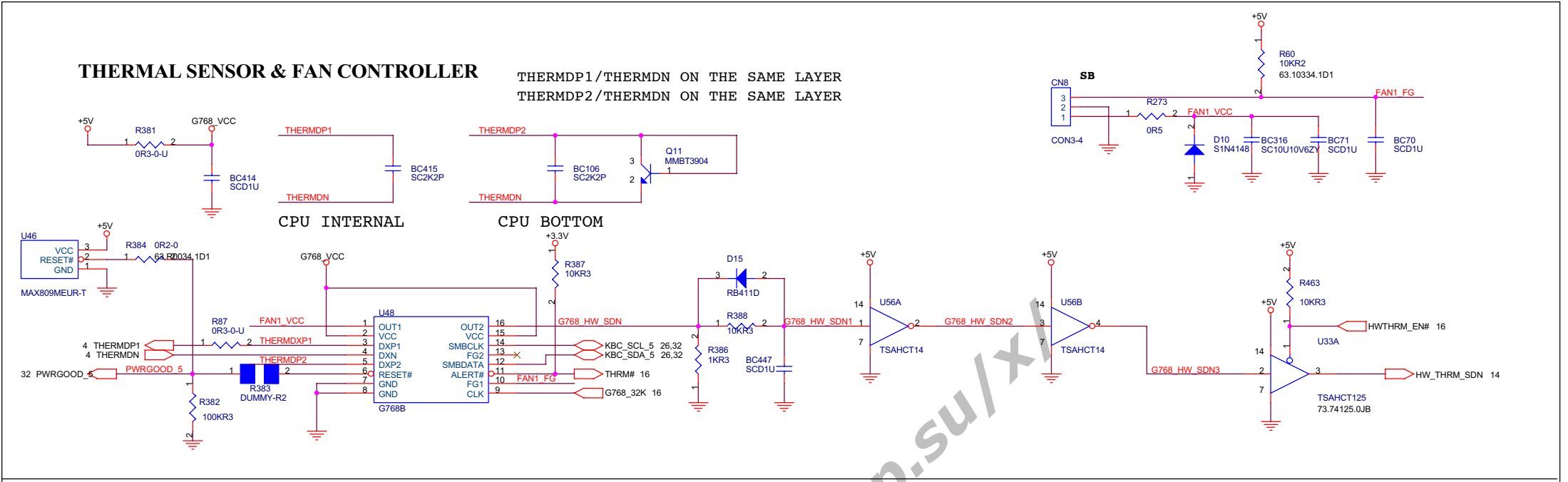
Title: CPU 2/2 CONFIGURATION

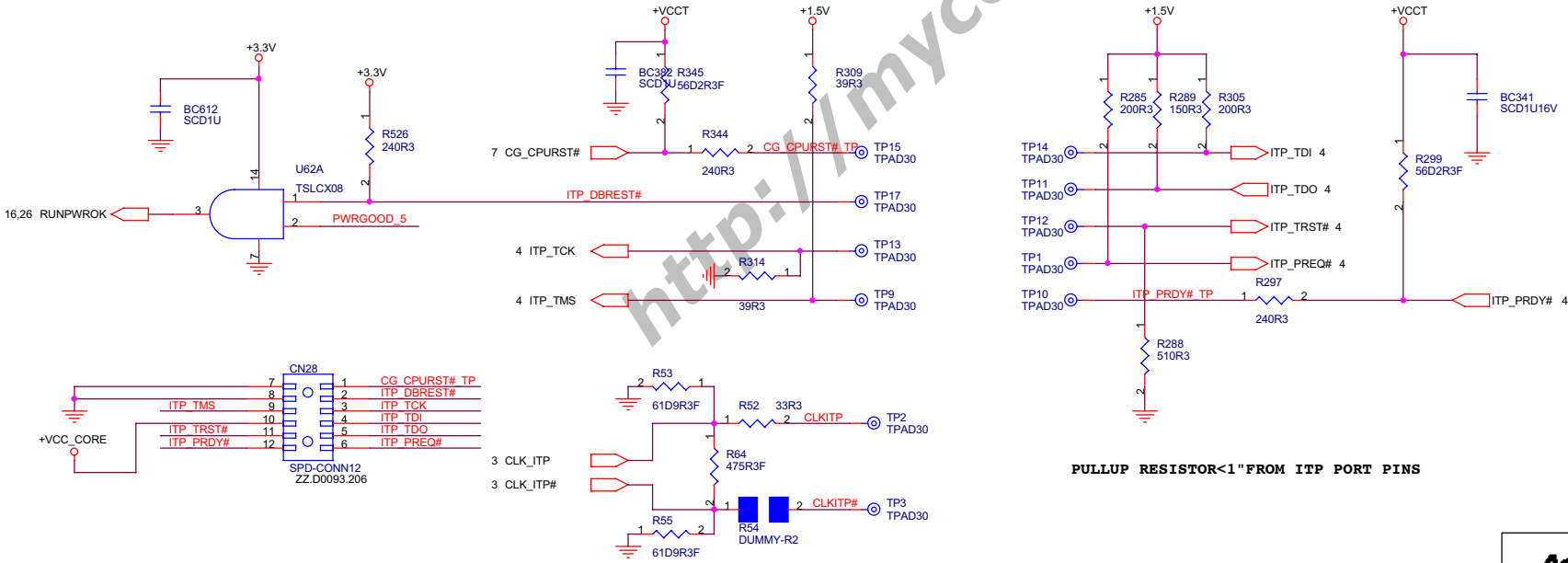
Size: Custom | Document Number: Acer Flamingo | Rev: SB

Date: Friday, July 13, 2001 | Sheet 5 of 38

THERMAL SENSOR & FAN CONTROLLER

THERMDP1/THERMDN ON THE SAME LAYER
THERMDP2/THERMDN ON THE SAME LAYER





PULLUP RESISTOR<1"FROM ITP PORT PINS

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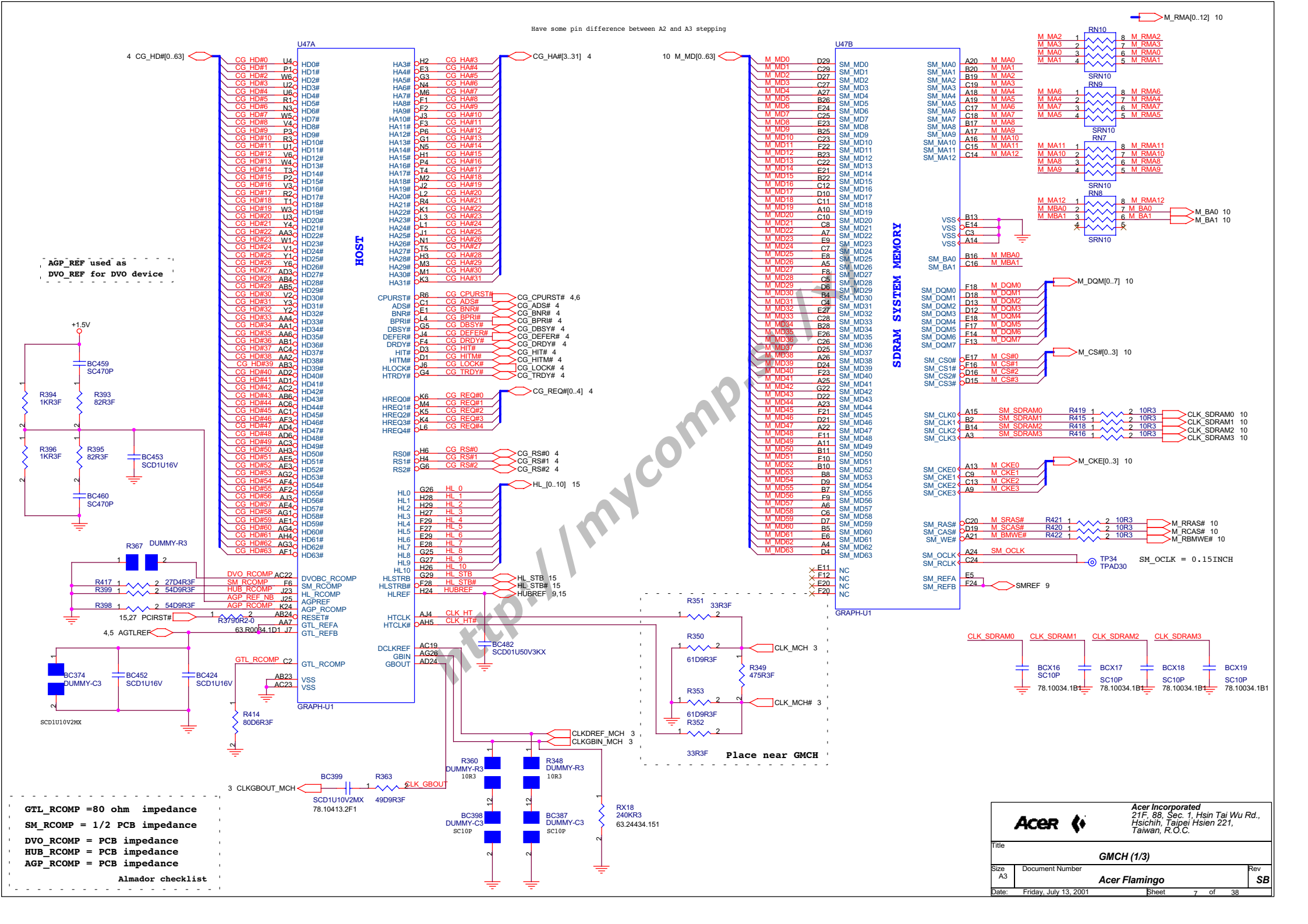
Title: THERMAL SENSOR/FAN/ITP

Size	Document Number	Rev
A3	Acer Flamingo	SB

Date: Friday, July 13, 2001 Sheet 6 of 38


Have some pin difference between A2 and A3 stepping
U47A
HOST
GRAPH-U1
U47B
SDRAM SYSTEM MEMORY
GRAPH-U1
AGP_REF used as
DVO_REF for DVO device
GTL_RCOMP =80 ohm impedance
SM_RCOMP = 1/2 PCB impedance
DVO_RCOMP = PCB impedance
HUB_RCOMP = PCB impedance
AGP_RCOMP = PCB impedance
Almador checklist
Place near GMCH
SM_OCLK = 0.15INCH
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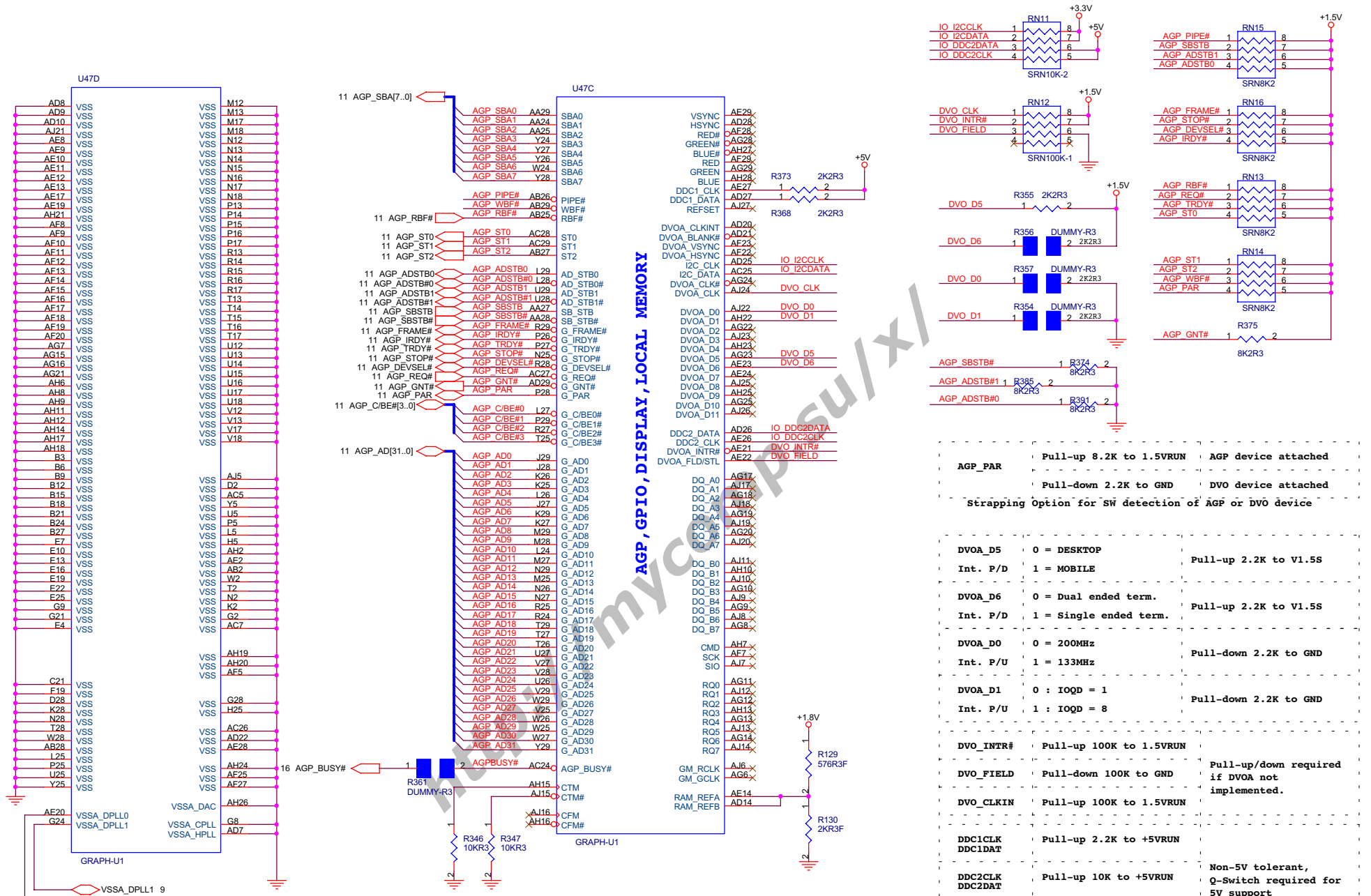
Taiwan, R.O.C.
Title
GMCH (1/3)
Size A3
Document Number
Acer Flamingo
Rev SB
Date: Friday, July 13, 2001
Sheet 7 of 38



AGP_PAR	Pull-up 8.2K to 1.5VRUN	AGP device attached
	Pull-down 2.2K to GND	DVO device attached

Strapping Option for SW detection of AGP or DVO device

DVOA_D5 Int. P/D	0 = DESKTOP 1 = MOBILE	Pull-up 2.2K to V1.5S
DVOA_D6 Int. P/D	0 = Dual ended term. 1 = Single ended term.	Pull-up 2.2K to V1.5S
DVOA_D0 Int. P/U	0 = 200MHz 1 = 133MHz	Pull-down 2.2K to GND
DVOA_D1 Int. P/U	0 : IOQD = 1 1 : IOQD = 8	Pull-down 2.2K to GND
DVO_INTR#	Pull-up 100K to 1.5VRUN	Pull-up/down required if DVOA not implemented.
DVO_FIELD	Pull-down 100K to GND	
DVO_CLKIN	Pull-up 100K to 1.5VRUN	
DDC1CLK DDC1DAT	Pull-up 2.2K to +5VRUN	Non-5V tolerant, Q-Switch required for 5V support
DDC2CLK DDC2DAT	Pull-up 10K to +5VRUN	
I2CCLK I2CDATA	Pull-up 10K to +3VRUN	

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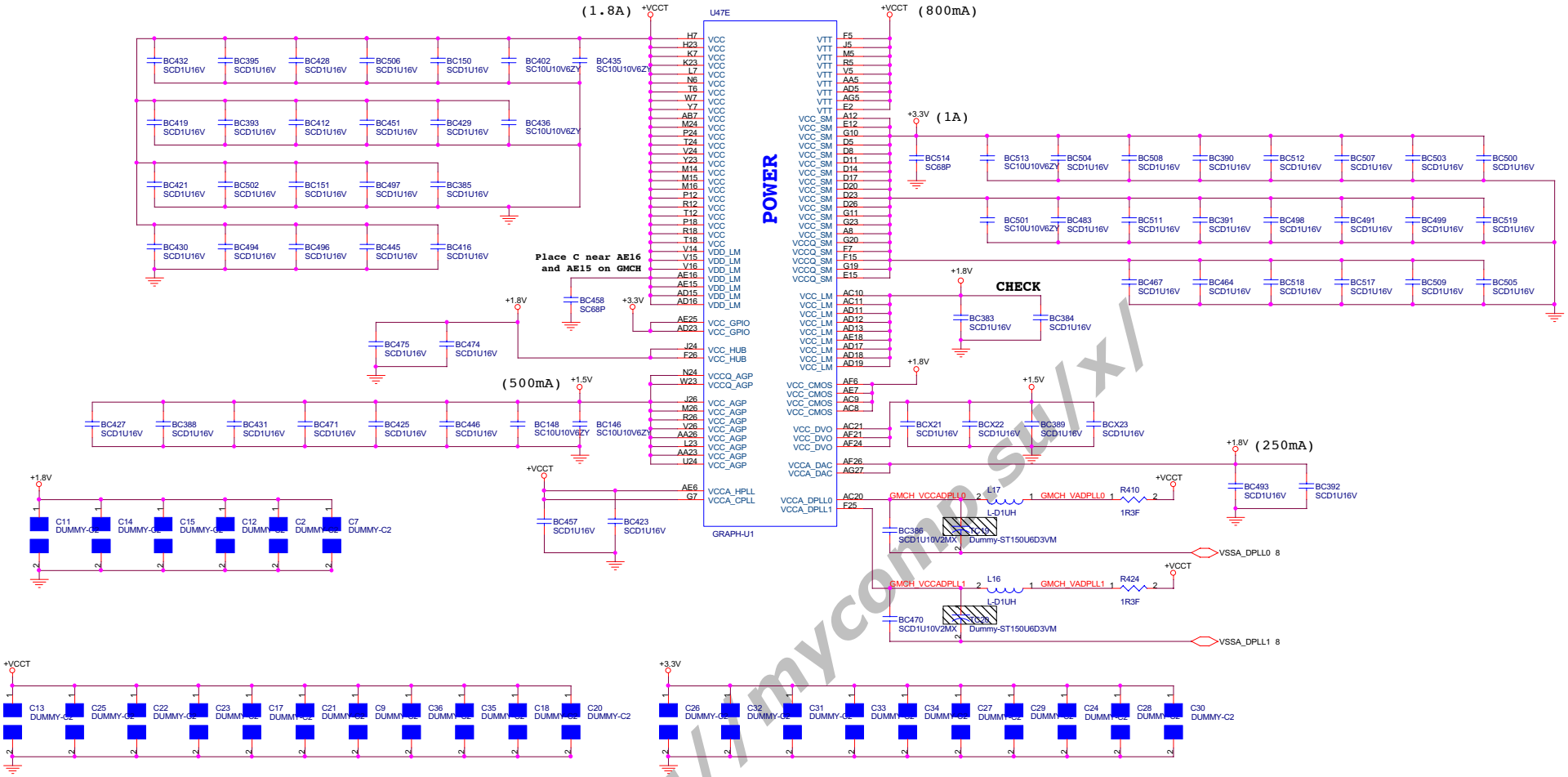
Title	GMCH (2/3)	
Size A3	Document Number: Acer Flamingo	Rev SB
Date: Friday, July 13, 2001	Sheet 8 of 38	

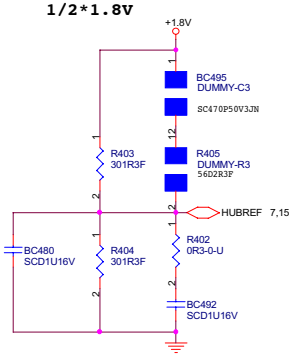


Decoupling Recommendation

				Freeza	Kodiak Ver. 0.5
V1.2S_GMCH	Decoupling Caps	0.1uF * 20	Distribute as close as possible to GMCH-M processor Quadrant		1uF * 20
	Bulk Caps			0.1uF * 20	150uF / 4V * 5 + 1 * NS
V1.2S_GMCHCORE	Decoupling Caps	68pF * 1	Close to VDD_LM, near pins AE15 and AE16 on Almador	100uF / 10V * 2	
		0.1uF * 40		68pF * 1	68pF * 1
	Bulk Caps				1uF * 40
V1.5S_GMCH	Decoupling Caps	0.1uF * 9	Distribute as close as possible to GMCH-M AGP/DVO Quadrant	0.1uF * 8	150uF / 4V * 10 + 1 * NS
		82pF * 4		0.01uF * 3	0.1uF * 9
	Bulk Caps			10uF / 10V * 1	82pF * 4
V1.8S_GMCH	Decoupling Caps	0.1uF * 4 + 4	Distribute as close as possible to GMCH-M Local Memory Quadrant	100uF / 10V * 1	22uF / 20V * 1
		82pF * 2	Additional 4* 0.1uF shall be distributed as close as possible to VCCPCMOS_LM	0.1uF * 2	0.1uF * 4 + 2
	Bulk Caps				82pF * 2
V3_GMCH	Decoupling Caps	0.1uF * 12 + 2	Distribute as close as possible to GMCH-M System Memory Quadrant		22uF / 20V * 2
		82pF * 4	Additional 4* 0.1uF shall be distributed as close as possible to IO Quadrant		68uF / 10V * 5
	Bulk Caps			0.1uF * 20	0.1uF * 12 + 2
				100uF / 10V * 1	82pF * 4
					22uF / 20V * 2

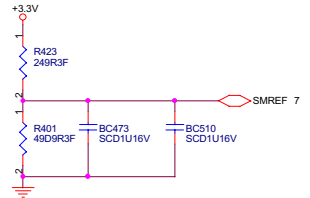
Almador-M Checklist Ver. 0.5 8/28

HUB INTERFACE REF 1/2*1.8V



Layout Note:
Place divider pair in middle of bus.
Place capacitors near GMCH.

SYSTEM MEMORY REF 0.55V



Place capacitor near GMCH.

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Title	GMCH(3/3)	
Size: Custom	Document Number: Acer Flamingo	Rev: SB
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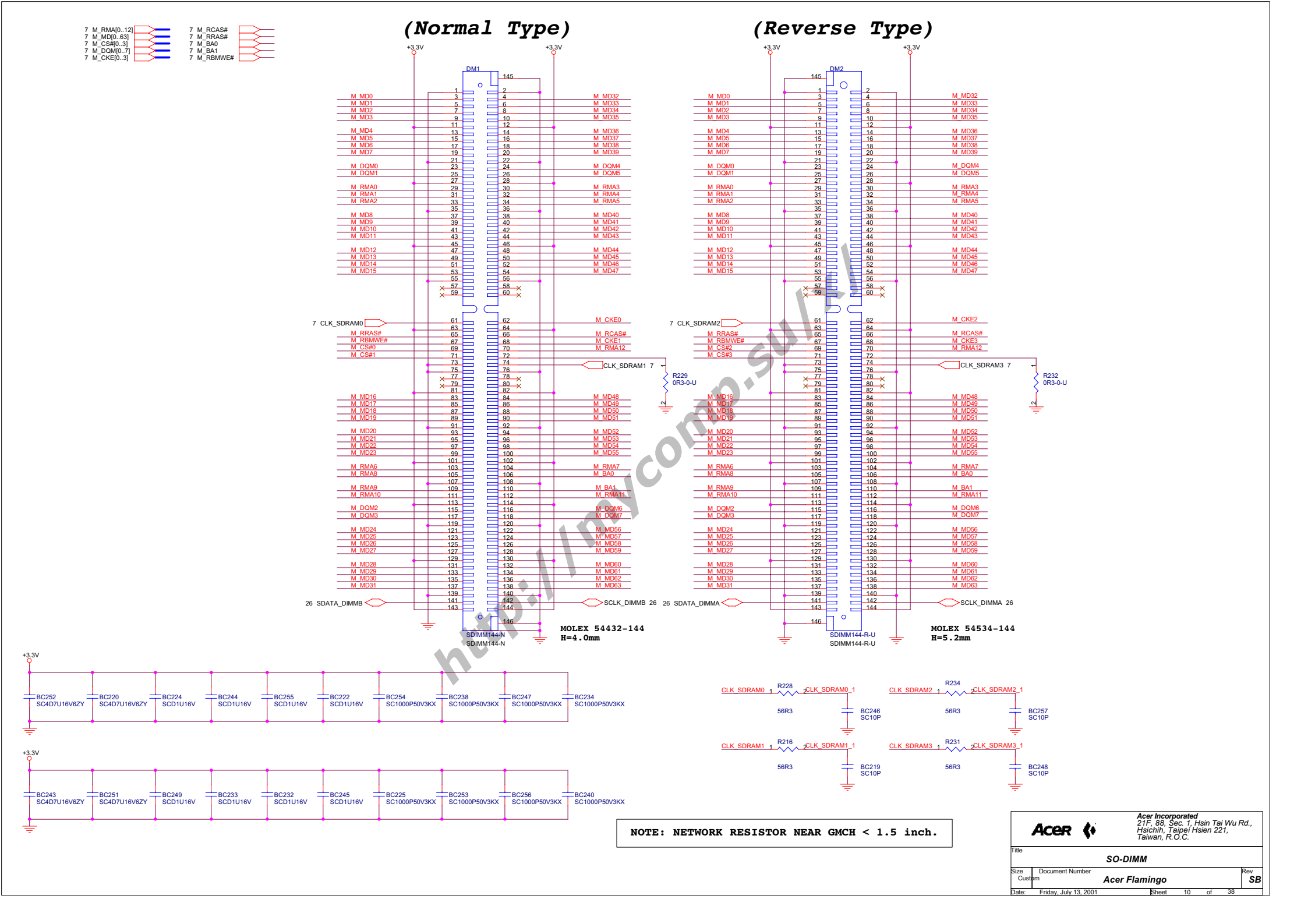

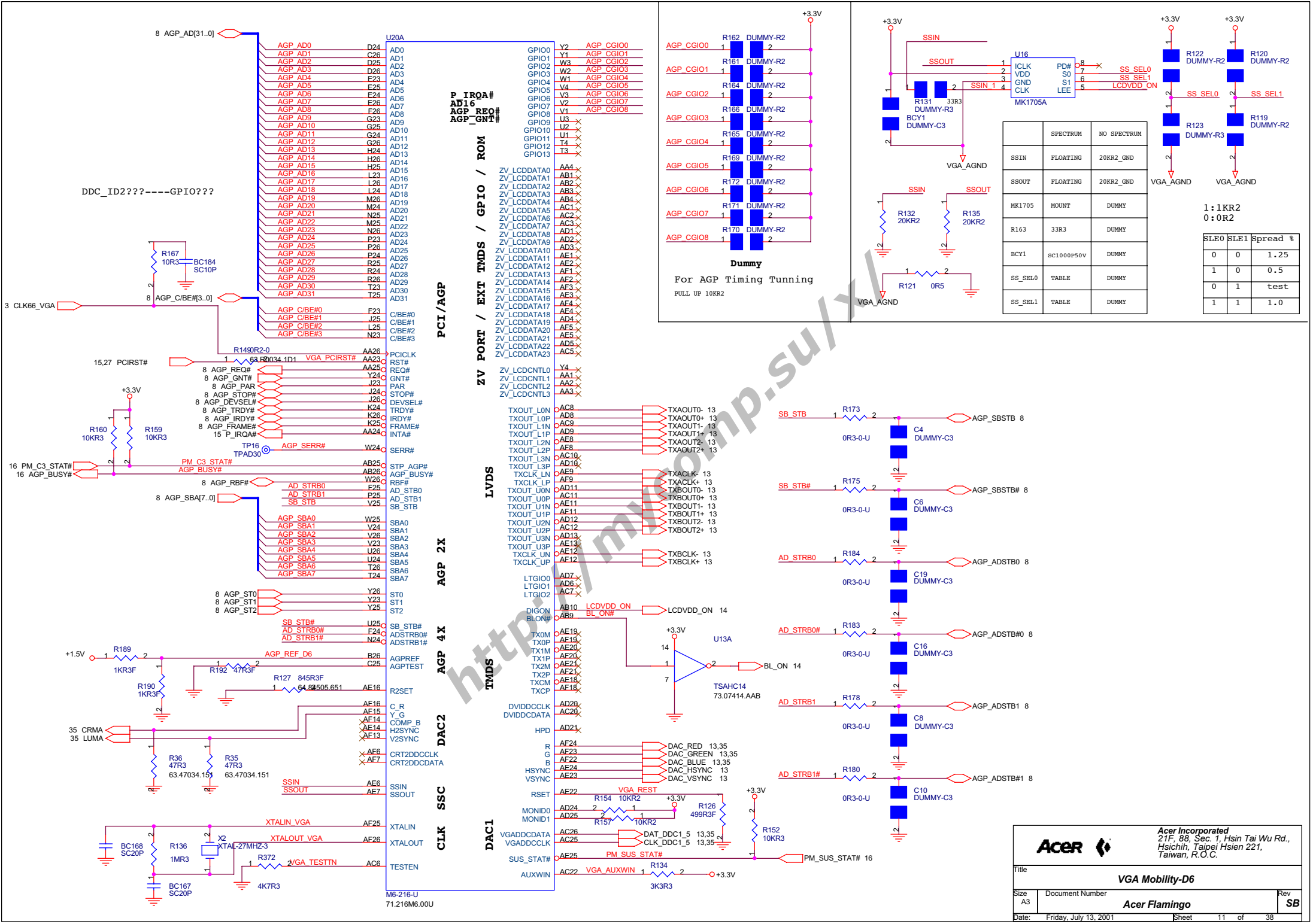

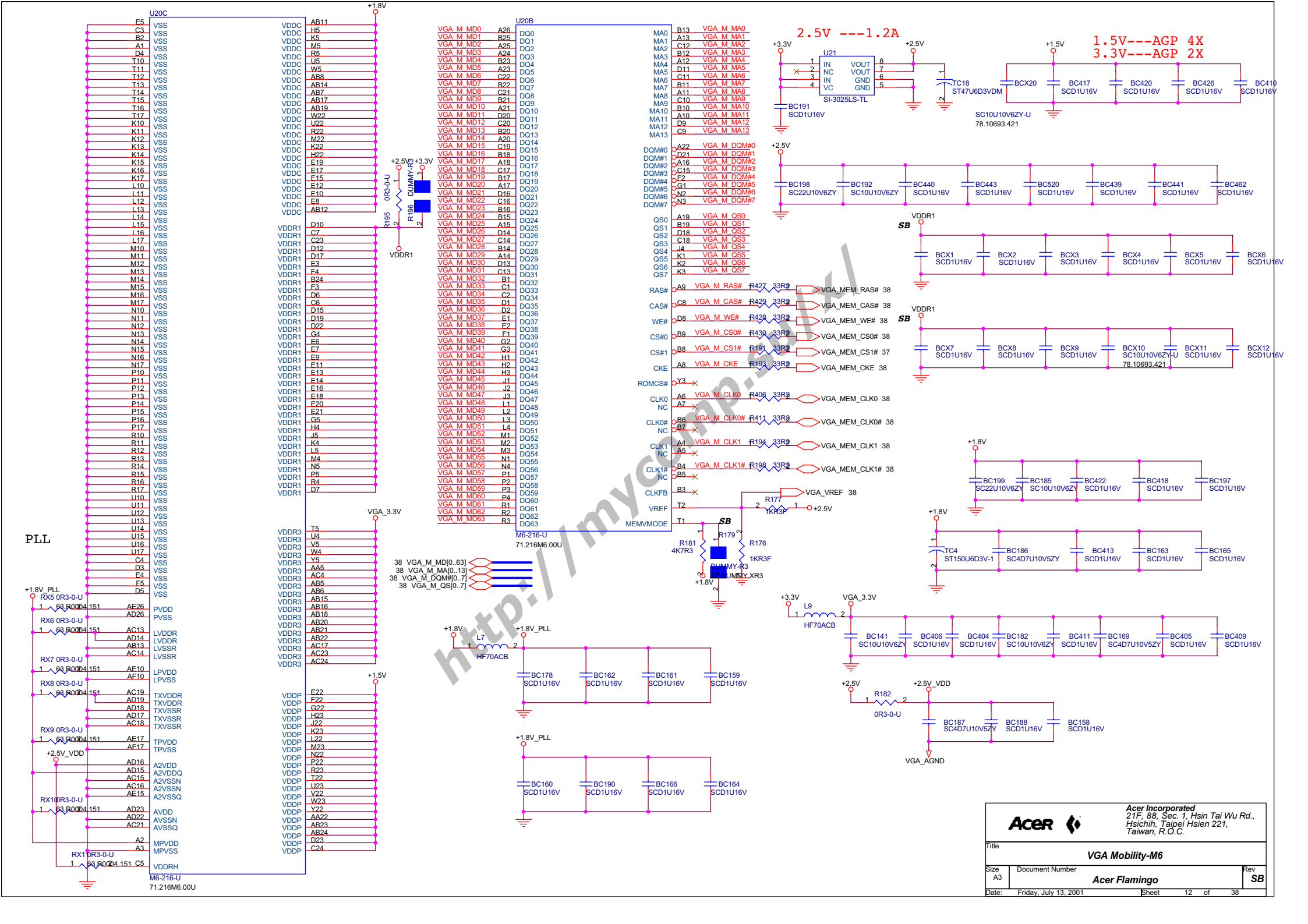
U20C
M6-216-U
71.216M6.00U
U20B
M6-216-U
71.216M6.00U
PLL
2.5V ---1.2A
1.5V---AGP 4X
3.3V---AGP 2X
U21
SI-3025LS-TL
SB
VGA_AGND
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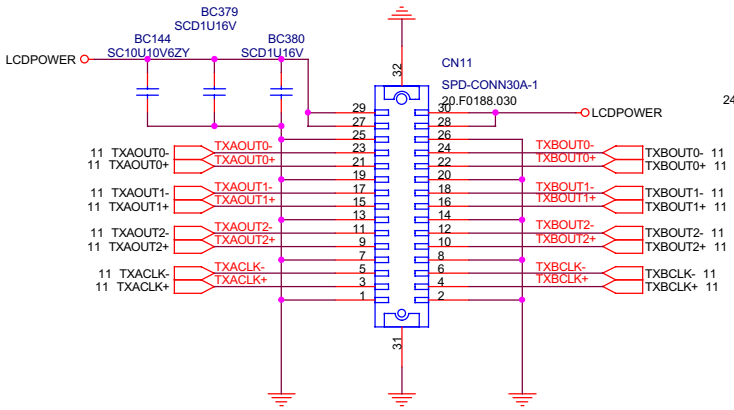
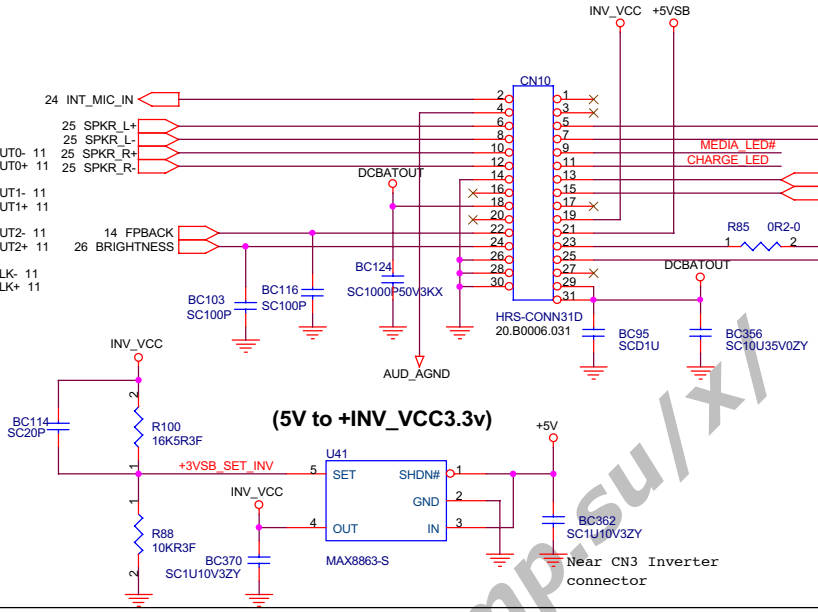
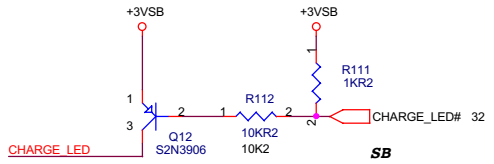
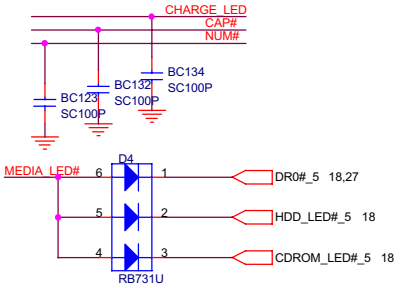
Title
VGA Mobility-M6
Size
A3
Document Number
Acer Flamingo
Rev
SB
Date: Friday, July 13, 2001
Sheet 12 of 38

LCD

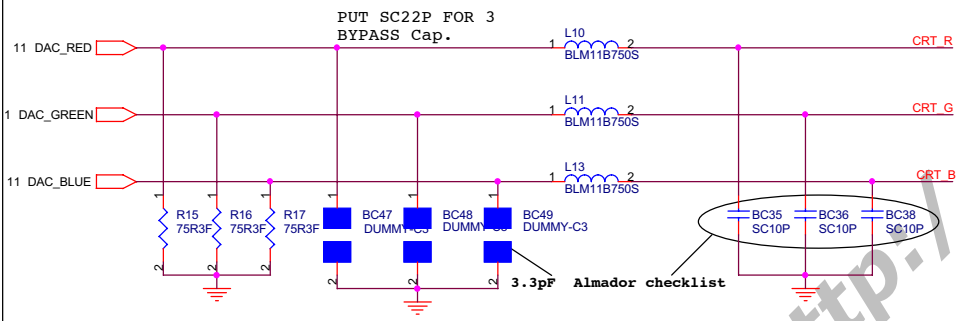


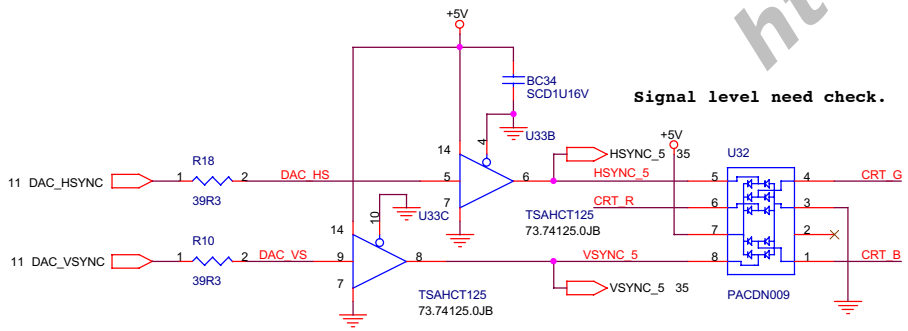


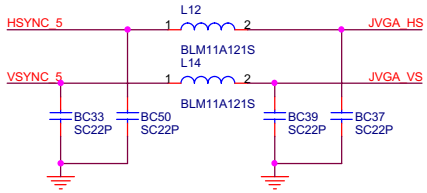


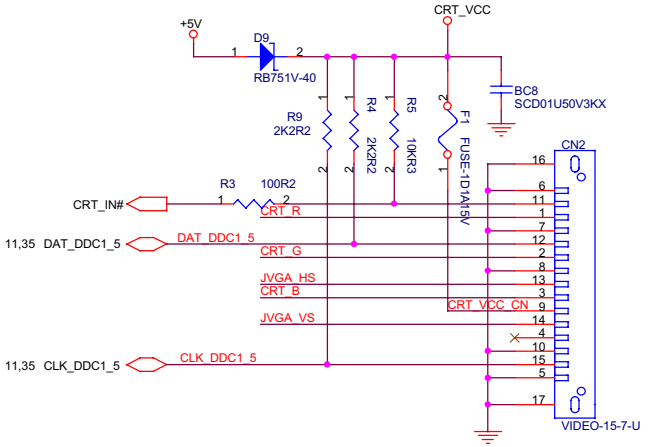


CRT









Layout Note:
Must be a ground return path between this ground and the ground on the VGA connector.

37.4_1% resistors must be placed after RGB pi filter ,near CRT connector.

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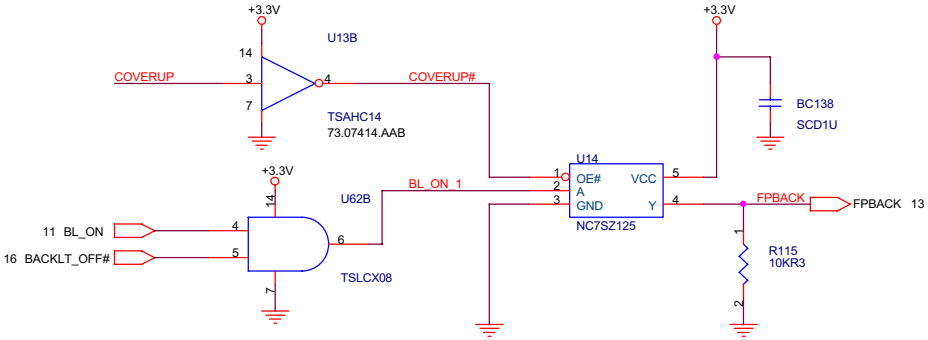
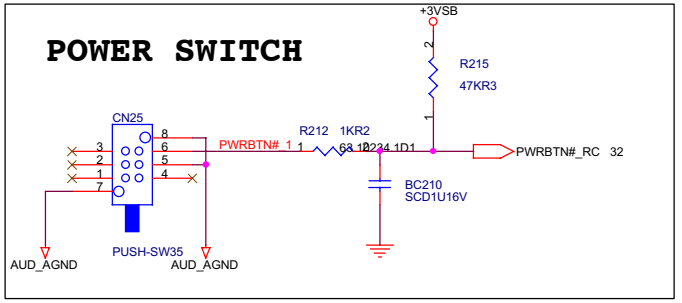
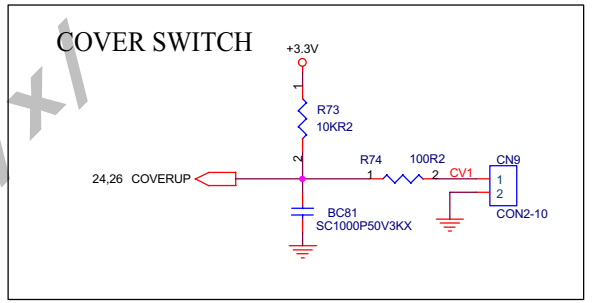
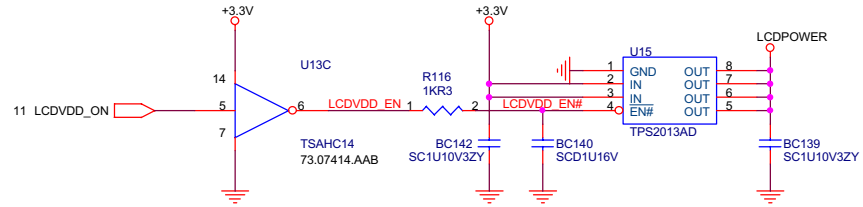
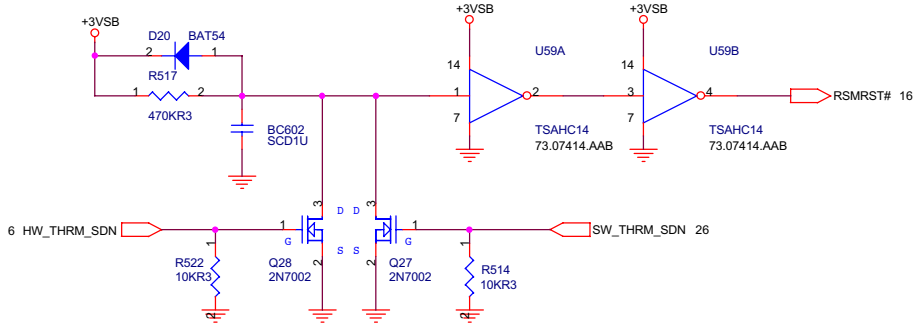
Title	LCD/INV/CRT CONN.	
Size A3	Document Number Acer Flamingo	Rev SB
Date: Friday, July 13, 2001	Sheet 13 of 38	

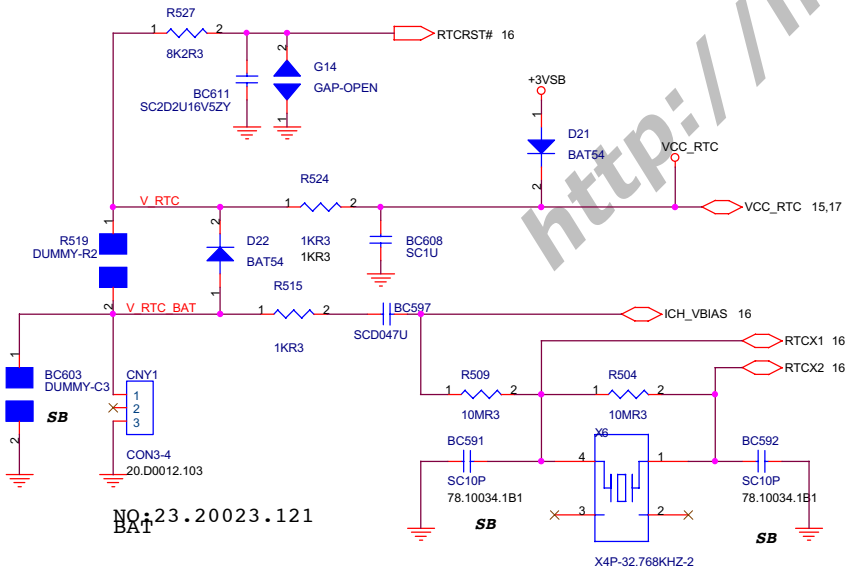












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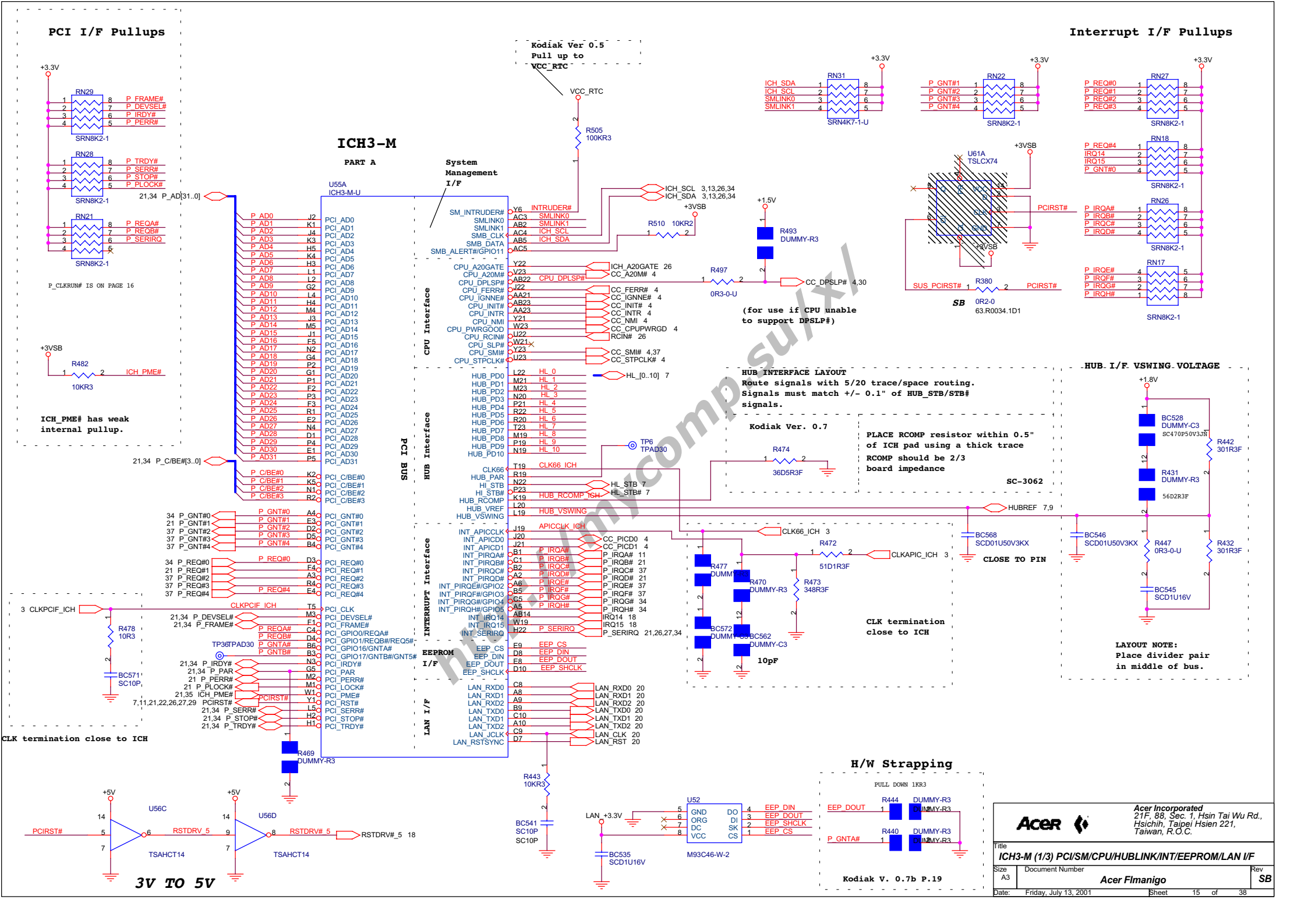
Taiwan, R.O.C.

Title: PWR SW/LCD PWR/RTC

Size: A3 | Document Number: Acer Flmanigo | Rev: SB

Date: Friday, July 13, 2001 | Sheet 14 of 38



BIOS NOTE:
BIOS should disable PM_STPCPU# on CK_Titan.
(Use H_DPSLP# instead)

ICH3-M

U55B
ICH3-M-U
PART B

POWER MANAGEMENT
UNMASKED GPIO
AC'97 LINK
LPC Interface
IDE BUS
USB Interface

PM_AGPBUSY#/GPIO6
LAN_RST#
PM_BATLOW#
PM_C3_STAT#/GPIO21
PM_CLKRUN#/GPIO24
PM_DPRSLPVR
PM_PWRBTN#
PM_PWROK
PM_RI#
PM_RSMRST#
PM_SLP_S1#/GPIO19
PM_SLP_S3#
PM_SLP_S5#
PM_STPCPU#/GPIO20
PM_STPPCI#/GPIO18
PM_SUS_CLK
PM_SUS_STAT#
PM_THRM#
PM_GMUXSEL/GPIO23
PM_CPUPERF#/GPIO22
PM_VGATE/VRMPWRGD
AC_BITCLK
AC_RST#
AC_SDATAIN0
AC_SDATAIN1
AC_SDATAOUT
AC_SYNC
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LPC_DRQ#0
LPC_DRQ#1
LPC_FRAME#
USB_PP0
USB_PP1
USB_PP2
USB_PP3
USB_PP4
USB_PP5
USB_PN#0
USB_PN#1
USB_PN#2
USB_PN#3
USB_PN#4
USB_PN#5
USB_OC#0
USB_OC#1
USB_OC#2
USB_OC#3
USB_OC#4
USB_OC#5
USB_LEDA#0/GPIO32
USB_LEDA#1/GPIO33
USB_LEDA#2/GPIO34
USB_LEDA#3/GPIO35
USB_LEDA#4/GPIO36
USB_LEDA#5/GPIO37
USB_LEDG#0/GPIO38
USB_LEDG#1/GPIO39
USB_LEDG#2/GPIO40
USB_LEDG#3/GPIO41
USB_LEDG#4/GPIO42
USB_LEDG#5/GPIO43
USB_RBIAS

GPIO_7
GPIO_8
GPIO_12
GPIO_13
GPIO_25
GPIO_27
GPIO_28
IDE_PDCS1#
IDE_PDCS3#
IDE_SDCS1#
IDE_SDCS3#
IDE_PDA0
IDE_PDA1
IDE_PDA2
IDE_SDA0
IDE_SDA1
IDE_SDA2
IDE_PDD0
IDE_PDD1
IDE_PDD2
IDE_PDD3
IDE_PDD4
IDE_PDD5
IDE_PDD6
IDE_PDD7
IDE_PDD8
IDE_PDD9
IDE_PDD10
IDE_PDD11
IDE_PDD12
IDE_PDD13
IDE_PDD14
IDE_PDD15
IDE_SDD0
IDE_SDD1
IDE_SDD2
IDE_SDD3
IDE_SDD4
IDE_SDD5
IDE_SDD6
IDE_SDD7
IDE_SDD8
IDE_SDD9
IDE_SDD10
IDE_SDD11
IDE_SDD12
IDE_SDD13
IDE_SDD14
IDE_SDD15
IDE_PDDACK#
IDE_SDDACK#
IDE_PDDREQ
IDE_SDDREQ
IDE_PDIOR#
IDE_SDIOR#
IDE_PDIOW#
IDE_SDIOW#
IDE_PIORDY
IDE_SIORDY
CLK_14
CLK_48
RTCRST#
CLK_RTCX1
CLK_RTCX2
CLK_VBIAS
SPKR

8,11 AGP_BUSY#
PM_C3_STAT#
P_CLKRUN#
PM_DPRSLPVR
PM_PWRBTN#
RUNPWROK
ICH_RI#
RSMRST#
PM_SLP_S1#
PM_SLP_S3#
PM_SLP_S5#
PM_STPCPU#
PM_STPPCI#
PM_SUSCLK
11,26 PM_SUS_STAT#
THRM#_1
30 ICH_GMUXSEL
4 PM_CPUPERF
30 VCORE_PWRGD
19,23 ICH_AC_RST#
23 ICH_AC_DIN0
19 ICH_AC_DIN1
19,23 ICH_AC_DOUT
AC_SYNC
19,23 ICH_AC_SYNC
LPC_LAD0
LPC_LAD1
LPC_LAD2
LPC_LAD3
26,27,29 LPC_LAD[0..3]
27 LPC_LDRQ#0
LPC_LDRQ#1
26,27,29 LPC_LFRAME#
19 USBP0P
19 USBP3P
USBP5P
19 USBP0N
19 USBP3N
USBP5N
USB_OC#0
USB_OC#1
USB_OC#2
USB_OC#3
USB_OC#4
BLTH_USB_OC#
EEPWP#
29 FWH_WP#
FWH_WP#
BLTH_RST#
BLTH_EN#
BLTH_PWCTL
14 BACKLT_OFF#
BACKLT_OFF#
32 CHRG_OFF
CHRG_OFF
6 HWTHRM_EN#
HWTHRM_EN#
3 DK_CLKON#
DK_CLKON#
35 DK_SUS#
DK_SUS#
34,35 DK_PCIRST#
DK_PCIRST#
23 ICH_SPKR
3 CLK48_ICH
3 CLK14_ICH
CLK14_ICH
CLK48_ICH
RTCRST# 14
RTCX1 14
RTCX2 14
ICH_VBIAS 14
PIDE_DACK# 18
SIDE_DACK# 18
PIDE_DREQ 18
SIDE_DREQ 18
PIDE_IOR# 18
SIDE_IOR# 18
PIDE_IOW# 18
SIDE_IOW# 18
PIDE_IORDY 18
SIDE_IORDY 18
PIDE_D[0..15] 18
PIDE_A[0..2] 18
SIDE_D[0..15] 18
SIDE_A[0..2] 18
ECSMI 26
ECSWI 26
ECSCI 26
BAT_RTC_WK# 32
DK_PWRON
DK_PWRON 34
MPCIACT#
PIDE_CS1# 18
PIDE_CS3# 18
SIDE_CS1# 18
SIDE_CS3# 18
PIDE_A0
PIDE_A1
PIDE_A2
SIDE_A0
SIDE_A1
SIDE_A2
PIDE_D0
PIDE_D1
PIDE_D2
PIDE_D3
PIDE_D4
PIDE_D5
PIDE_D6
PIDE_D7
PIDE_D8
PIDE_D9
PIDE_D10
PIDE_D11
PIDE_D12
PIDE_D13
PIDE_D14
PIDE_D15
SIDE_D0
SIDE_D1
SIDE_D2
SIDE_D3
SIDE_D4
SIDE_D5
SIDE_D6
SIDE_D7
SIDE_D8
SIDE_D9
SIDE_D10
SIDE_D11
SIDE_D12
SIDE_D13
SIDE_D14
SIDE_D15

R502 10KR3
R503 10KR3
R498 100KR3
28 COM_RI0#
21 CBUS_RI#
ICH_RI#
32K suspend clock output
R479 0R2-0
6 THRM#
23 ICH_AC_BITCLK
R455 DUMMY-R3
R451 33R3
R453 33R3
R454 33R3
R488 0R3-0-U
63.R0004.151
LAN_RST# 32
R486 DUMMY-R3
BC581 DUMMY-C3
R487 8K2R3
R481 8K2R3
R433 18K2R3F
R446 10R3
R445 10R3
BC529 SC10P
BC530 SC10P
CLK termination close to ICH

AC97 AC terminations

ICH_AC_BITCLK
ICH_AC_DIN0
ICH_AC_DIN1
R457 DUMMY-R3
R450 DUMMY-R3
R439 DUMMY-R3
BC540 DUMMY-C3
BC539 DUMMY-C3
BC536 DUMMY-C3

FPET7 Elec. P3-54

PIDE_IORDY 2
R511 4K7R3
SIDE_IORDY 2
R512 4K7R3

LPC I/F PULLL-UPs

RN30
LPC_LAD2
LPC_LAD1
LPC_LAD3
LPC_LAD0
DUMMY-SRN10K-2
22.10330.00A
No Stuff

KAHUNA SPEC. LPC47N252ENG.PDF
P22 NOTE.24

R476 DUMMY-R3 LPC_LDRQ#0
R480 DUMMY-R3 LPC_LDRQ#1
10KR3

LPC_LDRQ#0, 1 have weak internal pullups

RN20
THRM# 1
USB_OC#0
USB_OC#3
EEPWP#
SRN10K-2
RN24
USB_OC#4
USB_OC#1
USB_OC#2
BLTH_USB_OC#
SRN10K-2
RN19
USBP5P
USBP5N
SRN10K-2
RN23
BLTH_RST#
BLTH_EN#
BLTH_PWCTL
SRN10K-2

Almador checklist ver. 0.5

U57
OE#
A
GND
VCC
Y
NC7SZ125
PM_SUSCLK
32KHZ
R499 10R3
R506 10R3
R496 10R3
R494 10R3
G768_32K 6
OZ998_32K 26
OZ711_32K 21
OZSW_32K 22

R500 10KR2 BC589 DUMMY-C3
PM_SLP_S5#

U59C
TSAHC14
PM_SLP_S5# 32

ICH3 Integrated Pull-up and Pull-down Resistors

EE_DIN , EE_DOUT , LDRQ[1:0] , PME# GNT[B:A]#/GNT[5]#/GPIO[17:16] , LAD[3:0]#/FWH[3:0]# , PWRBTN#	ICH3 internal 24K pull-ups
LAN_RXD[2:0]	ICH3 internal 9K pull-ups
AC_BITCLK, AC_SDIN[0], AC_SDOUT, AC_SDIN[1]/GPIO[9], AC_SYNC,	ICH3 internal 20K pull-downs
SPKR	ICH3 internal 24K pull-downs
PDD[7]/SDD[7], PDDREQ / SDDREQ	ICH3 internal 5.9K pull-downs
DPRSLPVR	ICH3 internal TBD K pull-downs

FM-1882 P4-1,2

SB
Kodiak ver. 0.7b

+3.3V
R490 10KR3
P_CLKRUN#

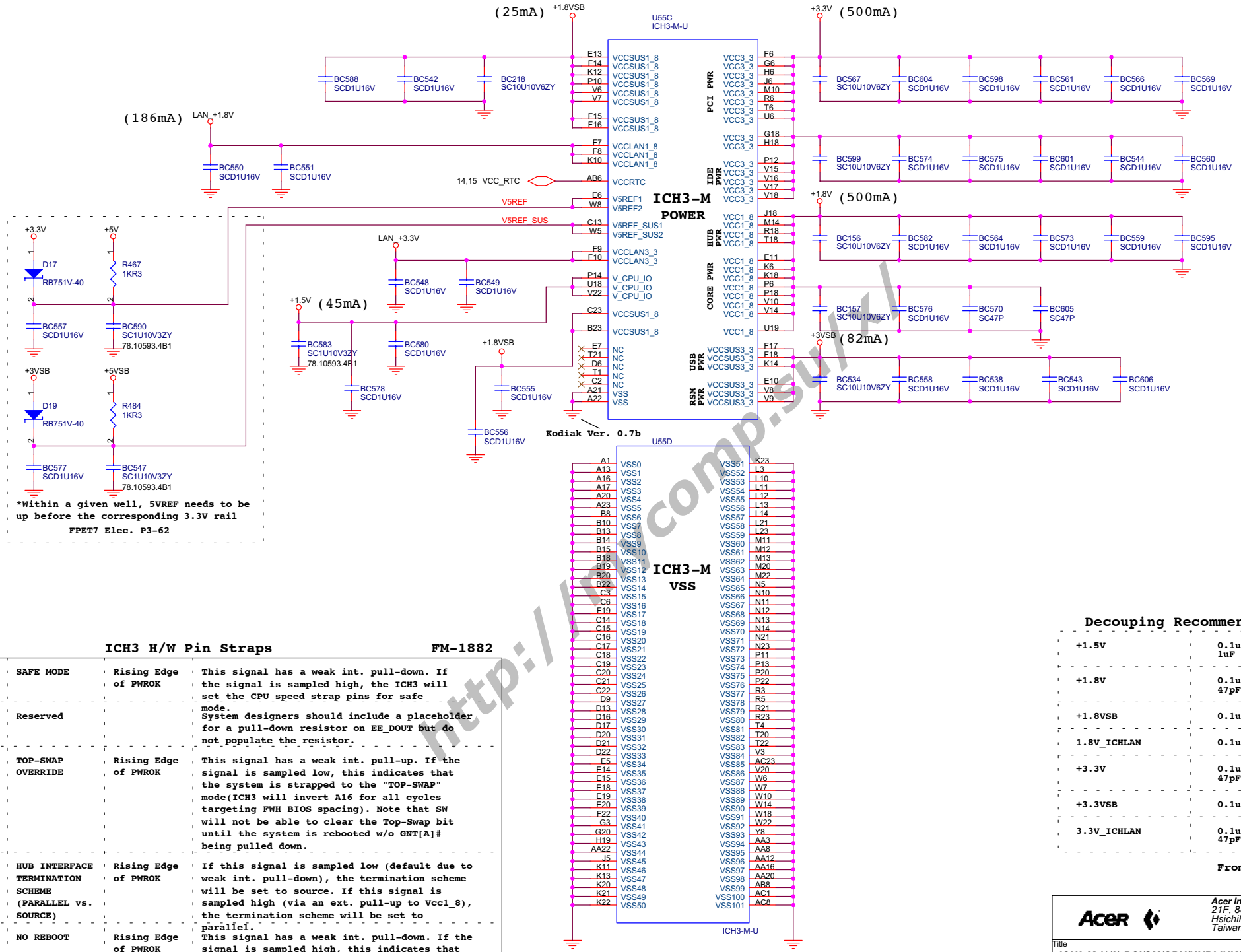
H/W Strapping

1KR3
ICH_SPKR
R465 DUMMY-R3
ICH_AC_DOUT
R452 DUMMY-R3

Kodiak V. 0.7b P.19

Acer Incorporated
21F, 88, Sec. 1, Hsin Tai Wu Rd.,
Hsichih, Taipei Hsien 221,
Taiwan, R.O.C.

Title: ICH3-M (2/3) PM,USB,AC'97,LPC,IDE,RTC
Size: A3
Document Number: Acer Flmanigo
Rev: SB
Date: Friday, July 13, 2001
Sheet 16 of 38



ICH3 H/W Pin Straps FM-1882

AC_SDOUT	SAFE MODE	Rising Edge of PWROK	This signal has a weak int. pull-down. If the signal is sampled high, the ICH3 will set the CPU speed strap pins for safe mode.
EE_DOUT	Reserved		System designers should include a placeholder for a pull-down resistor on EE_DOUT but do not populate the resistor.
GNT[A]#	TOP-SWAP OVERRIDE	Rising Edge of PWROK	This signal has a weak int. pull-up. If the signal is sampled low, this indicates that the system is strapped to the "TOP-SWAP" mode(ICH3 will invert A16 for all cycles targeting FWH BIOS spacing). Note that SW will not be able to clear the Top-Swap bit until the system is rebooted w/o GNT[A]# being pulled down.
DPRSLPVR	HUB INTERFACE TERMINATION SCHEME (PARALLEL vs. SOURCE)	Rising Edge of PWROK	If this signal is sampled low (default due to weak int. pull-down), the termination scheme will be set to source. If this signal is sampled high (via an ext. pull-up to Vcc1_8), the termination scheme will be set to parallel.
SPKR	NO REBOOT	Rising Edge of PWROK	This signal has a weak int. pull-down. If the signal is sampled high, this indicates that the system is strapped to the " No Reboot " mode (ICH3 will disable the TXO Timer system reboot feature).

Decouping Recommendation

+1.5V	0.1uF * 2 1uF / 16V * 1
+1.8V	0.1uF * 5 47pF * 2
+1.8VSB	0.1uF * 3
1.8V_ICHLAN	0.1uF * 2
+3.3V	0.1uF * 13 47pF * 5
+3.3VSB	0.1uF * 8
3.3V_ICHLAN	0.1uF * 2 47pF * 1

From Kris 8/10

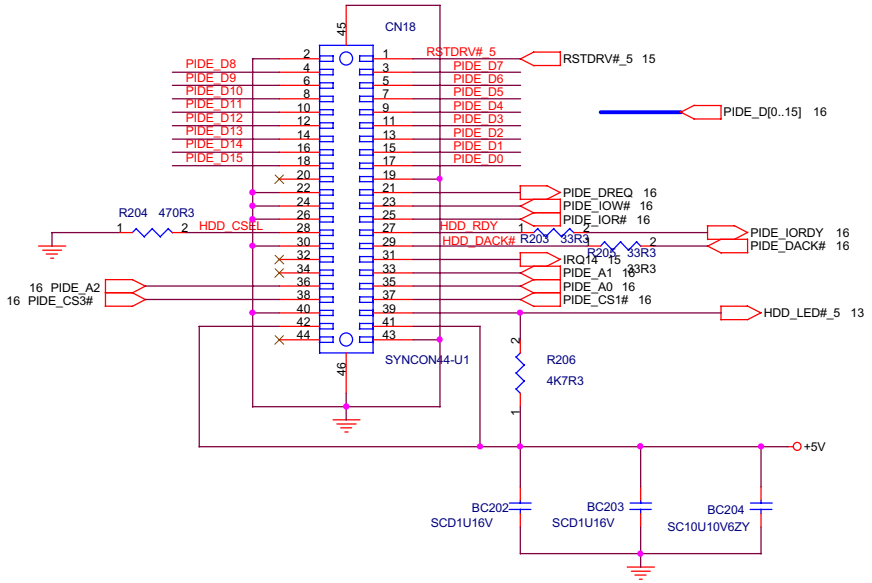
Acer Incorporated
21F, 88, Sec. 1, Hsin Tai Wu Rd.,
Hsichih, Taipei Hsien 221,
Taiwan, R.O.C.

Title: ICH3-M (1/3) PCI/SM/CPU/HUBLINK/INT/EEPROM/LAN I/F

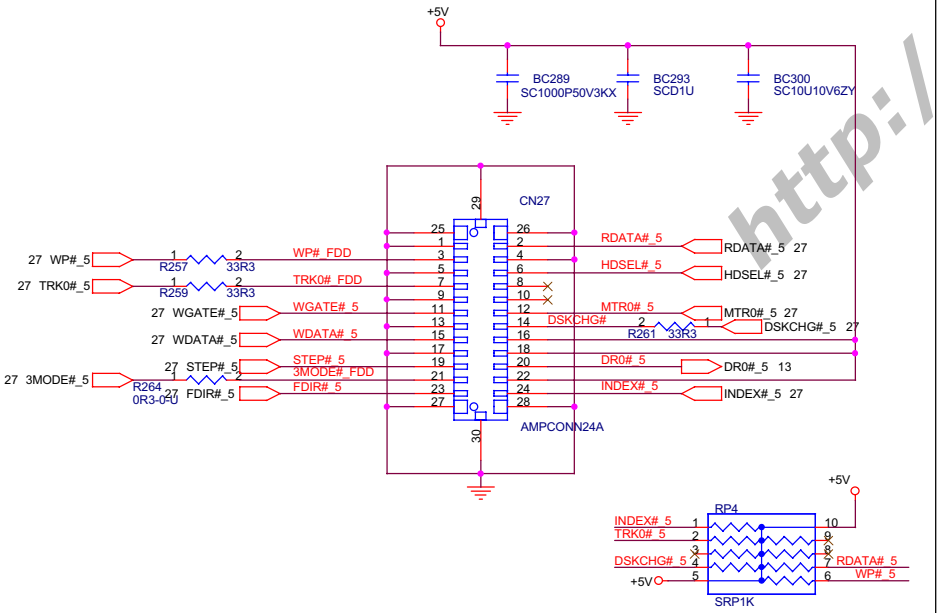
Size: A3 | Document Number: Acer Flmanigo | Rev: SB

Date: Friday, July 13, 2001 | Sheet 17 of 38

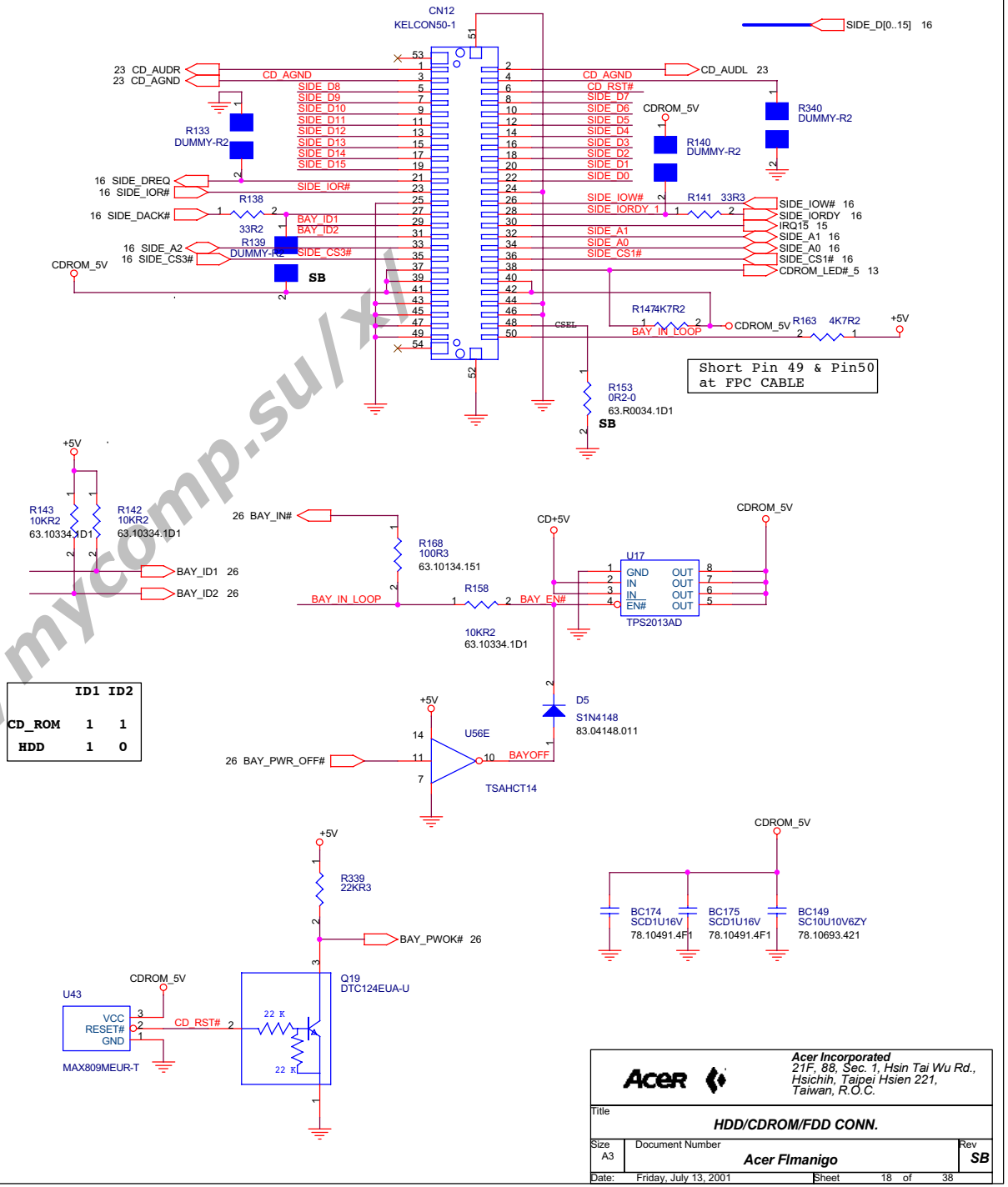
HDD



FDD



CDROM



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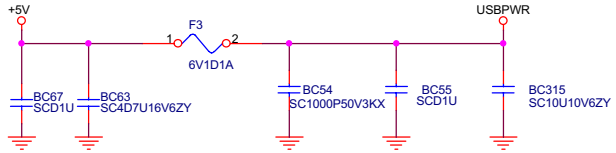
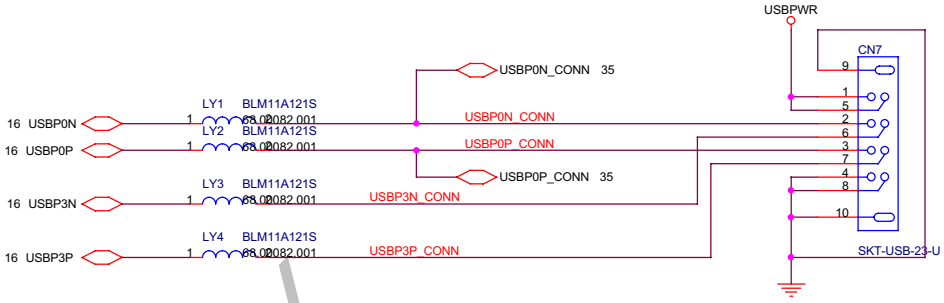
Taiwan, R.O.C.

Title	HDD/CDROM/FDD CONN.	
Size A3	Document Number Acer FImanigo	Rev SB
Date: Friday, July 13, 2001	Sheet 18 of 38	



USB Common mode choke
MURATA
PLW3216S900SQ2

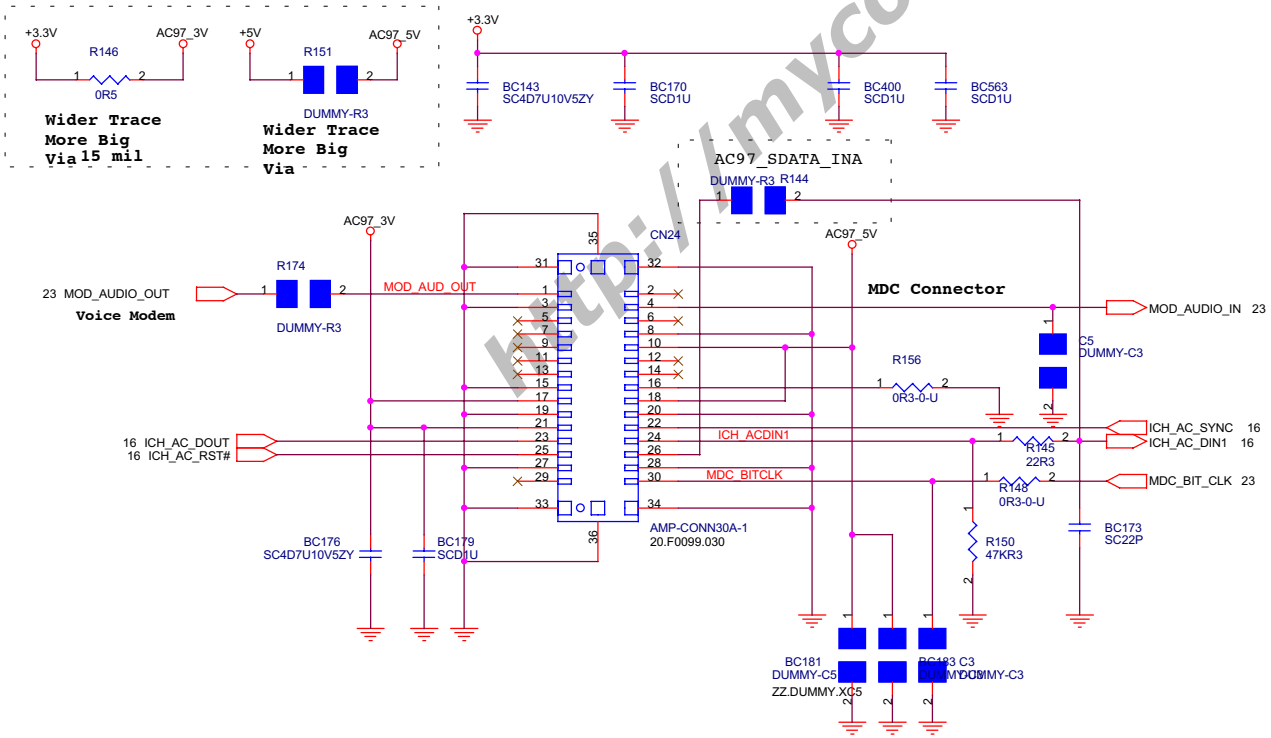
Filtering RC network located near ICH3-M
FPET7 Elec. P3-14



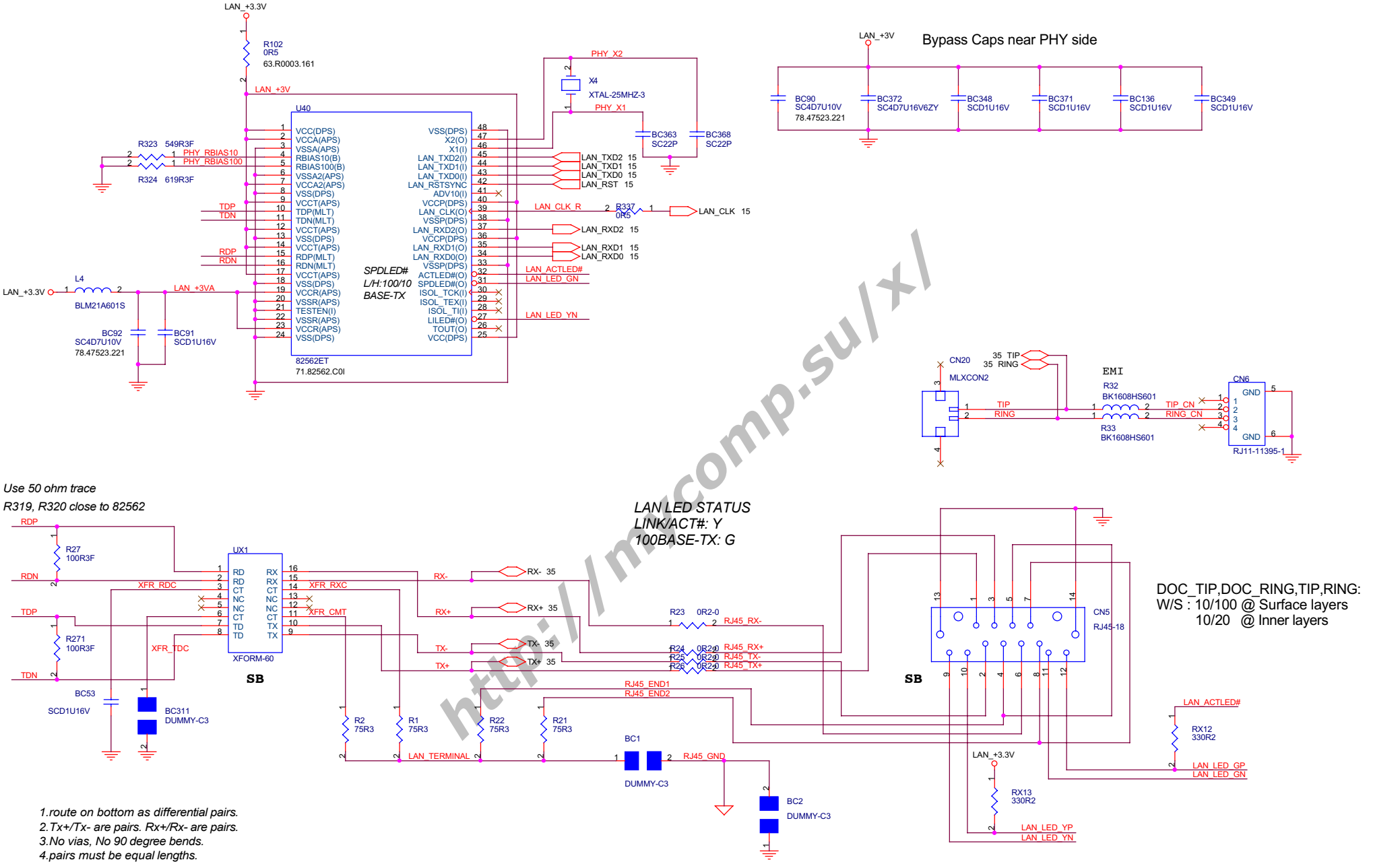
Filtering RC network located near ICH3-M
FPET7 Elec. P3-14

USB Common mode choke
MURATA
PLW3216S900SQ2

MDC



Acer Incorporated 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	USB / MDC CONN.	
Size A3	Document Number Acer Flmanigo	Rev SB
Date: Friday, July 13, 2001	Sheet 19 of 38	



1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

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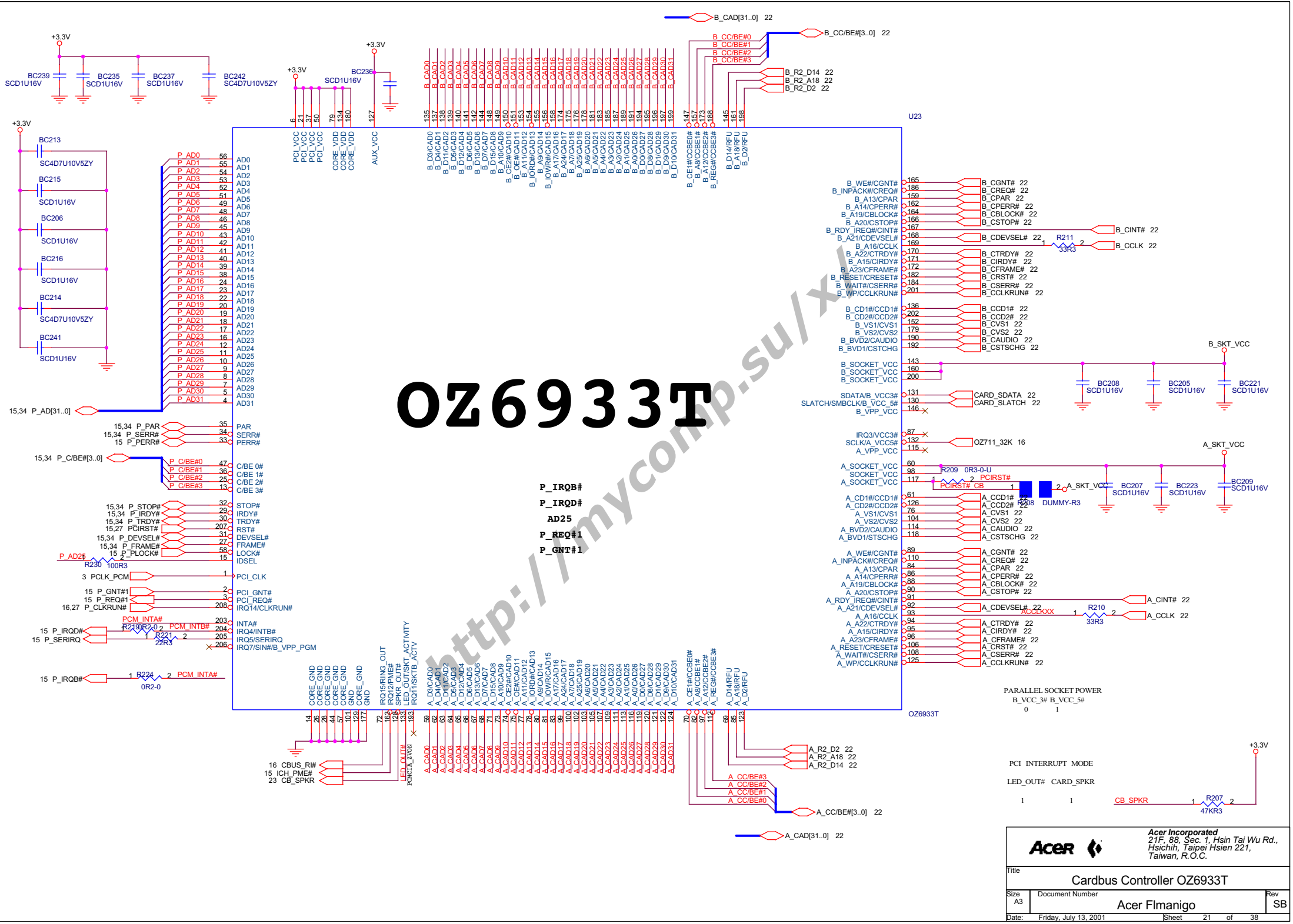
Taiwan, R.O.C.

Title: LAN

Size: A3 | Document Number: Acer Flmanigo | Rev: SB

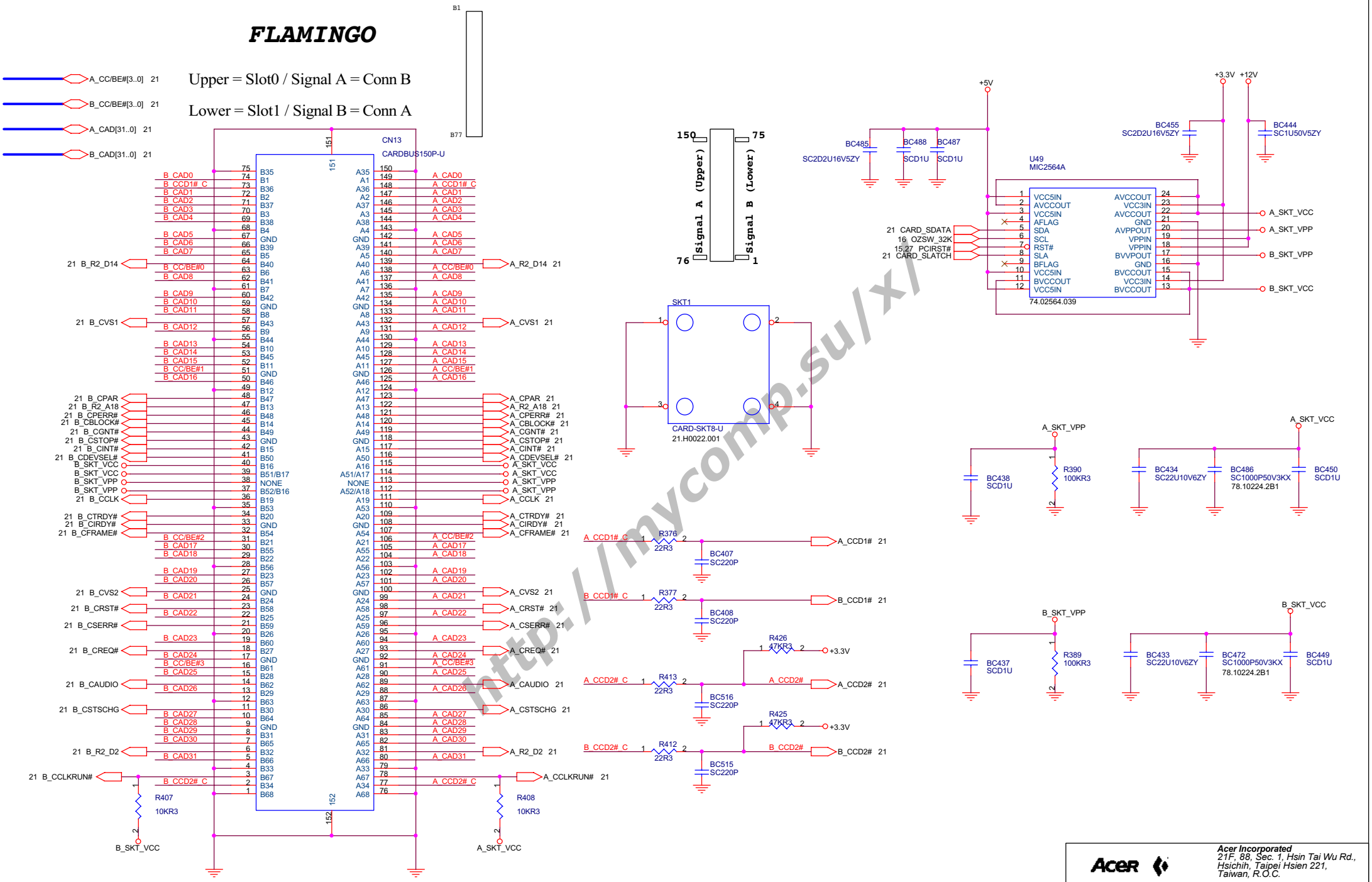
Date: Friday, July 13, 2001 | Sheet 20 of 38


OZ6933T
http://mycomp.su/x/
U23
OZ6933T
P_IRQB#
P_IRQD#
AD25
P_REQ#1
P_GNT#1
B_CAD[31..0] 22
B_CC/BE#[3..0] 22
A_CAD[31..0] 22
A_CC/BE#[3..0] 22
15,34 P_AD[31..0]
15,34 P_C/BE#[3..0]
PARALLEL SOCKET POWER
B_VCC_3# B_VCC_5#
0 1
PCI INTERRUPT MODE
LED_OUT# CARD_SPKR
1 1
CB_SPKR
Acer Incorporated
21F, 88, Sec. 1, Hsin Tai Wu Rd.,
Hsichih, Taipei Hsien 221,
Taiwan, R.O.C.
Title
Cardbus Controller OZ6933T
Size A3
Document Number
Acer FImanigo
Rev SB
Date: Friday, July 13, 2001
Sheet 21 of 38

FLAMINGO

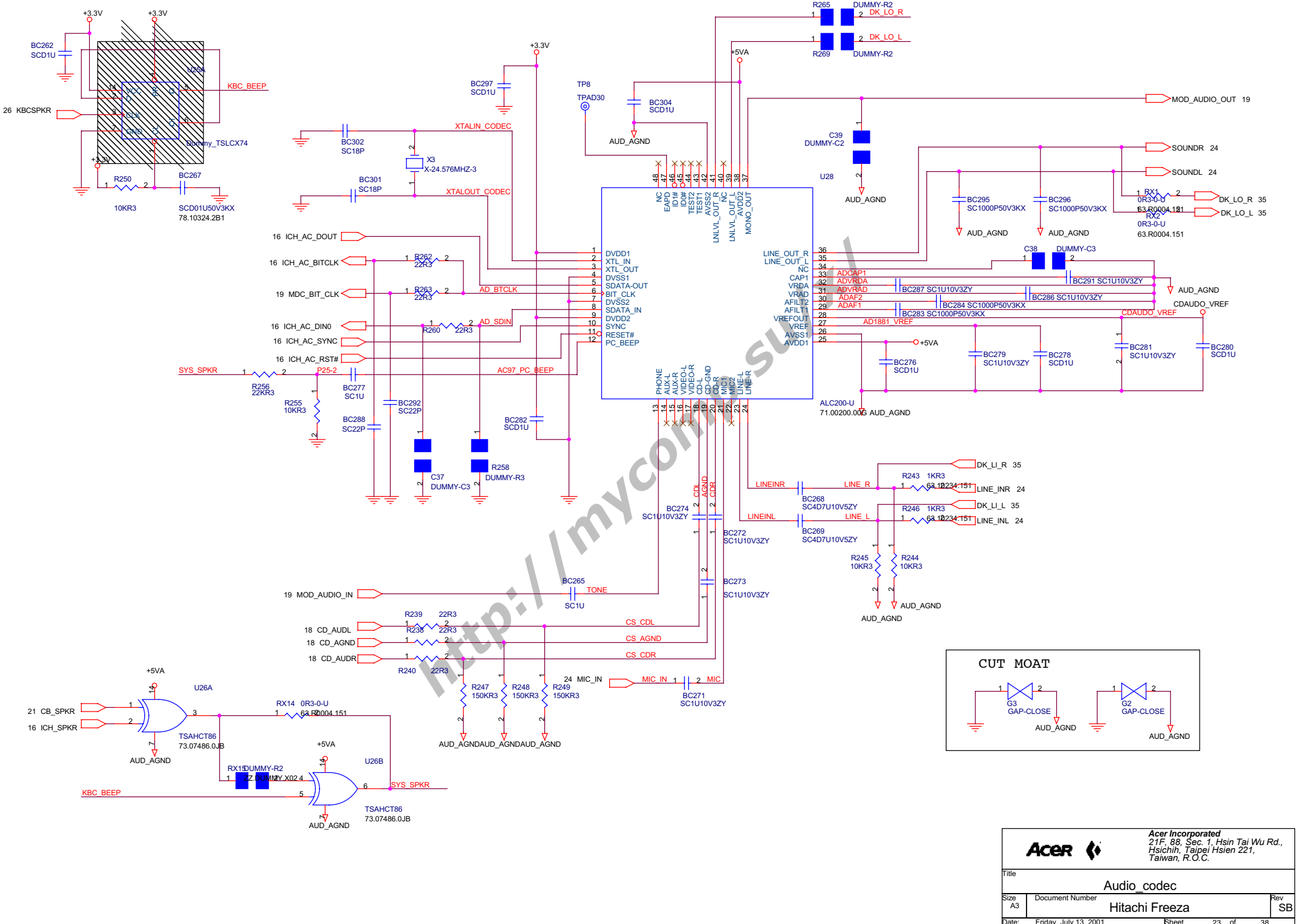
Upper = Slot0 / Signal A = Conn B

Lower = Slot1 / Signal B = Conn A

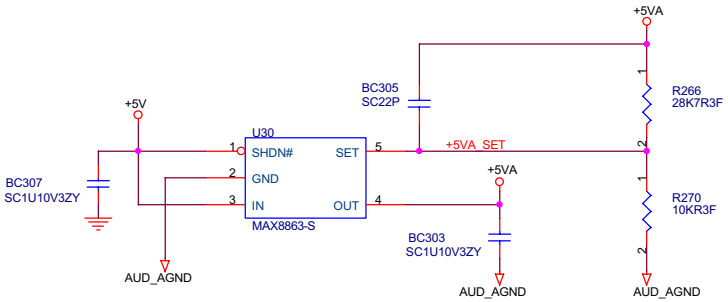


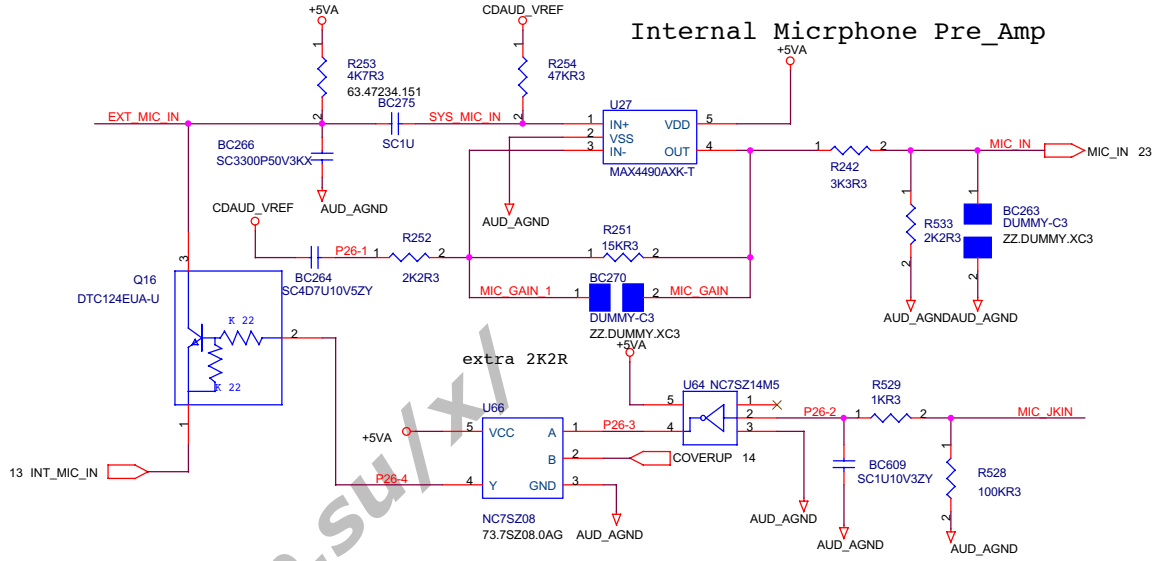
Acer Incorporated
21F, 88, Sec. 1, Hsin Tai Wu Rd.,
Hsichih, Taipei Hsien 221,
Taiwan, R.O.C.

Title	Cardbus Connector/Power SW	
Size A3	Document Number: Acer Flmanigo	Rev SB
Date: Friday, July 13, 2001	Sheet 22 of 38	



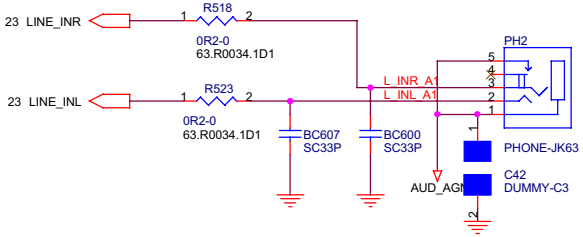
Acer Incorporated	21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	Audio_codec
Size	A3
Document Number	Hitachi Freeza
Rev	SB
Date:	Friday, July 13, 2001
Sheet	23 of 38



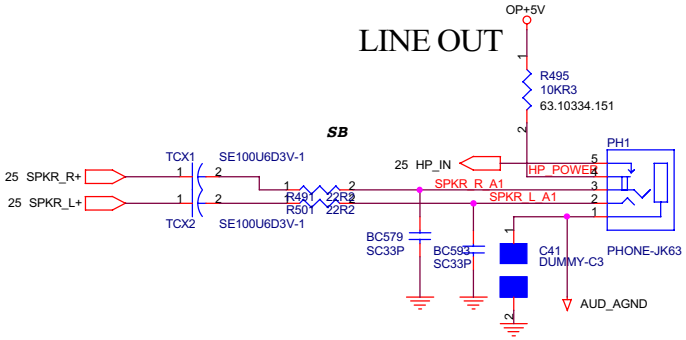


Reserve for Special Request When LCD Off, Int Mic turn off

LINE IN

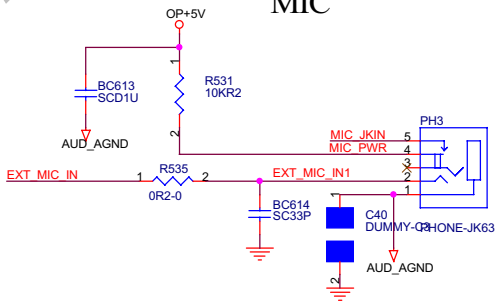


LINE OUT

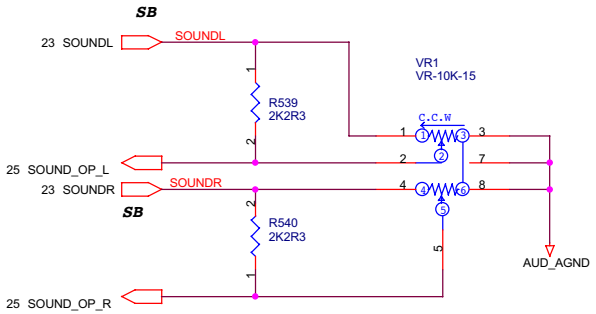


All 33pF capacitors are used for EMI concern

MIC

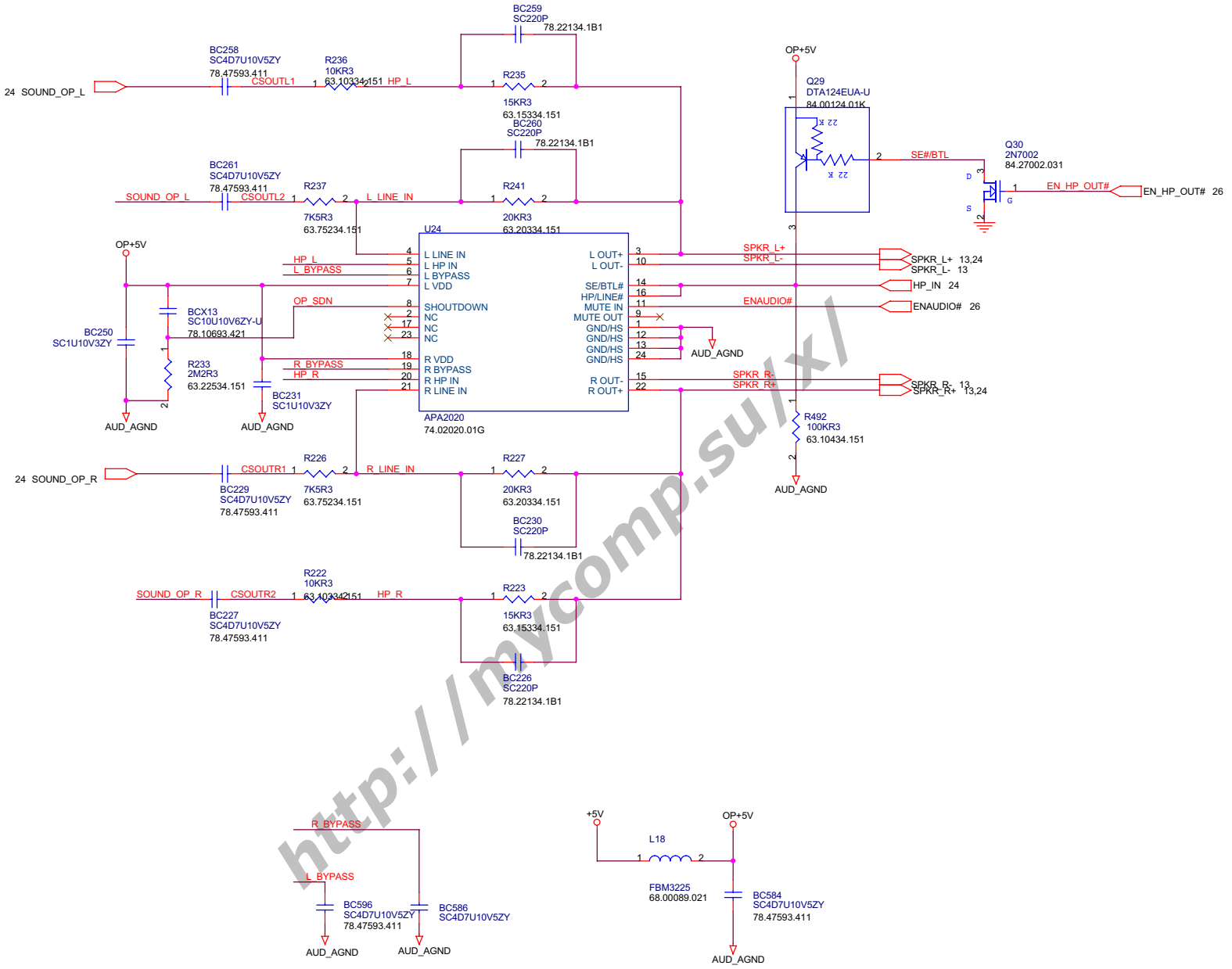


VR



Acer Incorporated
21F, 88, Sec. 1, Hsin Tai Wu Rd.,
Hsichih, Taipei Hsien 221,
Taiwan, R.O.C.

Title	CD AUDIO SWITCH	
Size A3	Document Number Acer Flamingo	Rev SB
Date: Friday, July 13, 2001	Sheet 24 of 38	



Acer Incorporated
21F, 88, Sec. 1, Hsin Tai Wu Rd.,
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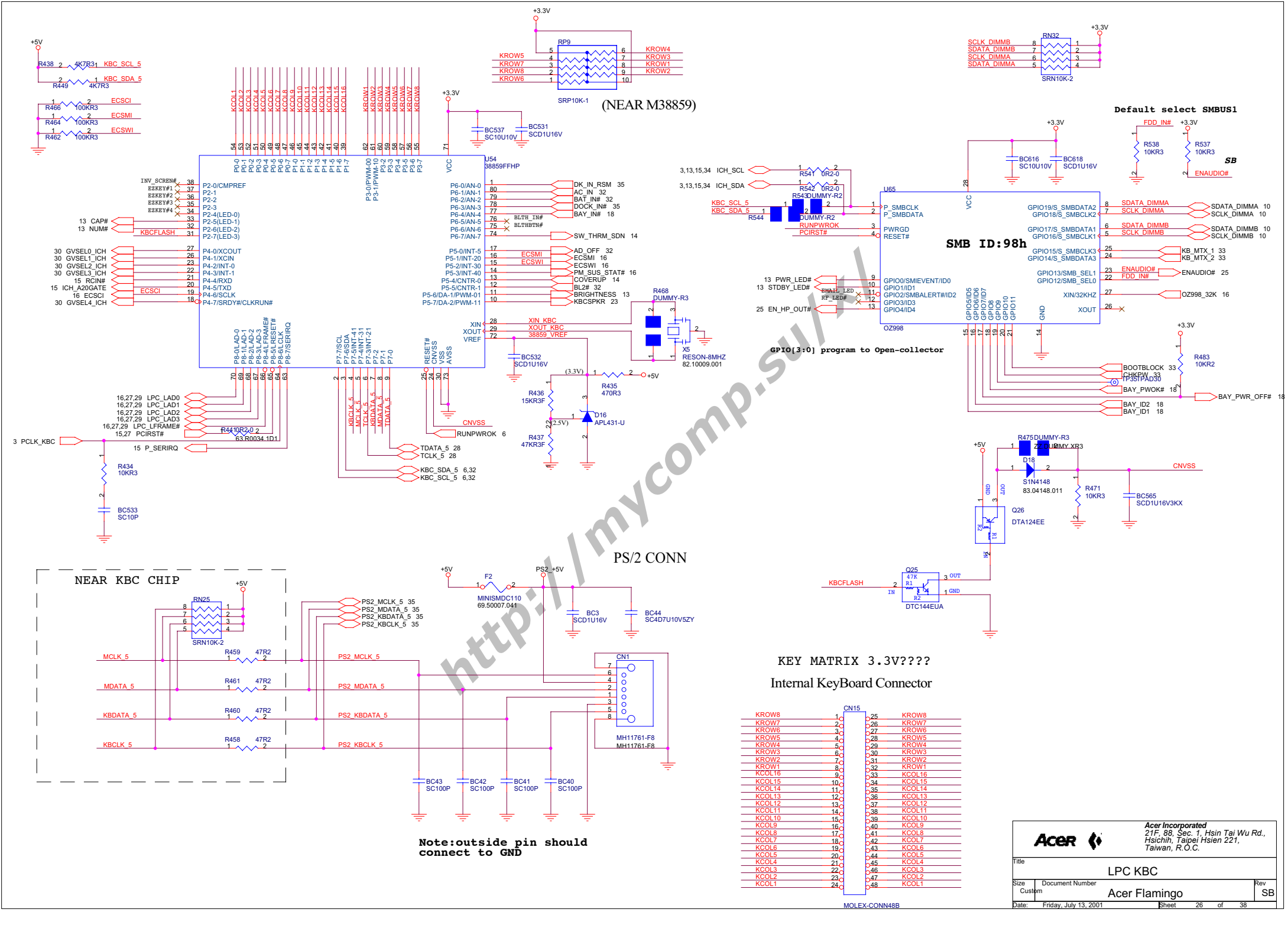
Taiwan, R.O.C.

Title: LINE_IN, LINE_OUT, MIC

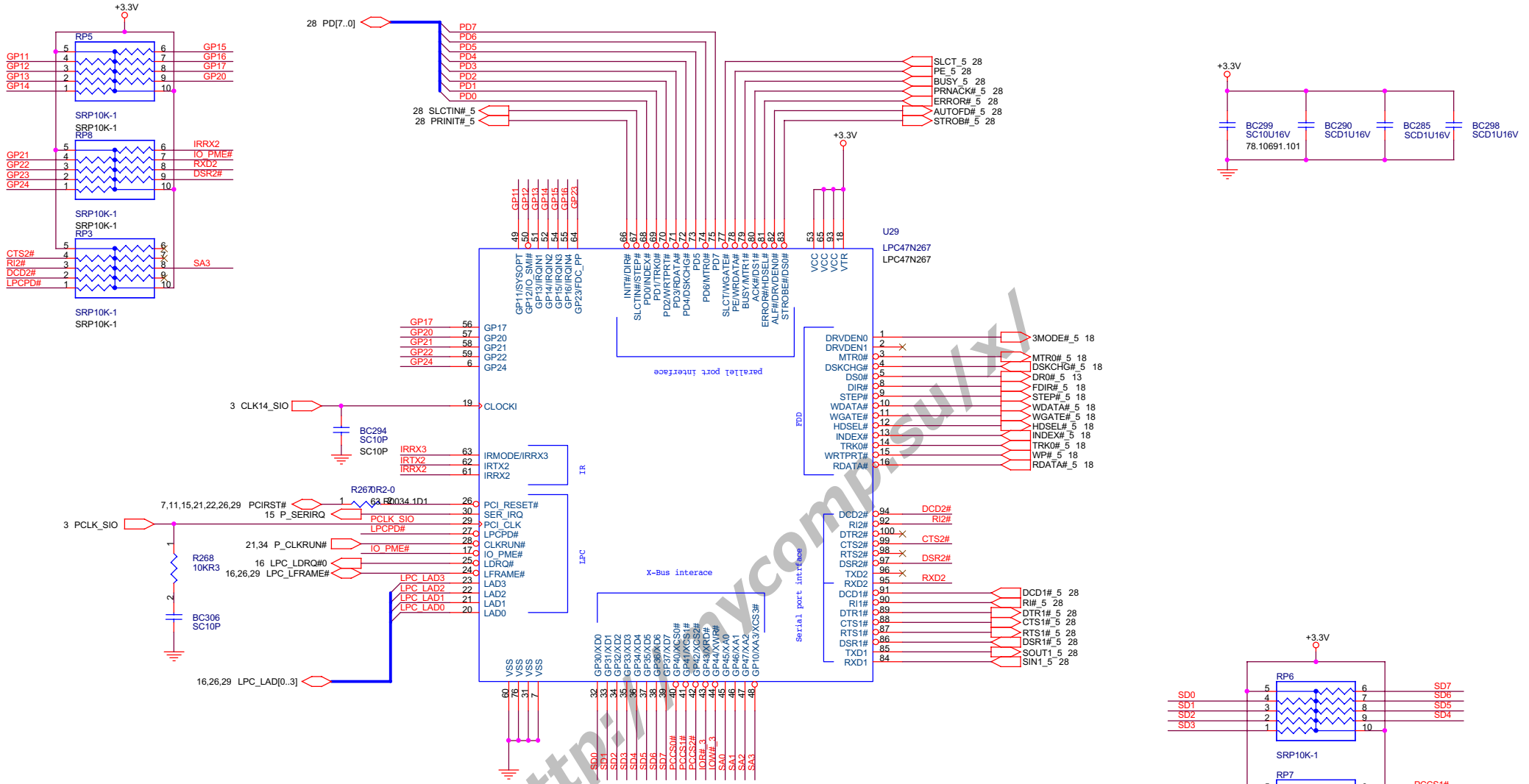
Size: A3 | Document Number: Acer Flamingo | Rev: SB

Date: Friday, July 13, 2001 | Sheet 25 of 38

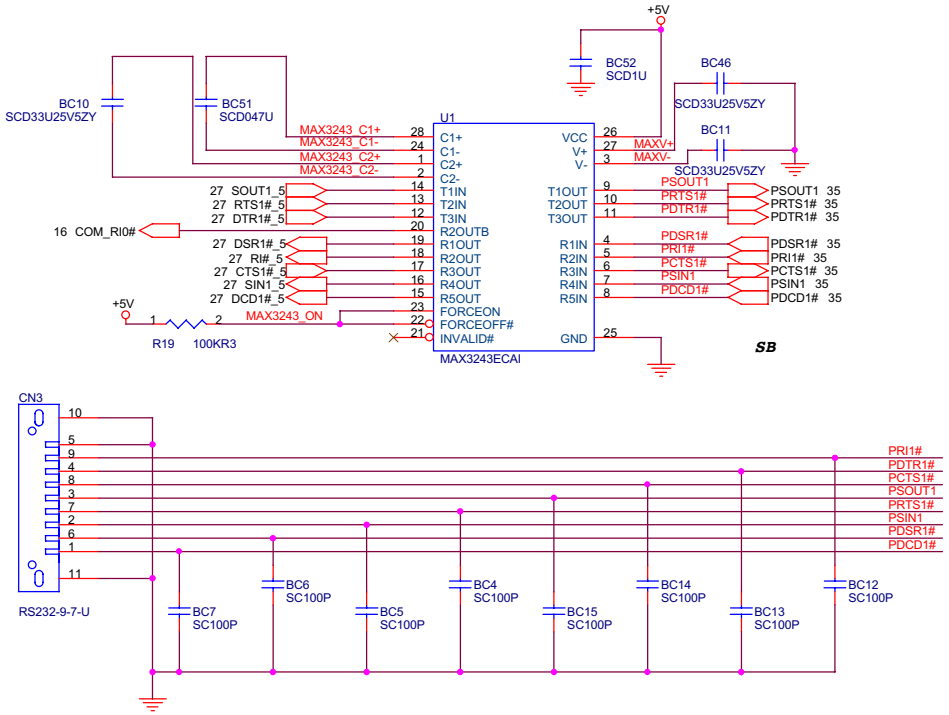


Acer Incorporated
21F, 88, Sec. 1, Hsin Tai Wu Rd.,
Hsichih, Taipei Hsien 221,
Taiwan, R.O.C.

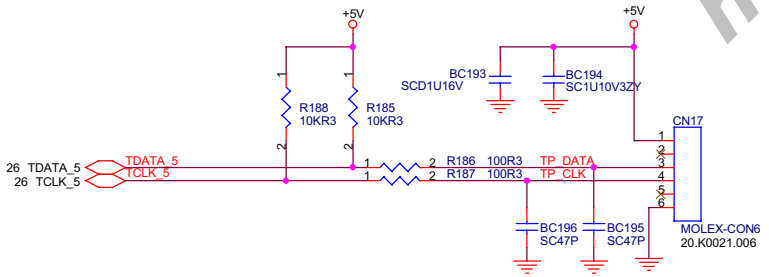
Title	LPC KBC	
Size: Custom	Document Number: Acer Flamingo	Rev: SB
Date: Friday, July 13, 2001	Sheet 26 of 38	



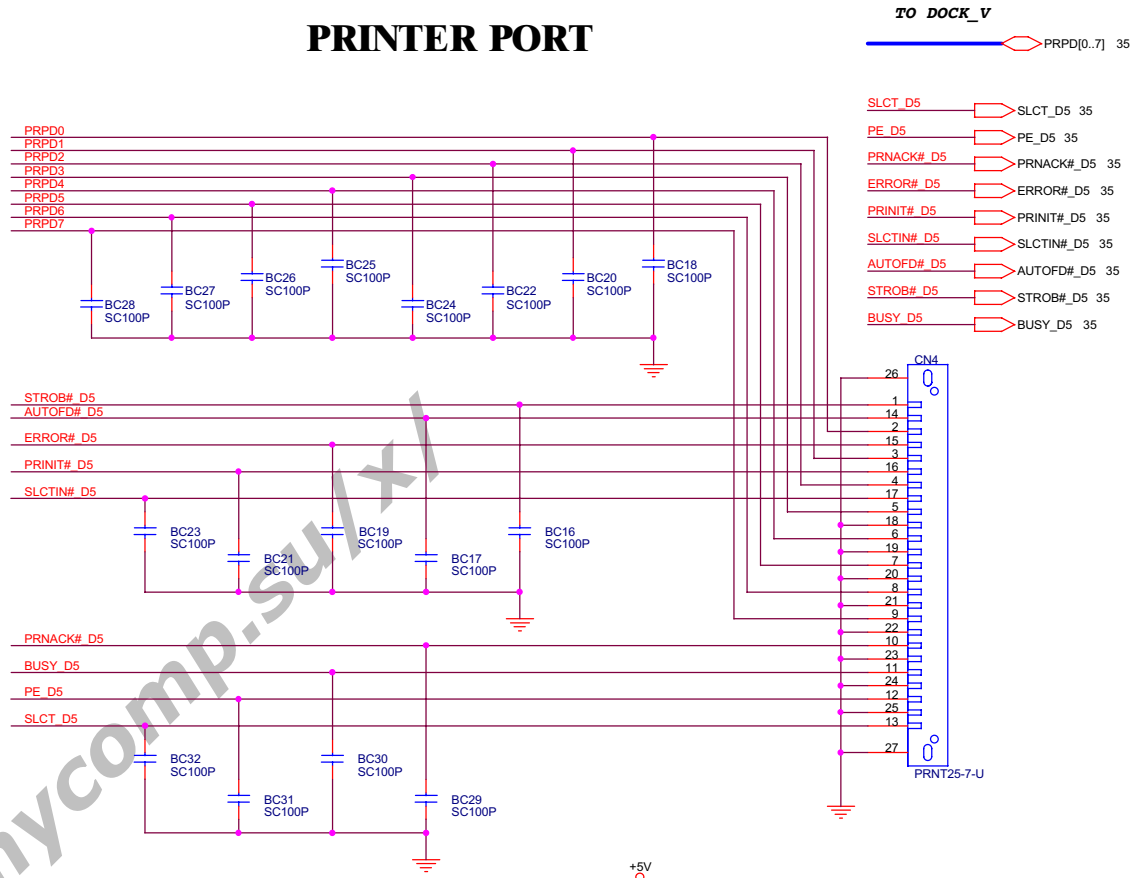
SERIAL PORT

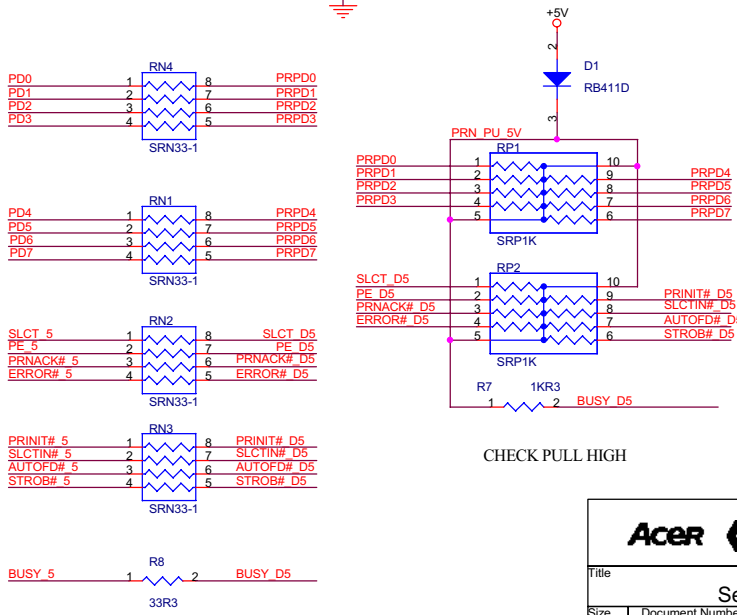


TOUCH PAD



PRINTER PORT

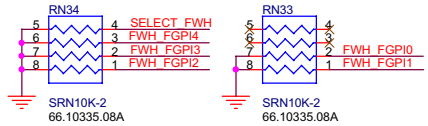




Acer Incorporated
21F, 88, Sec. 1, Hsin Tai Wu Rd.,
Hsichih, Taipei Hsien 221,
Taiwan, R.O.C.

Title	Serial, Parallel Port	
Size A3	Document Number Acer Flamingo	Rev SB
Date: Friday, July 13, 2001	Sheet 28 of 38	

Unused FGPI pins must not be float

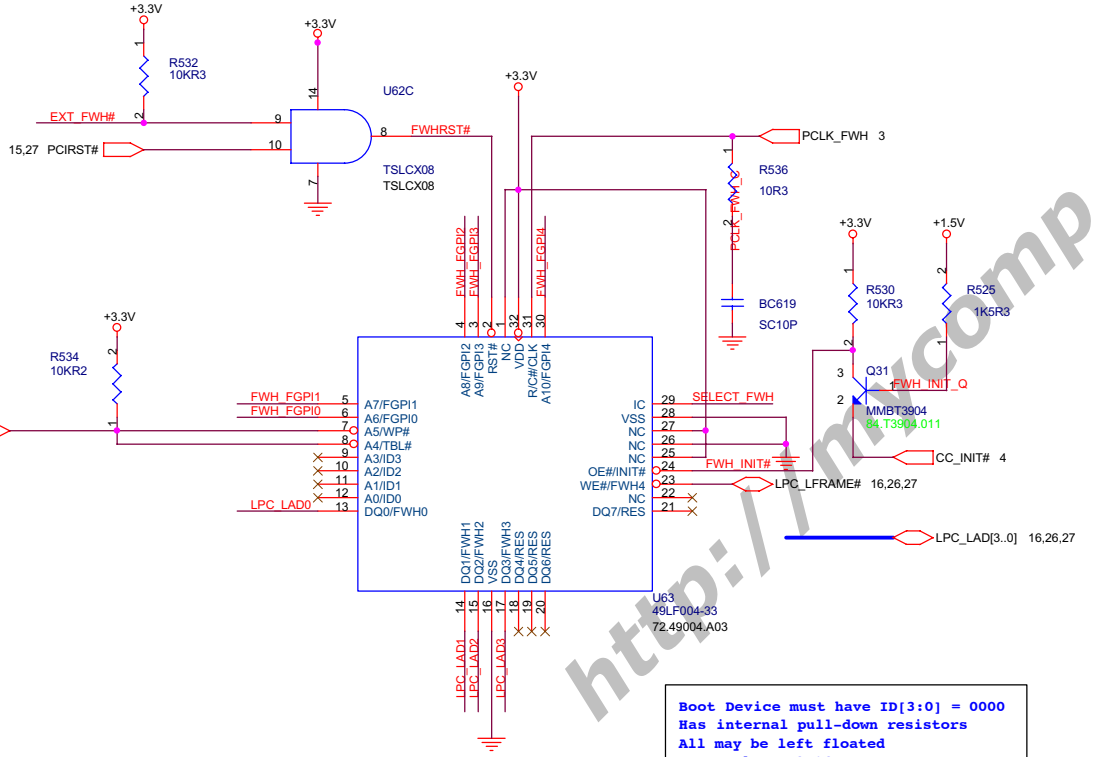


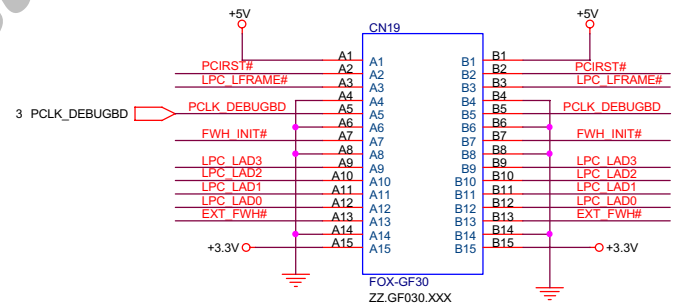
TOP VIEW

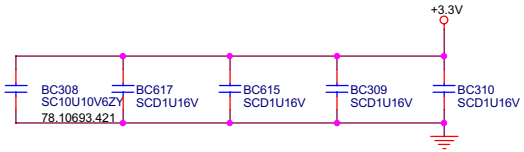
A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

(BOTTOM VIEW)

GOLDEN FINGER FOR DEBUG BOARD







Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46

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Title: FIRMWARE HUB & DEBUG PORT

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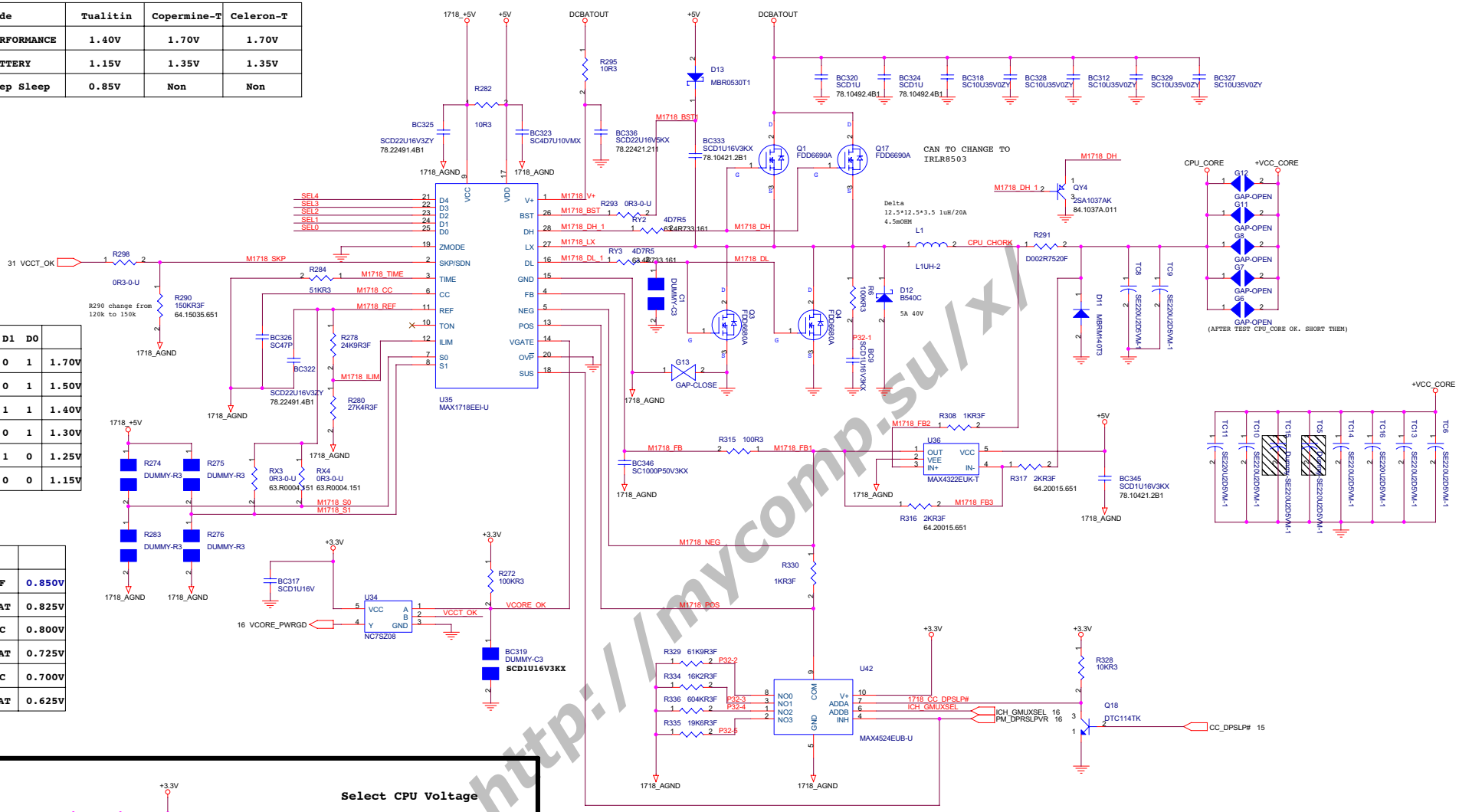
Mode	Tualitin	Copermine-T	Celeron-T
PERFORMANCE	1.40V	1.70V	1.70V
BATTERY	1.15V	1.35V	1.35V
Deep Sleep	0.85V	Non	Non

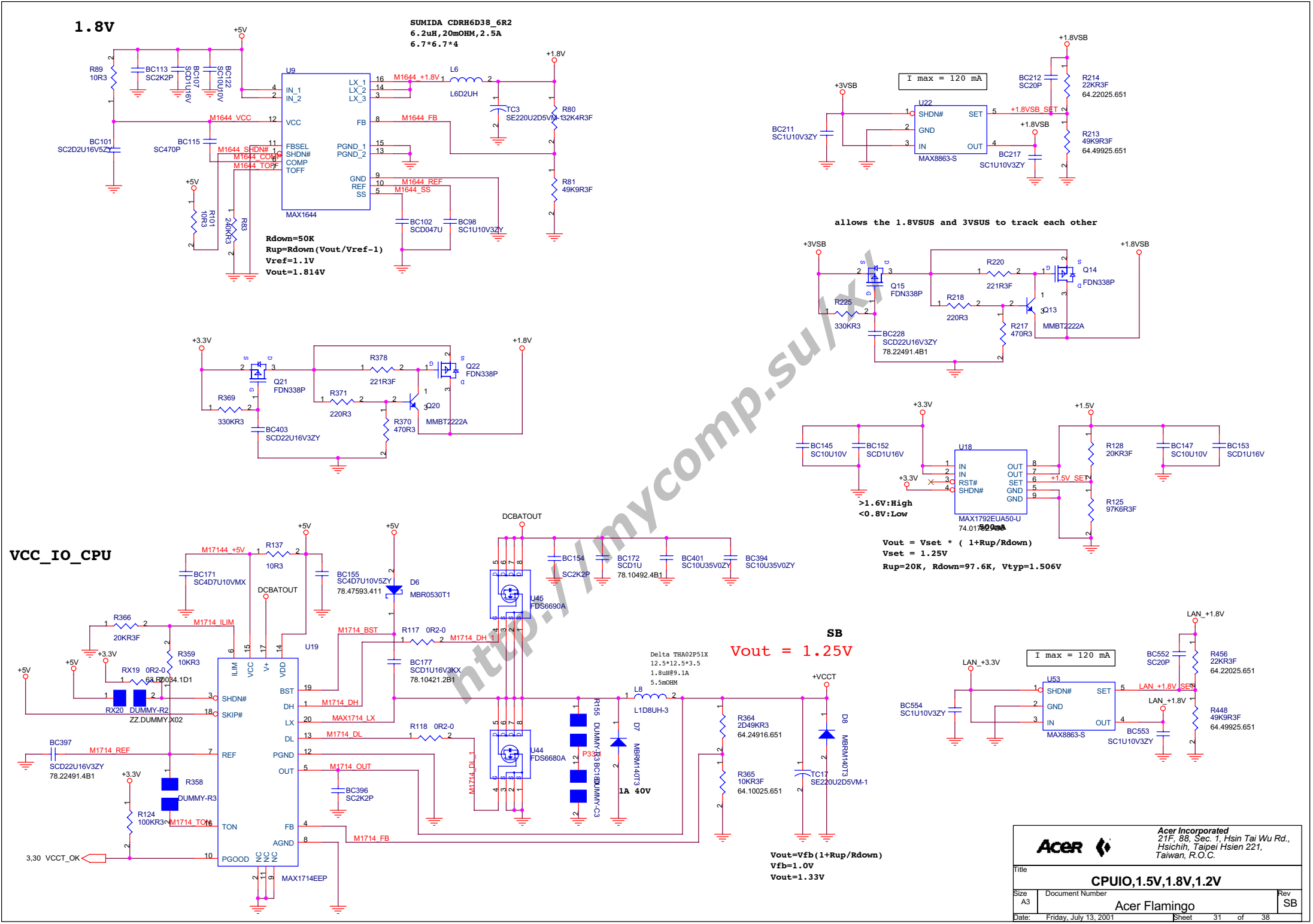
D4	D3	D2	D1	D0	
0	0	0	0	1	1.70V
0	0	1	0	1	1.50V
0	0	1	1	1	1.40V
0	1	0	0	1	1.30V
0	1	0	1	0	1.25V
0	1	1	0	0	1.15V

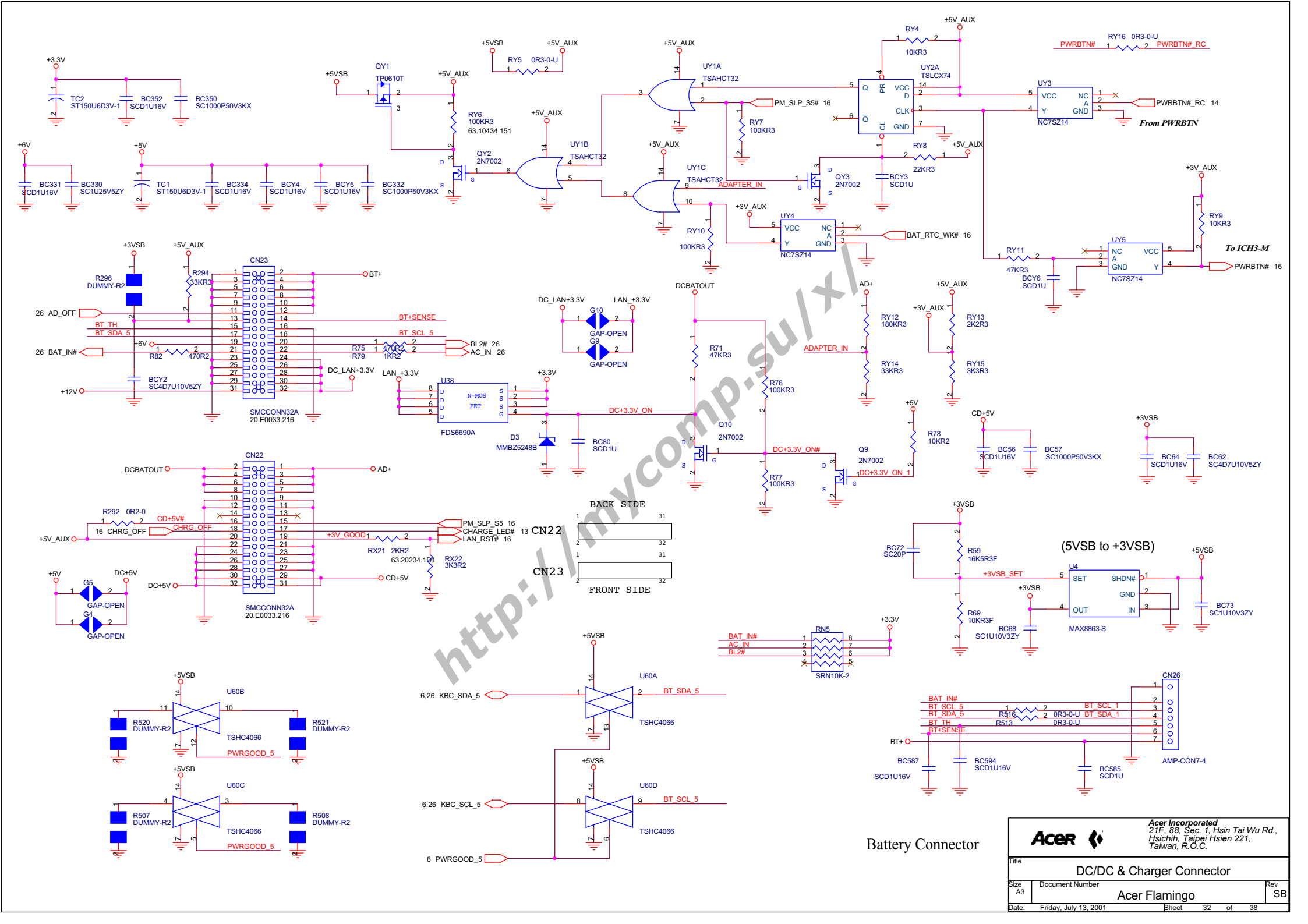
S1	S0	
REF	REF	0.850V
REF	FLOAT	0.825V
REF	VCC	0.800V
FLOAT	FLOAT	0.725V
FLOAT	VCC	0.700V
VCC	FLOAT	0.625V



BE#	BX	A0~A4	B0~B4
H	X	HIGH-Z	HIGH-Z
L	L	C0~C4	D0~D4
L	H	D0~D4	C0~C4

PM_DPRSLPVR	CC_DPSLP#	ICH_GMUXSEL	Voffset
1	X	X	0mV
0	0	0	-59mV
0	0	1	-52mV
0	1	0	-29mV
0	1	1	-3mV





Battery Connector

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Title	DC/DC & Charger Connector	
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CHKPW

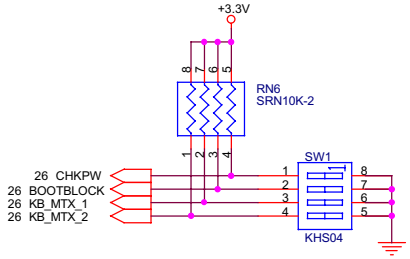
	Enable	Disable
SW1-1	ON	OFF

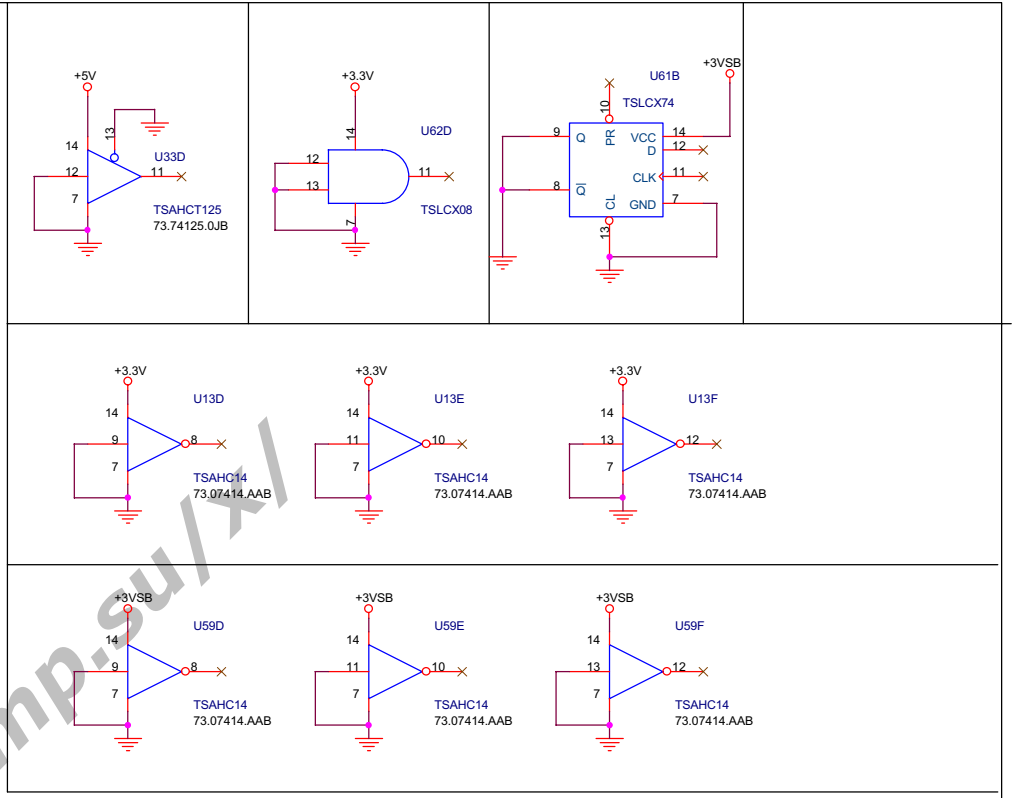
BIOS Bootblock erasable

	Enable	Disable
SW1-2	ON	OFF

Keyboard matrix

	US	Jap	Europe	US international
SW1-3	OFF	ON	OFF	OFF
SW1-4	OFF	OFF	ON	OFF





OEM Logo setting

COOLING SYSTEM SELECT

	Enable	Disable
SW1-8	ACER	HITACHI

	ACER	HITACHI	OEM2	OEM3
SW1-4	OFF	ON	OFF	ON
SW1-5	OFF	OFF	ON	ON

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Title: JUMP SETTING & NO USE GATE

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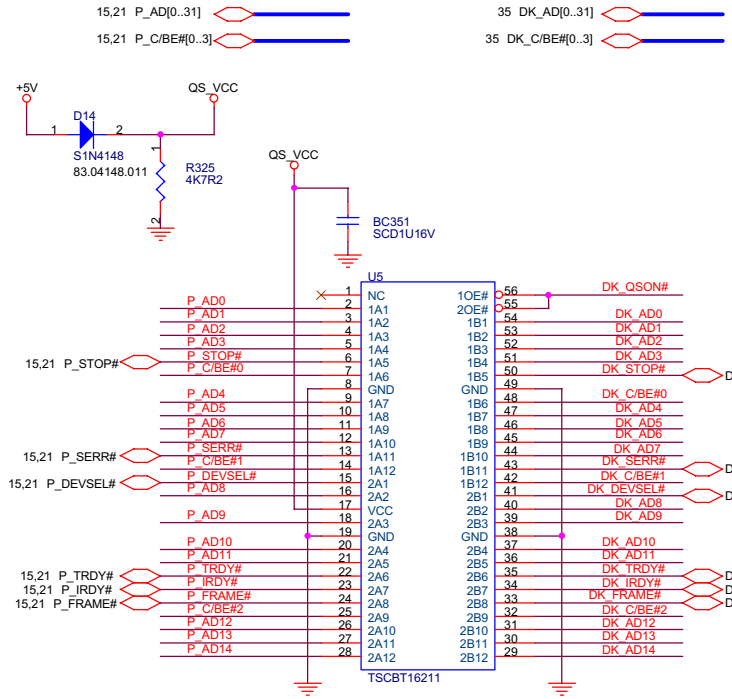
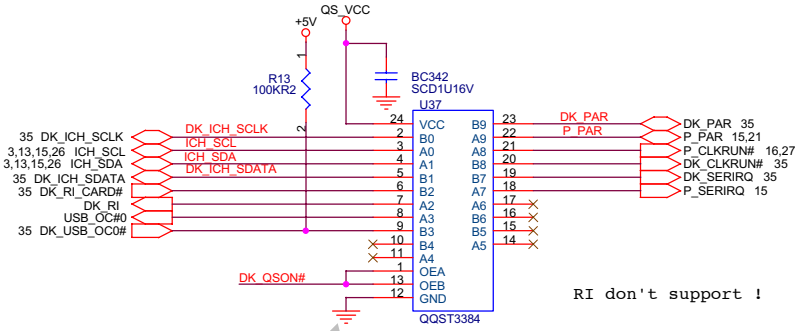
(CHANGE TO TSSOP PACKAGE)





RI don't support !

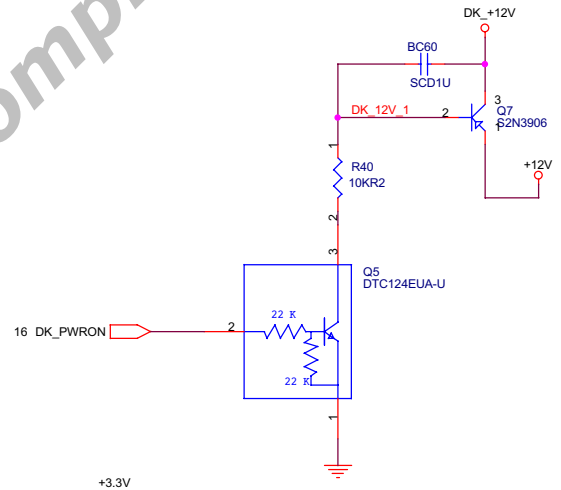
(STEP 1) SYSTEM CONTACT TO DOCK (GPIO[16] / DK_IN_5)

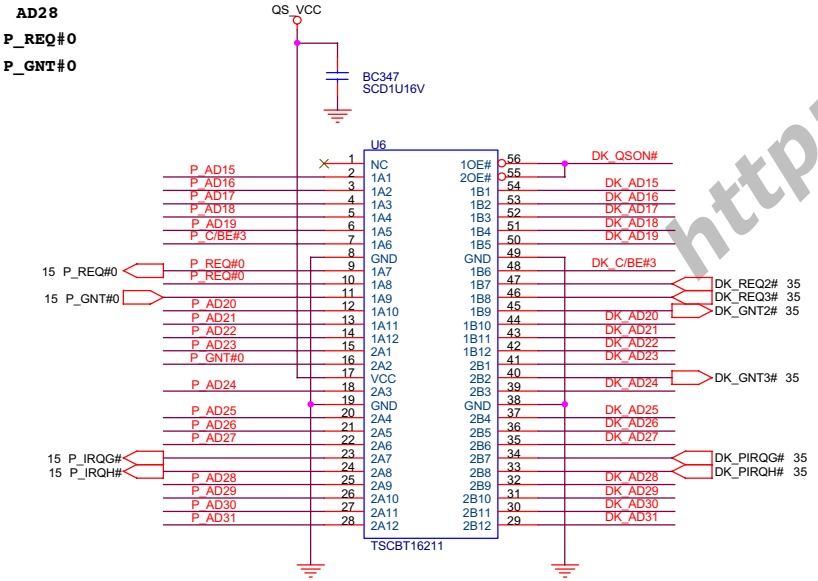
(STEP 2) TURN ON POWER (GPIO[14] / DK_PWR_ON_5) (POWER MOS AT DOCKING SIDE)

(STEP 3) CLK GEN. TURN ON DK PCICLK (KBC P61 / DK_CLK_ON#_3)

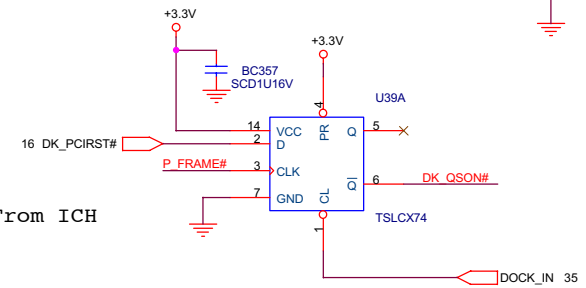
(STEP 4) GPO GENERATE PCIRST# (KBC P63 / DK_PCIRST)

(STEP5) TURN ON Q-SW





From ICH



From DOCK

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Title: DOCK (1/2)

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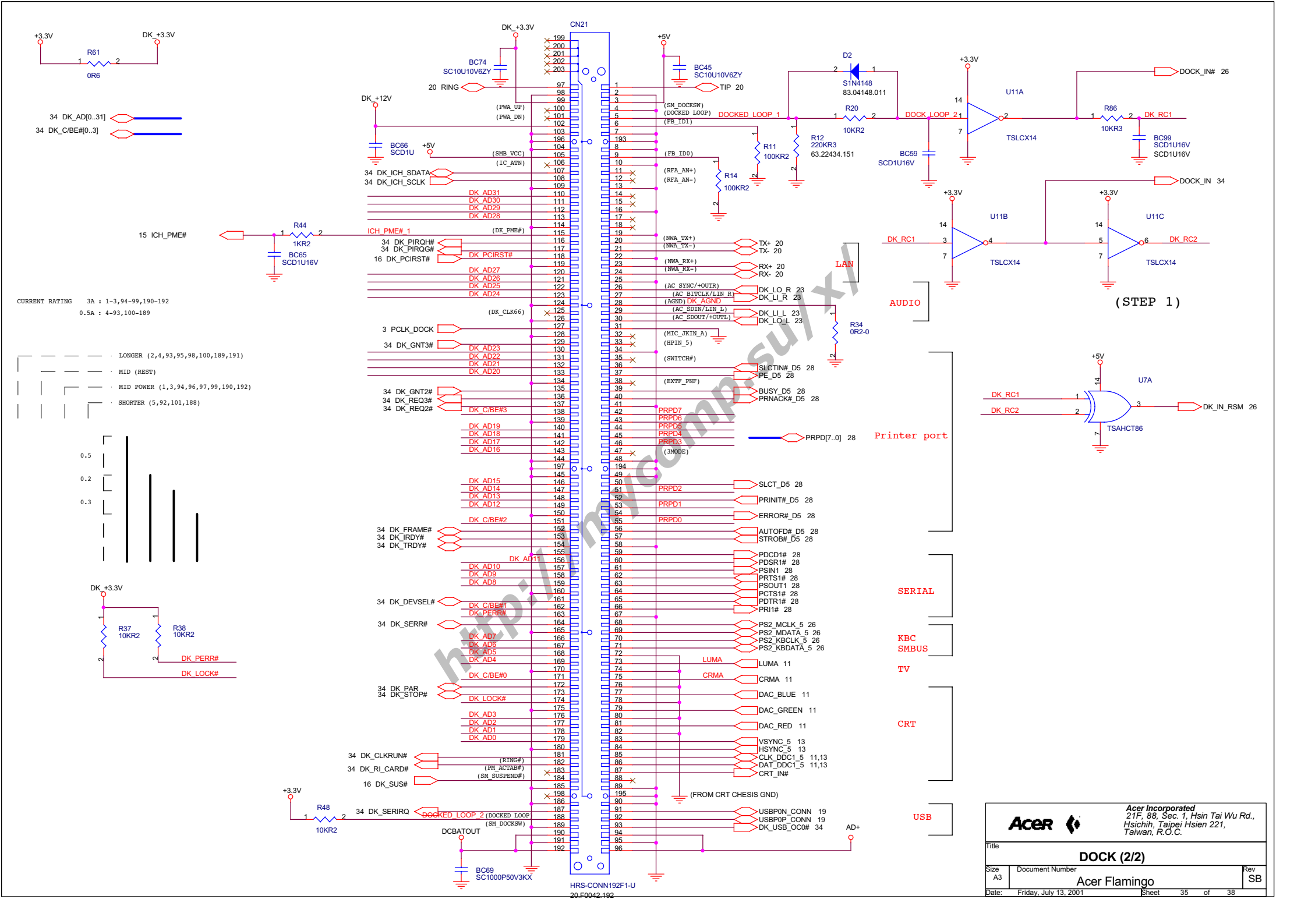

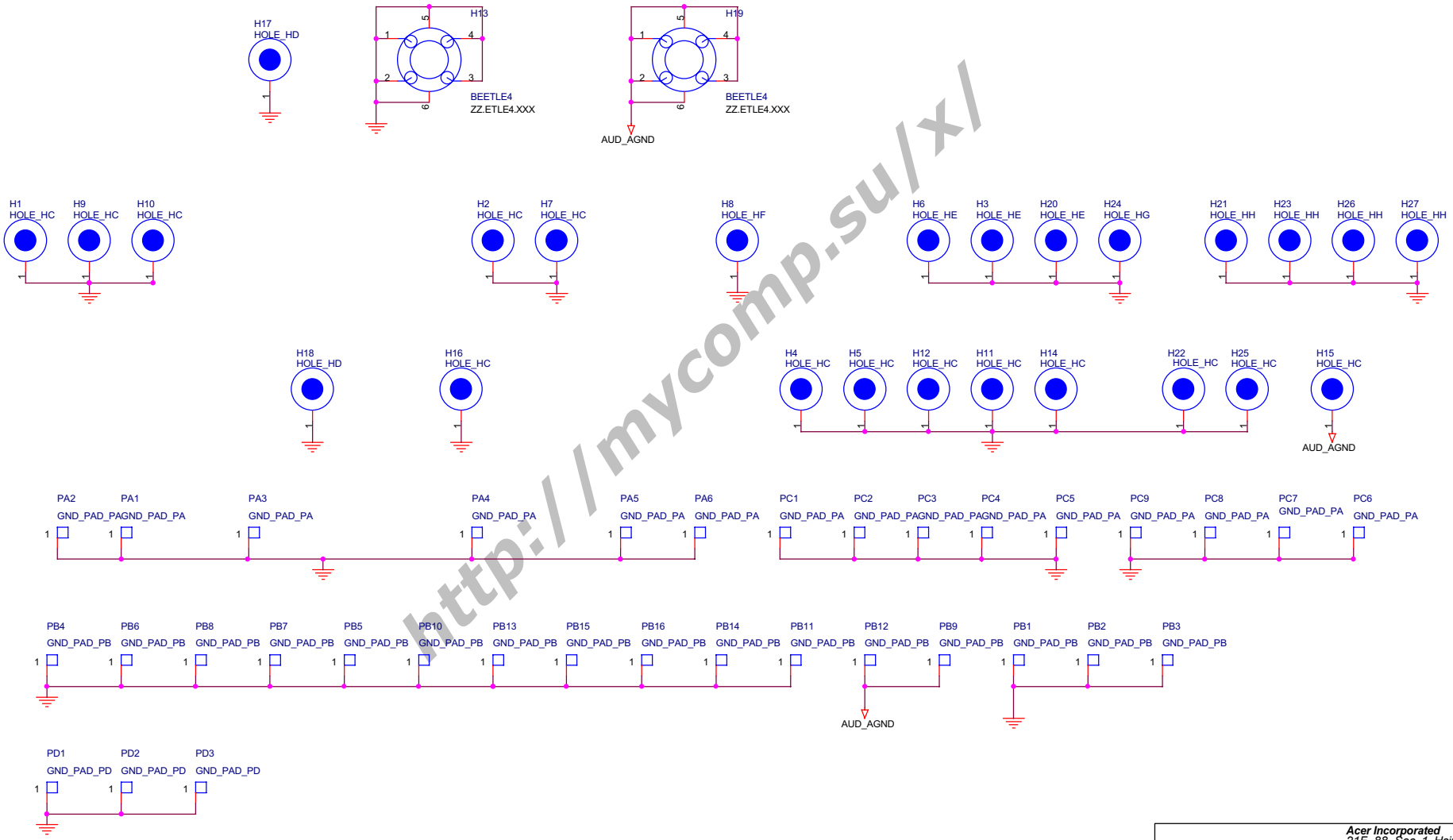

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Title
MACH. HOLE

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NEAR CPU

TP23 TPAD30
ZZ.PAD30.XXX
CC_SMI# 15

NEAR GMCH

NEAR VGA

TP22 TPAD30
ZZ.PAD30.XXX
VGA_MEM_CS1# 12

NEAR ICH3-M

TP24 TPAD30
ZZ.PAD30.XXX
P_IRQC# 15 15 P_REQ#2

TP26 TPAD30
ZZ.PAD30.XXX
P_IRQE# 15 15 P_REQ#3

TP28 TPAD30
ZZ.PAD30.XXX
P_IRQF# 15 15 P_REQ#4

TP25 TPAD30
ZZ.PAD30.XXX

TP27 TPAD30
ZZ.PAD30.XXX

TP29 TPAD30
ZZ.PAD30.XXX

TP30 TPAD30
ZZ.PAD30.XXX
15 P_GNT#2

TP31 TPAD30
ZZ.PAD30.XXX
15 P_GNT#3

TP32 TPAD30
ZZ.PAD30.XXX
15 P_GNT#4

NEAR IEEE1394

NEAR CARDBUS

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Taiwan, R.O.C.

Title: TEST POINT

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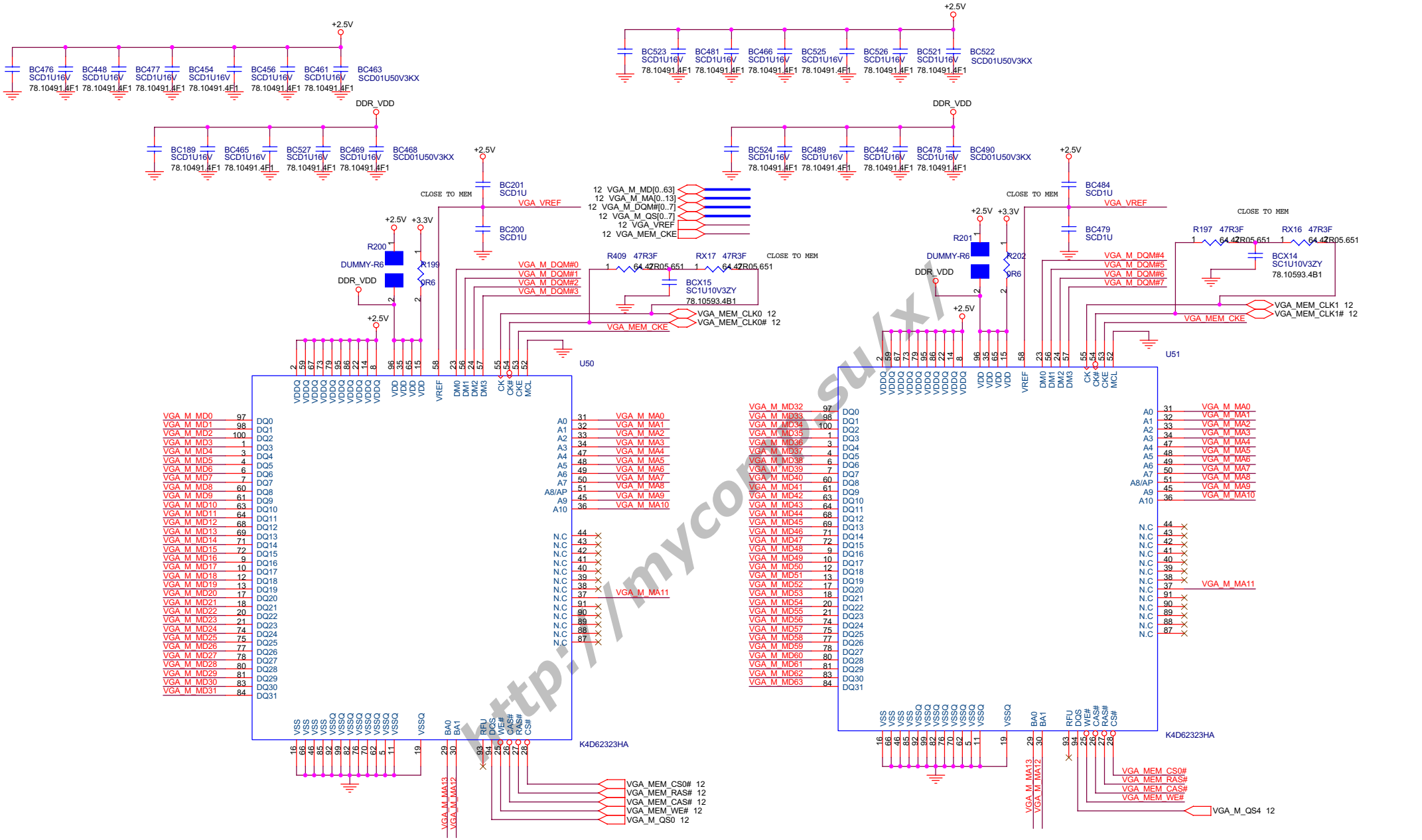

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Title: **TEST POINT**

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