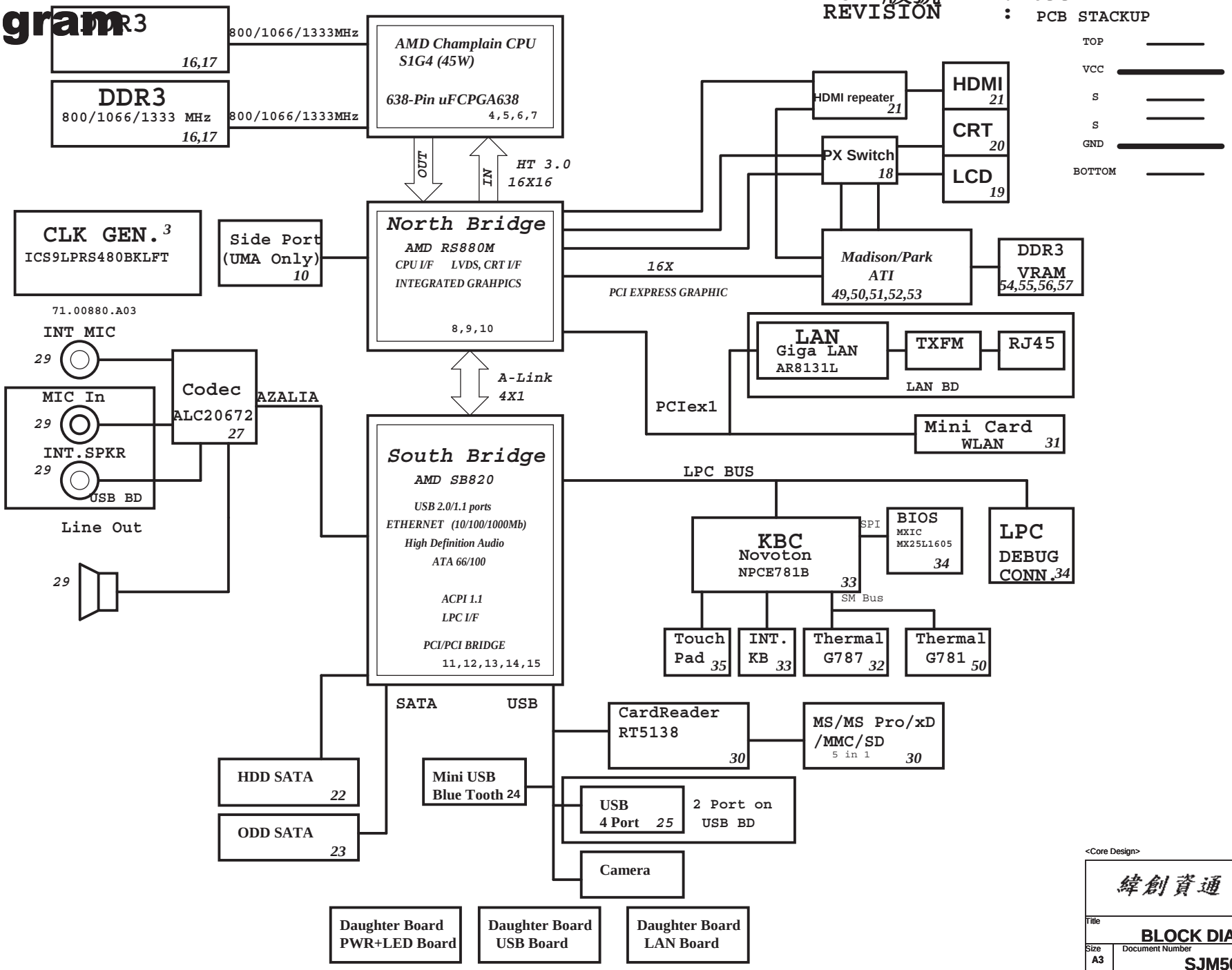
SJM50-DN Block Diagram

Project code: 91.4JJ01.001,91.4JK01.001
PCB P/N :
PCB 版號 : 09944
REVISION : PCB STACKUP



TOP
VCC
S
S
GND
BOTTOM

SYSTEM DC/DC RT8223 42	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(5.5A) 3D3V_S5(5A)

SYSTEM DC/DC RT8209E 43	
5V_S5	1D5V_S3(14A)

RT9026 43	
5V_S5	0D75_S3(1.2A)

SYSTEM DC/DC RT8209E 44	
INPUTS	
DCBATOUT	1D1V_S0(11A)

RT9025 44	
3D3V_S5	1D1V_S5(1.4A)

RT9025 45	
5V_S5	1D1V_VGA

RT9161 45	
3D3V_S0	2D5V_S0 (200mA)

RT9025 43	
1D5V_S3	1D05V_S0 (1.4A)

CHARGER BQ24745 46	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A UP+5V 5V 100mA

CPU DC/DC ISL6265HR 41	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.55V 18A VDDNB 0~1.55V 4A

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM
Size: A3 | Document Number: SJM50-DN | Rev: PD
Date: Monday, April 26, 2010 | Sheet 1 of 59

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: History

Size	Document Number	Rev
A3	SJM50-DN	PD

Date: Monday, April 26, 2010 Sheet 2 of 59

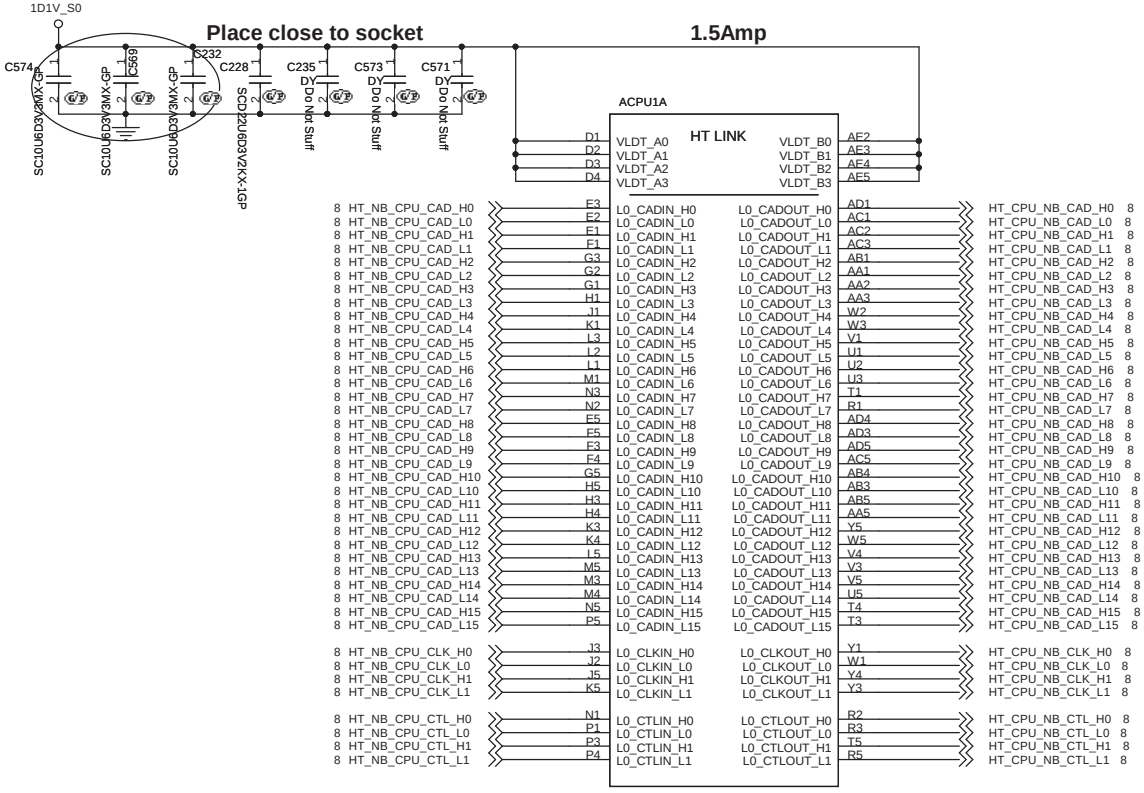
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CLKGEN_ICS9LPRS480

Size	Document Number	Rev
A3	SJM50-DN	PD

Date: Monday, April 26, 2010 Sheet 3 of 59

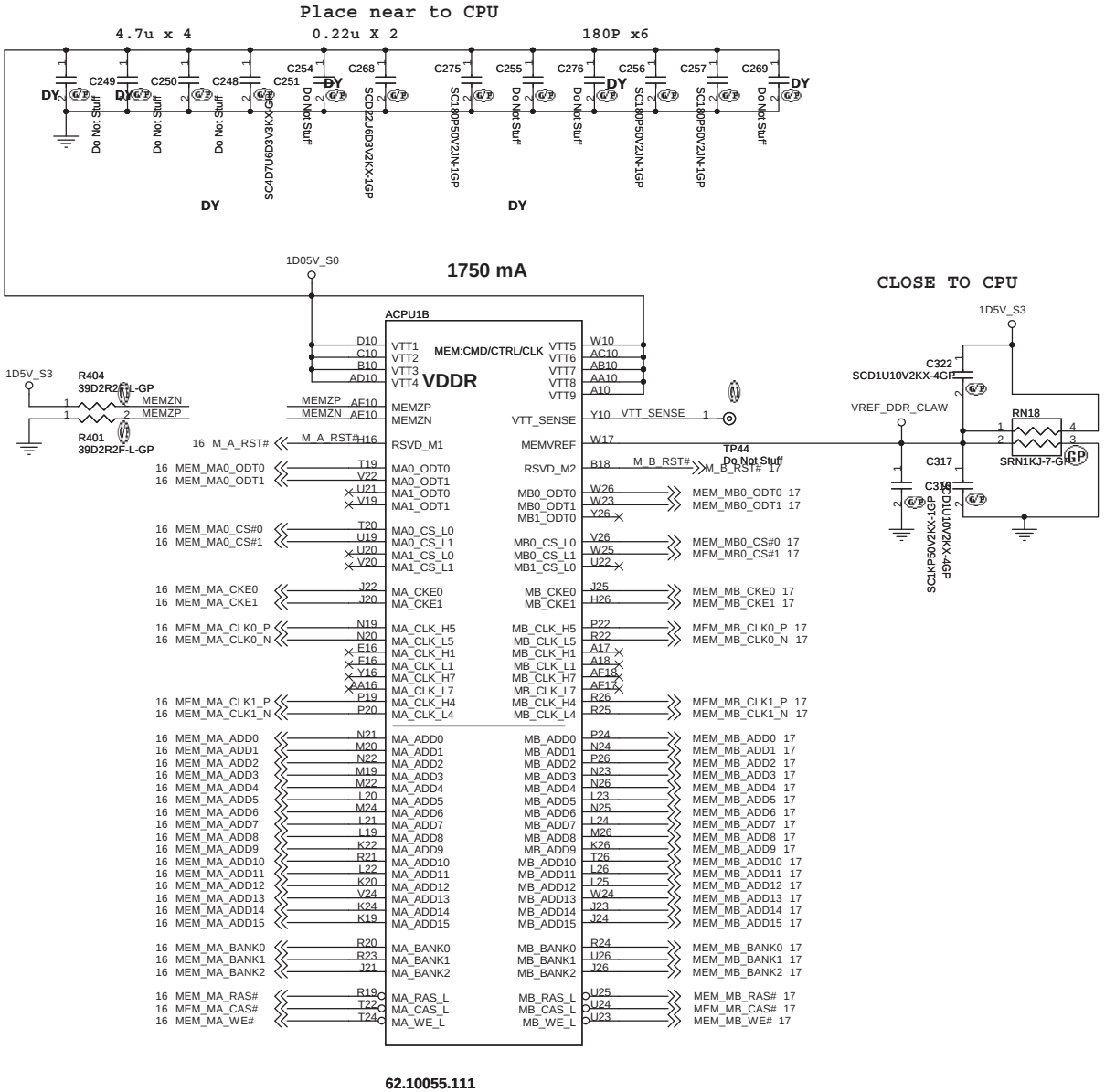


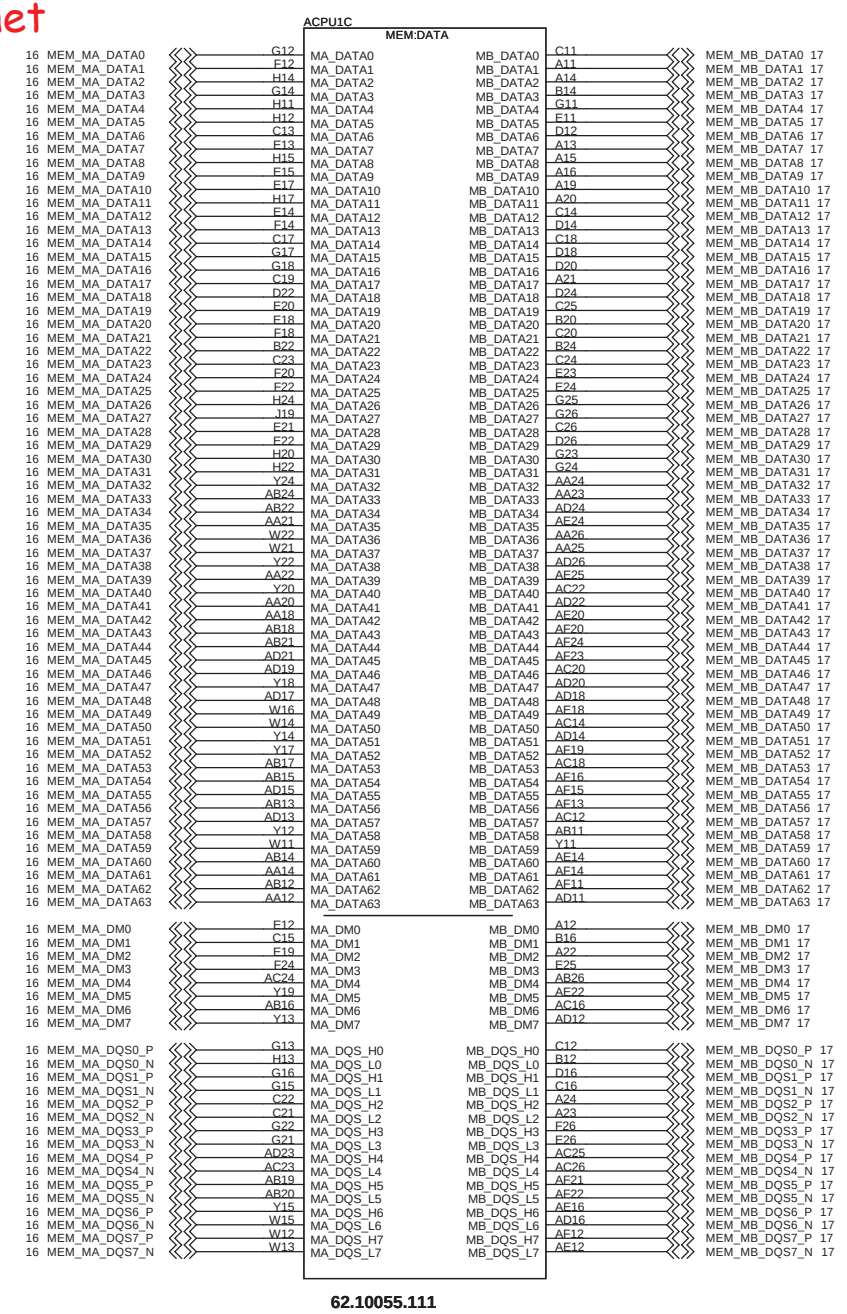
62.10055.111

SKT-BGA638H176

<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: CPU HT LINK I/F (1/4)		
Size: A3	Document Number: SJM50-DN	Rev: PD
Date: Monday, April 26, 2010	Sheet 4 of 59	





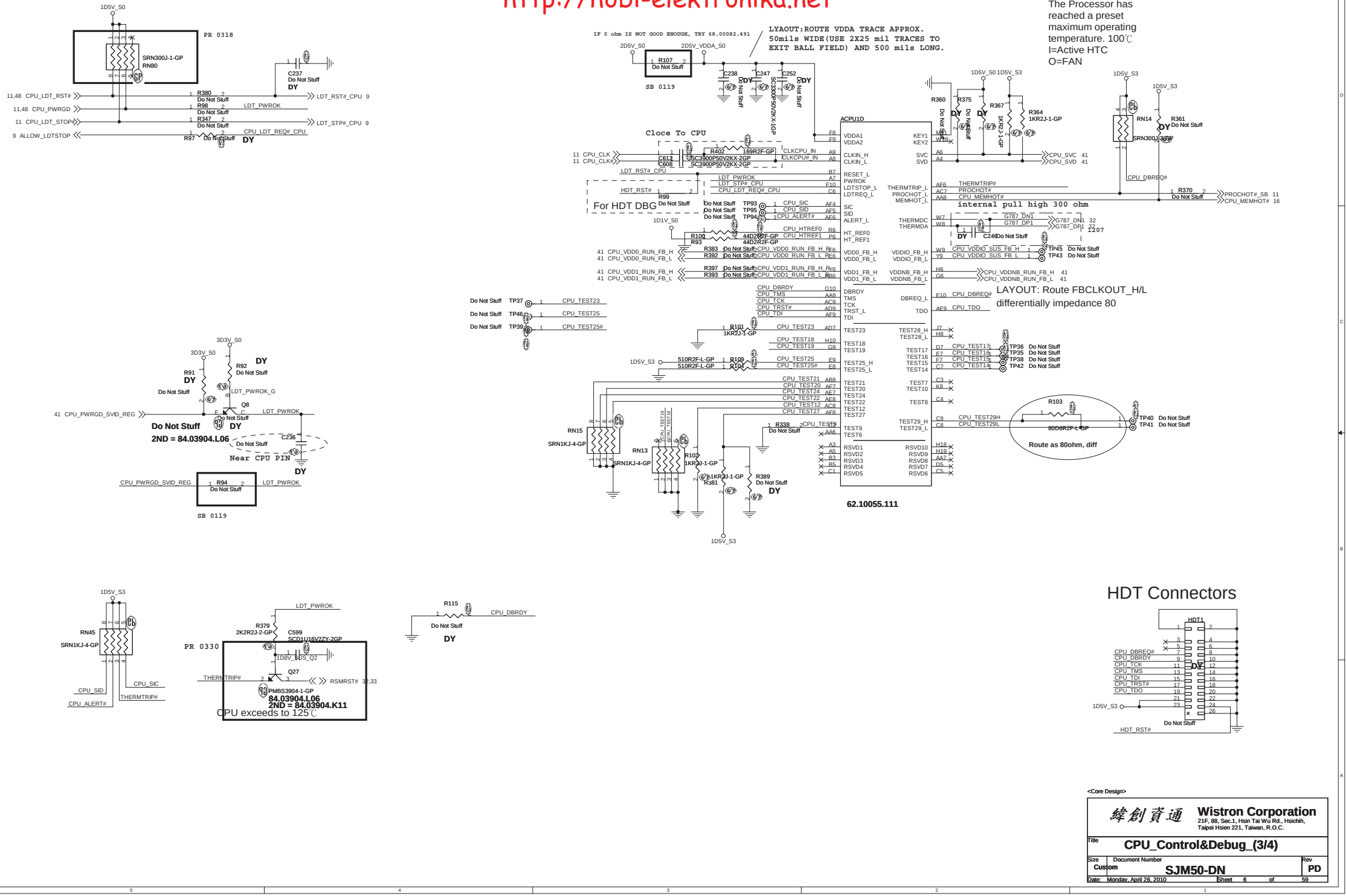
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_DDR_(2/4)

Size	Document Number	Rev
A3	SJM50-DN	PD

Date: Monday, April 26, 2010 Sheet 5 of 59



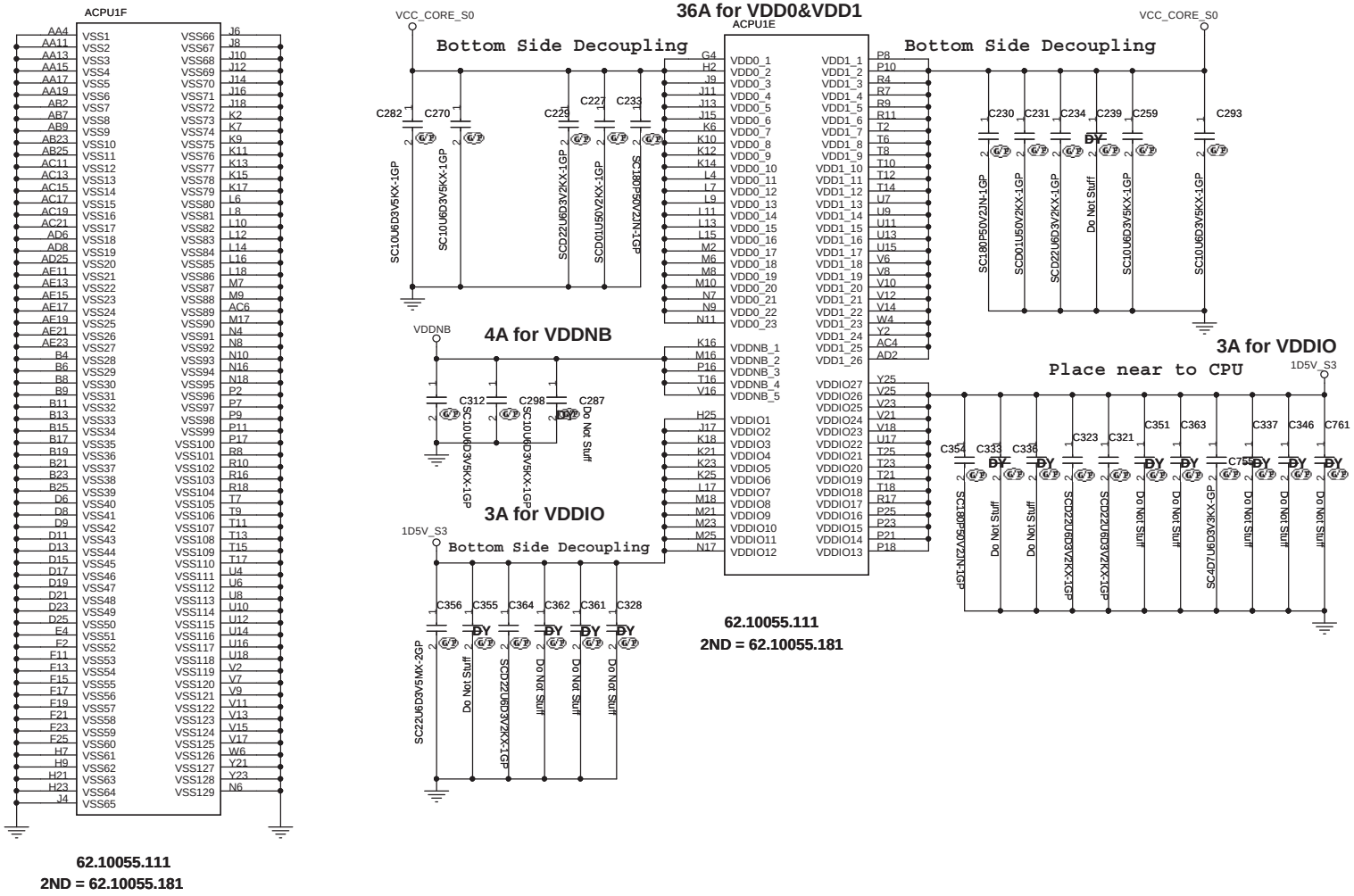
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_Control&Debug_(3/4)

Size: Custom | Document Number: SJM50-DN | Rev: PD

Date: Monday, April 26, 2010 | Sheet 6 of 59



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**CPU_Power_(4/4)**	
Size A3	Document Number **SJM50-DN**	Rev **PD**
Date: Monday, April 26, 2010	Sheet 7 of 59	

ANB1A

PART 1 OF 6

HYPER TRANSPORT CPU I/F

4 HT_CPU_NB_CAD_H0	Y25	HT_RXCAD0P	HT_TXCAD0P	D24	HT_NB_CPU_CAD_H0 4
4 HT_CPU_NB_CAD_L0	Y24	HT_RXCAD0N	HT_TXCAD0N	D25	HT_NB_CPU_CAD_L0 4
4 HT_CPU_NB_CAD_H1	V22	HT_RXCAD1P	HT_TXCAD1P	E24	HT_NB_CPU_CAD_H1 4
4 HT_CPU_NB_CAD_L1	V23	HT_RXCAD1N	HT_TXCAD1N	E25	HT_NB_CPU_CAD_L1 4
4 HT_CPU_NB_CAD_H2	V25	HT_RXCAD2P	HT_TXCAD2P	F24	HT_NB_CPU_CAD_H2 4
4 HT_CPU_NB_CAD_L2	V24	HT_RXCAD2N	HT_TXCAD2N	F25	HT_NB_CPU_CAD_L2 4
4 HT_CPU_NB_CAD_H3	U24	HT_RXCAD3P	HT_TXCAD3P	F23	HT_NB_CPU_CAD_H3 4
4 HT_CPU_NB_CAD_L3	U25	HT_RXCAD3N	HT_TXCAD3N	F22	HT_NB_CPU_CAD_L3 4
4 HT_CPU_NB_CAD_H4	T25	HT_RXCAD4P	HT_TXCAD4P	H23	HT_NB_CPU_CAD_H4 4
4 HT_CPU_NB_CAD_L4	T24	HT_RXCAD4N	HT_TXCAD4N	H22	HT_NB_CPU_CAD_L4 4
4 HT_CPU_NB_CAD_H5	P22	HT_RXCAD5P	HT_TXCAD5P	J25	HT_NB_CPU_CAD_H5 4
4 HT_CPU_NB_CAD_L5	P23	HT_RXCAD5N	HT_TXCAD5N	J24	HT_NB_CPU_CAD_L5 4
4 HT_CPU_NB_CAD_H6	P25	HT_RXCAD6P	HT_TXCAD6P	K24	HT_NB_CPU_CAD_H6 4
4 HT_CPU_NB_CAD_L6	P24	HT_RXCAD6N	HT_TXCAD6N	K25	HT_NB_CPU_CAD_L6 4
4 HT_CPU_NB_CAD_H7	N24	HT_RXCAD7P	HT_TXCAD7P	K23	HT_NB_CPU_CAD_H7 4
4 HT_CPU_NB_CAD_L7	N25	HT_RXCAD7N	HT_TXCAD7N	K22	HT_NB_CPU_CAD_L7 4
4 HT_CPU_NB_CAD_H8	AC24	HT_RXCAD8P	HT_TXCAD8P	F21	HT_NB_CPU_CAD_H8 4
4 HT_CPU_NB_CAD_L8	AC25	HT_RXCAD8N	HT_TXCAD8N	G21	HT_NB_CPU_CAD_L8 4
4 HT_CPU_NB_CAD_H9	AB25	HT_RXCAD9P	HT_TXCAD9P	G20	HT_NB_CPU_CAD_H9 4
4 HT_CPU_NB_CAD_L9	AB24	HT_RXCAD9N	HT_TXCAD9N	H21	HT_NB_CPU_CAD_L9 4
4 HT_CPU_NB_CAD_H10	AA24	HT_RXCAD10P	HT_TXCAD10P	J20	HT_NB_CPU_CAD_H10 4
4 HT_CPU_NB_CAD_L10	AA25	HT_RXCAD10N	HT_TXCAD10N	J21	HT_NB_CPU_CAD_L10 4
4 HT_CPU_NB_CAD_H11	Y22	HT_RXCAD11P	HT_TXCAD11P	J18	HT_NB_CPU_CAD_H11 4
4 HT_CPU_NB_CAD_L11	Y23	HT_RXCAD11N	HT_TXCAD11N	K17	HT_NB_CPU_CAD_L11 4
4 HT_CPU_NB_CAD_H12	W21	HT_RXCAD12P	HT_TXCAD12P	L19	HT_NB_CPU_CAD_H12 4
4 HT_CPU_NB_CAD_L12	W20	HT_RXCAD12N	HT_TXCAD12N	J19	HT_NB_CPU_CAD_L12 4
4 HT_CPU_NB_CAD_H13	V21	HT_RXCAD13P	HT_TXCAD13P	M19	HT_NB_CPU_CAD_H13 4
4 HT_CPU_NB_CAD_L13	V20	HT_RXCAD13N	HT_TXCAD13N	L18	HT_NB_CPU_CAD_L13 4
4 HT_CPU_NB_CAD_H14	U20	HT_RXCAD14P	HT_TXCAD14P	M21	HT_NB_CPU_CAD_H14 4
4 HT_CPU_NB_CAD_L14	U21	HT_RXCAD14N	HT_TXCAD14N	P21	HT_NB_CPU_CAD_L14 4
4 HT_CPU_NB_CAD_H15	U19	HT_RXCAD15P	HT_TXCAD15P	P18	HT_NB_CPU_CAD_H15 4
4 HT_CPU_NB_CAD_L15	U18	HT_RXCAD15N	HT_TXCAD15N	M18	HT_NB_CPU_CAD_L15 4
4 HT_CPU_NB_CLK_H0	T22	HT_RXCLK0P	HT_TXCLK0P	H24	HT_NB_CPU_CLK_H0 4
4 HT_CPU_NB_CLK_L0	T23	HT_RXCLK0N	HT_TXCLK0N	H25	HT_NB_CPU_CLK_L0 4
4 HT_CPU_NB_CLK_H1	AB23	HT_RXCLK1P	HT_TXCLK1P	L21	HT_NB_CPU_CLK_H1 4
4 HT_CPU_NB_CLK_L1	AA22	HT_RXCLK1N	HT_TXCLK1N	L20	HT_NB_CPU_CLK_L1 4
4 HT_CPU_NB_CTL_H0	M22	HT_RXCTL0P	HT_TXCTL0P	M24	HT_NB_CPU_CTL_H0 4
4 HT_CPU_NB_CTL_L0	M23	HT_RXCTL0N	HT_TXCTL0N	M25	HT_NB_CPU_CTL_L0 4
4 HT_CPU_NB_CTL_H1	R21	HT_RXCTL1P	HT_TXCTL1P	P19	HT_NB_CPU_CTL_H1 4
4 HT_CPU_NB_CTL_L1	R20	HT_RXCTL1N	HT_TXCTL1N	R18	HT_NB_CPU_CTL_L1 4
		HT_RXCALP	HT_TXCALP	B24	
		HT_RXCALN	HT_TXCALN	B25	

RS880M-1-GP

71.RS880.M05

R288 1 — HT_RXCALP — C23
301R2F-GP
HT_RXCALN — A24
Place < 100mils from pin C23 and A24

HT_TXCALP — B24 — 1 — R289 — 301R2F-GP
HT_TXCALN — B25
Place < 100mils from pin B25 and B24

Placement: close RS880

Placement: close RS880

for HDMI function

GTXP15	UMA_HDMI C483 1	Do Not Stuff	HDMI_DATA2+ 21
GTXN15	UMA_HDMI C476 1	Do Not Stuff	HDMI_DATA2- 21
GTXP14	UMA_HDMI C491 1	Do Not Stuff	HDMI_DATA1+ 21
GTXN14	UMA_HDMI C484 1	Do Not Stuff	HDMI_DATA1- 21
GTXP13	UMA_HDMI C496 1	Do Not Stuff	HDMI_DATA0+ 21
GTXN13	UMA_HDMI C490 1	Do Not Stuff	HDMI_DATA0- 21
GTXP12	UMA_HDMI C506 1	Do Not Stuff	HDMI_CLK+ 21
GTXN12	UMA_HDMI C498 1	Do Not Stuff	HDMI_CLK- 21

Exchange

ANB1B

PART 2 OF 6

PCIE I/F GFX

PEG_RXP15	D4	GFX_RX0P	GFX_TX0P	A5	GTXP15 DIS_PX1 C479 SCD1U16V2KX-3GP PEG_TXP15
PEG_RXN15	C4	GFX_RX0N	GFX_TX0N	B5	GTXN15 DIS_PX1 C475 SCD1U16V2KX-3GP PEG_TXN15
PEG_RXP14	A3	GFX_RX1P	GFX_TX1P	A4	GTXP14 DIS_PX1 C487 SCD1U16V2KX-3GP PEG_TXP14
PEG_RXN14	B3	GFX_RX1N	GFX_TX1N	B4	GTXN14 DIS_PX1 C480 SCD1U16V2KX-3GP PEG_TXN14
PEG_RXP13	C2	GFX_RX2P	GFX_TX2P	C3	GTXP13 DIS_PX1 C495 SCD1U16V2KX-3GP PEG_TXP13
PEG_RXN13	C1	GFX_RX2N	GFX_TX2N	B2	GTXN13 DIS_PX1 C486 SCD1U16V2KX-3GP PEG_TXN13
PEG_RXP12	E5	GFX_RX3P	GFX_TX3P	D1	GTXP12 DIS_PX1 C500 SCD1U16V2KX-3GP PEG_TXP12
PEG_RXN12	F5	GFX_RX3N	GFX_TX3N	D2	GTXN12 DIS_PX1 C497 SCD1U16V2KX-3GP PEG_TXN12
PEG_RXP11	G5	GFX_RX4P	GFX_TX4P	E2	GTXP11 DIS_PX1 C499 SCD1U16V2KX-3GP PEG_TXP11
PEG_RXN11	G6	GFX_RX4N	GFX_TX4N	E1	GTXN11 DIS_PX1 C505 SCD1U16V2KX-3GP PEG_TXN11
PEG_RXP10	H5	GFX_RX5P	GFX_TX5P	F4	GTXP10 DIS_PX1 C508 SCD1U16V2KX-3GP PEG_TXP10
PEG_RXN10	H6	GFX_RX5N	GFX_TX5N	F3	GTXN10 DIS_PX1 C510 SCD1U16V2KX-3GP PEG_TXN10
PEG_RXP9	J6	GFX_RX6P	GFX_TX6P	F1	GTXP9 DIS_PX1 C509 SCD1U16V2KX-3GP PEG_TXP9
PEG_RXN9	J5	GFX_RX6N	GFX_TX6N	F2	GTXN9 DIS_PX1 C511 SCD1U16V2KX-3GP PEG_TXN9
PEG_RXP8	J7	GFX_RX7P	GFX_TX7P	H4	GTXP8 DIS_PX1 C513 SCD1U16V2KX-3GP PEG_TXP8
PEG_RXN8	J8	GFX_RX7N	GFX_TX7N	H3	GTXN8 DIS_PX1 C515 SCD1U16V2KX-3GP PEG_TXN8
PEG_RXP7	L5	GFX_RX8P	GFX_TX8P	H1	GTXP7 DIS_PX1 C514 SCD1U16V2KX-3GP PEG_TXP7
PEG_RXN7	L6	GFX_RX8N	GFX_TX8N	H2	GTXN7 DIS_PX1 C516 SCD1U16V2KX-3GP PEG_TXN7
PEG_RXP6	M8	GFX_RX9P	GFX_TX9P	J2	GTXP6 DIS_PX1 C517 SCD1U16V2KX-3GP PEG_TXP6
PEG_RXN6	L8	GFX_RX9N	GFX_TX9N	J1	GTXN6 DIS_PX1 C519 SCD1U16V2KX-3GP PEG_TXN6
PEG_RXP5	P7	GFX_RX10P	GFX_TX10P	K4	GTXP5 DIS_PX1 C518 SCD1U16V2KX-3GP PEG_TXP5
PEG_RXN5	M7	GFX_RX10N	GFX_TX10N	K3	GTXN5 DIS_PX1 C520 SCD1U16V2KX-3GP PEG_TXN5
PEG_RXP4	P5	GFX_RX11P	GFX_TX11P	K1	GTXP4 DIS_PX1 C521 SCD1U16V2KX-3GP PEG_TXP4
PEG_RXN4	M5	GFX_RX11N	GFX_TX11N	K2	GTXN4 DIS_PX1 C522 SCD1U16V2KX-3GP PEG_TXN4
PEG_RXP3	R8	GFX_RX12P	GFX_TX12P	M4	GTXP3 DIS_PX1 C523 SCD1U16V2KX-3GP PEG_TXP3
PEG_RXN3	P8	GFX_RX12N	GFX_TX12N	M3	GTXN3 DIS_PX1 C524 SCD1U16V2KX-3GP PEG_TXN3
PEG_RXP2	R6	GFX_RX13P	GFX_TX13P	M1	GTXP2 DIS_PX1 C525 SCD1U16V2KX-3GP PEG_TXP2
PEG_RXN2	R5	GFX_RX13N	GFX_TX13N	M2	GTXN2 DIS_PX1 C526 SCD1U16V2KX-3GP PEG_TXN2
PEG_RXP1	P4	GFX_RX14P	GFX_TX14P	N2	GTXP1 DIS_PX1 C530 SCD1U16V2KX-3GP PEG_TXP1
PEG_RXN1	P3	GFX_RX14N	GFX_TX14N	N1	GTXN1 DIS_PX1 C527 SCD1U16V2KX-3GP PEG_TXN1
PEG_RXP0	T4	GFX_RX15P	GFX_TX15P	P1	GTXP0 DIS_PX1 C531 SCD1U16V2KX-3GP PEG_TXP0
PEG_RXN0	T3	GFX_RX15N	GFX_TX15N	P2	GTXN0 DIS_PX1 C532 SCD1U16V2KX-3GP PEG_TXN0

49 PEG_RXN[15..0]
49 PEG_RXP[15..0]

PEG_TXP[15..0] 49
PEG_TXN[15..0] 49

RS780M Display Port Support(muxed on GFX)

DP0	GFX_TX0,TX1,TX2,TX3,AUX0,HPD0
DP1	GFX_TX4,TX5,TX6,TX7,AUX1,HPD1

PCIE I/F GPP

GPP_RX0P	AE3	GPP_TX0P	AC1	TXP0	C537 1 SCD1U16V2KX-3GP PCIE_TXP0 26
GPP_RX0N	AD4	GPP_TX0N	AC2	TXN0	C538 1 SCD1U16V2KX-3GP PCIE_TXN0 26
GPP_RX1P	AE2	GPP_TX1P	AB4	TXP1	C533 1 SCD1U16V2KX-3GP PCIE_TXP1 31
GPP_RX1N	AD3	GPP_TX1N	AB3	TXN1	C534 1 SCD1U16V2KX-3GP PCIE_TXN1 31
GPP_RX2P	AD1	GPP_TX2P	AA2		
GPP_RX2N	AD2	GPP_TX2N	AA1		
GPP_RX3P	V5	GPP_TX3P	Y1		
GPP_RX3N	W6	GPP_TX3N	Y2		
GPP_RX4P	U5	GPP_TX4P	Y4		
GPP_RX4N	U6	GPP_TX4N	Y3		
GPP_RX5P	U8	GPP_TX5P	V1	GPP_TX5P	1
GPP_RX5N	U7	GPP_TX5N	V2	GPP_TX5N	1

LAN
MINICARD1

26 PCIE_RXP0
26 PCIE_RXN0
31 PCIE_RXP1
31 PCIE_RXN1

No mini2 card function
No new card function

TP14 Do Not Stuff 1 GPP_RX5P
TP13 Do Not Stuff 1 GPP_RX5N

No mini2 card function
No new card function

Exchange

LAN
MINICARD1

PCIE I/F SB

SB_RX0P	AA8	SB_TX0P	AD7	ALINK_NBTX_SBRX_P0	C544 1 SCD1U16V2KX-3GP ALINK_NBTX_C_SBRX_P0 11
SB_RX0N	Y8	SB_TX0N	AE7	ALINK_NBTX_SBRX_N0	C545 1 SCD1U16V2KX-3GP ALINK_NBTX_C_SBRX_N0 11
SB_RX1P	AA7	SB_TX1P	AE6	ALINK_NBTX_SBRX_P1	C541 1 SCD1U16V2KX-3GP ALINK_NBTX_C_SBRX_P1 11
SB_RX1N	Y7	SB_TX1N	AD6	ALINK_NBTX_SBRX_N1	C542 1 SCD1U16V2KX-3GP ALINK_NBTX_C_SBRX_N1 11
SB_RX2P	AA5	SB_TX2P	AB6	ALINK_NBTX_SBRX_P2	C549 1 SCD1U16V2KX-3GP ALINK_NBTX_C_SBRX_P2 11
SB_RX2N	AA6	SB_TX2N	AC6	ALINK_NBTX_SBRX_N2	C550 1 SCD1U16V2KX-3GP ALINK_NBTX_C_SBRX_N2 11
SB_RX3P	W5	SB_TX3P	AD5	ALINK_NBTX_SBRX_P3	C548 1 SCD1U16V2KX-3GP ALINK_NBTX_C_SBRX_P3 11
SB_RX3N	Y5	SB_TX3N	AE5	ALINK_NBTX_SBRX_N3	C547 1 SCD1U16V2KX-3GP ALINK_NBTX_C_SBRX_N3 11
		PCE_CALRP	AC8	PCE_PCAL	1
		PCE_CALRN	AB8	PCE_NCAL	R71 1 1K27R2F-L-GP 1D1V_S0
					R54 2KR2F-3-GP

A-LINK

11 ALINK_NBRX_SBTX_P0
11 ALINK_NBRX_SBTX_N0
11 ALINK_NBRX_SBTX_P1
11 ALINK_NBRX_SBTX_N1
11 ALINK_NBRX_SBTX_P2
11 ALINK_NBRX_SBTX_N2
11 ALINK_NBRX_SBTX_P3
11 ALINK_NBRX_SBTX_N3

RS880M-1-GP

Place < 100mils from pin AC8 and AB8

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-RS880M_HT LINK&PCIe(1/3)

Size: Custom | Document Number: SJM50-DN | Rev: PD

Date: Monday, April 26, 2010 | Sheet 8 of 59

STRAP_DEBUG_BUS_GPIO_ENABLEb
Enables the Test Debug Bus using GPIO.(PIN: RS880M--> VSYNC#)
*1 :Disable 0 : Enable

RS880: Enables Side port memory (RS880 use HSYNC#)
*1 :Disable 0 : Enable

SUS_STAT#
Selects Loading of STRAPS From EEPROM
*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

Close to NB ball

ENABLE External CLK GEN

UMA-->L1-->2R 0603
C62-->47U/6.3V
DIS-->L1-->Bead
C62-->DY

SB 0119

PR 0330

RS880M-1-GP

71.RS880.M05

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-RS880M LVDS&CRT (2/3)
Size: A3 | Document Number: SJM50-DN | Rev: PD
Date: Monday, April 26, 2010 | Sheet 9 of 59

1027 For AMD review request

0.6A per ANT Rev1.1, Page3

220 ohm @ 100MHz,2A

68.00206.121

2ND = 68.00216.161

0.45A per ANT Rev1.1, Page3

220 ohm @ 100MHz,2A

68.00206.121

2ND = 68.00216.161

80mil Width

220 ohm @ 100MHz,2A

68.00206.121

2ND = 68.00216.161

1.8 V at 25 mA.

1027 For AMD review request

300mil Width

1103

10A per ANT Rev1.1, Page3

Per check list (Rev 0.02)

RS780M: 1V ~ 1.1V, check PWR team

+NB_VCORE

0.95~1.1V

For side port 1110

1.5 V at 100 mA for DDR3

SB 0119

ANB1E PART 5/6 POWER

ANB1F PART 6/6 GROUND

RS880M-1-GP

Side-Port

ANB1D PART 4 OF 6 SBD_MEM/DVO_I/F

MEM_COMP_P and MEM_COMP_N trace width >=10mils and 10mils spacing from other Signals in X,Y,Z directions

68.00084.921

2ND = 68.00217.401

BLM15AG121SN-1GP

12/9

1006

U7 H5TQ1G63BFR-12C-GP

1210 swap

DDR3_RST# 12

CLOSE TO NB

CLOSE TO SDRAM

<Core Design>

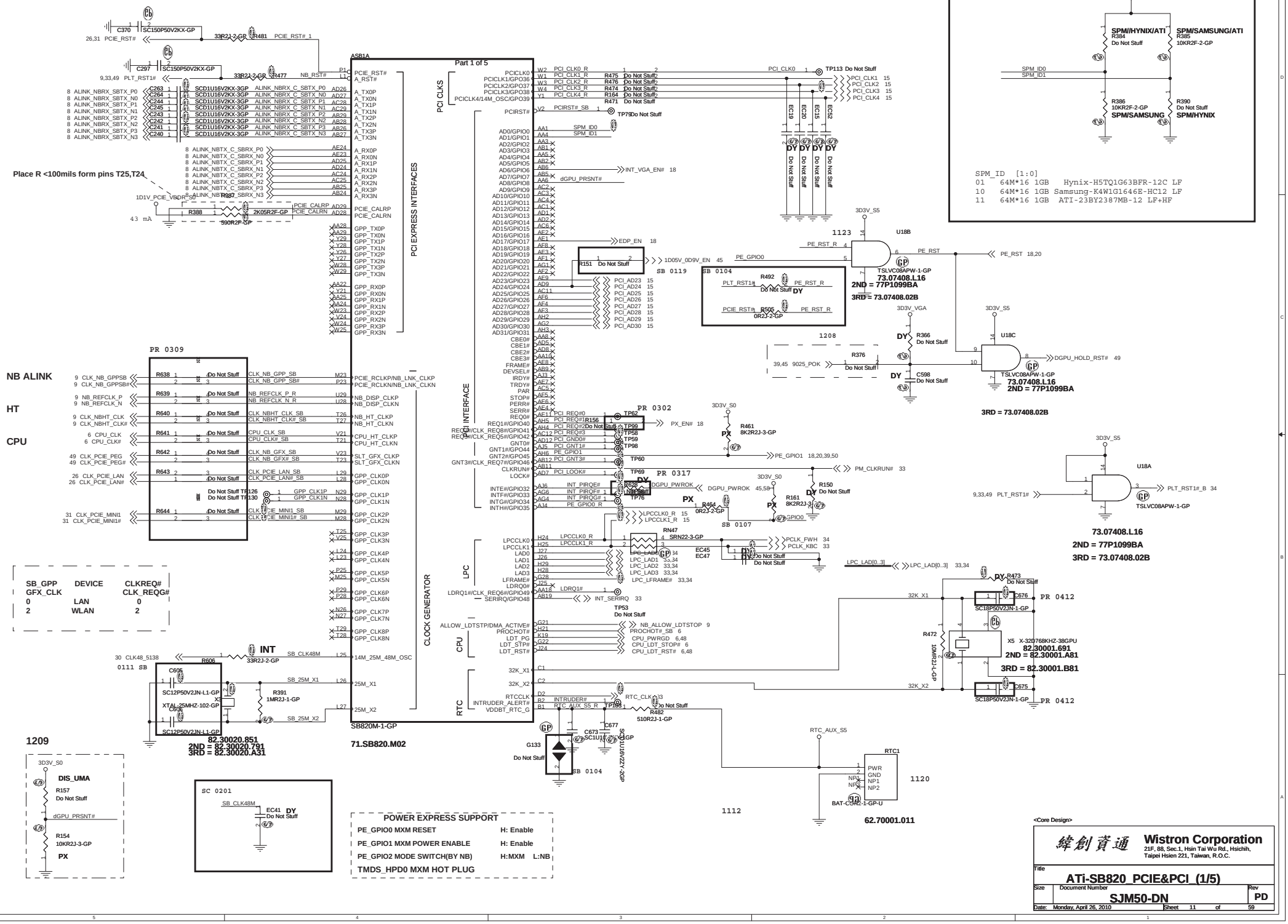
Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-RS880M_Side Port&PWR&GND(3/3)

Size: A2 | Document Number: SJM50-DN | Rev: PD

Date: Monday, April 26, 2010 | Sheet 10 of 59



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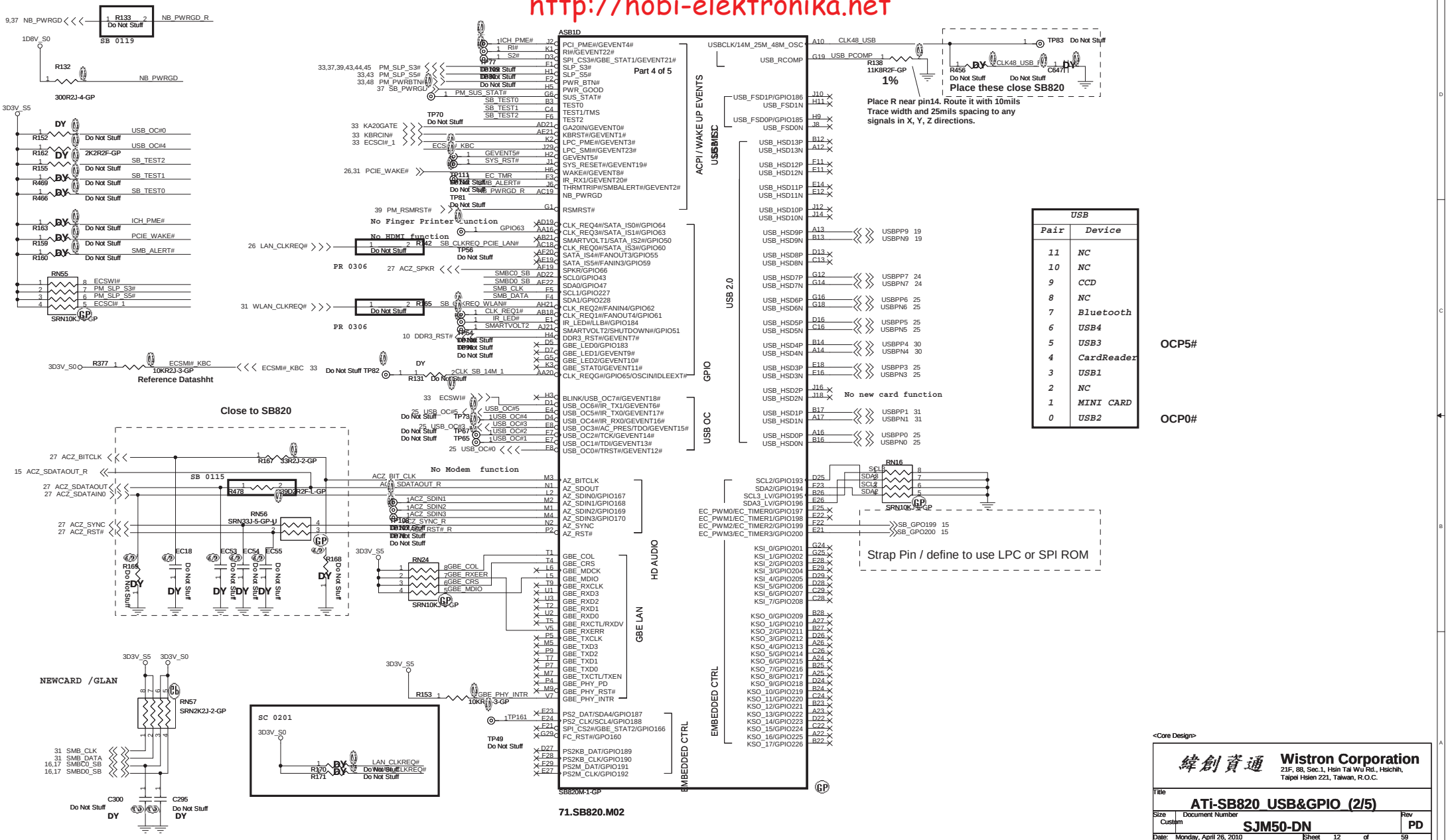
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB820_PCIE&PCI_(1/5)

Size | Document Number | Rev
SJM50-DN | PD

Date: Monday, April 26, 2010 | Sheet 11 of 59



<Core Design>
緯創資通 Wistron Corporation
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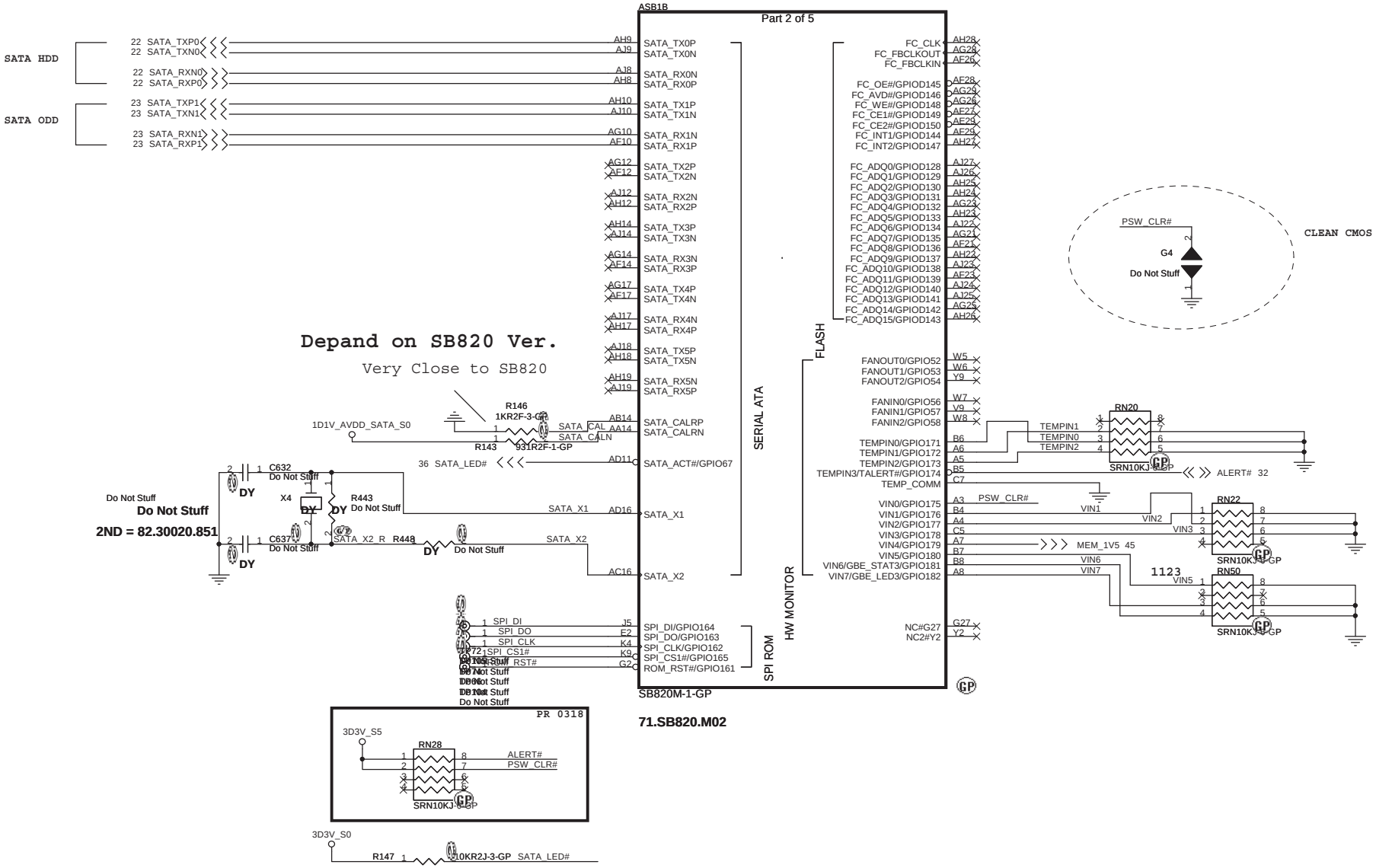
Title: ATi-SB820_USB&GPIO_(2/5)

Size: Custom | Document Number: SJM50-DN | Rev: PD

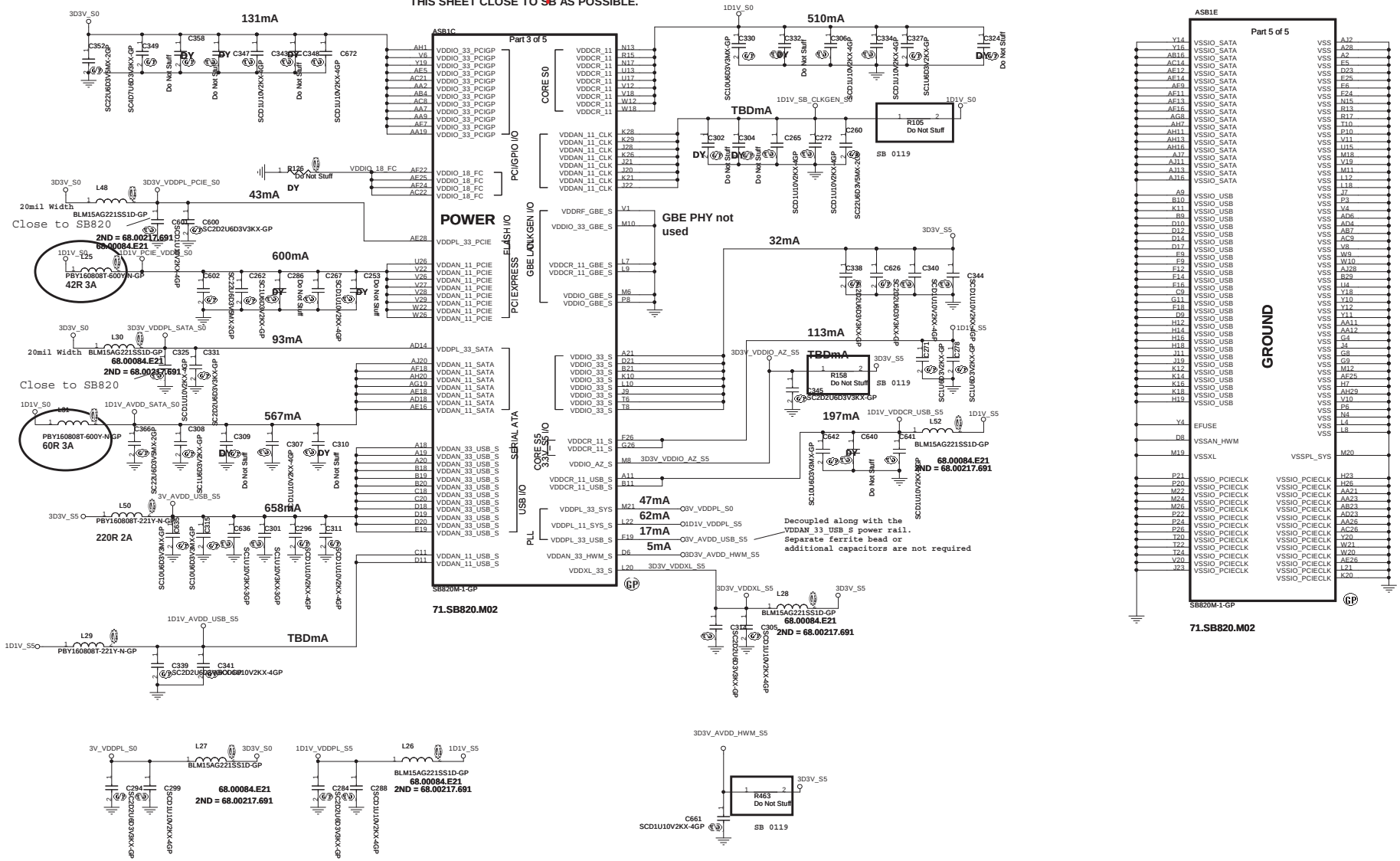
Date: Monday, April 26, 2010 | Sheet 12 of 59



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**ATi-SB820 SATA-IDE (3/5)**
Size: A3	Document Number: SJM50-DN
Rev: PD	
Date: Monday, April 26, 2010	Sheet 13 of 59

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

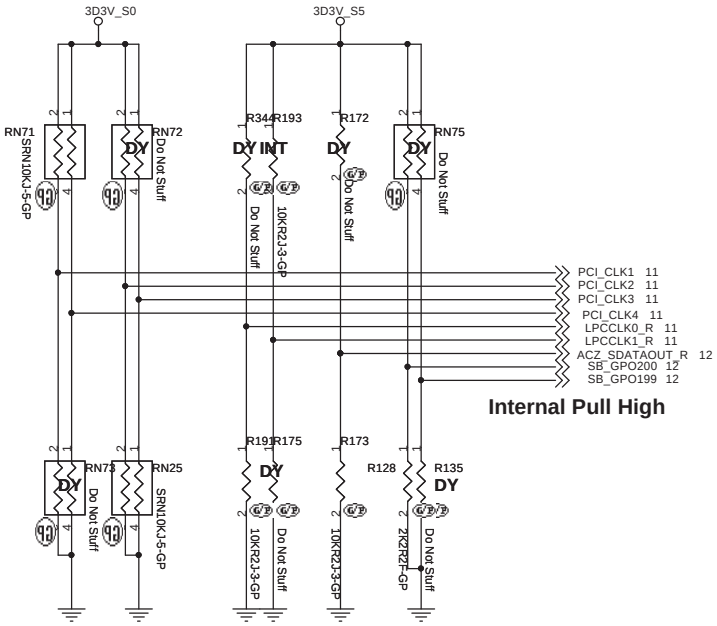


UMA

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: ATi-SB820_POWER&GND_(4/5)		
Size: Custom	Document Number: SJM50-DN	Rev: PD
Date: Monday, April 26, 2010	Sheet 14 of 59	

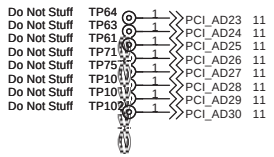
REQUIRED STRAPS

REQUIRED SYSTEM STRAPS



	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	AZ_SDOUT	GPIO200 GPIO199
PULL HIGH	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	LOW POWER MODE	H,H = Reserved H,L = SPI ROM
PULL LOW	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	PERFORMANCE MODE DEFAULT	L,H = LPC ROM (Default) L,L = FWH ROM

DEBUG STRAPS



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

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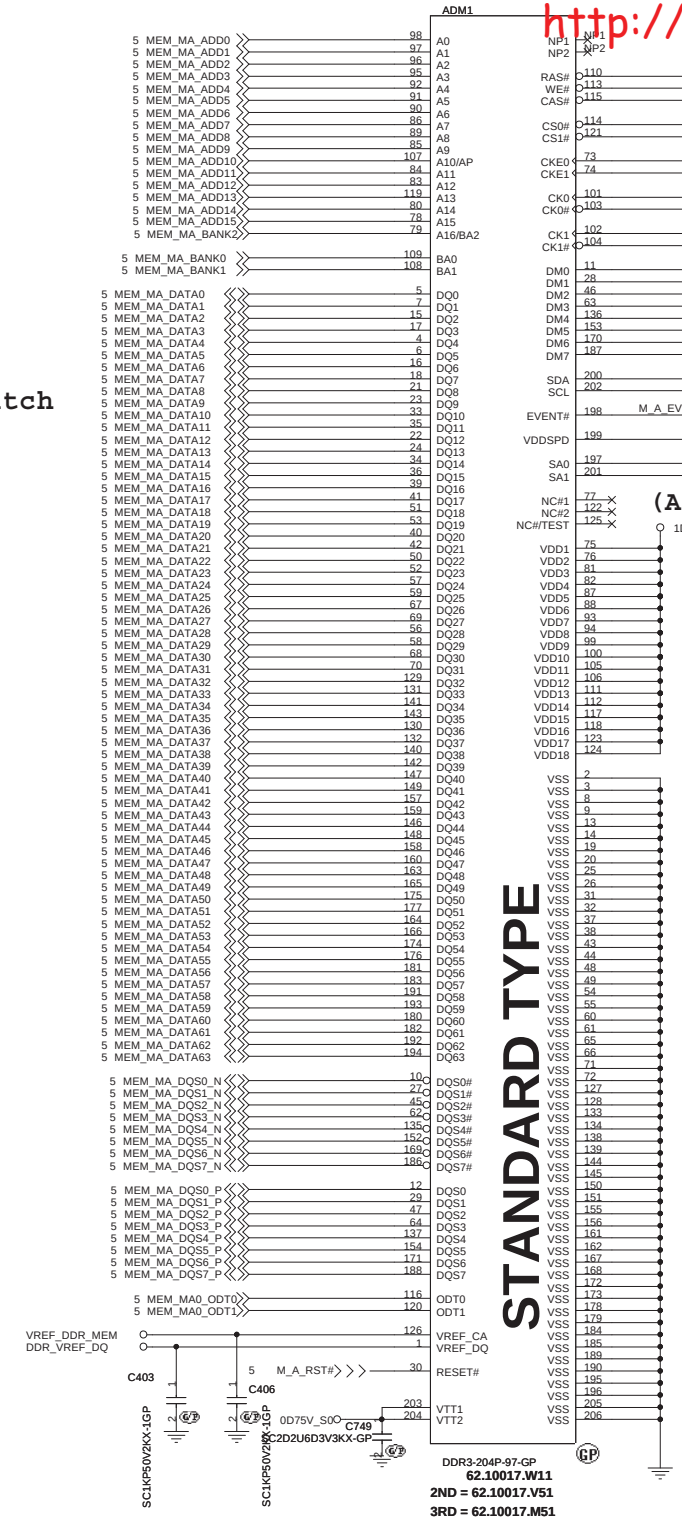
Title: ATi-SB820 STRAPPING (5/5)

Size: A3 | Document Number: SJM50-DN | Rev: PD

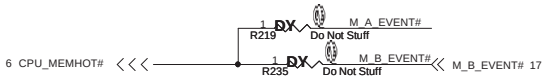
Date: Monday, April 26, 2010 | Sheet 15 of 59

place ADM1
close to CPU
for length match

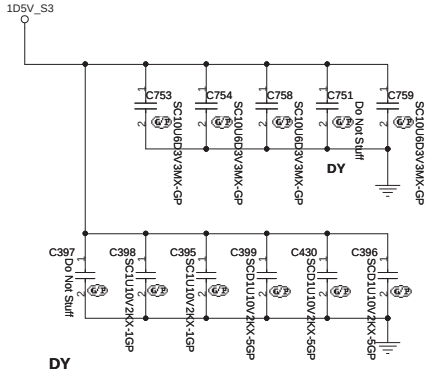


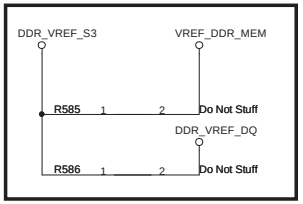
Layout Note:
Place these Caps near
SO-DIMMA.

Check if SB need
Memhot event



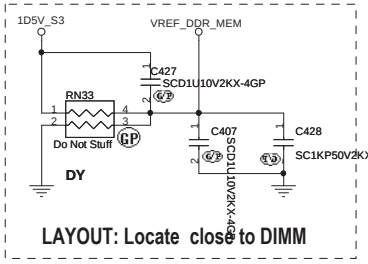
SODIMM A DECOUPLING





SB 0119

VREF_DDR_MEM



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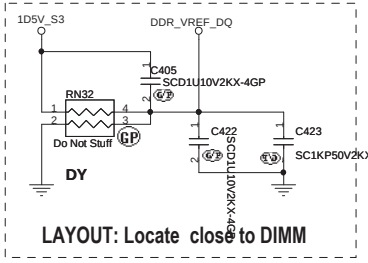

<Core Design>

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Title: DDRIII_SO-DIMM SKT_1

Size	Document Number	Rev
Custom	SJM50-DN	PD

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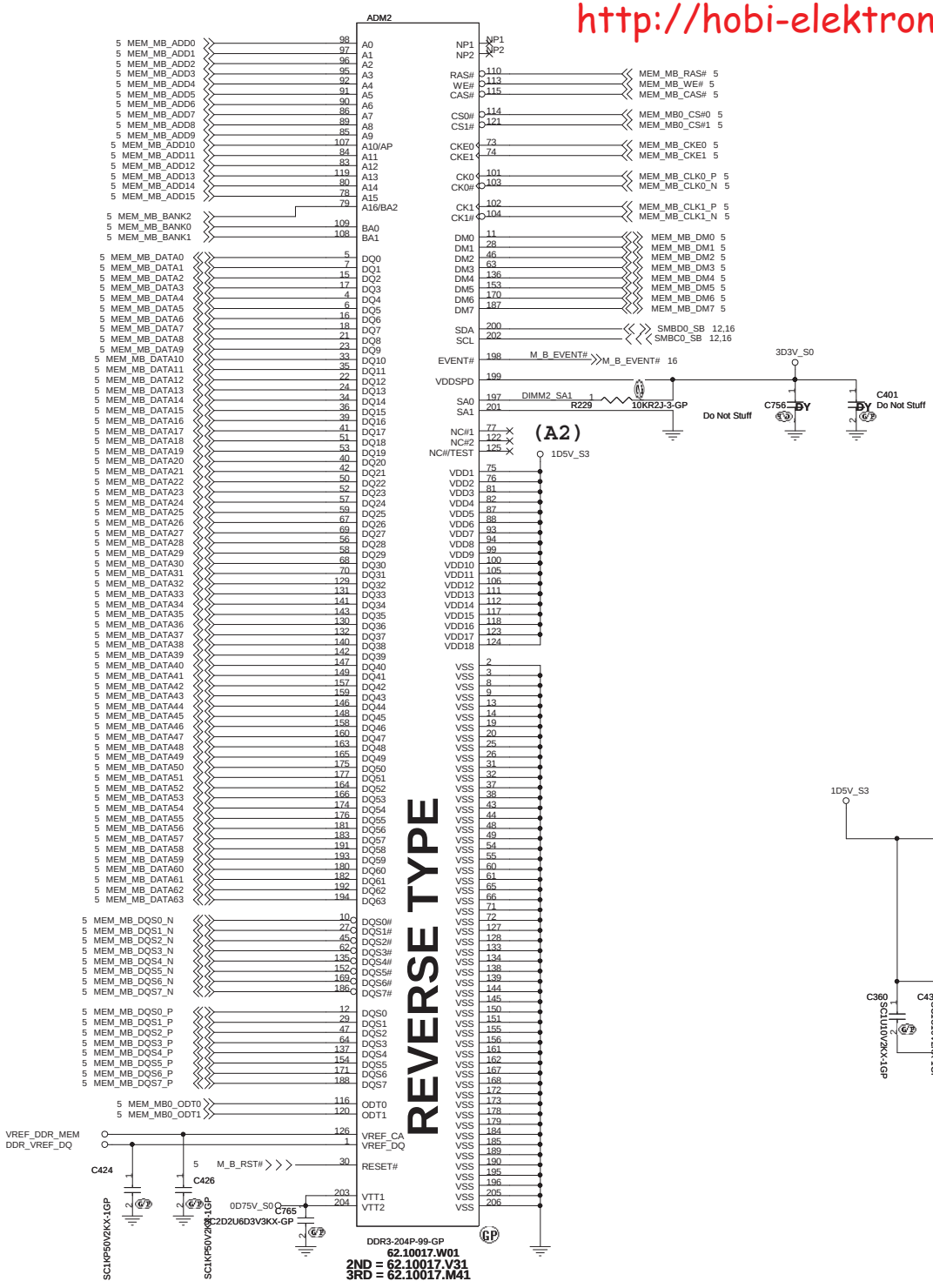

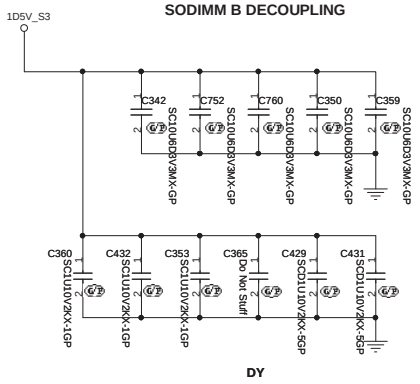

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: DDRIII_SO-DIMM SKT_2

Size	Document Number	Rev
Custom	SJM50-DN	PD

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LVDS

Truth Table

Function	SEL
A_N to $_NB_1$	L
A_N to $_NB_2$	H

CRT

$\overline{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S=0
L	H	IA1	IB1	IC1	ID1	S=1

EDID

Function Table

Input (S)	Function
L	B_0 Connected to A
H	B_1 Connected to A

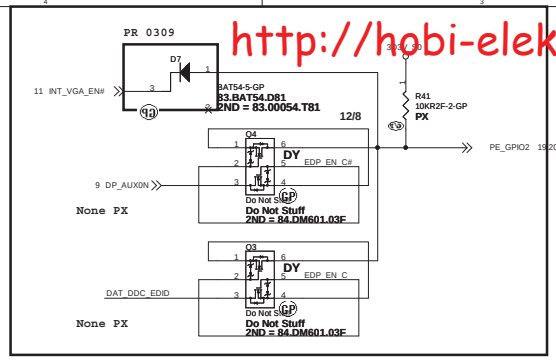
H = HIGH Logic Level L = LOW Logic Level

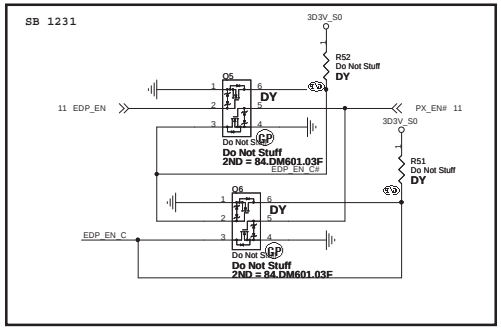
BLON_IN

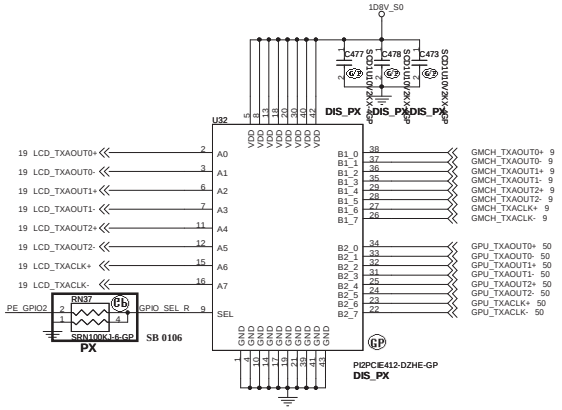
Function Table

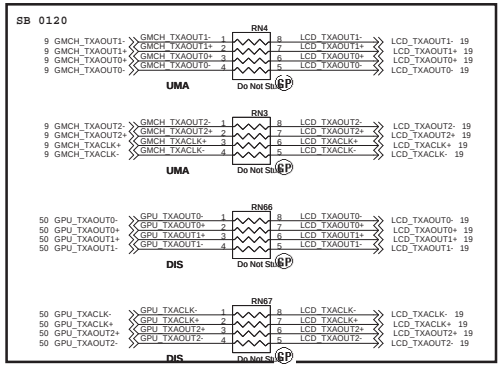
Input (S)	Function
L	B_0 Connected to A
H	B_1 Connected to A

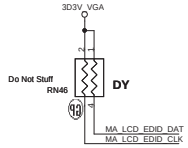
H = HIGH Logic Level L = LOW Logic Level

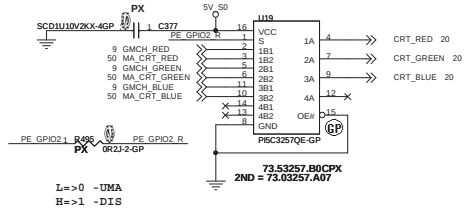


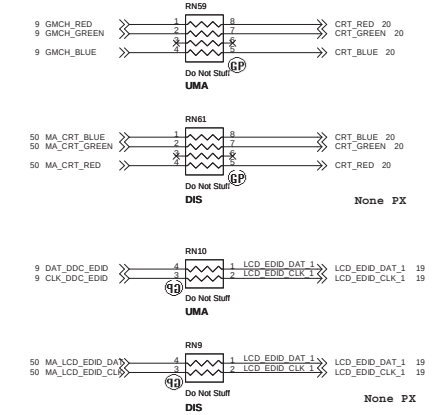


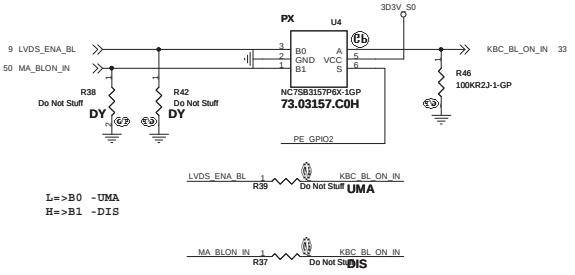


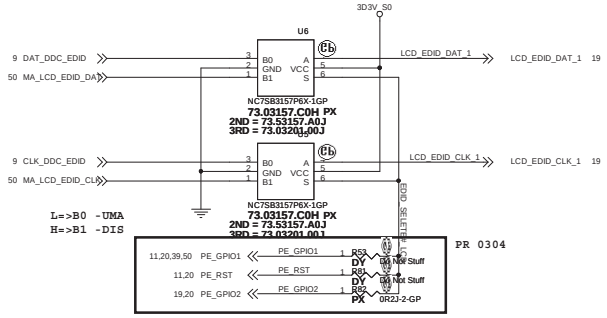












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Title: PX

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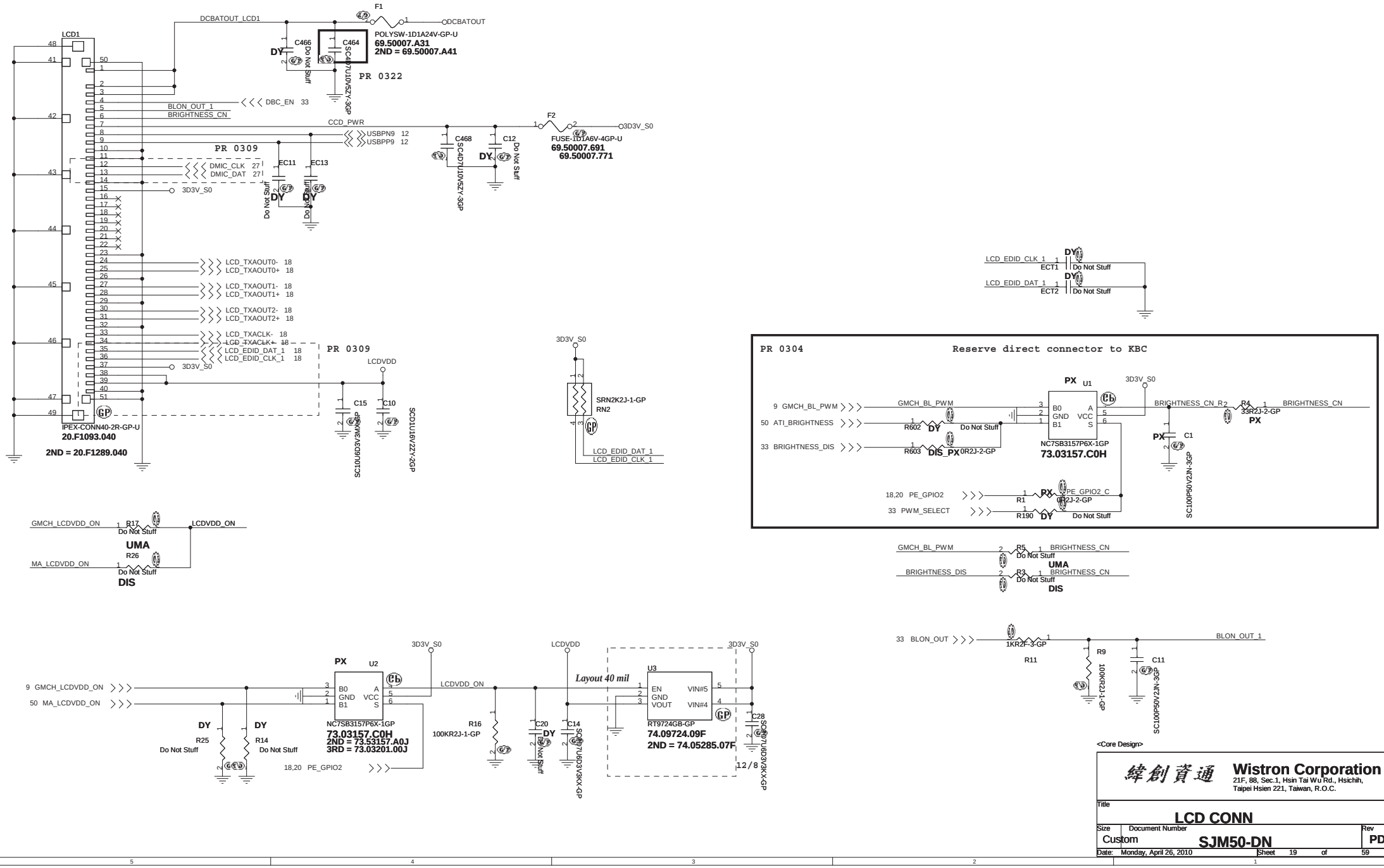
LCD/INVERTER/CCD CONN



<Core Design>

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Title: LCD CONN

Size: Custom | Document Number: SJM50-DN | Rev: PD

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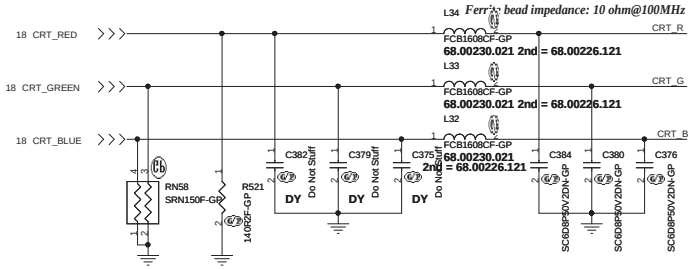
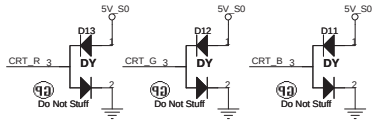
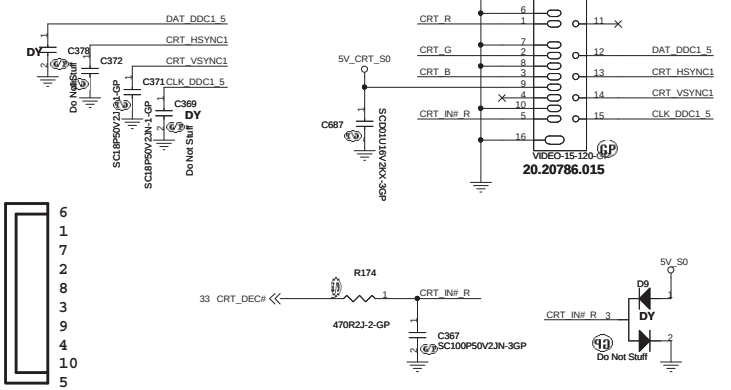
Layout Note:
Place these resistors close to the CRT-out connector



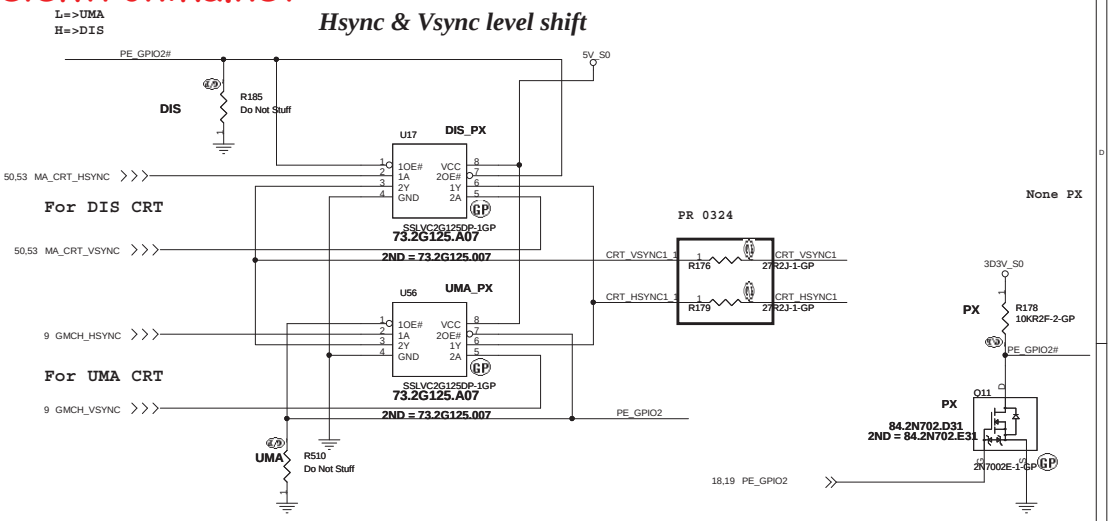


Layout Note:
** Must be a ground return path between this ground and the ground on the VGA connector.*
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

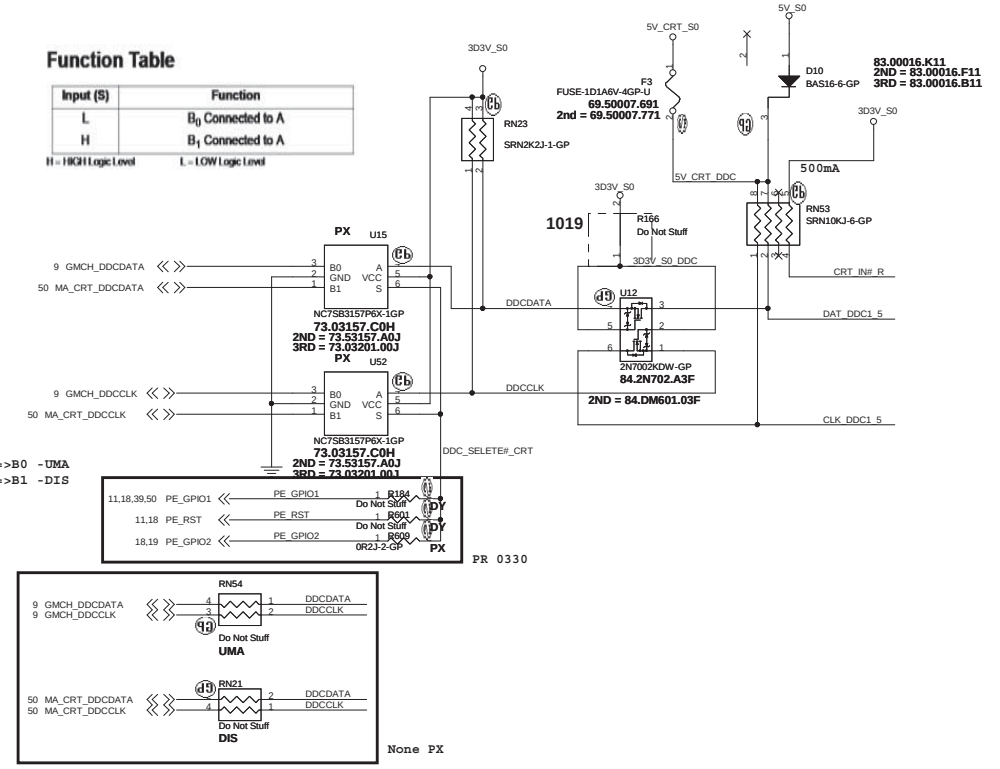
CRT I/F & CONNECTOR



Hsync & Vsync level shift



DDC_CLK & DATA level shift



<Core Design>
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Title: CRT Connector
Size | Document Number: SJM50-DN | Rev: PD
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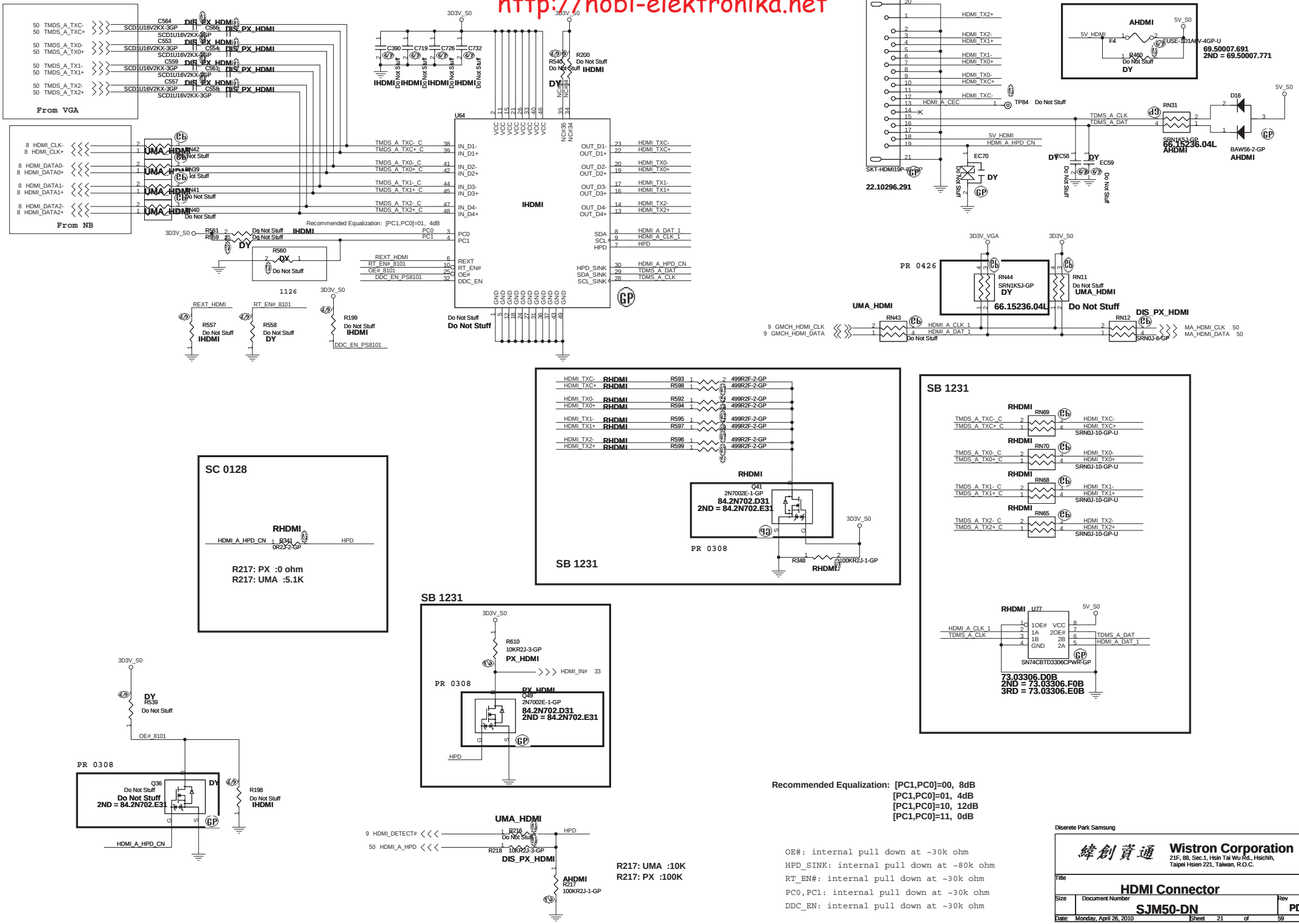

Diserete Park Samsung

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Connector

Size	Document Number	Rev
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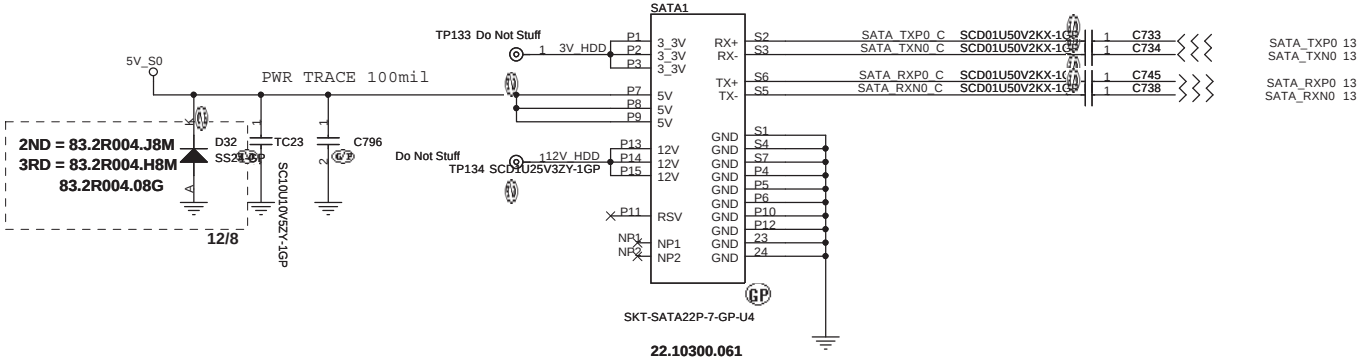
SATA Connector



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title		
HDD		
Size	Document Number	Rev
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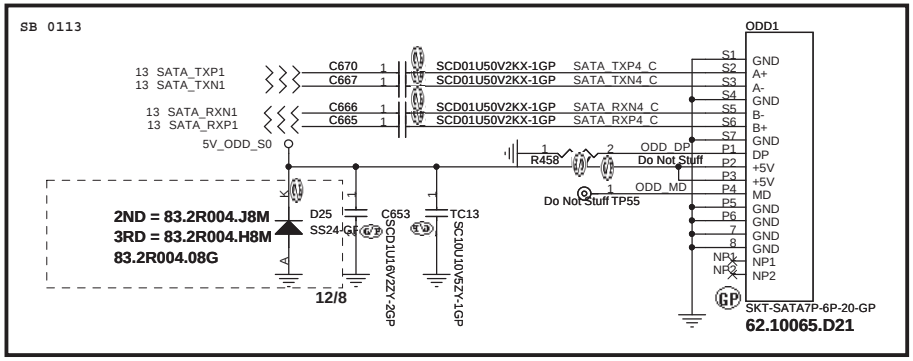
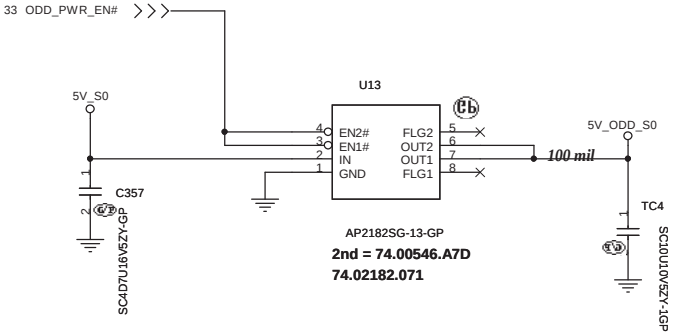
ODD Connector





<Core Design>

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Title		
ODD		
Size	Document Number	Rev
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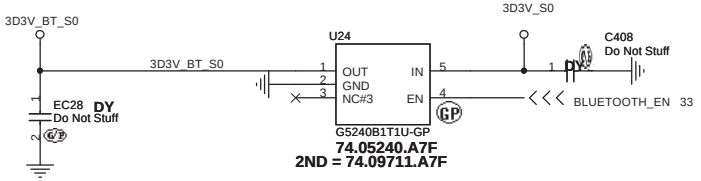
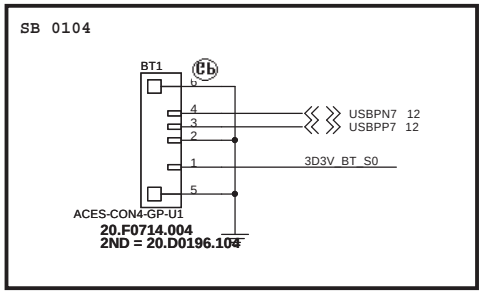
BLUETOOTH MODULE

1.5A / High Active Voltage 2V



EC21 put near BLUE1 / all USB put one choke near connector by EMI request



Pin 1 ->right side
20.D0197.104 Pin1 -> left side
change net sequence
can use JV50-CP Cable

Eiger

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Title: BLUETOOTH		
Size	Document Number: SJM50-DN	Rev: PD
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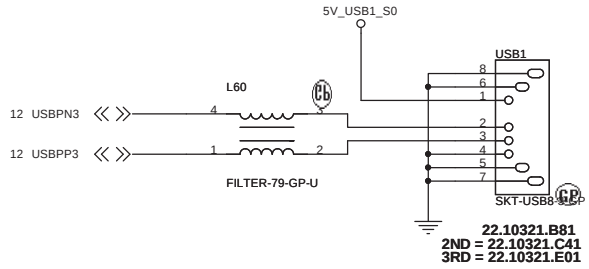

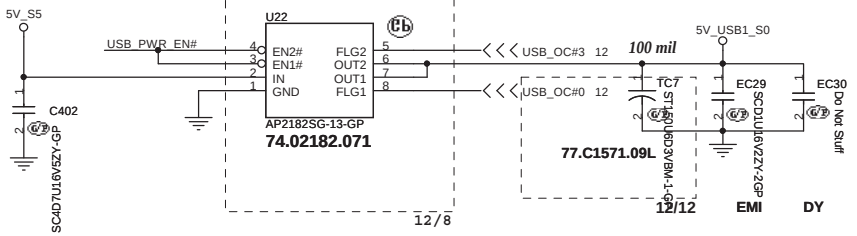

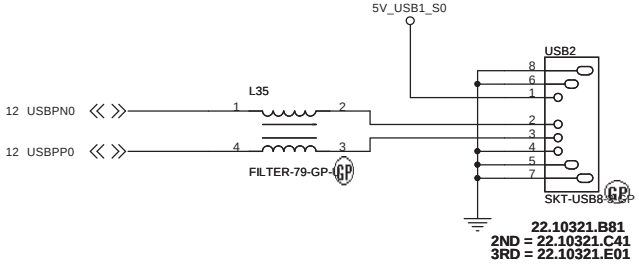

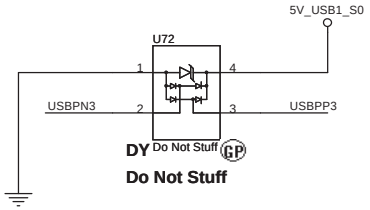

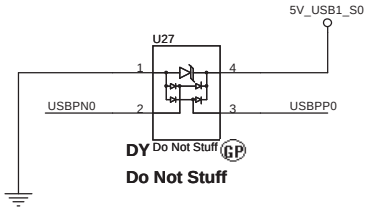

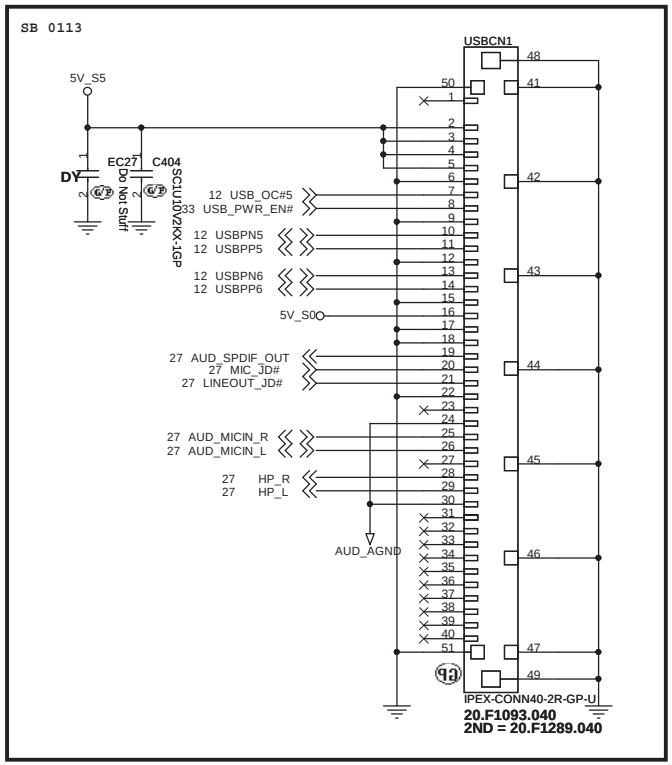

Eiger

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Taipei Hsien 221, Taiwan, R.O.C.

Title	USB	
Size	Document Number: SJM50-DN	Rev: PD
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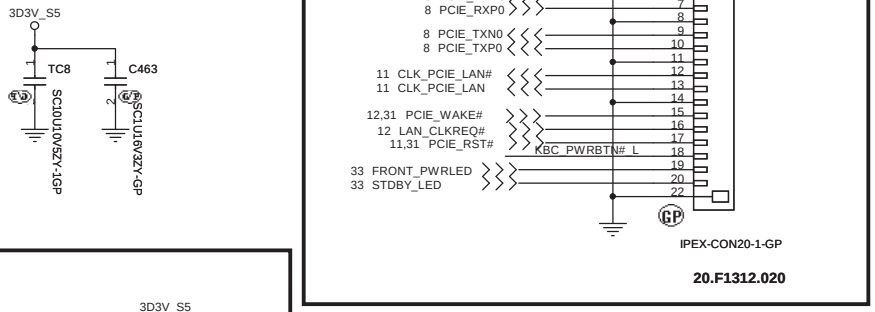

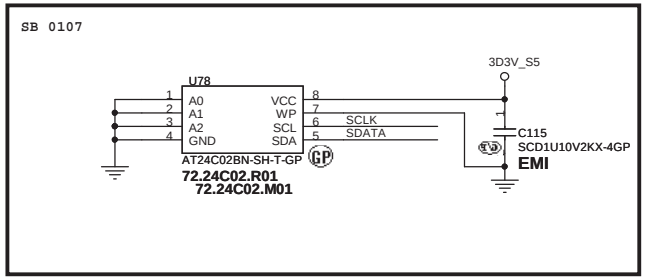

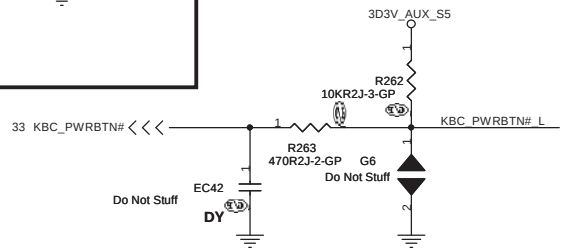

JV50

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Title: ***LAN CONN***

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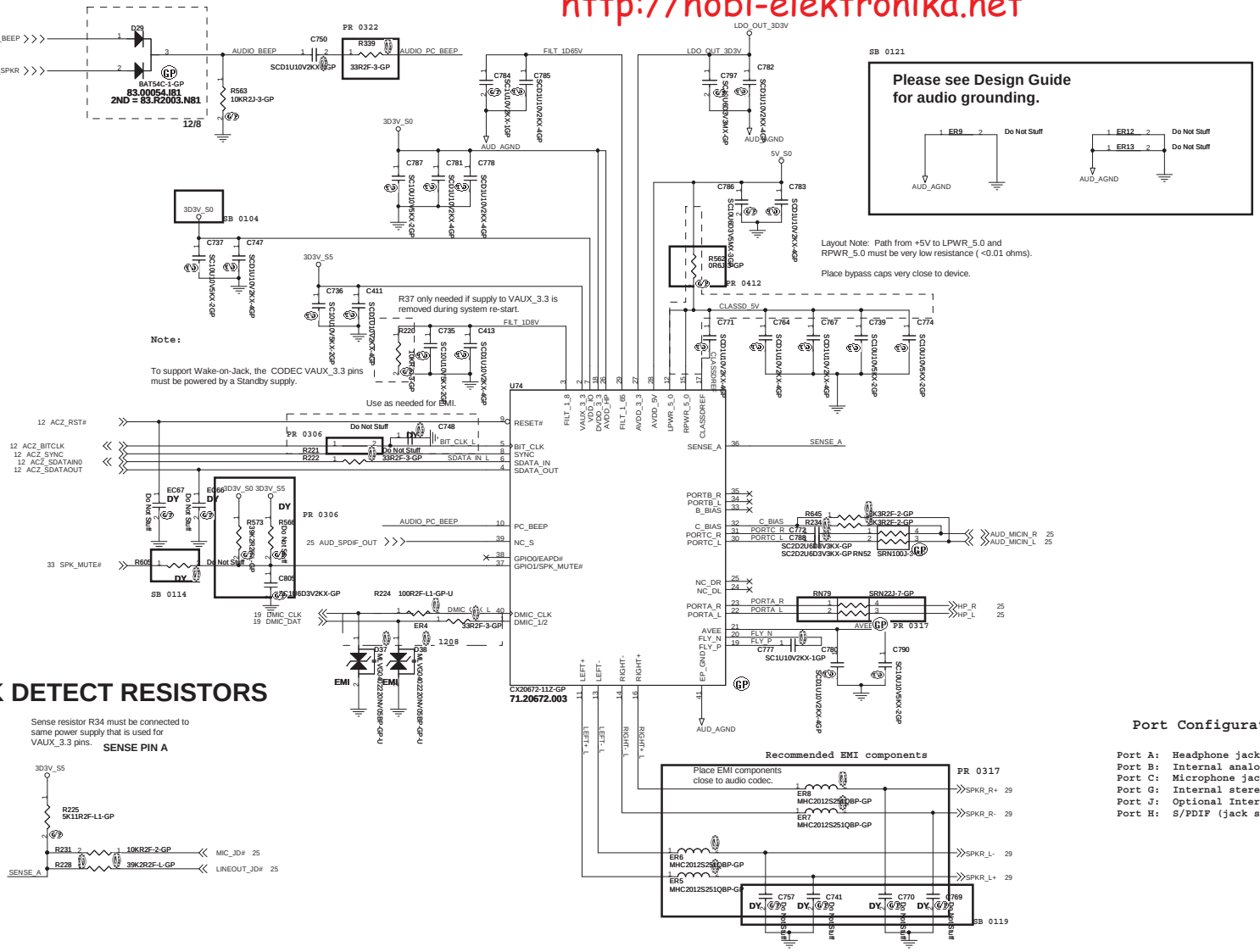

AUDIO OP AMPLIFIER

Eiger

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Title: AUDIO AMP		
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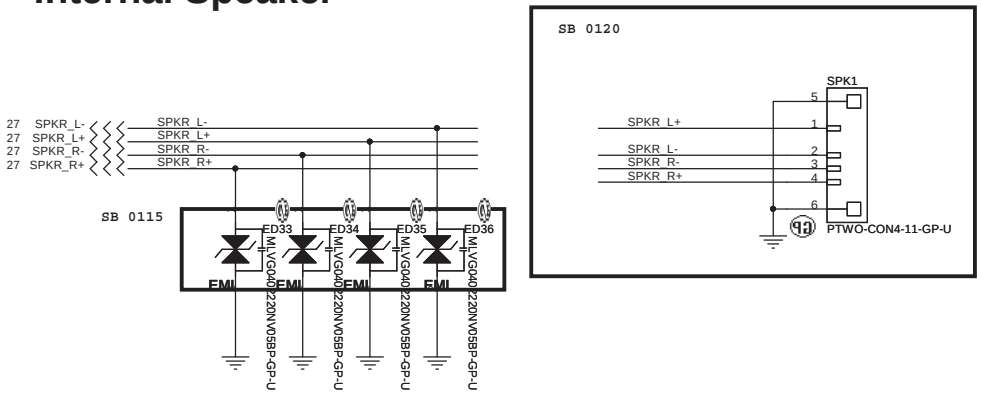
Internal Speaker



Eiger

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Title: **AUDIO JACK**		
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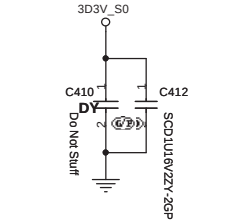
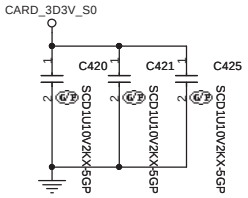
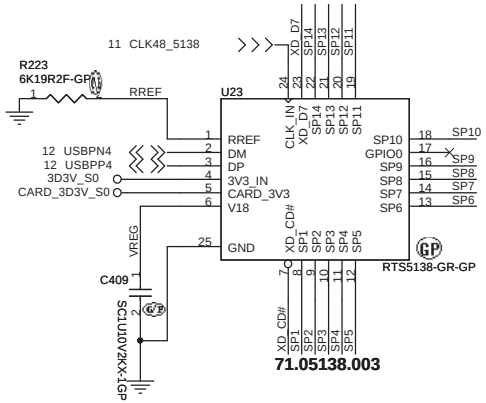
5 IN1 CARD-READER





C51,C52,C53 near CARD1 pin23, Pin14, Pin33



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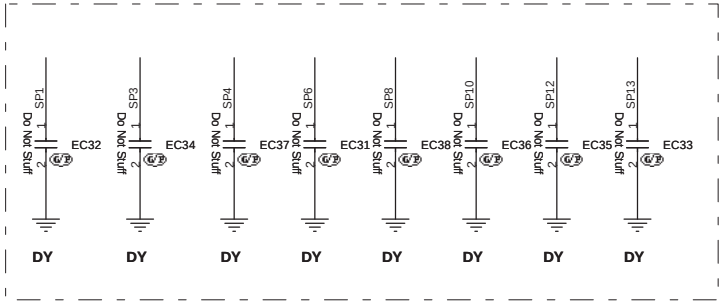

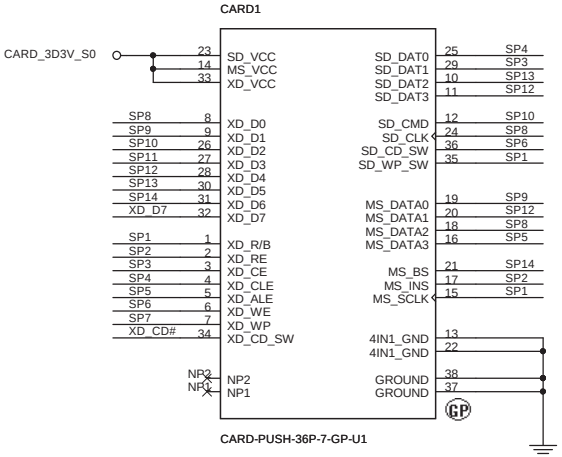

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MORAR3

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CARDREADER		
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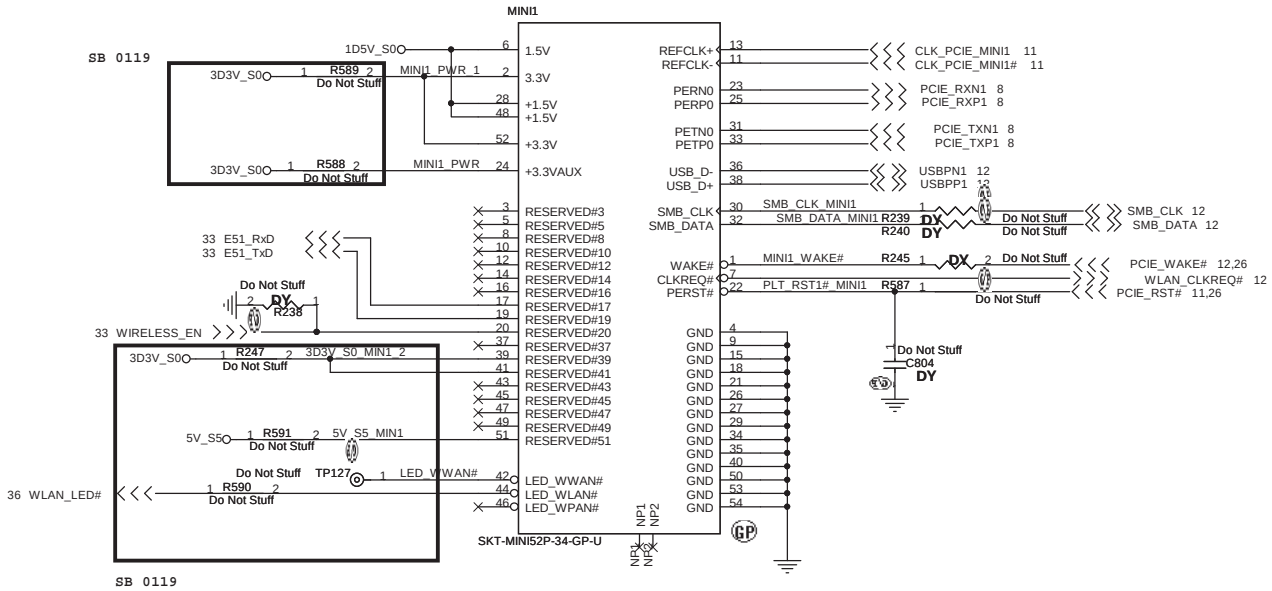
Mini Card Connector(WLAN)
Support debug-card



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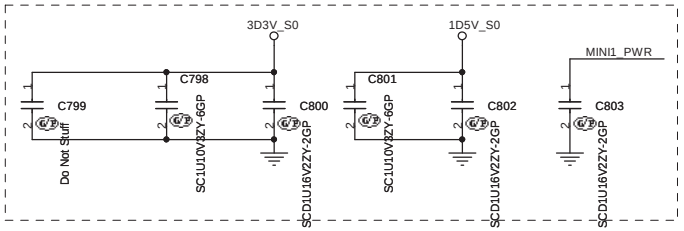
Place near MINI1



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Eiger

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Title: **MINI CARD**

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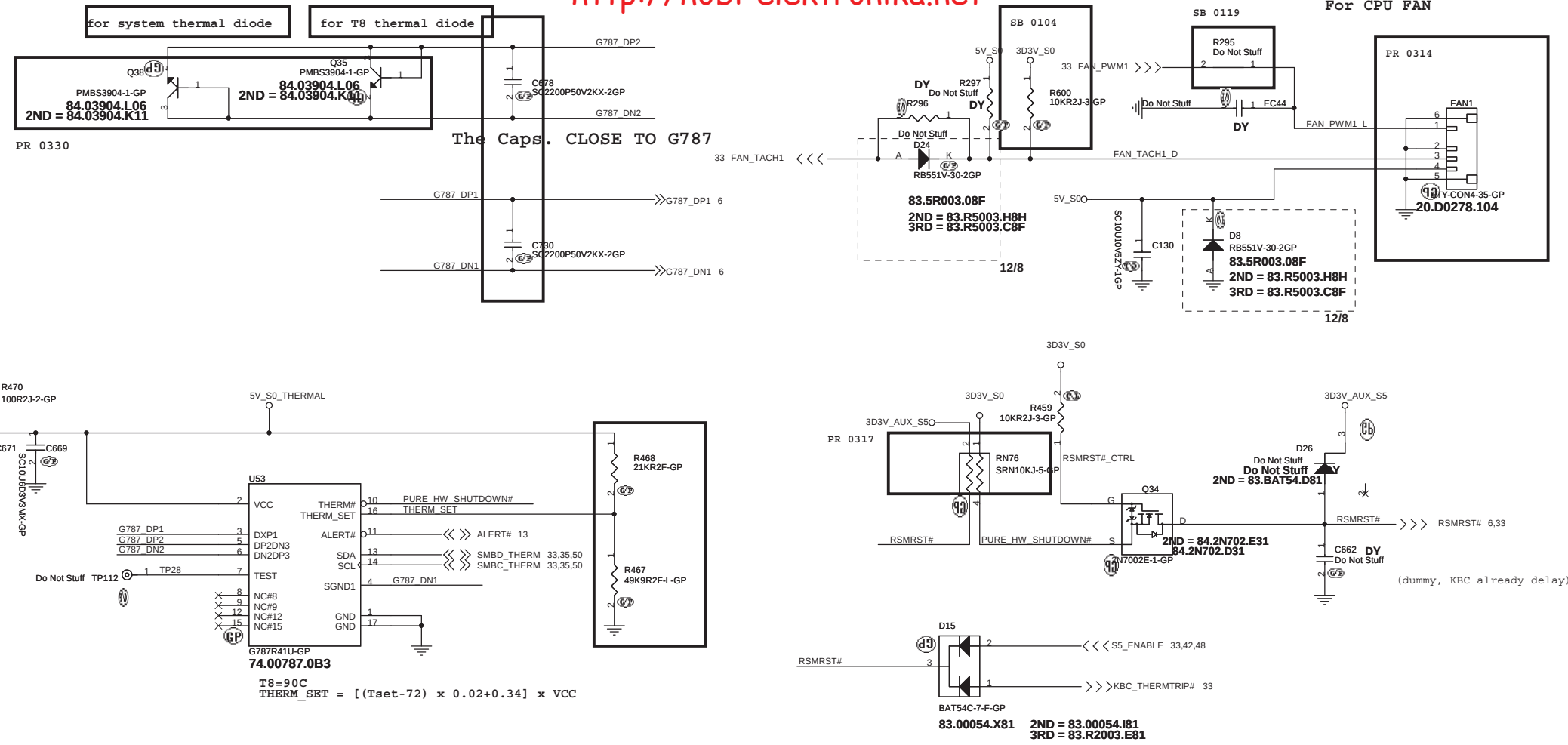

Diserete Madison Samsung

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Title	G792	
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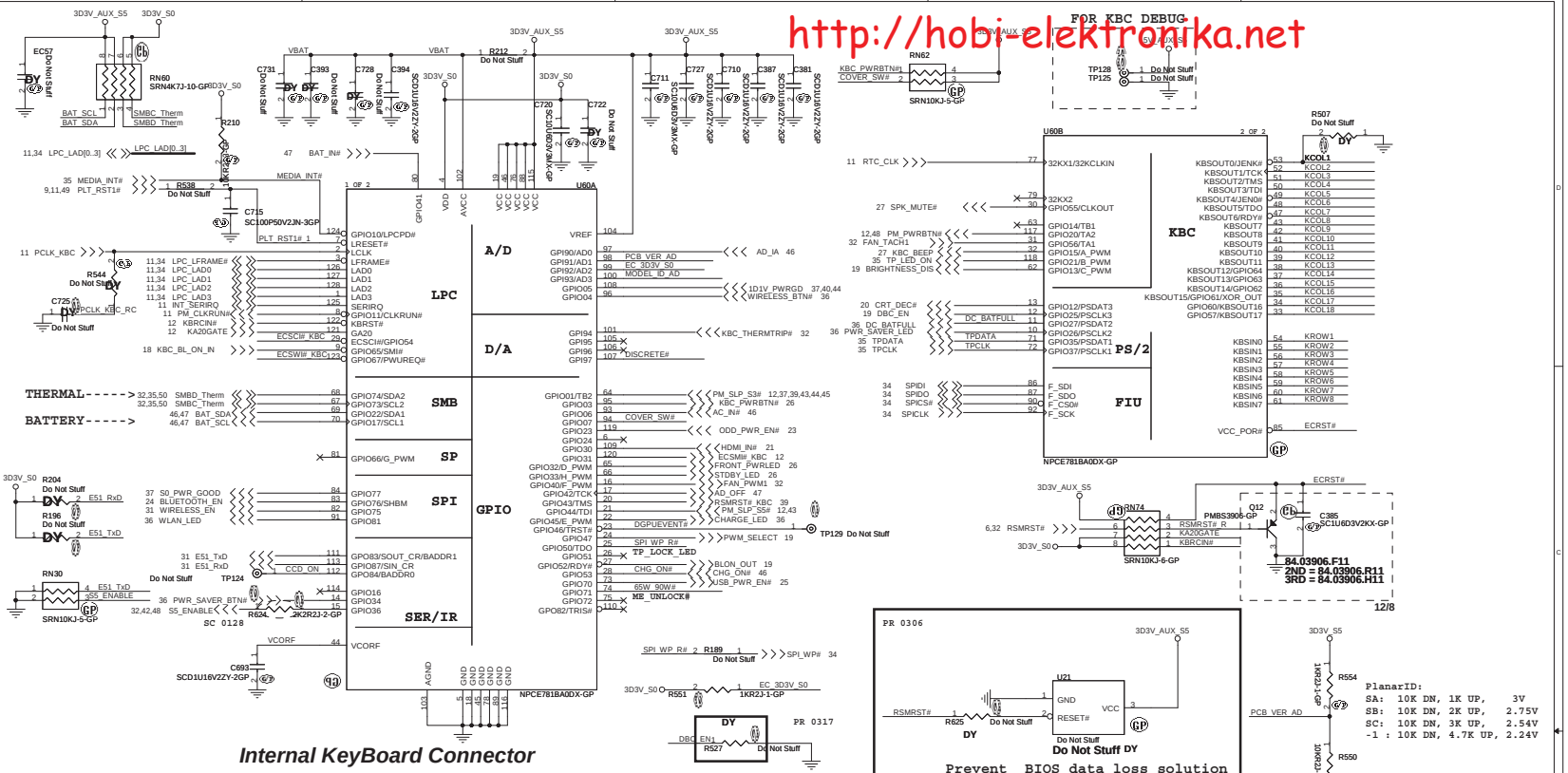
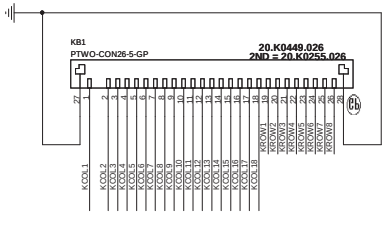


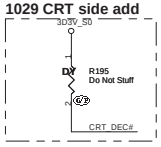
Internal KeyBoard Connector

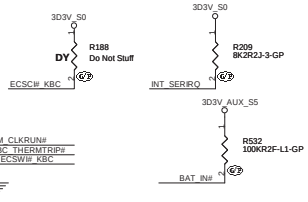


MB PIN DEFINE 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
KB PIN DEFINE 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1

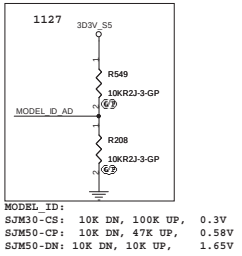
26 K/B 1

1029 CRT side add

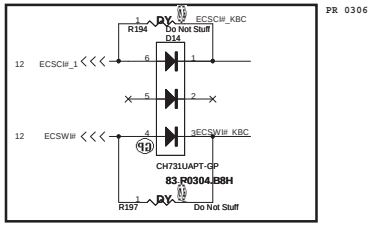




RSMRST#_KBC(P44) --> Pull low 100K

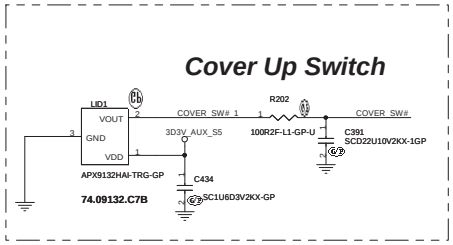


MODEL_ID:
SJM30-CS: 10K DN, 100K UP, 0.3V
SJM50-CP: 10K DN, 47K UP, 0.58V
SJM50-DN: 10K DN, 10K UP, 1.65V



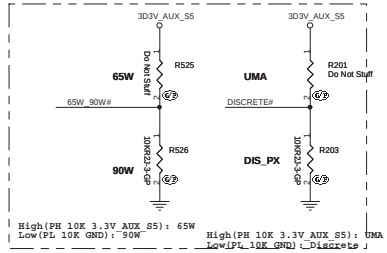
PlanarID:
SA: 10K DN, 1K UP, 3V
SB: 10K DN, 2K UP, 2.75V
SC: 10K DN, 3K UP, 2.54V
-1 : 10K DN, 4.7K UP, 2.24V

Cover Up Switch



Pull-High Resistor (3D3V_AUX_S5)	Voltage
1.0 K	3.0 V
2.0 K	2.75 V
3.0 K	2.54 V
4.7 K	2.24 V
6.98 K	1.94 V
8.2 K	1.81 V
10.0 K	1.65 V

1019



High(PH 10K 3.3V_AUX_S5): 65W
Low(PL 10K GND): 90W

High(PH 10K 3.3V_AUX_S5): UMA
Low(PL 10K GND): Discrete

<Core Design>

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Title: KBC NPCE781B
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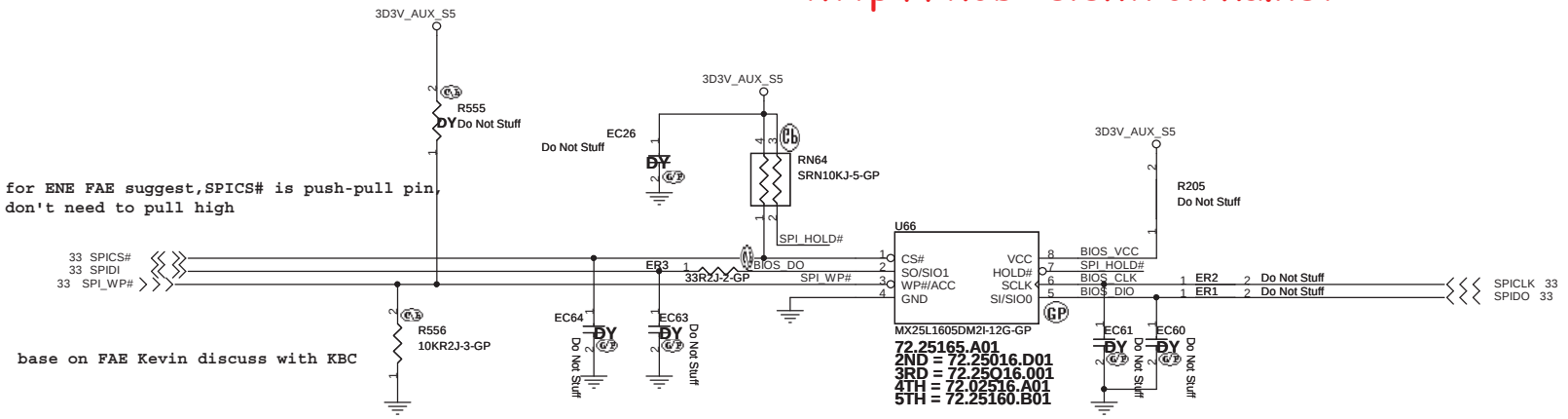
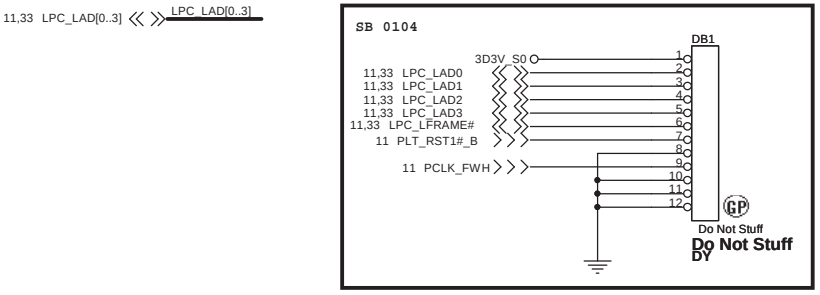


16M Bits

SPI FLASH ROM

GOLDEN FINGER FOR DEBUG BOARD



<Core Design>

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Title		
BIOS		
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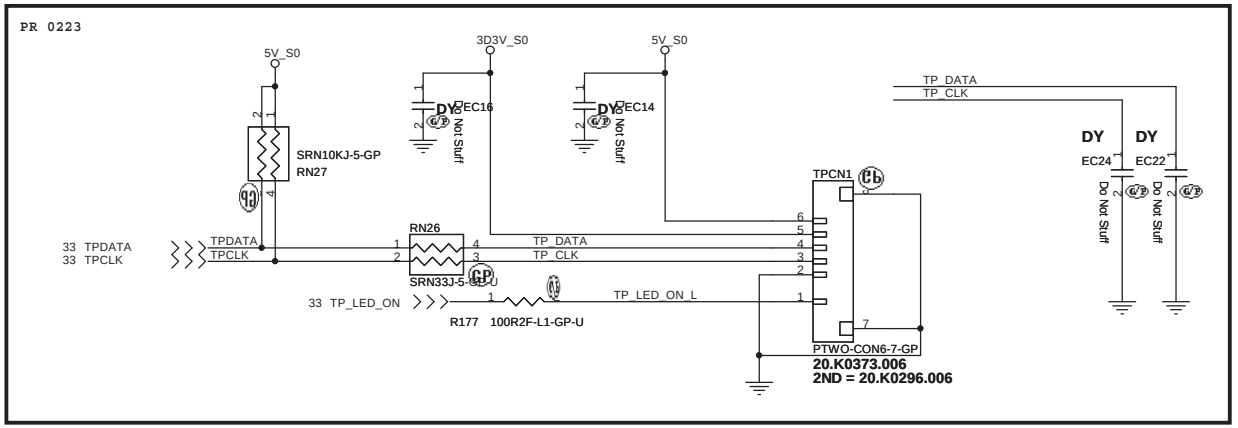

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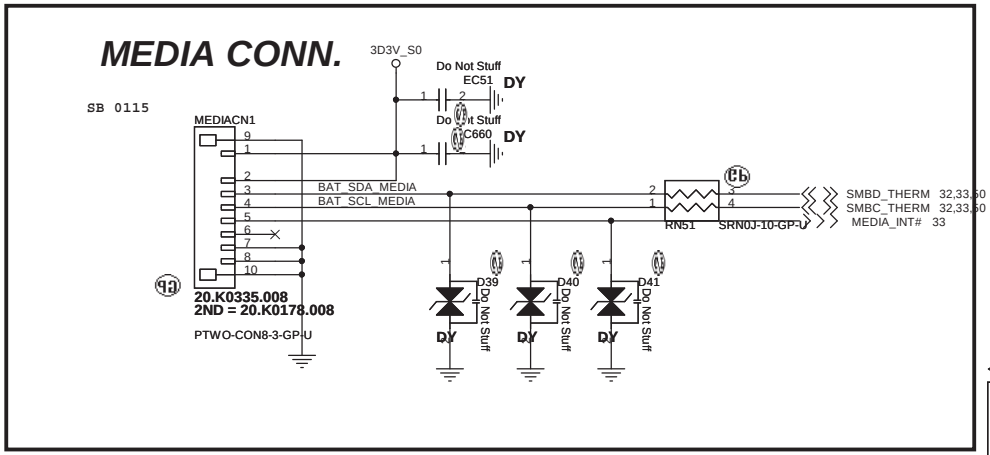
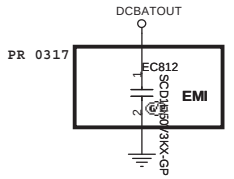
T/P



Near component MEDIACN1



<Core Design>

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Title	Touch PAD	
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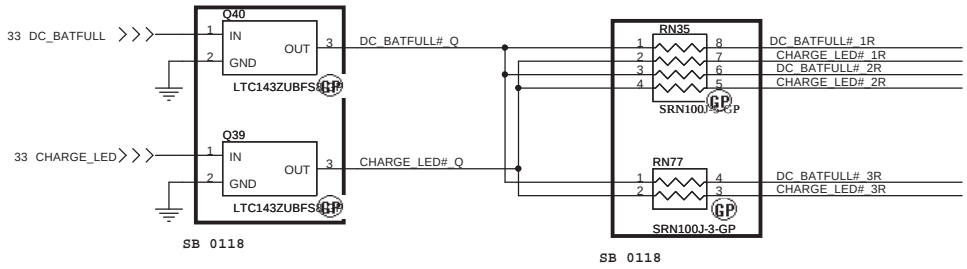
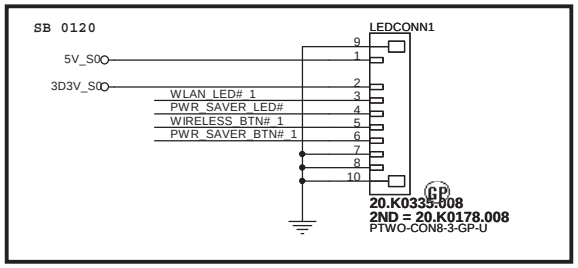
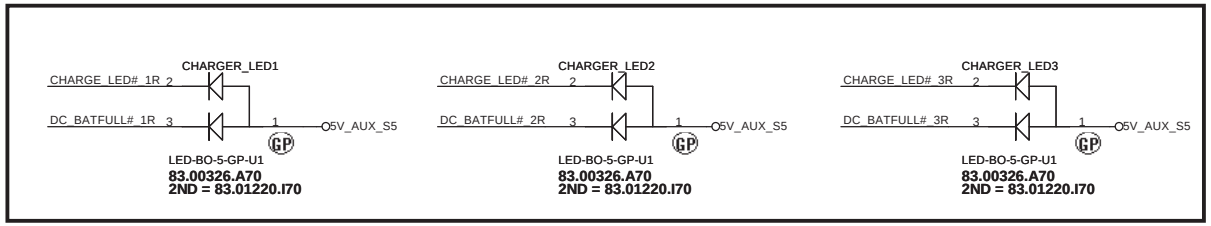
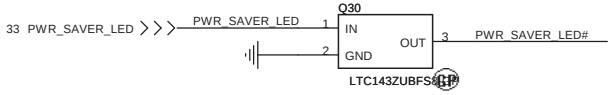
Charger LED

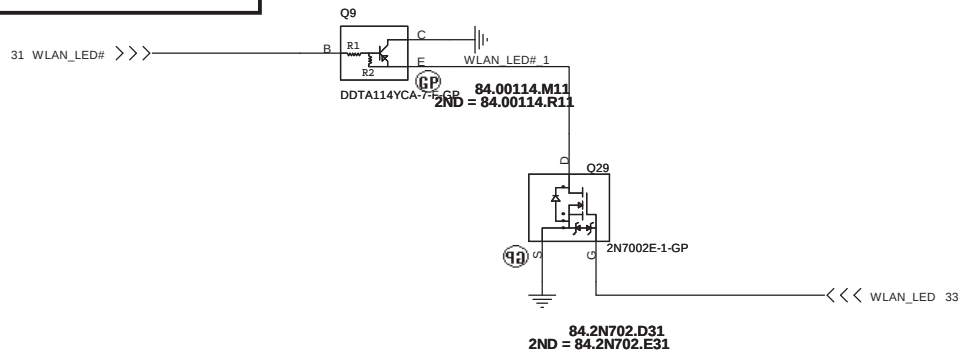


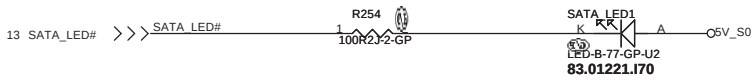


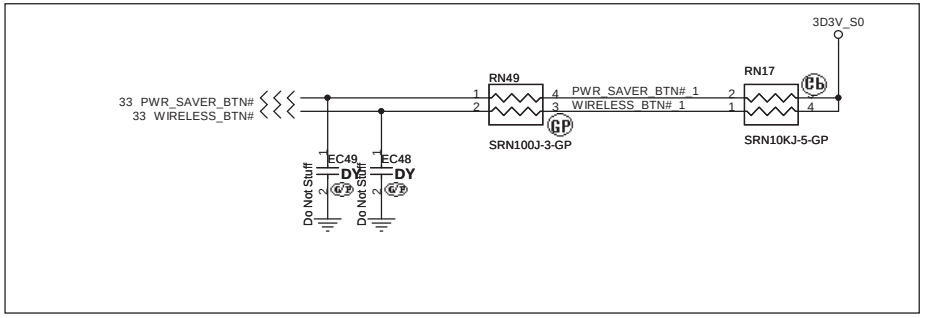
SB 0119

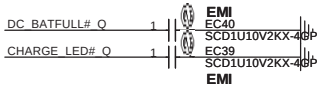












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Title: LED		
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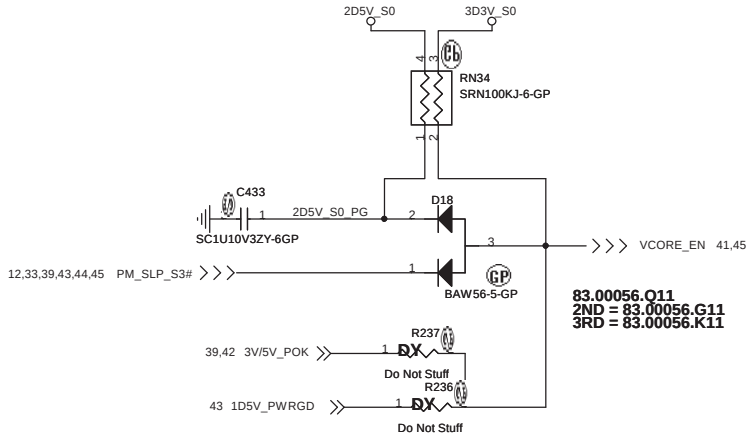
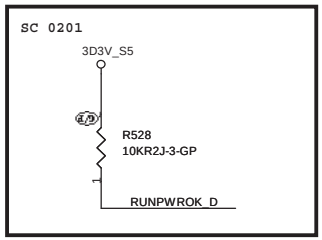
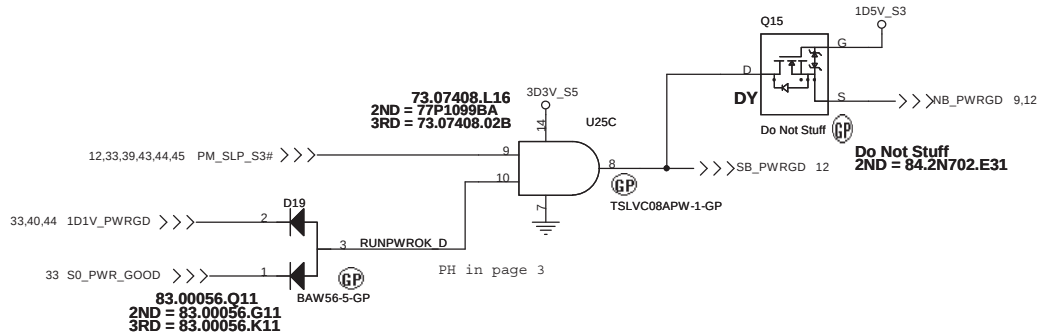


1D5V_S3_PWRGD

P/H @ 1D8V_S3 PAGE





<Core Design>

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Title: **POWER ON LOGIC**

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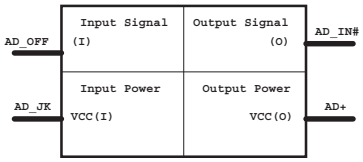
Adapter



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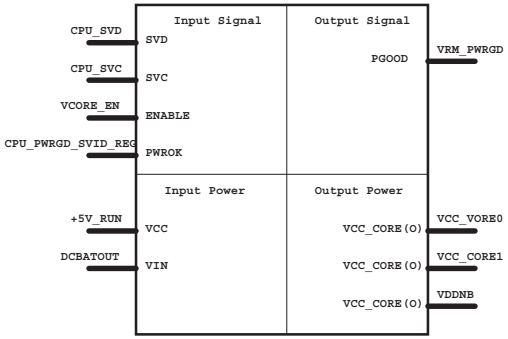
ISL6265HRTZ



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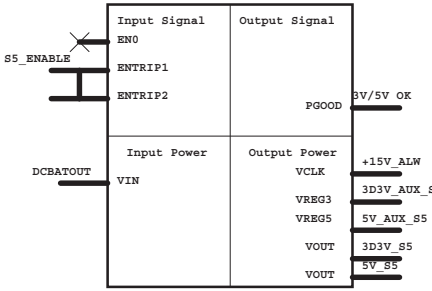
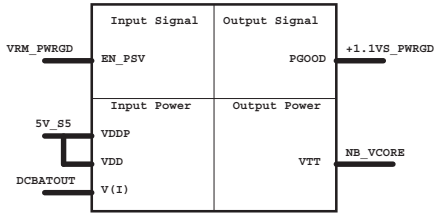


DCDC NB_VCORE (RT8208)



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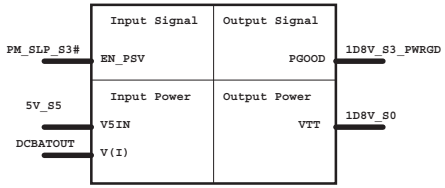

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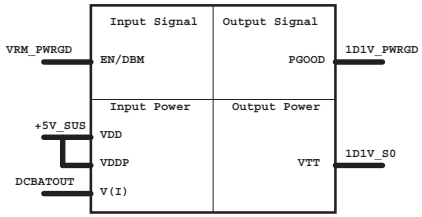
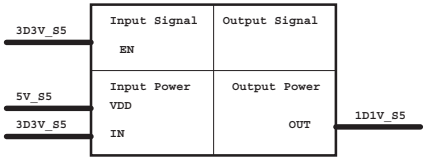
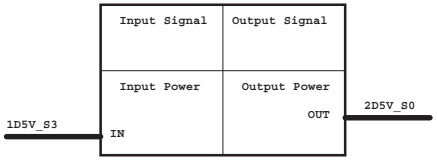


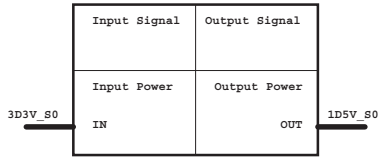
1D1V_S5 LDO RT9025



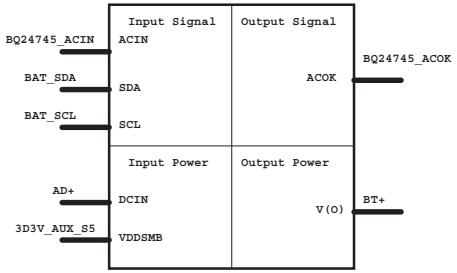
1V_VGA LDO R9025



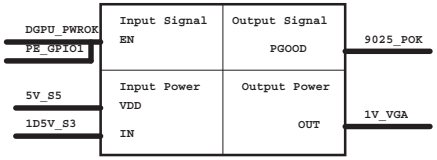
1D5V LDO G9571



CHARGER BQ24745



1V_VGA LDO RT9025



<Core Design>

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Title: Power Block Diagram

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Run Power

Aux Power

3D3V_AUX_S5

I min = 150 mA

2nd source:74.09198.G7F

PR 0308

PR 0309

PR 0306

SB 0119

SB For 2KV ESD protect

SB 0114

+3VS to 3.3V_DELAY Transfer

3D3V_VGA discharge CKT

Please closed U77 for Park issue

Diserete Madison Samsung

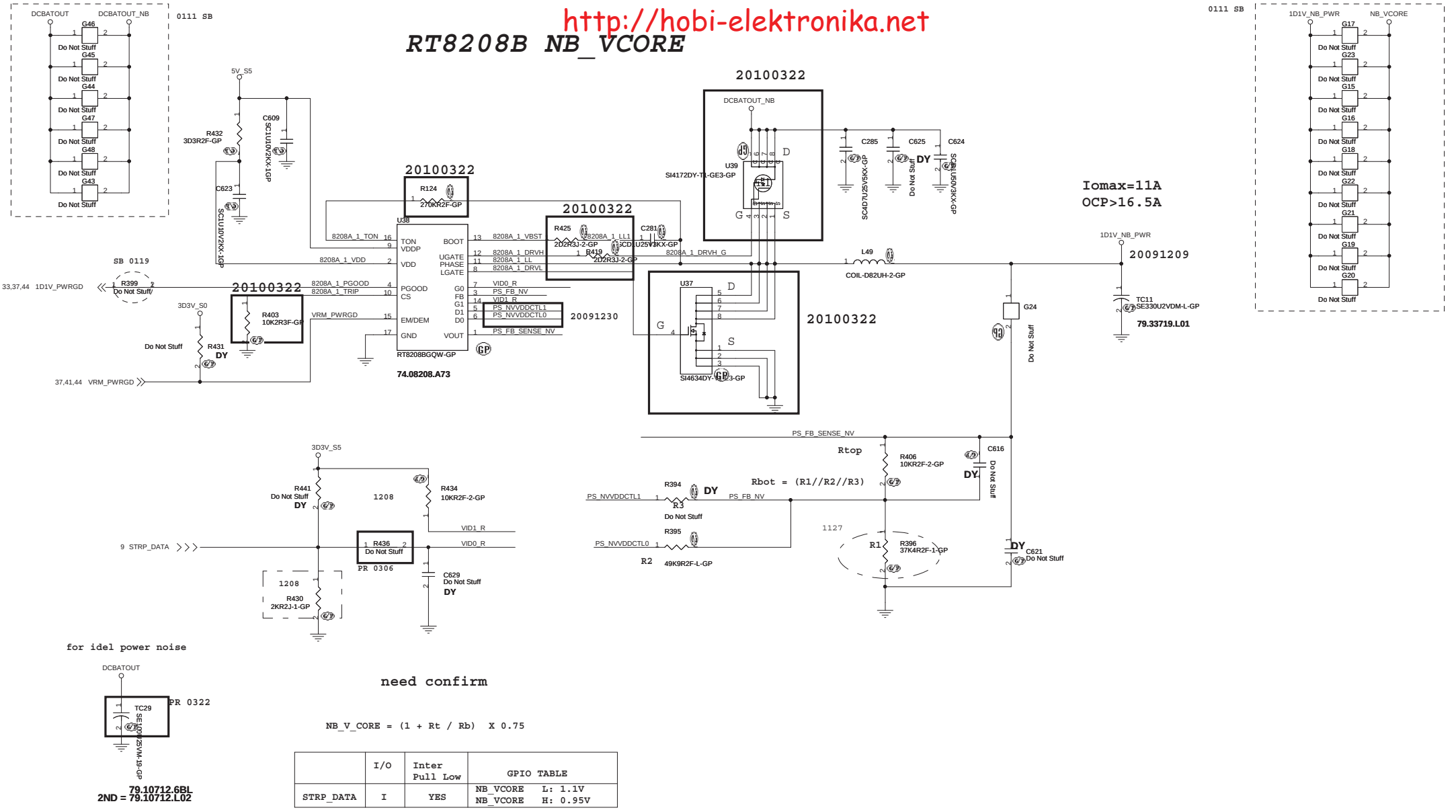
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RUN AND AUX POWER

Size: Custom | Document Number: SJM50-DN | Rev: PD

Date: Monday, April 26, 2010 | Sheet 39 of 59

RT8208B NB_VCORE



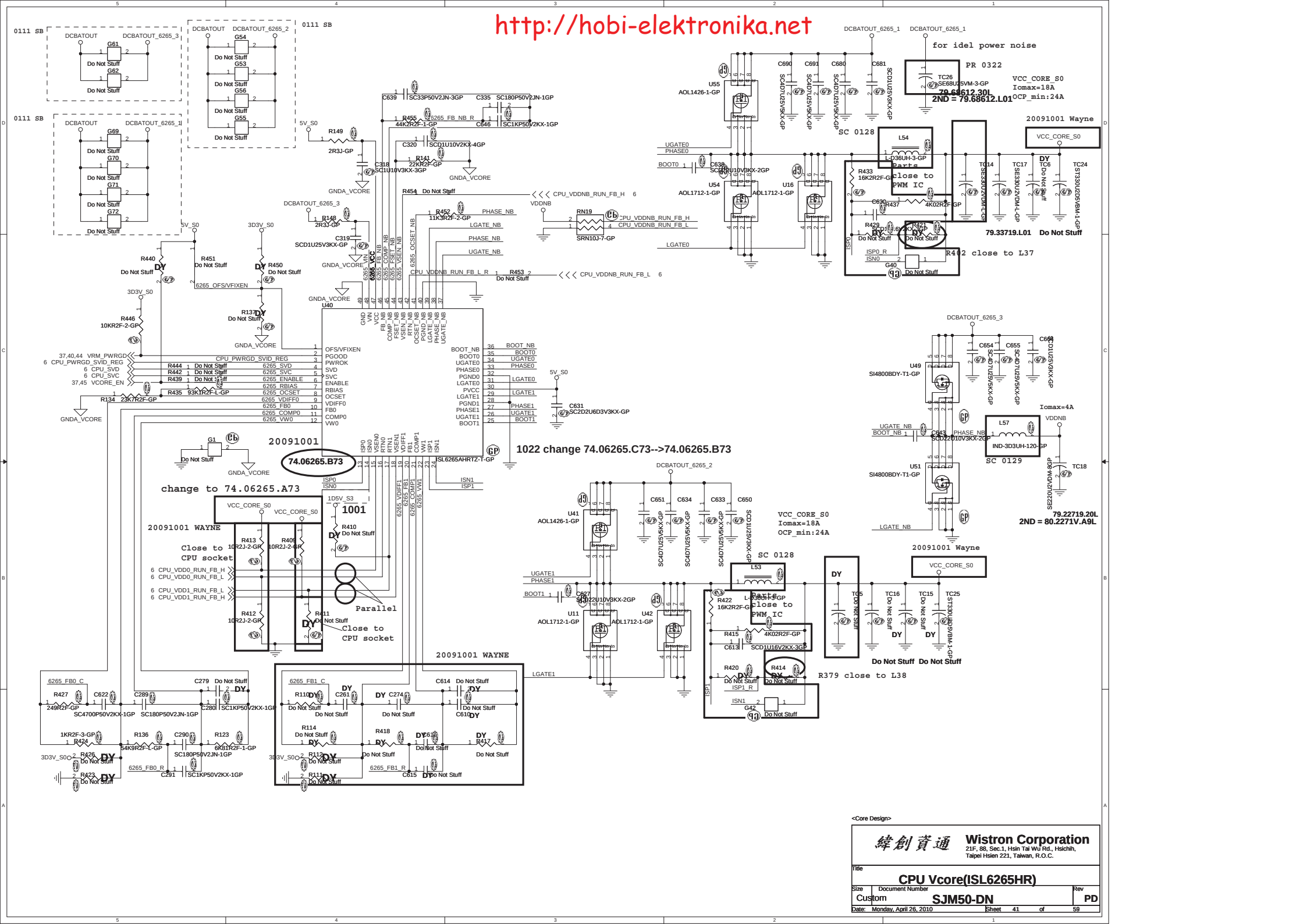
	I/O	Inter Pull Low	GPIO TABLE
STRP_DATA	I	YES	NB_VCORE L: 1.1V NB_VCORE H: 0.95V

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8208B_NB_VCORE

Size	Document Number	Rev
Custom	SJM50-DN	PD

Date: Monday, April 26, 2010 Sheet 40 of 59



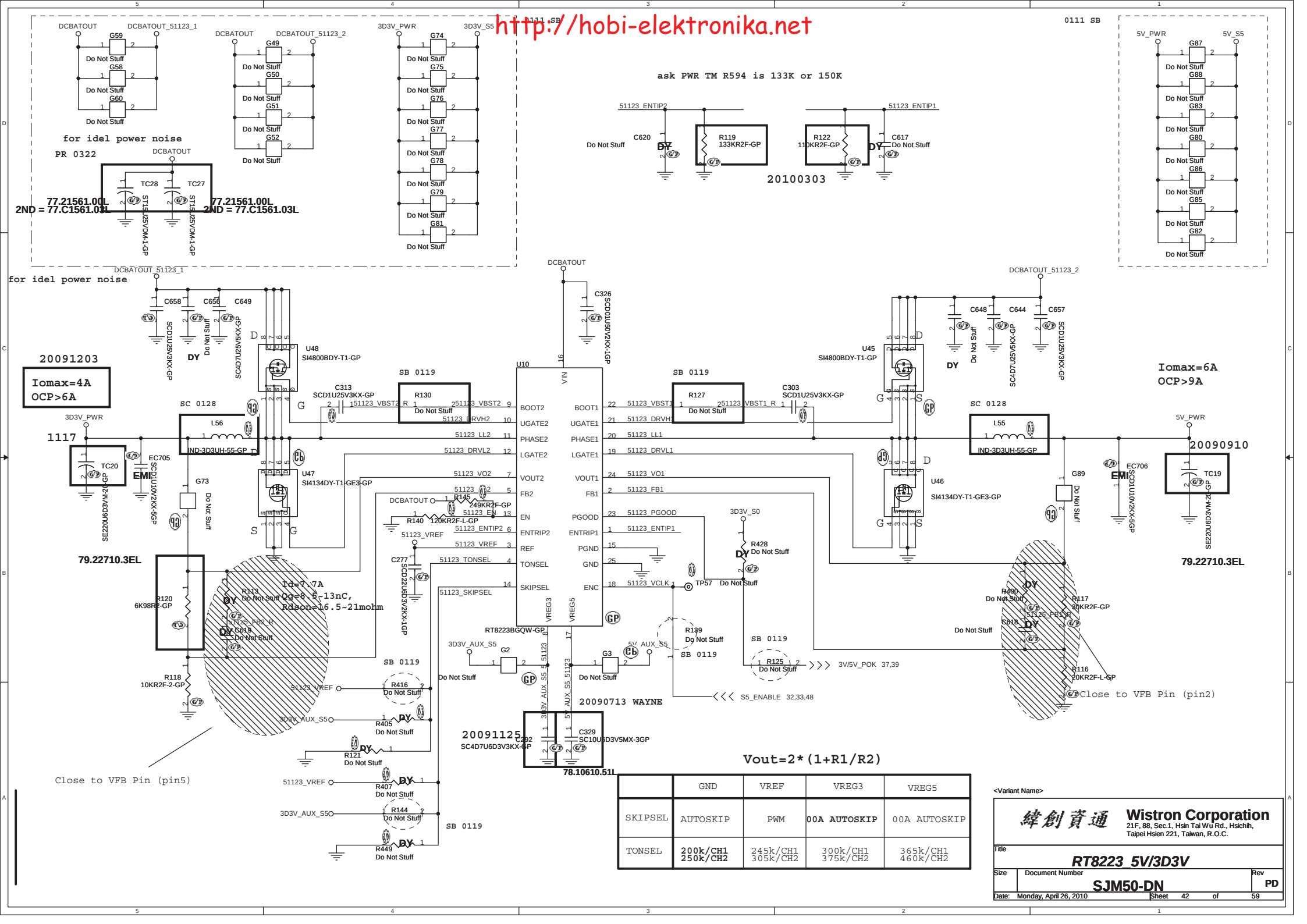
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU Vcore(ISL6265HR)

Size	Document Number	Rev
Custom	SJM50-DN	PD

Date: Monday, April 26, 2010 Sheet 41 of 59



	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	**00A AUTOSKIP**	00A AUTOSKIP
TONSEL	**200k/CH1 250k/CH2**	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

<Variant Name>

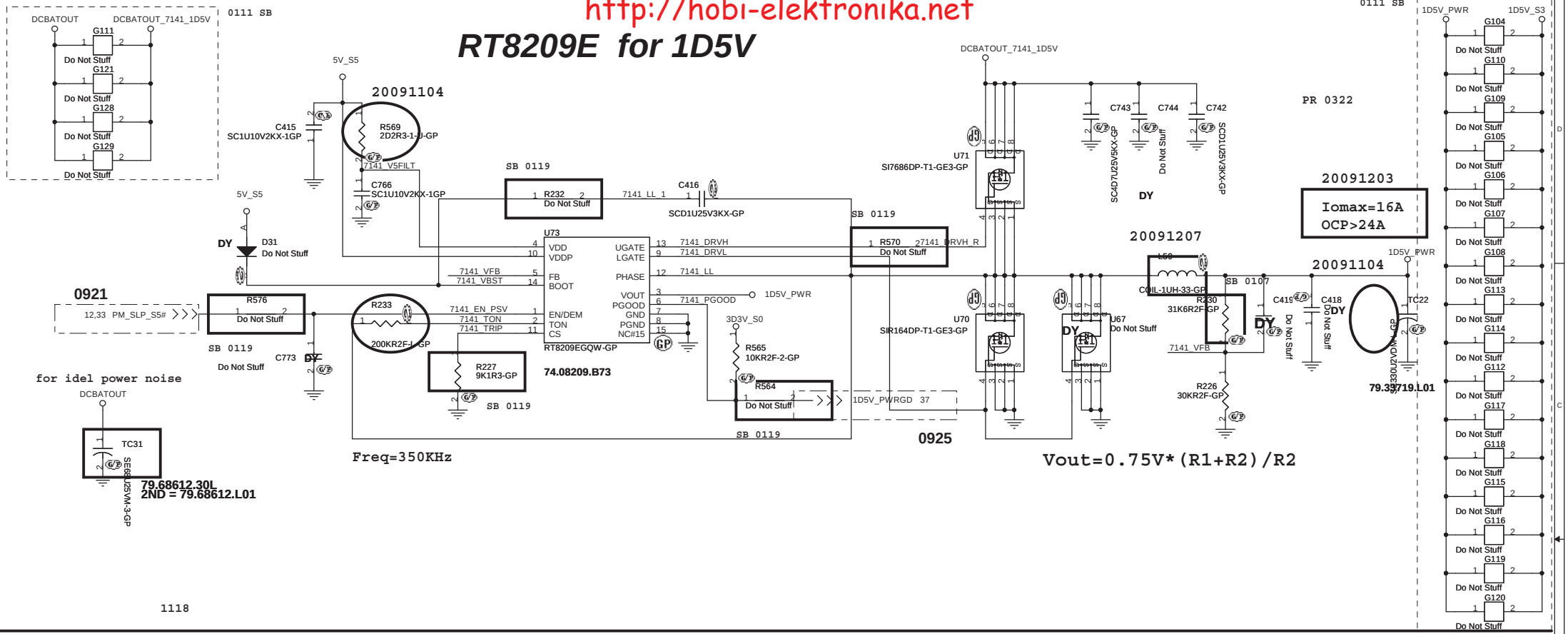
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

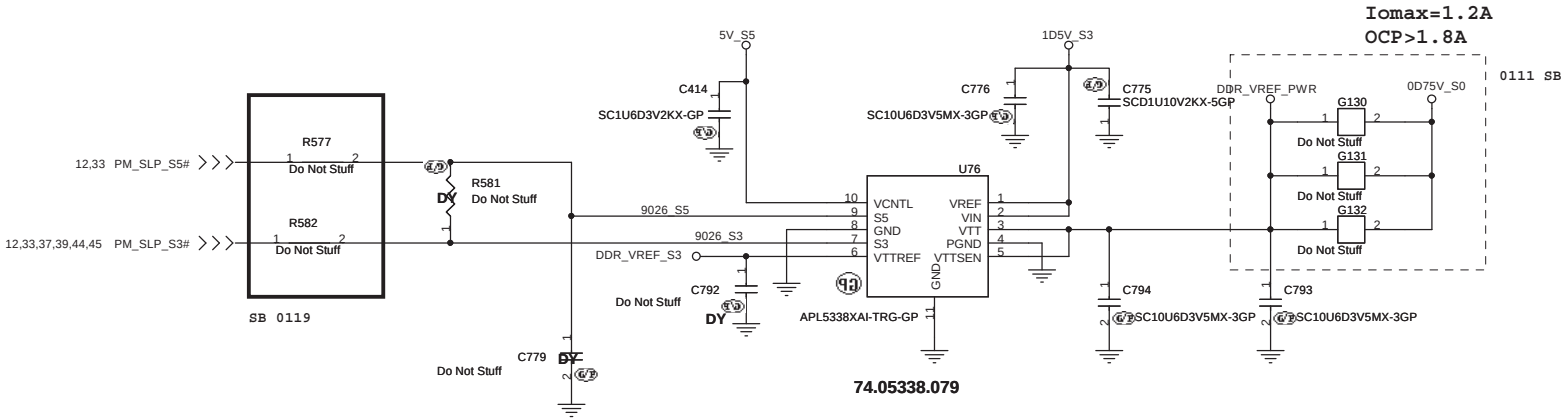
Title: ***RT8223_5V/3D3V***

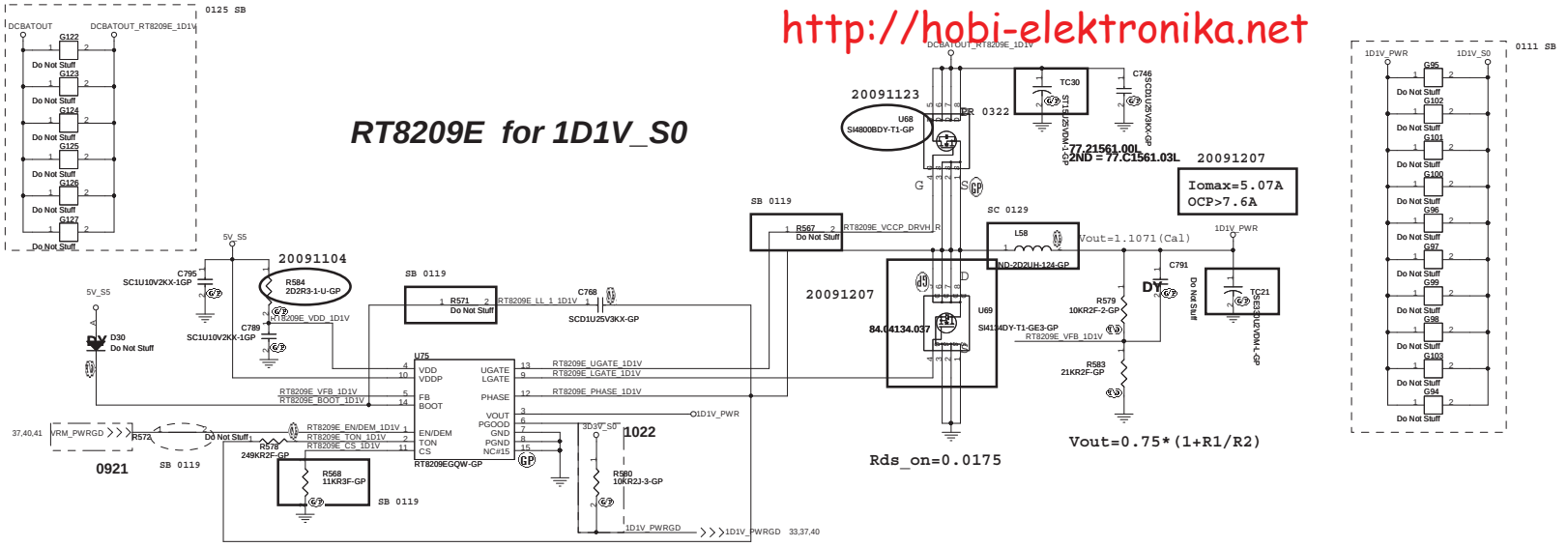
Size | Document Number: **SJM50-DN** | Rev: PD

Date: Monday, April 26, 2010 | Sheet 42 of 59

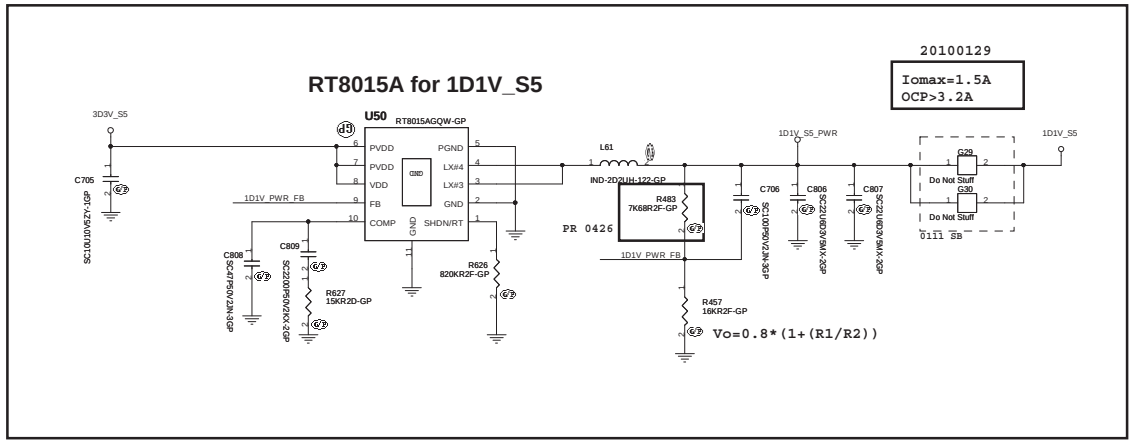
RT8209E for 1D5V

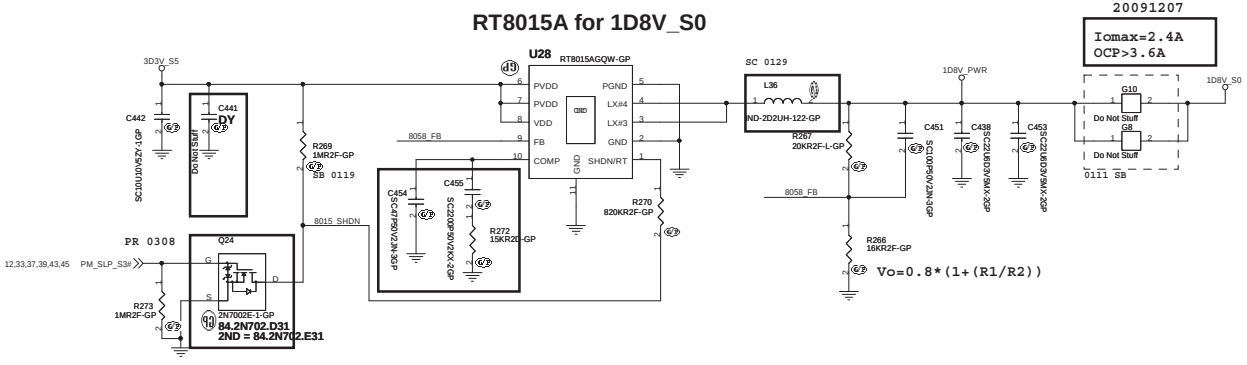






20100308





Diserete Park Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 1D1V_S0 & 1D1V_S5 & 1D8V_S0

Size | Document Number: SJM50-DN | Rev: PD

Date: Monday, April 26, 2010 | Sheet 44 of 59

RT8015A for 1D05V_S0

Iomax=1.75A
OCP>2.625A

U61 RT8015AGQW-GP

3D3V_S5
C685 SC10U10V5ZY-1GP
C684 DY
Do Not Stuff
R487 1MR2F-GP
8015A_SHDN
PVDD PVDD VDD FB COMP PGND LX#4 LX#3 GND SHDN/RT GND
1D05V_FB
C696 SC47P50V2JN-3GP
C701 SC2200P50V2KX-2GP
R498 15KR2D-GP
R497 820KR2F-GP
L63 IND-2D2UH-122-GP
1D05V_PWR
R637 3KR2F-GP
C689 SC100P50V2JN-3GP
C692 SC22U6D3V5MX-2GP
C695 SC22U6D3V5MX-2GP
G90 Do Not Stuff
G91 Do Not Stuff
0111 SB
1D05V_S0
R634 24KR2F-GP
Vo=0.8*(1+(R1/R2))
R636 16KR2F-GP
R632 Do Not Stuff
SB 0119
37,41 VCORE_EN
Q45 2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31
PR 0308
12,33,37,39,43,44 PM_SLP_S3#
R633 DY Do Not Stuff
R496 1MR2F-GP
Q46 2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31
PR 0308
1:VDDR:1.05V(1333MHz)
0:VDDR:0.9V(1066MHz)*default
3D3V_S0
PWR TM 1118
U82 74LVC1G08GW-1-GP
VCC Y GND A B
MEM_1V5 13
1D05V_0D9V_EN 11
CPU_VDDR_EN
R635 Do Not Stuff
CPU_VDDR_EN_R1
R631 Do Not Stuff DY
C818 SC100P50V2JN-3GP

20100308

20091207
Iomax=1.5A

1D5V_S3
5V_S5
C607 SC10U10V5KX-2GP DIS_PX
C603 SC10U16V3KX-2GP DIS_PX
1008
SC 0201
R408 Do Not Stuff
11,58 DGPU_PWROK
9025_EN_R
C628 DY Do Not Stuff
3D3V_VGA
R398 2K2R2J-2-GP DIS_PX
11,39 9025_POK
9025_POK
U36 RT9025-25PSP-GP 74.09025.03D
VDD VIN EN PGOOD GND NC#5 VOUT ADJ GND
9025_FB
R349 5K36R2F-GP DIS_PX
C595 SC100P50V2JN-3GP DIS_PX
R346 20KR2F-L-GP DIS_PX
C597 SC10U6D3V5KX-2GP DIS_PX
C592 DY Do Not Stuff
1V_VGA_PWR
G14 Do Not Stuff
G13 Do Not Stuff
1V_VGA
Vo=0.8*(1+(R1/R2))

20091207
2D5V
Iomax=0.25A

U59 RT9161-A-25PG-GP 74.09161.F3C
VOUT VIN GND
3D3V_S0
2D5V_LDO
C700 SC1U10V2ZY-6GP
C702 SC22U6D3V5MX-2GP
G84 Do Not Stuff
2D5V_S0

Diserete Park Samsung
Place near to CPU

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LDO 1D05V/2D5V/1V
Size: A3
Document Number: SJM50-DN
Rev: PD
Date: Monday, April 26, 2010
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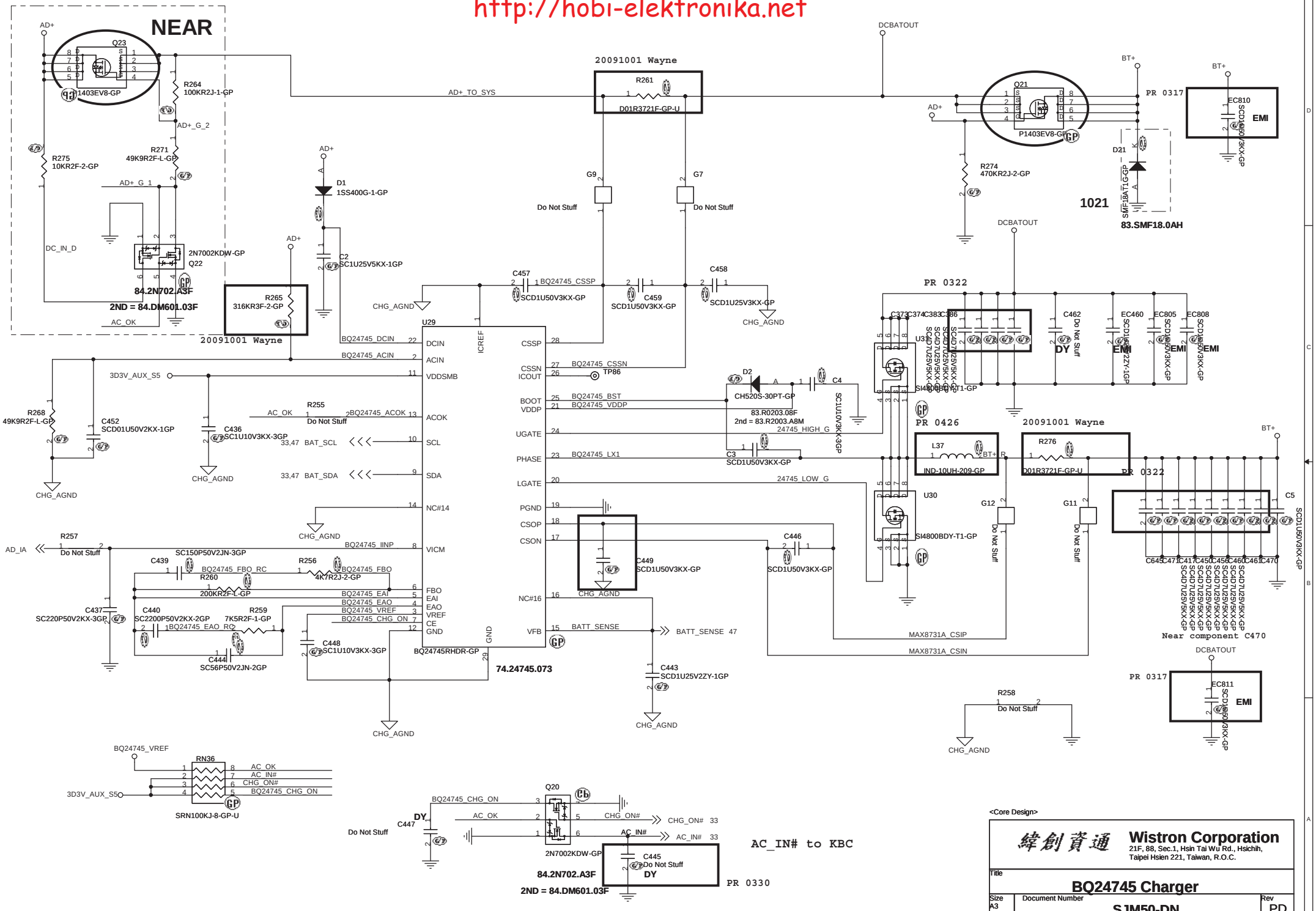


<Core Design>

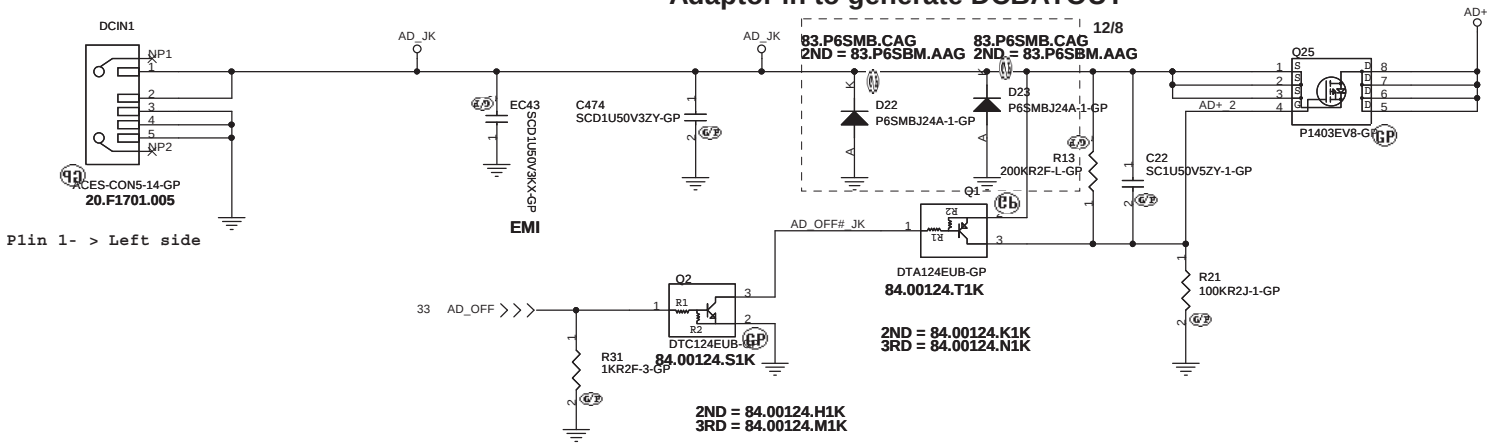
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

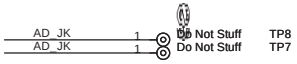
Title: BQ24745 Charger

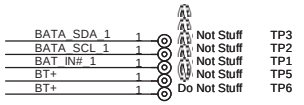
Size: A3 | Document Number: SJM50-DN | Rev: PD

Date: Monday, April 26, 2010 | Sheet 46 of 59

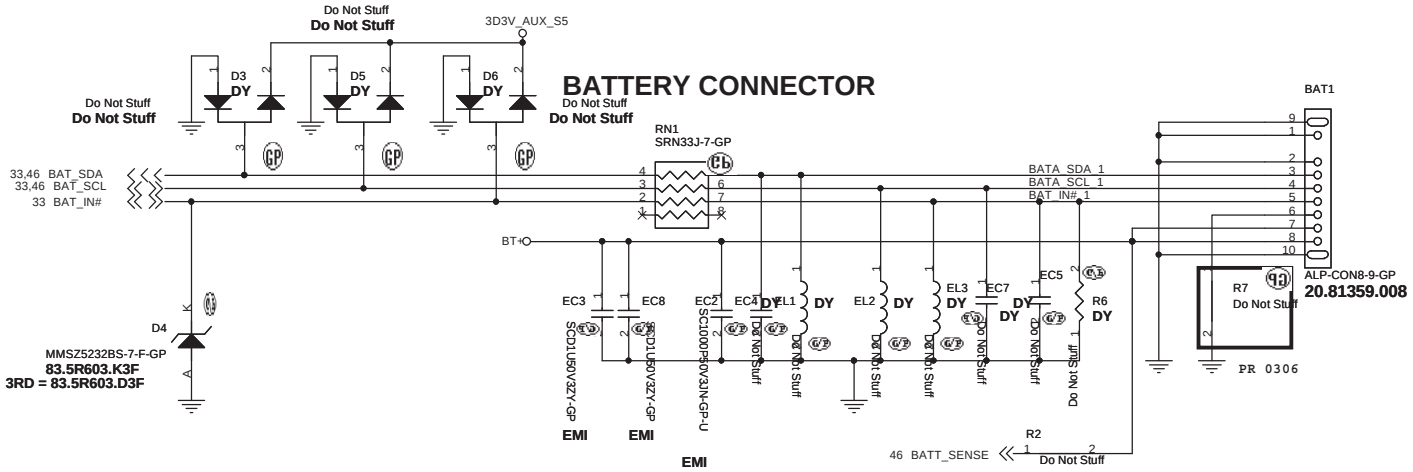
Adaptor in to generate DCBATOUT





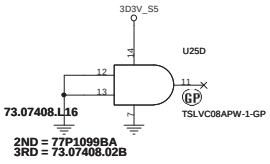


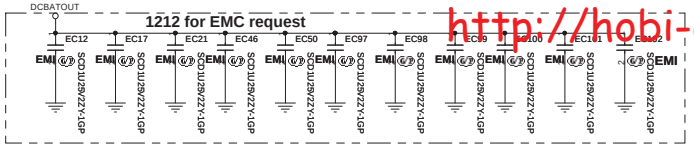
BATTERY CONNECTOR

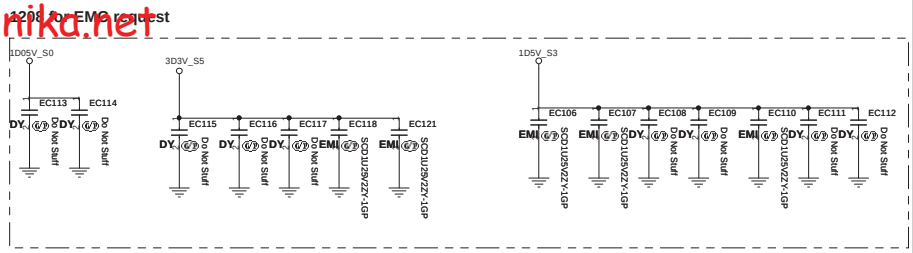


Eiger

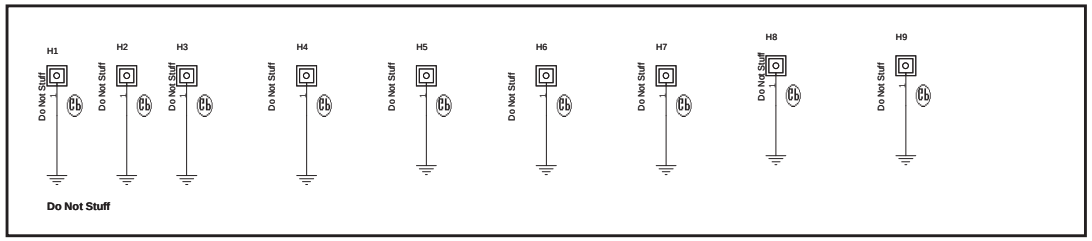
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: AD/BATT CONN		
Size	Document Number: SJM50-DN	Rev: PD
Date: Monday, April 26, 2010	Sheet 47 of 59	

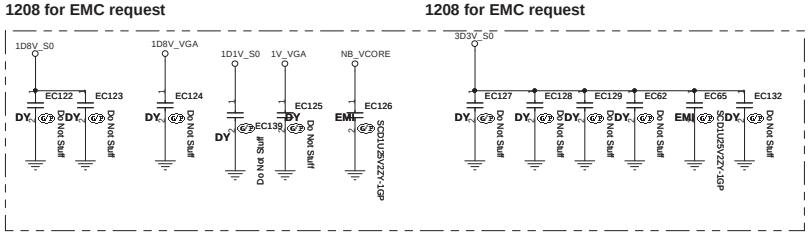


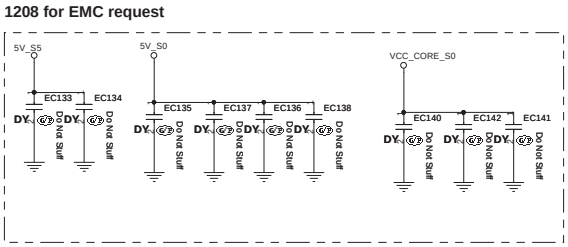


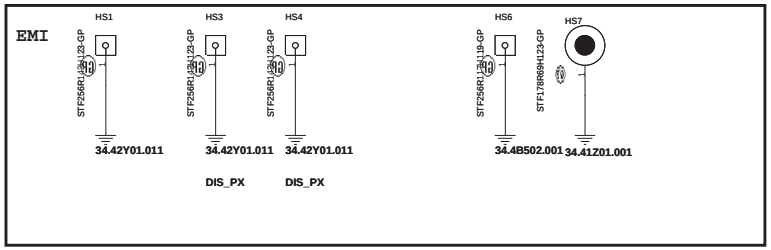


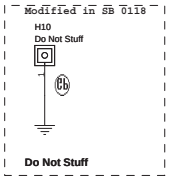
SA











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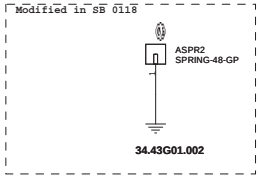
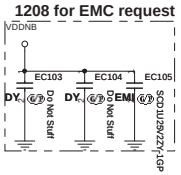
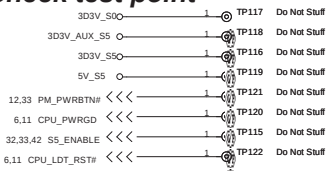




SA SB -1

Check test point



Test Point放在Dimm Door打開可量測處

Eiger

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: EMI/Spring/Boss

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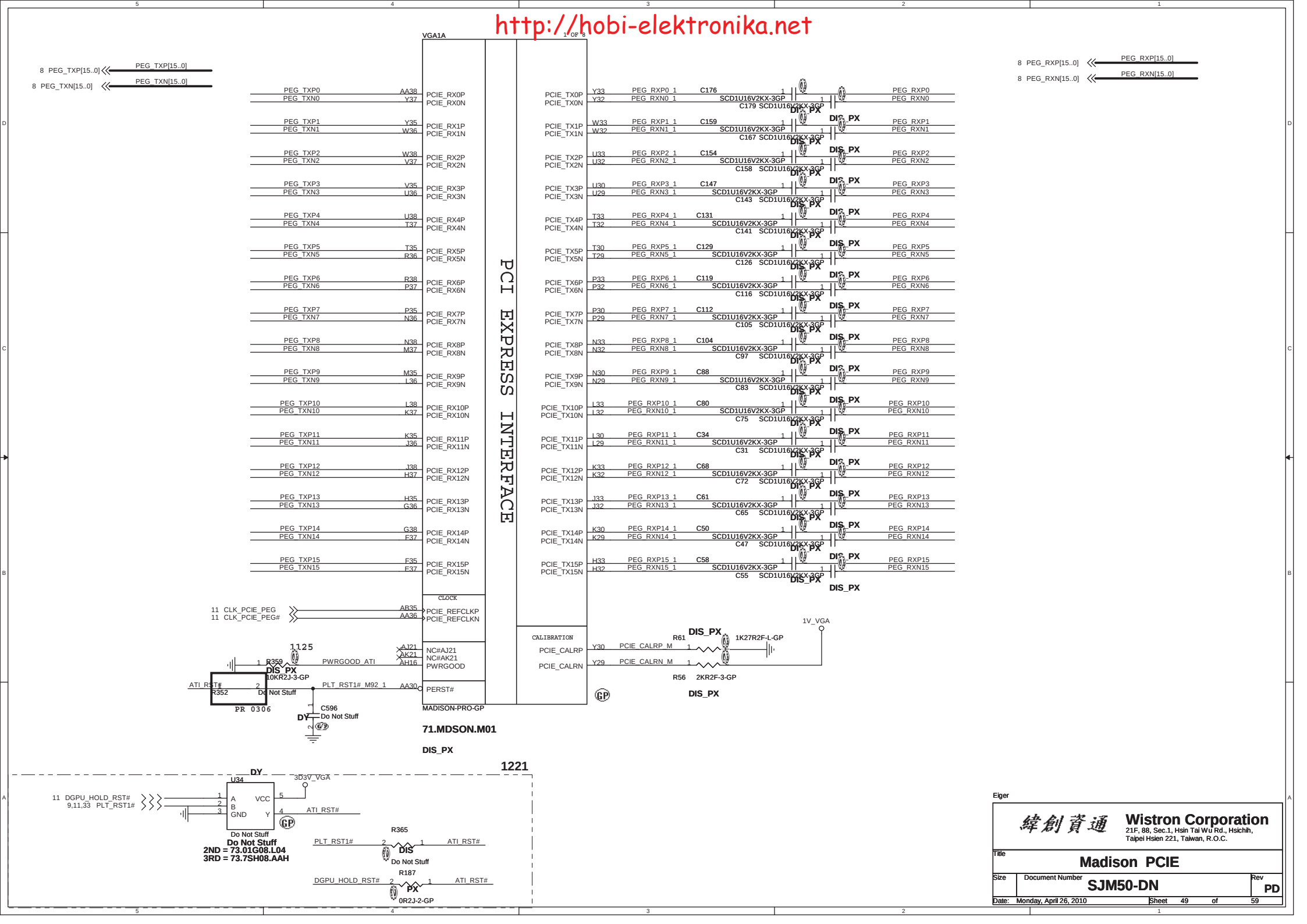


Eiger

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Madison PCIE	
Size	Document Number SJM50-DN	Rev PD
Date: Monday, April 26, 2010	Sheet 49 of 59	

Layout notice:
It should be pleace near HDMI connector

DVPDATA [3:2:1:0] for VRAM type selection H/W strap
Should provide VRAM Table for VBios request

DVPDATA [3:0]

0100	512MB	Hynix-H5PS1G63EFR-20L	(500MHz)
1000	512MB	Samsung-K4N1G164QE-HC20	(500MHz)
1100	512MB	ATI-23BY2387MB-12 LF+HF	(500MHz)

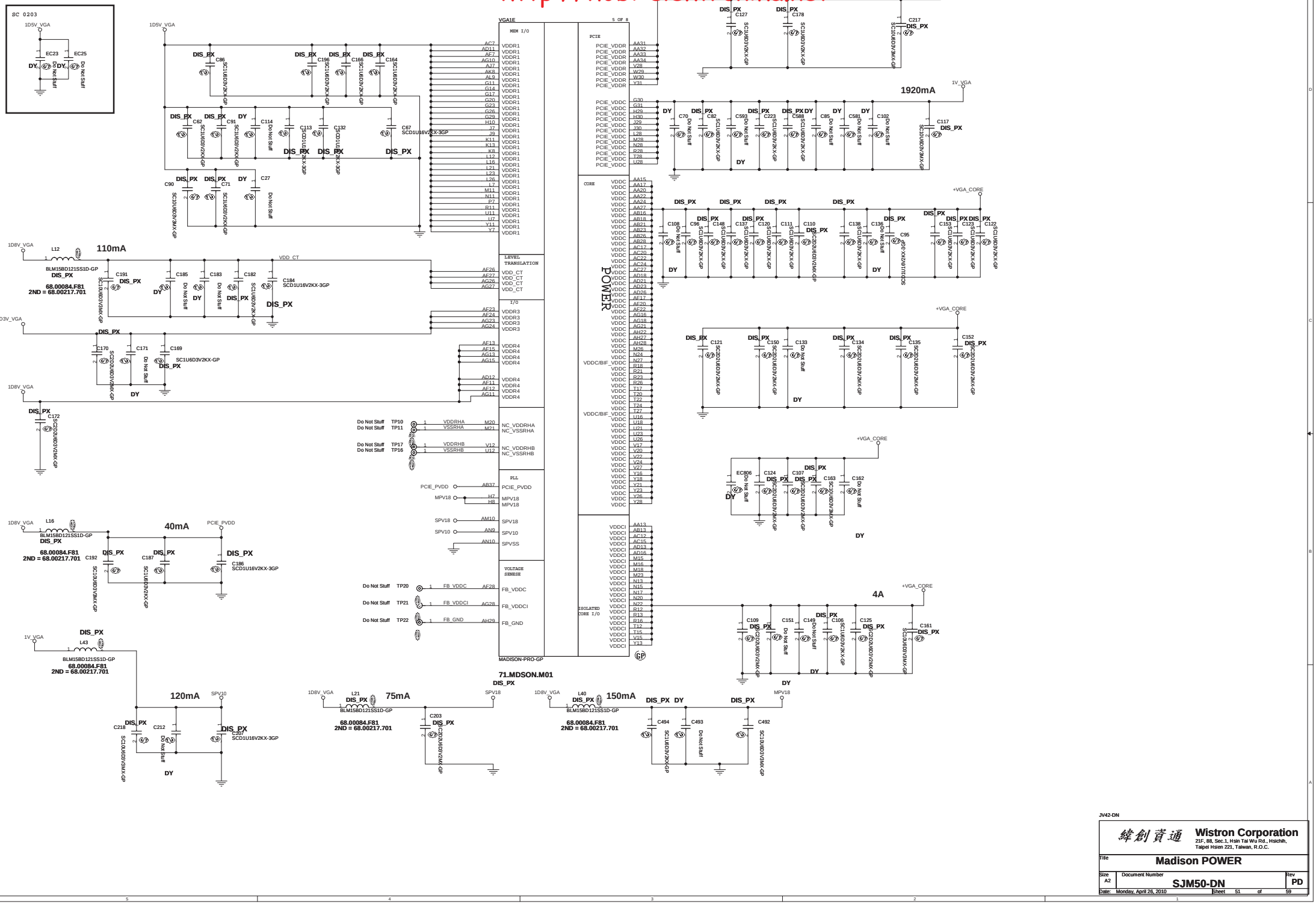
It's strap for GDDR3-136ball
Need to Clarify

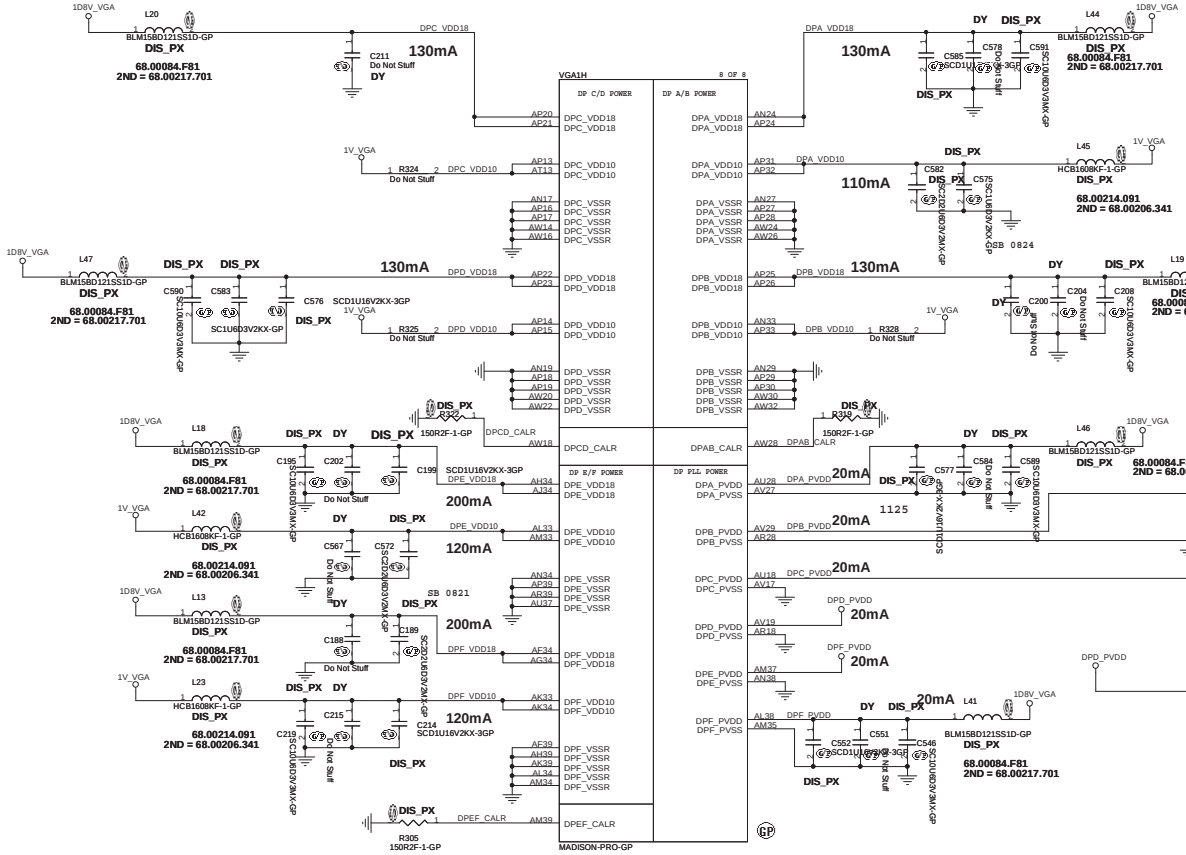
VREFG VOLTAGE DIVIDER IS (VREFG = VDDR4,5(1.8V) / 3 = 0.6V)

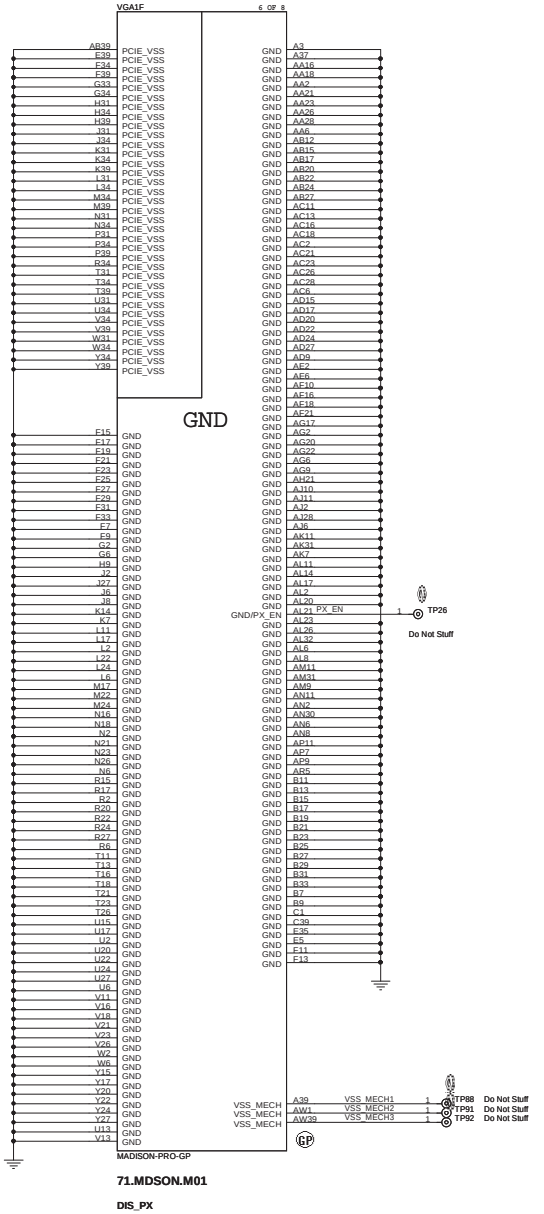
For Thermal sensor

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Madison IO
Size: Document Number: SJM50-DN Rev: PD
Date: Monday, April 26, 2010 Sheet 50 of 59

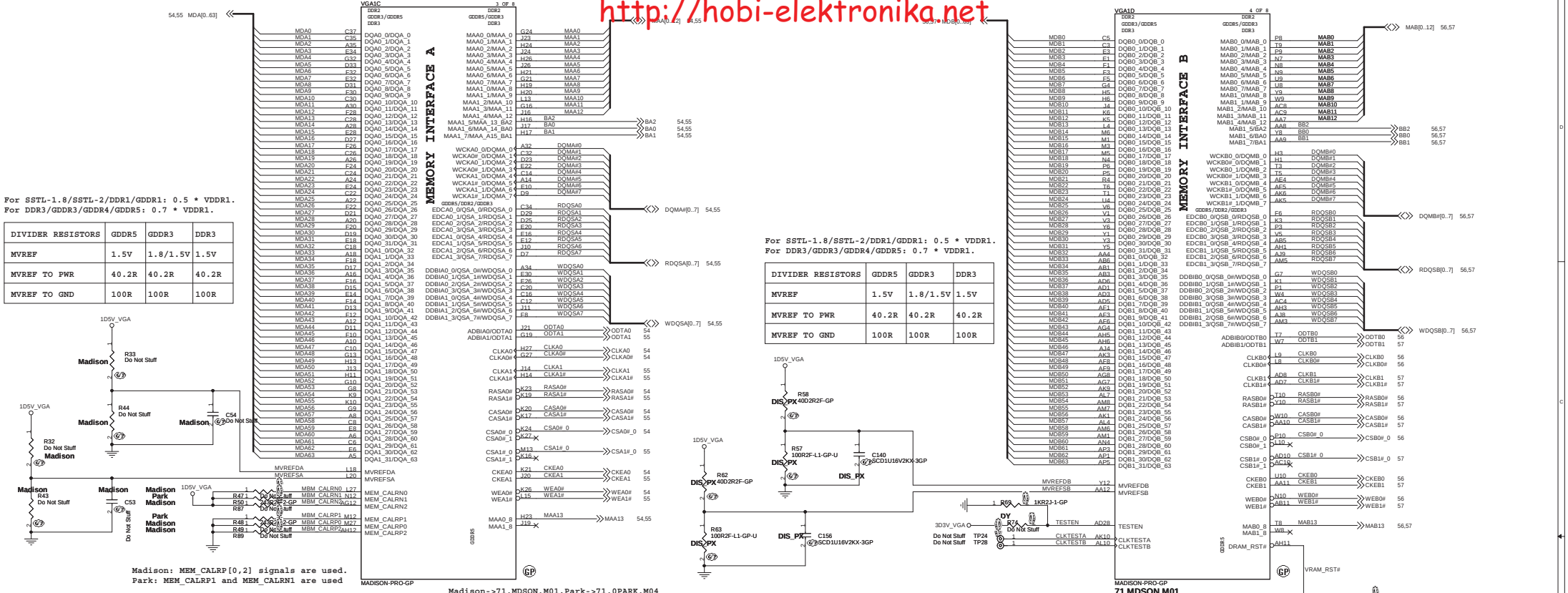






JV70-CP

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: DP POWER_GND		
Size: A2	Document Number: SJM50-DN	Rev: PD
Date: Monday, April 26, 2010	Sheet 52 of 59	



STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
TX_PWRS_ENB (Internal PD)	GPIO0	PCIE FULL TX OUTPUT SWING Tansmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	X
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	X
RESERVED	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RESERVED	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
VIP_DEVICE_STRAP_ENA (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory apeture size	X X X
RSVD	V2SYNC		0
RSVD	H2SYNC		0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI	X X

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC, GENERICC, GPIO2, GPIO21

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
V 128MB	x000	ST Microelectronics	M25P05A	0100
256MB	x001		M25P10A	0101
64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
2GB	x		Pm25LV010A	0101
4GB	x			

Designator	For M97-M2	For Mannhatton
R_MEM_1	10K	10K
R_MEM_2	40R/Short	680R
R_MEM_3	DY	DY
C_MEM	2.2nF	68pF

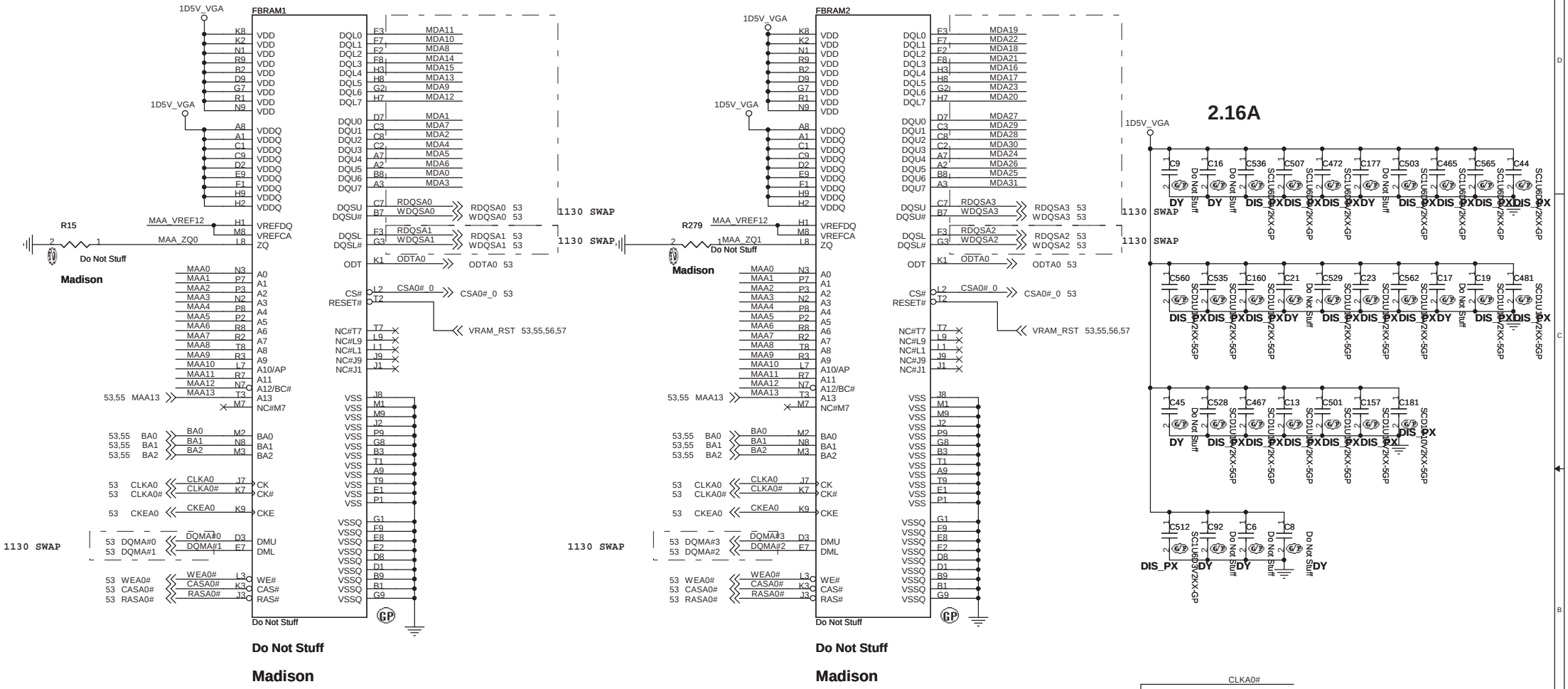
JV42-DN
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

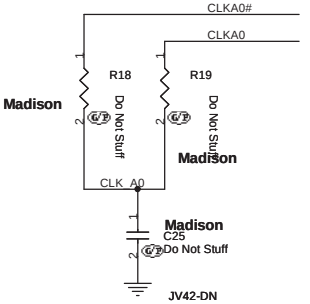
Title: Madison Memory / Straps

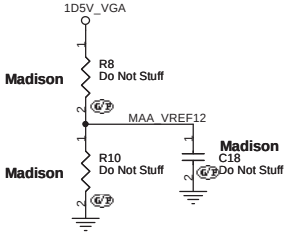
Size: A2 | Document Number: SJM50-DN | Rev: PD

Date: Monday, April 26, 2010 | Sheet 53 of 59

DDR3







SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U

53,55 DQMA#[0..7]
53,55 RDQSA[0..7]
53,55 WDQSA[0..7]
53,55 MAA[0..12] MAA[0..12]
53,55 MDA[0..63] MDA[0..63]

緯創資通	**Wistron Corporation**
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: ***VRAM(1/4)***

Size	Document Number	Rev
A3	SJM50-DN	PD

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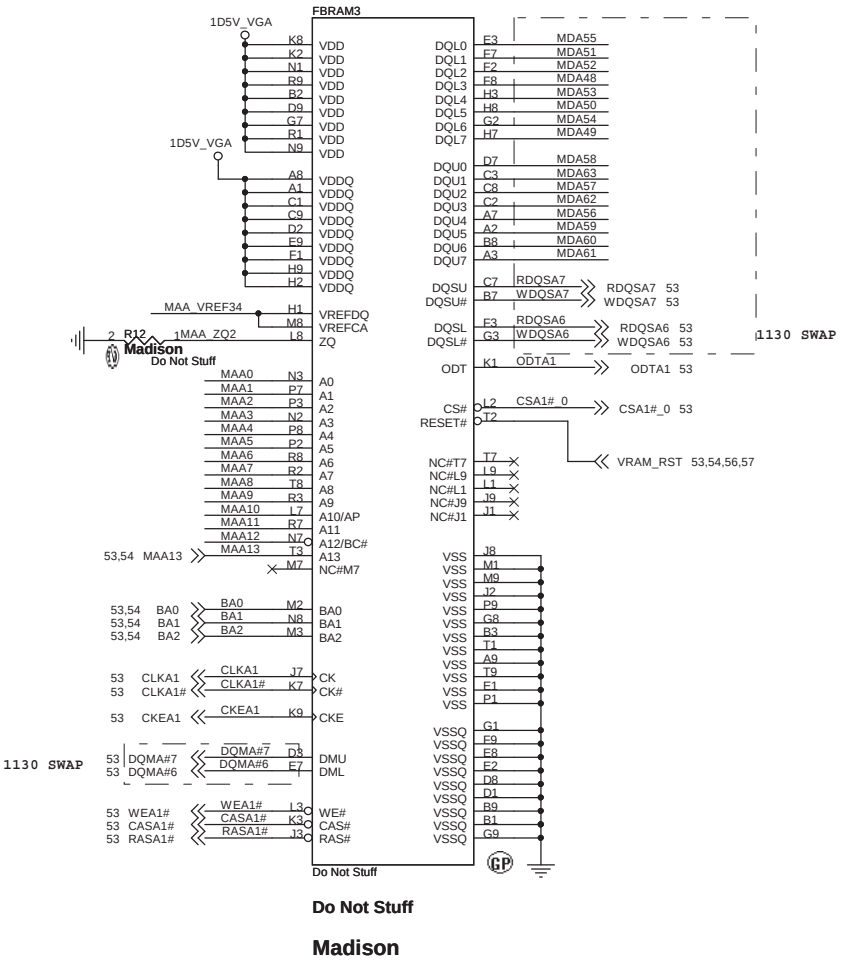
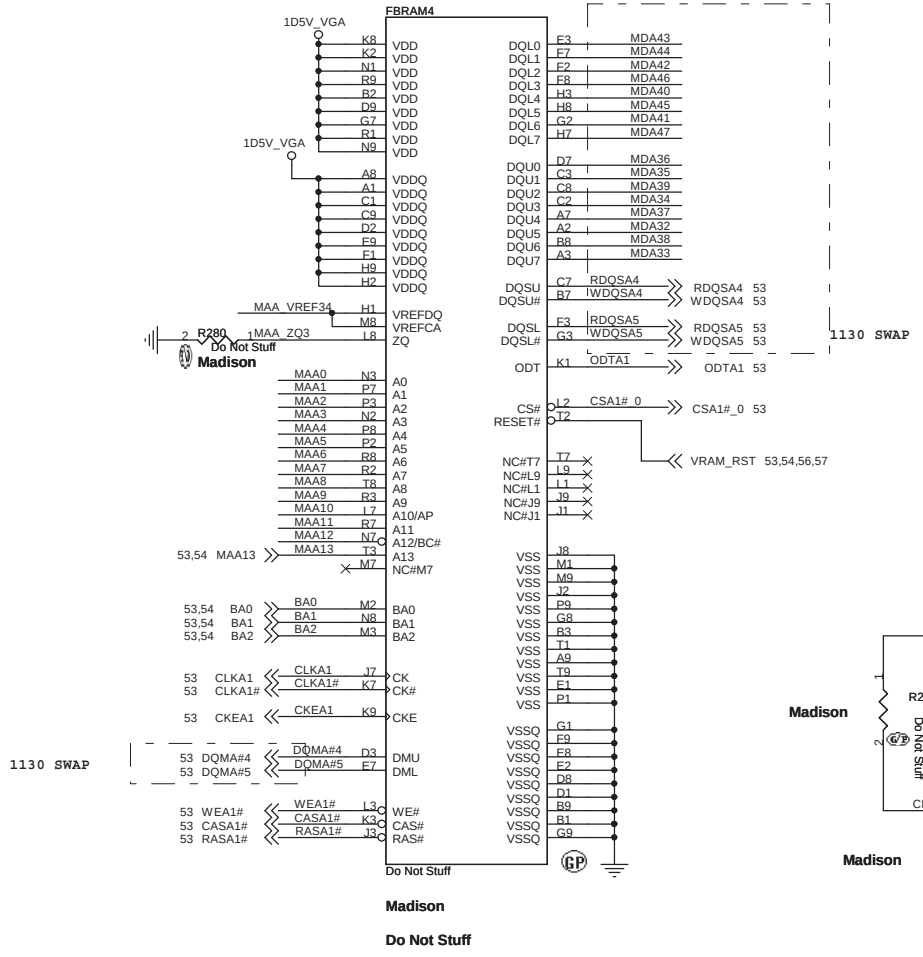
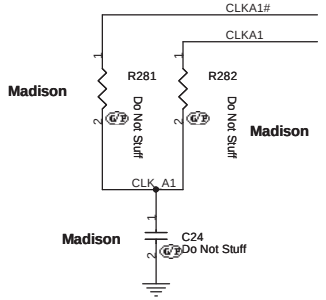
DDR3







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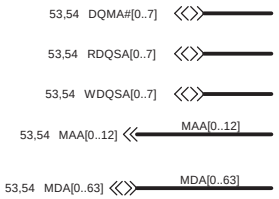
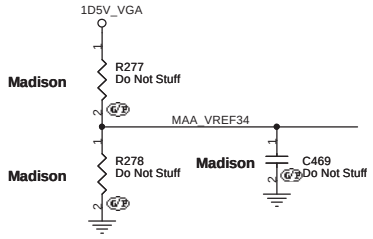
HYNIX: 72.51G63.C0U





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Title: *VRAM(2/4)*		
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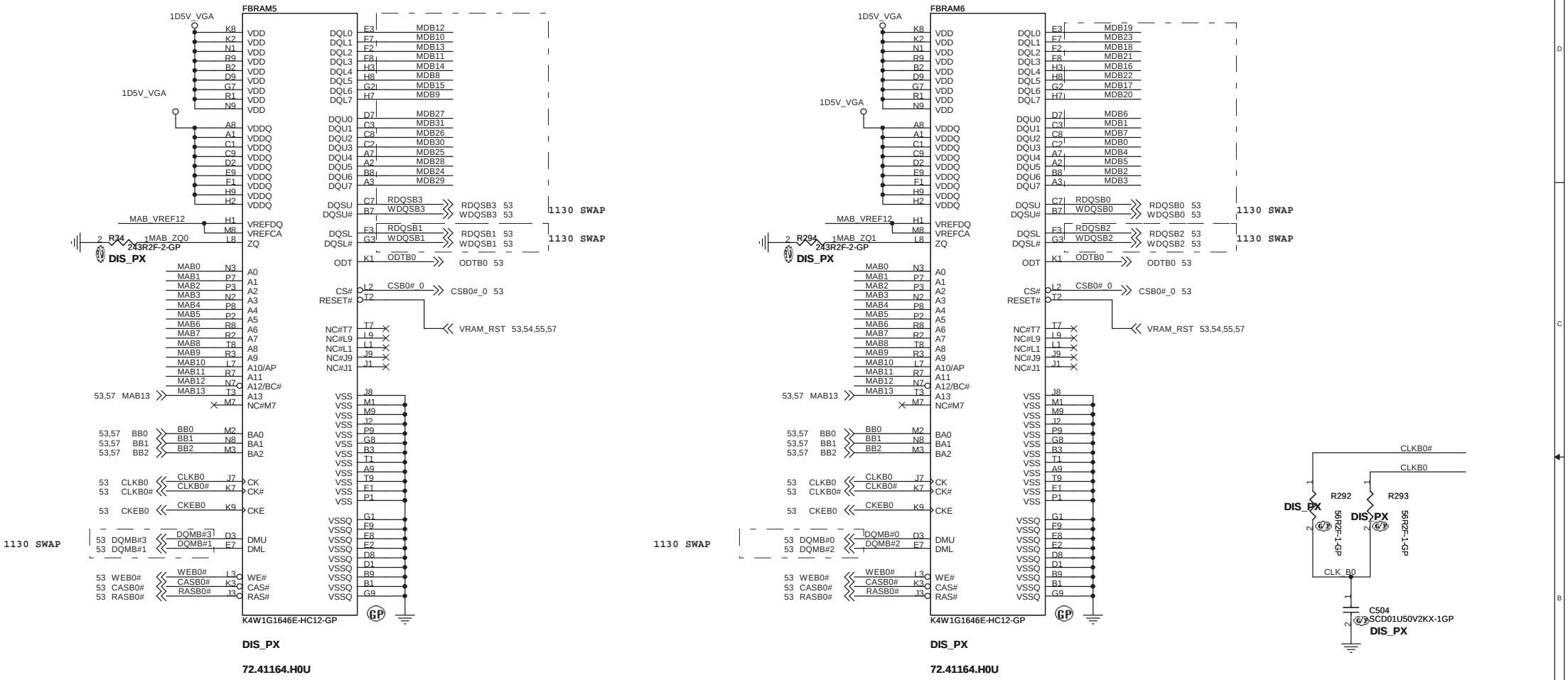
DDR3



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53,57 RDQSB[0..7]
53,57 WDQSB[0..7]
53,57 MAB[0..12]
53,57 MDB[0..63]

JV42-DN

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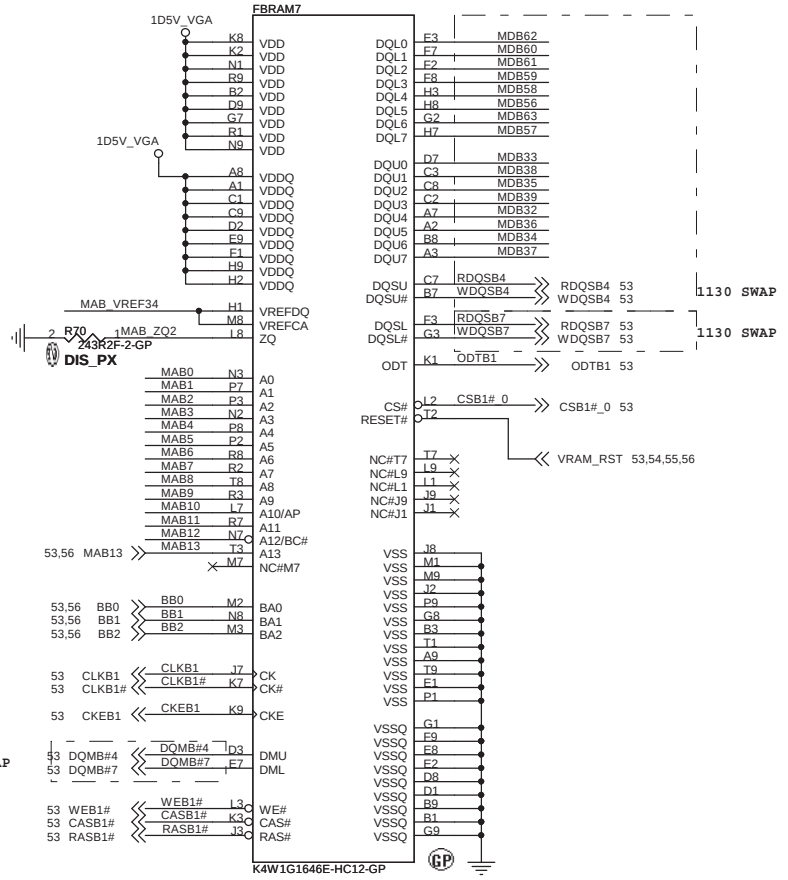
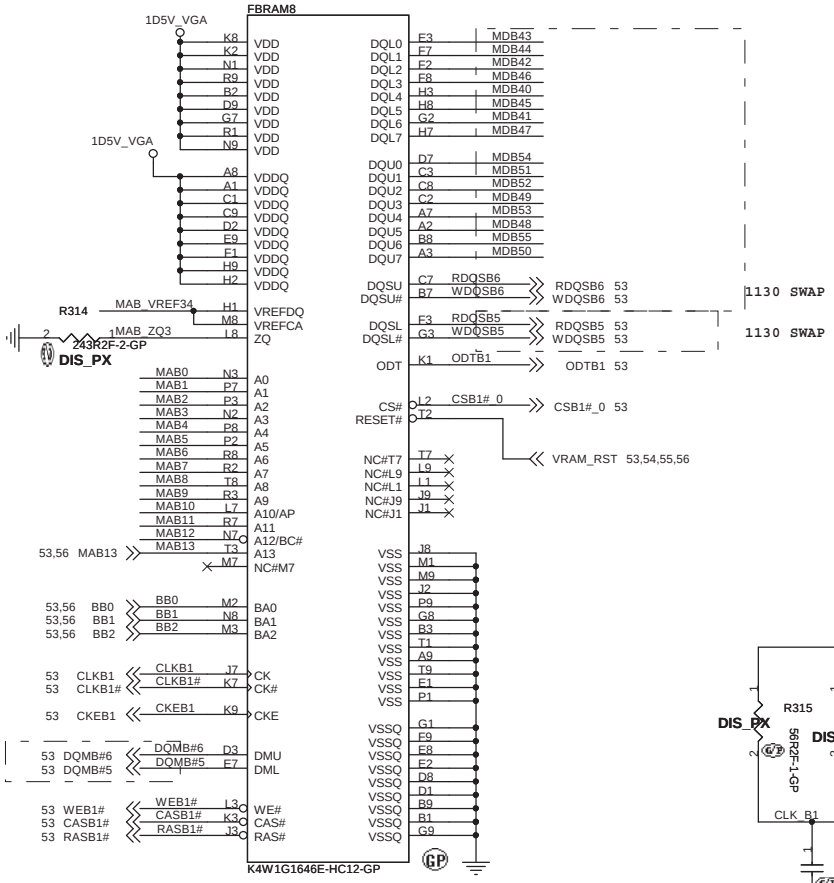
DDR3





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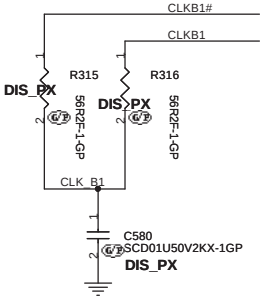

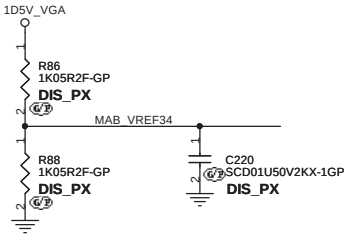

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53,56 RDQSB[0..7]

53,56 WDQSB[0..7]

53,56 MAB[0..12] MAB[0..12]

53,56 MDB[0..63] MDB[0..63]

JV42-DN

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Title: *VRAM(4/4)*		
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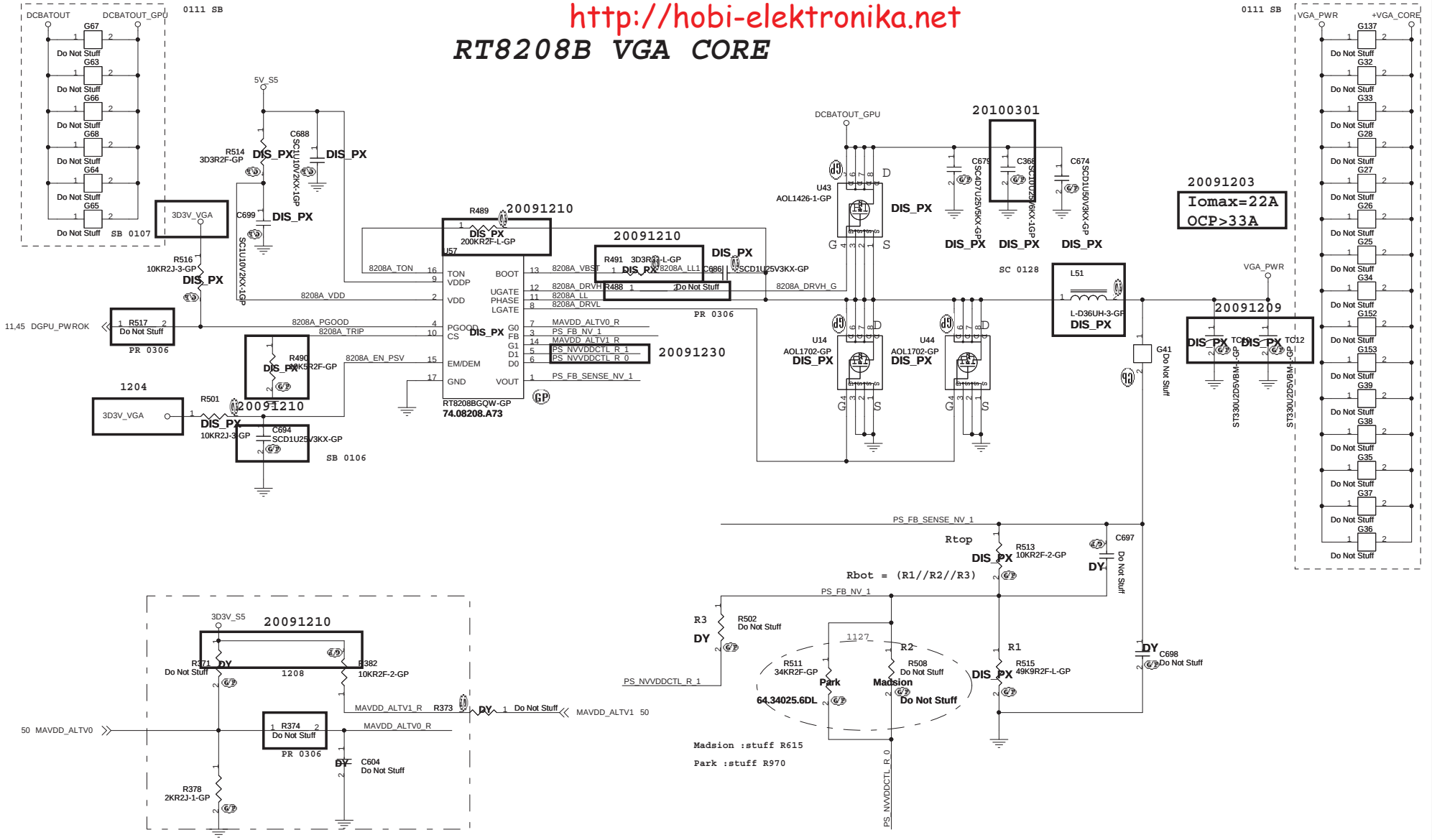
RT8208B VGA CORE



MADSION PRO

	I/O	Inter Pull Low	GPIO TABLE
NVVDD_ALTV0	O	YES	GPU VOLTAGE L: 1.00V GPU VOLTAGE H: 0.90V

PARK XT

	I/O	Inter Pull Low	GPIO TABLE
NVVDD_ALTV0	O	YES	GPU VOLTAGE L: 1.12V GPU VOLTAGE H: 0.90V

Diserete Park Samsung

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NB

RS780-->RS880M

71.RS780.M02-->71.RS880.M02

SB

SB820M-1-GP

71.SB820.00U-->71.SB820.M03

SATA_CALRP

A11: 80歐姆 1% resistor to GND

A12: TBD歐姆 1% resistor to GND

SATA_CALRN

A11:A11: 931歐姆1% resistor to VDDAN_11_SATA

A12: TBD歐姆 1% resistor to VDDAN_11_SATA.

VGA

Madison--> PN:71.MDSON.M01

Park--> PN:71.0PARK.M04

VRAM

Samsung-->VRAM FBRAM1~8 PN:VR.1GB0B.006

Hynix--> VRAM FBRAM1~8 PN:VR.1GB0G.004

ATI-> VRAM FBRAM1~8 PN:VR.1GB0T.002

HDMI

R217 : DIS & PX-->100K

UMA-->10K(63.10334.1DL R402H16 10KR2J-3-GP)

R341 : DIS & PX-->0 OHM

UMA-->5.1K(63.51234.1D1 5.1K J 1/16W 0402)

Side port

Samsung-->VRAM FBRAM1~8 PN:VR.1GB0B.006

Hynix--> VRAM FBRAM1~8 PN:VR.1GB0G.004

ATI-> VRAM FBRAM1~8 PN:VR.1GB0T.002

CRT

UMA-->L1-->2R 0603

C30-->47U/6.3V

DIS-->L1-->Bead(L1 68.00217.711 L1608-UH38 SBK160808T-221Y-N-GP)

C30-->DY

PX--> 150 歐姆 (R521 64.15005.6DL CHIP RES 150 F 1/16W 0402)

MINI1

MINI1--> 20.F1516.052

BOM

```
1st -> PX Diserete Madison Samsung
Side port -> Samsung
HDMI      ->NO repeater

1nd  -> PX Diserete Park Hynix
Side port -> Hynix
HDMI      ->repeater

1st -> UMA
Side port -> Samsung
HDMI      ->NO repeater
```

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	NOTE	
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