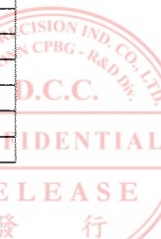


Schematics Page Index (Title / Revision / Change Date)

Page	Title of Schematics Page	Rev.	Date	Page	Title of Schematics Page	Rev.	Date
01	Schematics Page Index	1.00	1215	36	SATA HDD/CD-ROM	1.00	1215
02	Block Diagram	1.00	1215	37	EC+KBC	1.00	1215
03	Yonah(HOST BUS) 1/2	1.00	1215	38	Flash ROM/XBUS	1.00	1215
04	Yonah(HOST BUS) 2/3	1.00	1215	39	LED/LID SW#/Touch PAD	1.00	1215
05	Yonah(Power/Gnd) 3/3	1.00	1215	40	Mini-PCIE Card	1.00	1215
06	CALISTOGA (HOST) 1/7	1.00	1215	41	FAN/Bluetooth	1.00	1215
07	CALISTOG (DMI) 2/7	1.00	1215	42	EXPRESS/CAM/OIDE	1.00	1215
08	CALIST (GRAPHIC) 3/7	1.00	1215	43	AUDIO(CODEC & POWER)	1.00	1215
09	CALISTOGA (DDRII) 4/7	1.00	1215	44	AUDIO(AMP & HP & SPK)	1.00	1215
10	CALIST (POWER,VCC) 5/7	1.00	1215	45	AUDIO(EXTMIC&PHONE OUT)	1.00	1215
11	CALIST (VCC CORE) 6/7	1.00	1215	46	AUDIO (MUTE & INTMIC)	1.00	1215
12	CALIST (VSS) 7/7	1.00	1215	47	AUDIO (PHONE OUT)	1.00	1215
13	DDRII(SO-DIMM_0) 1/3	1.00	1215	48	PCI (PCI BUS)	1.00	1215
14	DDRII(SO-DIMM_1) 2/3	1.00	1215	49	PCI (ILINK)	1.00	1215
15	DDRII(Termination) 3/3	1.00	1215	50	PCI (MS-DUO/MDC)	1.00	1215
16	VGA(PCI-E/STRAP) 1/8	1.00	1215	51	PCI (PCMCIA)	1.00	1215
17	VGA(PCI-E/STRAP) 2/8	1.00	1215	52	USB2.0/DOCKING CONN.	1.00	1215
18	VGA(GDDR) 3/8	1.00	1215	53	USB HUB	1.00	1215
19	VGA(POWER) 4/8	1.00	1215	54	LAN (82562GT)	1.00	1215
20	VGA(POWER) 5/8	1.00	1215	55	Power Design Diagram	1.00	1215
21	VGA(POWER) 6/8	1.00	1215	56	DCIN&Charger	1.00	1215
22	VGA(MULTIUSE) 7/8	1.00	1215	57	SYS Power (+3_3V/+5V)	1.00	1215
23	VGA(LVDS/VDAC) 8/8	1.00	1215	58	SYS Power(+1_5V/+1_05V)	1.00	1215
24	VRAM(GDDR) 1/5	1.00	1215	59	DDR2 Power(+1_8V/+0_9V)	1.00	1215
25	VRAM(GDDR) 2/5	1.00	1215	60	CPU_Vcore ---MAX8771	1.00	1215
26	VRAM(POWERBYPASS) 3/4	1.00	1215	61	Others power plan	1.00	1215
27	VRAM(POWERBYPASS) 4/4	1.00	1215	62	OVP protection	1.00	1215
28	LVDS	1.00	1215	63	VGA POWER(+1_1V/ +1_2V)	1.00	1215
29	CRT	1.00	1215	64	CLOCK GEN	1.00	1215
30	S-VIDEO/Semi-PnP	1.00	1215	65	HOLE	1.00	1215
31	ICH7-M(PCI/USB) 1/5	1.00	1215	66	History (1)	1.00	1215
32	ICH7-M(LPC,IDE,SATA)2/5	1.00	1215	67	History (2)	1.00	1215
33	ICH7-M(GPIO) 3/5	1.00	1215	68	History (3)	1.00	1215
34	ICH7-M(POWER) 4/5	1.00	1215	69	History (4)	1.00	1215
35	ICH7-M(GND) 5/5	1.00	1215	70	History (5)	1.00	1215
				71	History (6)	1.00	1215
				72	History (7)	1.00	1215
				73	History (8)	1.00	1215
				74	History (9)	1.00	1215



Project Code & Schematics Subject: MS10 Main Board

PCB P/N: 1P-005C100-8011(FUBAI)
1P-005C500-8011(HANSTAR)
1P-005C200-8011(NAB YA)

P. Leader	Check by	Design by
陳秋鵬	陳光偉	張文翰
FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title Index Page		
Size A3	Document Number MS10-1-01 (MBX-149)	Rev 1.00
Date	Monday, December 19, 2005	
	Sheet	1 of 74

Schematics Page Index (Title / Revision / Change Date)

Page	Title of Schematics Page	Rev.	Date	Page	Title of Schematics Page	Rev.	Date
01	Schematics Page Index	1.00	1215	36	SATA HDD/CD-ROM	1.00	1215
02	Block Diagram	1.00	1215	37	EC+KBC	1.00	1215
03	Yonah(HOST BUS) 1/2	1.00	1215	38	Flash ROM/XBUS	1.00	1215
04	Yonah(HOST BUS) 2/3	1.00	1215	39	LED/LID SW#/Touch PAD	1.00	1215
05	Yonah(Power/Gnd) 3/3	1.00	1215	40	Mini-PCIE Card	1.00	1215
06	CALISTOGA (HOST) 1/7	1.00	1215	41	FAN/Bluetooth	1.00	1215
07	CALISTOG (DMI) 2/7	1.00	1215	42	EXPRESS/CAM/OIDE	1.00	1215
08	CALIST (GRAPHIC) 3/7	1.00	1215	43	AUDIO(CODEC & POWER)	1.00	1215
09	CALISTOGA (DDR2) 4/7	1.00	1215	44	AUDIO(AMP & HP & SPK)	1.00	1215
10	CALIST (POWER,VCC) 5/7	1.00	1215	45	AUDIO(EXTMIC&PHONE OUT)	1.00	1215
11	CALIST (VCC CORE) 6/7	1.00	1215	46	AUDIO (MUTE & INTMIC)	1.00	1215
12	CALIST (VSS) 7/7	1.00	1215	47	AUDIO (PHONE OUT)	1.00	1215
13	DDR2(S0-DIMM_0) 1/3	1.00	1215	48	PCI (PCI BUS)	1.00	1215
14	DDR2(S0-DIMM_1) 2/3	1.00	1215	49	PCI (ILINK)	1.00	1215
15	DDR2(Termination) 3/3	1.00	1215	50	PCI (MS-DUO/MDC)	1.00	1215
16	VGA(PCI-E/STRAP) 1/8	1.00	1215	51	PCI (PCMCIA)	1.00	1215
17	VGA(PCI-E/STRAP) 2/8	1.00	1215	52	USB2.0/DOCKING CONN.	1.00	1215
18	VGA(GDDR) 3/8	1.00	1215	53	USB HUB	1.00	1215
19	VGA(POWER) 4/8	1.00	1215	54	LAN (82562GT)	1.00	1215
20	VGA(POWER) 5/8	1.00	1215	55	Power Design Diagram	1.00	1215
21	VGA(POWER) 6/8	1.00	1215	56	DCIN&Charger	1.00	1215
22	VGA(MULTIUSE) 7/8	1.00	1215	57	SYS Power (+3_3V/+5V)	1.00	1215
23	VGA(LVDS/VDAC) 8/8	1.00	1215	58	SYS Power(+1_5V/+1_05V)	1.00	1215
24	VRAM(GDDR) 1/5	1.00	1215	59	DDR2 Power(+1_8V/+0_9V)	1.00	1215
25	VRAM(GDDR) 2/5	1.00	1215	60	CPU Vcore ---MAX8771	1.00	1215
26	VRAM(POWERBYPASS) 3/4	1.00	1215	61	Others power plan	1.00	1215
27	VRAM(POWERBYPASS) 4/4	1.00	1215	62	OVP protection	1.00	1215
28	LVDS	1.00	1215	63	VGA POWER(+1_1V/ +1_2V)	1.00	1215
29	CRT	1.00	1215	64	CLOCK GEN	1.00	1215
30	S-VIDEO/Semi-PnP	1.00	1215	65	HOLE	1.00	1215
31	ICH7-M(PCI/USB) 1/5	1.00	1215	66	History (1)	1.00	1215
32	ICH7-M(LPC, IDE, SATA)2/5	1.00	1215	67	History (2)	1.00	1215
33	ICH7-M(GPIO) 3/5	1.00	1215	68	History (3)	1.00	1215
34	ICH7-M(POWER) 4/5	1.00	1215	69	History (4)	1.00	1215
35	ICH7-M(GND) 5/5	1.00	1215	70	History (5)	1.00	1215
				71	History (6)	1.00	1215
				72	History (7)	1.00	1215
				73	History (8)	1.00	1215
				74	History (9)	1.00	1215

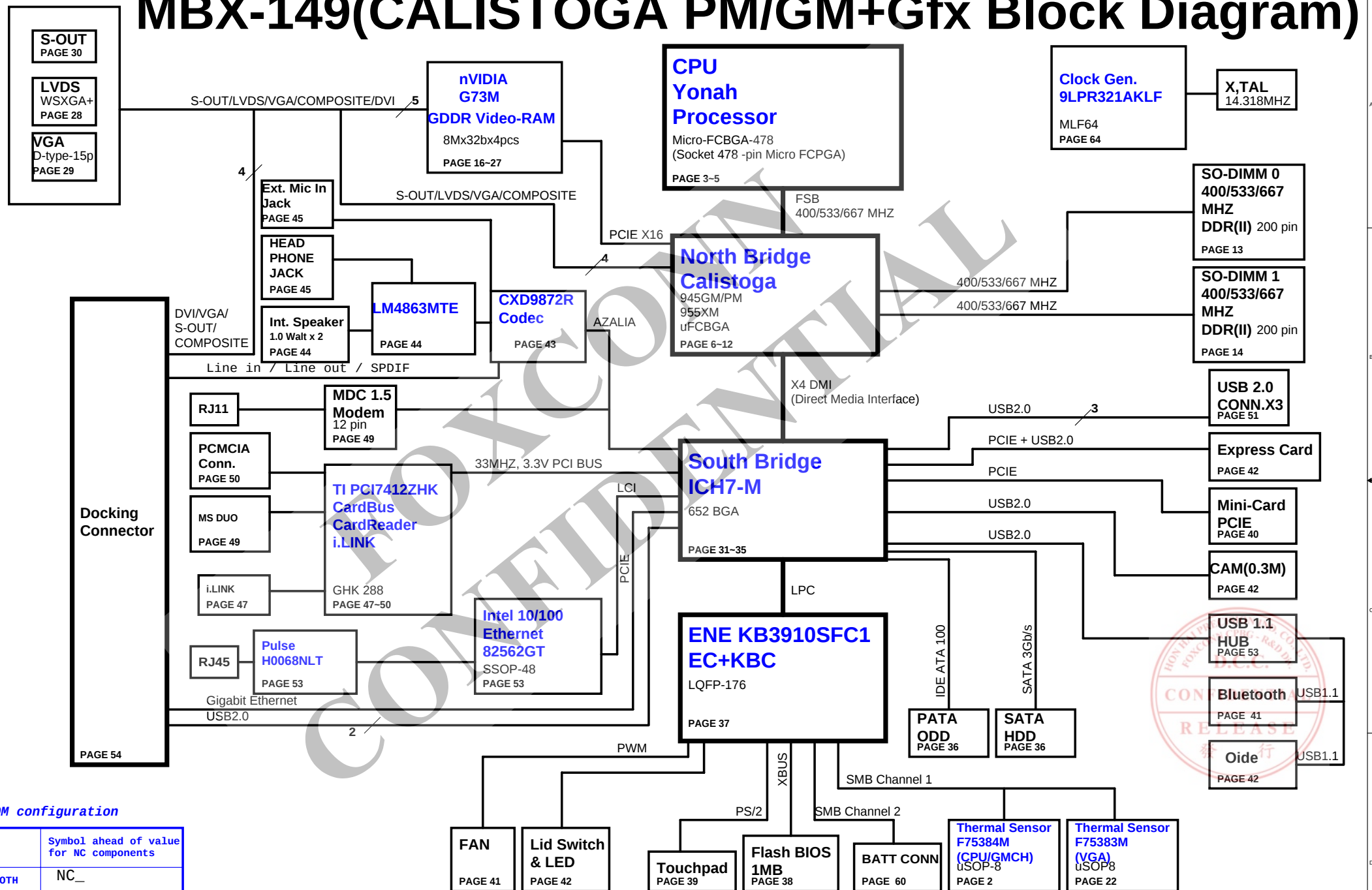
Project Code & Schematics Subject: MS10 Main Board

PCB P/N: 1P-005C100-8011(FUBAI)
1P-005C500-8011(HANSTAR)
1P-005C200-8011(NAB YA)

P. Leader	Check by	Design by

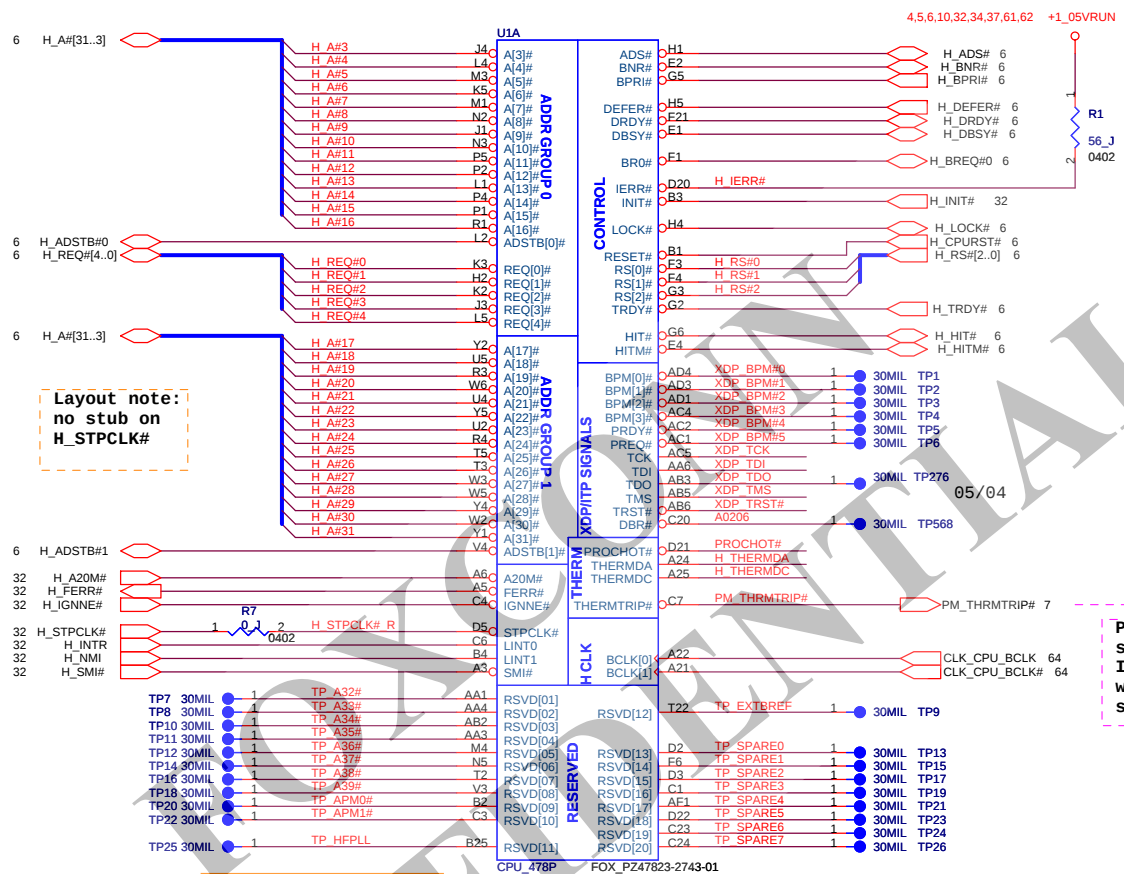
FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title Index Page	
Size A3	Document Number MS10-1-01 (MBX-149)
Date: Tuesday, December 20, 2005	Sheet 1 of 74

MBX-149(CALISTOGA PM/GM+Gfx Block Diagram)



BOM configuration

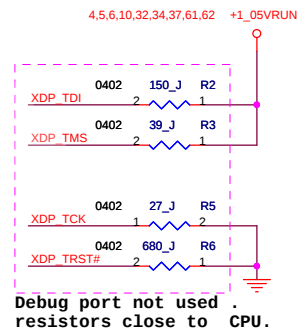
	Symbol ahead of value for NC components
BOTH	NC_
945PM + NV43M	CA_
945GM	NV_



Layout note:
no stub on
H_STPCLK#

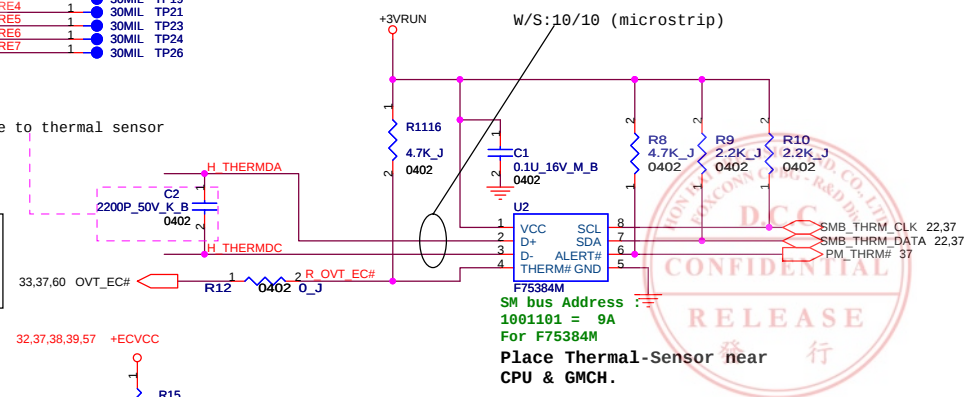
A#[32-39], APM#[0-1]:
Leave escape routing
on for future
functionality

ICH7M's GPIO12: VIL----> -0.5V ~ -0.8V
VIH----> 2.0V ~ 3.3+0.5V
YONAH's PROCHOT#: VIL----> -0.1V ~ -0.3*VCCP
VIH----> 0.7*VCCP ~ VCCP+0.1

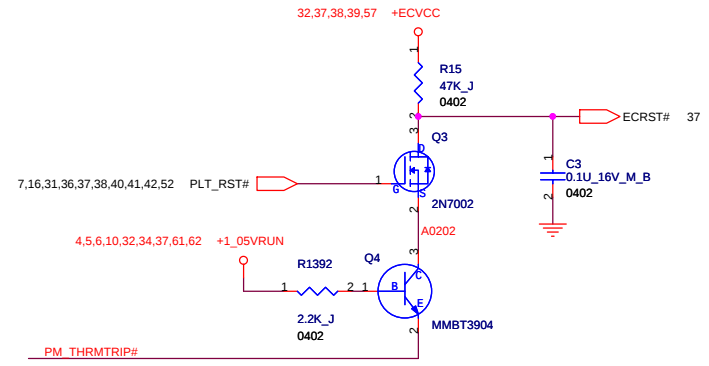
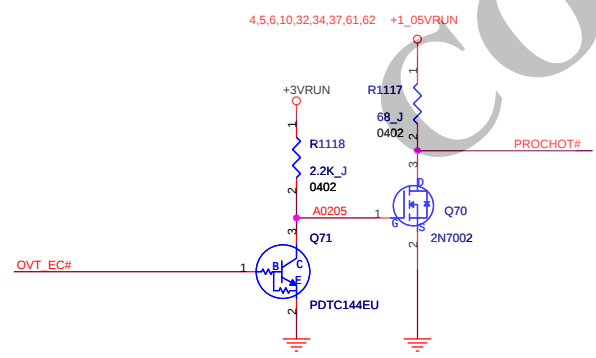


Debug port not used .
resistors close to CPU.

PM_THRMTRIP#
should connect to
ICH7-M and GMCH
without T-ing (No
stub)



SM bus Address :
1001101 = 9A
For F75384M
Place Thermal-Sensor near
CPU & GMCH.



Place close to CPU

3.5,6,10,32,34,37,61,62 +1_05VRUN

5 mil(microstrip)

Max Length 0.5 inch

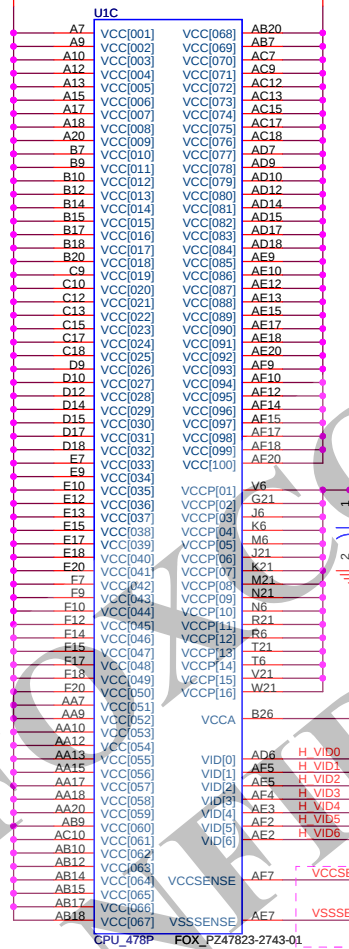
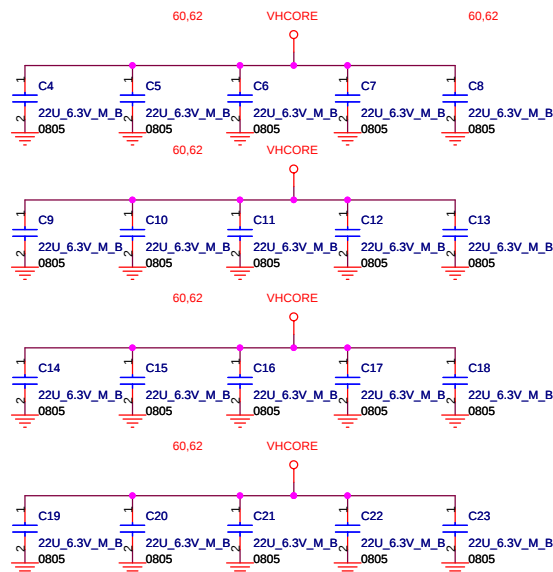
Layout Note:
Zo=55 ohm, 0.5"
max for GTLREF.

Layout Note:
Comp0,2 connect with Zo=27.4 ohm, make
trace length shorter then 0.5".
Comp1,3 connect with Zo=55 ohm, make
trace length shorter then 0.5".

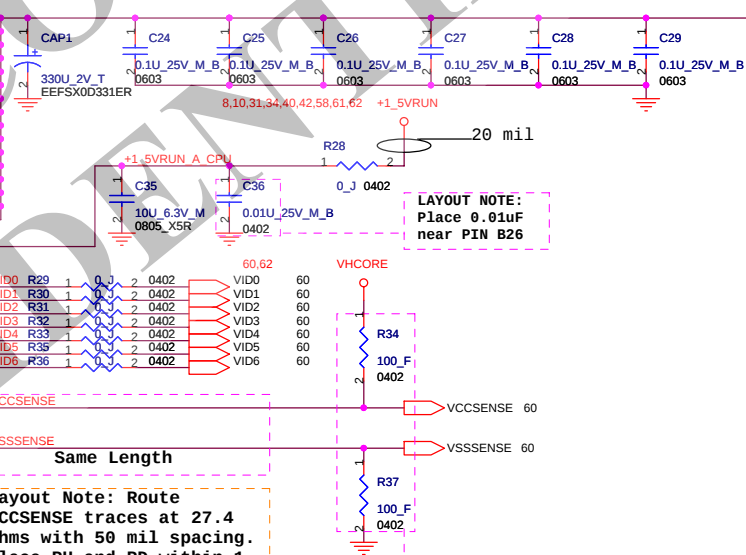
IMVP6 (max8736)
cpu PSI# <-> max8736 PSI#
max8736: VIHmin=0.67V
VILmax=0.33V
(ref. max8736 datasheet)

Layout:
Connect test
point with no
stub



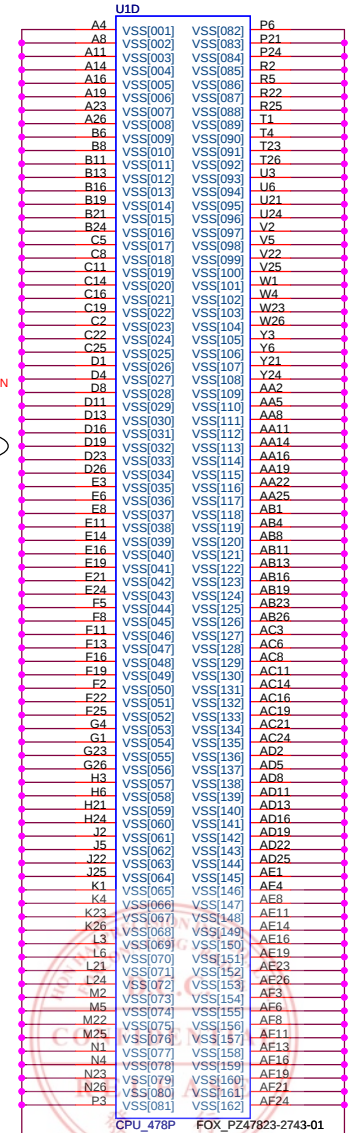
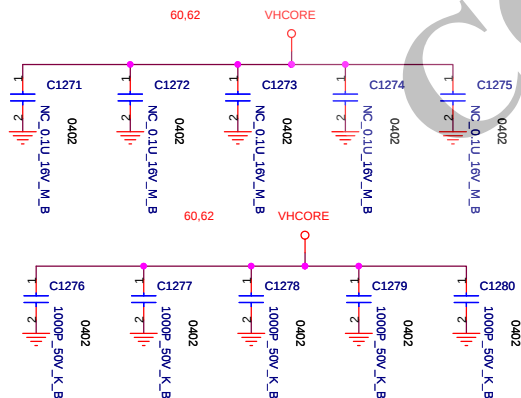


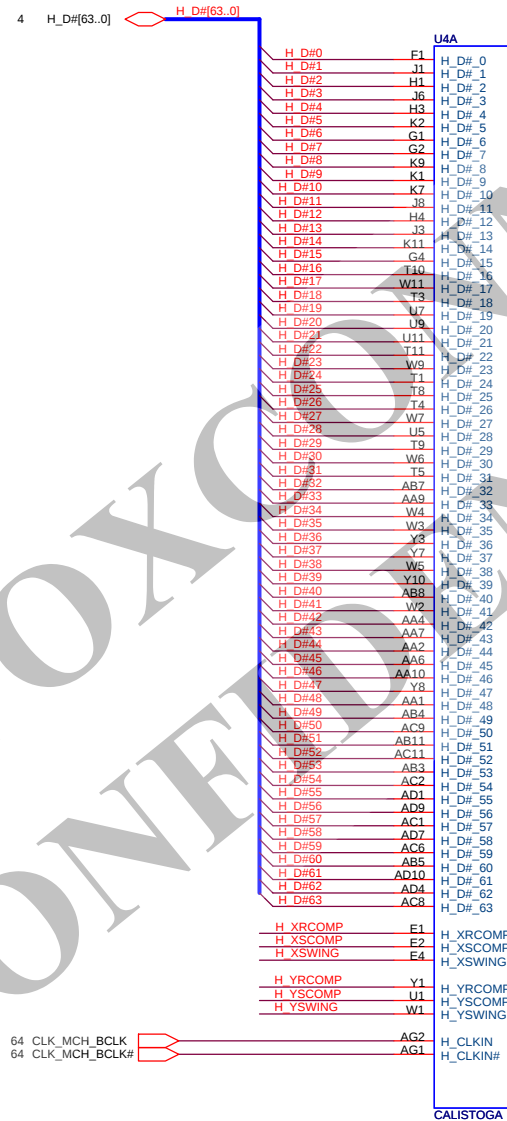
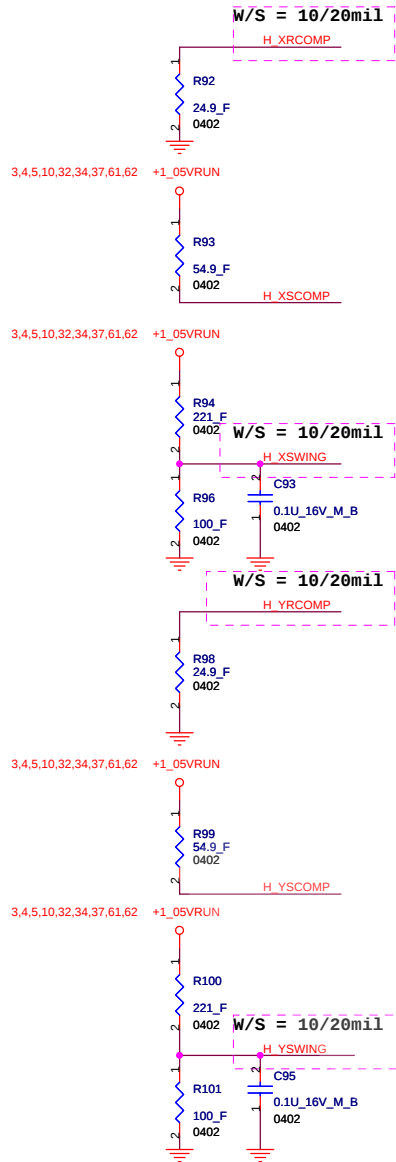
CPU_VCCA---->120mA
CPU_VCCP----->2.5A
CPU_VCC----->36A



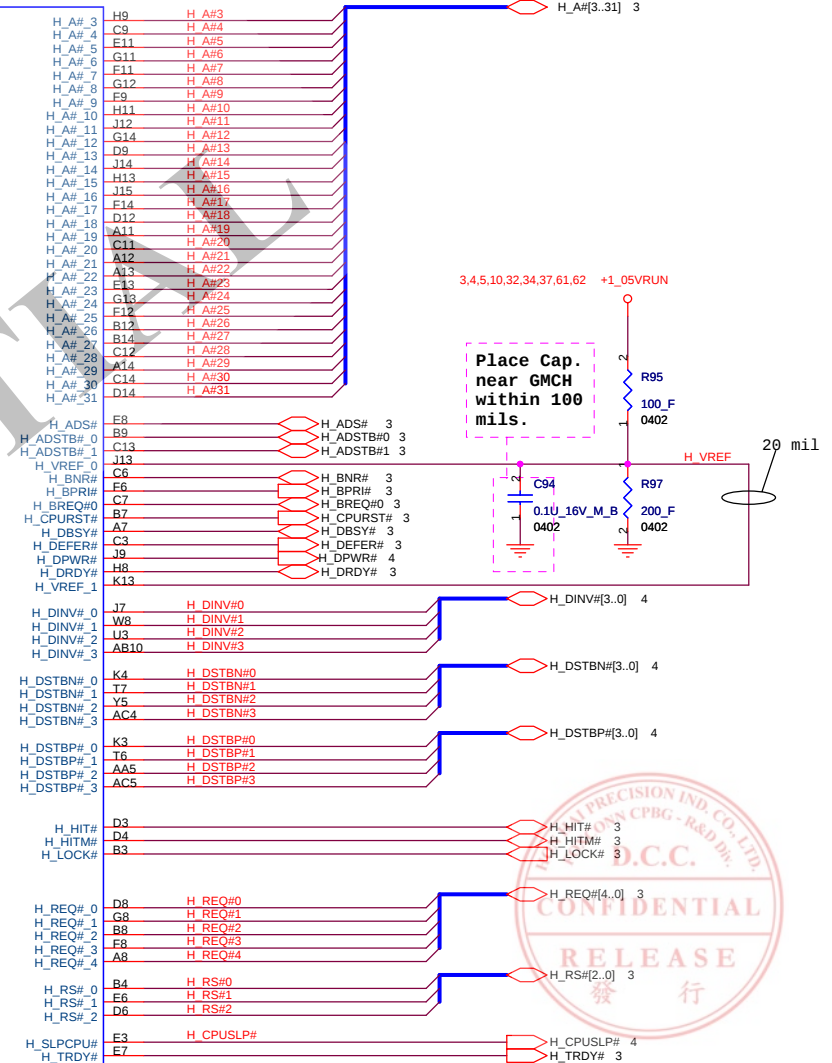
LAYOUT NOTE:
Place 0.01uF
near PIN B26

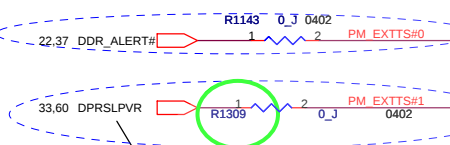
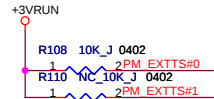
Layout Note: Route
VCCSENSE traces at 27.4
Ohms with 50 mil spacing.
Place PU and PD within 1
inch of cpu.
width=18 mil
spacing=7 mil



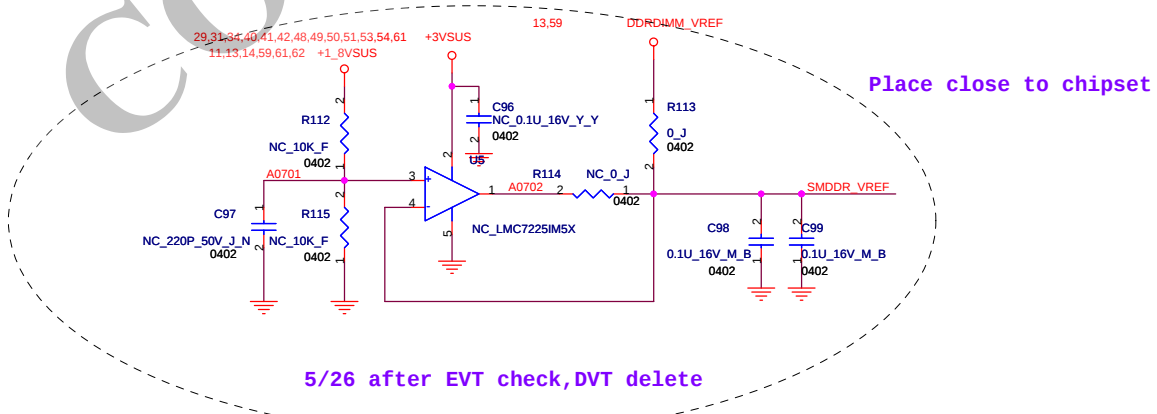
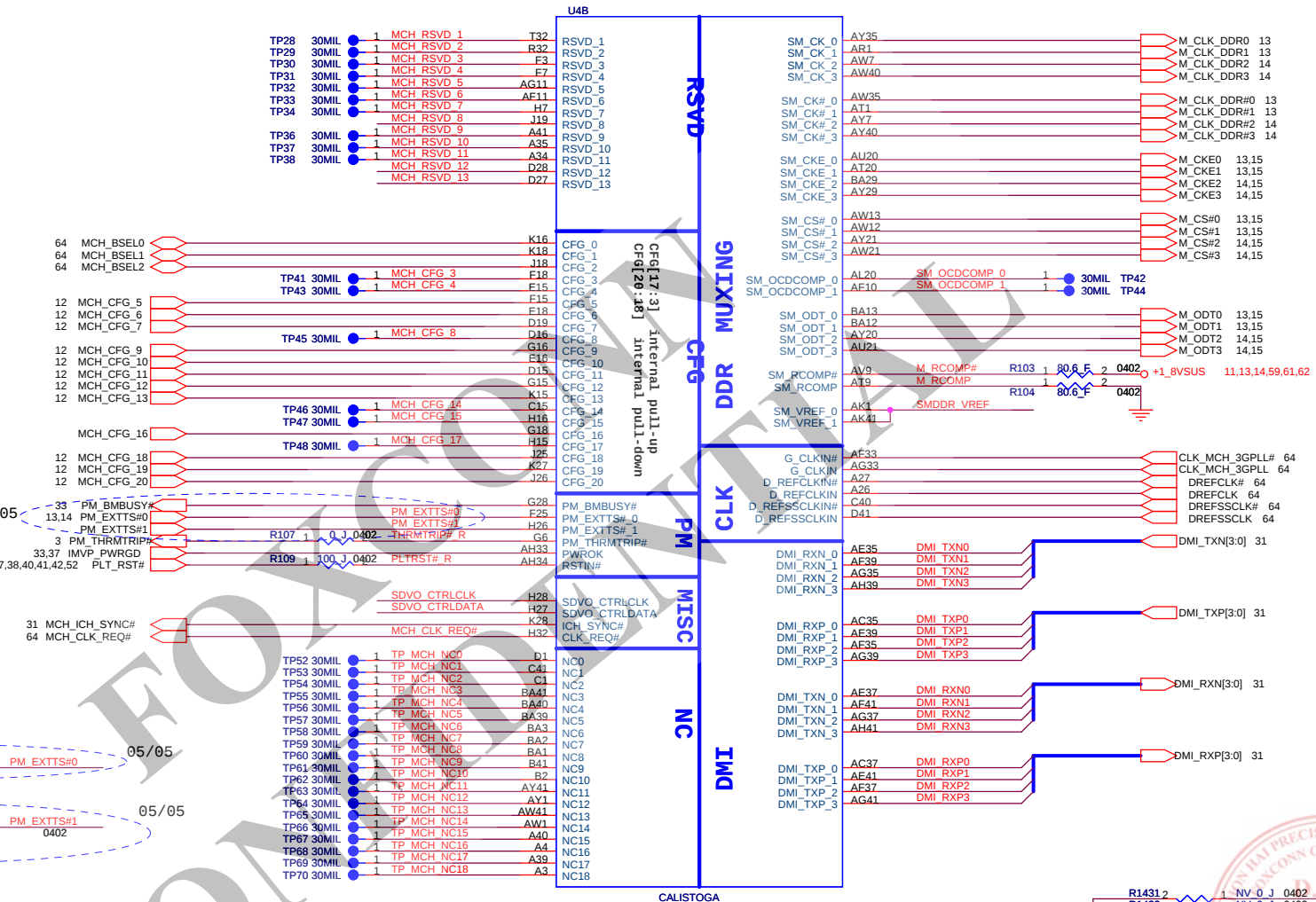


HOST

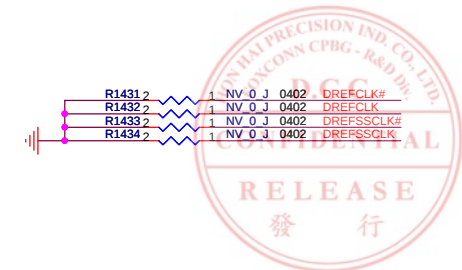


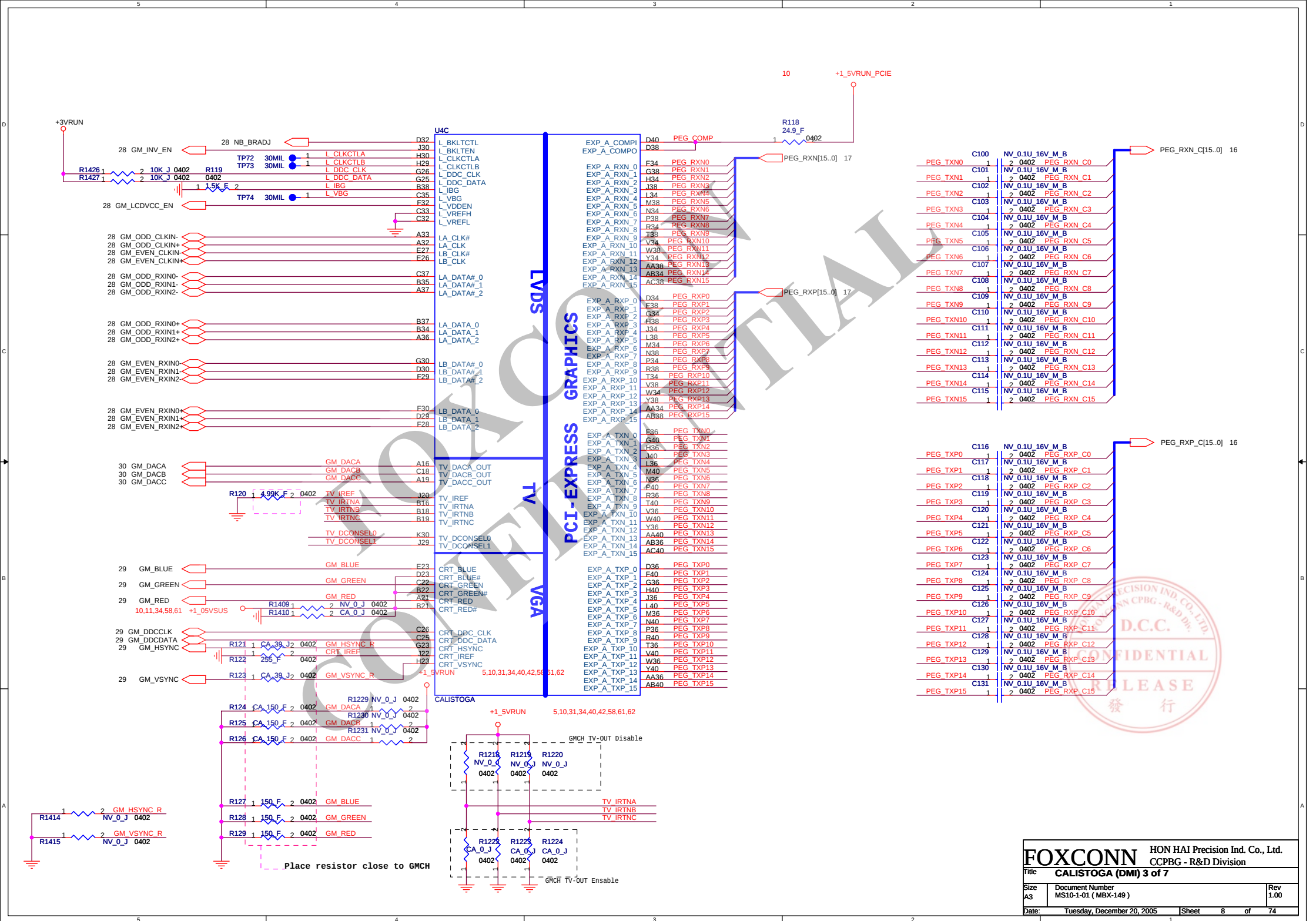


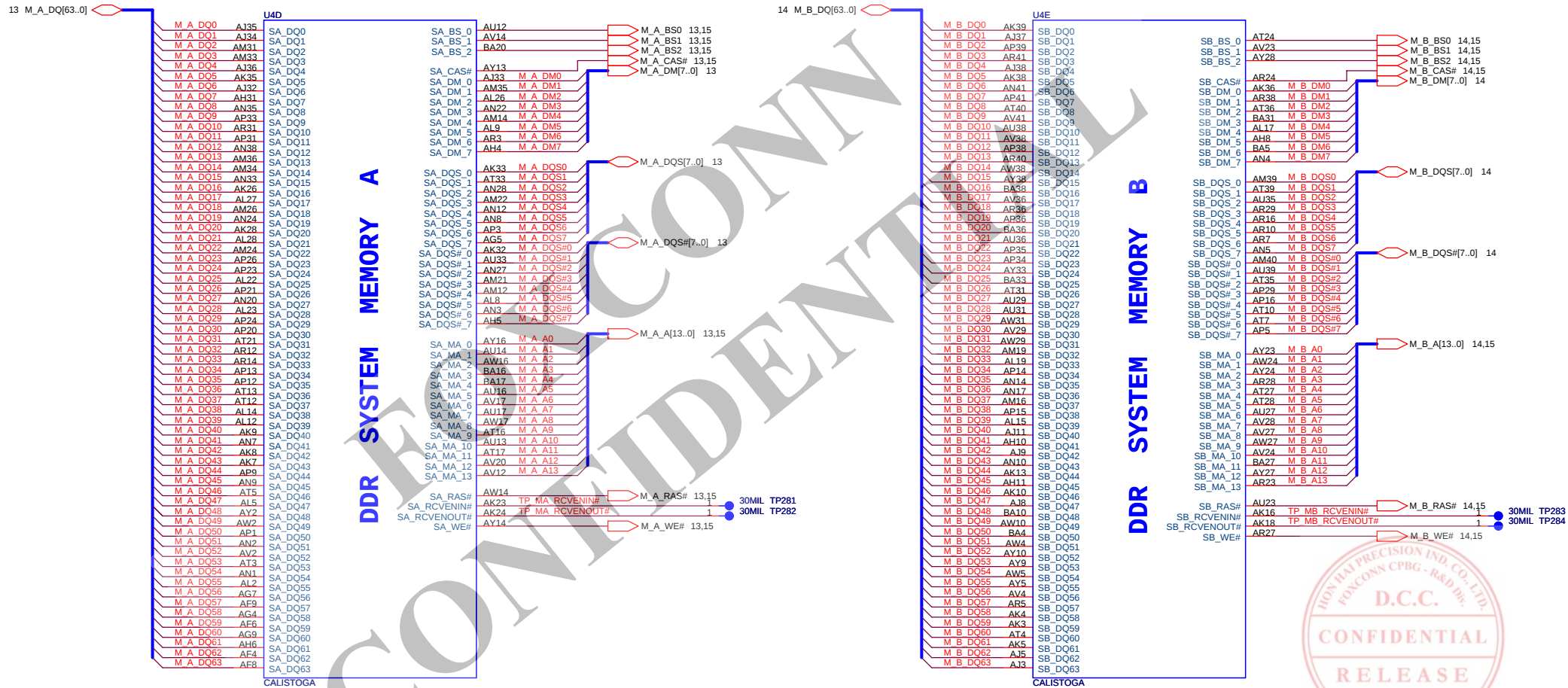
CRB rev:1.301 update

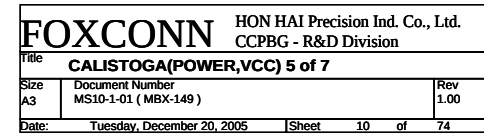


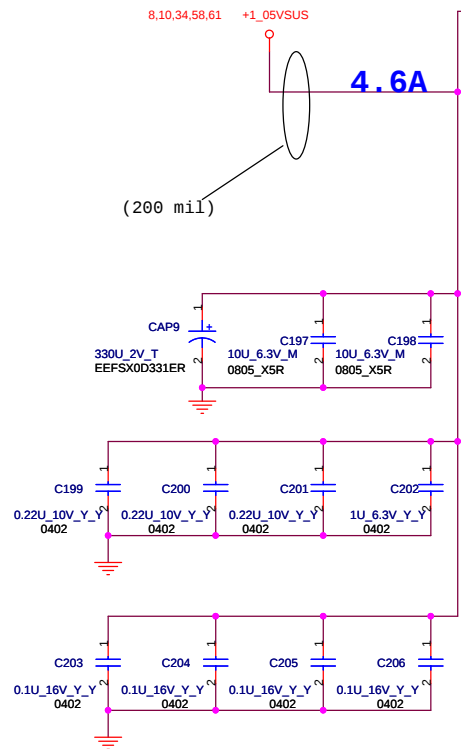
5/26 after EVT check, DVT delete





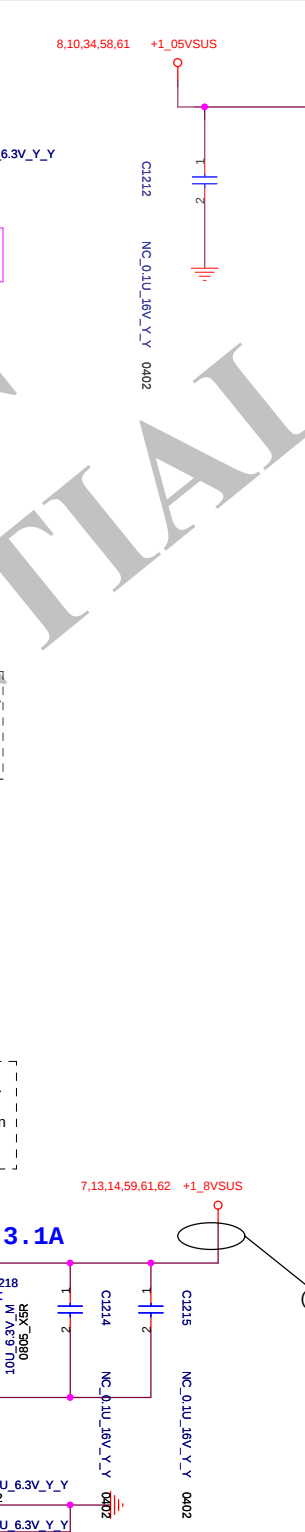
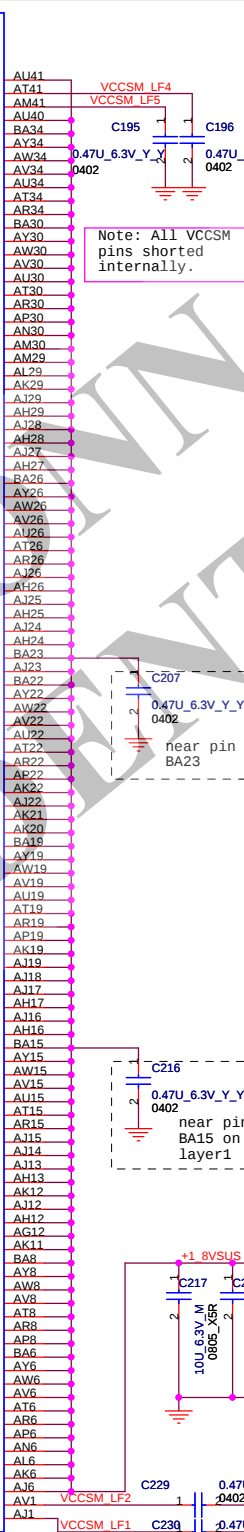






AA33 VCC_0
W33 VCC_1
P33 VCC_2
L33 VCC_3
J33 VCC_4
AA32 VCC_5
Y32 VCC_6
Y32 VCC_7
Y32 VCC_8
P32 VCC_9
N32 VCC_10
M32 VCC_11
L32 VCC_12
J32 VCC_13
J32 VCC_14
AA31 VCC_15
W31 VCC_16
V31 VCC_17
T31 VCC_18
R31 VCC_19
P31 VCC_20
N31 VCC_21
M31 VCC_22
W30 VCC_23
V30 VCC_24
U30 VCC_25
T30 VCC_26
R30 VCC_27
P30 VCC_28
N30 VCC_29
M30 VCC_30
L30 VCC_31
J30 VCC_32
J30 VCC_33
AA29 VCC_34
Y29 VCC_35
Y29 VCC_36
Y29 VCC_37
U29 VCC_38
R29 VCC_39
P29 VCC_40
M29 VCC_41
L29 VCC_42
J29 VCC_43
AA28 VCC_44
Y28 VCC_45
Y28 VCC_46
Y28 VCC_47
U28 VCC_48
R28 VCC_49
P28 VCC_50
M28 VCC_51
L28 VCC_52
J28 VCC_53
J28 VCC_54
AA27 VCC_55
Y27 VCC_56
Y27 VCC_57
Y27 VCC_58
U27 VCC_59
R27 VCC_60
P27 VCC_61
M27 VCC_62
L27 VCC_63
J27 VCC_64
J27 VCC_65
AA26 VCC_66
Y26 VCC_67
Y26 VCC_68
Y26 VCC_69
U26 VCC_70
R26 VCC_71
P26 VCC_72
M26 VCC_73
L26 VCC_74
J26 VCC_75
J26 VCC_76
AA25 VCC_77
Y25 VCC_78
Y25 VCC_79
Y25 VCC_80
U25 VCC_81
R25 VCC_82
P25 VCC_83
M25 VCC_84
L25 VCC_85
J25 VCC_86
J25 VCC_87
AA24 VCC_88
Y24 VCC_89
Y24 VCC_90
Y24 VCC_91
U24 VCC_92
R24 VCC_93
P24 VCC_94
M24 VCC_95
L24 VCC_96
J24 VCC_97
J24 VCC_98
AA23 VCC_99
Y23 VCC_100
Y23 VCC_101
Y23 VCC_102
U23 VCC_103
R23 VCC_104
P23 VCC_105
M23 VCC_106
L23 VCC_107
J23 VCC_108
J23 VCC_109
AA22 VCC_110

VCC_0
VCC_1
VCC_2
VCC_3
VCC_4
VCC_5
VCC_6
VCC_7
VCC_8
VCC_9
VCC_10
VCC_11
VCC_12
VCC_13
VCC_14
VCC_15
VCC_16
VCC_17
VCC_18
VCC_19
VCC_20
VCC_21
VCC_22
VCC_23
VCC_24
VCC_25
VCC_26
VCC_27
VCC_28
VCC_29
VCC_30
VCC_31
VCC_32
VCC_33
VCC_34
VCC_35
VCC_36
VCC_37
VCC_38
VCC_39
VCC_40
VCC_41
VCC_42
VCC_43
VCC_44
VCC_45
VCC_46
VCC_47
VCC_48
VCC_49
VCC_50
VCC_51
VCC_52
VCC_53
VCC_54
VCC_55
VCC_56
VCC_57
VCC_58
VCC_59
VCC_60
VCC_61
VCC_62
VCC_63
VCC_64
VCC_65
VCC_66
VCC_67
VCC_68
VCC_69
VCC_70
VCC_71
VCC_72
VCC_73
VCC_74
VCC_75
VCC_76
VCC_77
VCC_78
VCC_79
VCC_80
VCC_81
VCC_82
VCC_83
VCC_84
VCC_85
VCC_86
VCC_87
VCC_88
VCC_89
VCC_90
VCC_91
VCC_92
VCC_93
VCC_94
VCC_95
VCC_96
VCC_97
VCC_98
VCC_99
VCC_100
VCC_101
VCC_102
VCC_103
VCC_104
VCC_105
VCC_106
VCC_107



VCC_NCTF0
VCC_NCTF1
VCC_NCTF2
VCC_NCTF3
VCC_NCTF4
VCC_NCTF5
VCC_NCTF6
VCC_NCTF7
VCC_NCTF8
VCC_NCTF9
VCC_NCTF10
VCC_NCTF11
VCC_NCTF12
VCC_NCTF13
VCC_NCTF14
VCC_NCTF15
VCC_NCTF16
VCC_NCTF17
VCC_NCTF18
VCC_NCTF19
VCC_NCTF20
VCC_NCTF21
VCC_NCTF22
VCC_NCTF23
VCC_NCTF24
VCC_NCTF25
VCC_NCTF26
VCC_NCTF27
VCC_NCTF28
VCC_NCTF29
VCC_NCTF30
VCC_NCTF31
VCC_NCTF32
VCC_NCTF33
VCC_NCTF34
VCC_NCTF35
VCC_NCTF36
VCC_NCTF37
VCC_NCTF38
VCC_NCTF39
VCC_NCTF40
VCC_NCTF41
VCC_NCTF42
VCC_NCTF43
VCC_NCTF44
VCC_NCTF45
VCC_NCTF46
VCC_NCTF47
VCC_NCTF48
VCC_NCTF49
VCC_NCTF50
VCC_NCTF51
VCC_NCTF52
VCC_NCTF53
VCC_NCTF54
VCC_NCTF55
VCC_NCTF56
VCC_NCTF57

VSS_NCTF0
VSS_NCTF1
VSS_NCTF2
VSS_NCTF3
VSS_NCTF4
VSS_NCTF5
VSS_NCTF6
VSS_NCTF7
VSS_NCTF8
VSS_NCTF9
VSS_NCTF10
VSS_NCTF11
VSS_NCTF12
VSS_NCTF13
VSS_NCTF14
VSS_NCTF15
VSS_NCTF16
VSS_NCTF17
VSS_NCTF18
VSS_NCTF19
VSS_NCTF20
VSS_NCTF21
VSS_NCTF22
VSS_NCTF23
VSS_NCTF24
VSS_NCTF25
VSS_NCTF26
VSS_NCTF27
VSS_NCTF28
VSS_NCTF29
VSS_NCTF30
VSS_NCTF31
VSS_NCTF32
VSS_NCTF33
VSS_NCTF34
VSS_NCTF35
VSS_NCTF36
VSS_NCTF37
VSS_NCTF38
VSS_NCTF39
VSS_NCTF40
VSS_NCTF41
VSS_NCTF42
VSS_NCTF43
VSS_NCTF44
VSS_NCTF45
VSS_NCTF46
VSS_NCTF47
VSS_NCTF48
VSS_NCTF49
VSS_NCTF50
VSS_NCTF51
VSS_NCTF52
VSS_NCTF53
VSS_NCTF54
VSS_NCTF55
VSS_NCTF56
VSS_NCTF57

7 MCH_CFG_5 30MIL TP554

MCH_CFG_5
Low = DMIX2
High = DMIX4

MCH_CFG_18
(VCC_CORE Select)
Low = 1.05V(default)
High = 1.5V

7 MCH_CFG_6 30MIL TP556

MCH_CFG_6
Low = Moby Dick
High = Calistoga
DDR2 select (default high)

7 MCH_CFG_7 30MIL TP557

MCH_CFG_7
(CPU Strap)
Low = RSVD
High = Mobile Yonah processor

MCH_CFG_19
(DMI LANE REVERSAL)
Low = Normal(default)
High = LANES REVERSED

7 MCH_CFG_9 30MIL TP559

MCH_CFG_9
(PCIe Graphics Lane)
Low = Reverse Lane
High = Normal operation

MCH_CFG_20
(PCIe Backward Interoperability mode)
Low = Only SDVO or PCIe x1 is operational (defaults)
High = SDVO and PCIe x1 are operating simultaneously via the PEG port

For layout convenience

7 MCH_CFG_10 30MIL TP560

MCH_CFG_10
(HOST PLL VCC SELECT)
Low = RESERVED
High = MOBILITY

7 MCH_CFG_11 30MIL TP561

MCH_CFG_11
(PSB 4x CLK ENABLE)
Low = Calistoga
High = Reserved

Layout Noe:
Location of all MCH_CFG strap resistors needs to be close to trace to minimize stub

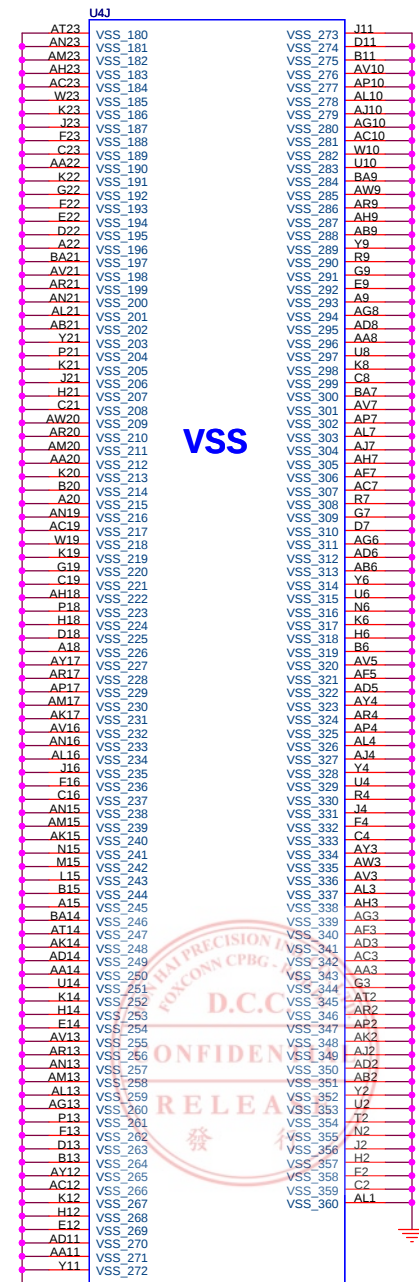
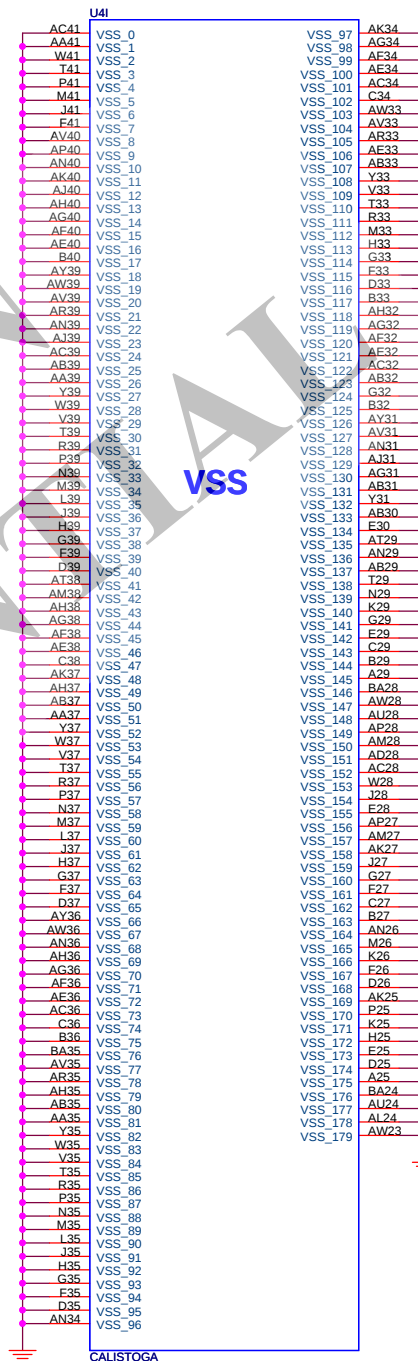
7 MCH_CFG_12 30MIL TP562

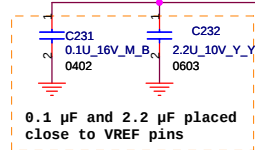
7 MCH_CFG_13 30MIL TP563

MCH_CFG [13:12]
(XOR/ALLZ)
00=Partial Clock Gating Disable
01=XOR Mode Enable
10=All-Z Mode Enable
11=Normal Operation(Default)

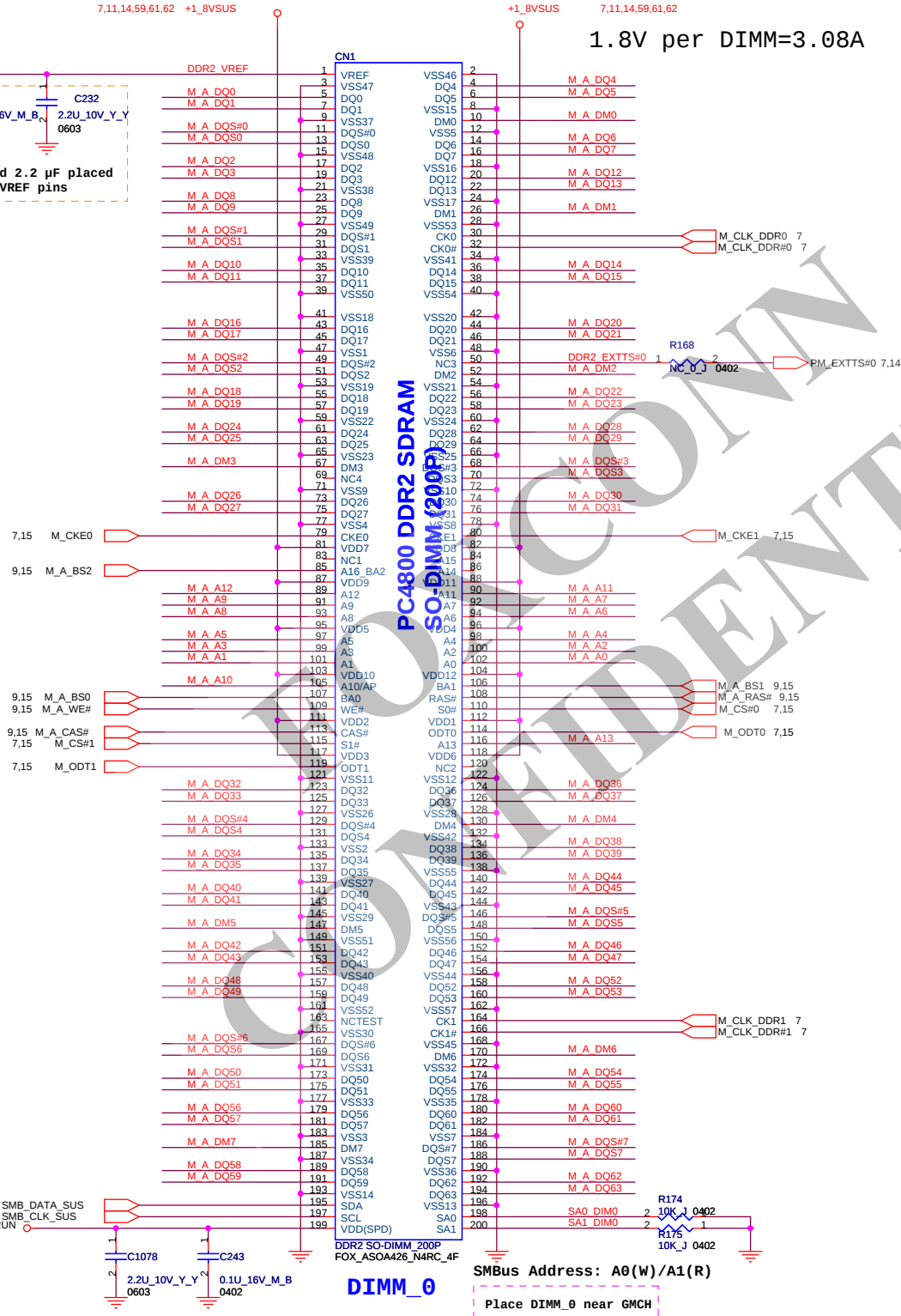
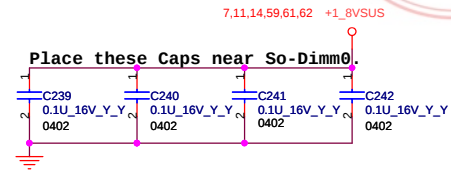
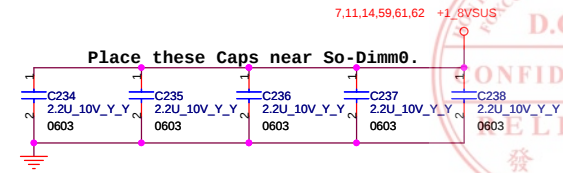
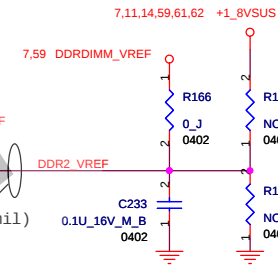
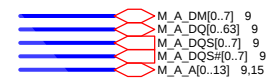
7 MCH_CFG_16

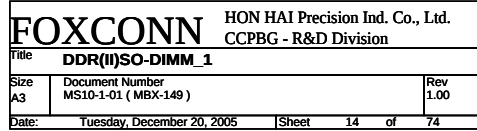
MCH_CFG_16
(FSB Dynamic ODT)
Low = Dynamic ODT Disabled
High = Dynamic ODT Enable





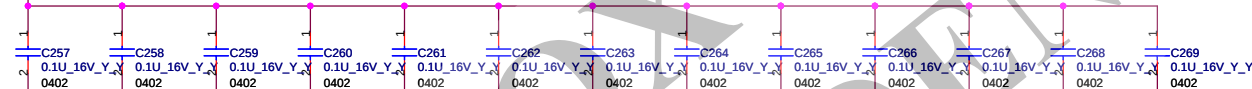
1.8V per DIMM=3.08A





59,62

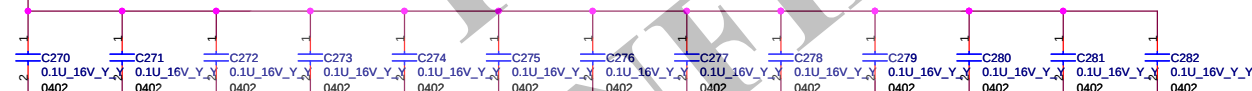
+0_9VSUS



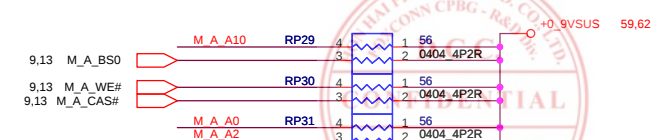
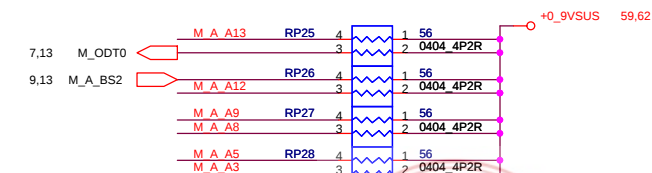
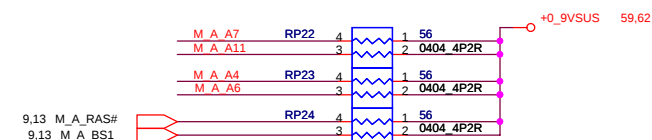
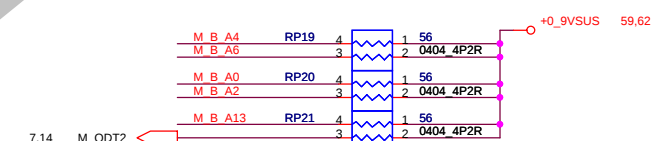
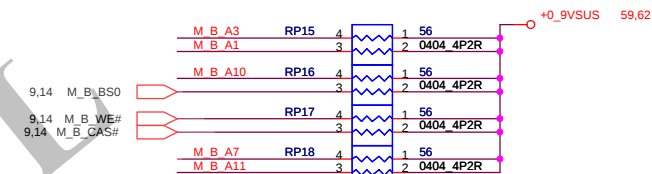
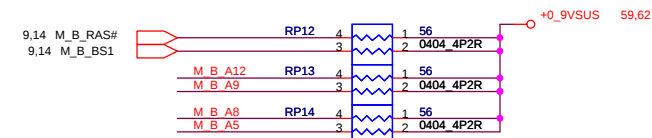
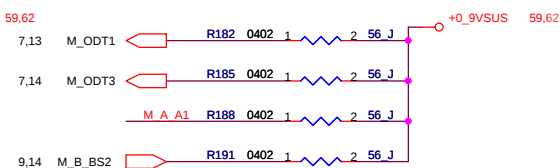
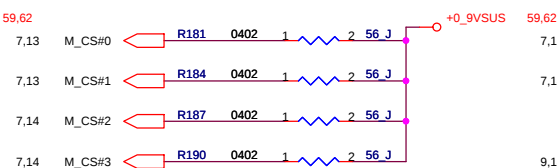
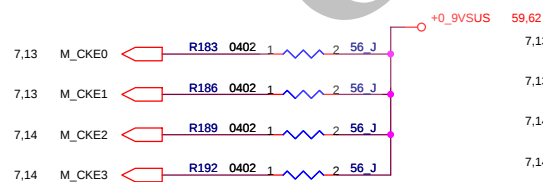
Layout note: Place 1 cap close to every 1 R-pack terminated to +0_9VSUS

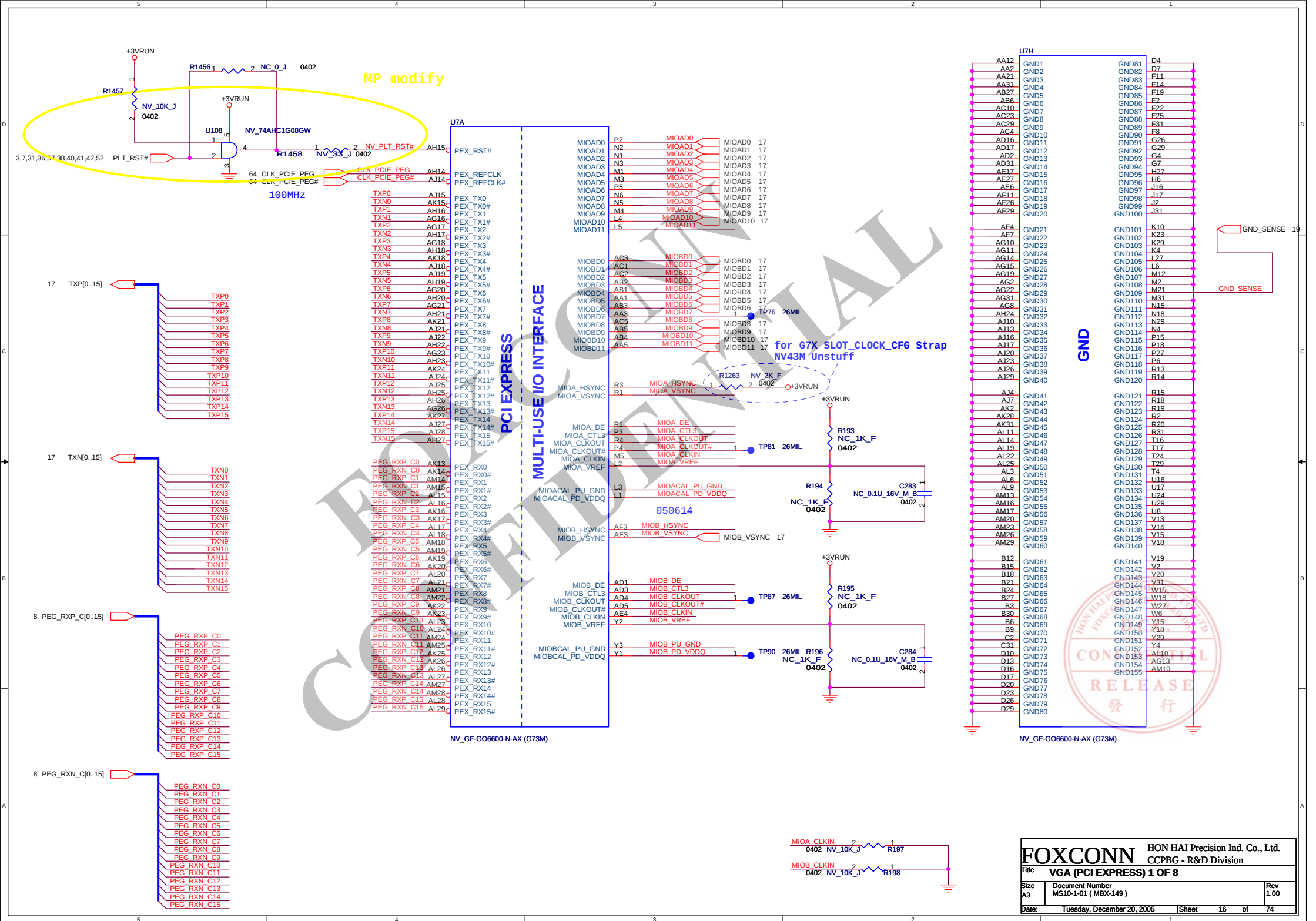
59,62

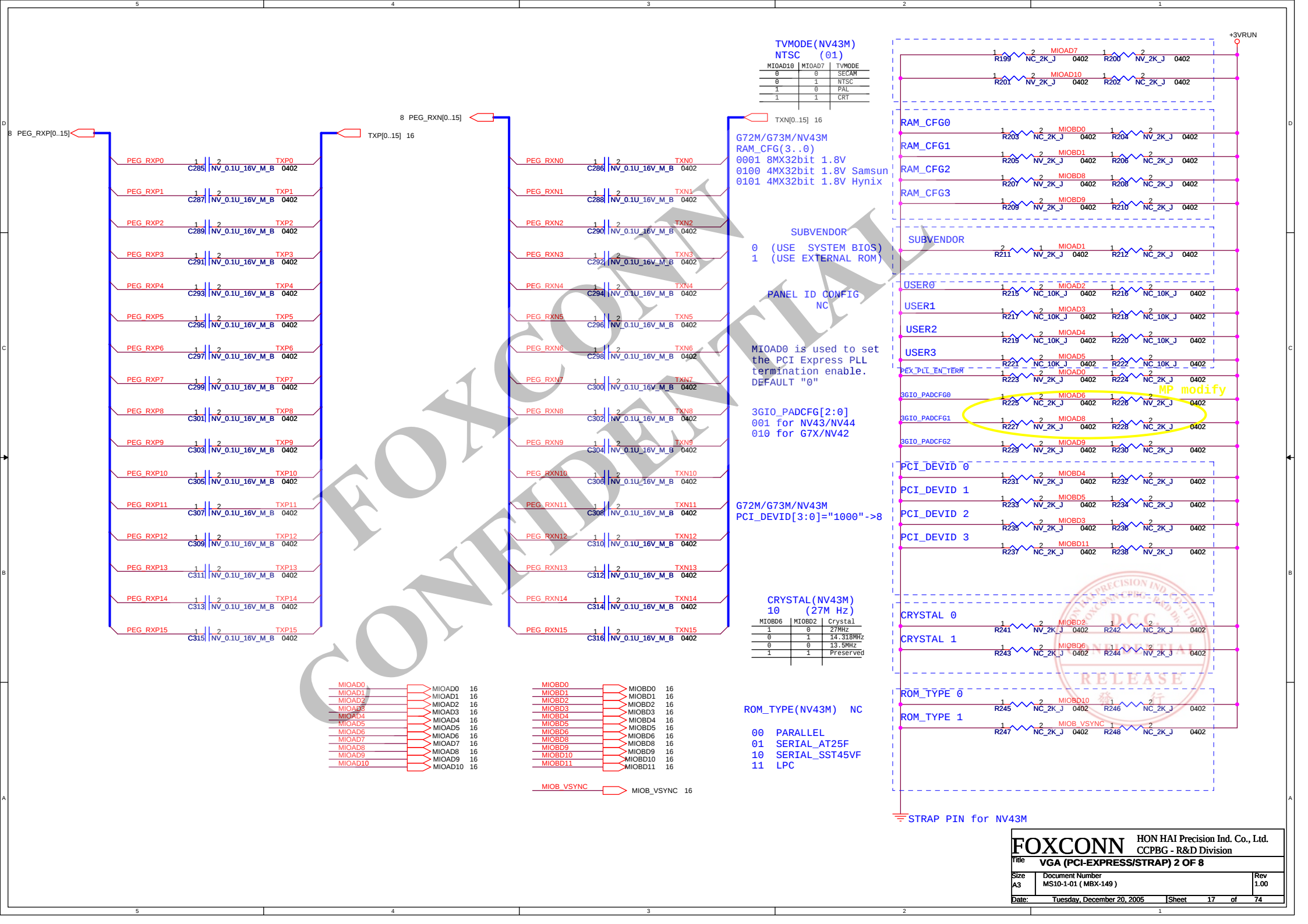
+0_9VSUS



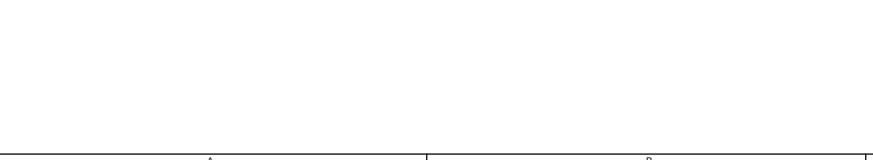
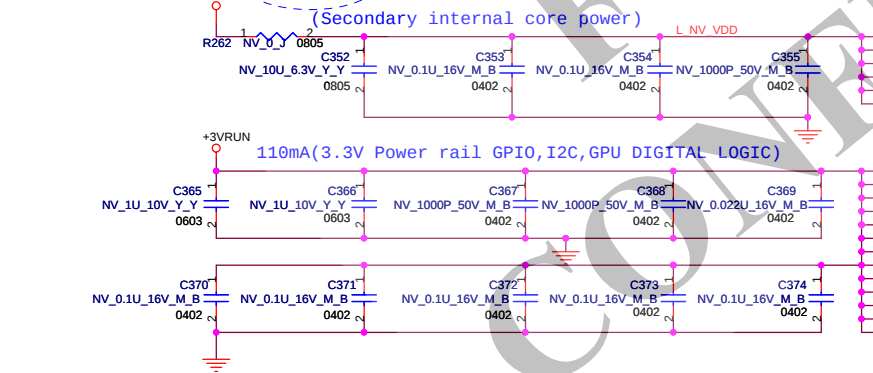
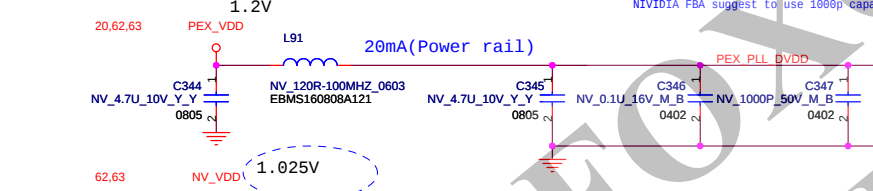
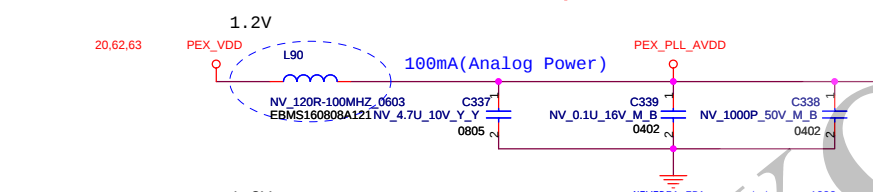
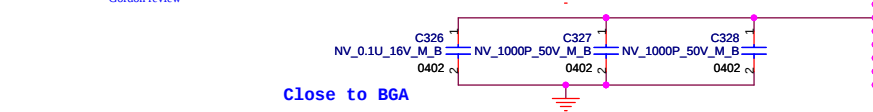
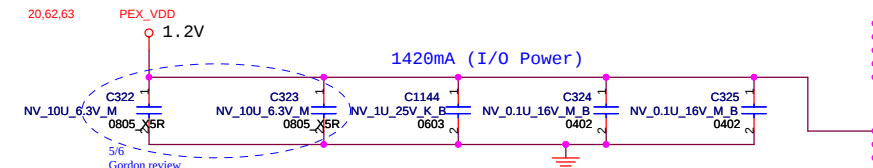
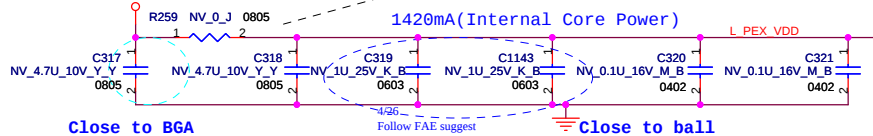
Layout note: Place 1 cap close to every 1 R-pack terminated to +0_9VSUS



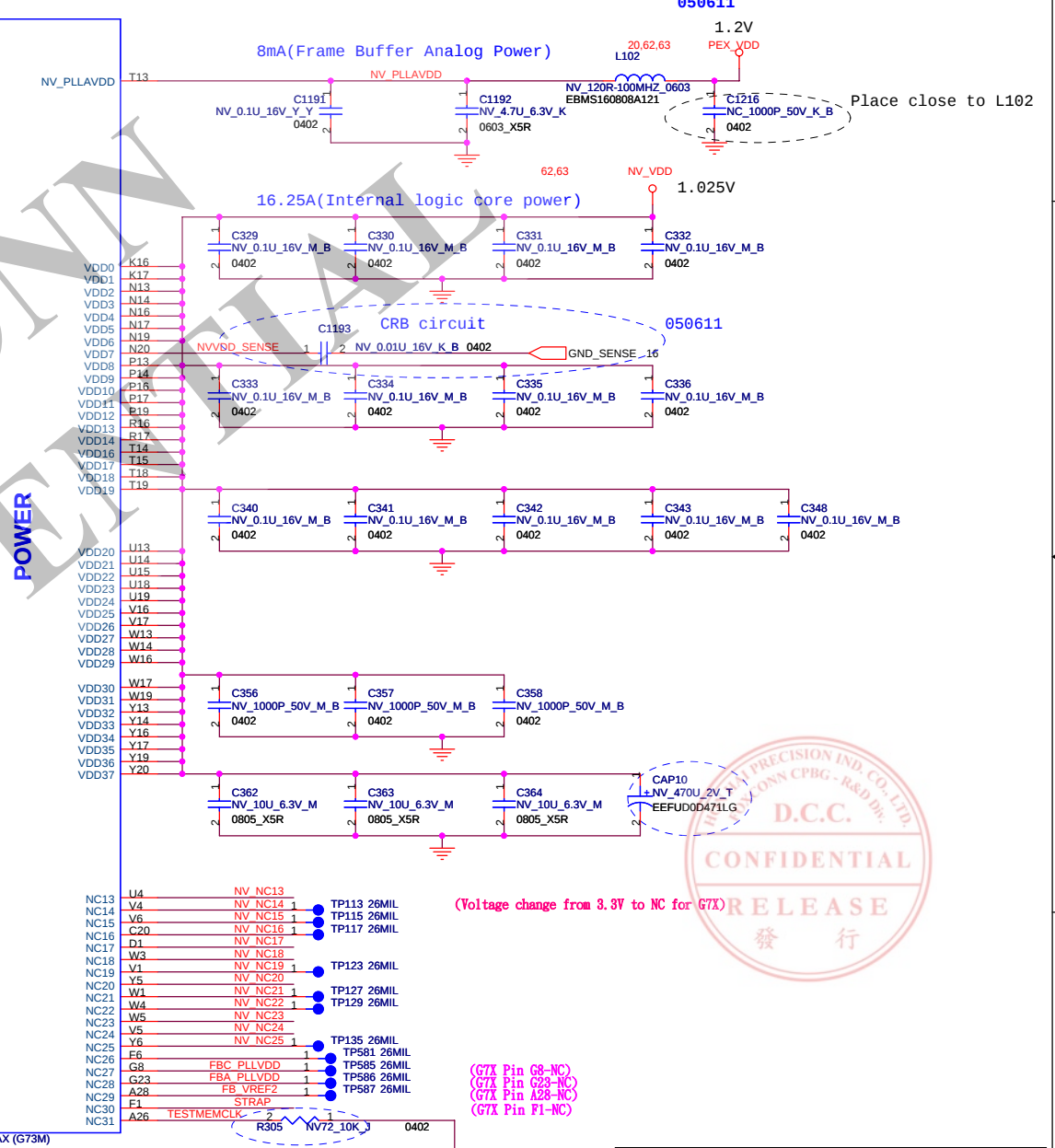




1.2V
20.62,63 PEX_VDD don't use inductor or bead for nvidia's experience. inductor can not make current change immediately



- POWER
- AD23 PEX_IOVDD0
 - AE24 PEX_IOVDD1
 - AE23 PEX_IOVDD2
 - AG24 PEX_IOVDD3
 - AG25 PEX_IOVDD4
 - AE22 PEX_IOVDD5
 - AC16 PEX_IOVDDQ0
 - AC17 PEX_IOVDDQ1
 - AC21 PEX_IOVDDQ2
 - AC22 PEX_IOVDDQ3
 - AE18 PEX_IOVDDQ4
 - AE22 PEX_IOVDDQ5
 - AE12 PEX_IOVDDQ6
 - AE18 PEX_IOVDDQ7
 - AE21 PEX_IOVDDQ8
 - AE22 PEX_IOVDDQ9
 - AE22 PEX_IOVDDQ10
 - AE15 PEX_PLAVDD
 - AE15 PEX_PLLDVDD
 - AE16 PEX_PLIGND
 - P20 VDD_LP1
 - T20 VDD_LP2
 - U20 VDD_LP3
 - U23 VDD_LP4
 - W20 VDD_LP5
 - W20 VDD_LP6
 - VDD33_0
 - VDD33_1
 - VDD33_2
 - VDD33_3
 - VDD33_4
 - VDD33_5
 - VDD33_6
 - VDD33_7
 - VDD33_8
 - VDD33_9
 - VDD33_10
 - VDD33_11
 - VDD33_12
 - NC1
 - NC2
 - NC3
 - NC4
 - NC5
 - NC6
 - NC7
 - NC8
 - NC9
 - NC10
 - NC11
 - NC12
 - AG12
 - AH13
 - B32
 - AM9
 - AM8
 - Y30
 - AC26
 - U3
 - V3
 - U6
 - U5
 - NC13
 - NC14
 - NC15
 - NC16
 - NC17
 - NC18
 - NC19
 - NC20
 - NC21
 - NC22
 - NC23
 - NC24
 - NC25
 - NC26
 - NC27
 - NC28
 - NC29
 - NC30
 - NC31
 - NC32



NV_GF-G06600-N-AX (G73M)

G73M Pin A28-NC
G72M Pin A28 need stuff R305 10K

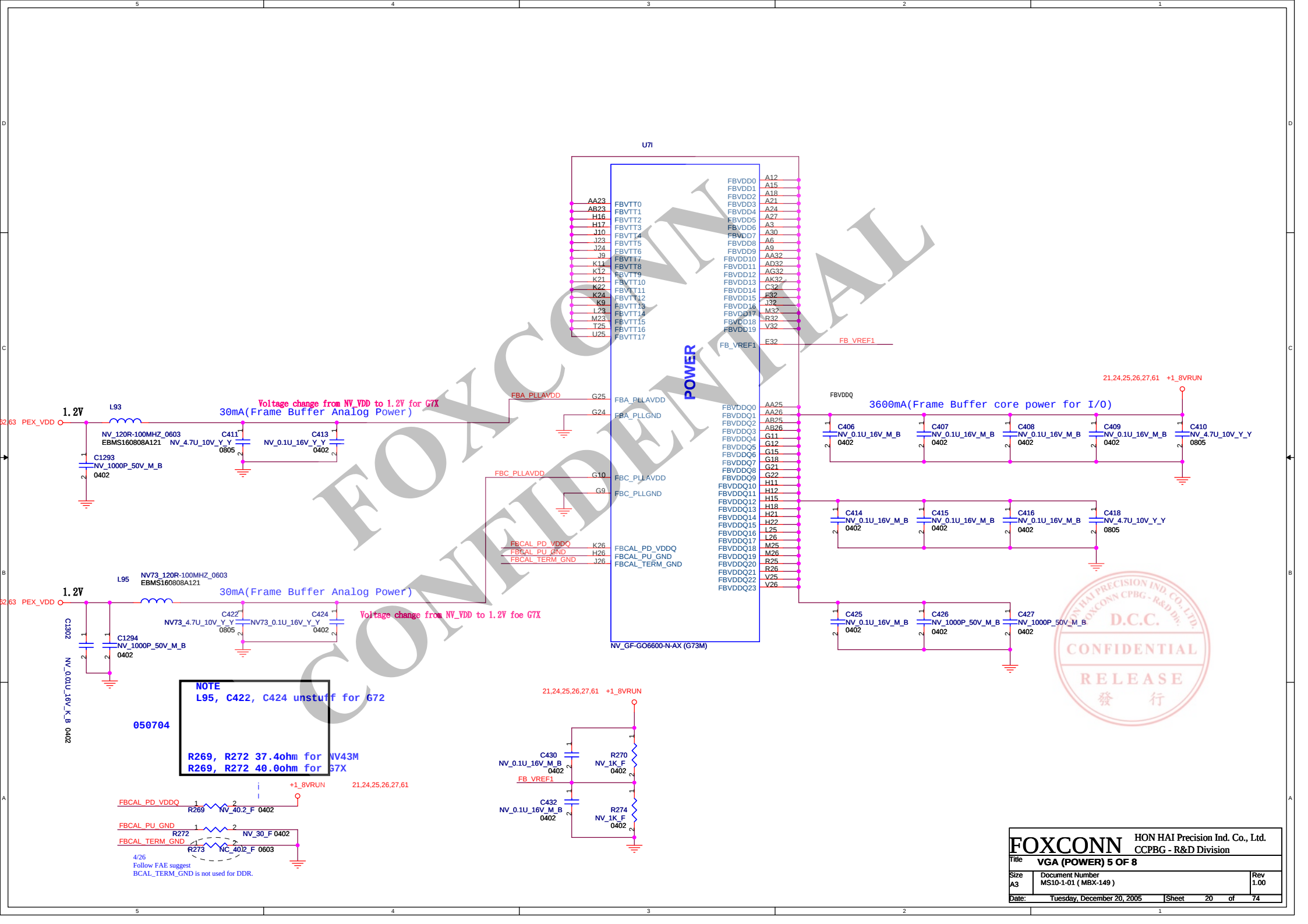
TP113 26MIL
TP115 26MIL
TP117 26MIL
TP123 26MIL
TP127 26MIL
TP129 26MIL
TP135 26MIL
TP581 26MIL
TP585 26MIL
TP586 26MIL
TP587 26MIL

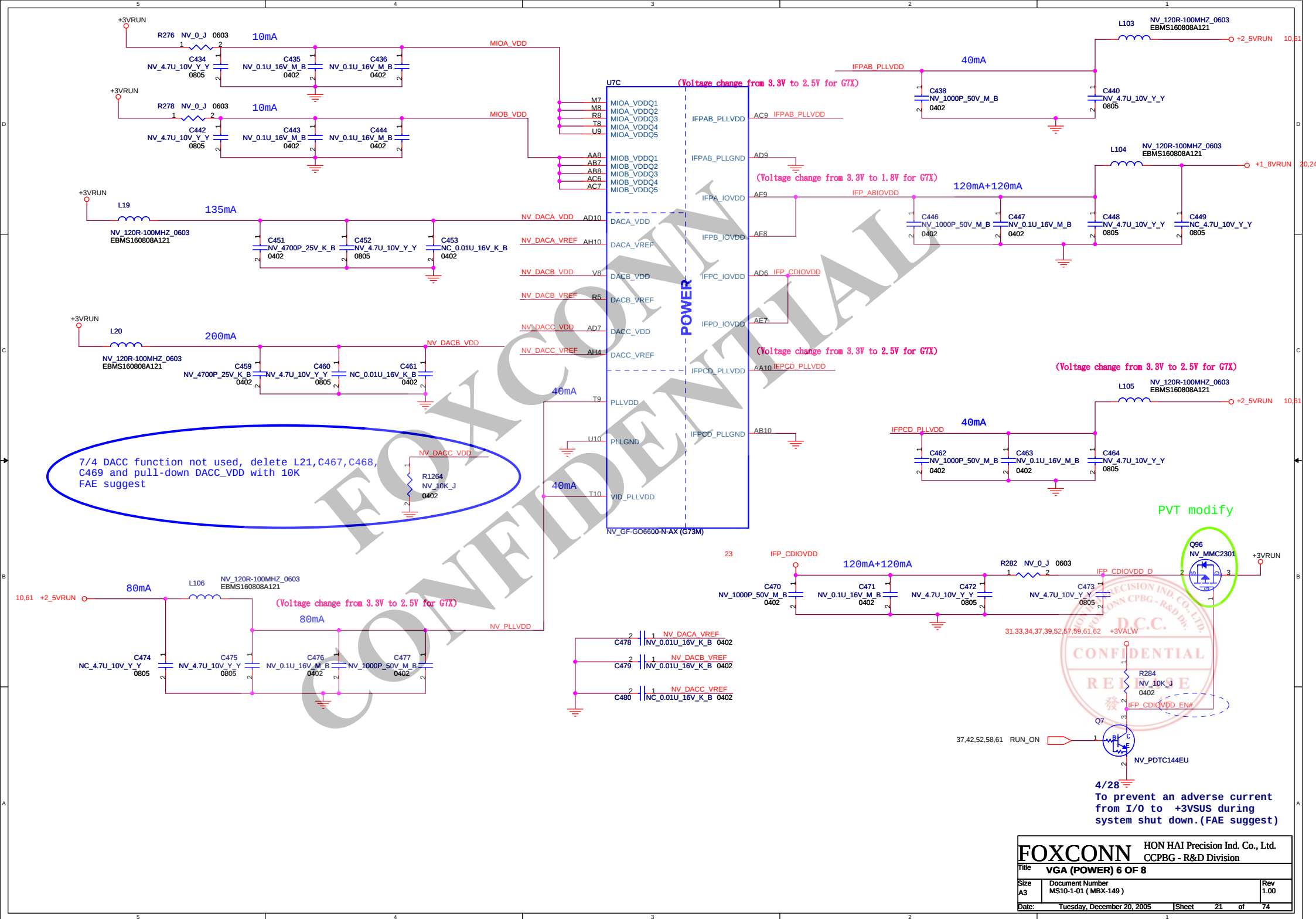
FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

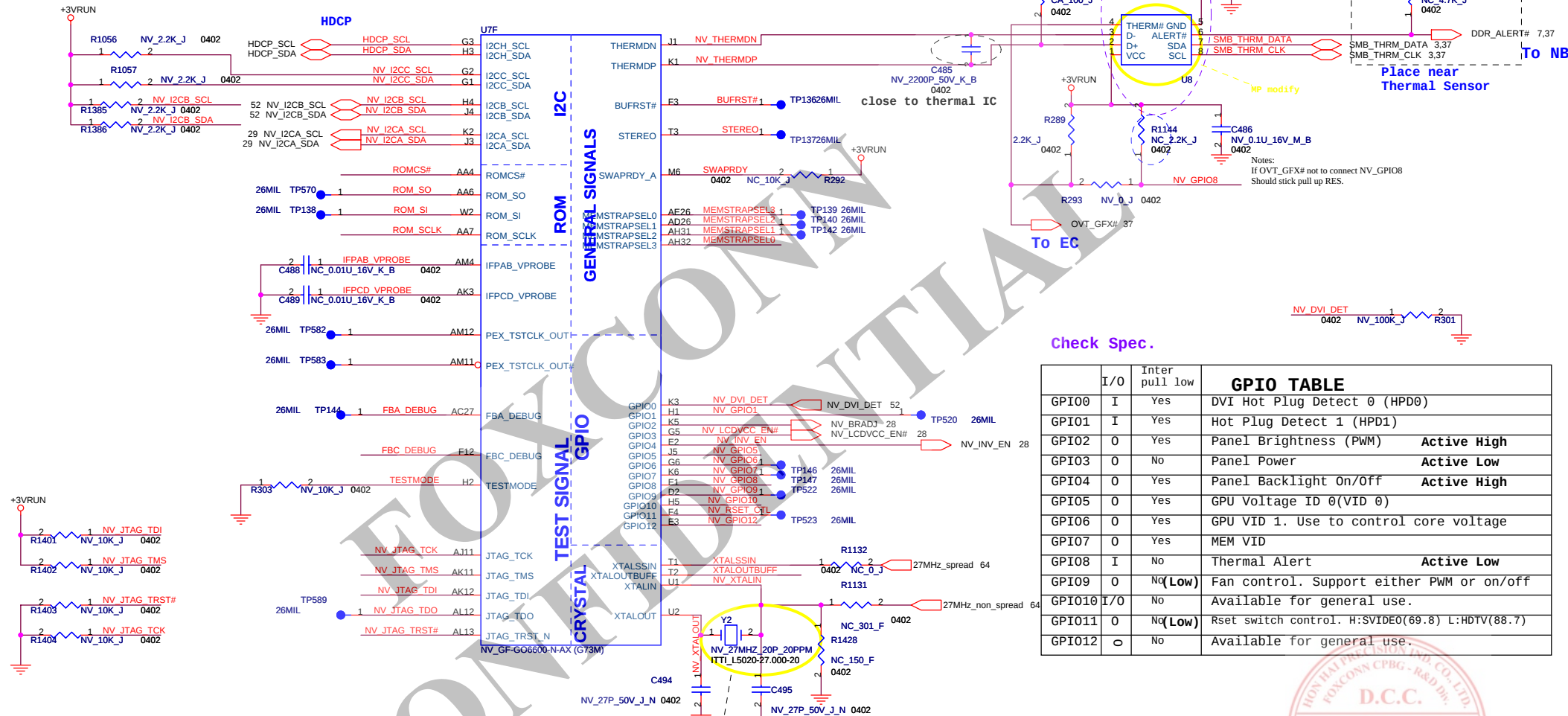
Title VGA (GDDR1/2C/ROM) 4 OF 8

Size A3 Document Number MS10-1-01 (MBX-149) Rev 1.00

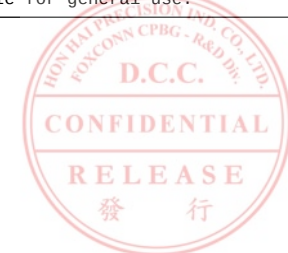
Date: Tuesday, December 20, 2005 Sheet 19 of 74



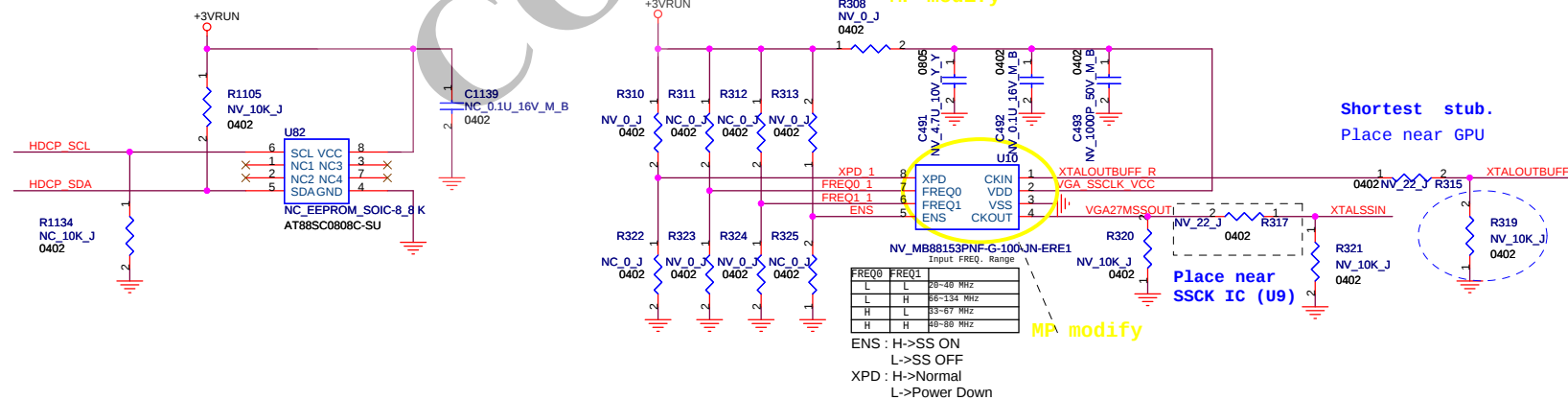




	I/O	Inter pull low	GPIO TABLE
GPIO0	I	Yes	DVI Hot Plug Detect 0 (HPD0)
GPIO1	I	Yes	Hot Plug Detect 1 (HPD1)
GPIO2	0	Yes	Panel Brightness (PWM) Active High
GPIO3	0	No	Panel Power Active Low
GPIO4	0	Yes	Panel Backlight On/Off Active High
GPIO5	0	Yes	GPU Voltage ID 0(VID 0)
GPIO6	0	Yes	GPU VID 1. Use to control core voltage
GPIO7	0	Yes	MEM VID
GPIO8	I	No	Thermal Alert Active Low
GPIO9	0	No(Low)	Fan control. Support either PWM or on/off
GPIO10	I/O	No	Available for general use.
GPIO11	0	No(Low)	Rset switch control. H:SVIDE0(69.8) L:HDTV(88.7)
GPIO12	0	No	Available for general use.



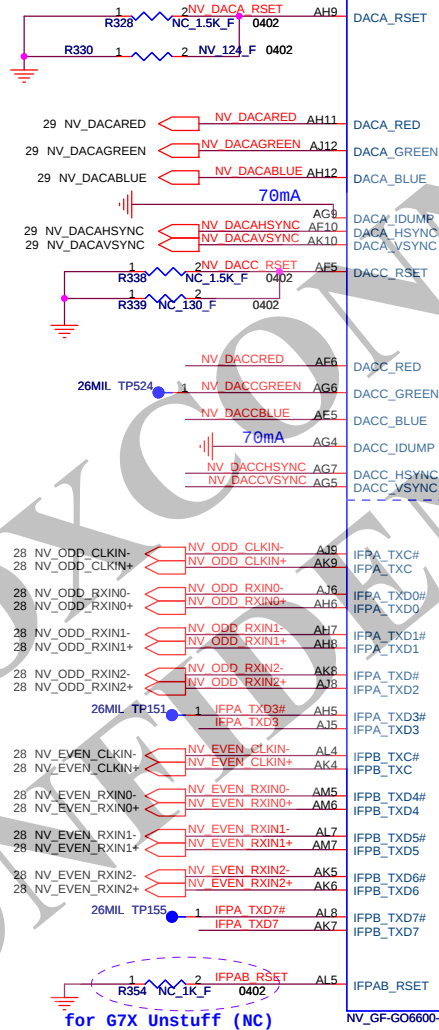
HDPC ROM



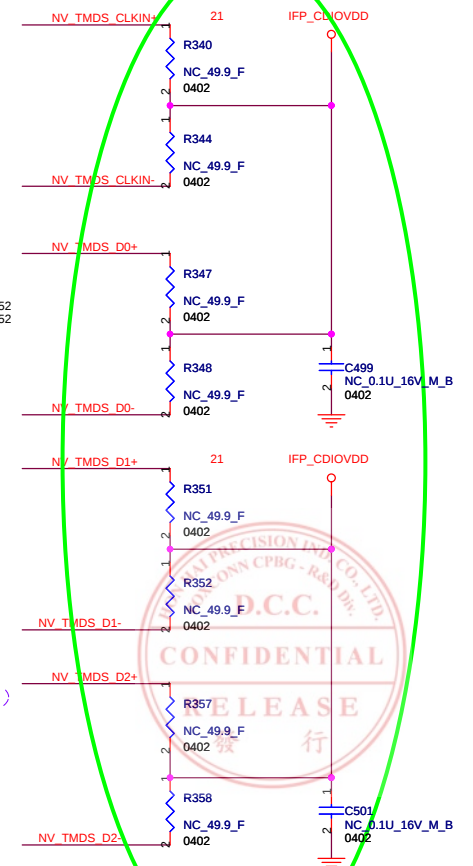
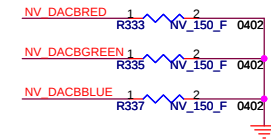
DACA	VGA-CRT			I2CA
DACA-RED	R			
DACA-GREEN	G			
DACA-BLUE	B			
DACA-HSYNC	HSYNC			
DACA-VSYNC	VSYNC			
	VGA-DBCLK			SCL
	VGA-DBDATA			SDA
DACB	S-VIDEO	COMPOSITE	D-CONNECTOR	I2CC
DACB-RED	C		PR	
DACB-GREEN	Y		Y	
DACB-BLUE		COMPOSITE		
			LINE1	SCL
			LINE2	SDA
			LINE3	
DACC	DVI-I			I2CB
DACC-RED	R			
DACC-GREEN	G			
DACC-BLUE	B			
DACC-HSYNC	HSYNC			
DACC-VSYNC	VSYNC			
	DVI-DBCLK			SCL
	DVI-DBDATA			SDA

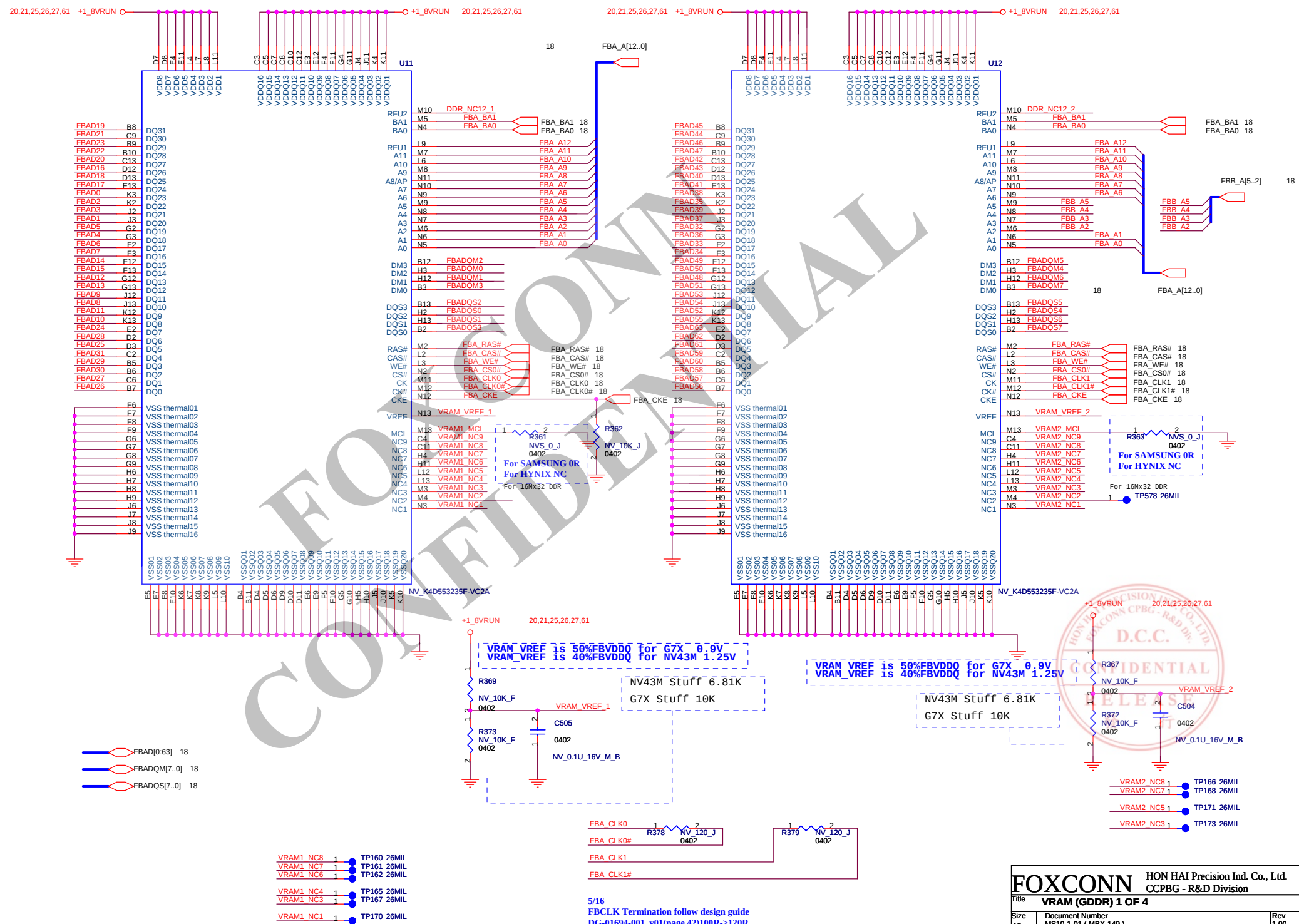
CLOSE TO GPU

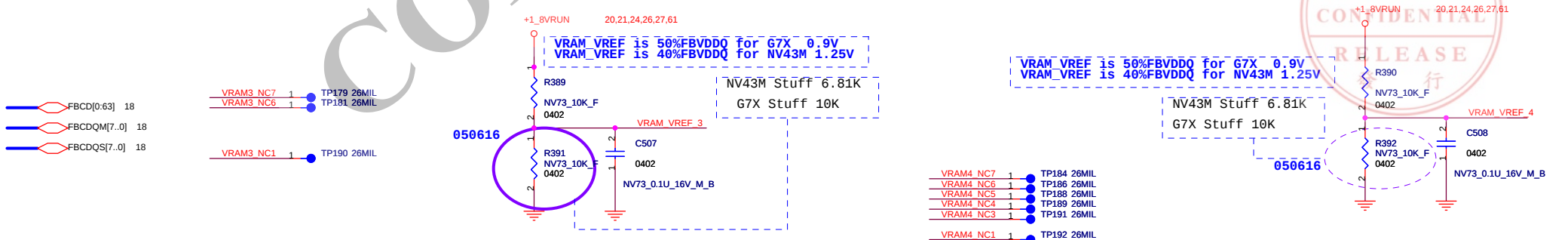
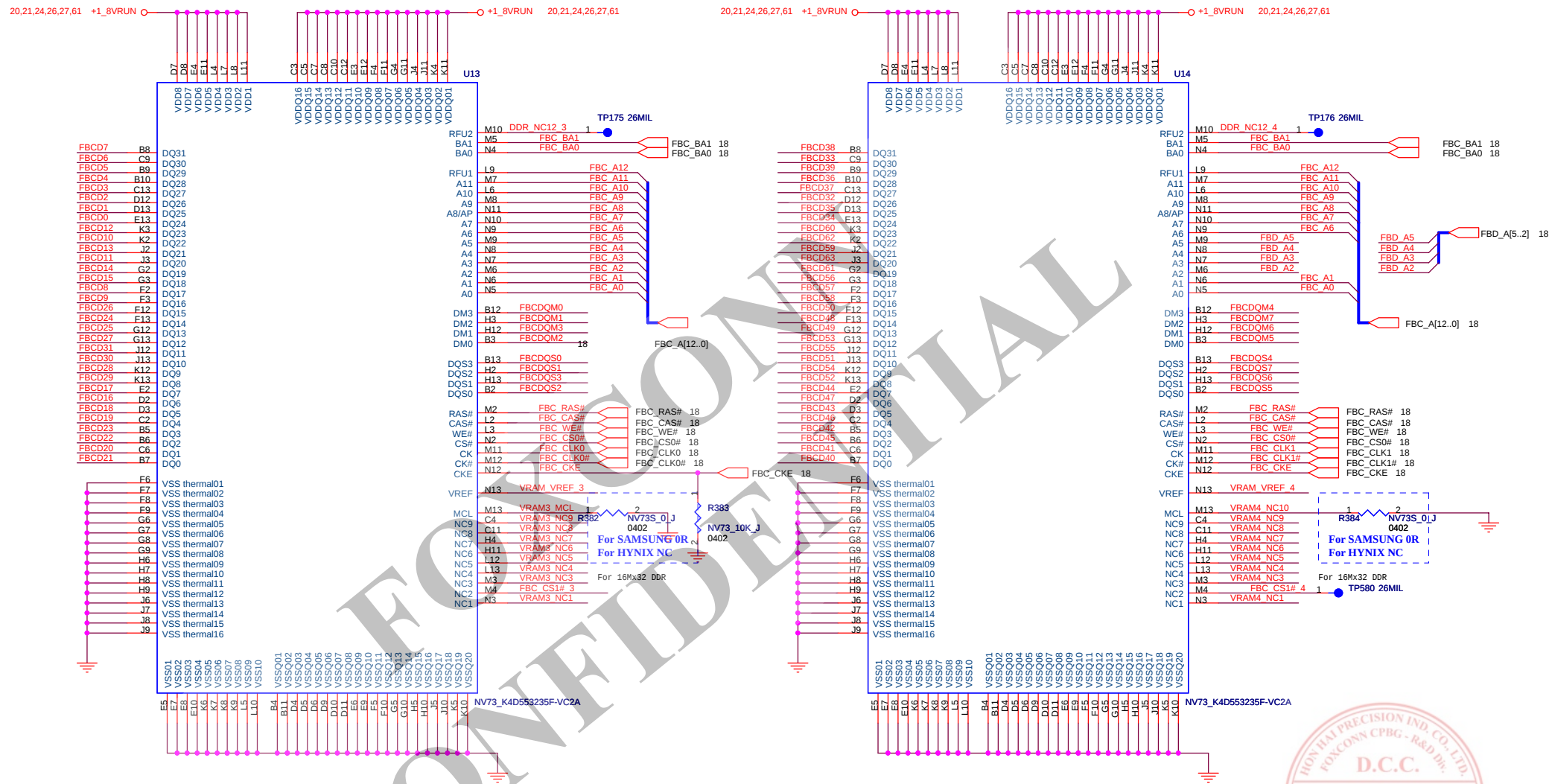
CLOSE TO GPU



CLOSE TO GPU

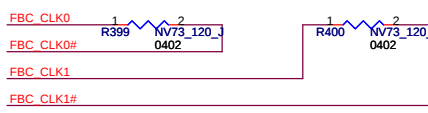






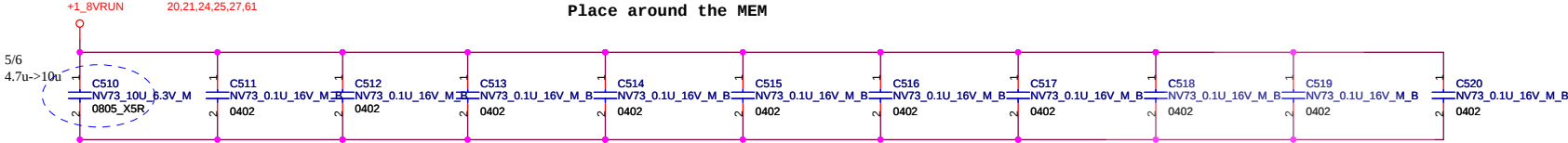
If use G72M, please unstuff U13, U14
and their related circuit

4/16
FBCLK Termination follow design guide
DG-01694-001_v01(page 42)100R->120R

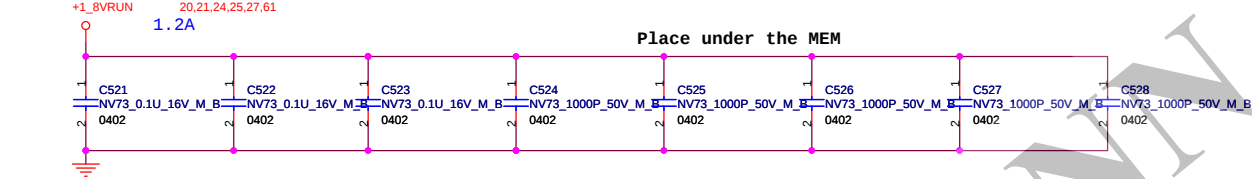


Decoupling for right MEMORY

Place around the MEM

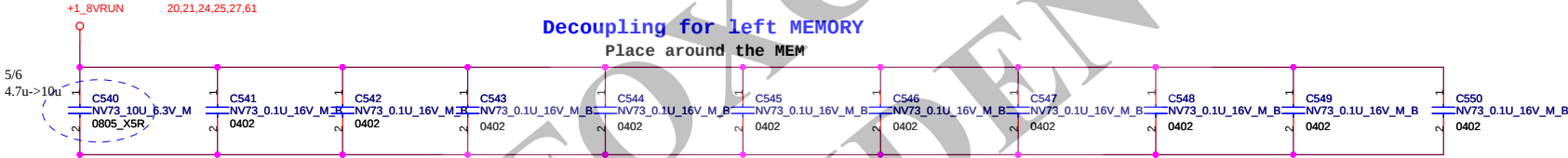


Place under the MEM

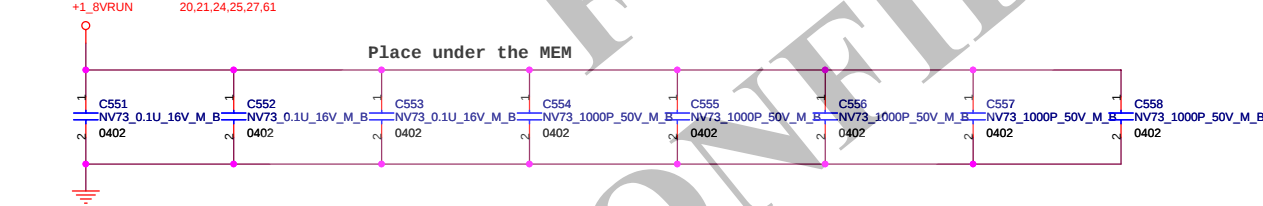


Decoupling for left MEMORY

Place around the MEM

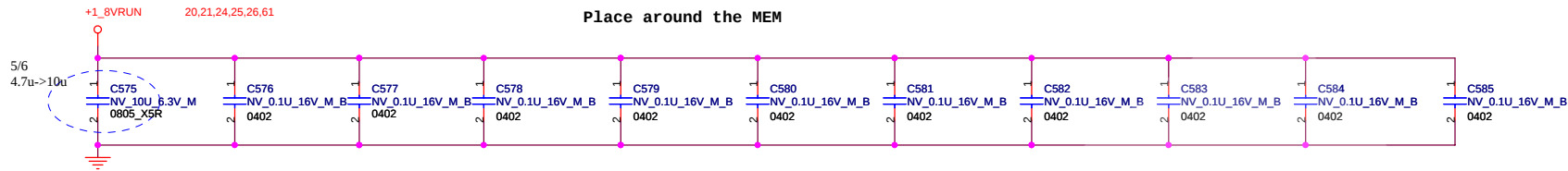


Place under the MEM

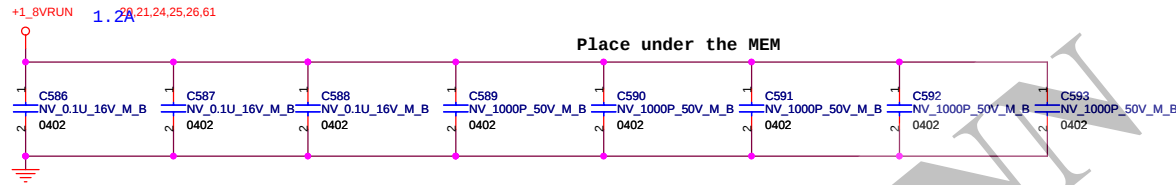


Decoupling for right MEMORY

Place around the MEM



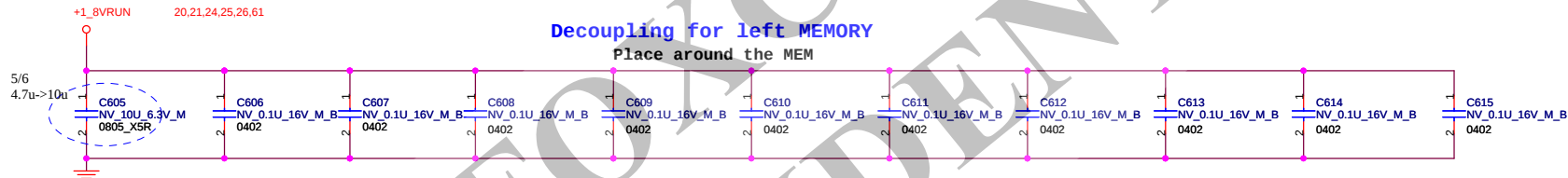
Place under the MEM



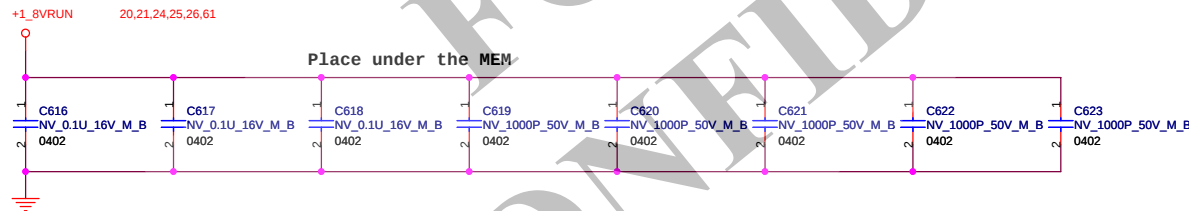
NO USE

Decoupling for left MEMORY

Place around the MEM

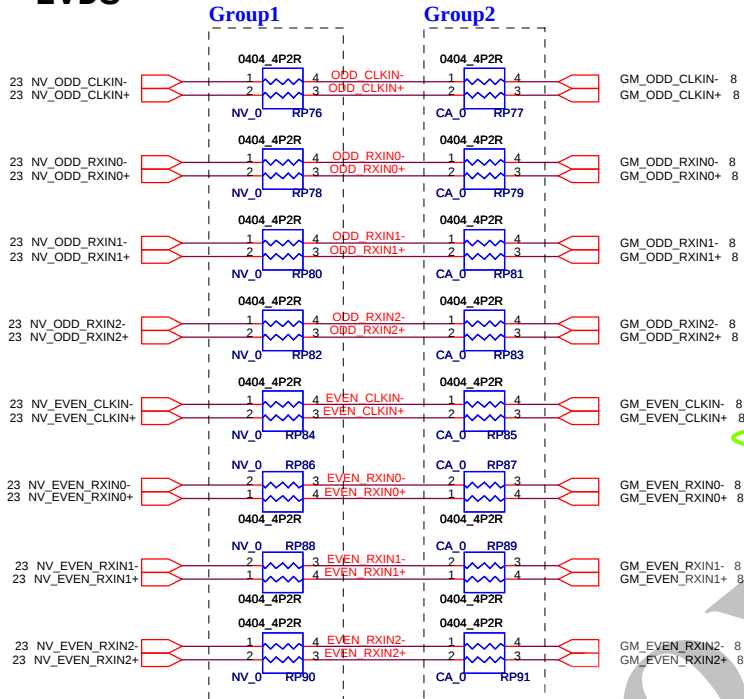


Place under the MEM

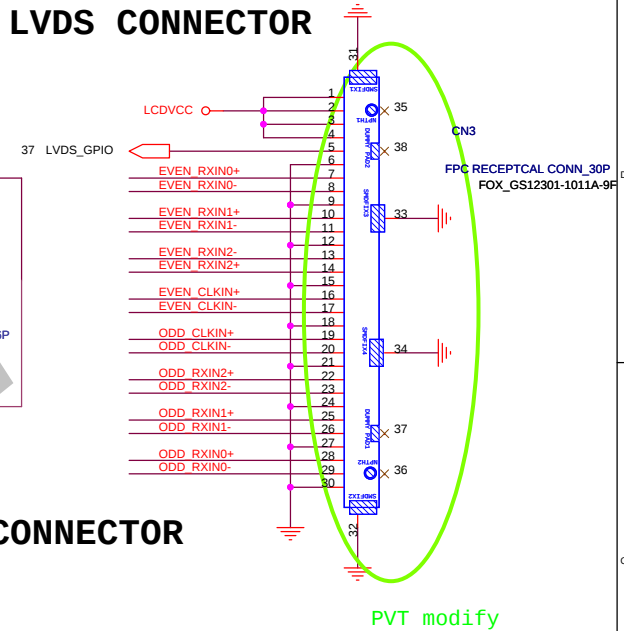


LVDS

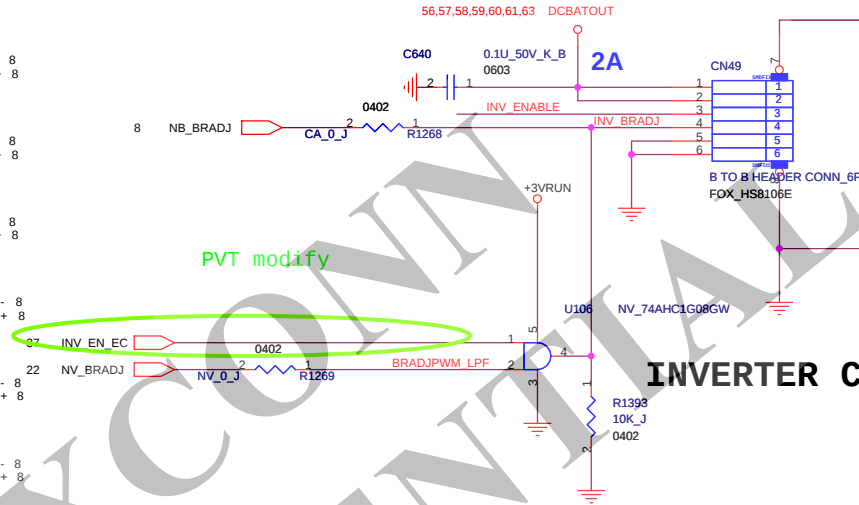
Group1,Group1 should be close



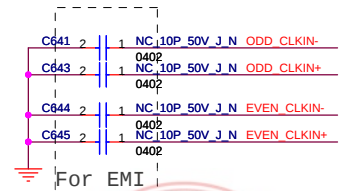
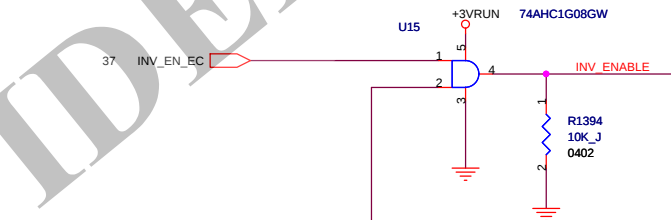
LVDS CONNECTOR



INVERTER CONNECTOR



PVT modify



PANEL ID



Type	WXGA	WXGA-HC	WSXGA+
Size	15.4" wide	15.4" wide	15.4" wide
Vender	Hitachi	Hitachi	Hitachi
Device Name	TX39D81VC1AAA	TX39D80VC1GAA	TX39D90VC1GAA
Panel ID Check[3...0]	1000	1000	1100

DISCHARGE

The R461 will consume about 0.054 Watt (3.3x3.3/200 = 0.054W). We changed resistor to 0603 size (1/8 Watt)

FOXCONN

HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title

LVDS

Size

MS10-1-01 (MBX-149)

Date:

Tuesday, December 20, 2005

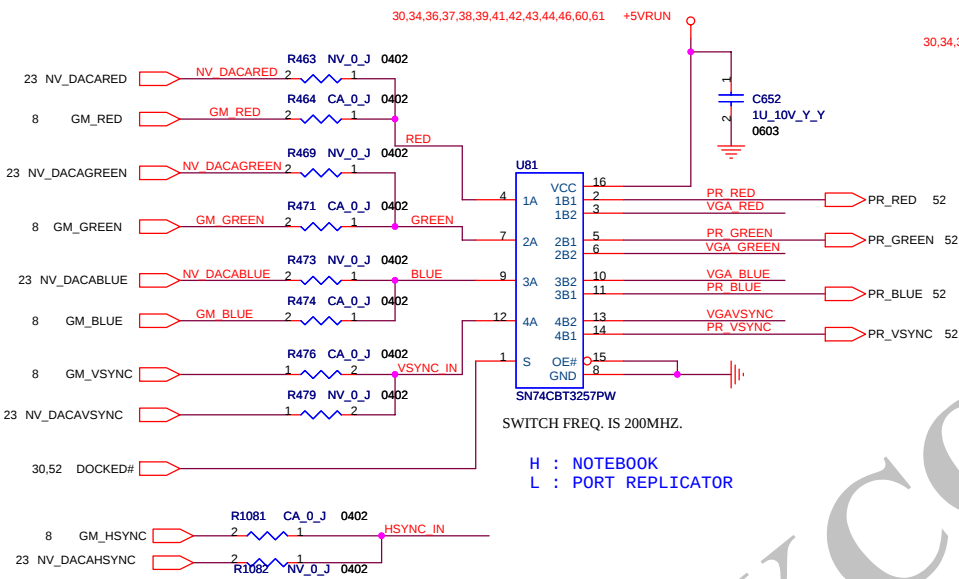
Sheet

28 of 74

Rev

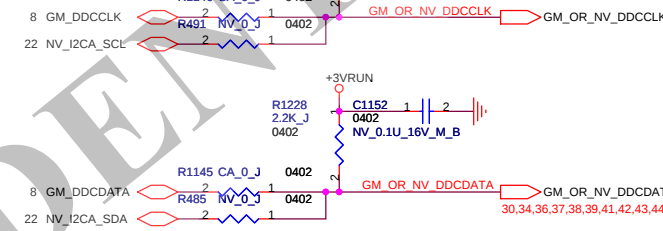
1.00

CRT ANALOG SWITCH

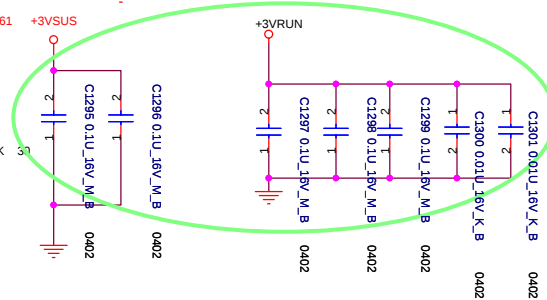


PVT modify

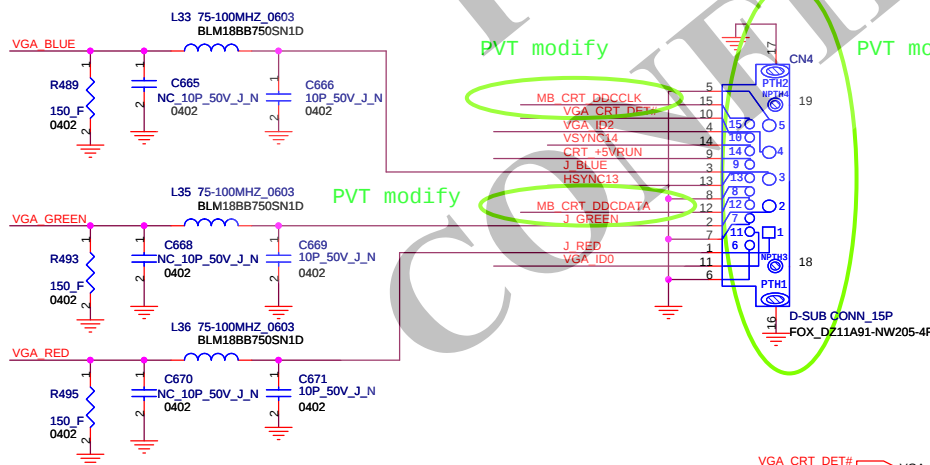
5/12
Follow Intel FAE suggest GM_DDCCLK
and GM_DDCDATA are 3.3V tolerance
signals from Calistoga



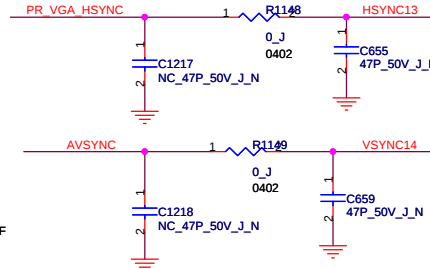
For EMI used



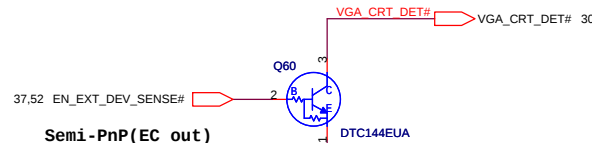
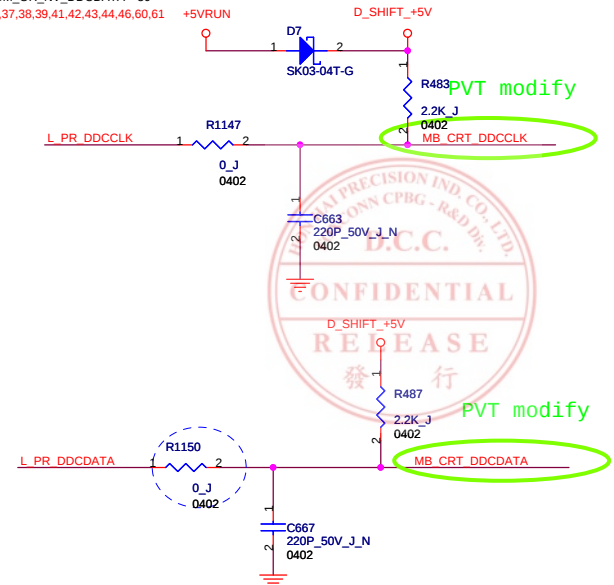
CRT CONNECTOR



PVT modify



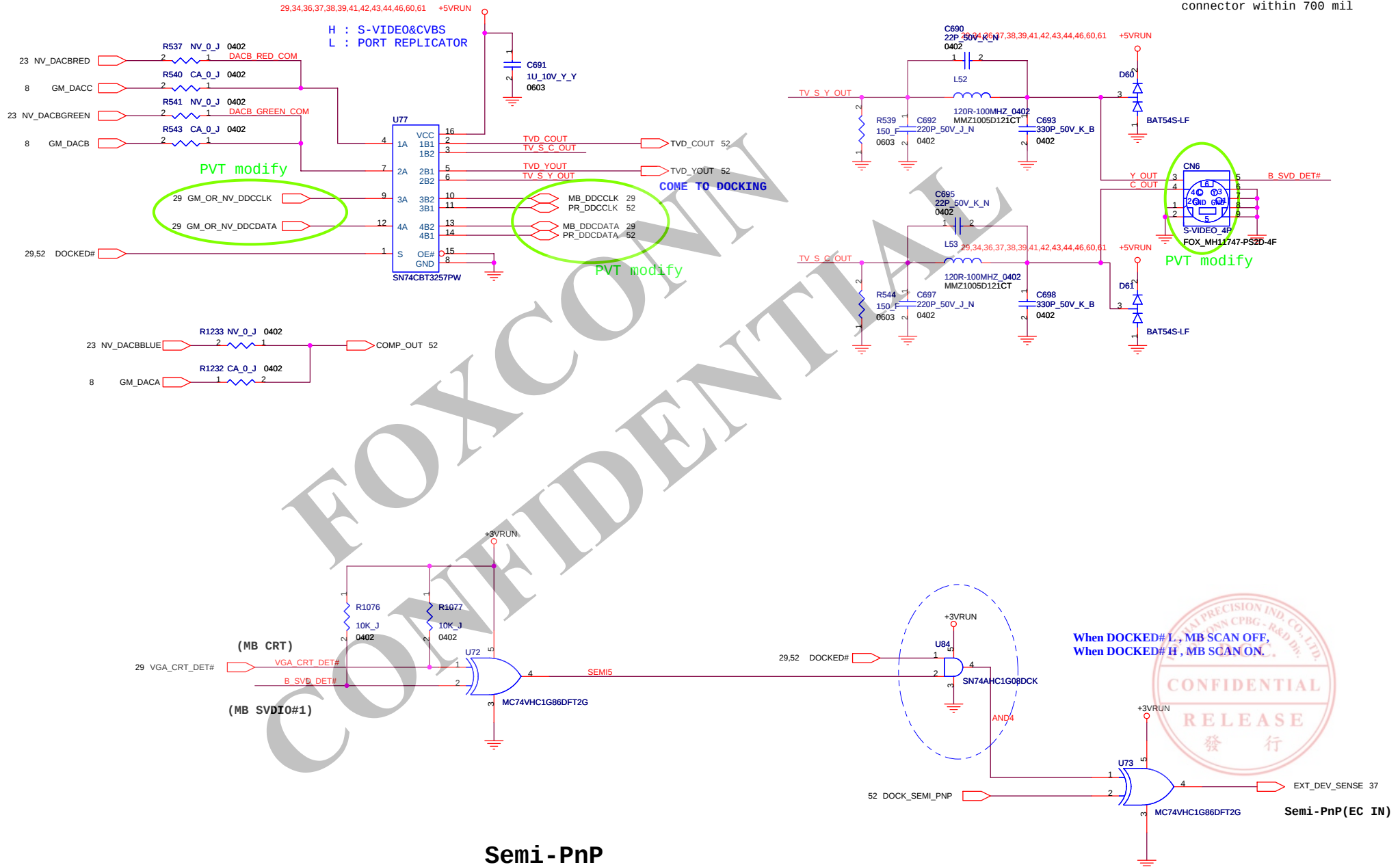
PVT modify

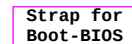


S-VIDEO ANALOG SWITCH

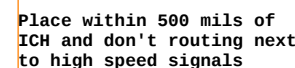
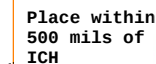
S-VIDEO

These compoent close to S-Video connector within 700 mil





	GNT5#	GNT4#
LPC(Default)	H1	H1
PCI	H1	LOW



RTCRST#

VccRTC

Min :
5ms

The traces inside this
block should be wider.
No digital signals routed
under XTAL

Check
resistor
value

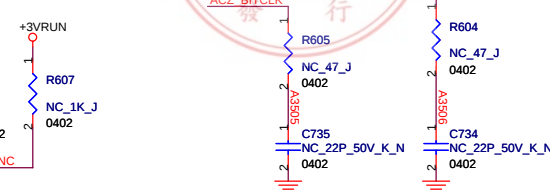
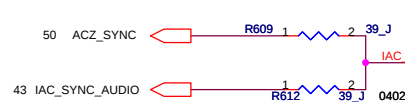
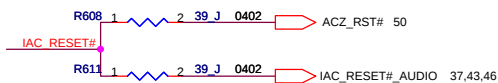
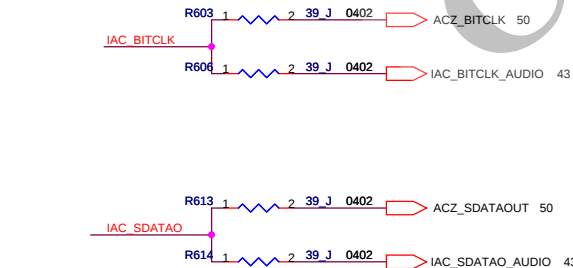
HEADER_2P

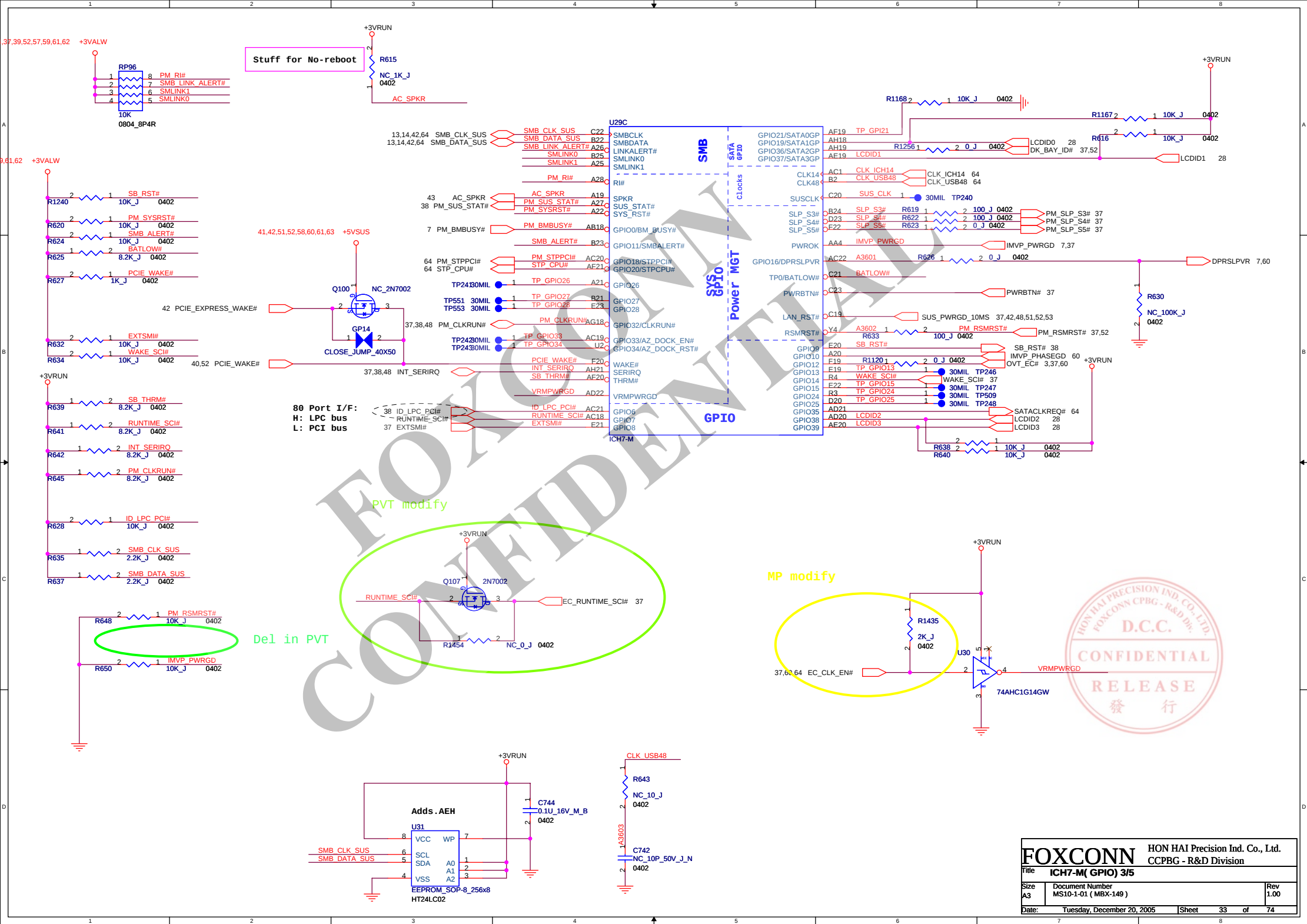
FOX_HS8202E

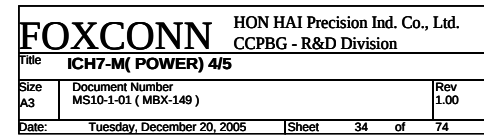
34,62

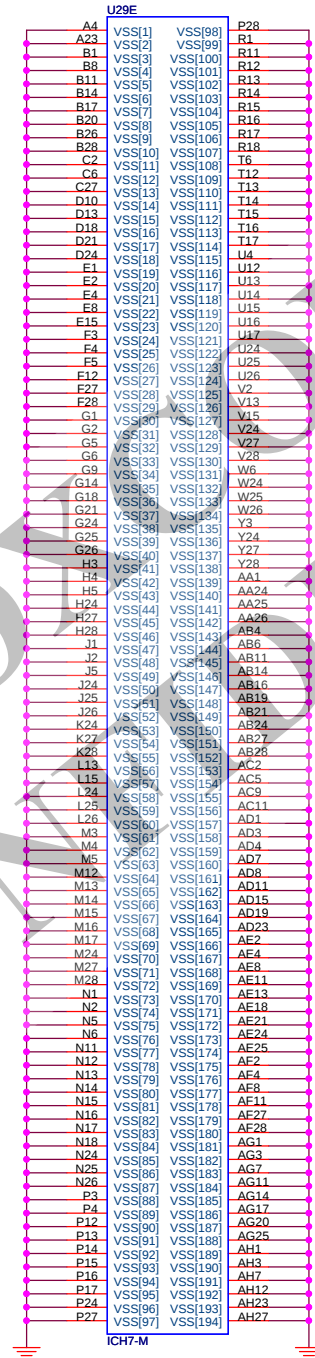
Pull-up to enable
internal VccSus1_05
regular
Pull-Low to disable

Distance between the ICH-7M
and C on the "P" signal
should be identical distance
between the ICH-7M and C on
the "N" signal for same pair

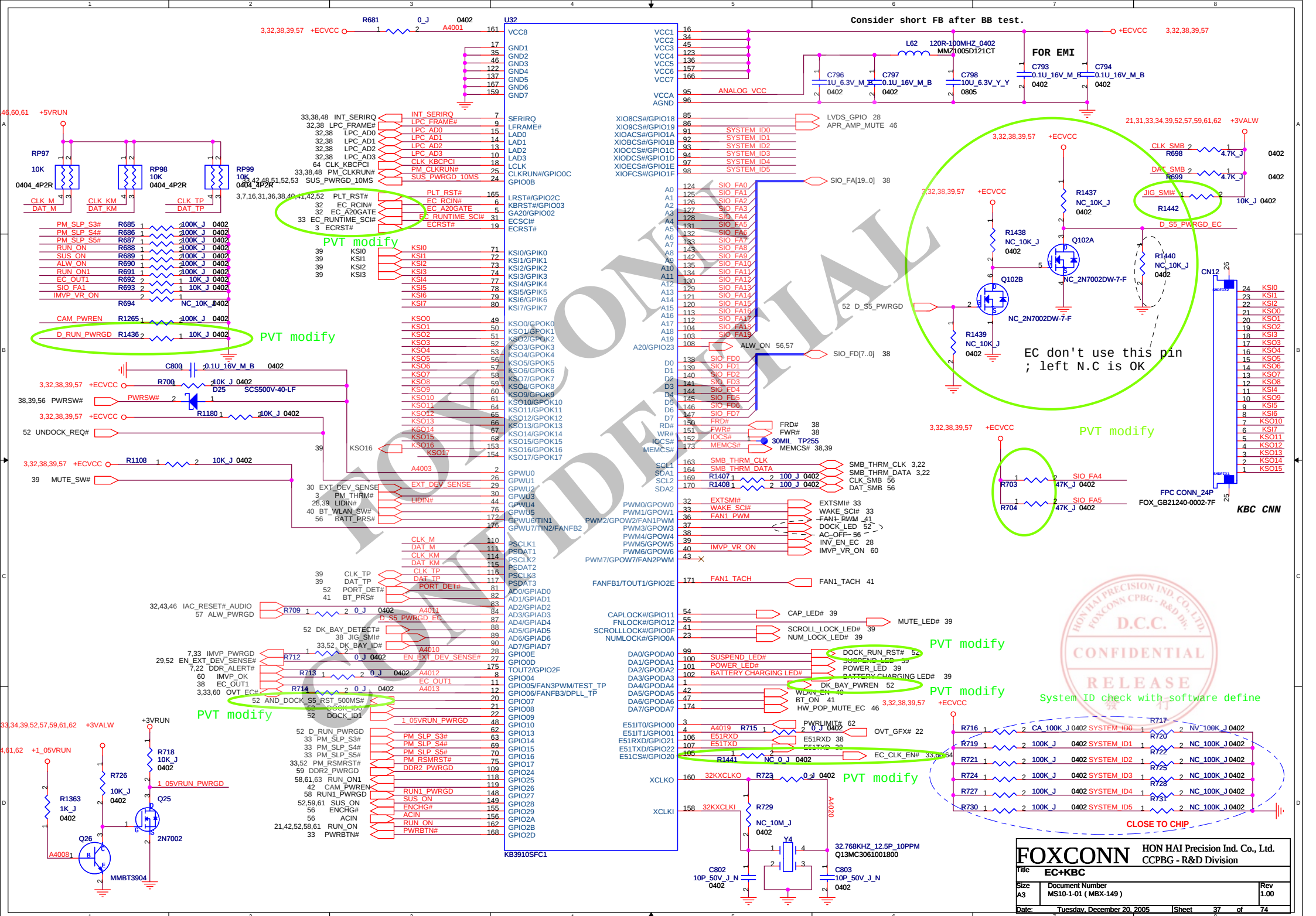


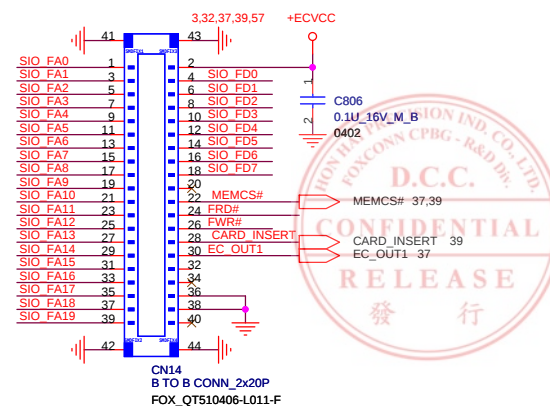


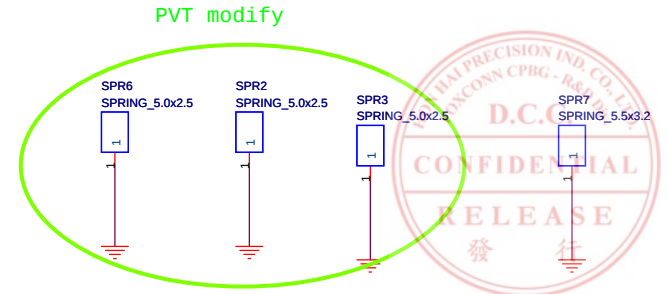
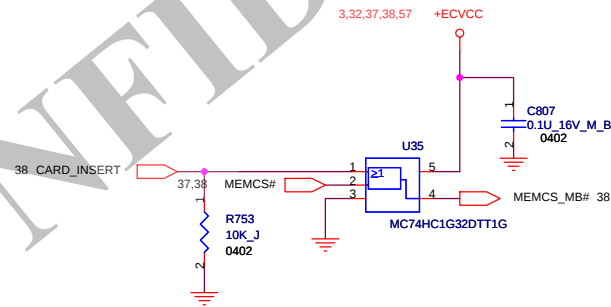
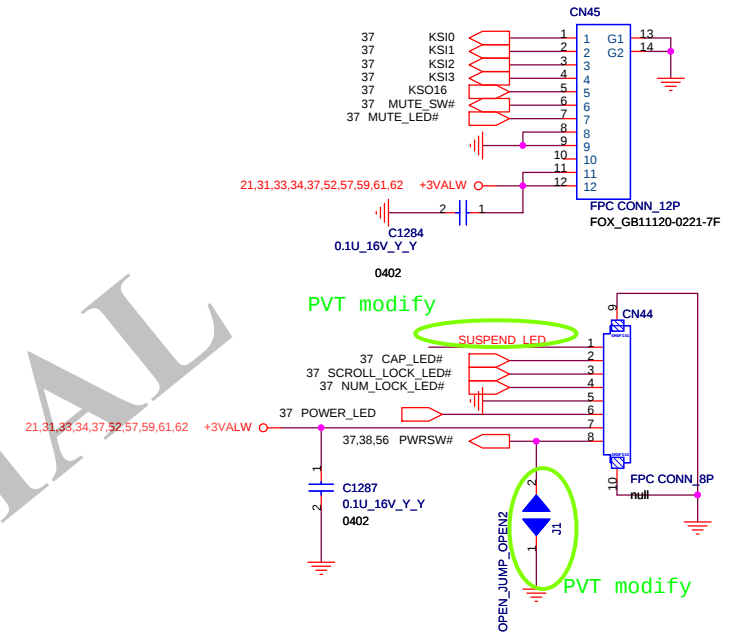
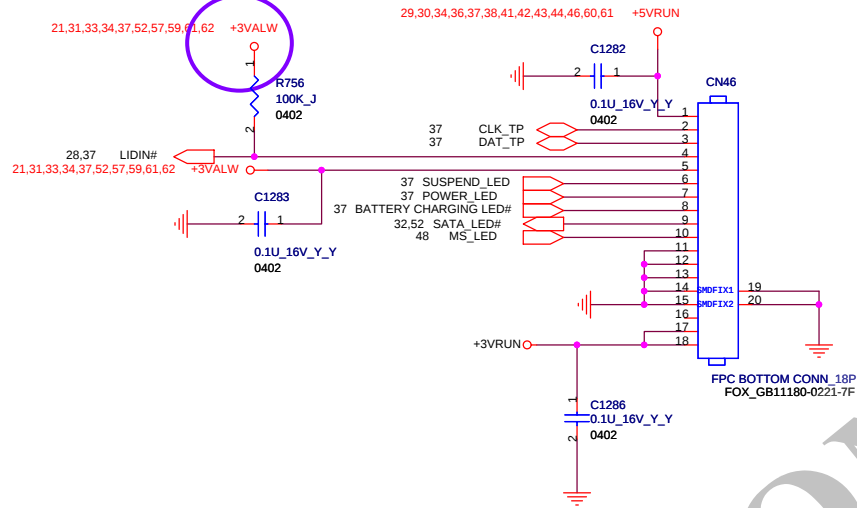


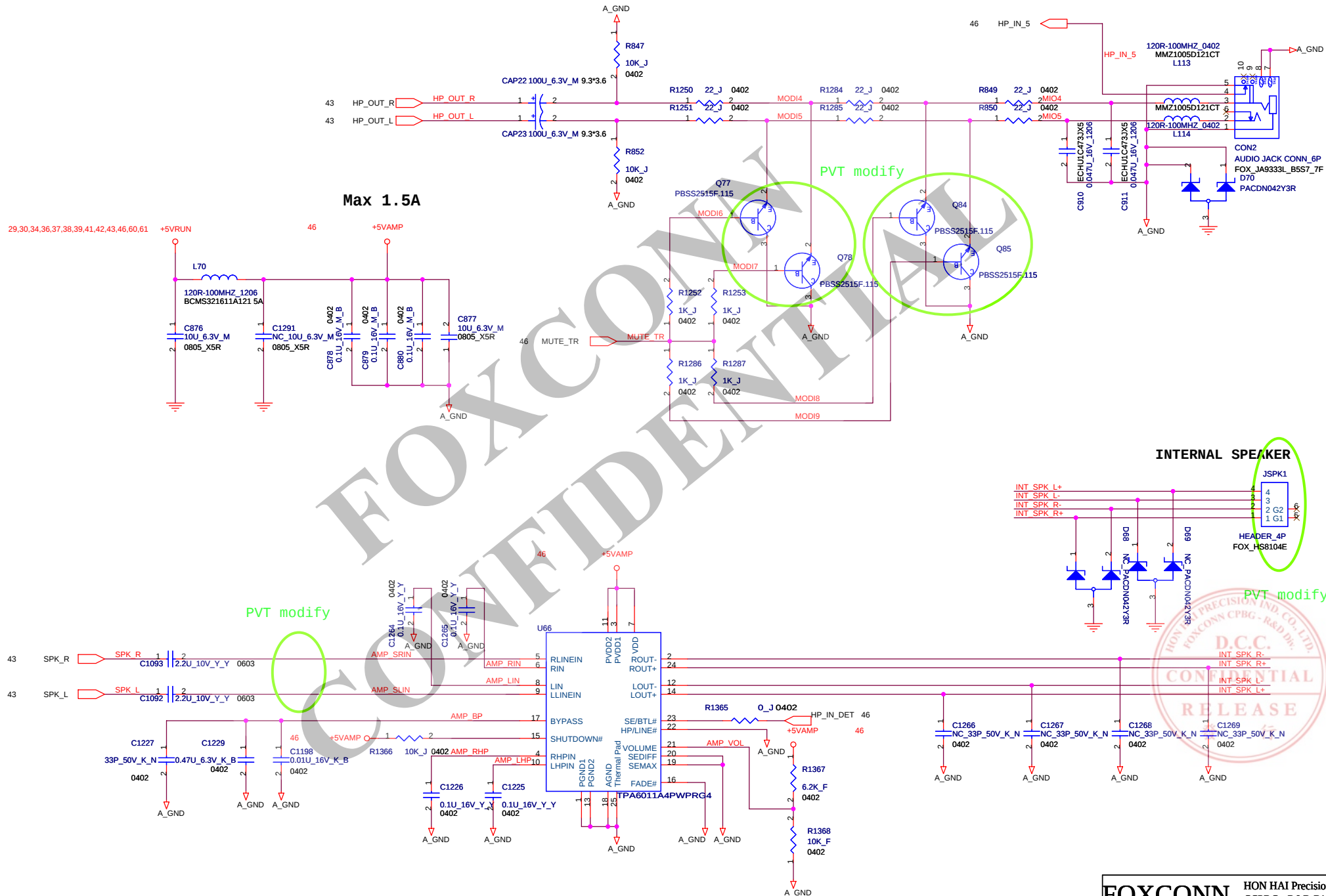


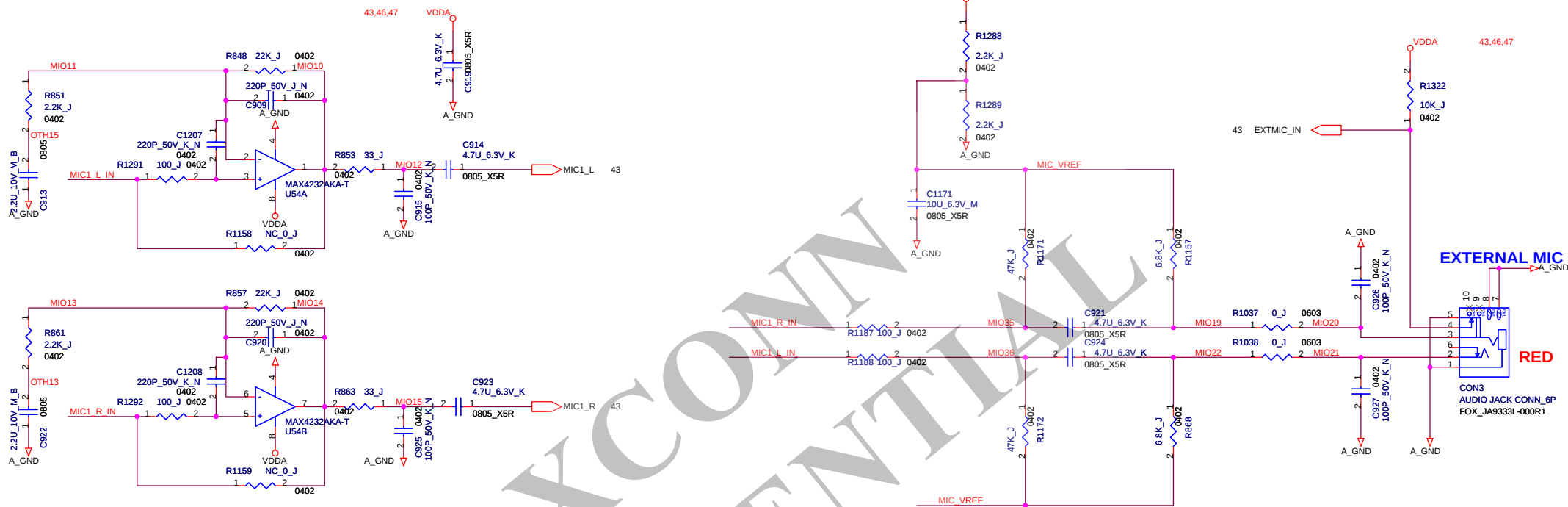
FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title		ICH7-M(GND) 5/5	
Size	Document Number	Rev	
A3	MS10-1-01 (MBX-149)	1.00	
Date:	Tuesday, December 20, 2005	Sheet	35 of 74



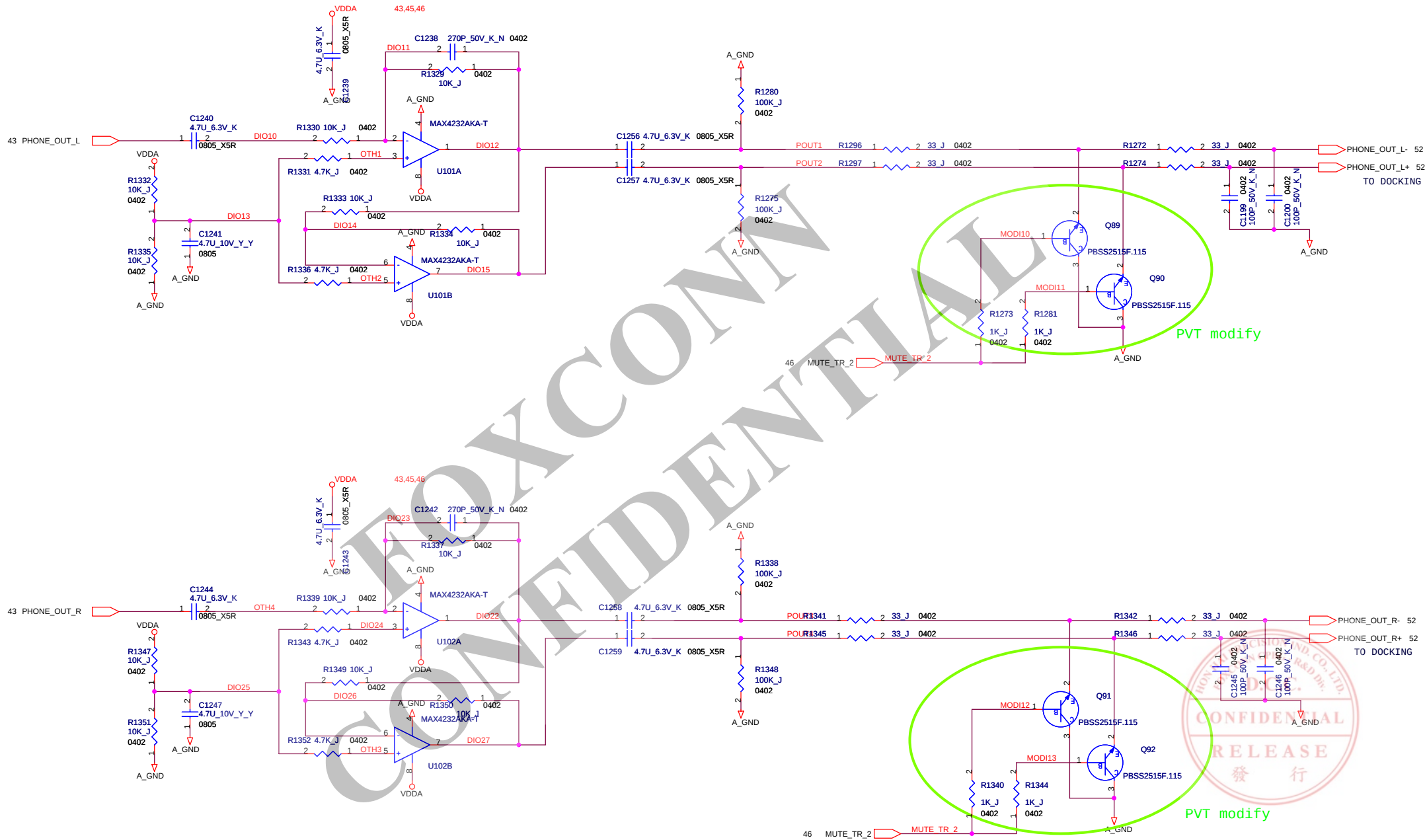


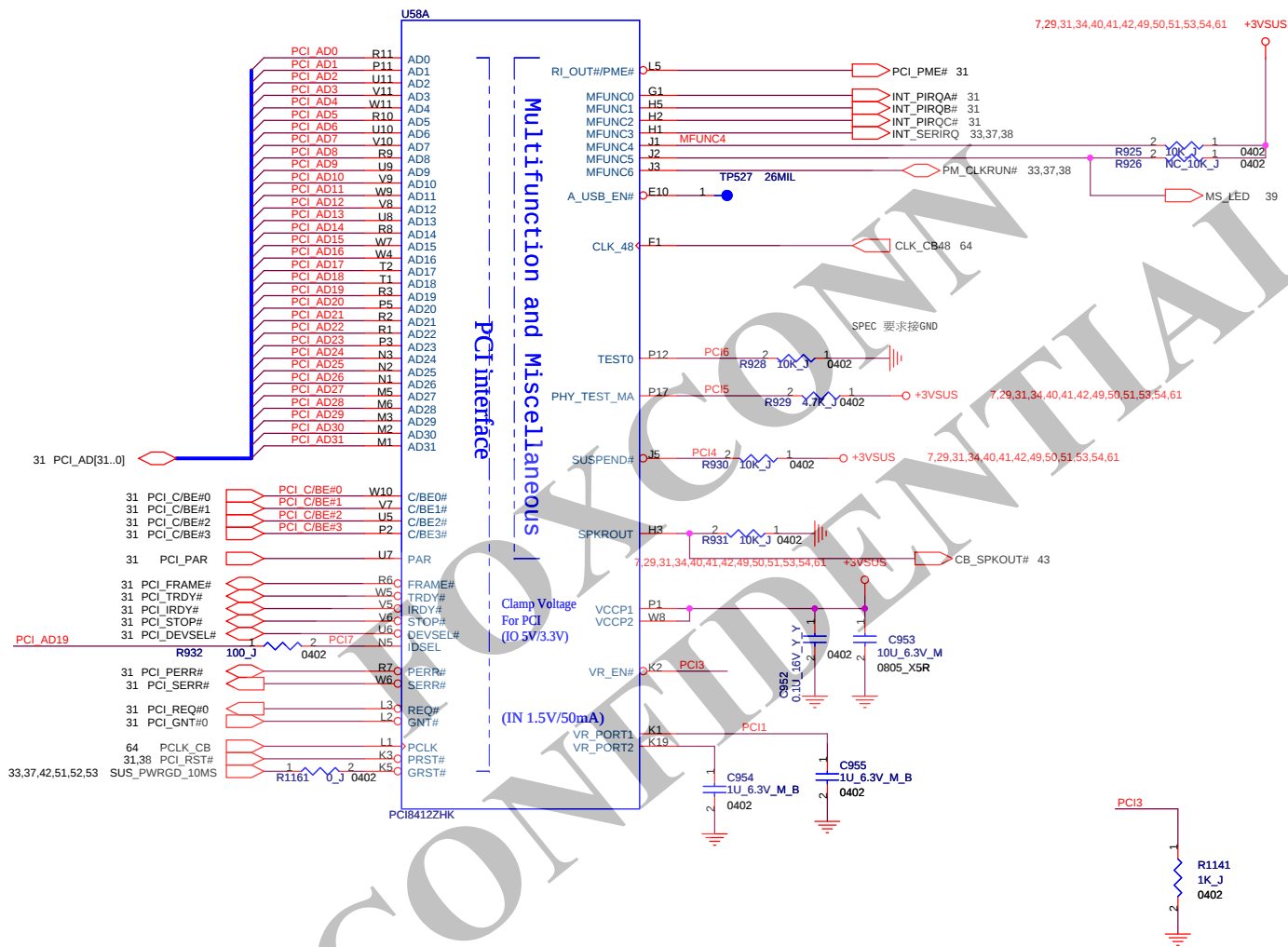












This array must be placed close to VDDPLL (Pin U19). They must be tied to a low-impedance GND.

This array must be placed close to AVDD (Pin P13,P14,U15). They must be tied to a low-impedance GND.

This capacitor should be placed between Pin P15 and Pin R17 .

This capacitor must be placed to IC pin

VSSPLL must be tied to a low-impedance GND.

iLink CONN.

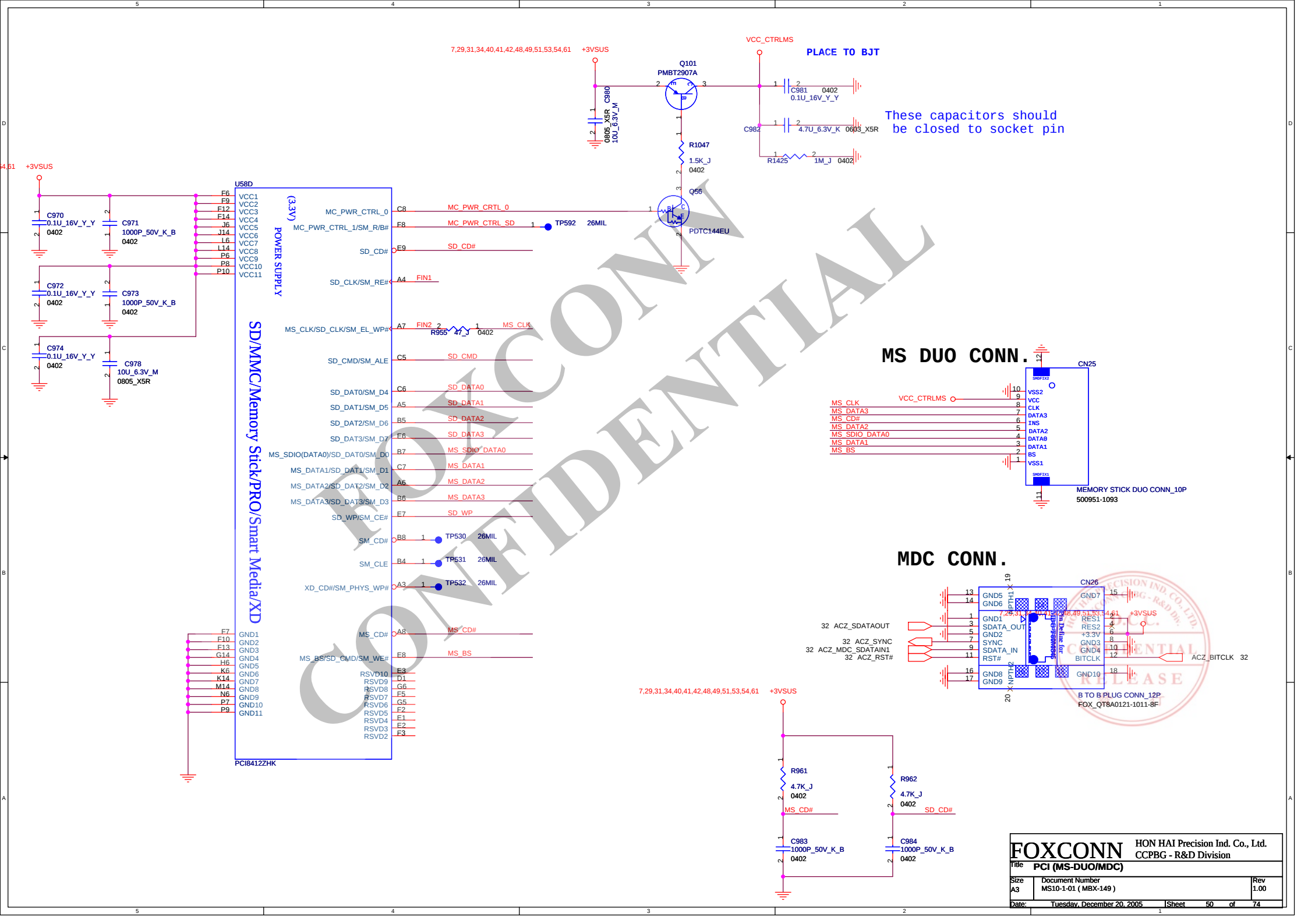
PVT modify

Place near PCI7412.

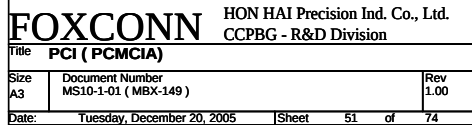
Resistors should be placed on the SCL and SDA terminals



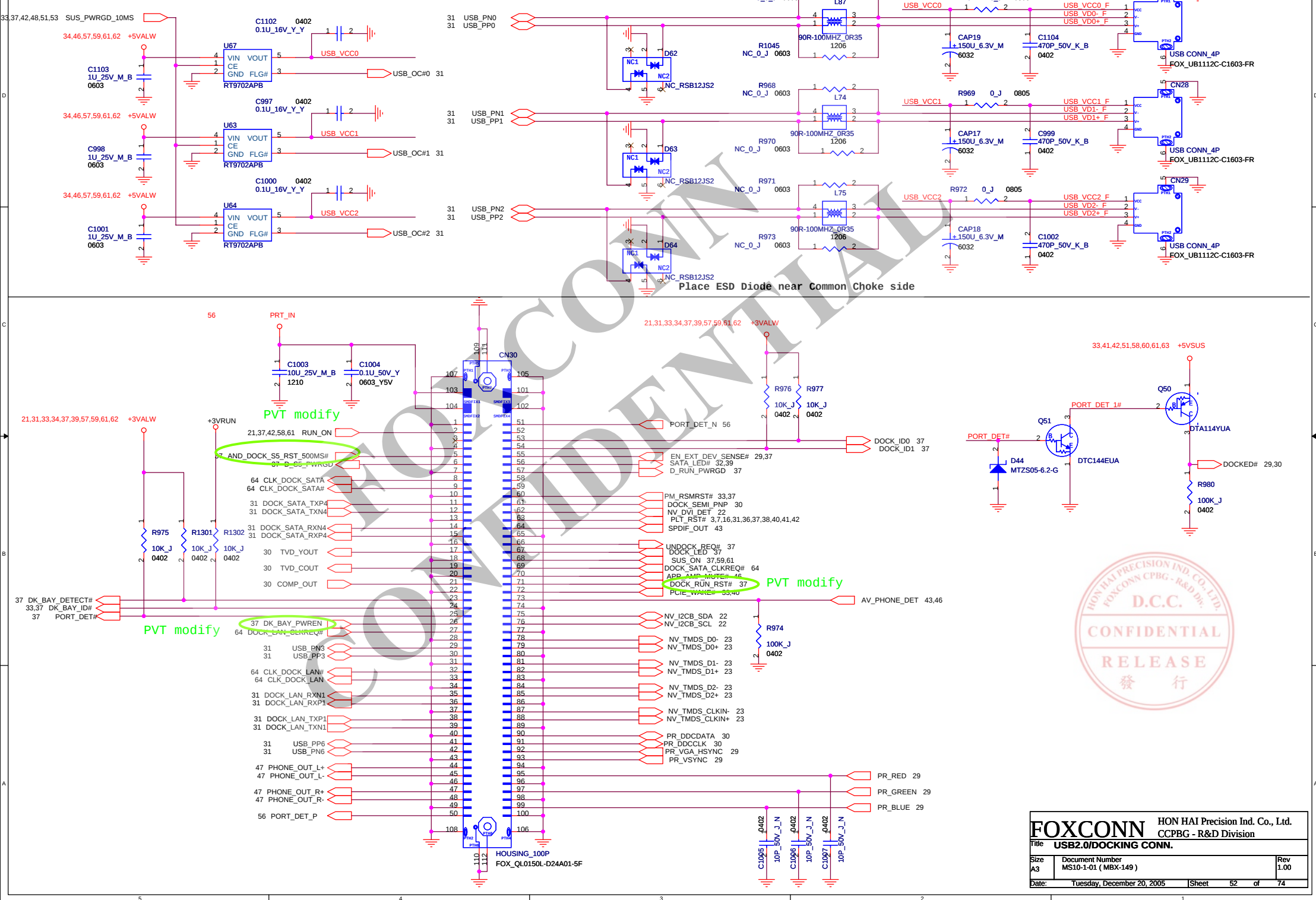
FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title PCI (iLINK)		
Size A3	Document Number MS10-1-01 (MBX-149)	Rev 1.00
Date: Tuesday, December 20, 2005	Sheet 49	of 74

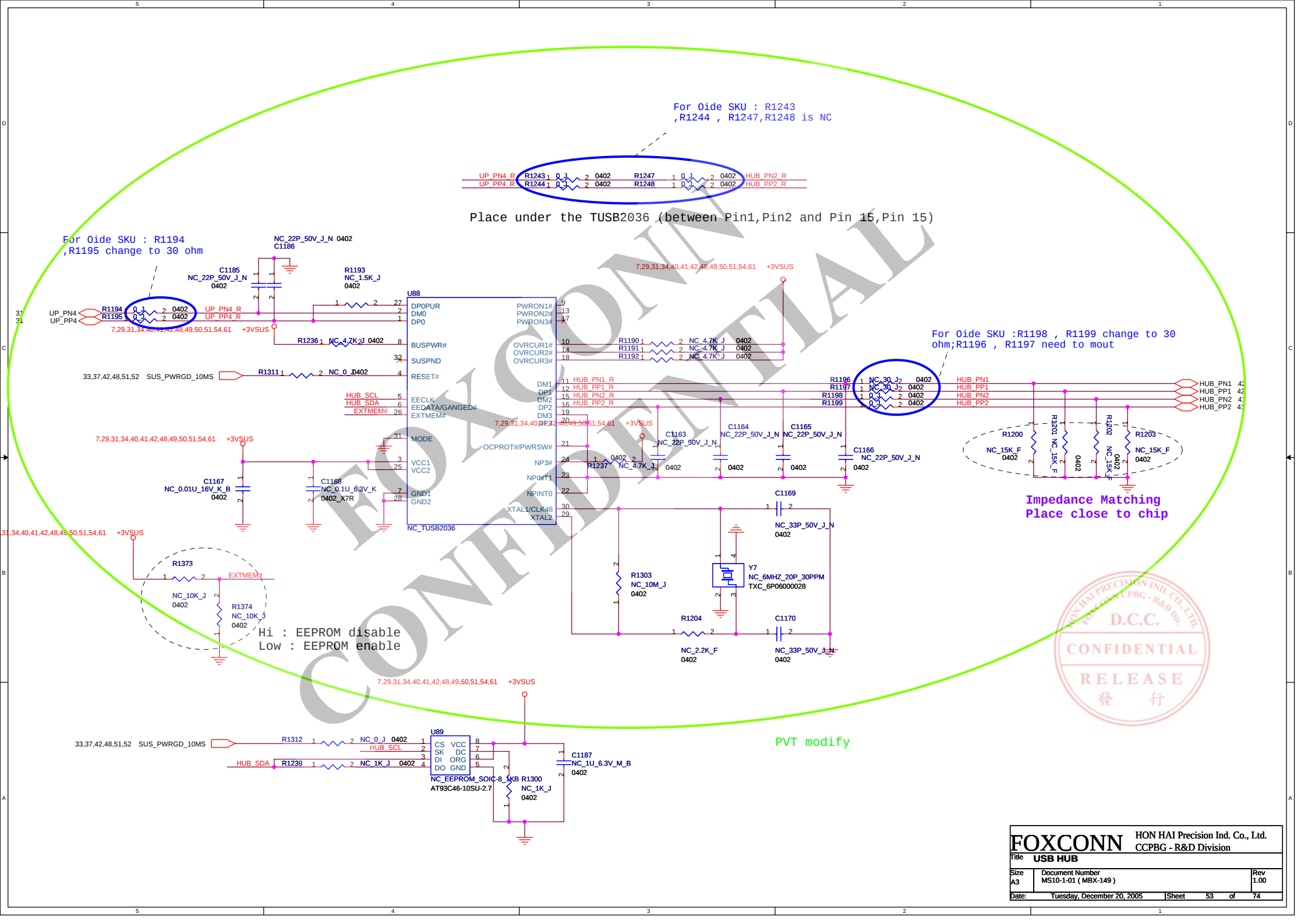


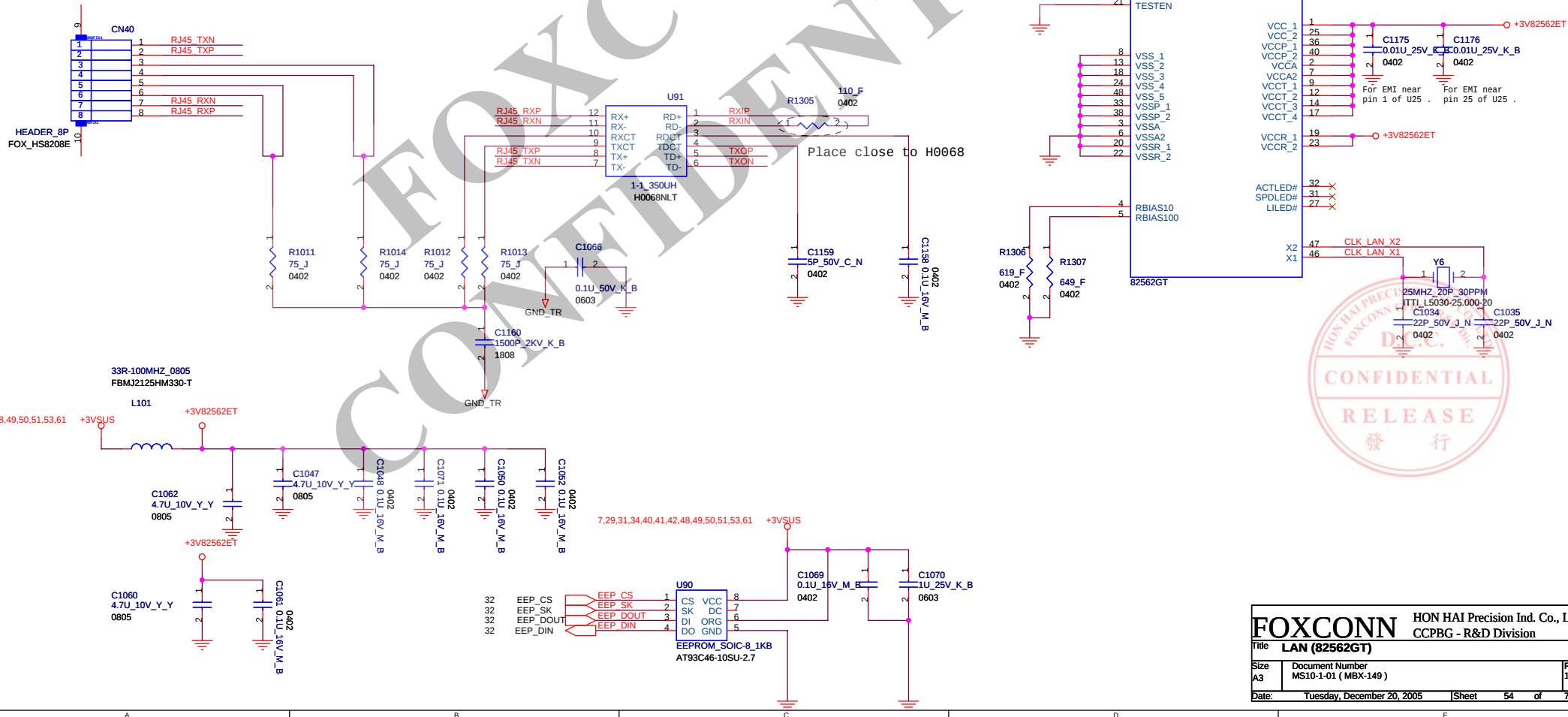
PVT modify

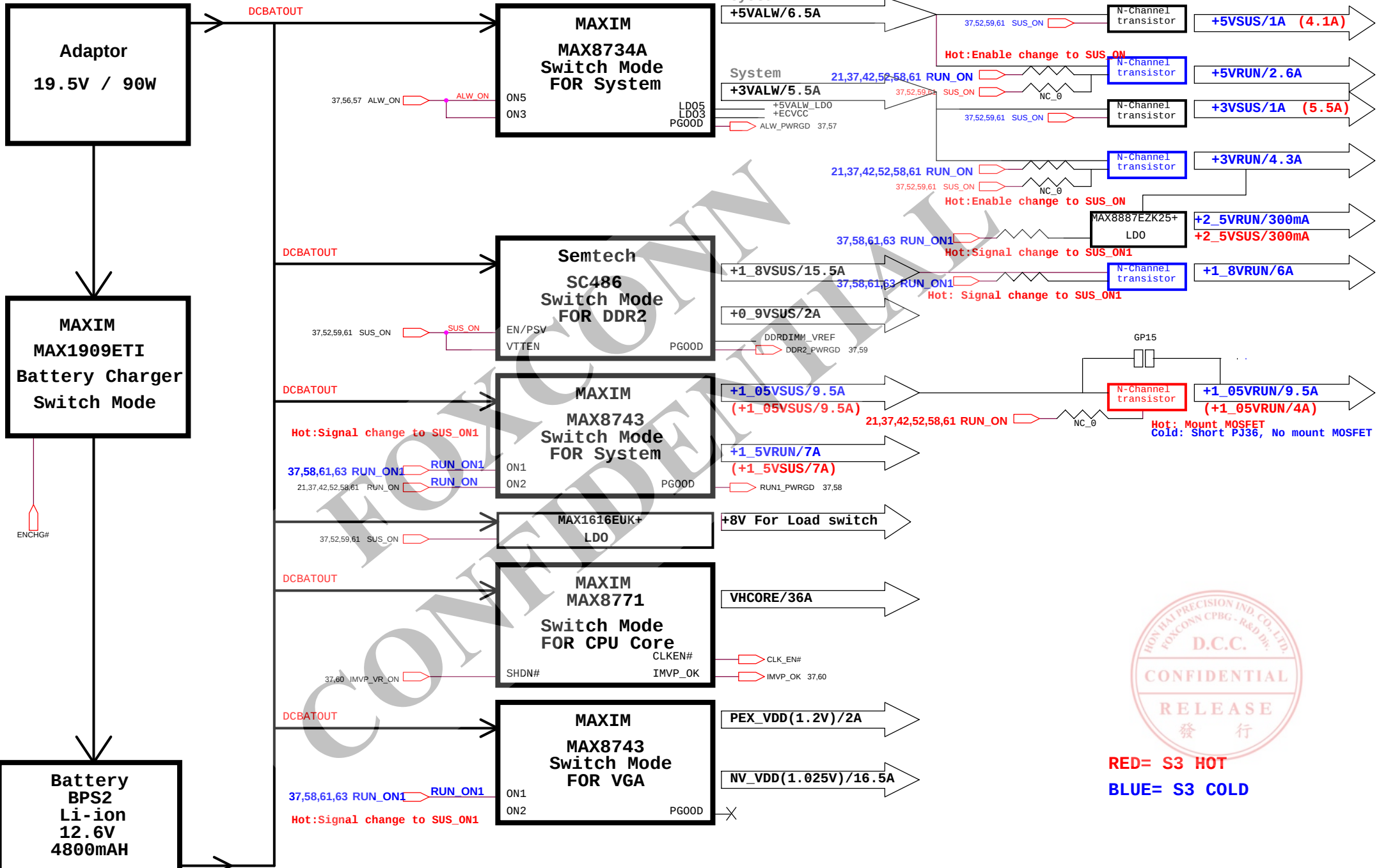
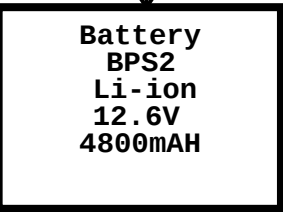
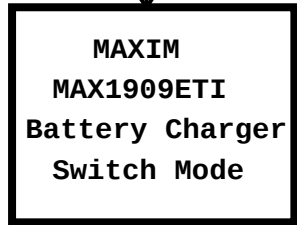
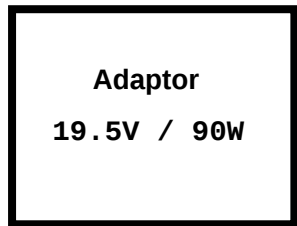


USB CONN X 3

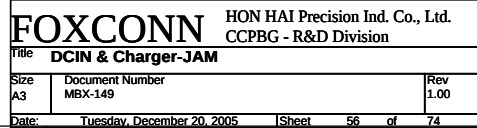


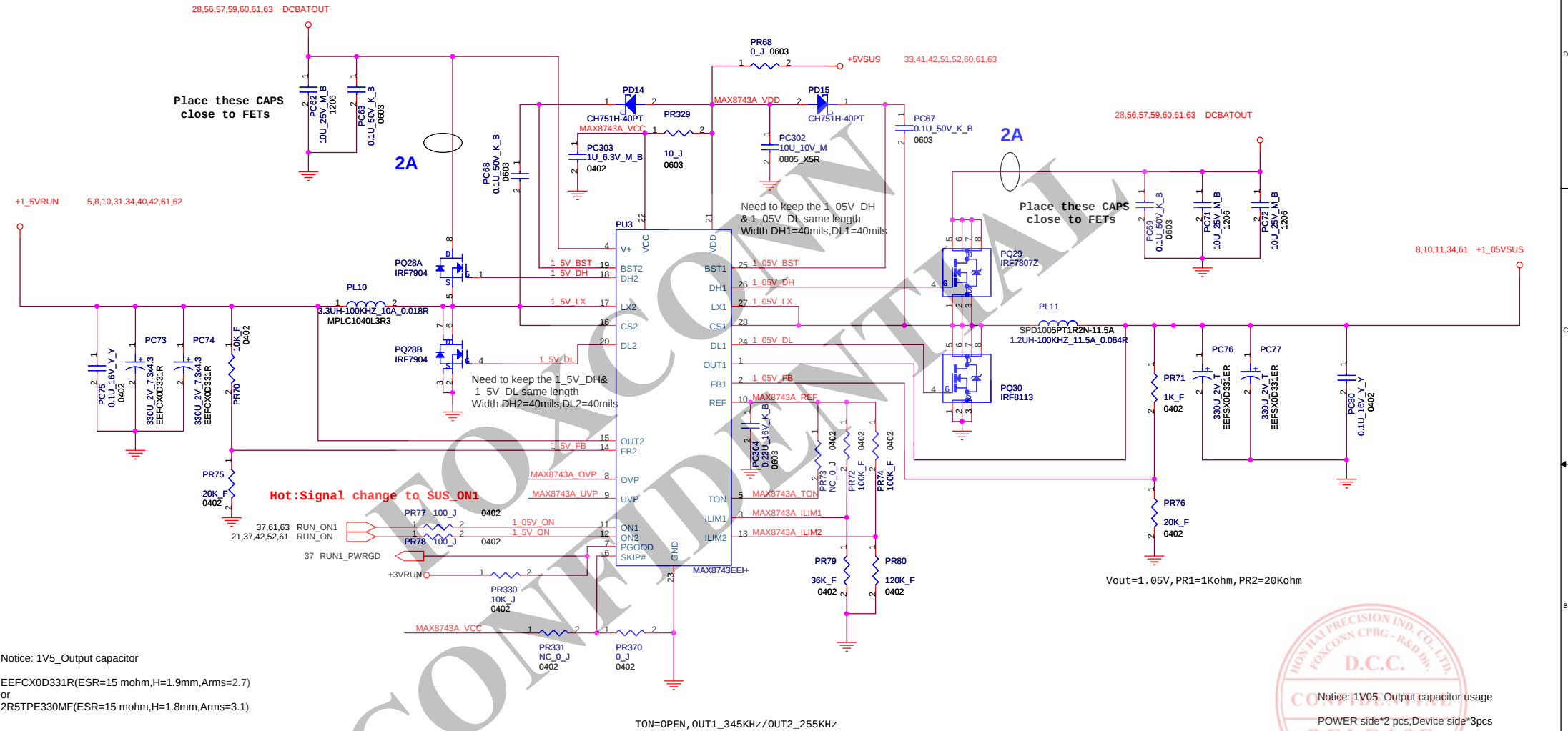




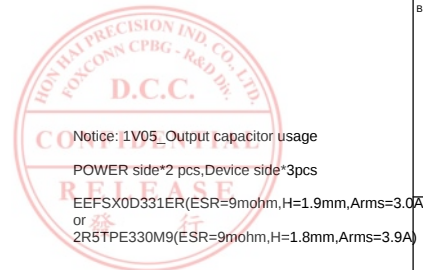
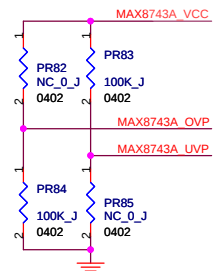


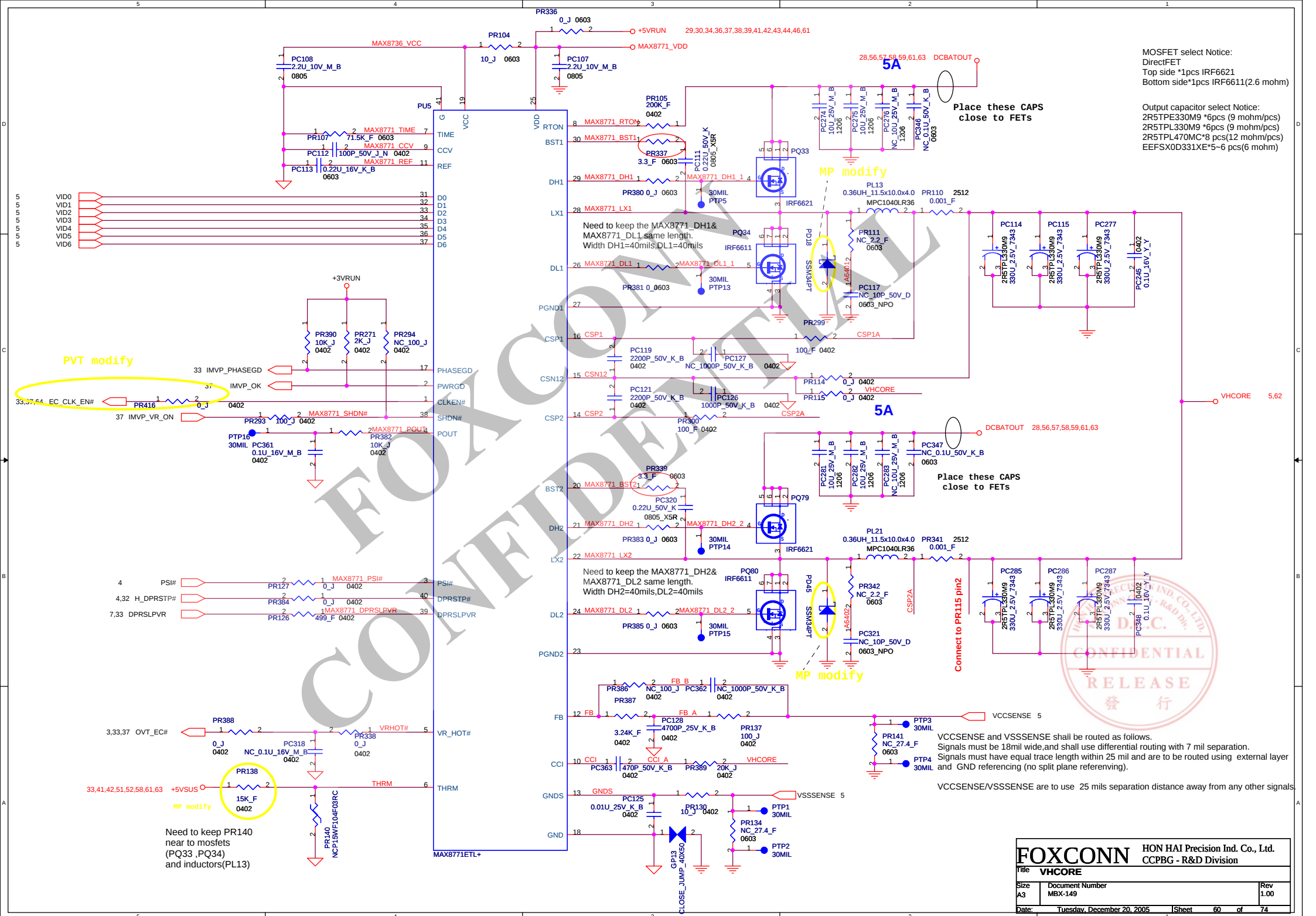
RED= S3 HOT
BLUE= S3 COLD





Notice: 1V5_ Output capacitor
EEFCX0D331R(ESR=15 mohm,H=1.9mm,Arms=2.7)
or
2R5TPE330MF(ESR=15 mohm,H=1.8mm,Arms=3.1)





MOSFET select Notice:
DirectFET
Top side *1pcs IRF6621
Bottom side*1pcs IRF6611(2.6 mohm)

Output capacitor select Notice:
2R5TPE330M9 *6pcs (9 mohm/pcs)
2R5TPL330M9 *6pcs (9 mohm/pcs)
2R5TPL470MC*8 pcs(12 mohm/pcs)
EEFSX0D331XE*5-6 pcs(6 mohm)

Place these CAPS
close to FETs

MP modify

Need to keep the MAX8771_DH1&
MAX8771_DL1 same length.
Width DH1=40mils,DL1=40mils

MP modify

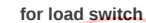
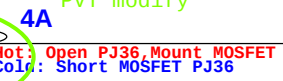
Need to keep the MAX8771_DH2&
MAX8771_DL2 same length.
Width DH2=40mils,DL2=40mils

MP modify

VCCSENSE and VSSSENSE shall be routed as follows.
Signals must be 18mil wide, and shall use differential routing with 7 mil separation.
Signals must have equal trace length within 25 mil and are to be routed using external layer
and GND referencing (no split plane referreving).

VCCSENSE/VSSSENSE are to use 25 mils separation distance away from any other signals.

Need to keep PR140
near to mosfets
(PQ33, PQ34)
and inductors(PL13)



Control ACIN OCP protect

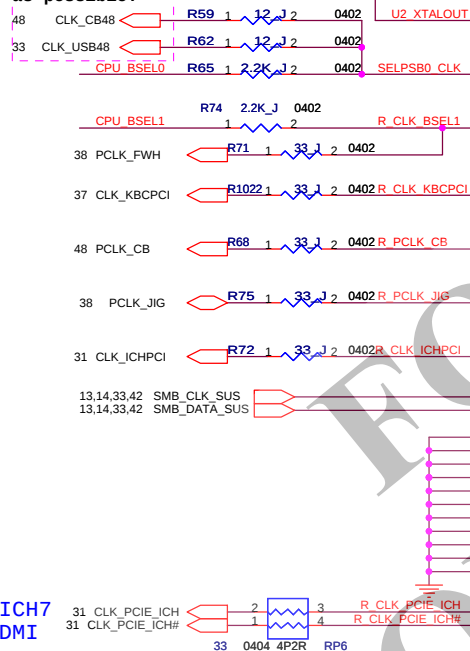
MP modify 1219



NC_10P_50V_E_N	2	1	CLK_C848
NC_10P_50V_E_N	2	1	CLK_USB48
NC_10P_50V_E_N	2	1	CLK_KBCPCI
NC_10P_50V_E_N	2	1	PCLK_CB
NC_10P_50V_E_N	2	1	PCLK_FWH
NC_10P_50V_E_N	2	1	CLK_ICHPCI
NC_10P_50V_E_N	2	1	CLK_ICH14
NC_10P_50V_E_N	2	1	PCLK_JIG
NC_10P_50V_E_N	2	1	C92 0402

close to clk gen (For EMI)

Length as short as possible.



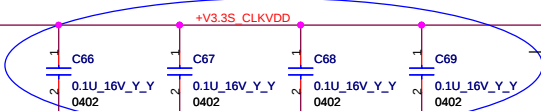
ICH7 DMI

06/17
CLK_PCIE_ICH changed to SRCLK7
CLK_DOCK_LAN changed to SRCLK8
SW Note: datasheet page13 Byte8.1 => SRCLK7 should be configured as "Not Controlled"

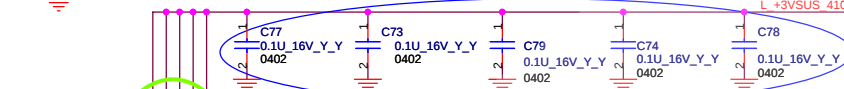
FSB Frequency Table:

FSLB	FSLA	CPU SRC[7:0]	PCI
0	0	100	100
0	1	133	100
1	0	200	100
1	1	166	100

06/17
DEL 0 ohm resistor R38, R47, R50,
0.1u Cap C71 C64
10u Cap C72
Cap C78 changed to 0.1u



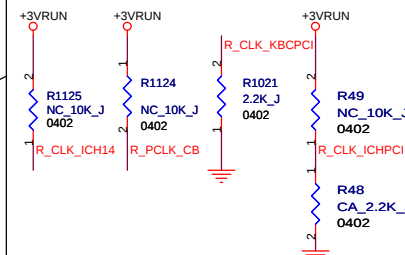
6/17
Layout note:
Place 1 cap close to each pin



CALISTOGA Chip HOST

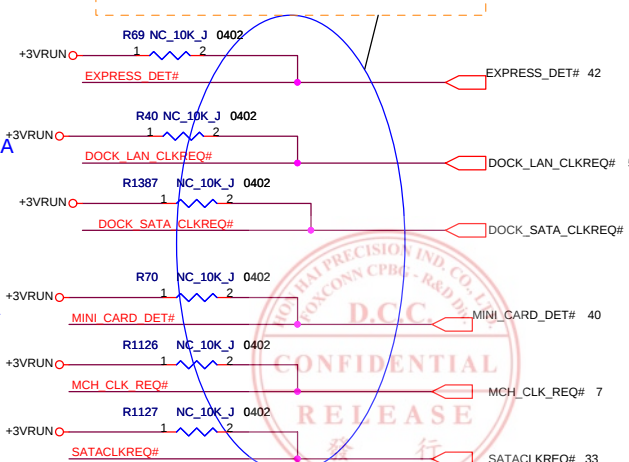
CPU

06/16
pin53/59/60/64 with internal pull-up resistor
No Stuff Pull-up Resistor (R1125, R1124, R49)
If EVT ok, del them in DVT
R1021/R48 changed to 2.2Kohm



Pin Straps	
Pin	Pin
pin53	pin 11/12
0	SRCLK0
1	27MHz (v)
pin59	pin 15/16
0	SRCLK0
1	SATA (v)
pin60	pin 37/38
0	SRCLK8 (v)
1	CPU 2 ITP
pin64	pin 13/14
0	LCDCLK_SS (CA)
1	SRCLK1 (NV)

06/09
CLKREQ with internal pull-up resistor
No Stuff Pull-up Resistor (R69, R40, R41, R70, R1126, R1127)
If EVT ok, del them in DVT



Nvidia Graphic

CALISTOGA DOT96

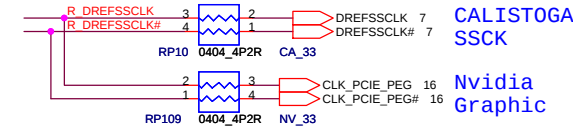
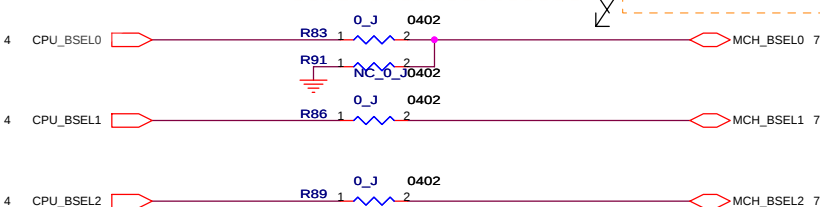
SM bus Address 9859LPR321BKLF
1101001 (ICH7)
For clock generator

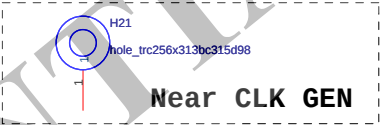
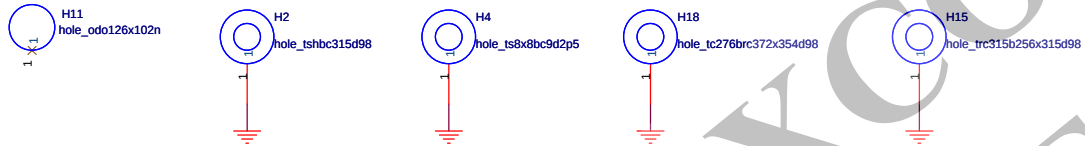
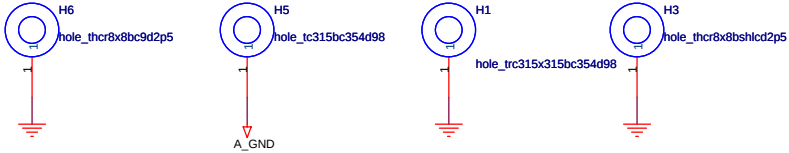
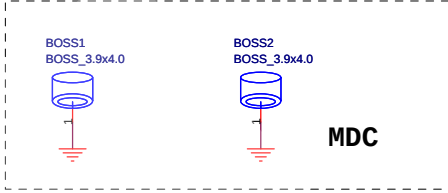
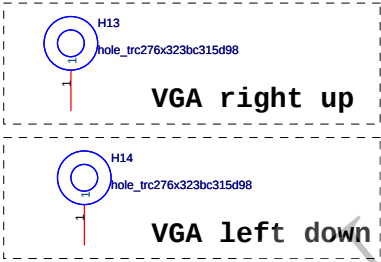
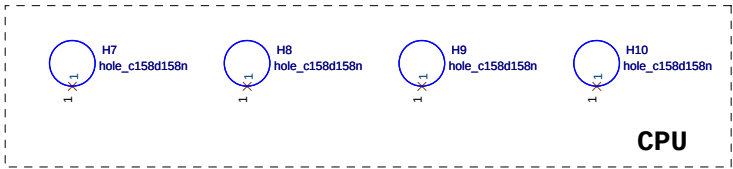
PVT modify

PVT modify

06/09
DEL pull-up resistor R80-82
pull-down resistor R85, R88
Del R84, R87, R90

06/16
ICS have recognized, FSLA/FSLB setting is different from CK410M spec. But MS10 will not use 100MHz, For test purpose, please move R91 from MCH_BSEL2 to MCH_BSEL0, and mount R89.





HISTORY (Before 2005/06/20)

P.2 Change Q71 , Q4 from MMBT3904 to PDTCT144EU to improvement quality
P.4 Reduce CPU VHCOR's capacitor (22uF * 12 PCS ; 0.1uF *10 PCS ; 1000p *10 PCS)
P.5 del C64,C71,C72,C82,C87,C1075
P.5 change C78 from 10U_6.3V_Y_Y to 0.1U_16V_Y_Y ; del D1 BAT54S-LF
P.5 del R38,R47,R50,R67,R77,R80,R81,R82,R84,R85,R87,R88,R90,R128
P.5 del SRC 49.9ohm termination resistor : R1053,R1054,R39,R42,R43,R44,R45,R46,R51,R52,R53,R54,R55,R56,R57,R58,R60,R61,R63,R64
P.5 del TestPad TP512,TP513,TP514,TP515
P.5 Add R74 2.2K_J ; Add R1308 NV_0_J ; change R1021 from 33_J to 2.2K_J
P.5 change R1124 from NV_10K_J to NC_10K_J ; change R1125 from CA_10K_J to NC_10K_J
P.5 change R1126,R1127 from 10K_J to NC_10K_J
P.5 change R48 from 49.9_F to CA_2.2K_J
P.5 change R49 from 49.9_F to NC_10K_J ; change R40,R41 from 49.9_F to NC_10K_J
P.5 change R69,R70 from 10K_J to NC_10K_J
P.5 change U18 Clkgen from Cypress_28445-5(68-pin MLF) to ICS_9LPR321AKLF (64pinMLF)
P.8 Add R1229-R1231
P.10 Reduce NB VTT plane's capacitor (C149-C157) adn change power plane from SUS to RUN plane
P.10 Reduce NB VCCAUX power plane 's capacitor C174-C190
P.10 Reduce NB VCC plane capacitor C208-C215 & del R148-R150
P.12 Del R154-R161 ,R163,R164 MCH_CFG's strap resistor
P.13,P.14 Del R170-R173 and change 1_8VSUS_DDR2 net name to 1_8VSUS;3VSUS_DDR2_SPD to 3VSUS
P.28 Connect LVDS signals directly to LVDS connector without choke
P.28 Del brightness PWM circuit and add R1268 , R1269
P.28 Change CN3.38-40 net name to DCBATOUT
P.28 Add GP11 R771 for BIOS_CRISIS# function
P.29 Modify GM_OR_NV_DDCCLK & GM_OR_NV_DDCDATA circuit
P.29 Del C1109 ,C1110 ,R1136 EMI's component and Del DVI function
P.30 Del TV-OUT composite connector ; add D60 ,D61 for ESD protection
P.30 Add R1233 ,R1232 and del DVI's ESD protection circuit
P.30 Modify Semi-PNP circuit and del S-Video 2 circuit
P.31 Modify U29 USB channel 4 net name for HUB
P.32 Del AZALIA interface 8 capacitor for EMI reserved
P.32 Connect SB's LAN interface to INTEL's FHY(change LAN solution)
P.33 Add R124 for JIG board ; del R618 , R621 ,R646 ,R651 , R653
P.33 Change R1184 to NC and mount R1183 for power sequence unstable issue
P.33 Modify LCDID0 ,1 to GPIO 19 #37; add R1256 for Dock_BAY ;Del R738 , R659 ,R661
P.36 Del SATA2(CN10) for EVT SPEC
P.37 Add R1265 pull low for CAM power on-off function
P.37 Add signal DK_BAY_DETECT# , CAM_PWREN , DK_BAYPWEN ; del R701 and drop FAN2_DAC function
P.37 Change Q24 ,Q26 from MMBT3904 to PDTCT144EU to improvement quality
P.38 Del BIOS socket ; del TPM function(CN35) J1 CN36(P52 function)
P.39 Make SW and LED to D/B(including LID SW , Touch Pad) add SPR2 ,SPR6 for EMI request
P.40 Move LED to D/B ; del C818-C821 , C824 ,C825 reserved capacitor
P.41 Del Fane circuit and change FAN connector from 4 pin to 3 pin
P.41 Move BT's LED circuit to D/B
P.42 Reduce Express Card power SW's capacitor and combin U36 pin 56 & 21 net name
P.42 Change Q35 part , and make Q35 & R772 to NC
P.42 Change Oide USB interface connet to USB HUB "TUSB2036"
P.48 Del R993 ,R1140 and mount R1141 for IT17412's ERRATA
P.49 Del R1174 , C1146-C1150 for IT17412's ERRATA
P.50 Del SD function and move MS's LED to D/B ; change CN25 , CN26 connector
P.52 Change CN37 , CN28 ,CN29 connector
P.53 Del Mini-PCI function and add USB TUB2036 HUB
P. 36 Del PATA HDD function and move HDD's LED to D/B
P.54 Change LAN solution to INTEL 82562GT
P.16 Add R1263 2K ohm pull up +3_3VSUS to U7A " R3 " pin, for G7X " SLOT_CLOCK_CFG " strap.
P.17 Unstuff R226, R227 and stuff R225, R228 change from " 3GIO_PADCFG[2:0] " 001 to 010 for G7X series.
P.19 Change R305 Unstuff to Stuff for G7X.
P.19 Add R1262 for G7X/ NV34M co-layout and R1262 no need stuff for G7X.
P.19 Chipset U7 Pin "F6","G8","G23","A28","F1" change to NC pin and C490 CAP no need stuff for G7X.
P.19 Add L102,C1191,C1192 on U7 Pin "T13" Voltage change from NV_VDD(1.1V) to PEX_VDD(1.2V), and add R1261 for G7X/ NV34M co-layout but R1261no need stuff for G7X
P.19 Add C1193 series connect U7 pin "M21"and "N20", is a nVIDIA CRB circuit suggest.
P.20 Delete power " FBVTT/ FBVDD " all Caps and FBVTT/FBVDDQ/FBVDD connect together.
P.20 Parts L92,L94,C402,C403,C405,C419,C421,C431,C433,R271,R275 unstuff for G7X
P.20 Delete L107,L108 and add L93,L95 for power "FAB_PLLAVDD/ FBC_PLLAVDD" from NV_VDD(1.1V) to PEX_VDD(1.2V) for G7X,
P.20 Change R269,R272 from 37.4ohm to 40ohm
P.21 Parts L21,C467,C468,C469 unstuff for G7X
P.21 Add R1264 10K pull low , when DACC is not used
P.21 Delete L96,L98 and add L103,L105 on power " IFPAB_PLLVDD/ IFPCD_PLLVDD " from +3VSUS to +2_5VSUS for G7X.
P.21 Delete L97 and add L104 on power " IFP_ABI0VDD " from LCDVCC to +1_8VSUS for G7X.
P.22 Delete R291,R294 if ROM interface no used.
P.22 Parts C488,C489,C487,R299,R300,R302,R304,R306,R307,R297,R1104 unstuff for G7X
P.23 Parts R339,R354,R355 unstuff for G7X
P.24 Parts R372,R373 change 6.81K ohm to 10K ohm for G7X
P.25 Parts R391,R392 change 6.81K ohm to 10K ohm for G7X

REV 0.A: (2005/06/21)

P.52 Change value U89 , C1187 , R1239 and add R1300
Del U87 , C1162 ,C1161 and change value R1191 , R1192
P.41 change net HUB_VCC1 to +5VSUS
P.37 Add R1282 0 ohm R
P.43 Add R1283 0ohm
P.43 NC R795 10K
P.43 Add C1201,C1202,C1203,C1204,C1205,C1206
P.44 Add R1284,R1285,Q84,Q85 for HP-OUT muting circuit
P.45 Add R1291,R1292,C1207,C1208
P.45 Add R1288,1289,1294,1295,C1171,C1172 for MIC1_VREF
P.45 Add R1296,R1297,Q86,Q87 for PHONE-OUT muting circuit

(2005/06/22)

P.2 del R1142 and change to test point
P.5 add R1308 to GND
P.7 Change GP11 to R1309 NC
P.32 Change R589 to 510 ohm and add R1310 510 ohm
P.33 change net name U29 pin AH19 to from DK_BAY_DETECT# to DK_BAY_ID#
P.33 Mount R1183 and change R1184 to NC
P.41 change CN42 from 4 pin to 3pin and del FAN2_DAC net name
P.47 Del R933 , R1140 and mount R1141
P.48 del R114 , C1146 ,C1147 , C1148 , C1149 , C1150
P.52 Add R1303 for crystal feedback resister ; Add R1311 , R1312 change net name from PLT_RST# to SUS_PWRGD_10MS
P.36 Add R1304 pull high and del D45
P.53 Add R1305 , R1306, R1307 ; del R1238 and modify U65's pin 21 to GND
P.51 add pull high R1301,R1302

(2005/06/23)

P.10 Add C1209 0.01uF , C1210 ,C1211reserve capicitor for EMI
P.11 Add C1212 ,C1213,C1214,C1215 0.1uF reserve capicitor for EMI
P.16 Del BOSS3,BOSS4 (only B8 use)
P.19 Add C1216 1000pF reserve capicitor for EMI
P.29 Add C1217,C1218 47pF reserve capicitor for EMI
P.34 Add C1219,C1220,C1221 0.01uF reserve capicitor for EMI
P.37 Change net name U32.37 from DOCK_LED# to DOCK_LED
P.51 Change net name U30.92 from DOCK_LED# to DOCK_LED
P.52 Move R1243 , R1244 ,R1247 ,R1248 from ICH7 to USB HUB side and del R1241 ,R1242(P.34) ; Mount U89 , R1300 ,C1187
P.41 short R1245 , R1246
P.30 Change CN6 from FOX_MH11741-0001 to FOX_MH11747-BS2D-4F
P.50 Change CN27 library for footprint change and add CN48 for PCMCIA hoswing portion
P.37 U32.62 pin net name from HW_POP_MUTE to HW_POP_MUTE_EC and del R1282
P.43 Delete R1283
P.43 Change net HW_POP_MUTE to HW_POP_MUTE_CODEC
P.46 Add U97 for HW_POP_MUTE
P.42 Add R1313-R1316,L110,L111 for EMI reserve and add CN47 for EXPRESS Card's hoswing portion

(2005/06/24)

P.32 Short C1177 -C1180

P.42 Update CN19 library for layout footprint

Arrange schematics :

1. Del original page 26 ,31
- 2.Move original P33 Semi-PNP circuit to P30 and del original P33
- 3.Move original P56 CD-ROM circuit to P36 and del original P56
- 4.rename all page number

(2005/06/24)Power circuit modify

P.56 Change PD1,3,10,11,12,40 for second source test in EVT.
P.56 Modify PD4 connect to BT+_4 (EMI [Jacjk Su] request)
P.57 Modify PJ1,3,2,4 allegro symbol from 80mil width to 40mil(change footprint to OPEN2B)
P.57 Change PL9 from SPD1005PT3R8N-7A to SPH1245PT5R6N
P.57 Change PL8 from RLF12545T-5R6N6R1 to SPH1245PT5R6N
P.57 Change PD13 from LASM02-03T4-G to BAT54WAPT for seconf source test
P.57 Change PU2 from MAX1999EEI+ to MAX8734AEEI+
P.58 Modify PJ5,6,7,8 allegro symbol from 80mil width to 40mil(change footprint to OPEN2B)
P.58 Change PD14,15 from SK0003-03T-G to CH751H-40PT for seconf source test
P.58 Change PL10 from SPD1005PT3R8N-7A to MPLC1040L3R3
P.58 Change PL11 from SPD1005PT1R5N-10A to MPLC1040L1R5
P.58 Change PQ28 from Dual mosfet IRF7904 to IRF7807Z
P.58 Add PQ97 IRF8113 for power budget change
P.58 Change PU3 from MAX1845EEI+ to MAX8743EEI+



FOXCONN			HON HAI Precision Ind. Co., Ltd.
History (1)			CCPBG - R&D Division
File	Document Number	Rev	
C	MS10-1-01 (MBX-149)	1.00	
Date:	Tuesday, December 20, 2005	Sheet	66 of 74

(2005/06/24) Power circuit modify

P.59 Change PD16 from SK0003-03T-G to CH751H-40PT for seconf source test
P.59 Del PR100 0_J 0402 , Add GP12 close jump for separate A GND and P GND
P.59 Modify PJ9,10,11,37 allegro symbol from 80mil width to 40mil(change footprint to OPEN2B)
P.60 Del PR120 470_J 0402 and PQ36 and H_DPRSTP# signal & PJ41
P.60 Change PD17 from SK0003-03T-G to CH751H-40PT for seconf source test
P.60 Change PD18 from SKS30-04AT-G to SSM34APT for seconf source test
P.60 Del PR133 0_J 0603 , Add GP13 close jump for separate A GND and P GND
P.61 Change PD44 from SK0003-03T-G to CH751H-40PT for seconf source test
P.61 Change PD45 from SKS30-04AT-G to SSM34APT for seconf source test
P.62 Change PQ50,52 from FDC653N to IRF7402PBF for power budget change
P.62 Del PR344 0_J 0402 ,PJ36 (cause H/W request in EVT need use +1_5VRUN and +1_05VRUN) So mount parts of PQ53,55
P.62 Change PU19 from MAX1615EUK+ to MAX1616EUK+ make 8V for load switch turn on
P.62 Del +1_5ALW circuit of PU9,PJ29,PC171,PC173,PC170,PJ30

P.63 Change PD25,26,27,28,29,30,31,32,33,35,36,37,38,39,41 for second source test in EVT.
P.64 Modify PJ32,33,34,35 allegro symbol from 80mil width to 40mil(change footprint to OPEN2B)
P.64 Add PC359,360 for EMI (6/23 Jacky Su request)
P.64 Change PD42,43 from SK0003-03T-G to CH751H-40PT for seconf source test
P.64 Change PU16 from MAX1845EEI+ to MAX8743EEI+

(2005/06/27)Power circuit modify

P.58 Change PR68 from 0_J 0402 to 0_J 0603
P.59 Change PR332 from 0_J 0402 to 0_J 0603
P.63 Change PR361 from 0_J 0402 to 0_J 0603
P.60 P.61 Del MAX8736ETL+ and MAX8552ETB+ solution then add P.60 Change to MAX8771ETL+ for new two phase power controller.
P.62 Del PJ27

(2005/06/27)

P.33 Del R636 for thermal SPEC change
P.42 Add C1222 for CAM power drop issue
P.52 Change Y7 part value to 6MHZ_20P_30PPMM
P.51. Del RUN_ON net name (primily reserved)
P.52 Change U89,R1312,R1239,R1300,C1187 TO NC(do not install)
P.28 Del net name BRADJ_EC and del R445 reserved
P.37 Change pin U32.43 net name from BRADJ_EC to tast point
P.36 Move R1304 to P32 and change net name from PATAADD_LED# to SATA_LED# & change CN32 to NC pin
P.40 Modify CN18.18pin connect to GND ; connect CN18.44 pin to MINI_CARD_LED
P.40 Add R1317 and SW16 for BT & WLAN function SW
P.39 CN44 ,CN45 ,CN46 pin define modify , still need to confirm ID status
P.49 Change CN26 connect to FOX_QT8A0121-1011-8F
P.24, P25 Change U11,U12,U13,U14 for 350 MHZ VRAM

(2005/06/28)

P.42 Change R772 to NC(do not install)
P.41 Del R1098 reserved resister

Audio circuit modify

PS : Remove orginal P54 (HOLE) to P64 ; add one audio page and also arrange PCMCIA , power circuit page number
P.43 Change C1203,C1204,C1205,C1206 to 820pF
P.43 Change net HP_SPK_L,HP_SPK_R to HP_OUT_L,HP_OUT_R
P.44 Change net HP_SPK_L,HP_SPK_R to HP_OUT_L,HP_OUT_R
P.43 Add net SPK_L,SPK_R from U39 PIN16,PIN17
P.44 Change net HP_SPK_L,HP_SPK_R to SPK_L,SPK_R
P.46 Add INT MIC amp circuit block
P.46 Add Mechanical selecter block
P.47 PHONE-OUT change from signal-ends to differential , add PHONE-OUT differential block
P.44 Add C1223,C1224,C1225,C1226,C1227,C1228,C1229 33pF capacitor for RF noise
P.45 Change R1288,R1289,R1294,R1295 from 1K to 2.2K

(2005/06/29) Power circuit modify

P.60 Add PR390 NC_0_J 0402 resister

(2005/06/29)

P.32 Change R1206-R1208 from 110 ohm to 22 ohm same as MS01's value
P.37 Connect U32.99 "DOCK_RST_100MS#" to P.52 CN30.98
P.33 Change R1256 value from 100 ohm to 0 ohm
P.37 Del U32.174 pin EC_DOCK_MUTE and del CN30.97 EC_DOCK_MUTE
P.40 Add R1357 pull high to +3VSUS and change net name from MINI_CARD_LED to MINI_CARD_LED#
P.32 Modify R698 to 61.9 ohm 1% and add R1358 parallel R608 for SATA amplitudel over SPEC
P.32 Change R585 from 100K ohm to 20 K ohm for RTCRST# tming verify
P.31 Swrap RP92 , RP94,RP93 pull high net name for layout routing convenience
P.24 ,25 short R359 ,R360 ,R380,R381
P.24 ,25 Del R364 , R365 ,R382 , R386 two BANK VRAM reserved

(2005/06/30) Audio circuit modify

P.43 Add R1359 10K_J 0402 resister
P.43 Add C1253, C1254,C1249, C1251 33P_50V_K_N 0402 capacitor
P.43 Add C1250, C1252 12P_50V_K_N 0402 capacitor
P.43 Add C1248 1U_6.3V_M_B 0402 capacitor
P.44 Add D70 PACDN042Y3R ESD Diode
P.45 Change R851,R861 to 2.2K_J 0402 resistor
P.45 Change R848,R857 to 22K_J 0402 resistor
P.45 Change C913, C922 to 2.2U_10V_M_B 0805 capacitor
P.46 del R1112
P.46 del U70
P.46 del Testpad TP304
P.46 Change C1232 to 2.2U_10V_M_B 0805 capacitor
P.46 Change R1319 to 2.2K_J 0402 resistor
P.46 Change R1318 to 22K_J 0402 resistor
P.46 Add C1255 220P_50V_K_N 0402 capacitor
P.46 Change R1318 to 22K_J 0402 resistor
P.46 del U98A,U94B, U95C
P.46 Add U103,U104, U50,U105
P.47 Change R1332,R1335,R1329,R1330,R1333,R1334 to 10K_J 0402 resistor
P.47 Change C1241 to 4.7U_10V_Y_Y 0805 capacitor
P.47 Change R134,R1351,R1337,R1339,R1349,R1350 to 10K_J 0402 resistor
P.47 Change C1247 to 4.7U_10V_Y_Y 0805 capacitor
P.47 del CAP24,CAP25,CAP26,CAP27
P.47 Add C1256,C1257,C1258,C1259 4.7U_6.3V_K 0805 X5R capacitor
P.47 del Q82,Q83,Q86,Q87,Q88,Q89,Q90,Q91
P.47 del R1276,R1277,R1298,R1299,R1353,R1354,R1355,R1356

(2005/06/30)

P.50 Change Q56 S & D connetion for voltage leakage
P.19 Change C1216 location to L102 righ side
P.3 add JIG_SMI# in CN15.29 &U32.89 pin , add EC_BRADJ U32.43
P.37 Add R1362 ,R1363 and change Q24 ,Q26 for PWRGD fail issue

(2005/06/30) Audio change

P.45 Add R1369 0_J 0402 for mechanical switch solution
P.46 Add R1372 NC_0_J 0402
P.46 change U103 to TC7SET04FU
P.46 change U104 to SN74AHC1G14DCK
P.46 Add U105 TC7SET04FU
P.46 Del R1112
P.46 Del U70 TC7SET32FU

(2005/07/01) Audio change

P.43 Del R803
P.43 Del C872,C1194,C1195
P.43 Change C873 to 1U_25V_Y_Y 0805
P.43 Change C869 to 10U_10V_M 0805 X5R
P.43 Change U41 to MAX1818EUT50
P.43 Del Y6 Xtal
P.43 Add R1364 0_J 0402
P.43 Add C1262 33P_50V_K_N 0402
P.43 Add C1263 12P_50V_K_N 0402
P.44 Add C1264 0.1U_16V_M_B 0402
P.44 Add C1265 0.1U_16V_M_B 0402
P.44 Add C1263 12P_50V_K_N 0402
P.44 Change C1229 to 0.47U_6.3V_K_B 0402
P.44 Change C878 to 0.1U_16V_M_B 0402
P.44 Add R1336 10K_J 0402
P.44 Del C1197,C1224,C1196,C1223
P.44 Del R1278,R1279
P.44 Add R1368 10K_F 0402
P.44 Add R1367 5.6K_F 0402
P.44 Add R1365 0_J 0402
P.44 Change U66 to TPA6011A4PWRG4
P.46 Change R1249 to 560K_J 0402
P.46 Add R1370 470K_J 0402
P.46 Add R1371 47K_J 0402



FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
File History (2)			
Size	Document Number	Rev	
C	MS10-1-01 (MBX-149)	1.00	
Date:	Tuesday, December 20, 2005	Sheet	67 of 74

(2005/07/04)

P.52 CN30 Docking pindefine change for Docking layout critical

P.19 Delete R1261 for NV43 reserved

P.20 Delete C402, L92, C403, C405, L94, C419, C421,C431, C433, R271, R275,L107, L108 for NV43M reserved

P.21 Delete L21, C467, C468, C469,C487, R299, R300, R297, R1104 for NV43M reserved

P.53 Change Y7 to AKER_CXB-006000-7X4X2 for small size ; add R1373 , R1374 for EEPROM select

P.30 Change CN6 pin 3 & pin 4 signal for S-Video fail issue

P.39 Del CN17 and make Touch Pad to D/B

P.64 Change screw hole size for new ME drawing

P.39 Change CN44 to 8 pin MOLEX _52893-0895 ; modify CN45 pin define

(2005/07/05) Audio circuit modify

P.43 Change C862 to 10U_10V_M_B 0805 X5R

P.44 Del C1228

P.44 Change C1092, C1093 to 2.2U_10V_Y_Y 0603

P.44 Change C1225,C1226 to 0.1U_16V_Y_Y 0402

P.45 Change R1290,R1293 to NC_0_J 0402

P.46 Del Q75

P.46 Del R1249,R1371

P.46 Del U97

P.46 Add Q87

P.46 Change Q81B to Q76B

(2005/07/05)Power circuit modify

P.57 Add PJ29 jump for ECVCC separate with system

P.57 Add PC 364 ,PC365 for solve Inverter audio noise.

P.57 Change PR64 from 147K_F 0402 to 47K_F 0402

P.57 Change PR65 from 100K_F 0402 to 56K_F 0402

P.58 Change PR80 from 75K_F 0402 to 33K_F 0402

P.58 Change PR79 from 61.9K_F 0402 to 39.2K_F 0402

P.59 Change PR305 from 5.1K_F 0402 to 5.6K_F 0402

P.59 Change PQ31 from IRF7807Z to IRF7821

P.59 Change PQ77,PQ78 from IRF7832 to IRF8113

P.60 Add PR115 0_J 0402 resister

P.60 Add PC126,PC127 1000P_50V_K_B

P.60 Change PR337,PR339 from 0_J 0402 to 3.3_F 0603

P.60 Del PR139 , PC247 same Evkit

P.60 Add PTP16

P.60 Add PR294 100_J 0402

P.60 Add PR390 10K_F 0402

P.60 Change PR272 form 2K_J 0402 to 100K_F 0402

P.60 Change PC113 form 0.1u_25V 0603 to 0.22u_16V 0603

P.60 Add IMVP_PHASEGD signal

P.61 Change PR373 from 80.6K_F 0402 to 56K_F 0402

P.61 Add PR344 NC_0_J

P.61 Add PJ36 OPEN_JUMP_OPEN2B

P.62 Del PC324 , 325 same MS03 setting

P.63 Change PR226 from 61.9K_F 0402 to 47K_F 0402

P.63 Change PR227 from 33.2K_F 0402 to 39.2K_F 0402

P.63 Change PR217 from 1.58K_F 0402 to 560_F 0402 for 1.025V setting

P.63 Change PR224 from 10K_F 0402 to 22K_F 0402 for 1.025V setting

P.63 Change PL18 from SPD8D28PT4R7N to SPD8D43PT100M

P.63 Change PQ74,PQ75 from IRF7832 to IRF8113

P.60 Change PL13,PL21 from MPC1040LR56 to MPC1040LR36

(2005/07/05)

P.24 Change net name U11.M4 to VRAM1_NC2 ,U12.M4 to VRAM2_NC2

P.32 Change net name R1206 , R1207 ,R1208 LAN signal to correct

P.44 Change CON2 to FOX_JA9333L-000G2 for ME issue

P.45.Change CON3 to FOX_JA9333L-000R1 for ME issue

P.42 Change CN20 to FOX_HS6104E

P.42 Change CN20 to FOX_HS6104E

P.30 Change CN6 pin 3 & pin 4 signal for S-Video footpring modify

P.29 Del R1135

(2005/07/06)

P.46 Change Q86 to MMBT3906(PNP)

P.46 Add R1376 10K_J_0402

P.46 Add Q86 NC_DTA114YUA

P.47 Add Q89,Q90,Q91,Q92 for reservation

P.47 Change R1296,R1297,R1272,R1274,R1341,R1342,R1345,R1346 to 33_J_0402

P.37 Change R698 ,R699 from 10k to 4.7K ohm

P.22 Mount U8 , R286 , R289 thermal sensor ; change R308R310 , R323 ,R324 ,R315, R317,R320,C491-493 to NV_0 condition

P41. Add R1377 , LED9 ,Q93 ,Q94 ,R1378 , R1379 for BT's LED on board

P40. Del R1357 , add Q95 , R1380 , LED10 for WLAN on board and modify
P.39 CN46 connector pin define

P.37 Add RP99 10K for TOUCH PAD

(2005/07/07)

P.28 Add CN49 interver connector and change CN3 to 30 pin (for LVDS cable burn issue)

P.37 Move HW_POP_MUTE_EC to U32.174 pin ; add D_PWRGD netname in U32.62 & CN30.57 ; Del U32.87 BOOT_MODE# net name

P.52 Add HDCP_SCL,HDCP_SDA net name in CN30.58,59 and change U82 to NC

P.5 Change R65 ,R74 left side net name to CPU_BSEL0 ,CPU_BSEL1

P.5 Change C729 to NC_10U_6.3V_M

P.41 Del R769 reserved R

P.42 Change C849 , C848 to NC condition

P.44 Change C1266-1268's GND to analog GND

P.40 Change LED10 to HT-110UYG 90 degree for ID issue

P.41 Change LED9 to HT-110UYG 90 degree for ID issue

P.38 Del CN15's H_CPU_RST# signal for layout issue

P.42 Move R1315 ,R1316,L111 to EXPRESS CARD's CLK signal

P.42 Add R1381 , R1382 reserved R

P.10 Change CAP5,6,8 to EEFU00D471LG

P.43 Add C1270 decoupling capacitor

P.43 Change U41 to TPS79301DBVR (Audio power 4.75V/200mA)

P.43 Change C887 to 0.01U_25V_M_B

P.43 Change R801 to 30K_F 0402

P.43 Change C869 to 4.7U_10V_Y_Y 0805

P.3 Add C1271~ C1280 decoupling capatitor for EMI reserved

P.46 Change U50 to 74AHC1G08GW

P.36 Add C1281 10 uF capacitor and change CAP21 to NC condition

P.39 Add C1282~ 7 0.1uF in D/B power source for EMI

P.40 Add R1283 to correct connection

P.40 Del C817 , C018 capacitor

P.52 SWAP PHONE_OUT_R+ ,PHONET_OUTR- in CN connector

P.54 U90 change to AT93C46-10SU-2.7

P.53 Change AKER_CXA-751 6MHz to 4 pin

P.29 Change D7 to BAS316 for small size

P.3 Change R26 to 51ohm for Intel document update

P.52 Add PM_RSMRST# in docking connector

P.41 Change Q93,Q94 to PDTCT144EU and del R1154,R1155

P.21 Change U86 to Q96 MOSFET 2301

P.39 Add SPR3,SPR7 for EMI solution

P.43 SWAP pin U39.39,41 and U39.35,36 ;Add Gp14,L112 for EMI

P44 Add L113,L114 for EMI request

(2005/07/07)Power circuit modify

P.56 Change PD2 to MMP25250BFPT

P.58 Change PR79 to 47K_F 0402, PR80 to 120K_F 0402

P.58 Del PQ97

P.58 Change PQ28 to IRF7904

P.60 Mount PC245,PC248

P.62 Change PU10 to S-80925CNMC-68V-T2G

P.60 Del PTP6 , 8,9,10,11,12 reduce layout space

(2005/07/08)

P.42 SWAP L111 signals for layout routing smooth

P.64 Change H3 screw hole for ME request

P.50 Del C979 , C976 ,C975 ,C977 capacitor

P.52 Del docking connector netname " DOCK_SATA_CLKREQ#,PWRLIMIT# "

P.5 Del R41 for DOCK_SATA_CLKREQ# reserved R

(2005/07/09)

P.37 Add U106 ,R1348 for docking reset timing

P.39 Change SRP3,SRP7 type for EMI request

(2005/07/09) Power circuit modify

P.58 Change PR70,71,75,76 from 0603 to 0402

P.58 Change PR79 to 36K_F 0402

P.59 Change PQ77,78 to PQ77 mount IRF7832 , PQ78 NC

P.59 Change PR305 to 6.49K_F 0402

P.63 Change PR227 to 36k_F 0402

(2005/07/11)

P.21 Q96 Swap for leakege voltage

(2005/07/12)

P.34 Add 0 ohm R for VccSATAPLL

P.22 Add R1385,R1386 pull high for DVI "I2CB "

P.43 Modify R801 to 29.4K ohm

P.53 Change U52 to AT93C46-10SU-2.7 for use the same BOM

P.42 Add PWRSW# signal to CN15

(2005/07/12) Power circuit modify

P.61 Change PQ53,PQ55 to IRF821PBF

P.63 Change PL18 to CDRH8D38NP-4R7NC



FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title	History (3)		
Size	Document Number		Rev
C	MS10-1-01 (MBX-149)		1.00
Date:	Tuesday, December 20, 2005	Sheet	68 of 74

(2005/07/12)
P.64 Add R1387 and net name DOCK_SATA_CLKREQ# to docking connector
P.41 LED9 change to HT-110NB

(2005/07/14) Audio circuit modify

P.43 Change C1154 from 0.1uF 50V to 0.1uF 16V
P.43 Add C1290 0.1uF 16V_Y_Y ; change C855 close codec side
P.43 Add C1288 0.1uF 16V_Y_Y : connect SENSE_A to GND
P.43 Add C1289 0.1uF 16V_Y_Y : connect SENSE_B to GND
P.43 Replace GP14 Close Jump with R1388 NC_0 ohm 0402
P.44 Replace CAP13 to C1291 NC_10uF 6.3V_X5R 0805 and connect to DGND for Test
P.44 Change C877 to 10uF 6.3V_X5R 0805
P.44 Change R1185, R1186 to 0ohm 0402
P.44 Change CAP22,CAP23 to shoei A1 CAP

P.65 Change H5's GND to CHASSIS_GND for EMI request

(2005/07/15)

P.44 Connect C1266, C1267, C1268 & C1269 to AGND
P.37 Change CN12 from FOX_GB20240-0001-7F to FOX_GB20240-0002-7F for KBC drop in SMT issue

(2005/07/19)

P.52 Change CAP19,17,18 from 7343 size to 6032 size
P.38 Del CN14.32 net name BOOT_MODE#
P.50 Del R950 47 ohm for SD fucntion drop
P.37 Change R698 , R699 to 10K ohm
P.52 Add R1389 pull high R for PCMCIA issue

(2005/07/20)

P.63 Del PC205 for layout space issue
P.59 Change net name from 1V8/15A to 1V8/15.5A
P.54 Change R1210,R1305 from 100ohm to 110ohm for INTEL FAE suggest

(2005/07/21)

P.64 Change H15 screw hole for ME request
P.28 Add U106,R1390 for voltage level shift
P.37 Change net name SUSPEND_LED# & POWER_LED to SUSPEND_LED & POWER_LED
P.56 PD5,9 Change to PACDN042Y3R

(2005/07/24)

P.37 Del CN12 Pin 25,26 connect to GND ; Del TP114

(2005/07/25)

P.52 Change R1301 pull high from +3VSUS to +3VALW



FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title History (4)			
Size A3	Document Number MS10-1-01 (MBX-149)		Rev 1.00
Date:	Tuesday, December 20, 2005	Sheet 69 of 74	

DVT (2005/09/05)

PS : For S3 hot change to S3 cold :

Change all power plane form +1_5VSUS ,+1_05VSUS to +1_5VRUN and +1_05VRUN power plane

Change VGA & VRAM's power source from +1_8VSUS to +1_8RUN

Change most of power source from +3VSUS to +3VRUN expect chip TI7412 and other small portion

Change most of power source from +5VSUS to +3VSUS , but not all

P.27 Change C575 , C605 to NV_10U_6.3V_M
P.48 Seraprate C954 ,C955 to the different U58's pin
P.49 R934,R940,R955 change to 1K ohm for TI's reference design update
P.10 Del A1001 conection from R138 to D4 ; change L4 to HCB2012KF-121T30 for +1_5V drop issue
P.40 Change R1067 from MINI_PCIE_+3_3V to +3VALW for support WOL S4
P.34 Change R657 's power from +3VSUS to +3VALW for support WOL S4
P.54 Change L101,U90's power source from +3VSUS to +3VALW
P.33 Change U29 pin C29 to PM_RSMRST# for support S4 WOL and add R1391 0 ohm R
P.3 Change Q4 to MMB3904 and add R1392 (2.2K ohm)for PM_THRMTRIP# can't turn on issue
P.64 Swap U18 pin 58 & pin 64 connection for ICH clock free run
P.50 Short CN26's pin 2 & pin 6
P.29 Add R1394,R1394 pull down R for S4/S5 float issue
P.7 Add R1309 for intel reference design update
P.12 Del R162 for Intel's A02 CPU update
P.23 Change R330 , R331 to 124 ohm for Nvidia's suggestion
P.22 Add R1401-R1404 for Nvidia's JTAG can't floating issue
P.37 Del R718,Q25,R726,Q26,R1363,R706,Q23,R707,R1363,Q24 for S3 hot extra power good
Add NV_ mount condition to correct for U7,U11,U12,U13,U14,R1263,C322,C323,CAP10,Q7.
P.10 Change C141,C142 to 10uF C
P.23 Modify R354,R355 to NC
P.37 Change U32.118 pin ,R691 from SUS_ON1 to RUN_ON1
P.37 Change U32.48's net name to RUN1_PWRGD
P.20 Add C1293 ,C1294 for EMI request
P.22 Add R1405 100 ohm pull-down R to solve DDE_ALERT# always keep low issue
P.34 Short U29.AB17,AC17,T7,F17,G17,AB8,AC8 and del GP6,GP7,GP8 for progress power plane
P.33 Del R1184 for power sequence verify
P.29 Add C1295-C1301 for EMI request
P.65 Change H5's GND to A_GND
P.54 Del CN40 pin 8,9 GND
P.39 Change CN44 to foxconn vendor but pin to pin compitable with MOLEX
P.14 change R176 net name from PM_EXTTS#1 to PM_EXTTS#0
P.22 Change C1139 to NC condition
P.52 Change CN30 to FOX_QL0150L-D24A01-5F (add GND pad)
P.10 Change L4 to HCB2012KF-121T30 for voltage drop issue
P.28 Change R1268 , U106,R1390 mont condition
Audio circuit modify
P.43 Change C863 from 1uF 10V to 10uF 10V (Sigmatel: For anti-pop noise)
P.43 Change C857 from 4.7uF 6.3V to 10uF 10V (Sigmatel: For better performance)
P.43 Add C? 0.1uF 16V_Y_Y on Port-B (Non use Input port should connect to GND through 0.1uF)
P.43 Add Q?, Q? & Q? for Jack sense circuit.
P.43 Add R? 39.2K_F 0402; R? 10K_F 0402; R? & R?10K_J 0402; R? & R? 5.1K_F 0402 for Jack sense circuit.
P.44 Change R1367 5.6K_F to 6.2K_F (Set AMP gain = 10dB)
P.45 Del R1290, R1293, R1369, R1294, R1295 & C1172 (One Verf for MIC is enough)
P.46 Del U105 (HW_POP_MUTE_CODEC change to Active High)
P.46 Del R1375 (One MIC Verf is enough)
P.46 Del U100 & R1372 (MIC Switch is not needed)
P.44 Change CON2 connector to black color



FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title History (5)			
Size A3	Document Number MS10-1-01 (MBX-149)		Rev 1.00
Date:	Tuesday, December 20, 2005	Sheet	70 of 74

(2005/09/12)

P.52 Change CN30 to FOX_QL0150L-D24A01-5F (add GND pad)
P.36 Change CN32 to FOX_QT8H0506-H111R-4F
P.39 Change CN15 to FOX_QT510306-L011-7F for connector easy broken issue
P.42 Modify CN19 layout symbol(add 2 fixed GND for connector easy drop issue during SMT re-flow
P.28 Change U17 to G548
P.43 Del C1292 and del U39.21,U39.22 connection
P.43 Change U39 to co-lay packeage
P.49 Change CN23 to FOX_UV31413-WR56P-7F for reserve type
P.37 Add R718 , R726 , R1363 for S3 hot reserve
P.50 Change C982 from 10uF to 4.7uF and add R1406 for dischage
P.37 Change R698 , R699 from 10K ohm to 4.7K ohm and add R1407 , R1408 for SM Bus measurement fail issue
P.32 Del U29 SATA2 connection to docking
P.65 Modify H17 , H22 ,H1,H2,H18,H15,H14,H13,H21,H5,H16
P.20 Add C1302 for EMI request
P.28 Change R461 from 330 to 200 ohm
P.52 Add CN30 pin2 connection RUN_ON

(2005/09/13)

P.19 Change C1192 to 0603 size
P.10 Bypass R130 ,R136 0 ohm R
P.22 Del R1133 pull-low R and move R458 from R457pin1 to R457 pin2 location
P.34 Del R655 0ohm R
P.40 Change R1317 and R1067's power source to +3VSUS
P.41 Change R1377's power source to +5VRUN and del Q94
P.42 Del R772,Q35,R774 reserve circuit ; bypass R1096 0 ohm R

(2005/09/14)

P.33 Del R1183 0ohm R
P.52 Del CN30 pin 58,59 connection
P.37 Del U32 " BIOS_CRISIS# " , U32.20 " FWH_BOOT" connection
P.38 Del CN15 FWH_BOOT connection and del R735
P.28 Del GP11 and R771
P.39 Swap CN44's pin 6 and pin8 connection
P.40 Change SW16 vendor to Foxconn
P.42 Change Q79's power to +5VSUS
P.42 CN19 pin 11 name to PCIE_EXPRESS_WAKE# and connection
P.33 Add Q100 , GP14 for EXPRESS wake pin leakage voltage prevent
P.39 Change CN46 conection to U58.F8 pin
P.50 Modify U58.C8 , Q56 net name to MC_PWR_CRT_0
P.32 Change R602 value to 24.9ohm and del R1358 for SATA SI measurement

(2005/09/16)

P.33 U29.C19 net name to SUS_PWRGD_10MS for LAN don't not support S4 WOL
P.34 Modify R657's power to +3VSUS for LAN don't support S4 WOL
P.54 Change L101 , U90's power source to +3VSUS for LAN don't support S4 WOL
P.37 Change CN12 to FOX_GB21240-0002-7F
P.53 Change Y7 to TXC vendor

(2005/09/19)

P.8 Modify R120 mount condition
P.8Add R1409~R1415 for Intel's update
P.10 Modify R131,C132,C133,D3,R132,R136,C152,C153;and Add R1416,R1419
P.50 Modify MS's power circuit add Q101 ;modify R1047 ,Q56 value and del R1406
P.5 Del R27 0ohm R
P.37 Change R718,R726's power source to +3VSUS



FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title History (6)			
Size A3	Document Number MS10-1-01 (MBX-149)		Rev 1.00
Date:	Tuesday, December 20, 2005	Sheet	71 of 74

P.22 Change R286 mount condition to NC
P.28 Del R445 and BRADJ_EC line
P.34 Del GP9 ,R670,R667,R1384,R676,R674,R668,R666,R662

(2005/09/20) DVT power modify

P.56 Change PR379 to 1K_F 0402
P.56 Change PR363 to 10K_J 0402
P.56 Add PR392 to NC_0_J 0402 ,PR393 to 0_J 0402
P.56 Add PR391 22k_J 0402 ,PR394 33k_J 0402
P.56 Change PC337 to 0.01U_50V 0603
P.56 Change PR26 to 20k_F 0402
P.56 Change PC37 to 470p_50V 0603
P.56 Change PD11 to MMVZ5235BPT
P.56 Add PR406 56k_J 0402
P.56 Change PC336 to 1U_25V 0603
P.56 Del PR15,16 ,move to H/W side/ close KBC
P.56 Change PC9 to 47p_50V 0402
P.57 Change PR47 to 0_J 0805
P.57 Change PC47 to NC_4.7U_25V
P.57 Del PJ1,3,2,4,29
P.58 Change PR68 source to +5VSUS
P.58 Del PC78,79
P.58 PG00D pull high source change to +3VRUN
P.59 Del PC349
P.59 Change PC311,312 to EEFUD0D471LG
P.59 Del PJ9,10,37,11
P.59 PG00D pull high source change to +3VSUS
P.60 Change PC112 to 100p 50V 0402
P.60 Change PR272 to 2k_J 0402
P.60 Change PC125 to 0.01U_25V 0402
P.60 Change PR130 to 10_J 0402
P.60 Change PR336 source to +5VRUN
P.61 Change PQ50,52 to SI2316DS
P.61 Change PQ53 D ans S to +1_8VSUS and +1_8VRUN
P.61 Change PQ55 D ans S to +1_05VSUS and +1_05VRUN
P.61 Add PR410,411,412,413,399,398,408,409, PQ105,98,97,99
P.61 Del PJ28,40
P.61 Change PU8 enable signal to RUN_ON1
P.63 Change PR361 source to +5VSUS
P.63 Change PU16 enable signal to RUN_ON1
P.60 Change PR387 to 3k_F 0402

(2005/09/20)

P.20 Change R272 to 30 ohm for nVIDIA's suggestion
P.41 Change R1377 to 200 ohm
P.41 Add U107 , R1420 ,R1421,R1422,R1423,C1304,C1305,C1303 and change Q33 ,C827
P.38 Change U34 to EN29LV800BB-70TCP
P.37 Modify R726's power source to +3VALW
P.37 Change R698,R699,R1180's power source to +3VALW
P.39 Change R756's power source to +3VSUS
P.39 Change SPR2,SPR3,SPR6
P.21 Modify C474 mount condition to NC
P.22 Modify C488 ,C489,R292 mount condition to NC_
P.23 Change R339 mount condition to NC

P.19 Modify R305 mount condition to NV72_
P.20 Modify L95 ,C422,C424 mount condition to NV73_
P.25Modify U13 ,U14,R383 ,R389 ,R391 , C507,R399,R400 , R390,R392,C508 to NV73_
P.26 Modify mount condition to NV_73 all page
P.24 Modify R361 ,R363 mount condition to NVS_
P.25Modify R383 , R384 mount condition to NV73S
P63 Add PR414 , PR415 and modify PR217 ,PR224 mount condition

P.38 Add C1306

(2005/09/21)

P.50 Swap Q101 pin E & C and add R1425
P.54 Change R1307 to 620 ohm
P.8 Add R1426 ,R1427 pull high R
P.43 Modify R1359 to pll low
P.44 Change R847 ,R852 to 10K
P.52 Add U30 pin 5 ,pin 6 connection to U32.20,87
Modify PR64 to 51K ,PR305 to 8.2K,PR387 to 3.24k
P.37 Change R718's power source to +3VRUN ; R1180 to ECVCC
P.52 Modify CN30.71 & U32.99 net nace to DOCK_RUN_RST
P.52 Modify CN30.5 & U32.20 net name to AND_DOCK_S5_RST_100MS#
P.37 Add IAC_RESET#_AUDIO net to U32.83
P.22 Add R1428 and modify R1131
P.43 Change C1270 to 1uF
P.47 Change C1238 ,C1242 to 270pF
P.62 PR207 change to 1R-0006342-F200(63.4K)

Final BOM until above

Need to release E-ECN to factory
P.10 Add R1429 0 ohm
P.43 Add R1388 0 ohm to BOM
P.8 Add R1430 ohm
P.31 Connect U29.AE5,AD5,AD9,AE9 to GND
P.21 Change C480 to NC
P.7 Add R1431 ,R1432 ,1433 , R1434 NV_ for Intel's seggestion
P.64 Change R1129 ,R1130 to NC condition
P.34 Del R1384 0 ohm ; add L115 (10uH) , C1307 (10uF)

(2005/09/23)

P.48 Change R926 mount to NC
p.36 Add CN32.51 to GND
P.8 Del R1221 , R1411 ,R1412 ,R1413 R1430



FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title History (7)			
Size A3	Document Number MS10-1-01 (MBX-149)		Rev 1.00
Date:	Tuesday, December 20, 2005	Sheet 72 of 74	

**PVT start
(2005/10/12)**

P.62 Change PR207 to 41.2K ohm
P.61 change PC175 to 0.047uF
P.46 Mount Q88 for pop-noise
P.47 Mount Q91,Q92 ,R1340,R1344 ,Q89,Q90,R1273,R1281 for pop-noise
P.30 Change U72 , U73 to MC74VHC1G86DFT2G
P.7 Change R110 mont condition to NC
P.29 Change D7 to SK03-04T-G for D_SHIFT_+5V drop issue
P.58 Change +1_5VRUN's enable singal from RUN_ON1 to RUN_ON
P.22 Change Y2 27MHz from 30 PPMto 20 PPM
P.10 Change L7,L8 ,L115(P.34) to MAX ECHO vendor
P.39 Change U35 to MC74HC1G32DTT1G
P.46 Change U45 , U83 to MC74VHC1GT32DF2G
P.46 Change U103 to MC74VHC1GT04DF
P.49 Change L71,L72,L19,L20,L90,L91,L93,L95,L102,L103,L104,L105,L106 to EBMS160808A121
P.34 L60 ,L70(44) change to BCMS321611A121 5A
P.41 U107 pin 8 change from 8V to DCBATOUT for FAN can't full on issue for DVT short term solution
P.54 Change R1307 to 649 ohm
P.61 PQ53 change to IRF8113
P.37 Change R703 , R704 from 47K ohm to 470K ohm

(2005/10/29)

P.41 Change U107 to rail to rail type and swap pin2 & pin3 connection ; change Q33 to P-MOS
P.10 Change CAP5 , CAP6 mount condition to CA_
P.33 Change U30 pin 2 conection to EC_CLKEN# and add R1435 pull up R
P.37 Add U32 pin 105 EC_CLK_EN#
P.40 Change Q95 pin1 power source from +3VRUN to+3VSUS
P.64 Change Clock GEN's pin2 to EC_CLK_EN#
P.44 Swap JSPK1's pin define

(2005/11/03)

P.21 Q96, P41 Q33 ,P42 Q79 update MMC2301 layout footprint
P.39 Add J1 for factory request
P.29 Change CN4 to FOX_DZ11A91-NW205-4F for ID request
P.51 modify CN48's part number
P.42 Change CN47's part number

(2005/11/07)

P.52 Mount R1243,R1244,R1247,R1248 and change R1194 ,R1195 , R1198,R1199 to 0ohm R for no Oide SKU ; change the others to NC on this page
P.42Change CN21 , L67 ,C1086 ,R782 ,R787 to NC for no Oide SKU
P.41 Change C827 to 22uF for FAN VCC quality ; add D71
P.64 Change U18 to B version
P.52 Change CN29,CN28,CN37 to FOX_UB1112C-C1603-FR for ID request
P.30 Change CN6 to FOX_MH11747-PS2D-4F for ID request
P.49 Chagne CN23 to FOX_UV31413-VR56P-7F for ID request
P.28 Modify CN3 connector (add two dummy pad)
P.37 Add R1436 pull down R
P.41 Add C1308 reserve C

(2005/11/10)

P.37 Reserved R1438 ,R1437 , R1439 ,R1440 ,Q102 for RS11 reserve
P.39 Change SPR2,3,6 to 5.0X2.5

(2005/11/12)

P.39 Change CN44 pin1 to SUSPEND_LED and del C1285
P.37 Add R1441 0 ohm R on U32 pin 105 ; change R703 ,R704 to 470K ohm
P.37 Change U32.99 pin & CN30.71 pin net name to DOCK_RUN_RST#
P.37 Add R1442 pull up R ; change R703 , R704 to 47 K ohm



FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
History (8)			
Title			
Size	Document Number	Rev	
A3	MS10-1-01 (MBX-149)	1.00	
Date:	Tuesday, December 20, 2005	Sheet	73 of 74

(2005/11/14)
P.64 Add R1443 ,R1444 2.2ohm R
P.43 Change U39 to Kversion
P.52 Change CN30.5 name to AND_DOCK_S5_RST_500
P.52 Change CN30.26 name to DK_BAY_PWREN
P.43 Change C863 to 1uF for pop noise
P.46 Change C1188 to 4.7uF for pop noise
P.44 Change Q77 , Q78 ,Q84, Q85 to PBSS2515 for procurement issue
P.47 Change Q89 , Q90 ,Q91, Q92 to PBSS2515 for procurement issue
P.33 Del R649
P.48 Change U58 pin j2 CN46 pin 10 net name to MS_LED
P.31 Change R579,R580,R581's power souce to +3VSUS

(2005/11/14) Power modify

P.56 Add PC370 connect PQ11 pin3
P.56 Change PR391 to 10K_J ,PR349 to 15K_F same MS20 setting
P.59 Add PC371 connect to +1_8VSUS back up for output ,no mount
P.60 Add PR416 0ohm R and del PR272 pull up R
P.61 Change PR410 , PC369 , PQ105 , PR411 , PR413 to NC condition
P.61 Change PQ104 pin1 net name to A6703

(2005/11/15)

P.44 Bypass R1186 , R1185
P.43 Add R1445 , Q103 and add P.61 A603 port
P.43 Add R1446 , R1447 , R1448 ,R1449 mount option
P.36 Add R1450 reserved R
P.64 Del R1443 , R1444 to 0ohm R
P.40 Add Q104 for WLAN LED issue
P.32 Add Q105 , Q106 , R1451 ,R1452 for leakage voltage
P.41 Change R1377 to 390 ohm for ME request

(2005/11/16)

P.41 Change LED9 to HT-110NB5 for ME request
P.40 Add R1453 reserved R
P.29 Change U76 pin 10 , 11 net name to MB_DDCCLK & MB_DDCDATA
P.29 Change CN4 pin 15,12 & R483 pin2 , R487 pin2 netname to MB_CRT_DDCCLK ,MB_CRT_DDCDATA
P.30 Del R1060 , R1059 and connect U77 pin 9 to GM_OR_NV_DDCCLK ; connect U77 pin 12 to GM_OR_NV_DDCDATA
P.30 Connect U77 pin 10 , 11,13,14 to MB side and docking's CRT DDC CLK and DATA signal
P.33 Add Q107 and R1454 for RUNTIME_SCI# leakage current

(2005/11/18)

P.23 Change R340,R344,R347,R348,R351,R352,R357,R358,C499,C501 to NC condition
P.28 Del R1390 and connect U106 pin 1 to INV_EN_EC
P.43 Add R1455 0 ohm R
P.16 Add R1457 , U108 , R1456 for Nvidia reset glith issue
P.16 Add R1458 33ohm

(2005/11/18) Power modify

P.61 Del PJ36 then add GP15 at PJ36 location for short +1_05VSUS with +1_05VRUN
P.61 No mount PQ103

Any change need to modify BOM by manual
(2005/11/19)

P.42 C1222 change to 2,2uF

MP schematics modify

PVT released ECR to modify BOM as below list :

(2005/12/03)

P.42 Change C1222 from 2.2uF to 1uF ; R1267 change to 10K ohm
P.33 R1435 change from 10Kohm to 2K ohm
P.43 Add R1446 and R1447 ; Del R1448 , R1449 at BOM
P.37 Del R1441 and add PR416 for CLK_EN# control by Max8771
P.17 Del R225,R228 and add R226 , R227 for 3GIO_PADCFG setting
P.22 Change U8 from 0.26p to 0.28p version
P.22 Change Y2 mount condition to NV_

Power modify

P.56 PD1 change to SSM34PT
P.60 Change PR138 to 15K ohm
P.60 PD18,PD45 change to SSM34PT
P.56 Change PQ84 to A04607

New modify for MP stage (including BOM and schematics)

(2005/12/09)

P.57 Add PR417 1K ohm pull-low for +ECVCC discharge circuit (modify layout)
P.42 Add R1459 , R1460 pull up resistor for ExpressCard logo apply (modify layout)
P.43 Change U39 footprint to QFN package only (modify layout)

P.40 Del TP267 for layout space tight issue

(2005/12/12)

P.16 Change R1457 , U108 , R1458 to NV_ condition

(2005/12/13)

P.42 Change R1459 , R1460's power source to +3VAUX_PCIE_OUT (modify layout)

(2005/12/14)

P.42 Del R1459 , R1460 for layout space critical issue (modify layout)

P.22 Change U10 to G-100(down scale 1%) for G72M can accept 1.25% issue

(2005/12/15)

P.46 Change C1232 to 0.68uF and C1230 change to 470pF for bandwidth change
P.61 Change PQ54 , PR412 , PR169 , PR168 , PC175 , PQ53 PC174 to NV_ condition
P.42 Add C1309 for CAM quality progress
P.61 Change PR402 , PQ102 to NV_ mount condition

(2005/12/16)

P.42 Delete C1309.

(2005/12/19)

P.62 For UL_IN# lock issue

FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title History (8)			
Size A3	Document Number MS10-1-01 (MBX-149)		Rev 1.00
Date:	Tuesday, December 20, 2005	Sheet 74 of 74	