HSF Property: ROHS

ACER_BAP31U

MAIN BOARD

2009.05.13

Wednesday, May 20, 2009		A01
DATE	CHANGE NO.	REV

	EE	DATE	POWER	DATE
DRAWER				
DESIGN				
CHECK				
RESPONSIBLE				

SIZE= VER:

FILE NAME: XXXX-XXXXXX-XX

P/N XXXXXXXXXXX

INVENTEC

TITLE ACER_BAP31U

SIZE	CODE	DOC.NUMBER	REV
C	AX1	D-CS-1310A2264501-ALG	A01

SHEET 1 of 35

1. Schematic Page Description :

Montevina Schematic Ver : A02

1. Title
2. Schematic Page DESCR
3. Block Diagram
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5. Schematic Modify
6. Timing Diagram
7. Power Block Diagram
8. Adaptor in/Charge
9. 5VLA/5VA/3VA
10. 3VS/5VS/1.5V (DDR3)
11. 1.05VS/1.5S/1.8V/1.5VA
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25. DDR3 SDRAM SO-DIMM0
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27. ICH9M CPU/IDE/SATA(1/4)
28. ICH9M PCI/PCIE/DMI/USB(2/4)
29. ICH9M GPIO(3/4)
30. ICH9M Power/GND(4/4)
31. LCD CNN/SATA/3G/WLAN
32. KBC ITE8512F
33. IO CN
34. IO CN
35. AUDIO CODEC

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TITLE: BAP31U

Schematic Page

SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01

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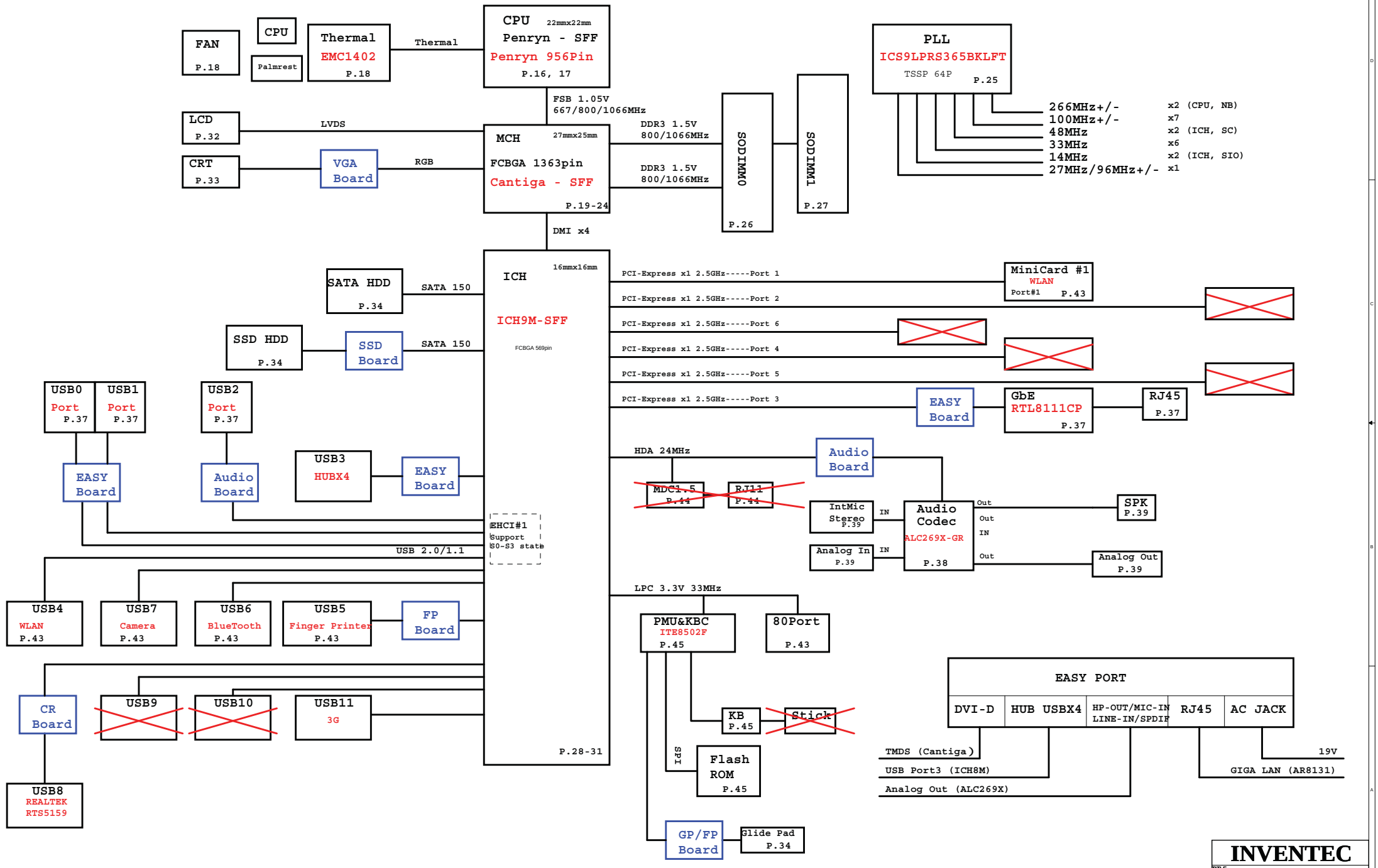
3. Block Diagram :



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TITLE: BAP31U

Block Diagram

SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01

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4. Net name Description

Voltage Rails

DCIN	Primary DC system power supply
+5VLA	5.0V always on power rail by LATCH or ACIN
+5VA	5.0V always on power rail by ECPWON
+3VA	3.3V always on power rail by ECPWON
+5VS	5.0V switched power rail by SLP_S3#_3R
+3VS	3.3V switched power rail by SLP_S3#_3R
+1.8VS	1.8V switched power rail by SLP_S3#_3R
VCC_CORE	Core Voltage for CPU
+1.05VS	1.05V power rail for AGTL+ termination/Core for GMCH by SLP_S3#_3R
+1.25VS	1.25V switched power rail by SLP_S3#_3R
+1.5VS	1.5V power rail for CPU PLL/DMI;PCIE;DDRIII DLLs for GMCH/Core;PCIE for ICH9m by SLP_S3#_3R
+1.5V	1.5V power rail for DDRII by SLP_S5#_3R
0.75VDDT_DDRIII	0.75V DDRII Termination Voltage by SLP_S3#_3R

Part Naming Conventions

C	=	Capacitor
CN	=	Connector
D	=	Diode
F	=	Fuse
L	=	Inductor
Q	=	Transistor
R	=	Resistor
RP	=	Resistor Pack
U	=	Arbitrary Logic Device
Y	=	Crystal and Osc

Net Name Suffix

#	=	Active Low signal

5. Board Stack up Description

PCB Layers

Layer 1	Component Side, Microstrip signal Layer
Layer 2	Ground Plane
Layer 3	Stripline Layer
Layer 4	Power Plane
Layer 5	Stripline Layer
Layer 6	Stripline Layer
Layer 7	Ground Plane
Layer 8	Solder Side,Microstrip signal Layer

	Differential Impedance for Microstrip	Differential Impedance for Stripline
Host Clock	95 ohm +/- 20%	95 ohm +/- 20%
PCI-E Clock	95 ohm +/- 20%	95 ohm +/- 20%
DDR3 CLK	75 ohm +/- 20%	75 ohm +/- 20%
DDR3 Strobe	90 ohm +/- 20%	90 ohm +/- 20%
DMI Bus	95 ohm +/- 20%	95 ohm +/- 20%
PCIE Bus	95 ohm +/- 20%	95 ohm +/- 20%
SDVO	95 ohm +/- 20%	95 ohm +/- 20%
SATA	95 ohm +/- 20%	95 ohm +/- 20%
USB	90 ohm +/- 20%	90 ohm +/- 20%
LVDS	95 ohm +/- 20%	95 ohm +/- 20%
Lan	95 ohm +/- 20%	95 ohm +/- 20%

Power Rail	Destination	Voltage	S0 Current
VCC_CORE	Penryn SFF-HFM:	1.3319V~1.4375V~1.4591V	18A
	LFM:	0.9221V~0.9625V~0.9739V	
1.05VS	Penryn SFF : AGTL+ termination	1V~1.05V~1.10V	4.5A
	Cantiga GS: Core	0.997V~1.05V~1.102V	8.7A
	Cantiga GS: PCIE	0.9975V~1.05V~1.1025V	1.78A
	Cantiga GS:Core+IMEL+HSIO	0.9975V~1.05V~1.1025V	2.898A
	Cantiga GS:VCC_GMCH	0.997V~1.05V~1.102V	10.154A
	Cantiga GS:VCCA_SM_CK and NCTF	0.997V~1.05V~1.102V	37.95mA
	Cantiga GS:VCC_DMI	0.997V~1.05V~1.102V	456mA
	Cantiga GS:VCCA_SM	0.997V~1.05V~1.102V	747.5mA
	Cantiga GS:VTT	0.997V~1.05V~1.102V	852mA
	ICH9M:VCC1_05	0.997V~1.05V~1.102V	1.634A
	ICH9M:DMI	0.997V~1.05V~1.102V	48mA
	ICH9M:CPU_IO	0.997V~1.05V~1.102V	2mA
1.5VS	Penryn SFF PLL	1.425V~1.5V~1.575V	130mA
	Cantiga GS: QDAC	1.425V~1.5V~1.575V	0.5mA
	Cantiga GS: LVDS	1.71V~1.8V~1.89V	60.31mA
	Cantiga GS: TVDAC	1.425V~1.5V~1.575V	35mA
	Cantiga GS: Various PLLS analog supply	1.425V~1.5V~1.575V	485mA
	Cantiga GS: VCC_SM_CK	1.425V~1.5V~1.575V	149.5mA
	Cantiga GS: VCC_SM	1.425V~1.5V~1.575V	3.1625A
	ICH9M:PCIE_ICH	1.425V~1.5V~1.575V	646mA
	ICH9M:SATA_ICH	1.425V~1.5V~1.575V	1.342A
	ICH9M:VCC_GLAN	1.425V~1.5V~1.575V	80mA
	Mini Card:		
	Express Card:	1.425V~1.5V~1.575V	650mA
1.5V	Cantiga GS: DDRIII System Memory	1.425V~1.5V~1.575V	3.1A(800M) 4.1A(1067M)
0.75VDDT_DDRIII	DDRIII Terminator:	0.7125V~0.75V~0.7875V	1.0A
3VS	Cantiga GS: HV CMOS	3.135V~3.3V~3.465V	105.3mA
	Cantiga GS: VCCS_TVDAC	3.135V~3.3V~3.465V	78mA
	ICH9M:VCC3_3	3.135V~3.3V~3.465V	308mA
	ICH9M:VCCGLAN3_3	3.135V~3.3V~3.465V	1mA
	Thermal Sensor:	3.0V~3.3V~3.6V	5mA
	Mini Card: UMTS		
	Express Card:	3.135V~3.3V~3.465V	1.3A
	CLK Generator: ICS9LPRS365BKLFT	3.135V~3.3V~3.465V	500mA
	Mini Card: WirelessLan		
	Bluetooth:	3.0V~3.3V~3.6V	
	Super I/O: IT8305E		
	Azalia Codec: ALC262		
	Azalia MDC:		
1.8VS	DVI	3.0V~3.3V~3.6V	120mA
3VA	ICH9M: RTC	2V~3.3V~3.465V	6uA
	ICH9M:VCCSUS3_3	3.135V~3.3V~3.465V	212mA
	ICH9M:VCCCL3_3	3.135V~3.3V~3.465V	73mA
	ICH9M:VCCLAN3_3	3.135V~3.3V~3.465V	78mA
	LCD:	3.0V~3.3V~3.6V	2A
	Lan:AR8131	3.0V~3.3V~3.6V	1A
	Azalia MDC:		
	Flash ROM: BIOS	3.0V~3.3V~3.6V	
5VS	Cardreader: RTS5159	3.0V~3.3V~3.6V	
	Azalia Codec: ALC269	3.0V~3.3V~3.6V	
	HDD: SATA	4.75V~5.0V~5.25V	Max: 1.5A ; R/W: 460mA ; STDBY: 70mA
	~~ODD: SATA~~	~~4.75V~5.0V~5.25V~~	~~Max: 1.5A ; R/W: 900mA ; STDBY: 45mA~~
	~~Audio AMP: G1432~~		
	Inverter:		
	WebCam	4.75V~5.0V~5.25V	1A
5VA	USB: x 2 ports	5VA	2A
	USB	5VA	1.5A
5VLA	Control Power		
3VLA	EC: ITE8512E	3.0V~3.3V~3.6V	300mA

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TITLE BAP31U

ANNOTATIONS

SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01

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6.Schematic modify Item and History:

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DATE	Wednesday, May 20, 2009		

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TITLE
BAP31U
Schematic Modify

SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01

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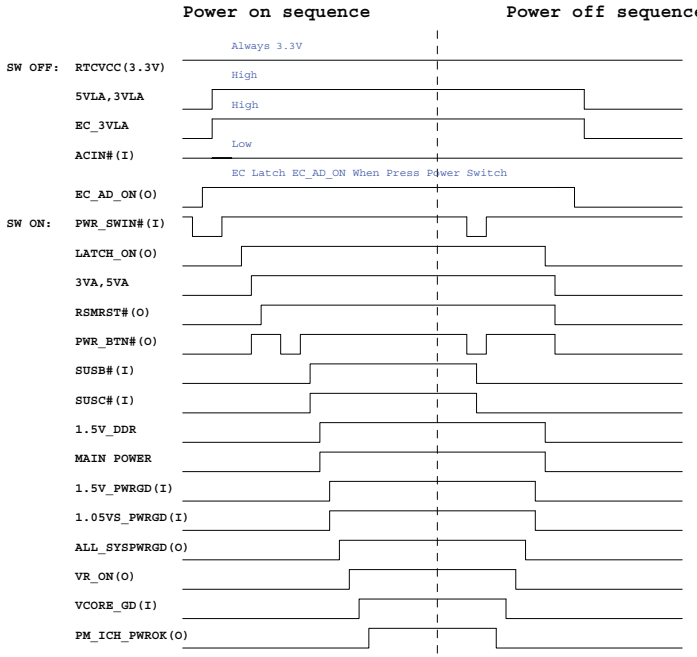
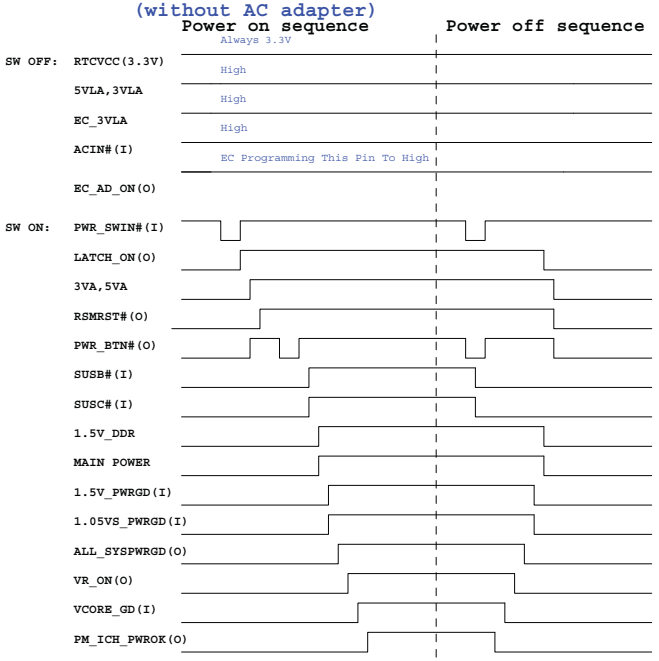
SYSTEM POWER ON/OFF SEQUENCE

Drawing : Wendy, Huang

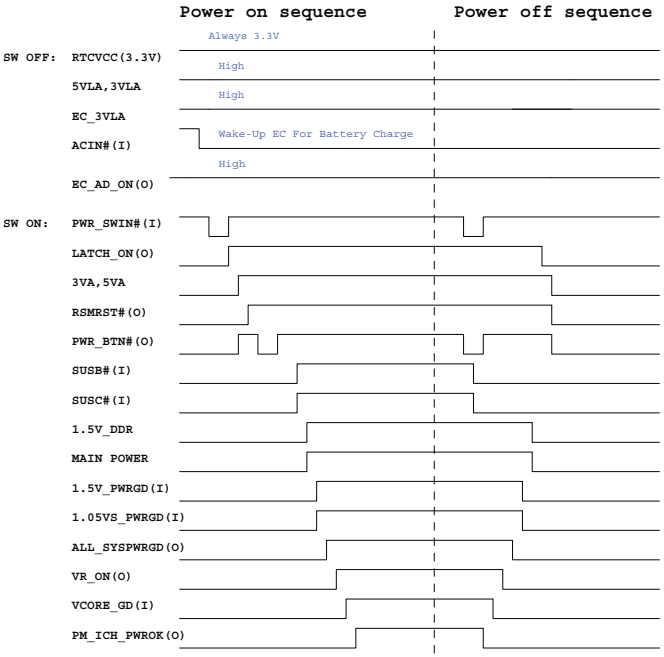
Power on/off sequence AC insert (without Battery Pack)



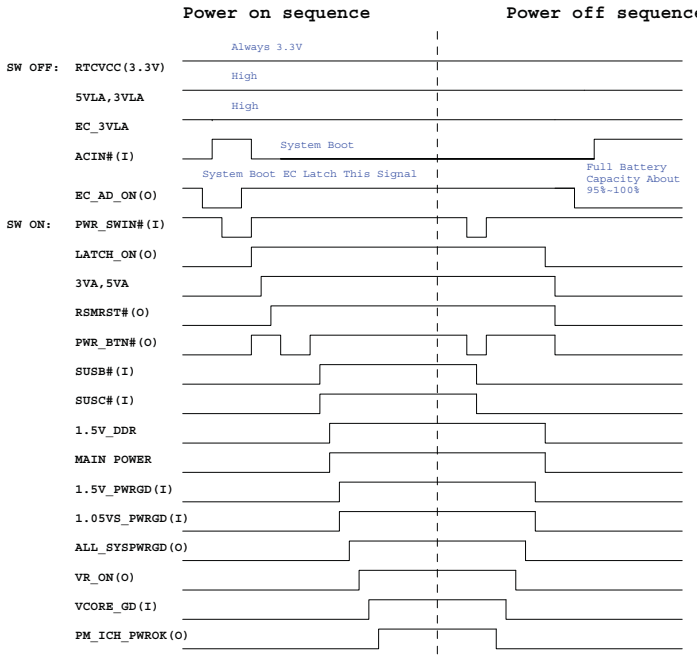
Power on/off sequence Battery insert (without AC adapter)



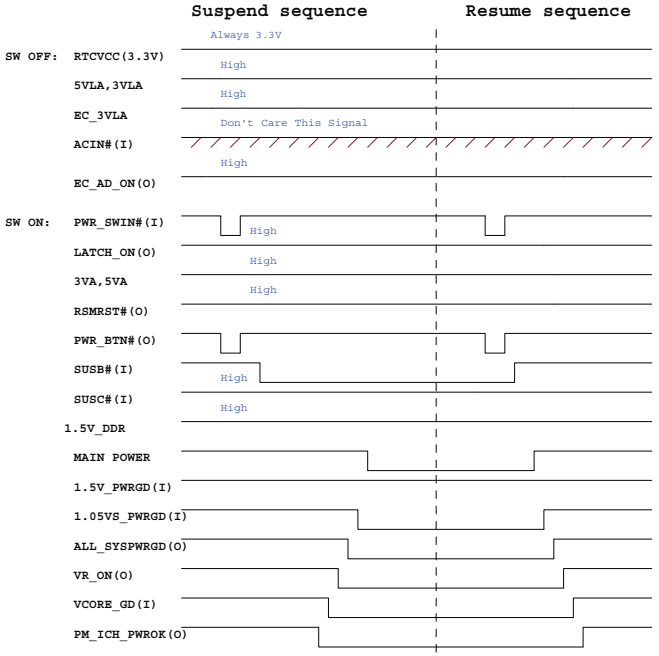
Power on/off sequence AC insert(with charge over 95%)



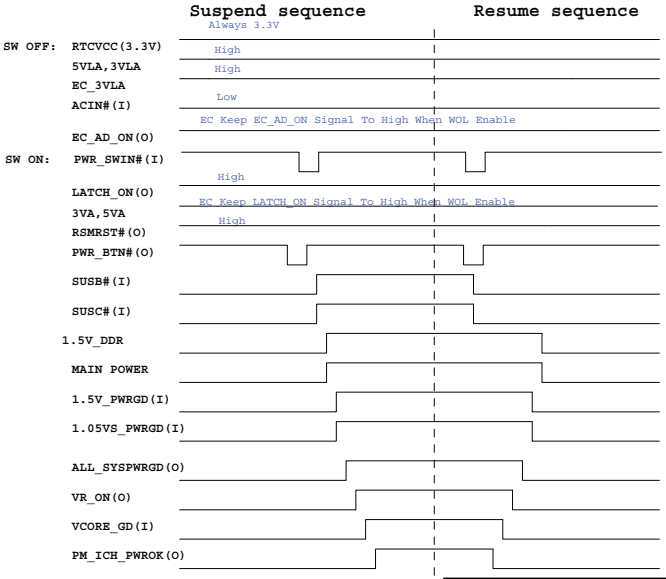
Power on/off sequence AC insert(without charge over 95%)



Suspend And Resume Sequence (S3)



Power on/off sequence after windows shoutdown (WOL enable)



INVENTEC

TITLE
BAP31U
Time Diagram

SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01

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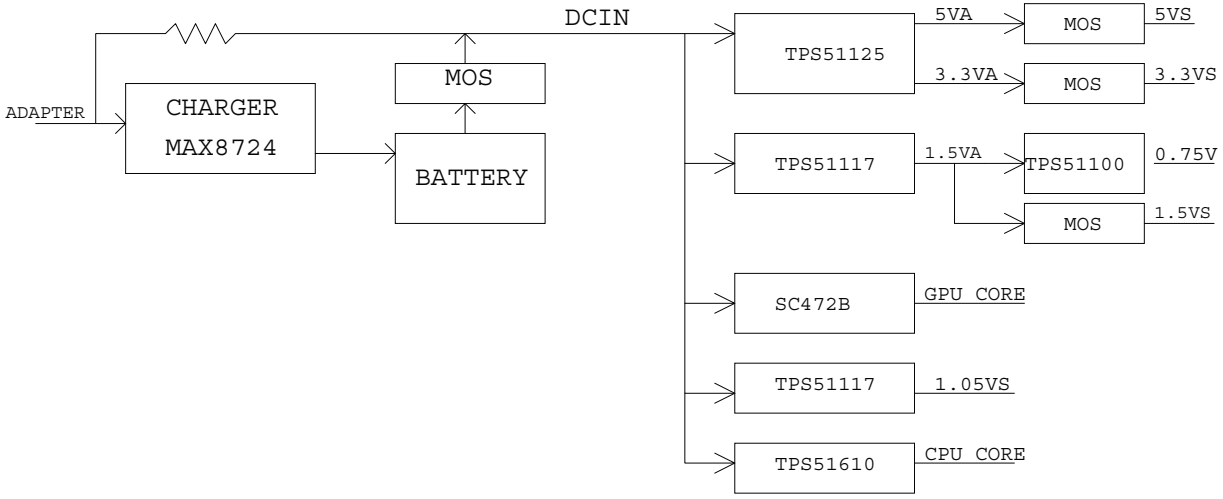
CHANGE by	Harry Chen	DATE	Wednesday, May 20, 2009

Power Block Diagram :



CHANGE by	Harry Chen	DATE	Wednesday, May 20, 2009

INVENTEC

TITLE BAP31U

Power Block Diagram

SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01

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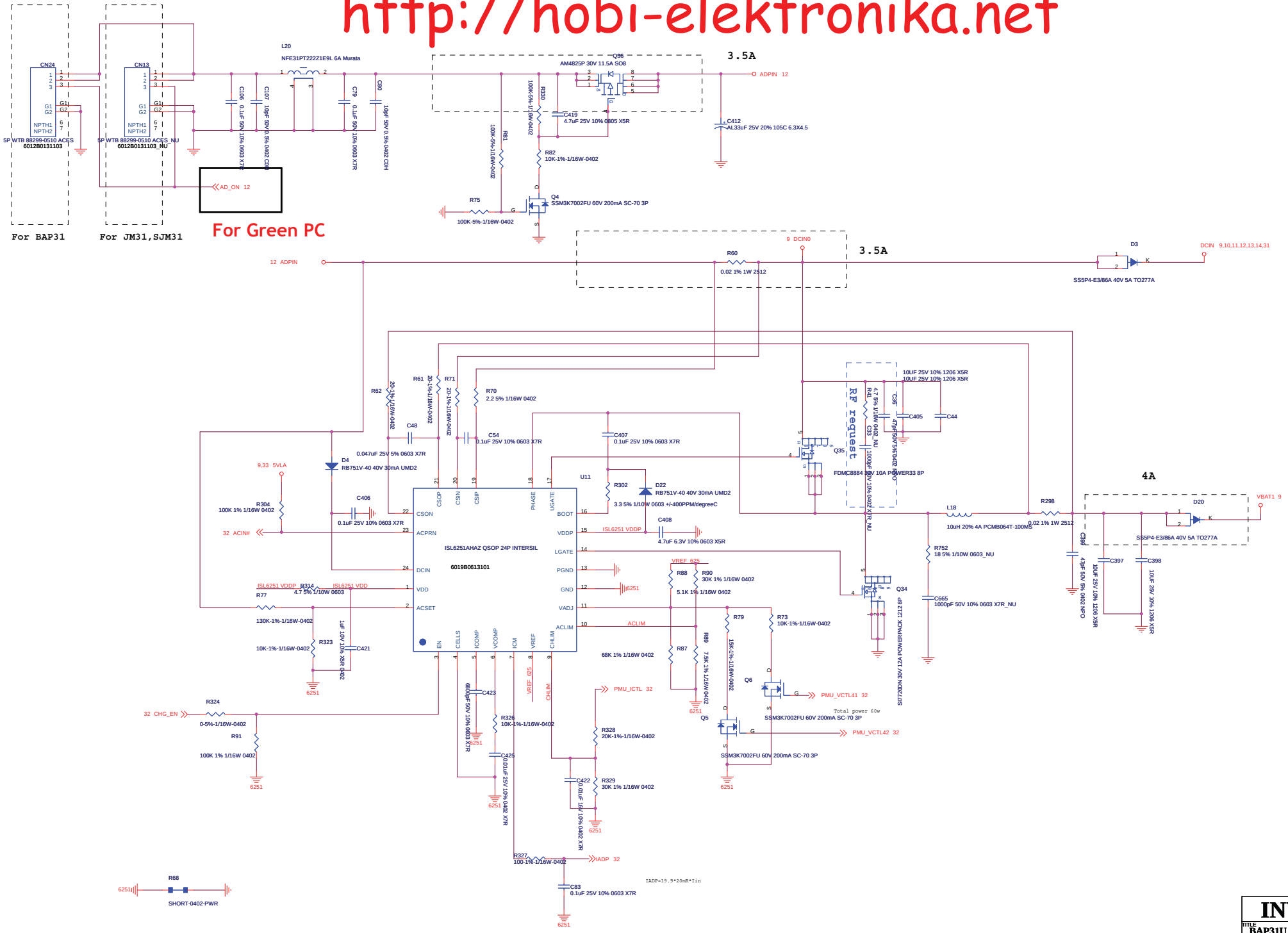

CHANGE by	Harry Chen	DATE	Wednesday, May 20, 2009

INVENTEC

TITLE: **BAP31U** — Adaptor in / Charge

SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01

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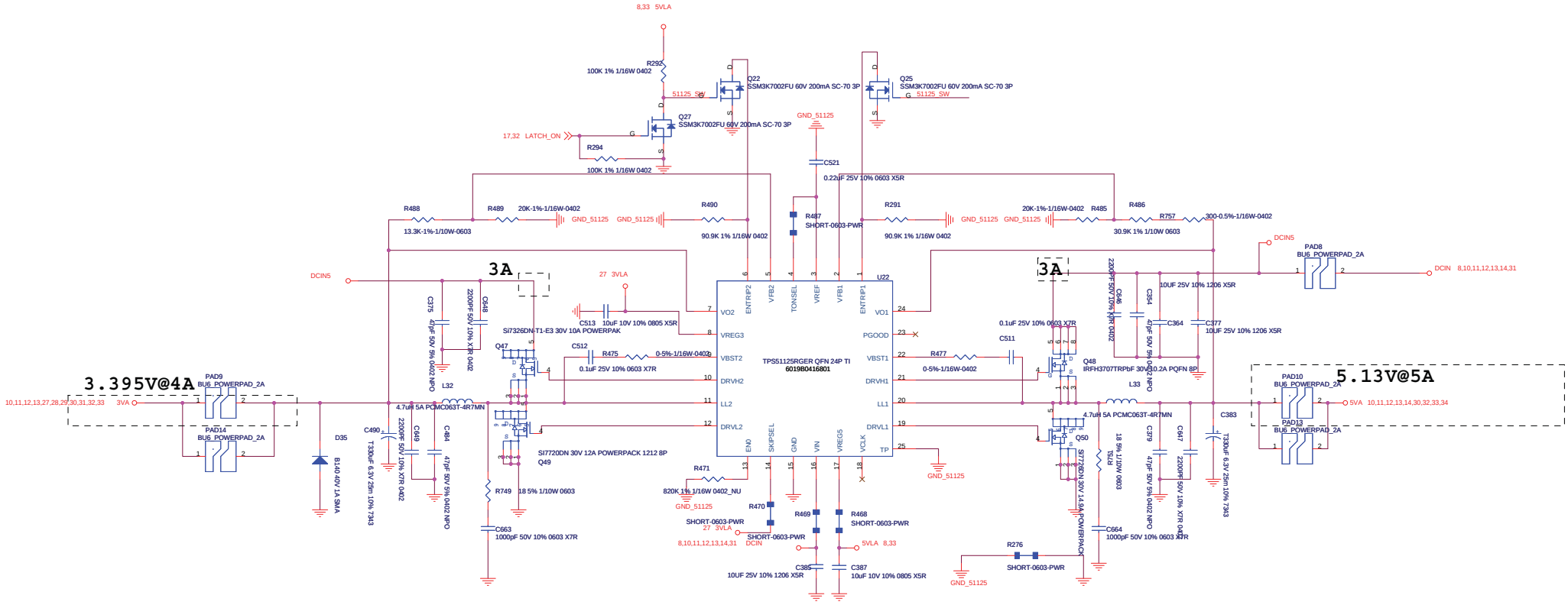
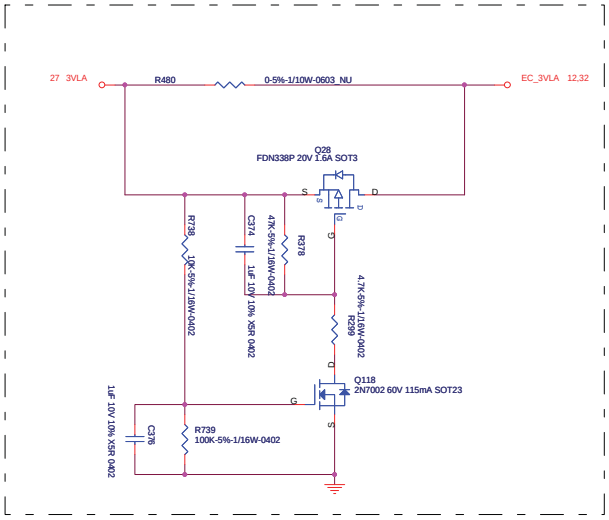
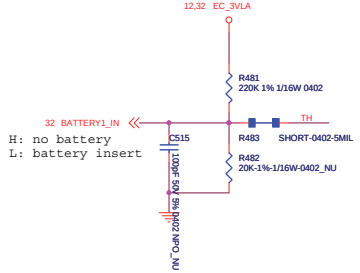
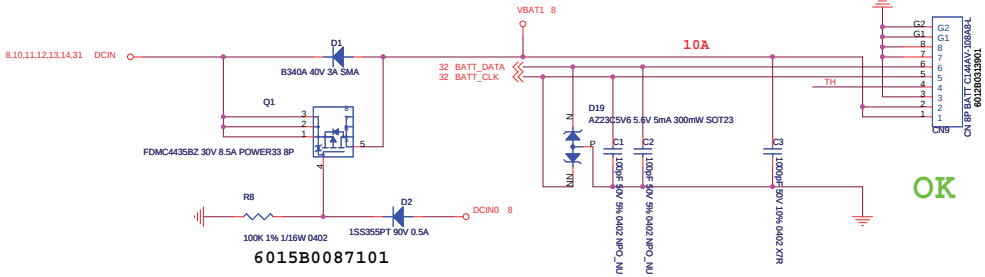


For Green PC







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INVENTEC

TITLE **BAP31U**

5VLA/5VA/3VLA/3VA

SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01

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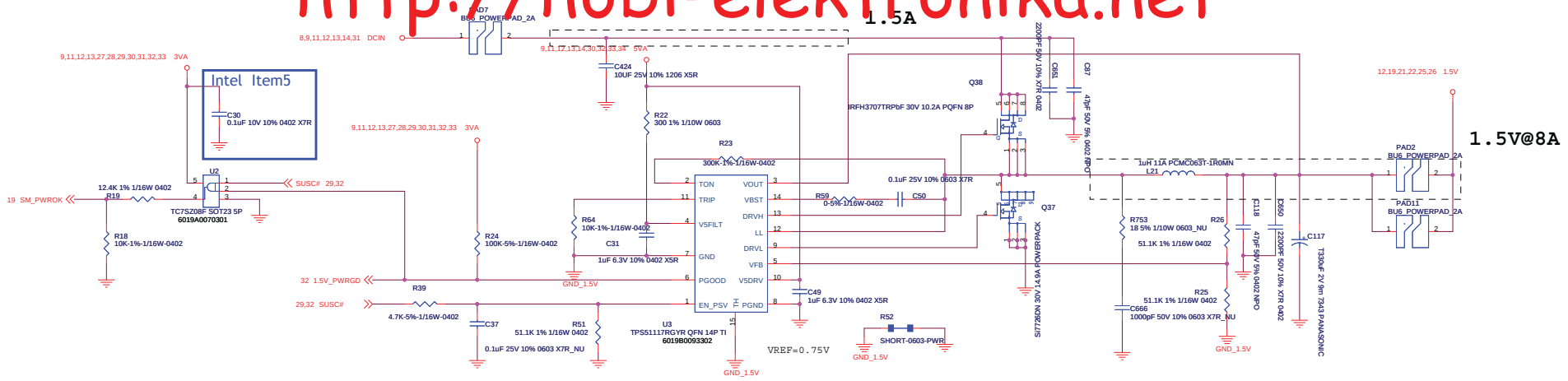

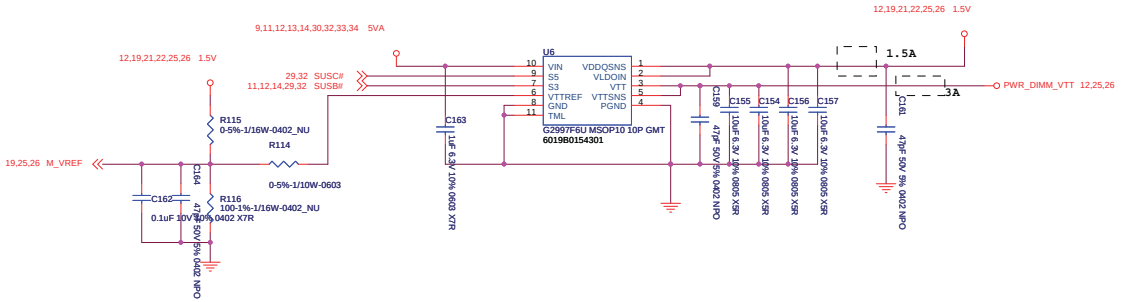

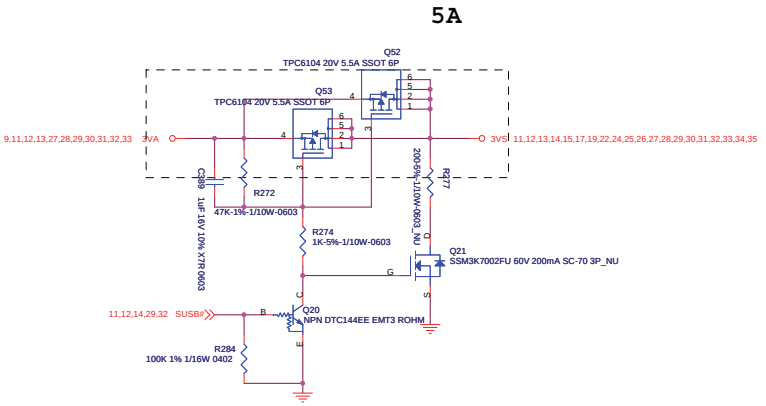

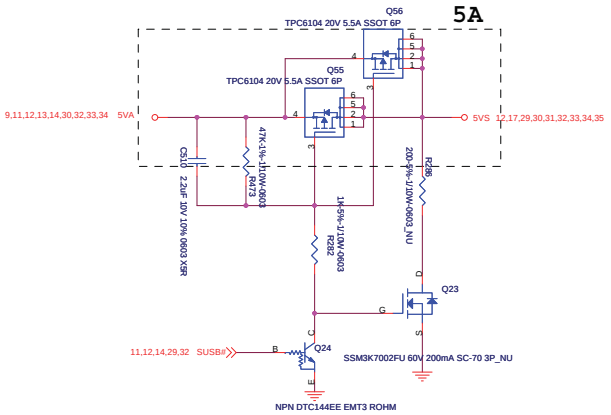

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INVENTEC

TITLE: BAP31U
3VS/5VS/1.5V (DDR3)

SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01
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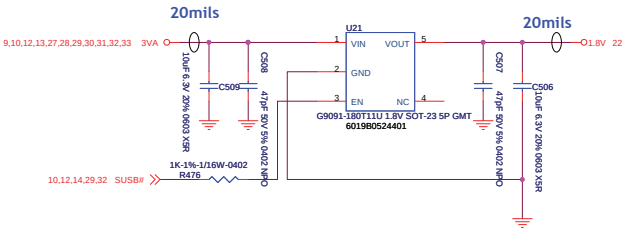

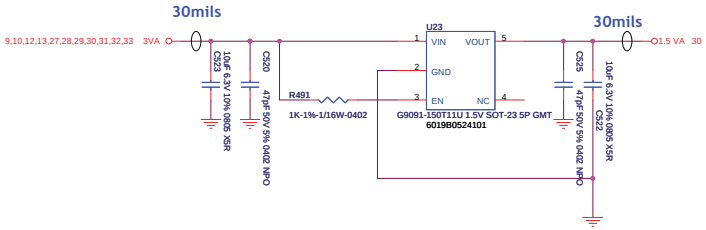

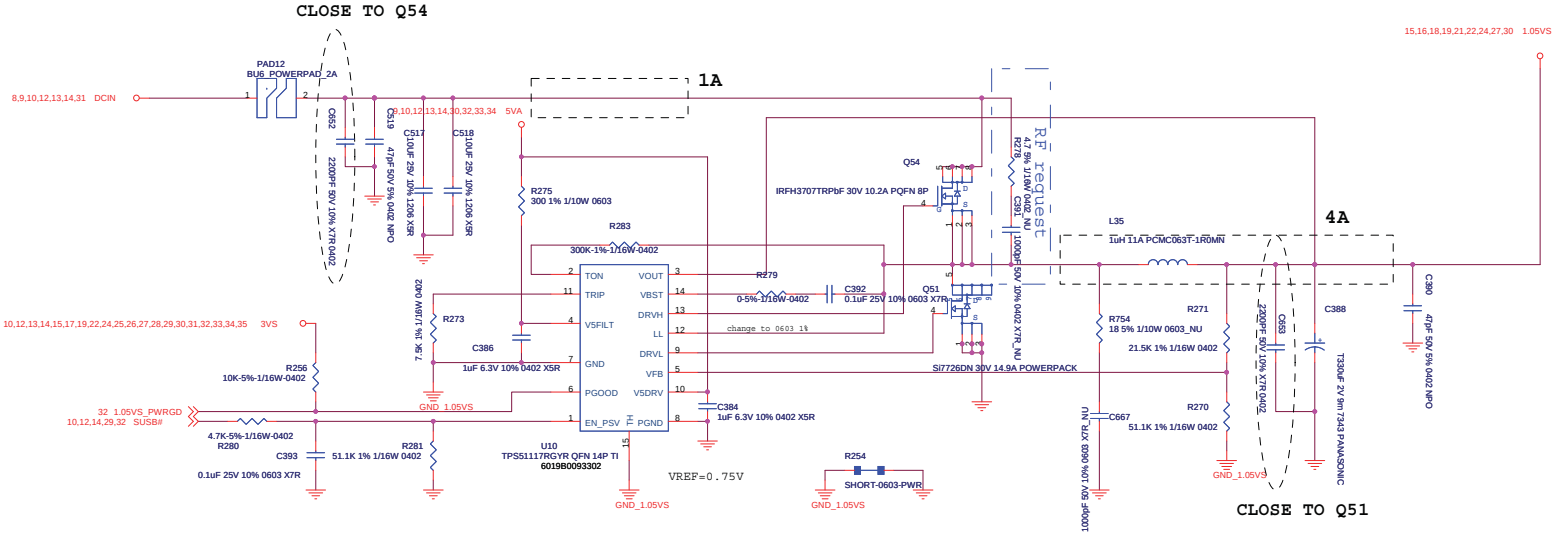

CHANGE by	Harry Chen	DATE	Wednesday, May 20, 2009

INVENTEC

TITLE: BAP31U
1.05VS/1.5S/1.8V/1.5VA

SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01

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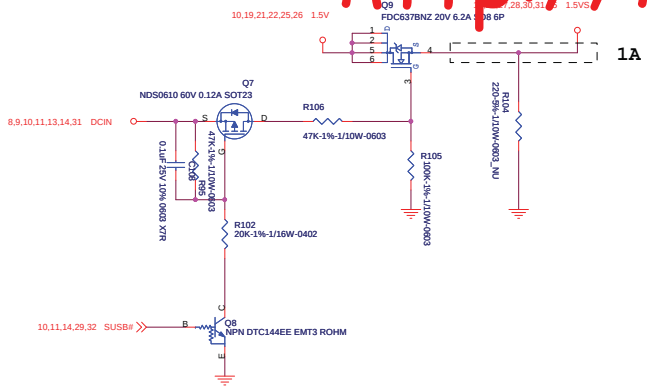
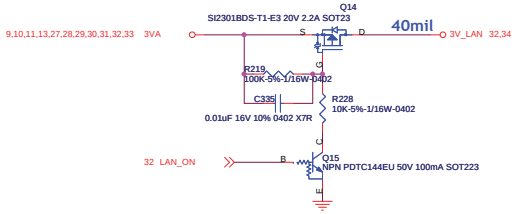
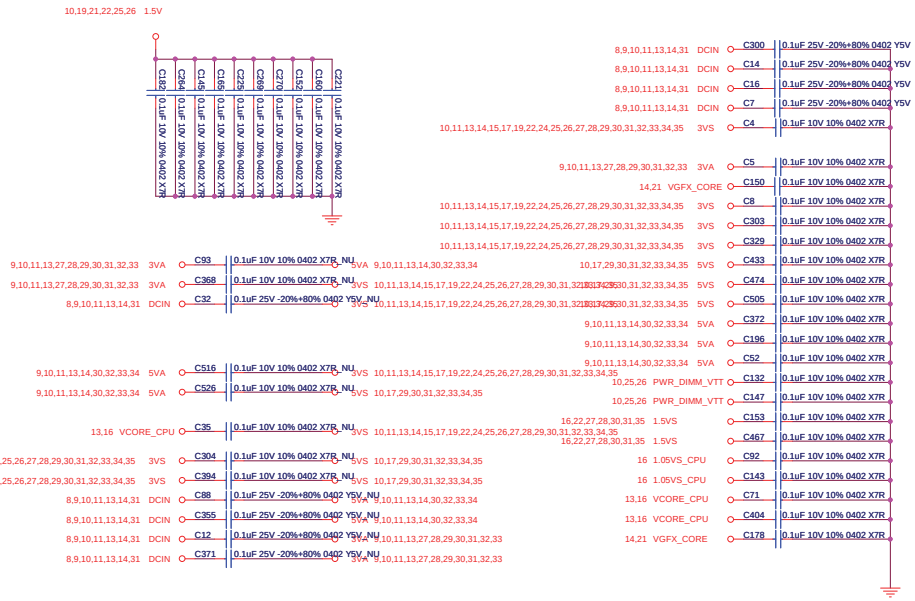
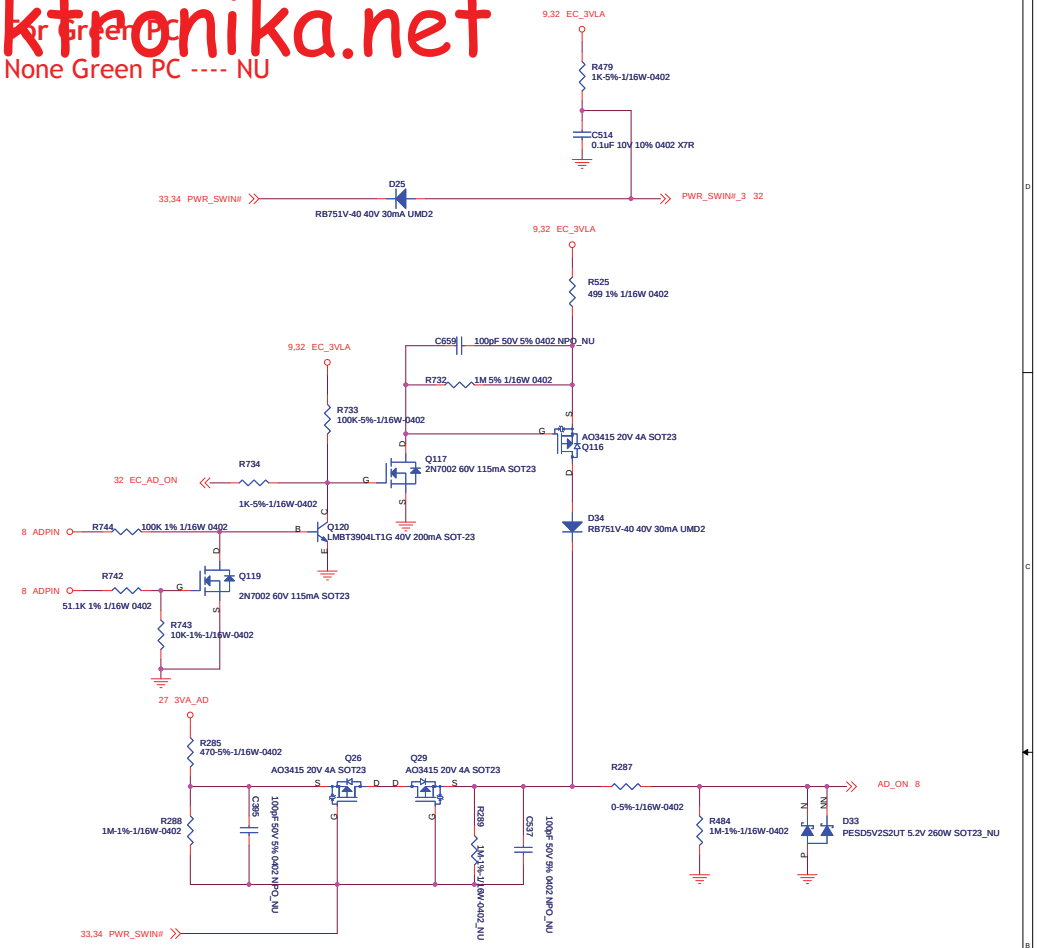
1.5VS

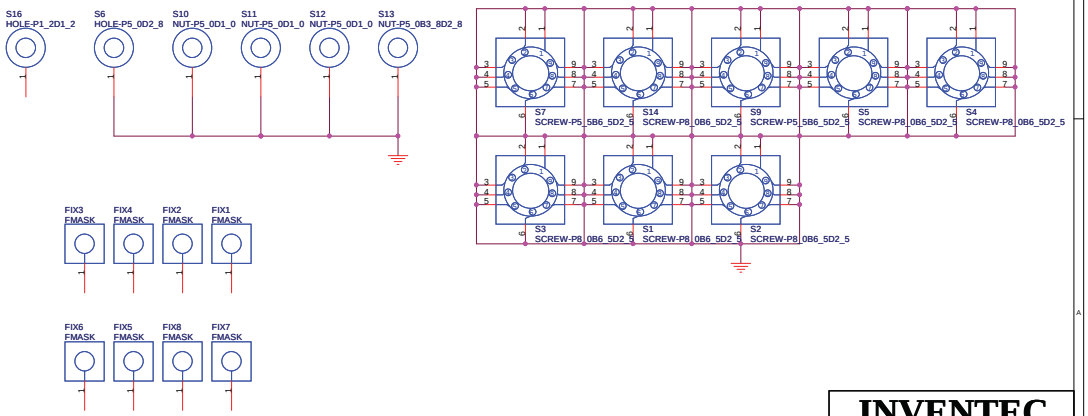




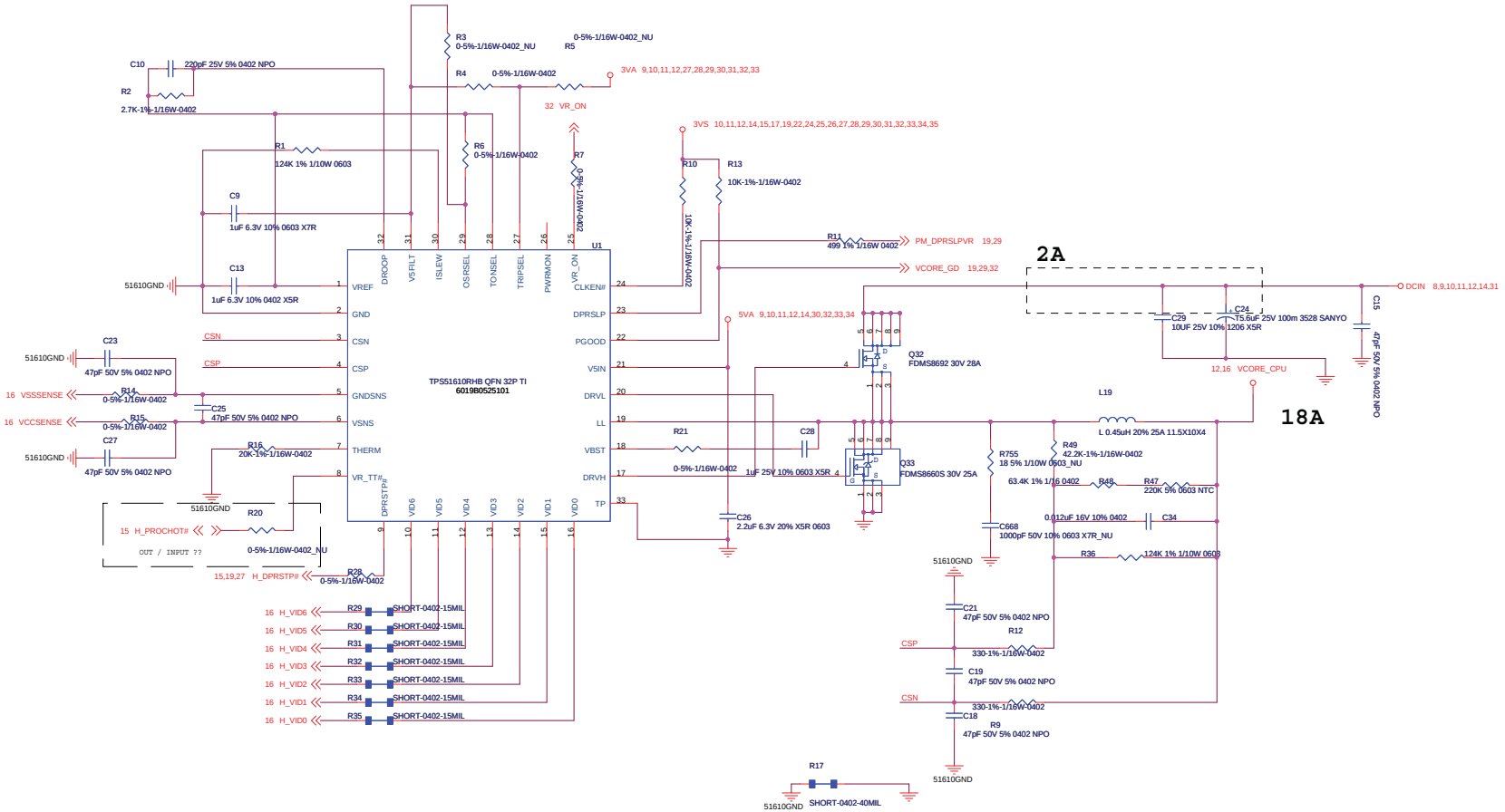
EMI Cap



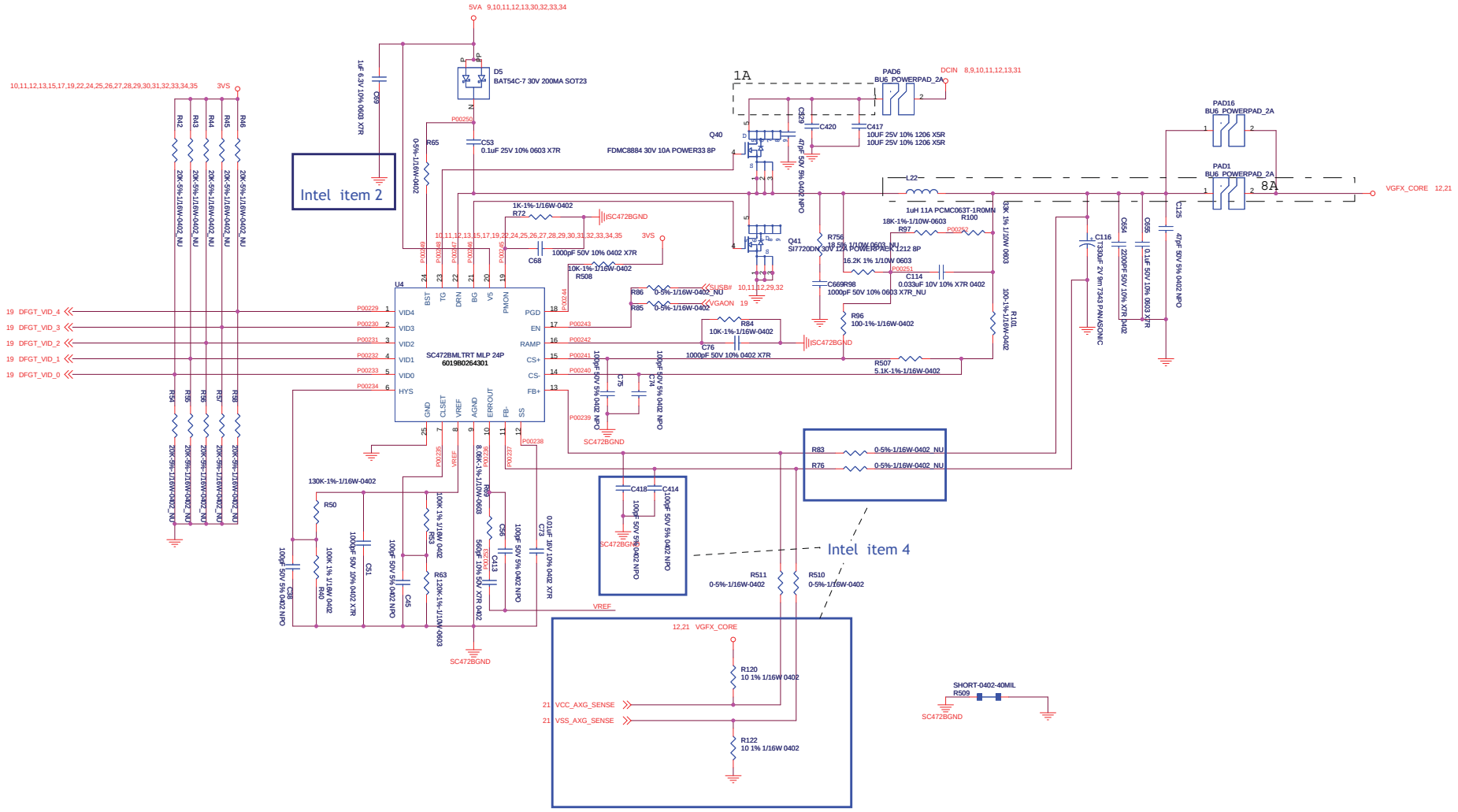




INVENTEC			
TITLE: BAP31U			
Power on latch			
SIZE: Custom	CODE: AX1	DOC.NUMBER: D-CS-1310A2264501-ALG	REV: A01
CHANGE by: Harry Chen	DATE: Wednesday, May 20, 2009	SHEET: 12 of 35	



INVENTEC			
TITLE: BAP31U			
CPU Core Power			
SIZE: Custom	CODE: AX1	DOC.NUMBER: D-CS-1310A2264501-ALG	REV: A01
		SHEET: 13 of 35	
CHANGE by: Harry Chen	DATE: Wednesday, May 20, 2009		



CHANGE by	Harry Chen	DATE	Wednesday, May 20, 2009

INVENTEC

TITLE **BAP31U**

GPU CORE

SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01

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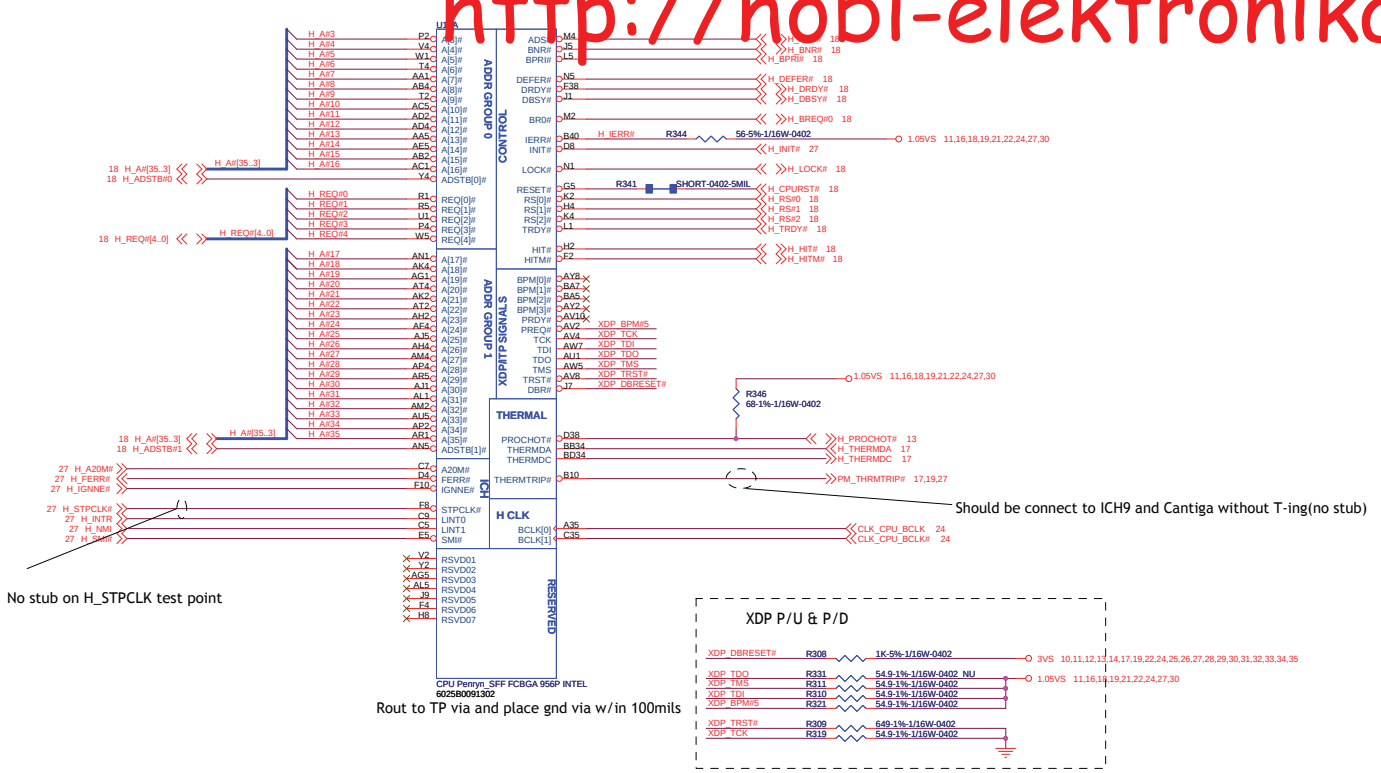
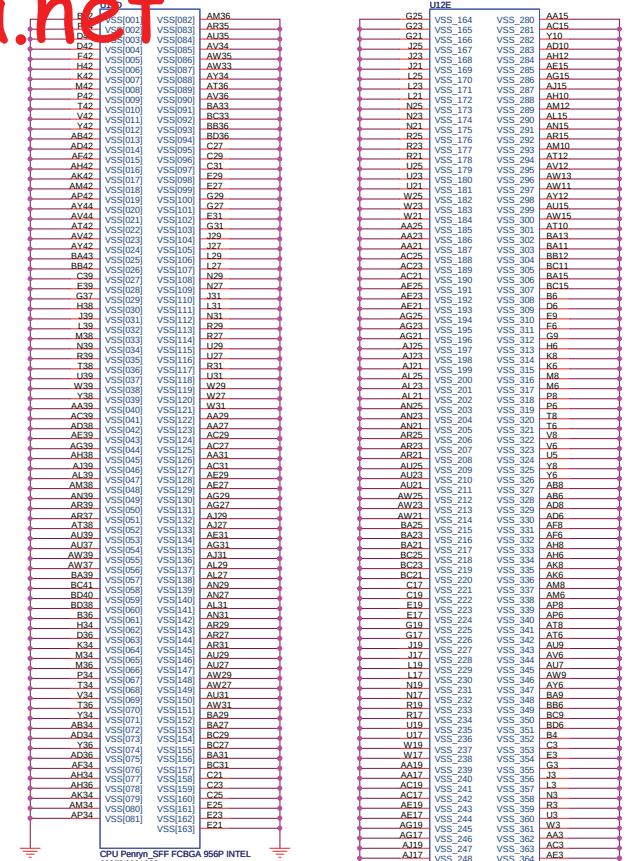
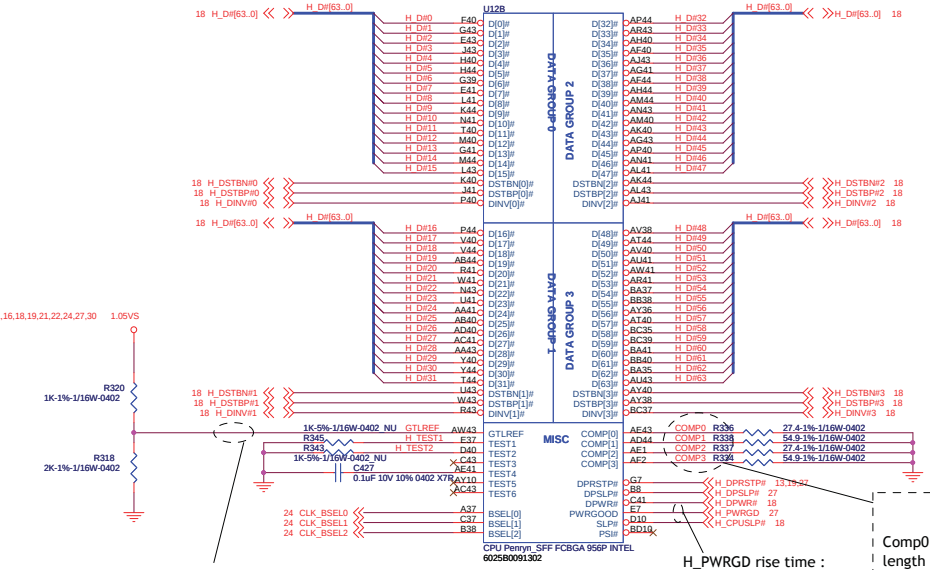


A#[32-39], APM#[0-1]:Leave escape routing on for future functionality



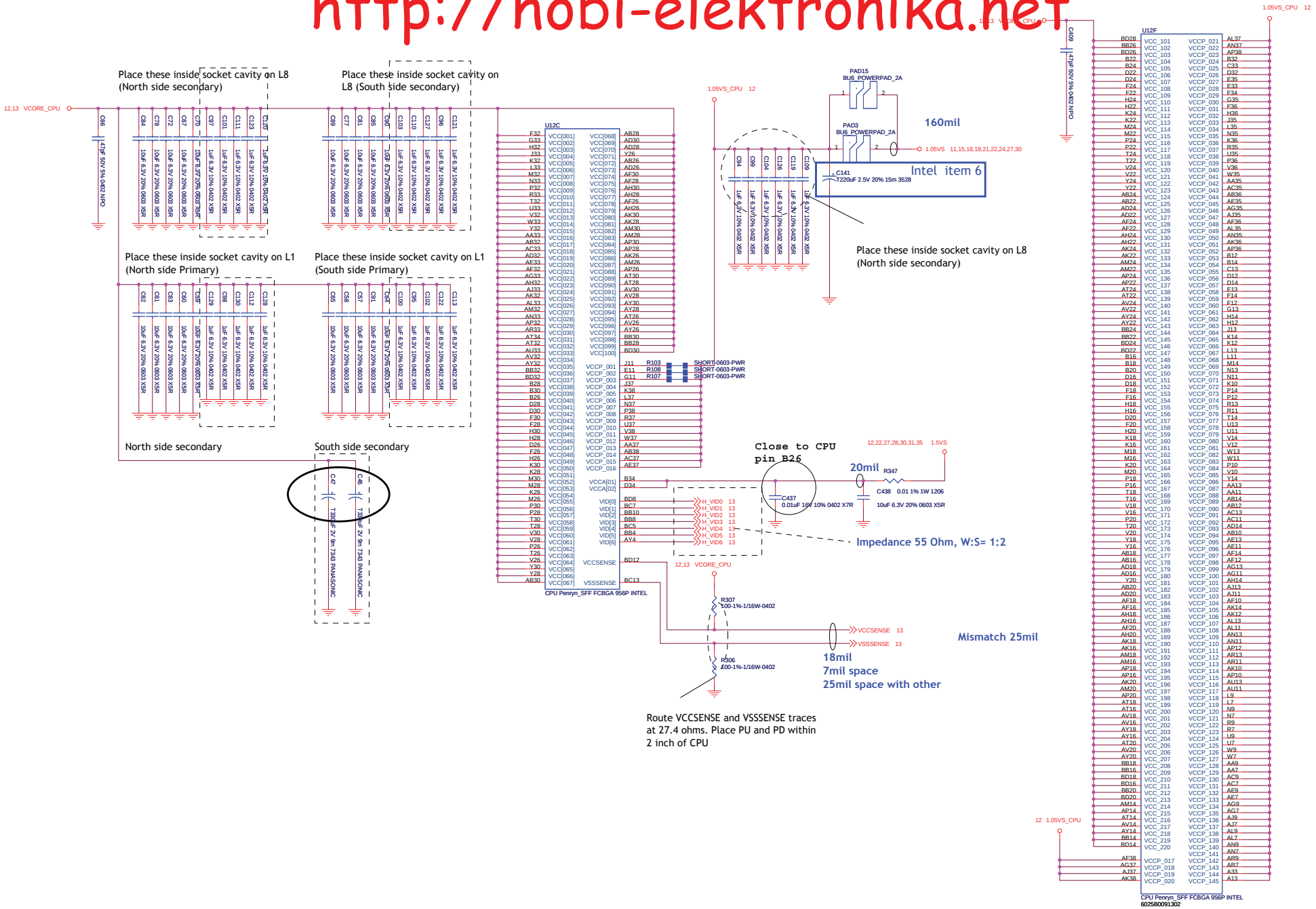


CHANGE by	Harry Chen	DATE	Wednesday, May 20, 2009		
SIZE	CODE	DOC.NUMBER		REV	
Custom	AX1	D-CS-1310A2264501-ALG		A01	
		SHEET	15	of	35

INVENTEC

TITLE: BAP31U

Penryn Processor(1/2)



CHANGE by	Harry Chen	DATE	Wednesday, May 20, 2009

INVENTEC

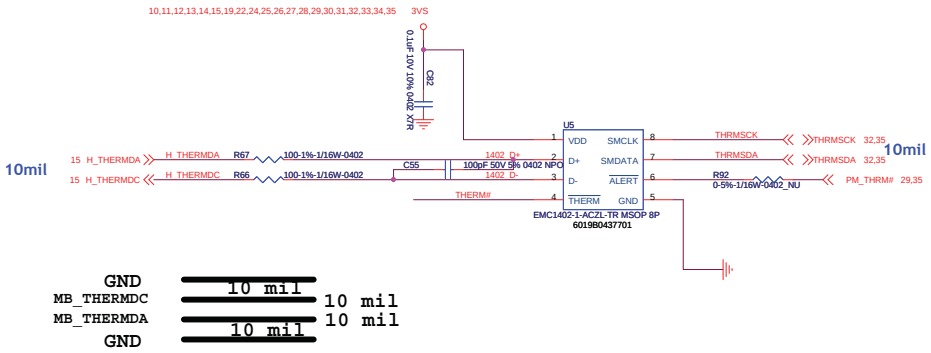
TITLE **BAP31U**

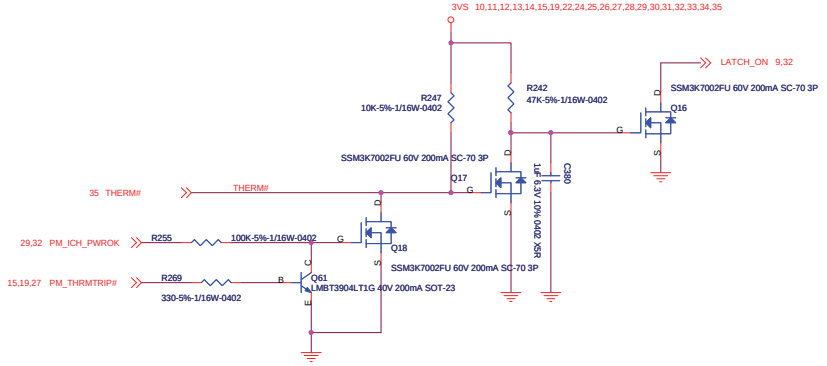
Penryn Processor(2/2)

SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01

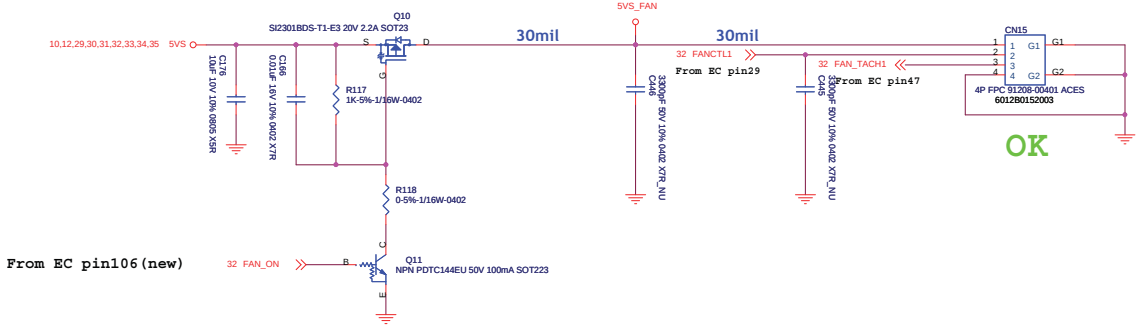
SHEET 16 of 35

THERMAL SENSOR





Fan control



CHANGE by	Harry Chen	DATE	Wednesday, May 20, 2009

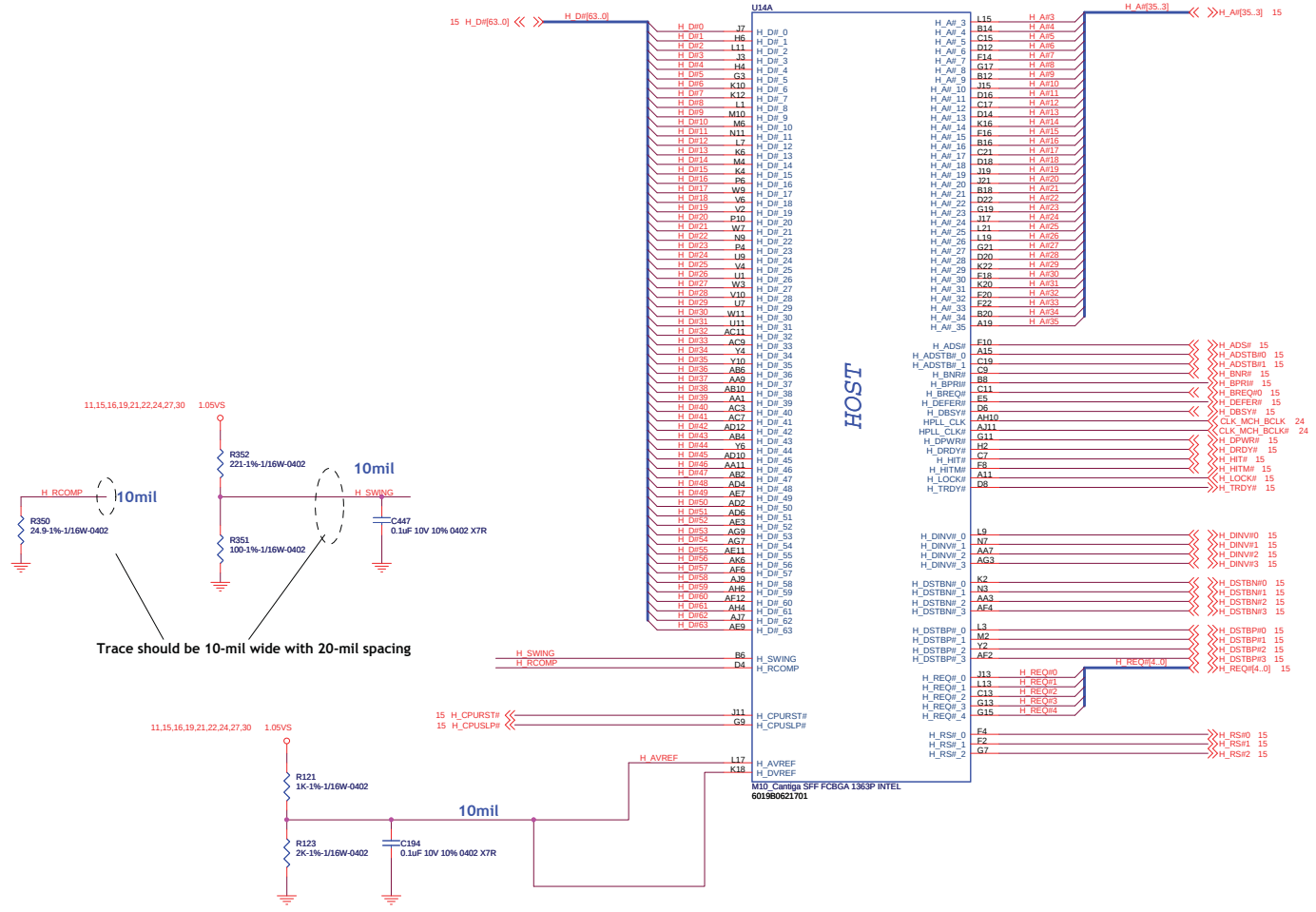
INVENTEC

TITLE: **BAP31U**

CPU Thermal

SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01

SHEET 17 of 35



CHANGE by	Harry Chen	DATE	Wednesday, May 20, 2009

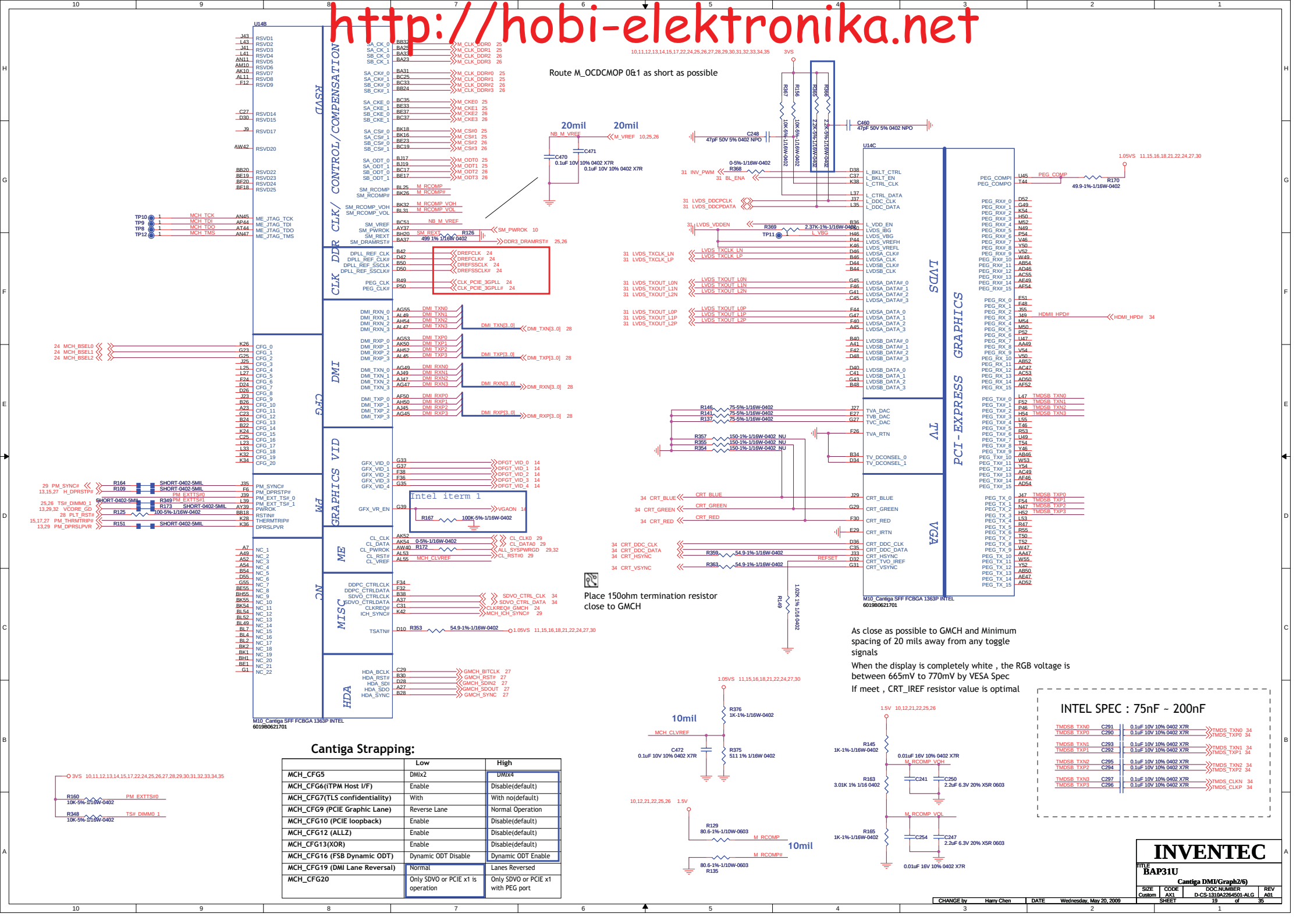
INVENTEC

TITLE: **BAP31U**

Cantiga Host(1/6)

SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01

SHEET 18 of 35

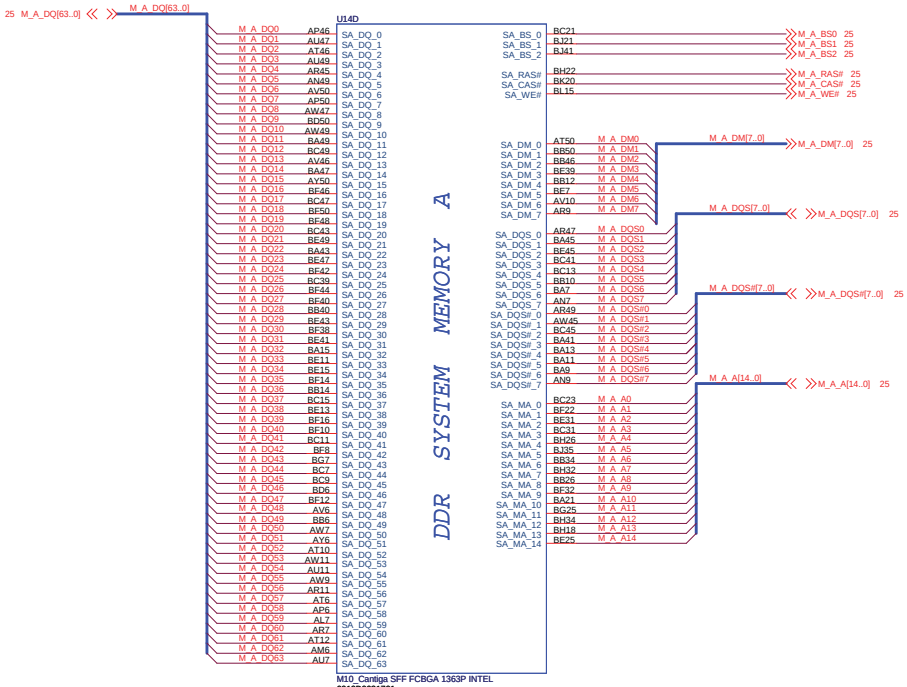


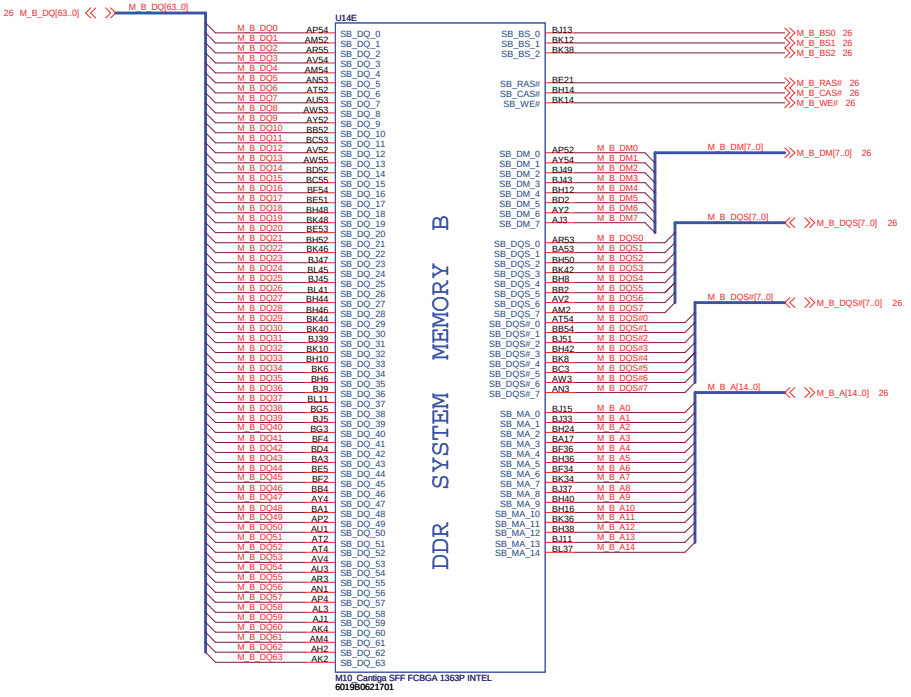
Cantiga Strapping:

	Low	High
MCH_CFG5	DMIx2	DMIx4
MCH_CFG6(iTPM Host I/F)	Enable	Disable(default)
MCH_CFG7(TLS confidentiality)	With	With no(default)
MCH_CFG9 (PCIE Graphic Lane)	Reverse Lane	Normal Operation
MCH_CFG10 (PCIE loopback)	Enable	Disable(default)
MCH_CFG12 (ALLZ)	Enable	Disable(default)
MCH_CFG13(XOR)	Enable	Disable(default)
MCH_CFG16 (FSB Dynamic ODT)	Dynamic ODT Disable	Dynamic ODT Enable
MCH_CFG19 (DMI Lane Reversal)	Normal	Lanes Reversed
MCH_CFG20	Only SDVO or PCIE x1 is operation	Only SDVO or PCIE x1 with PEG port

CHANGE by	Harry Chen	DATE	Wednesday, May 20, 2009	
SIZE	CODE	DOC.NUMBER		REV
Custom	AX1	D-CS-1310A2264501-ALG		A01
		SHEET	19 of 35	

INVENTEC
TITLE: BAP31U
Cantiga DMI/Graph2/6)





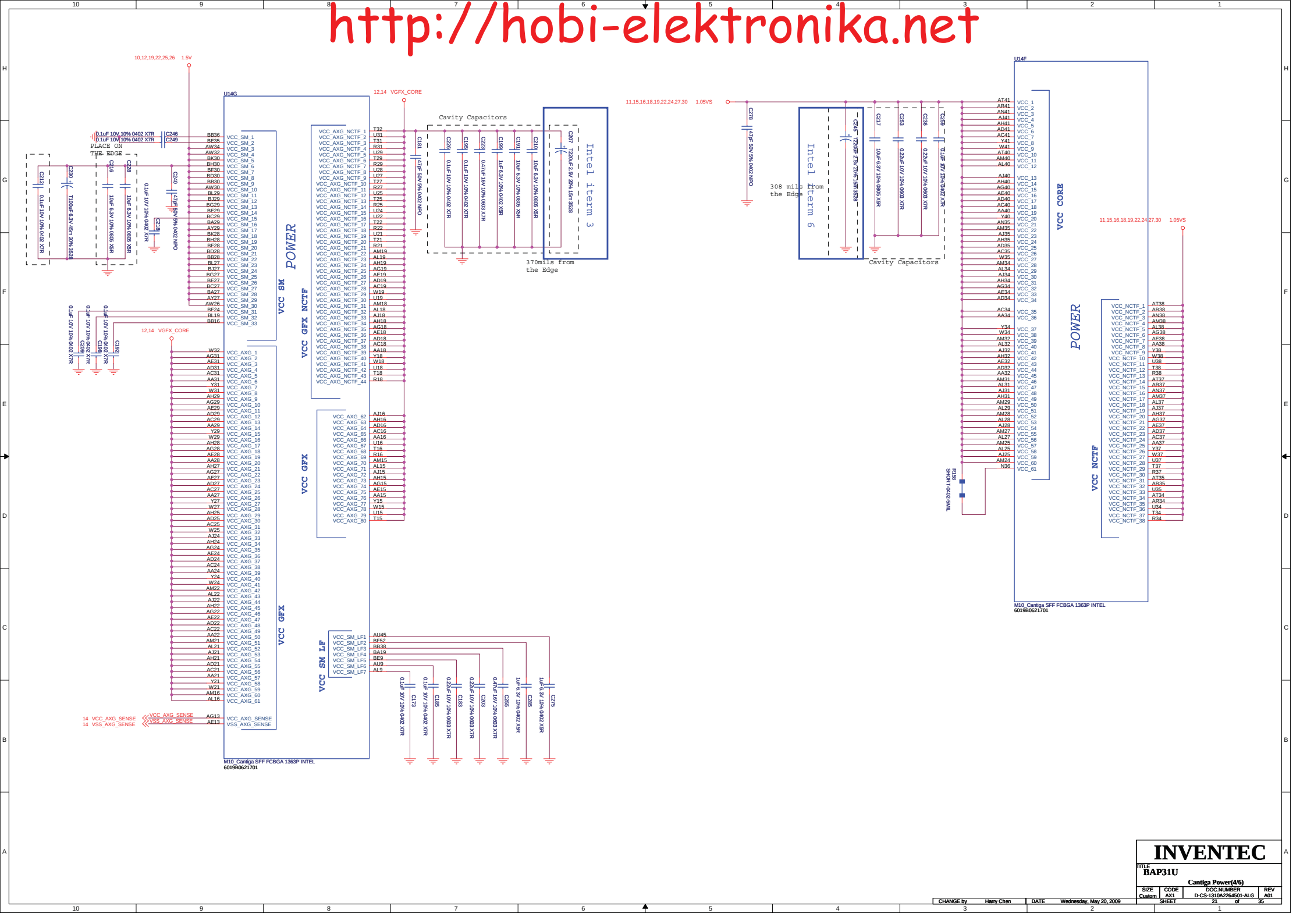
CHANGE by	Harry Chen	DATE	Wednesday, May 20, 2009

INVENTEC

TITLE
BAP31U
Cantiga DDR3(3/6)

SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01

SHEET 20 of 35



CHANGE by	Harry Chen	DATE	Wednesday, May 20, 2009

INVENTEC

TITLE: BAP31U

Cantiga Power(4/6)

SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01

SHEET 21 of 35

0.1uf caps in 1.5VDDM_xPLL need to be located as edge caps within 200mils

30mil

11,15,16,18,19,21,24,27,30 1.05VS

L9 100ohm 25% 2A 0.1ohm 0603 (40mA) 10mil 1.05VS_DPLLA
C277 10uF 6.3V 10% 0805 X5R
C271 0.1uF 10V 10% 0402 X7R

L10 100ohm 25% 2A 0.1ohm 0603 (40mA) 10mil 1.05VS_DPLLB
C288 10uF 6.3V 10% 0805 X5R
C289 0.1uF 10V 10% 0402 X7R

L2 100ohm 25% 2A 0.1ohm 0603 (45mA) 10mil 1.05VS_HPLL
C177 4.7uF 6.3V 10% 0603 X5R
C169 0.1uF 10V 10% 0402 X7R

L28 100ohm 25% 2A 0.1ohm 0603 (45mA) 10mil 1.05VS_MPLL
C441 10uF 6.3V 10% 0805 X5R
C439 0.1uF 10V 10% 0402 X7R

L7 100ohm 25% 2A 0.1ohm 0603 10mil 1.05VS_PEGPLL
C283 10uF 6.3V 10% 0805 X5R
C282 0.1uF 10V 10% 0402 X7R

12,16,27,28,30,31,35 1.5VS

R124 0-5%-1/10W-0603 (24mA) 10mil 1.5VS_TVDAC
C201 0.1uF 10V 10% 0402 X7R
C206 0.01uF 16V 10% 0402 X7R

180ohm 25% 1.5A 0603(FBM-11-160808-181A15T)
L6 10mil 1.5VS_QDAC
C243 0.1uF 10V 10% 0402 X7R
C238 0.01uF 16V 10% 0402 X7R

Caps used in 1.5VDDM_TVDAC and 1.5VDDM_QTVDAC should be within 250mils of edge

3VS 10,11,12,13,14,15,17,19,24,25,26,27,28,29,30,31,32,33,34,35

R134 0-5%-1/10W-0603 (120mA) 10mil VCCS_TVDACA
C224 0.1uF 10V 10% 0402 X7R
C231 0.01uF 16V 10% 0402 X7R

3VDDM_TVDAC should be within 250mils of edge

Vout
R1 Vout=Vref(1+R2/R1)+Iadj*R2
R2=R1(Vout/Vref-1)
FB 1117 Vref=1.250V,Iadj=55uA
R2
GND

180ohm 25% 1.5A 0603(FBM-11-160808-181A15T)
3VS L5
10,11,12,13,14,15,17,19,24,25,26,27,28,29,30,31,32,33,34,35
C219 0.01uF 16V 10% 0402 X7R 20mil
C229 0.1uF 10V 10% 0402 X7R
C244 0.01uF 16V 10% 0402 X7R 20mil
C239 0.1uF 10V 10% 0402 X7R

U14H

CRT: VCCA_CRT_DAC J31; VCCA_DAC_BG L31; VSSA_DAC_BG M33
PLL: 1.05VS_DPLLA J45 VCCA_DPLLA; 1.05VS_DPLLB L49 VCCA_DPLLB; 1.05VS_HPLL AE10 VCCA_HPLL; 1.05VS_MPLL AE1 VCCA_MPLL
A PEG A LVDS: 1.8V_TXLVDS C260 1000pF 50V 10% 0402 X7R; VCCA_LVDS1 U43; VCCA_LVDS2 U41; VSSA_LVDS V44
12,16,27,28,30,31,35 1.5VS C262 0.1uF 10V 10% 0402 X7R; VCCA_PEG_BG AJ43; 1.05VS_PEGPLL VCCA_PEG_PLL AG43
D POWER A SM: 11,15,16,18,19,21,24,27,30 1.05VS
C197 10uF 6.3V 10% 0805 X5R; C198 4.7uF 6.3V 10% 0603 X5R; C205 10uF 6.3V 10% 0805 X5R; C186 1uF 6.3V 10% 0402 X5R
VCCA_SM_1 AW24; VCCA_SM_2 AU24; VCCA_SM_3 AW22; VCCA_SM_4 AU22; VCCA_SM_5 AU21; VCCA_SM_6 AW20; VCCA_SM_7 AU19; VCCA_SM_8 AW18; VCCA_SM_9 AU18; VCCA_SM_10 AW16; VCCA_SM_11 AU16; VCCA_SM_12 AT16; VCCA_SM_13 AR16; VCCA_SM_14 AU15; VCCA_SM_15 AT15; VCCA_SM_16 AR15; VCCA_SM_17 AW14
VCCA_SM_NCTF_1 AT24; VCCA_SM_NCTF_2 AR24; VCCA_SM_NCTF_3 AT22; VCCA_SM_NCTF_4 AR22; VCCA_SM_NCTF_5 AT21; VCCA_SM_NCTF_6 AR21; VCCA_SM_NCTF_7 AT19; VCCA_SM_NCTF_8 AR19; VCCA_SM_NCTF_9 AT18; VCCA_SM_NCTF_10 AR18
11,15,16,18,19,21,24,27,30 1.05VS
C222 10uF 6.3V 10% 0805 X5R; C227 4.7uF 6.3V 10% 0603 X5R; C215 0.1uF 10V 10% 0402 X7R
VCCA_SM_CK_4 AU27; VCCA_SM_CK_3 AU28; VCCA_SM_CK_2 AU29; VCCA_SM_CK_1 AU31
VCCA_SM_CK_NCTF_1 AT31; VCCA_SM_CK_NCTF_2 AR31; VCCA_SM_CK_NCTF_3 AT29; VCCA_SM_CK_NCTF_4 AR29; VCCA_SM_CK_NCTF_5 AT28; VCCA_SM_CK_NCTF_6 AR28; VCCA_SM_CK_NCTF_7 AT27; VCCA_SM_CK_NCTF_8 AR27
11,15,16,18,19,21,24,27,30 1.05VS
0.1uF 10V 10% 0402 X7R C258; VCCD_HPLL AH12
1.05VS_PEGPLL C261 0.1uF 10V 10% 0402 X7R; VCCD_PEG_PLL AE43
VCCD_LVDS_1 M46; VCCD_LVDS_2 L45
11 1.8V C274 1uF 6.3V 10% 0402 X5R
M10_Cantiga SFF FCBGA 1363P INTEL 6019B0621701

VTT: VTT_1 R13, VTT_2 T12, VTT_3 R11, VTT_4 T10, VTT_5 R9, VTT_6 T8, VTT_7 R7, VTT_8 T6, VTT_9 R5, VTT_10 T4, VTT_11 R3, VTT_12 T2, VTT_13 R1
11,15,16,18,19,21,24,27,30 1.05VS
C444 4.7uF 6.3V 10% 0603 X5R; C443 4.7uF 6.3V 10% 0603 X5R; C442 2.2uF 6.3V 20% X5R 0603; C440 0.47uF 10V 10% 0603 X7R
PLACE ON THE EDGE
C158 T100uF 6.3V 45m 20% 3528_NU
TV: VCCA_TV_DAC K30 10mil VCCS_TVDACA
HDA: VCC_HDA A31 1.5VS 12,16,27,28,30,31,35; C454 0.1uF 10V 10% 0402 X7R
TV/CRT HDA: VCCD_QDAC N34 1.5VS_QDAC; VCCD_TVDAC N32 1.5VS_TVDAC
AXF: VCC_AXF_1 M25, VCC_AXF_2 N24, VCC_AXF_3 M23
30mil 1uF 6.3V 10% 0402 X5R 1.05VS 11,15,16,18,19,21,24,27,30
C211 C202 10uF 6.3V 10% 0805 X5R_NU
30mil C204 0.1uF 10V 10% 0402 X7R C200 10uF 6.3V 10% 0805 X5R L3 1.5V 10,12,19,21,25,26 100ohm 25% 2A 0.1ohm 0603
SM CK: VCC_SM_CK_1 BK24, VCC_SM_CK_2 BL23, VCC_SM_CK_3 BJ23, VCC_SM_CK_4 BK22
1.8V_TXLVDS
1000pF 50V 10% 0402 X7R 10mil L8 120ohm 25% 200mA 0603(BLM11A121S) 1.8V 11
VCC_TX_LVDS T41
VCC_HV_1 C33, VCC_HV_2 A33 3VS_HV
C256 C252 22uF 6.3V 20% 0805 X5R_NU
HV: 30mil 10uF 6.3V 10% 0805 X5R
PEG: VCC_PEG_1 AB44, VCC_PEG_2 Y44, VCC_PEG_3 AC43, VCC_PEG_4 AA43
C281 C279 T100uF 6.3V 45m 20% 3528_NU 1.05VS 11,15,16,18,19,21,24,27,30
DMI: VCC_DMI_1 AM44, VCC_DMI_2 AN43, VCC_DMI_3 AL43
20mil C276 C280 0.1uF 10V 10% 0402 X7R
VTTLF: VTTLF1 K14, VTTLF2 Y12, VTTLF3 P2; VTTLF_CAP1, VTTLF_CAP2, VTTLF_CAP3
C175 0.47uF 16V 10% 0603 X7R; C188 0.47uF 16V 10% 0603 X7R; C189 0.47uF 16V 10% 0603 X7R; 10uF 6.3V 10% 0805 X5R

3VS 10,11,12,13,14,15,17,19,24,25,26,27,28,29,30,31,32,33,34,35
R360 10-5%-1/10W-0603 D23 1SS355PT 90V 0.5A 1.05VS 11,15,16,18,19,21,24,27,30
R361 SHORT-0402-15MIL 20mil C456 0.1uF 10V 10% 0402 X7R 3VS_HV

CHANGE by	Harry Chen	DATE	Wednesday, May 20, 2009

INVENTEC

TITLE BAP31U

Cantiga Power(5/6)

SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01

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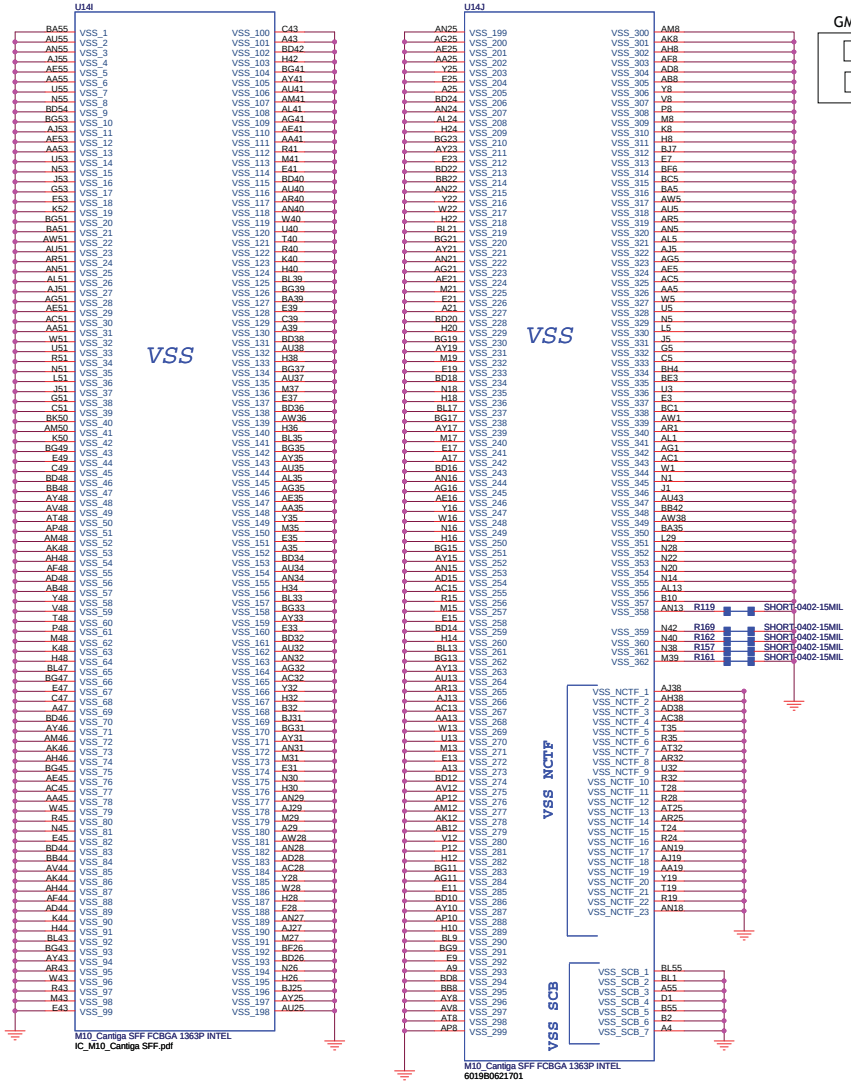
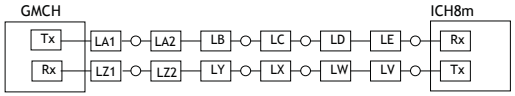


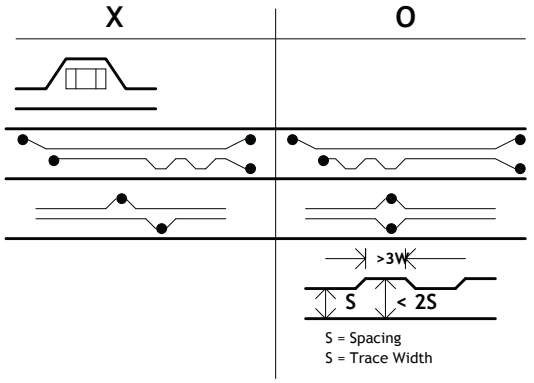
DMI Routing Guideline



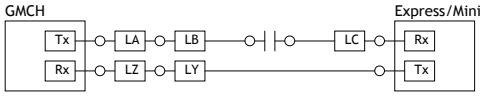
Breakout/in LA/LZ	Main Route LB/LY		Breakout/in LE/LV
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip

Parameter	Main Route Guideline	Breakout Guideline
Uncoupled Single End Impedance	55 +/- 15%	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils	
Nominal Didderential Pair-Pitch	Inner Layer : 7 mils Outer Layer : 7 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Pair-to-Pair Pitch	Inner Layer : 37 mils Outer Layer : 37 mils	Inner Layer : 27 mils Outer Layer : 27 mils
Bus-to-Bus Pitch	Inner Layer : 22 mils Outer Layer : 20 mils	Inner Layer : 15 mils Outer Layer : 12 mils
Reference Plane	Ground	Ground
Splits/Voids	No routing over plane splits No routing over voids	
Trace Length-LA (GMCH Breakout)	Max = 250 mils	
Trace Length-LB (GMCH Breakout to Via2)	Max = 3600 mils	
Trace Length-LC (Via2 to Via3)	Max = 5900 mils	
Trace Length-LD (Via3 to ICH7m Breakout)	Max = 3600 mils	
Trace Length-LE (ICH7m Breakout)	Max = 400 mils	
Trace Length-L1 (LA+LB+LC+LD+LE)	Max = 8000 mils	
Trace Length-LV (ICH7m Breakout)	Max = 400 mils	
Trace Length-LW (ICH7m Breakout to Via2)	Max = 3600 mils	
Trace Length-LX (Via2 to Via3)	Max = 5900 mils	
Trace Length-LY (Via3 to GMCH Breakout)	Max = 3600 mils	
Trace Length-LZ (GMCH Breakout)	Max = 400 mils	
Trace Length-L2 (LV+LW+LX+LY+LZ)	Max = 8000 mils	

*** When routing near the edge of their reference plane , trace should maintain at least 40 mils space to the edge of the plane
*** Match the trace lengths of the complementary signals within each differential pair to +/- 5 mils



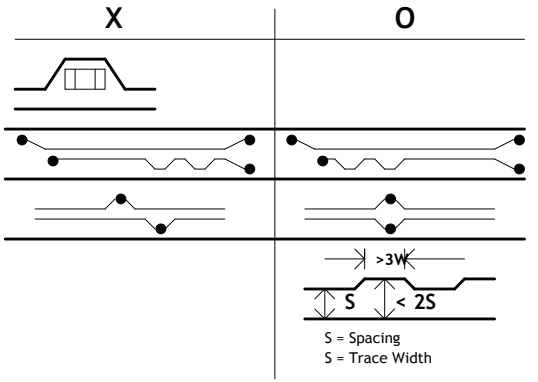
PCIE Routing Guideline



Breakout/in LA/LZ	Main Route LB/LC/LY	Main Route LD/LW	Breakout/in LE/LV
Stripline	Microstrip	Same Routing layer as LE/LV	Microstrip

Parameter	Main Route Guideline	Breakout Guideline
Uncoupled Single End Impedance	55 +/- 15%	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils	
Nominal Differential Trace Space	Inner Layer : 7 mils Outer Layer : 7 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Pair-to-Pair Pitch	Inner Layer : 37 mils Outer Layer : 37 mils	Inner Layer : 27 mils Outer Layer : 27 mils
Bus-to-Bus Pitch	Inner Layer : 20 mils Outer Layer : 20 mils	Inner Layer : 15 mils Outer Layer : 12 mils
Reference Plane	Ground	Ground
Splits/Voids	No routing over plane splits No routing over voids	
Trace Length-LA (ICH7m Breakout)	Max = 400 mils	
Trace Length-LB (ICH7m Breakout to AC cap)	Max = 10750 mils	
Trace Length-LC (AC cap to PCIe CN)	Max = 10750 mils	
Trace Length-L1 (LA+LB+LC)	Max = 12000 mils	
Trace Length-LY (PCIe CN to ICH7m Breakout)	Max = 11950 mils	
Trace Length-LZ (ICH7m Breakout)	Max = 400 mils	
Trace Length-L2 (LY+LZ)	Max = 12000 mils	

*** When routing near the edge of their reference plane , trace should maintain at least 40 mils space to the edge of the plane
*** Match the trace lengths of the complementary signals within each differential pair to +/- 5 mils



CHANGE by	Harry Chen	DATE	Wednesday, May 20, 2009

INVENTEC

TITLE
BAP31U
Cantiga Ground(6/6)

SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01

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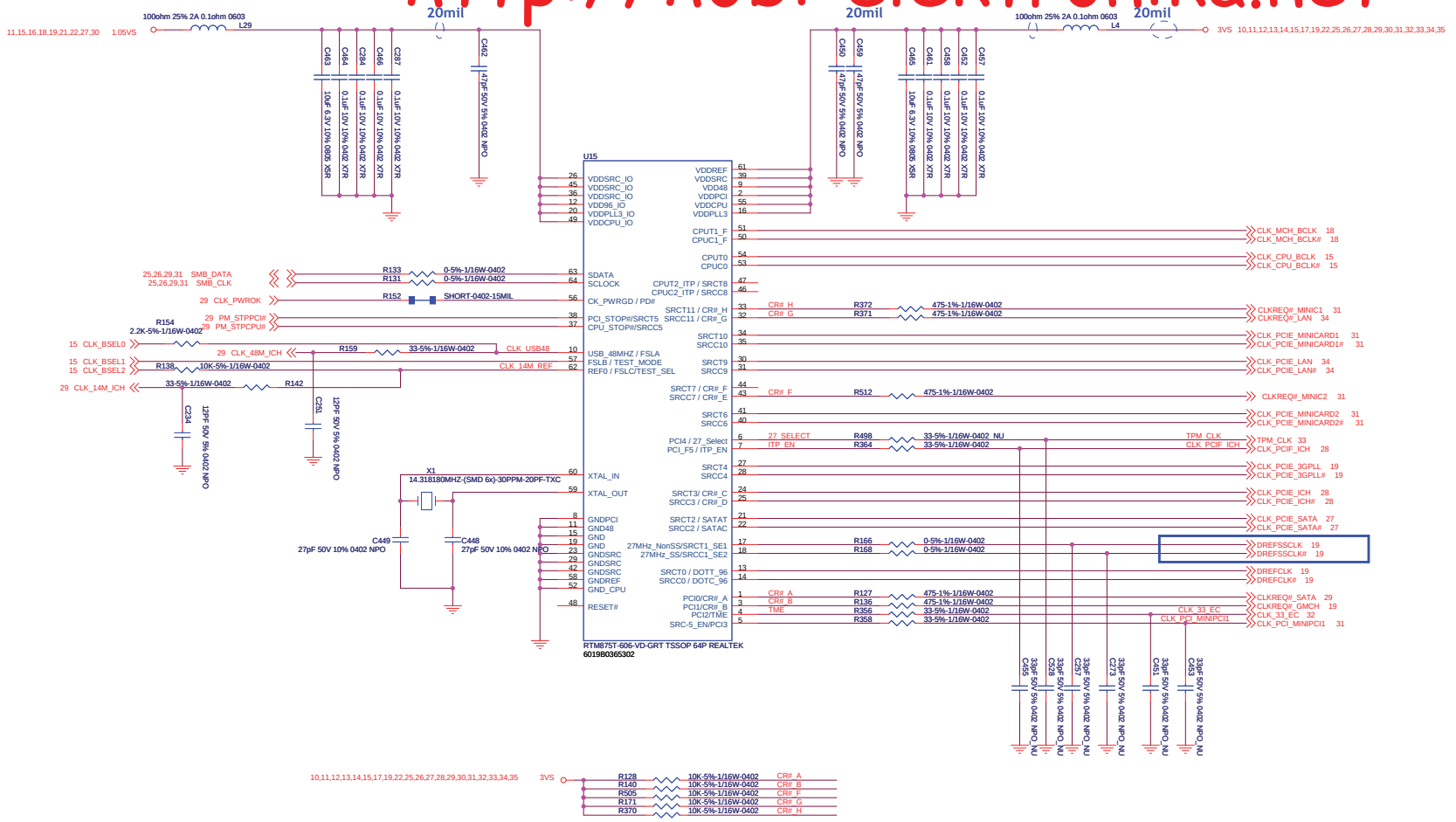

CR#_A:	Byte 5 bit 6=0--->SRC0 bit 6=1--->SRC2	BIT 7=1 (Enable)
CR#_C:	Byte 5 bit 2=0--->SRC0 bit 2=1--->SRC2	BIT 3=1 (Enable)
CR#_B:	Byte 5 bit 4=0--->SRC1 bit 4=1--->SRC4	BIT 5=1 (Enable)
CR#_D:	Byte 5 bit 0=0--->SRC1 bit 0=1--->SRC4	BIT 1=1 (Enable)
CR#_E:	SRC6 (Byte 6)	BIT 7=1 (Enable)
CR#_F:	SRC8 (Byte 6)	BIT 6=1 (Enable)
CR#_G:	SRC9 (Byte 6)	BIT 5=1 (Enable)
CR#_H:	SRC10 (Byte 6)	BIT 4=1 (Enable)

FSA	FSB	FSC	FSB CLOCK FREQUENCY	HOST CLOCK FREQUENCY
1	1	0	667	166
0	1	0	800	200
0	0	0	1067	266 *

By Tony

CHANGE by	Harry Chen	DATE	Wednesday, May 20, 2009	

INVENTEC

TITLE: BAP31U

Clock Generator

SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01

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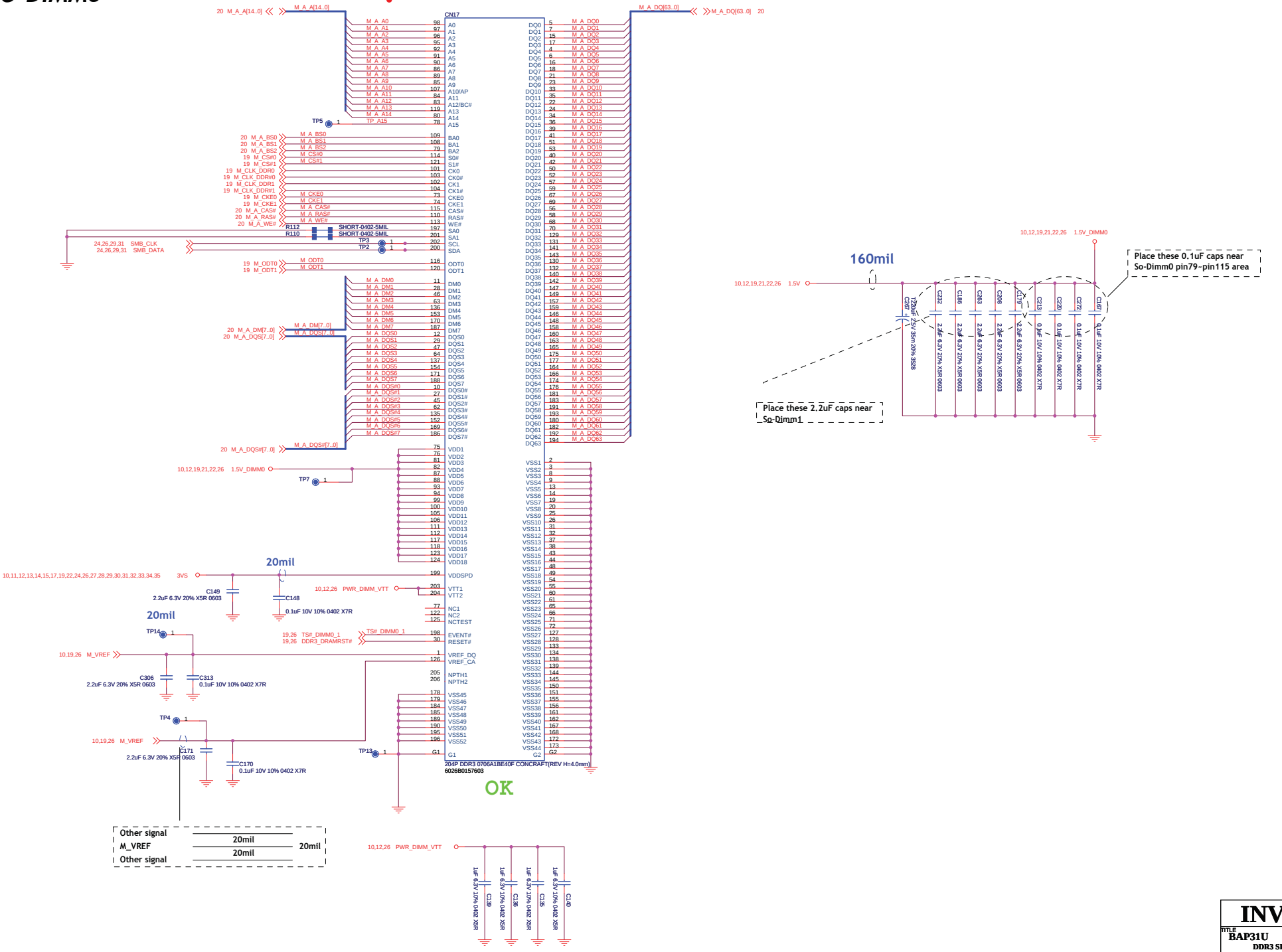
SO-DIMM0



CHANGE by	Harry Chen
DATE	Wednesday, May 20, 2009

INVENTEC

TITLE: **BAP31U**
DDR3 SDRAM SO-DIMM0

SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01

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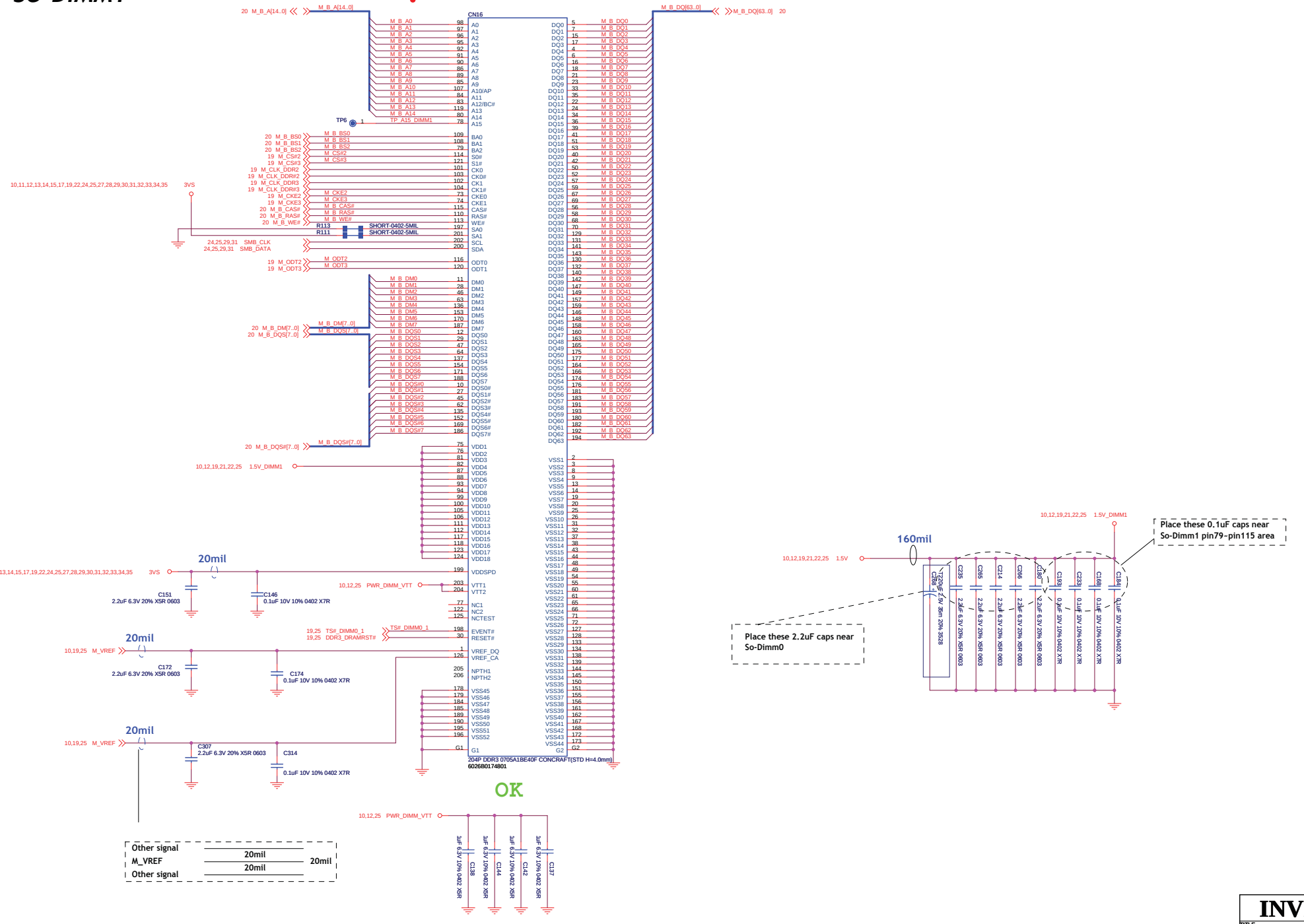
SO-DIMM1



CHANGE by	Harry Chen	DATE	Wednesday, May 20, 2009

INVENTEC

TITLE
BAP31U
DDR3 SDRAM SO-DIMM1

SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01
	SHEET	26 of 35	

RTC Circuit

1. RC delay time should be in the range of 18~25ms
2. It is recommended that this larger capacitor and small resistor value in order to reduce the likelihood of glitching of RTCRST#

1. The ICH7m requires a length less than 1 inch on each branch (from crystal's terminal to RTCXn ball)
2. Routing the RTC circuit should be kept simple to simplify the trace length measurement and increase accuracy on calculating trace capacitances
3. On FR-4, a 5-mils trace has approximately 2pF per inch
4. Trace signal coupling must limited as much as possible by avoiding the routing of adjacent PCI signals close to RTCX1 and RTCX2
5. Ground guard plane is highly recommended

For JM31,SJM31 For BAP31

For Green PC

BATT1

CABLE,ROUND,3POS,75mm,1,RTC_NU
6027B0066801

Place all series resistors 0.6 to 2.6 inches from the ICH9

Needs to be placed within 2" of ICH9m

Must be placed within 2" of 24.9 ohm w/o stub

Distance between the ICH9-M and cap on the "P" signal should be identical distance between the ICH9-M and cap on the "N" signal for same pair.

Placed within 500mils of ICH9m ball

ICH8m internal VR enable strap

	Enable	Disable
INTVRMEN	1(Default)	0

Internal VRM enabled for VccSus1_05, VccSus1_5, VccCL1_5, VccLAN1_05 and VccCL1_05

Short pins AG1 and AG2 at the package

ACZ_SDATAOUT strap functionality base on RSVD9 strap
XOR chain entrance (RSVD9 pulled low)
PCIE port config bit 1(RSVD9 not pulled low)

Stuff for XOR chain testing

XOR Chain Entrance Strap - to be updated		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1

By Tony

INVENTEC

TITLE: BAP31U
ICH9M CPU/IDE/SATA(1/4)

SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01

CHANGE by: Harry Chen | DATE: Wednesday, May 20, 2009 | SHEET 27 of 35

PCIE AC coupling caps need to be within 250mils of the driver

WLAN
3G
LAN

U18D
PCI-Express
Direct Media Interface
SPI
USB
M10_ICH9M_SFF FCBGA 569P INTEL
6019B06218801

STUFF for iTPM enable

Place within 500mils of ICH
10mil
Place within 500mils of ICH
5/5 mils spacing on microstrip

U16
W25X32VSSIG SOIC 8P Winbon_NU
6019B0499501_NU

By Tony

U18B
PCI
Interrupt I/F
M10_ICH9M_SFF FCBGA 569P INTEL
6019B0621801

PCI Pull up

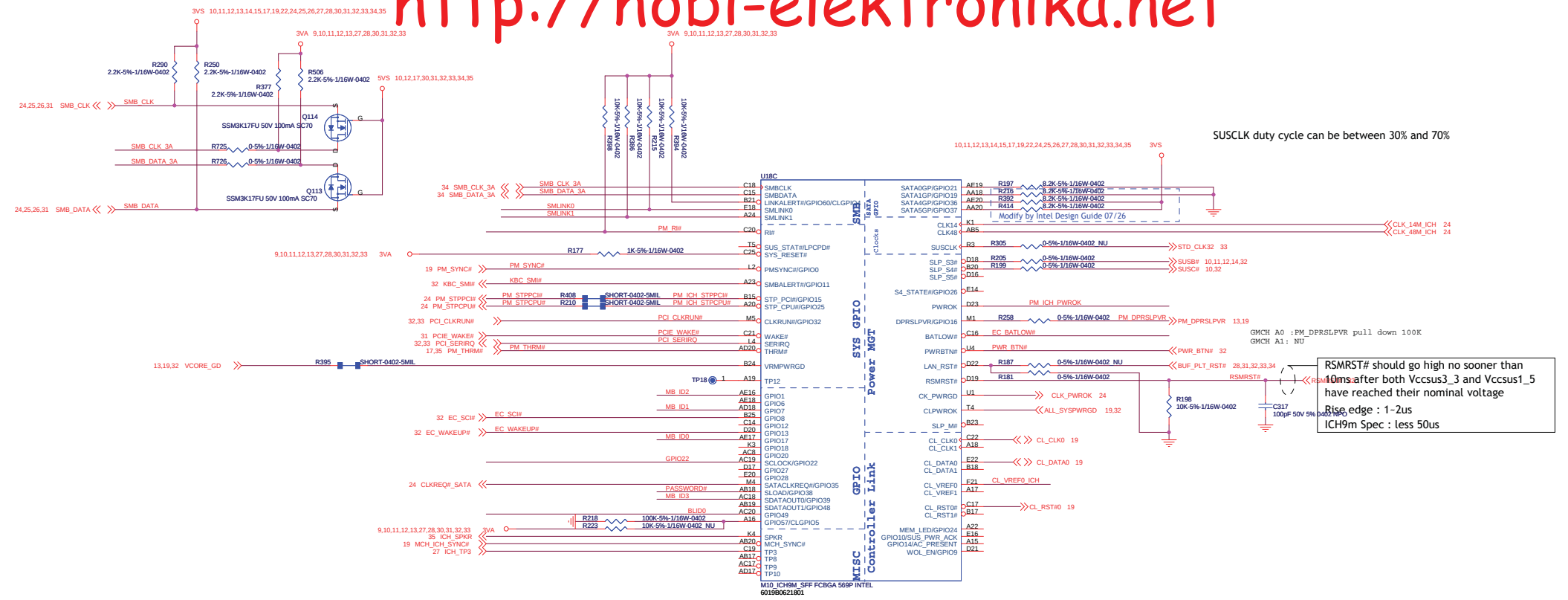
Buffer to reduce loading on PLT_RST#

PCI_GNT#3	No stuff : by default Stuff : For A16 swap override

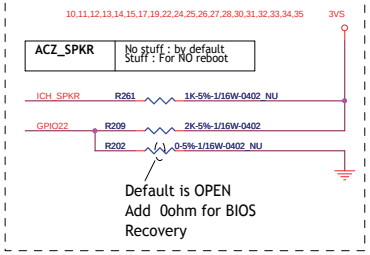
PCI_GNT#0	SPI_CS1#	
1	1	LPC
1	0	PCI
0	1	SPI

Check BIOS type

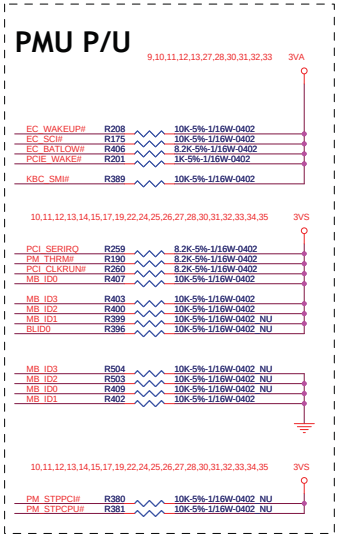
INVENTEC
TITLE: BAP31U
ICH9M PCI/PCIE/DMI/USB(2/4)
SIZE: Custom | CODE: AX1 | DOC.NUMBER: D-CS-1310A2264501-ALG | REV: A01
CHANGE by: Harry Chen | DATE: Wednesday, May 20, 2009 | SHEET: 28 of 35



ICH9m strap

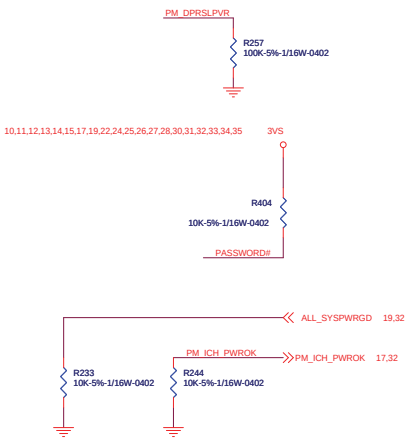


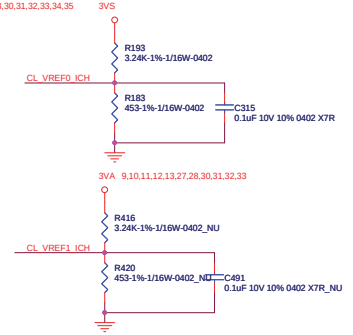
PMU P/U



BIOS ID setting

Project	MB_ID3	MB_ID2	MB_ID1	MB_ID0
JM31 (UMA)	1	1	1	1
SJM31 (UMA)	1	1	1	0
BAP31 (UMA)	1	1	0	1
	1	1	0	0
	1	0	1	1
	1	0	1	0
	1	0	0	1
	1	0	0	0
	0	1	1	1
	0	1	1	0
	0	1	0	1
	0	1	0	0
	0	0	1	1
	0	0	1	0
	0	0	0	1
	0	0	0	0





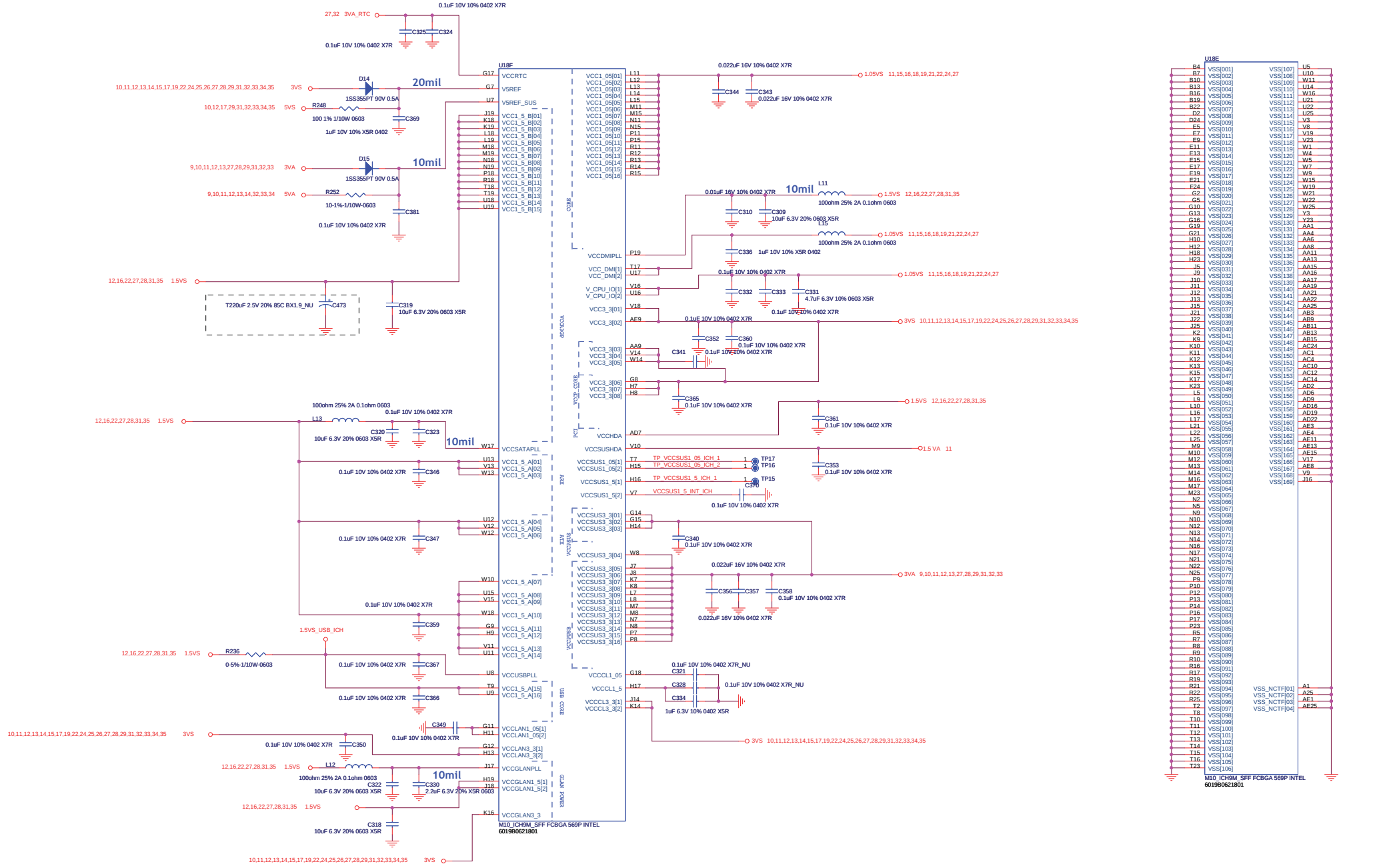
CHANGE by	Harry Chen	DATE	Wednesday, May 20, 2009

INVENTEC

TITLE: BAP31U
ICH9M GPIO(3/4)

SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01

SHEET 29 of 35



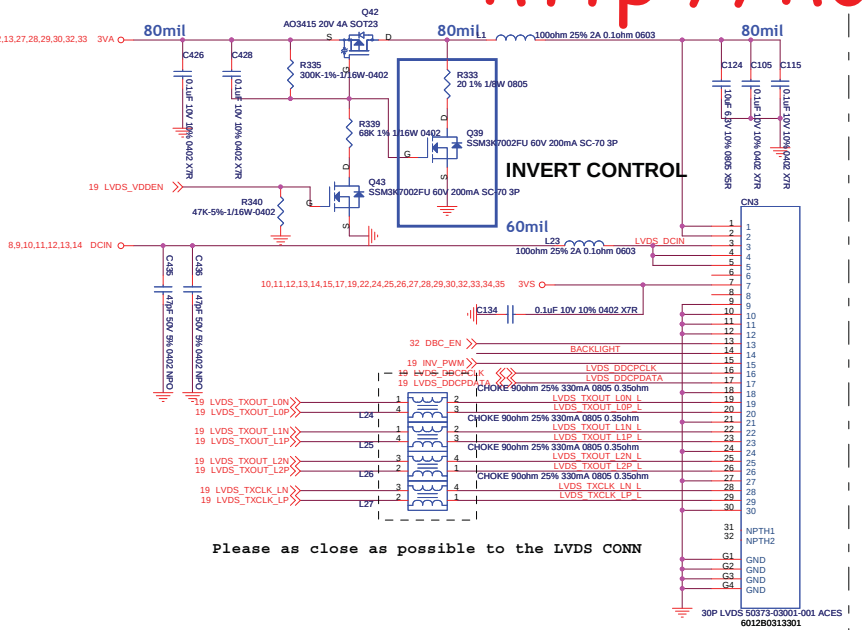
CHANGE by	Harry Chen	DATE	Wednesday, May 20, 2009

INVENTEC

TITLE
BAP31U
ICH9M Power/GND(4/4)

SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01
	SHEET	30 of 35	

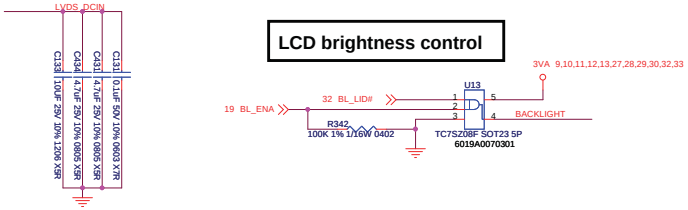
LVDS Interface



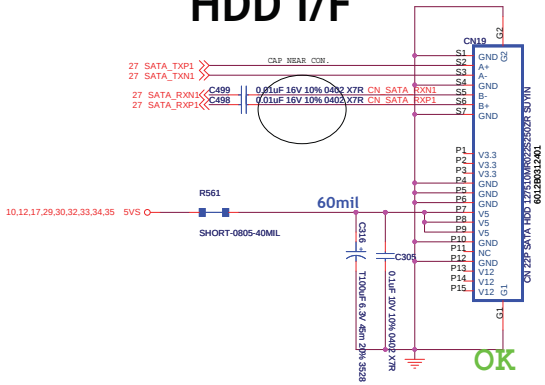
Please as close as possible to the LVDS CONN

OK

LCD brightness control

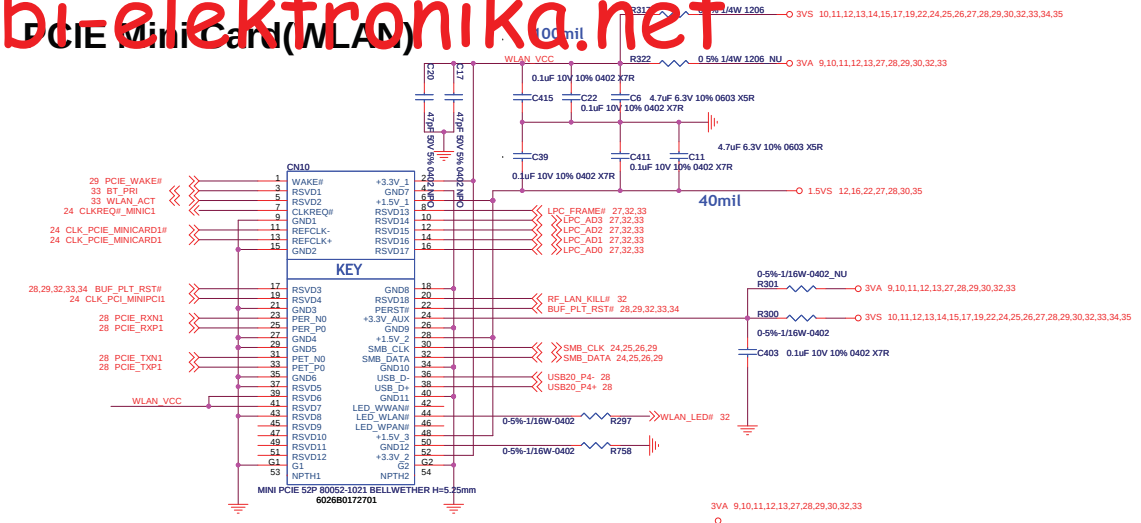


HDD I/F



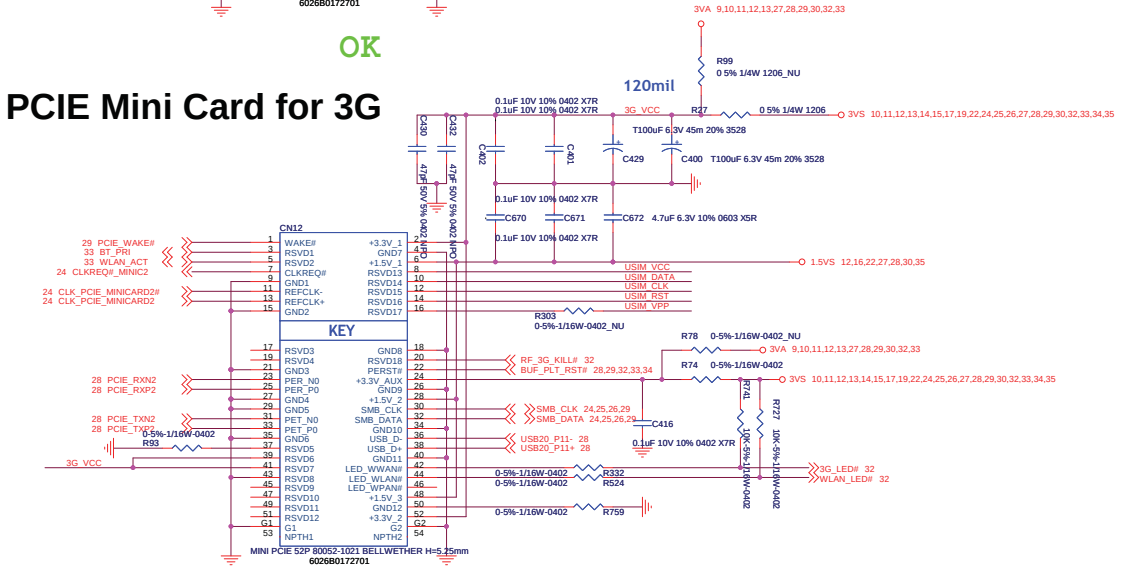
OK

PCIE Mini Card(WLAN)



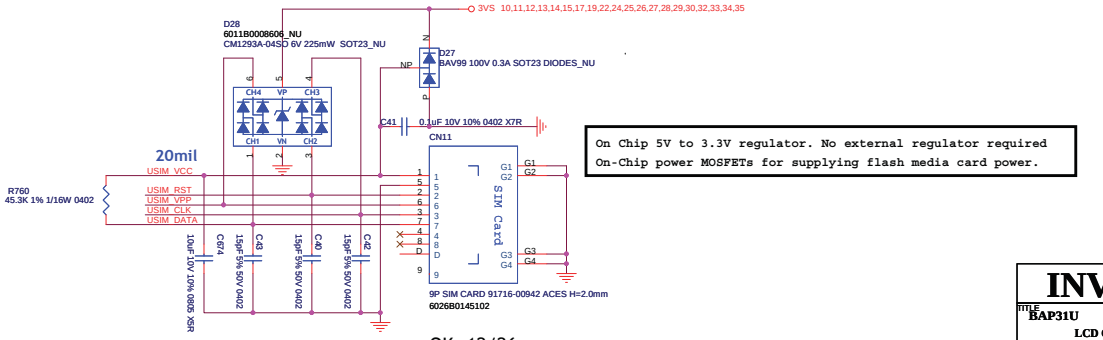
OK

PCIE Mini Card for 3G



SIM CARD slot

OK



On Chip 5V to 3.3V regulator. No external regulator required
On-Chip power MOSFETs for supplying flash media card power.

OK, 12/26

INVENTEC	
TITLE	BAP31U
	LCD CNN & WLAN & 3G
SIZE	Custom
CODE	AX1
DOC.NUMBER	D-CS-1310A2264501-ALG
REV	A01
SHEET	31 of 35
CHANGE by	Harry Chen
DATE	Wednesday, May 20, 2009

IT8502E-L

For Green PC

SPI FLASH

U20 W25X16AVSSIG 16M SOIC 8P
6019B0307303

Don't place any pull-up resistor on GPG0 and GPG6

Pull down is for SPI flash

IT8502E-L LQFP 128P ITE
6019B0617001

GPIO groud I are only input mode
Group I and J are not 5V tolerant
GPIO groud J are only output mode

SW Sensor BOARD(For JM31,SJM31)

CN2 CN 12P 88501-1201 ACES_NU
6012B0104502_NU

OK

SW (FOR JM31,BAP31) OK

SW2 5P NTC020-LA1J-B160T MISAKI
6026B0061801

SW (FOR SJM31) OK

SW3 5P NTC020-LA1J-B160T MISAKI_NU
6026B0061801_NU

To K/B(For JM31,BAP31)

CN4 CN 26P FPC 88502-2601 ACES
6012B0042110

OK

	R239	C363
For IT8502IX	0 Ohm	NU
For IT8502JX	NU	0.1uF

CHANGE by	Harry Chen	DATE	Wednesday, May 20, 2009

INVENTEC

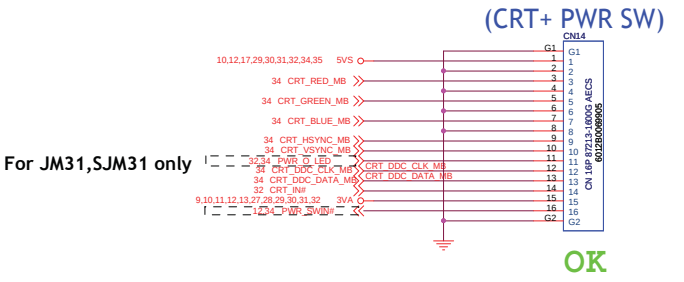
TITLE: BAP31U
KBC ITE8512F/IO

SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01

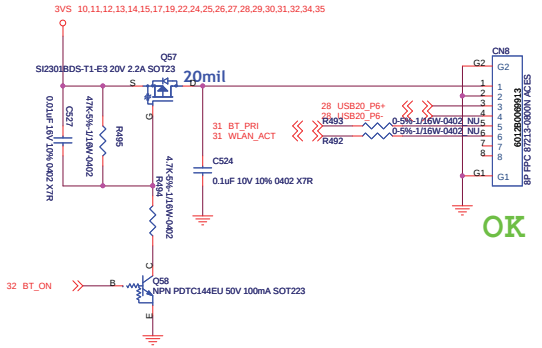
SHEET 32 of 35

VGA Board CN

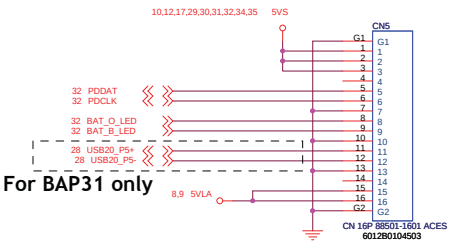
(CRT+ PWR SW)



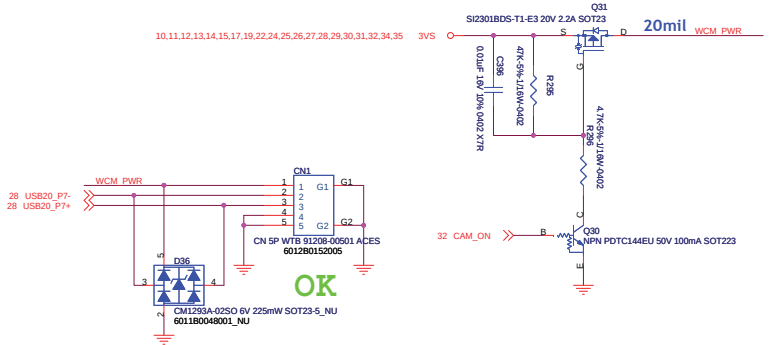
Bluetooth CON.



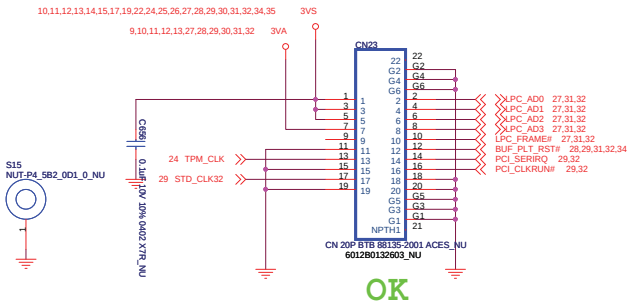
MB(GP) TO GP/B



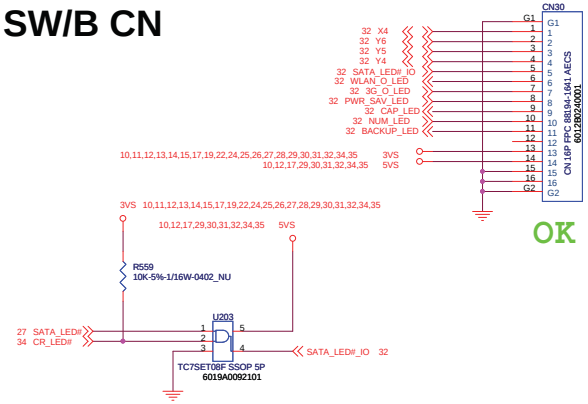
WEB Cam.

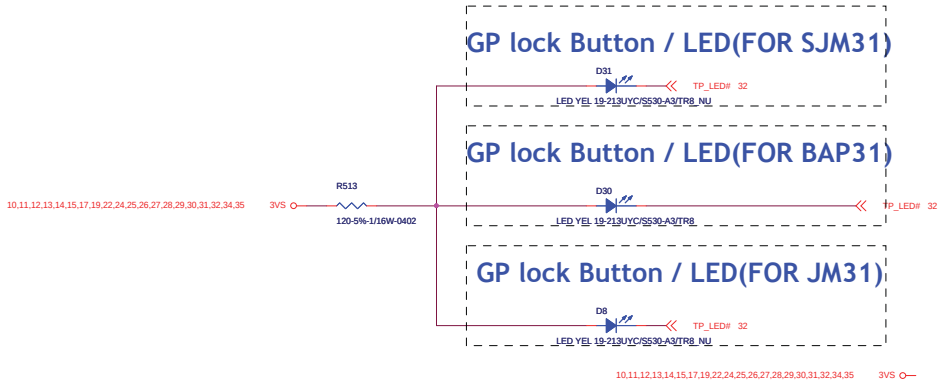


TPM CN



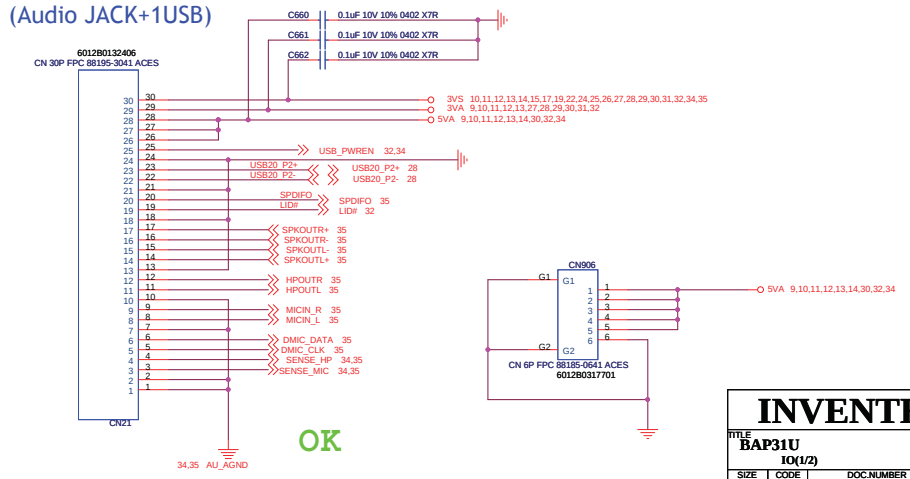
SW/B CN





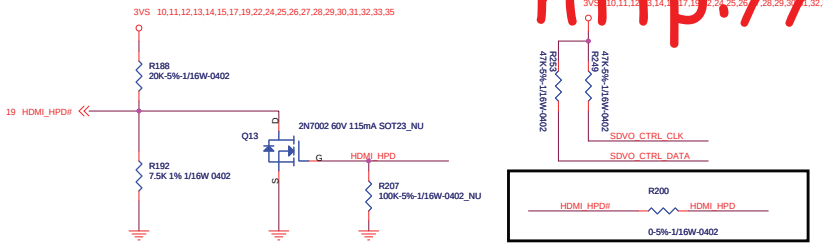
AUDIO Board CN

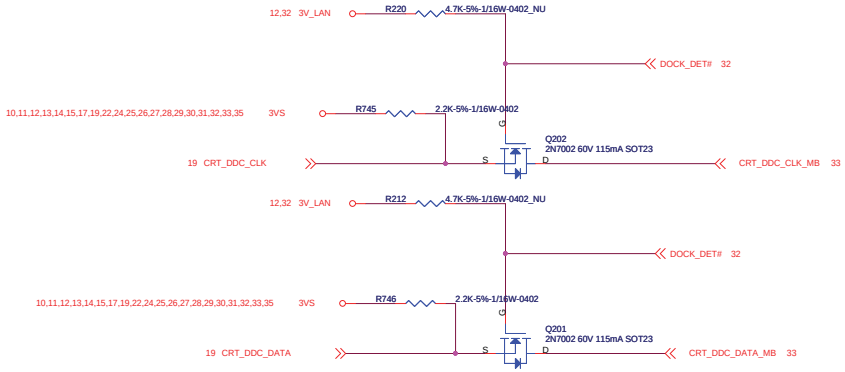
(Audio JACK+1USB)

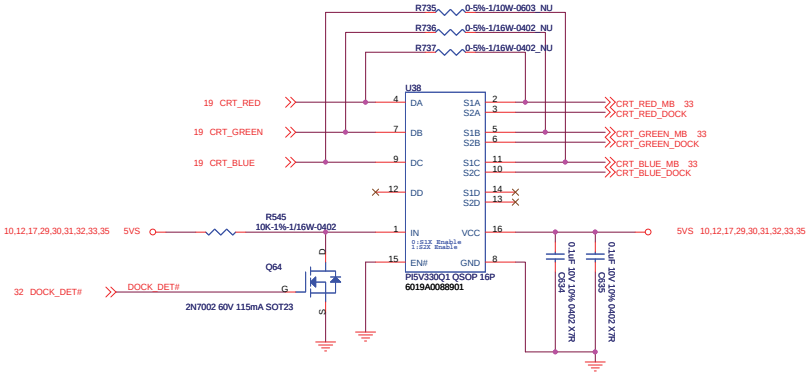


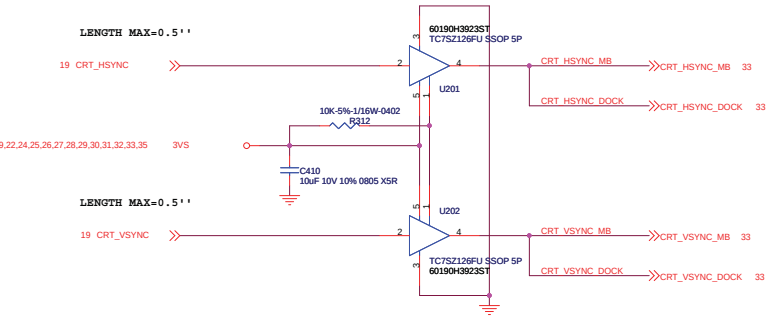
INVENTEC			
TITLE: BAP31U IO(1/2)			
SIZE: Custom	CODE: AX1	DOC NUMBER: D-CS-1310A2264501-ALG	REV: A01
CHANGE by: Harry Chen	DATE: Wednesday, May 20, 2009	SHEET: 33 of 35	

For BAP31 IO/B

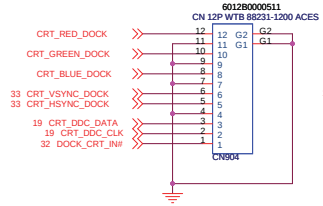




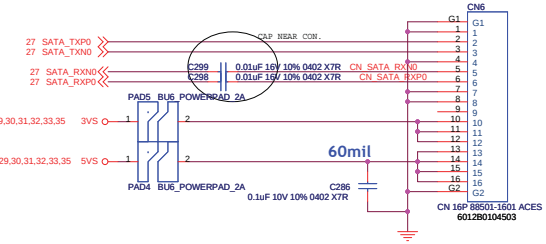




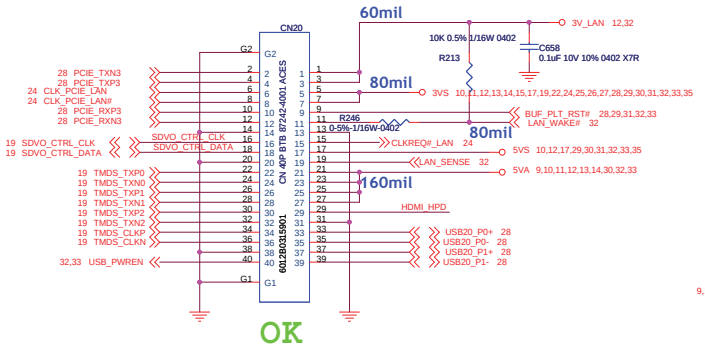
MB(RGB) TO IO/B



MB(SSD) TO IO/B

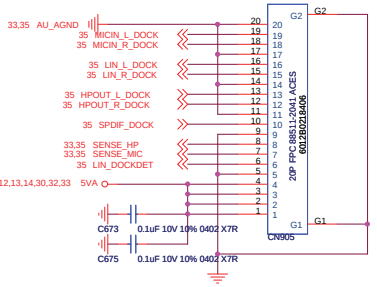


MB(LAN+HDMI+2USB) TO IO/B

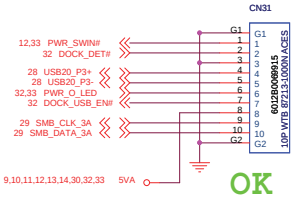


OK

MB(AUDIO) TO IO/B

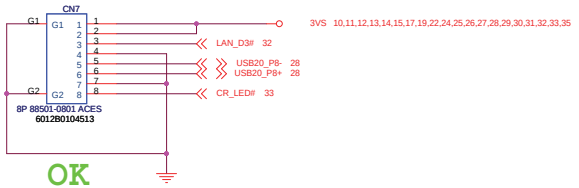


MB(USB) TO IO/B



OK

MB(CardReader) TO IO/B



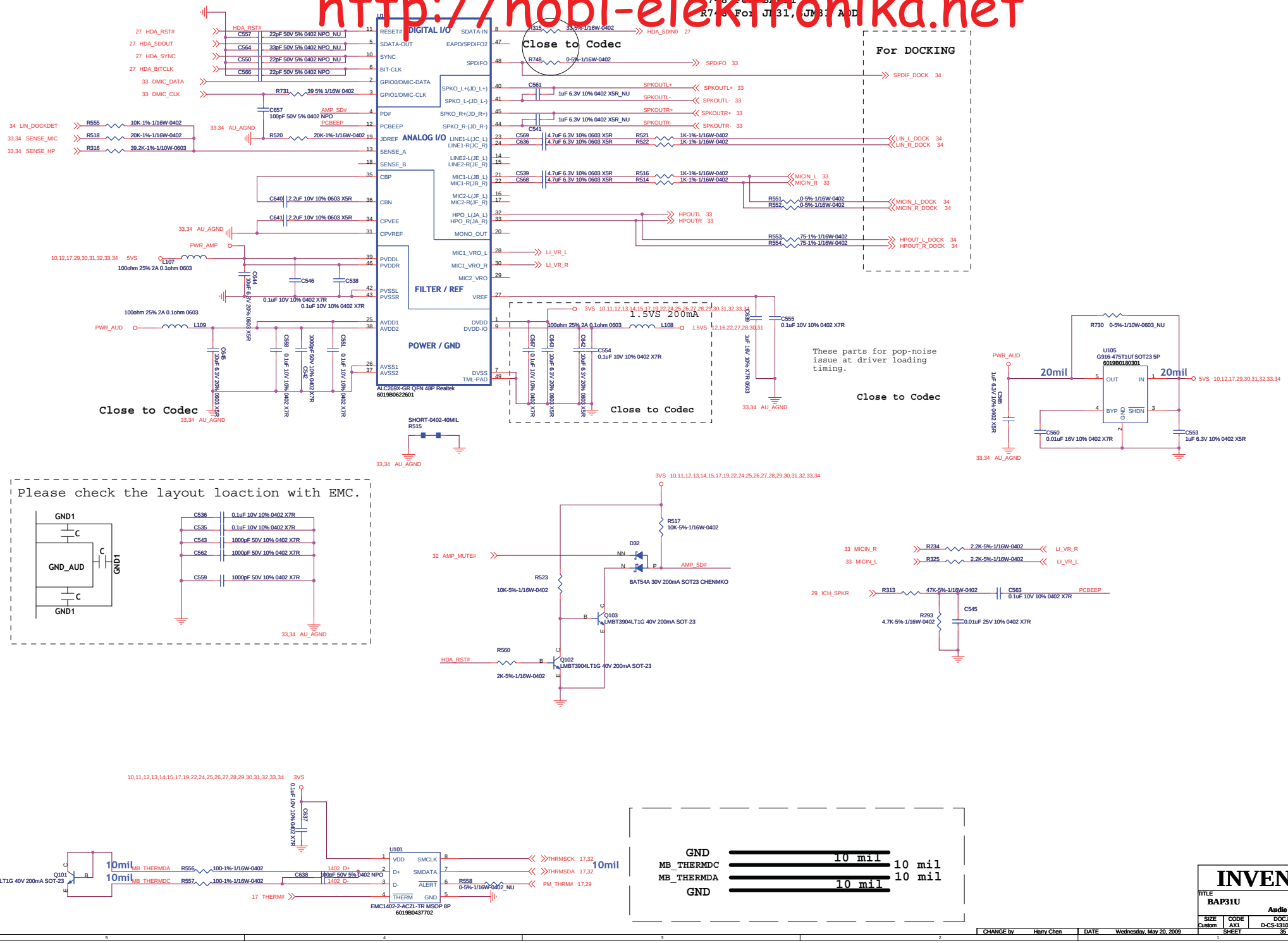
OK

CHANGE by	Harry Chen	DATE	Wednesday, May 20, 2009		

INVENTEC

TITLE: BAP31U
IO(2/2)

SIZE	CODE	DOC NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01
		SHEET 34 of 35	



INVENTEC	
TITLE	BAP31U
	Audio Codec
SIZE	Custom
CODE	AX1
DOC NUMBER	D-CS-1310A2264501-ALG
REV	A01
SHEET	35 of 35
CHANGE by	Harry Chen
DATE	Wednesday, May 20, 2009