Inventec Corporation
R&D Division

Board name : Mother Board Schematic

Project : E25

Version : A02 (MV Build)

Initial Date : Jan 1 , 2006

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1. Schematic Page Description :

Schematic Ver : A01

For E23 Add and Del Function Component List.

```
Remove MDC function (Page 20)
CN13 L38 R292 C384

Add one USB port (Page 30)
U1002 L1002 C1003 C1004 CN1003

Add audio Function (Page 29)
Del C344 R266
Add R263 C345

For K/B Function
Del R44 R52
Add R45 R50
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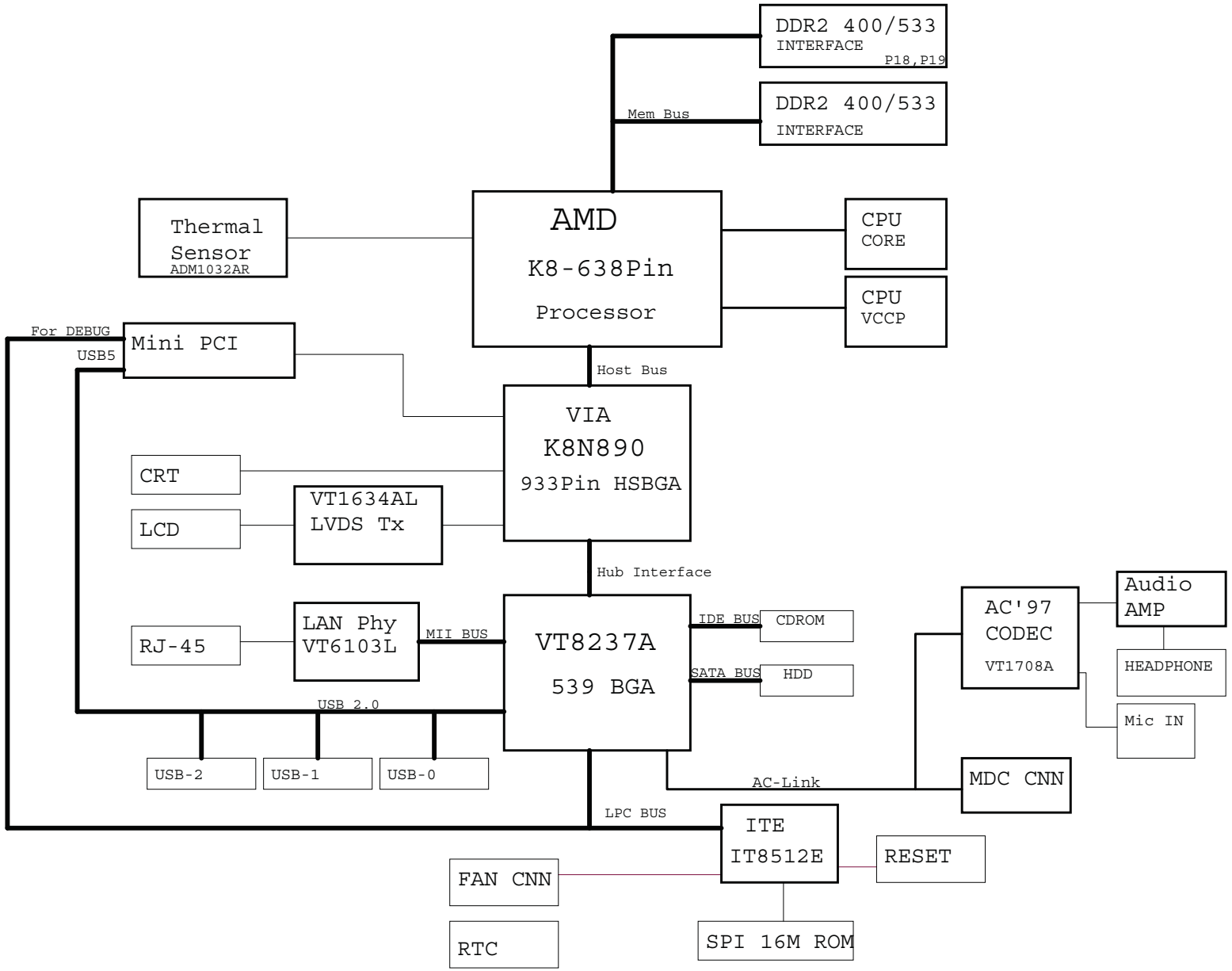
3. Block Diagram :



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4. Nat name Description :

Voltage Rails

DCIN	Primary DC system power supply
5VLA	5.0V always on power rail by LATCH or ACIN
5VA	5.0V always on power rail by ECPWON
3VA	3.3V always on power rail by ECPWON
5V	5.0V power rail by SLP_S5#_3R
3V	3.3V power rail by SLP_S5#_3R
5VS	5.0V switched power rail by SLP_S3#_3R
3VS	3.3V switched power rail by SLP_S3#_3R
Vcore_CPU	Core Voltage for CPU
VCCP	1.05V for AGTL+ Termination Voltage
+V1.8_CPU	1.8V for CPU PLL Voltage
+V0.9_DDR	0.9V DDR Termination Voltage
+V1.5S	1.5V switched power rail
+V1.5	1.5V power rail
+V1.5A	1.5V always on power rail
+V2.5S	2.5V power rail for SATA

Part Naming Conventions

C	=	Capacitor
CN	=	Connector
D	=	Diode
F	=	Fuse
L	=	Inductor
Q	=	Transistor
R	=	Resistor
RS	=	Resistor Pack
U	=	Arbitrary Logic Device
Y	=	Crystal and Osc

Net Name Suffix

0	=	Active Low signal

Signal Conditioning

_D_	=	Damped (by a resistor)
_Q_	=	Isolated (by a Q-switch)
_L_	=	Filtered (by an inductor or bead)

3.Board Stack up Description

PCB Layers — **PCB Thickness :1.2mm+/-0.1 mm .**

Layer 1		Component Side, Microstrip signal Layer
Layer 2		Power Plane
Layer 3		Stripline Layer(AGTL,CLOCK,DDR)
Layer 4		Stripline Layer(Analog,LVDS,other)
Layer 5		Ground Plane
Layer 6		Solder Side,Microstrip signal Layer

Table 1-3. Six-Bit Voltage Identification (VID) Codes

VID[5:0]	Voltage (V)	VID[5:0]	Voltage (V)	VID[5:0]	Voltage (V)	VID[5:0]	Voltage (V)
000000	1.5500	010000	1.1500	100000	0.7625	110000	0.5625
000001	1.5250	010001	1.1250	100001	0.7500	110001	0.5500
000010	1.5000	010010	1.1000	100010	0.7375	110010	0.5375
000011	1.4750	010011	1.075	100011	0.7250	110011	0.5250
000100	1.4500	010100	1.050	100100	0.7125	110100	0.5125
000101	1.4250	010101	1.025	100101	0.7000	110101	0.5000
000110	1.4000	010110	1.000	100110	0.6875	110110	0.4875
000111	1.3750	010111	0.975	100111	0.6750	110111	0.4750
001000	1.3500	011000	0.950	101000	0.6625	111000	0.4625
001001	1.3250	011001	0.925	101001	0.6500	111001	0.4500
001010	1.3000	011010	0.900	101010	0.6375	111010	0.4375
001011	1.2750	011011	0.875	101011	0.6250	111011	0.4250
001100	1.2500	011100	0.850	101100	0.6125	111100	0.4125
001101	1.2250	011101	0.825	101101	0.6000	111101	0.4000
001110	1.2000	011110	0.800	101110	0.5875	111110	0.3875
001111	1.1750	011111	0.775	101111	0.5750	111111	0.3750

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6.Schematic modify Item and History :

Version 0.1 change to 0.2 change list.

1.D6 from BAT54C-7 change to PNP DTA144EUA 50V 30mA SC70
2.C493 Change BOM to NU
3.BOM Change EEPROM FROM SST25VF080B TO W25X80VSSIG
4.CN5 K/B Connect FROM 25PIN CHANGE TO 24PIN
5.C312 BOM Change TO 1000pF
6.HDD FROM PATA CHANGE TO SATA
7.R471 BOM Cange To NU
8.R268 R269 R 270 R271 R272 From 220Ohm CHANGE To 100Ohm BOM Change
9.Schematic Change R268 R269 Connect To 3VLA
10.Q28 DEL By BOM Change
11.C481 From 1uF Change To 10uF BOM Change
12.R135 From Pulldown Change To pullhigh
13.Add LED for Wireless-LAN
14.2.5VS UP to 2.6VS
15.1.5VS UP to 1.6VS
16.Jmp wire from C513 to Q45 567Pin.
17.X1 and X3 Pin 1,4 and 2,3 change.
18.Jmp wire from C513 to Q45 567Pin.
19.R542 and R543 BOM Change to 2.2K
20.R540 and R541 BOM Change to 0Ohm
21.A20GET U31,W3 Pin connect to U18,126 Pin
22.KBRC U31,V1 Pin connect to U18,16Pin
23.R183, R221 BOM Change to 47K
24.C266, C311 Change to 4.7uF 25V 1206
25.R149 Change to 51K BOM Change.
26.R547 Change to 2.1K BOM Change.
27.C479 DEL
28.C436 BOM change NU
29.C425,C429,C433 BOM change to 22p For VESA
30.R264 R266 BOM change to 15K.
31.R547 BOM change to 2.1K.
32.L47,L48,L49 BOM change to 17 ohm + - 25% 100MHZ 0.1 ohm 600mA (0805).
33.SPEC.change PATA to SATA
34.Battery schematic change.

Version 0.2 change to 0.3 change list.

35.Function change EC-ON-power issue.3VLA plan Delete.
36.Function change CPU THERMTRIP# ON/OFF POWER for 5VLA.
37.SATA-Pull -Power 2.5V modify.
38.POWER ON sequence For Battery only time Change.
39.SATA-Connect change to DIP.
40.PCB From 1.4mm change to 1.2mm
41.Add HDD Led Pull High.
42.Power Del mOhm resistance.(All Power Plan)
43.BOM change. Del C91 & C92 For some Memory issue.
44.W-lan change to green LED.
45.Modify SATA-IDE clock 25Mhz.

Version 0.3 change to AX1 change list.(SI buid)

46.ADD EMI Solution on SPEAKER Side 150pF.
47.ADD USB Solution on SB8237A PLLPower.
48.Modify EC Power ON solution. Add R624
49.Modify SATA LED add pull HIGH.
50.Modify USB test R531 from 6.4K change to 5.11K.

(SI buid) Change List

51.Modify BOM for Mini-PCIE connect too High over botton cover.

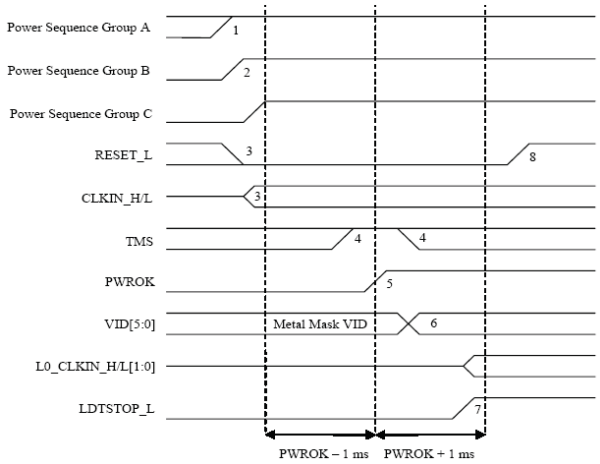
Version AX1 change to A01 change list.(PV buid)

52.Add Function For Modem RING#.(L38 Power plan change to 3VA)
53.Modify BOM for DC-IN connect .(ME)
54.Modify BOM for C596,C597,C598,C599 from 5pF to 0.1uF (EMI)
55.Add BOM for L68 (EMI)
56.change BOM for AUDIO function R264 and 266 From 10k change to 20K
57.change BOM for EMI function Add R672 22ohm.
58.change BOM for EMI function Add C623~631 0.1uF
59.change BOM for USB function Issue R531 from 5.1K change to 6.04K
60.change USB power plan function Support S3 wake up.
61.change WLAN LED function Only Support ON-OFF.
62.change BOM for LCD on-off.

VDDIO=DRAM POWER 1.8V VDD=CPU core POWER by VID (first 0.9V) VLDT=CPU POWER 1.2V

VTT=DRAM Vref POWER 0.9V

VDDA=CPU POWER 2.5V



A01 change A02 BOM change list.(PV buid to MP BOM cheng List)

63. 將Vcore Voltage 調高每增加1A Vcore voltage 下降 0.75mV原本是每增加1A Vcore voltage 下降 1.5mV.
Modify R611,R612,R613,R614-----60130B1020ZT(1K---0402)
change to 6013A0018401---2k 1% ---0402

64. USB eye-pattern 調大 From R531 6.04K 1% 0603 (6013A0068501) change to 5.62K 1% 0603 (60130B56219T)
65. Change BOM L66,L62,L23 to R630,R631,R632 from (60140EA0063T) to 0 OHM 5% (60130B00000Z) and (60130BA0003T)
66. SATA eye-pattern 調大 From R559 6.19K 1% 0603 (6013A0068501) change to 5.62K 1% 0603 (60130B56219T)
67. RTC C515,C511 change to (6010078R220Y) CAPACITOR-CHIP,8.2PF,50V,D,NP0,0603,TR
68. R446 NU
69. EMI issue Change C323,C535,C320,C327,C321 From 12pF change to 22pF 50V 5% 0603 NPO (60100722020Z)
70. For North bridge Thermal issue ADD R486 4.7K 5% 1/16W 0402(60130B4720ZT)
71. North bridge Vref. V-LINK Change R592 From 1K 5%(60130B1020ZT) to 1K 1%(60130B10019Z)
72. Change South bridge Voltage to 2.5V R547 from 2.1K 1% 1/10W 0603 change to 2.2K 1%(60130B22019T)

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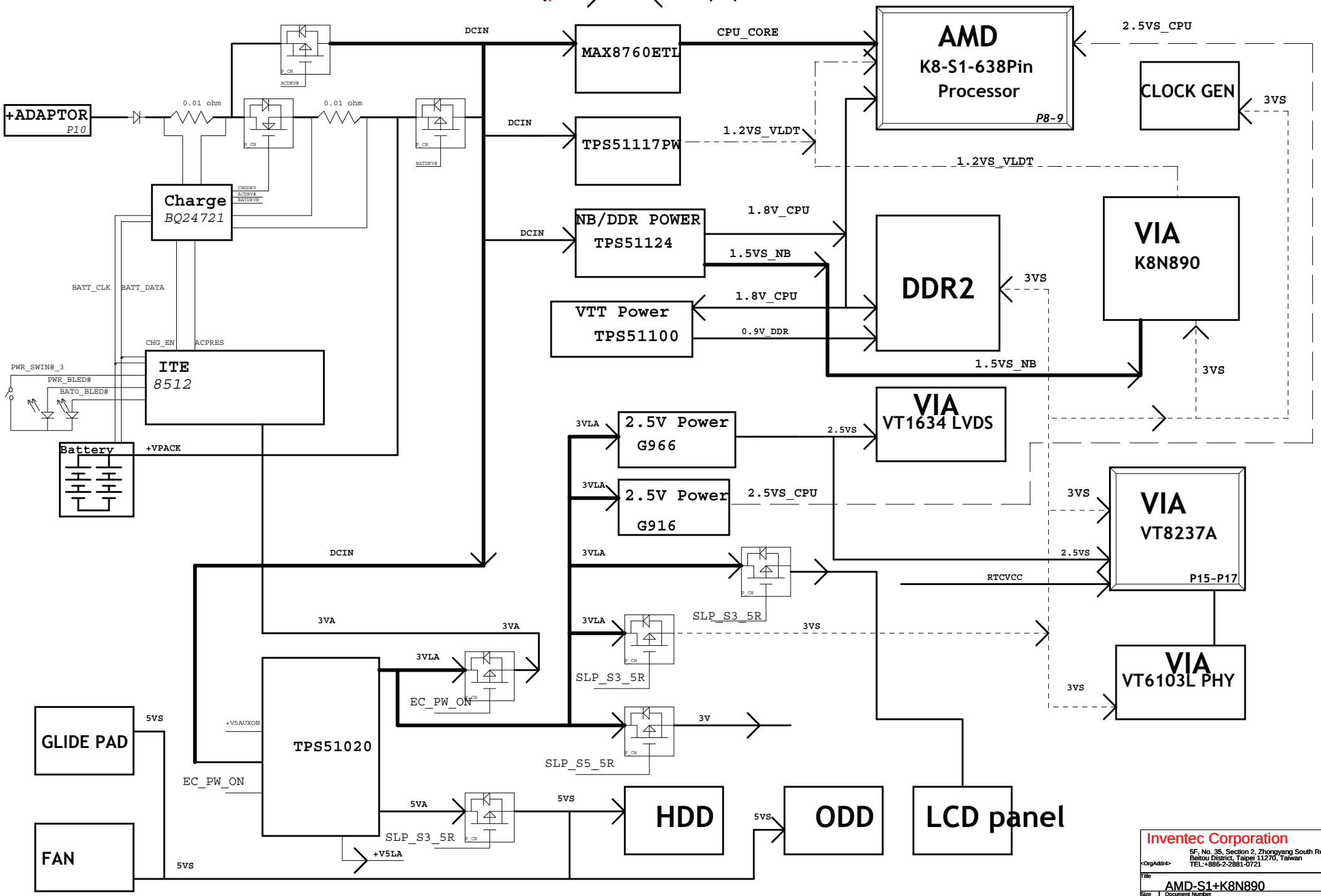

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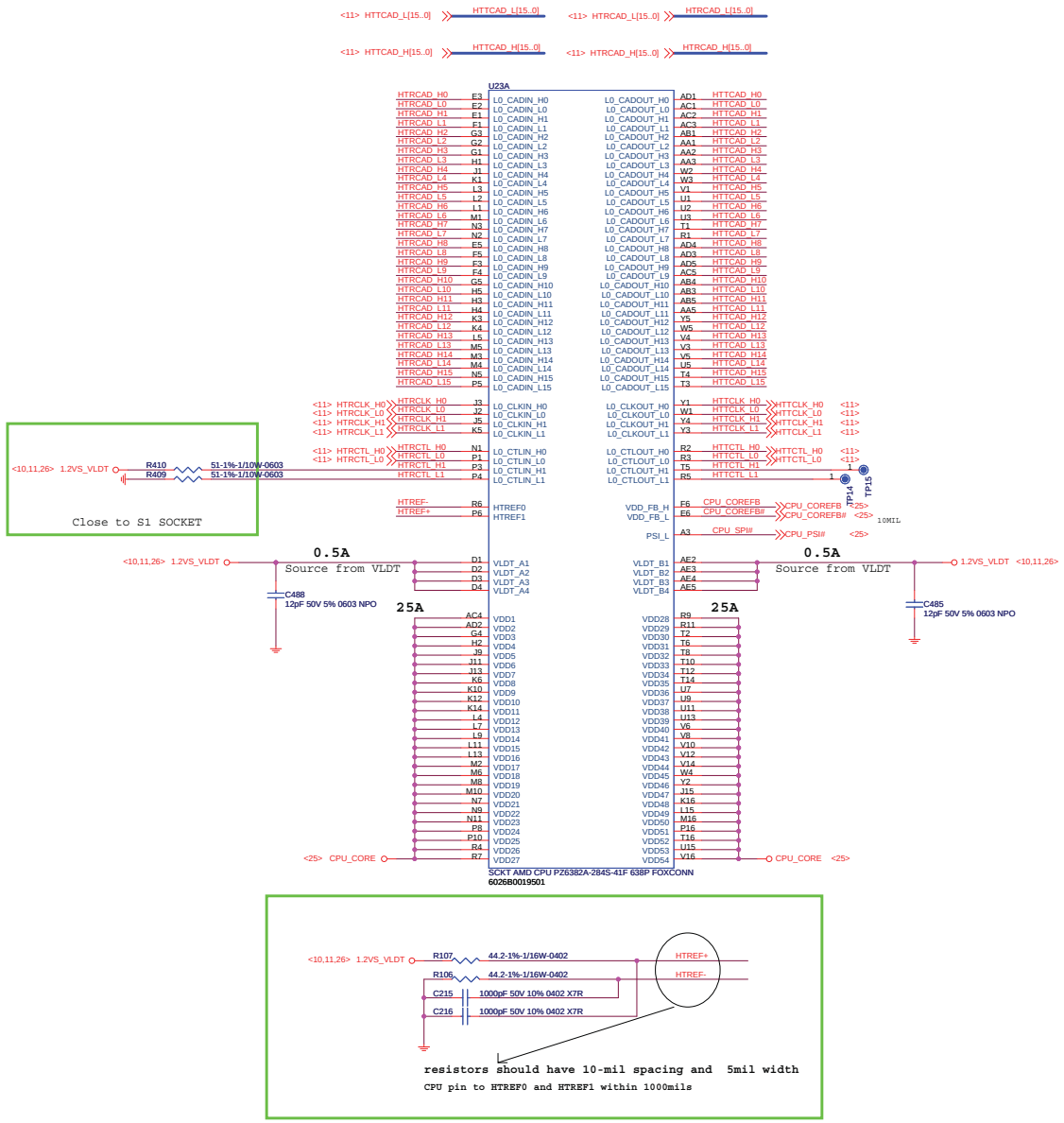
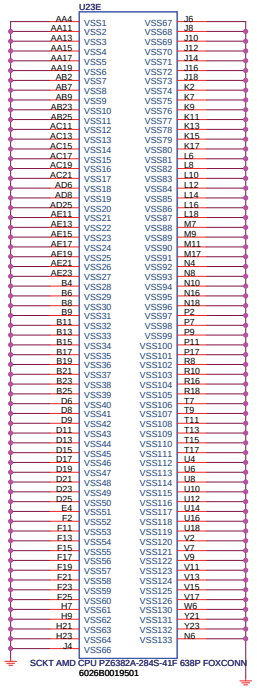
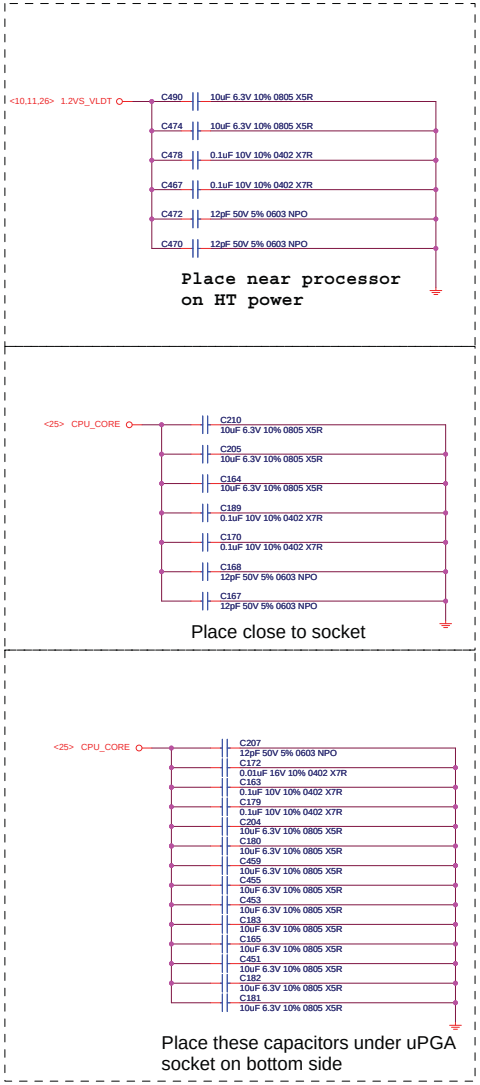
ClawHammer HT Interface

LAYOUT: Place HT bypass caps on topside near unconnected Clawhammer HT Link







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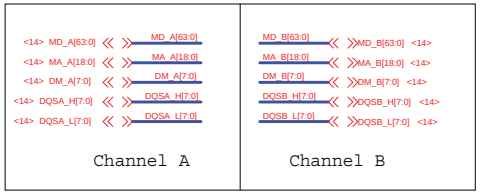

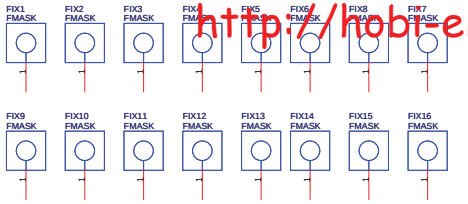

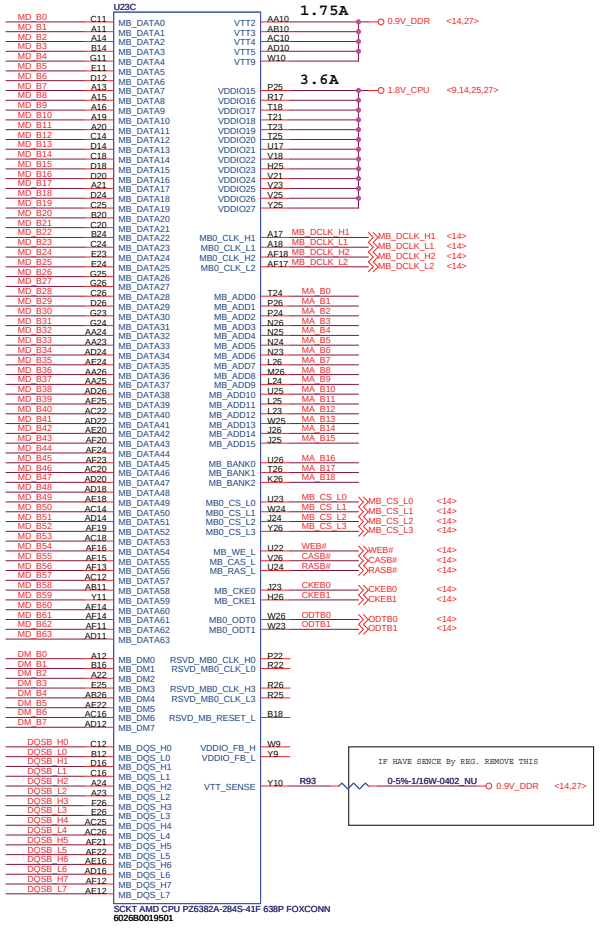

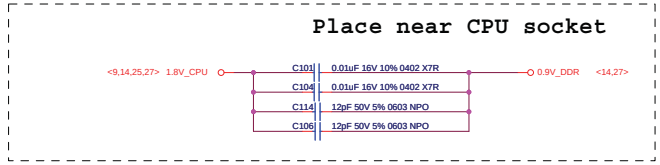

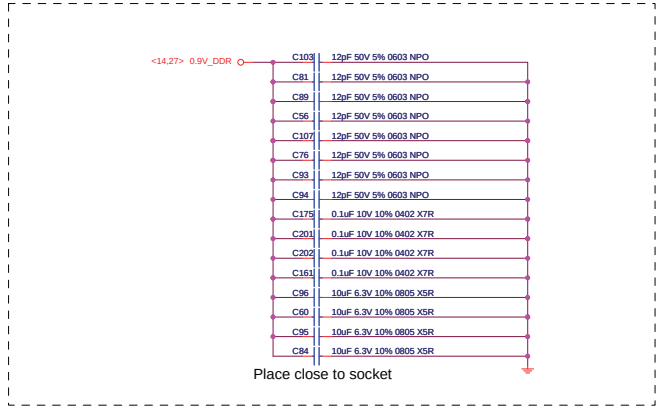

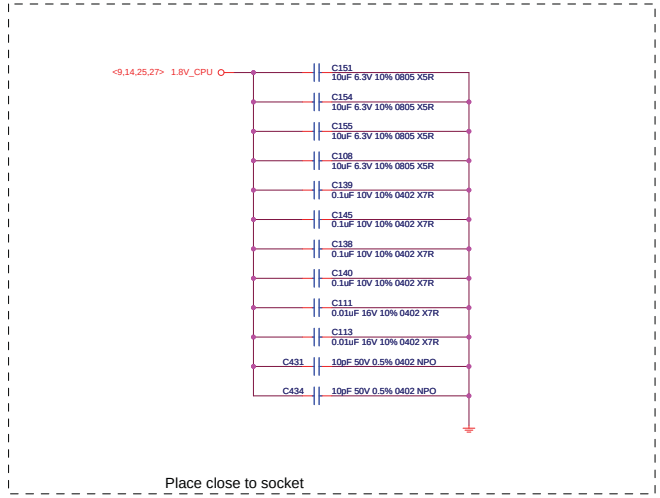

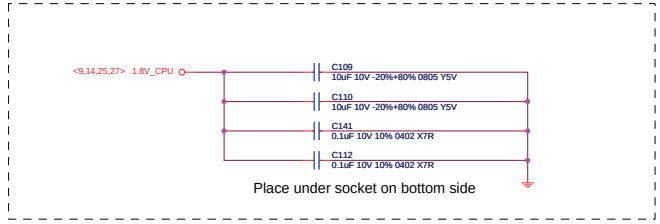

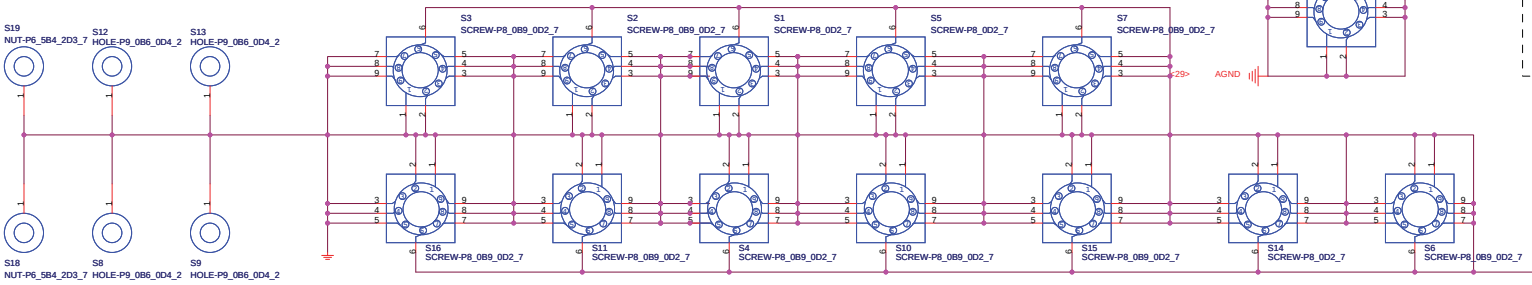

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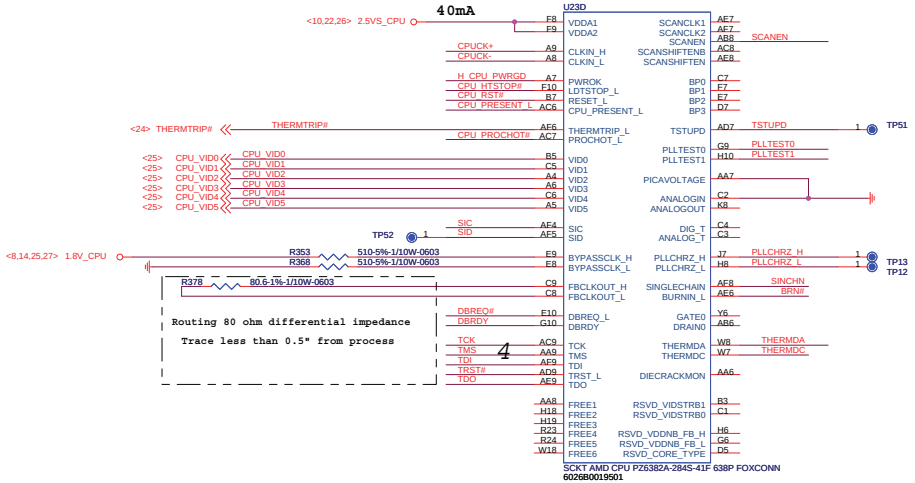
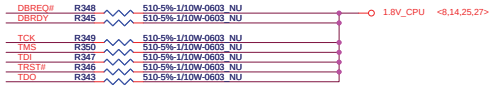
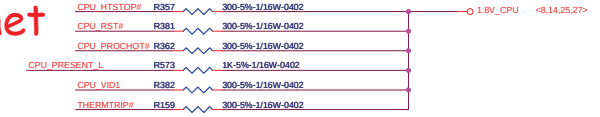
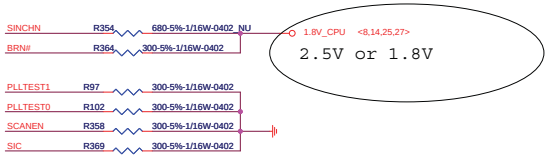
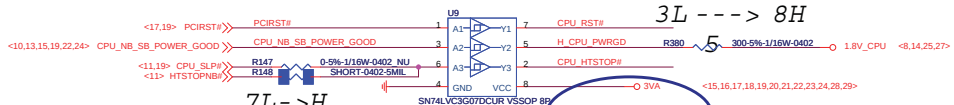






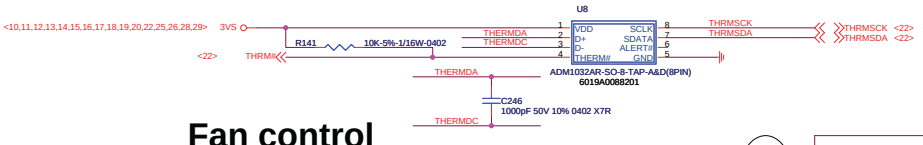


CPU POWER GOOD

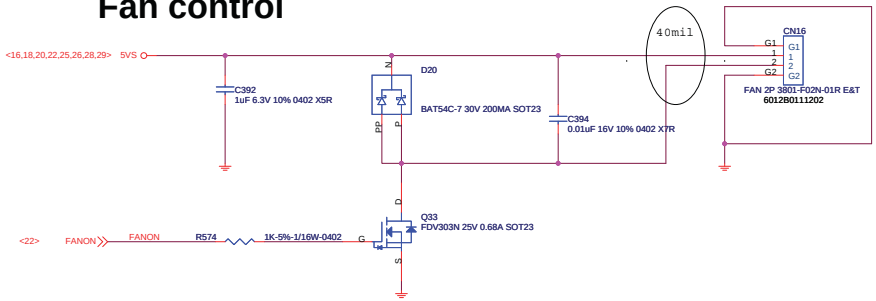


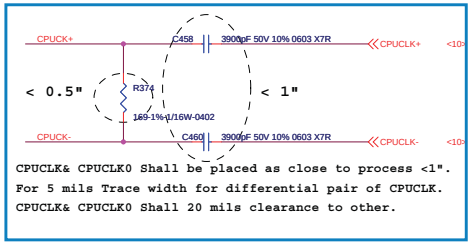
EC FUNCTION

THERMAL SENSOR



Fan control





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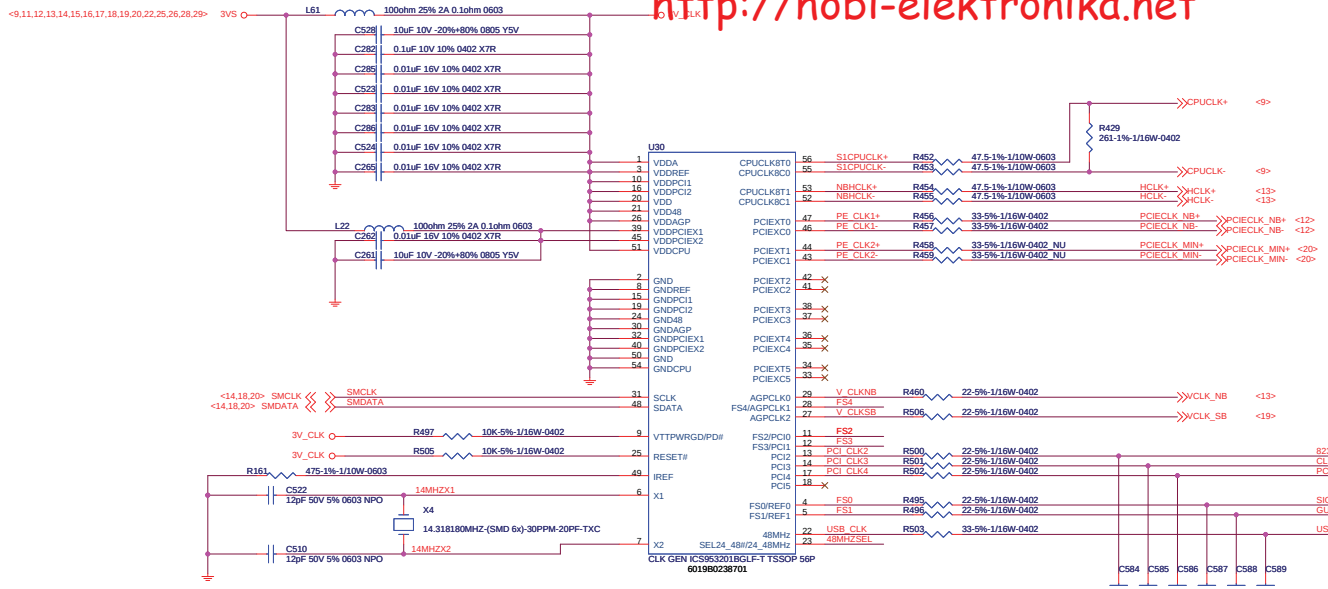
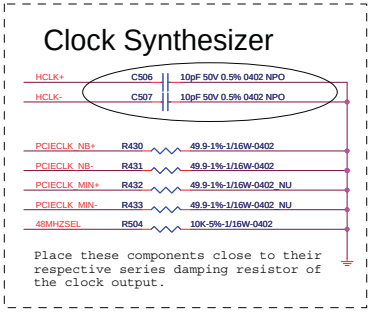
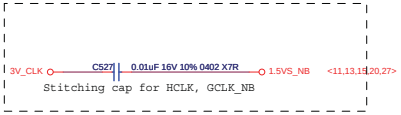
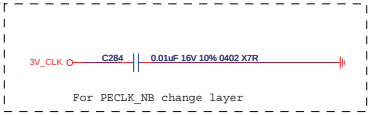


Clock Synthesizer

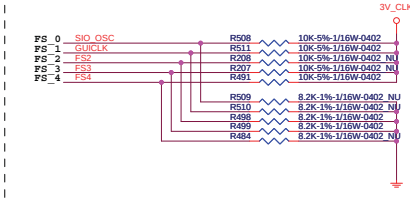




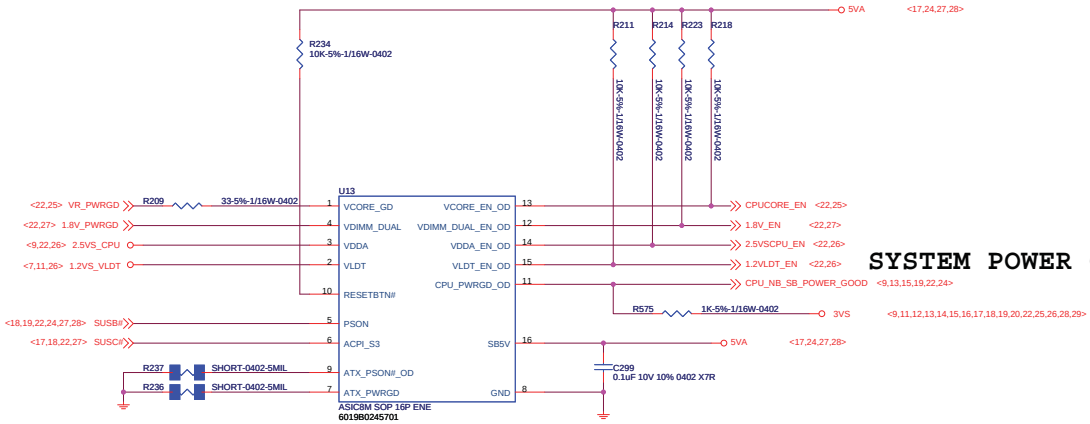


FS_[4:0]	CPU	PCIEX	AGP	PCI
00000	100.90	100.90	67.27	33.63
00001	133.90	100.43	66.95	33.48
00010	168.00	100.80	67.20	33.60
00011	202.00	101.00	67.33	33.67
00100	100.20	100.20	66.80	33.40
00101	133.50	100.13	66.75	33.38
00110	166.70	100.02	66.68	33.34
00111	200.40	100.20	66.80	33.40
01000	160.00	100.00	66.67	33.33
01001	202.00	101.00	67.33	33.67
01010	210.00	105.00	70.00	35.00
01011	212.00	106.00	70.67	35.33
01100	270.00	101.25	67.50	33.75
01101	225.00	112.50	75.00	37.50
01110	266.67	100.00	66.67	33.33
01111	300.00	112.50	75.00	37.50

FS_[4:0]	CPU	PCIEX	AGP	PCI
10000	100.00	100.00	66.67	33.33
10001	133.00	100.00	66.67	33.33
10010	166.66	104.16	69.44	34.72
10011	**200.00**	**100.00**	**66.67**	**33.33**
10100	103.00	103.00	68.67	34.33
10101	137.33	103.00	68.66	34.33
10110	171.66	103.00	68.66	34.33
10111	206.00	103.00	68.67	34.33
11000	208.00	104.00	69.33	34.67
11001	210.00	105.00	70.00	35.00
11010	215.00	107.50	71.67	35.83
11011	220.00	110.00	73.33	36.67
11100	226.00	113.00	75.33	37.67
11101	230.00	115.00	76.67	38.33
11110	240.00	120.00	80.00	40.00
11111	250.00	125.00	83.33	41.67



CPU POWER ON CONTROL



SYSTEM POWER GOOD

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Title: AMD-S1+K8N890

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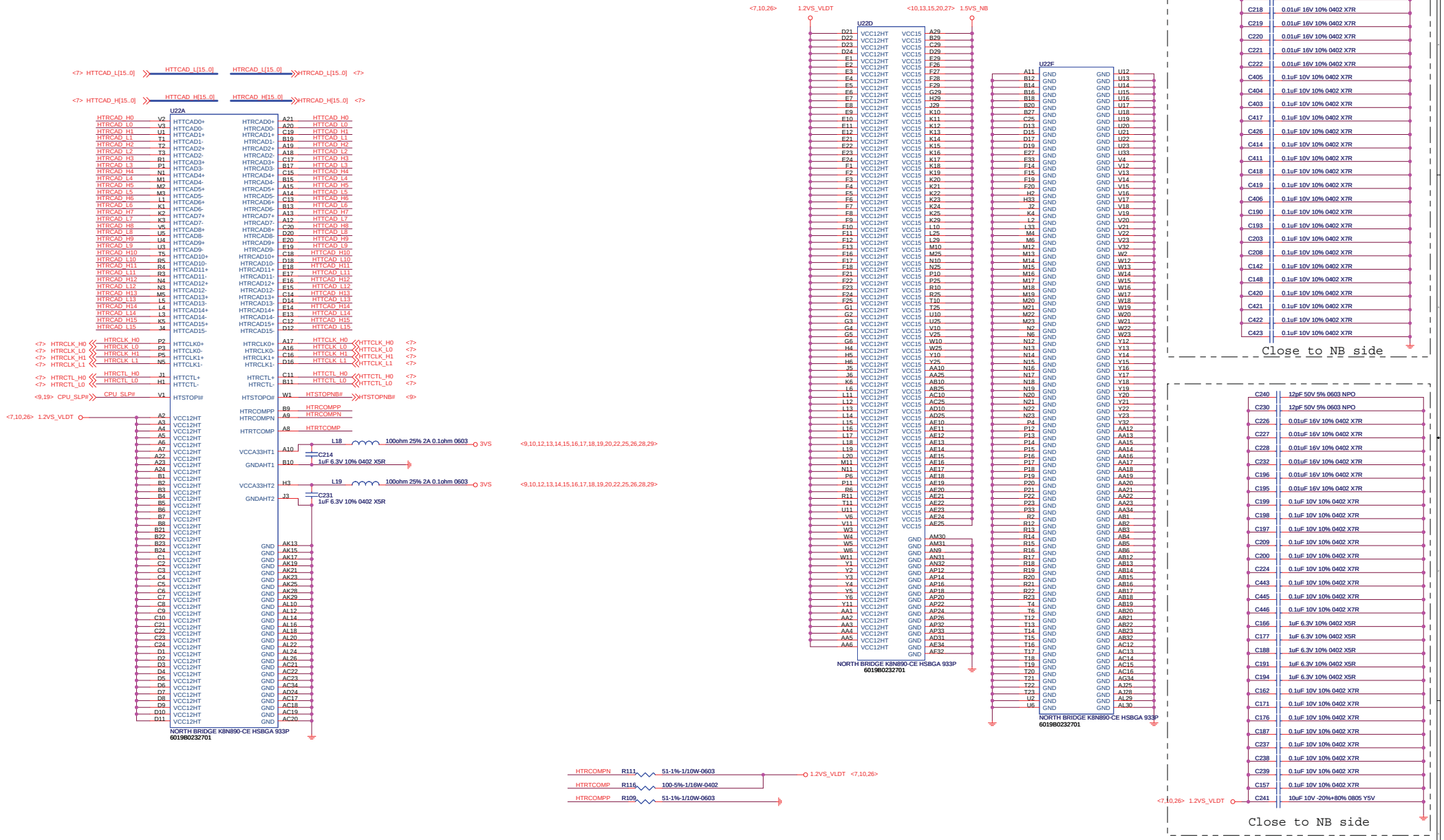

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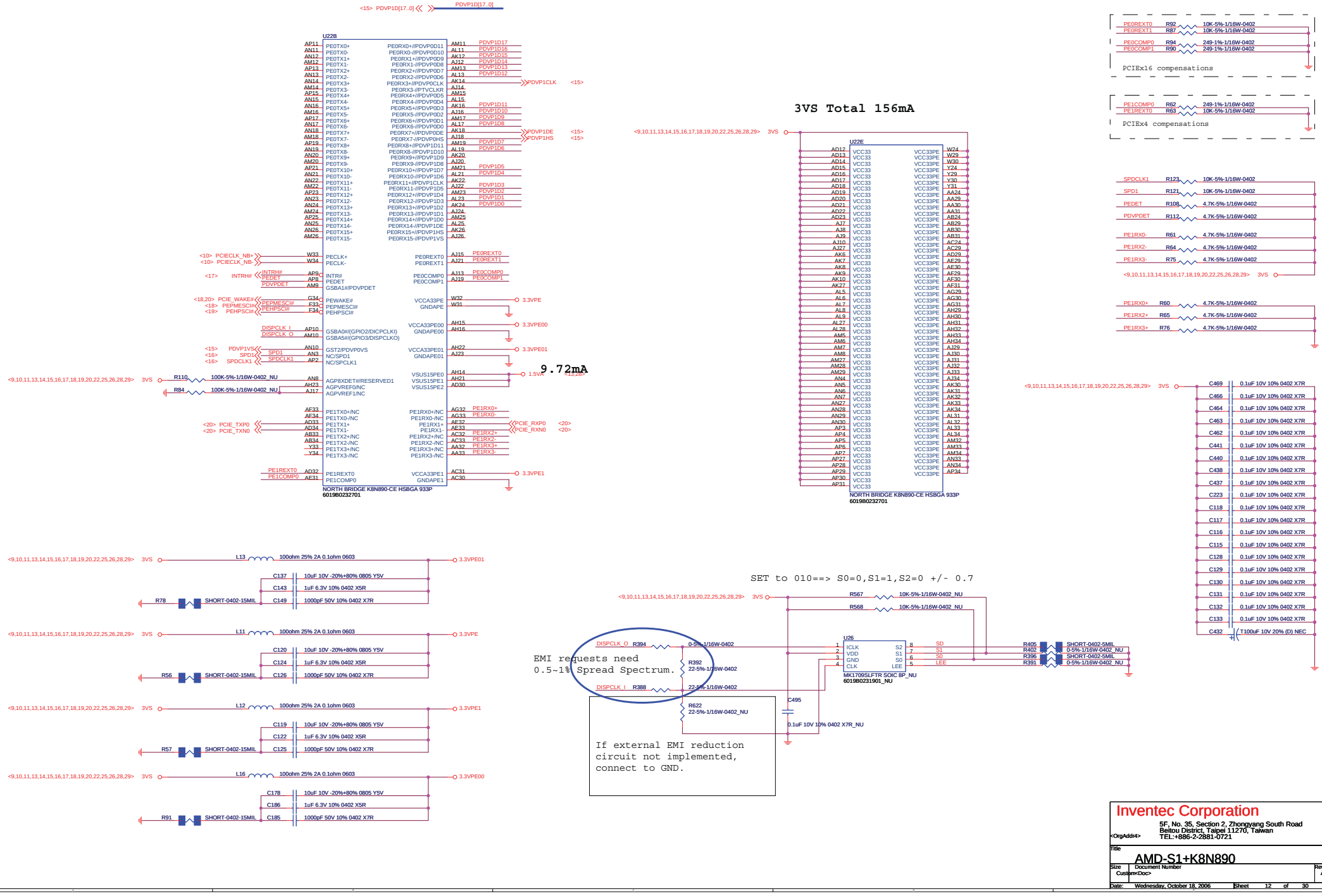
Note:
K8M890CE support 1 X1 Lane PCI Express
K8T900 support 4 X1 Lane or 1 X4 Lane PCI Express.



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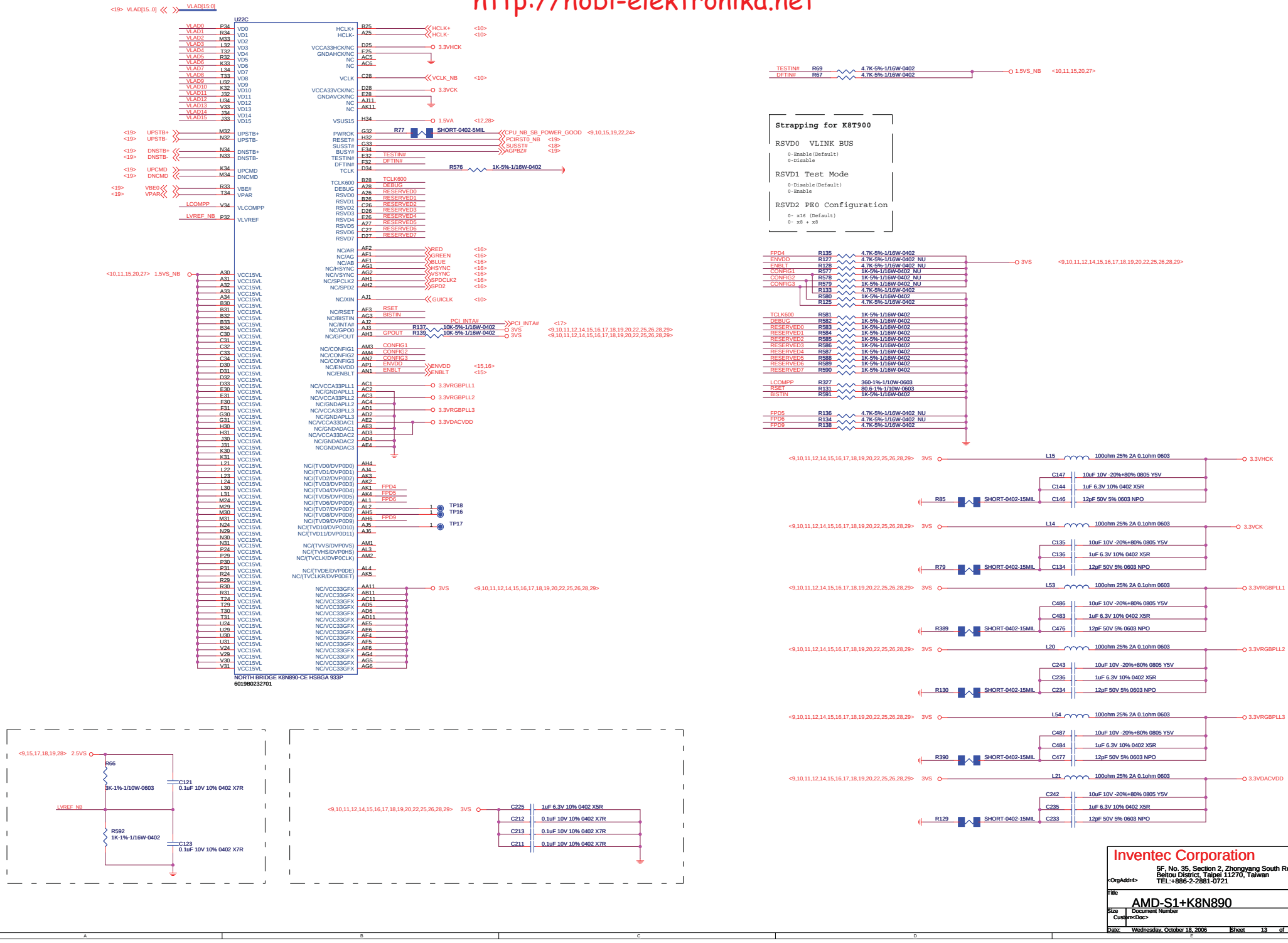

SO-DIMM0

CPUside

MA_DCLK_H1	C158	1.5pF 16V +-0.1pF 0402 C0H	MA_DCLK_L1
MA_DCLK_H2	C160	1.5pF 16V +-0.1pF 0402 C0H	MA_DCLK_L2
MA_DCLK_H1	C614	1.5pF 16V +-0.1pF 0402 C0H_NU	MA_DCLK_L1
MA_DCLK_H2	C616	1.5pF 16V +-0.1pF 0402 C0H_NU	MA_DCLK_L2

MEMORYside

Channel A

MD_A[63:0], MA_A[18:0], DM_A[7:0], DQSA_H[7:0], DQSA_L[7:0]

CN15

MA_A0 MA_A1 MA_A2 MA_A3 MA_A4 MA_A5 MA_A6 MA_A7 MA_A8 MA_A9 MA_A10 MA_A11 MA_A12 MA_A13 MA_A14 MA_A15 MA_A18 MA_A17 MA_A16

MA_CS_L0 MA_CS_L1 MA_DCLK_H1 MA_DCLK_L1 MA_DCLK_H2 MA_DCLK_L2 CKEA0 CKEA1 CASA# RASA# WEA#

SMCLK SMDATA

ODTA0 ODTA1

DM_A0 DM_A1 DM_A2 DM_A3 DM_A4 DM_A5 DM_A6 DM_A7

DQSA_H0 DQSA_H1 DQSA_H2 DQSA_H3 DQSA_H4 DQSA_H5 DQSA_H6 DQSA_H7 DQSA_L0 DQSA_L1 DQSA_L2 DQSA_L3 DQSA_L4 DQSA_L5 DQSA_L6 DQSA_L7

MD_A[0..63]

<8,9,25,27> 1.8V_CPU

<9,10,11,12,13,15,16,17,18,19,20,22,25,26,28,29> 3VS

MA_CS_L2 MA_CS_L3

<8,27> M_VREF

C57 0.1uF 10V 10% 0402 X7R

DDR2 DIMM 200P AS0A421-N2RN-7F 5.2mm REV FOXCONN
6026B0022001

SO-DIMM1

CPUside

MB_DCLK_H1	C153	1.5pF 16V +-0.1pF 0402 C0H	MB_DCLK_L1
MB_DCLK_H2	C150	1.5pF 16V +-0.1pF 0402 C0H	MB_DCLK_L2
MB_DCLK_H1	C615	1.5pF 16V +-0.1pF 0402 C0H_NU	MB_DCLK_L1
MB_DCLK_H2	C617	1.5pF 16V +-0.1pF 0402 C0H_NU	MB_DCLK_L2

MEMORYside

Channel B

MD_B[63:0], MA_B[18:0], DM_B[7:0], DQSB_H[7:0], DQSB_L[7:0]

CN14

MA_B0 MA_B1 MA_B2 MA_B3 MA_B4 MA_B5 MA_B6 MA_B8 MA_B9 MA_B10 MA_B11 MA_B12 MA_B13 MA_B14 MA_B15 MA_B18 MA_B17 MA_B16

MB_CS_L0 MB_CS_L1 MB_DCLK_H1 MB_DCLK_L1 MB_DCLK_H2 MB_DCLK_L2 CKEB0 CKEB1 CASB# RASB# WEB#

R13 10K-5%-1/16W-0402

SMCLK SMDATA

ODTB0 ODTB1

DM_B0 DM_B1 DM_B2 DM_B3 DM_B4 DM_B5 DM_B6 DM_B7

DQSB_H0 DQSB_H1 DQSB_H2 DQSB_H3 DQSB_H4 DQSB_H5 DQSB_H6 DQSB_H7 DQSB_L0 DQSB_L1 DQSB_L2 DQSB_L3 DQSB_L4 DQSB_L5 DQSB_L6 DQSB_L7

MD_B[0..63]

<8,9,25,27> 1.8V_CPU

<9,10,11,12,13,15,16,17,18,19,20,22,25,26,28,29> 3VS

MB_CS_L2 MB_CS_L3

<8,27> M_VREF

C27 0.1uF 10V 10% 0402 X7R

DDR2 DIMM 200P AS0A426-NARN-7F 9.2mm REV FOXCONN
6026B0051101

Place one cap close to every 2 pullup resistors terminated to 0.9VDDT_DDRII

<8,27> 0.9V_DDR

SO-DIMM0

400 mils

MA_A8	RS14	R-AR-8P4R-47-5%-1/16W-2010	C62 0.1uF 10V 10% 0402 X7R
MA_A5			
MA_A1			C58 0.1uF 10V 10% 0402 X7R
MA_A3			
MA_A0	RS13	R-AR-8P4R-47-5%-1/16W-2010	
MA_A17			C54 0.1uF 10V 10% 0402 X7R
MA_A10			
MA_A16			C61 0.1uF 10V 10% 0402 X7R
MA_A4	RS8	R-AR-8P4R-47-5%-1/16W-2010	
MA_A7			C64 0.1uF 10V 10% 0402 X7R
MA_A11			
MA_A14			C53 0.1uF 10V 10% 0402 X7R
MA_A2	RS12	R-AR-8P4R-47-5%-1/16W-2010	
MA_A6			C48 0.1uF 10V 10% 0402 X7R
MA_A15			
MA_A9			C49 0.1uF 10V 10% 0402 X7R
ODTA0	RS10	R-AR-8P4R-47-5%-1/16W-2010	
WEA#			C65 0.1uF 10V 10% 0402 X7R
CASA#			
MA_CS_L1			C52 0.1uF 10V 10% 0402 X7R
MA_A13	RS9	R-AR-8P4R-47-5%-1/16W-2010	
ODTA1			C55 0.1uF 10V 10% 0402 X7R
RASA#			
MA_CS_L0			C66 0.1uF 10V 10% 0402 X7R
CKEA1	RS11	R-AR-8P4R-47-5%-1/16W-2010	
MA_A12			C51 0.1uF 10V 10% 0402 X7R
MA_A18			
CKEA0			C50 0.1uF 10V 10% 0402 X7R
MA_CS_L2	R16	47-5%-1/10W-0603	
MA_CS_L3	R14	47-5%-1/10W-0603	C59 0.1uF 10V 10% 0402 X7R

SO-DIMM1

MA_B1	RS4	R-AR-8P4R-47-5%-1/16W-2010	
MA_B4			C24 0.1uF 10V 10% 0402 X7R
MA_B2			
MA_B3			C23 0.1uF 10V 10% 0402 X7R
MA_B9	RS6	R-AR-8P4R-47-5%-1/16W-2010	
MA_B11			C22 0.1uF 10V 10% 0402 X7R
MA_B7			
MA_B14			C21 0.1uF 10V 10% 0402 X7R
ODTB0	RS2	R-AR-8P4R-47-5%-1/16W-2010	
WEB#			C20 0.1uF 10V 10% 0402 X7R
MA_B16			
MA_B10			C19 0.1uF 10V 10% 0402 X7R
MA_B5	RS5	R-AR-8P4R-47-5%-1/16W-2010	
MA_B8			C18 0.1uF 10V 10% 0402 X7R
MA_B6			
MA_B12			C17 0.1uF 10V 10% 0402 X7R
MA_B0	RS3	R-AR-8P4R-47-5%-1/16W-2010	
MB_CS_L0			C16 0.1uF 10V 10% 0402 X7R
RASB#			
MA_B17			C15 0.1uF 10V 10% 0402 X7R
CASB#	RS1	R-AR-8P4R-47-5%-1/16W-2010	
MB_CS_L1			C14 0.1uF 10V 10% 0402 X7R
ODTB1			
MA_B13			C13 0.1uF 10V 10% 0402 X7R
MA_B15	RS7	R-AR-8P4R-47-5%-1/16W-2010	
CKEB1			C12 0.1uF 10V 10% 0402 X7R
CKEB0			
MA_B18			C11 0.1uF 10V 10% 0402 X7R
MB_CS_L2	R9	47-5%-1/10W-0603	
MB_CS_L3	R8	47-5%-1/10W-0603	C10 0.1uF 10V 10% 0402 X7R

160mil

<8,9,25,27> 1.8V_CPU

Place these 22uF caps near So-Dimm1 pin79~pin115 area

C383 C382 C381 C380 C379 C30 C31 C32 C33 C34 C35 C378 C377 — 22uF 6.3V 10% 0402 X5R

Place these 2.2uF caps near So-Dimm1

Other signal
M_VREF — 20mil — 20mil
Other signal

160mil

<8,9,25,27> 1.8V_CPU

Place these 1uF caps near So-Dimm1 pin79~pin115 area

C388 C387 C385 C391 C390 C389 C42 C43 C44 C386 C45 C46 C47 — 1uF 6.3V 10% 0402 X5R

Place these 1uF caps near So-Dimm1

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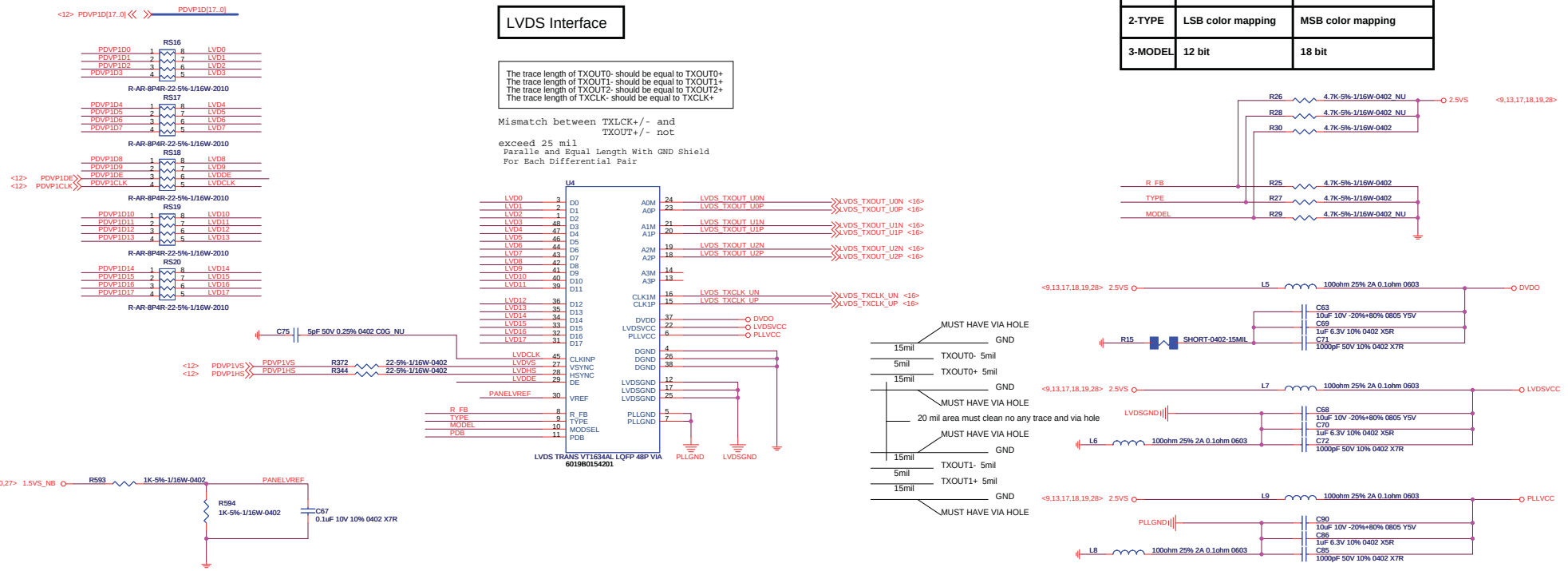
LVDS Interface

	LOW	HIGH
1-R_FB	Rising Edge	Falling Edge
2-TYPE	LSB color mapping	MSB color mapping
3-MODEL	12 bit	18 bit

The trace length of TXOUT0- should be equal to TXOUT0+
The trace length of TXOUT1- should be equal to TXOUT1+
The trace length of TXOUT2- should be equal to TXOUT2+
The trace length of TXCLK- should be equal to TXCLK+

Mismatch between TXLCK+/- and TXOUT+/- not exceed 25 mil
Faralle and Equal Length With GND Shield For Each Differential Pair

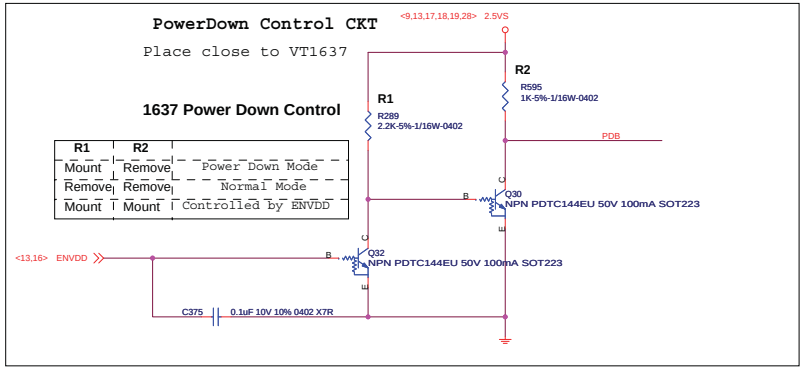


PowerDown Control CKT

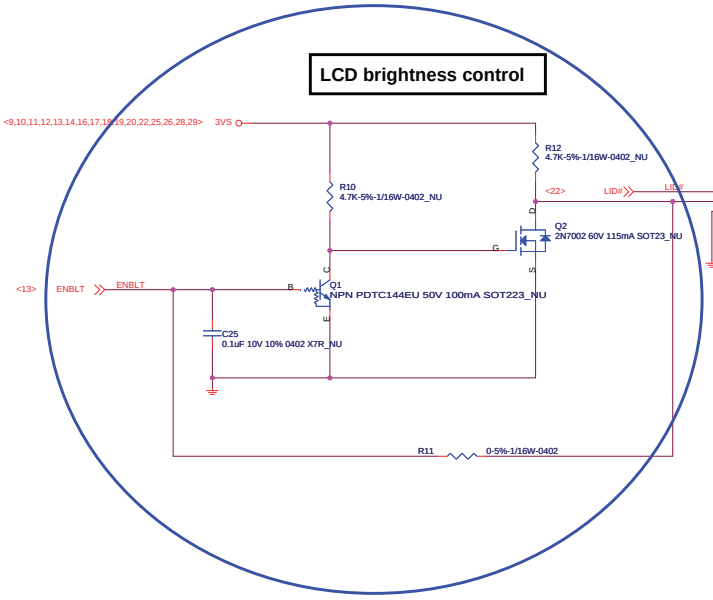
Place close to VT1637

1637 Power Down Control

R1	R2	
Mount	Remove	Power Down Mode
Remove	Remove	Normal Mode
Mount	Mount	Controlled by ENVDD



LCD brightness control



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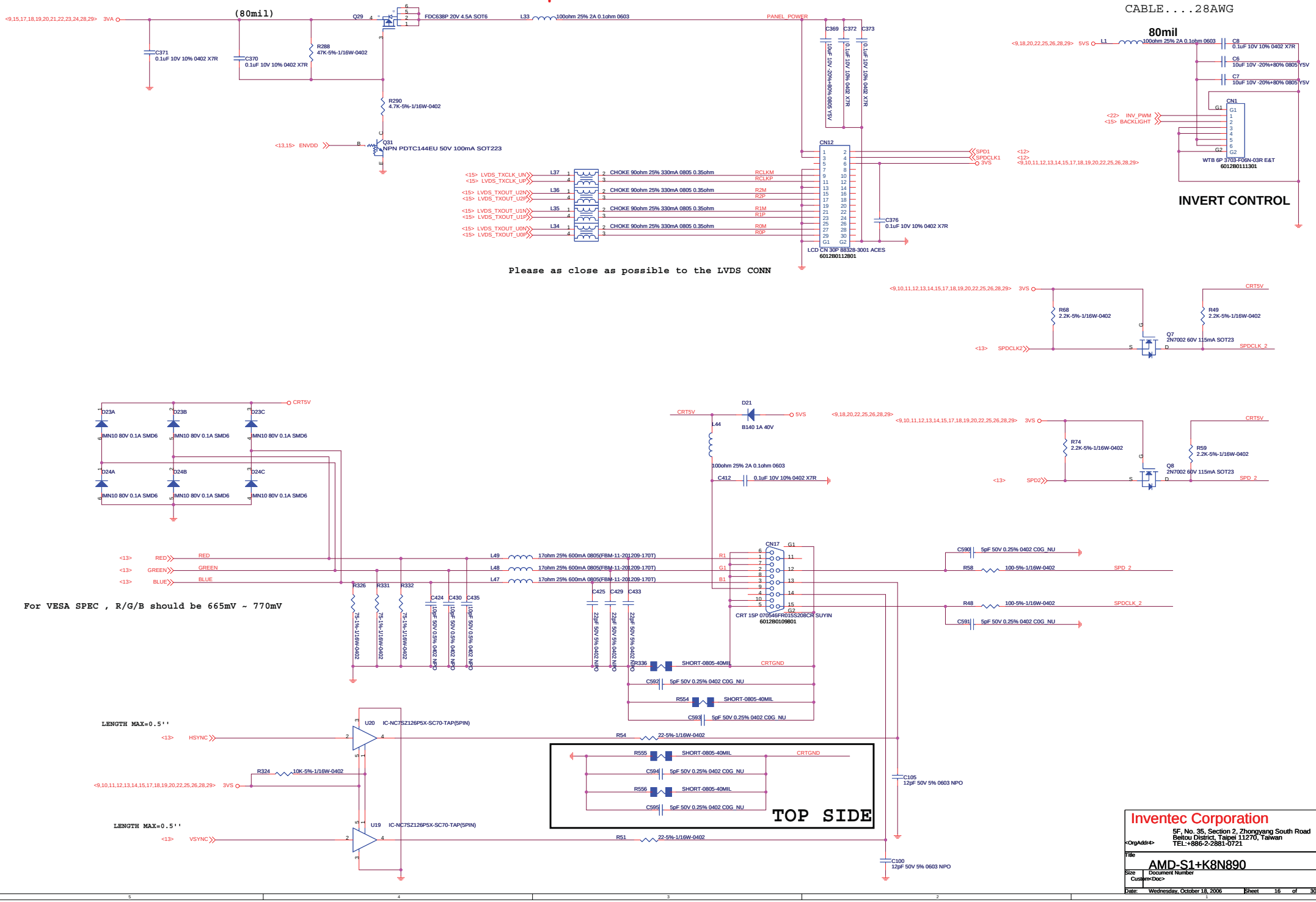
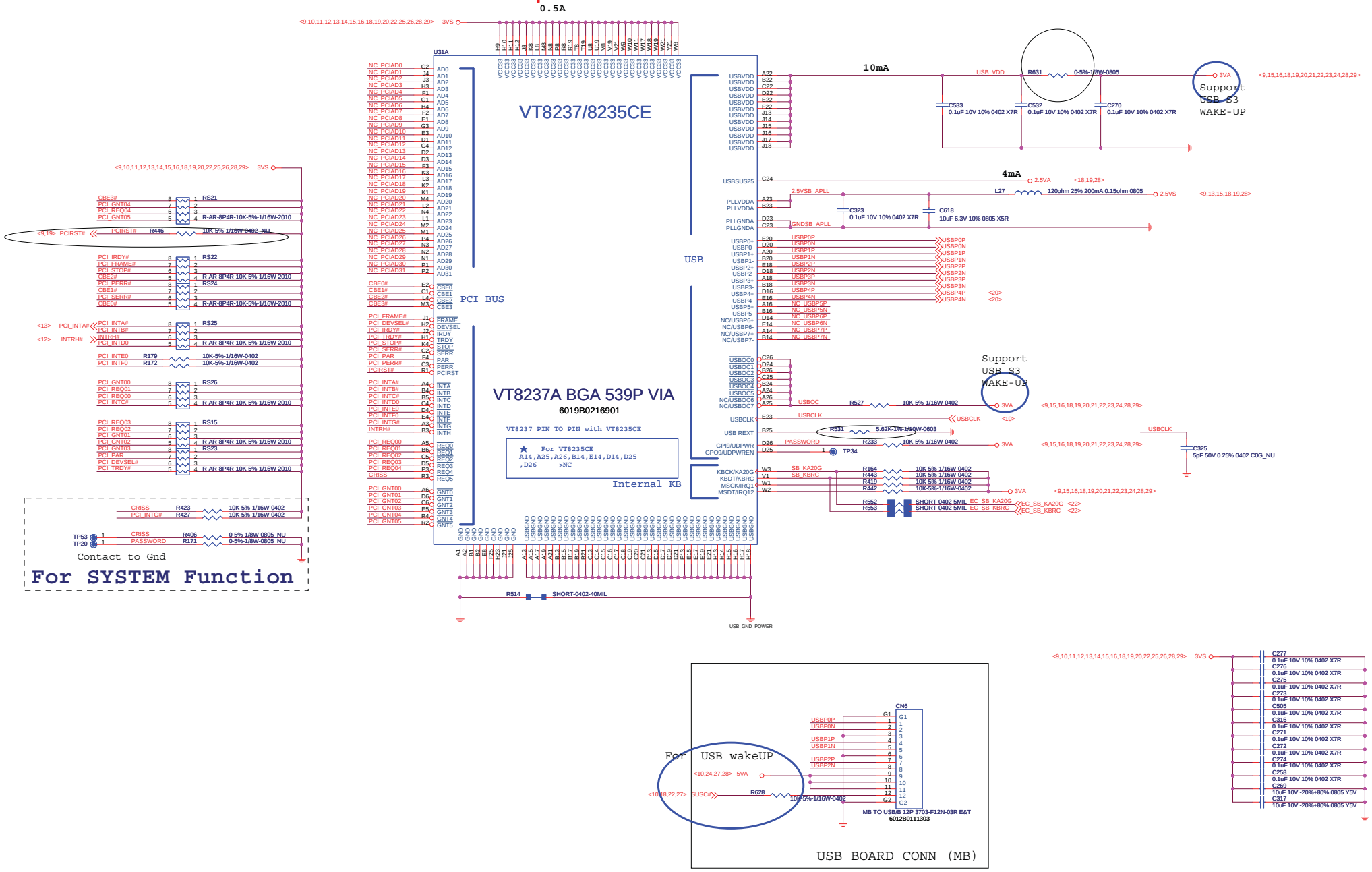
LVDS Interface





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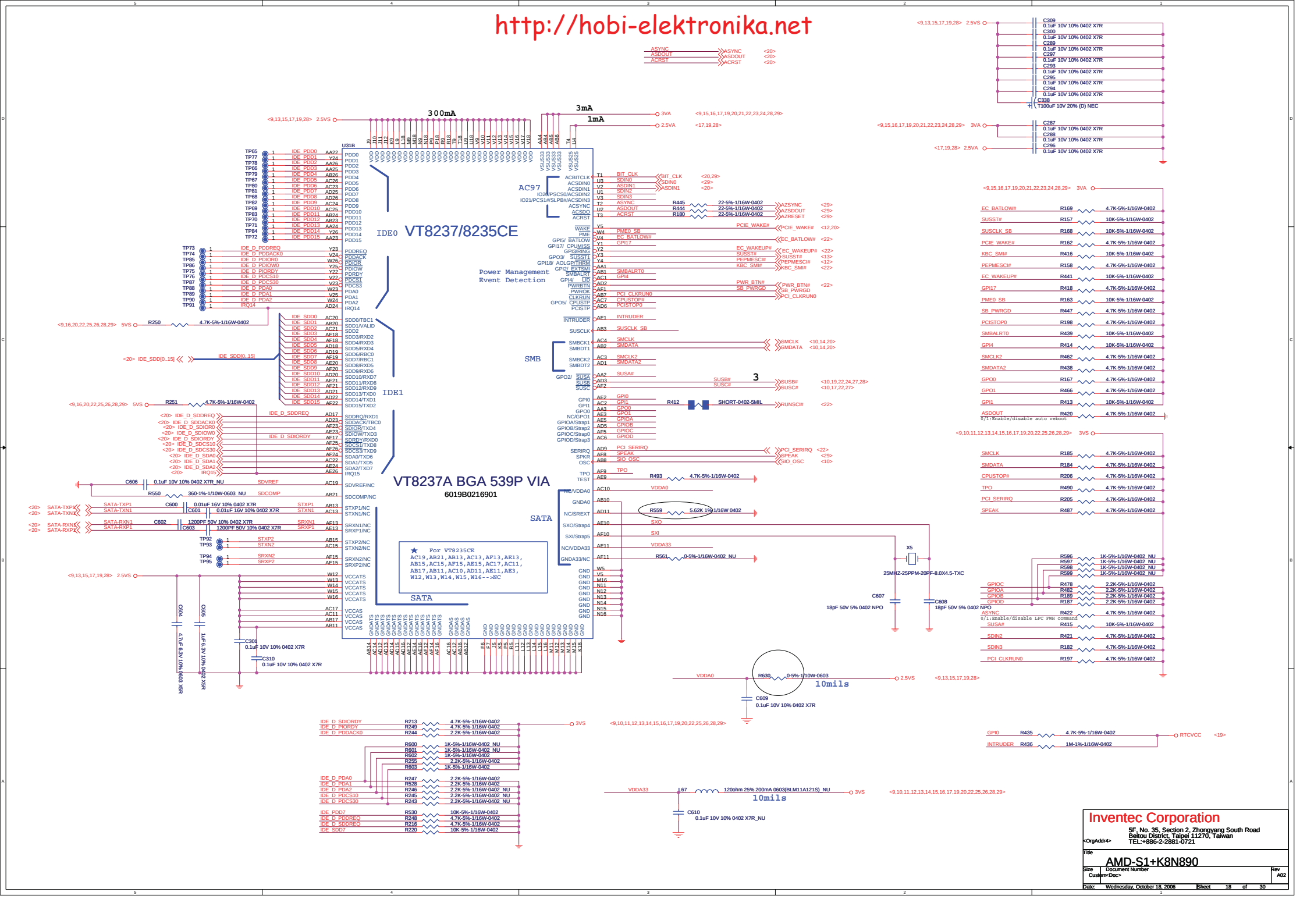

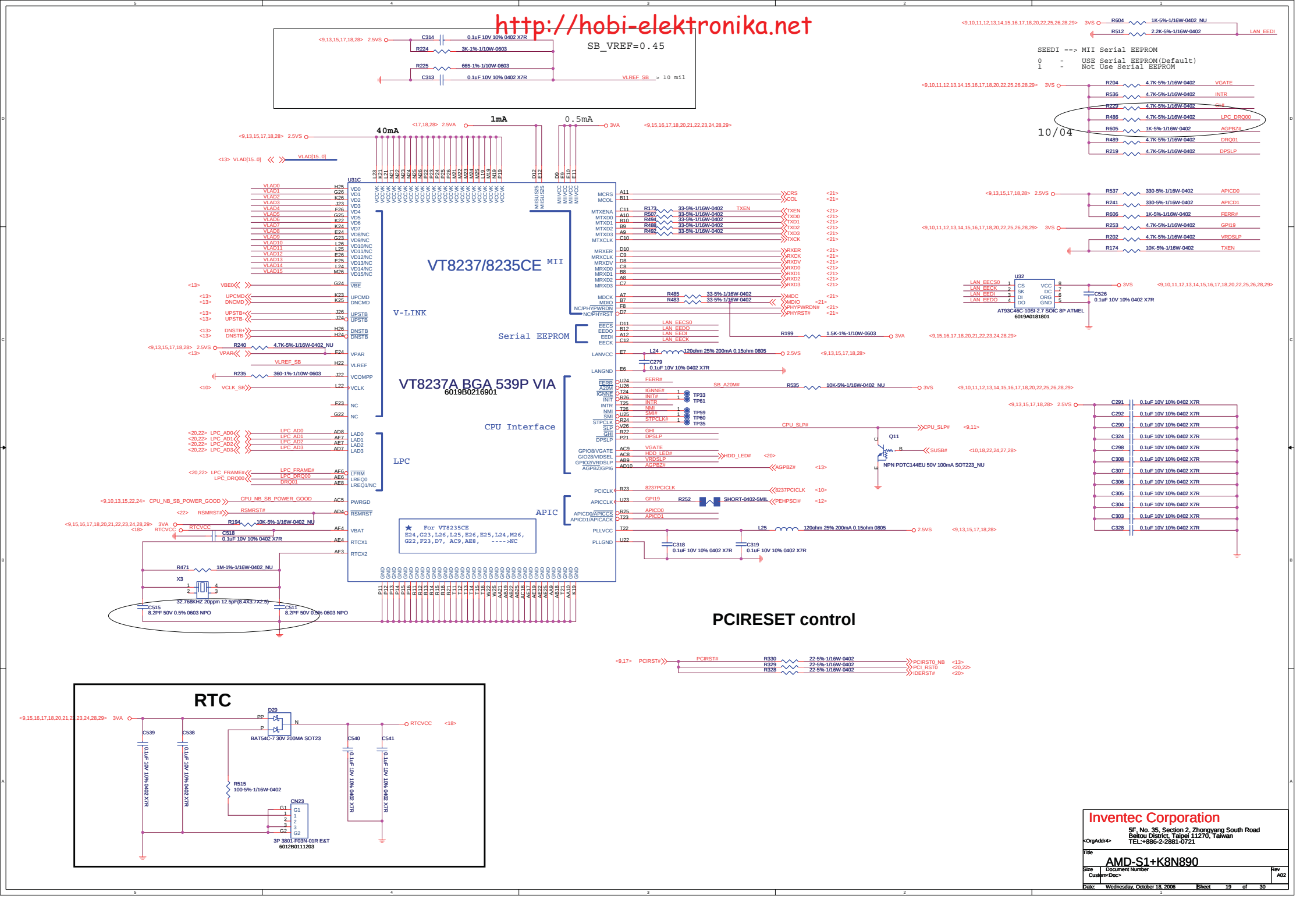

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PCIE Mini Card

Please close to mini card each pin

C521 0.1uF 10V 10% 0402 X7R
C525 0.1uF 10V 10% 0402 X7R_NU
C535 0.1uF 10V 10% 0402 X7R
C529 0.1uF 10V 10% 0402 X7R_NU
C560 0.1uF 10V 10% 0402 X7R
C558 0.1uF 10V 10% 0402 X7R_NU

CN24 KEY

MINI PCIE 52P PFPETO-ABGLBG1ZZ4N0 H=6.7mm
6026B0057401

Change BOM from 9.7mm to 6.7mm

C533 5pF 50V 0.25pF 0402 COG NU
C548 5pF 50V 0.25pF 0402 COG NU

C531 0.1uF 10V 10% 0402 X7R
C534 0.1uF 10V 10% 0402 X7R

Q54 NPN PDTC144EU 50V 100mA SOT223

For LAN LED on-off function.

D30 LED YG 17-215/G6C-FN2P2B/3T R551 100-5%-1/10W-0603

SATA-HDD I/F

R569 4.7K-5%-1/16W-0402
R570 4.7K-5%-1/16W-0402 60190H4161ST
U37 NC7SZ08M5X SOT23 5P
D12 LED YG 17-215/G6C-FN2P2B/3T R267 200-5%-1/8W-0805

CN7 DTP HDD SATA 22P 180D 12.2mm 4.4mm ALLTOP
6012B0129101

C530 1000pF 10V 20% (O)NEC
C329 0.1uF 10V 10% 0402 X7R

For E23 do not use

MDC CNN

CN13
MDC 12P 1134-F12C-03R E&T
6012B0111902

20mil L38 120ohm 25% 200mA 0.15ohm 0805
C384 0.1uF 10V 10% 0402 X7R

RJ11 By CABLE

CD-ROM CNN

CN21
ODD 50P C124M3-15001-L ALLTOP
6012B0129201

(80mil) (4VIA)
(80mil) (4VIA)

R47 100K-5%-1/16W-0402_NU
R607 1K-5%-1/16W-0402

C409 0.1uF 10V 10% 0402 X7R
C410 0.1uF 10V 10% 0402 X7R

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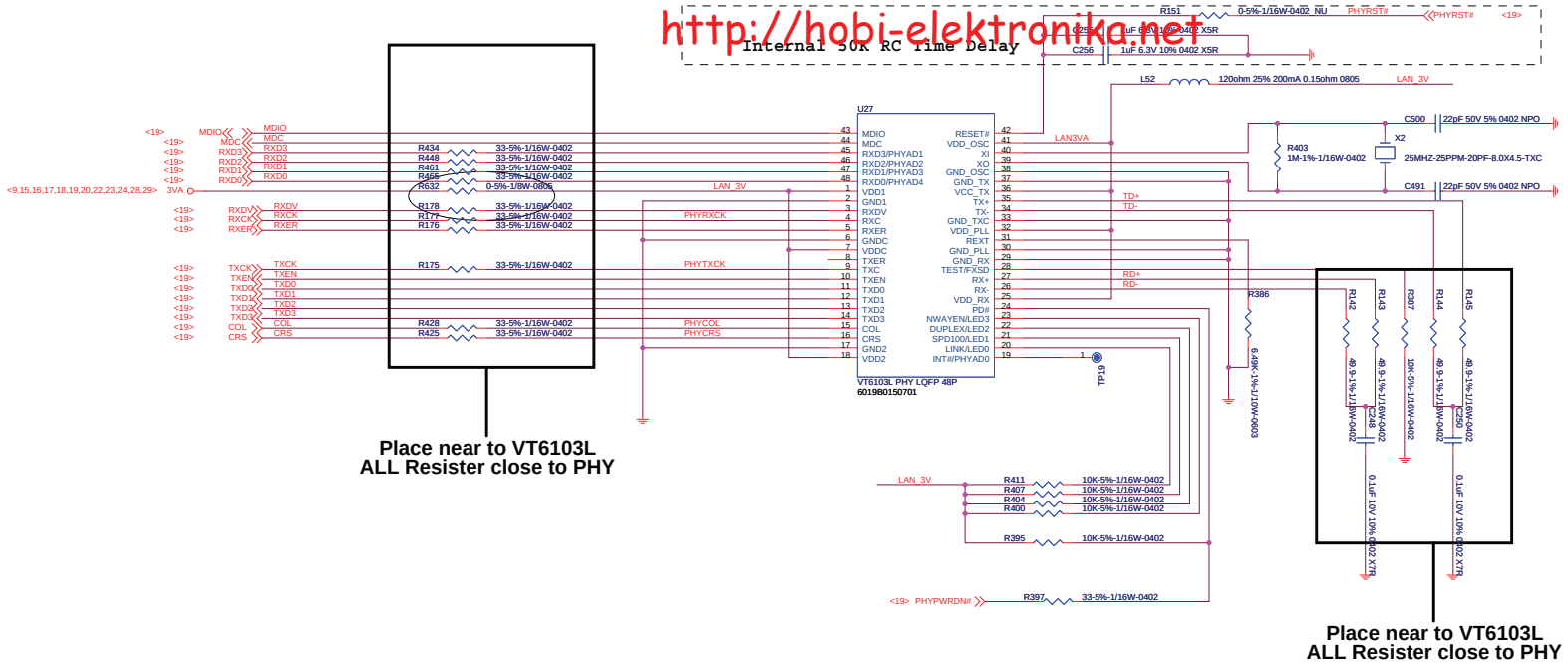
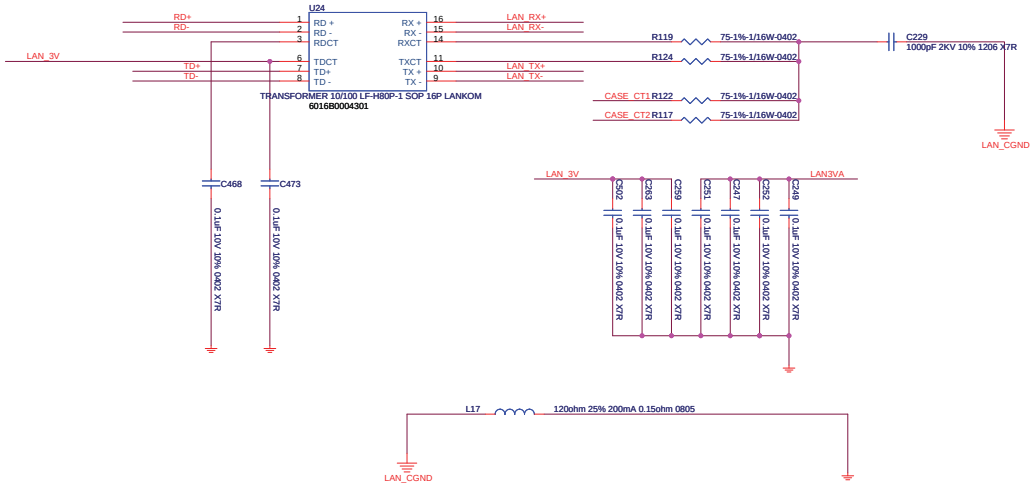
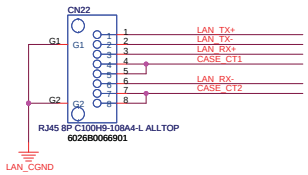




LAN RJ45 JACK



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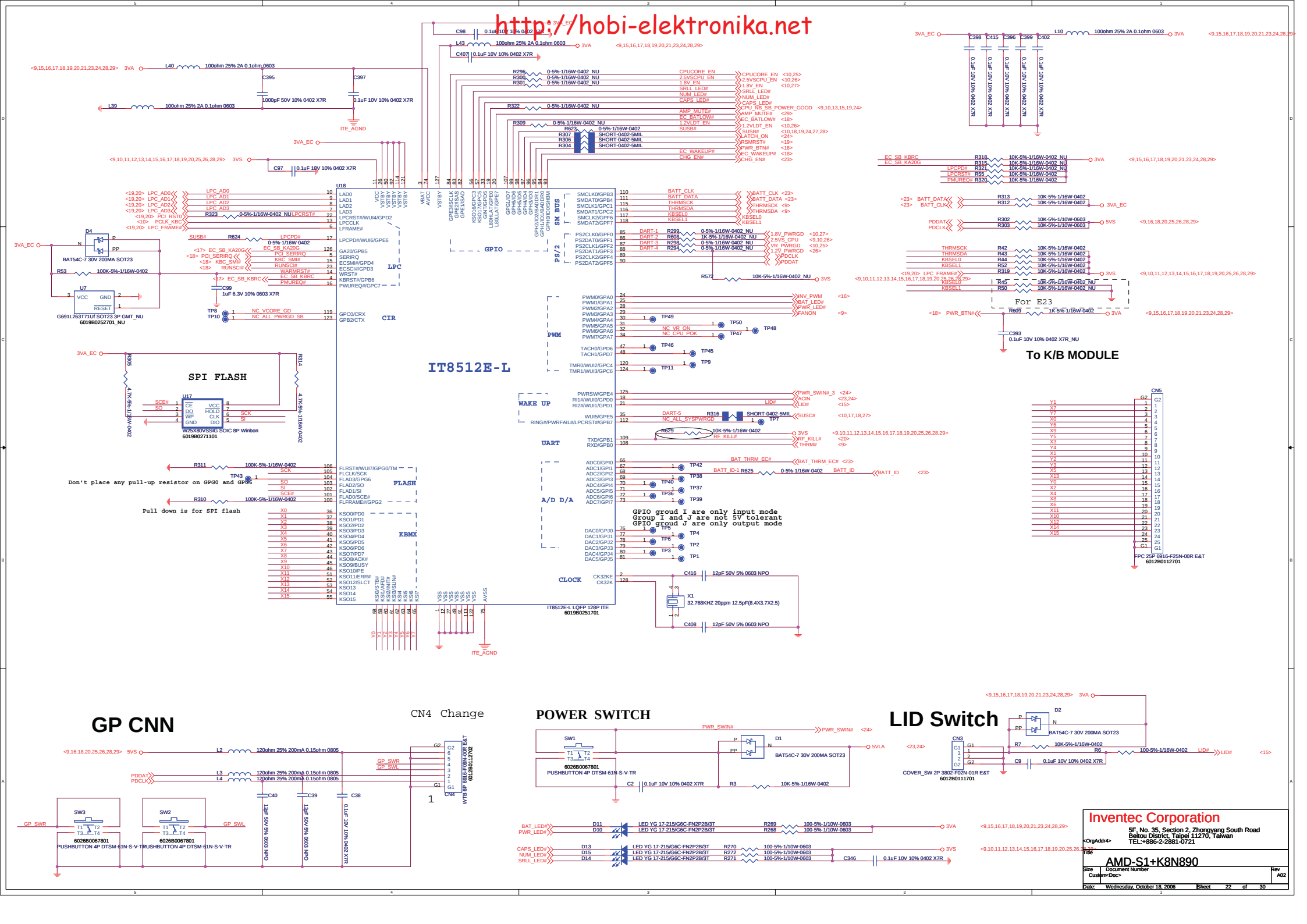
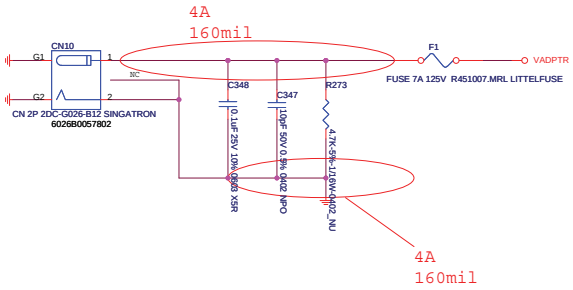
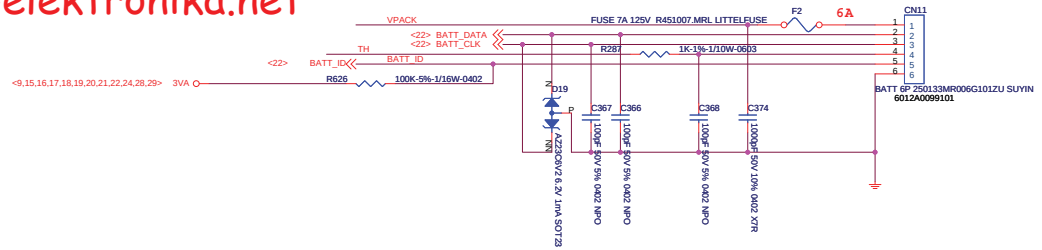
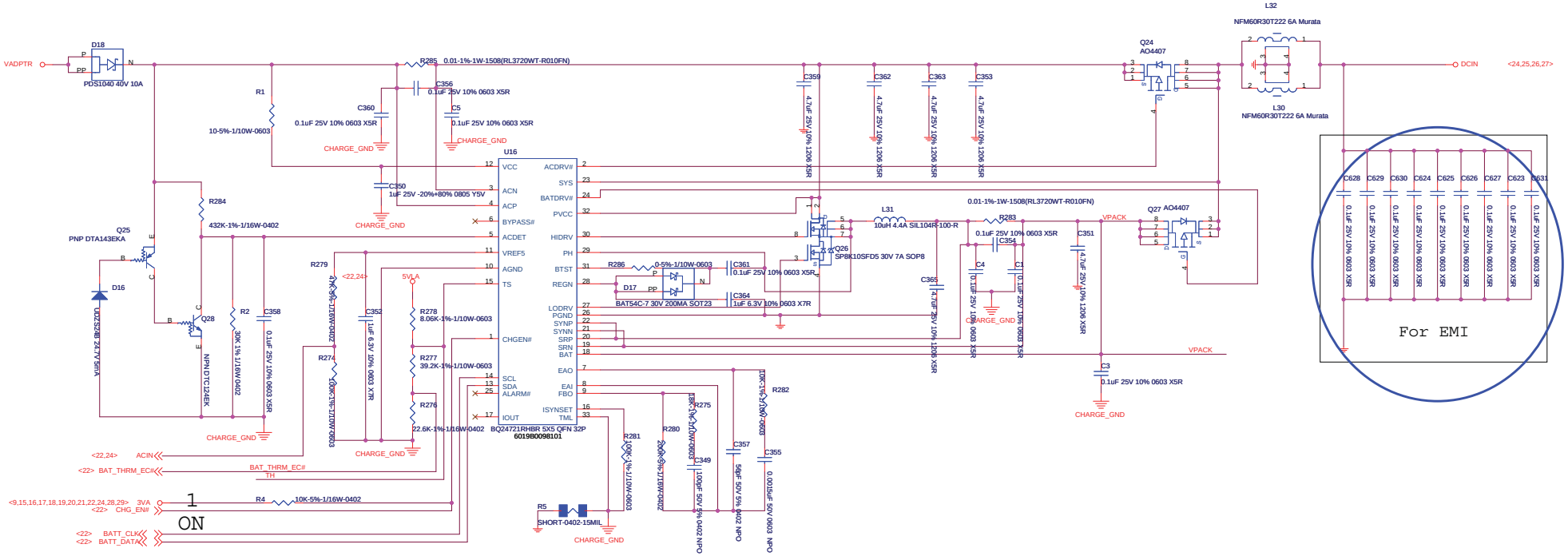


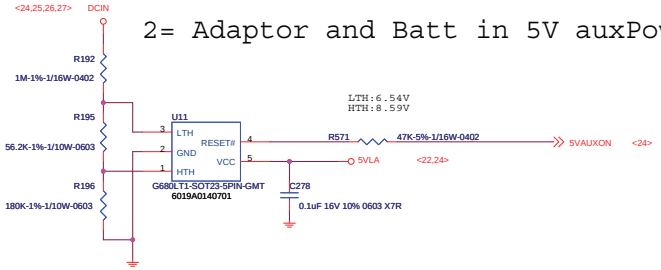




20mil



1= Adaptor and Batt in power



2= Adaptor and Batt in 5V auxPower

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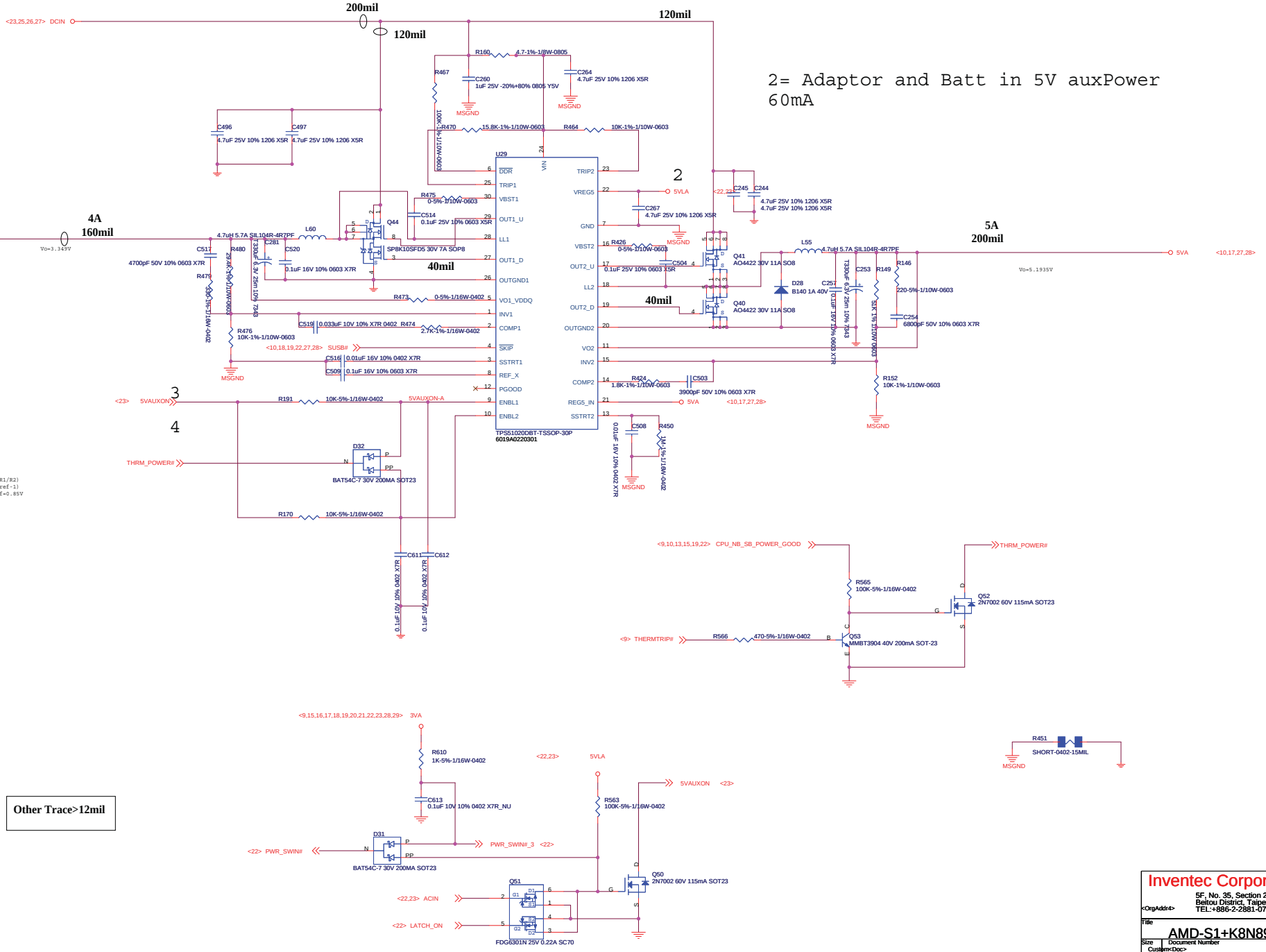
+V5A/+V5LA/+V3A/+V3LA



Other Trace>12mil

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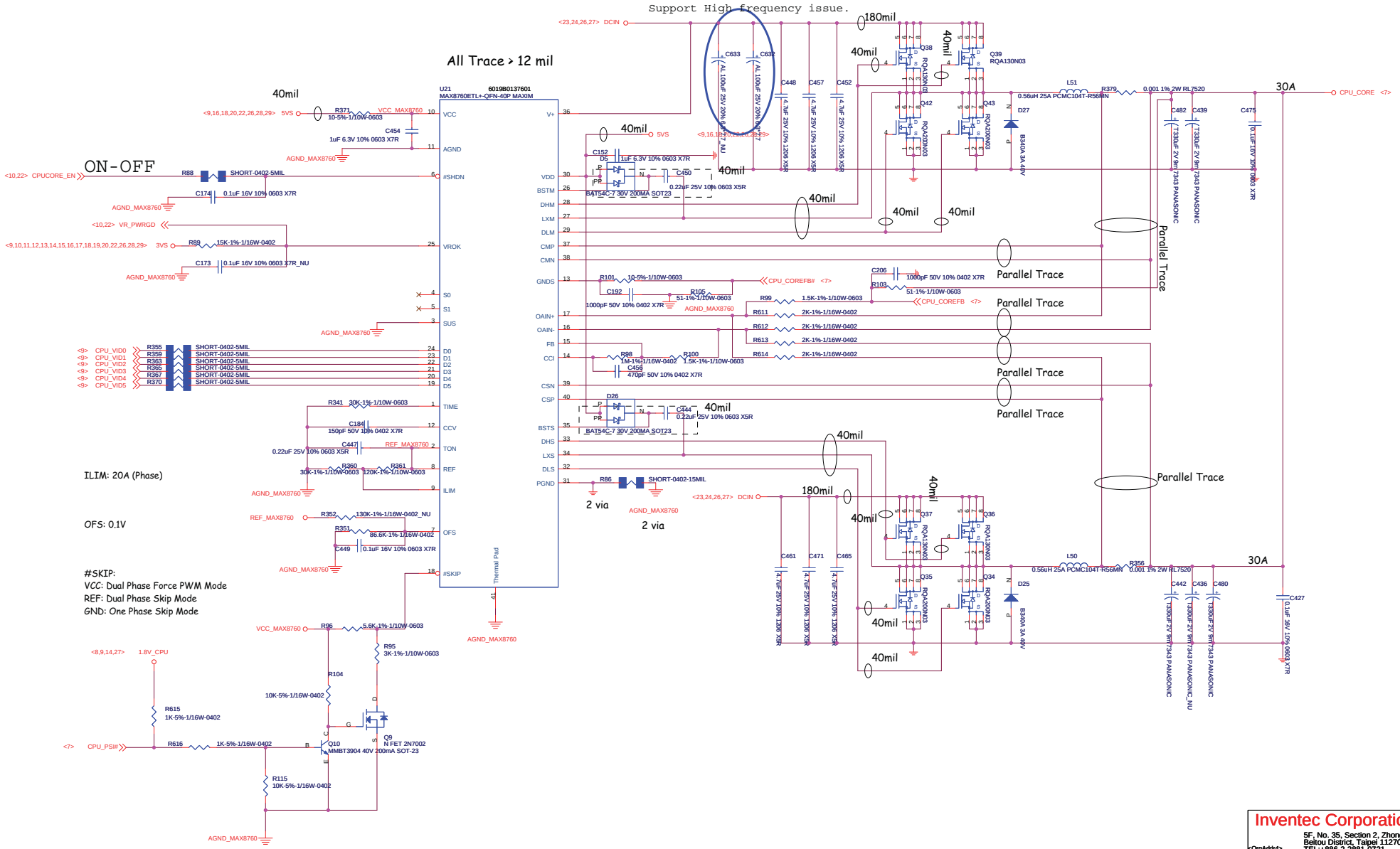
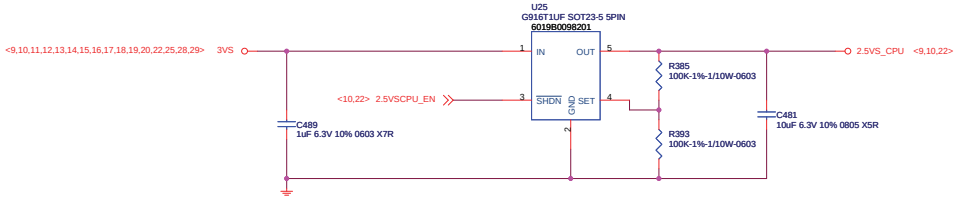
AMD K8 CPU Core Power (MAX8760)



CPU 2.5V

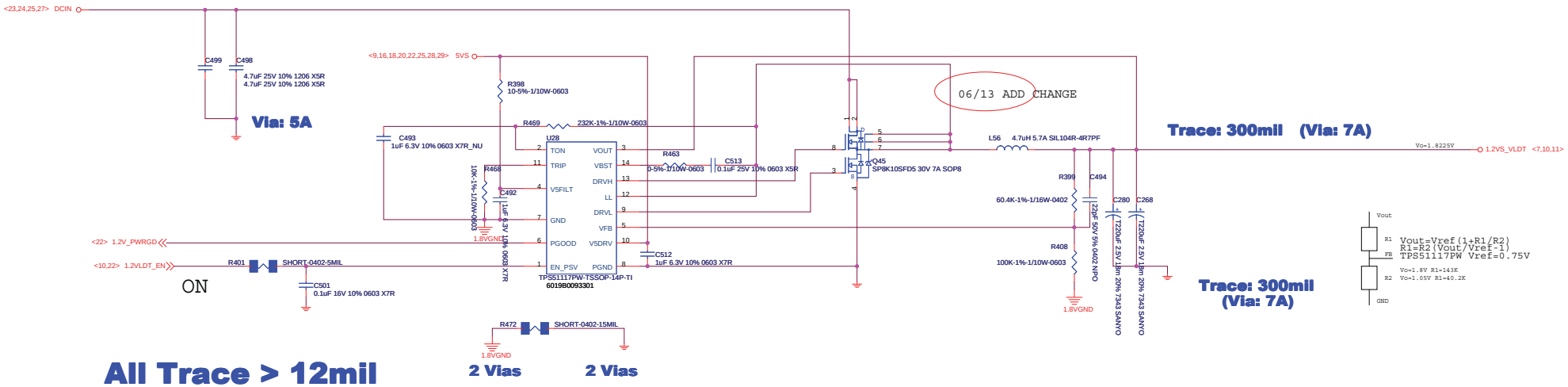
1.8V_PWRGD to 2.5VS_CPU = 2ms



2.5VS_CPU to CPUCORE_EN = 2ms

CPU +1.2VHT

Trace: 200mil (Via: 5A)



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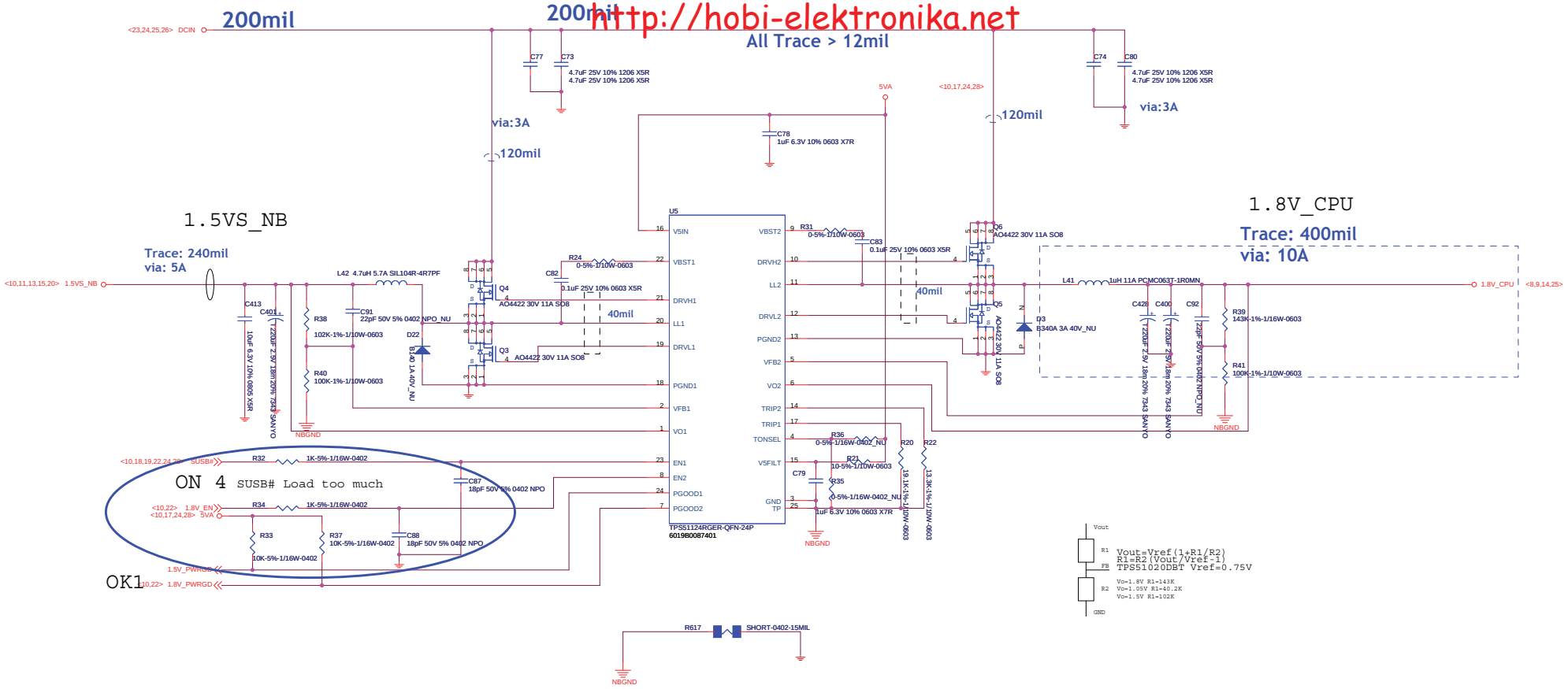
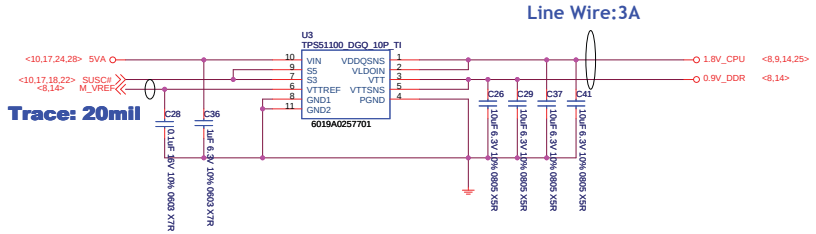


DDRII Terminator Power



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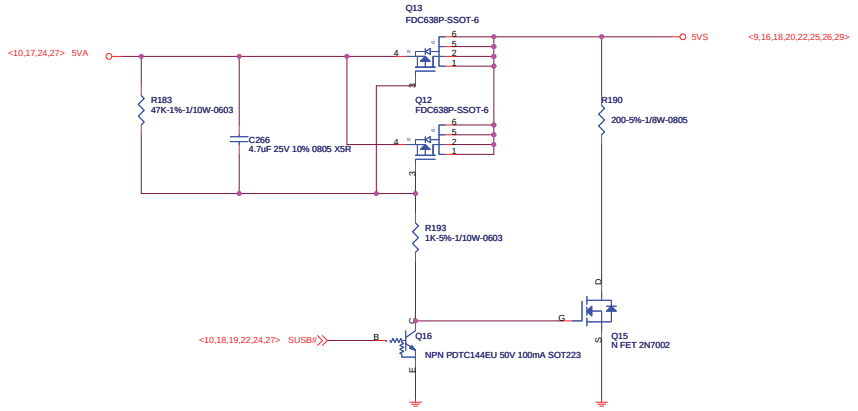
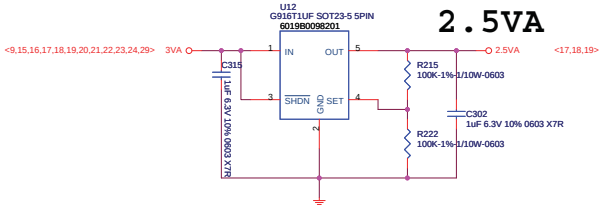
SB POWER 2A (S3 OFF)

5VS

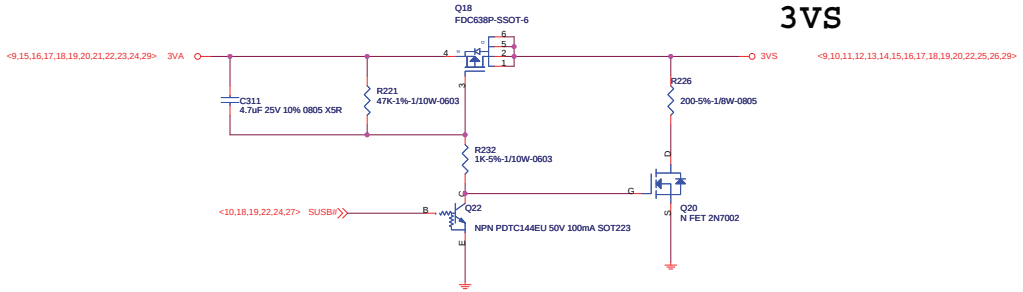


POWER 300mA (S3 ON)

2.5VA

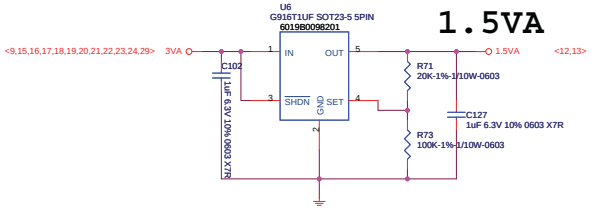


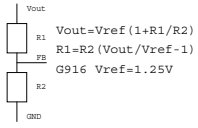
3VS



POWER 300mA (S3 ON)

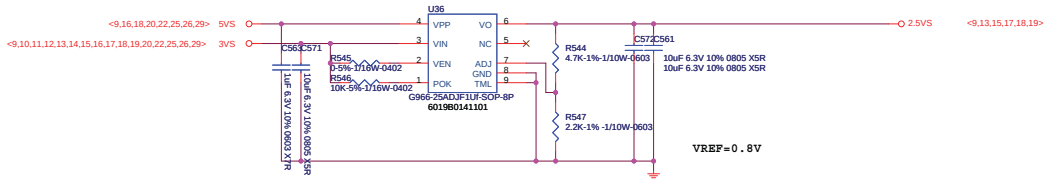
1.5VA





Vout=Vref(1+R1/R2)
R1=R2(Vout/Vref-1)
G916 Vref=1.25V

2.5VS



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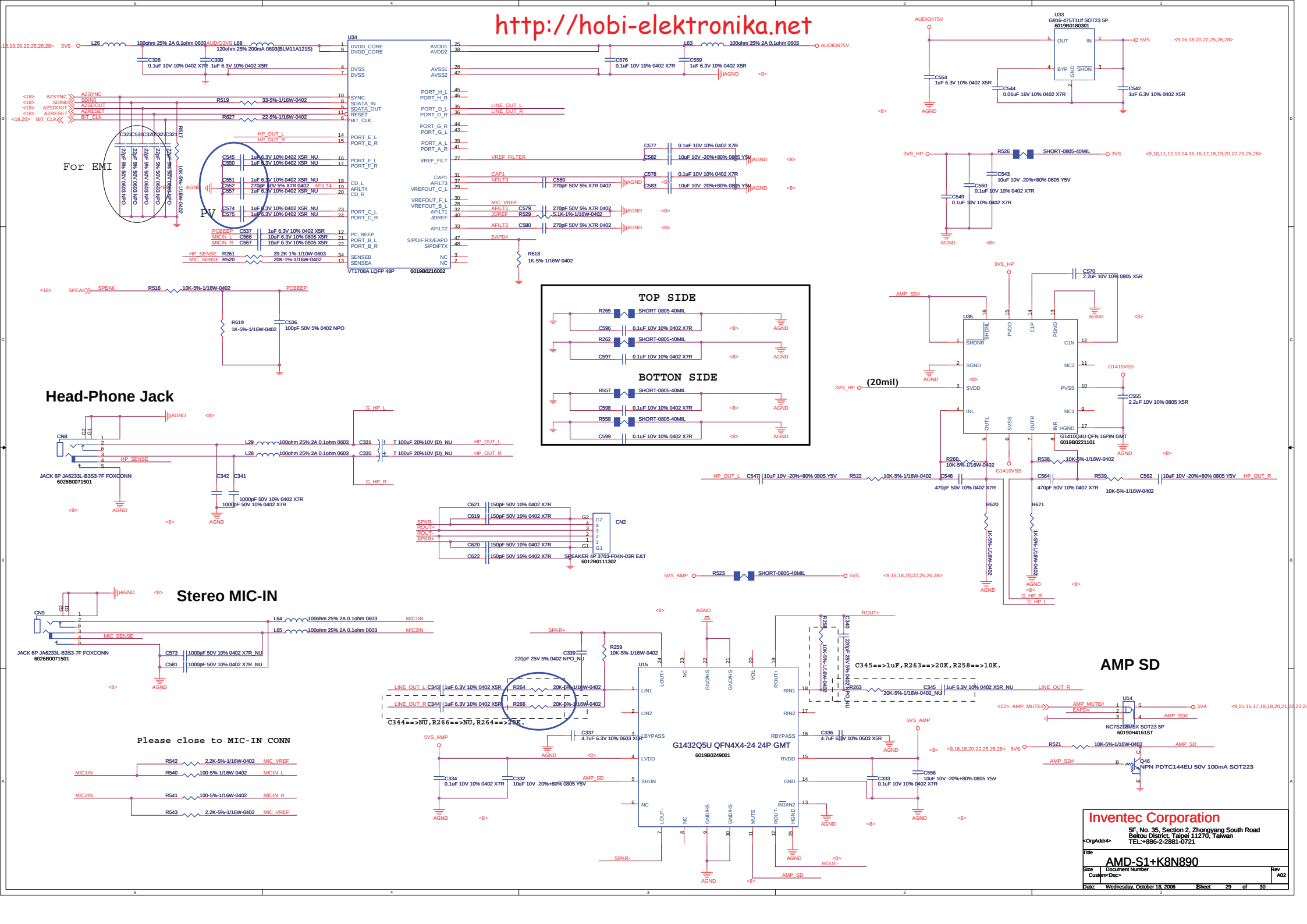

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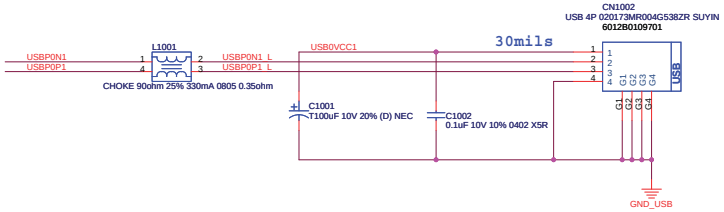

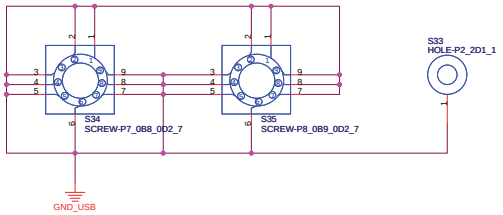

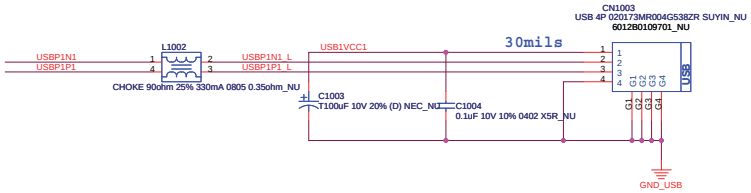

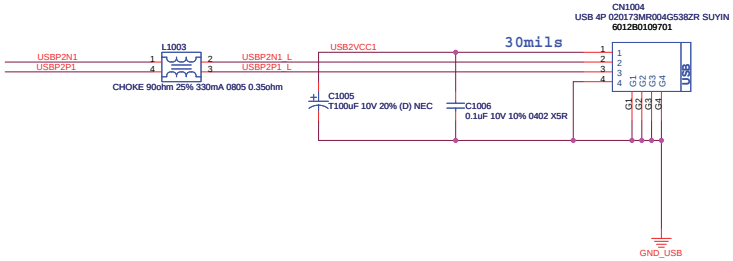

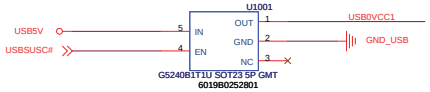

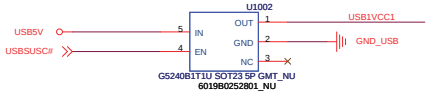

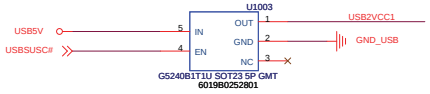

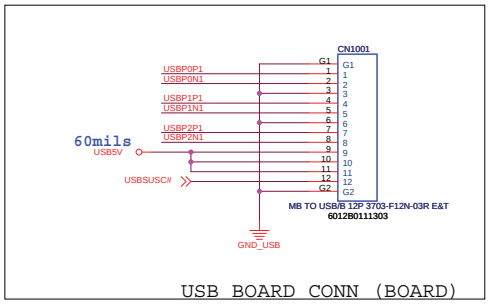

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